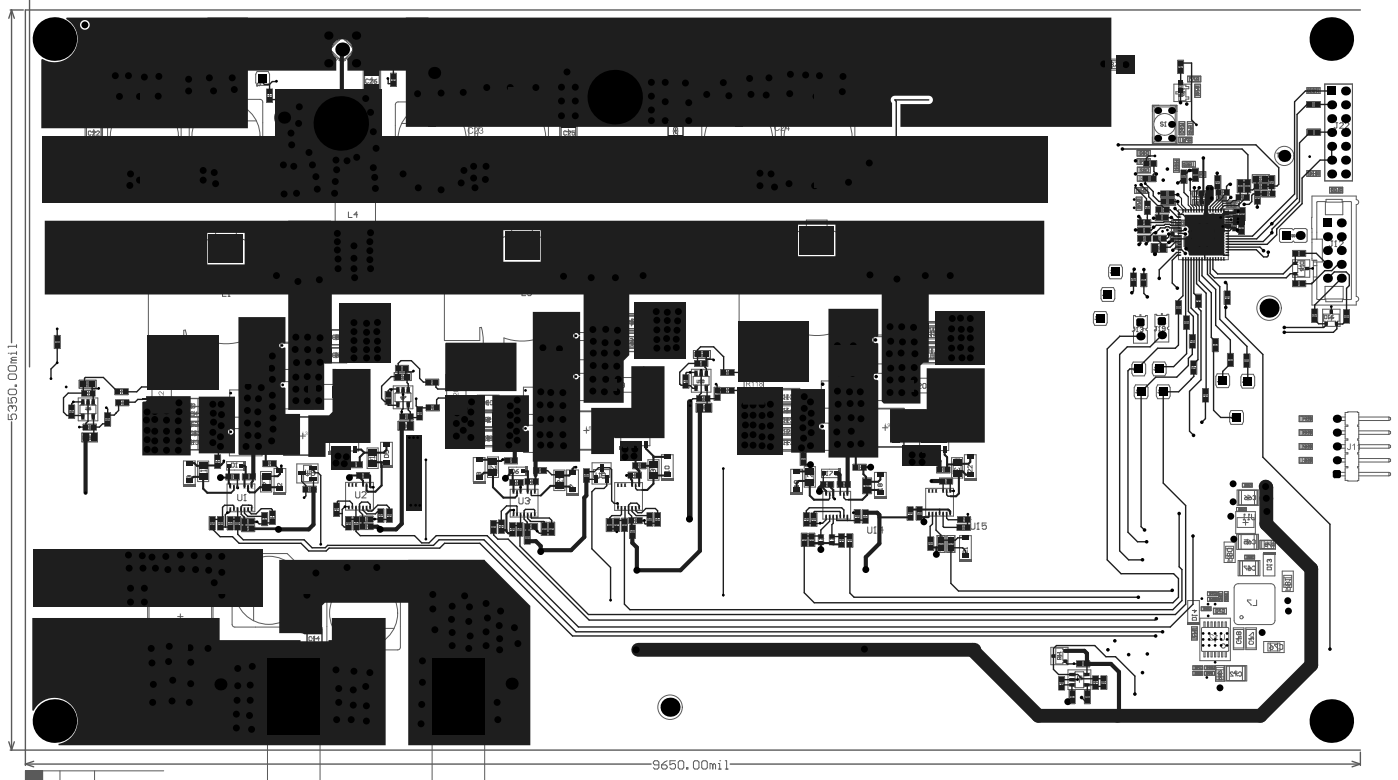
Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

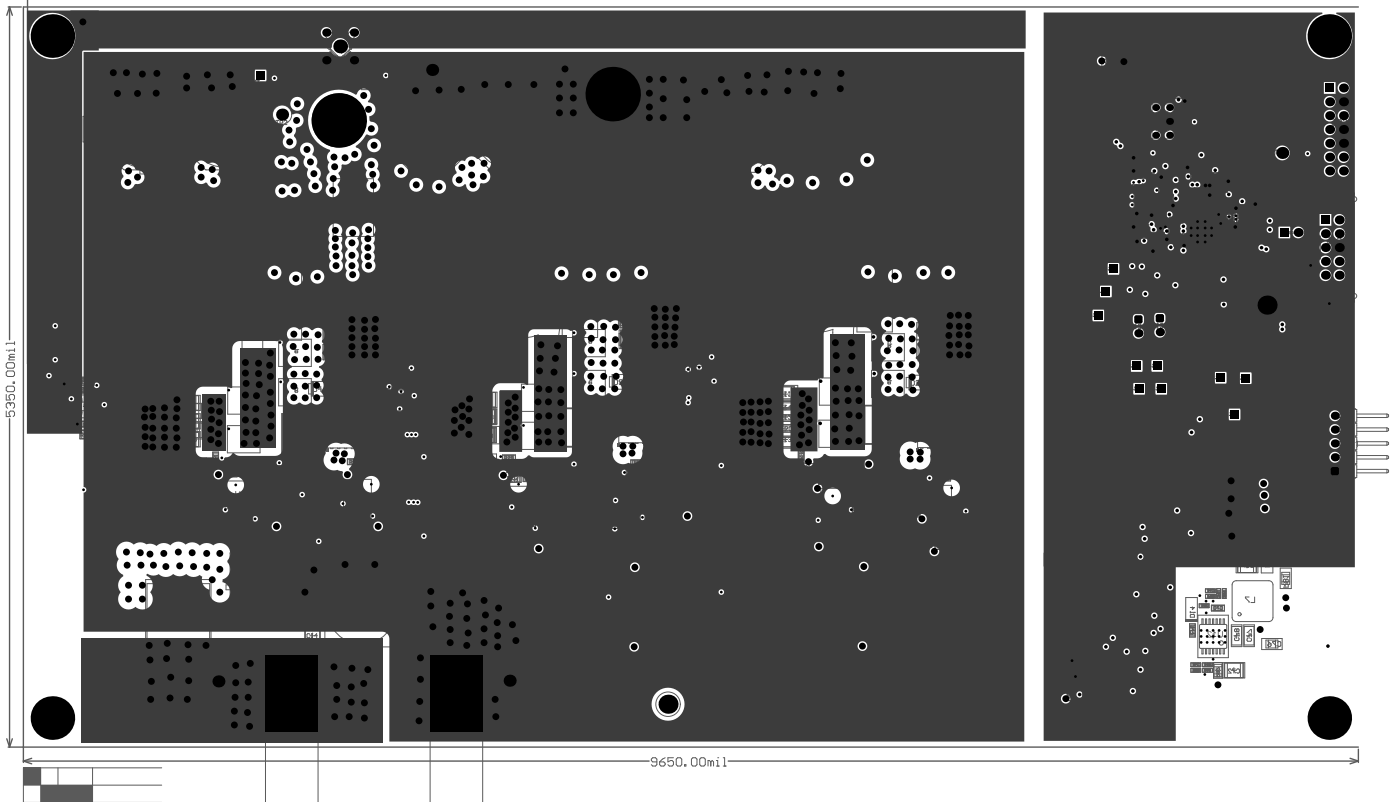
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Assembly Bottom
TID #:
GENERATED: 12/15/2022 11:10:15 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
These assemblies are ESD sensitive, ESD precautions shall be observed.
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

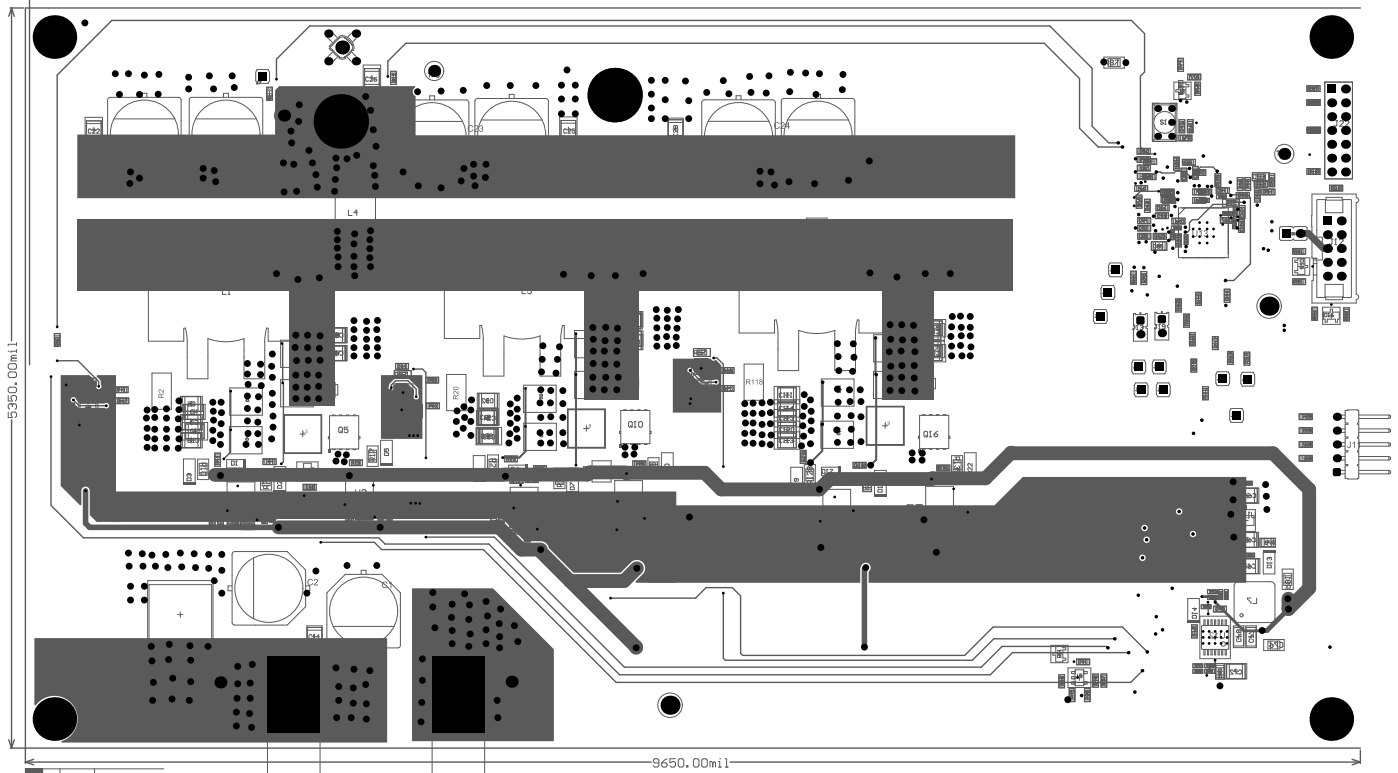
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Signal Layer 1
TID #:
GENERATED: 12/15/2022 11:10:15 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

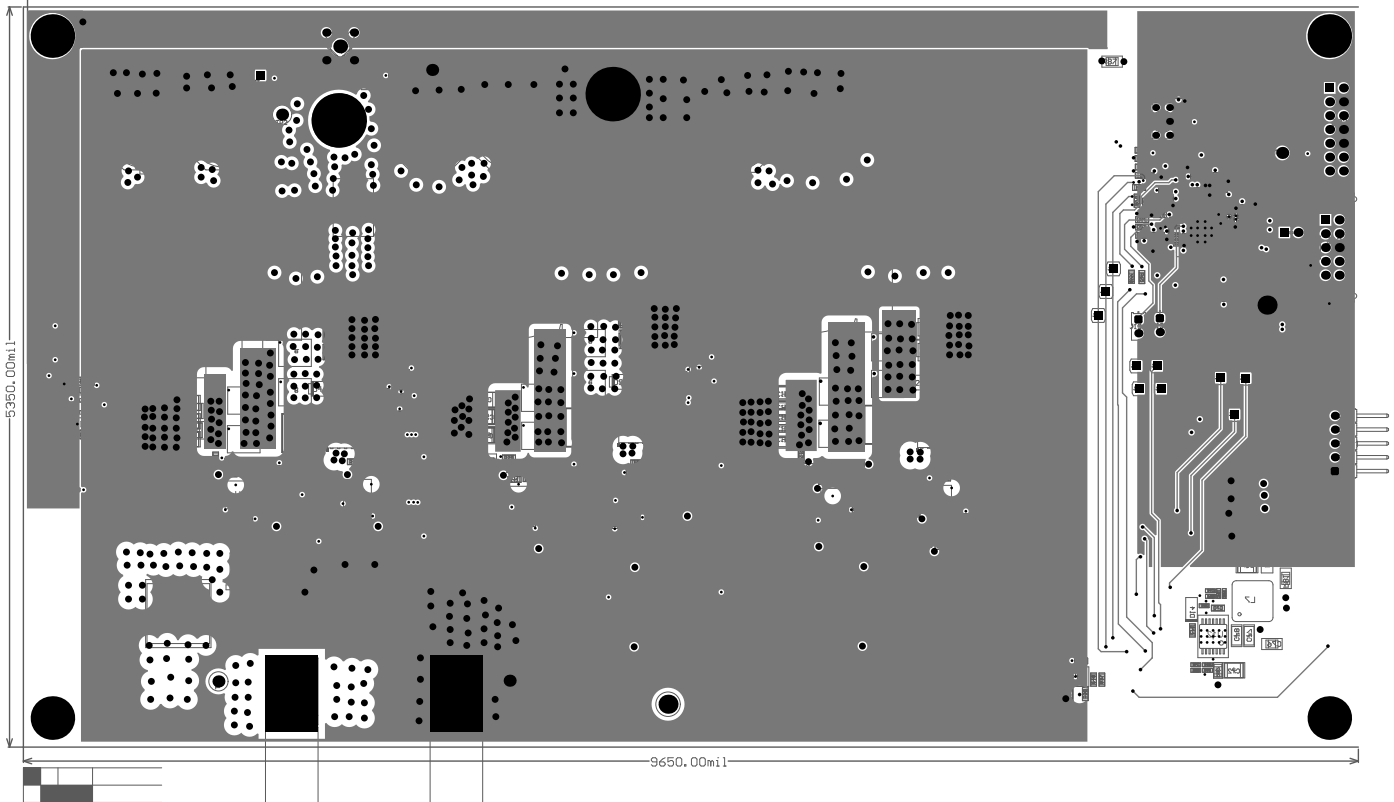
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
BOARD #: PMP20587 REV: C
TID #: PMP20587
GENERATED: 12/15/2022 11:10:15 AM
TEXAS INSTRUMENTS
LAYER NAME = Signal Layer 2
PLOT NAME = Signal Layer 2

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

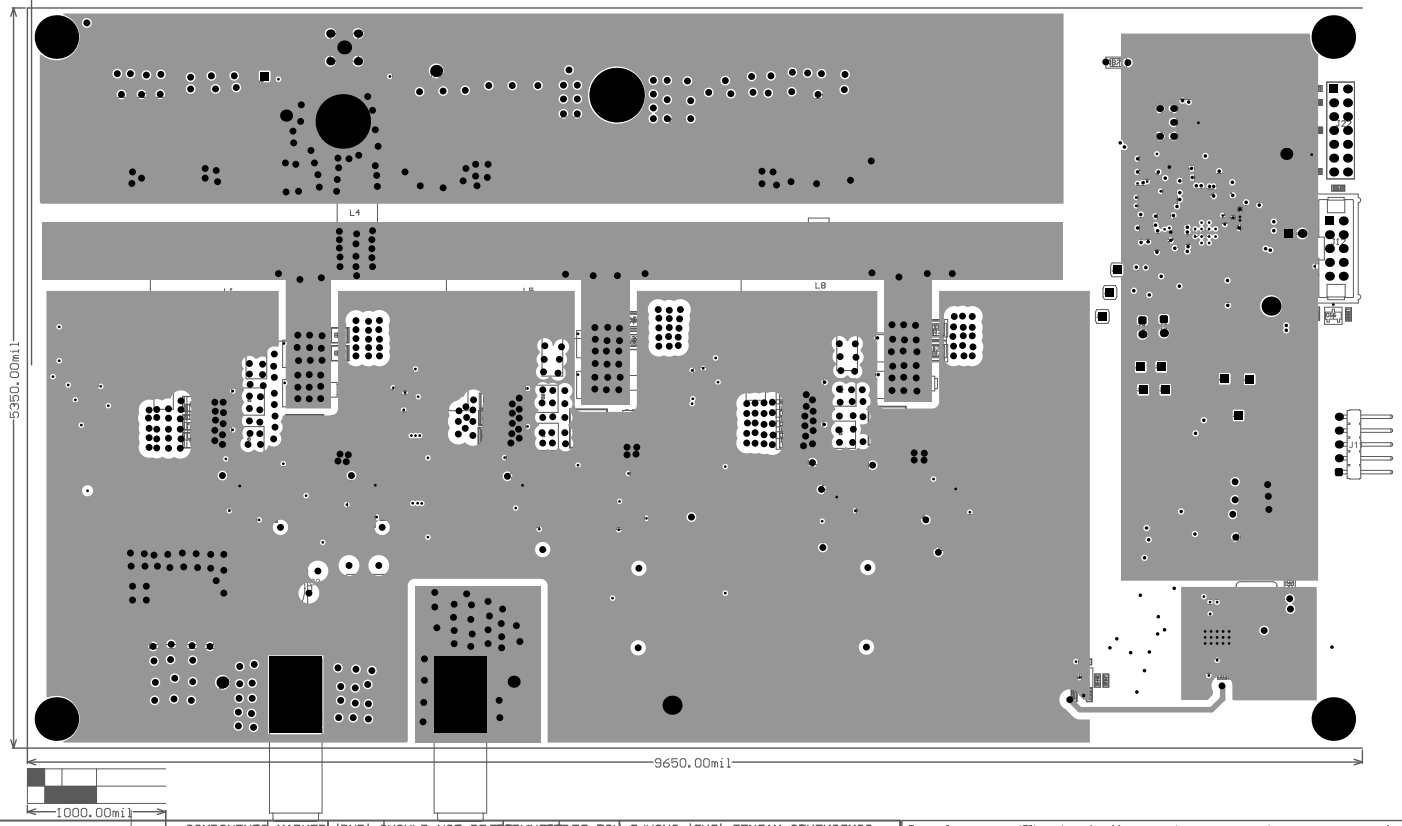
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Signal Layer 3
TID #:
GENERATED: 12/15/2022 11:10:15 AM
PLOT NAME = Signal Layer 3

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

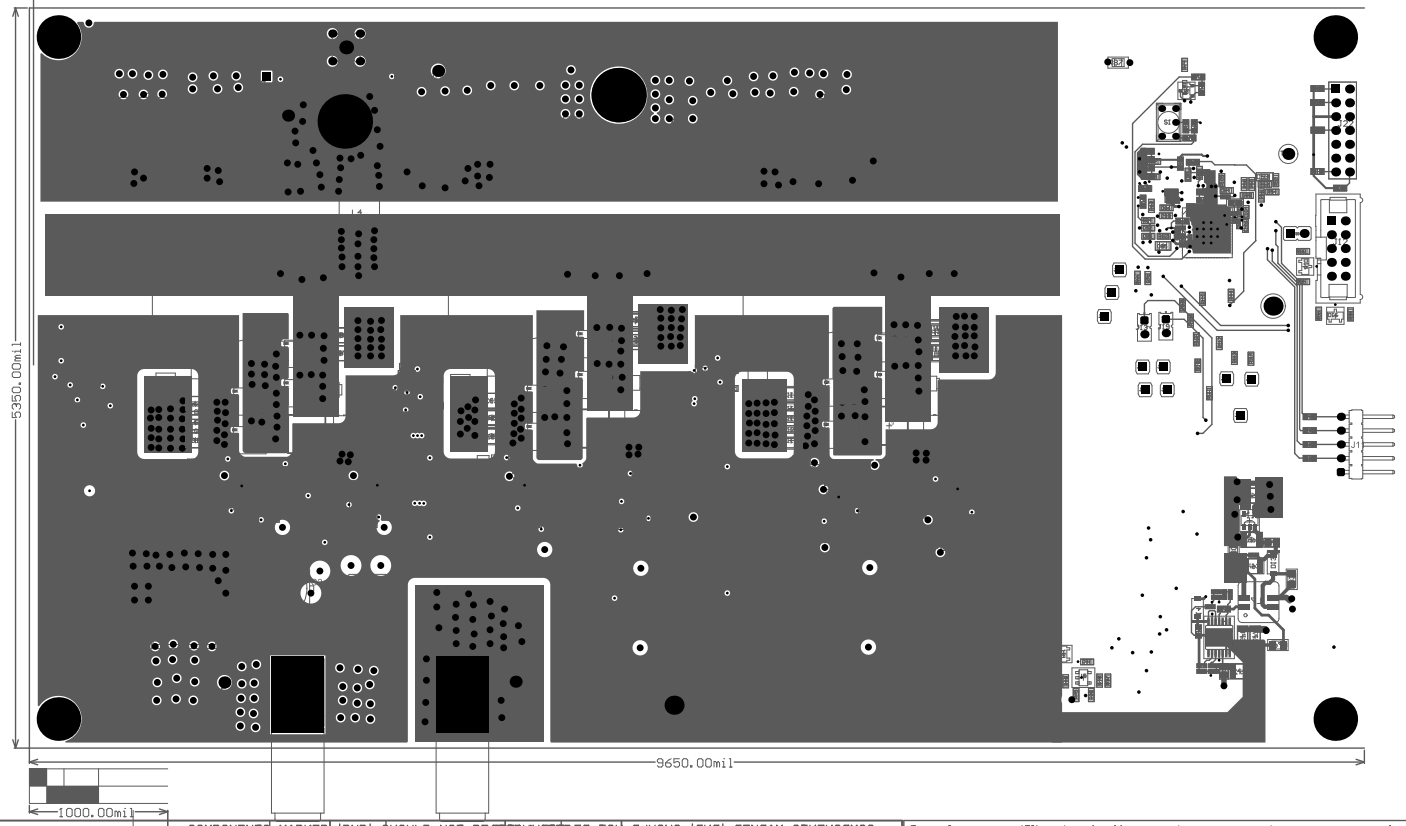
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Signal Layer 4
TID #:
GENERATED: 12/15/2022 11:10:15 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

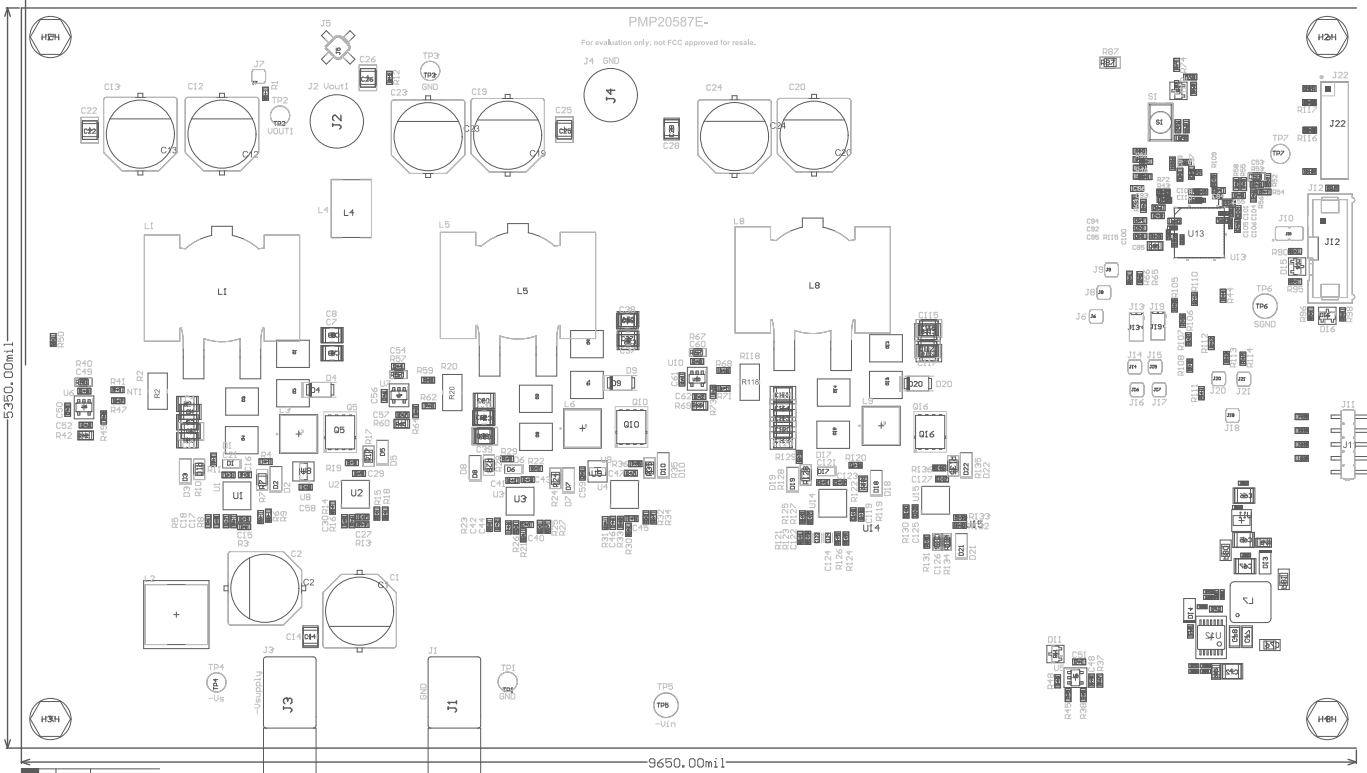
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Bottom
TID #:
GENERATED: 12/15/2022 11:10:15 AM
PLOT NAME = Bottom Layer

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH: 8 MIL MIN. CLEARANCE: 0.2 mm MIN. VIA PAD SIZE: 24 MIL MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/- BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-	
DRILLING: REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH: SILKSCREEN: [X] TOP [X] BOTTOM SILKSCREEN COLOR: [X] WHITE [ ] OTHER SOLDER RESIST COLOR: [X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF: [X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3 [X] RoHS [ ] OTHER PER ORDER ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: [ ] YES BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: [No Variations]

LAYER NAME = Assembly Bottom

PLOT NAME = Silkscreen Overlay

BOARD #: PMP20587 :# DWG

TID #: PMP20587 :# DIT

GENERATED :: 12/15/2022 11:10:16 AM

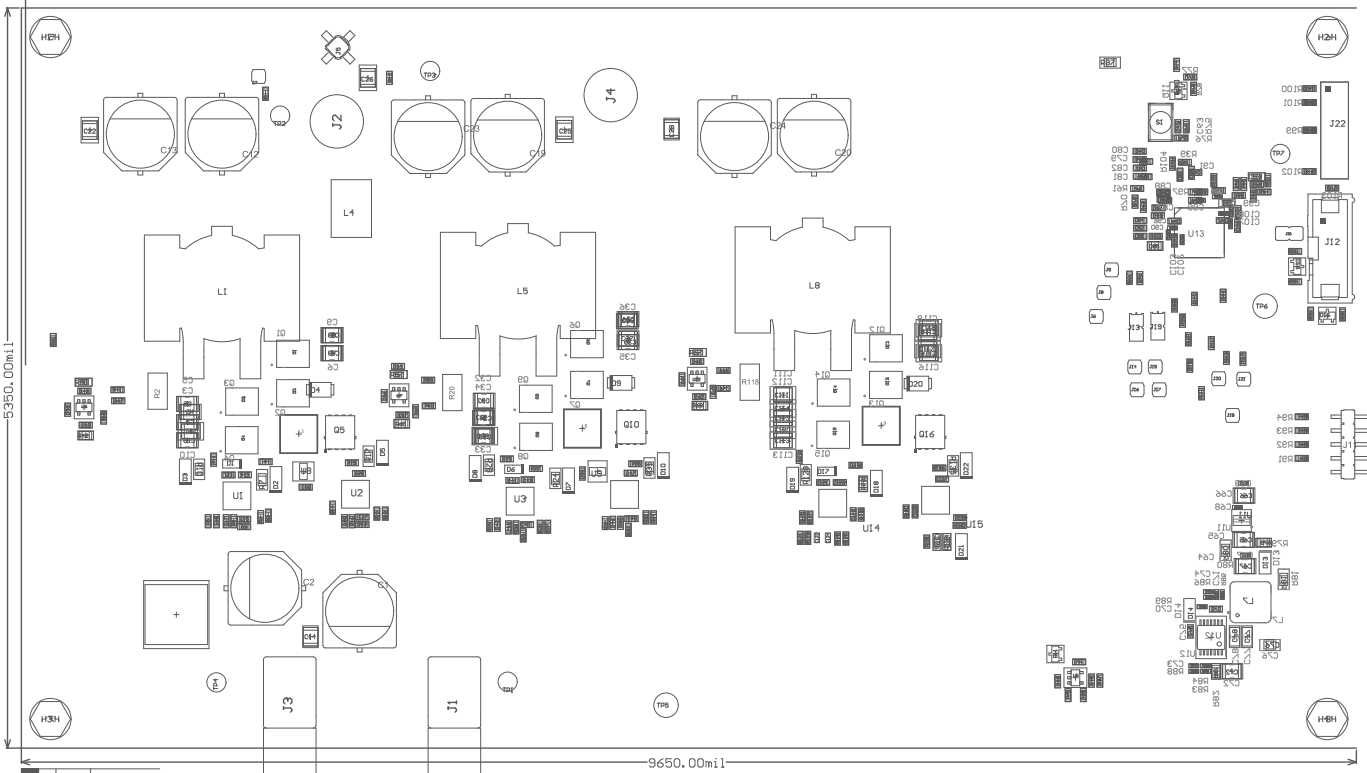
TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost	
DESIGNED FOR: Public Release	
FILE NAME: PMP20587_REVE.PcbDoc	
ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Bottom
TID #:
PLOT NAME = Bottom Silkscreen Overlay
GENERATED:

ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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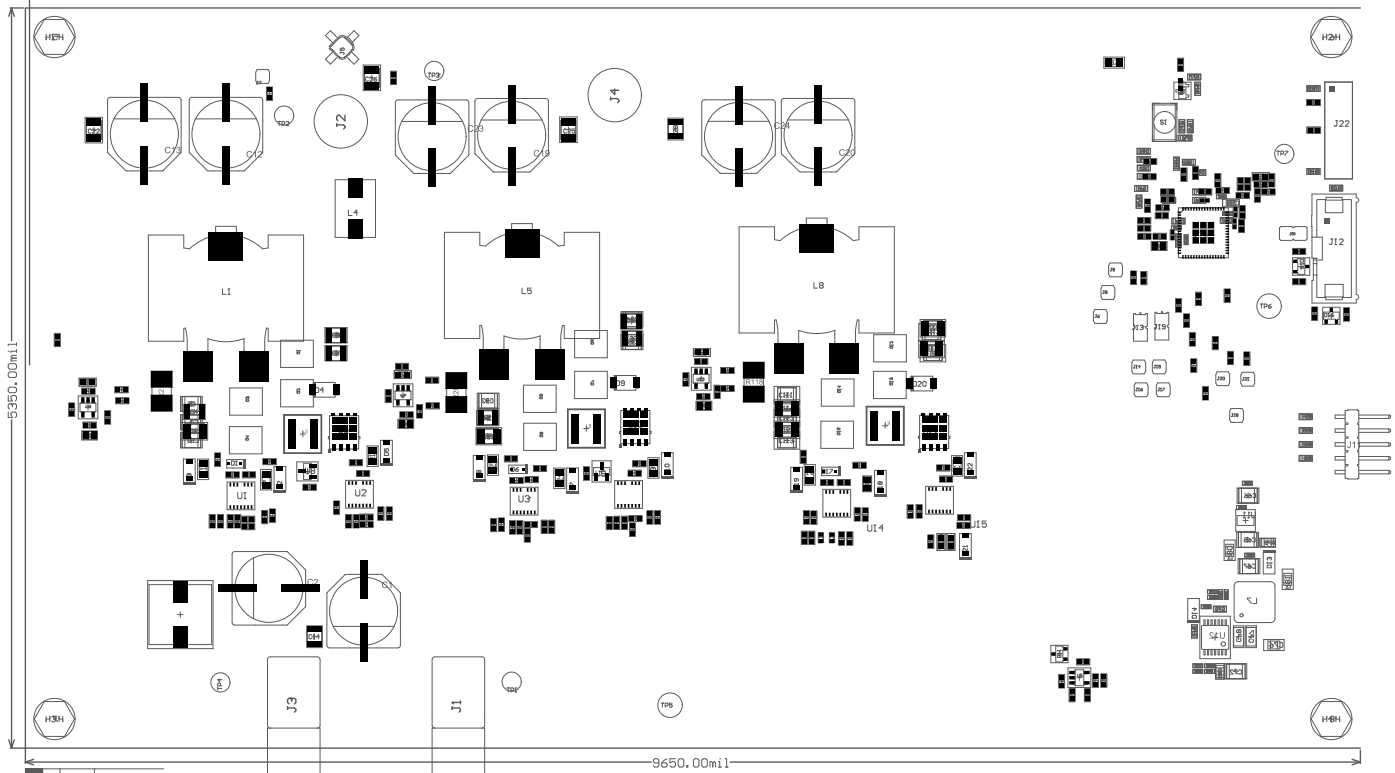
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc
ENGINEER:	Sean Xu & Sean Yu
LAYOUT BY:	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

LAYER NAME = Mask Paste Bottom
TID #:
GENERATED: 12/15/2022 11:10:16 AM
Mask Paste
TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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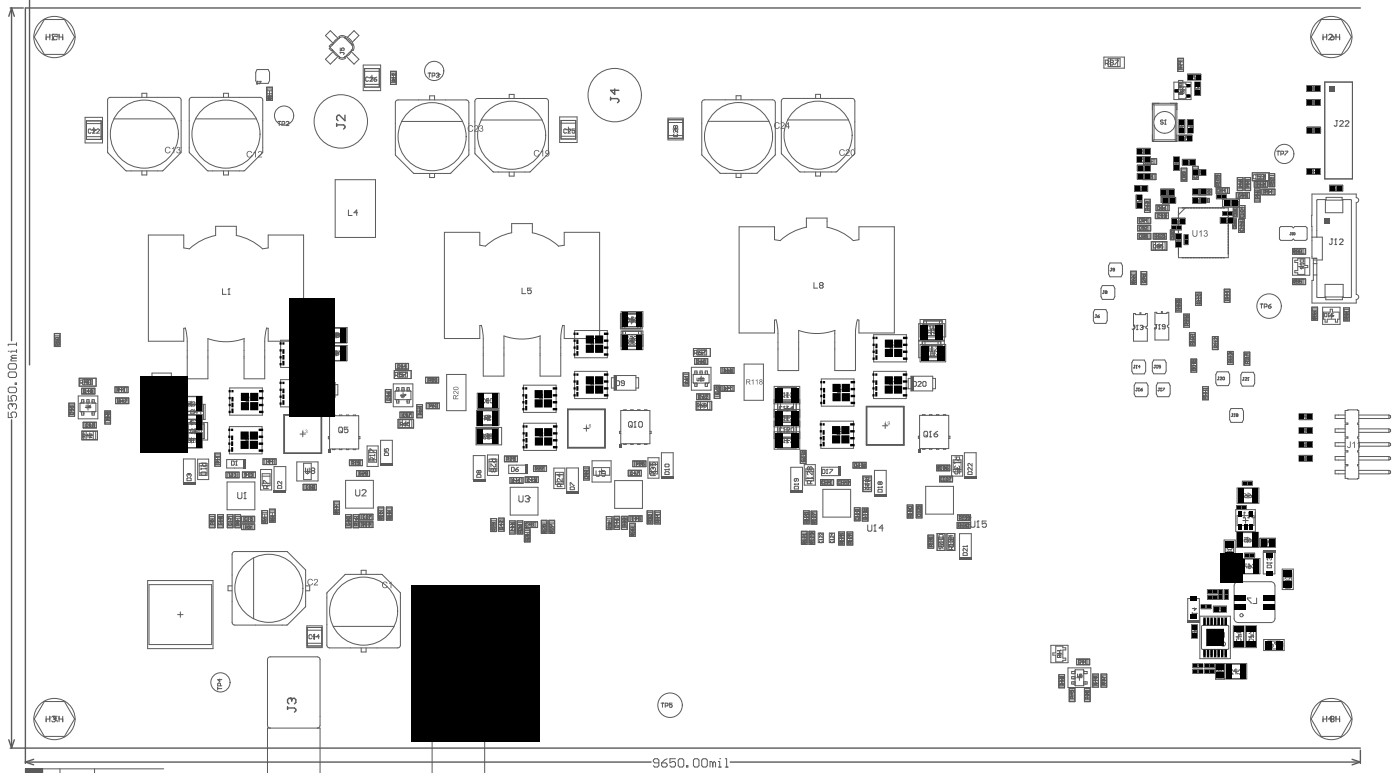
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

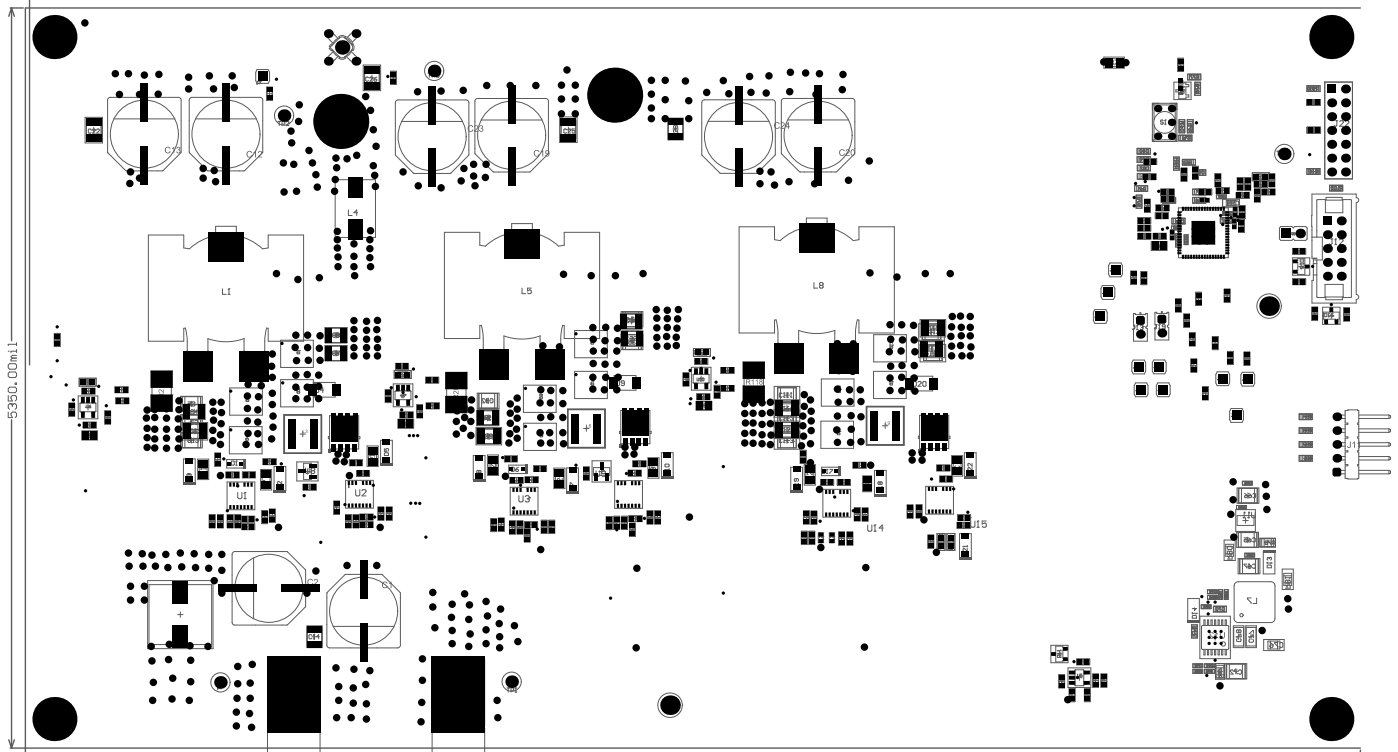
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Bottom Paste Mask Print
TID #:
GENERATED: 12/15/2022 11:10:16 AM

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

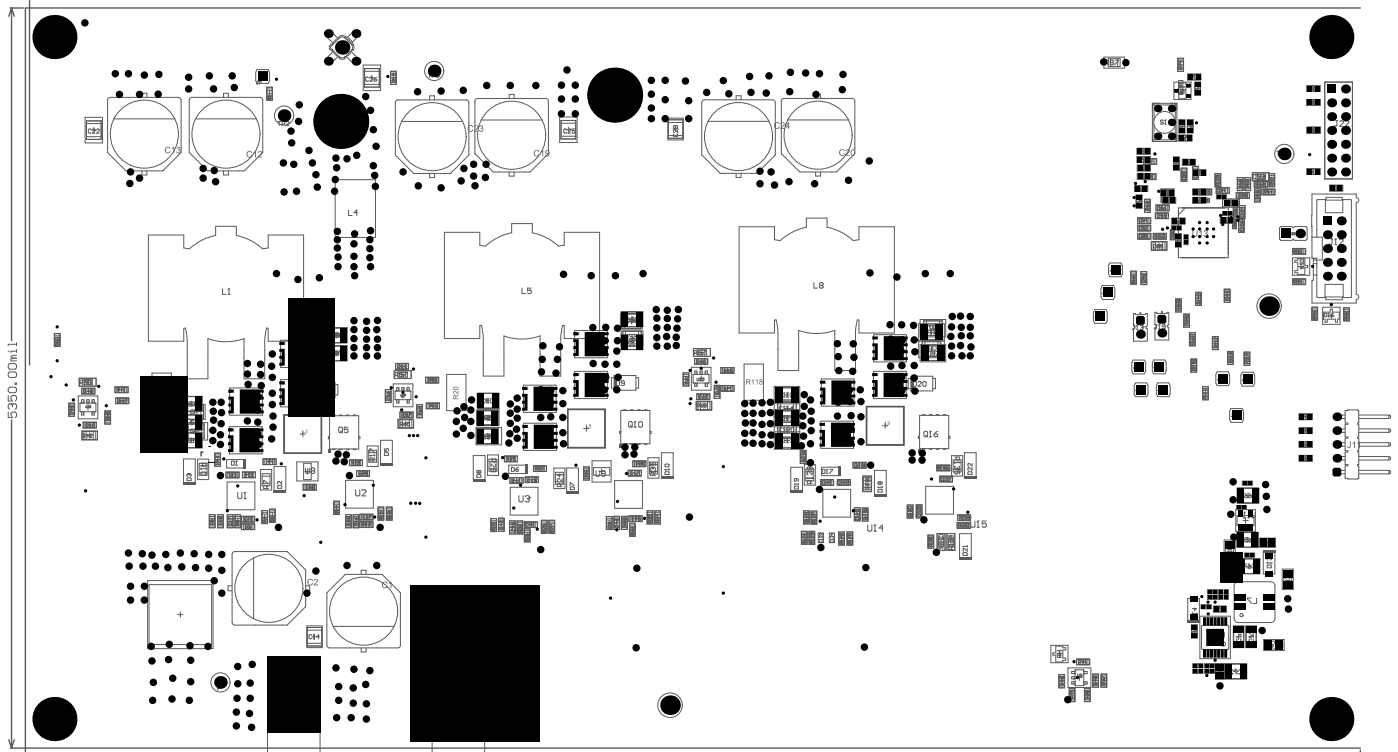
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Top Solder
PLOT NAME = Top Solder Mask Panel
BOARD #: PMP20587 REV: E
TID #: PMP20587 DIT
GENERATED: 12/15/2022 11:10:16 AM
TEXAS INSTRUMENTS

ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS:	[X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE:	[X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST:	[X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
DRILLING:	
REFERENCE:	[X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS:	[X] 20-30 um [ ] OTHER
BOARD FINISH:	
SILKSCREEN:	[X] TOP [X] BOTTOM
SILKSCREEN COLOR:	[X] WHITE [ ] OTHER
SOLDER RESIST COLOR:	[X] GREEN [ ] OTHER [X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH:	[X] IMMERSION GOLD (ENIG) [ ] ENEPIG [ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL:	[ ] CUT AND TRIM PER M1 BOARD OUTLINE [ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION:	MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF: [X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3 [X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION:	[ ] YES
BARE BOARD ELEC. TEST:	[ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: [No Variations]			
LAYER NAME = Bottom Solder Mask Panel	TID #:		
PLOT NAME = Bottom Solder Mask Panel	GENERATED: 12/15/2022 11:10:16 AM	TEXAS INSTRUMENTS	

ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
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	Dielectric 2		10.00mil	4.2				
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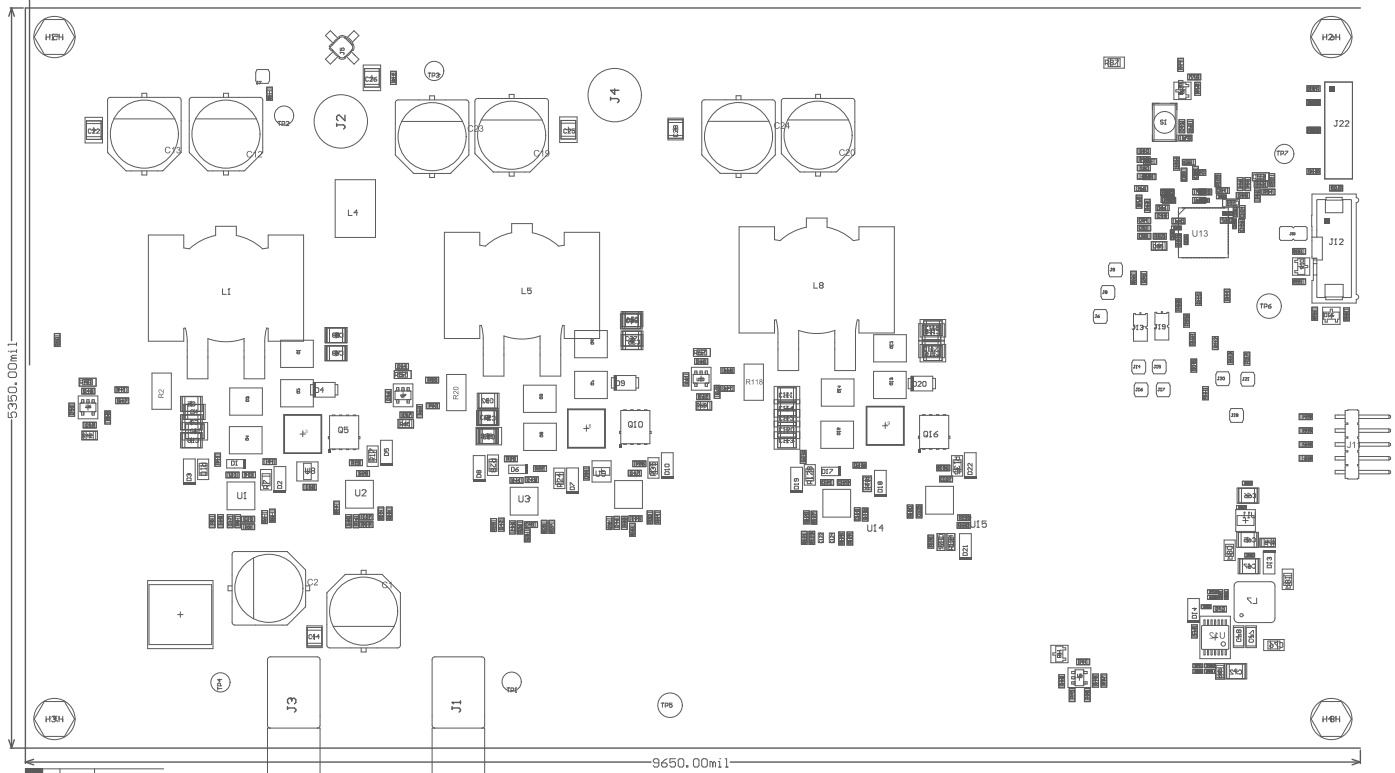
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

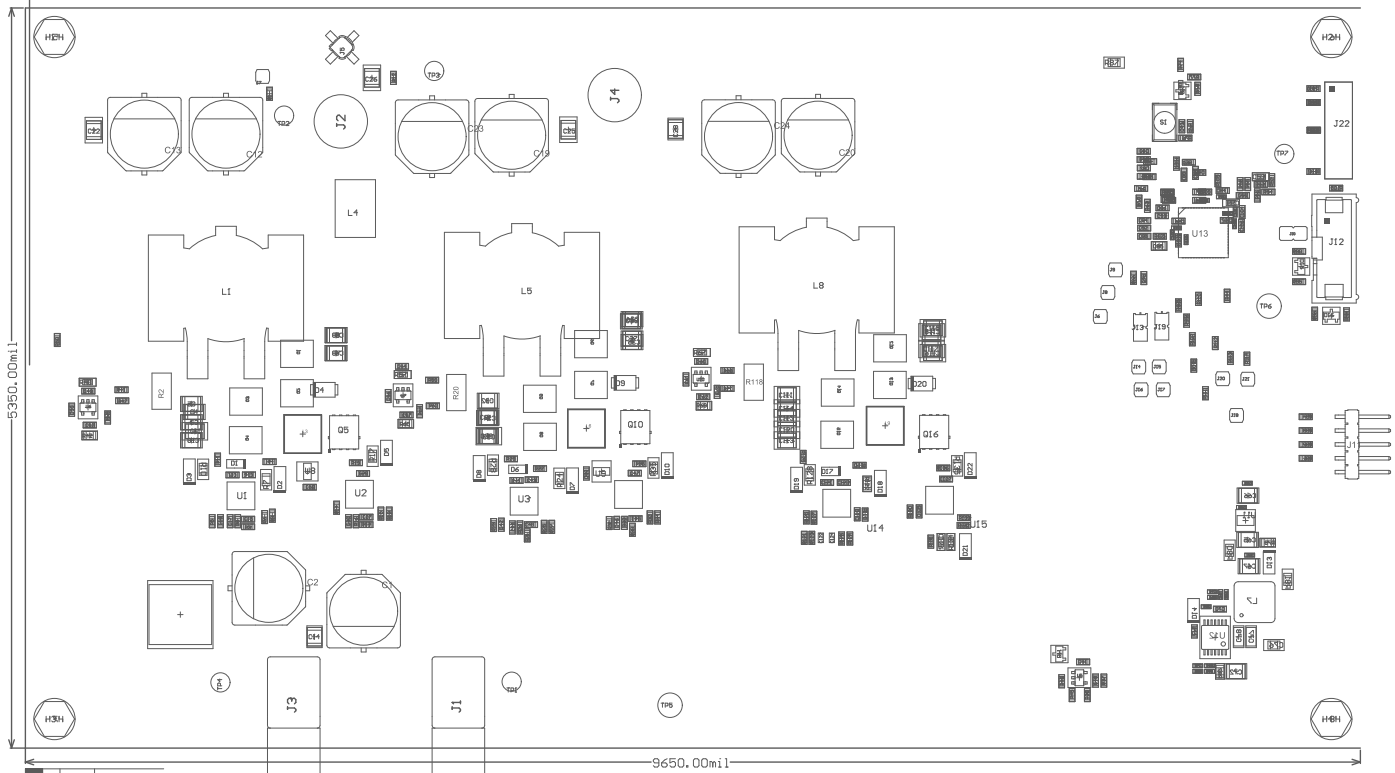
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Board Outline
TID #:
GENERATED: 12/15/2022 11:10:16 AM
TEXAS INSTRUMENTS

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: [No Variations]

LAYER NAME = M1 Assembly Bottom | TID #: [illegible] | :# DIT

PLOT NAME = M2 Board Dimensions | GENERATED :: 12/15/2022 11:10:17 AM | by TEXAS INSTRUMENTS

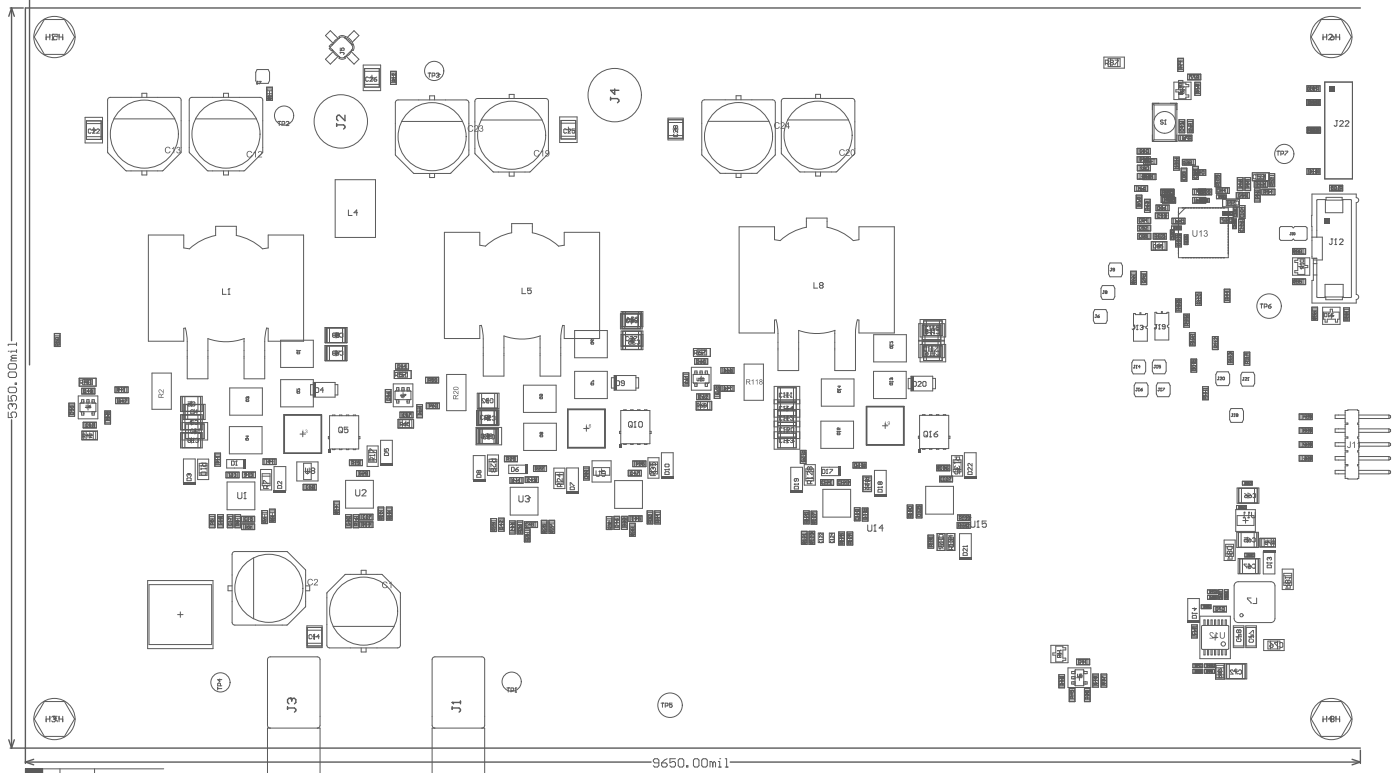
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc
ENGINEER:	Sean Xu & Sean Yu
LAYOUT BY:	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

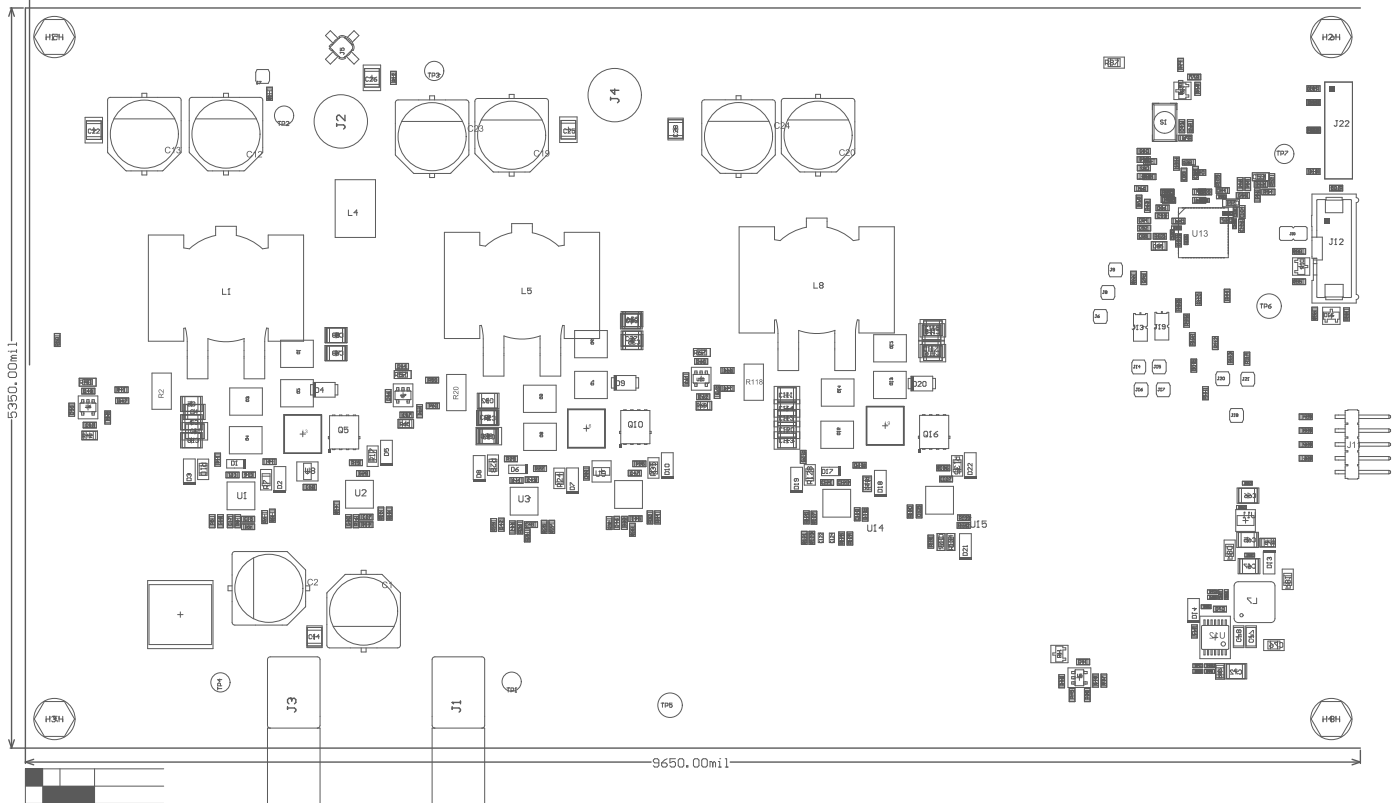
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Top
TID #:
GENERATED: 12/15/2022 11:10:17 AM
PLOT NAME = Top
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

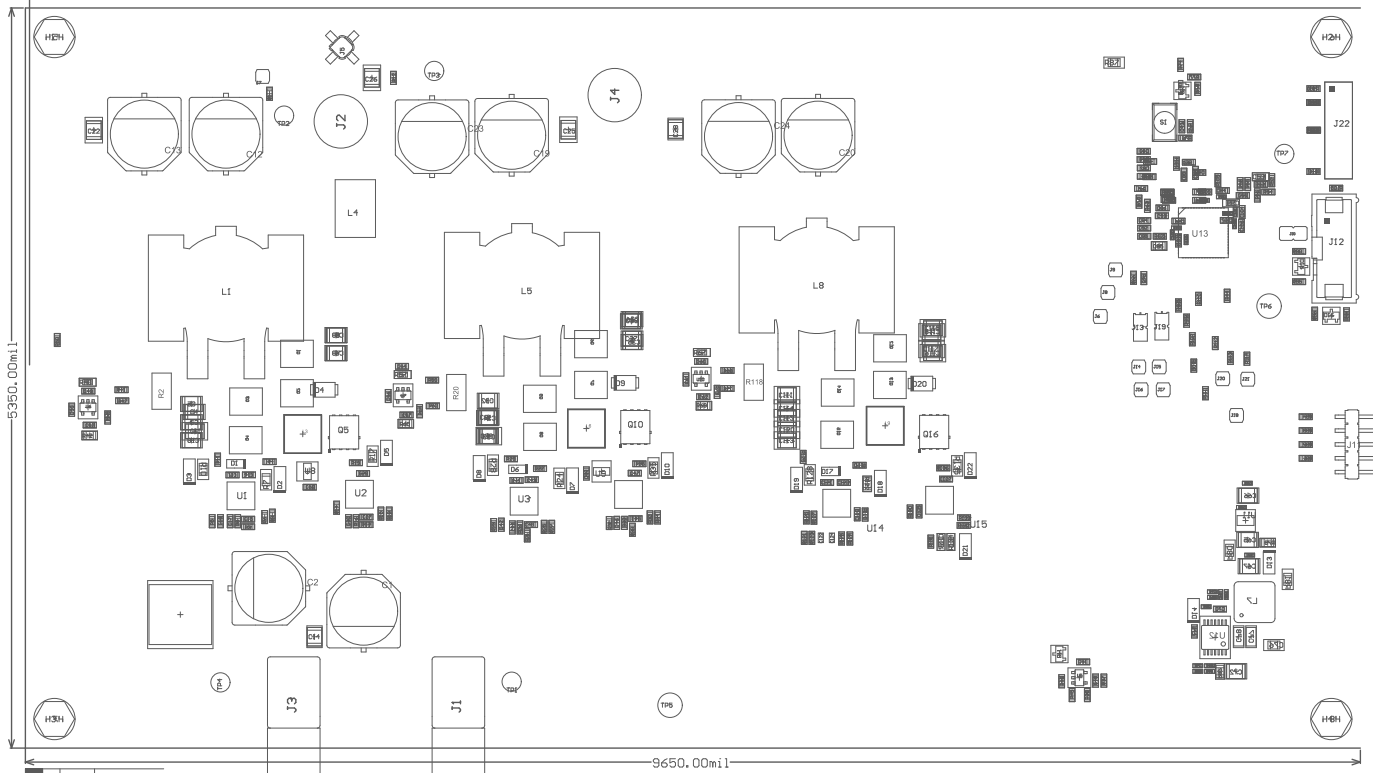
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Bottom
TID #:
PLOT NAME = BOTTOM
PLOT STEP = 1
GENERATED: 12/15/2022 11:10:17 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

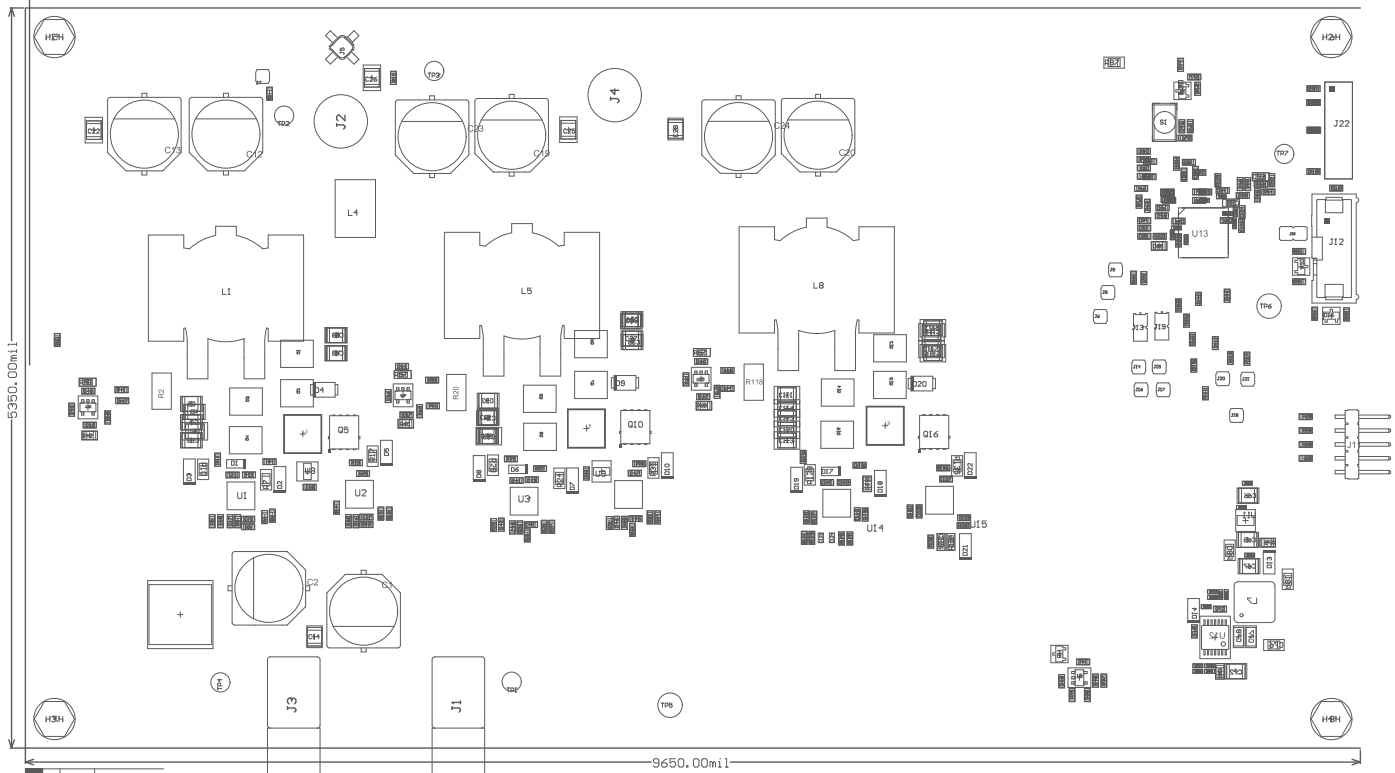
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Assembly Top
TID #:
GENERATED: 12/15/2022 11:10:17 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

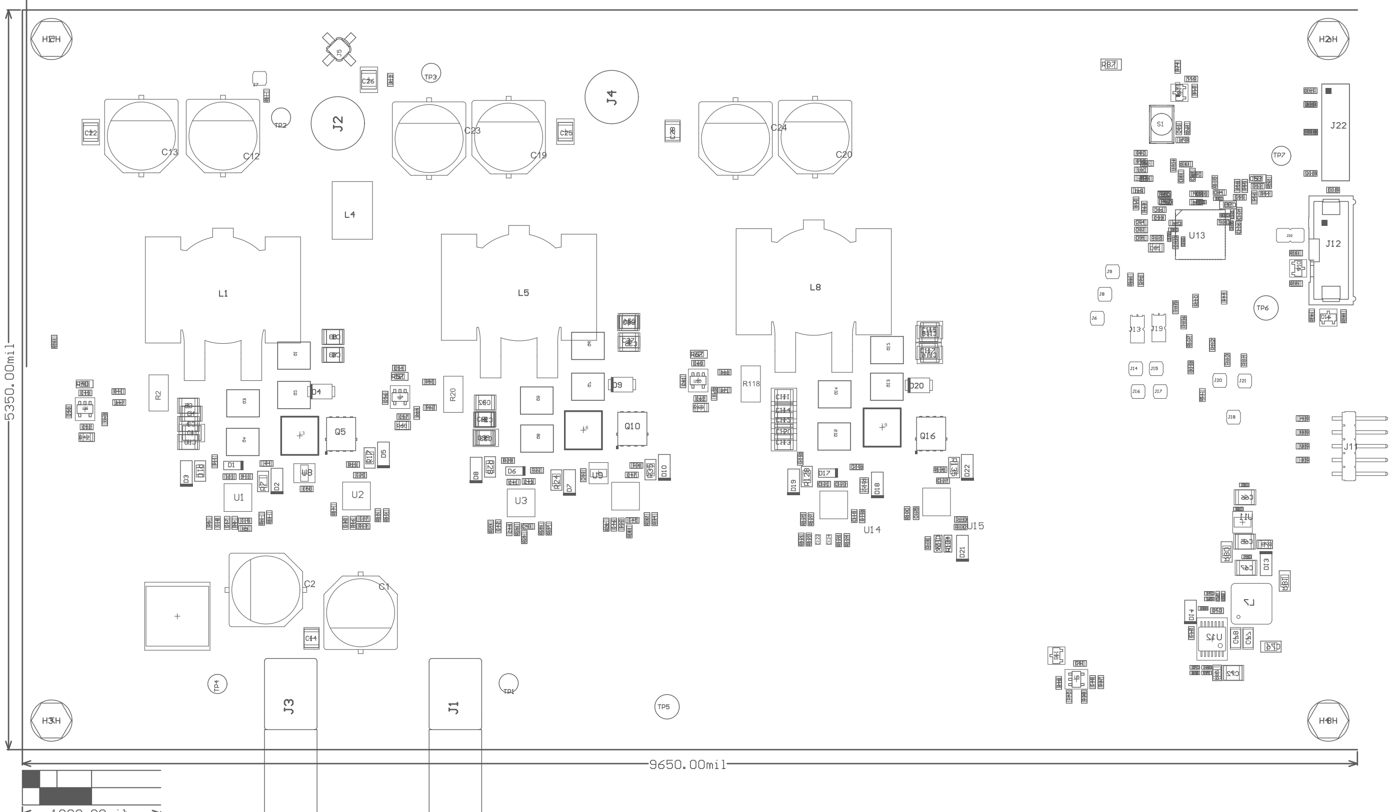
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
BOARD #: PMP20587 :# BOARD
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Assembly Bottom
TID #: PMP20587 :# TID
PLOT NAME = Assembly Bottom
GENERATED: 12/15/2022 11:10:17 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

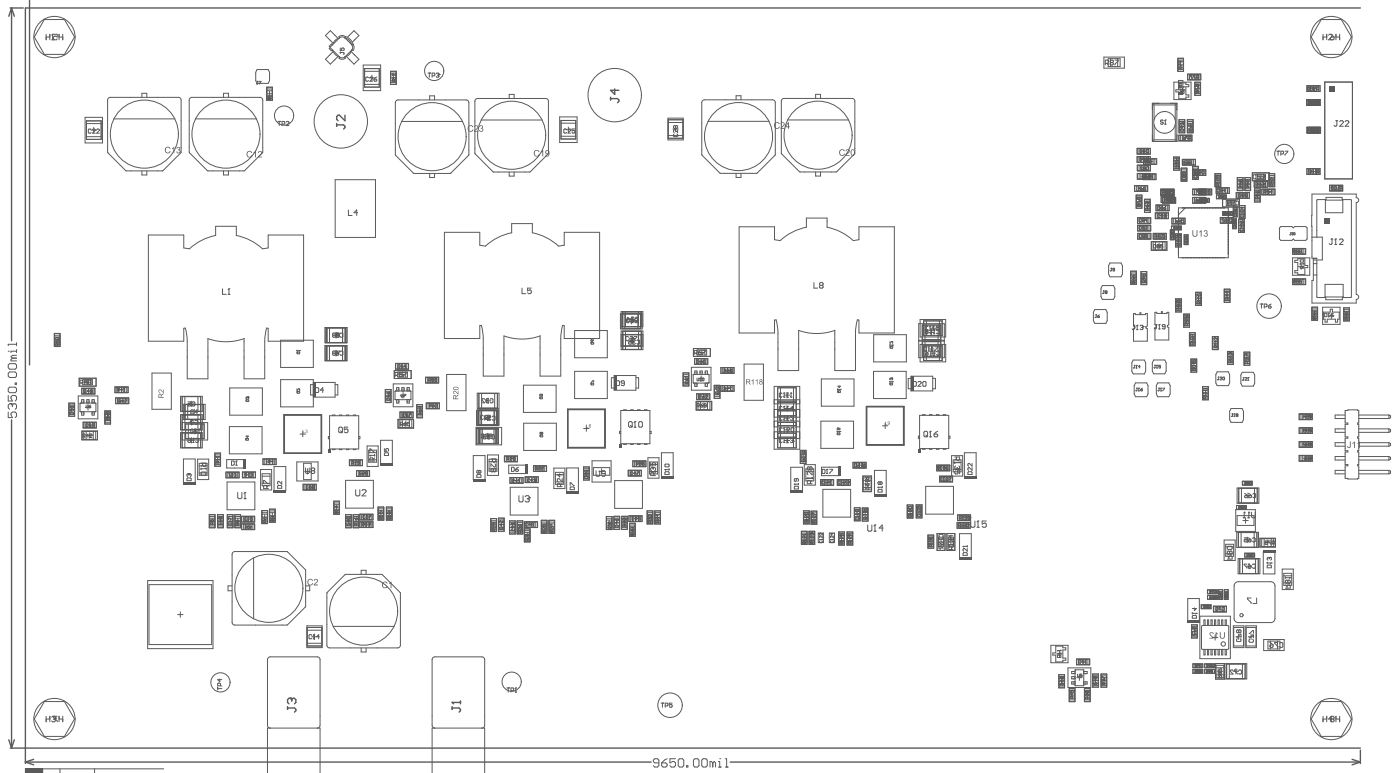
TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc
ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
BOARD #: PMP20587 REV: E
LAYER NAME = [illegible]
TID #: PMP20587
PLOT NAME = Title Sheet
GENERATED : 12/15/2022 11:10:17 AM
TEXAS INSTRUMENTS

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

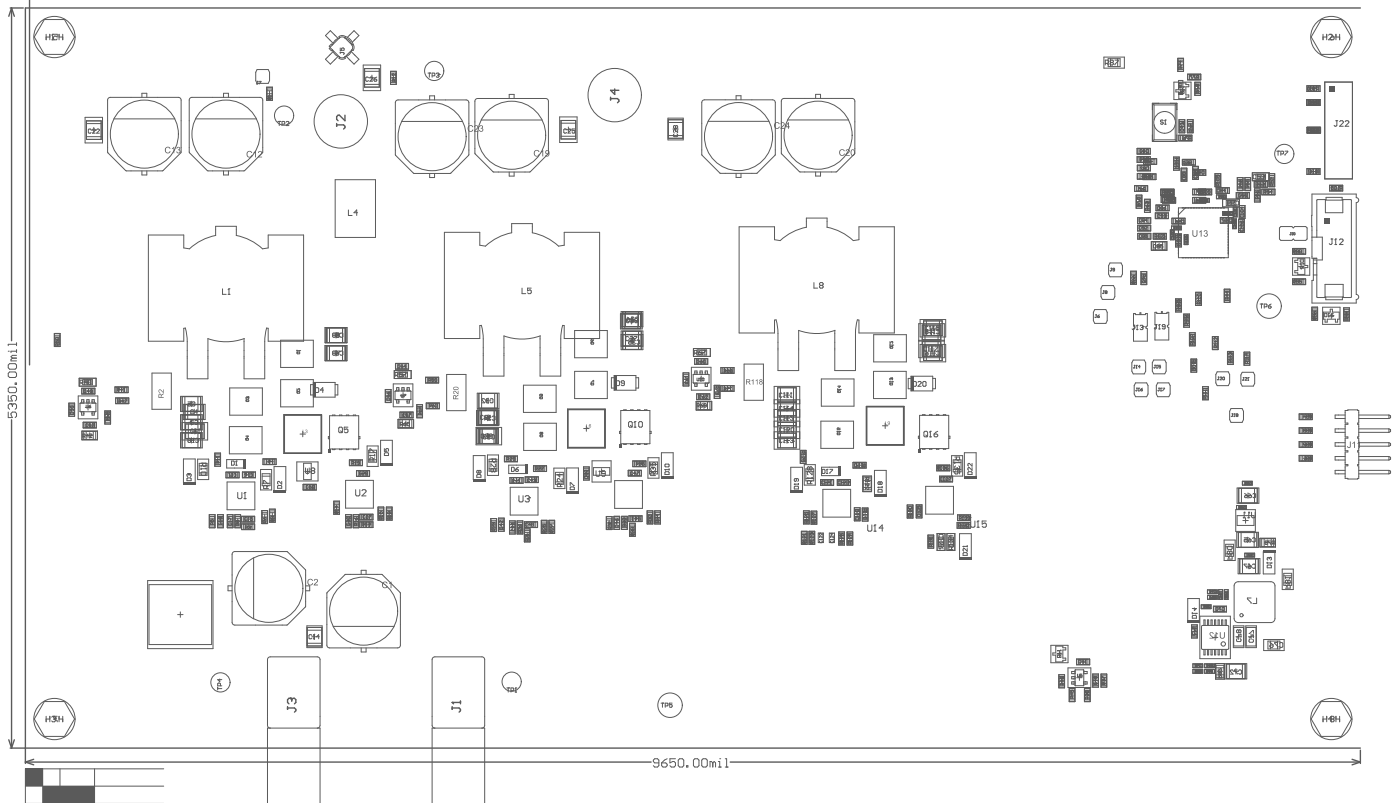
COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
BOARD #: PMP20587 :# BOARD
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Assembly Bottom
TID #: PMP20587 :# TID
PLOT NAME = M3 Notes
GENERATED: 12/15/2022 11:10:17 AM
TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED

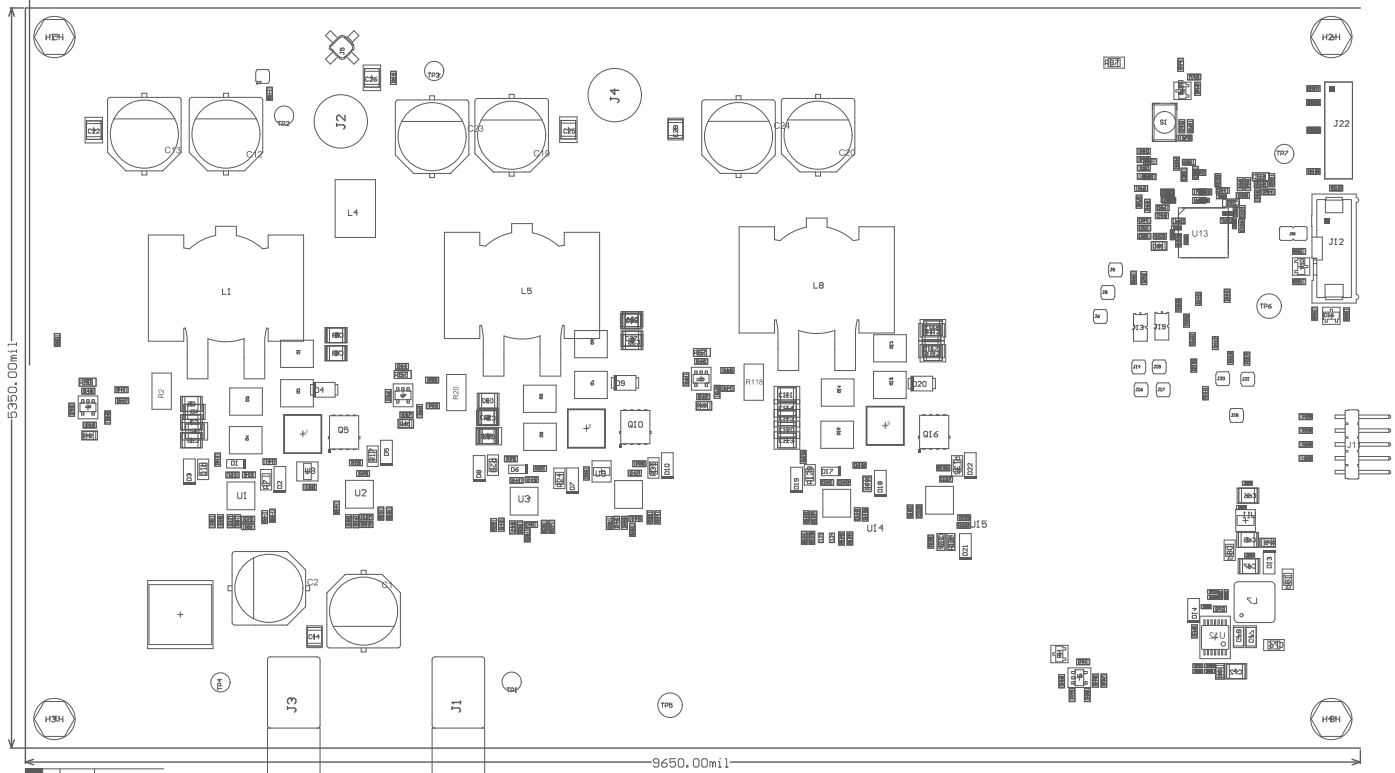
ASSEMBLY VARIANT: [No Variations]			
LAYER NAME = M[illegible]Assembly Bottom	TID #: [illegible]	:# DIT	
PLOT NAME = M[illegible]Gerber Information	GENERATED :: 12/15/2022 11:10:18 AM	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	Sean Xu & Sean Yu	LAYOUT BY:	Sean Xu
SCALE:	0.72	ALTIUM DESIGNER VERSION:	22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED

ASSEMBLY VARIANT: [No Variations]

LAYER NAME = [illegible]

PLOT NAME = M20XX_Stackup

GENERATED: 12/15/2022 11:10:18 AM

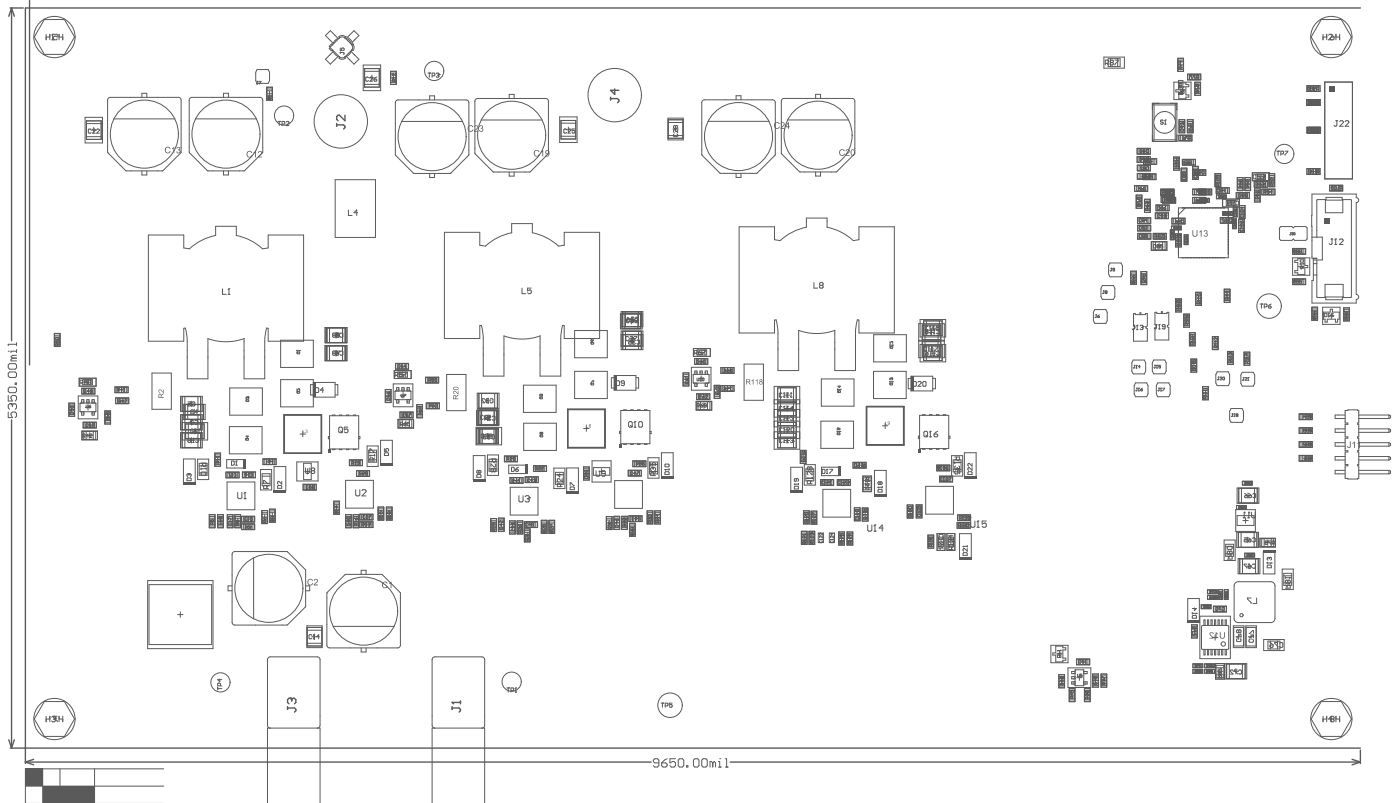
TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc
ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc

ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
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	Dielectric 2		10.00mil	4.2				
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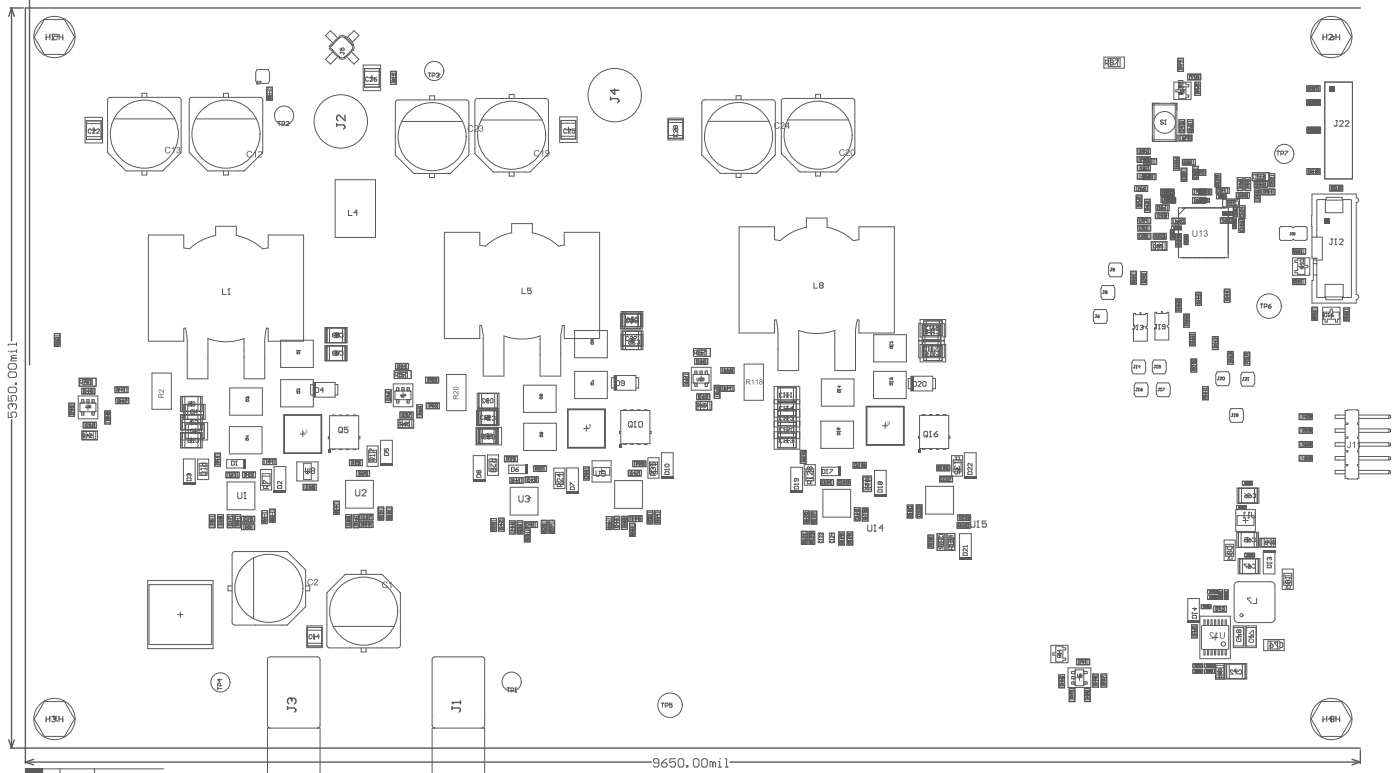
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
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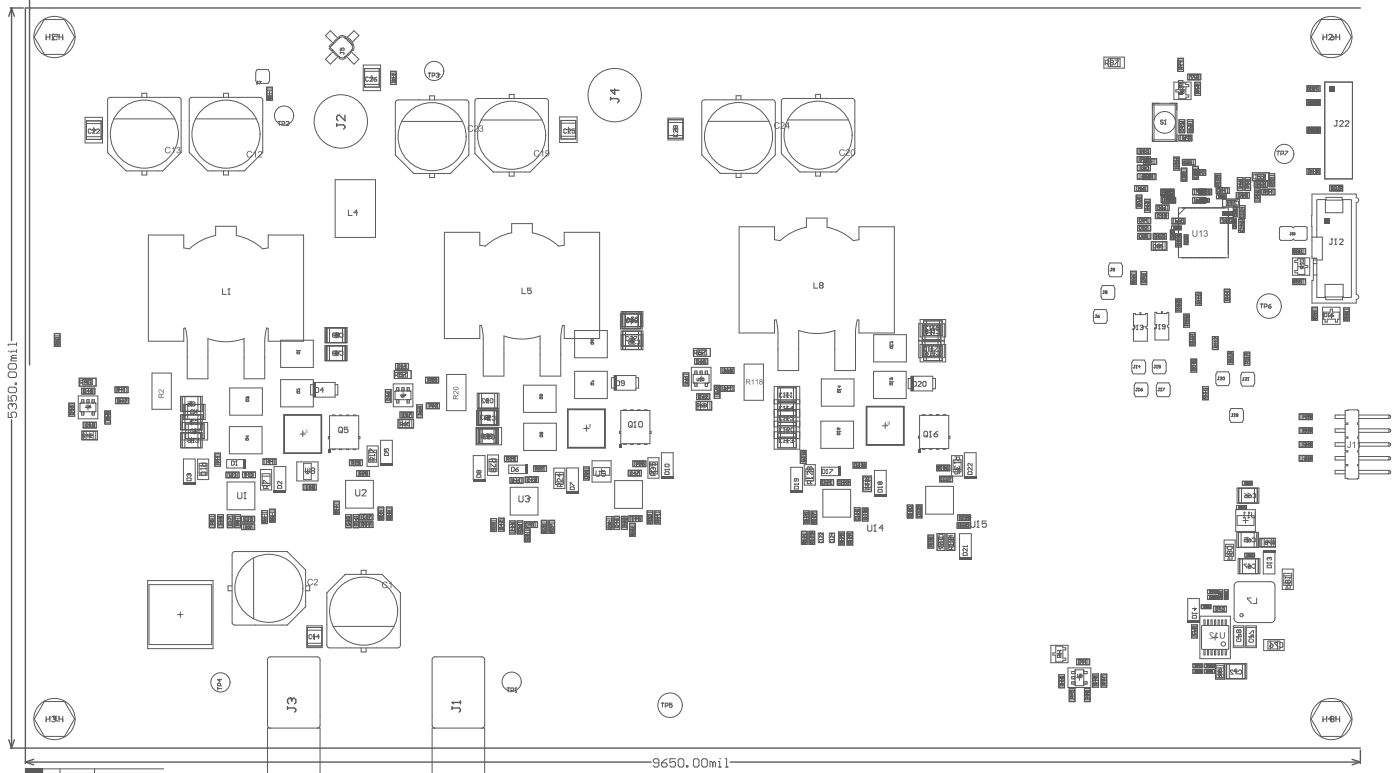
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

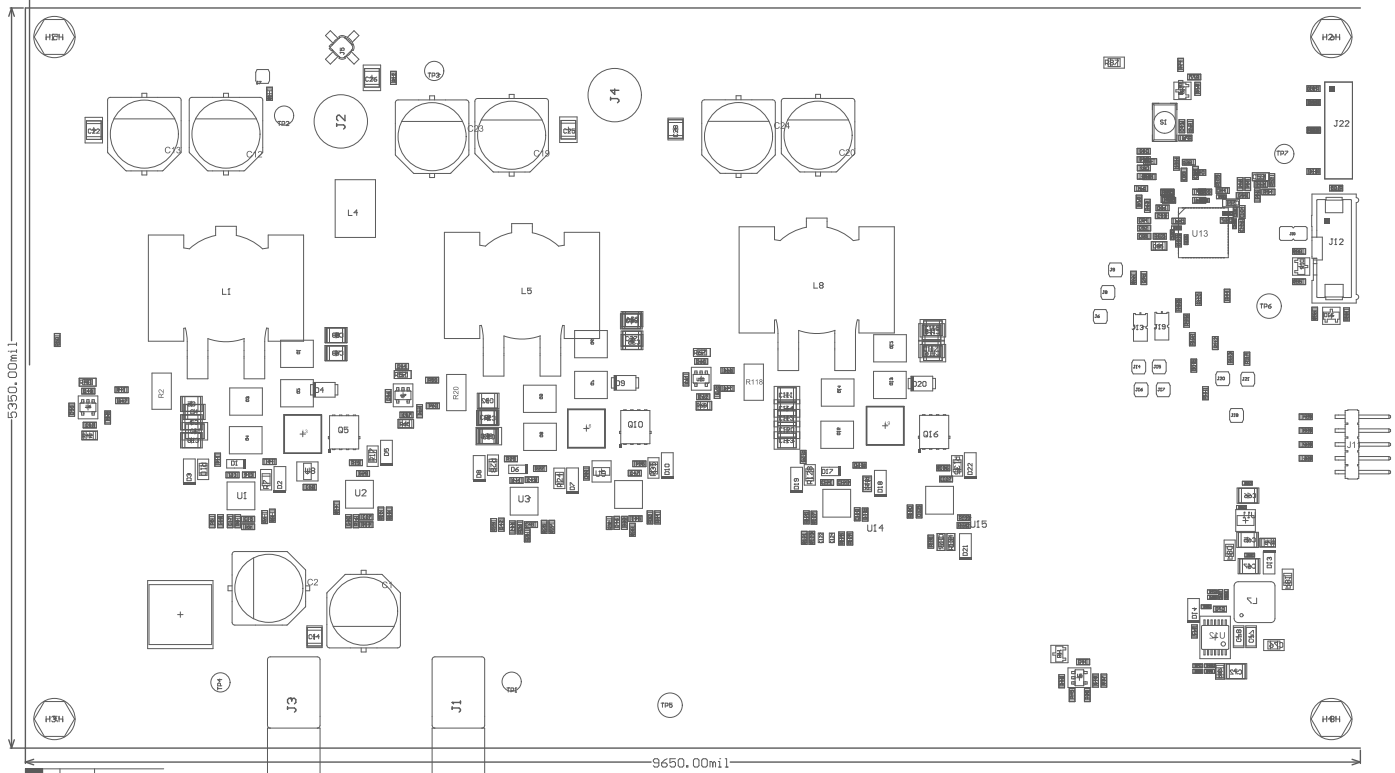
TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc
ENGINEER:	Sean Xu & Sean Yu
LAYOUT BY:	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
BOARD #: PMP20587 :# DRAWING
TID #: PMP20587 :# DIT
GENERATED :: 12/15/2022 11:10:18 AM
TEXAS INSTRUMENTS
LAYER NAME = M28 Courtyards Top
PLOT NAME = M28 Courtyards Top

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL
MATERIAL:	
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER	
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER	
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2	
[ ] OTHER +/-	
DRILLING:	
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES	
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER	
BOARD FINISH:	
SILKSCREEN: [X] TOP [X] BOTTOM	
SILKSCREEN COLOR: [X] WHITE [ ] OTHER	
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER	
[X] MATTE [ ] SEMI-GLOSS	
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG	
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER	
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE	
[ ] N.C. ROUTE [X] V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:	
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3	
[X] RoHS [ ] OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS: MICROSECTION: [ ] YES	
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER	

TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED

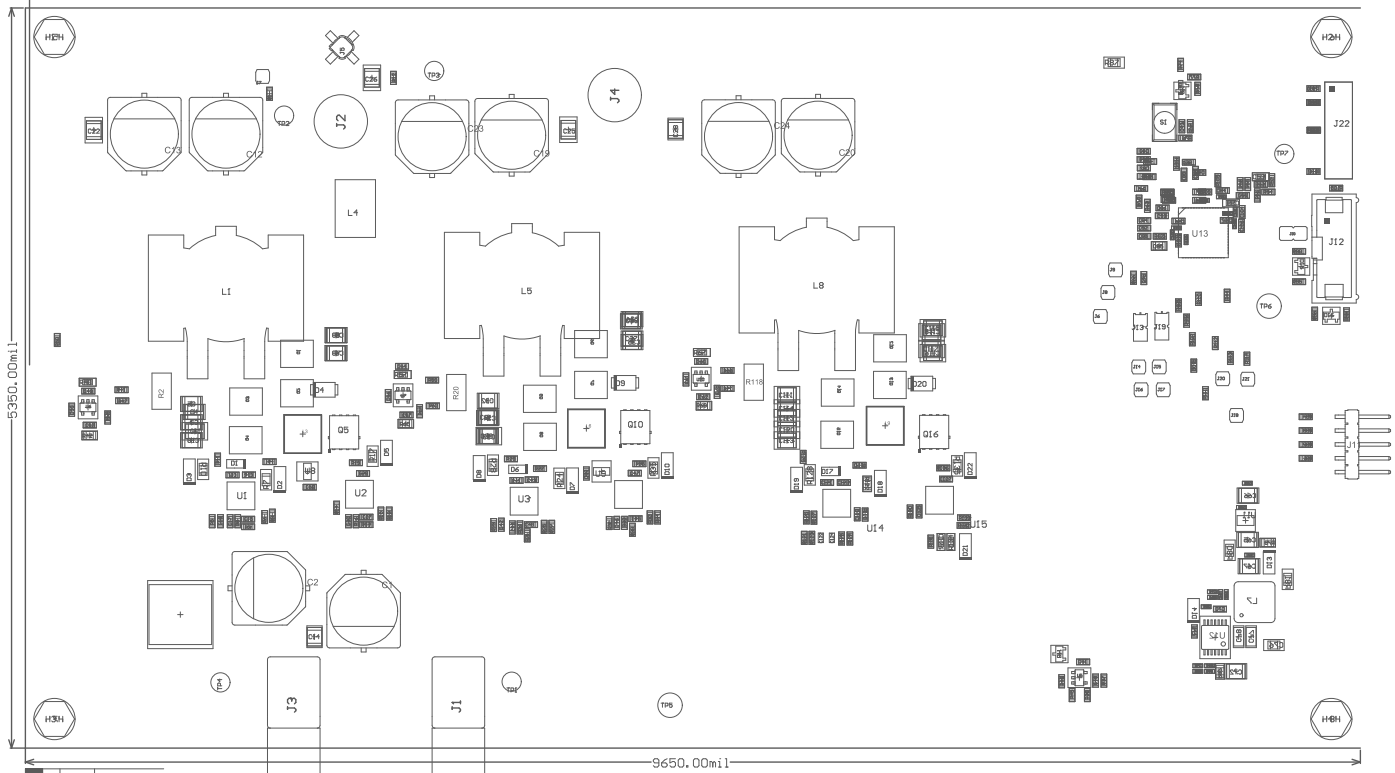
ASSEMBLY VARIANT: [No Variations]			
LAYER NAME = M1 Courtyards Bottom	TID #:		
PLOT NAME = M1 Courtyards Bottom	GENERATED: 12/15/2022 11:10:18 AM		

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: Sean Xu & Sean Yu	LAYOUT BY: Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

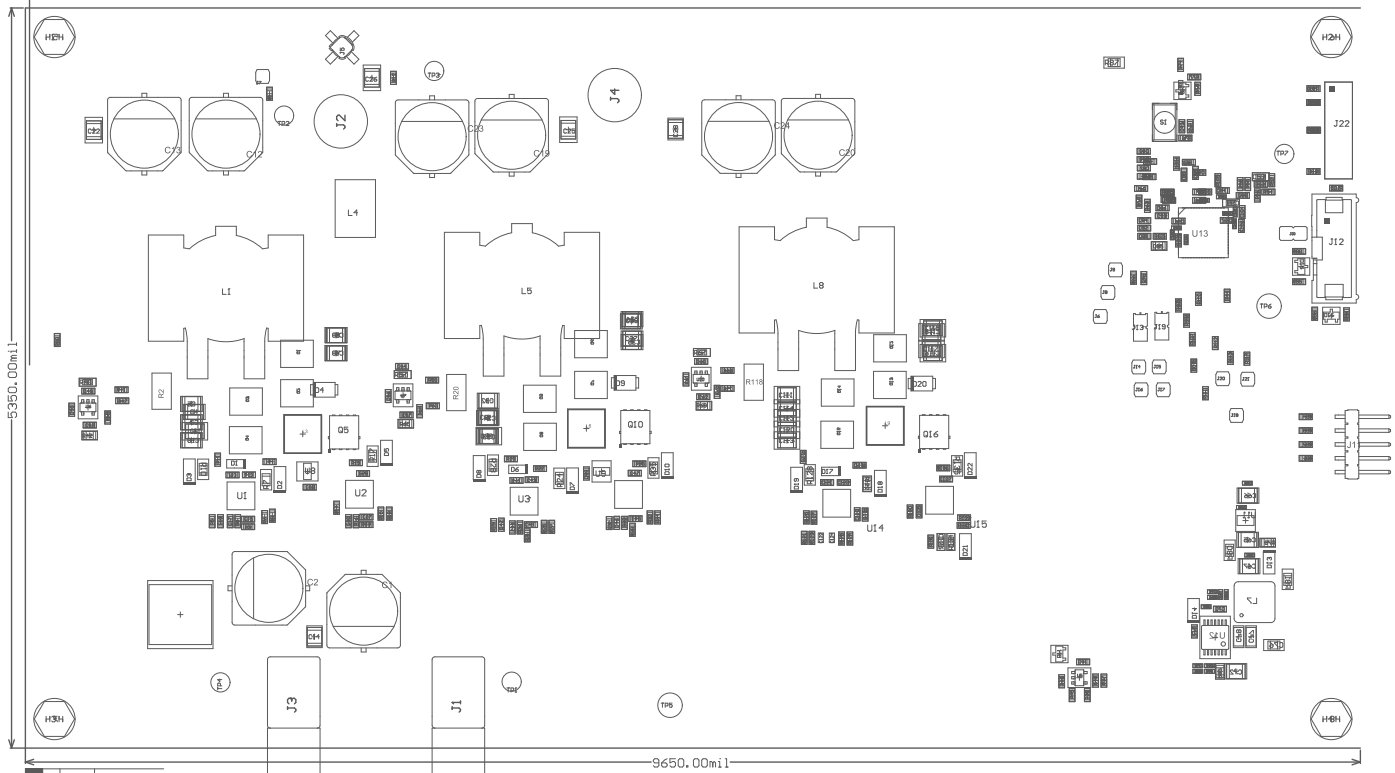
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Embedded Cavity
TID #: :# DIT
PLOT NAME = Embedded Cavity
GENERATED :: 12/15/2022 11:10:18 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

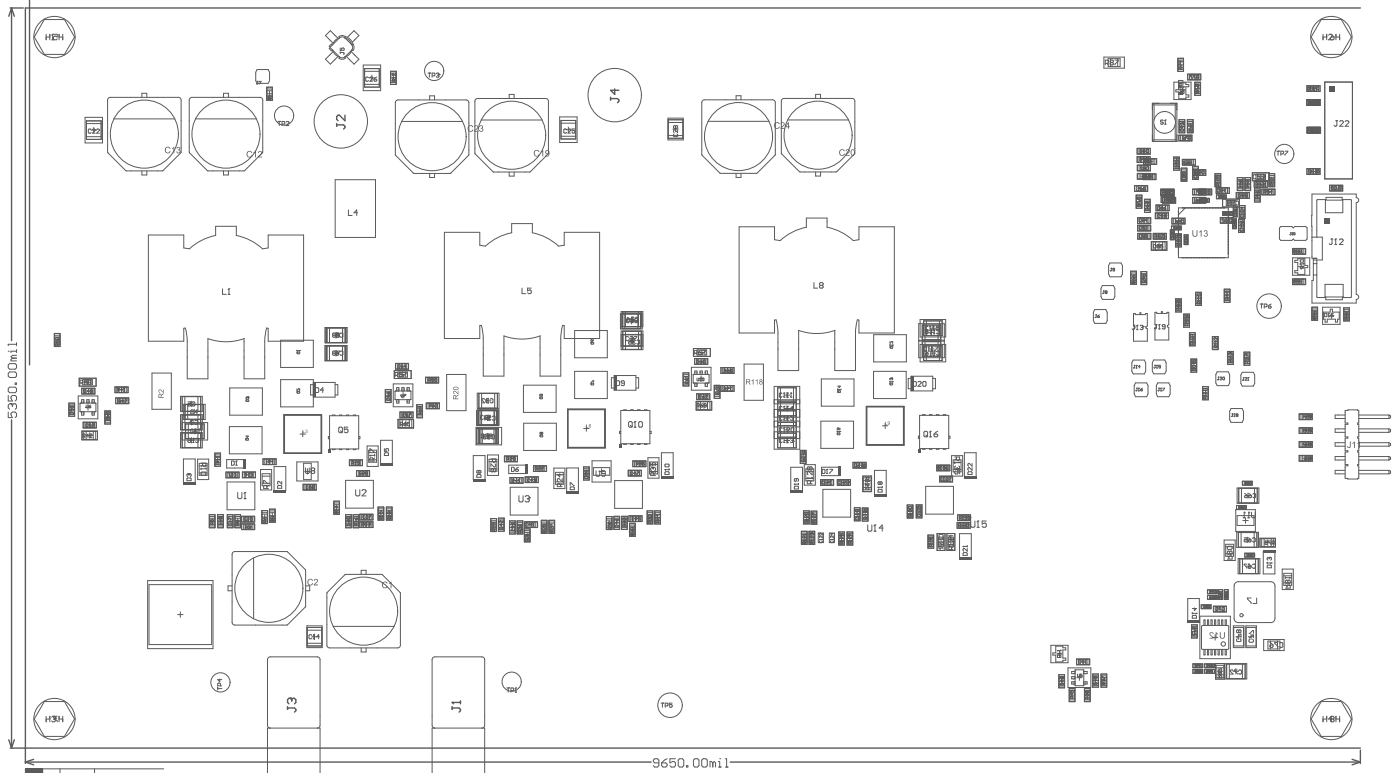
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = [illegible]
PLOT NAME = [illegible]
BOARD #: PMP20587 :# DWG REV: E
TID #: PMP20587 :# DIT
GENERATED: 12/15/2022 11:10:19 AM
TEXAS INSTRUMENTS

ENGINEER: Sean Xu & Sean Yu
LAYOUT BY: Sean Xu
SCALE: 0.72
ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

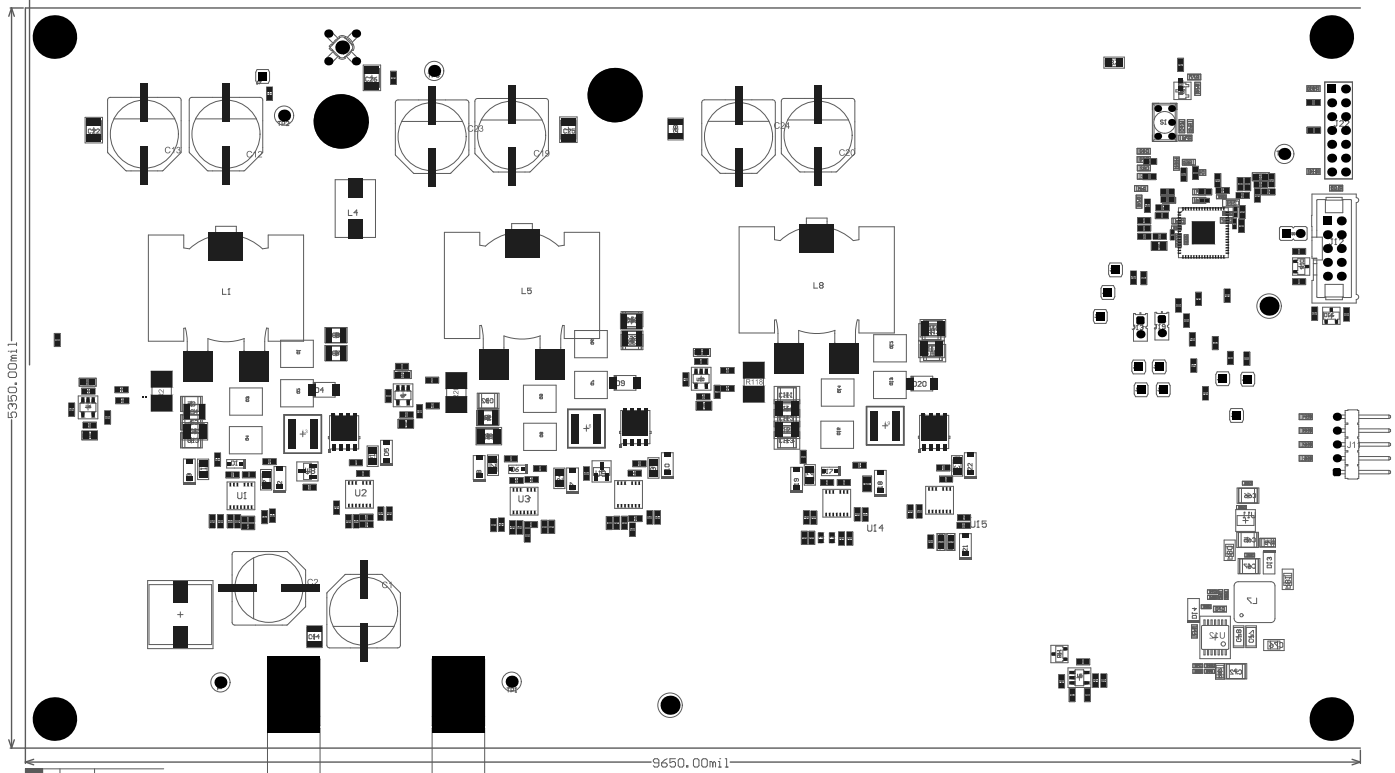
TEXAS INSTRUMENTS

PROJECT TITLE:	UCD3138 Digital Inverting Buck Boost
DESIGNED FOR:	Public Release
FILE NAME:	PMP20587_REVE.PcbDoc
ENGINEER:	Sean Xu & Sean Yu
LAYOUT BY:	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Assembly Bottom
TID #:
PLOT NAME = Embedded Keepout
GENERATED:
TEXAS INSTRUMENTS

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

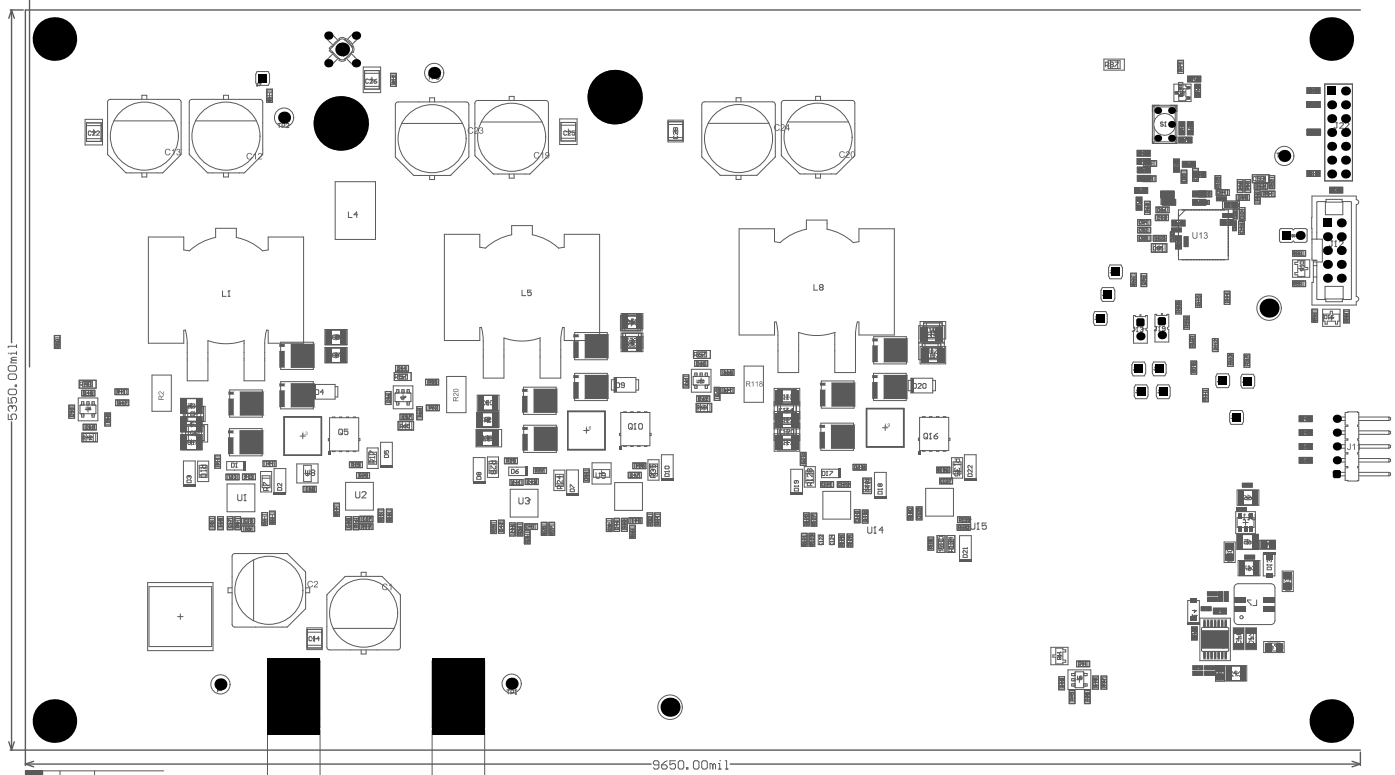
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Assembly Bottom
TID #:
PLOT NAME = Top Pad Master
GENERATED: 12/15/2022 11:10:19 AM
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

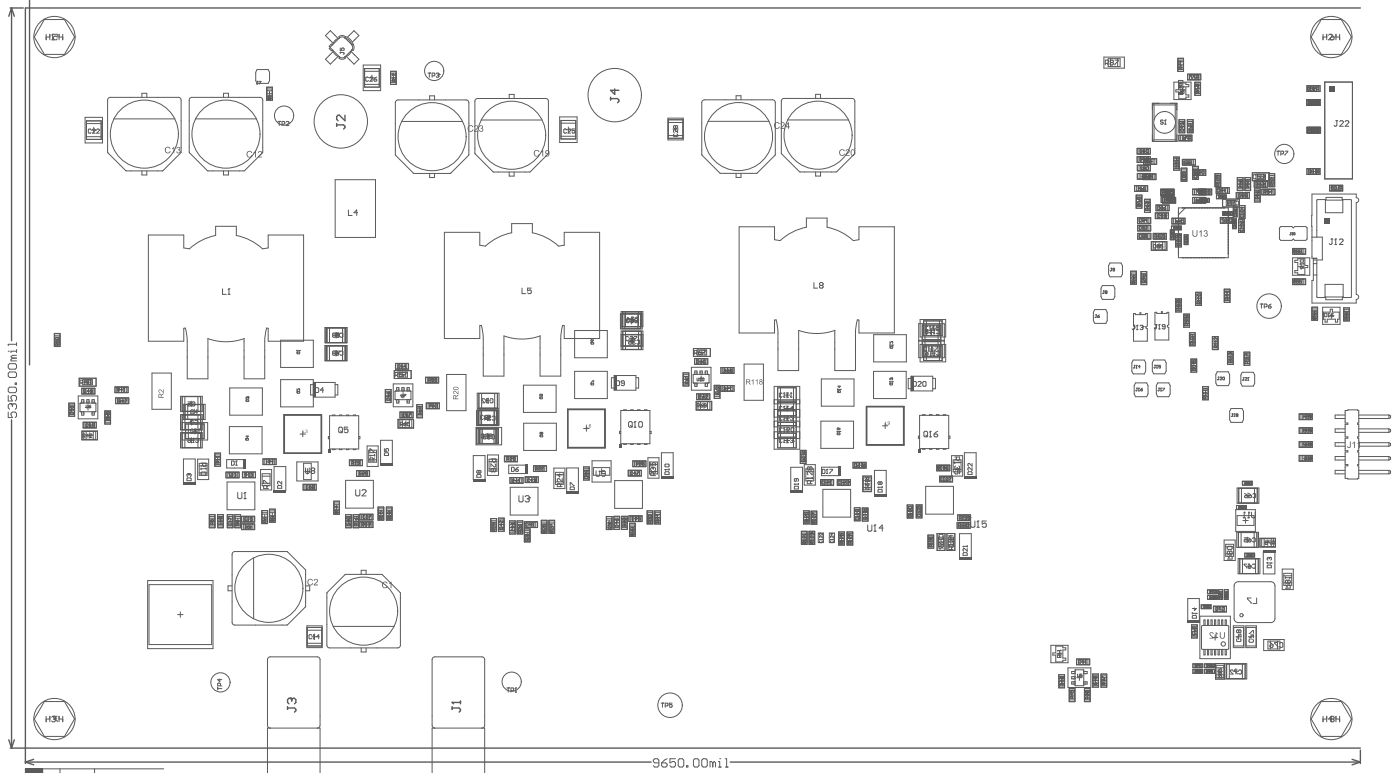
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Master
TID #:
GENERATED: 12/15/2022 11:10:19 AM Master Pad TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED

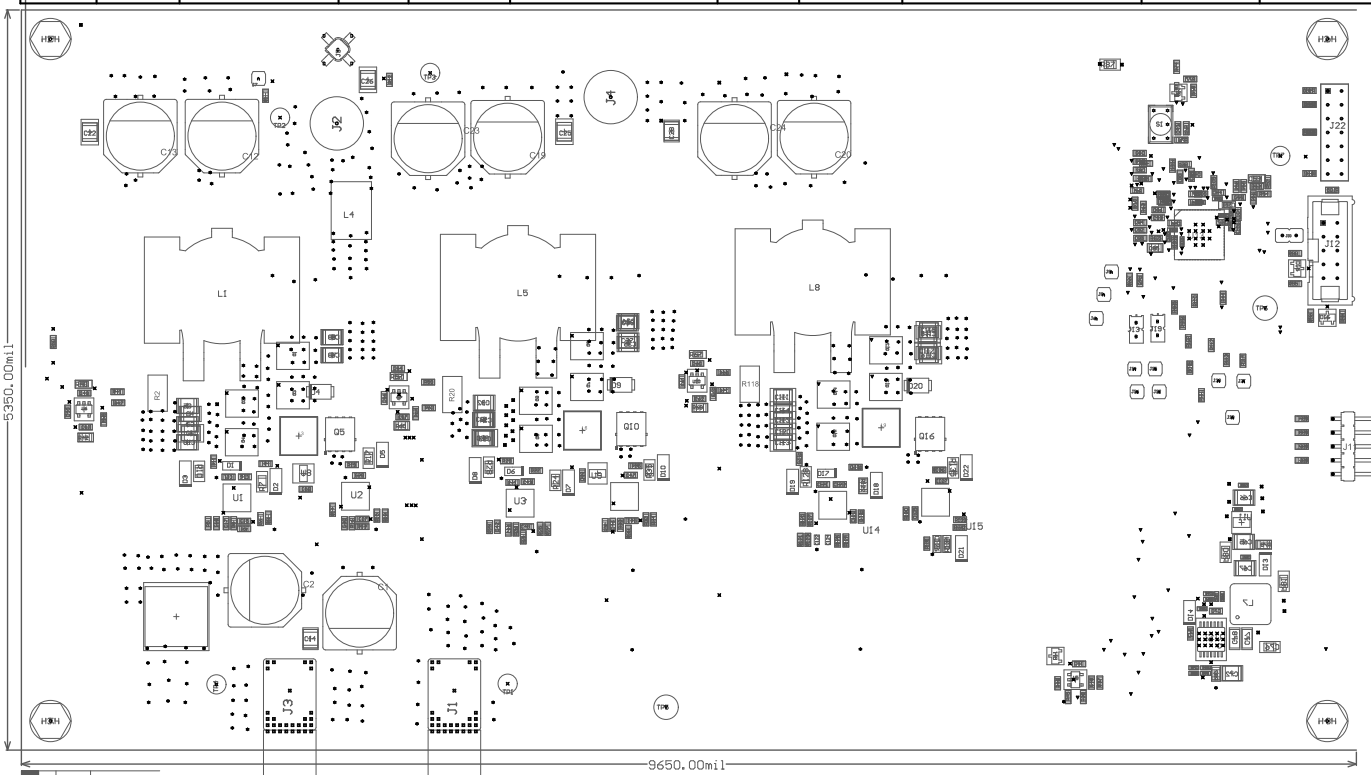
LAYER NAME = Assembly Bottom
TID #: [illegible] :# DIT
ASSEMBLY VARIANT: [No Variations]
GENERATED: 12/15/2022 11:10:19 AM
PLOT NAME = Assembly Bottom Layer
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
C	1	68.00mil (1.727mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c254h173			
▽	2	98.43mil (2.500mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c350h250			
☒	2	188.00mil (4.775mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rectangle	r1397_965h478o-114_0p914_483			
⊙	2	214.57mil (5.450mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c1000h545			
D	1	38.00mil (0.965mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c152h97			
B	40	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
○	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c800h320			
☆	50	26.00mil (0.660mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c127h66			
⊕	5	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
⊠	3	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c221h160			
◇	11	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rectangle	s165h115			
◎	78	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
⊗	22	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v127h71			
⊡	56	16.00mil (0.406mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v81h41			
▽	3	14.50mil (0.368mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)			
⊠	18	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)			
✱	478	25.00mil (0.635mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v127h64			
	833 Total										

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
1	Top Overlay								
	Top Solder								
	Top Layer		1.40mil						
	Dielectric1	FR-4	10.00mil	4.8					
2	Signal Layer		1.20mil						
	Dielectric		20.00mil						
3	Signal Layer		1.20mil						
	Dielectric 2		10.00mil	4.2					
4	Signal Layer		1.20mil						
	Dielectric 3		10.00mil	4.2					
5	Signal Layer		1.20mil						
	Dielectric		20.00mil						
6	Bottom Layer		1.40mil						
	Bottom Solder	Solder Resist	0.40mil	3.5					
	Bottom Overlay								

Install labels in silkscreen location. Text shall be 8 mil thick. Text shall not overlap other labels, pads, or plated holes.
These assemblies are ESD sensitive, ESD precautions shall be observed.
These assemblies must be cleaned after soldering to remove all contaminants. No clean flux is not acceptable.
These assemblies must comply with workmanship standards IPC-610 Class 2 unless otherwise specified.



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

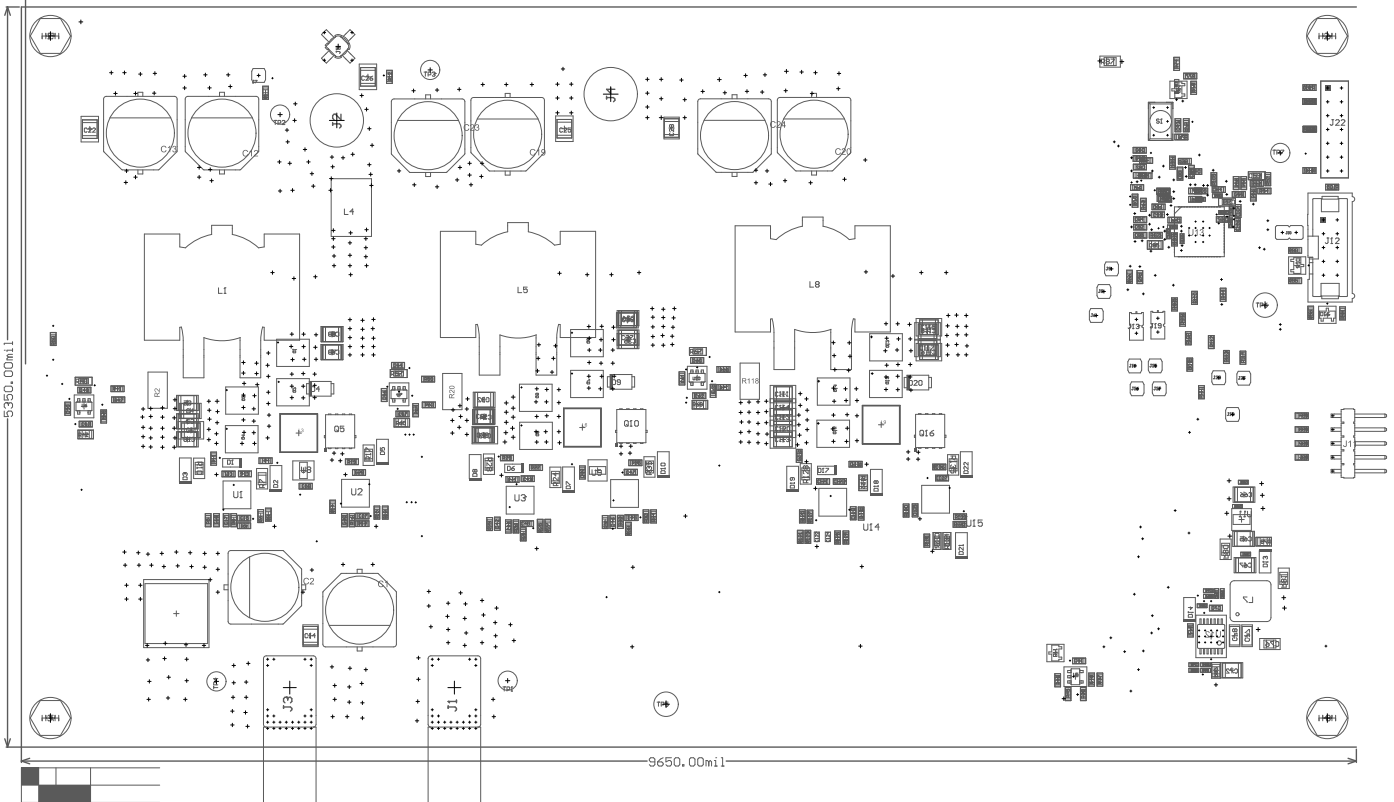
PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Drawing For Manufacturer
TID #: PMP20587 :# QIT
PLOT NAME = PMP20587 Drawing For Manufacturer
TEXAS INSTRUMENTS

ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack	Board Layer Stack	Board Layer Stack
	Top Overlay							
	Top Solder	Solder Resist	0.40mil	3.5				
1	Top Layer		2.80mil					
	Dielectric1	FR-4	10.00mil	4.8				
2	Signal Layer 1		4.20mil					
	Dielectric 3		10.00mil	4.2				
3	Signal Layer 2		4.20mil					
	Dielectric 2		10.00mil	4.2				
4	Signal Layer 3		4.20mil					
	Dielectric 5		10.00mil	4.2				
5	Signal Layer 4		4.20mil					
	Dielectric 4		10.00mil	4.2				
6	Bottom Layer		2.80mil					
	Bottom Solder	Solder Resist	0.40mil	3.5				
	Bottom Overlay							



DESIGN INFORMATION	
MIN. TRACK WIDTH:	8 MIL
MIN. CLEARANCE:	0.2 mm
MIN. VIA PAD SIZE:	24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):	+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: UCD3138 Digital Inverting Buck Boost
DESIGNED FOR: Public Release
FILE NAME: PMP20587_REVE.PcbDoc

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]
LAYER NAME = Bottom
TID #: PMP20587
PLOT NAME = PMP20587 Guide For (Top Layer)

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ENGINEER:	LAYOUT BY:
Sean Xu & Sean Yu	Sean Xu
SCALE: 0.72	ALTIUM DESIGNER VERSION: 22.1.2.22

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