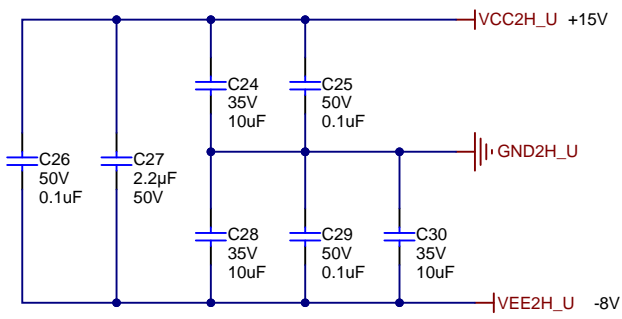
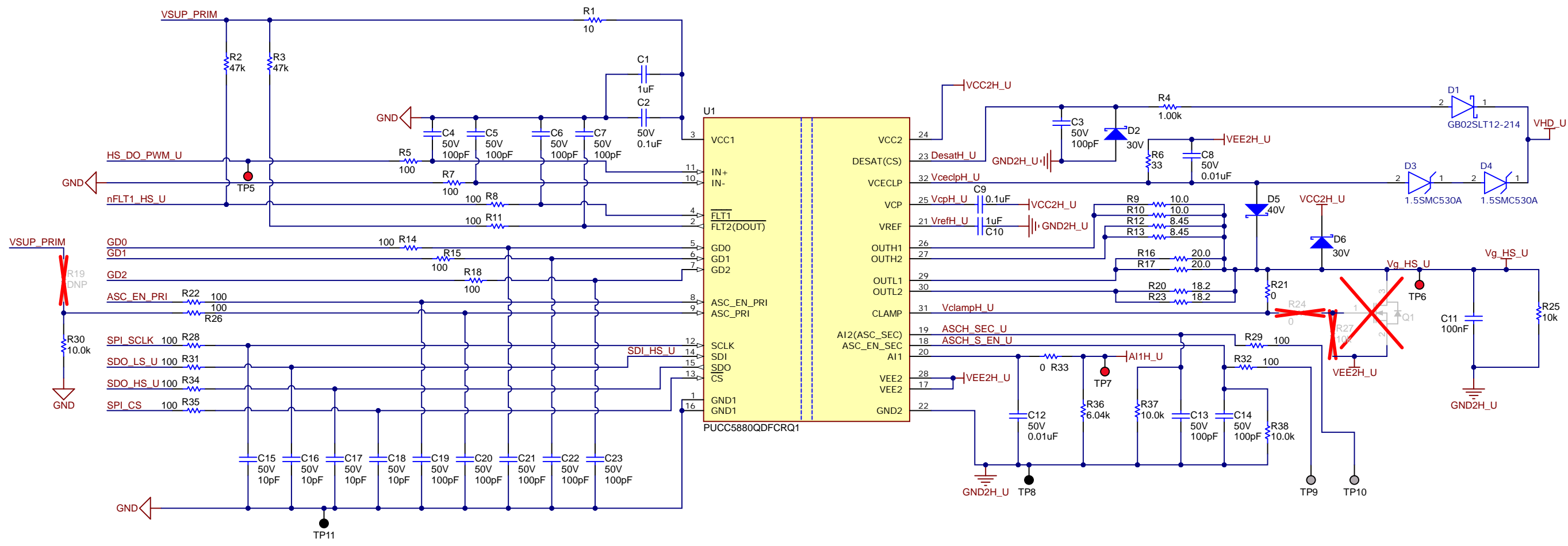
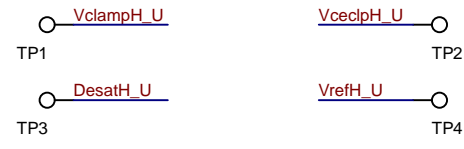


Revision History	
Revision	Notes
A	* first draft



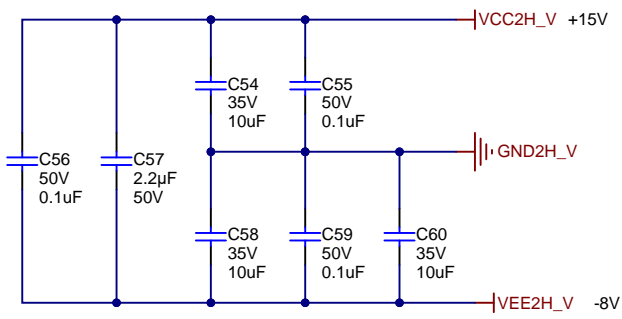
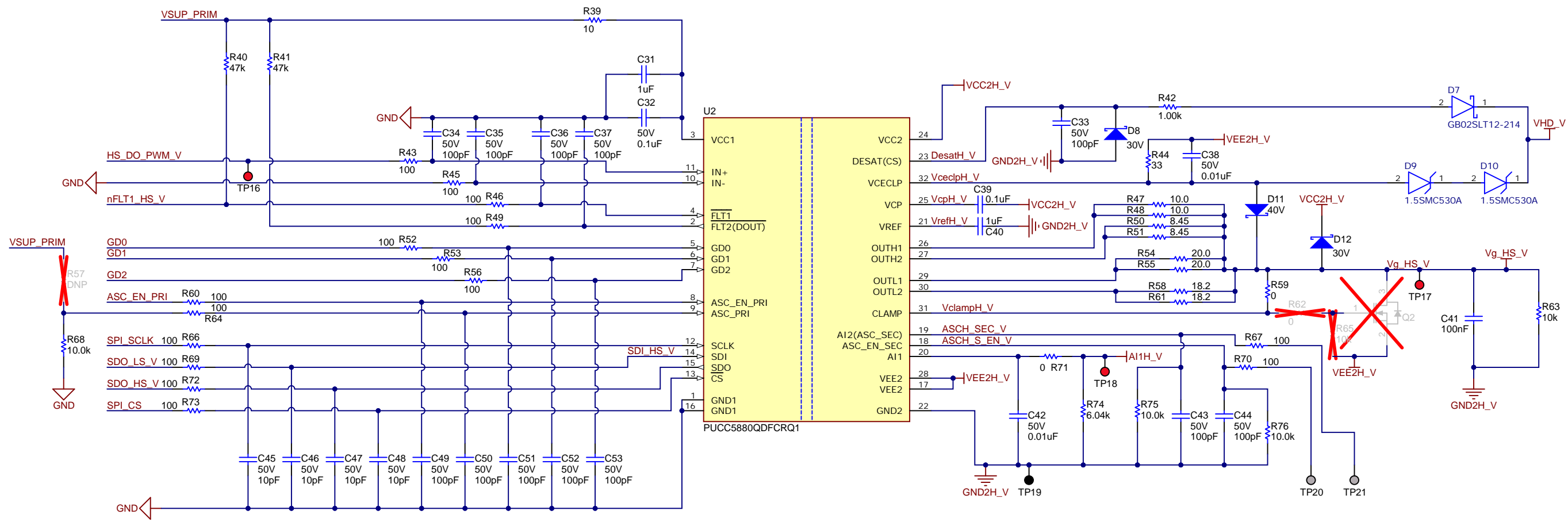
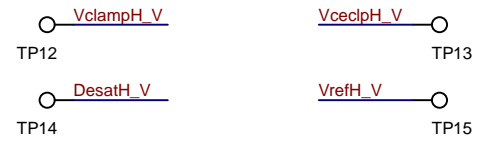
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TID #: N/A	Project Title: Gate Drive Board for IGBT HybridPack	
Number: PMP31236	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 1 of 11
Drawn By:	File: PMP31236RevA_HS_U.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	



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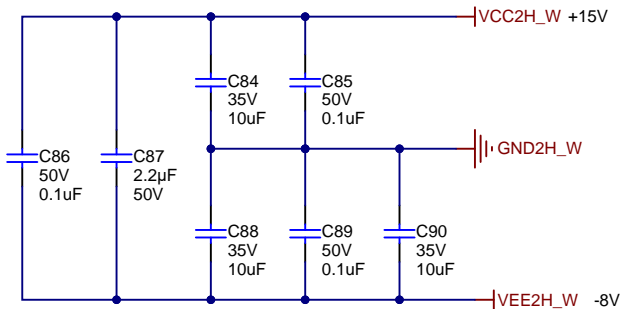
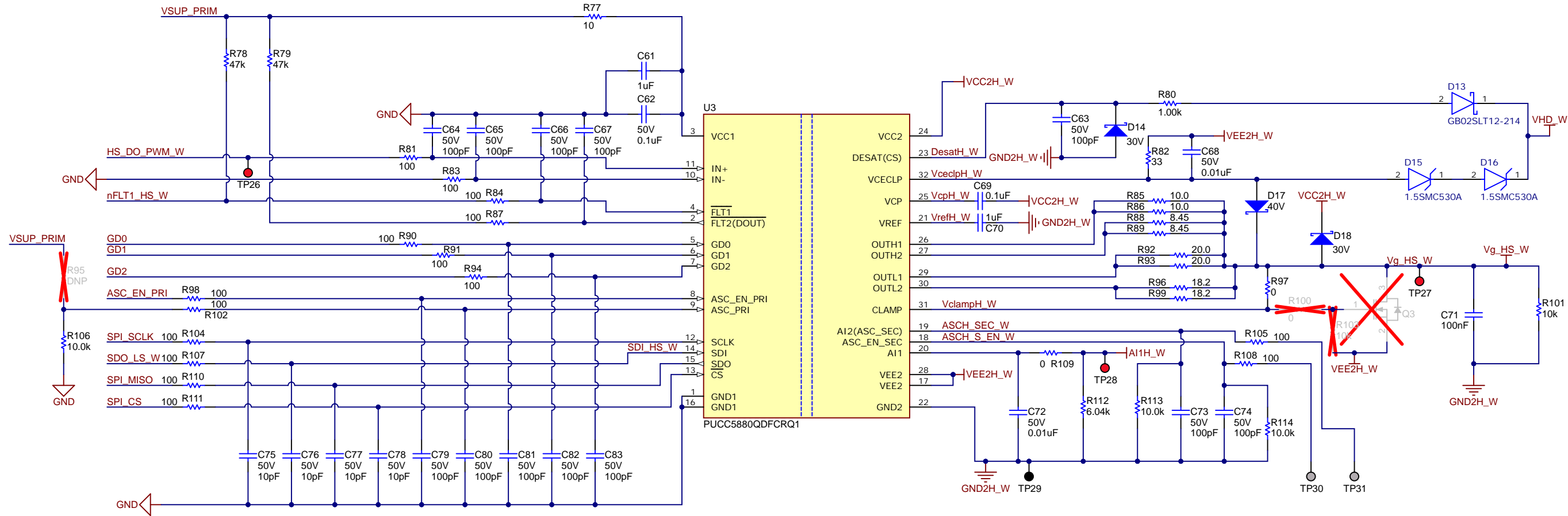
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TID #: N/A	Project Title: Gate Drive Board for IGBT HybridPack	
Number: PMP31236	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 2 of 11
Drawn By:	File: PMP31236RevA_HS_V.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	



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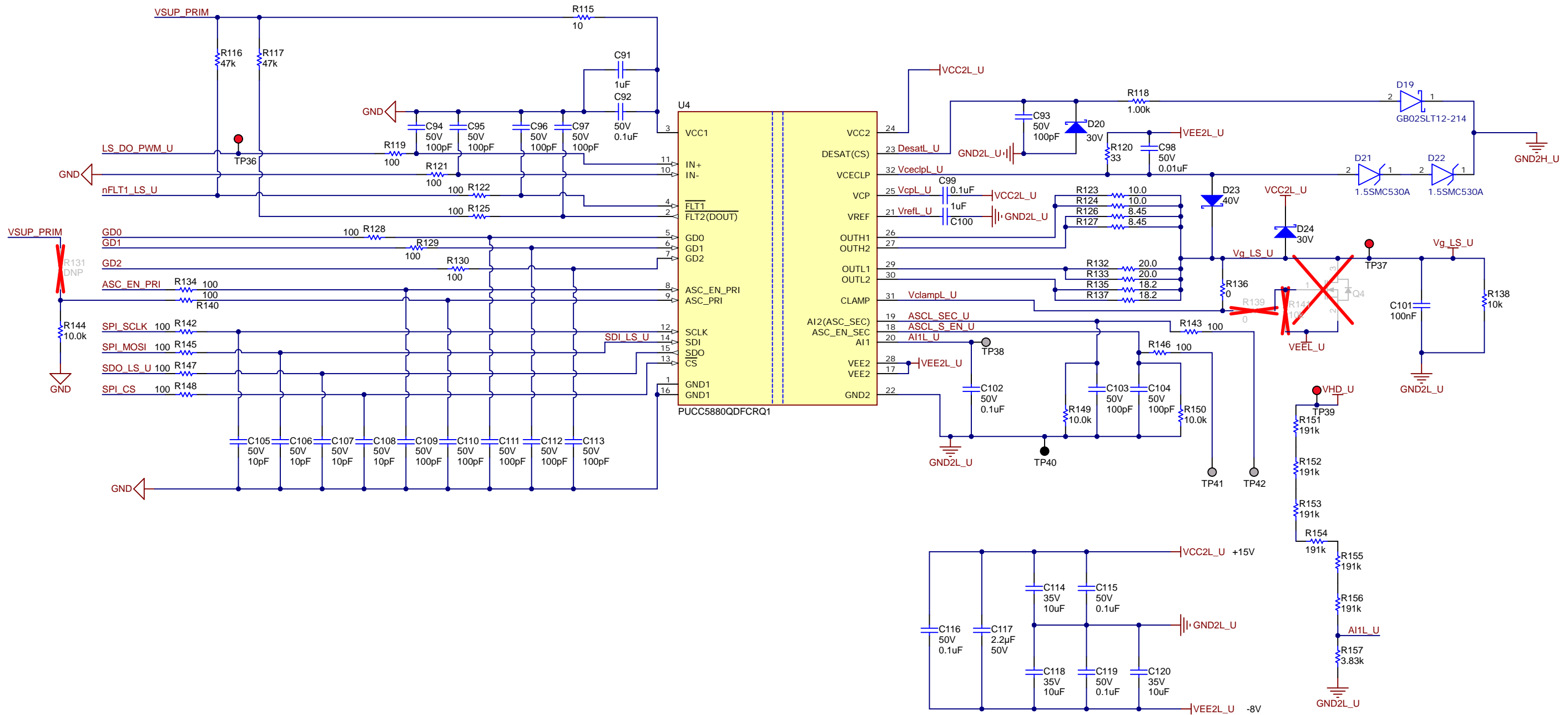
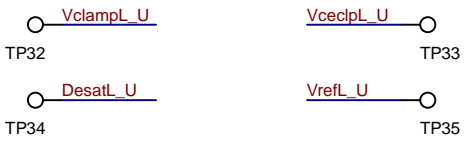


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TID #: N/A	Project Title: Gate Drive Board for IGBT HybridPack	
Number: PMP31236	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 3 of 11
Drawn By:	File: PMP31236RevA_HS_W.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	



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Revision	Notes
A	* first draft

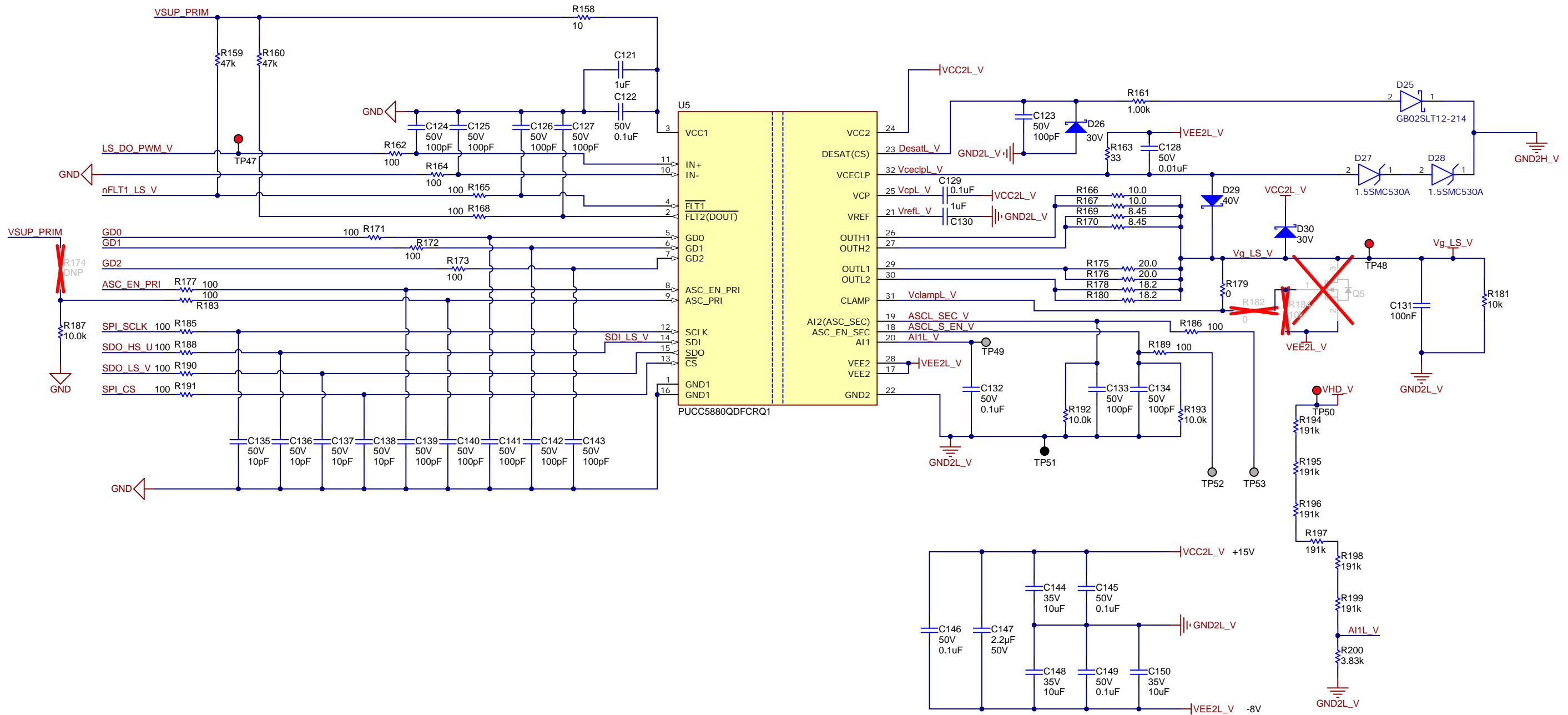
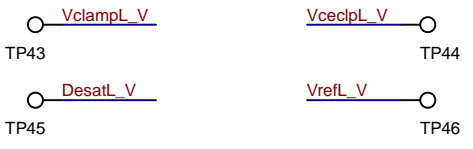


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Number: PMP31236	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 4 of 11
Drawn By:	File: PMP31236RevA_LS_U.SchDoc	Size: B
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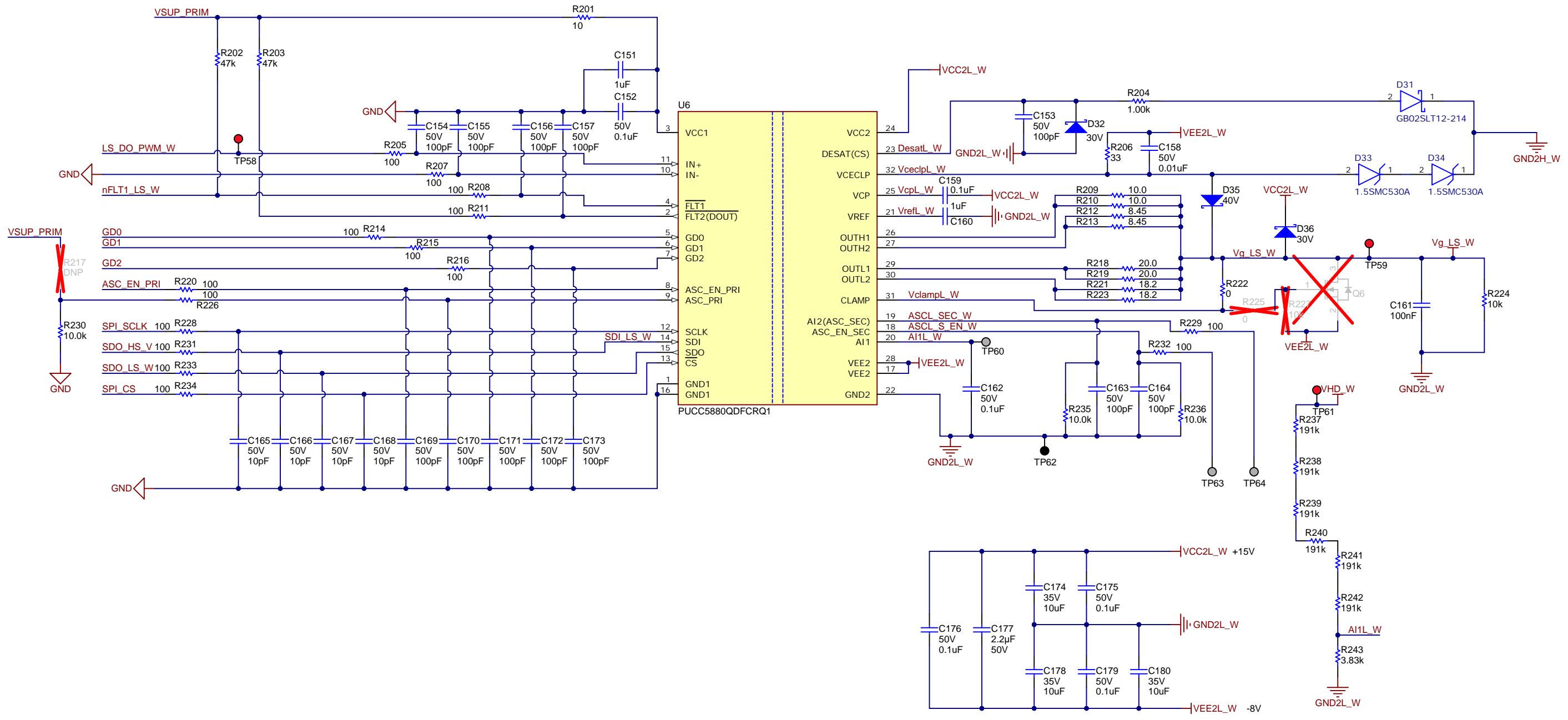
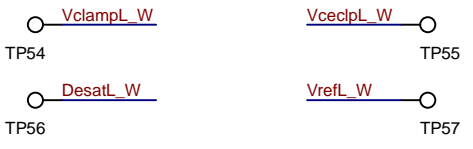


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Number: PMP31236	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 5 of 11
Drawn By:	File: PMP31236RevA_LS_V.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	



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Revision	Notes
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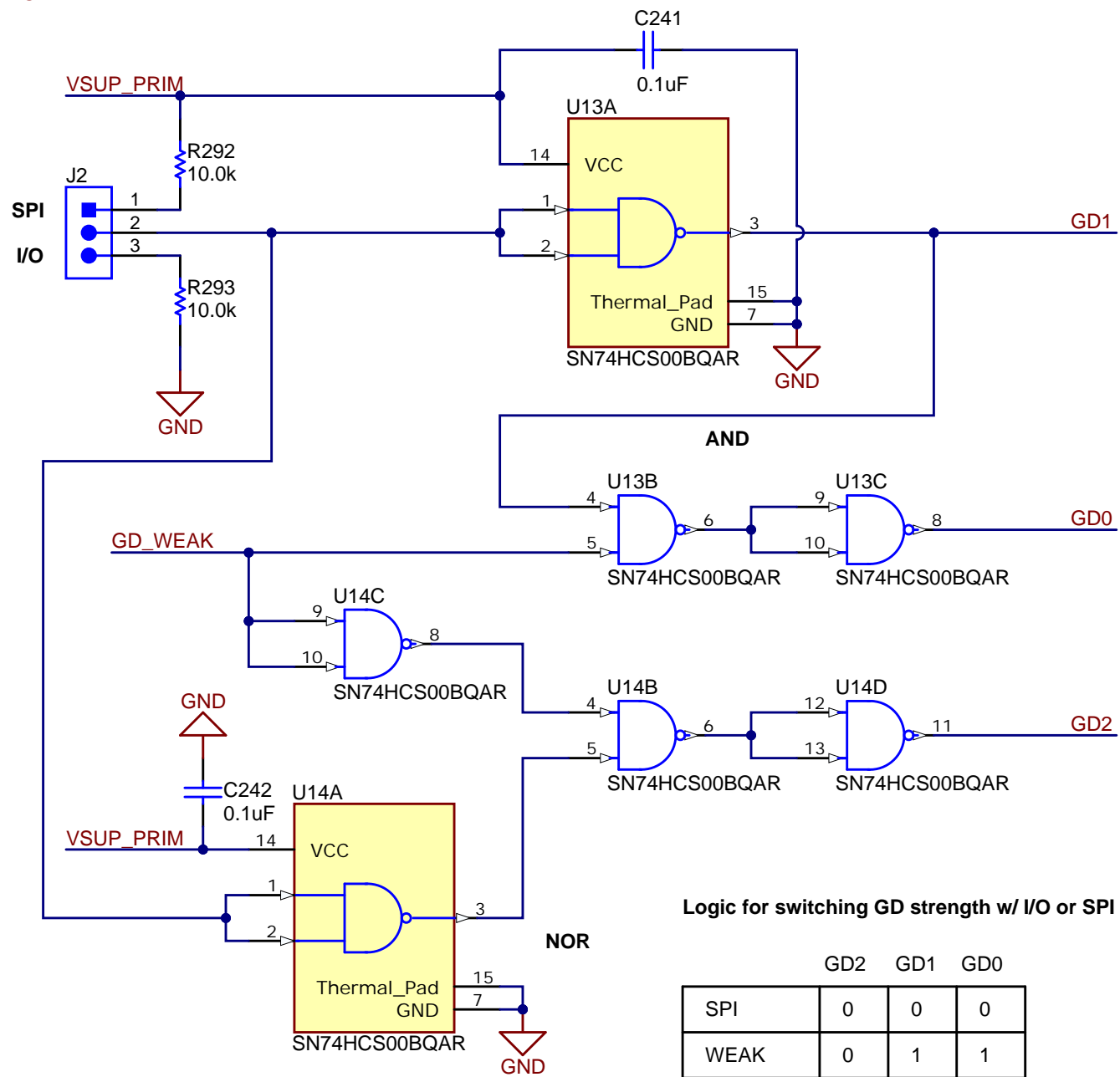
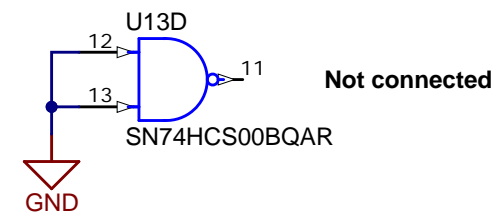
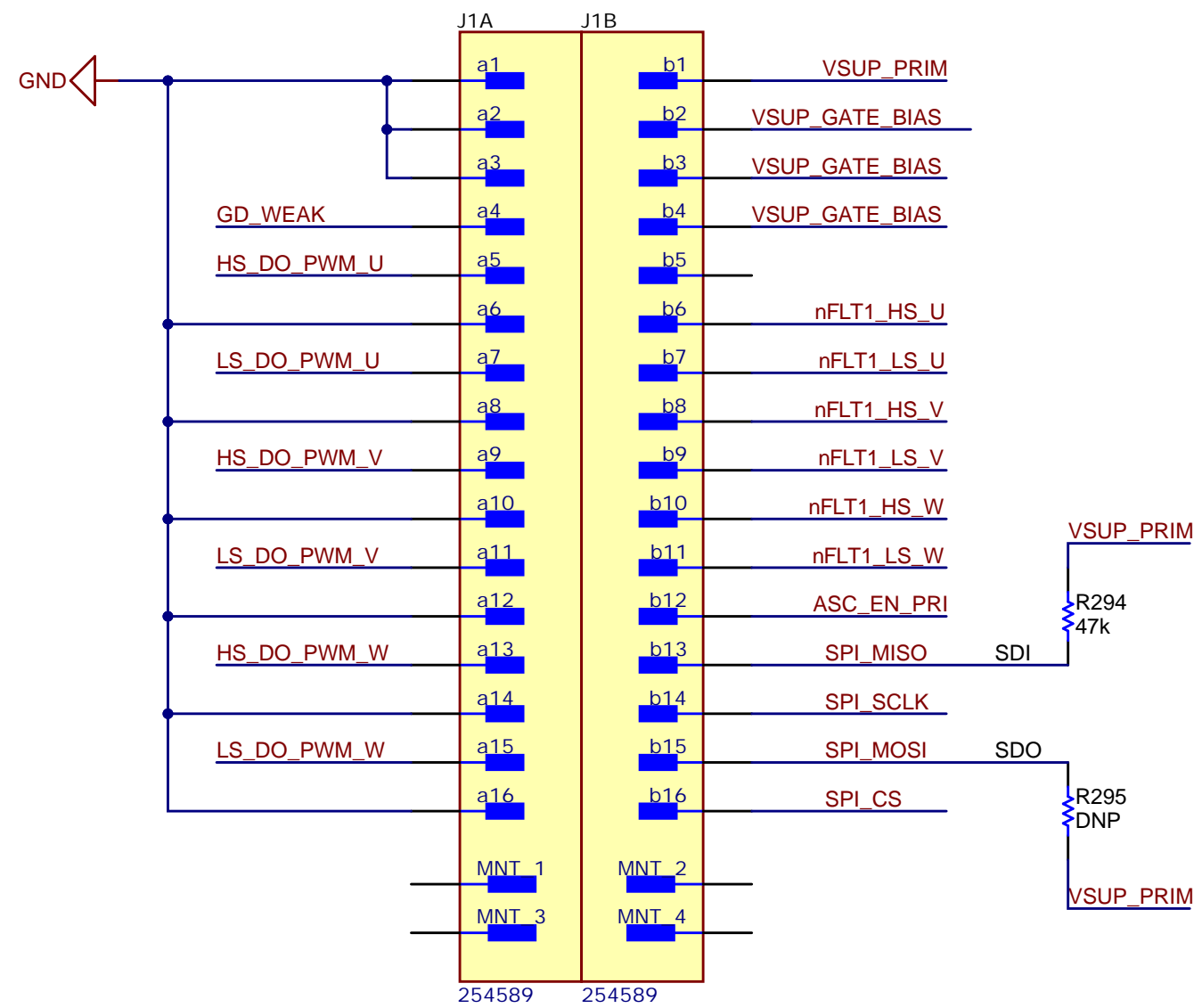


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TID #: N/A	Project Title: Gate Drive Board for IGBT HybridPack	
Number: PMP31236	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 6 of 11
Drawn By:	File: PMP31236RevA_LS_W.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	



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Revision	Notes
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Logic for switching GD strength w/ I/O or SPI

	GD2	GD1	GD0
SPI	0	0	0
WEAK	0	1	1
STRONG	1	1	0

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TID #: N/A	Project Title: Gate Drive Board for IGBT HybridPack	
Number: PMP31236	Rev: A	Sheet Title: Interface
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 7 of 11
Drawn By:	File: PMP31236RevA_Interface.SchDoc	Size: A4
Engineer: M Zehendner	Contact: https://www.ti.com/support	

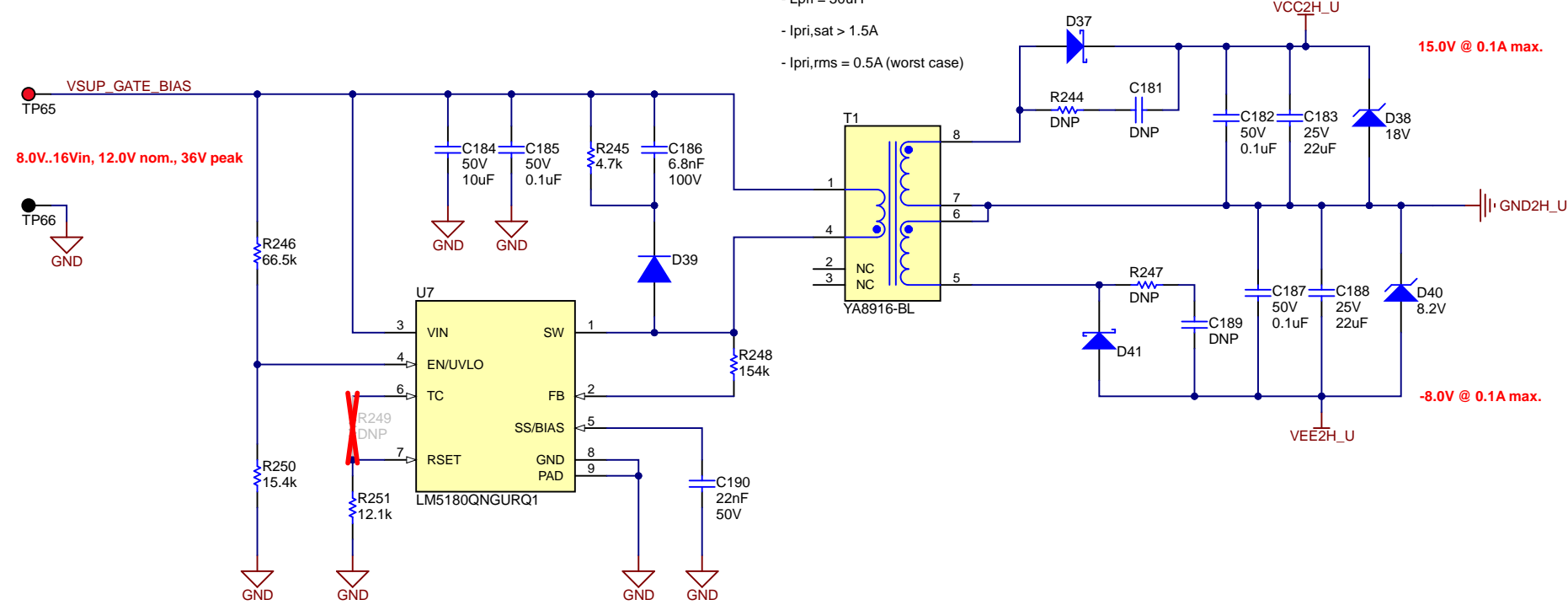




**Design Notes:**

- D38 / D43 only needed for no load conditions
- Snubber networks need to be optimized in the lab
- DNP = Do Not Populate

Revision History	
Revision	Notes
A	* first draft

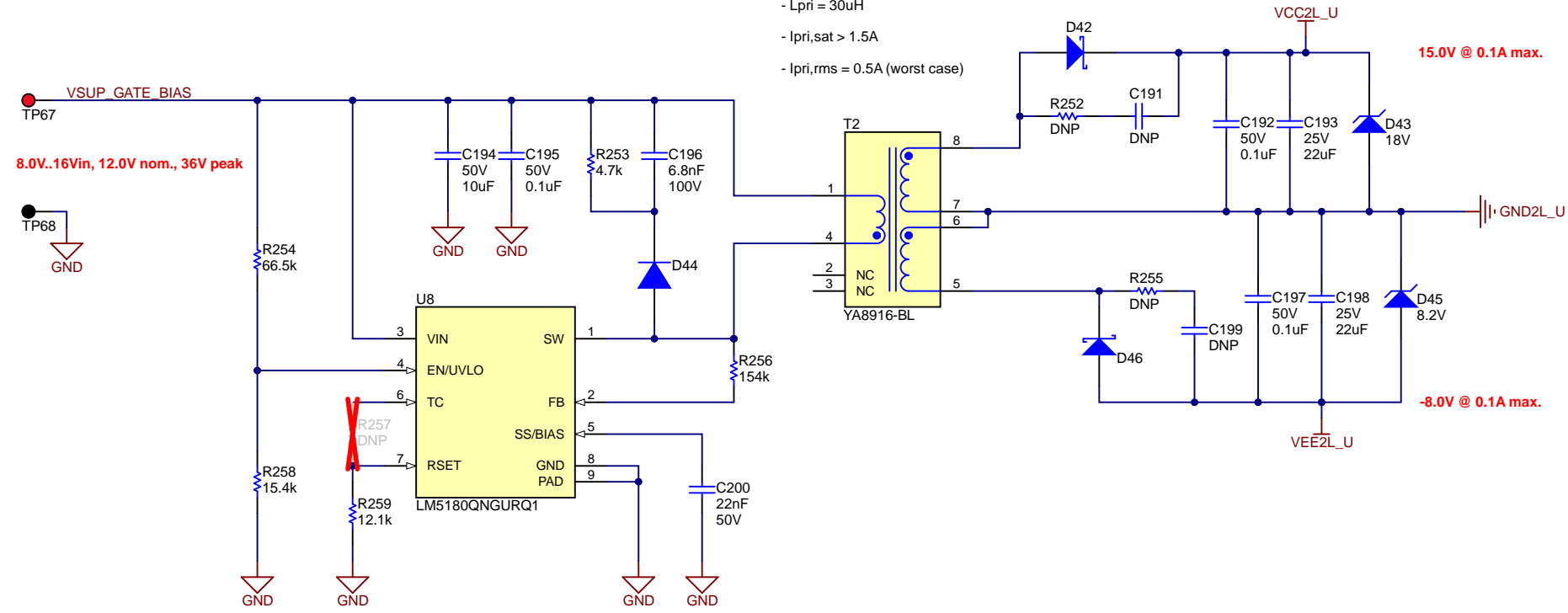


**Transformer specification**

- $N_p : N_{s1} : N_{s2} = 1 : 1 : 0.52$
- $L_{pri} = 30\mu H$
- $I_{pri,sat} > 1.5A$
- $I_{pri,rms} = 0.5A$  (worst case)

**CAUTION:**

Secondary switching slew rate (dv/dt) should not be too large when using a PSR Flyback converter as the parasitic interwindings capacitance can introduce significant common mode current on the primary, which can potentially lead to a shut down of the bias supply.



**Transformer specification**

- $N_p : N_{s1} : N_{s2} = 1 : 1 : 0.52$
- $L_{pri} = 30\mu H$
- $I_{pri,sat} > 1.5A$
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Orderable:	Designed for:	Mod. Date: 5/12/2023
TID #: N/A	Project Title: Gate Drive Board for IGBT HybridPack	
Number: PMP31236	Rev: A	Sheet Title: PMP30750_RevB
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 8 of 11
Drawn By:	File: PMP31236RevA_Supply_U.SchDoc	Size: B
Engineer: M Zehendner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	





Revision History	
Revision	Notes
A	* first draft

**Design Notes:**

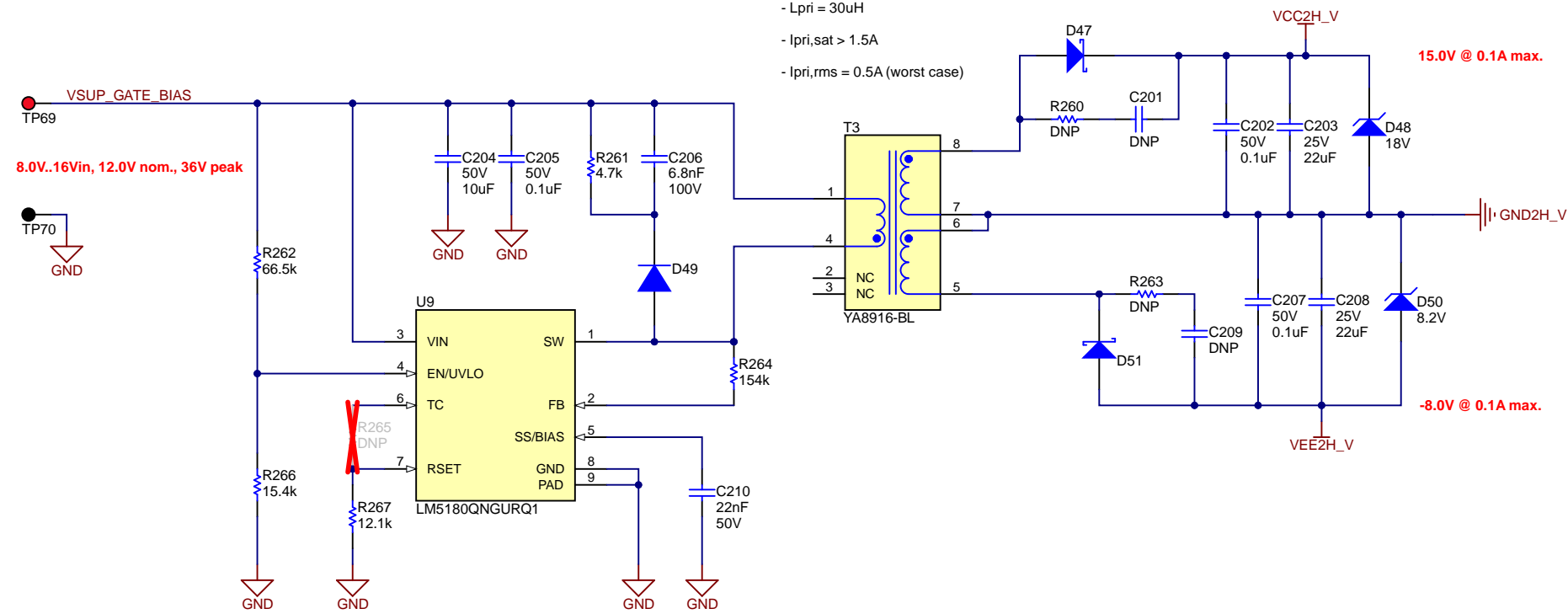
- D48 / D53 only needed for no load conditions
- Snubber networks need to be optimized in the lab
- DNP = Do Not Populate

**CAUTION:**

Secondary switching slew rate (dv/dt) should not be too large when using a PSR Flyback converter as the parasitic interwindings capacitance can introduce significant common mode current on the primary, which can potentially lead to a shut down of the bias supply.

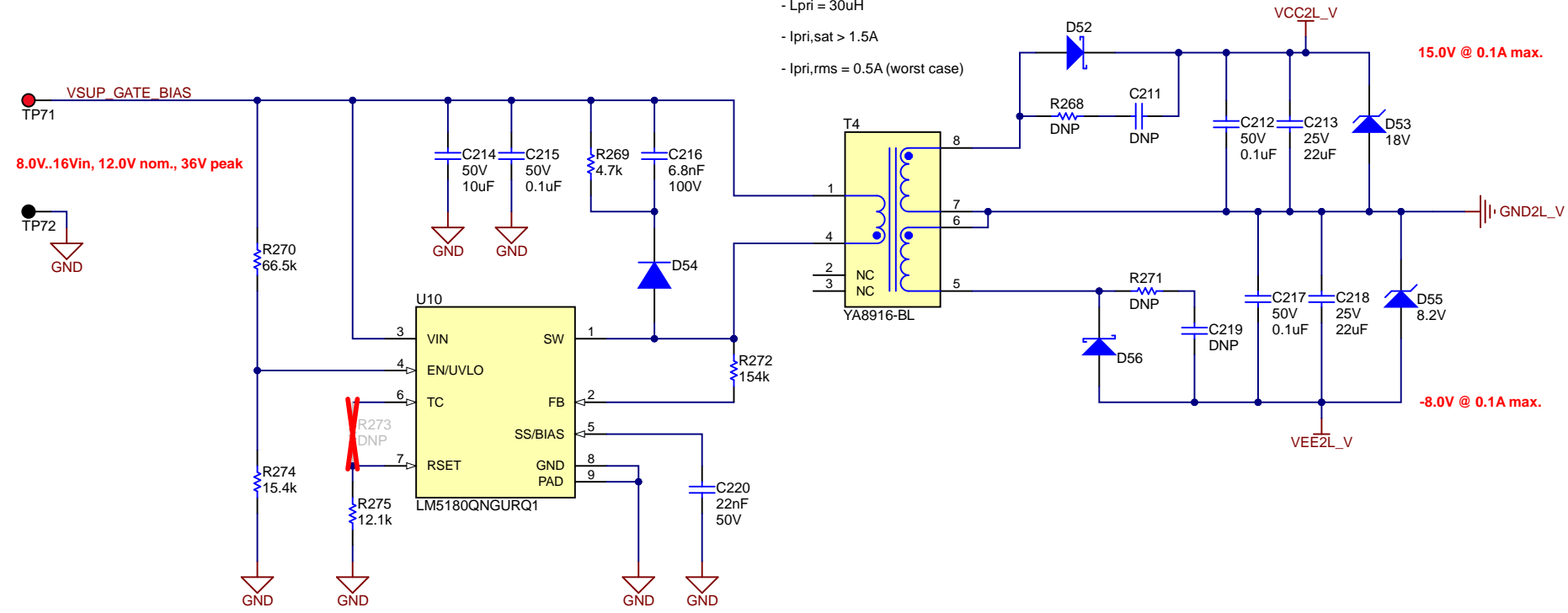
**Transformer specification**

- Np : Ns1 : Ns2 = 1 : 1 : 0.52
- Lpri = 30uH
- Ipri,sat > 1.5A
- Ipri,rms = 0.5A (worst case)



**Transformer specification**

- Np : Ns1 : Ns2 = 1 : 1 : 0.52
- Lpri = 30uH
- Ipri,sat > 1.5A
- Ipri,rms = 0.5A (worst case)



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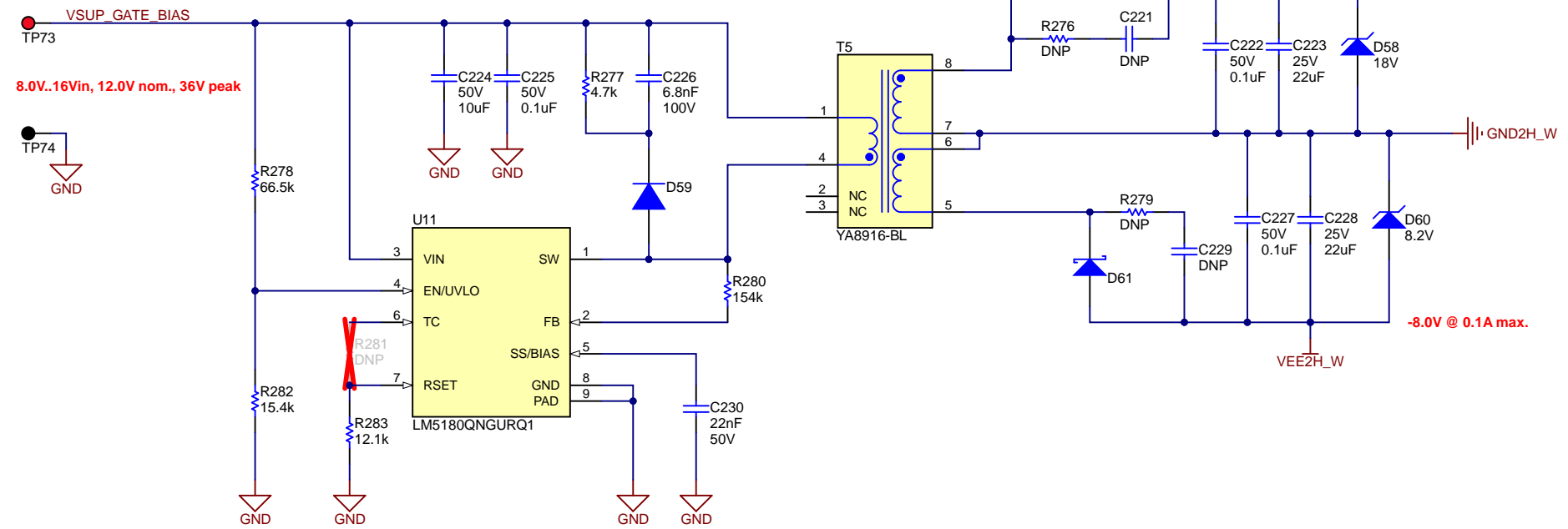
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Number: PMP31236	Rev: A	Sheet Title: PMP30750_RevB
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 9 of 11
Drawn By:	File: PMP31236RevA_Supply_V.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	



**Design Notes:**

- D58 / D63 only needed for no load conditions
- Snubber networks need to be optimized in the lab
- DNP = Do Not Populate

Revision History	
Revision	Notes
A	* first draft

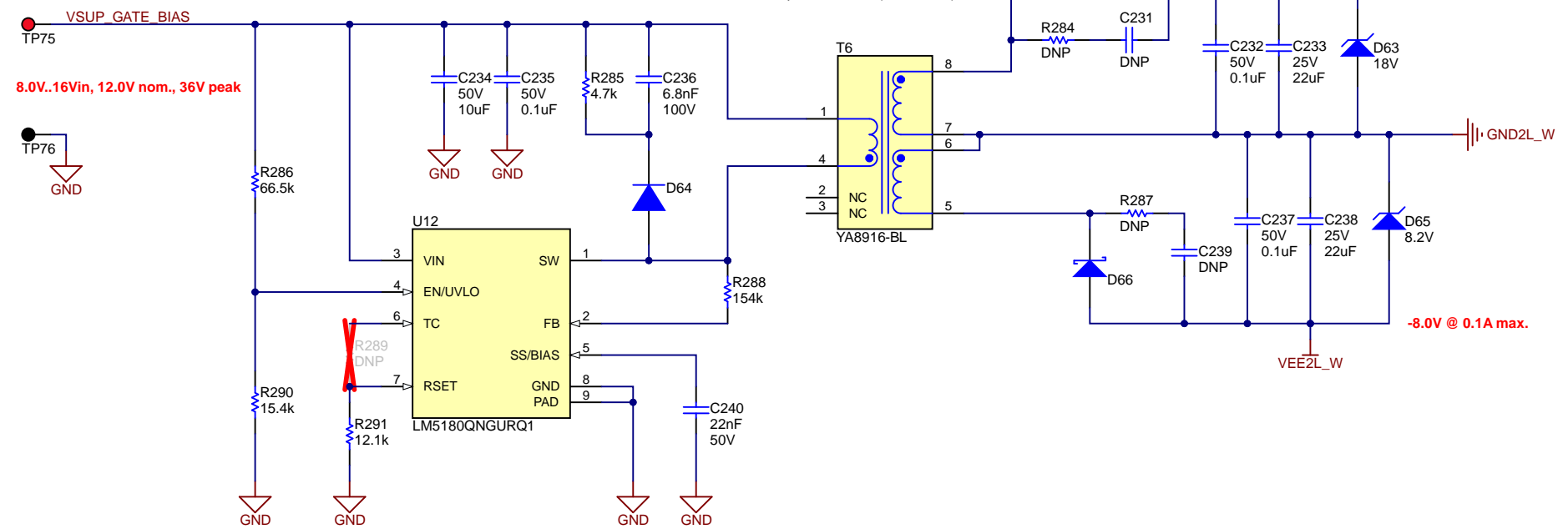


**Transformer specification**

- $N_p : N_{s1} : N_{s2} = 1 : 1 : 0.52$
- $L_{pri} = 30\mu H$
- $I_{pri,sat} > 1.5A$
- $I_{pri,rms} = 0.5A$  (worst case)

**CAUTION:**

Secondary switching slew rate (dv/dt) should not be too large when using a PSR Flyback converter as the parasitic interwindings capacitance can introduce significant common mode current on the primary, which can potentially lead to a shut down of the bias supply.



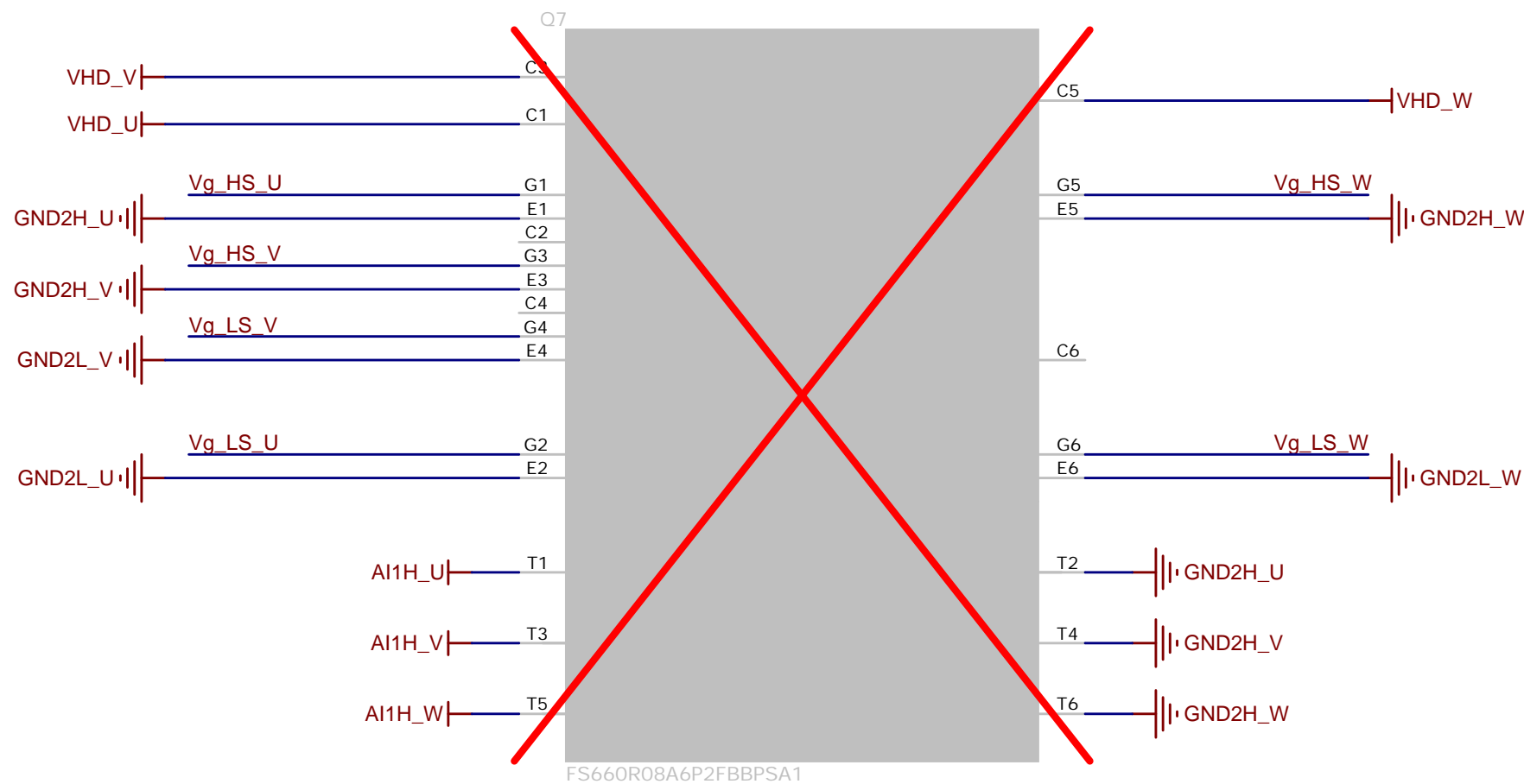
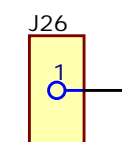
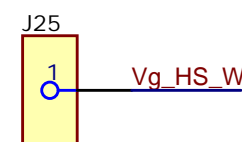
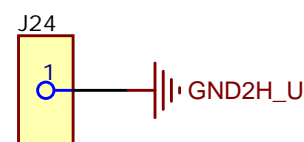
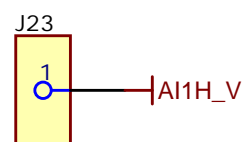
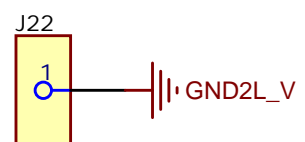
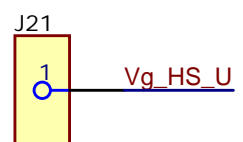
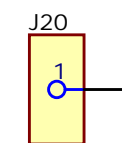
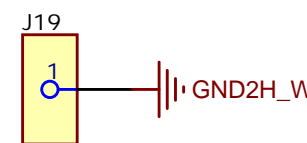
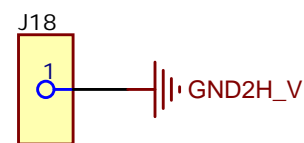
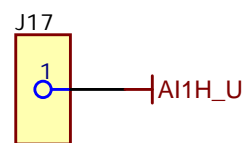
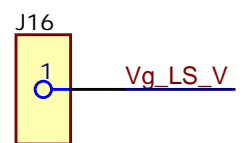
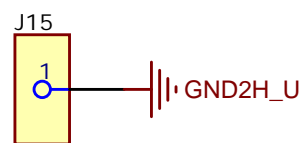
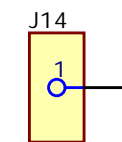
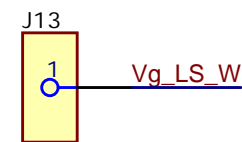
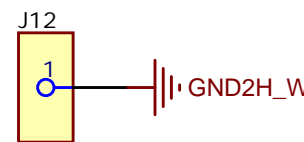
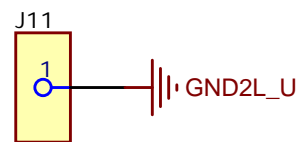
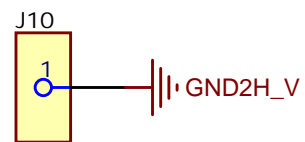
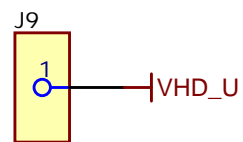
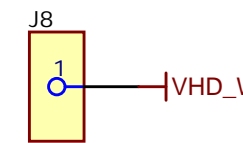
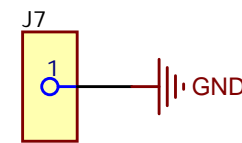
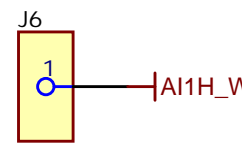
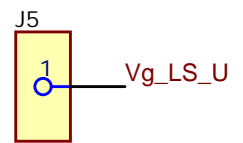
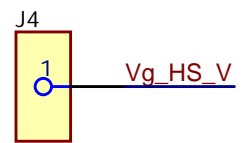
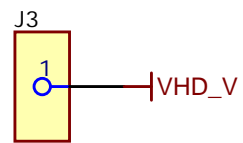
**Transformer specification**

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Number: PMP31236	Rev: A	Sheet Title: PMP30750_RevB
SVN Rev: Not in version control	Assembly Variant: Assembly PMP31236	Sheet: 10 of 11
Drawn By:	File: PMP31236RevA_Supply_W.SchDoc	Size: B
Engineer: M Zehndner	Contact: <a href="https://www.ti.com/support">https://www.ti.com/support</a>	





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Drawn By:	File: PMP31236RevA_IGBT_Module.SchDoc	Size: A4
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