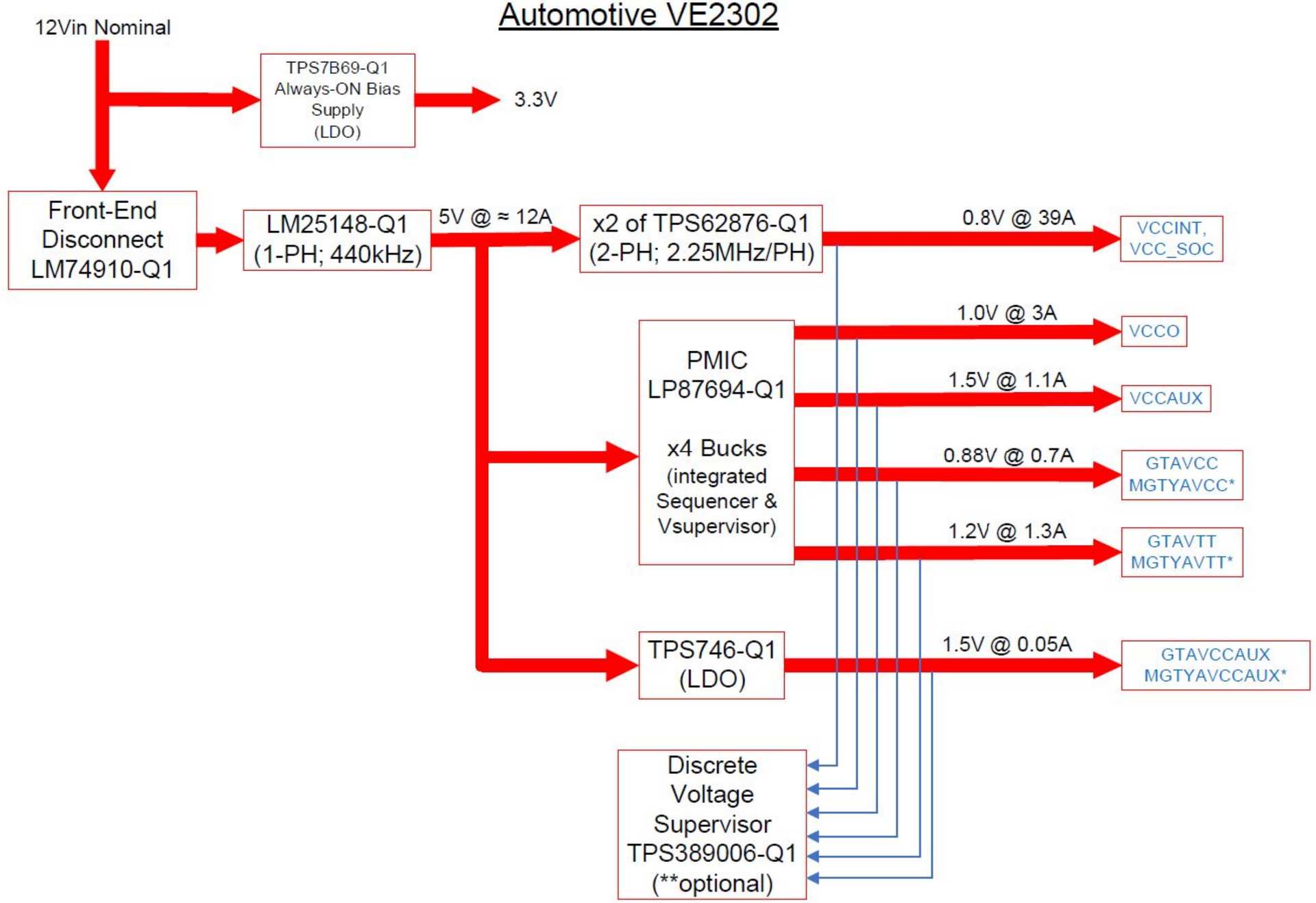
| Revision History | | | | |
|---|---|---|---|---|
| Rev | ECN # | Approved Date | Approved by | Notes |
| N/A | N/A | N/A | N/A | N/A |

# Automotive VE2302




NOTE: All or portions of these blocks may be used for the VE2202, as well as other Versal AI Edge platforms.

**Discrete voltage supervision option available as an alternative to that integrated in the PMIC: see schematic for details

*Only a part of VEK1752 platform.



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| Orderable: ChangeMe in variant | Designed for: | Mod. Date: 12/7/2023 |
| TID #: PMP23227 | Project Title: AMD Versal™ AI Edge Series Power Ref Design | |
| Number: PMP23227 Rev: -1 | Sheet Title: | |
| SVN Rev: Not in version control | Assembly Variant: 001 | Sheet: 1 of 5 |
| Drawn By: | File: PMP23227_Block Diagram.SchDoc | Size: B |
| Engineer: Hrag Kasparian | Contact: http://www.ti.com/support | |

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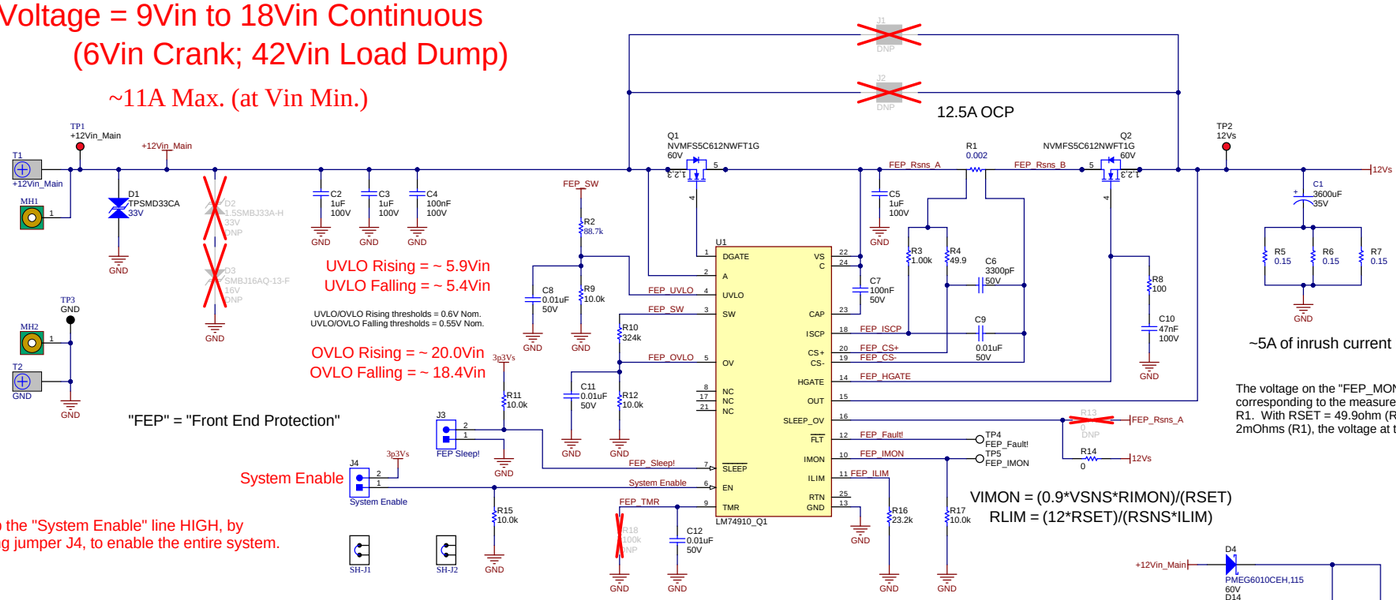
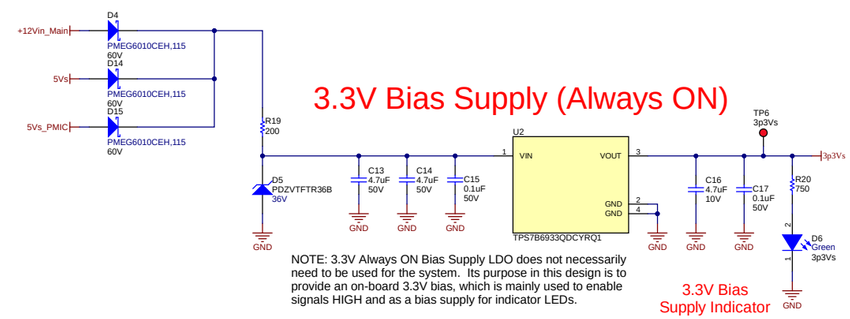
# Front-End Protection

Input Voltage = 9Vin to 18Vin Continuous
(6Vin Crank; 42Vin Load Dump)

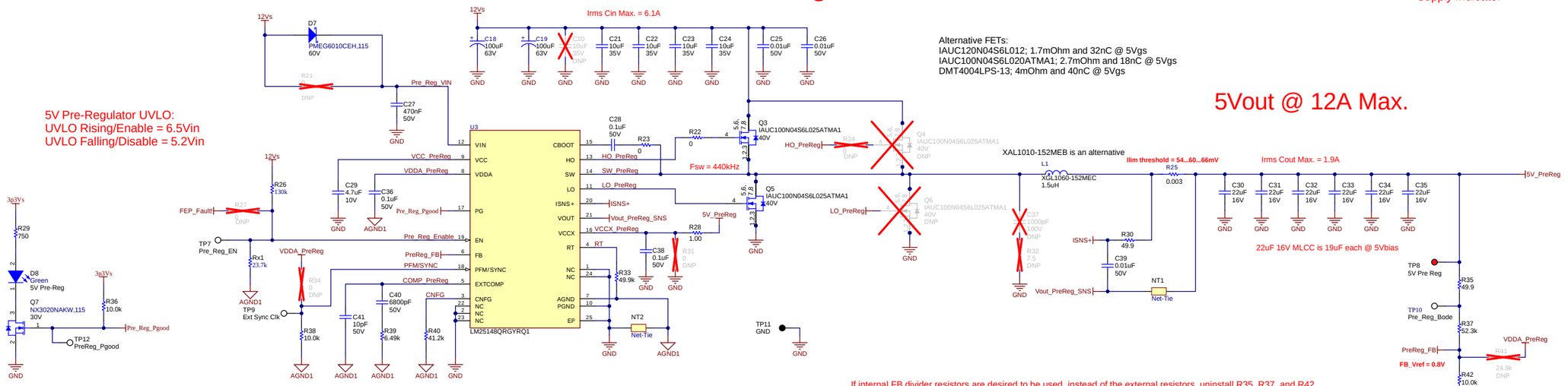
~11A Max. (at Vin Min.)




## 3.3V Bias Supply (Always ON)




# 12Vin to 5Vout Pre-Regulator




NOTE: There may be components in the design that may have higher voltage ratings, or other over-designed characteristics. This is due to a combination of availability of components, price, and other such factors. If other appropriately rated components are available and desired, then use those.

If internal FB divider resistors are desired to be used, instead of the external resistors, uninstall R35, R37, and R42, and follow the following instructions:

-Connect FB to VDDA via a 0 ohm resistor for R41, for 3.3Vout regulation using resistor dividers internal to the IC.

-Connect FB to VDDA via a 24.9k resistor for R41, for 5Vout regulation using resistor dividers internal to the IC.

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| Orderable: ChangeMe in variant | Designed for: Mod. Date: 12/6/2023 |
| TID #: PMP23227 | Project Title: AMD Versal™ AI Edge Series Power Ref Design |
| Number: PMP23227 Rev: -1 | Sheet Title: |
| SVN Rev: Not in version control | Assembly Variant: 001 Sheet: 2 of 5 |
| Drawn By: | File: PMP23227_Schematic_1.SchDoc Size: C |
| Engineer: Hrag Kasparian | Contact: http://www.ti.com/support |

# Automotive 0V70 Digital Rail

-To test the pre-regulator circuit independently, install J6 and J8 jumpers, and remove J7 and J9 jumpers.
-To bypass the on-board pre-regulator and use an outside power supply, remove J6 and J8 jumpers, and install J7, J9, and J11 jumpers. C43, R48 (and R49, if needed) are used to dampen the input from high input impedance usually caused by long leads connecting to an external power supply. These are not necessarily needed in the final solution, depending on the system setup.
[Use T3 and T4 (or MH3 and MH4 Metric 4 mounting holes) as the main terminals for supplying/loading for both cases.]

For normal, full-system operation, install J6, J7, J8 and J9, and remove J11, in order to allow the on-board pre-regulator output to supply the remaining rails.

Vcore
0V70 (Digital); VCCINT, VCC_PMC, VCC_PSFP, VCC_PSLP, VCC_CPM5*, VCC_RAM, VCC_GT, VCC_SOC, VCC_IO

0.8V/0.88V @ 39A
DC Spec. = ±1%
AC Spec. = ±17mV
Load Step = 33%
Seq. # 2

1. Alternatives for Rsns:
PS0612FKL070R001L
PS0612FKF070R001L

2. Current sense filter values selected using 1.15mm as length/width of Rsns gap and estimate of 5nH/cm for parasitic inductance of a length of wire (amounting here to about 0.6nH).

3. Current sense resistors R46 and R are only needed for testing current sharing during design evaluation. In a production run, R46 and R59 can be removed and directly connect the inductors to the output capacitors. Also, J5, J12, R43, R44, R55, R56, C42, and C68 can be removed.

J10 is a shielded connector for measuring output voltage

Default Vcore = 0.8V

Default ADDRESS for 0.8V output is 0x44

Inductor Alternatives

Inductor Alternatives

I2C interface communication with USB2ANY:
VBUS is not required to be connected
USB2ANY interface has an internal 3.3V VBUS supply

USB2ANY comunication interface connector

On-Board Load Stepper Operation Guide:

1. In order to perform a load transient test using the on-board load stepper, enable the circuit by shunting jumper J14. The timing for this is acheived using a 555 timer IC is configured in astable operation mode. The load step pulse lasts approximately 0.5ms and will repeat approximately every 1 second.

2. If an external load step pulse signal is desired to be used, shunt the J14 jumper, to power the circuit, and connect the external pulse signal to the "TP19" testpoint, referenced to GND on "TP20". Make sure to NOT run the load step pulse longer than the peak and average power ratings of the load resistors and the SOA of the installed FETs. If driving 120A of load step current try not to exceed 1ms pulse time. Do NOT allow the HIGH level voltage exceed 5V. See LM5112 datasheet for rising/falling thresholds of the "IN" pin (i.e. Pin 4).

3. The two potentiometers, R65 and R72, are used to control the rising and falling load step current slew rates, respectively. Install/short J15 jumper to achieve fastest possible rise and fall slew rates. This will be limited by the parasitic inductance of the copper traces and polygons of the board.

## On-Board Core Rail Output Load Transient Stepper

0.8V Default Vout

Connect load to these set of terminals.

T5 and T6 are screw-type terminal lugs, while MH5 and MH6 are metric 4 (i.e. M4) mounting holes.

May also use LMC555CM/NOPB

***60mOhm load/sense resistor provides about 33% Load Step (~ 13.2A) with Vout set to 0.8V -->***
***With R104 (0.06 Ohm) installed, the scale for current sensing will be 60mV/A. -->***

*NOTES:

1. The load step currents mentioned also take into account the Rds_ON resistance of the two, paralleled load step FETs, which have about 1.25mOhms each.

2. Current sense resistor PCB footprint accommodations have been made for the following sizes (Imperial units), as well as some other sizes in between: 1206 WIDE, 2512 WIDE, 2827 WIDE, 4320 WIDE, 5929 WIDE

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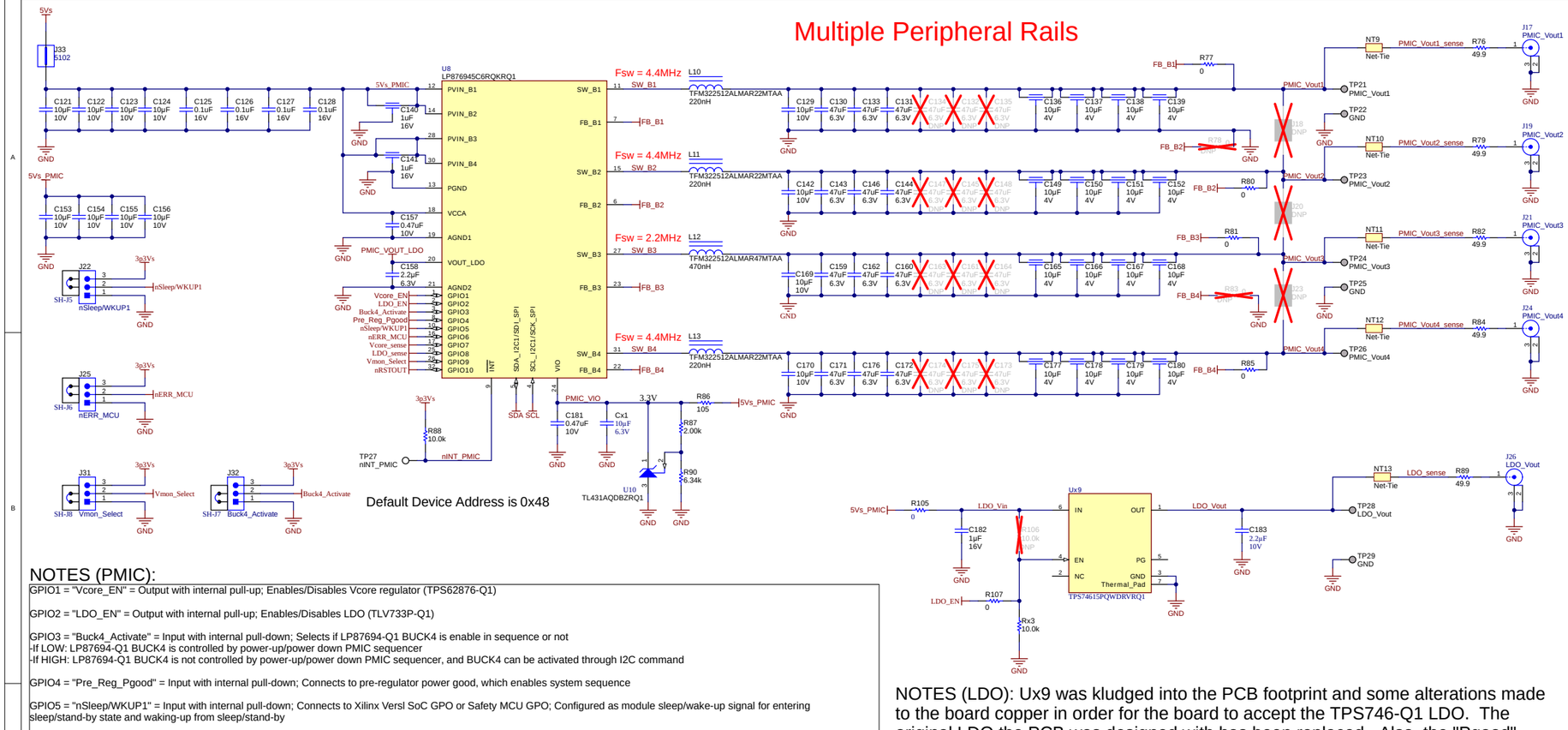
| Orderable: ChangeMe in variant | | Designed for: | Mod. Date: 12/6/2023 |
| TID #: PMP23227 | | Project Title: AMD Versal™ AI Edge Series Power Ref Design | |
| Number: PMP23227 | Rev: -1 | Sheet Title: | |
| SVN Rev: Not in version control | | Assembly Variant: 001 | Sheet: 3 of 5 |
| Drawn By: | | File: PMP23227_Schematic_2.SchDoc | Size: C |
| Engineer: Hrag Kasparian | | Contact: http://www.ti.com/support | |

# Multiple Peripheral Rails




PMIC_Vout1
VCCO_HDIO/XPIO
1.0V @ 3A
DC Spec. = ±1%
AC Spec. = ±5%
Load Step = 100%
Seq. # 1

PMIC_Vout2
VCCAUX, VCCAUX_PMC, VCCAUX_SMON
1V5 (Digital)
1.5V @ 1.1A
DC Spec. = ±1%
AC Spec. = ±2%
Load Step = 100%
Seq. # 3

PMIC_Vout3
GTAVCC
0V88 (Analog)
0.88V @ 0.7A
DC Spec. = ±2%
AC Spec. = 10mVpp
Load Step = 70%
Seq. # 4

PMIC_Vout4
GTAVTT, MGTYAVTT
1V2 (Analog)
1.2V @ 1.3A
DC Spec. = ±2%
AC Spec. = 10mVpp
Load Step = 70%
Seq. # 6

LDO_Vout
GTAVCCAUX or MGTYAVCCAUX
1V5 (Analog)
1.5V @ 0.05A
DC Spec. = ±2%
AC Spec. = 10mVpp
Load Step = 70%
Seq. # 5

Key

Schematic Rail Name
Xilinx Rail Name
Output Voltage @ Current
Output Voltage DC Spec.
Output Voltage AC Spec.
Output Load Step
Sequence Stage Number

## NOTES (PMIC):

GPIO1 = "Vcore_EN" = Output with internal pull-up; Enables/Disables Vcore regulator (TPS62876-Q1)

GPIO2 = "LDO_EN" = Output with internal pull-up; Enables/Disables LDO (TLV733P-Q1)

GPIO3 = "Buck4_Activate" = Input with internal pull-down; Selects if LP87694-Q1 BUCK4 is enable in sequence or not
-If LOW: LP87694-Q1 BUCK4 is controlled by power-up/power down PMIC sequencer
-If HIGH: LP87694-Q1 BUCK4 is not controlled by power-up/power down PMIC sequencer, and BUCK4 can be activated through I2C command

GPIO4 = "Pre_Reg_Pgood" = Input with internal pull-down; Connects to pre-regulator power good, which enables system sequence

GPIO5 = "nSleep/WKUP1" = Input with internal pull-down; Connects to Xilinx Versl SoC GPO or Safety MCU GPO; Configured as module sleep/wake-up signal for entering sleep/stand-by state and waking-up from sleep/stand-by

GPIO6 = "nERR_MCU" = Input with internal pull-down; Connects to "ERROR_OUT" of Xilinx SoC

GPIO7 = "Vcore_sense" = Voltage sense input configured as VMON1 UV/OV monitoring to monitor TPS62876-Q1 VOUT and measures the "Vcore" voltage

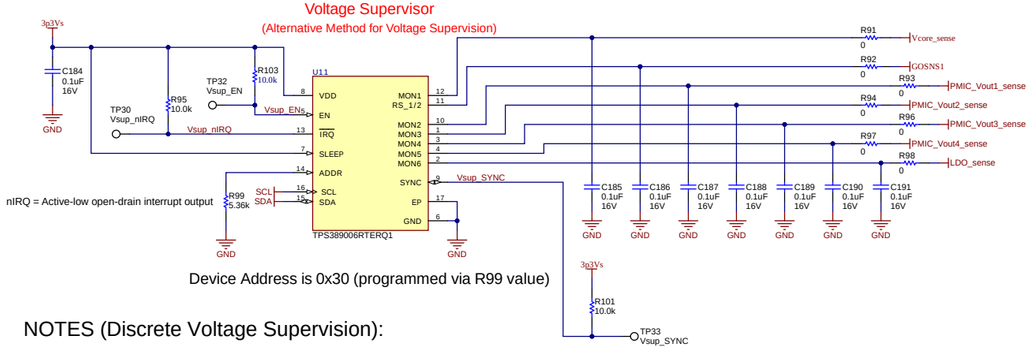
GPIO8 = "LDO_Vout" = Voltage sense input configured as VMON2 UV/OV monitoring to monitor TLV733P-Q1 VOUTConnects to and measures the "LDO_Vout" voltage

GPIO9 = "Vmon_Select" = Input; Configures VMON type select input for TPS62876-Q1 (Vcore) rail
-If LOW: LP8769-Q1 VMON1 is used (as mapped to LP8769-Q1 GPIO7)
-If HIGH: External discrete VMON is used (this is needed only when differential voltage monitoring is required to achieve accurate remote sensing of the SoC core rail. This becomes especially important for high current SoC Core rail applications)
*for example, the "nIRQ" output of the discrete voltage supervisor can be connected to a GPIO of the PMIC that is programmed as one of the input sourece for "nRSTOUT" signal generation
*another example of using the discrete voltage supervisor is to gang/tie together its open-drain "nIRQ" output with the "nRSTOUT" output of the PMIC

GPIO10 = "nRSTOUT" = Open-drain output; Configured as "NRSTOUT" output that is connected to Xilinx Versal SoC reset input

## Voltage Supervisor

(Alternative Method for Voltage Supervision)




Device Address is 0x30 (programmed via R99 value)

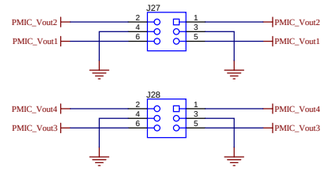
## NOTES (Discrete Voltage Supervision):

1. Voltage supervision is currently set up to be performed by LP87694-Q1, which has integrated voltage supervision capabilities. If a dedicated voltage supervisor is desired, the TPS389006-Q1 can be used. One benefit of using the TPS389006-Q1 is that the core rail output voltage can potentially be monitored more precisely, using differential voltage sensing, due to its dedicated GND sense on the MON1 channel (i.e. Pin 11).
2. Device I2C address is programmed via the R99 value. See TPS389006-Q1datasheet for details.
3. Please contact the voltage supervisors product line for precise device variant used for board testing.

## NOTES (LDO):

Ux9 was kludged into the PCB footprint and some alterations made to the board copper in order for the board to accept the TPS746-Q1 LDO. The original LDO the PCB was designed with has been replaced. Also, the "Pgood" output of the new LDO has not been routed out, but can easily be done on final design using a pullup resistor connected to an acceptable positive voltage rail.

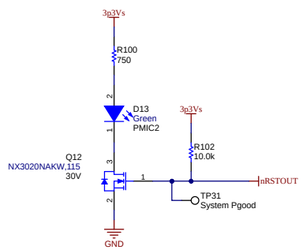
## High dI/dt Power Connectors




Install J29 (along with J18, J20, J23) if a single-output, 4-phase configuration is desired for the PMIC.

## NOTES (Sequencing):

Currently the LP87694-Q1 performs the sequencing for all system rails, via the programmable GPIOs. If a dedicated, programmable sequencer is desired, one option is the TPS38700-Q1.




## NOTES (General):

1. All components that have an "-x" in their designator signify components that were not part of the original design. These have been kludged onto the board, since the PCB does not have the appropriate footprints to accommodate them.
2. J27 and J28 have been placed to be used with a load stepper board that can be found at the following link: https://www.ti.com/tool/PMICLOADBOARDEVM. However, this tool is not absolutely needed for evaluating the circuit.

H1 1 NY PMS 440 0025 PH

H2 1 NY PMS 440 0025 PH

H3 1 NY PMS 440 0025 PH

H4 1 NY PMS 440 0025 PH

H5 1902C

H6 1902C

H7 1902C

H8 1902C

FID1 FID2 FID3

PCB Number: PMP23227
PCB Rev: B

CE Mark

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

LBL1
PCB Label
THT-14-423-10
Size: 0.65" x 0.20 "

| Variant/Label Table | |
|---|---|
| Variant | Label Text |
| 001 | |
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| Orderable: ChangeMe in variant | | Designed for: | Mod. Date: 3/13/2024 |
| TID #: PMP23227 | | Project Title: AMD Versal™ AI Edge Series Power Ref Design | |
| Number: PMP23227 | Rev: -1 | Sheet Title: | |
| SVN Rev: Not in version control | | Assembly Variant: 001 | Sheet: 5 of 5 |
| Drawn By: | | File: PMP23227_Hardware.SchDoc | Size: B |
| Engineer: Hrag Kasparian | | Contact: http://www.ti.com/support | |

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