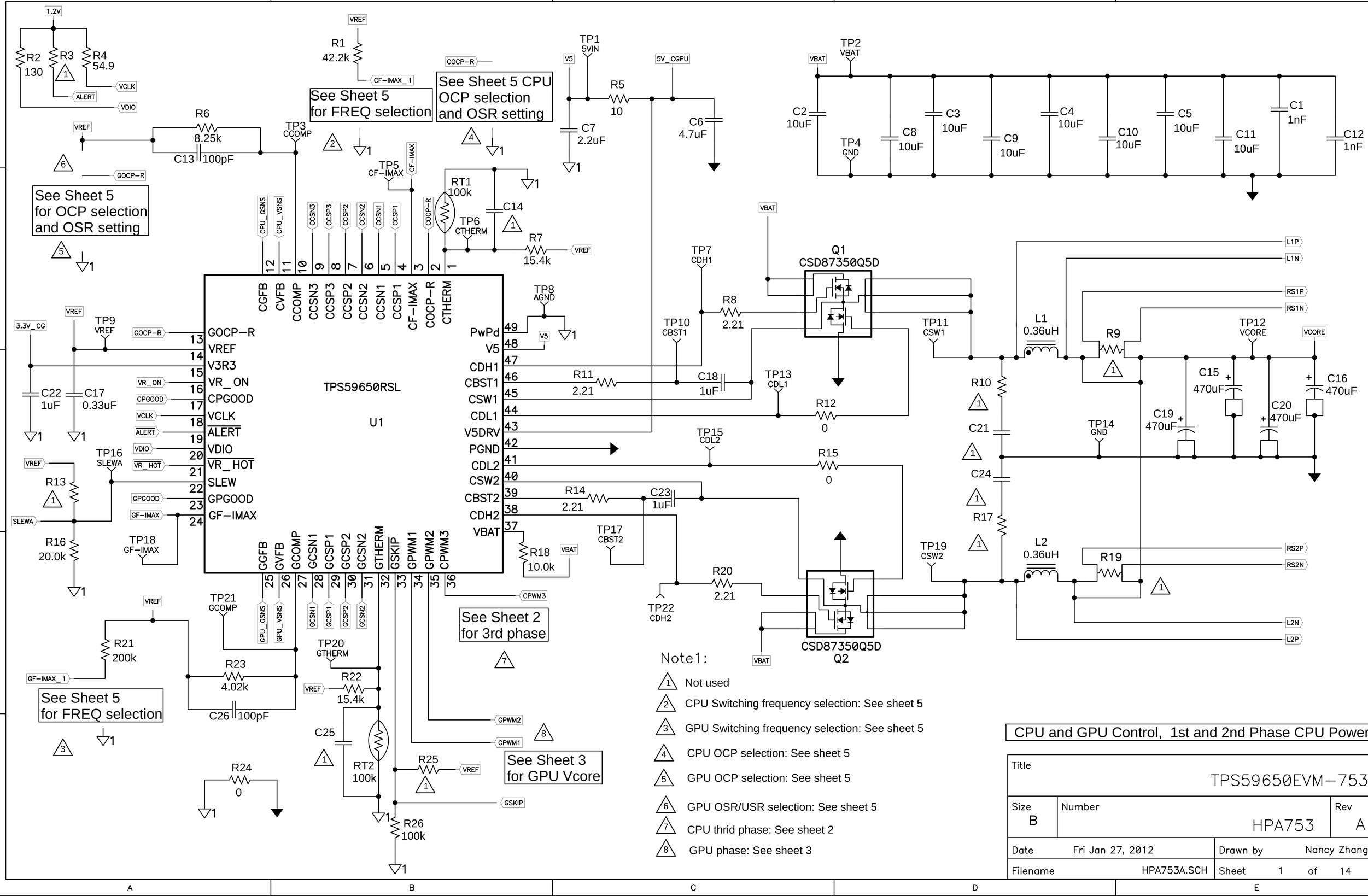

TPS59650RSL
U1
CSD87350Q5D
Q2
Q1
CSD87350Q5D
See Sheet 5 for FREQ selection
See Sheet 5 for OCP selection and OSR setting
See Sheet 5 for FREQ selection
See Sheet 5 CPU OCP selection and OSR setting
See Sheet 2 for 3rd phase
See Sheet 3 for GPU Vcore
Note1:
1 Not used
2 CPU Switching frequency selection: See sheet 5
3 GPU Switching frequency selection: See sheet 5
4 CPU OCP selection: See sheet 5
5 GPU OCP selection: See sheet 5
6 GPU OSR/USR selection: See sheet 5
7 CPU thrid phase: See sheet 2
8 GPU phase: See sheet 3
CPU and GPU Control, 1st and 2nd Phase CPU Power
Title
TPS59650EVM–753
Size B
Number HPA753
Rev A
Date Fri Jan 27, 2012
Drawn by Nancy Zhang
Filename HPA753A.SCH
Sheet 1 of 14

TP23
VBAT

TP24
GND

C27 10uF
C28 10uF
C29 10uF
C30 10uF
C31 1nF

VBAT

TP26
CBST3

TP25
CDRVH3

TP27
CSW3

Q3
CSD87350Q5D

L3P
L3N
RS3P
RS3N

R27
1

VCORE

R29 2.21
C33 1uF
R28 2.21

0.36uH
L3

R30
1

C35
1

C32
1

C34
1

TP29
CPWM

U2
TPS51601ADRB

| | | | |
|---|---|---|---|
| 1 | BST | DRVH | 8 |
| 2 | SKIP | LL | 7 |
| 3 | PWM | VDD | 6 |
| 4 | GND | DRVL | 5 |
| | PwPd | | 9 |

5V_CGPU
CPWM3
5V_CGPU

TP28
CDRVL3

R31
0

C36
2.2uF

C37 22uF
C38 22uF
C39 22uF
C40 22uF
C41 22uF
C42 22uF
C43 22uF
C44 10uF
C45 22uF
C46 10uF
C47 1
C48 1
C49 22uF
C50 22uF
C51 22uF
C52 22uF
C53 22uF
C54 22uF
C55 22uF
C56 22uF
C57 10uF
C58 10uF
C59 10uF
C60 10uF
C61 10uF
C62 10uF
C63 10uF
C64 10uF

VCORE

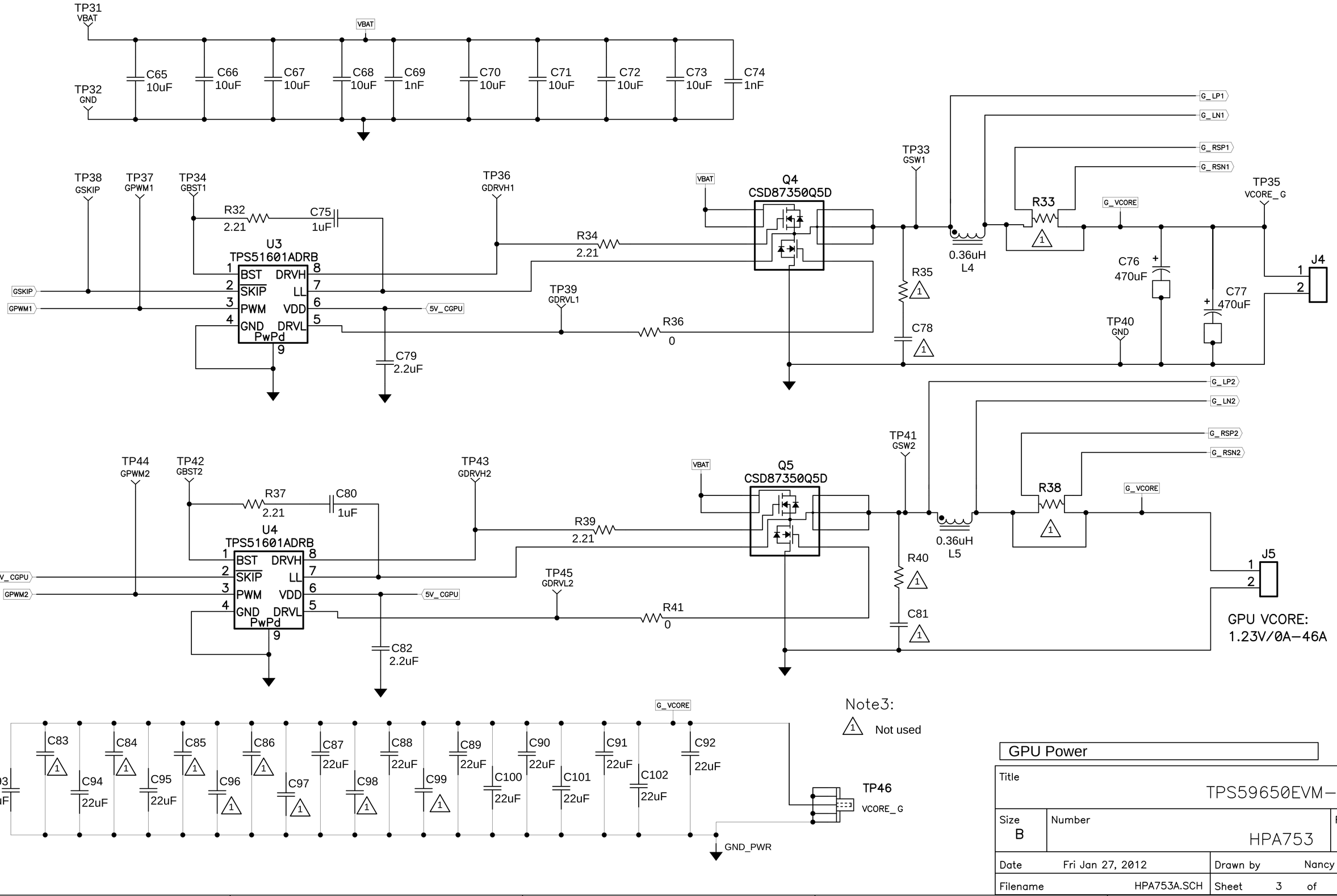
J1
J2
J3
CPU VCORE:
1.05V/0A–94A

TP30
VCORE_C

Note2:
1 Not used

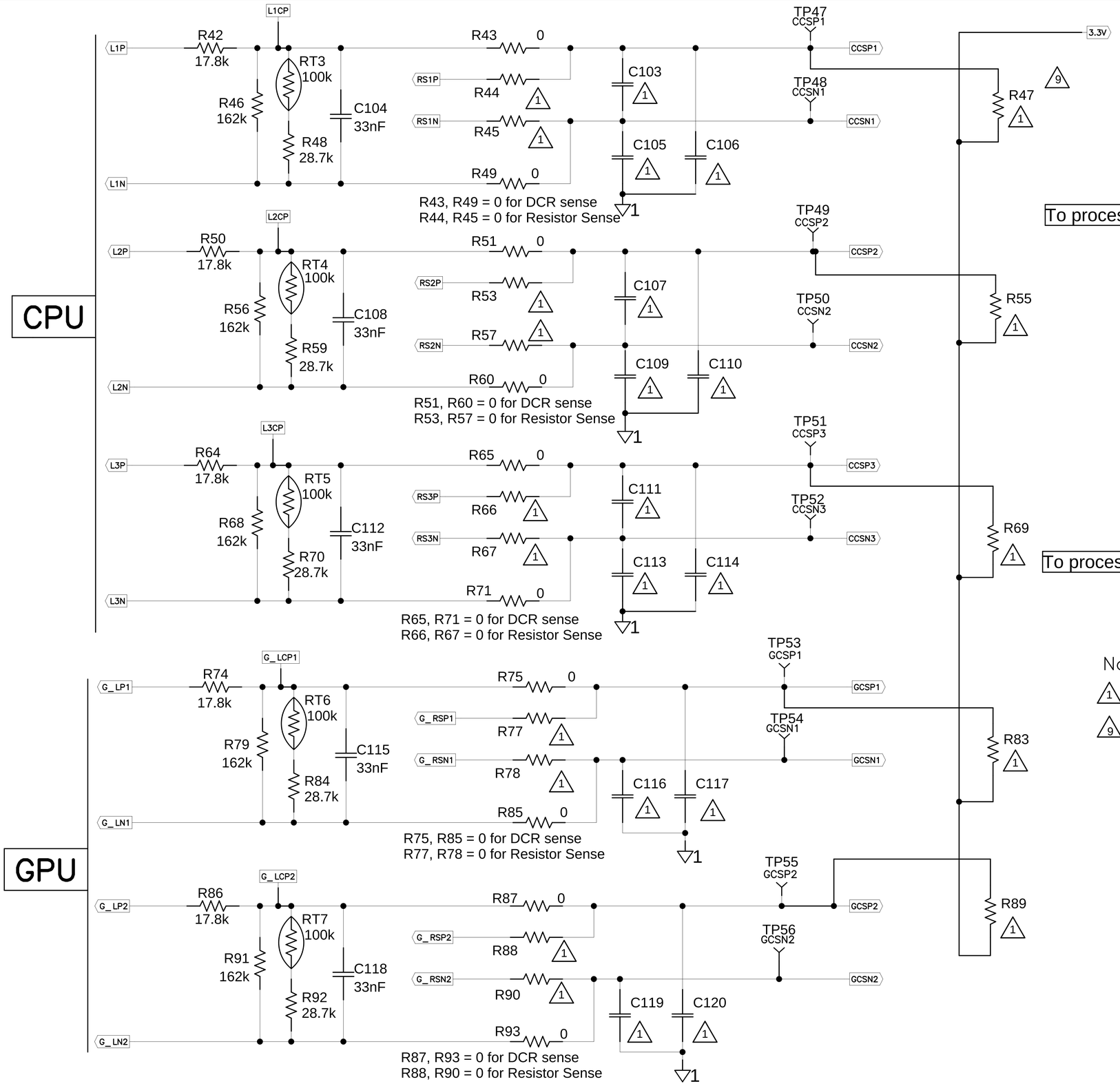
CPU 3rd Phase Power

| | | |
|---|---|---|
| Title | TPS59650EVM–753 | |
| Size B | Number HPA753 | Rev A |
| Date Fri Jan 27, 2012 | Drawn by Nancy Zhang | |
| Filename HPA753A.SCH | Sheet 2 of 14 | |




GPU Power

| | | |
|---|---|---|
| Title | TPS59650EVM–753 | |
| Size B | Number HPA753 | Rev A |
| Date Fri Jan 27, 2012 | Drawn by Nancy Zhang | |
| Filename HPA753A.SCH | Sheet 3 of 14 | |




Note4:

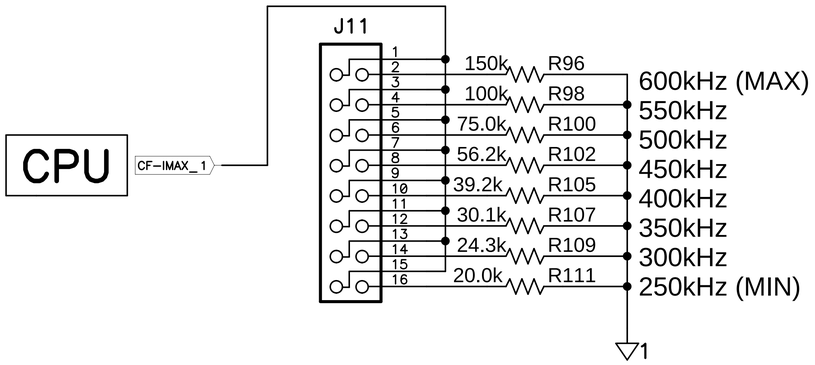
1. Not used
2. A phase can be disabled by pulling the corresponding xCSPx pin to 3.3V.
   Default setting for CPU: 3 phase operation
   Dafault setting for GPU: 2 phase operation
   CPU:
   Phase disable can be done in reverse order.Phase 3, then 2, then 1.
   1. CPU 3 Phase operation: R47, R55, R69 open
   2. CPU 2 Phase operation: R69 used 0ohm
   3. CPU 1 Phase operation: R47, R55 used 0ohm

   GPU:
   1. GPU 2 Phase operation: R83, R89 open
   2. GPU 1 Phase operation: R89 used 0ohm

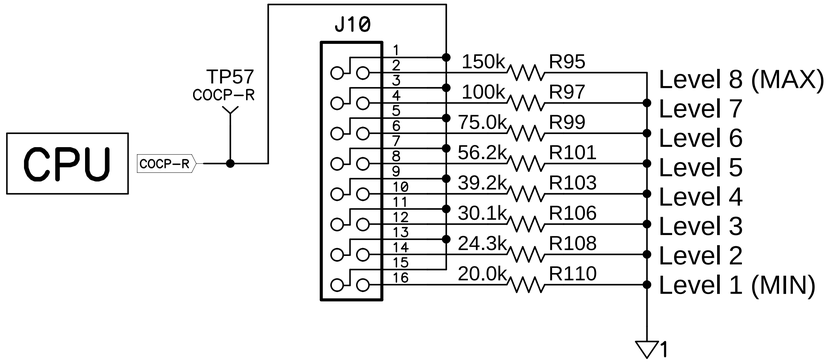
Current Feedback Selection and Filtering
Differential Voltage Feedback and termination

| | | |
|---|---|---|
| Title: TPS59650EVM–753 | | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | | Drawn by: Nancy Zhang |
| Filename: HPA753A.SCH | | Sheet 4 of 14 |

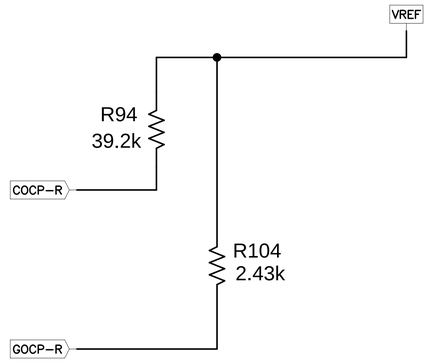
## ⚠10 SWITCHING FREQUENCY SELECTION

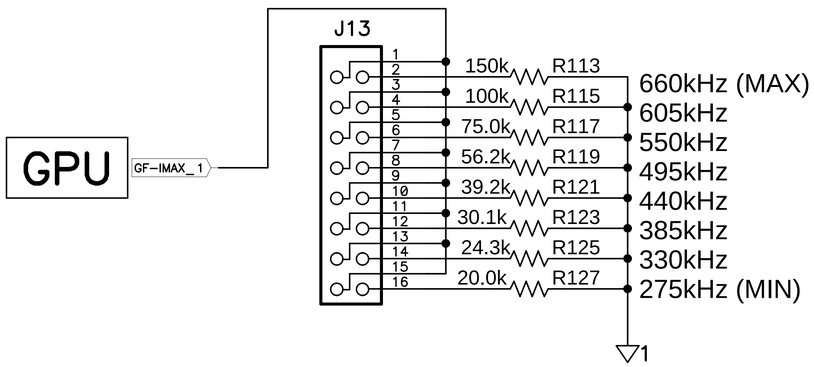


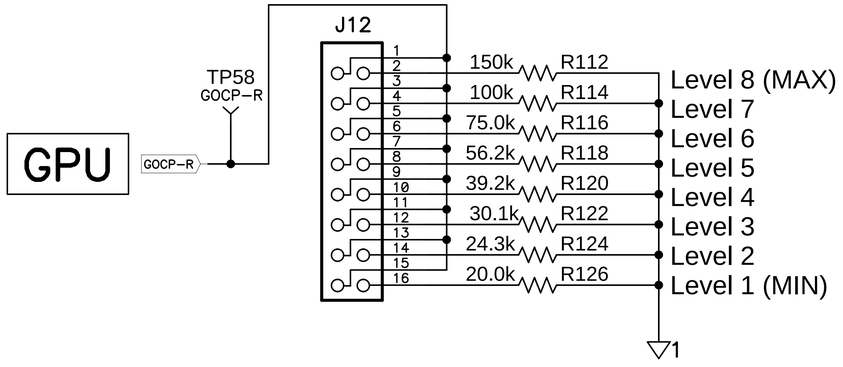

## ⚠11 OVER-CURRENT PROTECTION SELECTION

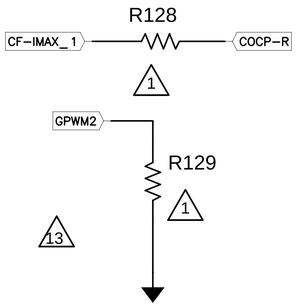



## ⚠12 OSR / USR SETTING




Note5:

⚠1 Not used

⚠10 Switching Frequency Selection:
1. CPU Switching Frequency Default Setting: Jumper shorts on pin13 and pin14 to set 300kHz
2. GPU Switching Frequency Default Setting: Jumper shorts on pin 11 and pin12 to set 385kHz

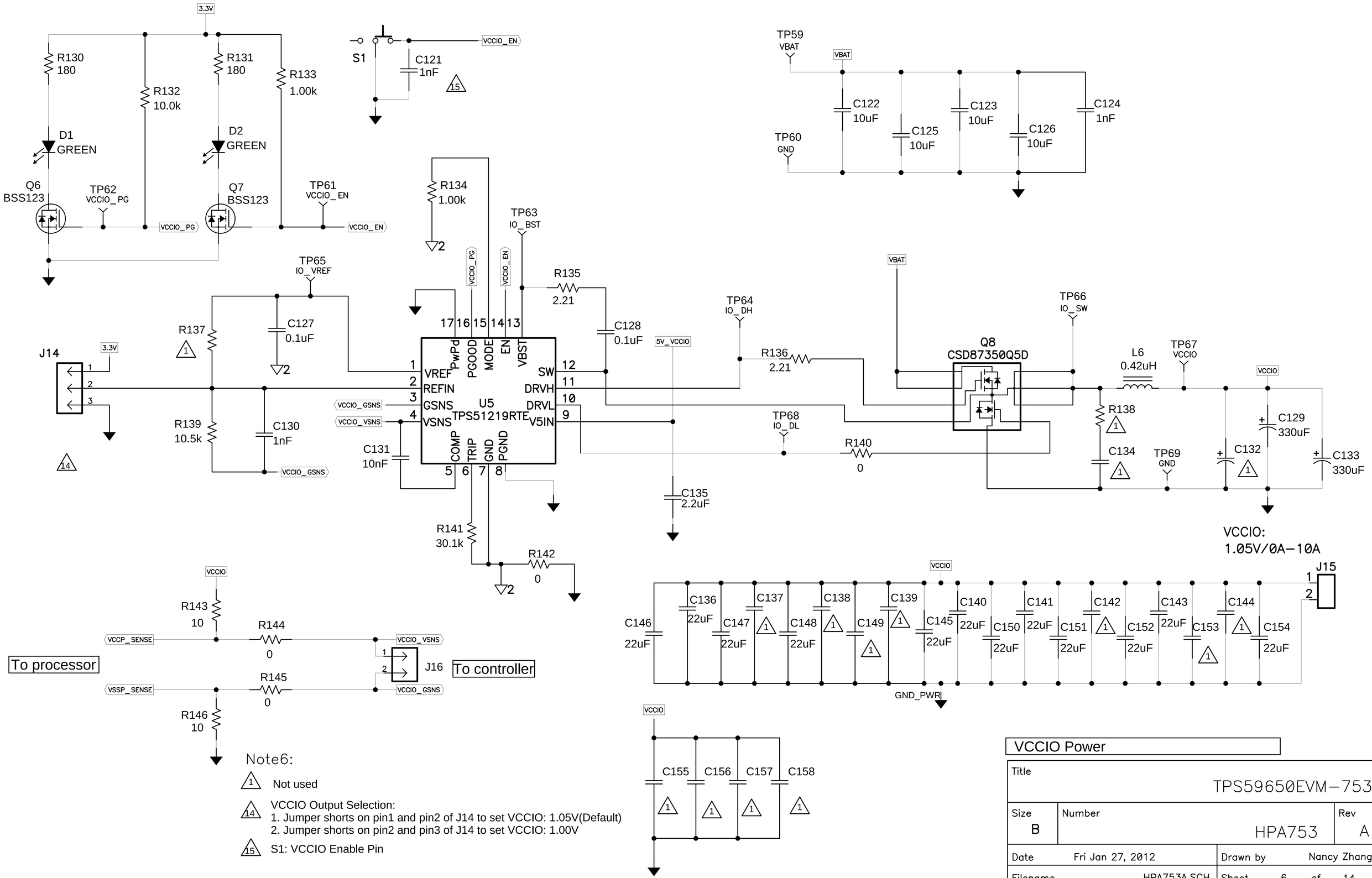
⚠11 Over Current Protection Selection:
1. CPU Over Current Protection Per Phase Default Setting: Jumper shorts on pin 7 and pin 8 to level 5 (set 40A)
2. GPU Over Current Protection Per Phase Default Setting: Jumper shorts on pin 7 and pin 8 to level 5 (set 40A)

⚠12 Over-Shoot /Under-Shoot Reduction Selection:
1. CPU OSR/USR Default Setting: OSR/USR Reduction middle level
2. GPU OSR/USR Default Setting: OSR/USR Reduction off

⚠13 Optional parts for using TPS51640

Frequency and OCP SELECTIONS for CPU and GPU

| | | |
|---|---|---|
| Title: TPS59650EVM-753 | | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet: 5 of 14 | |

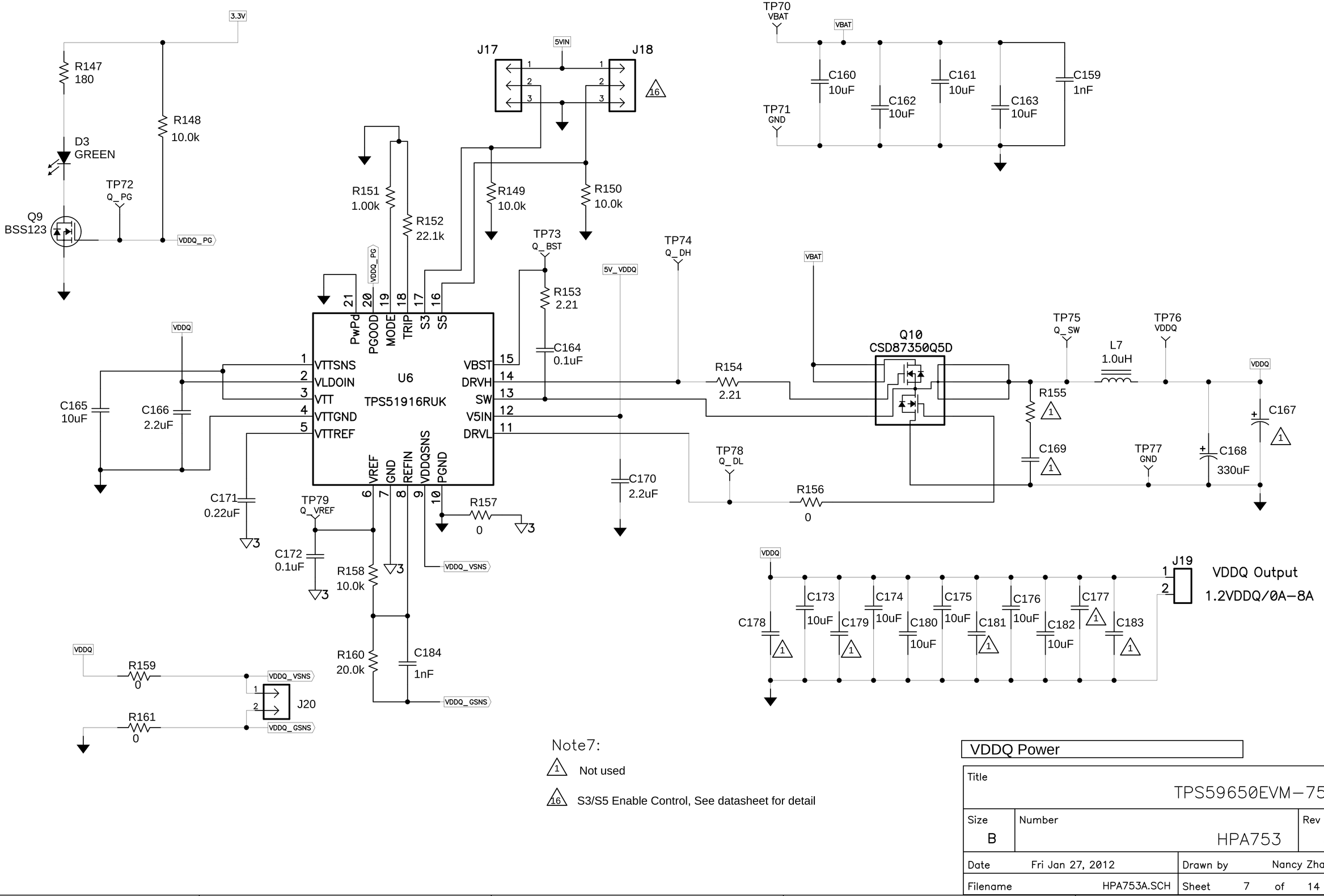



Note6:

1. Not used
14. VCCIO Output Selection:
    1. Jumper shorts on pin1 and pin2 of J14 to set VCCIO: 1.05V(Default)
    2. Jumper shorts on pin2 and pin3 of J14 to set VCCIO: 1.00V
15. S1: VCCIO Enable Pin

VCCIO Power

| | | |
|---|---|---|
| Title | TPS59650EVM–753 | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet 6 of 14 | |




Note7:

1 Not used

16 S3/S5 Enable Control, See datasheet for detail

VDDQ Power

| | | |
|---|---|---|
| Title | TPS59650EVM-753 | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet 7 of 14 | |

VBAT Conversion Voltage Input:
9V -20V

VBAT
J21
C187
C186
TP82 VBAT
TP84 GND

TP87 5V_IO
TP86 5V_Q
TP88 5V_CG
5V_VCCIO
5V_VDDQ
5V_CGPU
R169 1
R170 1
R171 1
J22
5VIN

5V Bias
Voltage Input

Silk:
VCCIO_DL
GFX_DL
CPU_DL1
CPU_DL2

TP81 5VIN
5VIN
C188 0.1uF
C189 10uF
TP83 GND
R162 100k
PGD_1

1.8V LDO
U7
TPS70102PWP
NC VIN1 VIN1 MR2 MR1 ENABLE SEQUENCE GND VIN2 VIN2 PwrPad
NC VOUT1 VOUT1 VSENSE1 PGD_1 RESET VSENSE2 VOUT2 VOUT2 NC
TP80 1.8V
R163 15.0k
R165 30.1k
C185 10uF
R164 2.00k
3.3V
RESET
R166 30.1k
C190 0.1uF
R167 51.1k
TP85 3.3V
C191 10uF
R168 1
3.3V_CG

3.3V LDO

Note8:

1 Not used

17 VCCIO, GPU and CPU Dynamic Load:
1. Switch to "ON" position to enable the Dynamic Load
2. Switch to "OFF" position to disable the Dynamic Load (Default)

18 J23: Default setting: Jumper shorts on to
Enable on board dynamic load

1.2V LDO
U8
TPS71712DCK
IN GND EN OUT NR/FB
150mA LDO
TP89 1.2V
C192 0.1uF
C193 2.2 uF
C194 0.01uF

VCORE
R172 0.01
R173 0.01
R174 0.05
R175 0.05

VCCIO
G_VCORE
R177 0.05
R179 0.05
R178 0.01
R180 0.05
Q11 CSD16407Q5
Q12 CSD16407Q5
TP91 DYN_C
TP92 GND
C195 1uF
R181 0.005

R182 8.06k
R183 10.0k
U12
TLC555CD
VCC RESET DISCH THRES TRIG GND OUT CONT
R184 100k
D6 BAT54
R185 10.0k
C197 0.01uF
C201 0.1uF
C198 0.1uF
C199 0.1uF

S2 ON OFF
S3
R176 10.0k
17
J23
3.3V

TP90 DL_CLK
U9:A
U9:B
U9:C
U9:D
SN74HC08D
GND_PWR

U10
UCC27324D
NC INA GND INB NC OUTA VDD OUTB
C196 1uF

U11
UCC27324D
NC INA GND INB NC OUTA VDD OUTB
C202 1uF

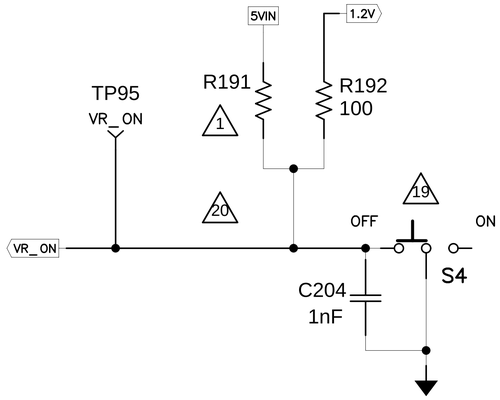
D4 RED
D5 RED
D7 RED
D8 RED
R186 330
R187 330
R188 330
R190 330

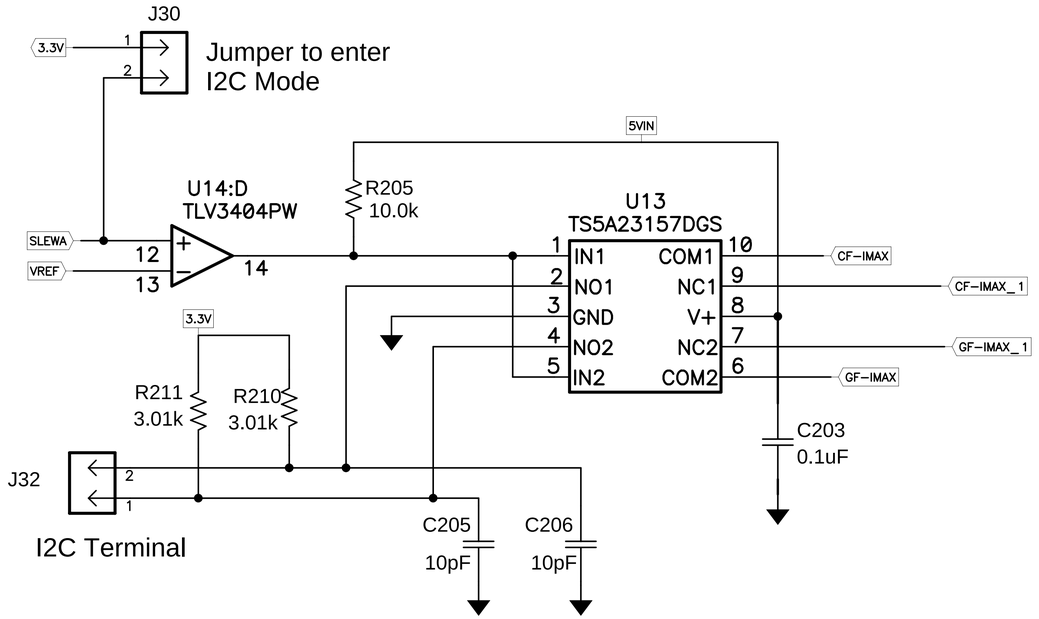
Q13 CSD16407Q5
Q14 CSD16407Q5

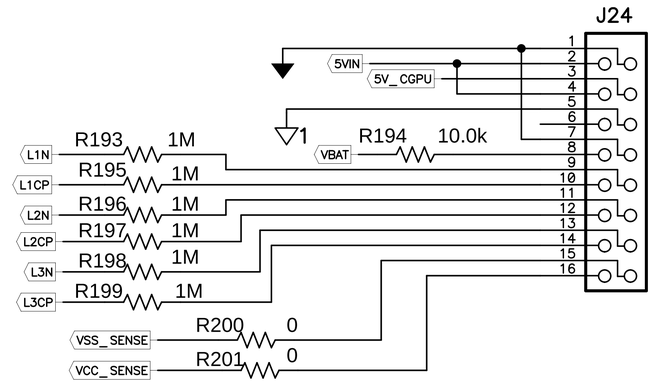
TP93 DYN_G_IO
TP94 GND
C200 1uF
R189 0.005

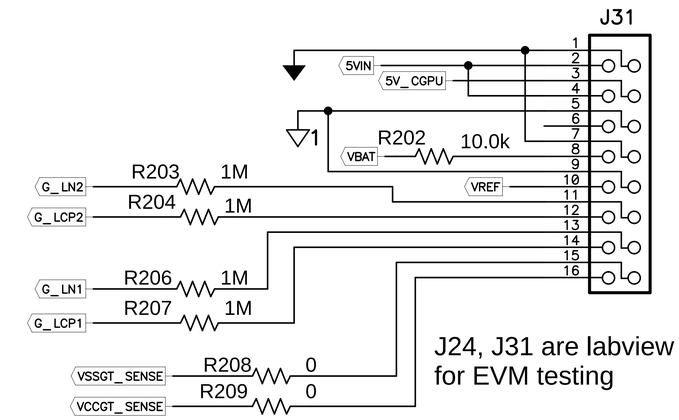
DYNAMIC LOADs

| | | |
|---|---|---|
| Title | TPS59650EVM-753 | |
| Size B | Number HPA753 | Rev A |
| Date Fri Jan 27, 2012 | Drawn by Nancy Zhang | |
| Filename HPA753A.SCH | Sheet 8 of 14 | |

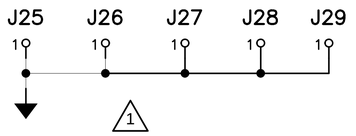


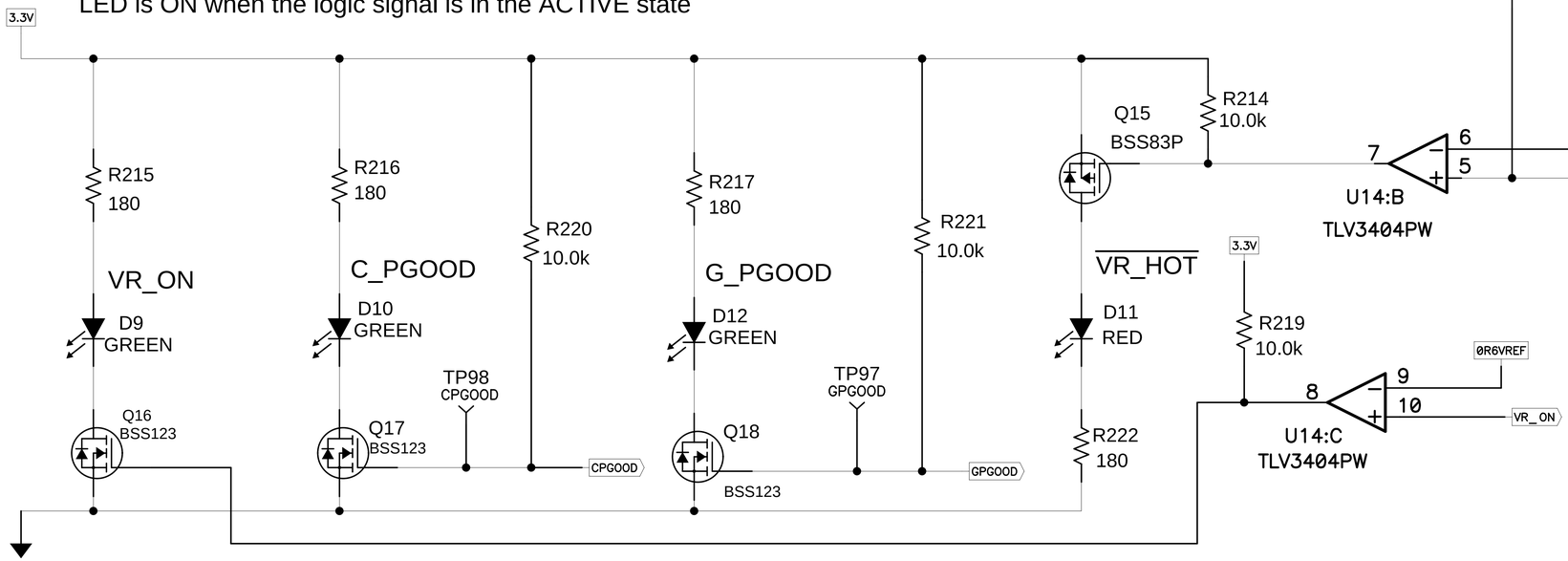

J24, J31 are labview connections for EVM testing

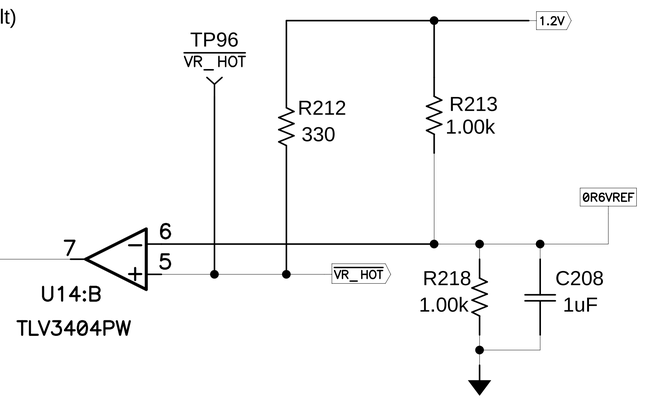


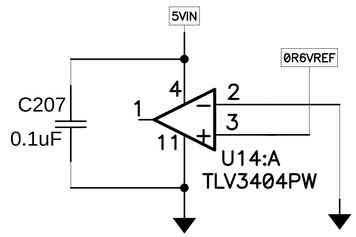

Note9:

1. Not used
19. S4: IMVP-7 VR Enable:
    1. Switch to "ON" position to Enable TPS59650 controller
    2. Switch to "OFF" position to Disable TPS59650 controller(Default)
20. Default Trim: R117 = Not used, R116 = 1.00k

Logic Signal Termination and Status LED's
LED is ON when the logic signal is in the ACTIVE state

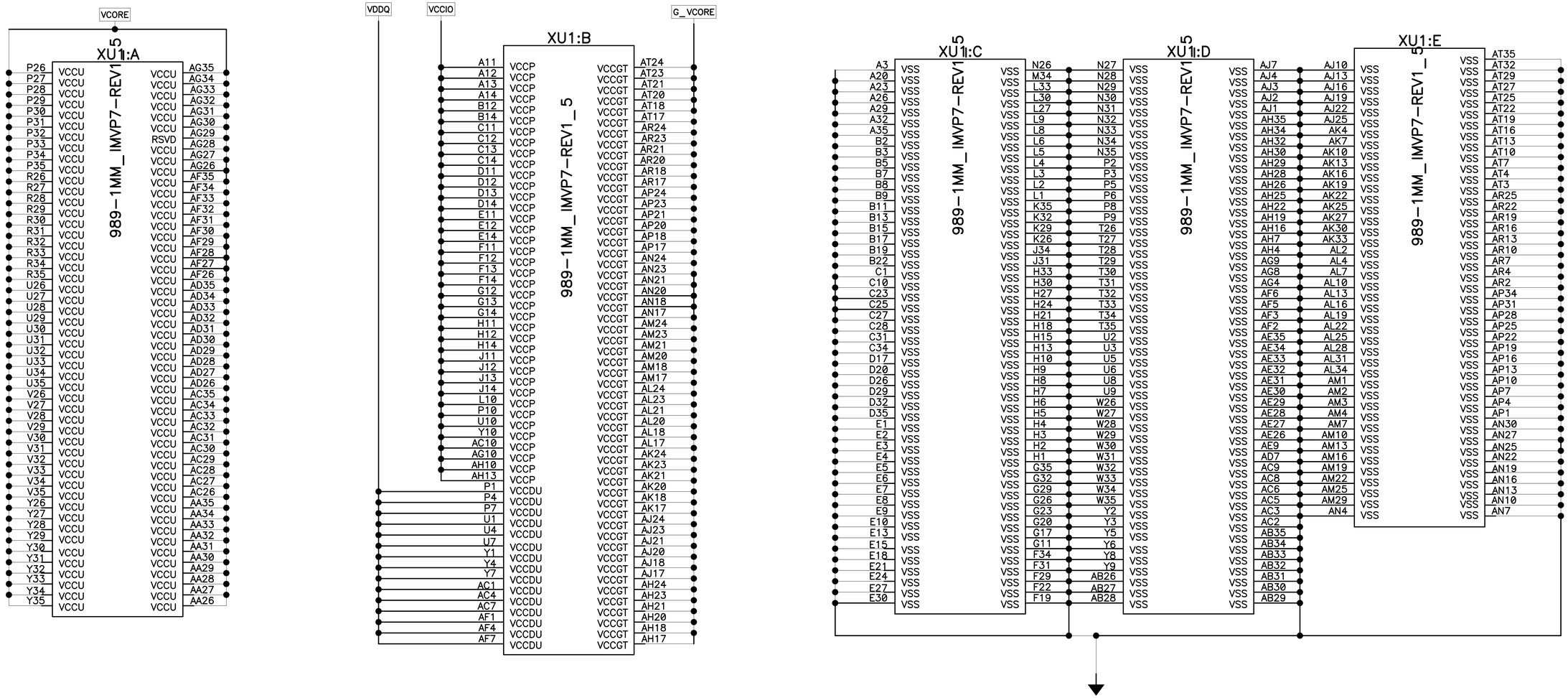


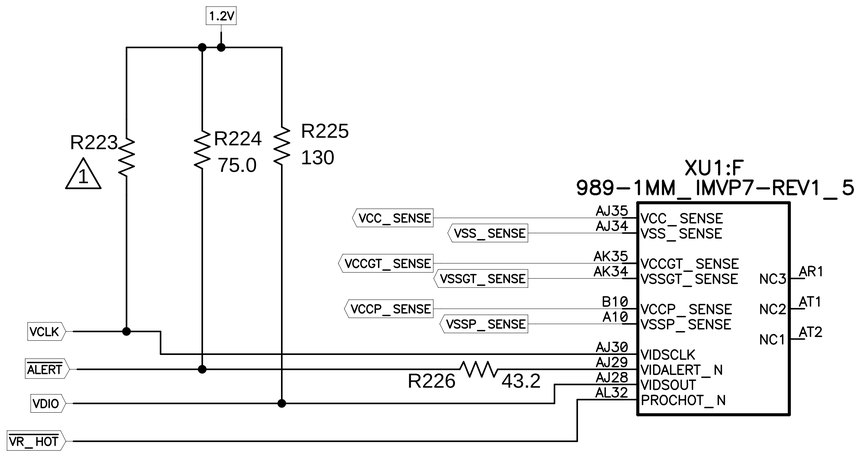




Support and Pull-ups

| | | |
|---|---|---|
| Title | TPS59650EVM-753 | |
| Size: BB | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet: 9 of 14 | |



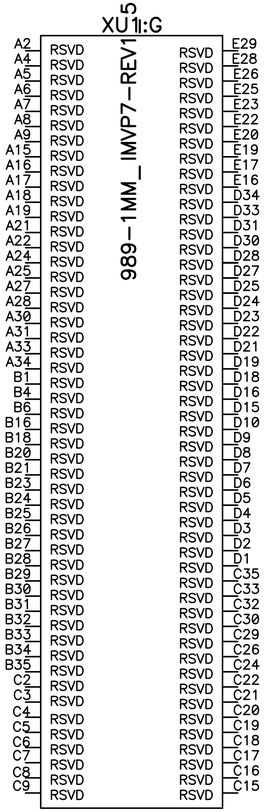



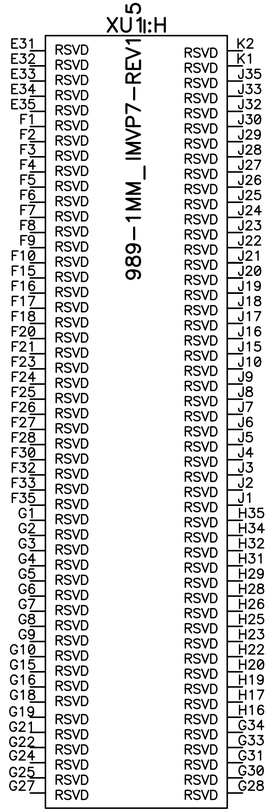

Note10:

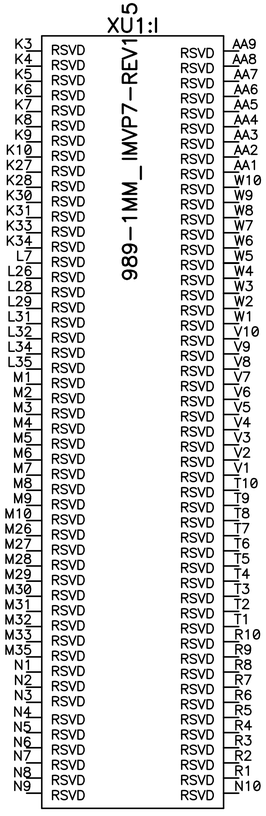
1 Not used

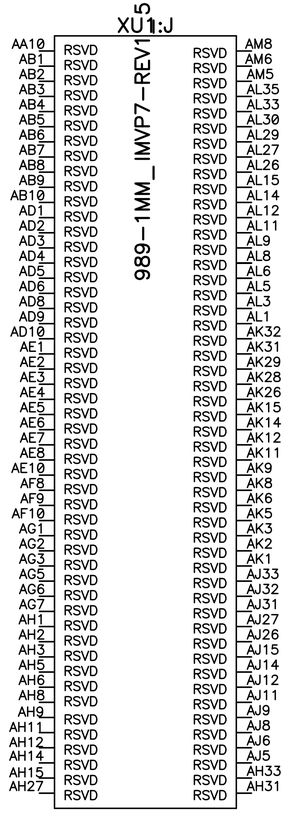
uC Socket Main

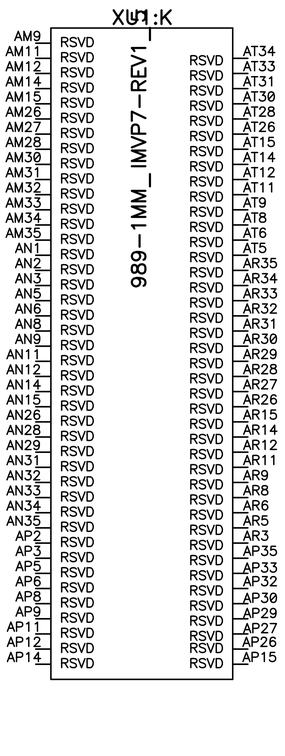
| | | |
|---|---|---|
| Title: TPS59650EVM-753 | | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet 10 of 14 | |



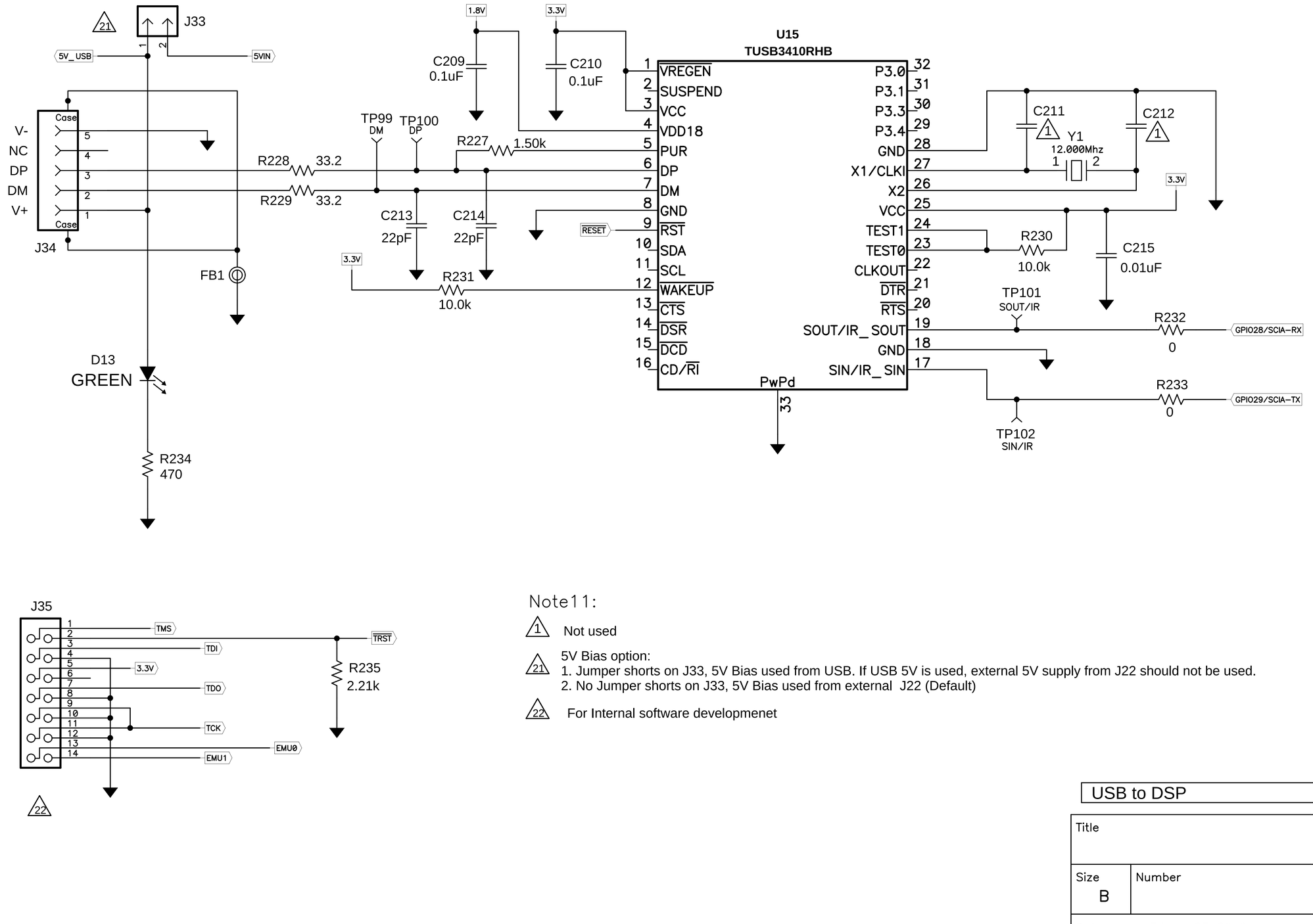




uC Socket Others

| | | |
|---|---|---|
| Title | TPS59650EVM-753 | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet 11 of 14 | |

Jumper to use 5V from USB







Note11:

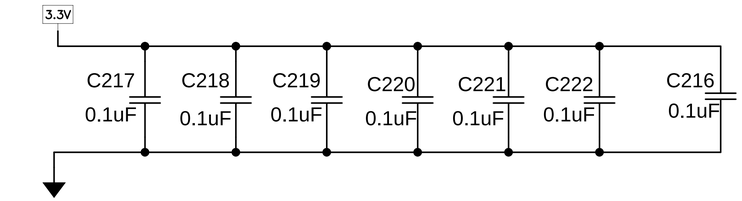
1. Not used

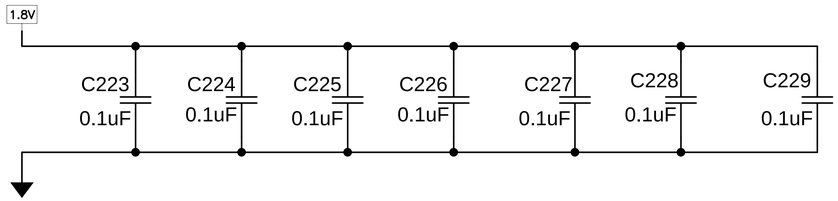
21. 5V Bias option:
    1. Jumper shorts on J33, 5V Bias used from USB. If USB 5V is used, external 5V supply from J22 should not be used.
    2. No Jumper shorts on J33, 5V Bias used from external J22 (Default)

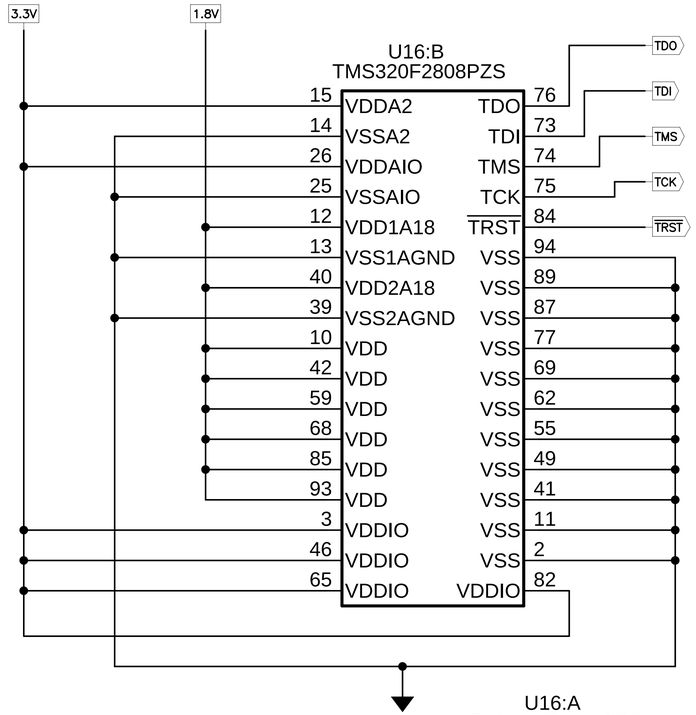
22. For Internal software developmenet

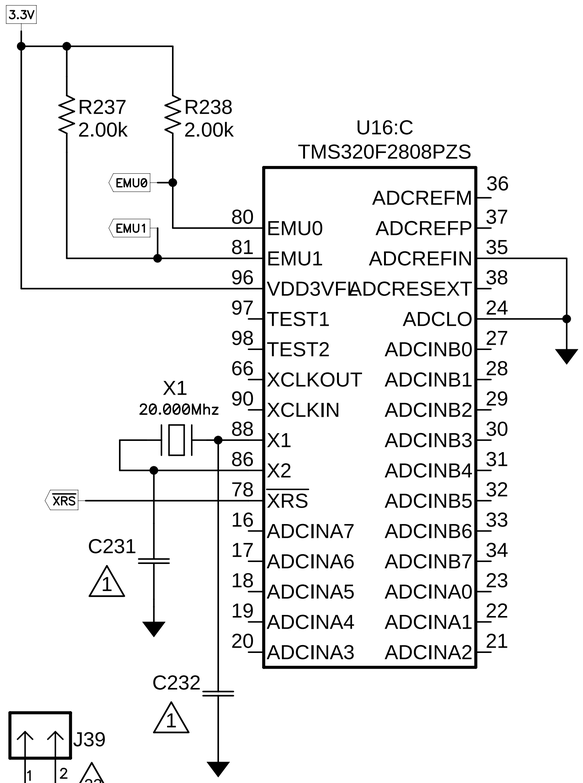
USB to DSP

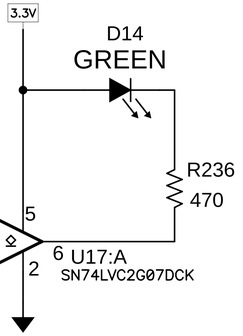
| | | |
|---|---|---|
| Title: TPS59650EVM-753 | | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | | Drawn by: Nancy Zhang |
| Filename: HPA753A.SCH | | Sheet 12 of 14 |

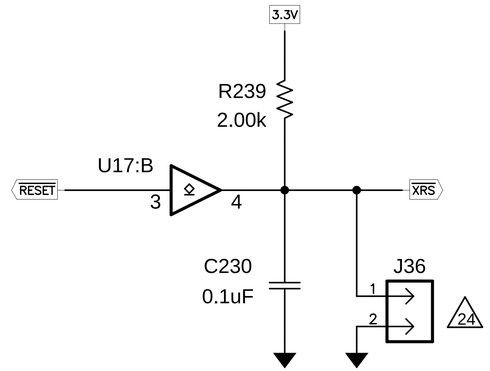


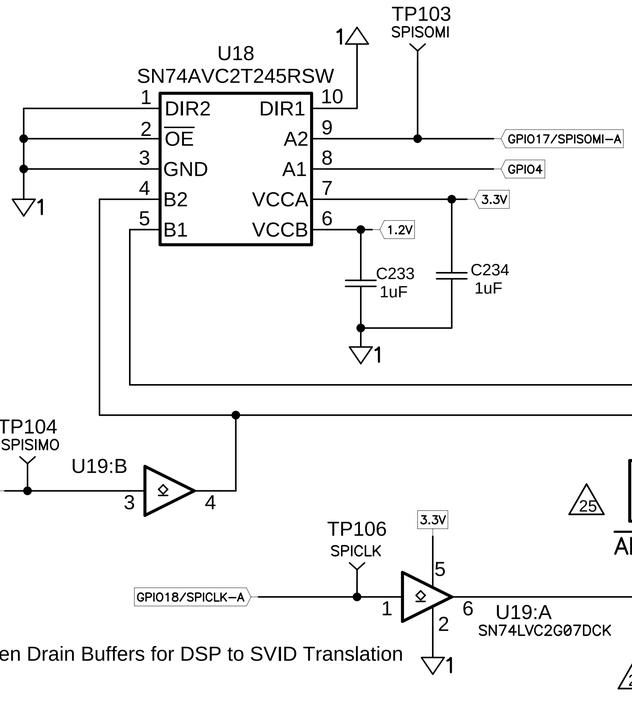



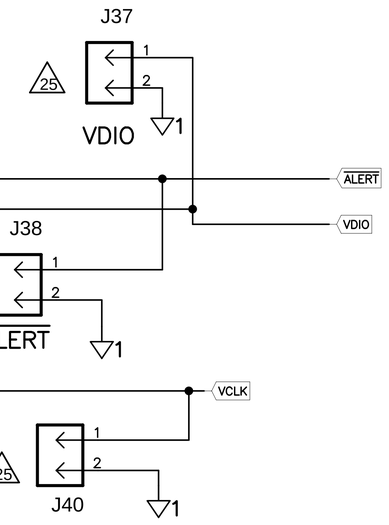



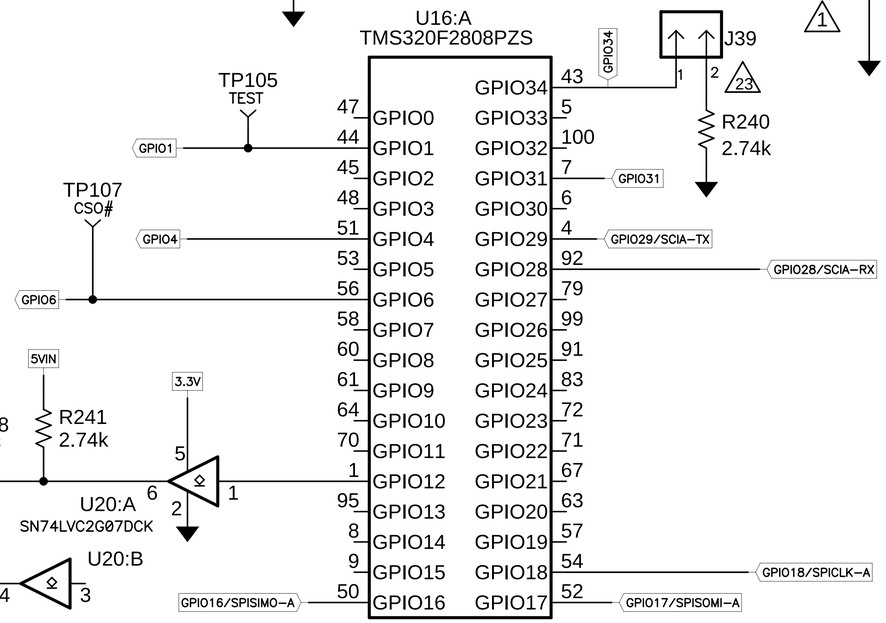



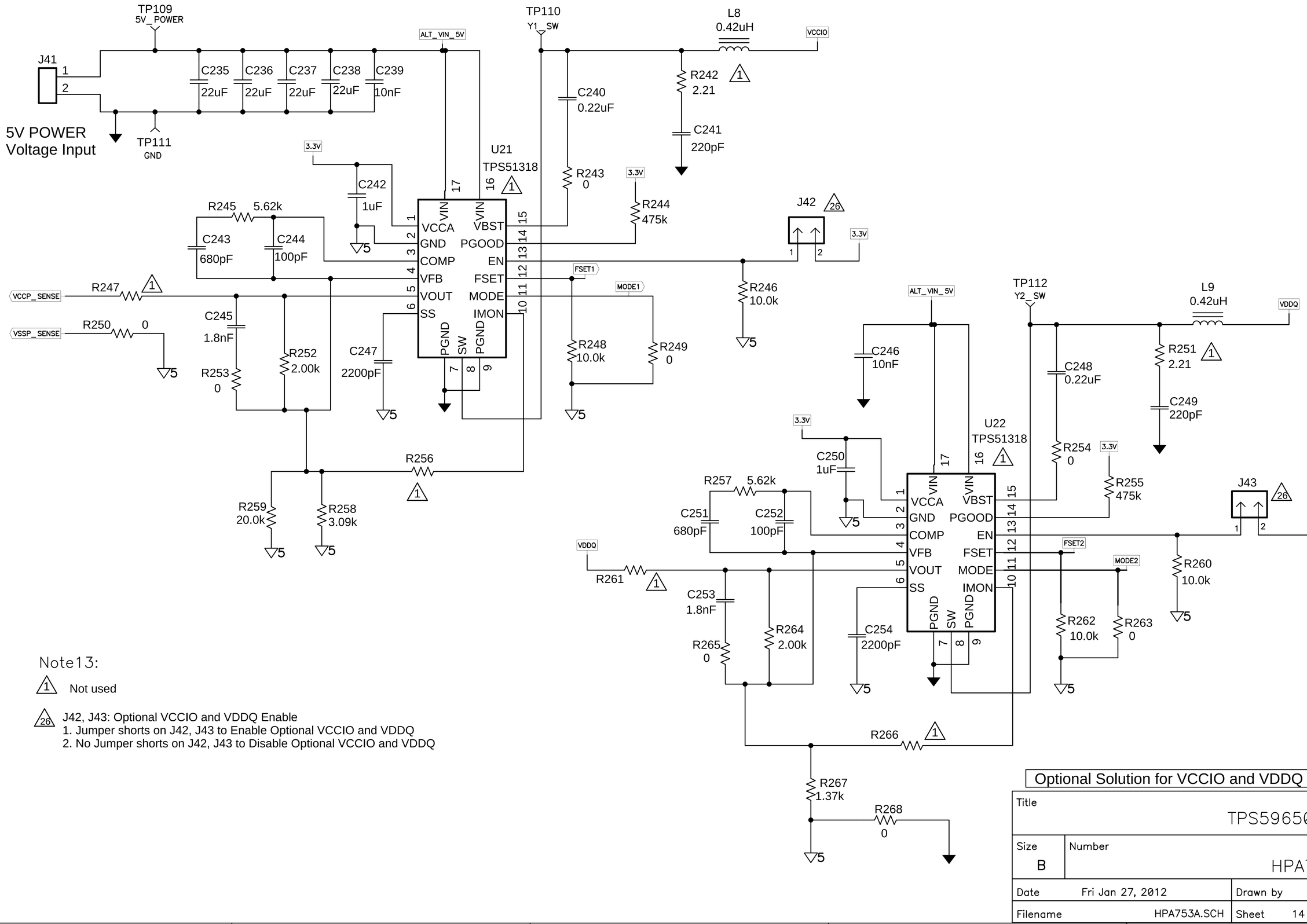

Level Shifting Tranceiver and Open Drain Buffers for DSP to SVID Translation

Note12:

1. Not used
2. J39: F2808 DSP Program Mode Selection:
   1. Jumper shorts for F2808 DSP Program Mode
   2. No Jumper shorts for normal operation (Default)
3. GUI and Intel VRTT Tool Selection
   1. Jumper shorts to use Intel VRTT Tool
   2. No Jumper shorts to user GUI (Default)
4. Differential Probe Test Point

DSP to SVID

| | | |
|---|---|---|
| Title: TPS59650EVM-753 | | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet 13 of 14 | |




Note13:

1 Not used

26 J42, J43: Optional VCCIO and VDDQ Enable
1. Jumper shorts on J42, J43 to Enable Optional VCCIO and VDDQ
2. No Jumper shorts on J42, J43 to Disable Optional VCCIO and VDDQ

Optional Solution for VCCIO and VDDQ

| | | |
|---|---|---|
| Title | TPS59650EVM-753 | |
| Size: B | Number: HPA753 | Rev: A |
| Date: Fri Jan 27, 2012 | Drawn by: Nancy Zhang | |
| Filename: HPA753A.SCH | Sheet 14 of 14 | |

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