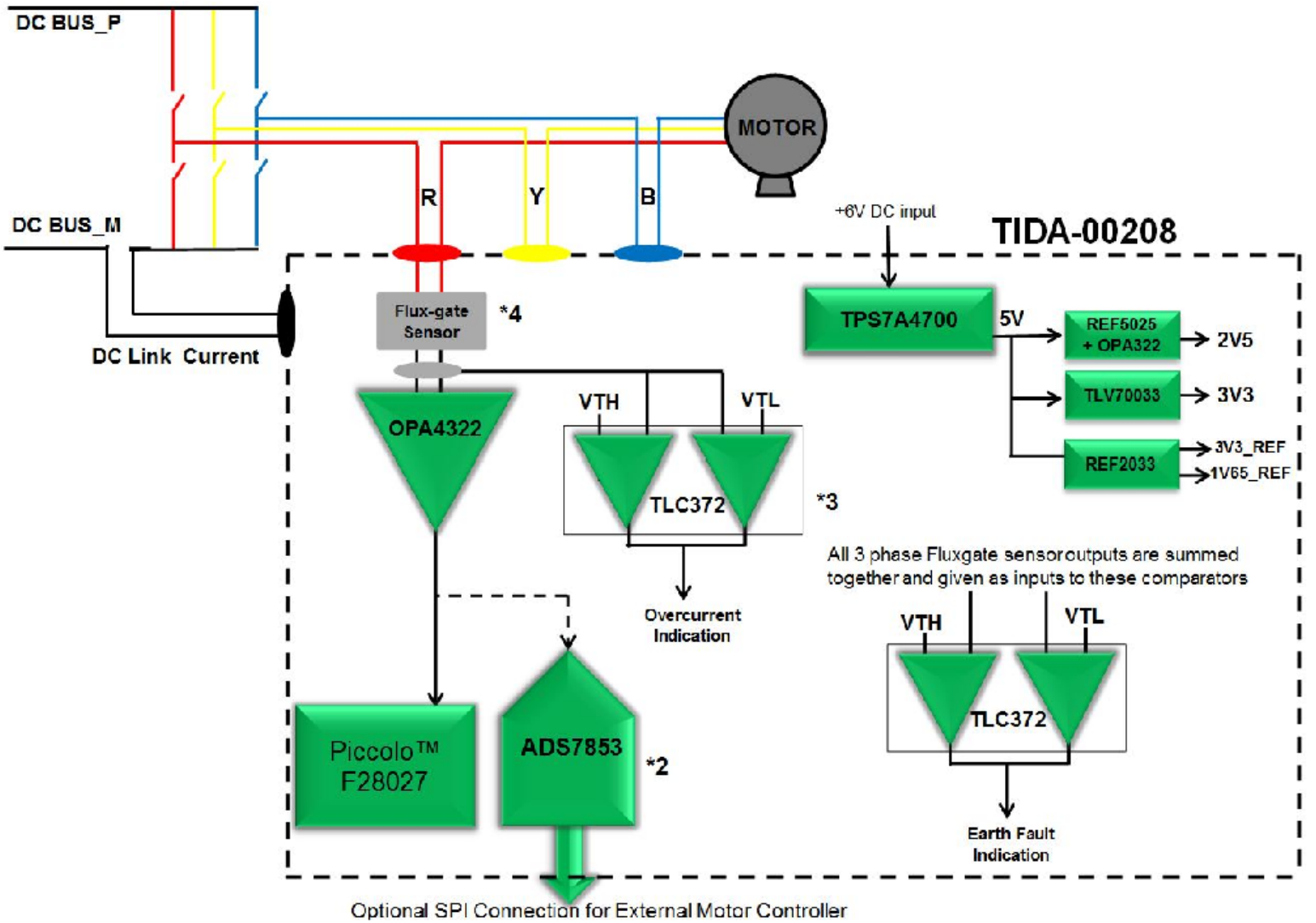

Designed for: Public Release	Mod. Date: 10/17/2014
Project Title: SE I/P ADC Signal Conditioning for Fluxgate Senso	
Number: TIDA-00208 Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001 Sheet: 1 of 6
Drawn By:	File: Pg1_Cover.SchDoc Size: B
Engineer: Sanjay Pithadia	Contact: http://www.ti.com/support

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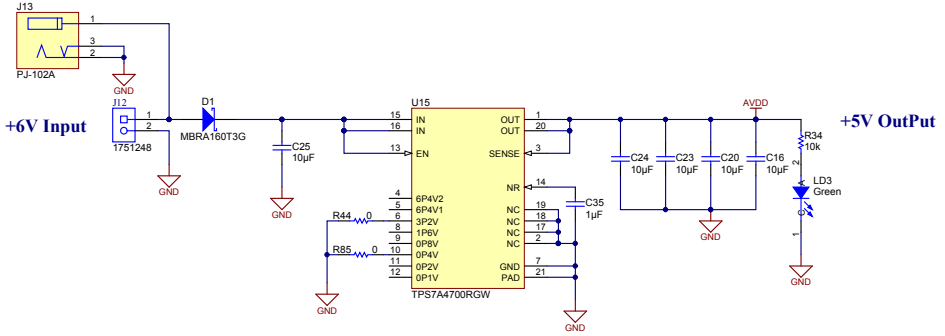
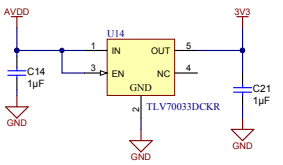


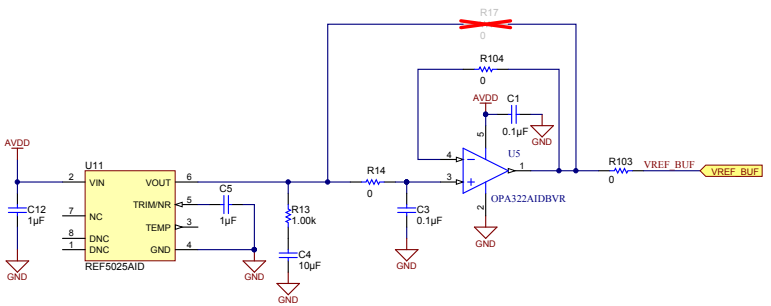
+6V Input

+5V OutPut

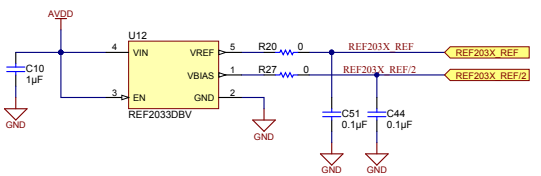
+6V to +5V Conversion



+5V to +3.3V Conversion

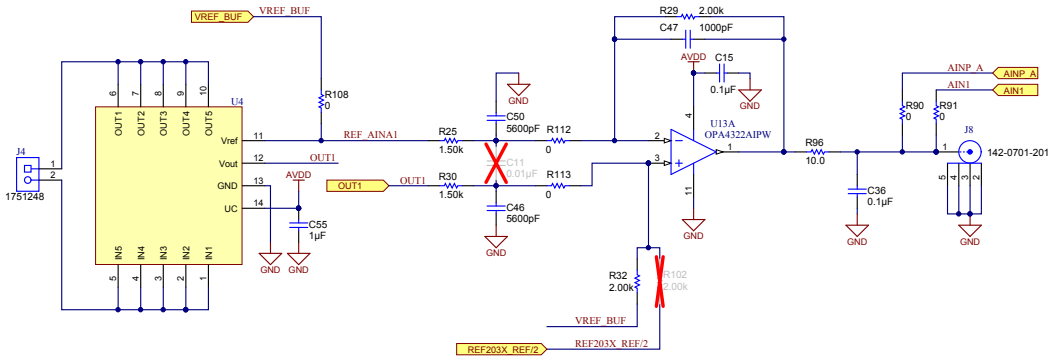


+2.5V Reference

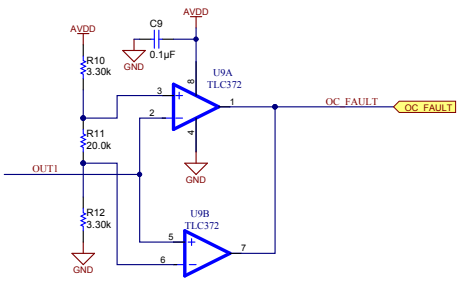


+3.3V Reference and +1.65V Bias supply

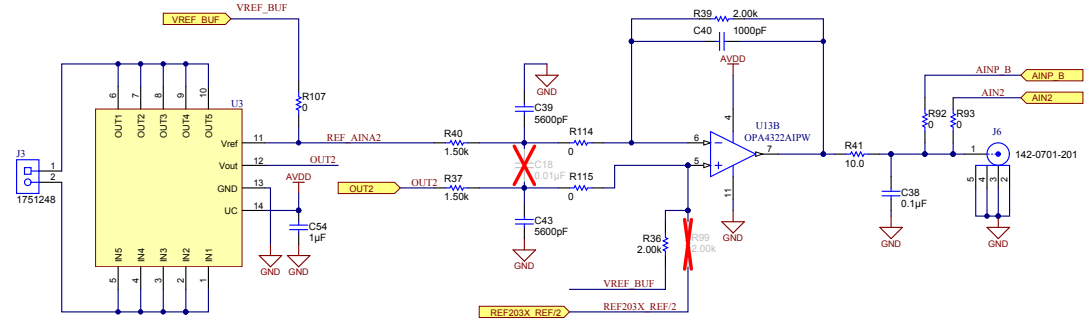
Designed for: Public Release		Mod. Date: 9/29/2014	
Project Title: SE I/P ADC Signal Conditioning for Fluxgate Senso			
Number: TIDA-00208	Rev: E1	Sheet Title: Main	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 6
Drawn By: Sanjay Pithadia		File: Pg2_Power.SchDoc	Size: B
Engineer: Sanjay Pithadia		Contact: http://www.ti.com/support	http://www.ti.com



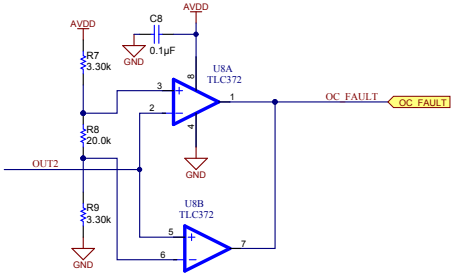
CH1 SIGNAL CONDITIONING



CH1 OVERCURRENT FAULT DETECTION

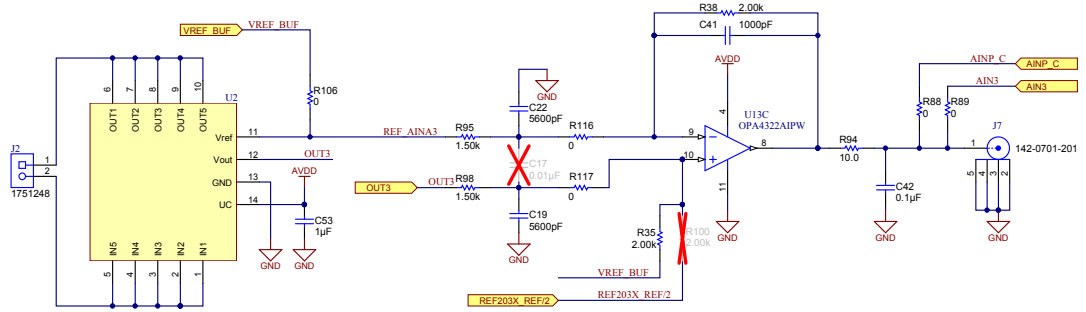


CH2 SIGNAL CONDITIONING

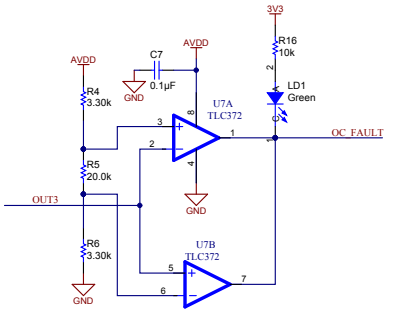


CH2 OVERCURRENT FAULT DETECTION

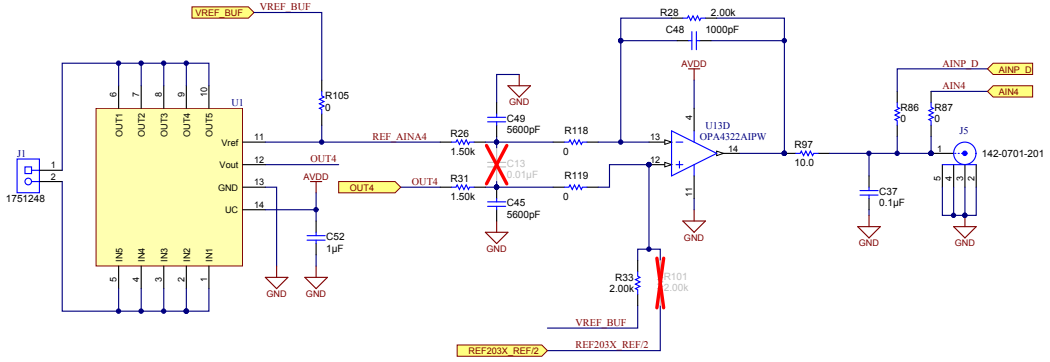
Designed for: Public Release		Mod. Date: 10/16/2014	
Project Title: SE I/P ADC Signal Conditioning for Fluxgate Senso			
Number: TIDA-00208	Rev: E1	Sheet Title: Main	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet:3 of 6
Drawn By:Sanjay Pithadia		File: Pg3_Channel-1_2.SchDoc	Size: B
Engineer: Sanjay Pithadia		Contact: http://www.ti.com/support	http://www.ti.com



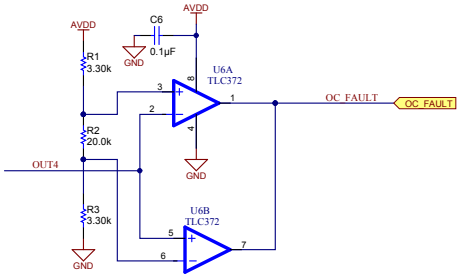
CH3 SIGNAL CONDITIONING



CH3 OVERCURRENT FAULT DETECTION

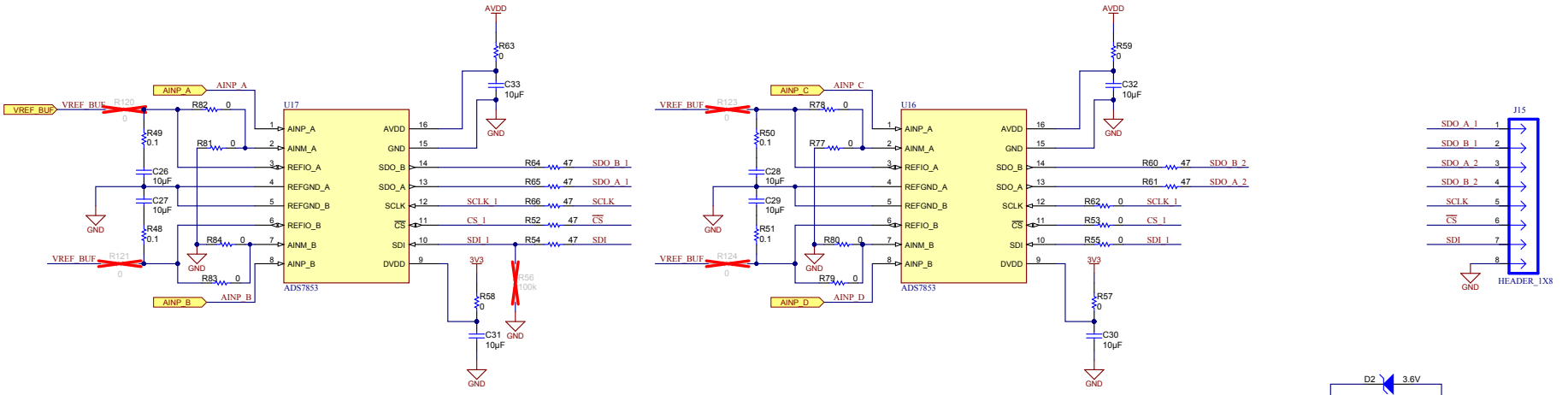


CH4 SIGNAL CONDITIONING

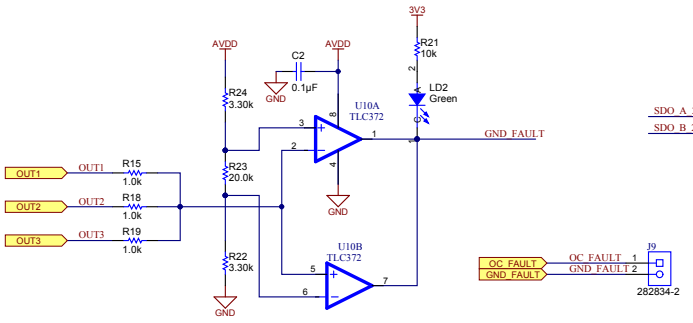


CH4 OVERCURRENT FAULT DETECTION

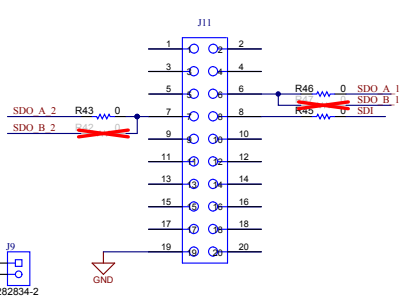
Designed for: Public Release		Mod. Date: 10/16/2014	
Project Title: SE I/P ADC Signal Conditioning for Fluxgate Senso			
Number: TIDA-00208	Rev: E1	Sheet Title: Main	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 6
Drawn By: Sanjay Pithadia		File: Pg4_Channel-3_4.SchDoc	Size: B
Engineer: Sanjay Pithadia		Contact: http://www.ti.com/support	http://www.ti.com

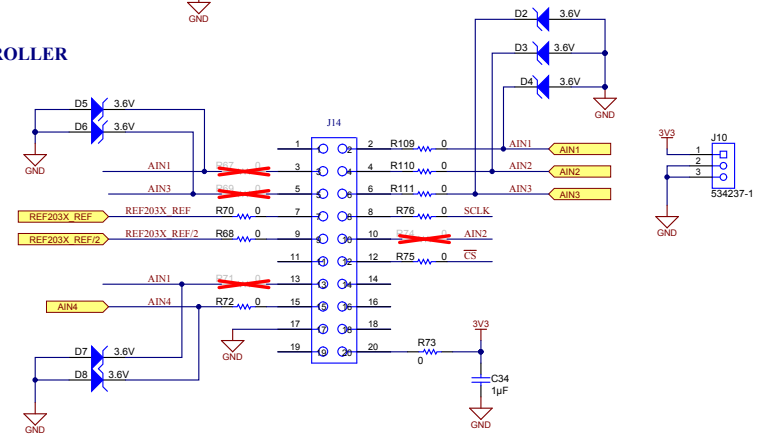


TWO ADS7853s FOR INTERFACING WITH EXTERNAL MOTOR CONTROLLER



GROUND FAULT DETECTION





INTERFACE FOR C2000 LAUNCHPAD

Designed for: Public Release		Mod. Date: 10/6/2014	
Project Title: SE I/P ADC Signal Conditioning for Fluxgate Senso			
Number: TIDA-00208	Rev: E1	Sheet Title: Main	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 6
Drawn By: Sanjay Pithadia		File: Pg5_ADC - Connectors.SchDoc	Size: B
Engineer: Sanjay Pithadia		Contact: http://www.ti.com/support	

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H3
NY PMS 440 0025 PH

H5
NY PMS 440 0025 PH

H1
NY PMS 440 0025 PH

H6
NY PMS 440 0025 PH

H2
NY PMS 440 0025 PH

H4
1902C

H8
1902C

H10
1902C

H7
1902C

H9
1902C

FID1 FID3 FID2 FID6 FID5 FID4

PCB Number: TIDA-00208
PCB Rev: E2

PCB
LOGO
Texas Instruments

LBL1
PCB Label
Size: 0.65" x 0.20 "

ZZ2
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ3
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ1
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Designed for: Public Release		Mod. Date: 10/17/2014	
Project Title: SE I/P ADC Signal Conditioning for Fluxgate Senso			
Number: TIDA-00208	Rev: E1	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 6
Drawn By:		File: Pg6_Hardware_ANSI-B.SchDoc	Size: B
Engineer: Sanjay Pithadia		Contact: http://www.ti.com/support	http://www.ti.com

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