Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.42mil		▨
4	Dielectric1	370HR	14.00mil	4.2	▨
5	Signal Layer 1	Copper	1.42mil		▨
6	Dielectric 2	370HR	10.00mil	4.2	▨
7	Signal Layer 2	Copper	1.42mil		▨
8	Dielectric 3	370HR	14.00mil	4.2	▨
9	Bottom Layer	Copper	1.42mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

Impedance Control:

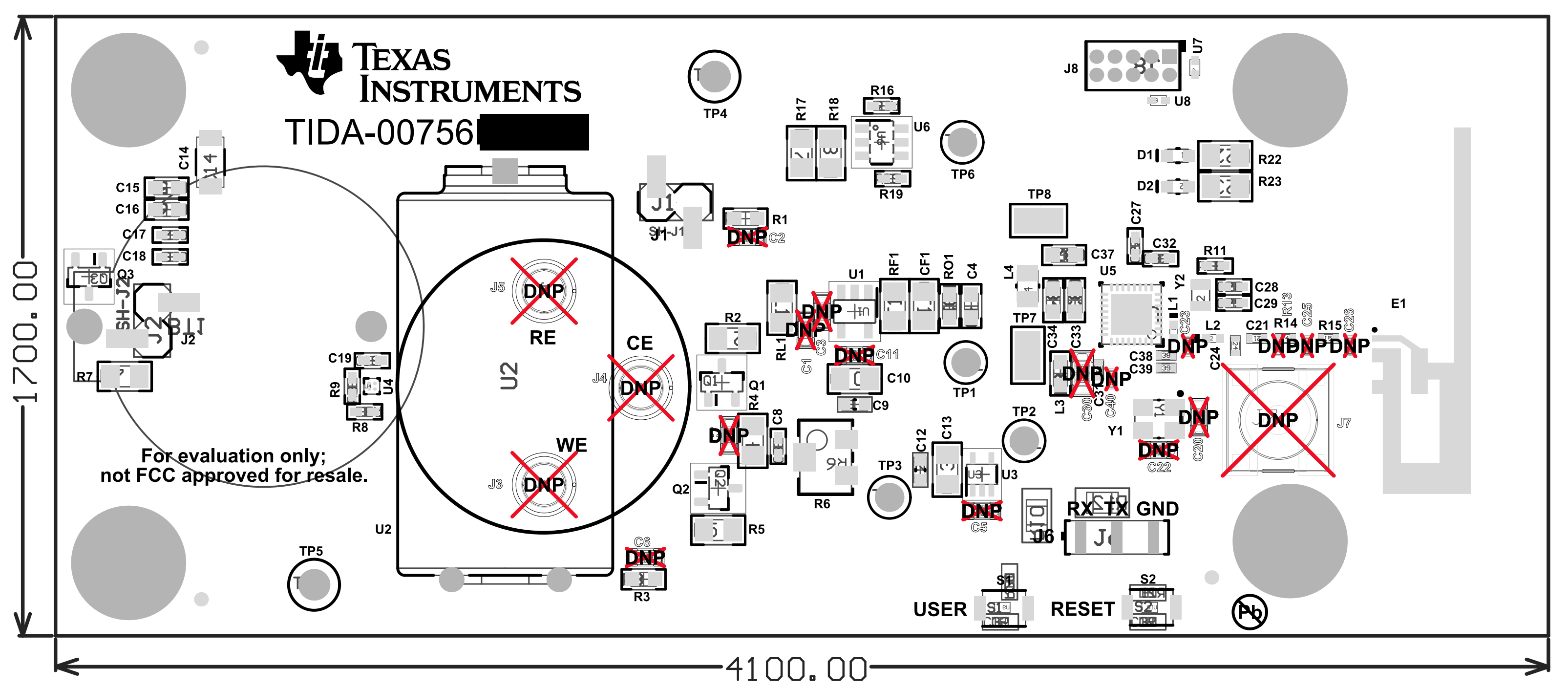
- Top layer contains 50 ohm impedance (+/- 10%) single ended using 24 mil lines (from E1 to U5)

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 20 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ________
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 44 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ________
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ________
DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ________
BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ________
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ________
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ________
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #:	TIDA-00756	REV:	E2	SVN REV: Not in version control
LAYER NAME = Top Overlay	TID #:	TIDA-00756			
PLOT NAME = Top Layer Assembly Drawing	GENERATED :	11/[illegible]/2016	2:41:30 PM		TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE:
Low Power CO Gas Sensor w/ BLE Connectivity

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-00756.PcbDoc

ENGINEER:	LAYOUT BY:
Gustavo Martinez	Krypton Solutions/RS
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.42mil		▨
4	Dielectric1	370HR	14.00mil	4.2	▨
5	Signal Layer 1	Copper	1.42mil		▨
6	Dielectric 2	370HR	10.00mil	4.2	▨
7	Signal Layer 2	Copper	1.42mil		▨
8	Dielectric 3	370HR	14.00mil	4.2	▨
9	Bottom Layer	Copper	1.42mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

Impedance Control:

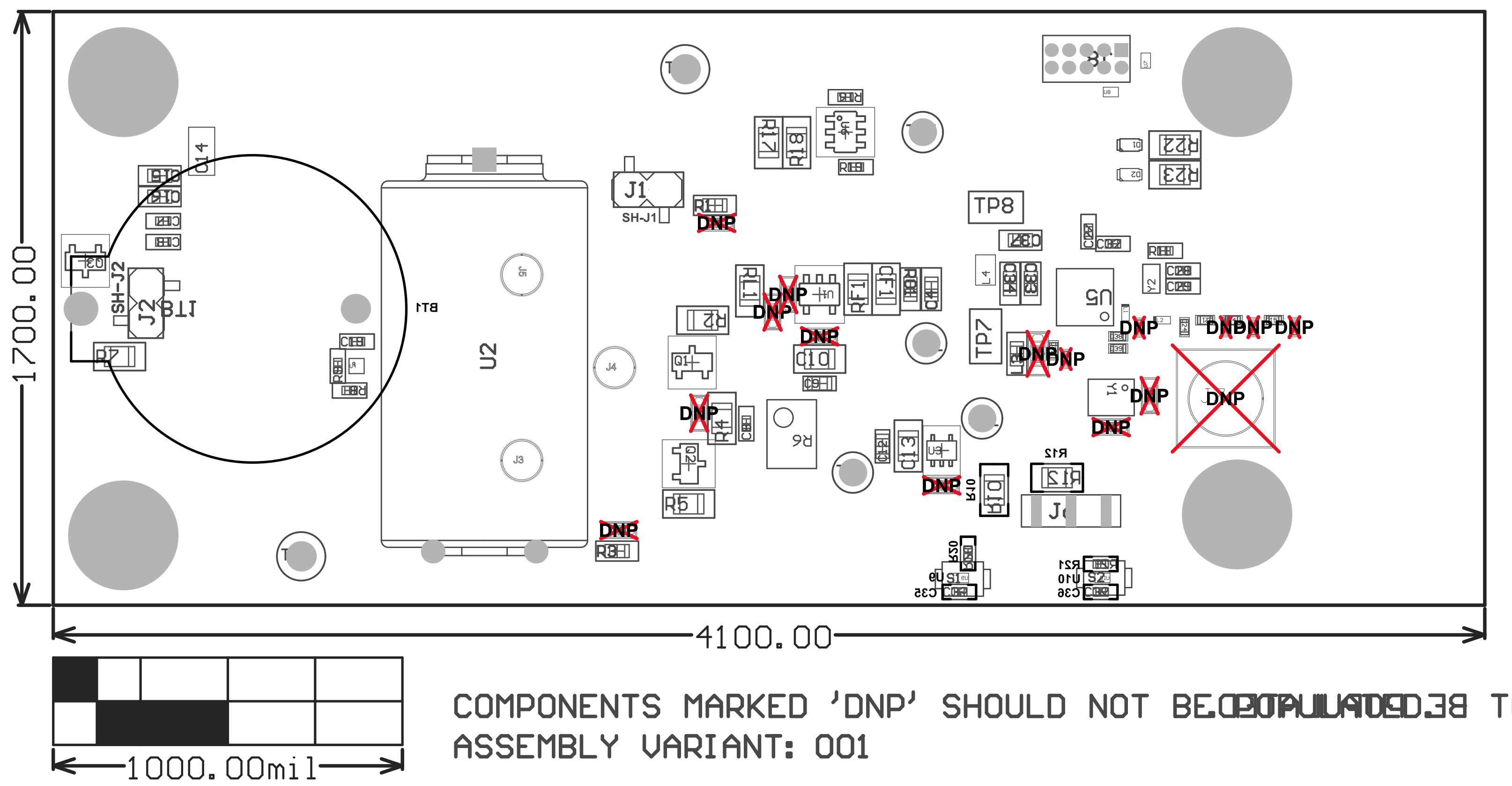
- Top layer contains 50 ohm impedance (+/- 10%) single ended using 24 mil lines (from E1 to U5)

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 20 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ______
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 44 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______
DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ______
BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ______
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ______
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ______
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00756	REV: E2	SVN REV: Not in version control
LAYER NAME = Bottom Overlay	TID #: TIDA-00756		
PLOTNAME = Signal Layer 1 Assembly Drawing	GENERATED : 11/17/2016 2:41:41 PM		TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

PROJECT TITLE:
Low Power CO Gas Sensor w/ BLE Connectivity

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-00756.PcbDoc

ENGINEER:
Gustavo Martinez

LAYOUT BY:
Krypton Solutions/RS

SCALE: 1.00

ALTIUM DESIGNER VERSION:
16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.42mil		▨
4	Dielectric1	370HR	14.00mil	4.2	▨
5	Signal Layer 1	Copper	1.42mil		▨
6	Dielectric 2	370HR	10.00mil	4.2	▨
7	Signal Layer 2	Copper	1.42mil		▨
8	Dielectric 3	370HR	14.00mil	4.2	▨
9	Bottom Layer	Copper	1.42mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				

Impedance Control:

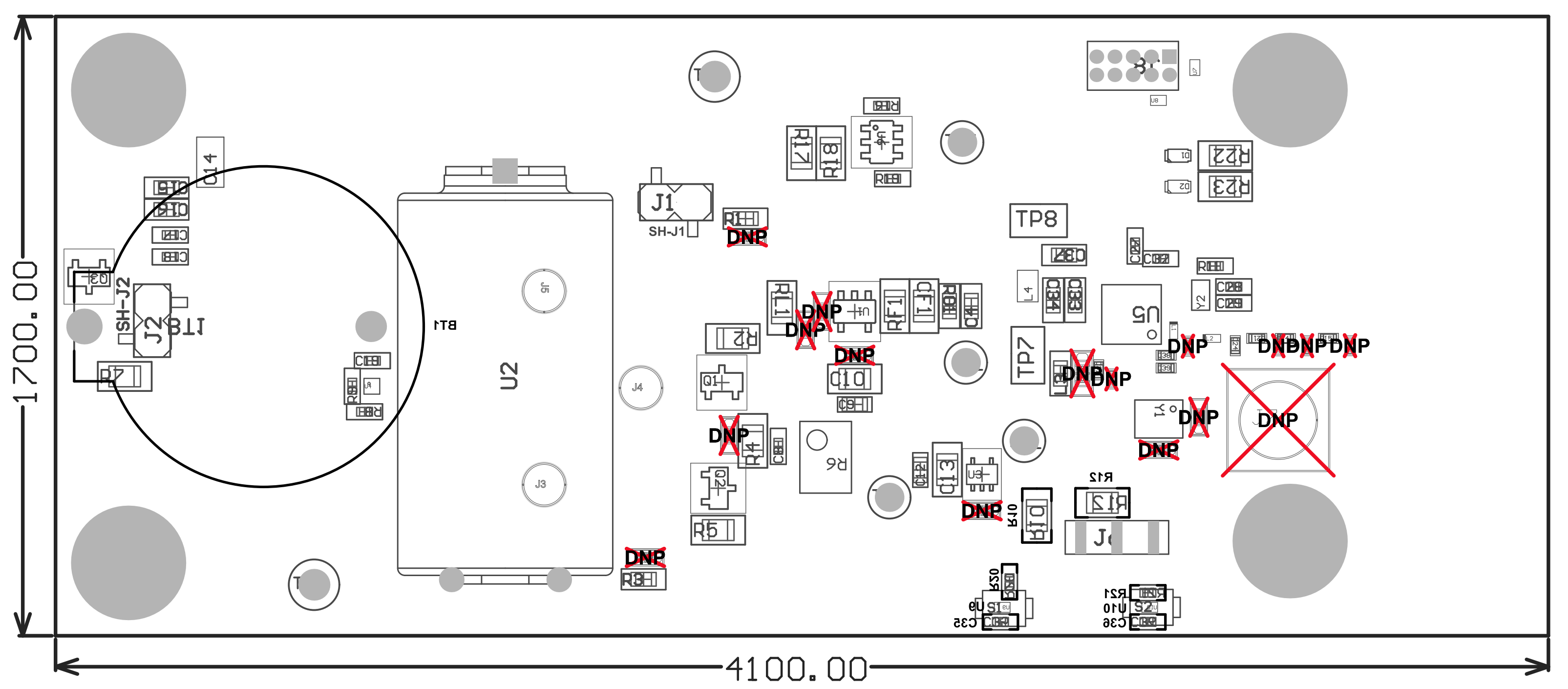
- Top layer contains 50 ohm impedance (+/- 10%) single ended using 24 mil lines (from E1 to U5)

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 20 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ______
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 44 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______
DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ______
BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ______
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ______
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ______
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER



1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

PCB ARTWORK VIEWED FROM TOP SIDE	E3	BOARD #:	TIDA-00756	REV:	E2
LAYER NAME = Bottom		TID #:	TIDA-00756		
PLOT NAME = Signal Layer 2 Assembly Drawing		GENERATED : 11/17/2016 2:41:52 PM			TEXAS INSTRUMENTS

PROJECT TITLE:
Low Power CO Gas Sensor w/ BLE Connectivity

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-00756.PcbDoc

ENGINEER:	LAYOUT BY:
Gustavo Martinez	Krypton Solutions/RS
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.9.368

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.42mil		▨
4	Dielectric1	370HR	14.00mil	4.2	▨
5	Signal Layer 1	Copper	1.42mil		▨
6	Dielectric 2	370HR	10.00mil	4.2	▨
7	Signal Layer 2	Copper	1.42mil		▨
8	Dielectric 3	370HR	14.00mil	4.2	▨
9	Bottom Layer	Copper	1.42mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

Impedance Control:

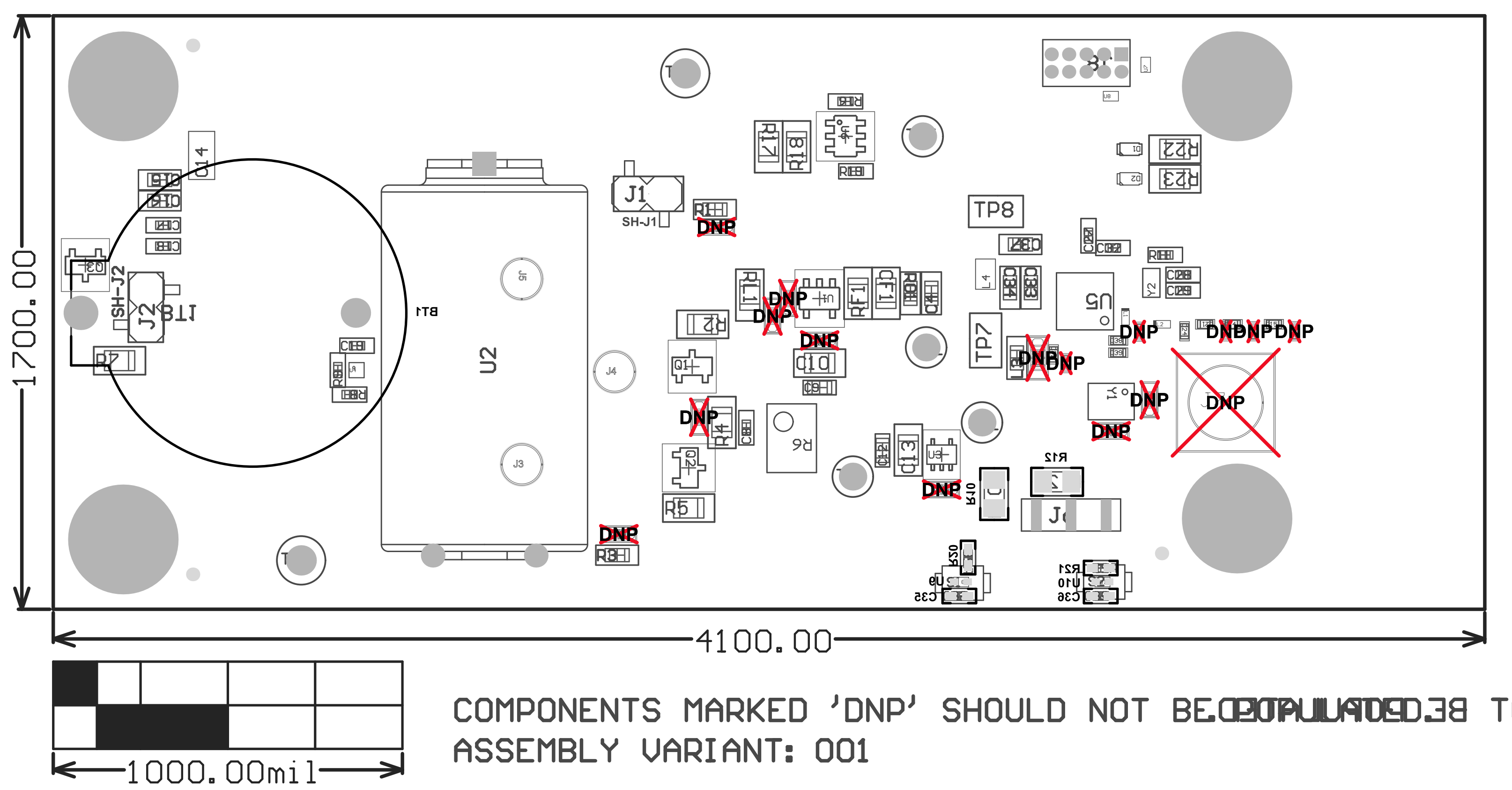
- Top layer contains 50 ohm impedance (+/- 10%) single ended using 24 mil lines (from E1 to U5)

DESIGN INFORMATION

MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA PAD SIZE: 20 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ________
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 44 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ________
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ________
DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ________
BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ________
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ________
☒ MATTE ☐ SEMI-GLOSS
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ________
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: 001

TEXAS INSTRUMENTS

PROJECT TITLE:
Low Power CO Gas Sensor w/ BLE Connectivity

DESIGNED FOR:
Public Release

FILE NAME:
TIDA-00756.PcbDoc

PCB ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00756	REV: E2	SVN REV: Not in version control
LAYER NAME = Bottom Overlay	TID #: TIDA-00756		
PLOT NAME = Layer Assembly Drawing	GENERATED : 11/17/2016 2:42:06 PM		TEXAS INSTRUMENTS

ENGINEER:
Gustavo Martinez

LAYOUT BY:
Krypton Solutions/RS

SCALE: 1.00

ALTIUM DESIGNER VERSION:
16.0.9.368

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