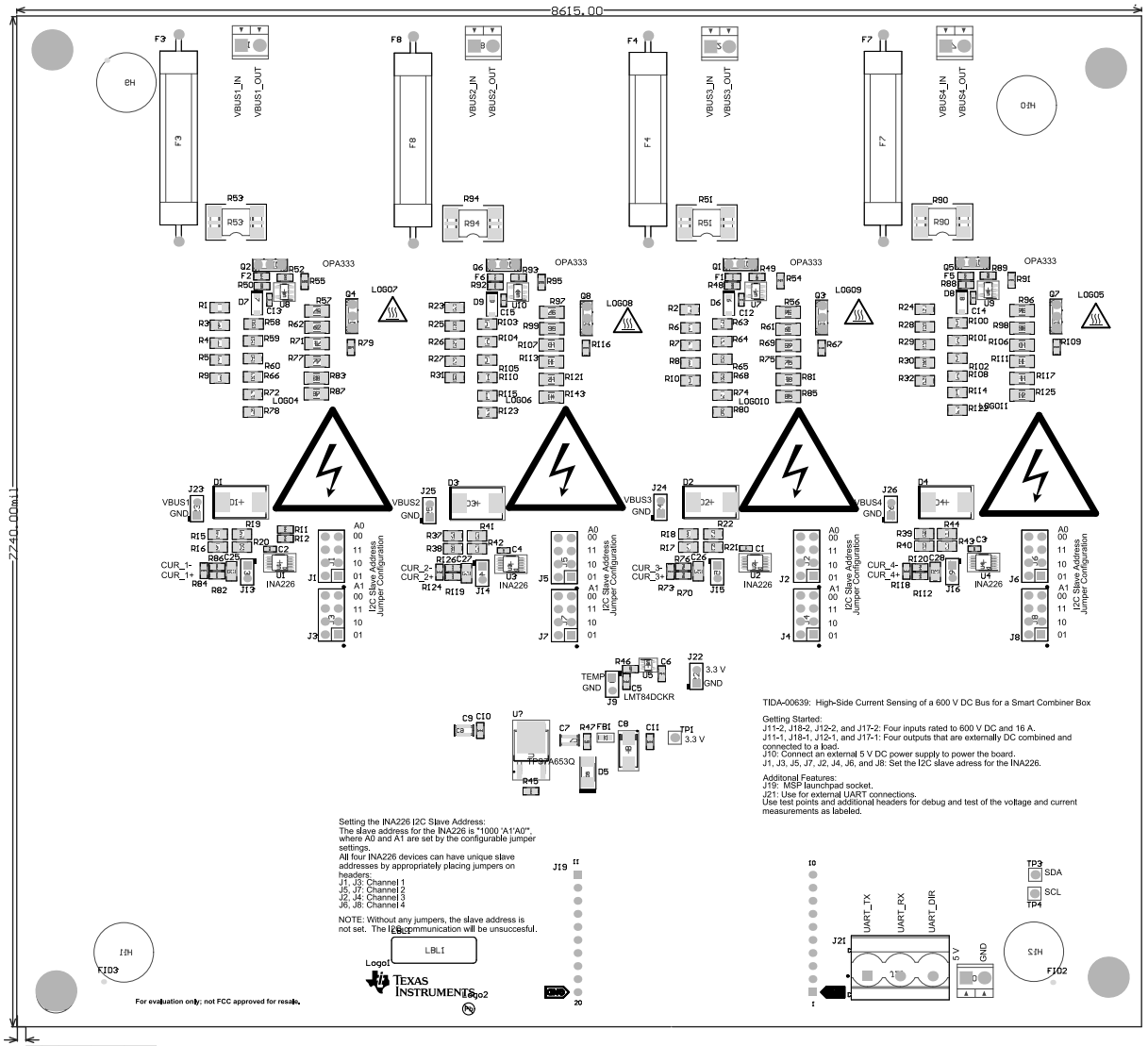
Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top Layer	Copper	1.40mil			
4	Dielectric1	FR-4	59.20mil	4.8		
5	Bottom Layer	Copper	1.40mil			
6	Bottom Solder	Solder Resist	0.40mil	3.5		
7	Bottom Overlay					

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-00639
DESIGNED FOR: Public Release
FILE NAME: PCB_Project_1_TIDA-00639.PcbDoc

ENGINEER: Katelyn Wiggenhorn	LAYOUT BY: Katelyn Wiggenhorn
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.8.354

Z21 ■Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
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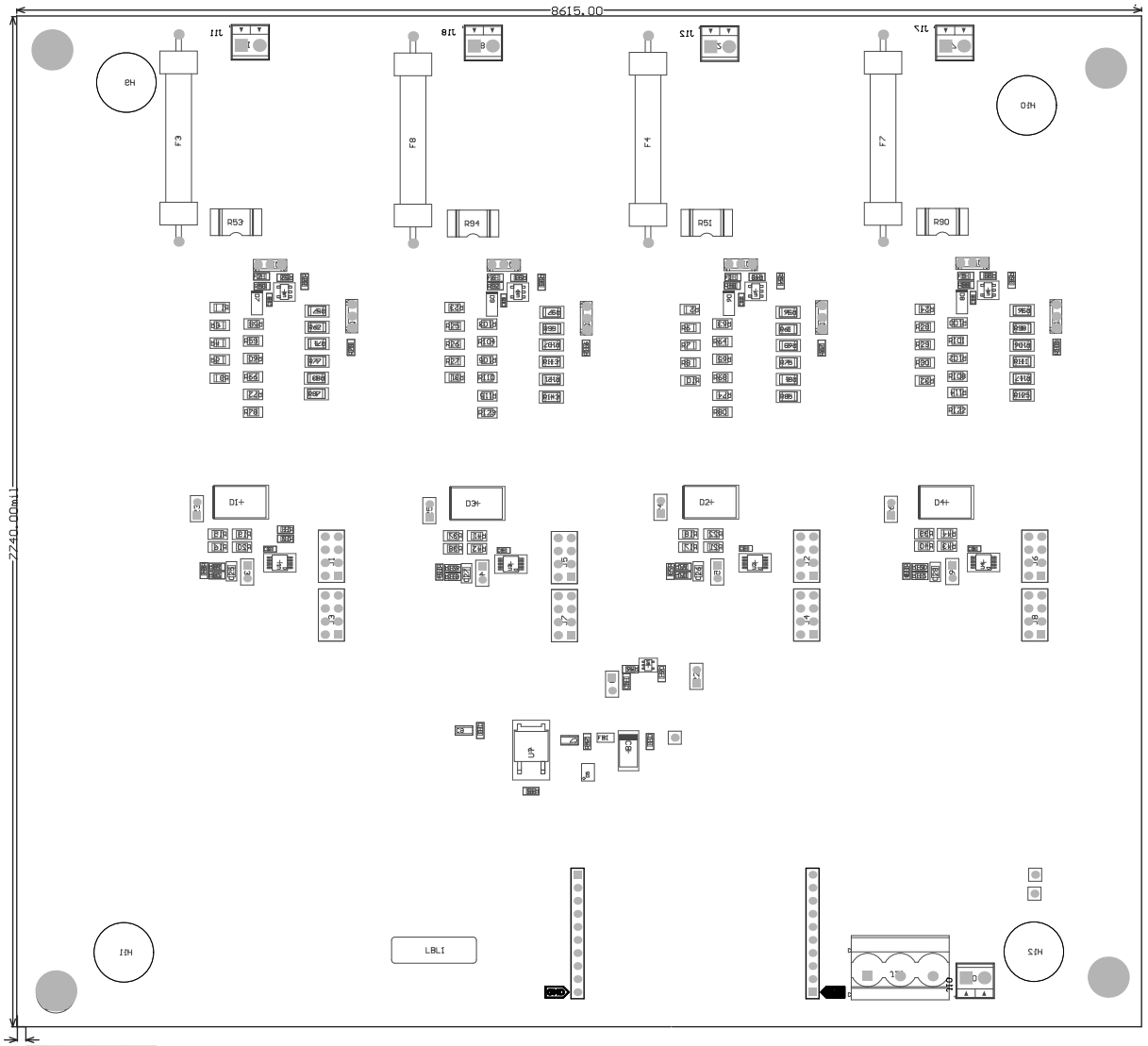

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[ ] OTHER +/-
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[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
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ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

65.00
1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-00639
DESIGNED FOR: Public Release
FILE NAME: PCB_Project_1_TIDA-00639.PcbDoc

ENGINEER: Katelyn Wiggenhorn	LAYOUT BY: Katelyn Wiggenhorn
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.0.8.354

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265