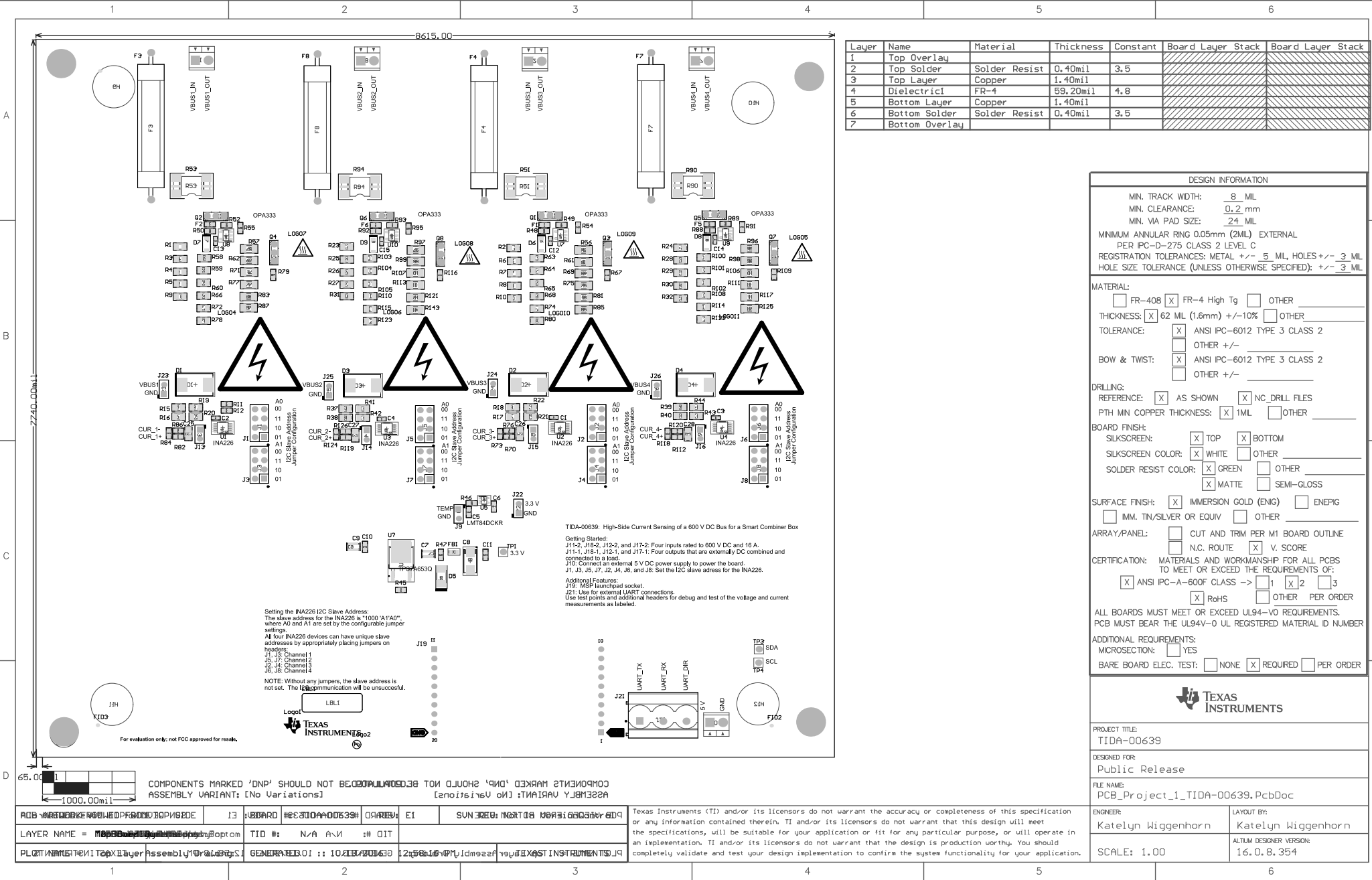


- Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
- Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
- Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top Layer	Copper	1.40mil			
4	Dielectric	FR-4	59.20mil	4.8		
5	Bottom Layer	Copper	1.40mil			
6	Bottom Solder	Solder Resist	0.40mil	3.5		
7	Bottom Overlay					

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____

THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____

TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL_FILES

PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 1MM. TN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

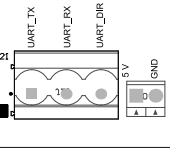
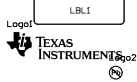
TIDA-00639: High-Side Current Sensing of a 600 V DC Bus for a Smart Combiner Box

Getting Started:
 J11-2, J18-2, J12-2, and J17-2: Four inputs rated to 600 V DC and 16 A.
 J11-1, J18-1, J12-1, and J17-1: Four outputs that are externally DC combined and connected to a load.
 J10: Connect an external 5 V DC power supply to power the board.
 J1, J5, J7, J2, J4, J6, and J8: Set the I2C slave address for the INA226.

Additional Features:
 J19: MSP launchpad socket.
 Z21: Use for external UART connections.
 Use test points and additional headers for debug and test of the voltage and current measurements as labeled.

Setting the INA226 I2C Slave Address:
 The slave address for the INA226 is "1000 A1A0", where A0 and A1 are set by the configurable jumper settings.
 All four INA226 devices can have unique slave addresses by appropriately placing jumpers on headers:
 J1: I2C Channel 1
 J5: I2C Channel 2
 J2: I2C Channel 3
 J6: I2C Channel 4

NOTE: Without any jumpers, the slave address is not set. The I2C communication will be unsuccessful.



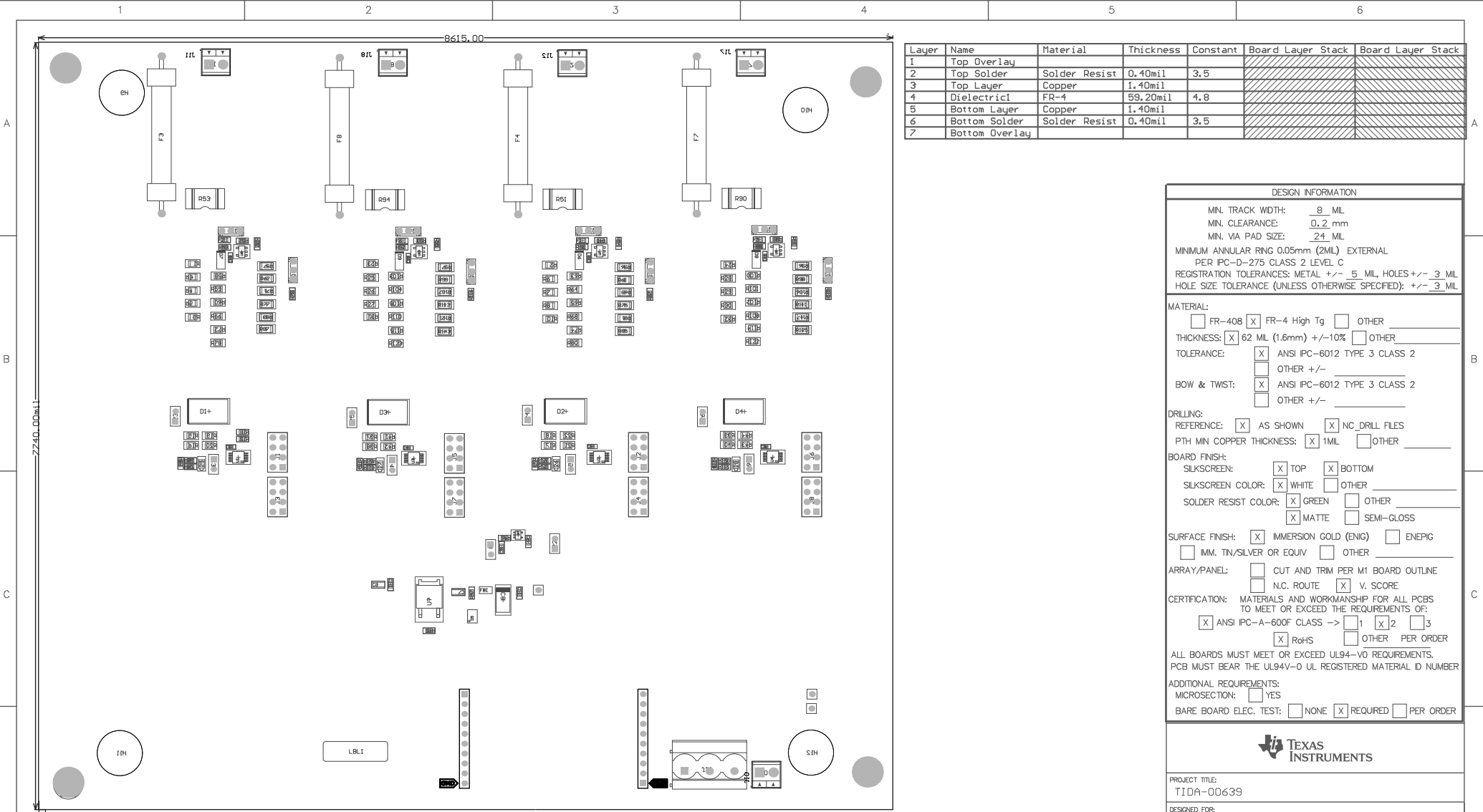
1	2	3	4	5	6
COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED FROM THE SUPPLIER. ASSEMBLY VARIANT: [No Variations]					
LAYER NAME = TOP Layer Assembly Drawing					
SCALE: 1:1000.00mil					

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PROJECT TITLE: TIDA-00639
 DESIGNED FOR: Public Release
 FILE NAME: PCB_Project_1_TIDA-00639_PcbDoc

ENGINEER: Katelyn Wiggernhorn
 LAYOUT BY: Katelyn Wiggernhorn
 ALTUM DESIGNER VERSION: 16.0.8.354

221 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 222 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
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DESIGN INFORMATION

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 MIN. VIA PAD SIZE: 24_MIL

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 PER IPC-D-275 CLASS 2 LEVEL C
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 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL

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TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

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 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
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SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
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 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER

65.00
 1000.00mil
 COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED FROM THE MANUFACTURER
 ASSEMBLY VARIANT: [No Variations]

ADDITIONAL INFORMATION: [No Variations]

PCB PROJECT: TIDA-00639
 LAYER NAME = Bottom Solder
 PLATE NAME: Bottom Solder

GENERATED ON: 10/23/2013 12:58:32 PM
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PROJECT TITLE: TIDA-00639
 DESIGNED FOR: Public Release
 FILE NAME: PCB_Project_1_TIDA-00639.PcbDoc

ENGINEER: Katelyn Wiggernhorn
 LAYOUT BY: Katelyn Wiggernhorn
 ALTUM DESIGNER VERSION: 16.0.8.354

SCALE: 1.00

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