Test Report: PMP31246

Discontinuous Mode SEPIC Reference Design With Modulated Output Voltage

Description

This automotive single-ended primary inductor converter (SEPIC) using the LM5156-Q1 or LM51561-Q1 devices is designed to support a modulated output voltage, in this design a sinusoidal waveform 60 V_{PP} at up to 120 Hz. Descriptions of two of the dynamic limitations with this reference design follow:

1. A SEPIC operating in continuous-conduction mode (CCM) is dynamically limited by the right half plane zero (RHPZ)
2. By using a nonsynchronous rectification at low output voltages, the discharge current at the output capacitor by resistive load gets small, the output voltage cannot follow the desired modulating waveform anymore

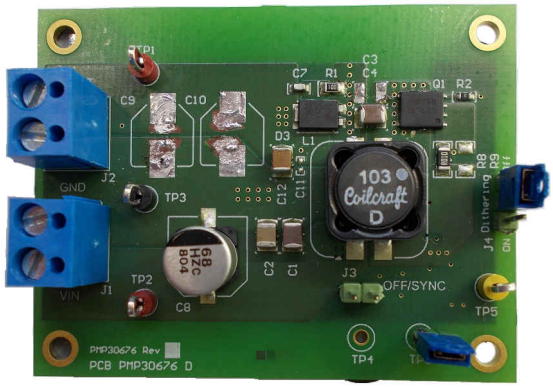
The magnetizing inductance is minimized to operate the power stage in discontinuous mode (DCM), moving the RHPZ at the lowest input voltage and maximum load (worst case) beyond 300 kHz. However, the dynamics are still limited by the gain bandwidth of the error amplifier and the Nyquist criteria. A loop bandwidth of 10 kHz is sufficient for only 100 Hz at the output. Furthermore, DCM removes Q_{rr} ringing at the semiconductors and the dual inductor gets fairly small. The disadvantage is the high ripple current resulting in magnetizing losses, AC losses at the winding, and a large output ripple voltage. In this situation this disadvantage is acceptable (for such a low maximum output power of 18 W).

Features

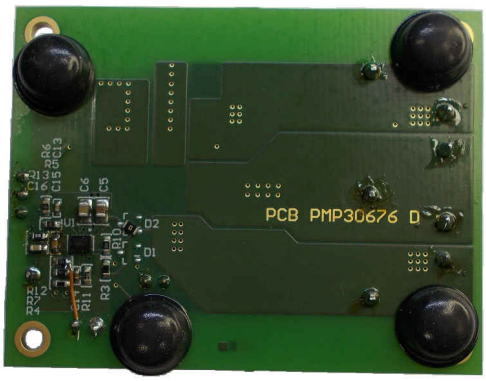
- For the best dynamics, a loop bandwidth of 10 kHz is used
- The output voltage can be modulated up to a frequency of 120 Hz sinusoidal
- This reference design is completely built and tested in a lab

Applications

- Smart glass module



Top Photo



Bottom Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	8 V – 16 V (12 V nominal), load dump up to 36 V_{PK}
Output Voltage	60 V_{AC} with DC Offset
Output Current	0.3 A_{MAX}
Switching Frequency	100 kHz
Topology	DCM SEPIC
IC	LM51561-Q1

1.2 Considerations

During operation, the circuit started to switch around 8.9 V and the switching stops at around 8.2 V.

A resistor was used as load. Unless otherwise indicated, the output current was adjusted to 0.3 A and the input voltage was set to 12-V nominal input voltage.

For the waveforms in Section 3, the modulating input J201 is shorted. The output is set to 60 V_{DC} and maximum output power is 18 W.

The prototype device NVMFS021N10MCL was used as Q1, due to availability.

1.3 Dimensions

The size of the four-layer board is 65 mm × 50 mm.

2 Testing and Results

2.1 Efficiency Graphs

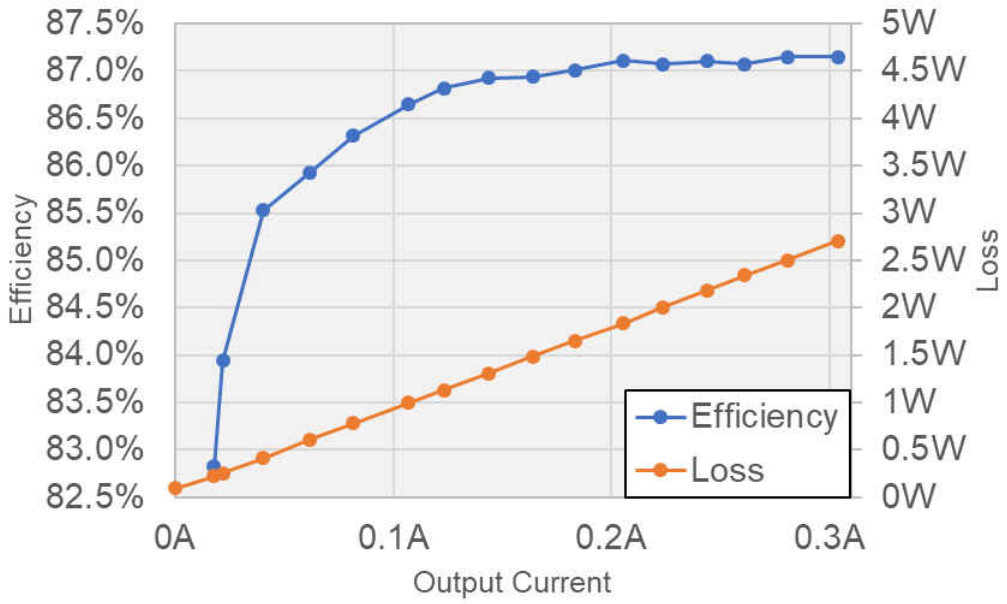


Figure 2-1. Efficiency and Loss vs Output Current

Discontinuous mode (DCM) lowers the typical efficiency of higher than 90%.

2.2 Load Regulation

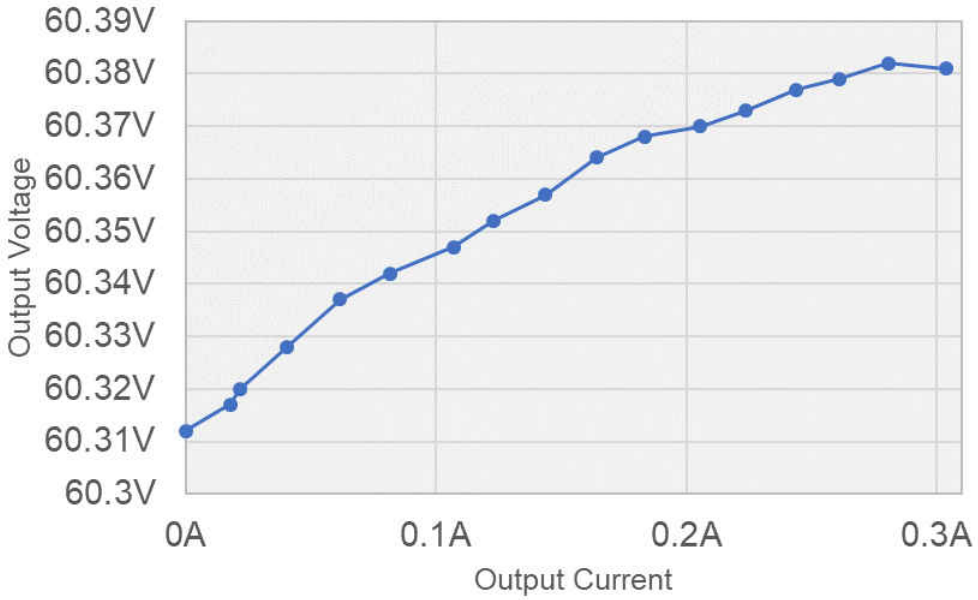


Figure 2-2. Output Voltage vs Output Current

2.3 Thermal Images

2.3.1 Unmodulated 60 V_{DC} - Output

Figure 2-3 is a thermal image taken at 60-V_{DC} output voltage and 0.3-A load (200 Ω).

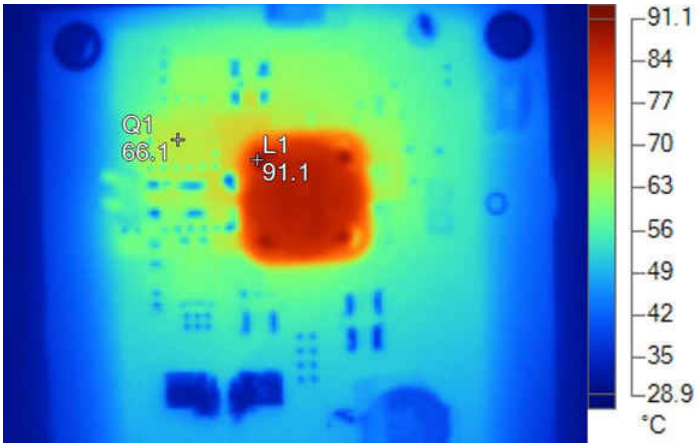


Figure 2-3. IR-Foto 60 V_{DC}, Output Power 18 W

Name	Temperature
L1	**91.1°C**
Q1	66.1°C

2.3.2 60 V_{AC} - Output Modulated With 120-Hz Sinus (0 V – 5 V)

The thermal image in Figure 2-4 is taken with a modulated output voltage. The modulation voltage V_{mod} was TTL level 5-V sinusoidal with DC offset at 120 Hz.

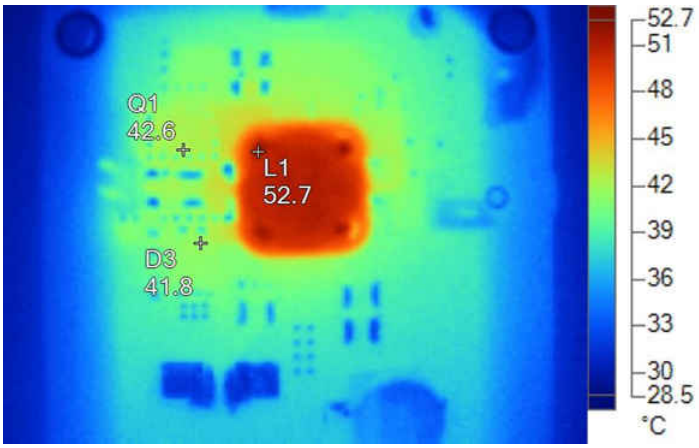


Figure 2-4. IR Foto 60 V_{AC}, Output Voltage Modulated

Name	Temperature
D3	41.8°C
L1	52.7°C
Q1	42.6°C

2.3.3 Conclusion

Using static operations at 60 V_{DC} with 18-W output power, the AC winding losses and core losses are fairly high.

By modulating the output, the dual inductor is well selected and the semiconductors can be shrunk (transistor 3 mm × 3 mm; Schottky in SMA).

2.4 Bode Plot at Maximum Duty Cycle

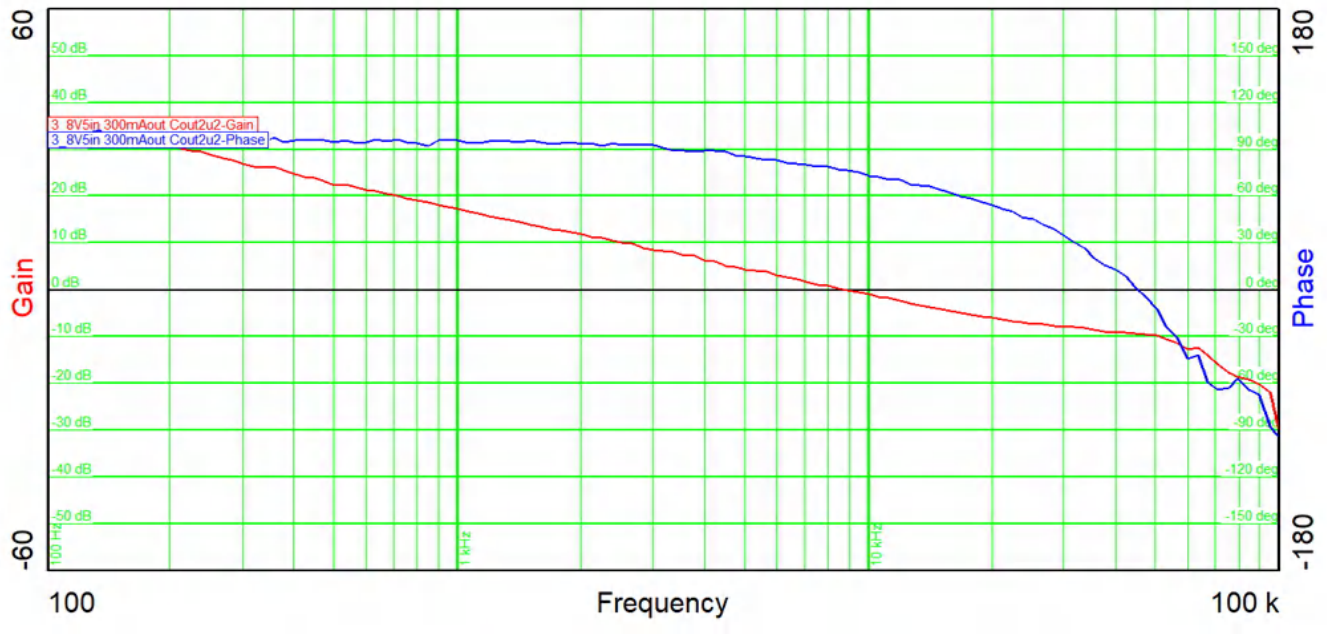


Figure 2-5. Bode Plot *Worst Case* = *RHPZ Minimum* (8.5 V_{IN}, 60 V_{OUT}, 0.3 A_{OUT})

Parameter	12 V_{IN}
Loop bandwidth (kHz)	8.76
Phase margin	77°
Slope (20 dB / decade)	–0.91
Gain margin (dB)	**–9.4** (1)
Slope (20 dB / decade)	–0.17
Rolloff frequency (kHz)	45.6

(1) Loop bandwidth close to 10 kHz results in gain margin (GM) of –10 dB; typically –15 dB is recommended to prevent drain jitter, but DCM results in safe operation.

Loop has been tweaked for maximum bandwidth, limit is the gain bandwidth G_{BW} of the transconductance amplifier, estimated 1 MHz. The amplifier pole causes the phase rolloff.

3 Waveforms

3.1 Switching

3.1.1 Transistor Q1 Operating in Deep DCM

3.1.1.1 Drain to Source

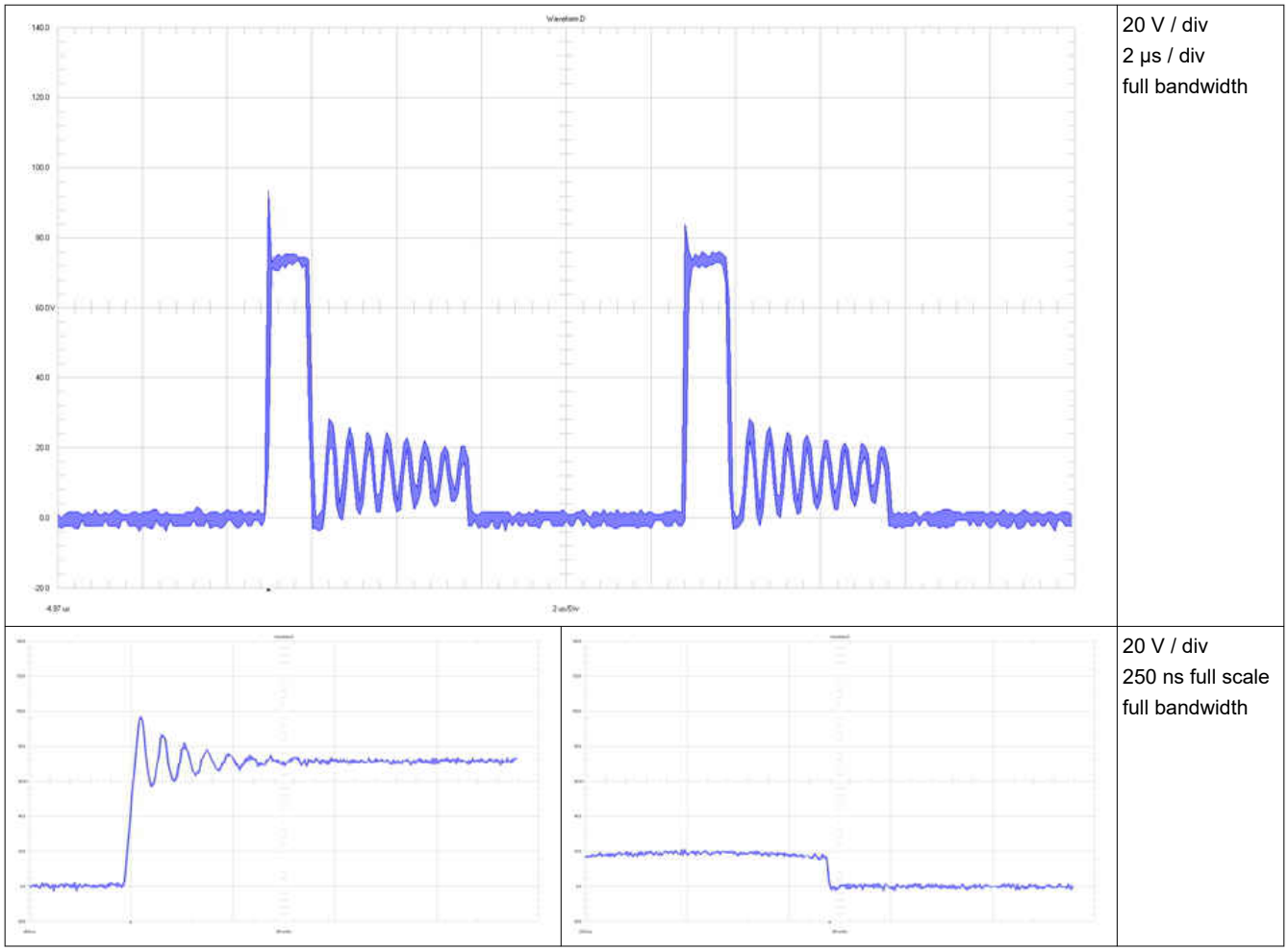


Figure 3-1. Switching Q1 (Drain-Source)

3.1.1.2 Gate to Source

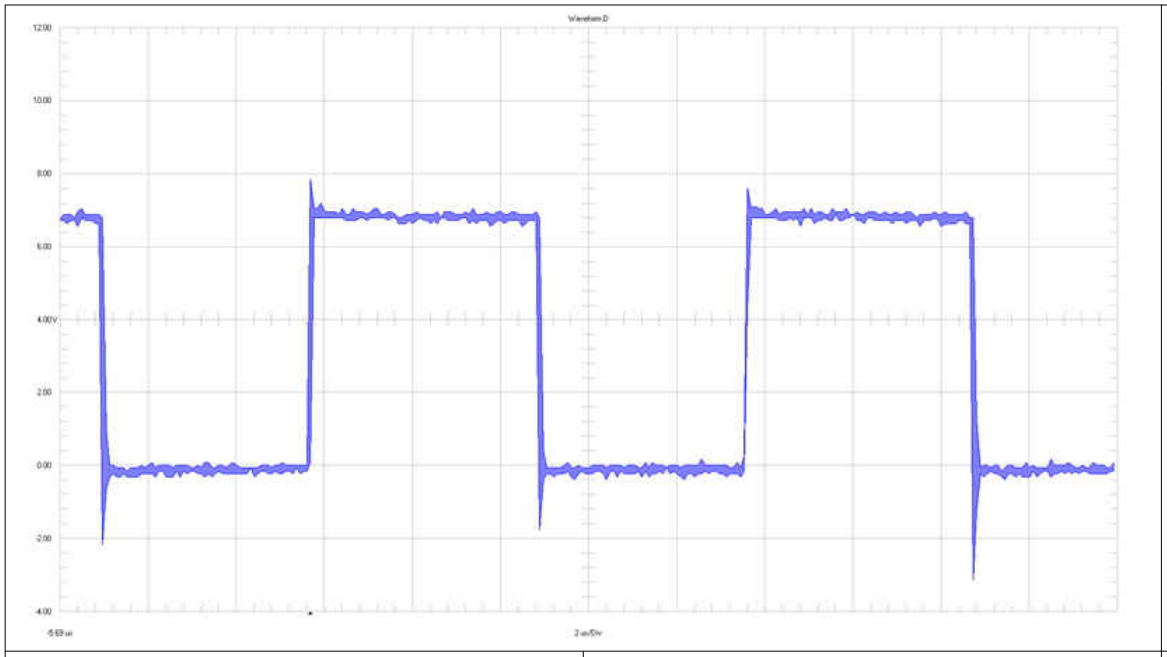


Figure 3-2. Switching Q1 (Gate-Source)

3.1.2 Diode D3 (Referenced to V_{OUT})

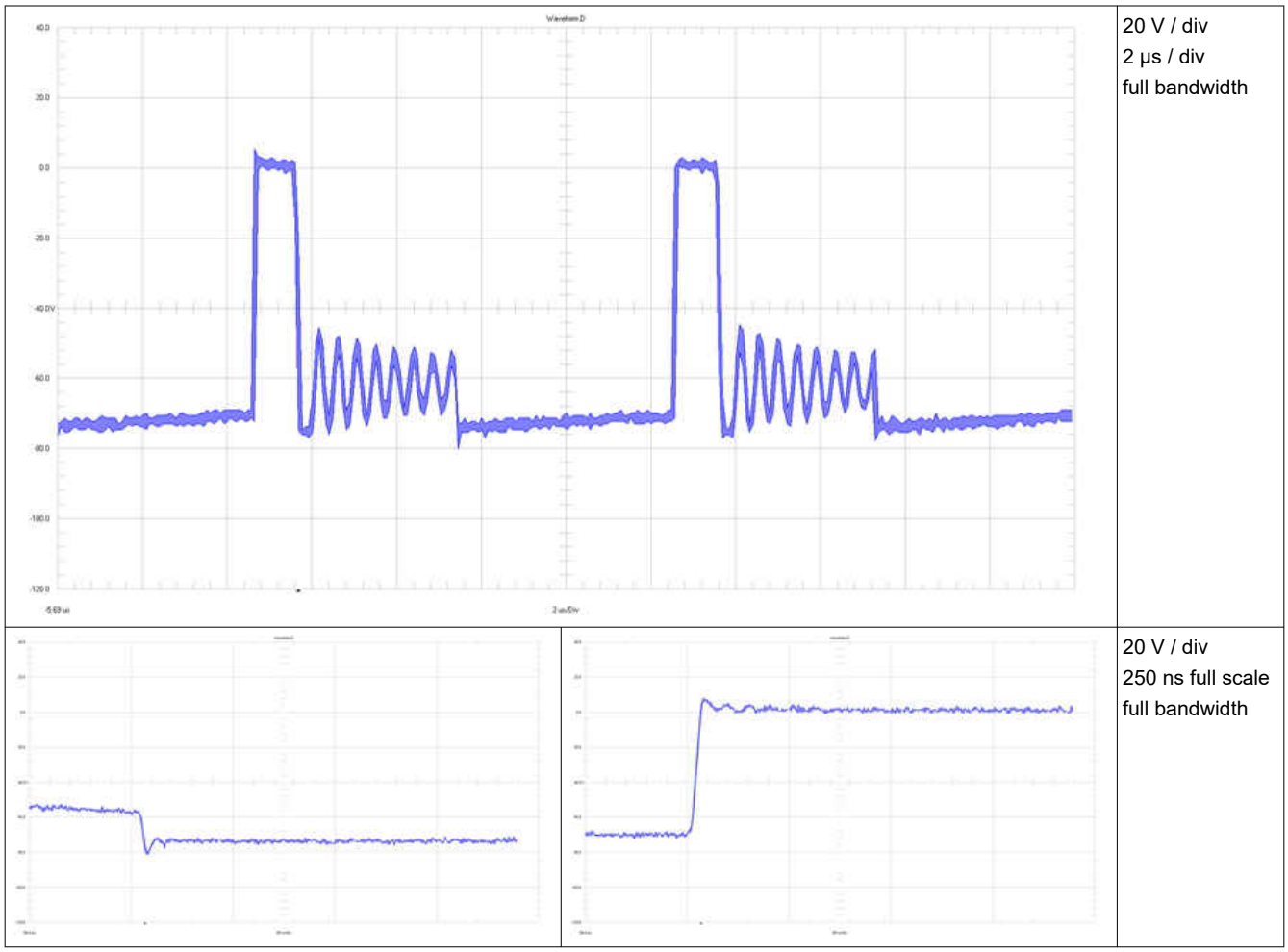


Figure 3-3. Switching D3, no Q_{rr} Ringing in DCM, no need for any RC Snubber, Low EMI

3.2 Output Voltage Ripple

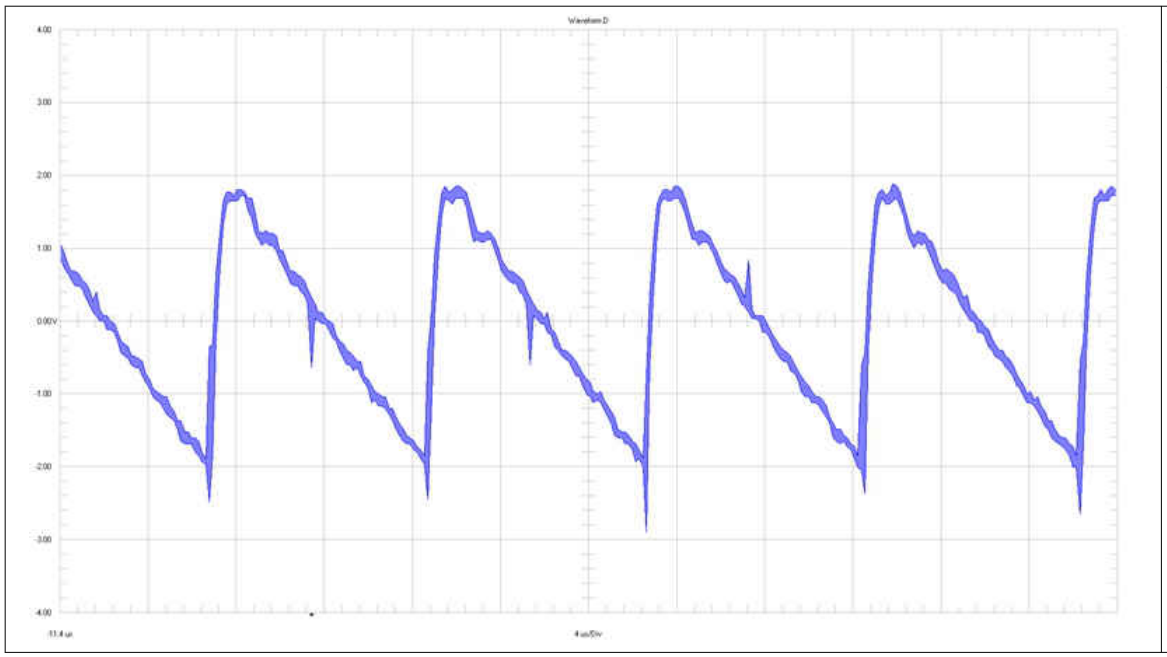


Figure 3-4. Output Voltage Ripple 2 V_{PP} Caused by 5.75 A_{PK} Ripple Current Across Output Cap

3.3 Input Voltage Ripple

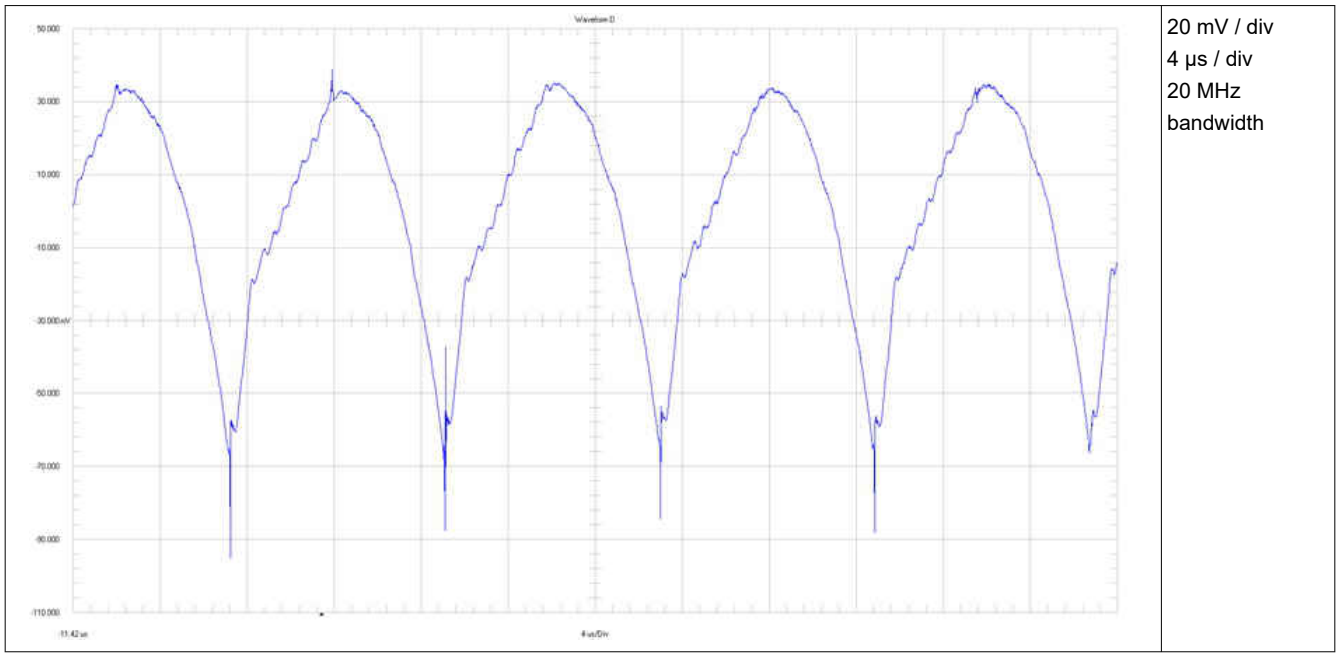


Figure 3-5. Input Voltage Ripple

3.4 Start-Up Sequence

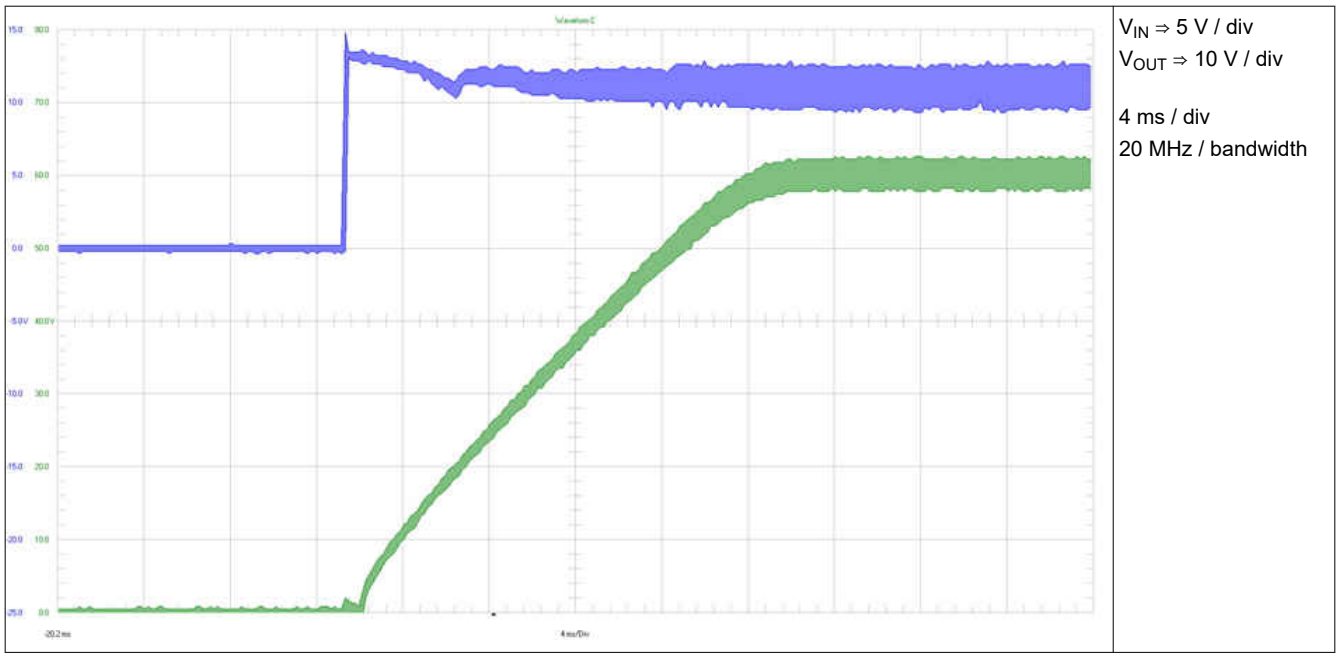


Figure 3-6. Start-Up

3.5 Shutdown Sequence

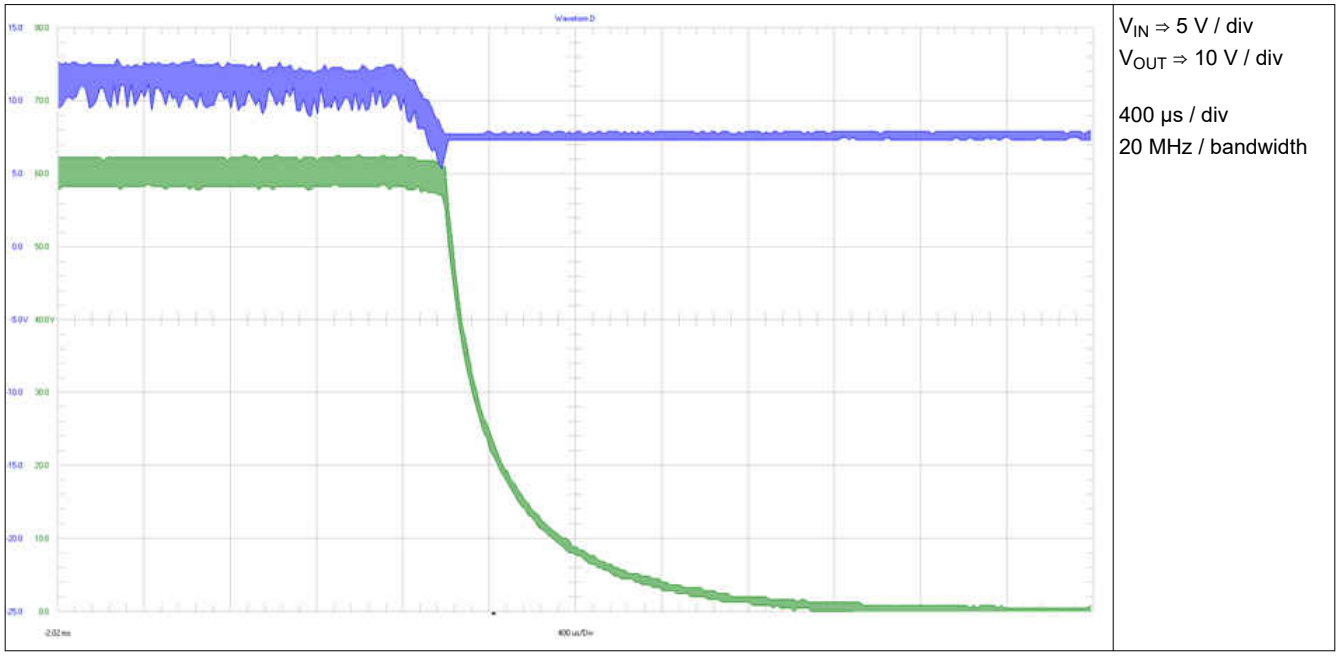


Figure 3-7. Shutdown

A Modulating the Output Voltage

A.1 Revision B

A.1.1 Bode Plot

Three output capacitors (2.2 µF, 100 V, 1210, X7R) are assembled in revision B of this reference design.

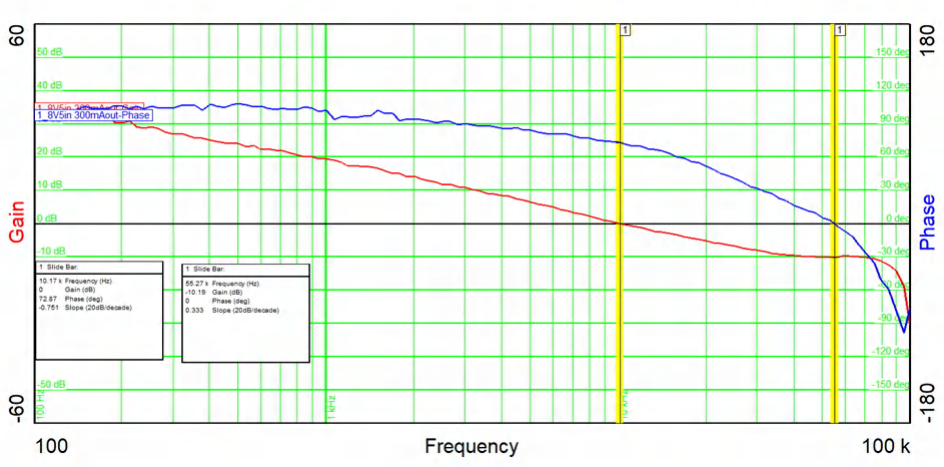


Figure A-1. Bode Plot, Revision B, Worst Case is 8.5 V_{IN}, 0.3 A_{OUT}

The plot in Figure A-1 shows the worst-case Bode plot for output capacitance, 3 × 2.2 µF and f_{CO} 10 kHz (R13 4.02 kΩ, C16 100 nF, C15 390 pF); despite achieved crossover frequency, f_{CO}, 10 kHz the modulated sinusoidal waveform showed non linearity beyond f_{mod} 40 Hz+, similar to the simulation seen in Figure A-2: the output voltage drops, discharge current of output capacitor drops, the sinusoidal function converts into an e-function.

A.1.2 Simulation

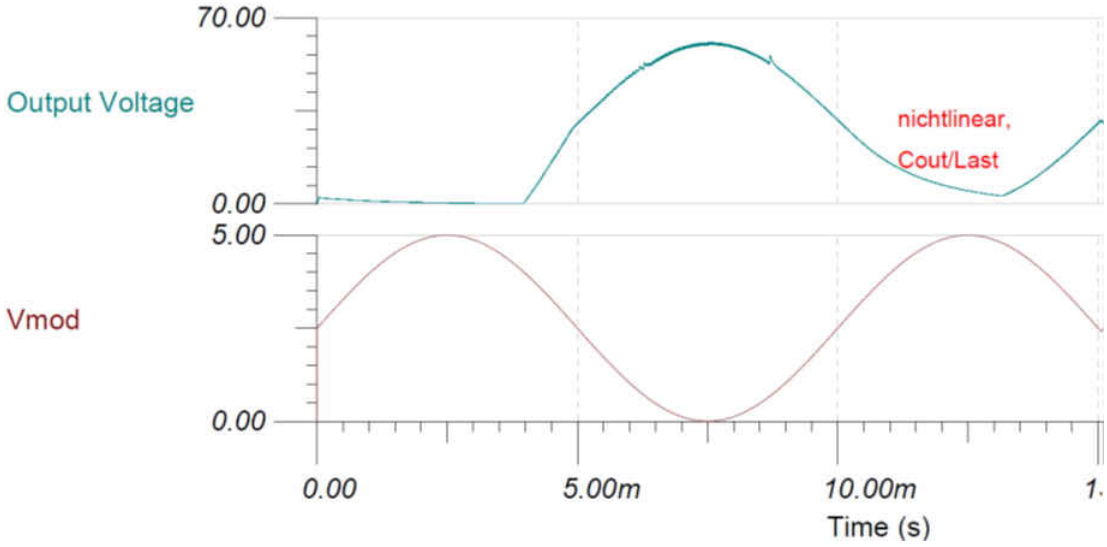


Figure A-2. Nonlinearity Between 11 ms and 13 ms, Sinusoidal Function Converts to e-function, Slow Discharging of C_{OUT}

A.1.3 Measured Waveforms

With the measurements of the Revision B hardware, the effective output capacitance was estimated to 4 µF to 5 µF.

A.1.3.1 Sinus 40 Hz

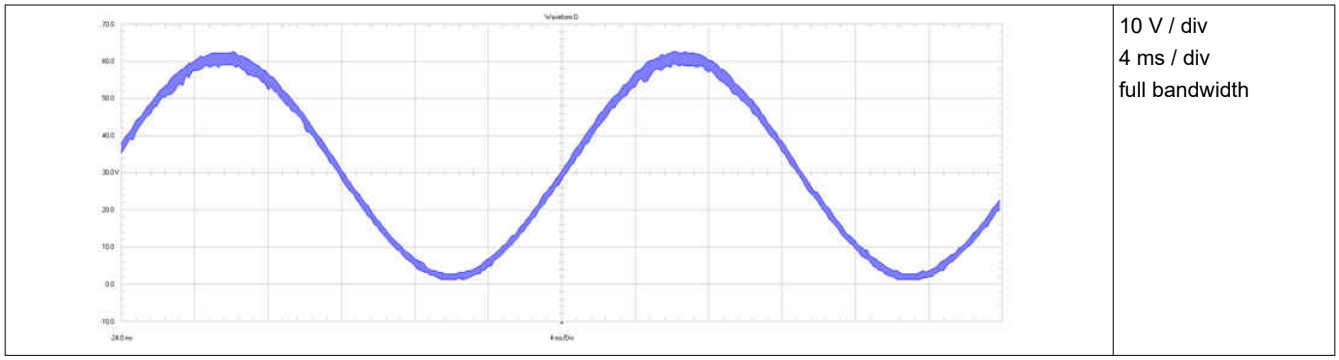


Figure A-3. Modulation Sinus (5 V_{PP} + 2.5 V) 40 Hz Only, 12 V_{IN}, 200-Ω Load ⇒ OK

A.1.3.2 Sinus 100 Hz

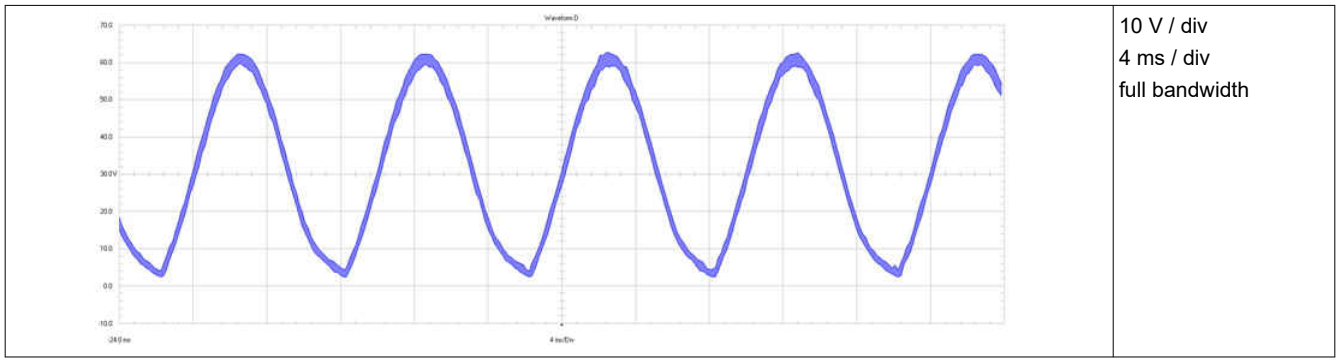


Figure A-4. Modulation Sinus (5 V_{PP} + 2.5 V) 100 Hz, 12 V_{IN}, 200-Ω Load

Note

The hardware shows the nonlinearity at F_{mod} 100 Hz similar to simulation.

A.1.3.3 Sawtooth 1

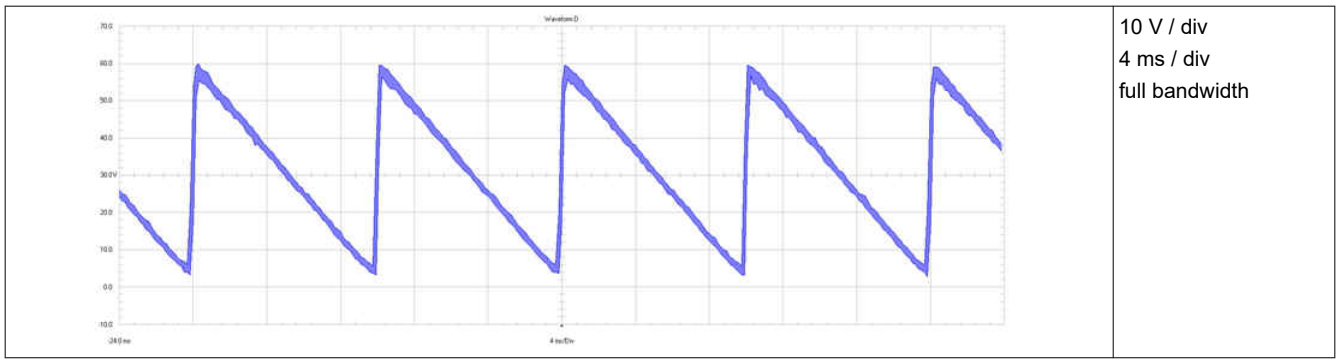
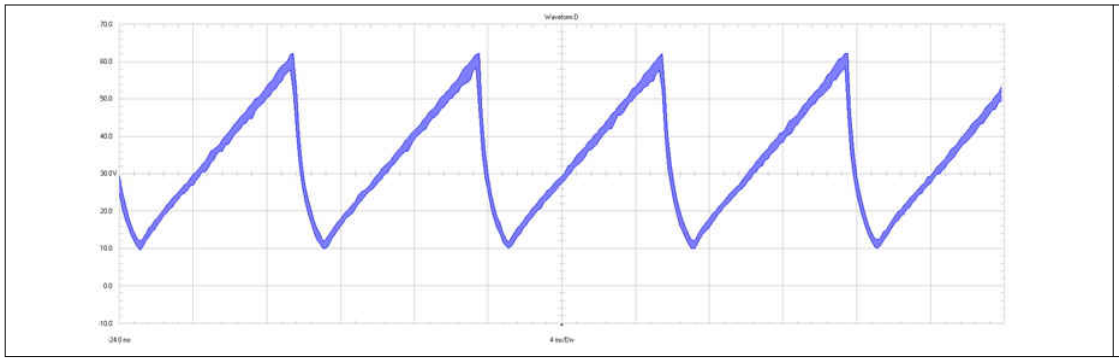


Figure A-5. Modulation Sawtooth 1 (5 V_{PP} + 2.5 V) 100 Hz, 12 V_{IN}, 200-Ω Load

The positive slope is acceptable, increasing duty cycle, **charging** the output capacitor.

A.1.3.4 Sawtooth 2



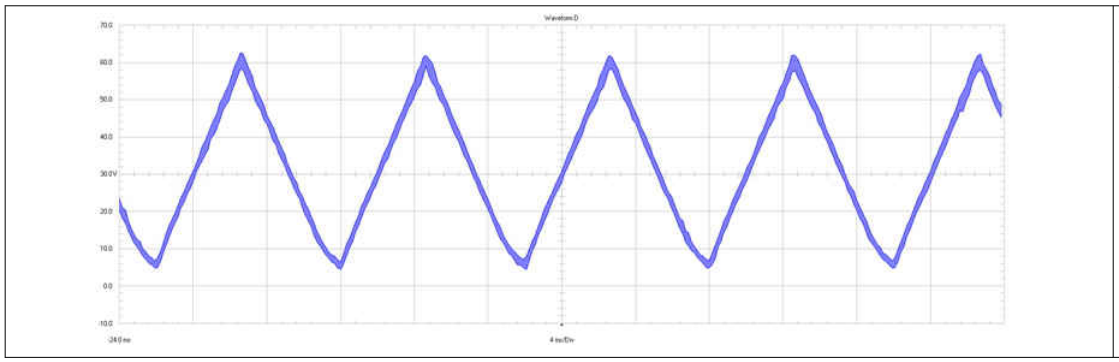
10 V / div
4 ms / div
full bandwidth

Figure A-6. Modulation Sawtooth 2 (5 V_{PP} + 2.5 V) 100 Hz, 12 V_{IN}, 200-Ω Load

Note

The negative slope is limited due to stored energy at the output capacitor.

A.1.3.5 Pure Triangle



10 V / div
4 ms / div
full bandwidth

Figure A-7. Modulation Pure Triangle (5 V_{PP} + 2.5 V) 100 Hz, 12 V_{IN}, 200-Ω Load

A.1.3.6 Conclusion

The reason for the nonlinearity in before minimum of the sinusoidal waveform at a certain point is that the small load current is not able to discharge the output capacitor fast enough; the output voltage cannot follow the modulation voltage anymore.

To enable high frequency modulation or more negative slope needs synchronous rectification in FPWM mode to discharge the output capacitor towards the power stage.

The output capacitance needs to be decreased, and the loop needs to be adjusted to the bigger load pole:

- Reduce gain to keep F_{CO} around 10 kHz
- Set compensation zero to 2 × load pole
- Adjust compensation pole to keep pole frequency around 100 kHz. For achieving higher linearity at F_{mod}, the output capacitance must be further reduced.

A rough linear estimation can be obtained with the following equations.

$$\text{Energy at output capacitor: } Q = C \times V = I \times t \tag{1}$$

Use Equation 2 to calculate the current needed to reduce the output voltage at an output capacitance of 5 µF by –10 V within 1 ms.

$$\text{Time discrete: } I = \frac{C \times du}{dt} = \frac{5\ \mu F \times 10\ V}{1\ ms} = 50\ mA \tag{2}$$

Equation 3 shows the current across a load resistance of 200 Ω at a low output voltage of 10 V.

$$\text{Load current: } I = 10\ V / 200\ \Omega = 50\ mA \tag{3}$$

Means by decreasing the sinusoidal output voltage below 10 V, the output is no longer able to follow the modulation, the sinusoidal voltage moves towards an e-function, resistive discharging of the output capacitor 5 µF. The non-synchronous rectification and the simple Schottky diode allows no current to go in the opposite direction to the power stage – the resolution steps are shown in the following list:

- Minimize output capacitance
- Synchronous rectification, **no** diode emulation
- Digital pre-distortion of the modulating signal, but negative slope is always limited

A.2 Revision C

The output capacitance decreased to 1 × 2.2 µF; 100 V; 1210; X7R.

A.2.1 Bode Plot

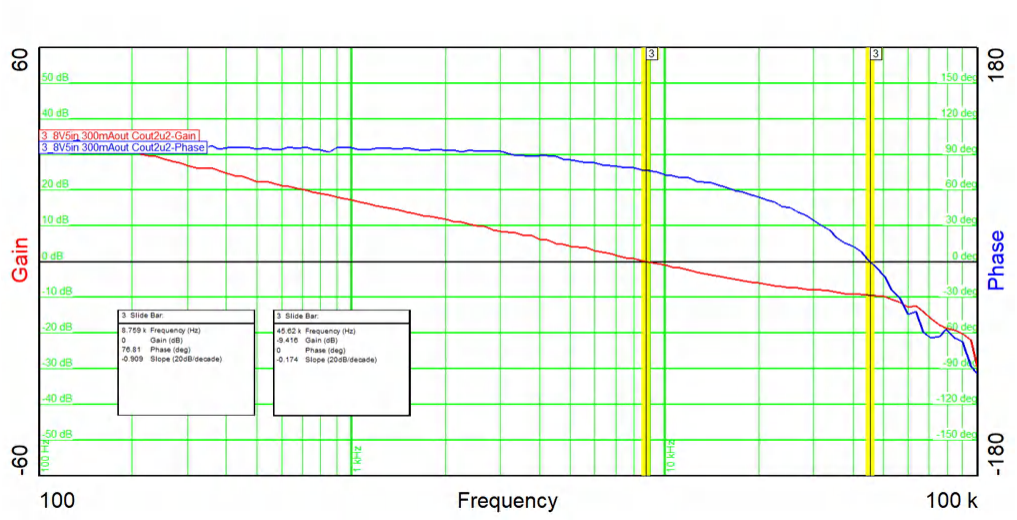


Figure A-8. Bode Plot 8.5 V_{IN}, 0.3 A_{OUT}

Single output capacitor 2.2 µF (with 100-V rating); R16 1 kΩ ; C16 100 nF ; C15 1.5 nF, loop bandwidth again tweaked close to 10 kHz; crossover frequency 9 kHz, phase margin 77°, gain margin –10 dB.

A.2.2 Measured Waveforms

A.2.2.1 Sinus 120 Hz

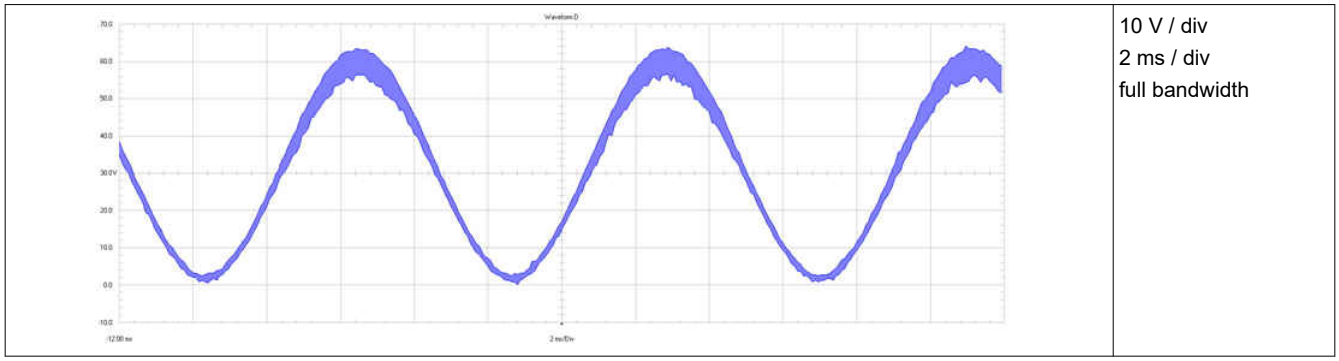


Figure A-9. Modulation Sinusoidal (5 V_{PP} + 2.5 V) 120 Hz, 12 V_{IN}, 200-Ω Load

Modulation set to 120 Hz, sinusoidal output voltage looks promising, but the output ripple voltage is increased by lowering output impedance.

Ripple reduction – instead of using a single output capacitor 2.2 µF,100 V, X7R, 1210, a small improvement can be achieved by using several smaller capacitors in parallel ⇒ 3 × 1 µF, 100 V, X7R, 1206, that is, Murata GCJ31CR72A105KA01.

A.2.2.2 Sawtooth 1

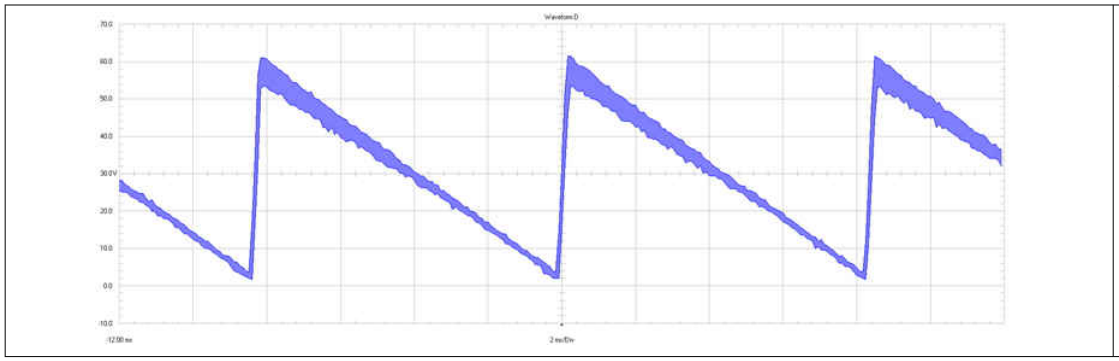


Figure A-10. Modulation Sawtooth 1 (5 V_{PP} + 2.5 V) 120 Hz, 12 V_{IN}, 200-Ω Load

A.2.2.3 Sawtooth 2

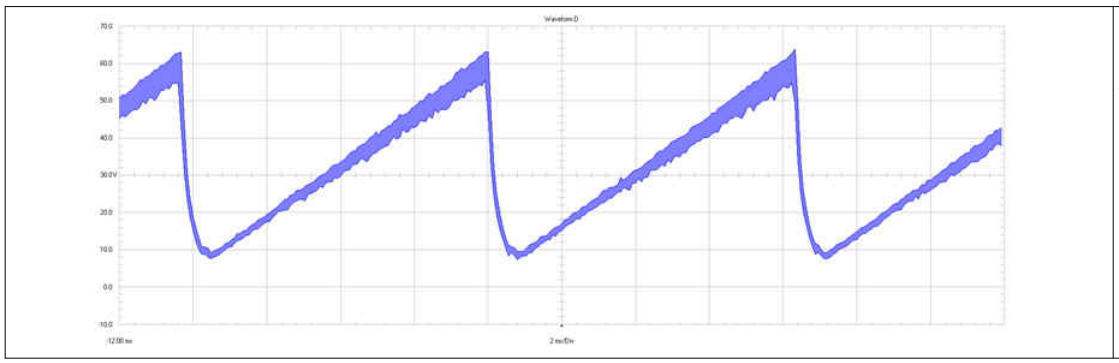


Figure A-11. Modulation Sawtooth 2 (5 V_{PP} + 2.5 V) 120 Hz, 12 V_{IN}, 200-Ω Load

Note

The negative slope is always limited, using non synchronous rectification.

A.2.2.4 Pure Triangle

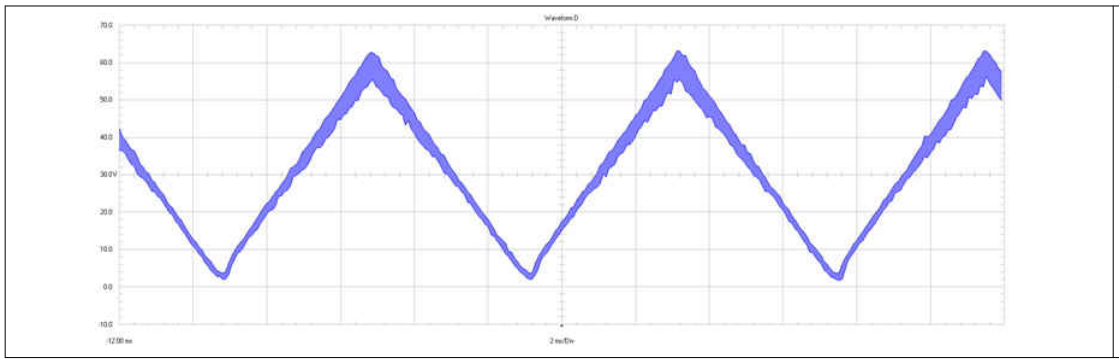


Figure A-12. Modulation Pure Triangle (5 V_{PP} + 2.5 V) 120 Hz, 12 V_{IN}, 200-Ω Load

A.2.3 Analysis Capacitor 1 µF, 100 V, X7R, 1206

This analysis is done for Murata GCJ31CR72A105KA01.

A.2.3.1 DC-Bias

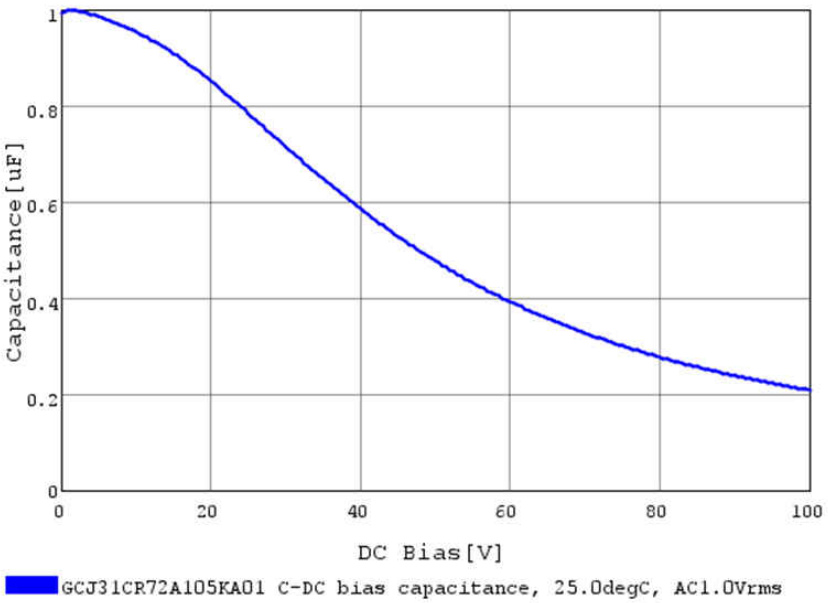


Figure A-13. Effective Capacitance vs DC Bias

Figure A-13 illustrates that with 60-V_{DC} output voltage the effective capacitance of the 1-µF capacitor is just 400 nF.

A.2.3.2 Resistance (ESR)

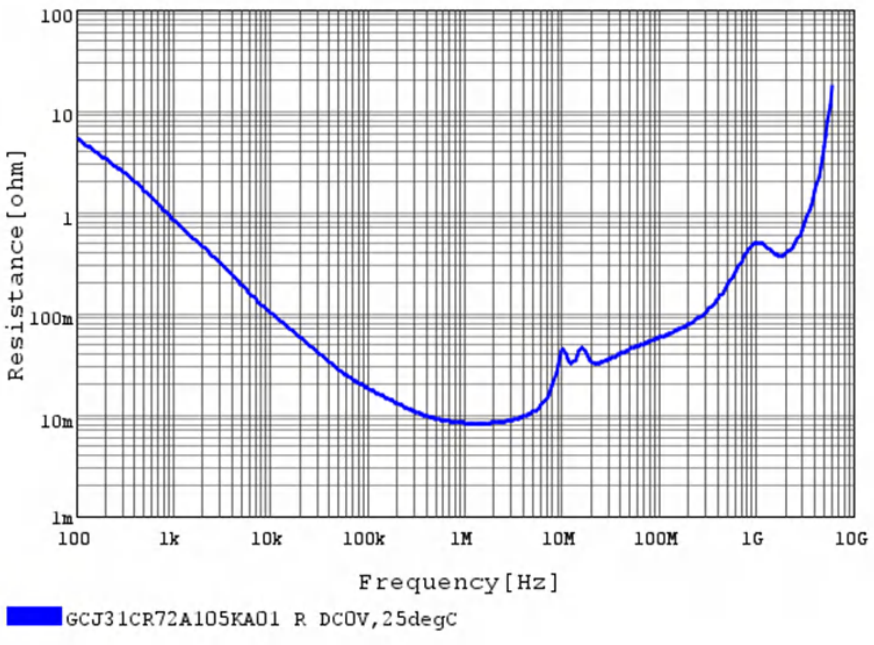


Figure A-14. Resistance (ESR) vs Frequency

In Figure A-14, the resistance (ESR) at the fundamental 100 kHz (switching frequency of the circuit) is at 20 mΩ.

A.2.3.3 Reactance

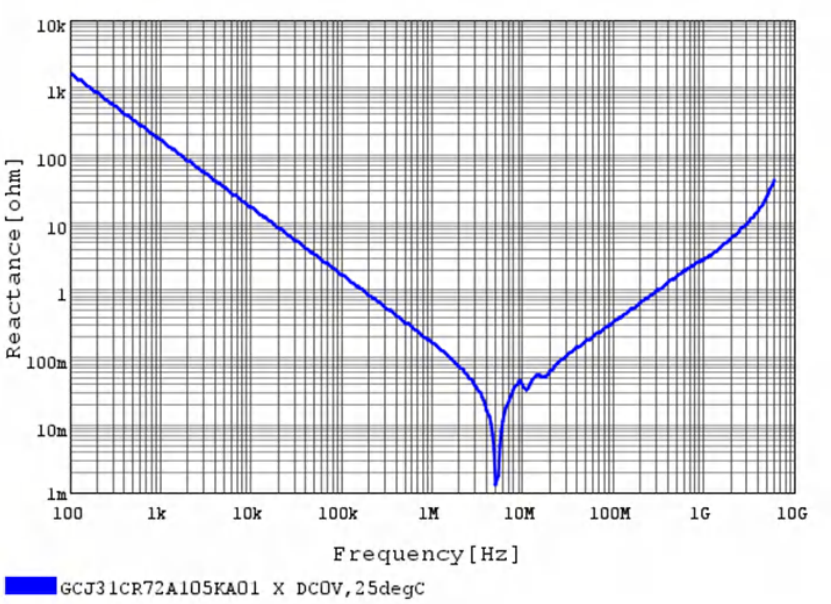


Figure A-15. Reactance vs Frequency

The reactance (seen in Figure A-15) at fundamental (100 kHz) results into 2 Ω.

A.2.3.4 Impedance

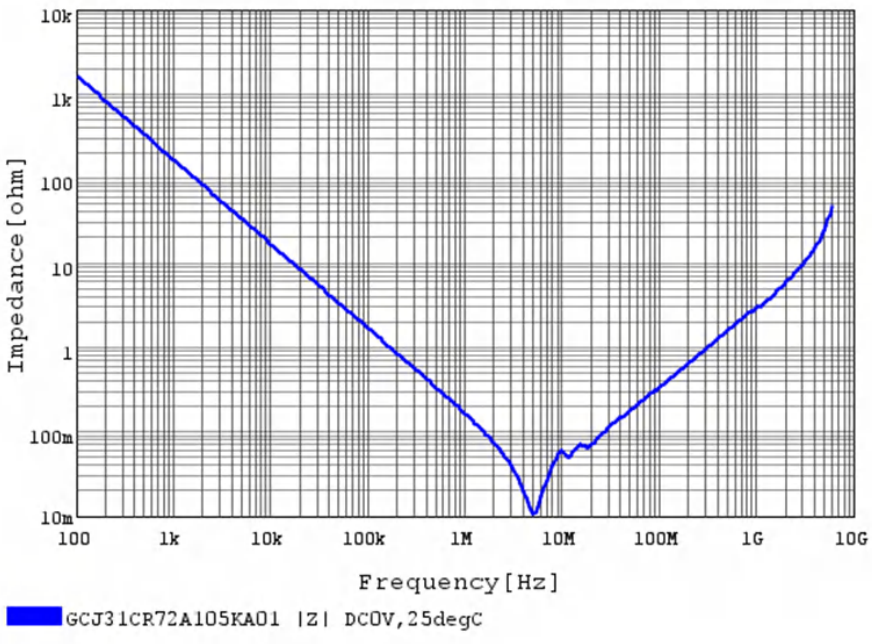


Figure A-16. Impedance vs Frequency

The reactance is dominant. The impedance (Figure A-16) has almost the same value.

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