Test Report: PMP31247

Automotive 9-W Dual Buck Converter Reference Design for C2000™ MCU

Description

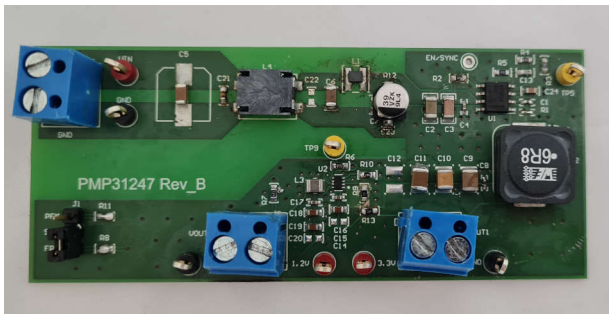
This reference design is an automotive power supply for C2000™ generating two output voltage rails from a nominal 12-V battery. LMR23630-Q1 converts the input voltage into a regulated 3.3-V rail; TPS628501-Q1, supplied by the first output, generates a 1.2-V output rail. Both converters are operating in forced pulse-width modulation (FPWM), to minimize output ripple and optimize load transient response. All the tests were done on the PMP31047 revision B board.

Features

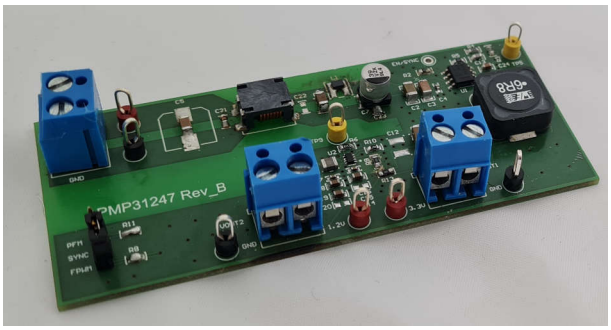
- Dual output (3.3 V and 1.2 V)
- Optimized and tested for conducted EMI (CISPR25 Class 5)
- High-efficiency conversion due to use of synchronous rectification
- Design was built and tested

Applications

- DC-fast charging
- Traction inverter-high voltage
- Automotive HVAC compressor module



Top of Board



Angled Board Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	6.0 V – 26.0 V
V_{OUT1}	3.3 V
I_{OUT1}	2.0 A, 2.5 A peak
V_{OUT2}	1.2 V
I_{OUT2}	1.0 A

1.2 Dimensions

The outline of the revision B board is 37.60 mm × 89.48 mm.

2 Testing and Results

2.1 Efficiency Graphs

Efficiency for V_{OUT1} is shown in the following figure. The efficiency was measured with both the CMC and input filters.

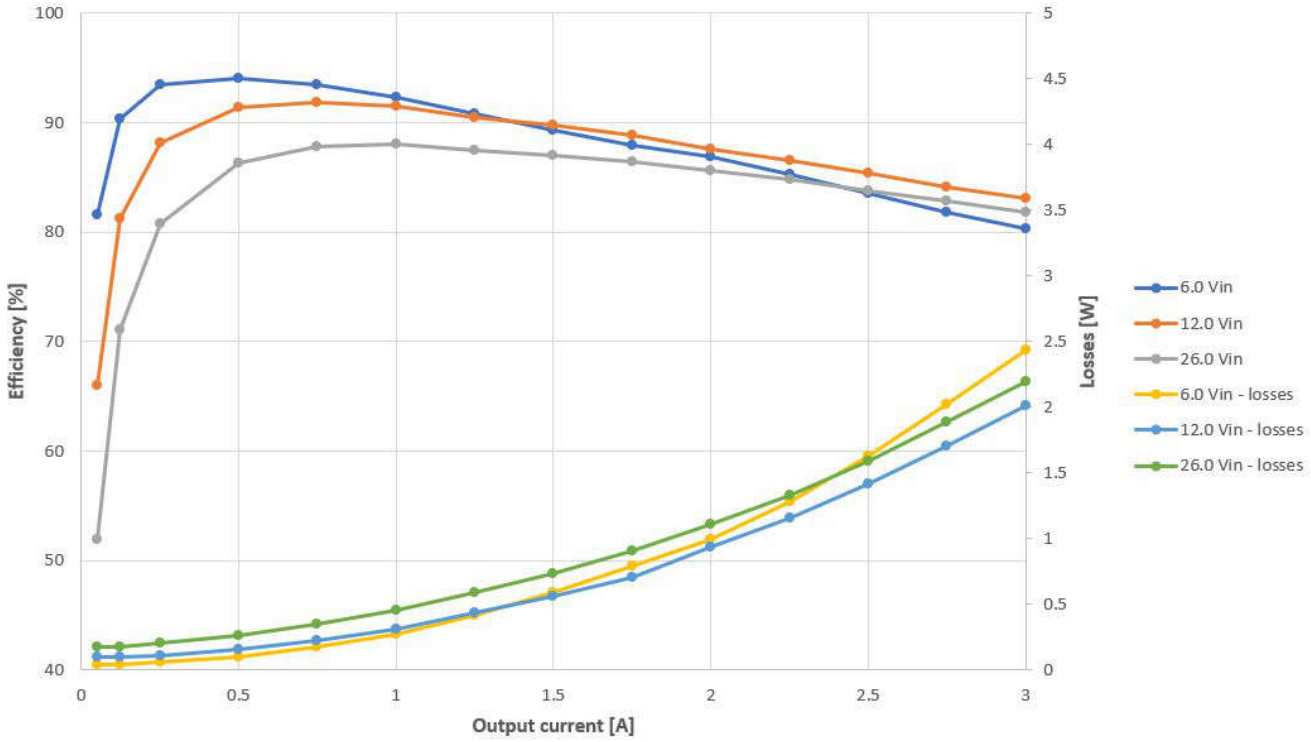


Figure 2-1. Efficiency Graph of V_{OUT1}

2.2 Efficiency Data

Efficiency data is shown in the following tables.

Table 2-1. Efficiency Data V_{OUT1}, V_{IN} = 6 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
6.01	0.038	3.316	0.057	0.230	0.188	0.042	81.6
6.01	0.081	3.315	0.132	0.486	0.439	0.047	90.4
6.05	0.151	3.315	0.257	0.910	0.850	0.060	93.4
6.03	0.295	3.315	0.505	1.778	1.673	0.105	94.1
6.01	0.446	3.315	0.756	2.682	2.505	0.176	93.4
6.05	0.597	3.314	1.007	3.615	3.337	0.278	92.3
6.03	0.757	3.313	1.251	4.566	4.145	0.421	90.8
6.07	0.918	3.312	1.501	5.566	4.971	0.594	89.3
6.05	1.090	3.310	1.750	6.588	5.793	0.795	87.9
6.03	1.264	3.309	2.001	7.616	6.621	0.994	86.9
6.06	1.442	3.307	2.252	8.733	7.447	1.285	85.3
6.03	1.639	3.305	2.500	9.888	8.263	1.626	83.6
6.01	1.849	3.303	2.751	11.109	9.087	2.022	81.8
5.98	2.063	3.301	3.002	12.343	9.910	2.433	80.3

Table 2-2. Efficiency Data V_{OUT1}, V_{IN} = 12 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
12.08	0.024	3.315	0.057	0.285	0.188	0.097	66.0
12.08	0.045	3.315	0.132	0.540	0.439	0.101	81.3
12.07	0.080	3.315	0.257	0.964	0.850	0.114	88.2
12.06	0.152	3.315	0.505	1.831	1.673	0.157	91.4
12.05	0.226	3.314	0.756	2.727	2.505	0.222	91.9
12.05	0.303	3.314	1.007	3.648	3.337	0.311	91.5
12.04	0.380	3.313	1.250	4.578	4.141	0.436	90.5
12.03	0.461	3.312	1.502	5.541	4.975	0.566	89.8
12.02	0.527	3.310	1.701	6.338	5.630	0.708	88.8
12.01	0.629	3.308	2.001	7.557	6.619	0.937	87.6
12.00	0.717	3.306	2.252	8.608	7.445	1.162	86.5
11.99	0.807	3.303	2.500	9.676	8.258	1.418	85.3
11.98	0.901	3.300	2.751	10.788	9.078	1.710	84.2
11.97	0.995	3.297	3.002	11.910	9.898	2.013	83.1

Table 2-3. Efficiency Data V_{OUT1}, V_{IN} = 26 V

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	P_{LOSS} (W)	Efficiency (%)
25.87	0.014	3.315	0.057	0.362	0.188	0.174	52.0
25.87	0.024	3.315	0.133	0.618	0.439	0.179	71.0
25.86	0.041	3.314	0.257	1.053	0.850	0.202	80.8
25.85	0.075	3.314	0.505	1.939	1.673	0.266	86.3
25.85	0.110	3.314	0.756	2.854	2.505	0.349	87.8
25.89	0.146	3.313	1.007	3.788	3.336	0.452	88.1
25.89	0.183	3.312	1.250	4.733	4.140	0.593	87.5
25.88	0.221	3.311	1.501	5.709	4.970	0.739	87.1
25.87	0.259	3.309	1.750	6.703	5.791	0.912	86.4
25.86	0.299	3.308	2.001	7.727	6.619	1.108	85.7
25.85	0.340	3.306	2.252	8.781	7.445	1.336	84.8
25.83	0.381	3.303	2.500	9.852	8.258	1.594	83.8
25.83	0.425	3.301	2.751	10.967	9.081	1.886	82.8
25.83	0.468	3.299	3.002	12.099	9.904	2.195	81.9

2.3 Thermal Images

Thermal images are shown in the following images for V_{IN} = 12 V.

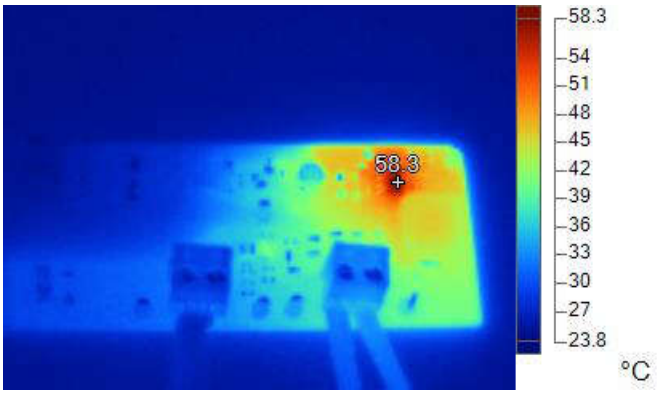


Figure 2-2. Thermal Image at Full DC Load (I_{OUT1} = 2 A, I_{OUT2} = 1 A)

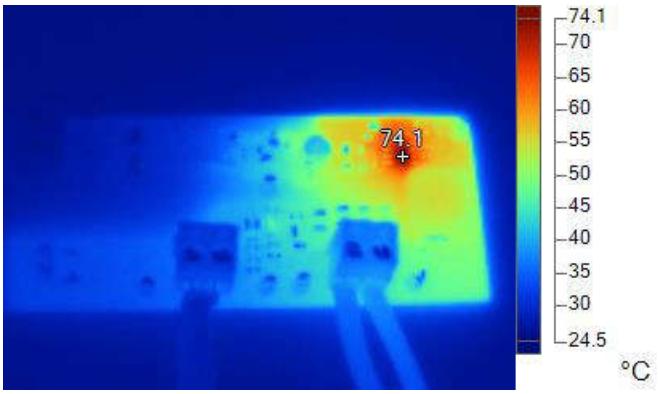
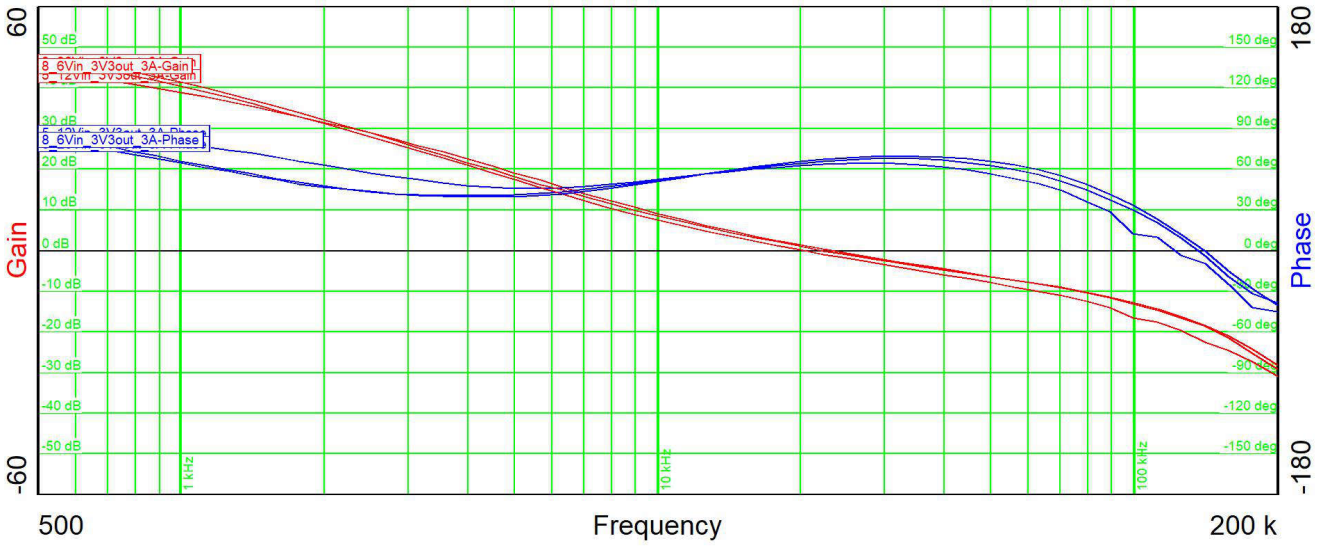


Figure 2-3. Thermal Image at Full Peak Load (I_{OUT1} = 2.5 A, I_{OUT2} = 1 A)

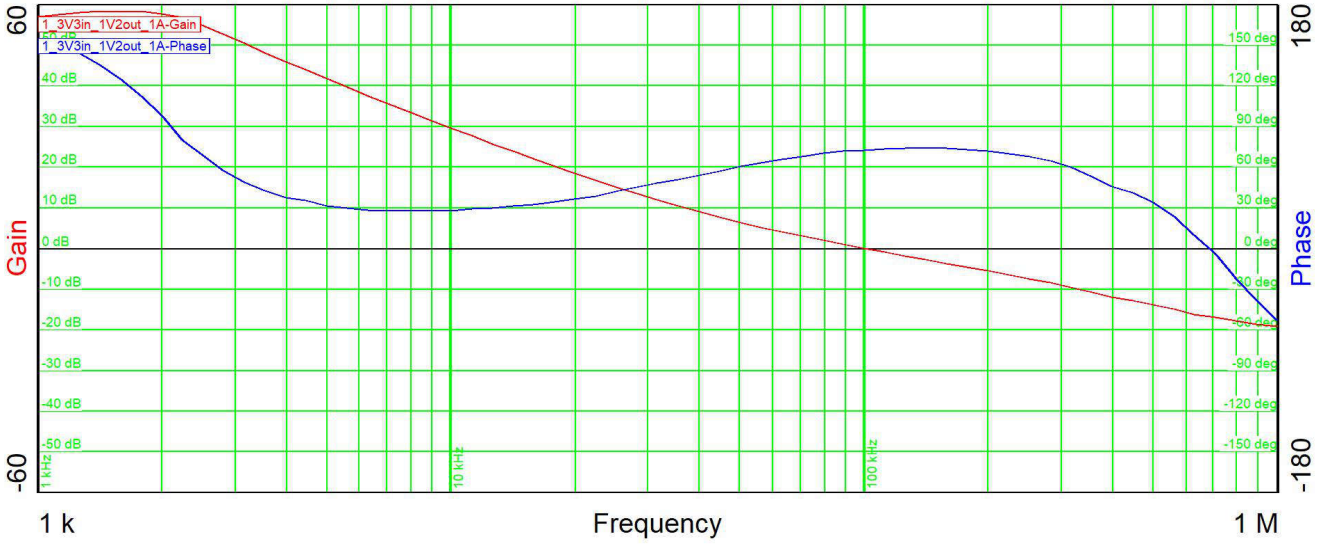
2.4 Bode Plots

Bode plots are shown in the following figures.



6.0 V_{IN}, 3.0 A load current: fco 20.2 kHz, 62 deg phase margin, –19 dB gain margin
12.0 V_{IN}, 3.0 A load current: fco 23.1 kHz, 66 deg phase margin, –18 dB gain margin
26.0 V_{IN}, 3.0 A load current: fco 22.2 kHz, 67 deg phase margin, –18 dB gain margin

Figure 2-4. Bode Plot V_{OUT1} = 3.3 V



3.3 V_{IN}, 1.0 A load current: fco 100. 5 kHz, 72.84 deg phase margin, –17 dB gain margin

Figure 2-5. Bode Plot V_{OUT2} = 1.2 V

2.5 EMI

Conductive EMI measurements are shown in the following figures. The test conditions are V_{IN} = 12 V, I_{OUT1} = 2.5 A (e-load), I_{OUT2} = 1.2 A (1-Ω resistor).

The measurement itself is split into two frequency ranges:

- “HF”, 150 kHz to 30 MHz (LW, MW, SW)
- “FM”, 30 MHz to 108 MHz (VHF)

The limit lines are set as per CISPR25 Class 5 (Peak and Average).

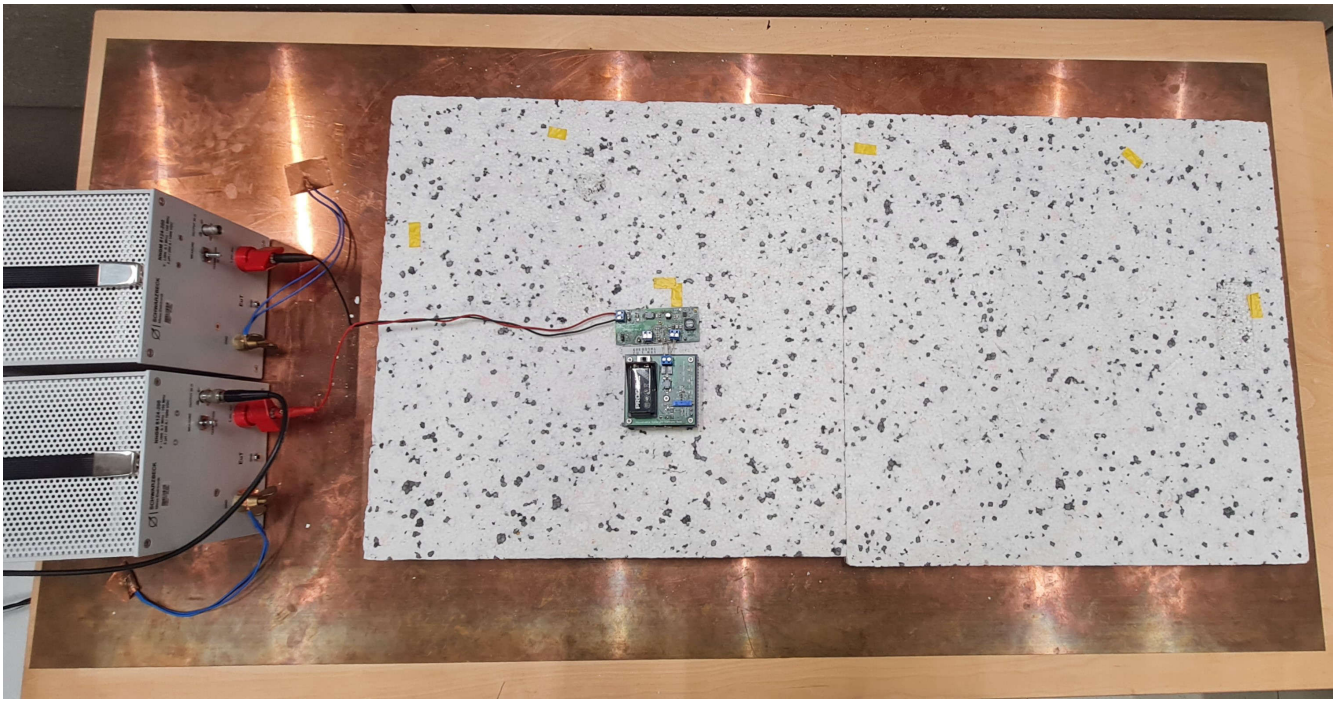


Figure 2-6. EMI Test Setup

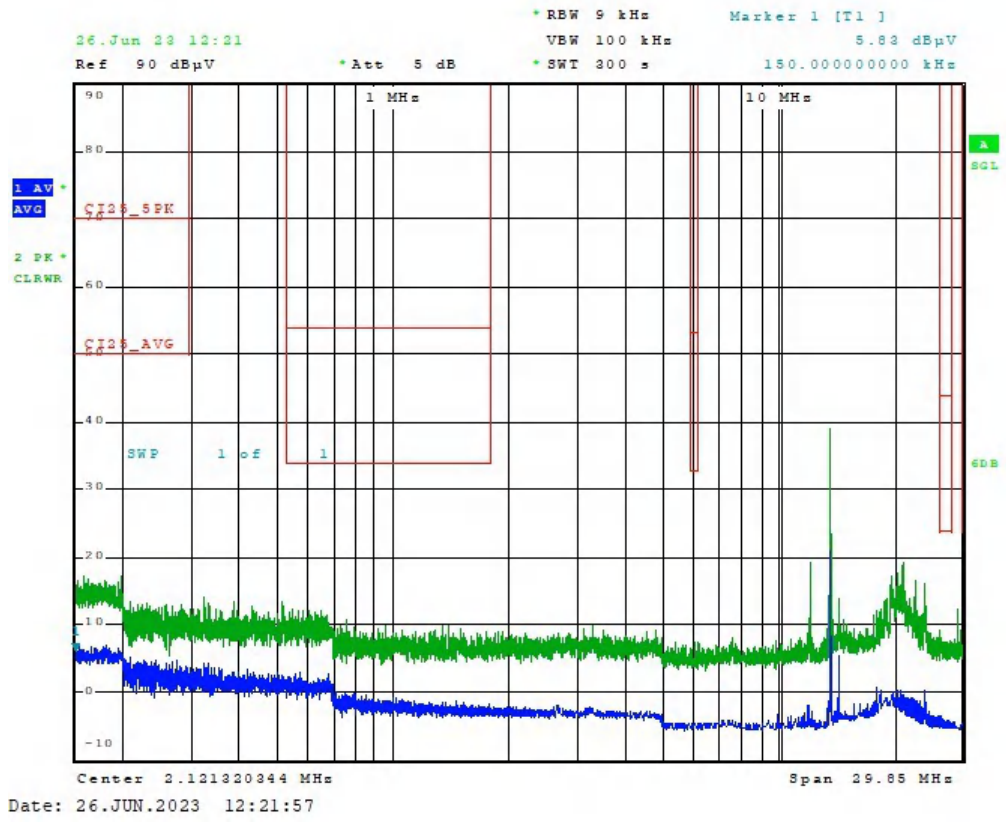


Figure 2-7. Negative Terminal, 150 kHz to 30 MHz, Noise Floor

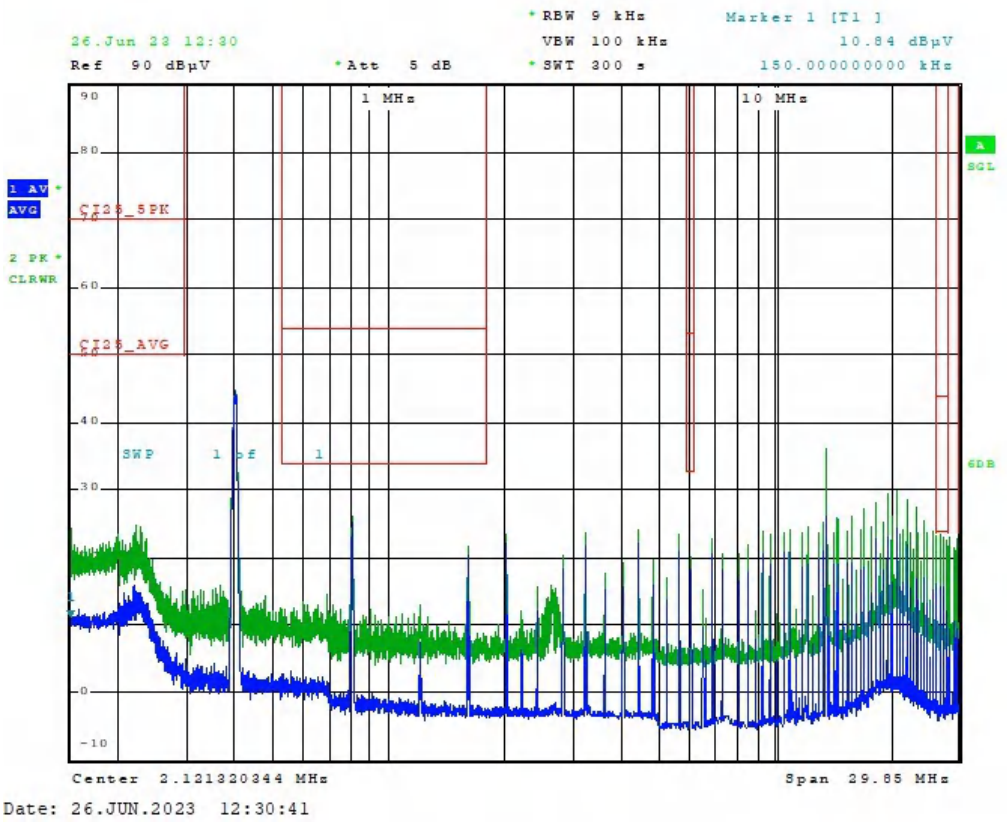


Figure 2-8. Negative Terminal, 150 kHz to 30 MHz, Board ON

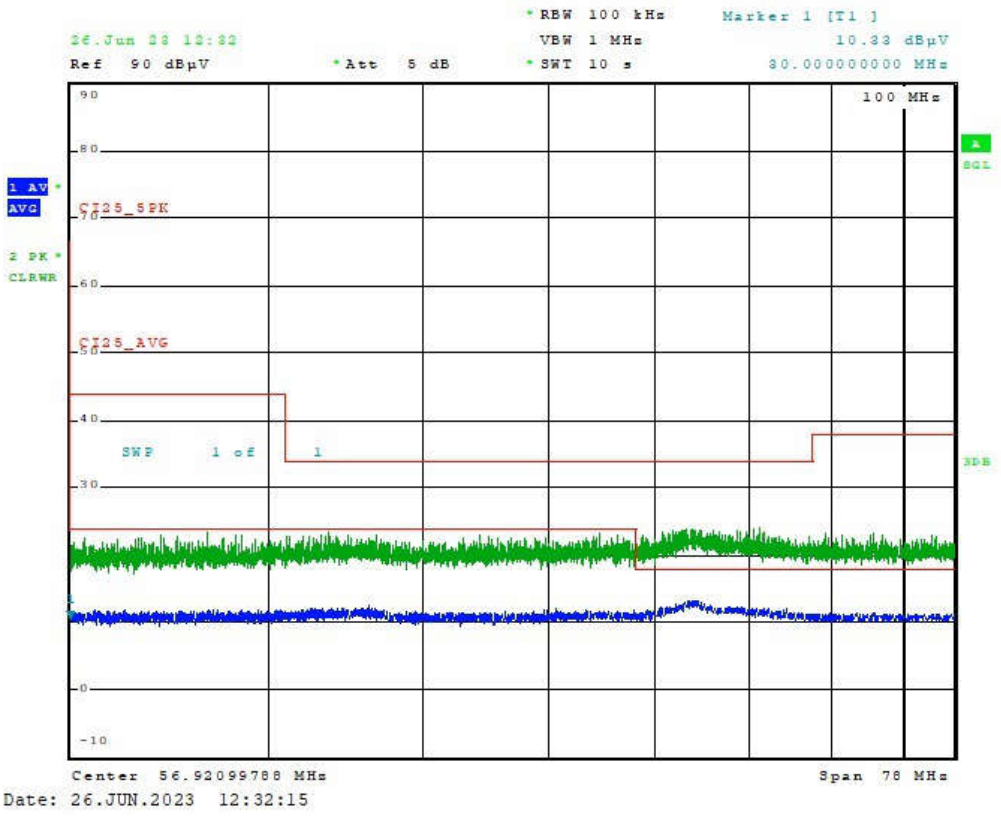


Figure 2-9. Negative Terminal, 30 MHz to 108 MHz, Noise Floor

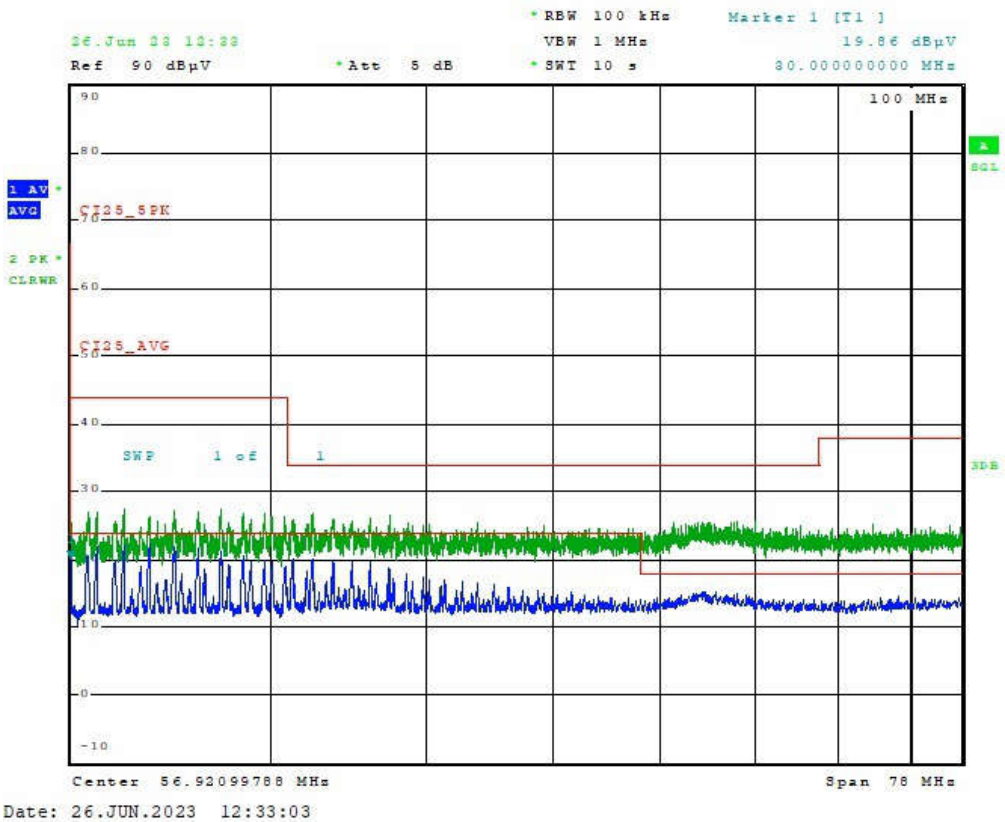


Figure 2-10. Negative Terminal, 30 MHz to 108 MHz, Board ON

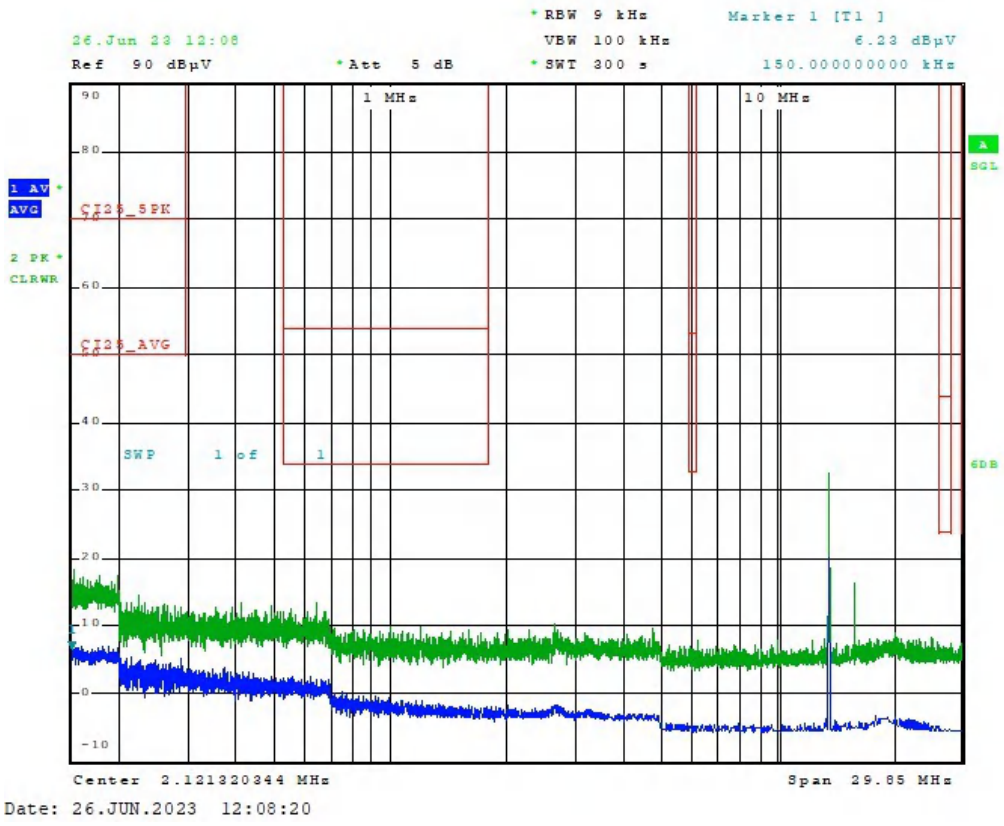


Figure 2-11. Positive Terminal, 150 kHz to 30 MHz, Noise Floor

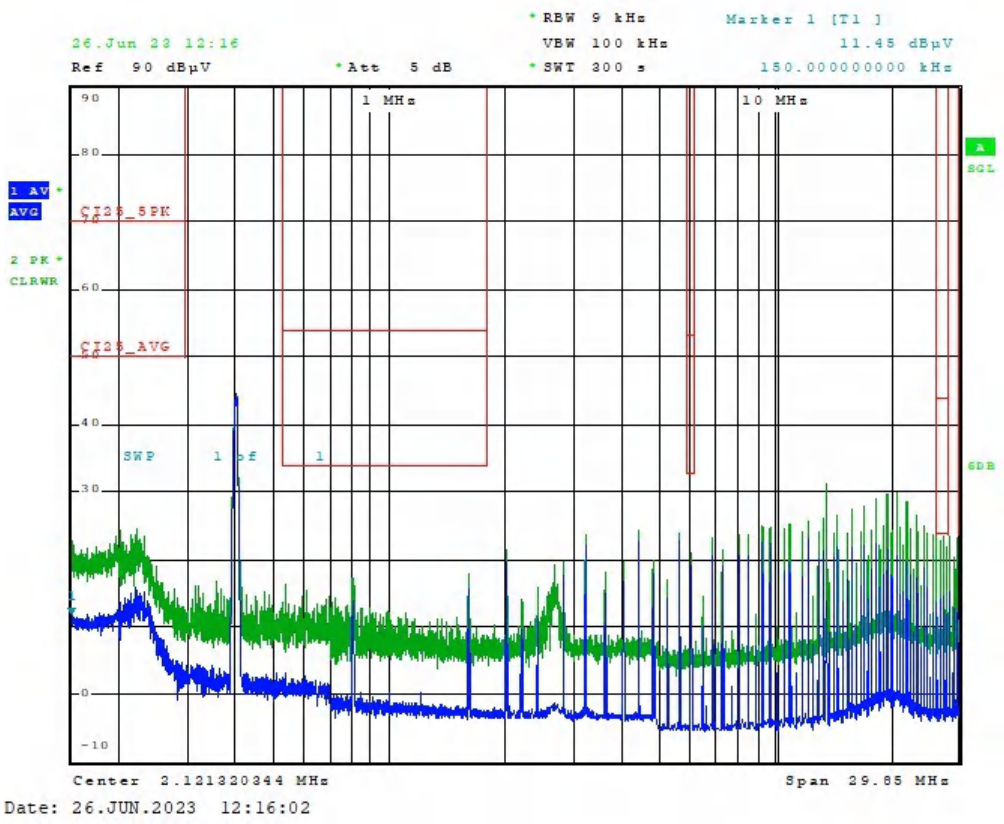


Figure 2-12. Positive Terminal, 150 kHz to 30 MHz, Board ON

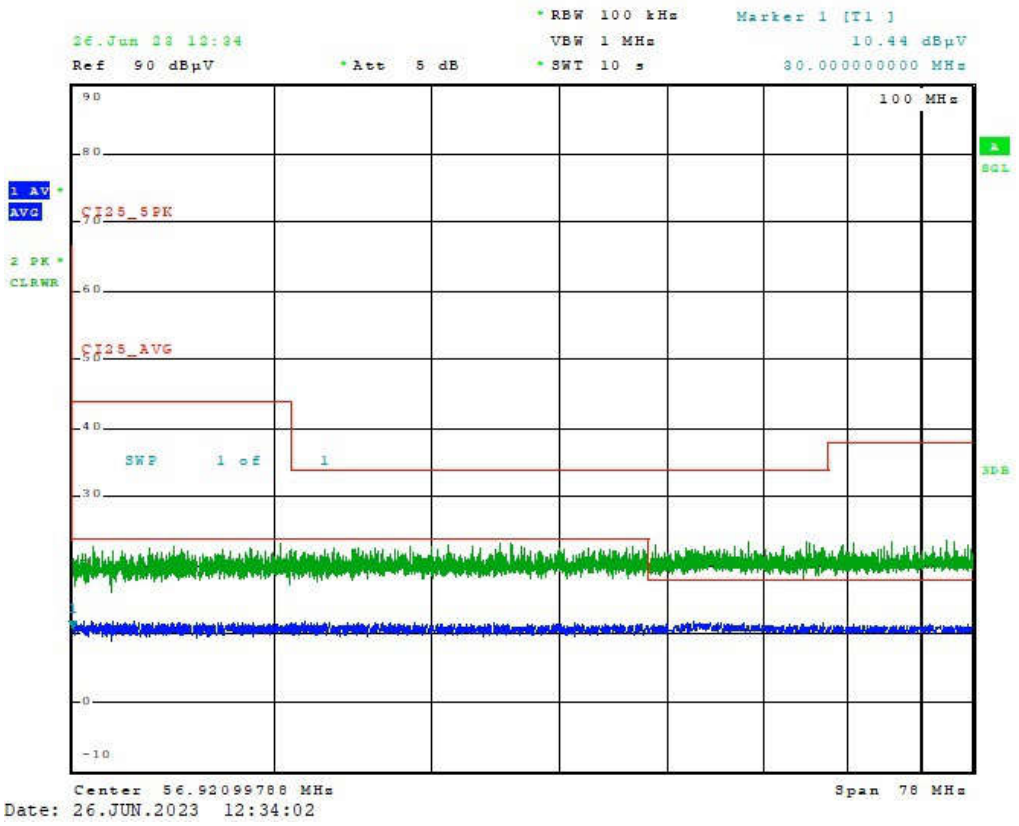


Figure 2-13. Positive Terminal, 30 MHz to 108 MHz, Noise Floor

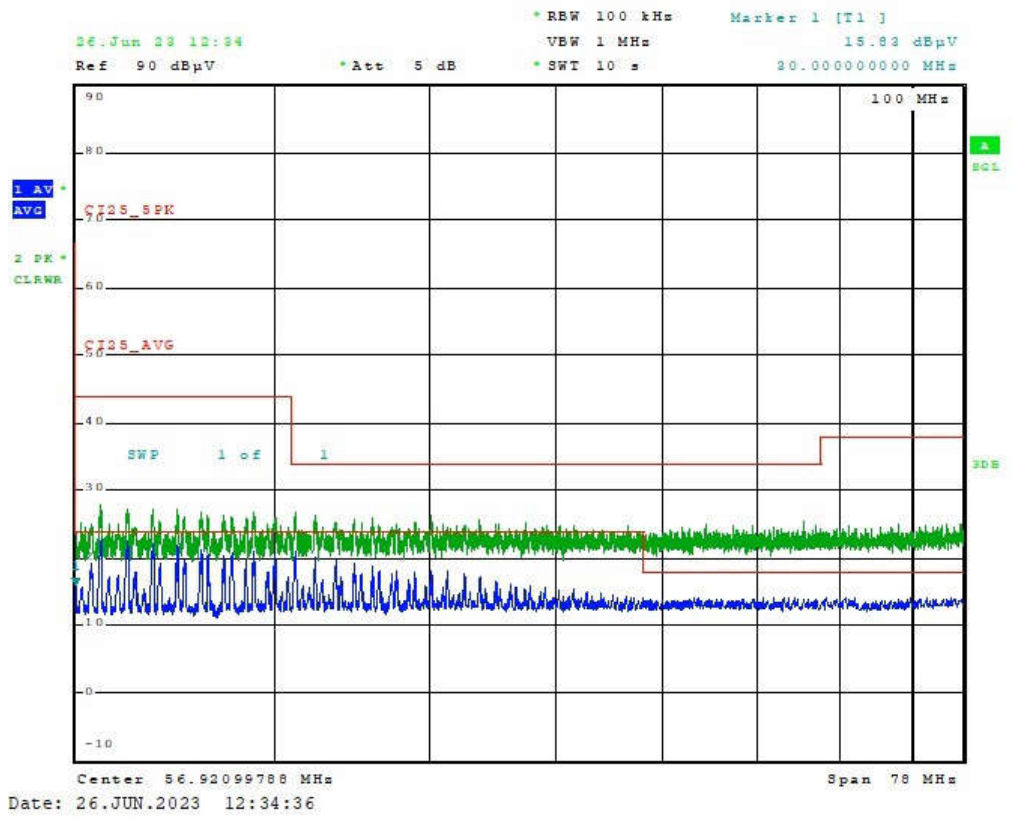


Figure 2-14. Positive Terminal, 30 MHz to 108 MHz, Board ON

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figures.

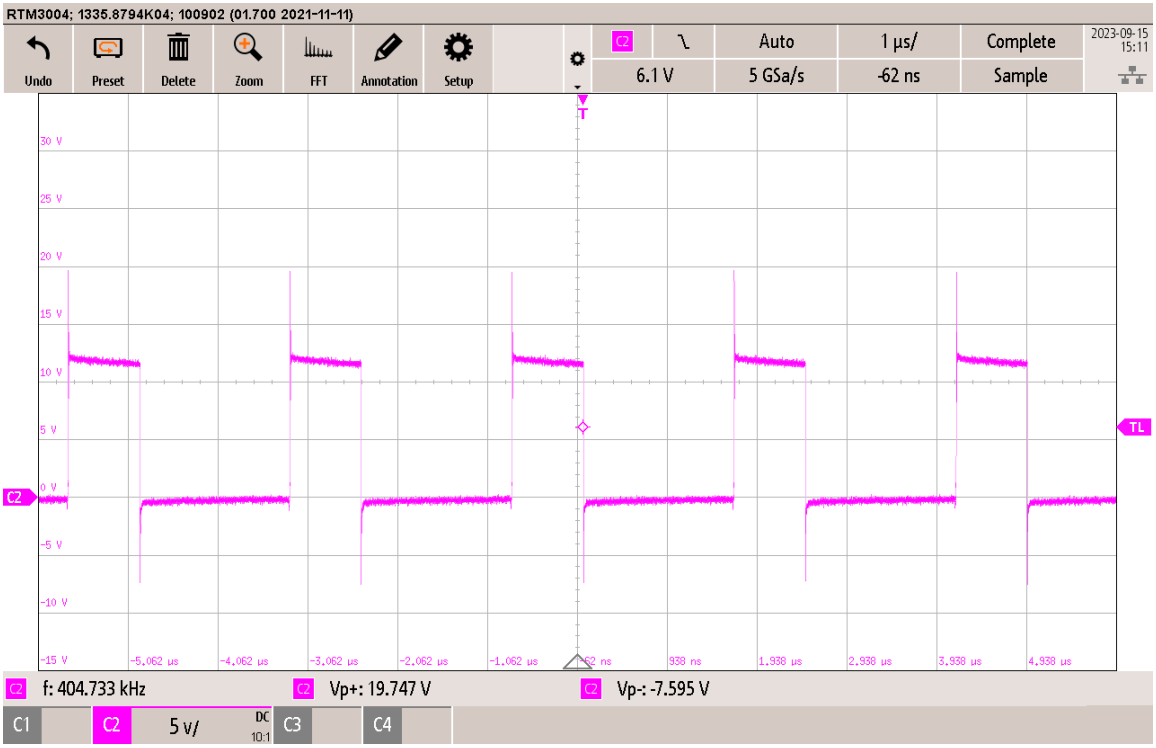


Figure 3-1. Switching 1 (V_{IN} = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 3 A)

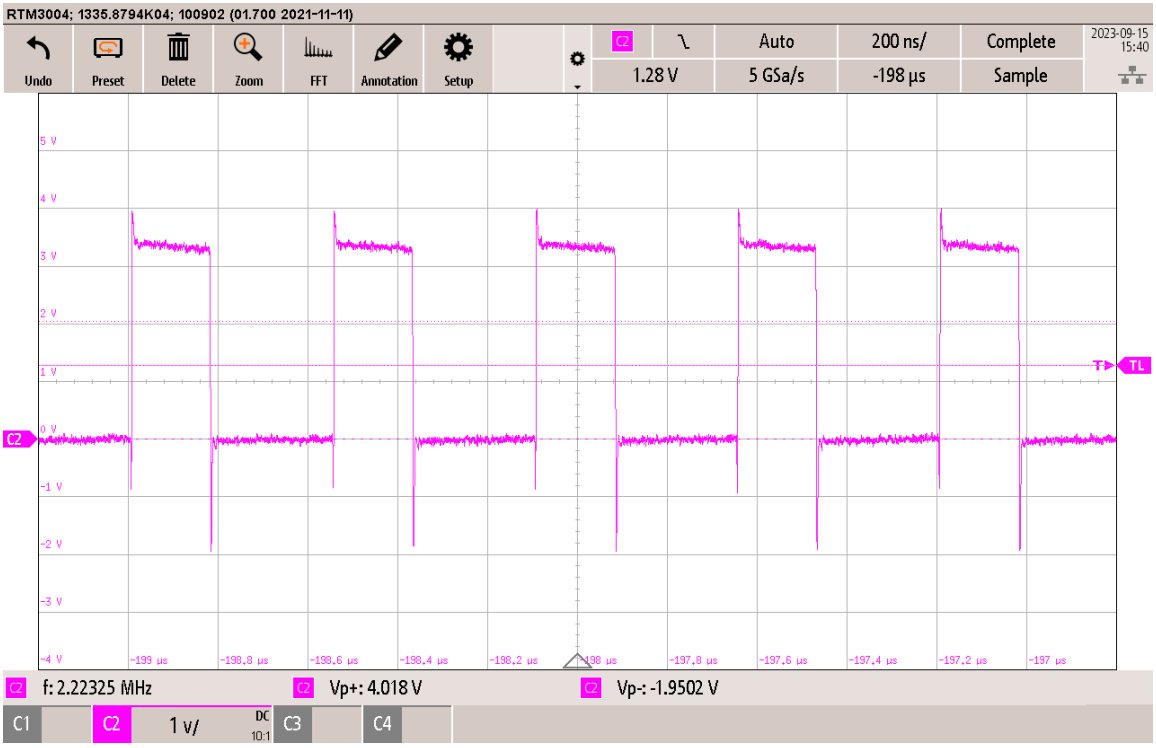


Figure 3-2. Switching 2 (V_{IN} = 3.3 V, V_{OUT2} = 1.2 V, I_{OUT2} = 1 A)

3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.

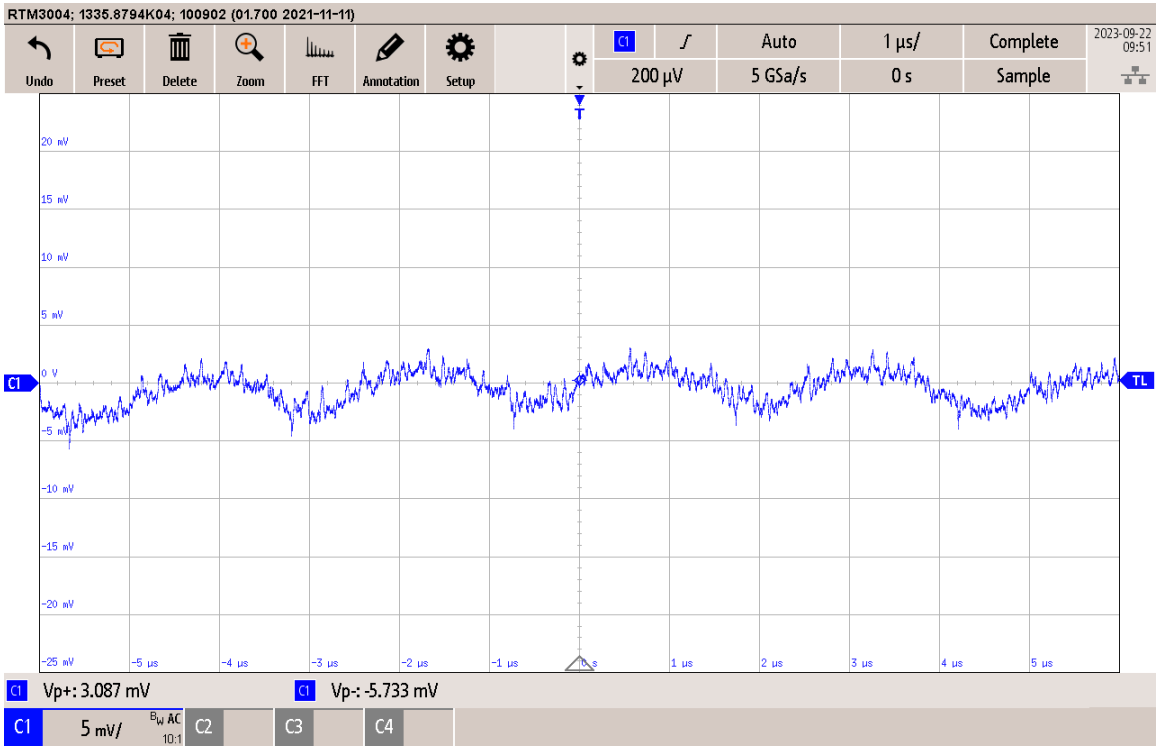


Figure 3-3. Output Voltage Ripple 1 (V_{IN} = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 3 A), 20-MHz Bandwidth Limited

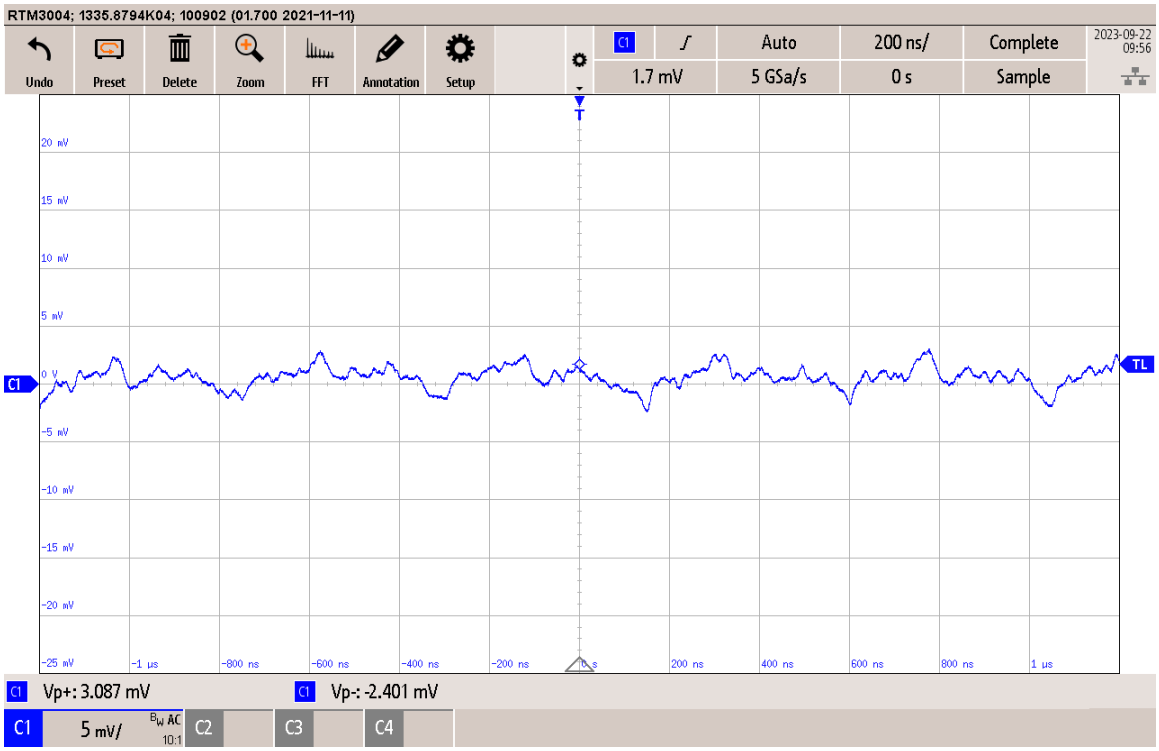


Figure 3-4. Output Voltage Ripple 2 (V_{IN} = 3.3 V, V_{OUT2} = 1.2 V, I_{OUT2} = 1 A), 20-MHz Bandwidth Limited

3.3 Input Voltage Ripple

Input voltage ripple is shown in the following figures.

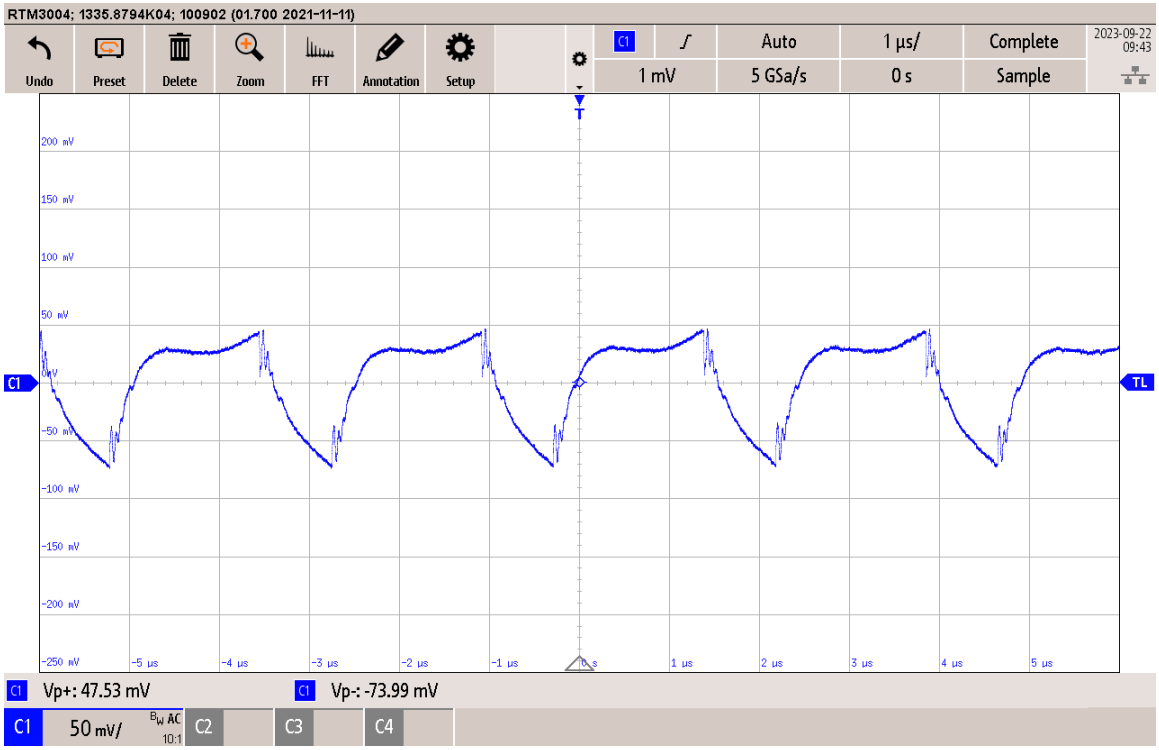


Figure 3-5. Input Voltage Ripple 1 (V_{IN} = 12 V, V_{OUT1} = 3.3 V, I_{OUT1} = 3 A), 20-MHz Bandwidth Limited

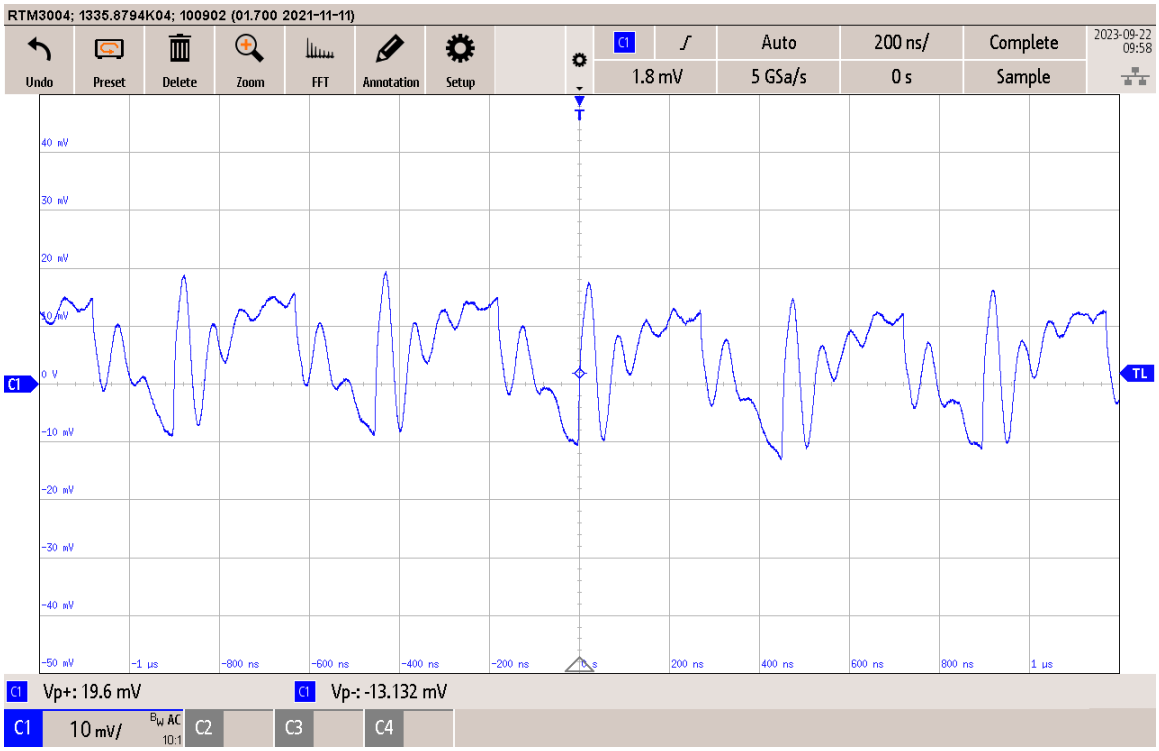


Figure 3-6. Input Voltage Ripple 2 (V_{IN} = 3.3 V, V_{OUT2} = 1.2 V, I_{OUT2} = 1 A), 20-MHz Bandwidth Limited

3.4 Load Transients

Load transient response waveforms are shown in the following figures.

Electronic load was used to create the load steps.

The output capacitors and compensation network need to be optimized according to the worst-case load step to meet the specific C2000 MCU supply requirements.

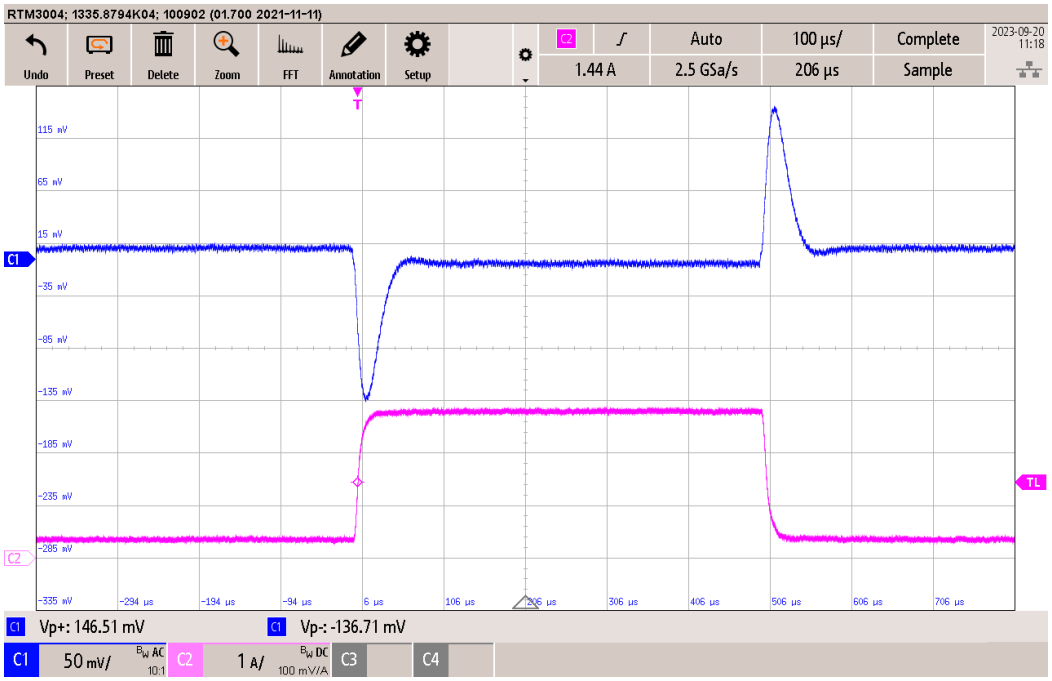


Figure 3-7. Load Transient 1 (V_{IN} = 12 V, CH1: V_{OUT1} = 3.3 V, CH2: I_{OUT1} = 0.3 → 2.7 A), 20-MHz Bandwidth Limited

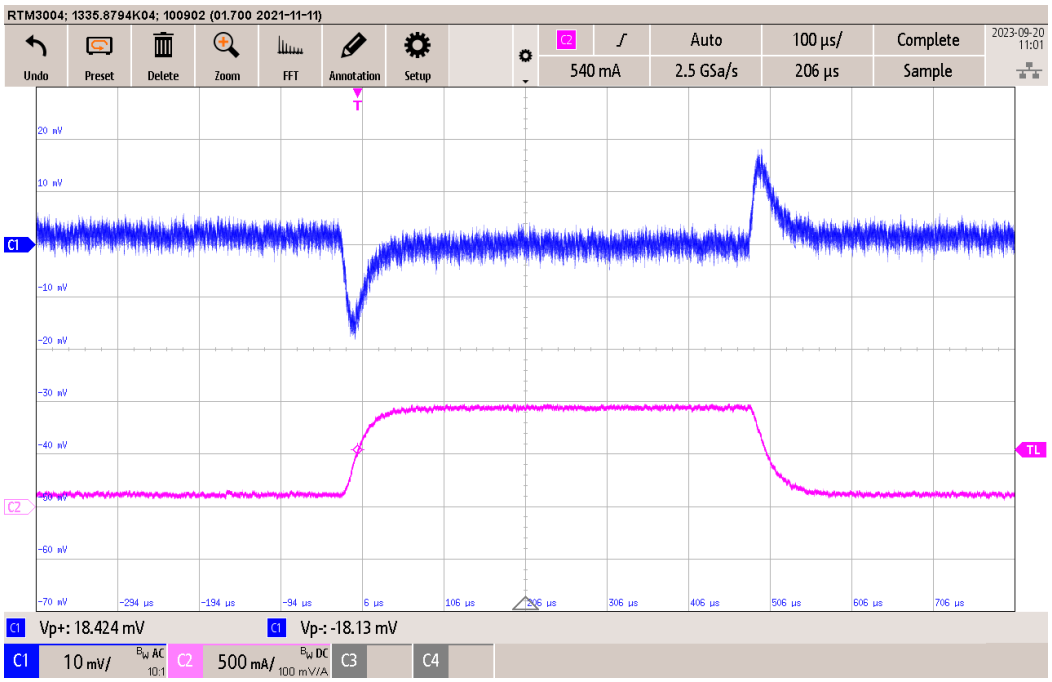


Figure 3-8. Load Transient 2 (V_{IN} = 3.3 V, CH1: V_{OUT2} = 1.2 V, CH2: I_{OUT2} = 0.1 → 0.9 A), 20-MHz Bandwidth Limited

3.5 Start-Up Sequence

Start-up behavior is shown in the following figure.

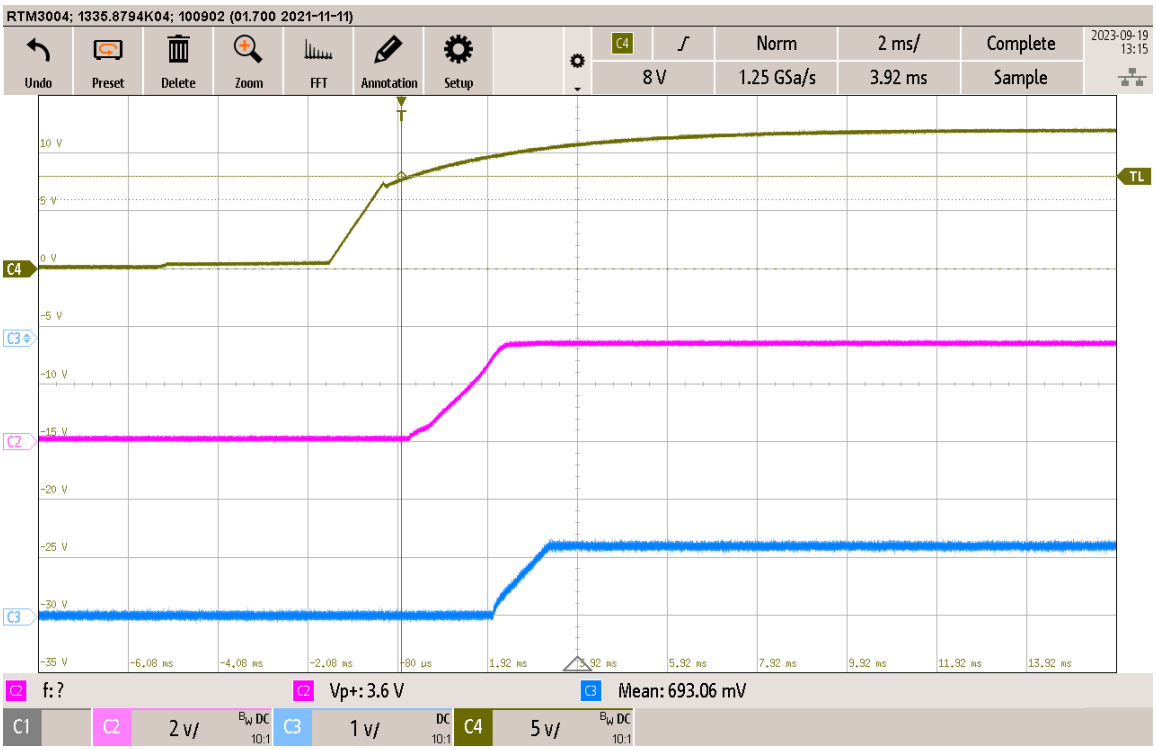


Figure 3-9. Start-Up (CH2: V_{OUT1}, CH3: V_{OUT2}, CH4: V_{IN} at 12 V)

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