Test Report: PMP23227

Power Delivery Reference Design for AMD Versal™ AI Edge Series

Description

This reference design demonstrates how the required power rails for the VE2302 device can be powered by TI's regulator ICs. See AMD's Power Design Manager (PDM) tool, for all available power consolidation options. Use PDM when estimating power for any application. This reference design uses example power estimations. The design can also be used as a foundation for designing the power tree for other devices of the AI Edge series. The original power source for this system is typically between $8V_{IN}$ to $18V_{IN}$ and capable of delivering about 50W of power.

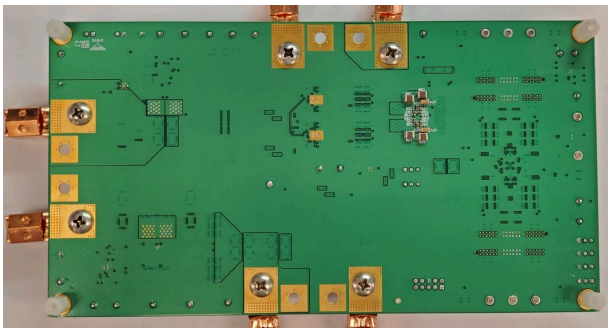
Features

- An optional front-end protection (FEP) sub-circuit, controlled by the LM74910-Q1 integrated circuit (IC), that acts as a programmable electronic safety switch with numerous safety features.
- A LM25148-Q1 buck converter, referred to as the 5V pre-regulator, that accepts the wide input voltage, and generates a well-regulated 5V voltage level. This 5V rail, in turn, supplies the main point-of-load (POL) converters, which regulate the various voltages needed to supply the VE2302 device.
- Two TPS62876-Q1 regulator ICs are used to implement a dual-phase, interleaved converter that powers the main digital core rail.
- A LP87694-Q1 Power Management IC (PMIC) and TPS746-Q1 Low Dropout (LDO) linear regulator are used for the remaining rails.
- The PMIC is highly integrated and contains programmable general-purpose input and output (GPIOs) pins which have been programmed in this design to both perform the voltage supervision, as well as the converter rail sequencing tasks. However, if a discrete, dedicated voltage supervisor is desired, a dedicated auxiliary voltage supervisor IC, TPS389006-Q1, is available for use in place of the voltage supervision implemented in the PMIC.
- There is also a TPS7B6933-Q1 LDO to generate an *always-ON* bias supply, which powers a number of subcircuits, such as the auxiliary voltage supervisor IC, as well as the power good indication LEDs. If a 3.3V always-ON power supply already exists in the system, then the TPS7B6933-Q1 LDO is not needed.

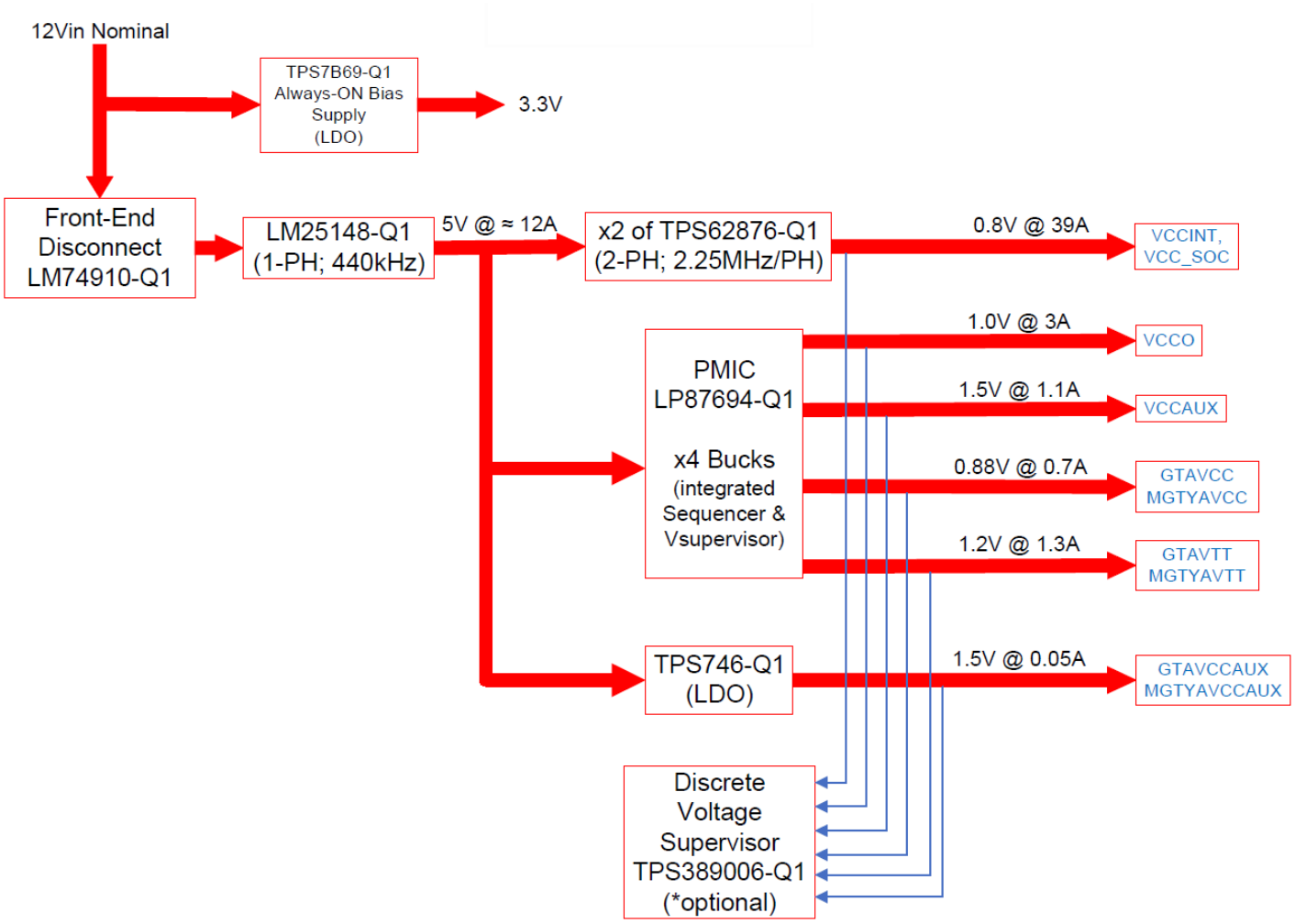
Applications

- ADAS domain controller
- Drive assist ECU
- Autonomous driving controller
- Automotive camera
- Driver monitoring
- Front camera
- Mirror replacement, camera mirror system
- Surround view system ECU
- In-cabin monitoring - radar
- Imaging radar
- Long range radar - 76 to 81GHz with RFCMOS
- Short and medium range radar - 76 to 81GHz with RFCMOS
- Radar ECU
- Mechanically scanning LIDAR

Top of Board



Bottom of Board



Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1 shows the power rail specifications including voltages and tolerances, load currents, and sequence order for each of the power rails pertaining to the VE2302 device. This reference design was designed to meet all AI Edge Series power delivery specifications.

Table 1-1. VE2302 Device Power Rail Specifications

Rail Name	Voltage	DC Spec.	AC Spec.	Current	Step	Sequence #
VCCINT, VCC_SOC	0.8V	±1%	±17mV	39A	33%	2
VCCO	1.5V	±1%	±5%	3A	100%	1
VCCAUX	1.5V	±1%	$10mV_{PP}$	1.1A	100%	3
GTAVCC, MGTYAVCC	0.88V	±2%	$10mV_{PP}$	0.7A	70%	4
GTAVTT, MGTYATT	1.2V	±2%	$10mV_{PP}$	1.3A	70%	6
GTAVCCAUX, MGTYAVCCAUX	1.5V	±2%	$10mV_{PP}$	0.05A	70%	5

Table 1-2 shows the voltages, currents, and switching frequencies pertaining to the reference design.

Table 1-2. Reference Design Overall Electrical Specifications

Parameters	Specifications
V_{IN}	$9V_{DC}$ to $18V_{DC}$ Continuous ($6V_{IN}$ Minimum Crank; $42V_{IN}$ Maximum Load Dump)
V_{OUT} (Buck 5V Pre-Regulator)	$5V_{DC}$
I_{OUT} (Buck 5V Pre-Regulator)	12A Maximum
F_{SW} (Buck Pre-Regulator)	440kHz Nominal
V_{OUT} (VCCINT, VCC SOC)	$0.8V_{DC}$
I_{OUT} (VCCINT, VCC SOC)	39A Maximum
F_{SW} (VCCINT, VCC SOC)	2.25MHz per phase (4.5MHz effective interleaved)
V_{OUT} (VCCO)	$1.0V_{DC}$
I_{OUT} (VCCO)	3A
F_{SW} (VCCO)	4.4MHz
V_{OUT} (VCCAUX)	$1.5V_{DC}$
I_{OUT} (VCCAUX)	1.1A
F_{SW} (VCCAUX)	4.4MHz Nominal
V_{OUT} (GTAVCC, MGTYAVCC)	$0.88V_{DC}$
I_{OUT} (GTAVCC, MGTYAVCC)	0.7A
F_{SW} (GTAVCC, MGTYAVCC)	2.2MHz Nominal
V_{OUT} (GTAVTT, MGTYAVTT)	$1.2V_{DC}$
I_{OUT} (GTAVTT, MGTYAVTT)	1.3A
F_{SW} (GTAVCC, MGTYAVCC)	4.4MHz Nominal
V_{OUT} (GTAVCCAUX, MGTYAVCCAUX)	$1.5V_{DC}$
I_{OUT} (GTAVCCAUX, MGTYAVCCAUX)	0.05A
F_{SW} (GTAVCCAUX, MGTYAVCCAUX)	0Hz (LDO)

1.2 Required Equipment

- Power supply (capable of 60W or higher, as well as 10A and higher for low V_{IN} conditions)
- Electronic loads (capable of functioning down to 0V)
- DMMs
- Oscilloscope
- Current probe

1.3 Considerations

UVLO Undervoltage Lock-Out = Voltage above the UVLO rising threshold enables a device or system.

OVLO Overvoltage Lock-Out = Voltage below the UVLO falling threshold disables a device or system.

OCP Overcurrent Protection = A current above the OCP threshold shuts down the device or system.

FEP Front-End Protection = the circuitry at the very input of the system which protects the downstream devices and circuitry from being damaged by overvoltage, overcurrent, or reverse polarity conditions.

2 Testing and Results

2.1 Efficiency and Power Loss Graphs

Figure 2-1 to Figure 2-12 show the efficiency and power loss graphs for the 5V pre-regulator, core rail regulator, as well as all four PMIC regulators. Figure 13 and Figure 14 show the current sharing of the core rail between the two phases, as well as the current-sharing tolerances over load.

Figure 2-1 and Figure 2-2 includes pre-regulator buck efficiency measurements taken with front-end protection in the circuit and pre-regulator buck isolated from downstream rails.

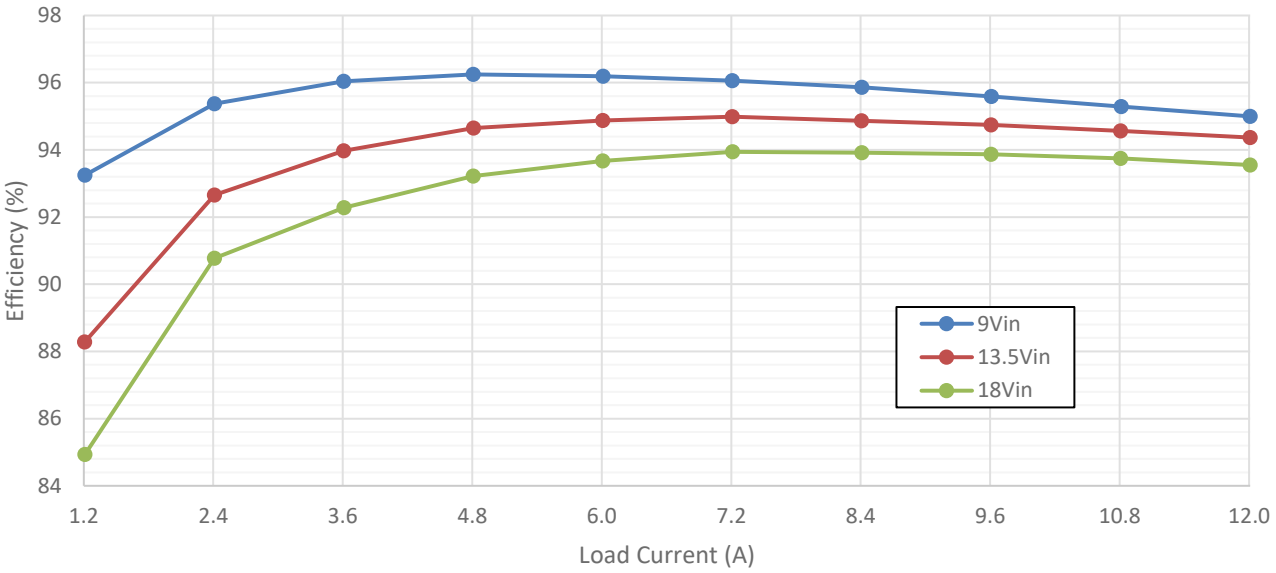


Figure 2-1. 5V Pre-Regulator Buck Efficiency

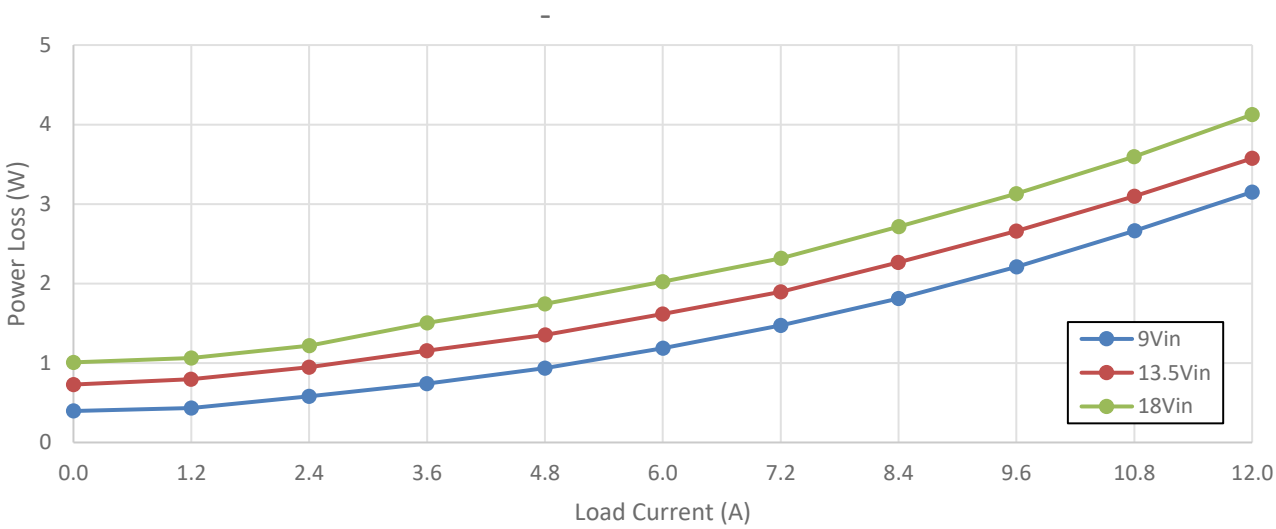


Figure 2-2. 5V Pre-Regulator Buck Power Loss

The graphs in Figure 2-3 and Figure 2-4 show 2-phase core rail buck core rail regulators isolated from both the 5V pre-regulator, as well as the PMIC regulators. The efficiency values displayed are calculated after negating the 1mΩ R_{SNS} power losses.

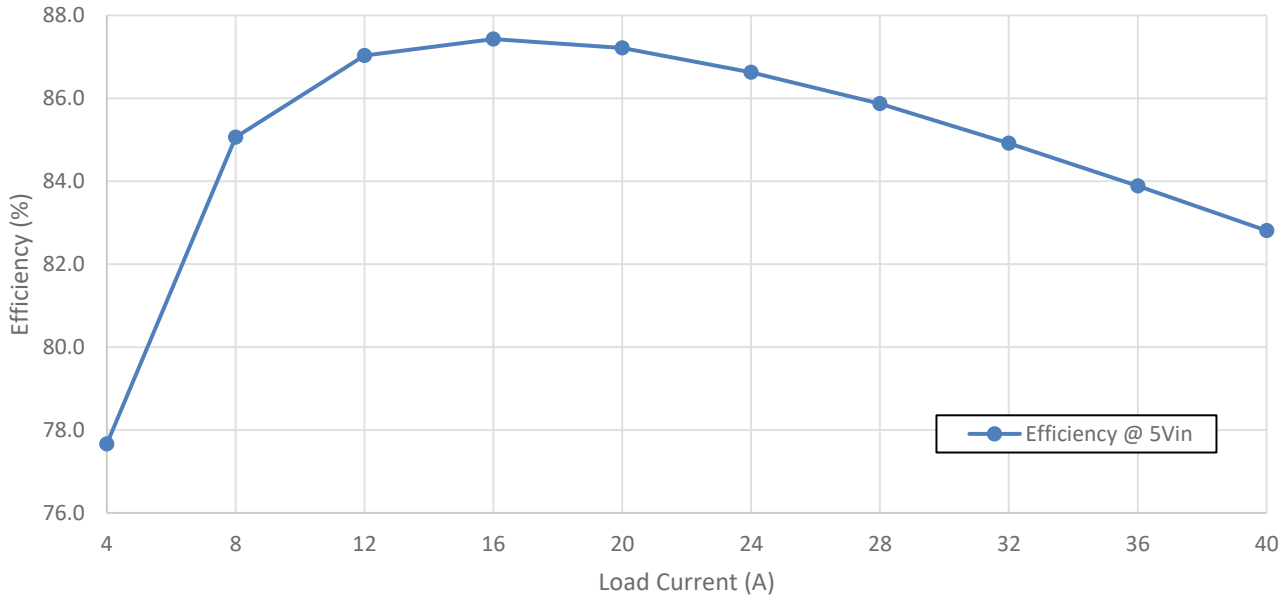


Figure 2-3. VCCINT/VCC SOC Efficiency

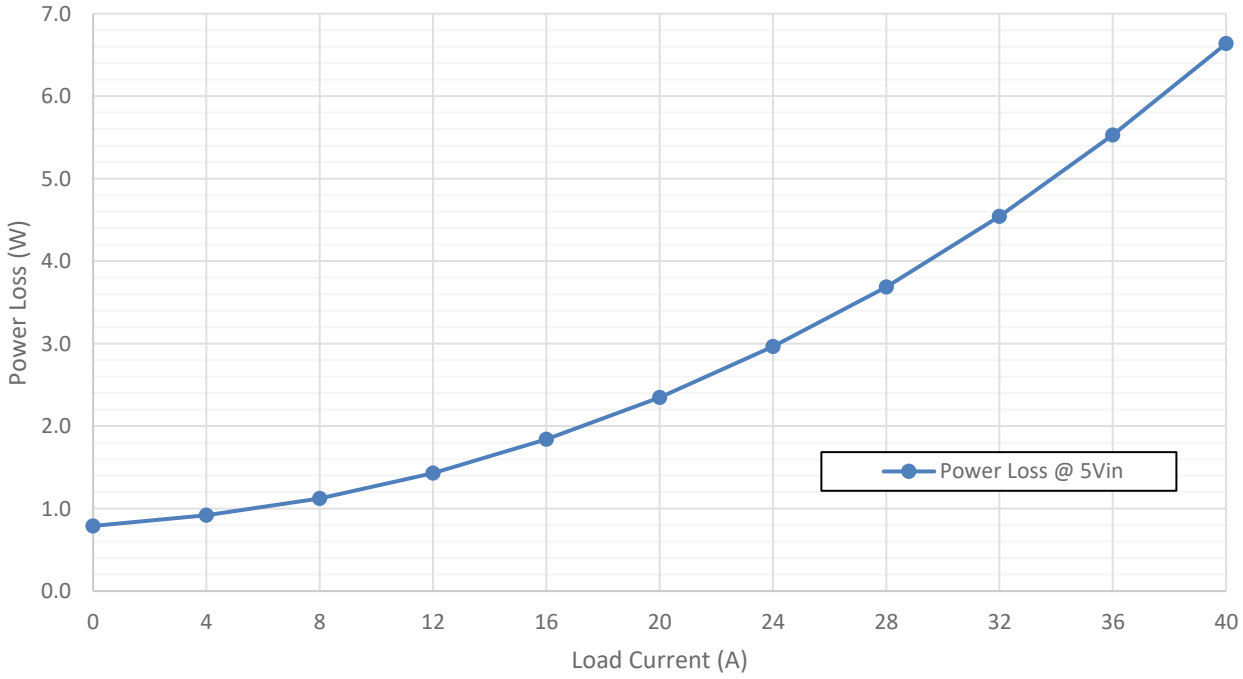


Figure 2-4. VCCINT/VCC SOC Power Loss

Figure 2-5 through Figure 2-12 include data taken from a different board with precisely the same PMIC configurations, operating conditions, and inductors used for PMP23227.

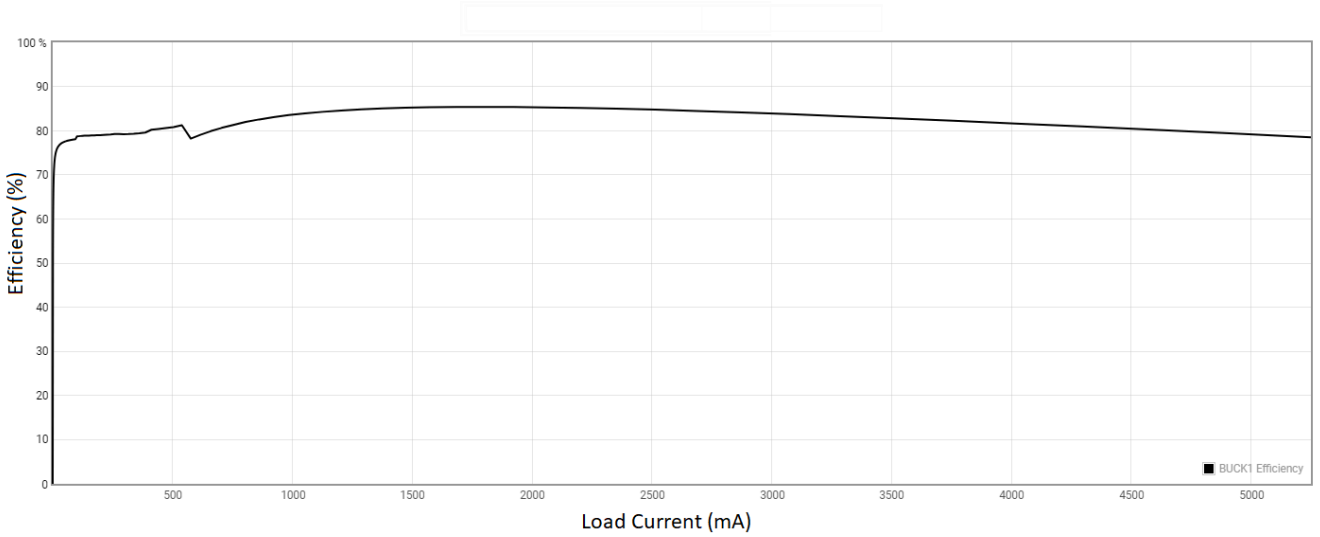


Figure 2-5. VCCO Rail Efficiency (PMIC Buck 1), PFM Mode Operation

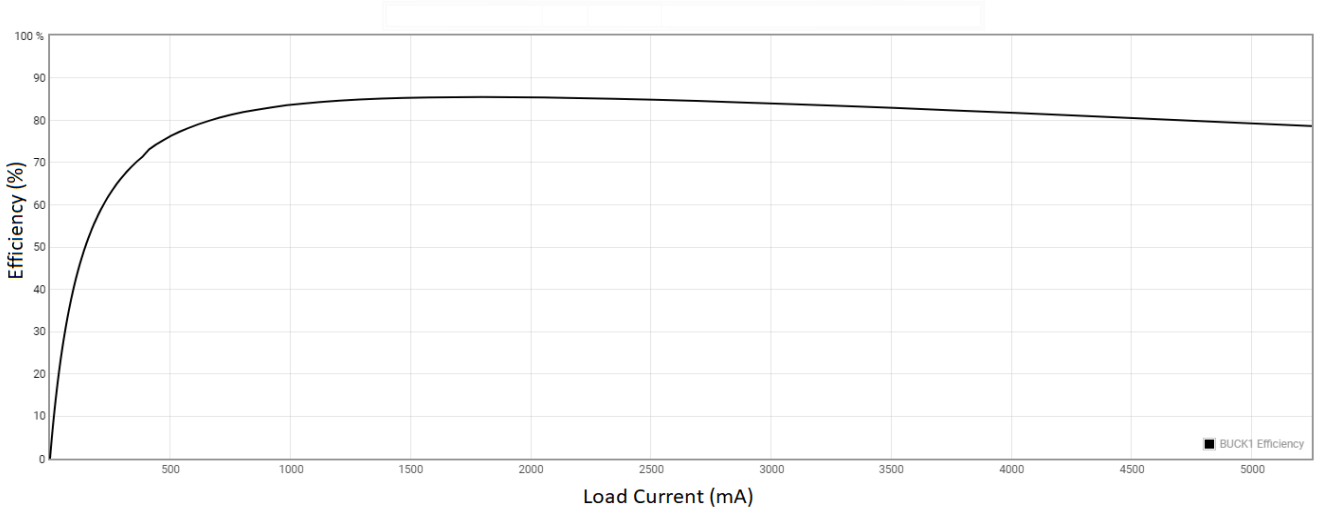


Figure 2-6. VCCO Rail Efficiency (PMIC Buck 1), FPWM Mode Operation

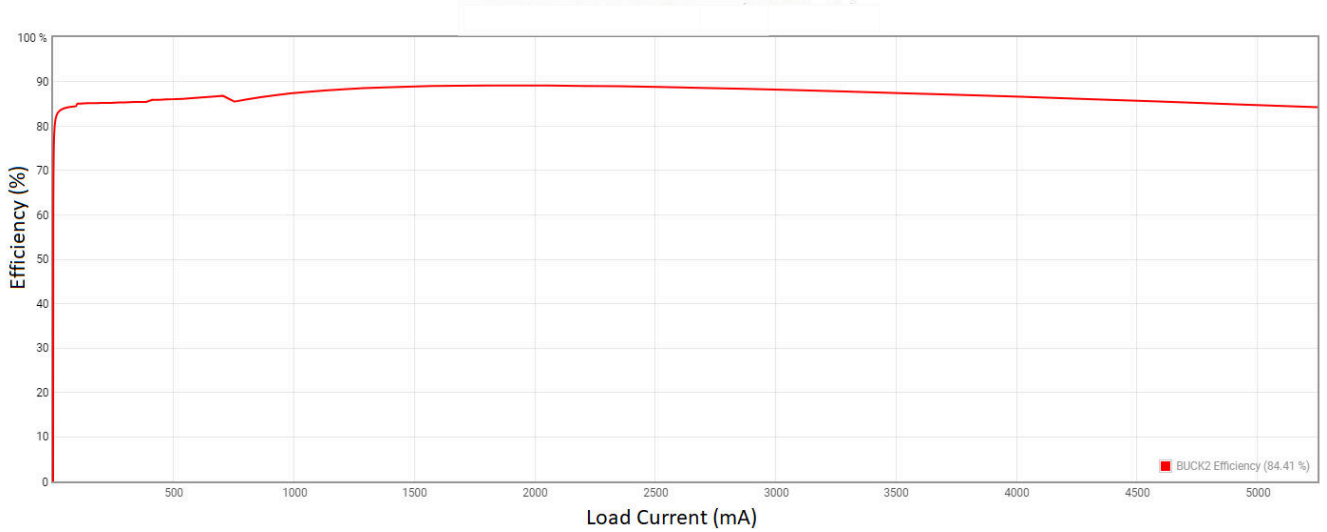


Figure 2-7. VCCAUX Rail Efficiency (PMIC Buck 2), PFM Mode Operation

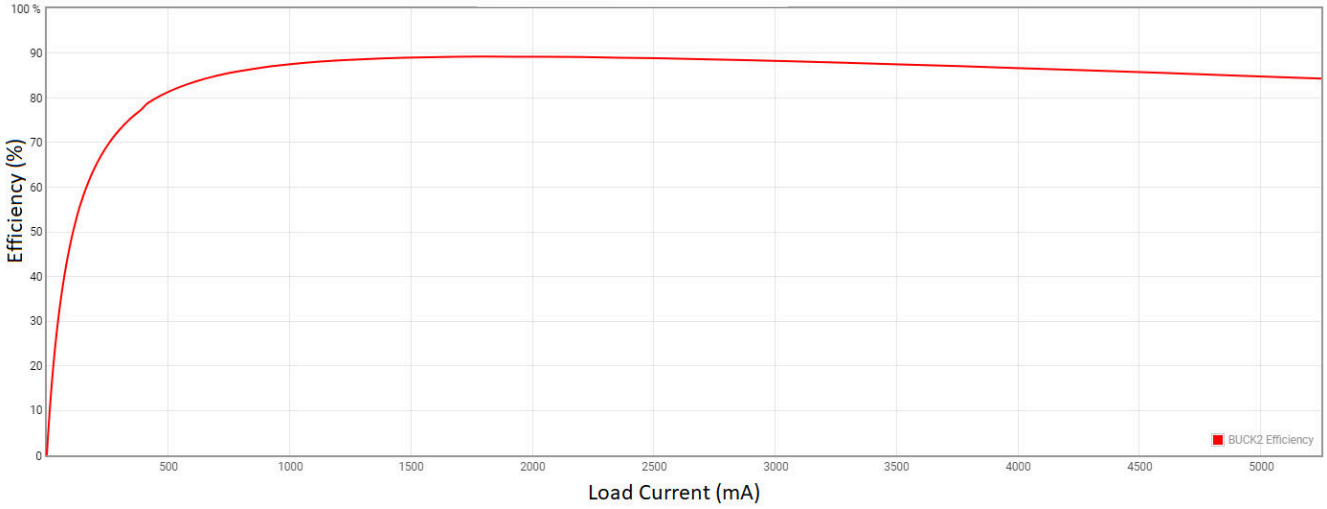


Figure 2-8. VCCAUX Rail Efficiency (PMIC Buck 2), FPWM Mode Operation

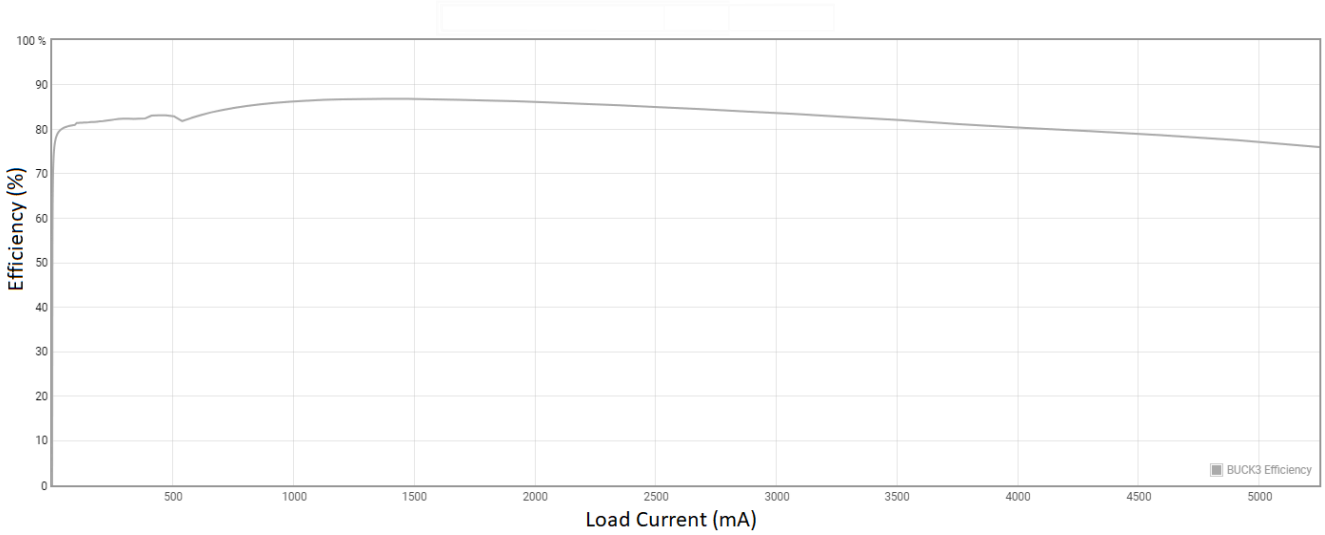


Figure 2-9. GTAVCC/MGTYAVCC Rail Efficiency (PMIC Buck 3), PFM Mode Operation

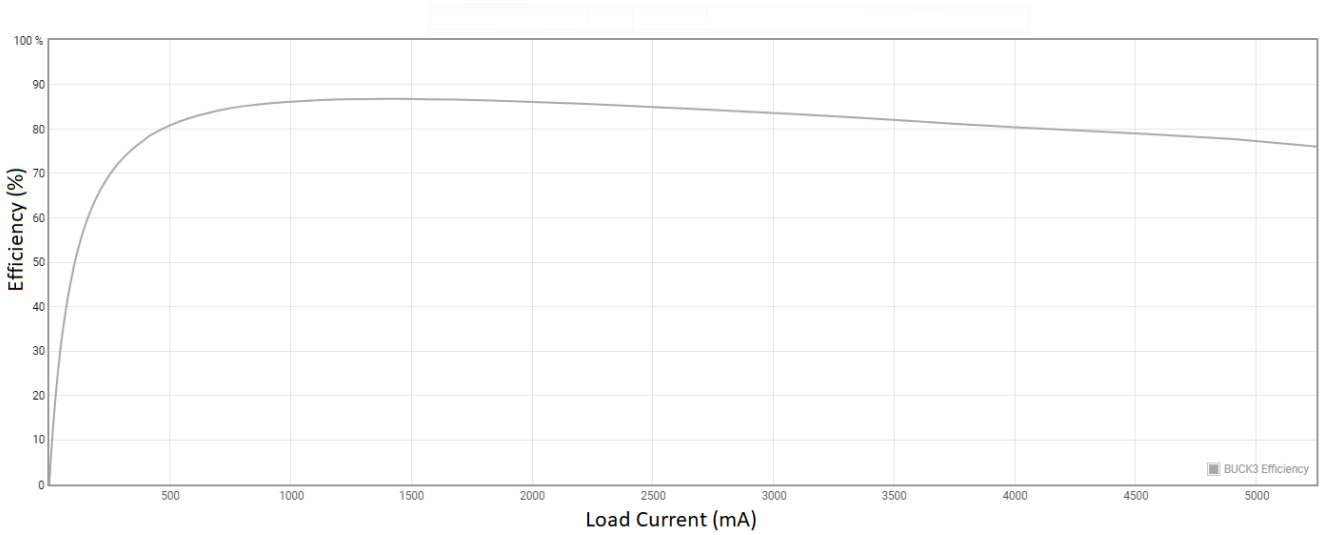


Figure 2-10. GTAVCC/MGTYAVCC Rail Efficiency (PMIC Buck 3), FPWM Mode Operation

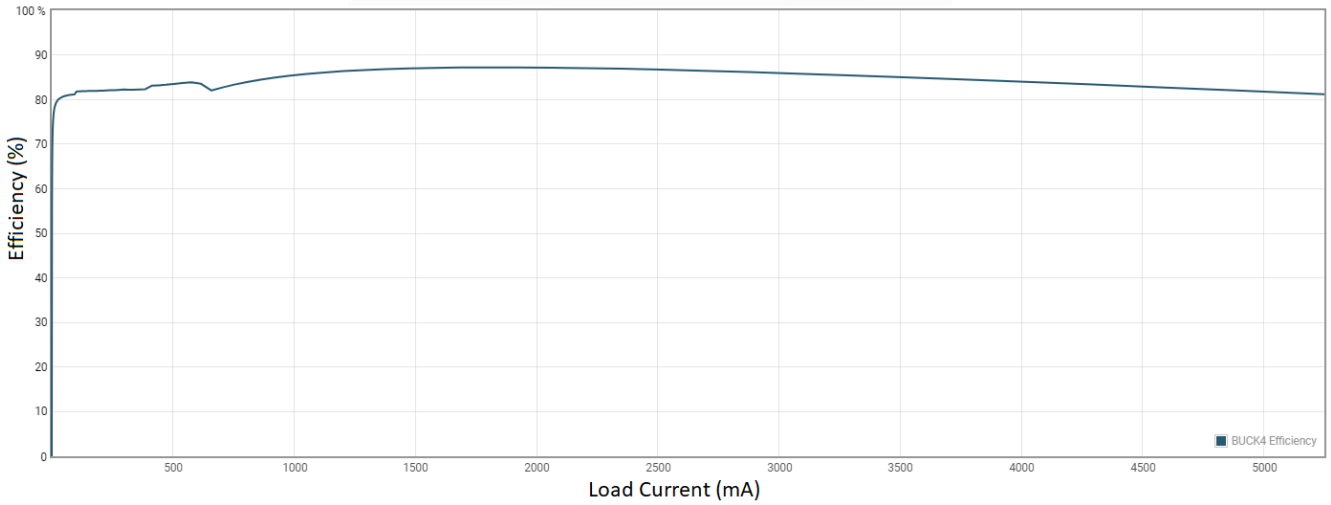


Figure 2-11. GTAVTT/MGTYAVTT Rail Efficiency (PMIC Buck 4),PFM Mode Operation

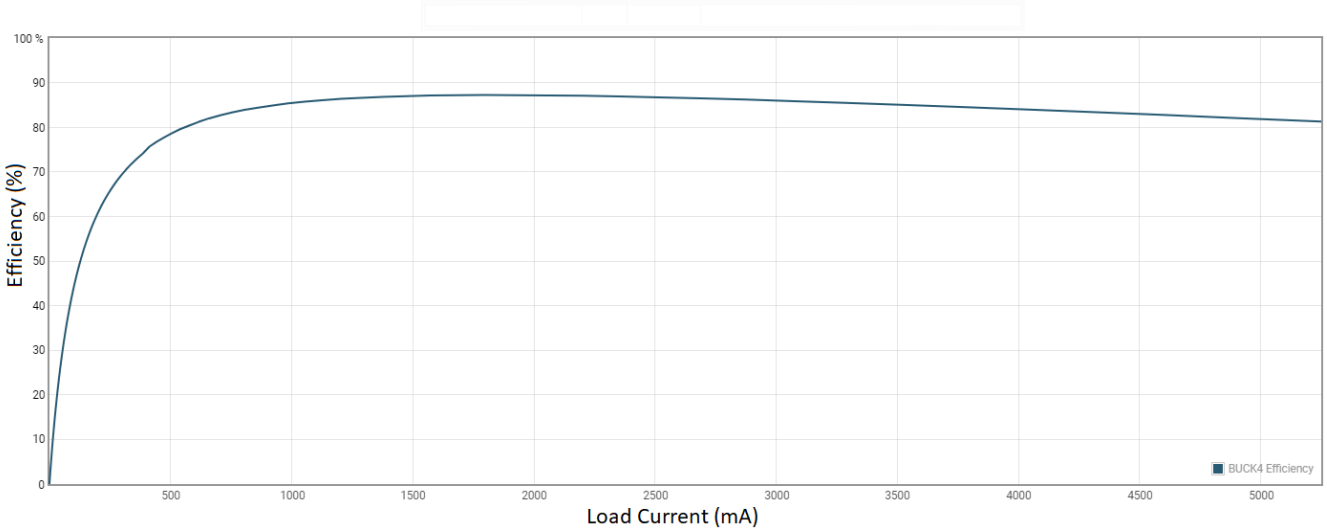


Figure 2-12. GTAVTT, MGTYAVTT Rail Efficiency (PMIC Buck 4), FPWM Mode Operation

2.2 VCCINT - Core Rail Current Sharing Tolerances

Figure 2-13 and Figure 2-14 show the current sharing tolerances between the two phases of the Core Rail regulator.

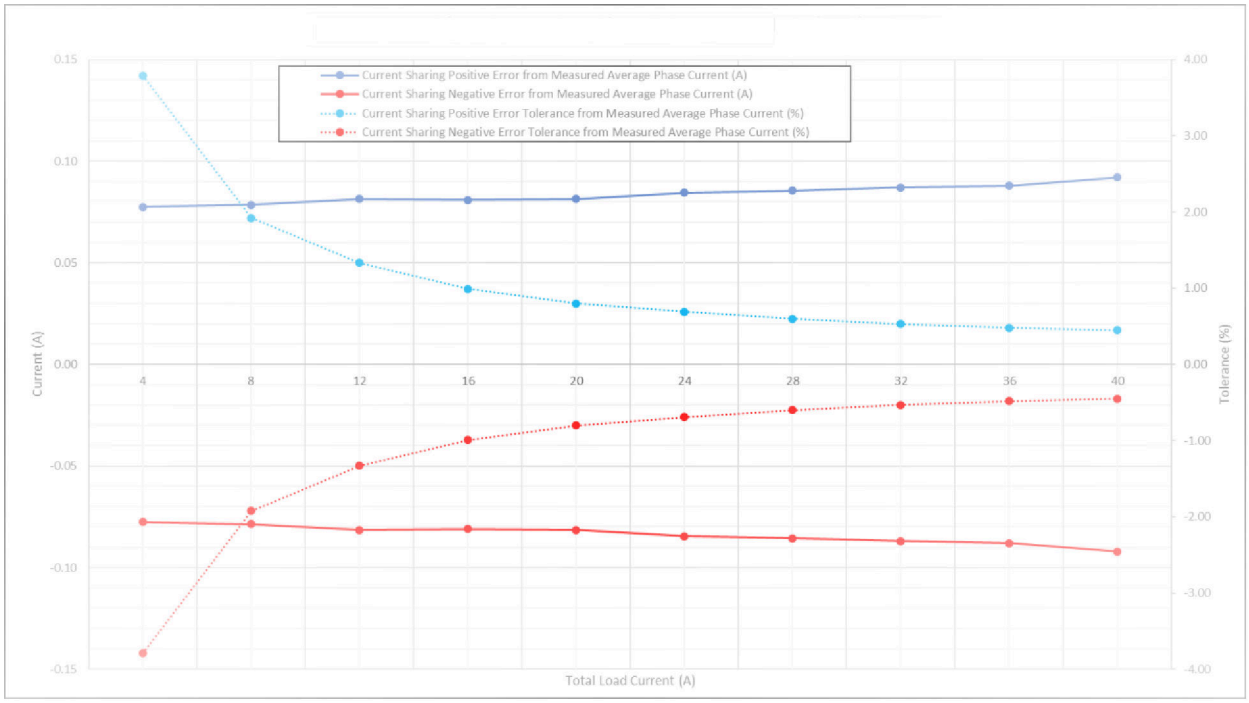


Figure 2-13. VCCINT- Core Rail Current Sharing Variance and Tolerance

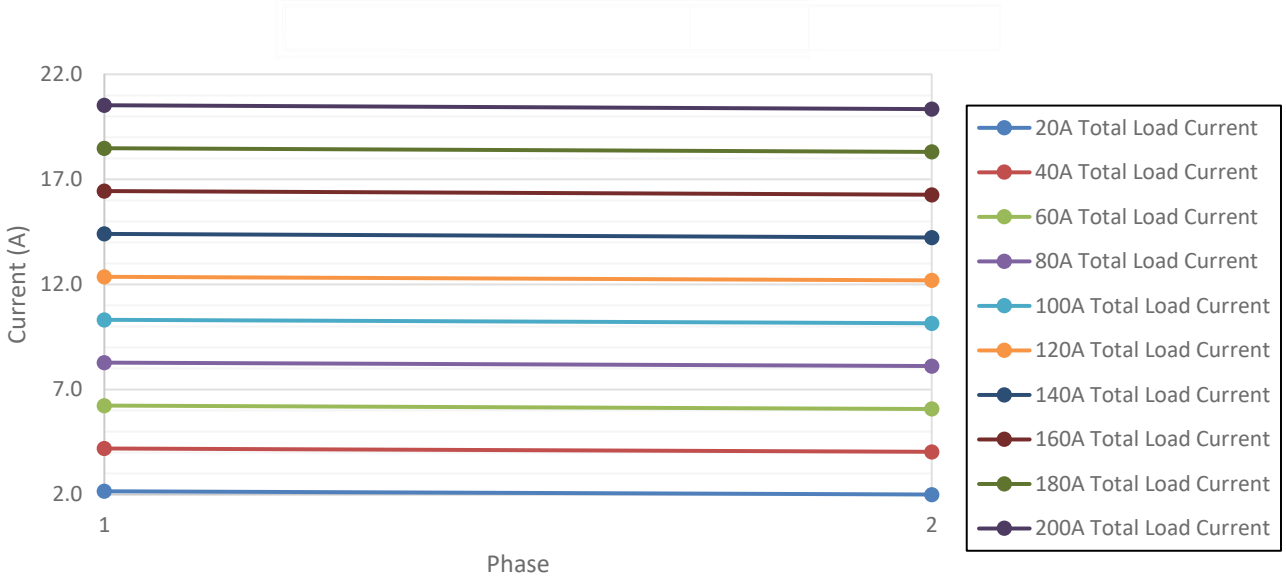


Figure 2-14. VCCINT- Core Rail Current Sharing Distribution

2.3 Thermal Images

The thermal images in Figure 2-15 to Figure 2-18 show the thermal performance of all of the rails at the specified input and output conditions. All images were taken at ambient room temperatures after reaching thermal equilibrium.

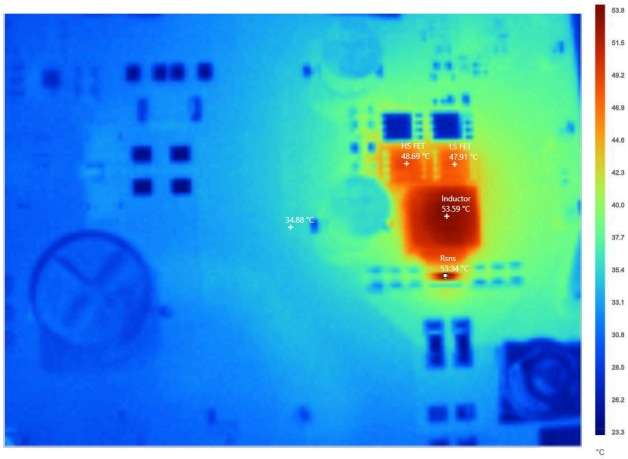


Figure 2-15. Thermal Image, Pre-Regulator Buck and FEP, 13.5V Input, 5V Output at 12A Load

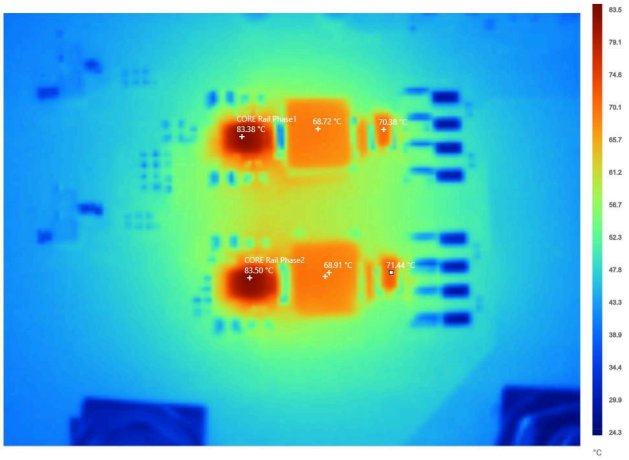


Figure 2-16. VCCINT - Thermal Image, Core Rail, 5V Input, 0.8V Output at 39A Load

The thermal image in Figure 2-17 shows all rails running at the respective full load current (buck 1: 1.0V output at 3A load; buck 2: 1.5V output at 1.1A load; buck 3: 0.88V output at 0.7A load; buck 4: 1.2V output at 1.3A load).

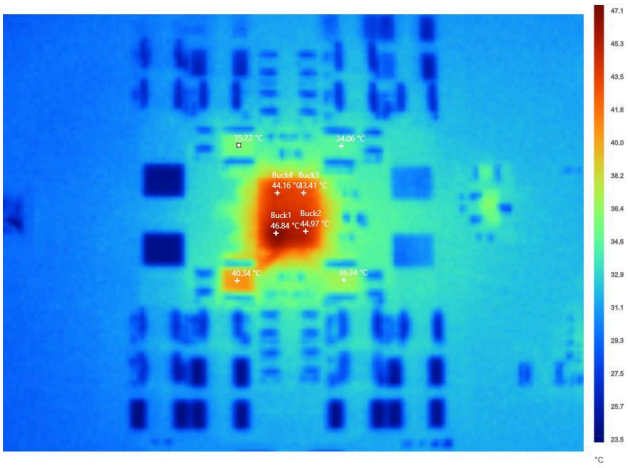


Figure 2-17. VCCO, VCCAUX, GTAVCC, GTAVTT - Thermal Image, PMIC, 5V Input

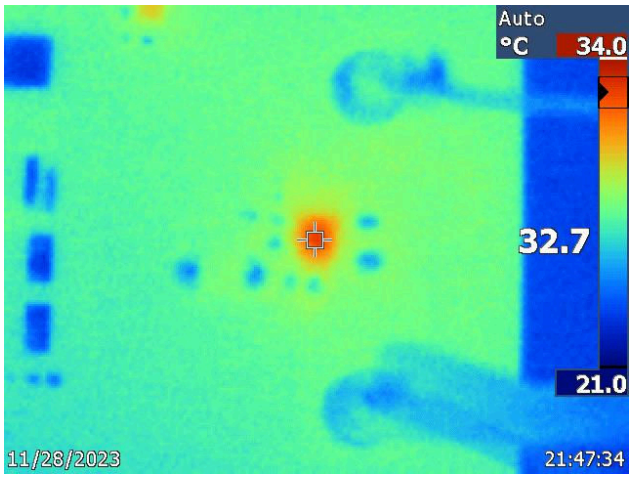


Figure 2-18. GTAVCCAUX - Thermal Image, LDO Linear Regulator, 5V Input, 1.5V Output at 0.05A Load

2.4 Dimensions

Figure 2-19 and Figure 2-20 present the top and bottom photos of the PMP23227 board, respectively. The board dimensions are 8.4in × 4.5in (21.3cm × 11.4cm). Remember, this is an evaluation board and has plenty of unutilized board space, for ease of testing. The final design size can be significantly reduced.

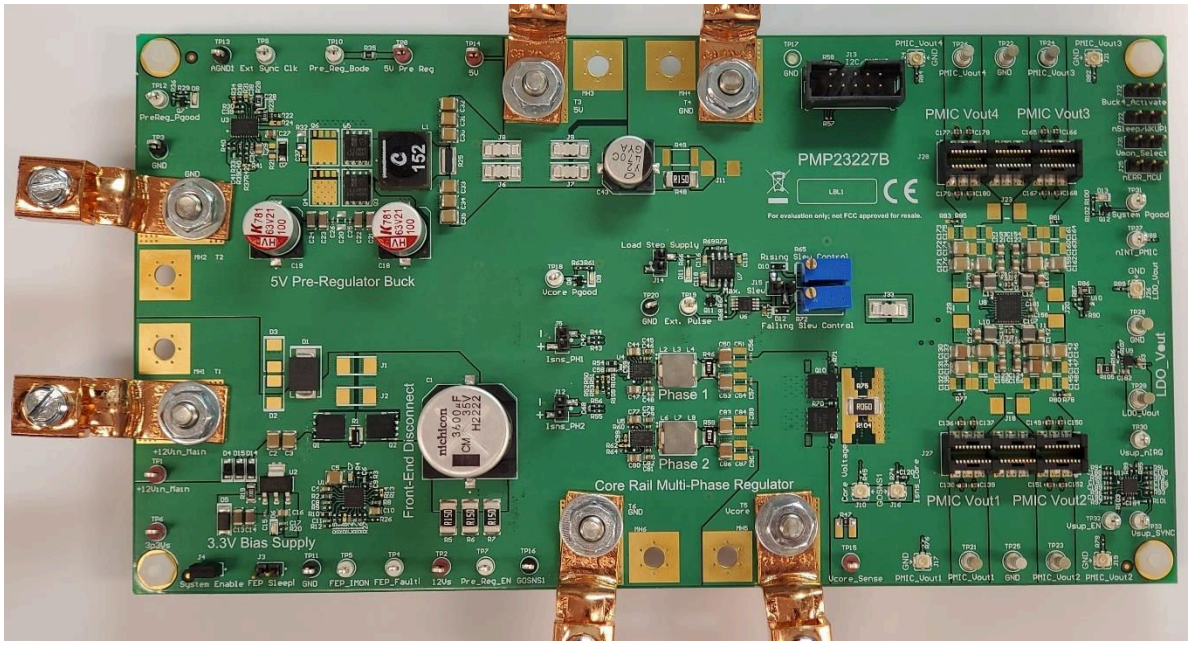


Figure 2-19. Top of PMP23227 Board

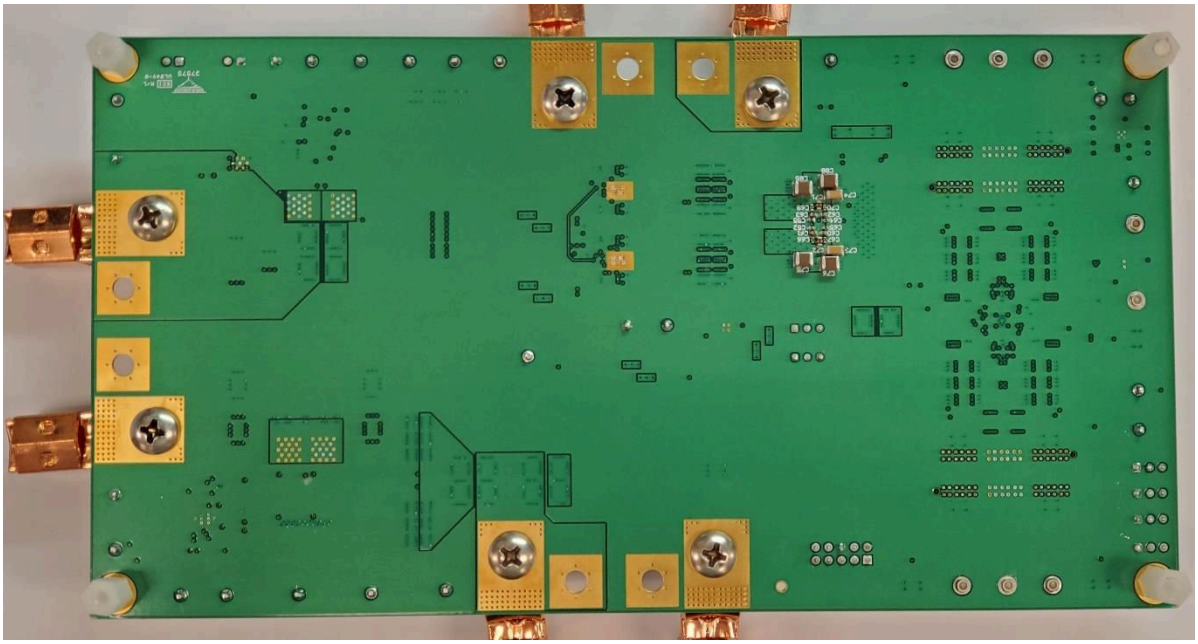


Figure 2-20. Bottom of PMP23227 Board

3 Waveforms

3.1 Switching

Figure 3-1 to Figure 3-11 show the switch node voltages of the converters at various input voltages and at various load conditions.

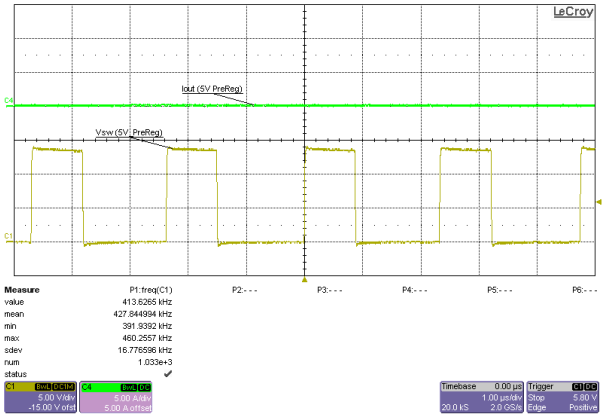


Figure 3-1. 5V Pre-Regulator, Switching 1

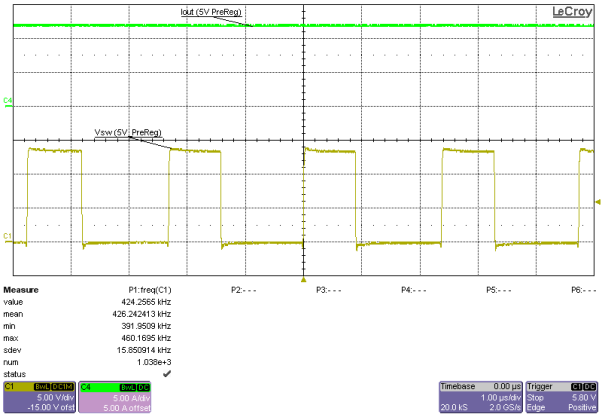


Figure 3-2. 5V Pre-Regulator, Switching 2

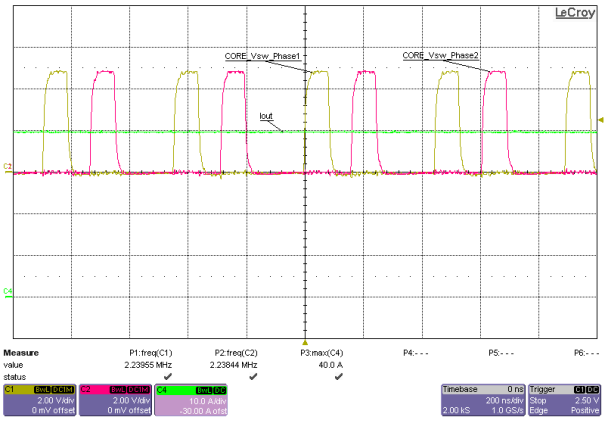


Figure 3-3. VCCINT Rail Switch Node Voltage (Core Rail Buck), 5V Input, 40A Load

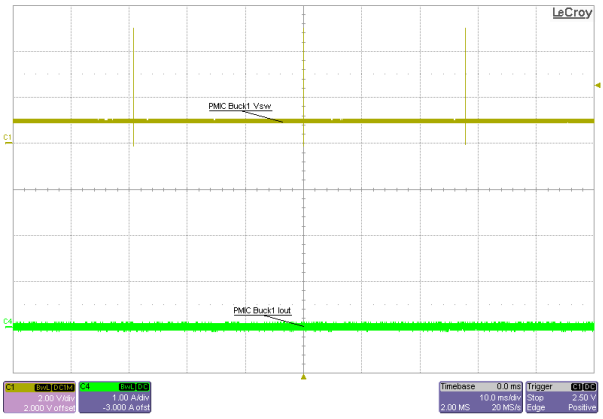


Figure 3-4. VCCO Rail Switch Node Voltage (PMIC Buck1), 5V Input, 1.0V_{OUT}, No Load, PFM Mode

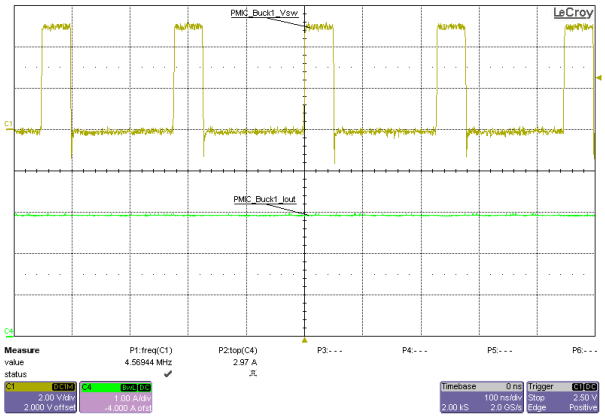


Figure 3-5. VCCO Rail Switch Node Voltage (PMIC_Buck1), 5V Input, 1.0V_{OUT}, 3A Load

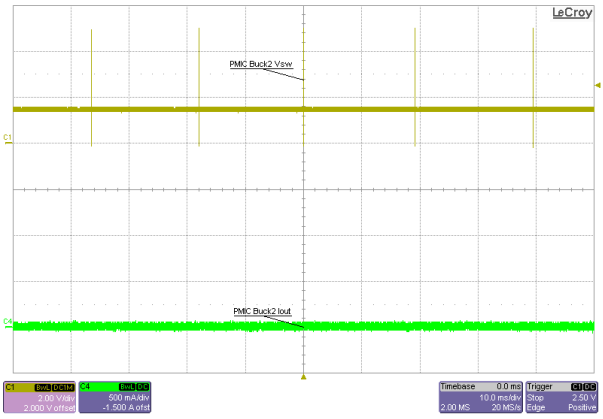


Figure 3-6. VCCAUX Switch Node Voltage (PMIC_Buck2), 5V Input, 1.5V_{OUT}, No Load, PFM Mode

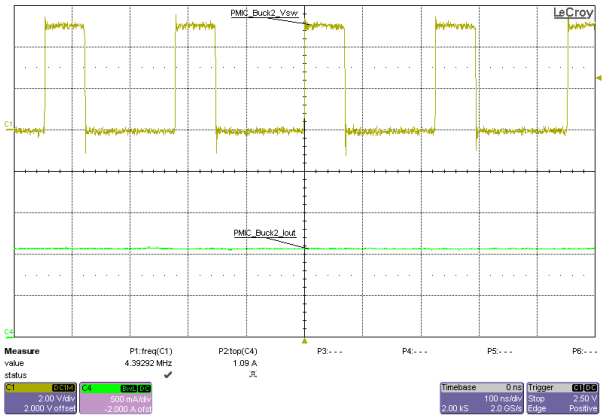


Figure 3-7. VCCAUX Rail Switch Node Voltage (PMIC_ Buck2), 5V Input, 1.5V_{OUT}, 1.1A Load

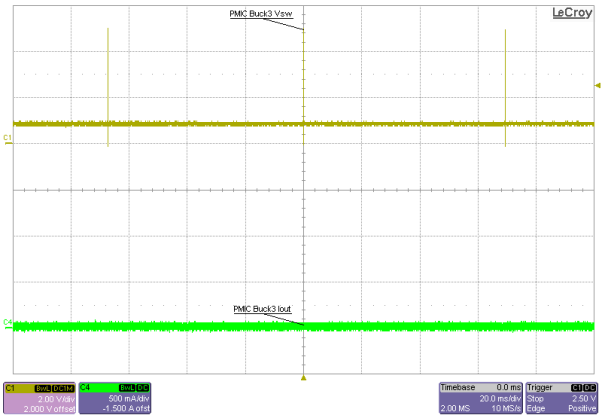


Figure 3-8. GTAVCC Rail Switch Node Voltage (PMIC_Buck3), 5V Input, 0.88V_{OUT}, No Load, PFM Mode

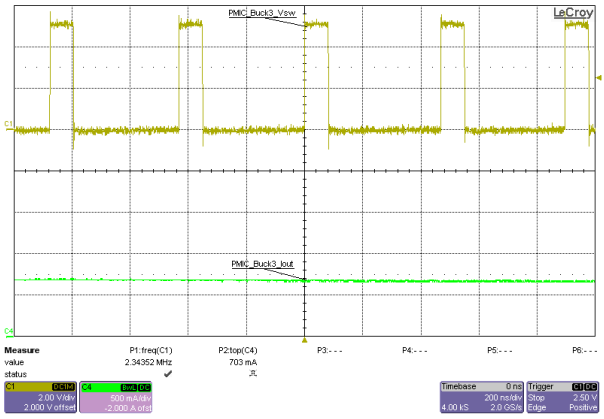


Figure 3-9. GTAVCC Rail Switch Node Voltage (PMIC_Buck3), 5V Input, 0.88V_{OUT}, 0.7A Load

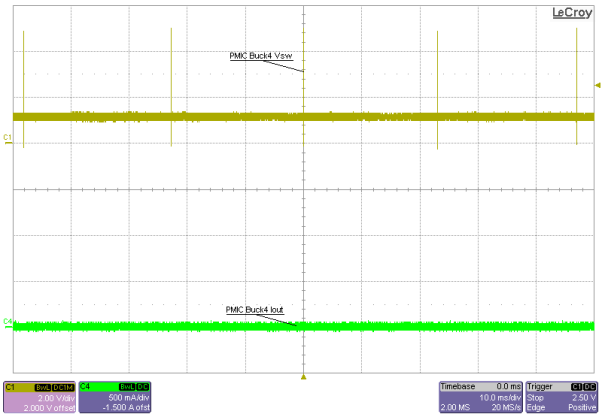


Figure 3-10. GTAVTT Rail Switch Node Voltage (PMIC_Buck4), 5V Input, 1.2V_{OUT}, No Load, PFM Mode

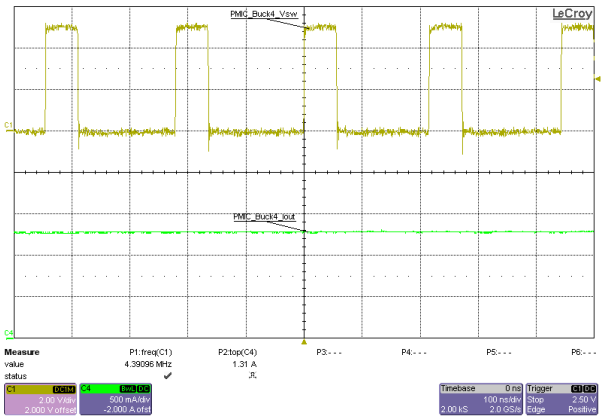


Figure 3-11. GTAVTT Rail Switch Node Voltage (PMIC_Buck4), 5V Input, 1.2V_{OUT}, 1.3A Load

3.2 Output Voltage Ripple

Figure 3-12 to Figure 3-23 show the output voltage ripple of the converters at the corresponding input voltages and various load currents.

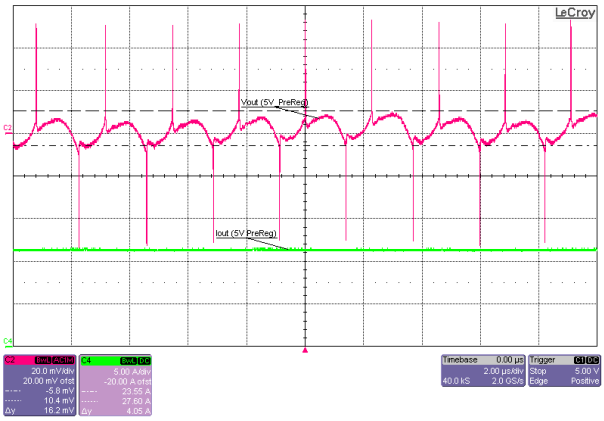


Figure 3-12. 5V Pre-Regulator Buck Output Voltage Ripple, 13.5V Input, 12A Load

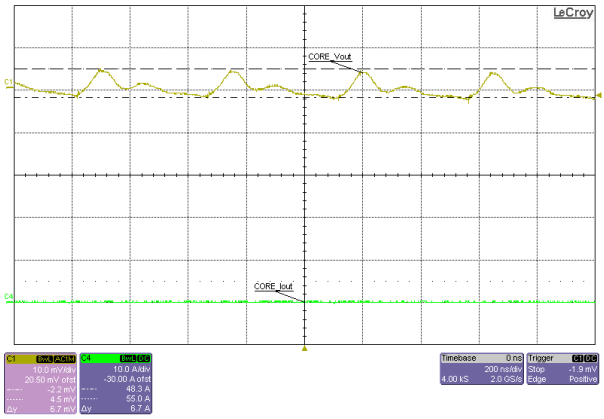


Figure 3-13. VCCINT Rail Output Voltage Ripple, 5V Input, 0.8V Output, No Load

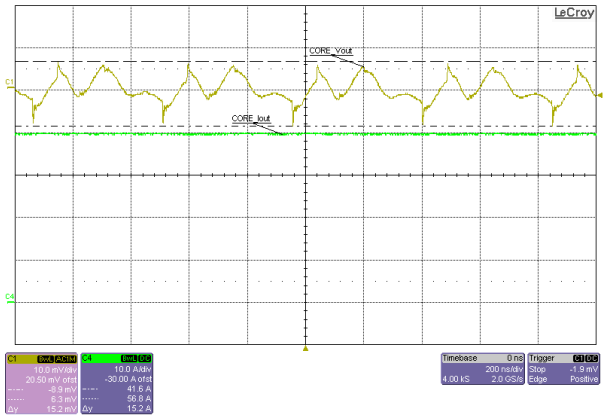


Figure 3-14. VCCINT Rail Output Voltage Ripple, 5V Input, 0.8V Output, 39A Load

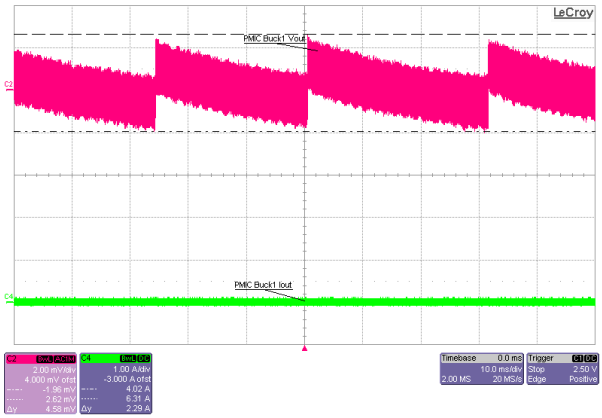


Figure 3-15. VCCO Output Voltage Ripple (PMIC_Buck1), 5V Input, 1.0V Output, No Load, PFM Mode

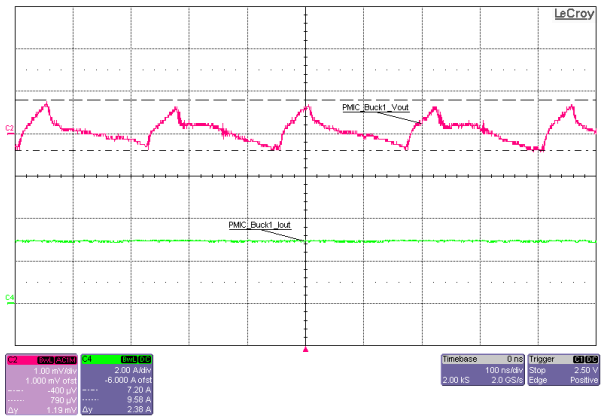


Figure 3-16. VCCO Output Voltage Ripple (PMIC_Buck1), 5V Input, 1.0V Output, 3A Load

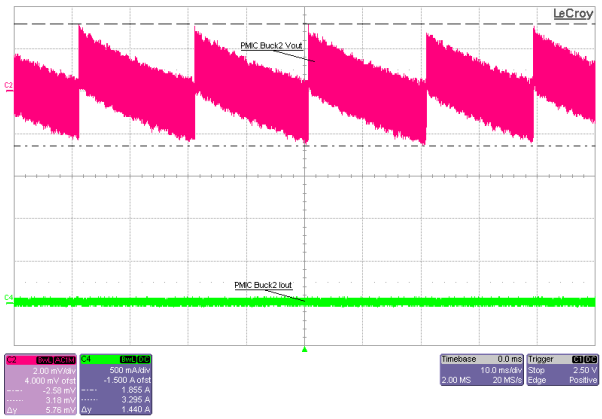


Figure 3-17. VCCAUX Output Voltage Ripple (PMIC_Buck2), 5V Input, 1.5V Output, No Load, PFM Mode

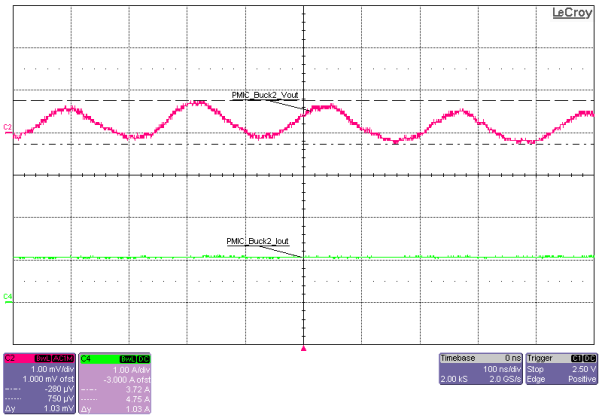


Figure 3-18. VCCAUX Output Voltage Ripple (PMIC_Buck2), 5V Input, 1.5V Output, 1.1A Load

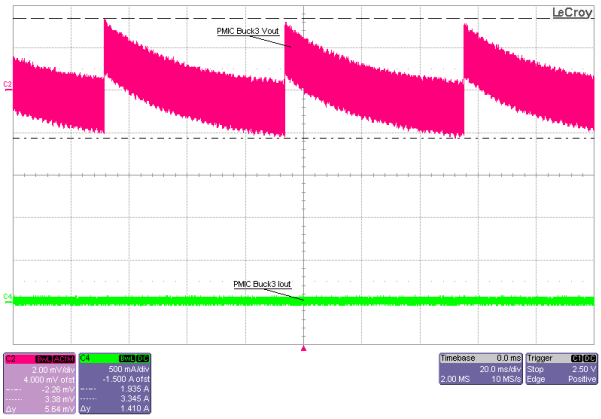


Figure 3-19. GTAVCC Output Voltage Ripple (PMIC_Buck3), 5V Input, 0.88V Output, No Load, PFM Mode

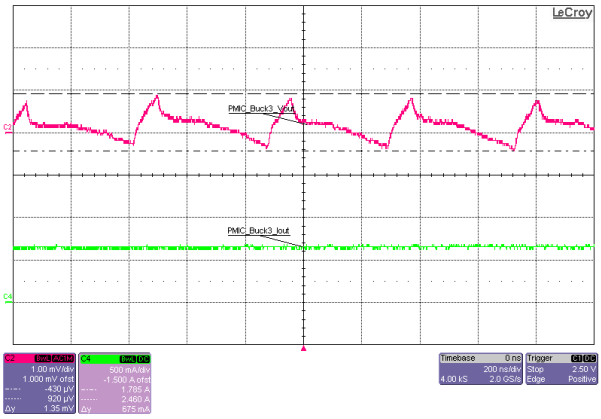


Figure 3-20. GTAVCC Output Voltage Ripple (PMIC_Buck3), 5V Input, 0.88V Output, 0.7A Load

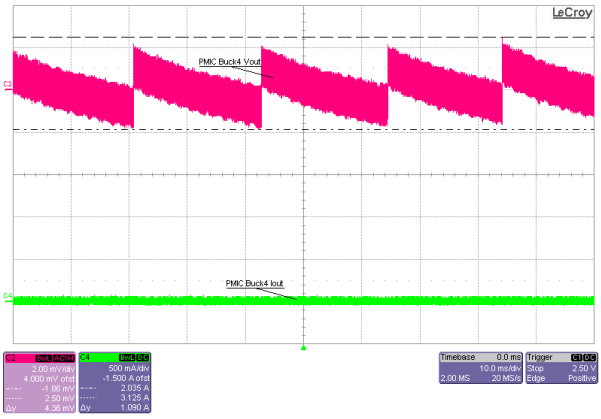


Figure 3-21. GTAVTT Output Voltage Ripple (PMIC_Buck4), 5V Input, 1.2V Output, No Load, PFM Mode

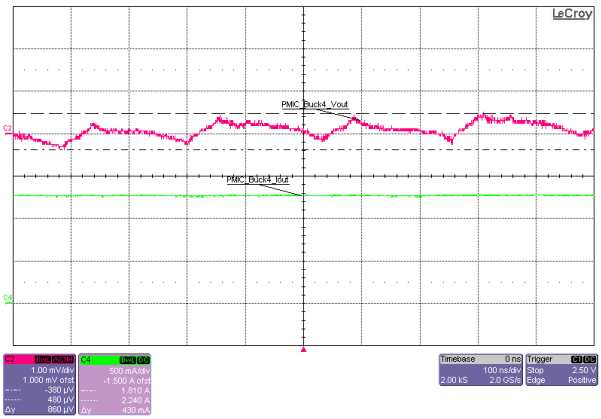


Figure 3-22. GTAVTT Output Voltage Ripple (PMIC_Buck4), 5V Input, 1.2V Output, 1.3A Load

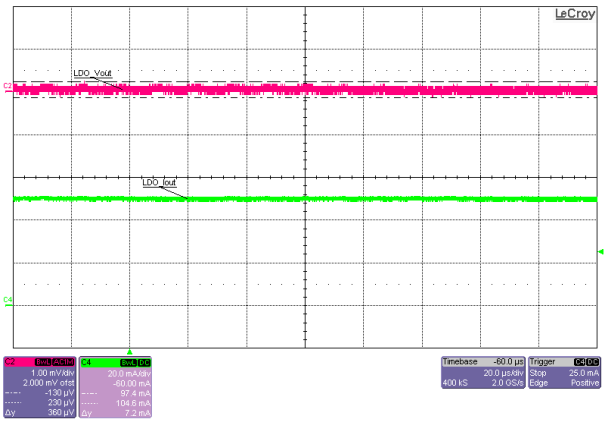


Figure 3-23. GTAVCCAUX Output Voltage Ripple (LDO), 5V Input, 1.5V Output, 0.05A Load

3.3 Load Transients

Figure 3-24 to Figure 3-39 show load transient waveforms of the converters at the corresponding input voltages and at various load step conditions.

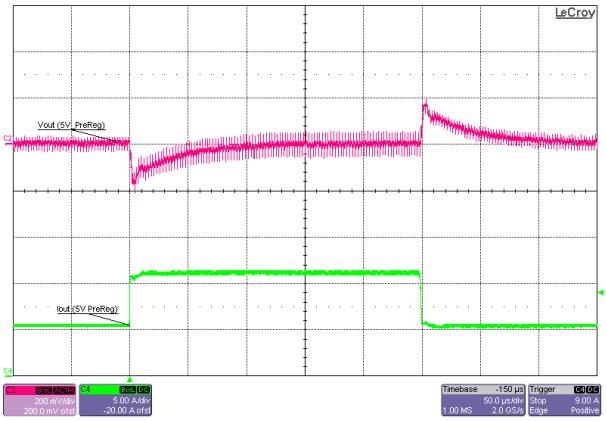


Figure 3-24. 5V Pre-Regulator Buck Converter Load Transient Response, 13.5V Input, ≈ 6A-to-12A Load Step

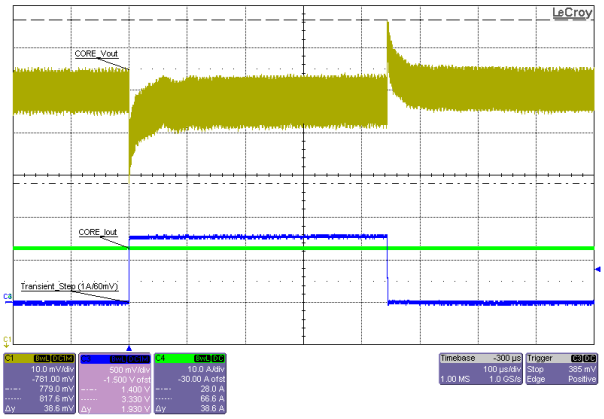


Figure 3-25. VCCINT - Core Rail Buck Converter Load Transient Response, at $5V_{IN}$, 12.8A-to-25.6A (that is, 33%-to-66%) Load Step

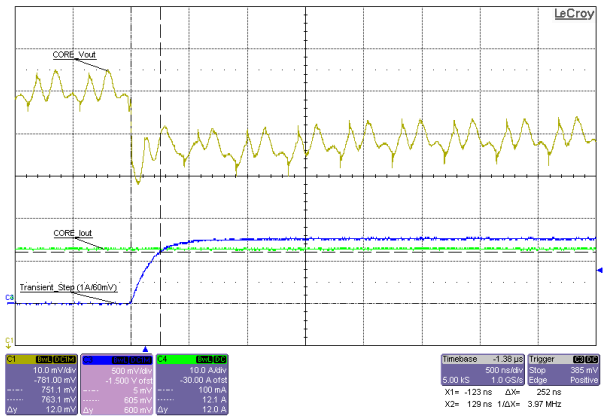


Figure 3-26. VCCINT - Core Rail Buck Converter Load Transient Response, Load Step Rising Slew Rate, at $5V_{IN}$, 12.8A-to-25.6A (that is, 33%-to-66%) Load Step (Slew Rate ≈ 40A/µs)

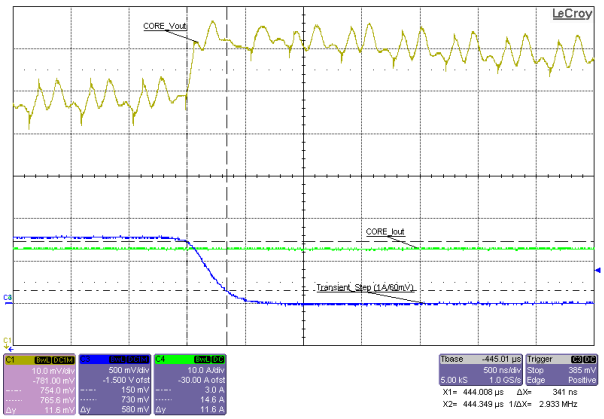


Figure 3-27. VCCINT - Core Rail Buck Converter Load Transient Response, Load Step Falling Slew Rate, at $5V_{IN}$, 25.6A-to-12.8A (that is, 66%-to-33%) Load Step (Slew Rate ≈ 28A/µs)

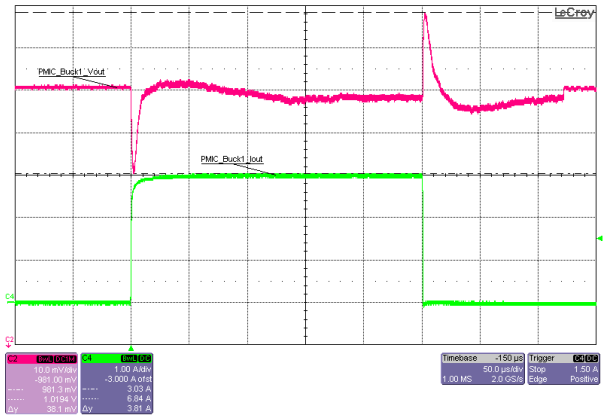


Figure 3-28. VCCO - PMIC_Buck1 Rail Converter Load Transient Response, at $5V_{IN}$, $1.0V_{OUT}$, 0A-to-3A (that is, 0%-to-100%) Load Step, PFM Mode

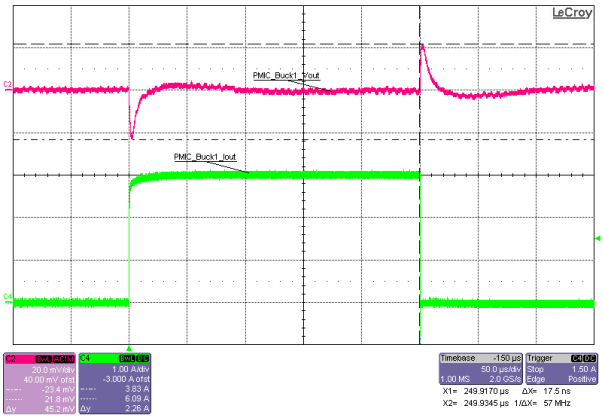


Figure 3-29. VCCO Rail Load Transient Response (PMIC_Buck1), at $5V_{IN}$, $1.0V_{OUT}$, 0A-to-3A (that is, 0%-to-100%) Load Step, FPWM Mode

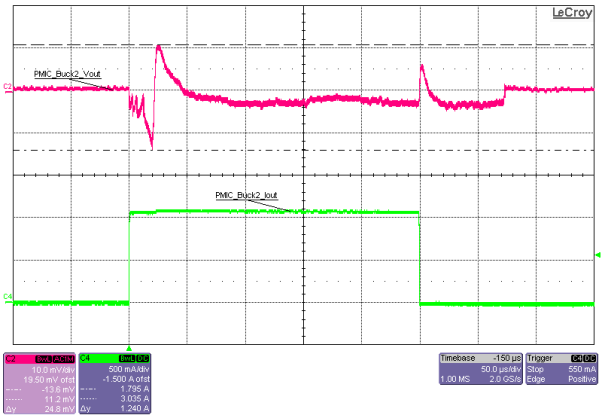


Figure 3-30. VCCAUX Rail Load Transient Response (PMIC_Buck2), at $5V_{IN}$, $1.5V_{OUT}$, 0A-to-1.1A (that is, 0%-to-100%) Load Step, PFM Mode

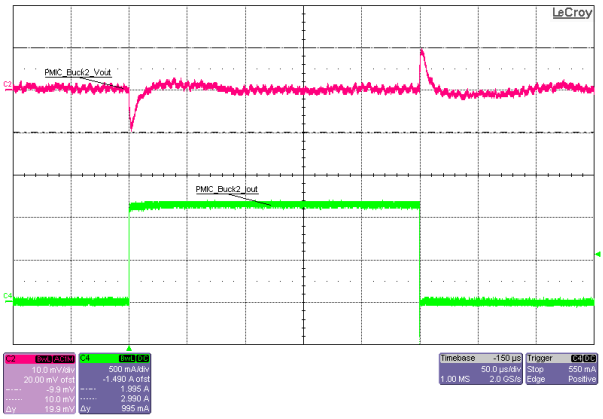


Figure 3-31. VCCAUX Rail Load Transient Response (PMIC_Buck2), at $5V_{IN}$, $1.5V_{OUT}$, 0A-to-1.1A (that is, 0%-to-100%) Load Step, FPWM Mode

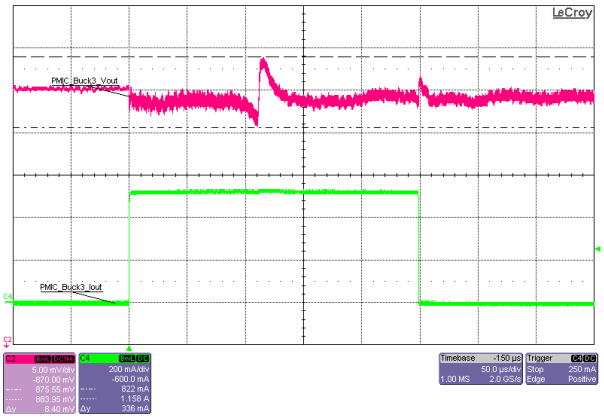


Figure 3-32. GTAVCC Rail Load Transient Response (PMIC_Buck3), at $5V_{IN}$, $0.88V_{OUT}$, 0A-to-0.49A (that is, 0%-to-70%) Load Step, PFM Mode

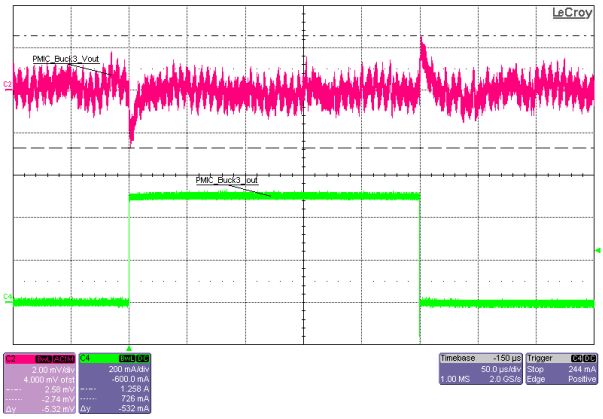


Figure 3-33. GTAVCC Rail Load Transient Response (PMIC_Buck3), at $5V_{IN}$, $0.88V_{OUT}$, 0A-to-0.49A (that is, 0%-to-70%) Load Step, FPWM Mode

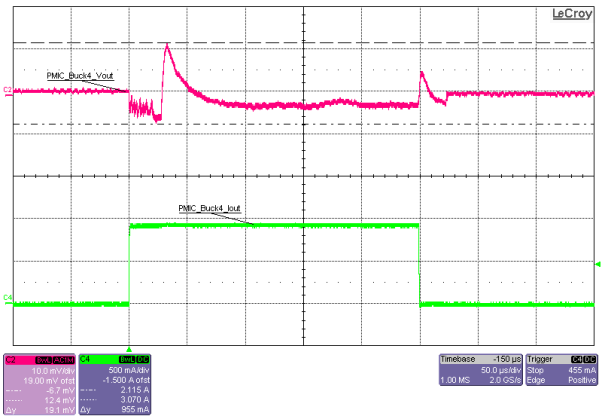


Figure 3-34. GTAVTT Rail Load Transient Response (PMIC_Buck4), at $5V_{IN}$, $1.2V_{OUT}$, 0A-to-0.91A (that is, 0%-to-70%) Load Step, PFM Mode

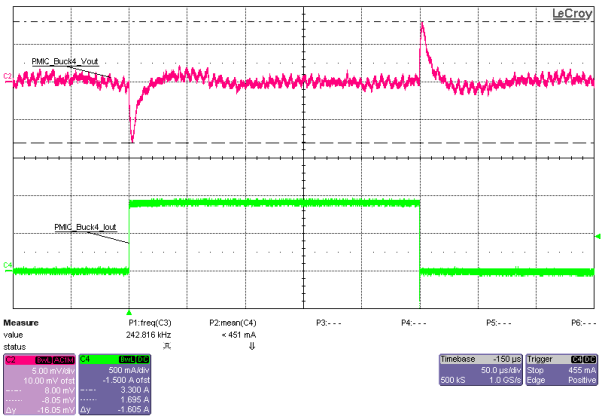


Figure 3-35. GTAVTT Rail Load Transient Response (PMIC_Buck4), at $5V_{IN}$, $1.2V_{OUT}$, 0A-to-0.91A (that is, 0%-to-70%) Load Step, FPWM Mode

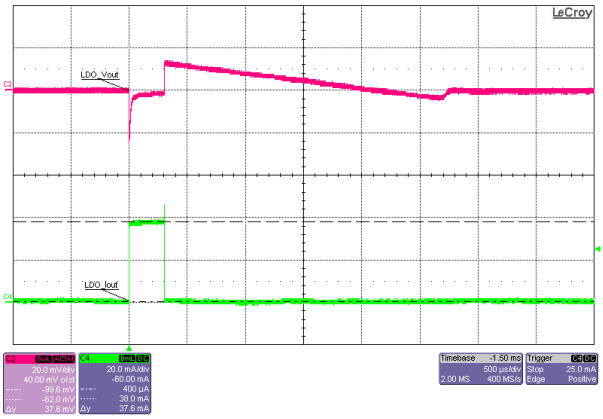


Figure 3-36. GTAVCCAUX Rail Load Transient Response (LDO), at $5V_{IN}$, $1.5V_{OUT}$, 0mA-to-35mA (that is, 0%-to-70%) Load Step, Full Step

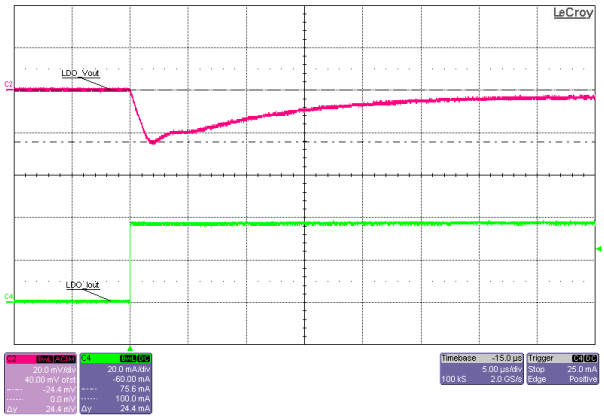


Figure 3-37. GTAVCCAUX Rail Load Transient Response (LDO), at $5V_{IN}$, $1.5V_{OUT}$, 0A-to-0.035A (that is, 0%-to-70%) Load Step, Undershoot

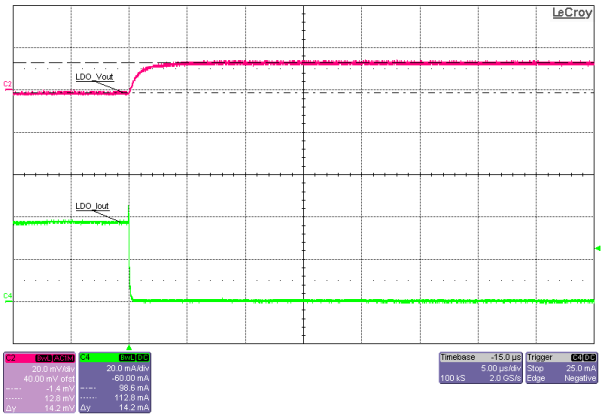


Figure 3-38. GTAVCCAUX Rail Load Transient Response (LDO), at $5V_{IN}$, $1.5V_{OUT}$, 0A-to-0.035A (that is, 0%-to-70%) Load Step, Overshoot

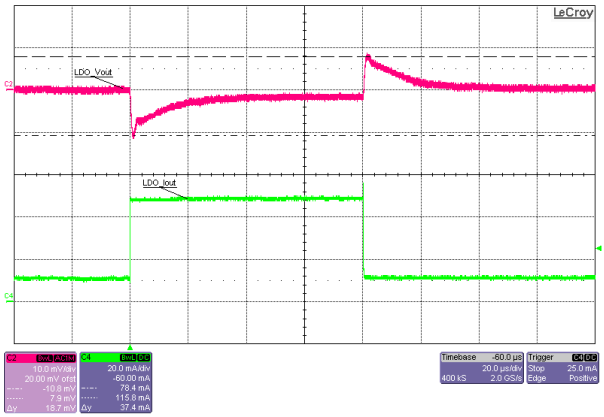


Figure 3-39. GTAVCCAUX Rail Load Transient Response (LDO), at $5V_{IN}$, $1.5V_{OUT}$, 11mA-to-48mA Load Step, Full Step

3.4 Start-Up Sequence

Figure 3-40 to Figure 3-57 show the start-up waveforms of the converters at the corresponding input voltages and at various load conditions.

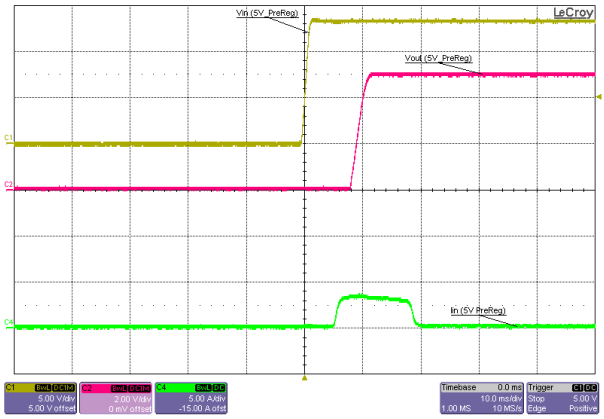


Figure 3-40. 5V Pre-Regulator Start-Up, 13.5V Input, No Load

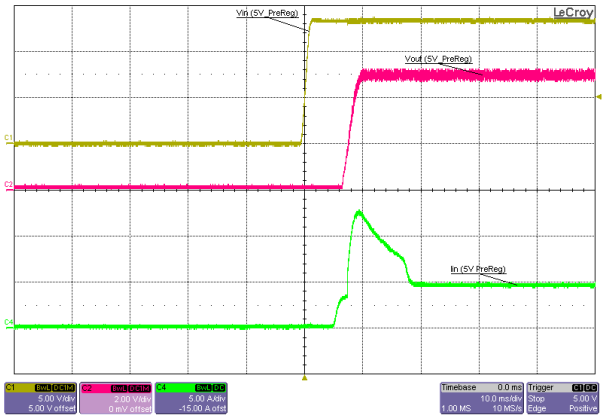


Figure 3-41. 5V Pre-Regulator Start-Up, 13.5V Input, 12A Constant-Current eLoad

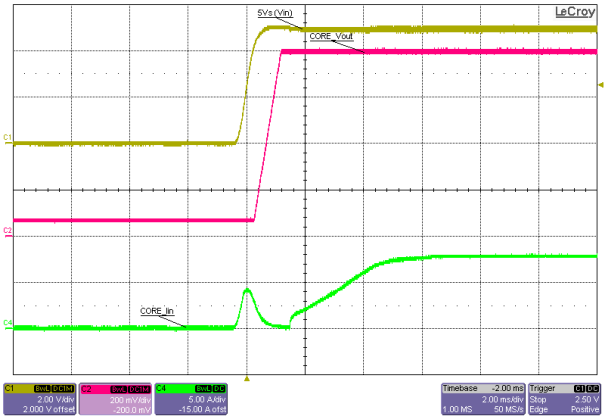


Figure 3-42. VCCINT - Core Rail Start-Up, 5V Input, 40A Constant-Resistance eLoad

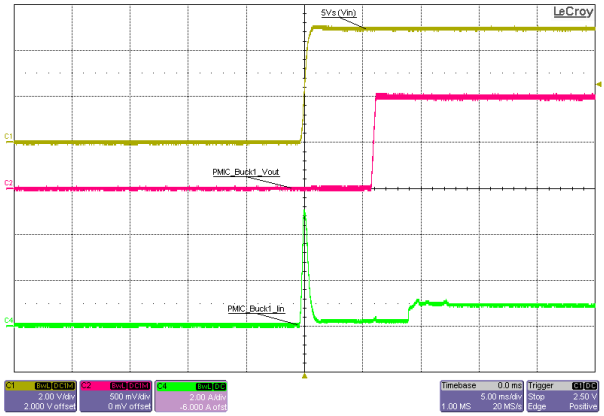


Figure 3-43. VCCO Rail Start-Up (PMIC_Buck1), 5V Input, 3A Constant-Resistance eLoad

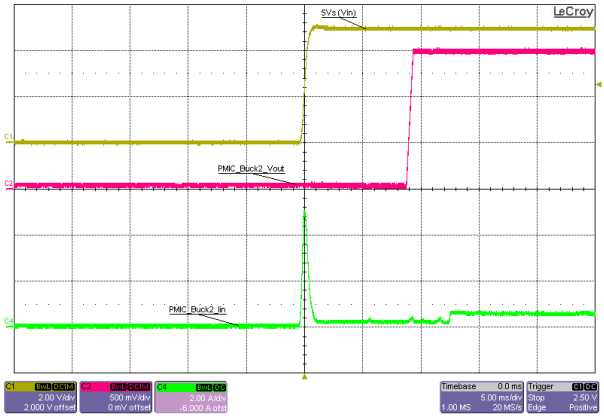


Figure 3-44. VCCAUX Rail Start-Up (PMIC_Buck2), 5V Input, 1.1A Constant-Resistance eLoad

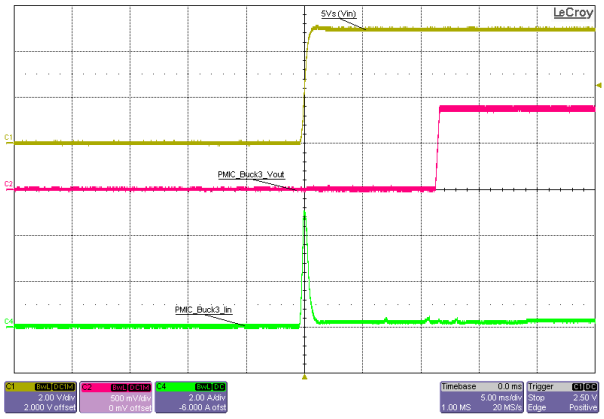


Figure 3-45. GTAVCC Rail Start-Up (PMIC_Buck3), 5V Input, 0.7A Constant-Resistance eLoad

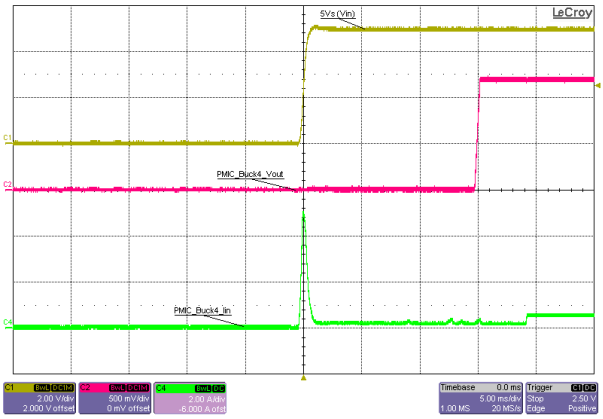


Figure 3-46. GTAVTT Rail Start-Up (PMIC_Buck4), 5V Input, 1.3A Constant-Resistance eLoad

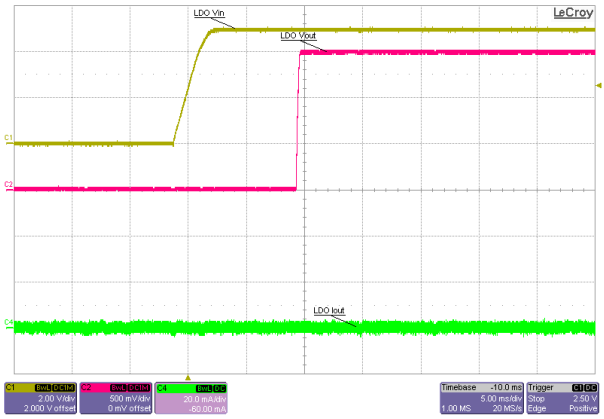


Figure 3-47. GTAVCCAUX Rail Start-Up (LDO), 5V Input, No Load

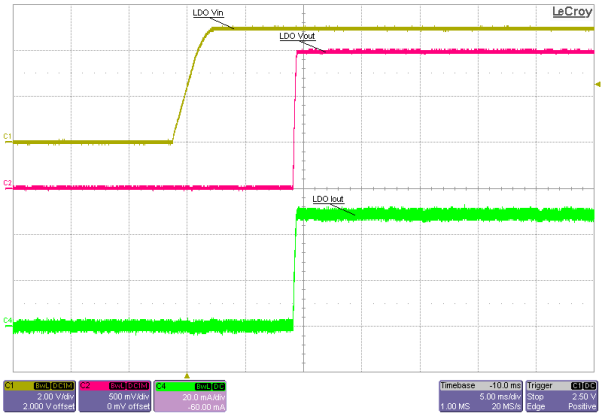


Figure 3-48. GTAVCCAUX Rail Start-Up (LDO), 5V Input, 0.05A Resistor Load

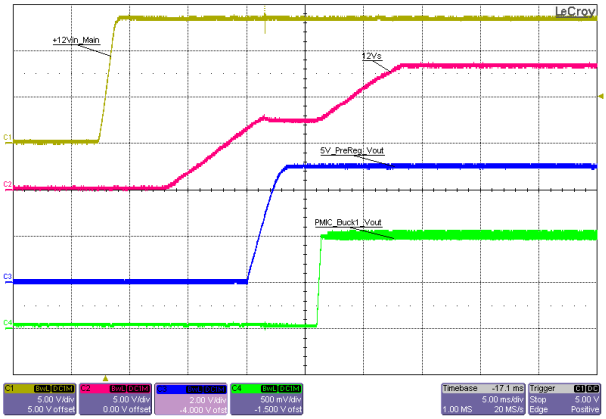


Figure 3-49. System Start-Up Into No Load, 13.5V Input, +12Vin_Main, 12Vs, 5V Pre-Regulator, VCCO (PMIC Buck 1)

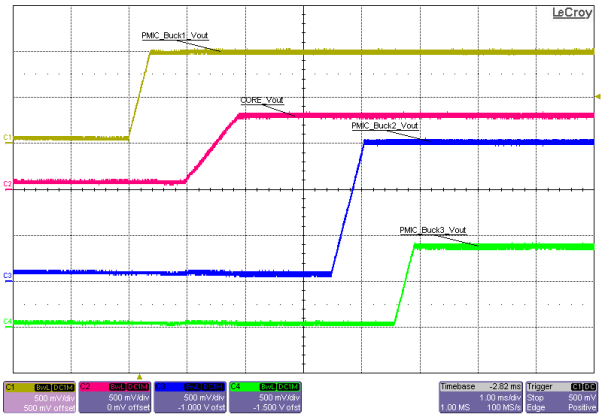


Figure 3-50. Sequence Power-Up, Sequence Rails 1, 2, 3, and 4, PMIC nRSTOUT, No Load

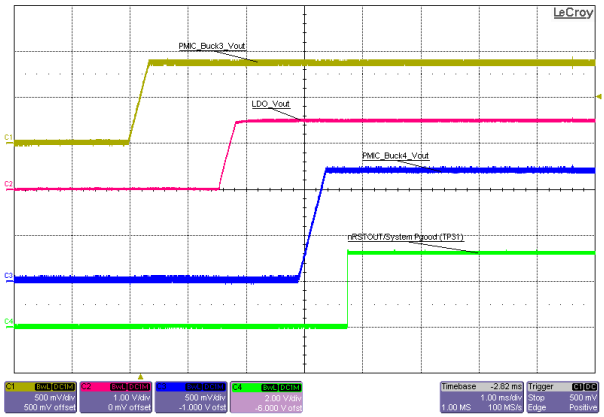


Figure 3-51. Sequence Power-Up, Sequence Rails 4, 5, and 6, PMIC nRSTOUT, No Load

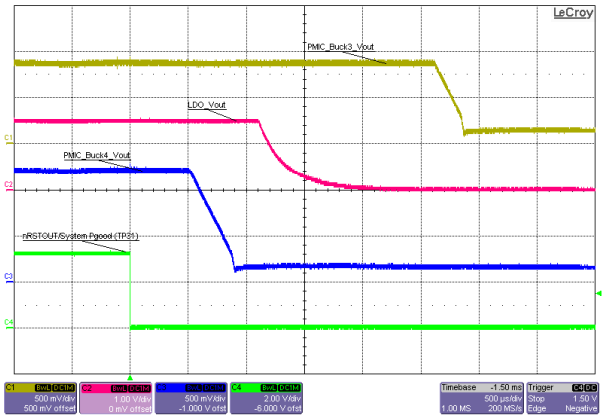


Figure 3-52. Sequence Power-Down, Sequence Rails 6, 5, and 4, PMIC nRSTOUT, No Load

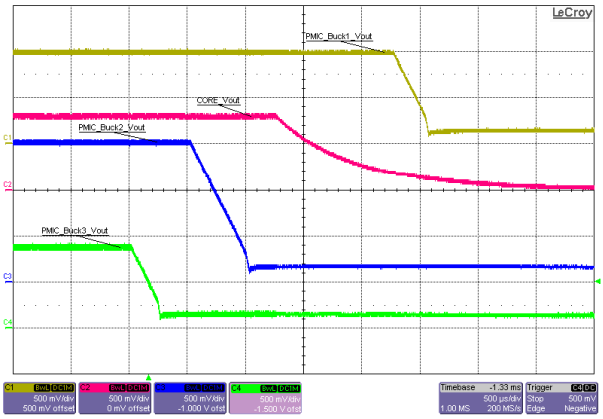


Figure 3-53. Sequence Power-Down, Sequence Rails 4, 3, 2, and 1, PMIC nRSTOUT, No Load

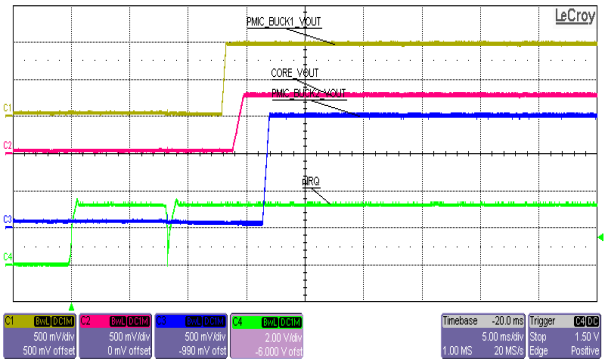


Figure 3-54. Sequence Power-Up, Sequence Rails 1, 2, 3, and 4, Discrete Vsupervisor nIRQ, No Load

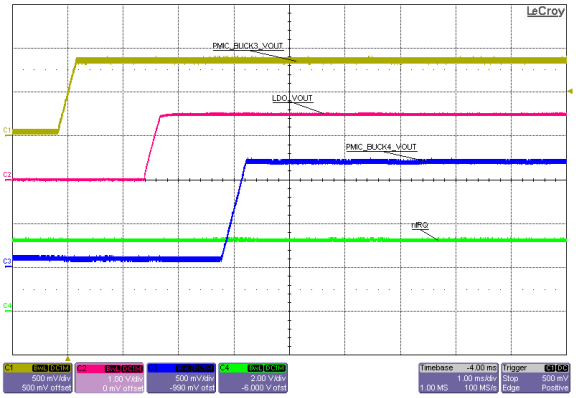


Figure 3-55. Sequence Power-Up, Sequence Rails 4, 5, and 6, Discrete Vsupervisor nIRQ, No Load

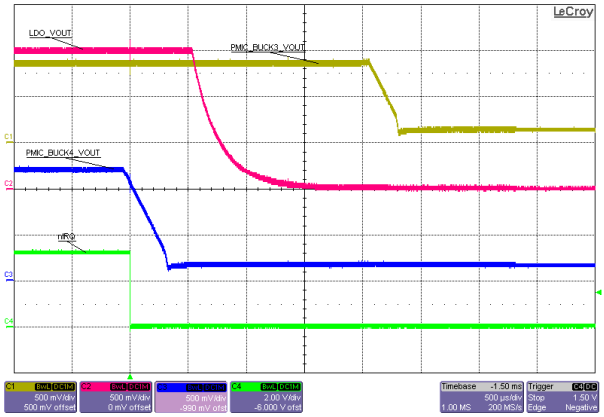


Figure 3-56. Sequence Power-Down, Sequence Rails 6, 5, and 4, Discrete Vsupervisor nIRQ, No Load

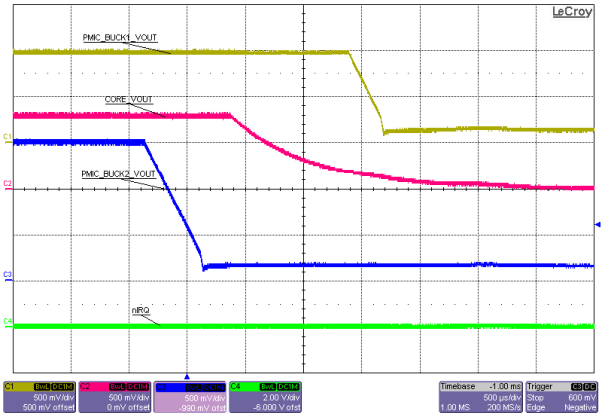


Figure 3-57. Sequence Power-Down, Sequence Rails 4, 3, 2, and 1, Discrete Vsupervisor nIRQ, No Load

3.5 Front-End Protection (FEP) Test Results

Figure 3-58 to Figure 3-62 show the UVLO, OVLO, and OCP thresholds of the front-end protection circuit.

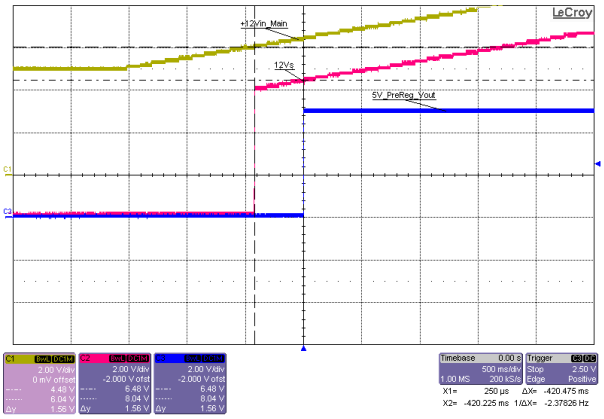


Figure 3-58. Front-End Protection, UVLO Rising Enable, 5V Pre-Regulator Buck Output No Load (FEP UVLO Enable Threshold ≈ 6.0V; 5V Pre-Regulator UVLO Enable Threshold ≈ 6.5V)

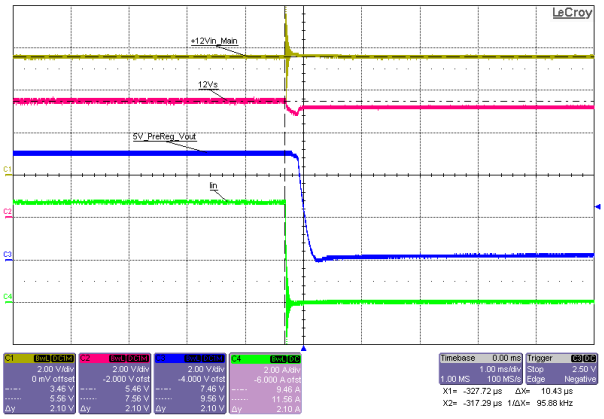


Figure 3-59. Front-End Protection, UVLO Falling Disable, 5V Pre-Regulator Buck Output Loaded at 5A Load (FEP UVLO Disable Threshold ≈ 5.6V; 5V Pre-Regulator UVLO Disable Threshold ≈ 5.2V)

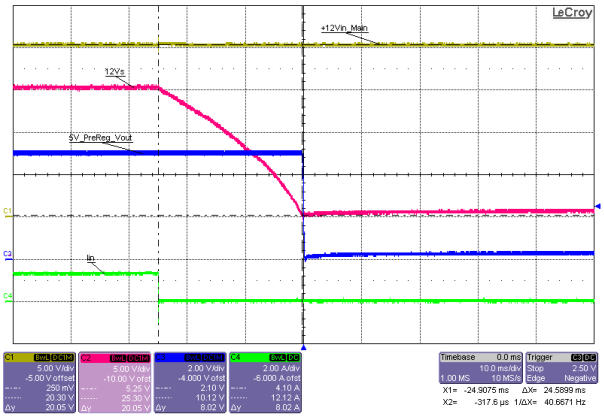


Figure 3-60. Front-End Protection, OVLO Rising Disable, 5V Pre-Regulator Buck Output Loaded at 5A Load (FEP OVLO Disable Threshold ≈ 20.3V; 5V Pre-Regulator UVLO Disable Threshold ≈ 5.2V)

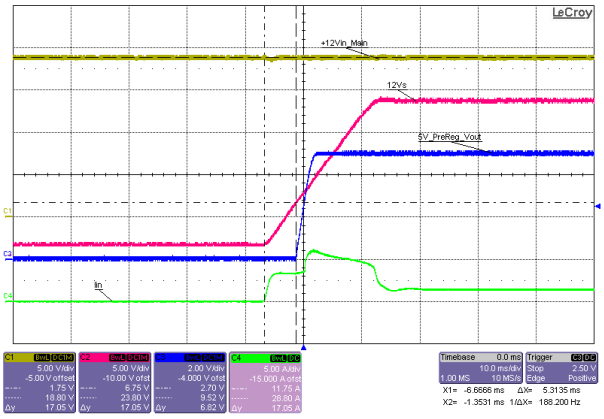


Figure 3-61. Front-End Protection, OVLO Falling Enable, 5V Pre-Regulator Buck Output Loaded at 5A Load (FEP OVLO Enable Threshold ≈ 18.8V; 5V Pre-Regulator UVLO Enable Threshold ≈ 6.75V)

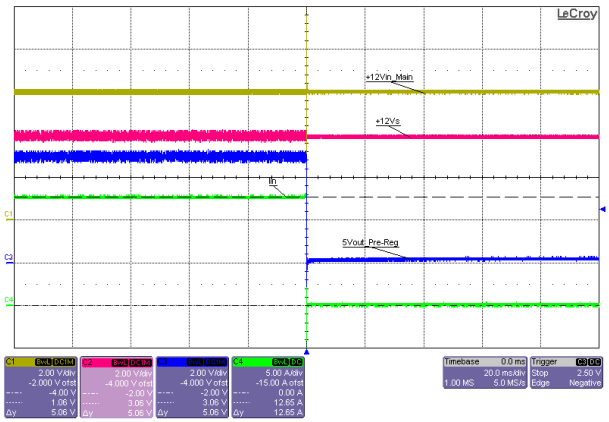


Figure 3-62. Front-End Protection, OCP Threshold Test, 5V Pre-Regulator Buck at 6V_{IN} With the Load Progressively Increasing; 100kΩ "TMR" Resistor Installed for this Test (FEP OCP Threshold ≈ 12.65A)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265