Using the TPS59650EVM-753 Intel™ IMVP-7 3-Phase CPU/2-Phase GPU SVID Power System

The TPS59650EVM-753 evaluation module (EVM) is a complete solution for Intel™ IMVP7 Serial VID(SVID) Power System from a 9V-20V input bus. This EVM uses the TPS59650 for IMVP7 - 3-Phase CPU and 2-Phase GPU Vcore controller, the TPS51219 for 1.05VCCIO, TPS51916 for DDR3L/DDR4 Memory rail (1.2VDDQ, 0.6VTT and 0.6VTTREF) and also uses the (CSD87350Q5D) a 5mm x 6mm TI's power block MOSFETs that uses Powerstack™ technology with high-side and low-side MOSFETs for high power density and superior thermal performance.

Contents

List of Figures

List of Tables

1 Description

The TPS59650EVM-753 is designed to use a 9V-20V Input bus to produce 6 regulated outputs for IMVP7 SVID CPU/GPU Power System. The TPS59650EVM-753 is specially designed to demonstrate the TPS59650 full IMVP7 mobile feature while providing GUI communication programing and a number of test points to evaluate the static and dynamic performance of TPS59650.

1.1 Typical Applications

- IMVP7 Vcore Applications for Adapter, Battery, NVDC or 3V/5V/12V rails

1.2 Features

The TPS59650EVM-753 features:

- Complete solution for 9V-20V Input Intel IMVP7 SVID Power System
- GUI communication to demonstrate full IMVP7 Mobile feature
- 3-Phase CPU Vcore can support up to 94A output current
- 2-Phase GPU Vcore can support up to 46A output current
- 8 Selectable Switching frequency for CPU and GPU power
- 8 Levels selectable current limit for CPU and GPU power
- Switches or Jumpers for each output enable
- On Board Dynamic Load for CPU, GPU Vcore and VCCIO output
- High efficiency and high density by using TI power block MOSFET
- Convenient test points for probing critical waveforms
- Eight Layer PCB with 1oz copper

2 TPS59650EVM-753 Power System Block Diagram

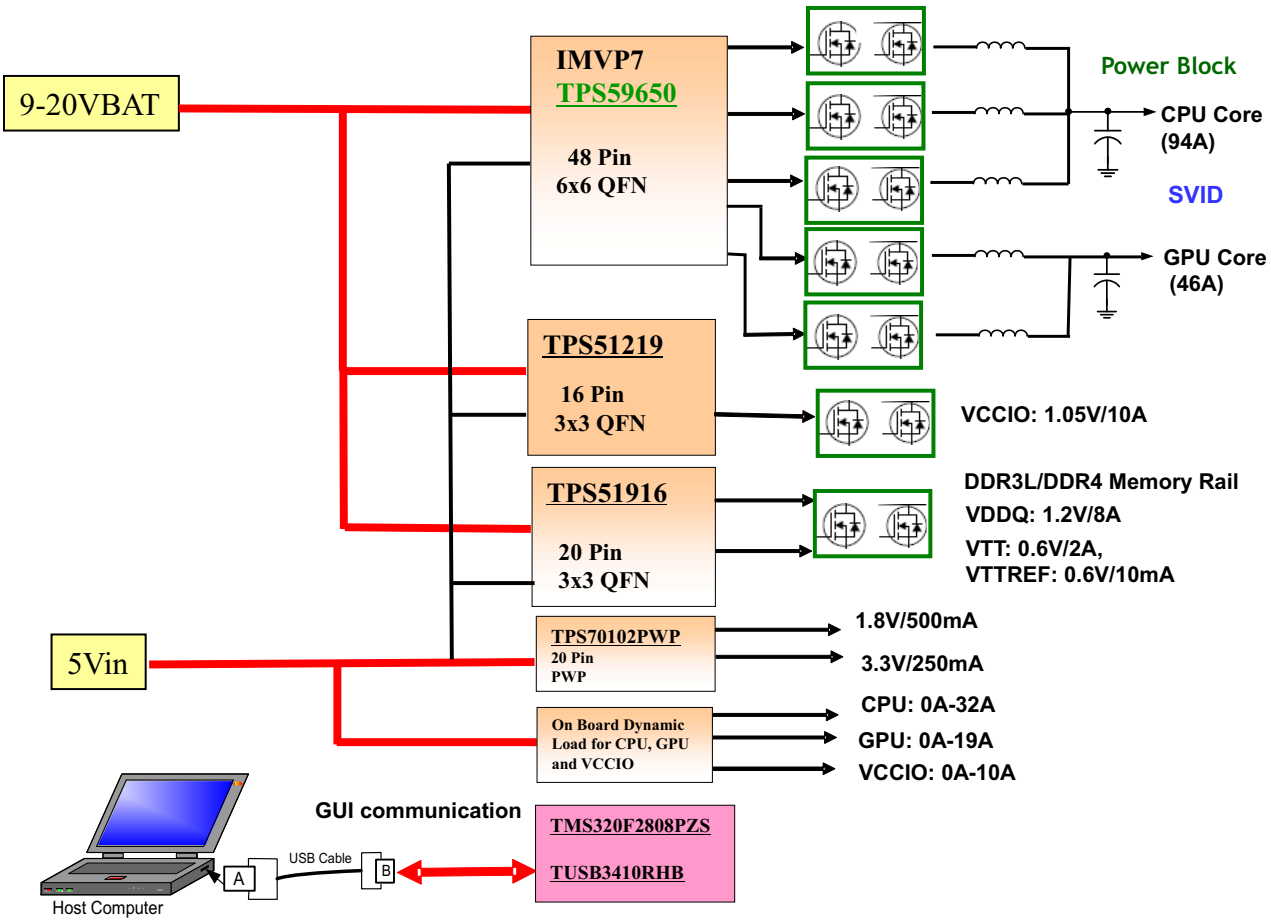


Figure 1. TPS59650EVM-753 Power System Block Diagram

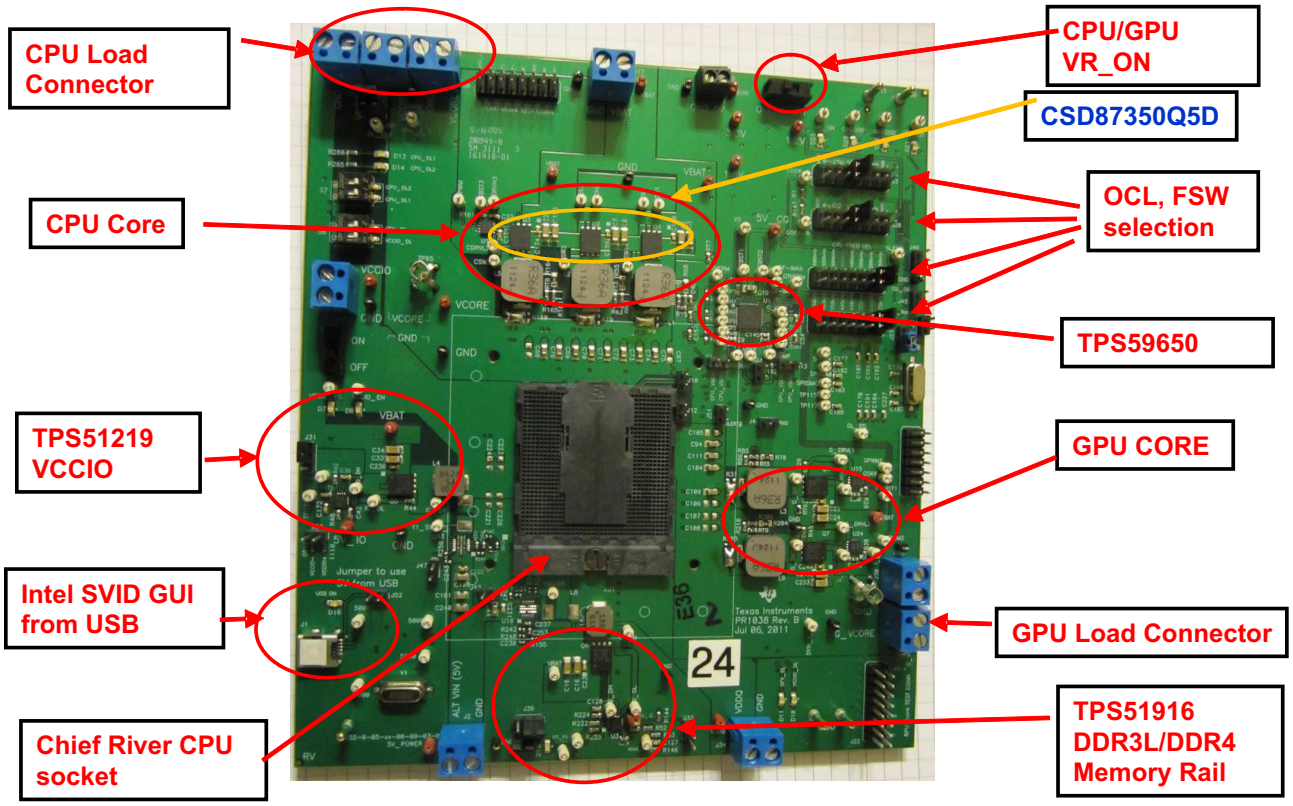


Figure 2. TPS59650EVM-753 EVM Illustration

3 Electrical Performance Specifications

Table 1. TPS59650EVM-753 Electrical Performance Specifications[(1)]

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
12VBAT input voltage range	VBAT	9	12	20	V
Maximum input current	VBAT = 12V, all full load (3-Phase CPU/2-Phase GPU)		15.5		A
No load input current	VBAT=12V, all no load(3-Phase CPU/2 Phase GPU)		0.14		A
5VIN input voltage range	5Vin	4.5	5	5.5	V
Maximum input current	VBAT =12 V, all full load		0.3		A
No load input current	VBAT=12V, all no load		0.1		A
OUTPUT CHARACTERISTICS					
CPU(TPS59650)					
Output voltage Vcore	SVID: Address:00 CPU, Payload: 1.05V		1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation(Droop) Load Line		–1.9		mΩ
Output voltage ripple	VBAT=12V, 1.05V/90A(3-Phase) at 300kHz		25		mVpp
Output load current	CPU 3-Phase operation	0		94	A
Output over current	Selectable per phase		37		A
Switching frequency	Selectable	250	300	600	kHz
Full load efficiency	VBAT=12V, 1.05V/95A at 300kHz		80.05%		
GPU(TPS59650)					
Output voltage Vcore	SVID: Address:01 GPU, Payload: 1.23V		1.23		V

(1) Jumpers set to default locations, see section 6 of this user's guide

Table 1. TPS59650EVM-753 Electrical Performance Specifications[(1)] (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output voltage regulation	Line regulation		0.1%		
	Load regulation(Droop) Load Line		–3.9		mΩ
Output voltage ripple	VBAT=12V, 1.23V/50A 2 Phase at 385kHz		30		mVpp
Output load current		0		50	A
Output over current	Selectable per phase		37		A
Switching frequency	Selectable	275	385	660	kHz
Full load efficiency	VBAT=12V, 1.23V/50A 2 Phase at 385KHz		86.58%		
1.05V VCCIO (TPS51219)					
Output voltage			1.05		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VBAT=12V, 1.05V/10A		30		mVpp
Output load current		0		10	A
Output over current			16		A
Switching frequency	Selectable		500		kHz
Full load efficiency	VBAT=12V, 1.05V/10A		89.87%		
DDR3L/DDR4 Memory Rail (TPS51916)					
Output voltage			1.2		V
Output voltage regulation	Line regulation		0.1%		
	Load regulation		0.1%		
Output voltage ripple	VBAT=12V, 1.2V/8A		30		mVpp
Output load current		0		8	A
Output over current			10		A
Switching frequency	Selectable		500		kHz
Full load efficiency	VBAT=12V, 1.2V/8A		89.07%		
Operating temperature			25		°C

4 Test Setup

4.1 Test Equipment

4.1.1 PC Computer (Host Computer)

Microsoft Windows XP or newer with available USB port

4.1.2 USB Cable

The USB Cable: Standard USB_A to USB_B 5 Pin Mini-B cable. See Figure 3 .

Figure 3. USB Cable

4.1.3 TPS59650 USB driver and SVID GUI Installation

1. Copy the both files: setup.exe and setup.msi to the host computer.
2. Run this setup.exe.
3. Following installation Instructions, this will install the driver and the Texas Instruments SVID GUI.
4. It will add the below icon

4.1.4 DC Source

12VBAT DC Source: The 12VBAT DC source should be a 0-20V variable DC source capable of supplying 20Adc current. Connect 12VBAT to J21 as shown in Figure 4.

5Vin DC Source: The 5Vin DC source should be a 0-5V variable DC source capable of supplying 1Adc current. Connect 5Vin to J22 as shown in Figure 4.

4.1.5 Meters

- **V1:** 5Vin at TP81(5Vin) and TP83(GND)
- **V2:** 12VBAT at TP82(VBAT) and TP24(GND)
- **V3:** CPU Vcore sense voltage at J7; GPU Vcore sense voltage at J9; VDDQ sense voltage at J20, VCCIO sense voltage at J16
- **A1:** 12VBAT input current

4.1.6 Load

The output load should be an electronic constant current load capable of 0-90Adc.

4.1.7 Oscilloscope

A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for 1MΩ impedance, 20MHz Bandwidth, AC coupling, 2us/division horizontal resolution, 50mV/division vertical resolution. Test point TP30 and TP46 can be used to measure the output ripple voltage for CPU and GPU. Do not use a leaded ground connection as this may induce additional noise due to the large ground loop.

4.2 Recommended Wire Gauge

1. **V5in to J22(5V input):**
   The recommended wire size is 1x AWG #18 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
2. **12VBAT to J21(12V input):**
   The recommended wire size is 1x AWG #16 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return).
3. **J1, J2, J3(CPU) to LOAD or J4, J5 (GPU) to LOAD or J19 (VDDQ) to LOAD or J15(VCCIO) to LOAD:**
   The minimum recommended wire size is 2x AWG #16, with the total length of wire less than 4 feet (2 feet output, 2 feet return)

4.3 Recommended Test Setup

Figure 4 is the recommended test set up to evaluate the TPS59650EVM-753.Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before handling the EVM.

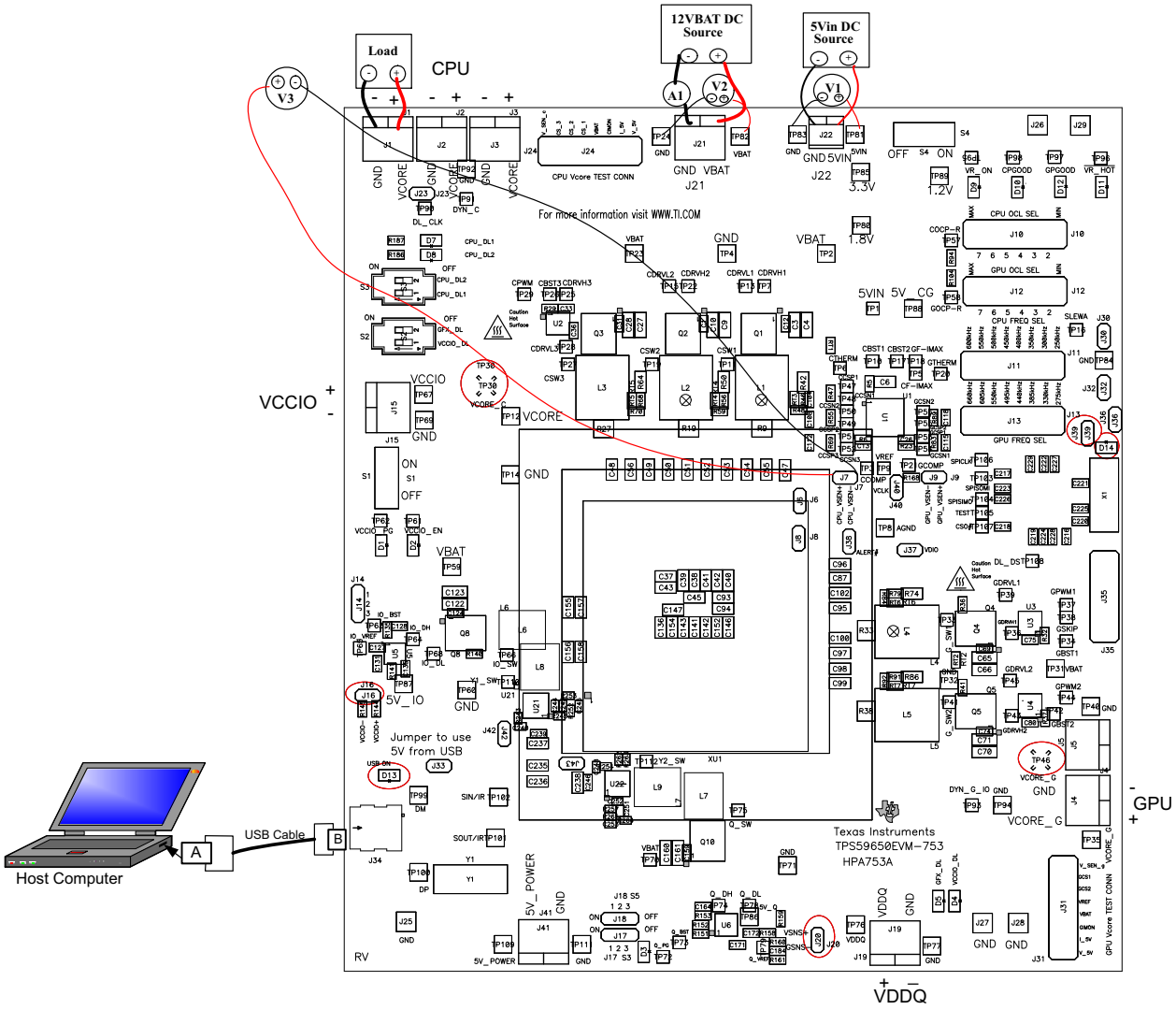


Figure 4. TPS59650EVM-753 Recommended Test Set Up

4.4 USB Cable Connections

A standard USB_A and 5 pin Mini_B USB cable needed to connect between host computer and J34 USB port (left bottom side). A GREEN LED(D13) will light up near the USB port on the EVM. This just means USB cable is connected.

4.5 Input Connections

1. Prior to connecting the 5Vin DC source, it is advisable to limit the source current from 5Vin to 1A maximum. Make sure 5Vin is initially set to 0V and connected as shown in Figure 4.
2. Prior to connecting the 12VBAT DC source, it is advisable to limit the source current from 12VBAT to 10A maximum. Make sure 12VBAT is initially set to 0V and connected as shown in Figure 4.
3. Connect voltmeters V1 at TP81 (5Vin) and TP83 (GND) to measure 5Vin voltage, V2 at TP82 (VBAT) and TP24 (GND) to measure 12VBAT voltage as shown in Figure 4.
4. Connect a current meter A1 between 12VBAT DC source and J21 to measure the 12VBAT input current.

4.6 Output Connections

1. Connect Load to J1, J2, J3 and set Load to constant resistance mode to sink 0Adc before 5Vin and 12VBAT are applied. This is for CPU operation.
2. Connect a voltmeter V3 at J7 to measure CPU Vcore sense voltage.

5 Configuration

All Jumper selections should be made prior to applying power to the EVM. User can configure this EVM per following configurations.

5.1 CPU and GPU Configuration

5.1.1 CPU/GPU Current Limit Trip Selection (J10 for CPU and J12 for GPU)

The current limit trip can be set by J10(COCP) and J12(GOCP).

Default setting: Level 5 for both CPU and GPU.

Table 2. Current Limit Trip Selection

Jumper set to	Connected Resistor	COCP/GOCP Limit (Typ.)
Left (1-2 pin shorted)	150k	Max
2nd(3-4 pin shorted)	100k	Level 7
3rd(5-6 pin shorted)	75k	Level 6
4th(7-8 pin shorted)	**56.2k**	**Level 5**
5th(9-10 pin shorted)	39.2k	Level 4
6th(11-12 pin shorted)	30.1k	Level 3
7th(13-14 pin shorted)	24.3k	Level 2
Right(15-16 pin shorted)	20.0k	Min

5.1.2 CPU Frequency Selection (J11)

The operating frequency can be set by J11

Default setting: 300 kHz for CPU

Table 3. CPU Frequency Selection

Jumper set to	Connected Resistor	CPU
Left (1-2 pin shorted)	150k	600 kHz
2nd(3-4 pin shorted)	100k	550 kHz
3rd(5-6 pin shorted)	75k	500 kHz
4th(7-8 pin shorted)	56.2k	450 kHz
5th(9-10 pin shorted)	39.2k	400 kHz
6th(11-12 pin shorted)	30.1k	350 kHz
7th(13-14 pin shorted)	**24.3k**	**300 kHz**
Right(15-16 pin shorted)	20.0k	250 kHz

5.1.3 GPU Frequency Selection (J13)

The operating frequency can be set by J13

Default setting: 385 kHz for GPU.

Table 4. GPU Frequency Selection

Jumper set to	Connected Resistor	GPU
Left (1-2 pin shorted)	150k	660 kHz
2nd(3-4 pin shorted)	100k	605 kHz
3rd(5-6 pin shorted)	75k	550 kHz
4th(7-8 pin shorted)	56.2k	495 kHz
5th(9-10 pin shorted)	39.2k	440 kHz
6th(11-12 pin shorted)	**30.1k**	**385 kHz**
7th(13-14 pin shorted)	24.3k	330 kHz
Right(15-16 pin shorted)	20.0k	275 kHz

5.1.4 F2808 DSP Program Mode Selection (J39)

The F2808 DSP Program Mode(GUI) Selection can be set by J39.

Default setting: No Jumper shorts on J39 for normal operation

Table 5. F2808 DSP Program Mode Selection

Jumper set to	Program Mode Selection
No Jumper on J39	**Normal Operation**
Jumper on J39	Flash the DSP program to the EVM

5.1.5 5Vin Bias Voltage Option (J33)

The 5Vin Bias Voltage can be used from USB or Externally

Default setting: No Jumper shorts on J33

Table 6. 5Vin Bias Voltage Option (J33)

Jumper set to	Selection
No Jumper	**5Vin Bias from J22 external**
Jumper on J39	5Vin Bias from USB, 5Vin from J22 should not be connected

5.1.6 On Board Dynamic Load Selection (S3 for CPU, S2(upper) for GPU, S2(lower) for VCCIO)

The on board dynamic load can be set by S2 and S3.

Default setting: Push S2 and S3 to "OFF" position to disable the on board dynamic load

Table 7. On Board Dynamic Load Selection

Switch set to	Dynamic Load Selection
Push S3 to "ON" position	Enable 32A on board dynamic load at CPU
Push S3 to "OFF" position	**Disable 32A on board dynamic load at CPU**
Push S2(upper) to "ON" position	Enable 19A on board dynamic load at GPU
Push S2(upper) to "OFF" position	**Disable 19A on board dynamic load at GPU**
Push S2(lower) to "ON" position	Enable 10A on board dynamic load at VCCIO
Push S2(lower) to "OFF" position	**Disable 10A on board dynamic load at VCCIO**

5.1.7 IMVP-7 VR_ON Enable Selection (S4)

The IMVP-7 CPU/GPU can be enabled and disabled by S4

Default setting: Push S4 to "OFF" position to disable both CPU and GPU

Table 8. VR_ON Enable Selection

Switch set to	VR_ON Selection
Push S4 to "ON" position	Enable IMVP-7 CPU/GPU Vcore
Push S4 to "OFF" position	**Disable IMVP-7 CPU/GPU Vcore**

5.2 1.2VDDQ, 0.6V VTT and 0.6V VTTREF Configuration

5.2.1 VDDQ S3, S5 Enable Selection

The controller can be enabled and disabled by J18 and J17.

Default setting: Jumper shorts on Pin2 and Pin3 of J18,
Jumper shorts on Pin2 and Pin3 of J17

Table 9. VDDQ S3, S5 Enable Selection

State	J17 (S3) set to	J18(S5) set to	VDDQ	VTTREF	VTT
S0	ON position	ON position	ON	ON	ON
S3	OFF position	ON position	ON	ON	OFF(High-Z)
S4/S5	**OFF position**	**OFF position**	**OFF(Discharge)**	**OFF(Discharge)**	**OFF(Discharge)**

5.3 1.05V VCCIO Configuration

5.3.1 1.05V Enable Selection (S1)

1.05V Enable can be set by S1

Default setting: Push S1 to "OFF" position

Table 10. 1.05V Enable Selection

Jumper set to	Selection
Push S1 to "ON" position	1.05V Enabled
Push S1 to "OFF" position	**1.05V Disabled**

5.3.2 VCCIO Output Voltage Selection (J14)

The VCCIO Output Voltage can be selected by J14

Default setting: Jumper shorts Pin1 and Pin2 of J14

Table 11. VCCIO Output Voltage Selection

Jumper set to	Selection
Jumper shorts on Pin1 and Pin2	**VCCIO: 1.05V**
Jumper shorts on Pin2 and Pin3	VCCIO: 1.00V

5.3.3 On Board Dyanamic Load Enable Pin (J23)

The on board dynamic load can be enabled or disabled by J23

Default setting: Jumper shorts on J23

Table 12. On Board Dynamic Load Enable/Disable selection

Jumper set to	Selection
Jumper shorts	**Enable on board dynamic load**
No Jumper short	Disable on board dynamic load

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

6.1.1 CPU

1. Set up EVM as described in Section 4.3 through Section 4.6 and Figure 4.
2. Ensure J39 no Jumper shorts on
3. Ensure all other Jumpers configuration setting by Section 5 before 5Vin and 12VBAT are applied.
4. Ensure Load is set to constant resistance mode and to sink 0Adc
5. Ensure S1 and S4 are in “OFF” position
6. Add scope probe on the TP30 for CPU Vcore ripple measurement
7. Ensure USB Cable is connected between host computer and USB port(J34) on the EVM
8. Increase 5Vin from 0V to 5V. Using V1 to measure 5Vin input voltage.
9. Increase 12VBAT from 0V to 12V. Using V2 to measure 12VBAT input voltage.

10. Double-Click the icon to launch the GUI program. The GUI window shown in Figure 5.
11. Push S4 to “ON” position to enable the VR_ON of TPS59650. VR_ON LED will light up.
12. Now the user is ready to send SVID commends. The GUI at start-up defaults:
    Address: 00 CPU, Commend: SetVIDslow, Payload: 1.05V (The user can select the SVID commend by using the pull-down menu”)
13. Click “send Commend” and CPU CPGOOD LED will light up, See the GUI window as Figure 5.
14. Measure V3: CPU Vcore at J7 and A1: 12VBAT input current
15. Vary CPU LOAD from 0Adc to 94Adc, CPU Vcore must remain in load line
16. Vary 12VBAT from 9V to 20V CPU Vcore must remain in line regulation
17. Push S4 to “OFF” position to disable CPU Vcore controller.
18. Decrease LOAD to 0A and disconnect the LOAD from terminal J1, J2, J3
19. Disconnect V3 from J7.
20. Disconnect scope probe from TP30

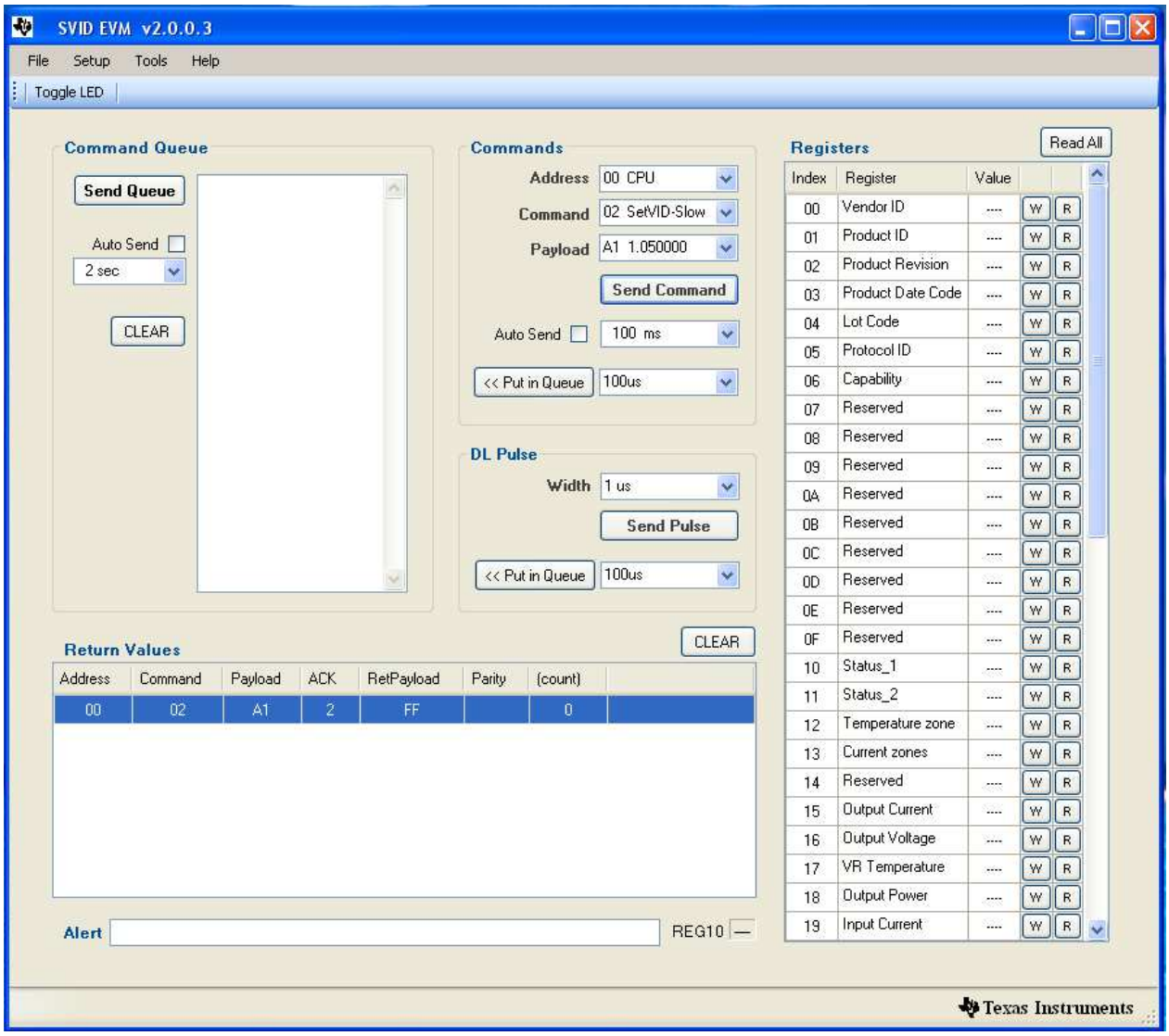


Figure 5. TPS59650EVM-753 CPU GUI set up Window

6.1.2 GPU

1. Connect the LOAD to GPU terminal J4, J5 and V3 at J9. Ensure correct polarity.
2. Add scope probe on the TP46 for GPU Vcore_G ripple measurement
3. Push S4 to “ON” position to enable the VR_ON of TPS59650. The VR_ON LED will light up.
4. Now you are ready to send SVID commends for GPU. Using pull-down menu:
   Address: 01 GPU, Commend: SetVIDslow, Payload: 1.23V
5. Click “send Commend” and GPU GPOOD LED will light up, See the GUI window as Figure 6.

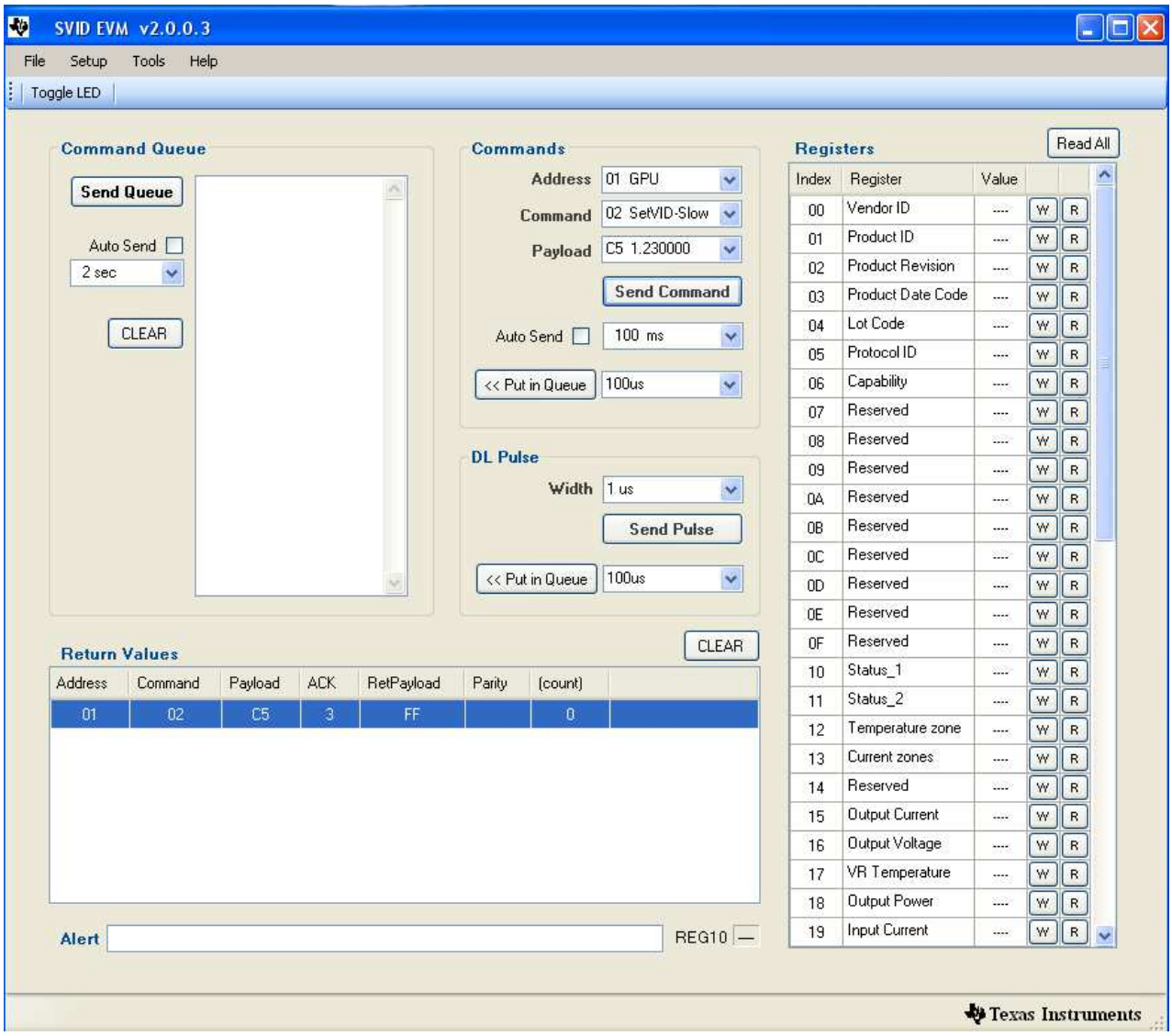


Figure 6. TPS59650EVM-753 GPU GUI set up Window

6. Measure V3: GPU Vcore_G at J9 and A1: 12VBAT input current
7. Vary GPU LOAD from 0Adc to 50Adc, GPU Vcore must remain in load line
8. Vary 12VBAT from 9V to 20V GPU Vcore must remain in line regulation
9. Push S4 to “OFF” position to disable GPU Vcore controller.
10. Decrease LOAD to 0A and disconnect the LOAD from terminal J11
11. Disconnect V3 from J9.
12. Disconnect scope probe from TP46
13. Exit SVID GUI window: click File → click Exit
14. Disconnect the USB cable between host Computer and EVM

6.1.3 VDDQ

1. Connect the LOAD to VDDQ terminal J19 and V3 at J20. Ensure correct polarity.
2. Remove Jumper from J17, J18 from pin2 and pin3 and put this Jumper on pin1 and pin 2 of J18, J17 to enable S5 of VDDQ controller. VDDQ PGOOD LED will light up.
3. Measure V3: VDDQ at J20 and A1: 12Vin input current
4. Vary VDDQ LOAD from 0Adc to 8Adc, VDDQ must remain in the load regulation
5. Vary 12VBAT from 9V to 20V, VDDQ must remain in the line regulation
6. Remove Jumper of J17, J18 and shorts back on pin2 and pin3 of J17, J18 to disable VDDQ controller.
7. Decrease LOAD to 0A and disconnect the LOAD from terminal J19
8. Disconnect V3 from J20.

6.1.4 VCCIO

1. Connect the LOAD to VCCIO terminal J15 and V3 at J16. Ensure correct polarity.
2. Push S1 to “ON” position to enable the VCCIO controller. VCCIO EN and PGOOD LED will light up.
3. Measure V3: VCCIO at J16 and A1: 12Vin input current
4. Vary VDDQ LOAD from 0Adc to 10Adc, VCCIO must remain in the load regulation
5. Vary 12VBAT from 9V to 20V, VCCIO must remain in the line regulation
6. Push S1 to “OFF” position to disable VCCIO controller.
7. Decrease LOAD to 0A and disconnect the LOAD from terminal J15
8. Disconnect V3 from J16.

6.2 Equipment Shutdown

1. Shut down Load
2. Shut down 12VBAT and 5Vin
3. Shut down oscilloscope
4. Shut down host computer

7 Performance Data and Typical Characteristic Curves

Figure 7 through Figure 91 present typical performance curves for TPS59650EVM-753. Jumpers set to default locations, see section 6 of this user's guide.

7.1 CPU 3-Phase Operation

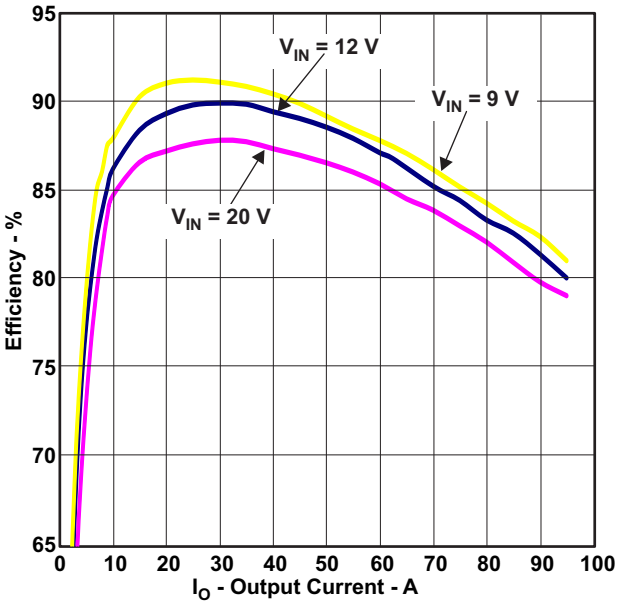


Figure 7. CPU3 Efficiency

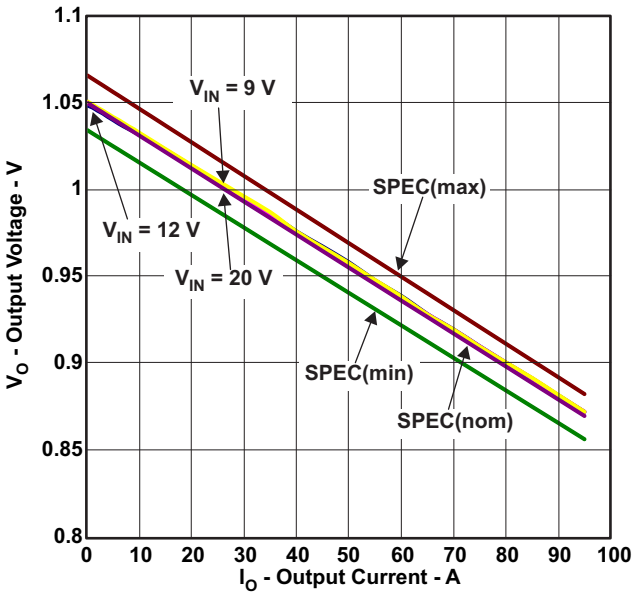


Figure 8. CPU3 Load regulation

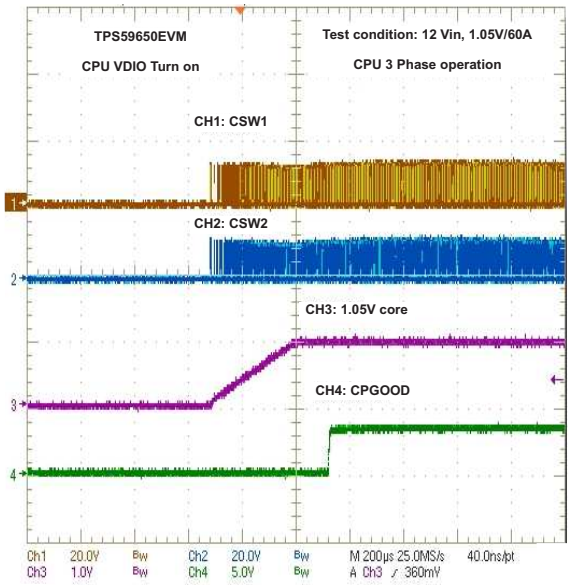


Figure 9. CPU3 Enable Turn on

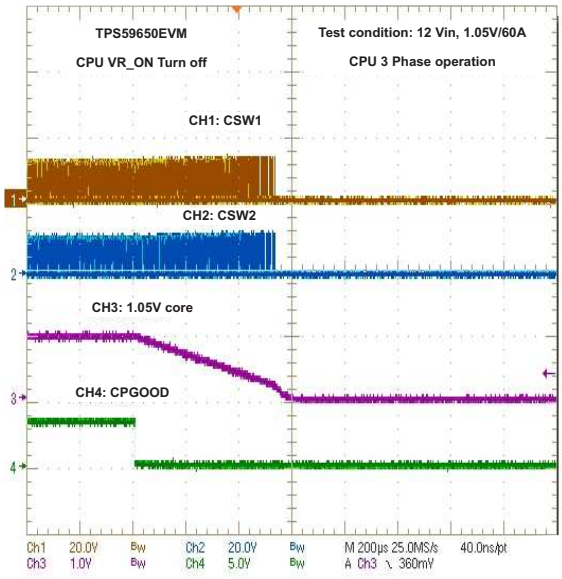


Figure 10. CPU3 Enable Turn off

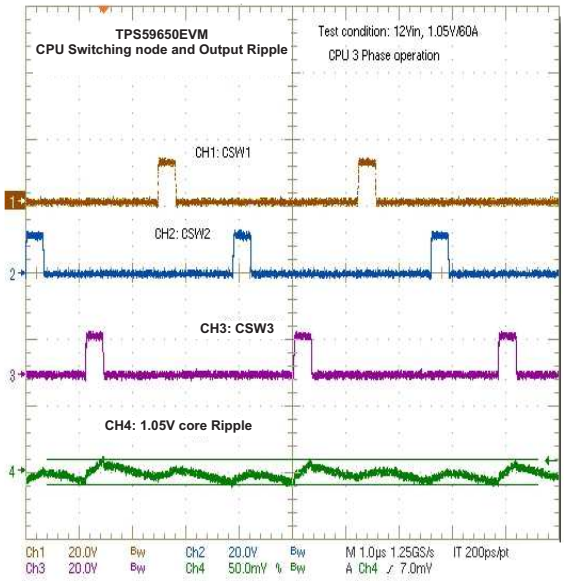


Figure 11. CPU3 Switching Node(Ripple)

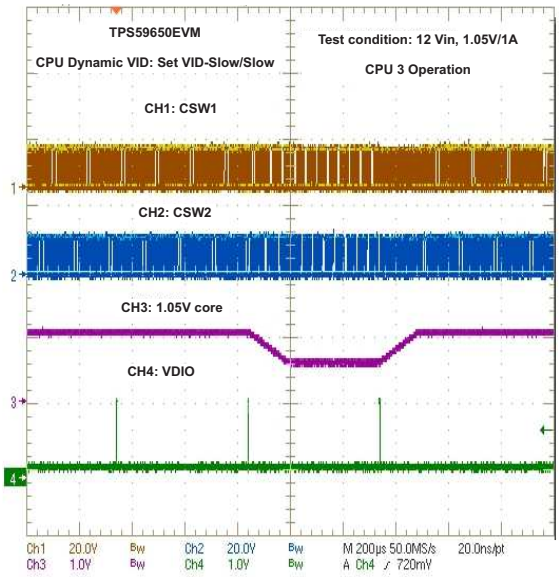


Figure 12. CPU3 Dynamic VID: SetVID-Slow/Slow

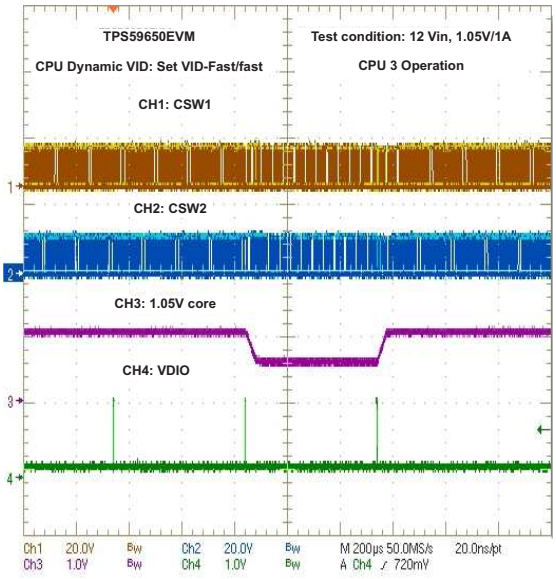


Figure 13. CPU3 Dynamic VID:SetVID-Fast/Fast

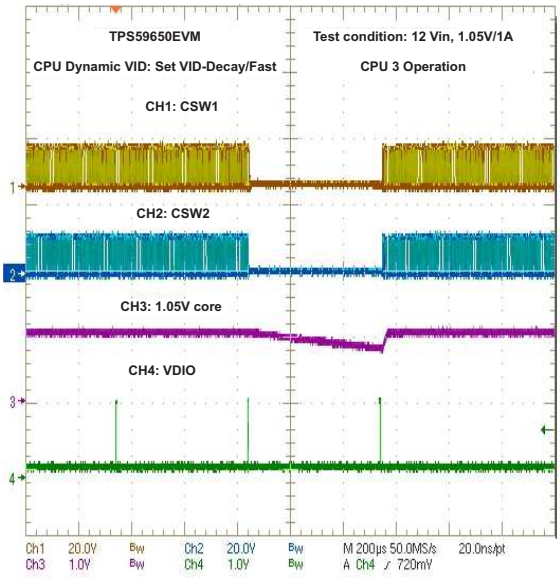


Figure 14. CPU3 Dynamic VID:SetVID-Decay/Fast

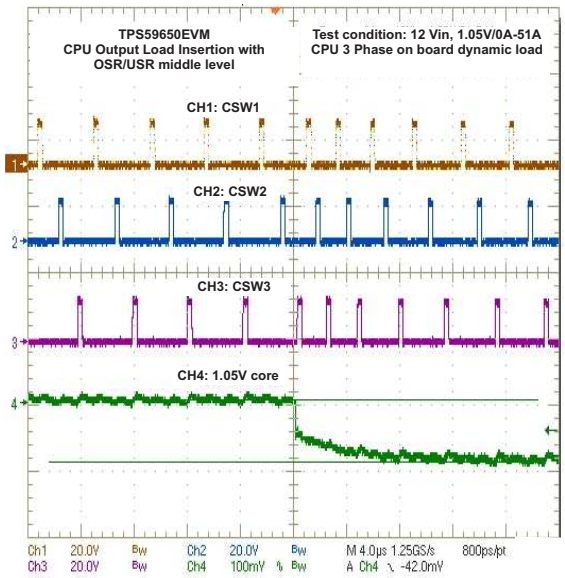


Figure 15. CPU3 Output Load Insertion with OSR/USR middle level

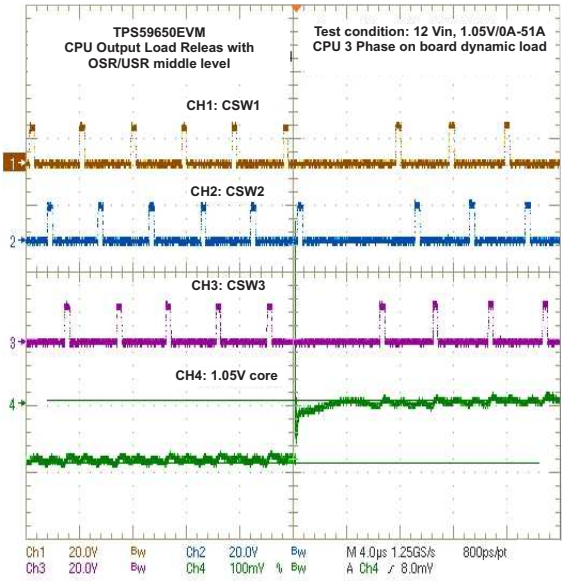


Figure 16. CPU3 Output Load Release with OSR/USR middle level

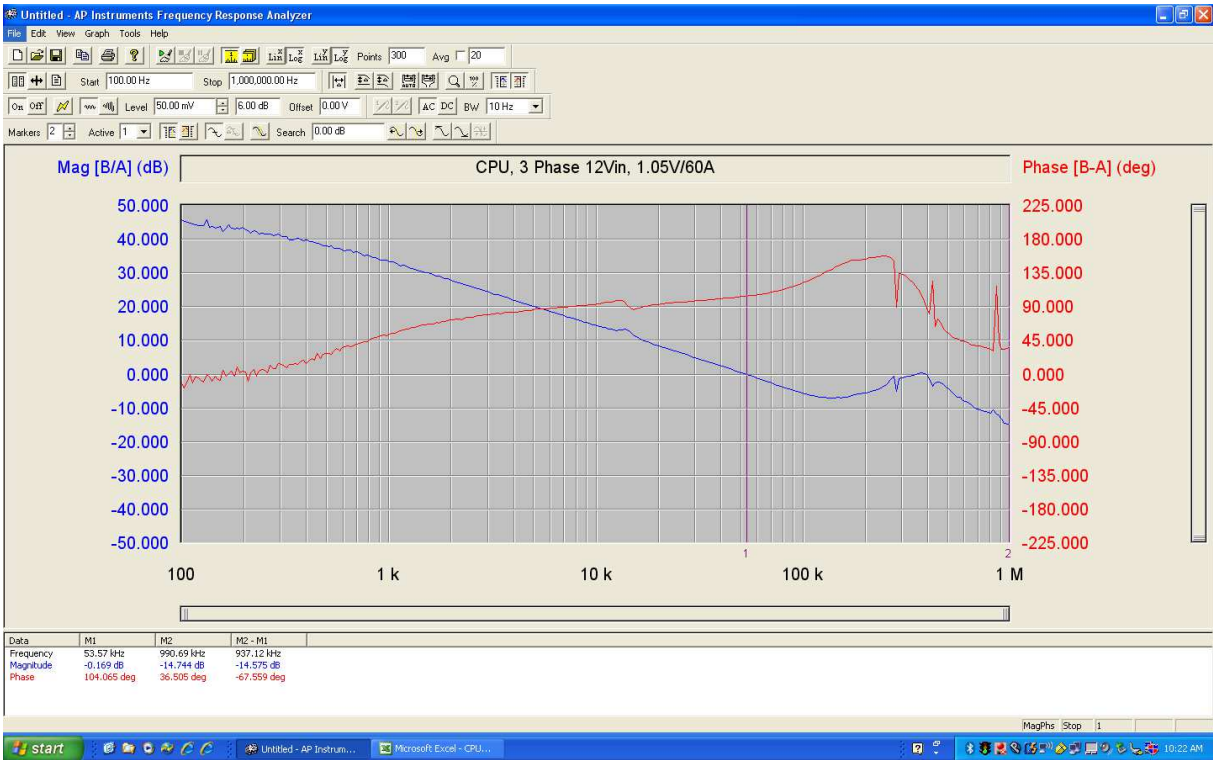


Figure 17. CPU3 Bode Plot at 12Vin, 1.05V/60A

Test condition: CPU3 12Vin, 1.05V/60A no airflow

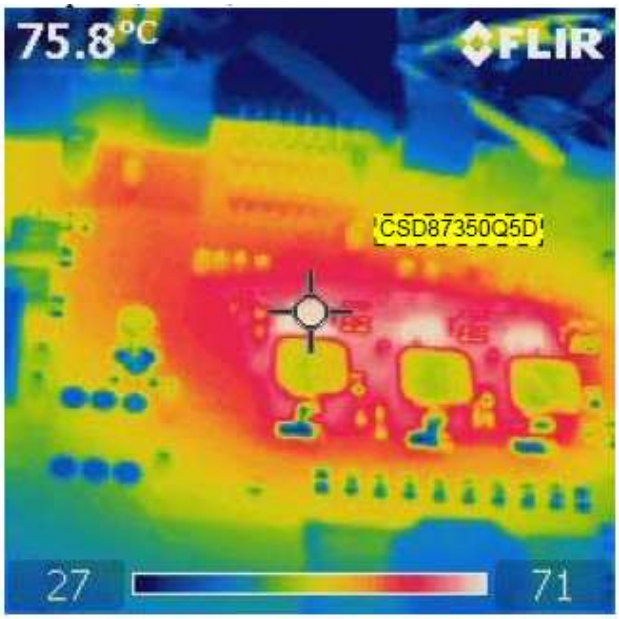


Figure 18. CPU3 MOSFET

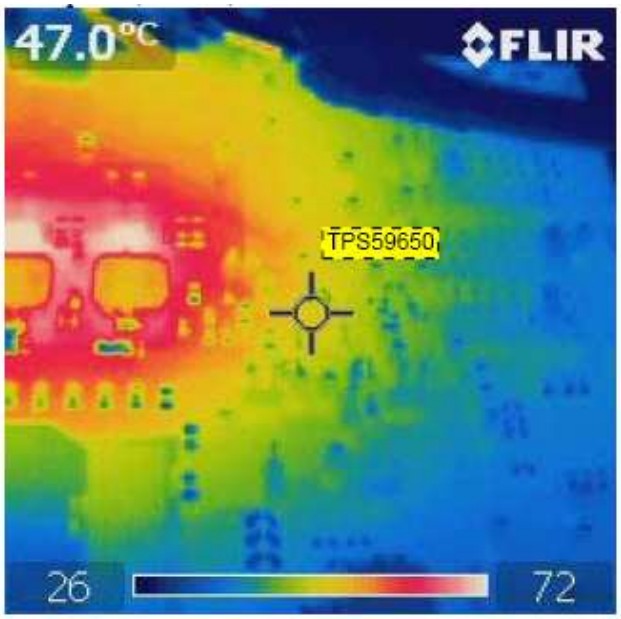


Figure 19. CPU3 IC

7.2 CPU 2-Phase Operation

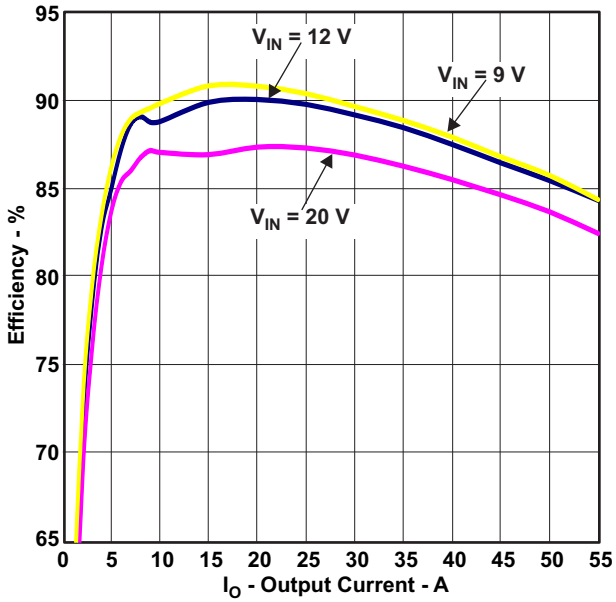


Figure 20. CPU2 Efficiency

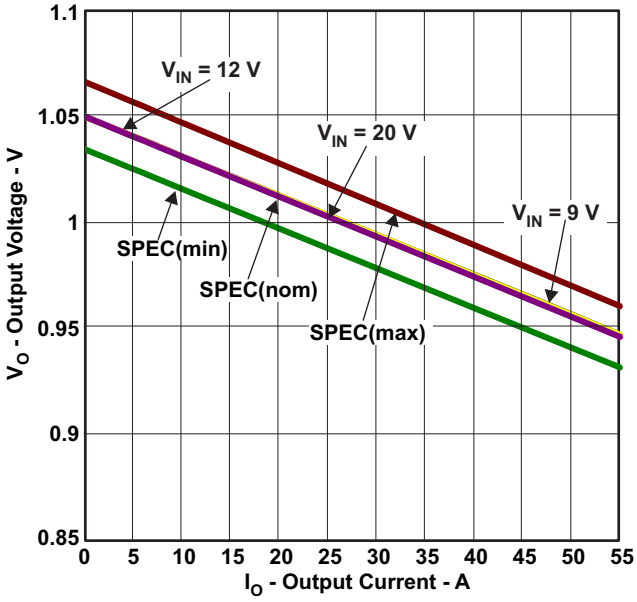


Figure 21. CPU2 Load regulation

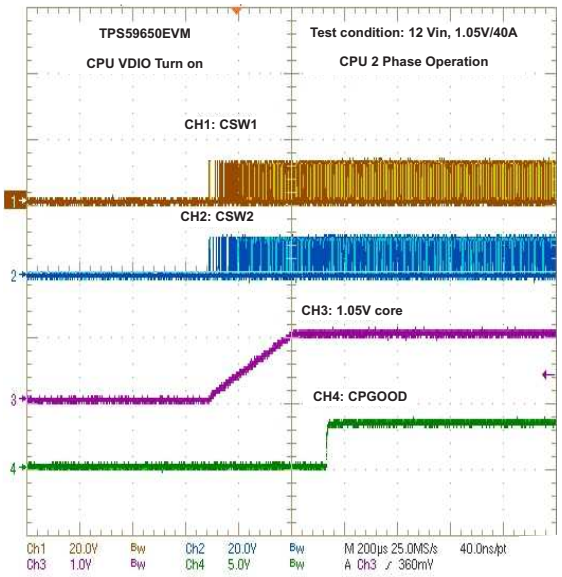


Figure 22. CPU2 Enable Turn on

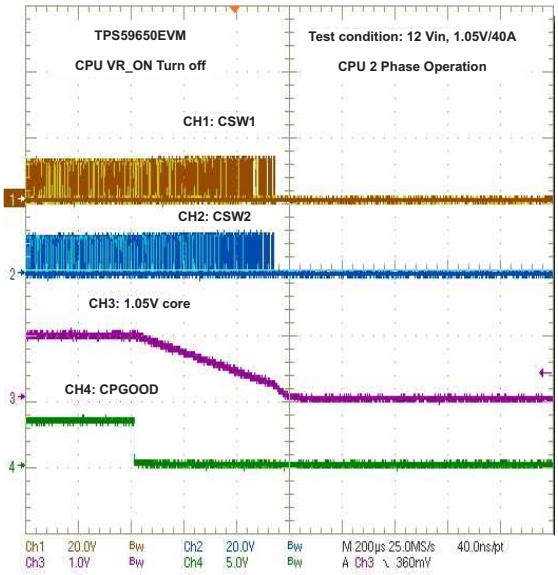


Figure 23. CPU2 Enable Turn off

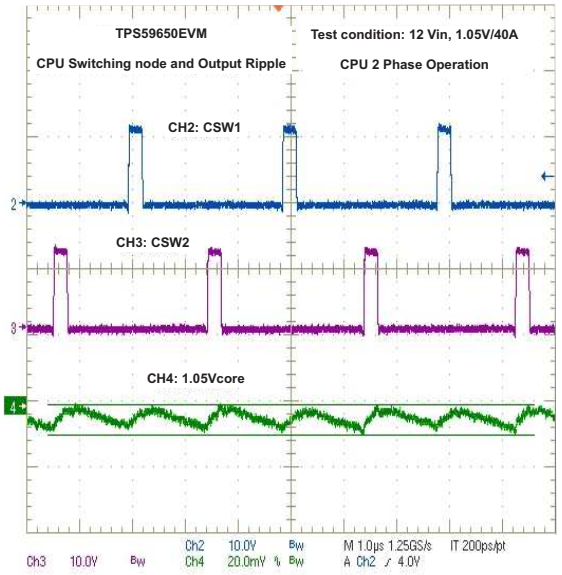


Figure 24. CPU2 Switching Node(Ripple)

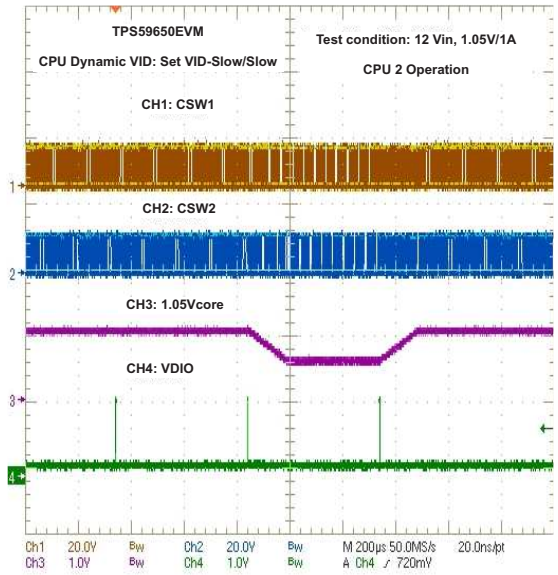


Figure 25. CPU2 Dynamic VID: SetVID-Slow/Slow

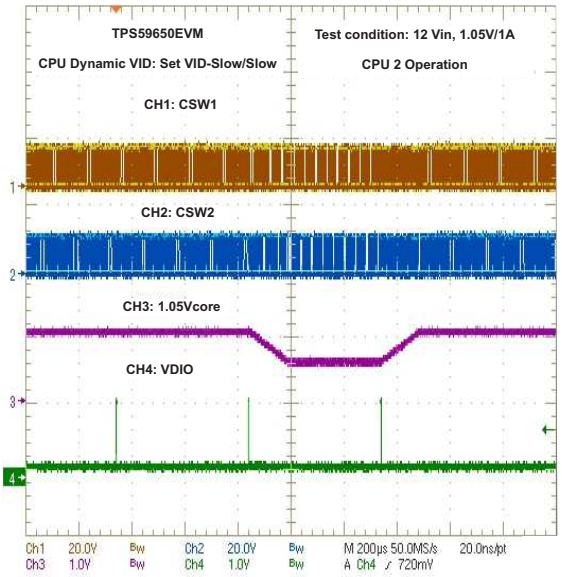


Figure 26. CPU2 Dynamic VID:SetVID-Fast/Fast

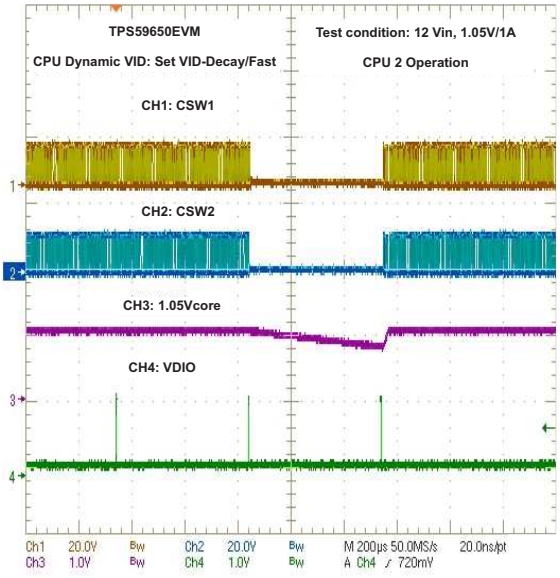


Figure 27. CPU2 Dynamic VID:SetVID-Decay/Fast

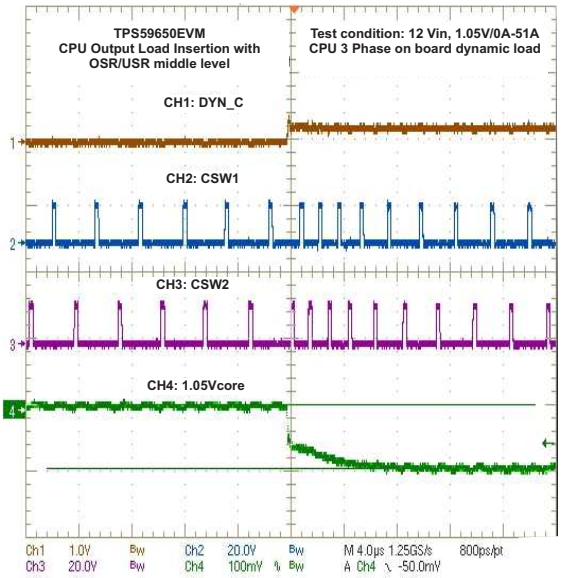


Figure 28. CPU2 Output Load Insertion with OSR/USR middle level

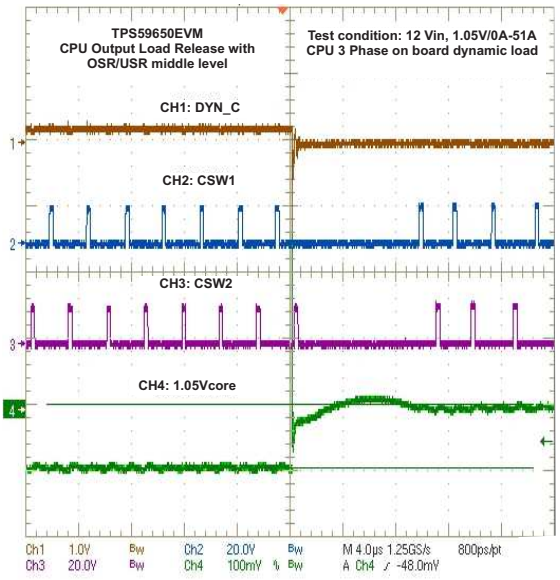


Figure 29. CPU2 Output Load Release with OSR/USR middle level

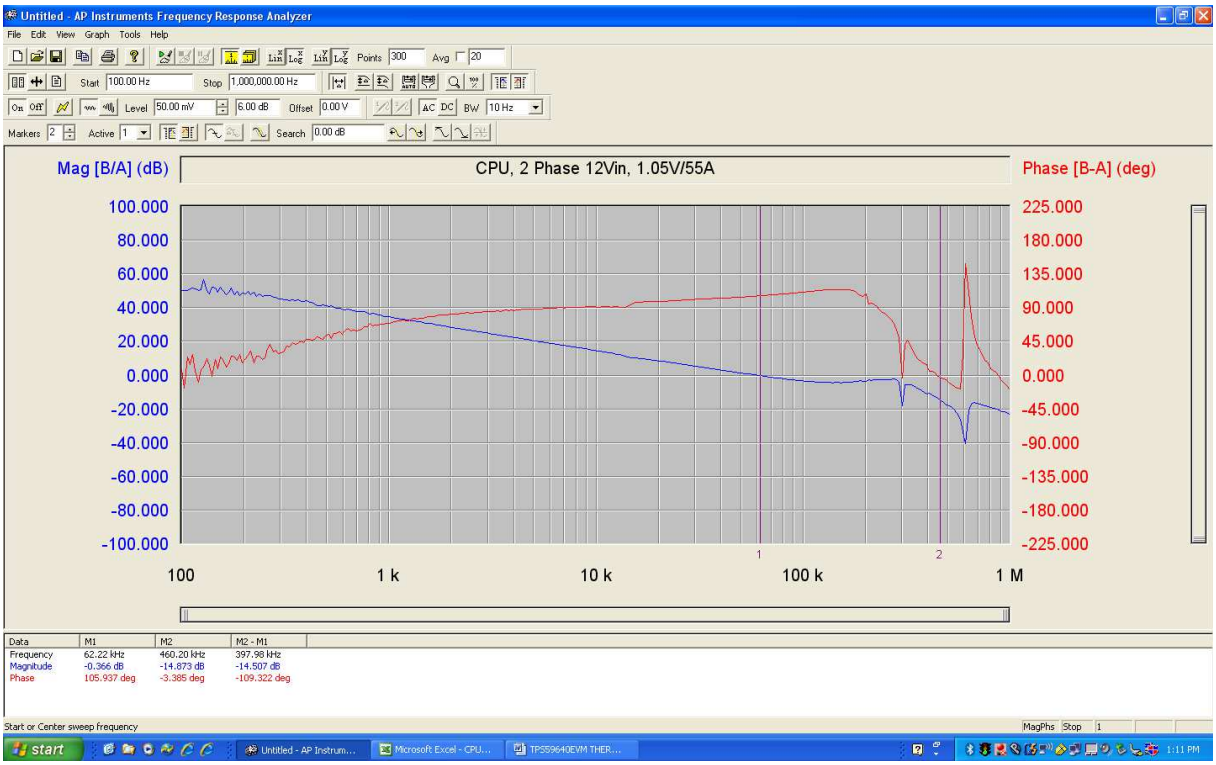


Figure 30. CPU2 Bode Plot at 12Vin, 1.05V/55A

Test condition: CPU2 12Vin, 1.05V/55A no airflow

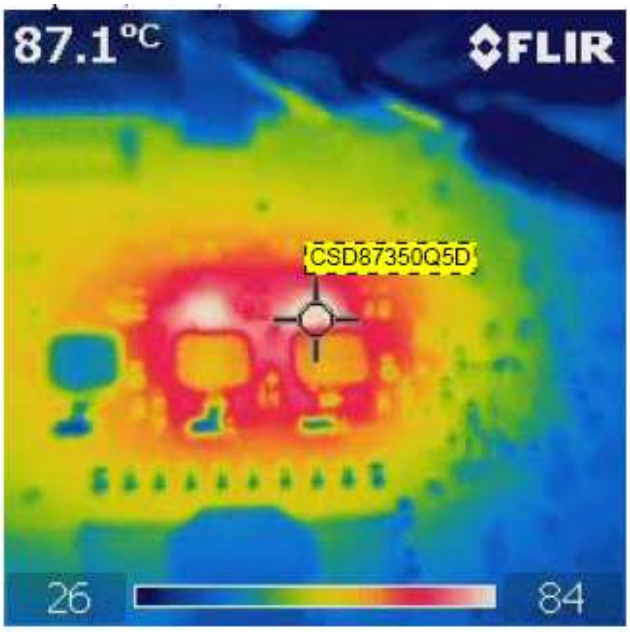


Figure 31. CPU2 MOSFET

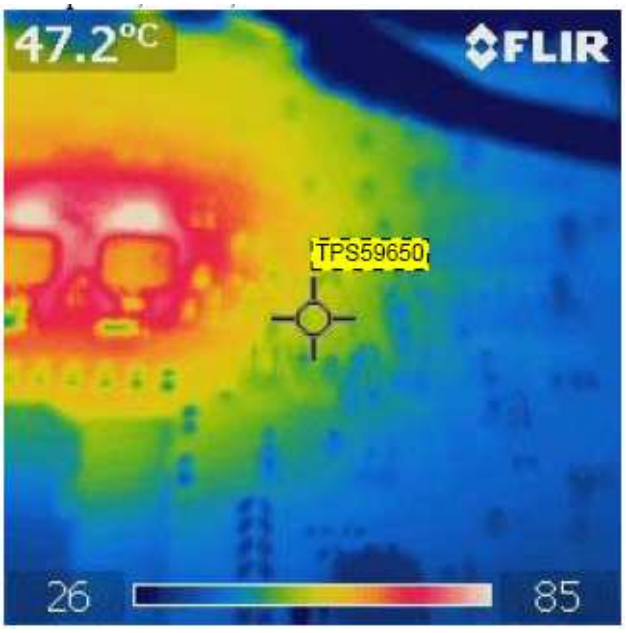


Figure 32. CPU2 IC

7.3 CPU1-Phase Operation

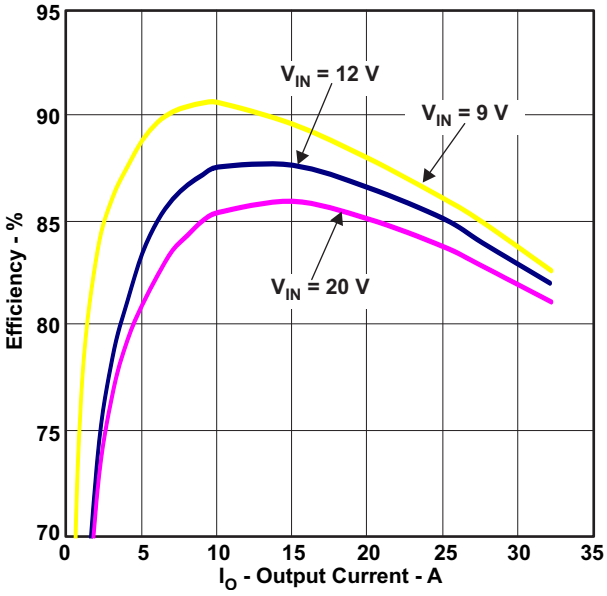


Figure 33. CPU1 Efficiency

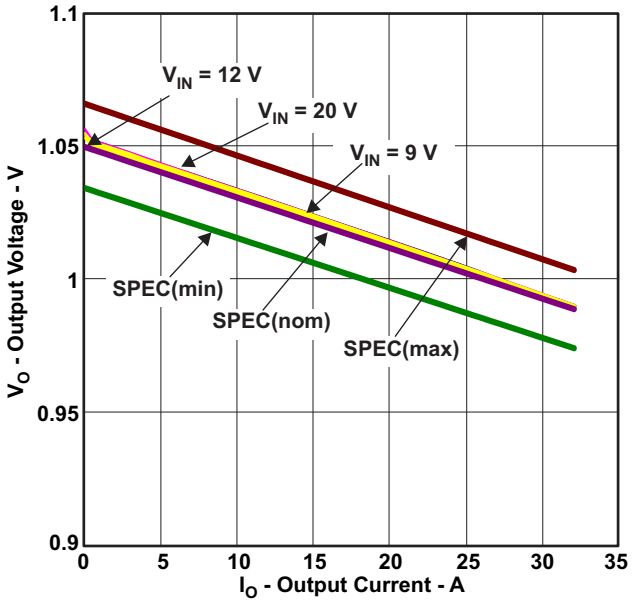


Figure 34. CPU1 Load regulation

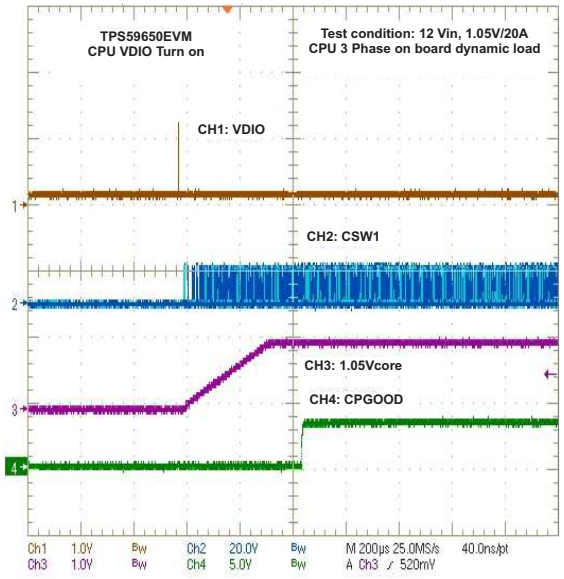


Figure 35. CPU1 Enable Turn on

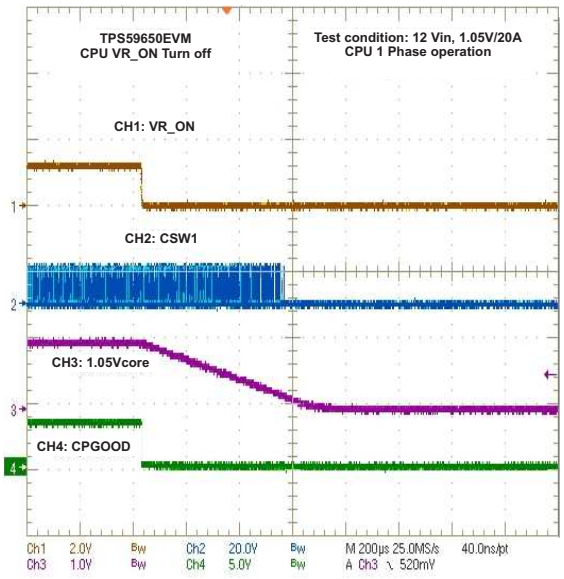


Figure 36. CPU1 Enable Turn off

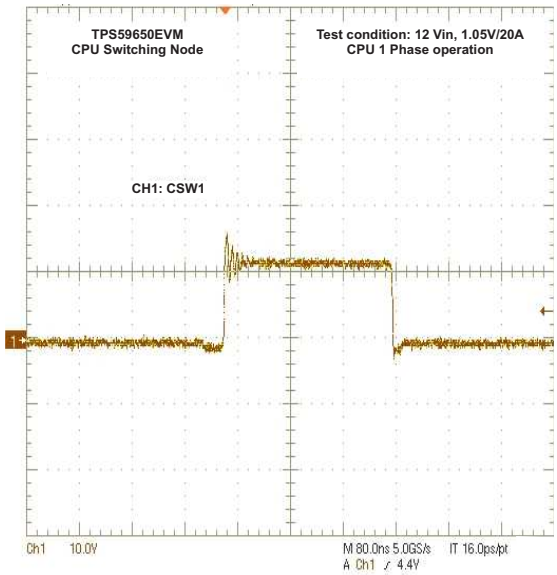


Figure 37. CPU1 Switching Node

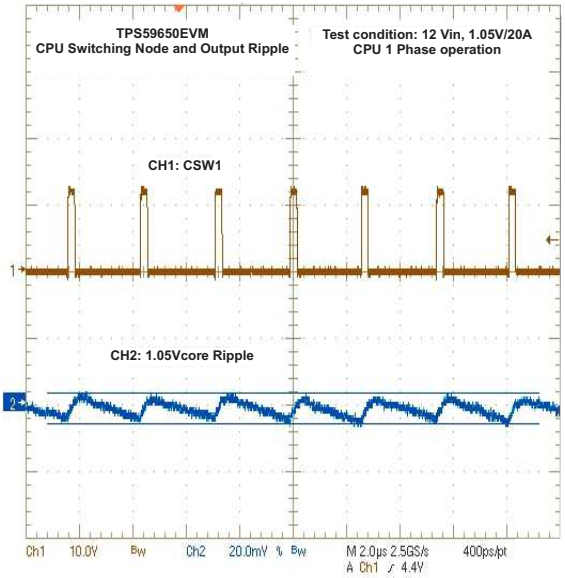


Figure 38. CPU1 Switching node and Ripple

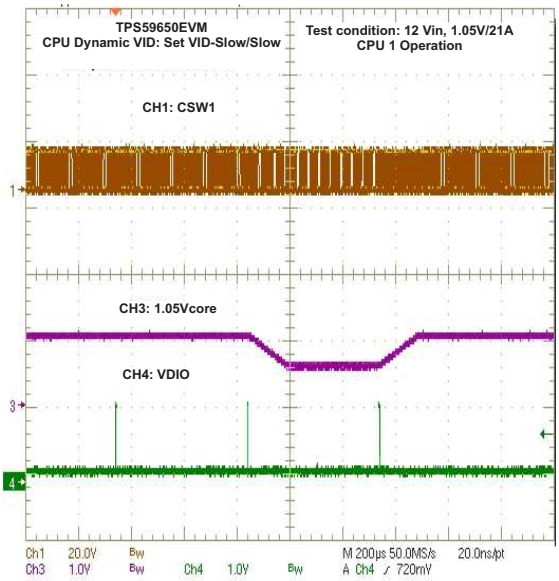


Figure 39. CPU1 Dynamic VID:SetVID-Slow/Slow

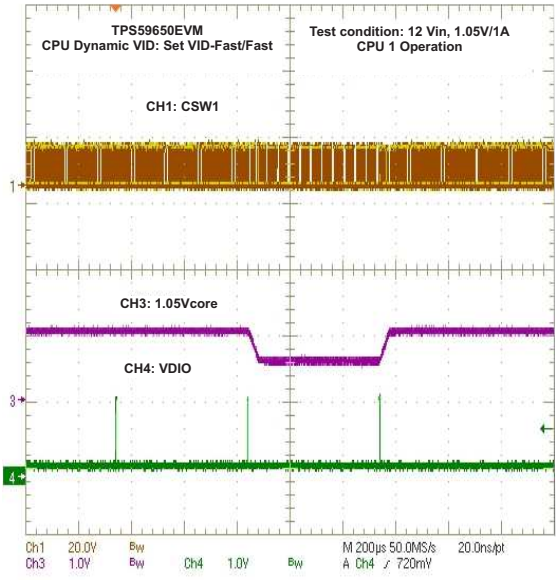


Figure 40. CPU1 Dynamic VID:SetVID-Fast/Fast

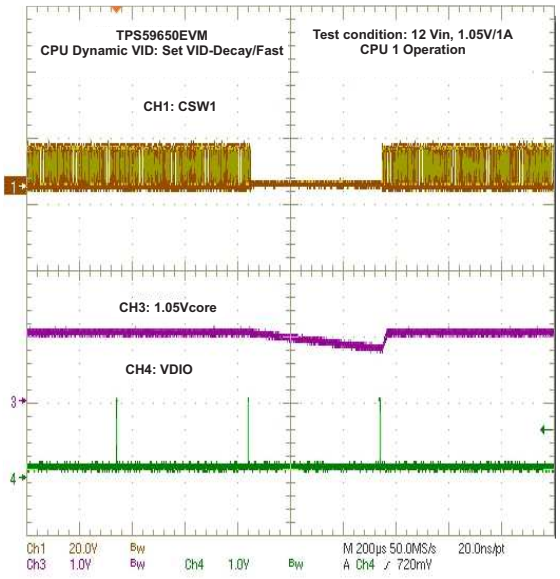


Figure 41. CPU1 Dynamic VID:SetVID-Decay/Fast

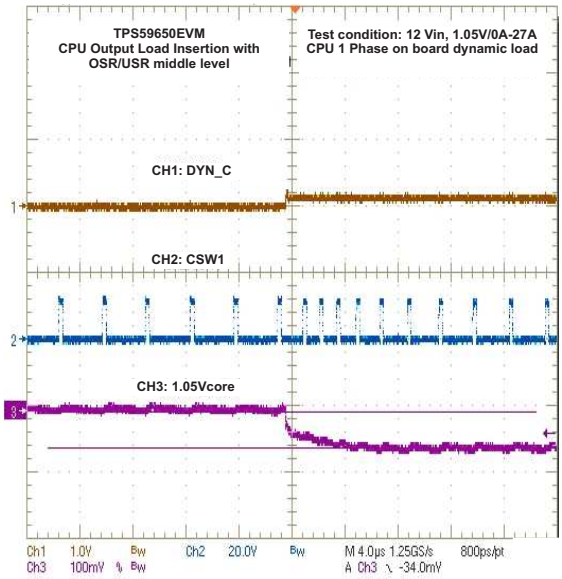


Figure 42. CPU1 Output Load Insertion with OSR/USR middle level

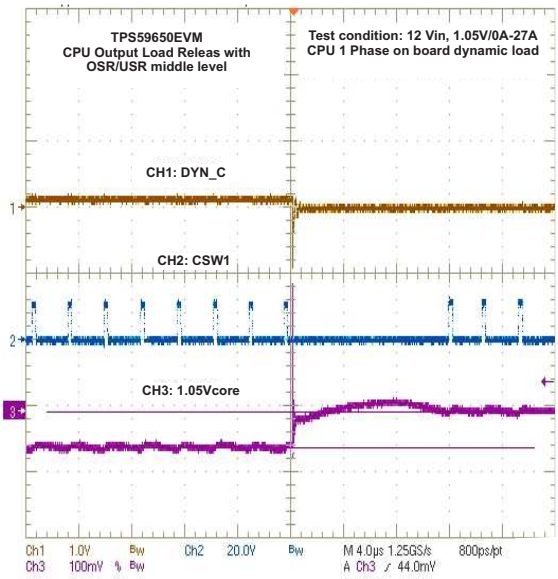


Figure 43. CPU1 Output Load Release with OSR/USR middle level

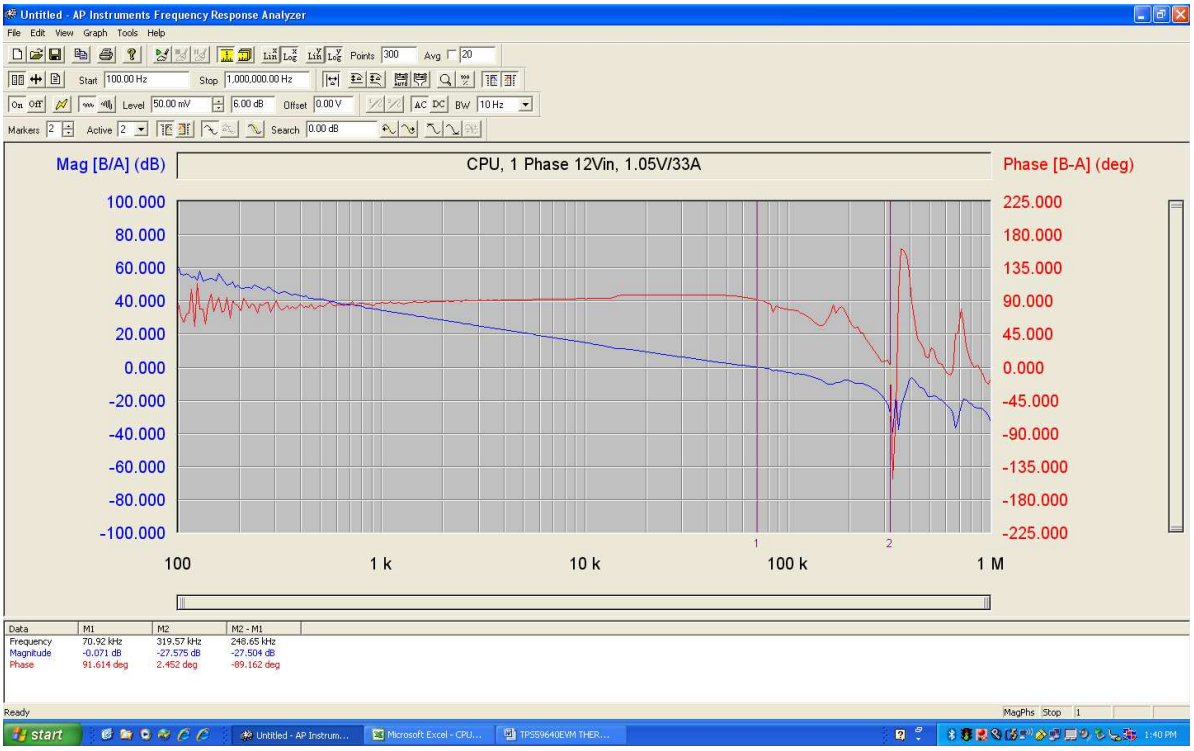


Figure 44. CPU1 Bode Plot at 12Vin, 1.05V/33A

Test condition: CPU1 12Vin, 1.05V/33A no airflow

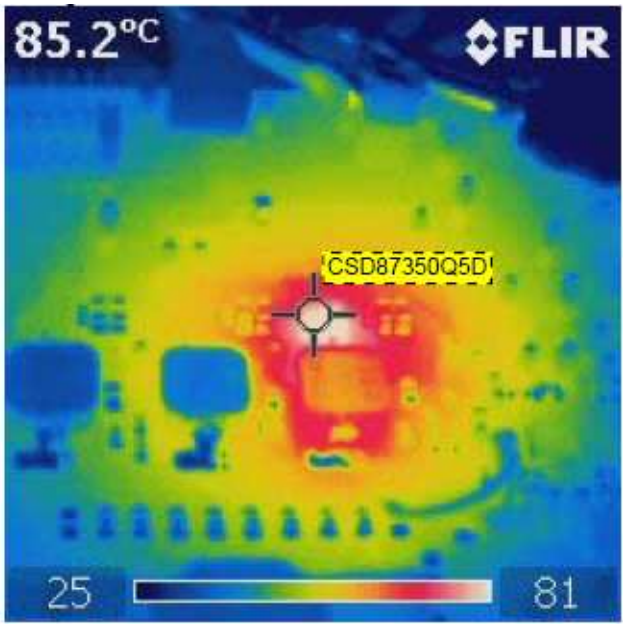


Figure 45. CPU1 MOSFET

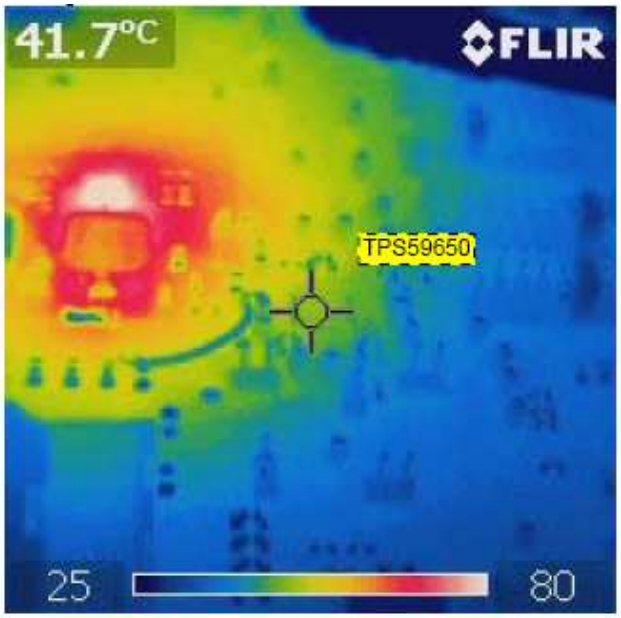


Figure 46. CPU1 IC

7.4 GPU 2 Phase Operation

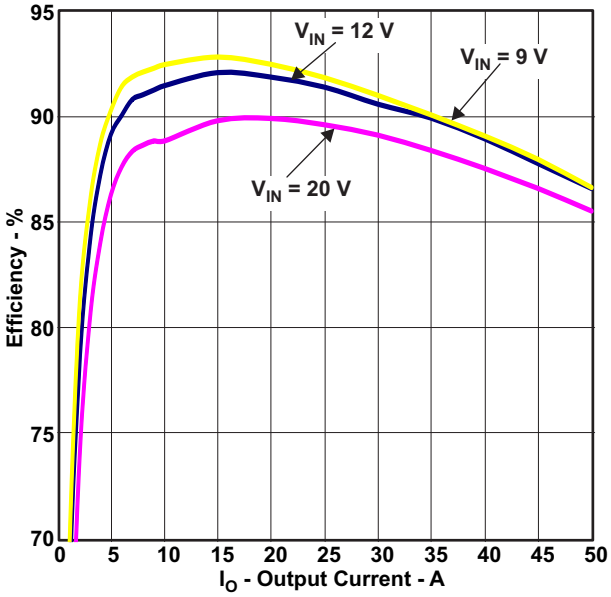


Figure 47. GPU2 Efficiency

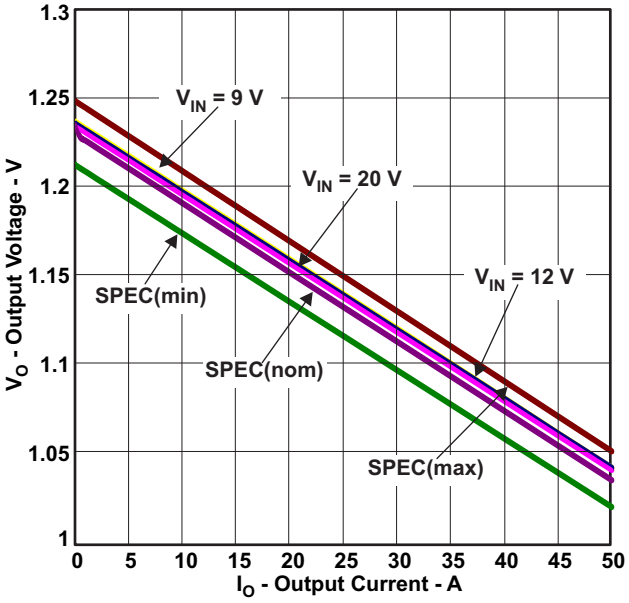


Figure 48. GPU2 Load regulation

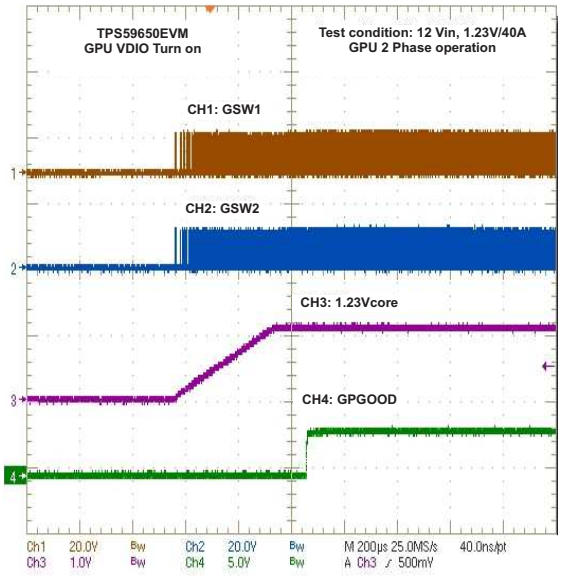


Figure 49. GPU2 Enable Turn on

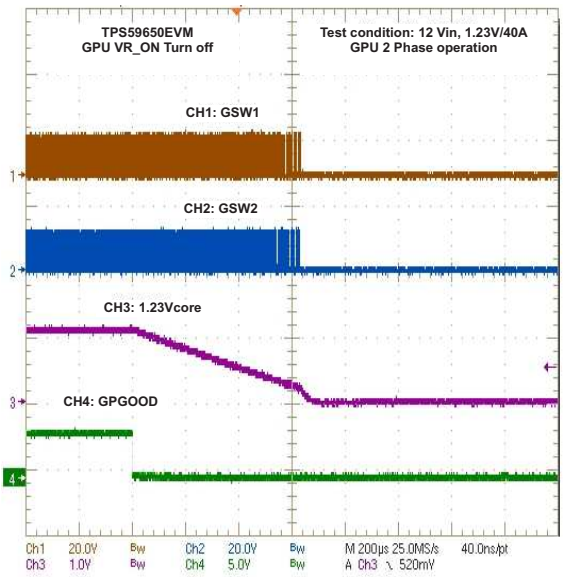


Figure 50. GPU2 Enable Turn off

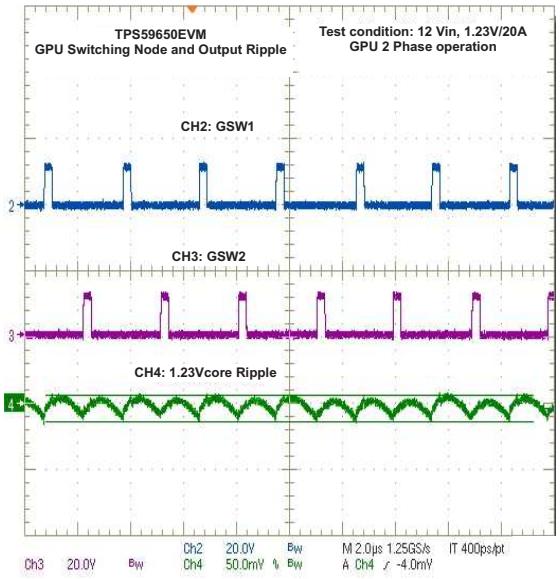


Figure 51. GPU2 Switching Node and Ripple

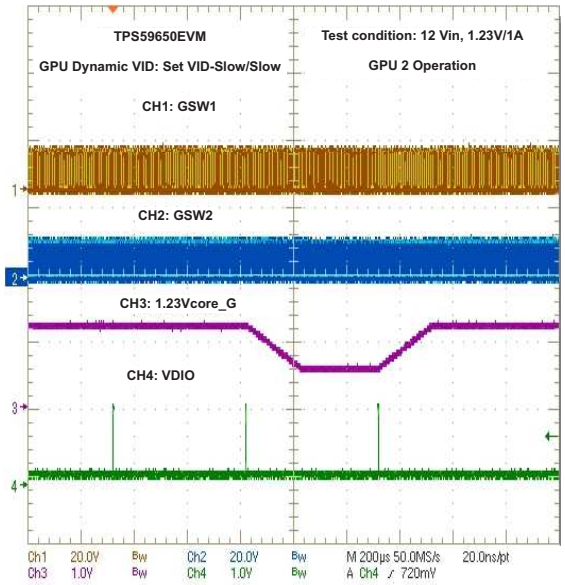


Figure 52. GPU2 Dynamic VID:SetVID-Slow/Slow

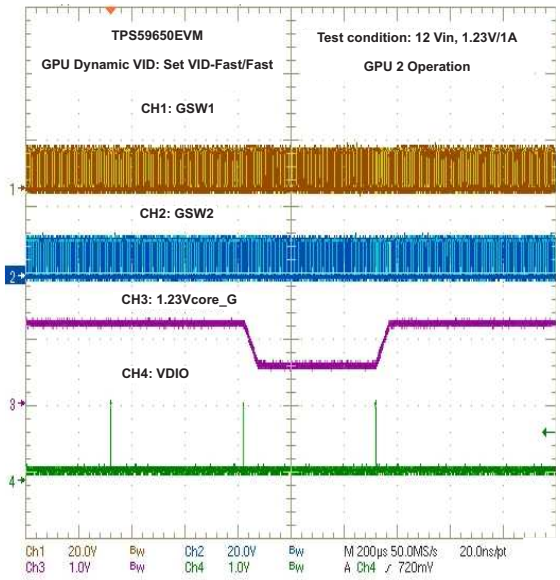


Figure 53. GPU2 Dynamic VID:SetVID-Fast/Fast

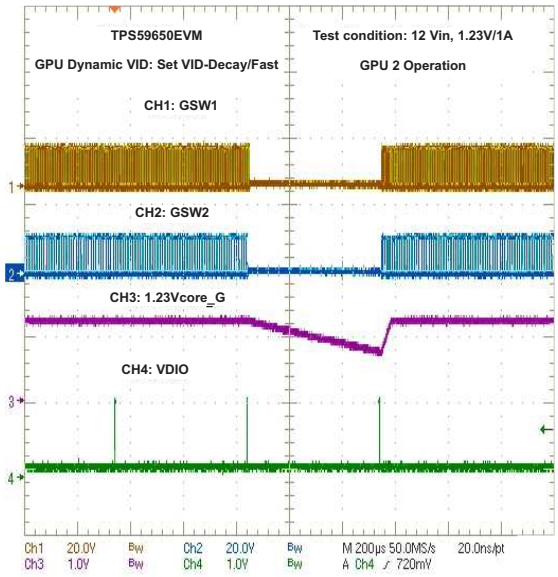


Figure 54. GPU2 Dynamic VID:SetVID-Decay/Fast

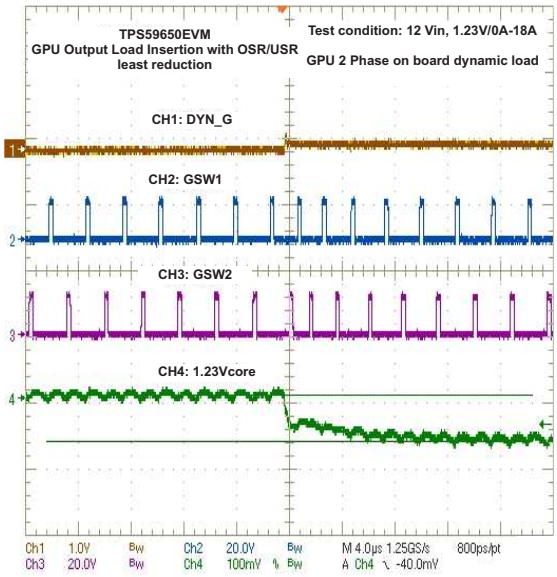


Figure 55. GPU2 Output Load Insertion with OSR/USR OFF

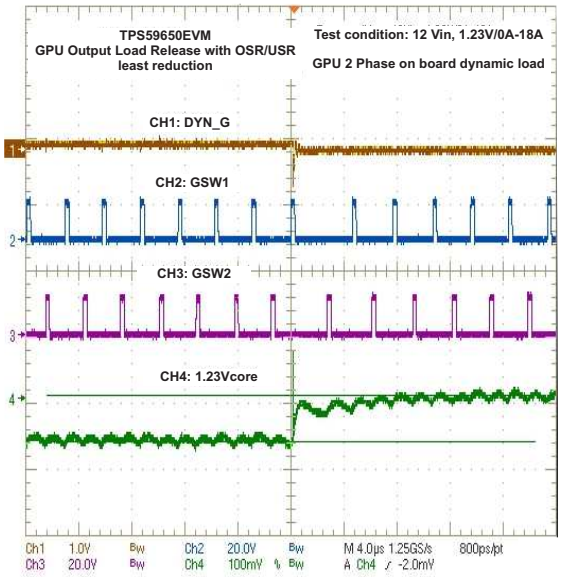


Figure 56. GPU2 Output Load Release with OSR/USR OFF

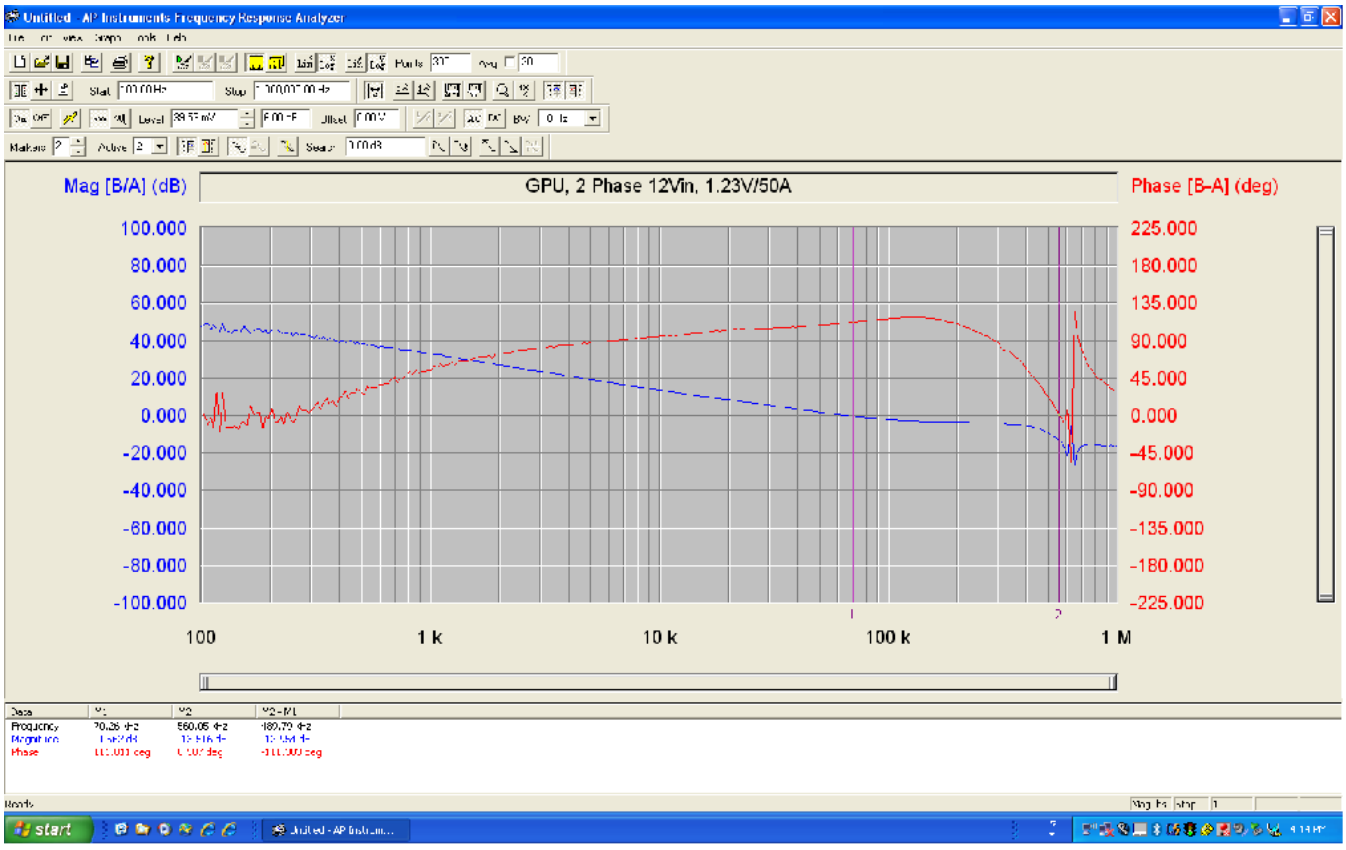


Figure 57. GPU2 Bode Plot at 12Vin, 1.23V/50A

Test condition: GPU2 12Vin, 1.23V/50A no airflow

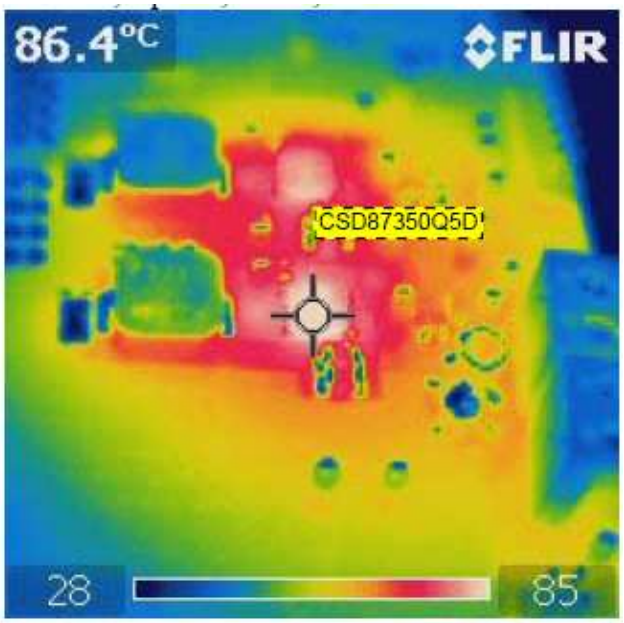


Figure 58. GPU2 MOSFET

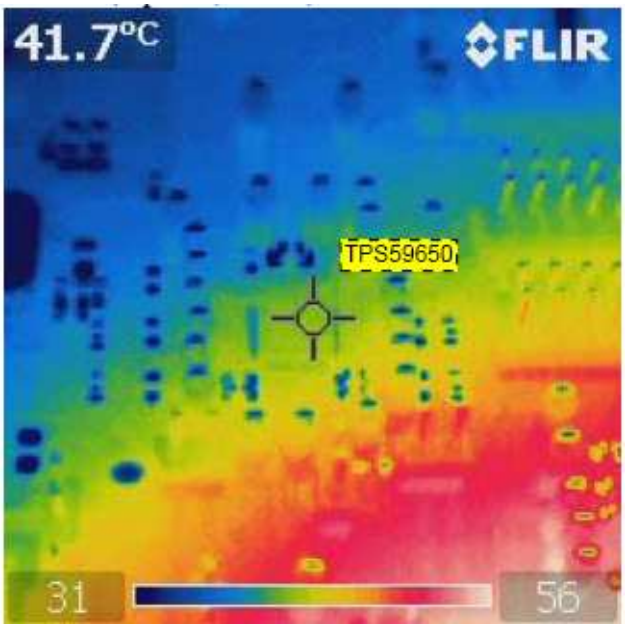


Figure 59. GPU2 IC

7.5 GPU 1 Phase Operation

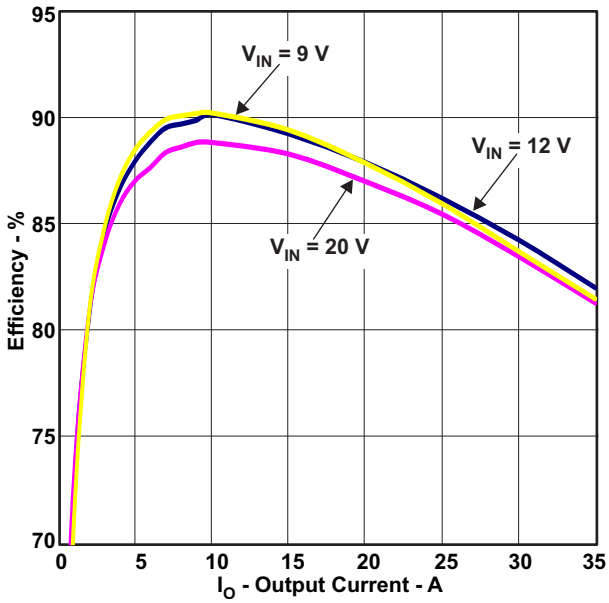


Figure 60. GPU1 Efficiency

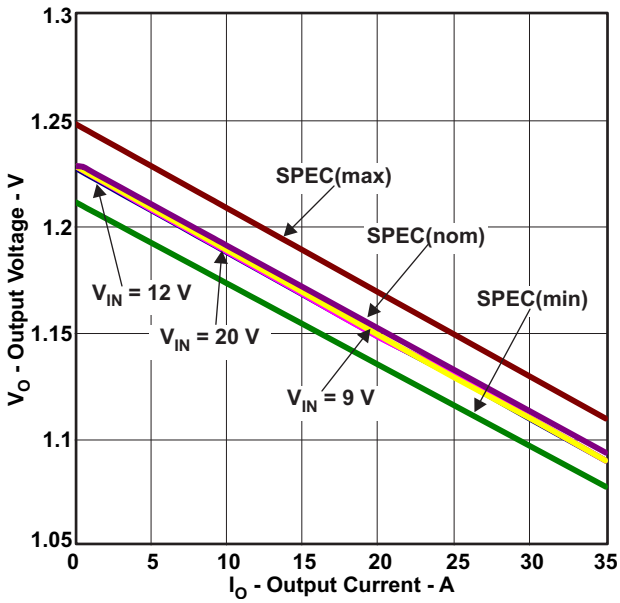


Figure 61. GPU1 Load regulation

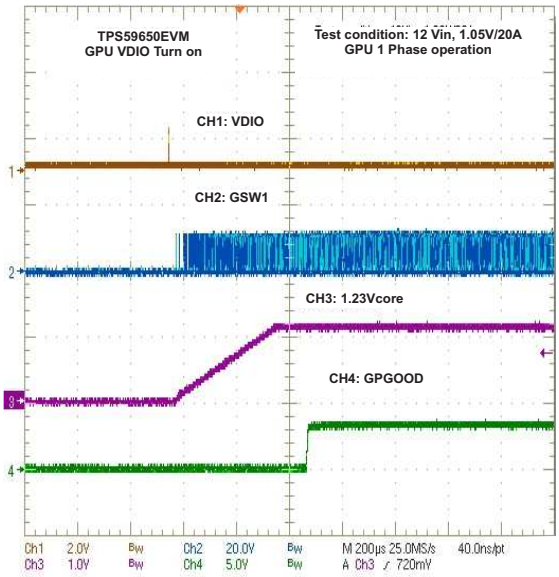


Figure 62. GPU1 Enable Turn on

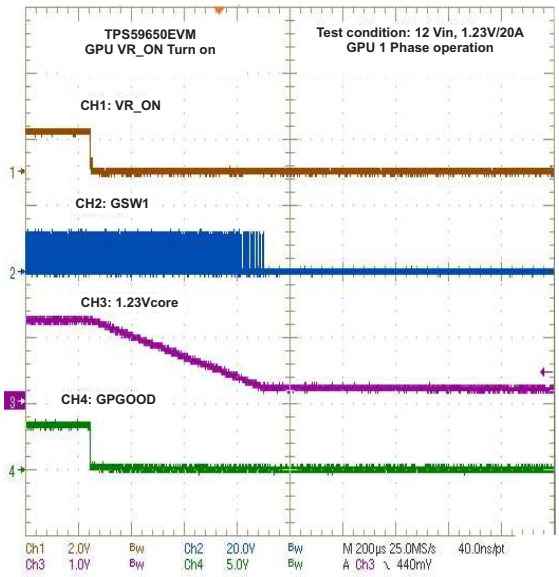


Figure 63. GPU1 Enable Turn off

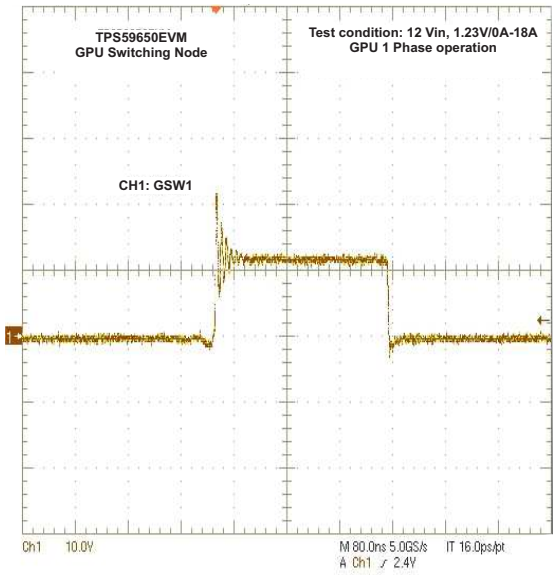


Figure 64. GPU1 Switching Node

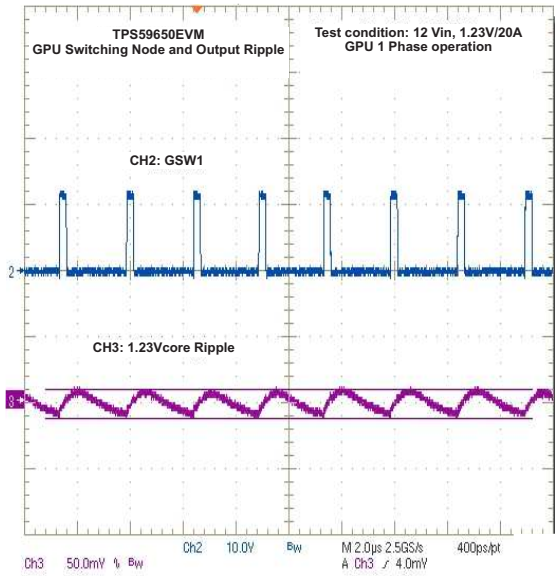


Figure 65. GPU1 Switching Node and Ripple

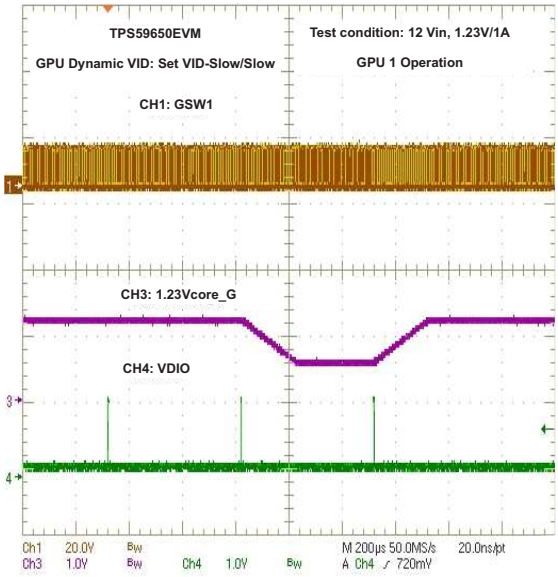


Figure 66. GPU1 Dynamic VID:SetVID-Slow/Slow

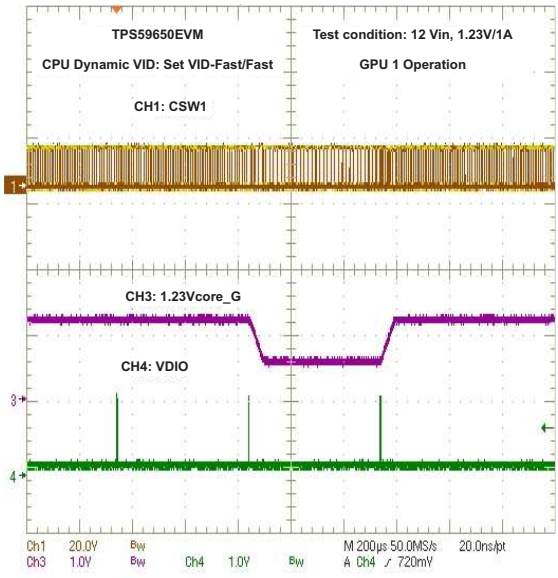


Figure 67. GPU1 Dynamic VID:SetVID-Fast/Fast

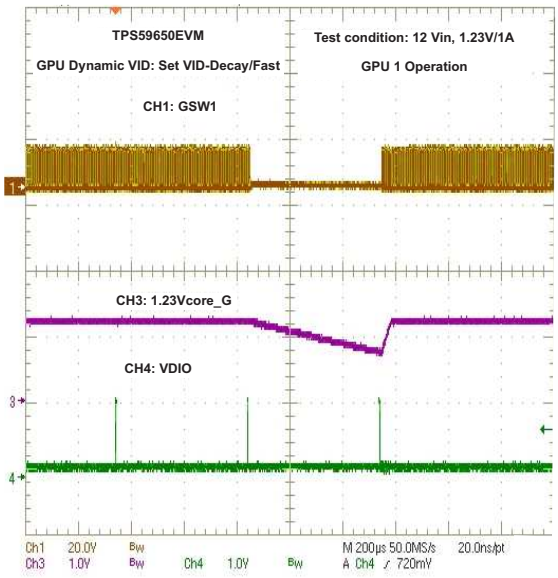


Figure 68. GPU1 Dynamic VID:SetVID-Decay/Fast

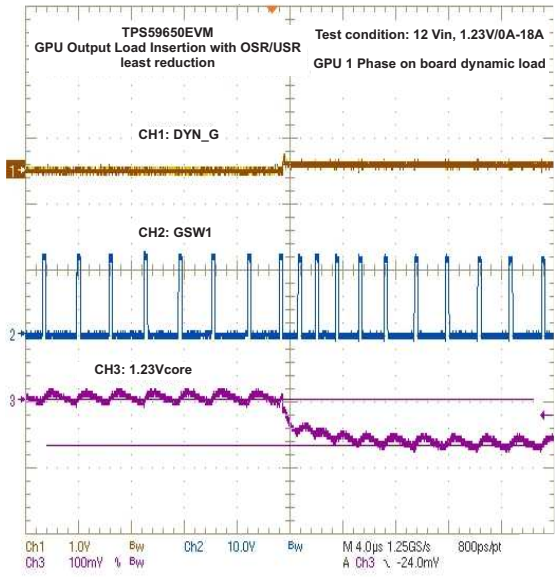


Figure 69. GPU1 Output Load Insertion with OSR/USR OFF

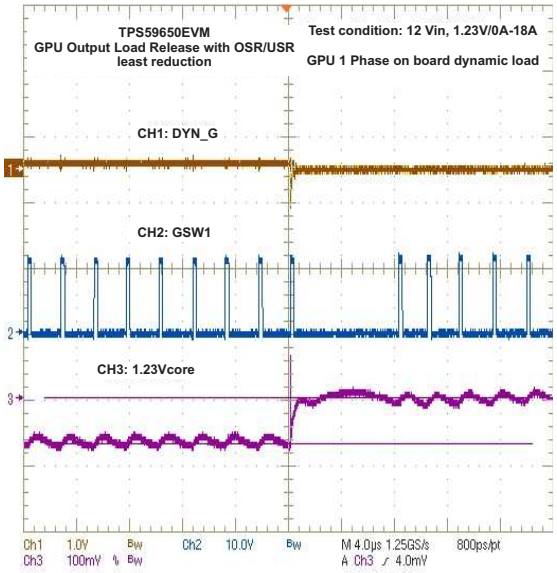


Figure 70. GPU1 Output Load Release with OSR/USR OFF

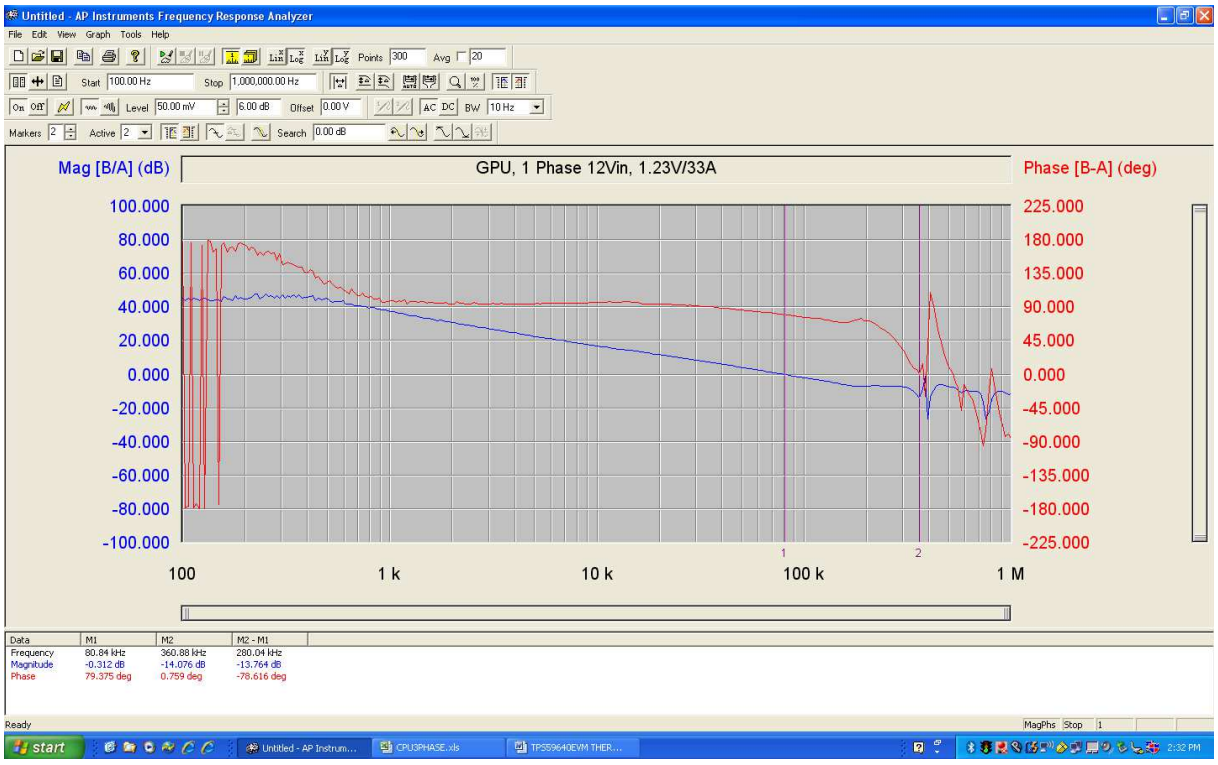


Figure 71. GPU1 Bode Plot at 12Vin, 1.23V/33A

Test condition: GPU1 12Vin, 1.23V/33A no airflow

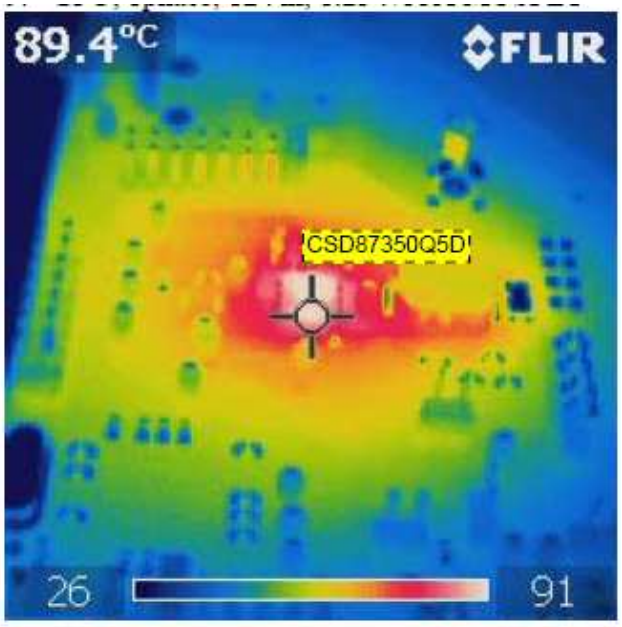


Figure 72. GPU1 MOSFET

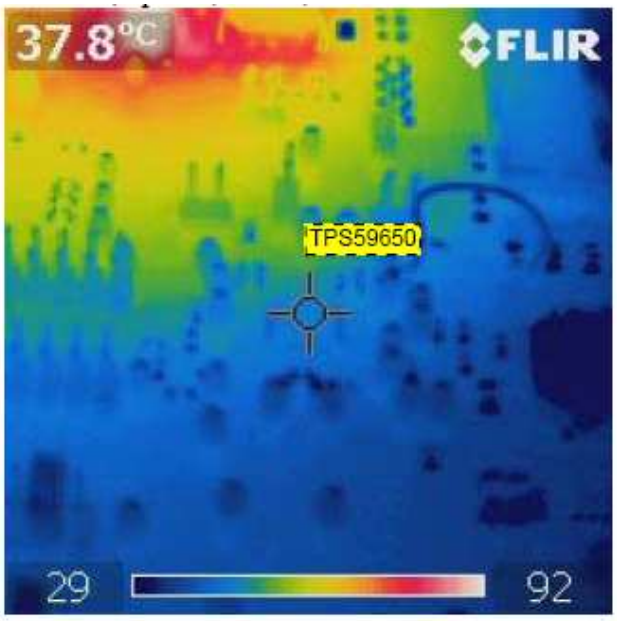


Figure 73. GPU1 IC

7.6 1.05V VCCIO

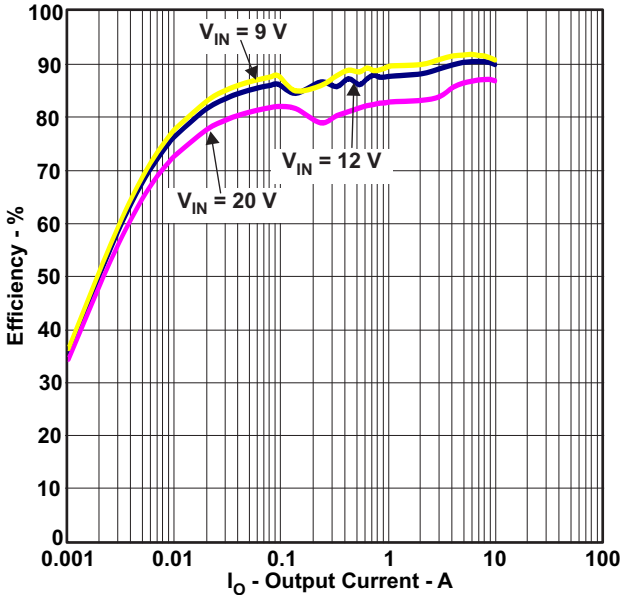


Figure 74. 1.05V Efficiency

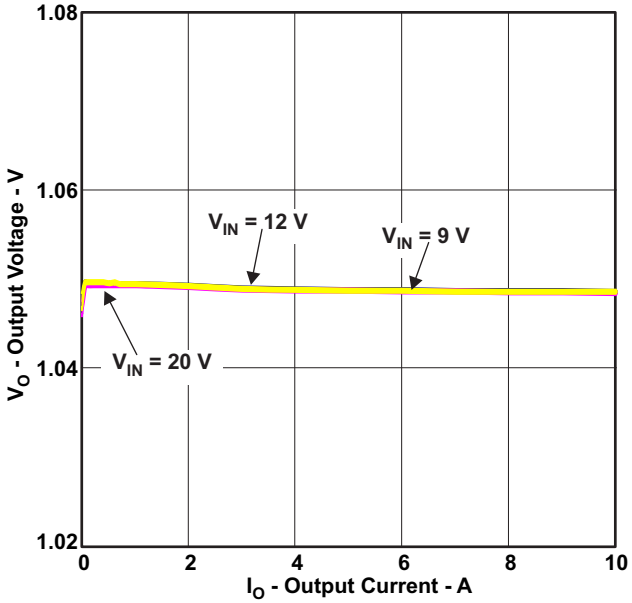


Figure 75. 1.05V Load regulation

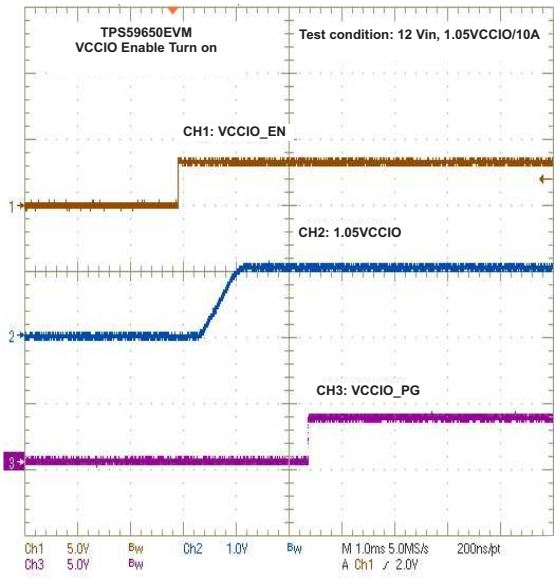


Figure 76. 1.05V Enable Turn on

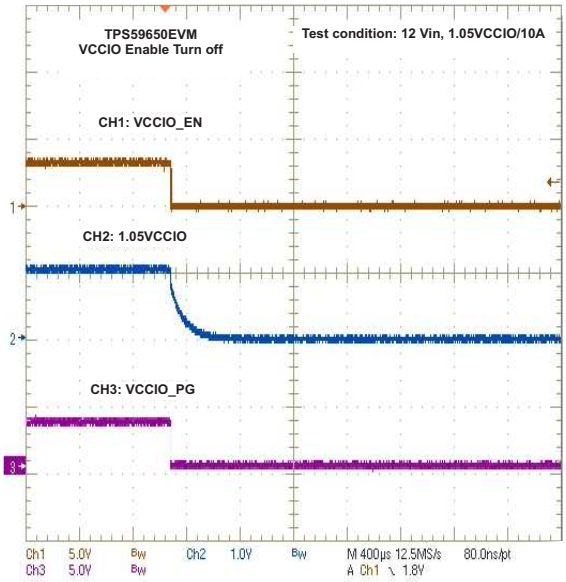


Figure 77. 1.05V Enable Turn off

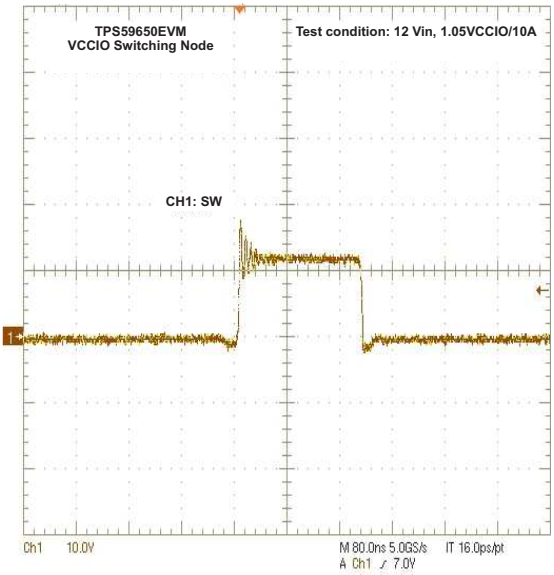


Figure 78. 1.05V Switching Node

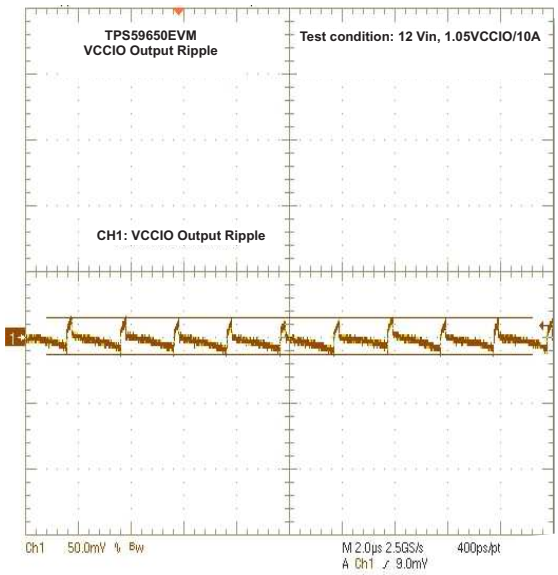


Figure 79. 1.05V Ripple

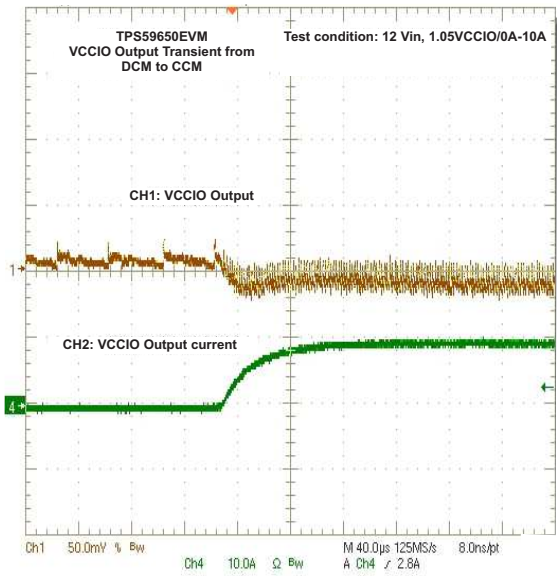


Figure 80. 1.05V Transient DCM TO CCM

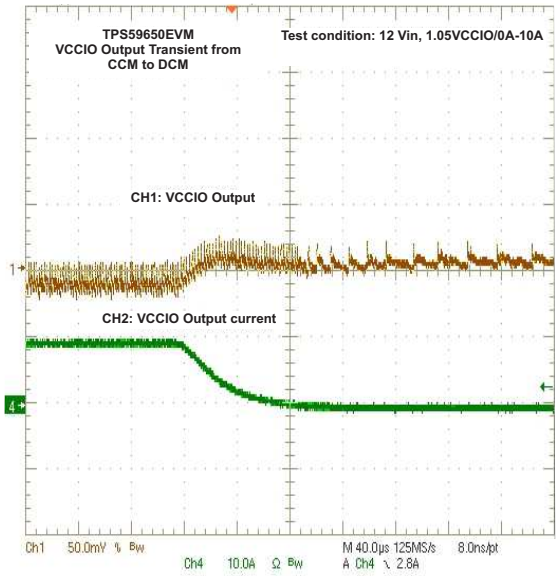


Figure 81. 1.05V Transient CCM to DCM

Test condition: 12Vin, 1.05V/10A no airflow

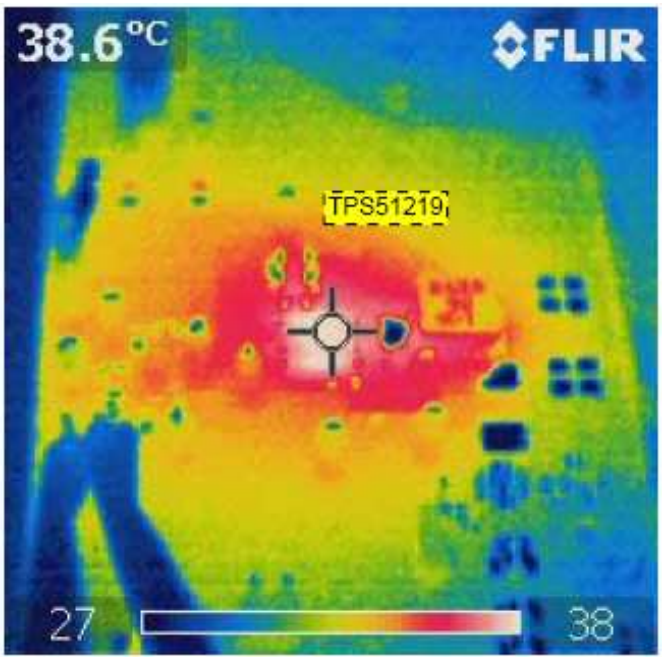


Figure 82. TPS51219 Thermal

7.7 1.2V VDDQ

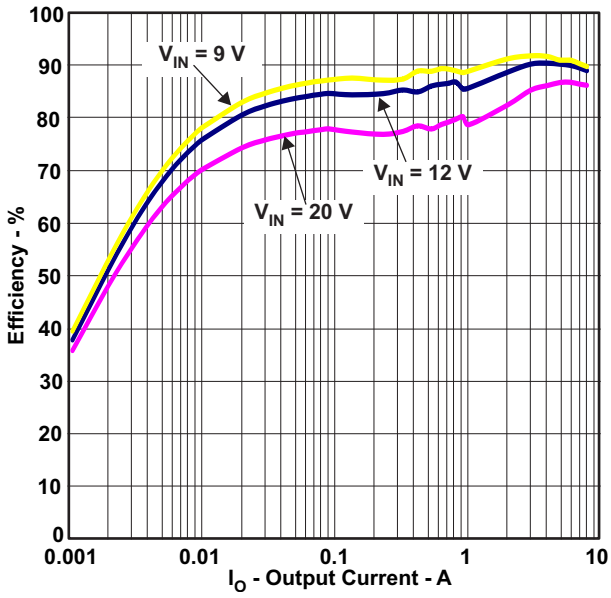


Figure 83. 1.2V Efficiency

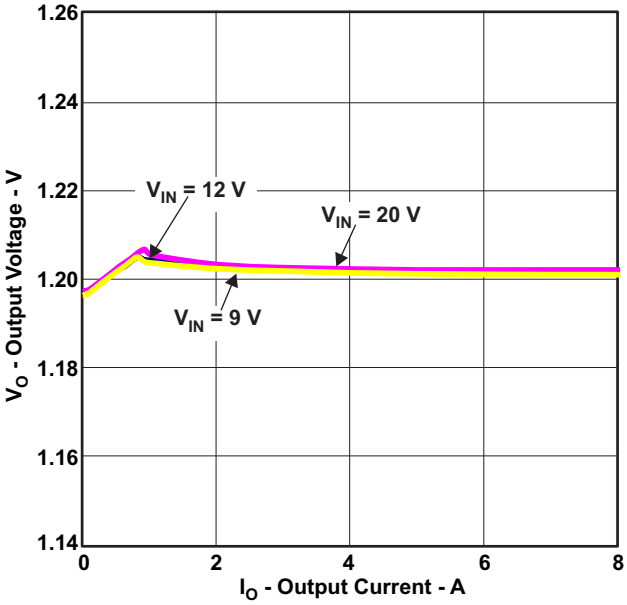


Figure 84. 1.2V Load regulation

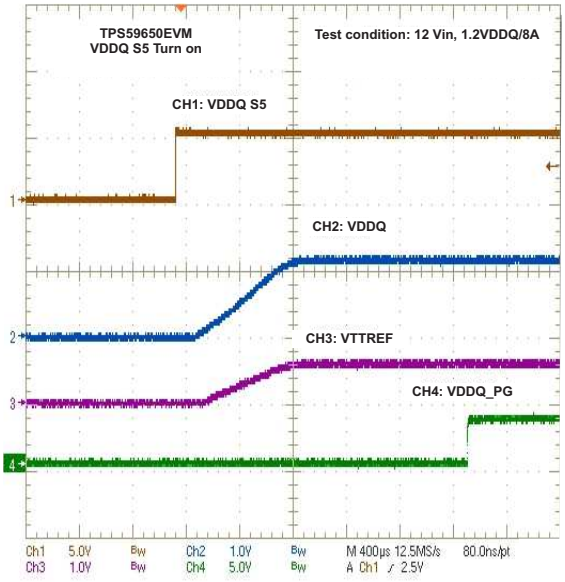


Figure 85. 1.2V Enable Turn on

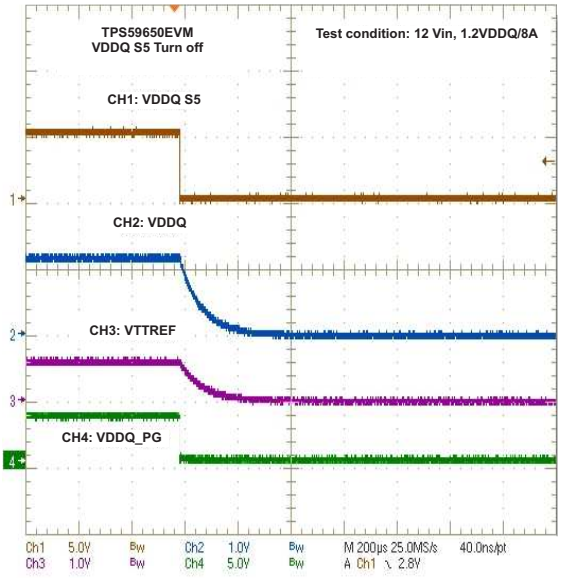


Figure 86. 1.2V Enable Turn off

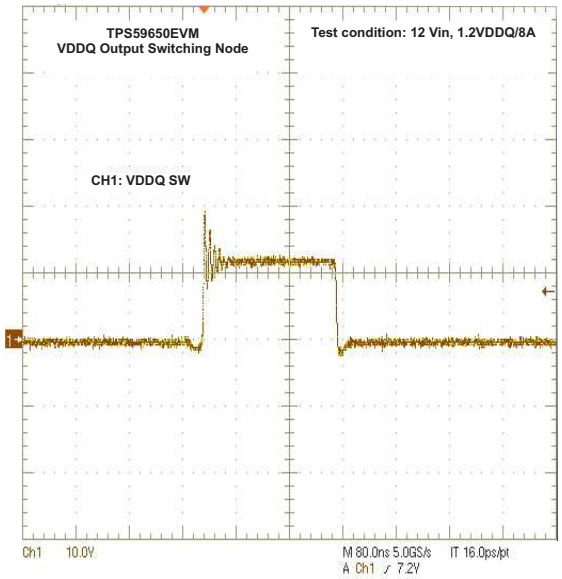


Figure 87. 1.2V Switching Node

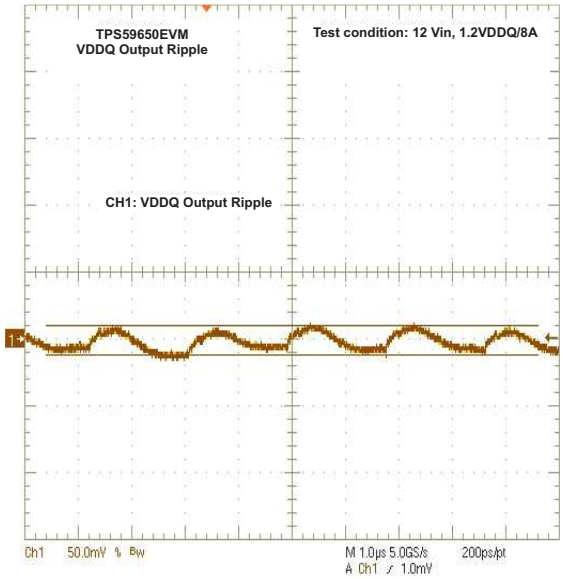


Figure 88. 1.2V Ripple

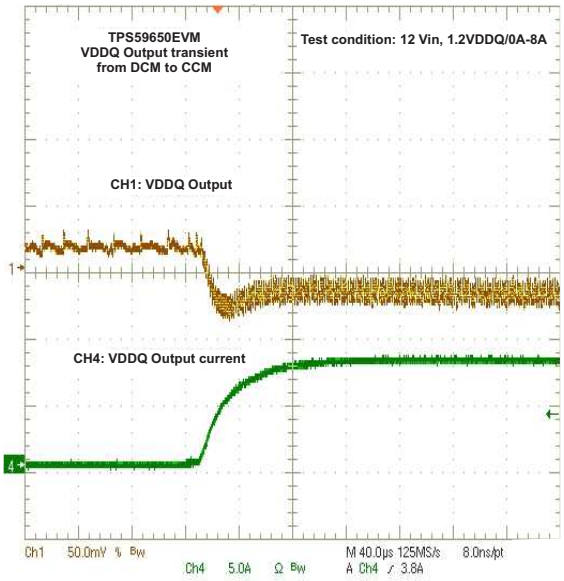


Figure 89. 1.2V Transient DCM TO CCM

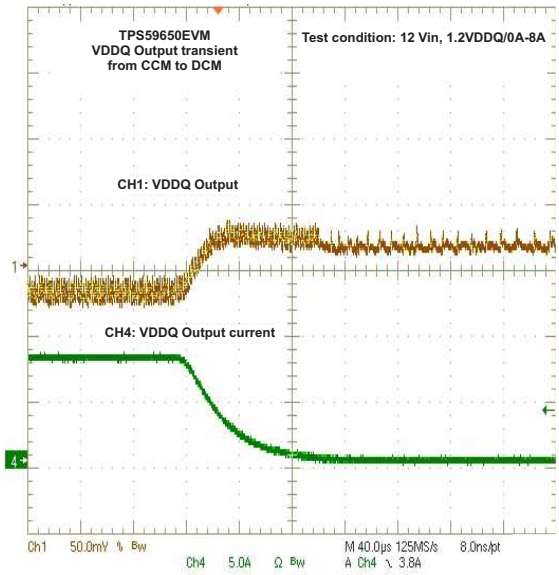


Figure 90. 1.2V Transient CCM to DCM

Test condition: 12Vin, 1.2V/7.5A no airflow

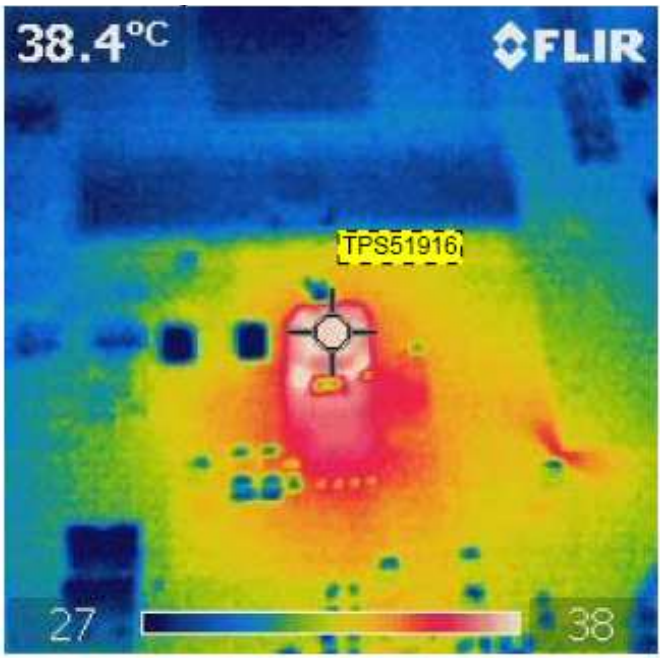


Figure 91. TPS51916 Thermal

8 EVM Assembly Drawings and PCB Layout

The following figures (Figure 92 through Figure 101) show the design of the TPS59650EVM-753 printed circuit board. The EVM has been designed using 8 Layers circuit board with 1oz copper on outside layers.

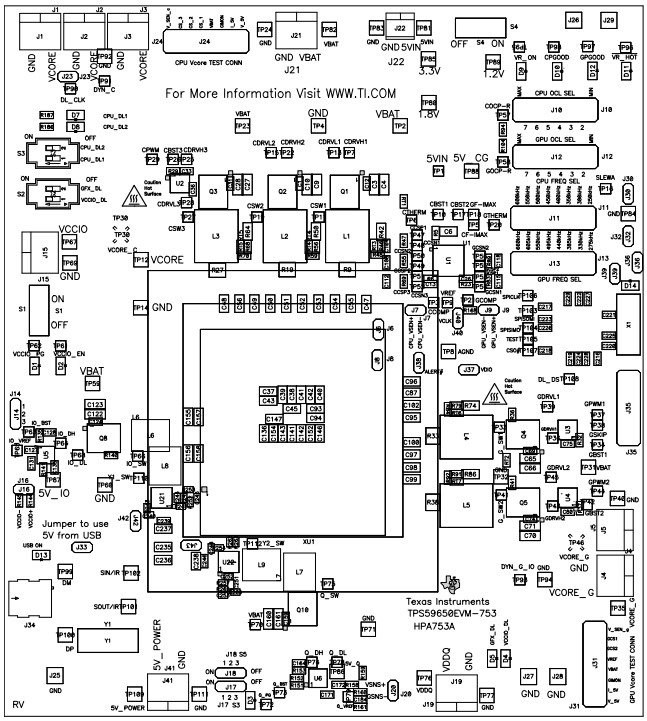


Figure 92. TPS59650EVM-753 Top Layer Assembly Drawing (Top view)

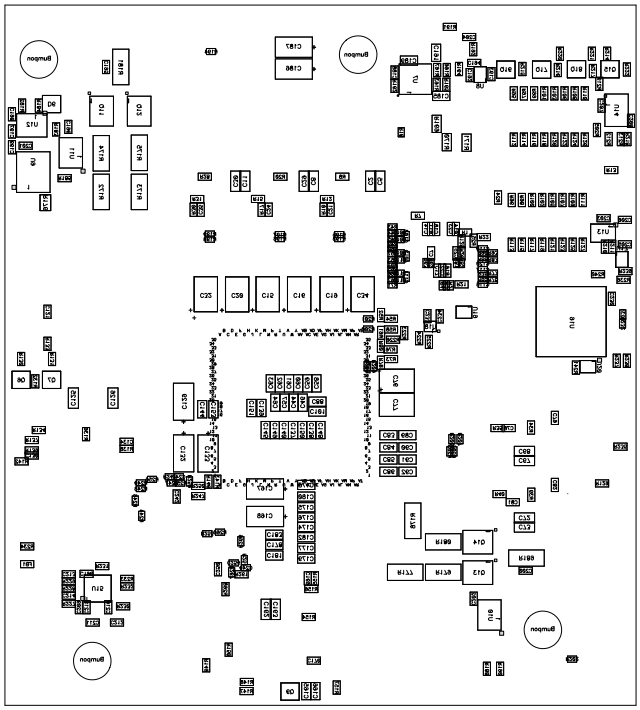


Figure 93. TPS59650EVM-753 Bottom Assembly Drawing (Bottom view)

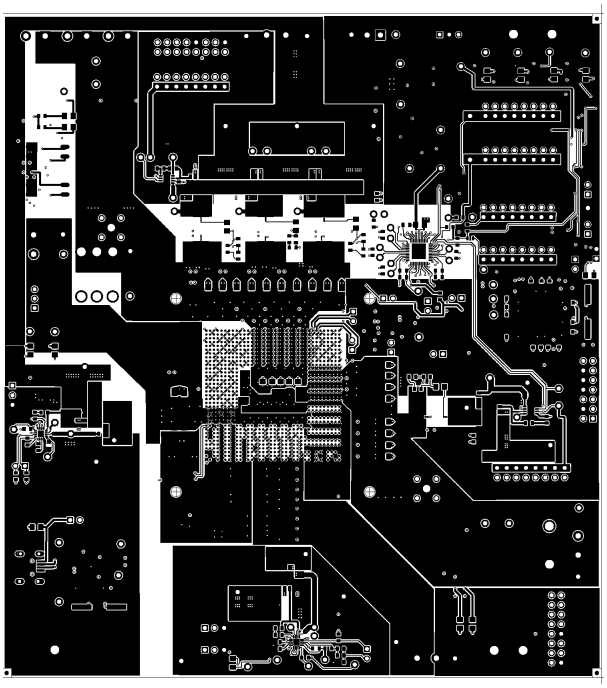


Figure 94. TPS59650EVM-753 Top Copper

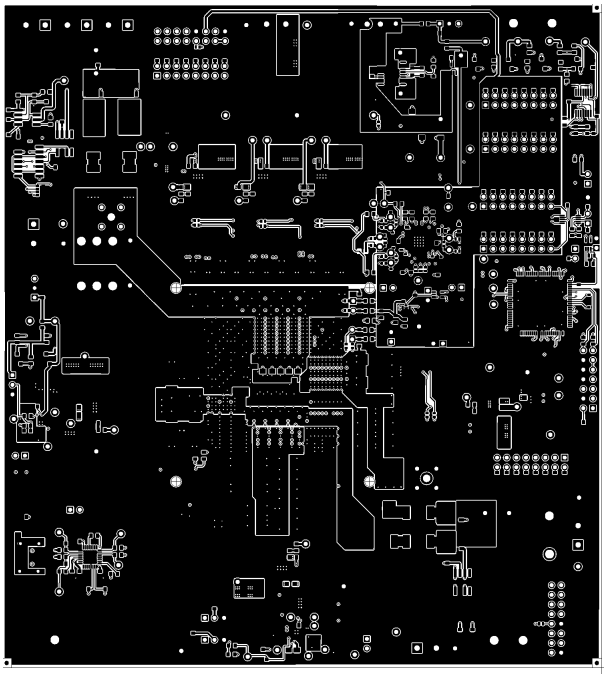


Figure 95. TPS59650EVM-753 Bottom Copper

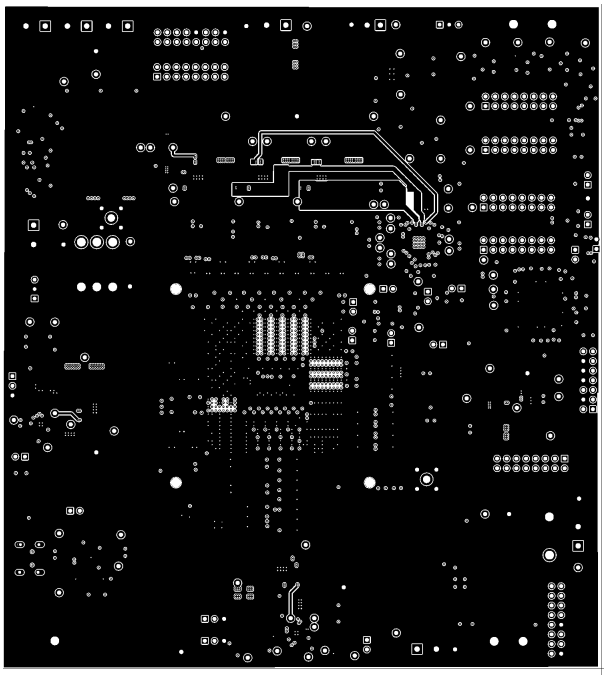


Figure 96. TPS59650EVM-753 Internal Layer 2

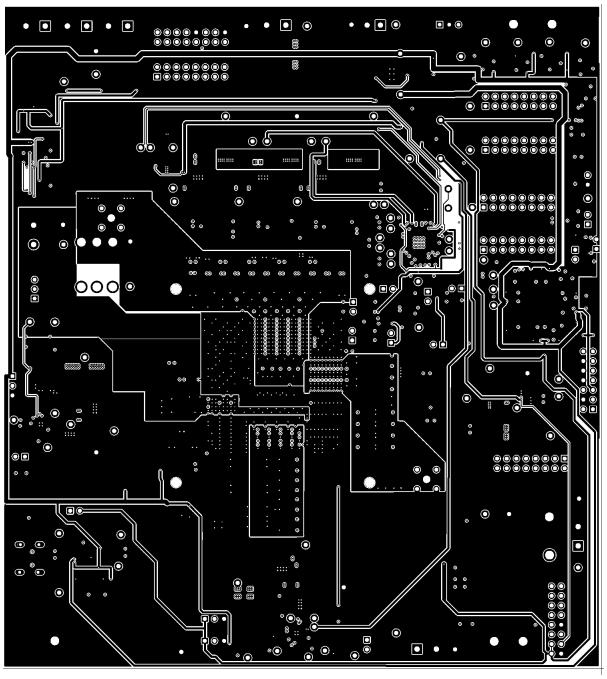


Figure 97. TPS59650EVM-753 Internal Layer 3

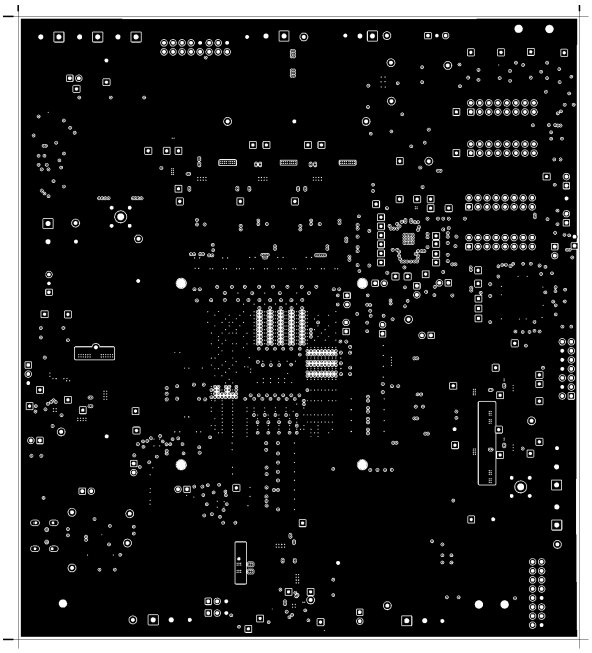


Figure 98. TPS59650EVM-753 Internal Layer 4

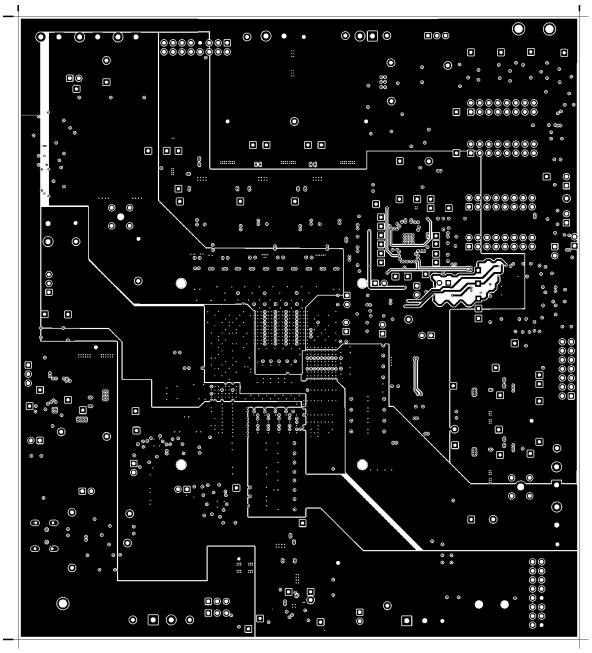


Figure 99. TPS59650EVM-753 Internal Layer 5

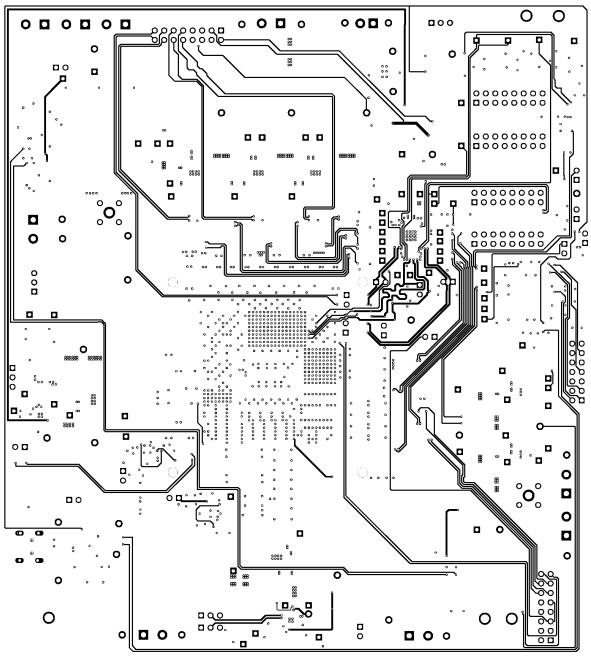


Figure 100. TPS59650EVM-753 Internal Layer 6

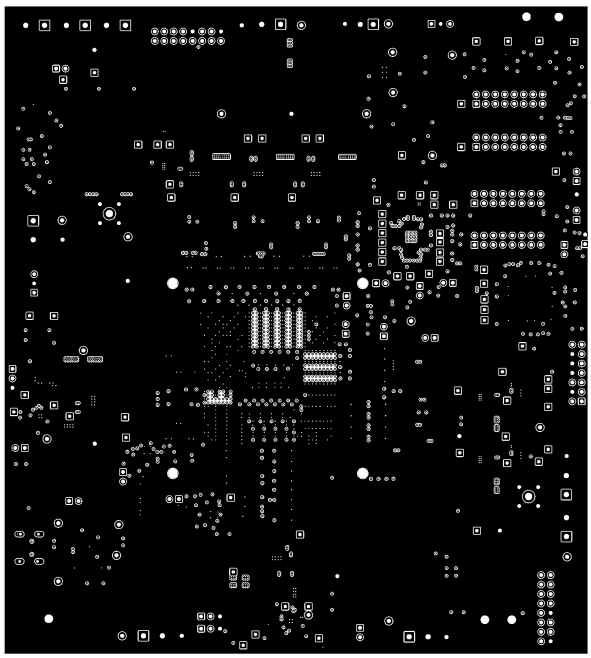


Figure 101. TPS59650EVM-753 Internal Layer 7

9 Bill of Materials

The EVM major components list according to the schematic shown in the following pages.

Table 13. EVM Major Components List

QTY	REF DES	Description	MFR	Part Number
11	C1, C12, C31, C69, C74, C124, C159, C121, C130, C184, C204	Capacitor, Ceramic, 1nF, 50V, X7R, 10%, 0603	STD	STD
5	C104, C108, C112, C115, C118	Capacitor, Ceramic, 33nF, 25V, X7R, 10%, 0603	STD	STD
29	C128, C164, C198, C199, C201, C127, C172, C188, C192, C203, C207, C190, C209, C210, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230	Capacitor, Ceramic, 0.1uF, 25V, X7R, 10%, 0603	STD	STD
3	C129, C133, C168	Capacitor, Polymer, 330uF, 2V, 6mohm, 20%, 7343	Sanyo	2TPF330M6
2	C13, C26	Capacitor, Ceramic, 100pF, 50V, C0G, 10%, 0603	STD	STD
3	C131, C239, C246	Capacitor, Ceramic, 10nF, 50V, X7R, 10%, 0603	STD	STD
6	C15, C16, C19, C20, C76, C77	Capacitor, Polymer, 470uF, 2V, 4mohm, 20%, D2T	Sanyo	2TPLF470M4E
1	C166	Capacitor, Ceramic, 2.2uF, 6.3V, X5R, 10%, 0805	STD	STD
1	C17	Capacitor, Ceramic, 0.33uF, 6.3V, X7R, 10%, 0603	STD	STD
1	C171	Capacitor, Ceramic, 0.22uF, 50V, X7R, 10%, 0603	STD	STD
15	C18, C23, C33, C75, C80, C196, C202, C208, C195, C200, C242, C250, C22, C233, C234	Capacitor, Ceramic, 1uF, 25V, X7R, 10%, 0603	STD	STD
7	C193, C36, C79, C82, C7, C135, C170	Capacitor, Ceramic, 2.2uF, 6.3V, X5R, 10%, 0603	STD	STD
3	C194, C197, C215	Capacitor, Ceramic, 0.01uF, 50V, X7R, 10%, 0603	STD	STD
28	C2, C3, C4, C5, C8, C9, C10, C11, C27, C28, C29, C30, C65, C66, C67, C68, C70, C71, C72, C73, C122, C123, C125, C126, C160, C161, C162, C163	Capacitor, Ceramic, 10uF, 25V, X7R, 20%, 1206	STD	STD
2	C205, C206	Capacitor, Ceramic, 10pF, 50V, C0G, 10%, 0603	STD	STD
2	C213, C214	Capacitor, Ceramic, 22pF, 50V, C0G, 10%, 0603	STD	STD
2	C240, C248	Capacitor, Ceramic, 0.22uF, 25V, X7R, 10%, 0402	STD	STD
2	C241, C249	Capacitor, Ceramic, 220pF, 25V, X7R, 10%, 0402	STD	STD
2	C243, C251	Capacitor, Ceramic, 680pF, 25V, X7R, 10%, 0402	STD	STD
2	C244, C252	Capacitor, Ceramic, 100pF, 25V, C0G, 10%, 0402	STD	STD
2	C245, C253	Capacitor, Ceramic, 1.8nF, 25V, X7R, 10%, 0402	STD	STD
2	C247, C254	Capacitor, Ceramic, 2200pF, 25V, X7R, 10%, 0402	STD	STD
44	C37, C38, C39, C40, C41, C42, C43, C45, C49, C50, C51, C52, C53, C54, C55, C56, C87, C88, C89, C90, C91, C92, C93, C94, C95, C100, C101, C102, C136, C140, C141, C143, C145, C146, C147, C148, C150, C151, C152, C154, C235, C236, C237, C238	Capacitor, Ceramic, 22uF, 6.3V, X5R, 10%, 0805	STD	STD
20	C44, C46, C57, C58, C59, C60, C61, C62, C63, C64, C173, C174, C175, C176, C180, C182, C165, C185, C189, C191	Capacitor, Ceramic, 10uF, 6.3V, X5R, 10%, 0805	STD	STD
1	C6	Capacitor, Ceramic, 4.7uF, 6.3V, X5R, 10%, 0805	STD	STD
8	D1, D2, D3, D9, D10, D12, D13, D14	Diode, LED, Green Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170GKT

Table 13. EVM Major Components List (continued)

QTY	REF DES	Description	MFR	Part Number
5	D4, D5, D7, D8, D11	Diode, LED, Red Clear, 20mcd, 0.079x0.049	Lite On	LTST-C170CKT
1	D6	Diode, Schottky, 200mA, 30V, SOT-23,	Vishay-Liteon	BAT54-V-GS08
1	FB1	Bead, SMD,Ferrite, 100MHz Max, 200mA, +/-25%, 0603	WE	74279266A
5	L1, L2, L3, L4, L5	Inductor, SMT, 0.36uH, 35A , 0.82mohm, 10x11.5mm	Toko	FCUL1040-H-R36M
1	L6	Inductor, SMT, 0.42uH, 17A , 1.5mohm, 8.7x7.0mm	Panasonic	ETQP4LR42AFM
1	L7	Inductor, SMT, 1.0uH, 8.1A , 6.9mohm, 7.3x6.6mm	Panasonic	ETQP3W1R0WFN
7	Q1, Q2, Q3, Q4, Q5, Q8, Q10	MOSFET, Synchronous Buck NexFET Power Block SON 5X6mm	TI	CSD87350Q5D
4	Q11, Q12, Q13, Q14	MOSFET, Nchan, 25V, 31A, 2.5mohm, QFN5X6mm	TI	CSD16407Q5
1	Q15	MOSFET, Pchan, -60V, -0.33A, 2ohm, SOT23	Infineon	BSS83P
6	Q6, Q7, Q9, Q16, Q17, Q18	MOSFET, Nchan, 100V, 0.17A, 6ohm, SOT23	Fairchild	BSS123
1	R1	Resistor, Chip, 42.2k, 1/10W, 1%, 0603	STD	STD
4	R101, R102, R118, R119	Resistor, Chip, 56.2k, 1/10W, 1%, 0603	STD	STD
1	R104	Resistor, Chip, 2.43k, 1/10W, 1%, 0603	STD	STD
7	R106, R107, R122, R123, R141, R165, R166	Resistor, Chip, 30.1k, 1/10W, 1%, 0603	STD	STD
4	R108, R109, R124, R125	Resistor, Chip, 24.3k, 1/10W, 1%, 0603	STD	STD
22	R12, R15, R24, R31, R36, R41, R54, R58, R73, R76, R140, R142, R144, R145, R156, R157, R159, R161, R232, R233, R250, R268	Resistor, Chip, 0, 1/10W, 1%, 0603	STD	STD
7	R130, R131, R147, R215, R216, R217, R222	Resistor, Chip, 180, 1/10W, 1%, 0603	STD	STD
14	R132, R148, R149, R150, R158, R183, R185, R205, R214, R219, R220, R221, R230, R231	Resistor, Chip, 10.0k, 1/10W, 1%, 0603	STD	STD
5	R133, R134, R151, R213, R218	Resistor, Chip, 1.00k, 1/10W, 1%, 0603	STD	STD
1	R139	Resistor, Chip, 10.5k, 1/10W, 1%, 0603	STD	STD
1	R152	Resistor, Chip, 22.1k, 1/10W, 1%, 0603	STD	STD
6	R16, R110, R111, R126, R127, R160	Resistor, Chip, 20.0k, 1/10W, 1%, 0603	STD	STD
1	R163	Resistor, Chip, 15.0k, 1/10W, 1%, 0603	STD	STD
4	R164, R237, R238, R239	Resistor, Chip, 2.00k, 1/10W, 1%, 0603	STD	STD
1	R167	Resistor, Chip, 51.1k, 1/10W, 1%, 0603	STD	STD
1	R168	Resistor, Chip, 1, 1/10W, 1%, 0603	STD	STD
1	R176	Resistor, Chip Array, 10.0k, 62.5mW, 5%, 1206	Yageo	TC164-JR-0710KL
3	R169, R170, R171	Resistor, Chip, 1, 1/8W, 1%, 0805	STD	STD
3	R172, R173, R178	Resistor, Chip, 0.01, 1W, 1%, 2512	STD	STD
5	R174, R175, R177, R179, R180	Resistor, Chip, 0.05, 1W, 1%, 2512	STD	STD
5	R176, R177, R178, R179, R199	Resistor, Chip, 330, 1/10W, 1%, 0603	STD	STD
7	R18, R194, R202, R246, R248, R260, R262	Resistor, Chip, 10.0k, 1/16W, 1%, 0402	STD	STD
2	R181, R189	Resistor, Chip, 0.005, 1W, 1%, 2512	STD	STD
1	R182	Resistor, Chip, 8.06k, 1/10W, 1%, 0603	STD	STD
5	R186, R187, R188, R190, R212	Resistor, Chip, 330, 1/10W, 1%, 0603	STD	STD
1	R192	Resistor, Chip, 100, 1/10W, 1%, 0603	STD	STD
10	R193, R195, R196, R197, R198, R199, R203, R204, R206, R207	Resistor, Chip, 1M, 1/16W, 1%, 0402	STD	STD
1	R2	Resistor, Chip, 130, 1/16W, 1%, 0402	STD	STD

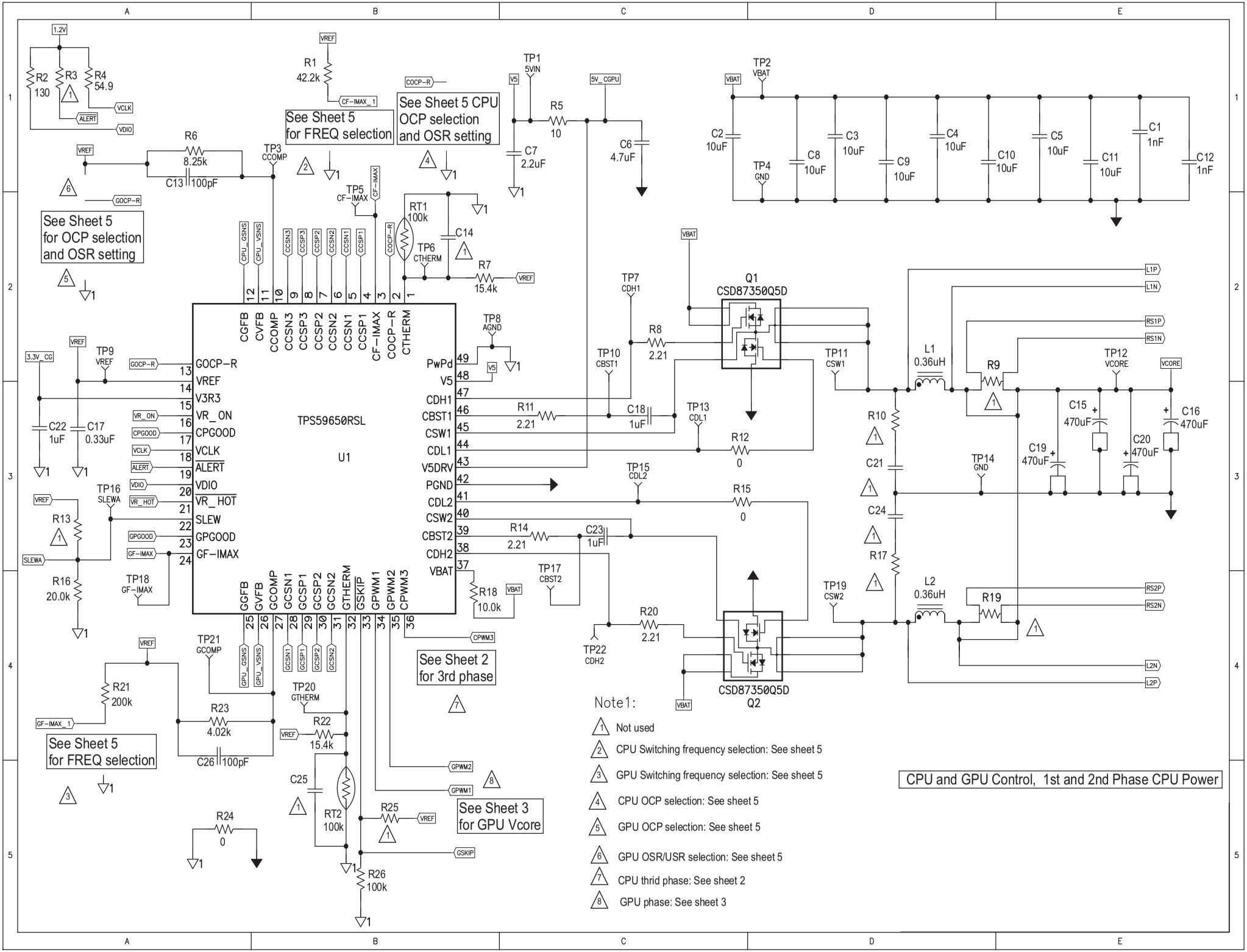
Table 13. EVM Major Components List (continued)

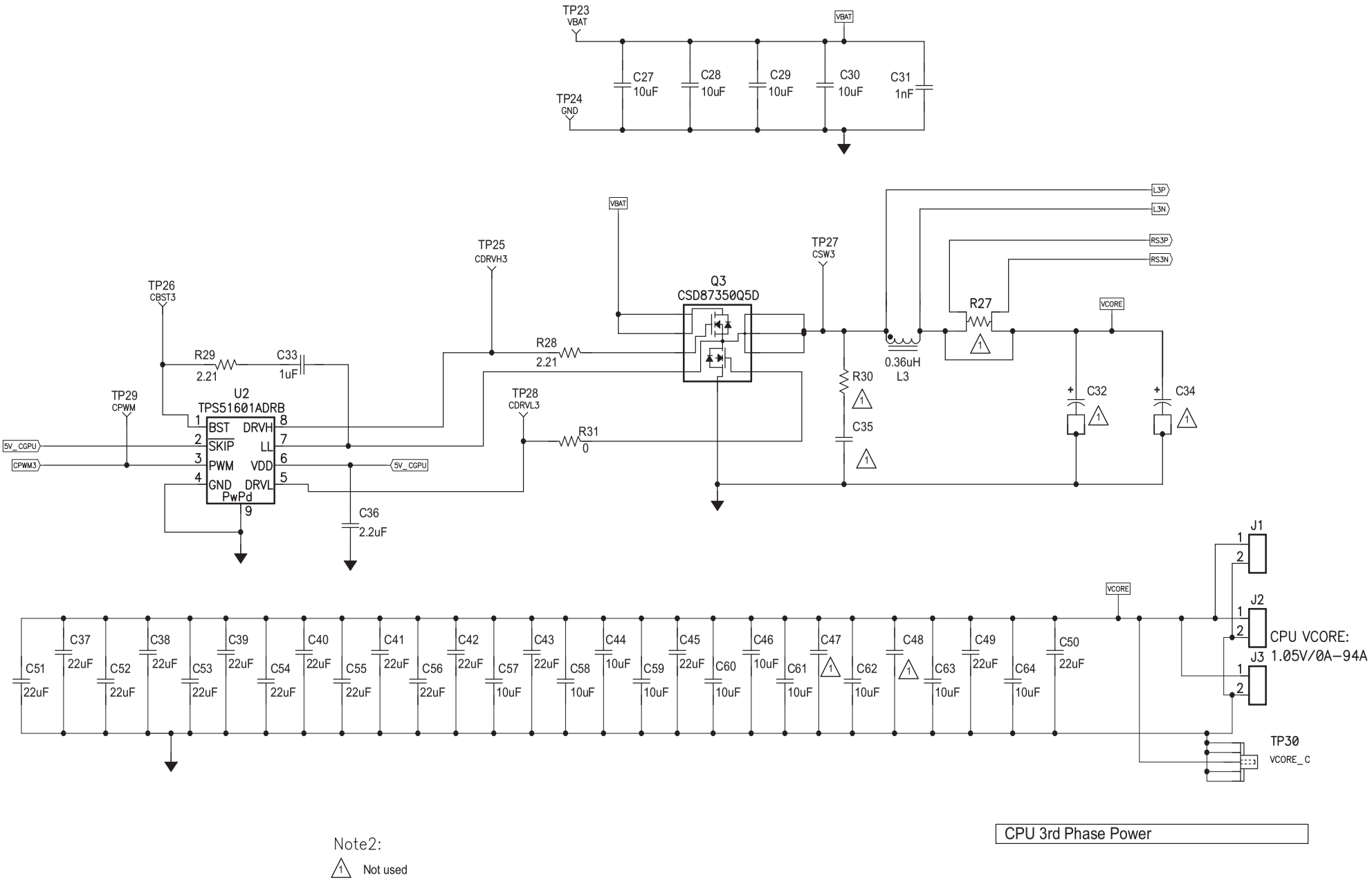
QTY	REF DES	Description	MFR	Part Number
20	R43, R49, R51, R60, R65, R71, R75, R85, R87, R93, R200, R201, R208, R209, R243, R249, R253, R254, R263, R265	Resistor, Chip, 0, 1/16W, 1%, 0402	STD	STD
1	R21	Resistor, Chip, 200k, 1/10W, 1%, 0603	STD	STD
2	R210, R211	Resistor, Chip, 3.01k, 1/10W, 1%, 0603	STD	STD
1	R224	Resistor, Chip, 75, 1/10W, 1%, 0603	STD	STD
1	R225	Resistor, Chip, 130, 1/10W, 1%, 0603	STD	STD
1	R226	Resistor, Chip, 43.2, 1/10W, 1%, 0603	STD	STD
1	R227	Resistor, Chip, 1.50k, 1/10W, 1%, 0603	STD	STD
2	R228, R229	Resistor, Chip, 33.2, 1/10W, 1%, 0603	STD	STD
1	R23	Resistor, Chip, 4.02k, 1/10W, 1%, 0603	STD	STD
2	R234, R236	Resistor, Chip, 470, 1/10W, 1%, 0603	STD	STD
1	R235	Resistor, Chip, 2.21k, 1/10W, 1%, 0603	STD	STD
2	R240, R241	Resistor, Chip, 2.74k, 1/10W, 1%, 0603	STD	STD
2	R242, R251	Resistor, Chip, 2.21, 1/16W, 1%, 0402	STD	STD
2	R244, R255	Resistor, Chip, 475k, 1/16W, 1%, 0402	STD	STD
2	R245, R257	Resistor, Chip, 5.62k, 1/16W, 1%, 0402	STD	STD
2	R252, R264	Resistor, Chip, 2.00k, 1/16W, 1%, 0402	STD	STD
1	R258	Resistor, Chip, 3.09k, 1/16W, 1%, 0402	STD	STD
1	R259	Resistor, Chip, 20.0k, 1/16W, 1%, 0402	STD	STD
7	R26, R97, R98, R114, R115, R162, R184	Resistor, Chip, 100k, 1/10W, 1%, 0603	STD	STD
1	R267	Resistor, Chip, 1.37k, 1/16W, 1%, 0603	STD	STD
1	R4	Resistor, Chip, 54.9, 1/16W, 1%, 0402	STD	STD
5	R42, R50, R64, R74, R86	Resistor, Chip, 17.8k, 1/8W, 1%, 0805	STD	STD
5	R46, R56, R68, R79, R91	Resistor, Chip, 162k, 1/10W, 1%, 0603	STD	STD
5	R48, R59, R70, R84, R92	Resistor, Chip, 28.7k, 1/10W, 1%, 0603	STD	STD
7	R5, R52, R61, R72, R80, R143, R146	Resistor, Chip, 10, 1/10W, 1%, 0603	STD	STD
1	R6	Resistor, Chip, 8.25k, 1/10W, 1%, 0603	STD	STD
2	R7, R22	Resistor, Chip, 15.4k, 1/10W, 1%, 0603	STD	STD
14	R8, R11, R14, R20, R28, R29, R32, R34, R37, R39, R135, R136, R153, R154	Resistor, Chip, 2.21, 1/10W, 1%, 0603	STD	STD
5	R94, R103, R105, R120, R121	Resistor, Chip, 39.2k, 1/10W, 1%, 0603	STD	STD
4	R95, R96, R112, R113	Resistor, Chip, 150k, 1/10W, 1%, 0603	STD	STD
4	R99, R100, R116, R117	Resistor, Chip, 75.0k, 1/10W, 1%, 0603	STD	STD
7	RT1, RT2, RT3, RT4, RT5, RT6, RT7	NTC Thermistor, 100k, 0603, 5%	Murata	NCP18WF104J03RB
1	U1	IC, 3+2 phase, IMVP-7 VCORE CPU and GPU Controller, QFN-48	TI	TPS59650RSL
1	U12	IC, Timer, Low-Power CMOS, SO-8	TI	TLC555CDR
1	U13	IC, Dual 10 ohm SPDT Analogy Switch, DGS_10P	TI	TS5A23157DGS
1	U14	IC, Nano Power, Open output comparators, PW14	TI	TLV3404IPW
1	U15	IC, USB to series port controller, QFN-32	TI	TUSB3410RHB
1	U16	IC, CMOS programmable controller, QFP-100	TI	TMS320F2808PZS
3	U17, U19, U20	IC, Dual Schmitt-trigger inverter, DCK-6	TI	SN74LVC2G07DCK
1	U18	IC, Dual-bit dual-supply bus transceiver, RSW-10	TI	SN74AVC2T245RSW
3	U2, U3, U4	IC, Dual high voltage, efficient synchronous MOSFET buck driver, QFN-8	TI	TPS51601ADRB
1	U5	IC, High performance, single synchronous step down controller, QFN-16	TI	TPS51219RTE
1	U6	IC, Complete DDR2, DDR3 and DDR3L memory power solution, QFN-20	TI	TPS51916RUK
1	U7	IC, Dual low dropout regulator, 500mA and 250mA outputs, PWP20	TI	TPS70102PWP
1	U8	IC, 150mA, low Iq, wide bandwidth, LDO, SC70	TI	TPS71712DCK

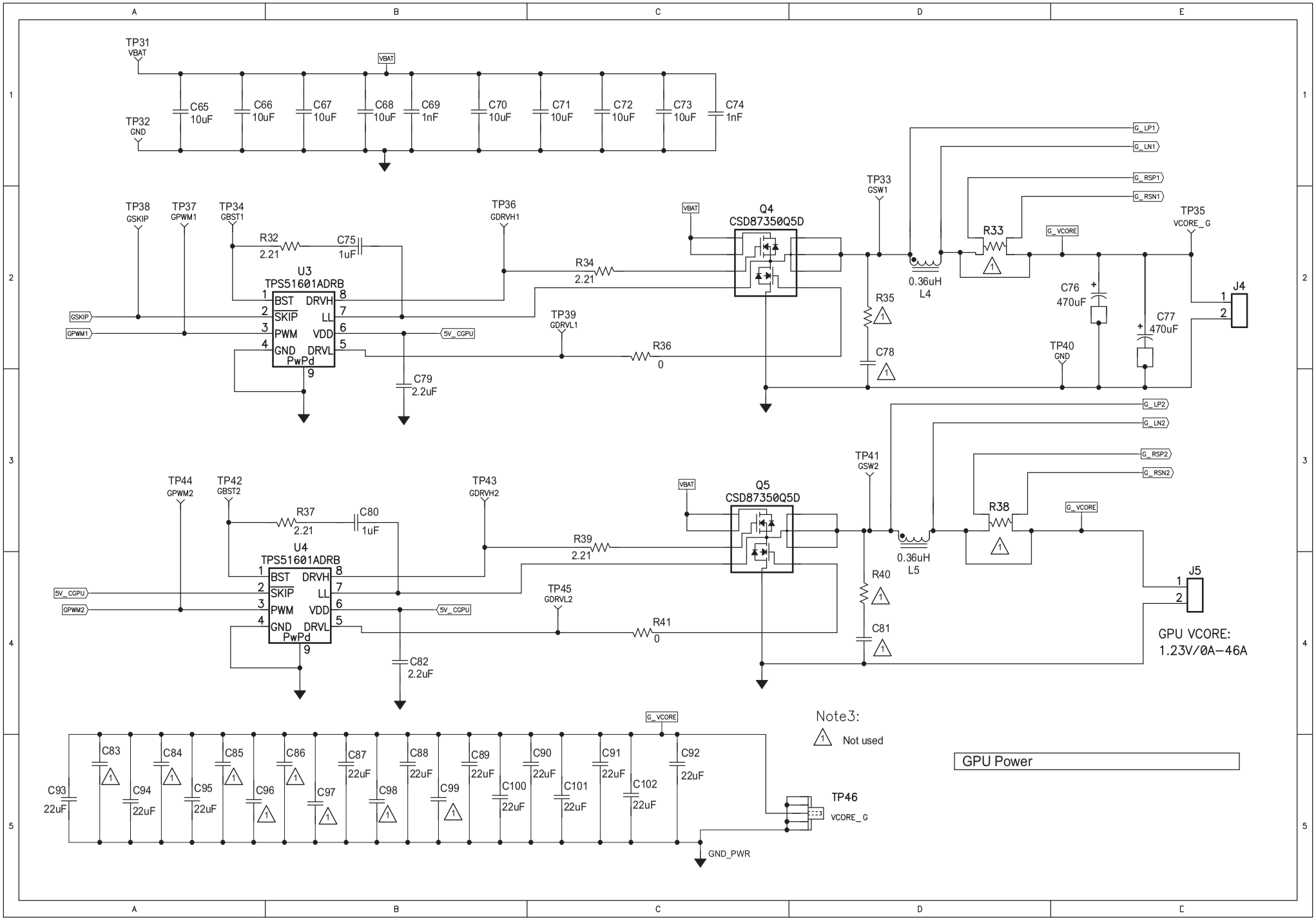
Table 13. EVM Major Components List (continued)

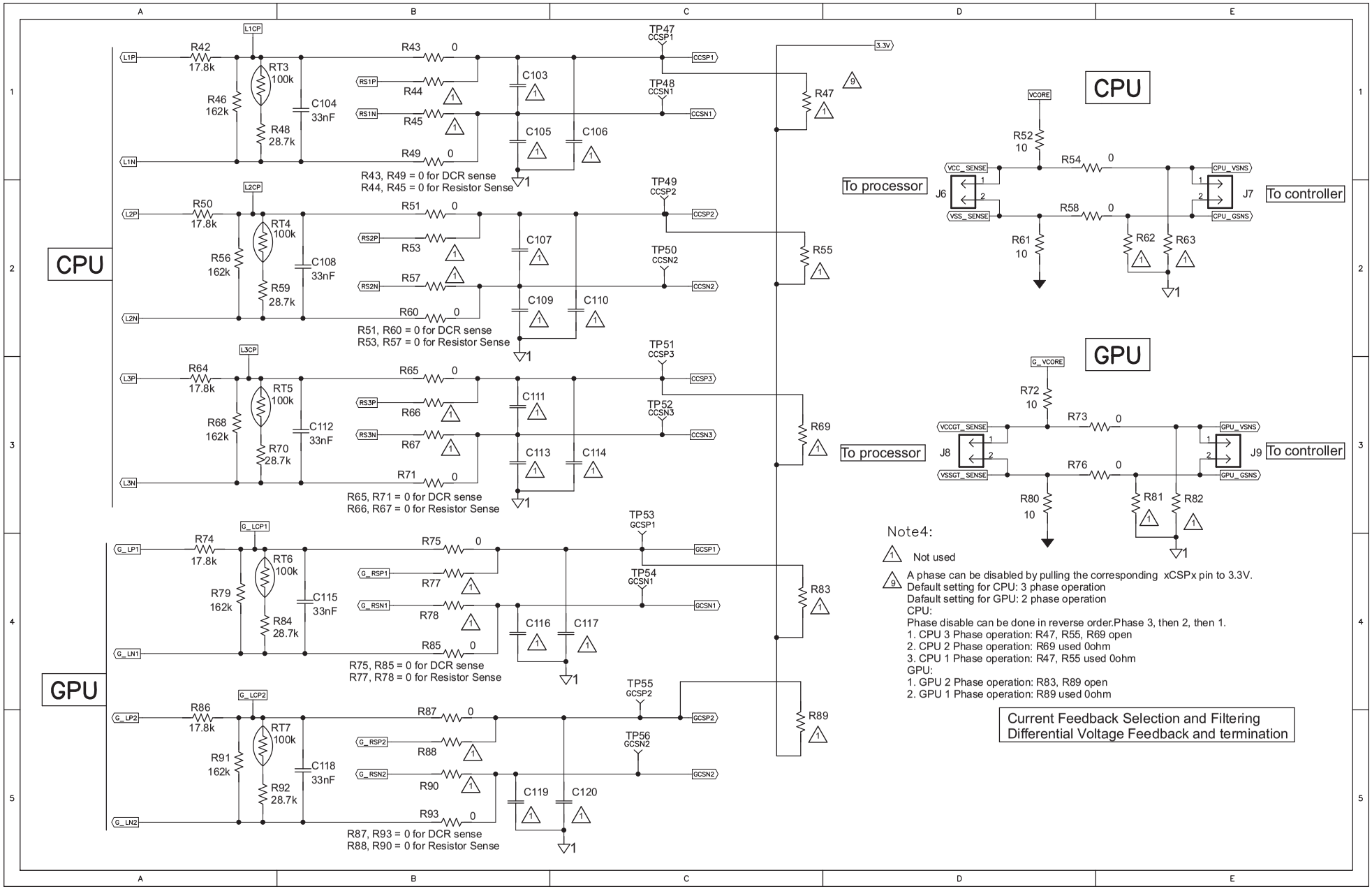
QTY	REF DES	Description	MFR	Part Number
1	U9	IC, Quadruple 2-input positive –AND gates, SO-14	TI	SN74HC08D
2	U10, U11	IC, Dual 4A High speed low side power MOSFET drivers, SO-8	TI	UCC27324D
1	X1	Crystal, controlled oscillators, 0.150”x0.528”	ABRACON	ABLS-20.000MHZ-B2-T
1	Y1	Crystal, controlled oscillators, 0.150”x0.528”	ABRACON	ABLS-12.000MHZ-B2-T
1	XU1	Socket, CPU	Molex	rPGA989

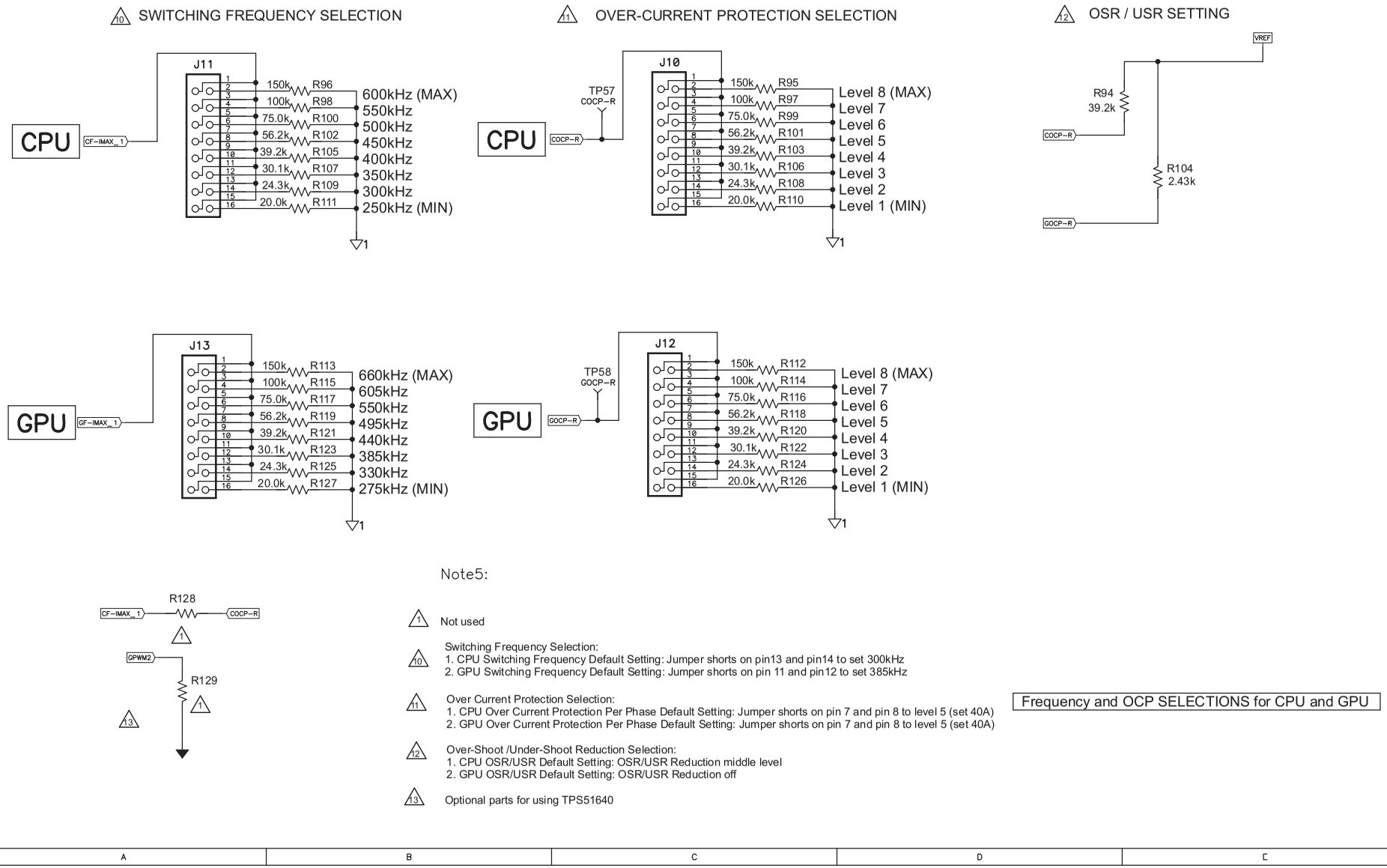
10 Schematics


TPS59650RSL
U1
Q1
CSD87350Q5D
Q2
CSD87350Q5D
CPU and GPU Control, 1st and 2nd Phase CPU Power
See Sheet 5 for FREQ selection
See Sheet 5 CPU OCP selection and OSR setting
See Sheet 5 for OCP selection and OSR setting
See Sheet 5 for FREQ selection
See Sheet 2 for 3rd phase
See Sheet 3 for GPU Vcore
Note1:
1 Not used
2 CPU Switching frequency selection: See sheet 5
3 GPU Switching frequency selection: See sheet 5
4 CPU OCP selection: See sheet 5
5 GPU OCP selection: See sheet 5
6 GPU OSR/USR selection: See sheet 5
7 CPU thrid phase: See sheet 2
8 GPU phase: See sheet 3


TP23
VBAT
TP24
GND
VBAT
C27
10uF
C28
10uF
C29
10uF
C30
10uF
C31
1nF
TP25
CDRVH3
TP26
CBST3
TP27
CSW3
Q3
CSD87350Q5D
L3P
L3N
RS3P
RS3N
R27
VCORE
R29
2.21
C33
1uF
R28
2.21
0.36uH
L3
R30
C32
C34
TP29
CPWM
U2
TPS51601ADRB
TP28
CDRVL3
R31
0
C35
5V_CGPU
CPWM3
BST
DRVH
SKIP
LL
PWM
VDD
GND
DRVL
PwPd
C36
2.2uF
J1
J2
J3
CPU VCORE:
1.05V/0A-94A
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
C51
C52
C53
C54
C55
C56
C57
C58
C59
C60
C61
C62
C63
C64
22uF
10uF
TP30
VCORE_C
Note2:
Not used
CPU 3rd Phase Power


TP31
VBAT
TP32
GND
C65 10uF
C66 10uF
C67 10uF
C68 10uF
C69 1nF
C70 10uF
C71 10uF
C72 10uF
C73 10uF
C74 1nF
TP38
GSKIP
TP37
GPWM1
TP34
GBST1
R32 2.21
C75 1uF
U3
TPS51601ADRB
BST
SKIP
PWM
GND
DRVH
LL
VDD
DRVL
PwPd
TP36
GDRVH1
R34 2.21
TP39
GDRVL1
R36 0
C79 2.2uF
5V_CGPU
Q4
CSD87350Q5D
TP33
GSW1
0.36uH
L4
R33
R35
C78
C76 470uF
C77 470uF
TP40
GND
TP35
VCORE_G
J4
G_LP1
G_LN1
G_RSP1
G_RSN1
G_VCORE
TP44
GPWM2
TP42
GBST2
R37 2.21
C80 1uF
U4
TPS51601ADRB
TP43
GDRVH2
R39 2.21
TP45
GDRVL2
R41 0
C82 2.2uF
Q5
CSD87350Q5D
TP41
GSW2
0.36uH
L5
R38
R40
C81
J5
G_LP2
G_LN2
G_RSP2
G_RSN2
GPU VCORE:
1.23V/0A–46A
C83
C84
C85
C86
C87 22uF
C88 22uF
C89 22uF
C90 22uF
C91 22uF
C92 22uF
C93 22uF
C94 22uF
C95 22uF
C96
C97
C98
C99
C100 22uF
C101 22uF
C102 22uF
TP46
VCORE_G
GND_PWR
Note3:
Not used
GPU Power


CPU
GPU
L1CP
L1P
L1N
R42
17.8k
RT3
100k
R46
162k
R48
28.7k
C104
33nF
R43
0
RS1P
R44
RS1N
R45
R49
0
C103
C105
C106
TP47
CCSP1
TP48
CCSN1
CCSP1
CCSN1
R43, R49 = 0 for DCR sense
R44, R45 = 0 for Resistor Sense
L2CP
L2P
L2N
R50
17.8k
RT4
100k
R56
162k
R59
28.7k
C108
33nF
R51
0
RS2P
R53
RS2N
R57
R60
0
C107
C109
C110
TP49
CCSP2
TP50
CCSN2
CCSP2
CCSN2
R51, R60 = 0 for DCR sense
R53, R57 = 0 for Resistor Sense
L3CP
L3P
L3N
R64
17.8k
RT5
100k
R68
162k
R70
28.7k
C112
33nF
R65
0
RS3P
R66
RS3N
R67
R71
0
C111
C113
C114
TP51
CCSP3
TP52
CCSN3
CCSP3
CCSN3
R65, R71 = 0 for DCR sense
R66, R67 = 0 for Resistor Sense
G_LCP1
G_LP1
G_LN1
R74
17.8k
RT6
100k
R79
162k
R84
28.7k
C115
33nF
R75
0
G_RSP1
R77
G_RSN1
R78
R85
0
C116
C117
TP53
GCSP1
TP54
GCSN1
GCSP1
GCSN1
R75, R85 = 0 for DCR sense
R77, R78 = 0 for Resistor Sense
G_LCP2
G_LP2
G_LN2
R86
17.8k
RT7
100k
R91
162k
R92
28.7k
C118
33nF
R87
0
G_RSP2
R88
G_RSN2
R90
R93
0
C119
C120
TP55
GCSP2
TP56
GCSN2
GCSP2
GCSN2
R87, R93 = 0 for DCR sense
R88, R90 = 0 for Resistor Sense
3.3V
R47
R55
R69
R83
R89
To processor
VCORE
R52
10
R54
0
VCC_SENSE
VSS_SENSE
J6
J7
CPU_VSNS
CPU_GSNS
R58
0
R61
10
R62
R63
To controller
G_VCORE
R72
10
R73
0
VCCGT_SENSE
VSSGT_SENSE
J8
J9
GPU_VSNS
GPU_GSNS
R76
0
R80
10
R81
R82
Note4:
Not used
A phase can be disabled by pulling the corresponding xCSPx pin to 3.3V.
Default setting for CPU: 3 phase operation
Default setting for GPU: 2 phase operation
CPU:
Phase disable can be done in reverse order.Phase 3, then 2, then 1.
1. CPU 3 Phase operation: R47, R55, R69 open
2. CPU 2 Phase operation: R69 used 0ohm
3. CPU 1 Phase operation: R47, R55 used 0ohm
GPU:
1. GPU 2 Phase operation: R83, R89 open
2. GPU 1 Phase operation: R89 used 0ohm
Current Feedback Selection and Filtering
Differential Voltage Feedback and termination



Note5:

1. Not used

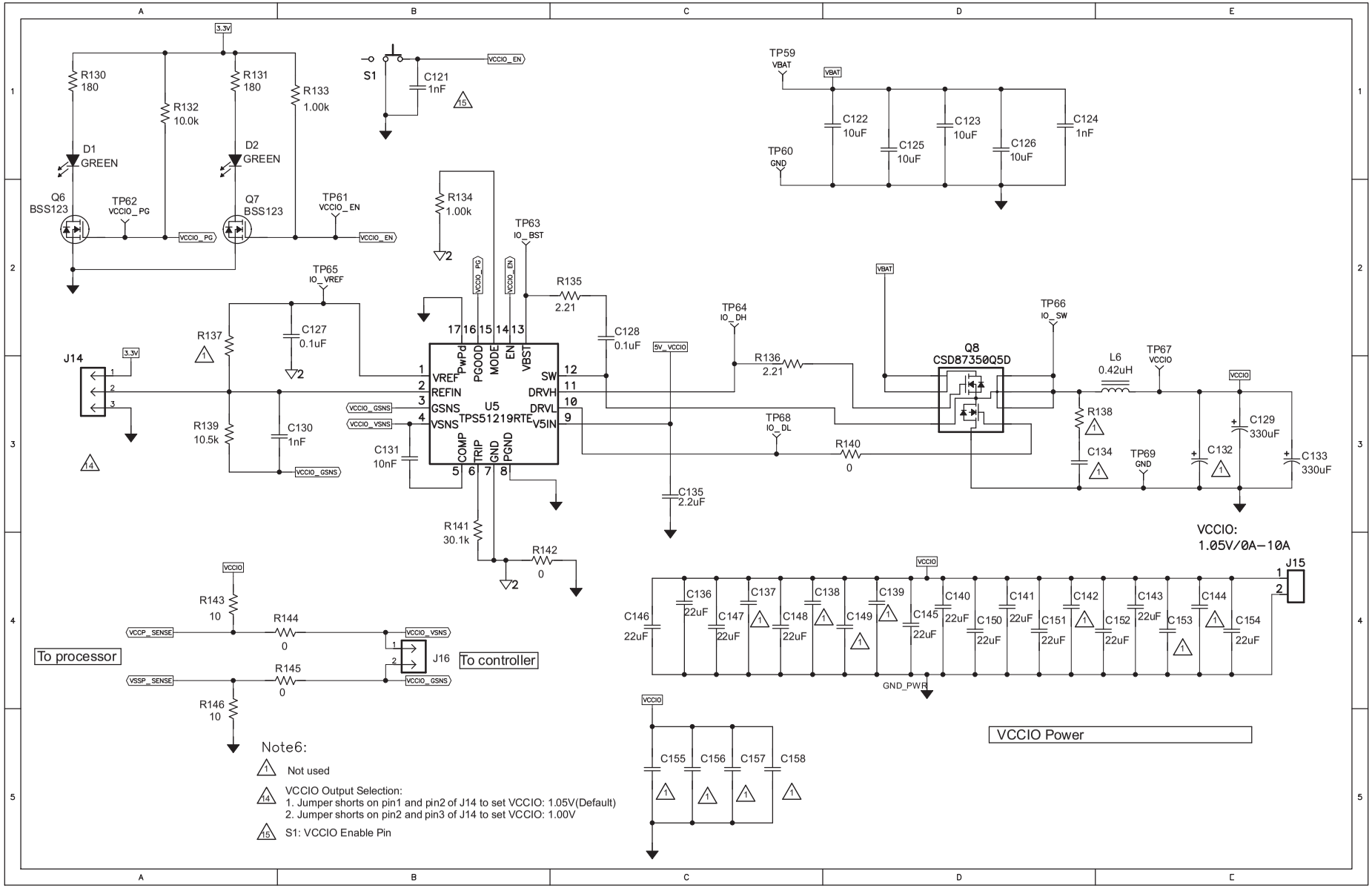
10. Switching Frequency Selection:
    1. CPU Switching Frequency Default Setting: Jumper shorts on pin13 and pin14 to set 300kHz
    2. GPU Switching Frequency Default Setting: Jumper shorts on pin 11 and pin12 to set 385kHz

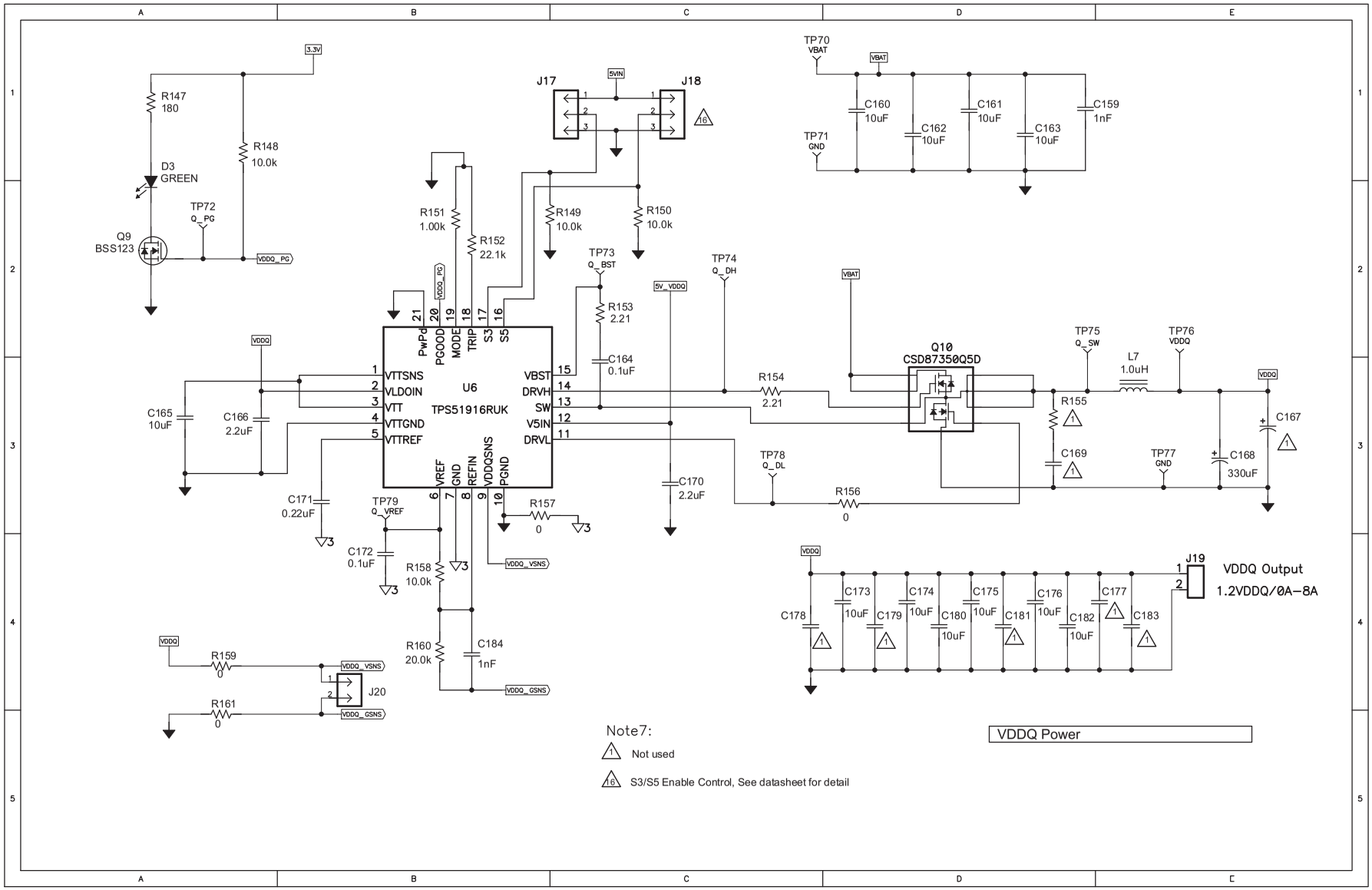
11. Over Current Protection Selection:
    1. CPU Over Current Protection Per Phase Default Setting: Jumper shorts on pin 7 and pin 8 to level 5 (set 40A)
    2. GPU Over Current Protection Per Phase Default Setting: Jumper shorts on pin 7 and pin 8 to level 5 (set 40A)

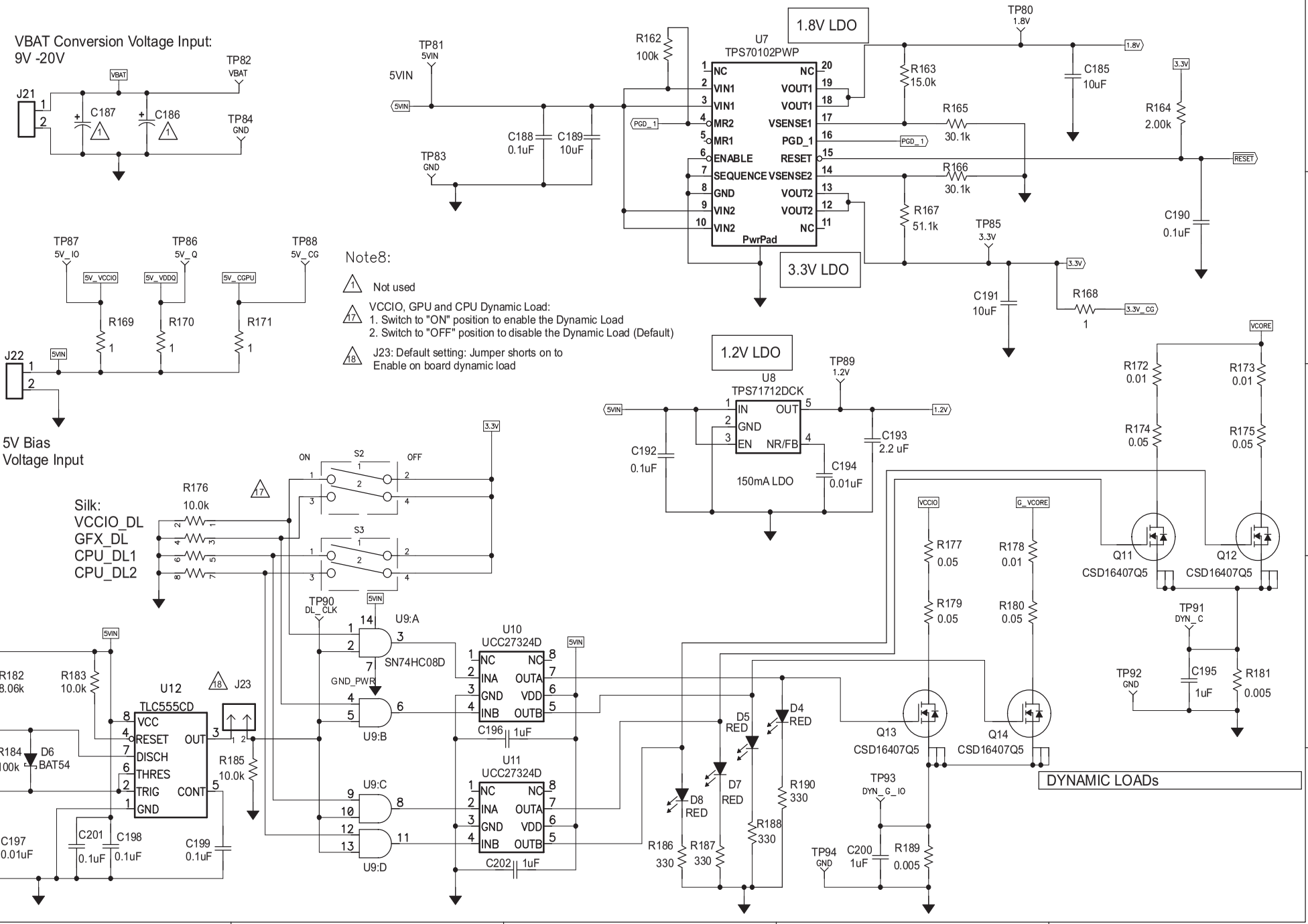
12. Over-Shoot /Under-Shoot Reduction Selection:
    1. CPU OSR/USR Default Setting: OSR/USR Reduction middle level
    2. GPU OSR/USR Default Setting: OSR/USR Reduction off

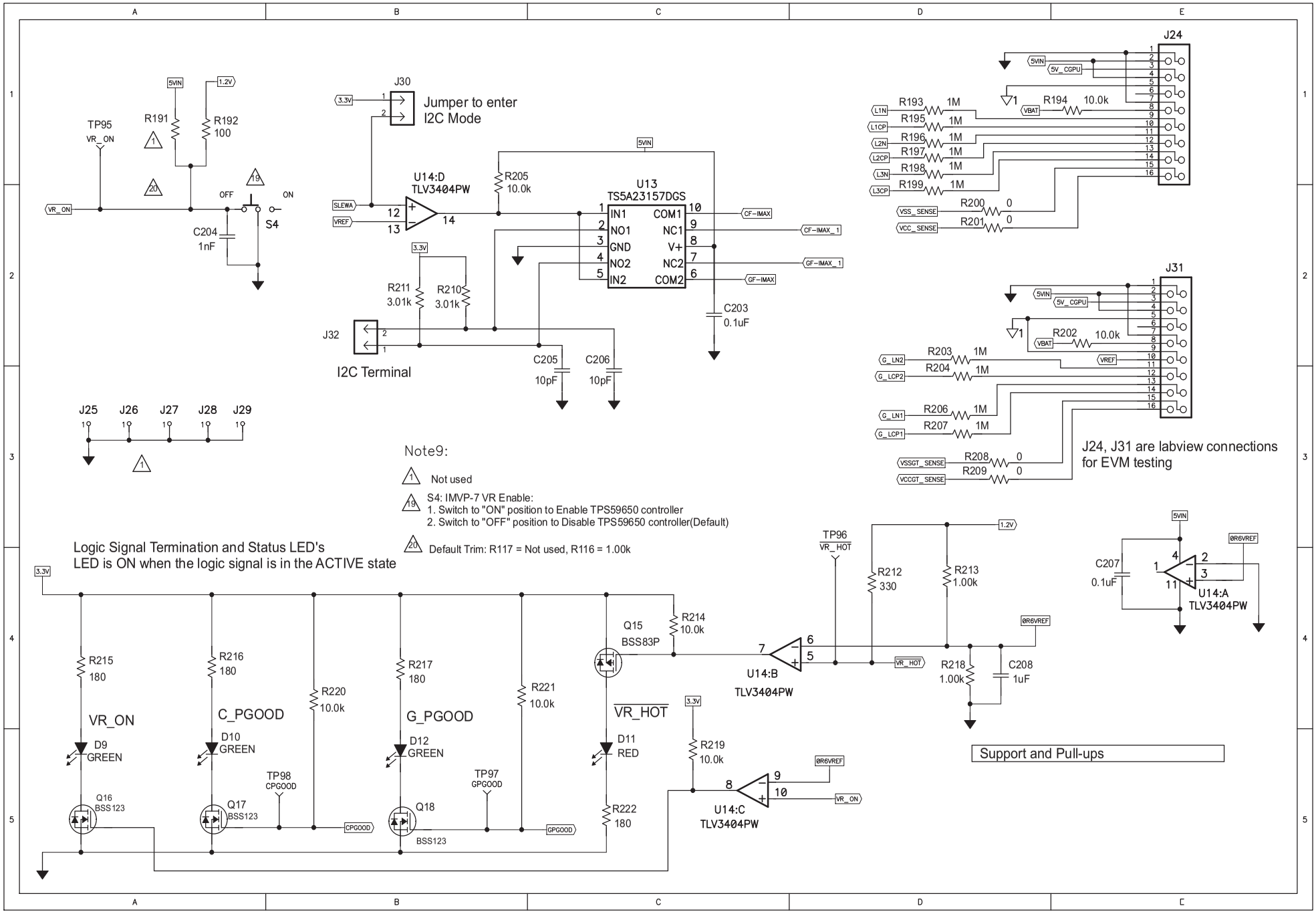
13. Optional parts for using TPS51640

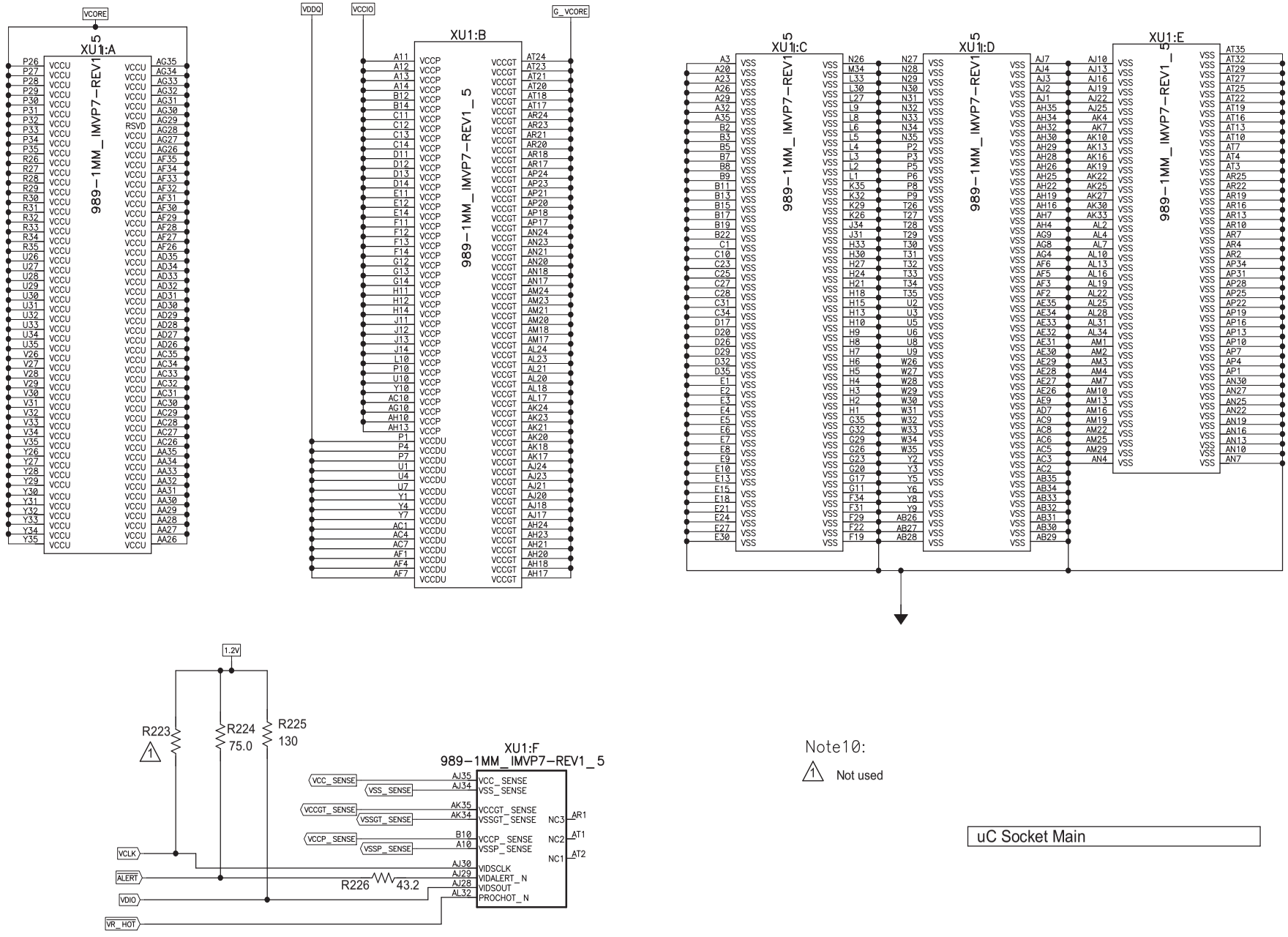
Frequency and OCP SELECTIONS for CPU and GPU

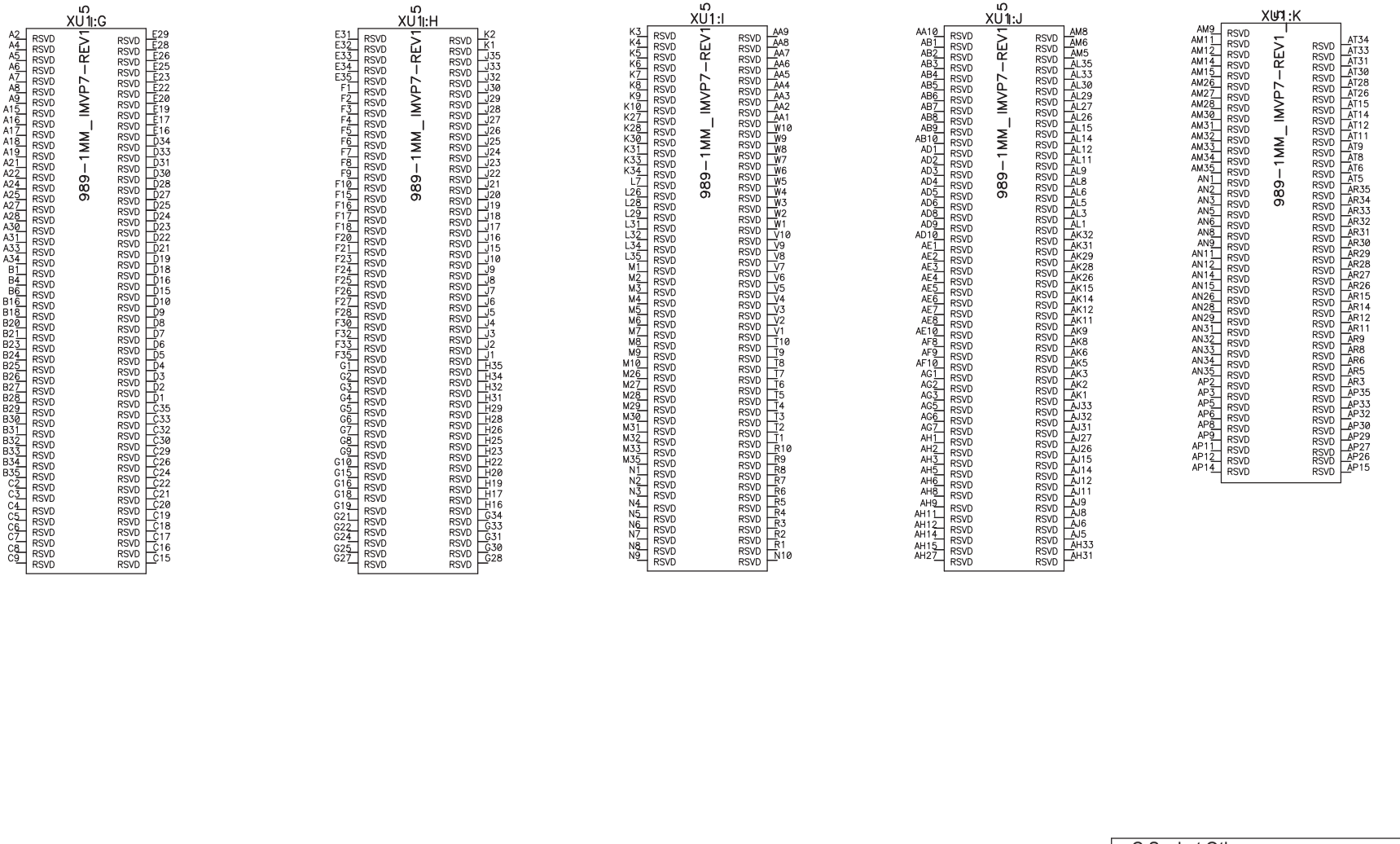

3.3V
R130 180
R131 180
R132 10.0k
R133 1.00k
D1 GREEN
D2 GREEN
Q6 BSS123
Q7 BSS123
TP62 VCCIO_PG
TP61 VCCIO_EN
S1
C121 1nF
R134 1.00k
TP63 IO_BST
TP65 IO_VREF
R135 2.21
C128 0.1uF
TP64 IO_DH
R136 2.21
TP66 IO_SW
Q8 CSD87350Q5D
L6 0.42uH
TP67 VCCIO
C129 330uF
C132
C133 330uF
R138
C134
TP69 GND
TP68 IO_DL
R140 0
C135 2.2uF
R137
C127 0.1uF
R139 10.5k
C130 1nF
C131 10nF
R141 30.1k
R142 0
J14
U5 TPS51219RTE
PwPd PGOOD MODE EN VBST
VREF REFIN GSNS VSNS
SW DRVH DRVL V5IN
COMP TRIP GND PGND
TP59 VBAT
TP60 GND
C122 10uF
C125 10uF
C123 10uF
C126 10uF
C124 1nF
VCCIO: 1.05V/0A–10A
J15
C136 22uF
C137
C138
C139
C140 22uF
C141 22uF
C142
C143 22uF
C144
C146 22uF
C147 22uF
C148 22uF
C149
C145 22uF
C150 22uF
C151 22uF
C152 22uF
C153
C154 22uF
GND_PWR
VCCIO Power
C155
C156
C157
C158
R143 10
R144 0
R145 0
R146 10
VCCP_SENSE
VSSP_SENSE
J16
To processor
To controller
Note6:
1 Not used
14 VCCIO Output Selection:
1. Jumper shorts on pin1 and pin2 of J14 to set VCCIO: 1.05V(Default)
2. Jumper shorts on pin2 and pin3 of J14 to set VCCIO: 1.00V
15 S1: VCCIO Enable Pin

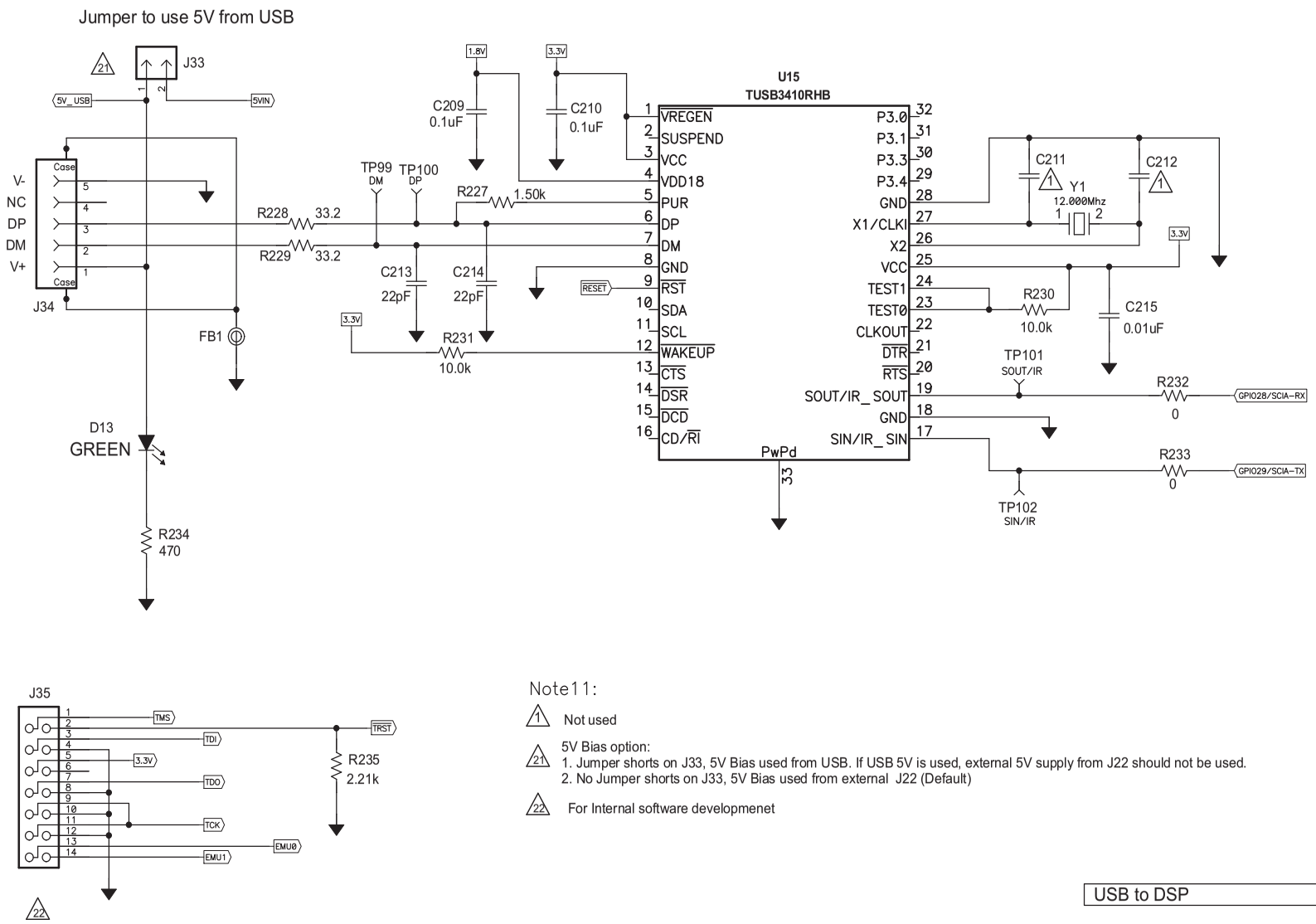

3.3V
R147
180
R148
10.0k
D3
GREEN
TP72
Q_PG
Q9
BSS123
VDDQ_PG
J17
5VIN
J18
TP70
VBAT
TP71
GND
C160
10uF
C162
10uF
C161
10uF
C163
10uF
C159
1nF
R151
1.00k
R152
22.1k
R149
10.0k
R150
10.0k
TP73
Q_BST
TP74
Q_DH
5V_VDDQ
VBAT
R153
2.21
C164
0.1uF
VDDQ
C165
10uF
C166
2.2uF
U6
TPS51916RUK
VTTSNS
VLDOIN
VTT
VTTGND
VTTREF
PwrGd
PGOOD
MODE
TRIP
S3
S5
VBST
DRVH
SW
V5IN
DRVL
VREF
GND
REFIN
VDDQSNS
PGND
Q10
CSD87350Q5D
R154
2.21
TP75
Q_SW
L7
1.0uH
TP76
VDDQ
C167
R155
C169
TP77
GND
C168
330uF
TP78
Q_DL
R156
0
C170
2.2uF
C171
0.22uF
TP79
Q_VREF
C172
0.1uF
R157
0
R158
10.0k
VDDQ_VSNS
R160
20.0k
C184
1nF
VDDQ_GSNS
R159
0
R161
0
J20
J19
VDDQ Output
1.2VDDQ/0A-8A
C178
C173
10uF
C179
C174
10uF
C180
C175
10uF
C181
C176
10uF
C182
C177
C183
Note7:
Not used
S3/S5 Enable Control, See datasheet for detail
VDDQ Power


VBAT Conversion Voltage Input:
9V -20V
TP82
VBAT
J21
C187
C186
TP84
GND
TP81
5VIN
TP83
GND
C188
0.1uF
C189
10uF
R162
100k
U7
TPS70102PWP
1.8V LDO
3.3V LDO
NC
VIN1
VIN1
MR2
MR1
ENABLE
SEQUENCE
GND
VIN2
VIN2
PwrPad
VOUT1
VOUT1
VSENSE1
PGD_1
RESET
VSENSE2
VOUT2
VOUT2
NC
TP80
1.8V
R163
15.0k
R165
30.1k
R166
30.1k
R167
51.1k
C185
10uF
R164
2.00k
C190
0.1uF
TP85
3.3V
C191
10uF
R168
1
3.3V_CG
TP87
5V_IO
TP86
5V_Q
TP88
5V_CG
5V_VCCIO
5V_VDDQ
5V_CGPU
R169
R170
R171
J22
5VIN
Note8:
Not used
VCCIO, GPU and CPU Dynamic Load:
1. Switch to "ON" position to enable the Dynamic Load
2. Switch to "OFF" position to disable the Dynamic Load (Default)
J23: Default setting: Jumper shorts on to
Enable on board dynamic load
1.2V LDO
U8
TPS71712DCK
IN
GND
EN
OUT
NR/FB
150mA LDO
TP89
1.2V
C192
0.1uF
C193
2.2 uF
C194
0.01uF
VCORE
R172
0.01
R173
0.01
R174
0.05
R175
0.05
5V Bias
Voltage Input
Silk:
VCCIO_DL
GFX_DL
CPU_DL1
CPU_DL2
R176
10.0k
S2
S3
ON
OFF
TP90
DL_CLK
U9:A
U9:B
U9:C
U9:D
SN74HC08D
GND_PWR
U10
UCC27324D
U11
UCC27324D
NC
INA
GND
INB
OUTA
VDD
OUTB
C196
1uF
C202
1uF
R182
8.06k
R183
10.0k
R184
100k
D6
BAT54
R185
10.0k
U12
TLC555CD
VCC
RESET
DISCH
THRES
TRIG
GND
OUT
CONT
J23
C197
0.01uF
C201
0.1uF
C198
0.1uF
C199
0.1uF
VCCIO
G_VCORE
R177
0.05
R179
0.05
R178
0.01
R180
0.05
Q11
CSD16407Q5
Q12
CSD16407Q5
Q13
CSD16407Q5
Q14
CSD16407Q5
TP91
DYN_C
TP92
GND
C195
1uF
R181
0.005
D4
RED
D5
RED
D7
RED
D8
RED
R186
330
R187
330
R188
330
R190
330
TP93
DYN_G_IO
TP94
GND
C200
1uF
R189
0.005
DYNAMIC LOADs


TP95
VR_ON
R191
R192
100
5VIN
1.2V
OFF
ON
S4
C204
1nF
J30
Jumper to enter
I2C Mode
3.3V
SLEWA
VREF
U14:D
TLV3404PW
R205
10.0k
U13
TS5A23157DGS
IN1
NO1
GND
NO2
IN2
COM1
NC1
V+
NC2
COM2
CF-IMAX
CF-IMAX_1
GF-IMAX_1
GF-IMAX
C203
0.1uF
R211
3.01k
R210
3.01k
J32
I2C Terminal
C205
10pF
C206
10pF
J24
R193
R195
R196
R197
R198
R199
1M
L1N
L1CP
L2N
L2CP
L3N
L3CP
VBAT
R194
10.0k
R200
R201
0
VSS_SENSE
VCC_SENSE
J31
R202
10.0k
R203
R204
R206
R207
G_LN2
G_LCP2
G_LN1
G_LCP1
VREF
R208
R209
VSSGT_SENSE
VCCGT_SENSE
J24, J31 are labview connections
for EVM testing
J25
J26
J27
J28
J29
Note9:
Not used
S4: IMVP-7 VR Enable:
1. Switch to "ON" position to Enable TPS59650 controller
2. Switch to "OFF" position to Disable TPS59650 controller(Default)
Default Trim: R117 = Not used, R116 = 1.00k
Logic Signal Termination and Status LED's
LED is ON when the logic signal is in the ACTIVE state
TP96
VR_HOT
R212
330
R213
1.00k
1.2V
ØR6VREF
C207
0.1uF
U14:A
TLV3404PW
R214
10.0k
Q15
BSS83P
U14:B
TLV3404PW
R218
1.00k
C208
1uF
R215
180
R216
180
R217
180
R220
10.0k
R221
10.0k
R222
180
VR_ON
C_PGOOD
G_PGOOD
VR_HOT
D9
GREEN
D10
GREEN
D12
GREEN
D11
RED
TP98
CPGOOD
TP97
GPGOOD
Q16
BSS123
Q17
BSS123
Q18
BSS123
R219
10.0k
U14:C
TLV3404PW
Support and Pull-ups


XU1:A
989-1MM_IMVP7-REV1_5
VCORE
XU1:B
989-1MM_IMVP7-REV1_5
VDDQ
VCCIO
G_VCORE
XU1:C
989-1MM_IMVP7-REV1_5
XU1:D
989-1MM_IMVP7-REV1_5
XU1:E
989-1MM_IMVP7-REV1_5
1.2V
R223
R224
75.0
R225
130
R226
43.2
XU1:F
989-1MM_IMVP7-REV1_5
VCC_SENSE
VSS_SENSE
VCCGT_SENSE
VSSGT_SENSE
VCCP_SENSE
VSSP_SENSE
VIDSCLK
VIDALERT_N
VIDSOUT
PROCHOT_N
VCLK
ALERT
VDIO
VR_HOT
NC1
NC2
NC3
Note10:
Not used
uC Socket Main

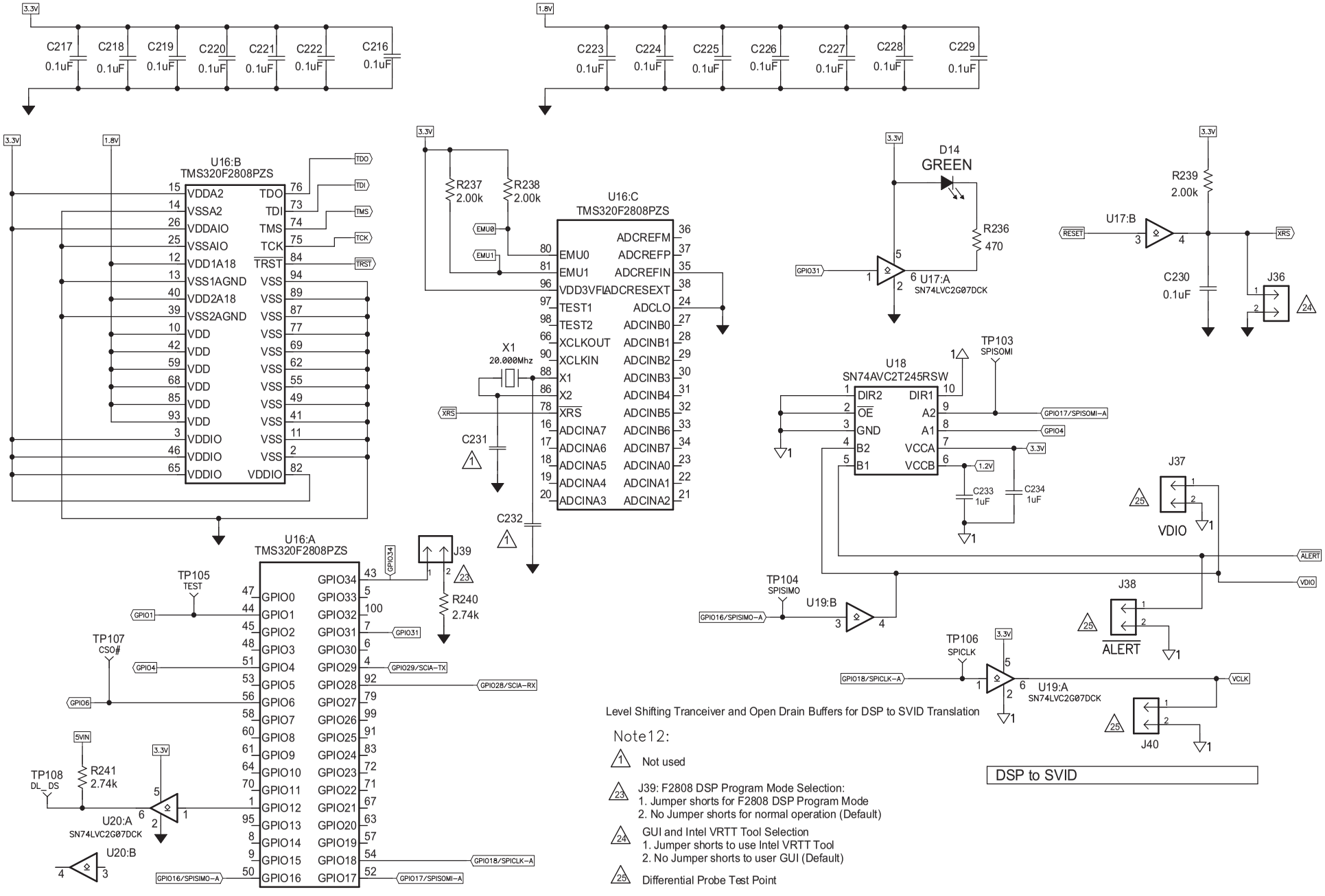

XU11:G
XU11:H
XU11:I
XU11:J
XU11:K
989-1MM_IMVP7-REV1
RSVD
uC Socket Others

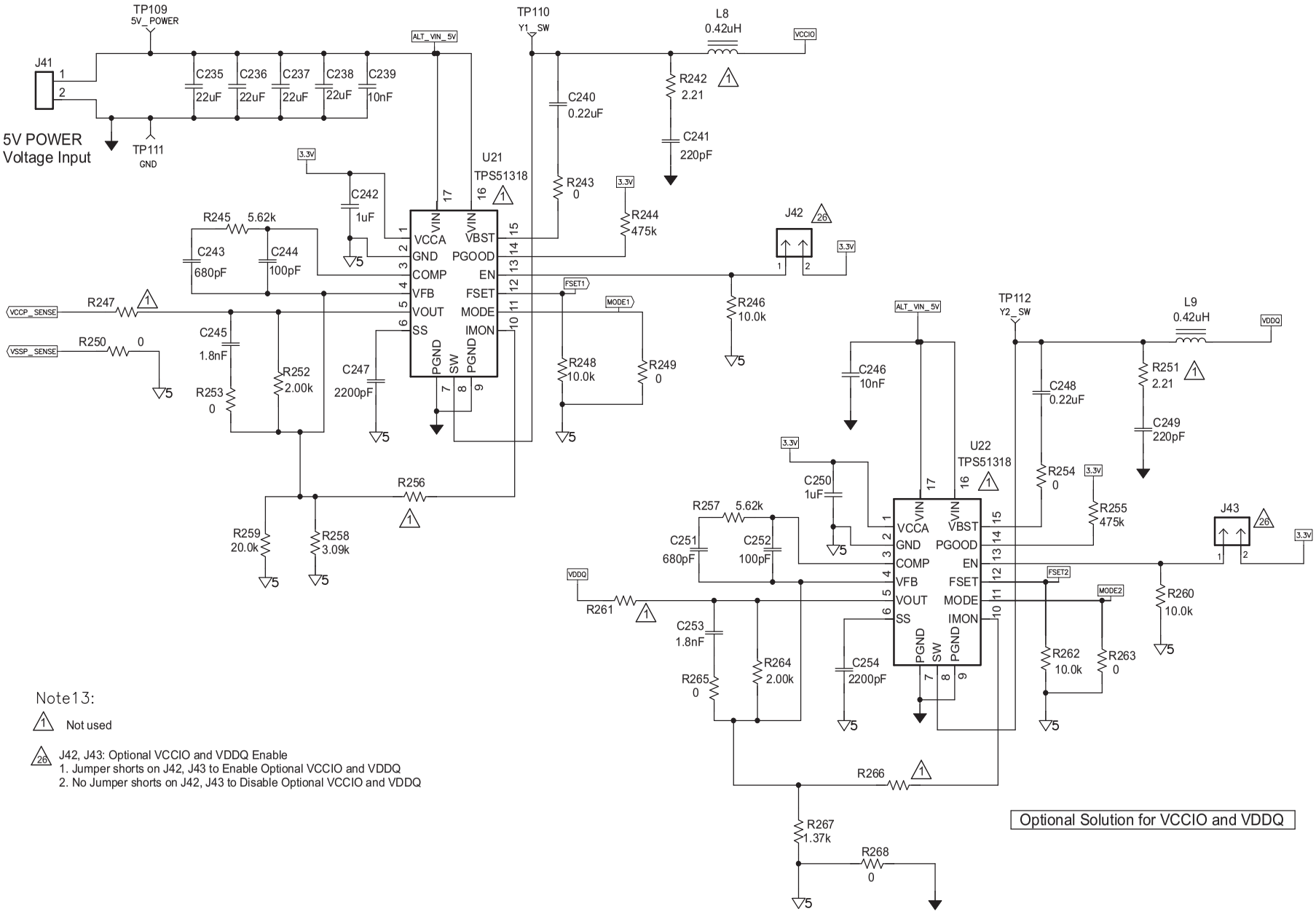


Note11:

1. Not used
2. 5V Bias option:
   1. Jumper shorts on J33, 5V Bias used from USB. If USB 5V is used, external 5V supply from J22 should not be used.
   2. No Jumper shorts on J33, 5V Bias used from external J22 (Default)
3. For Internal software developmenet

USB to DSP


C217 0.1uF
C218 0.1uF
C219 0.1uF
C220 0.1uF
C221 0.1uF
C222 0.1uF
C216 0.1uF
C223 0.1uF
C224 0.1uF
C225 0.1uF
C226 0.1uF
C227 0.1uF
C228 0.1uF
C229 0.1uF
U16:B TMS320F2808PZS
U16:C TMS320F2808PZS
U16:A TMS320F2808PZS
R237 2.00k
R238 2.00k
X1 20.000Mhz
C231
C232
D14 GREEN
R236 470
U17:A SN74LVC2G07DCK
R239 2.00k
U17:B
C230 0.1uF
J36
U18 SN74AVC2T245RSW
TP103 SPISOMI
C233 1uF
C234 1uF
J37 VDIO
TP104 SPISIMO
U19:B
J38 ALERT
TP106 SPICLK
U19:A SN74LVC2G07DCK
J40
TP105 TEST
TP107 CS0#
J39
R240 2.74k
TP108 DL_DS
R241 2.74k
U20:A SN74LVC2G07DCK
U20:B
Level Shifting Tranceiver and Open Drain Buffers for DSP to SVID Translation
Note12:
1 Not used
23 J39: F2808 DSP Program Mode Selection:
1. Jumper shorts for F2808 DSP Program Mode
2. No Jumper shorts for normal operation (Default)
24 GUI and Intel VRTT Tool Selection
1. Jumper shorts to use Intel VRTT Tool
2. No Jumper shorts to user GUI (Default)
25 Differential Probe Test Point
DSP to SVID


TP109
5V_POWER
J41
C235 22uF
C236 22uF
C237 22uF
C238 22uF
C239 10nF
5V POWER
Voltage Input
TP111
GND
ALT_VIN_5V
TP110
Y1_SW
L8
0.42uH
VCCIO
R242 2.21
C240 0.22uF
C241 220pF
U21
TPS51318
C242 1uF
R243 0
R244 475k
R245 5.62k
C243 680pF
C244 100pF
J42
VCCP_SENSE
R247
VSSP_SENSE
R250 0
C245 1.8nF
R252 2.00k
R253 0
C247 2200pF
R246 10.0k
R248 10.0k
R249 0
FSET1
MODE1
R256
R259 20.0k
R258 3.09k
TP112
Y2_SW
L9
0.42uH
VDDQ
C246 10nF
C248 0.22uF
R251 2.21
C249 220pF
U22
TPS51318
C250 1uF
R254 0
R255 475k
R257 5.62k
C251 680pF
C252 100pF
J43
R260 10.0k
R261
C253 1.8nF
R264 2.00k
R265 0
C254 2200pF
R262 10.0k
R263 0
FSET2
MODE2
R266
R267 1.37k
R268 0
Optional Solution for VCCIO and VDDQ
Note13:
1 Not used
26 J42, J43: Optional VCCIO and VDDQ Enable
1. Jumper shorts on J42, J43 to Enable Optional VCCIO and VDDQ
2. No Jumper shorts on J42, J43 to Disable Optional VCCIO and VDDQ

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjukku-ku, Tokyo, Japan

http://www.tij.co.jp

【ご使用にあたっての注】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

【ご使用にあたっての注】

本開発キットは技術基準適合証明を受けておりません。

本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

EVALUATION BOARD/KIT/MODULE (EVM)
WARNINGS, RESTRICTIONS AND DISCLAIMERS

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265