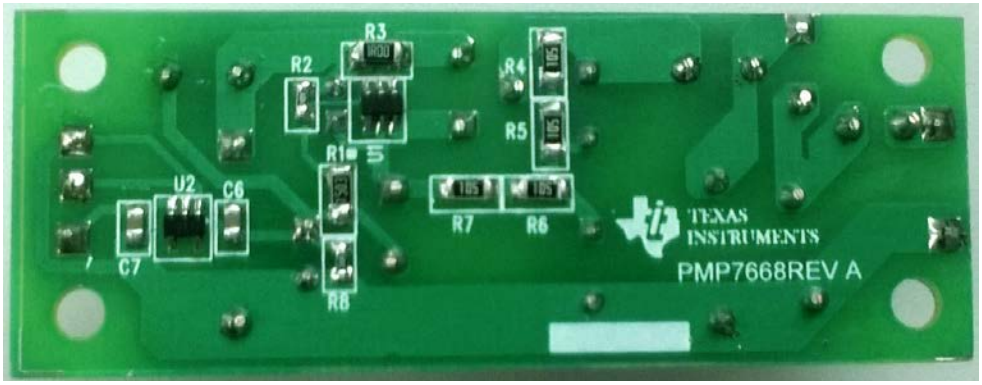
Test Report of 2W Wide Input Buck Bias Supply

PMP7668



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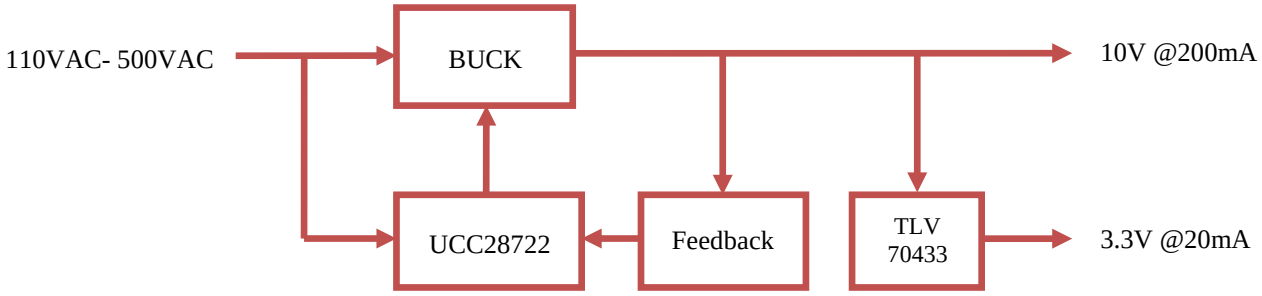
I. INTRODUCTION

The following document is a compilation of test results of the PMP7668 reference design, a 2W bias supply using UCC28722 in buck configuration. The test results are taken over an input voltage range of 80V – 275V AC and 400V – 705V DC, driving a load up to 200mA.

II. DESCRIPTION

The PMP7668 is developed with the UCC28722 controller IC. The design is targeted for small form factor (69mm x 26mm) bias power solutions, especially for applications like e-metering. The differentiating feature of this design is its ability to operate over a wide input range (110 – 500VAC). It can work down to 80VAC with reduced output current. The design has an operating efficiency of around 70% at full load, with a voltage regulation of +/- 1%. Regulation, efficiency, output ripple, startup and switching stress of the design were tested under various conditions and are documented in this report. The circuit has an optional 3.3V output also.

III. BLOCK DIAGRAM



IV. SPECIFICATIONS

Input Voltage Range: 110VAC - 500VAC
Output Voltage: 10V +/- 1V
Output Current: 200mA
Board Form Factor: 69mm x 26mm
Expected efficiency: >65%

V. TEST SETUP

Input conditions:
Vin: 80 – 275 VAC, 400 – 705 VDC
Set Input current limit to 0.2A

Output:
Variable resistive load to 200mA

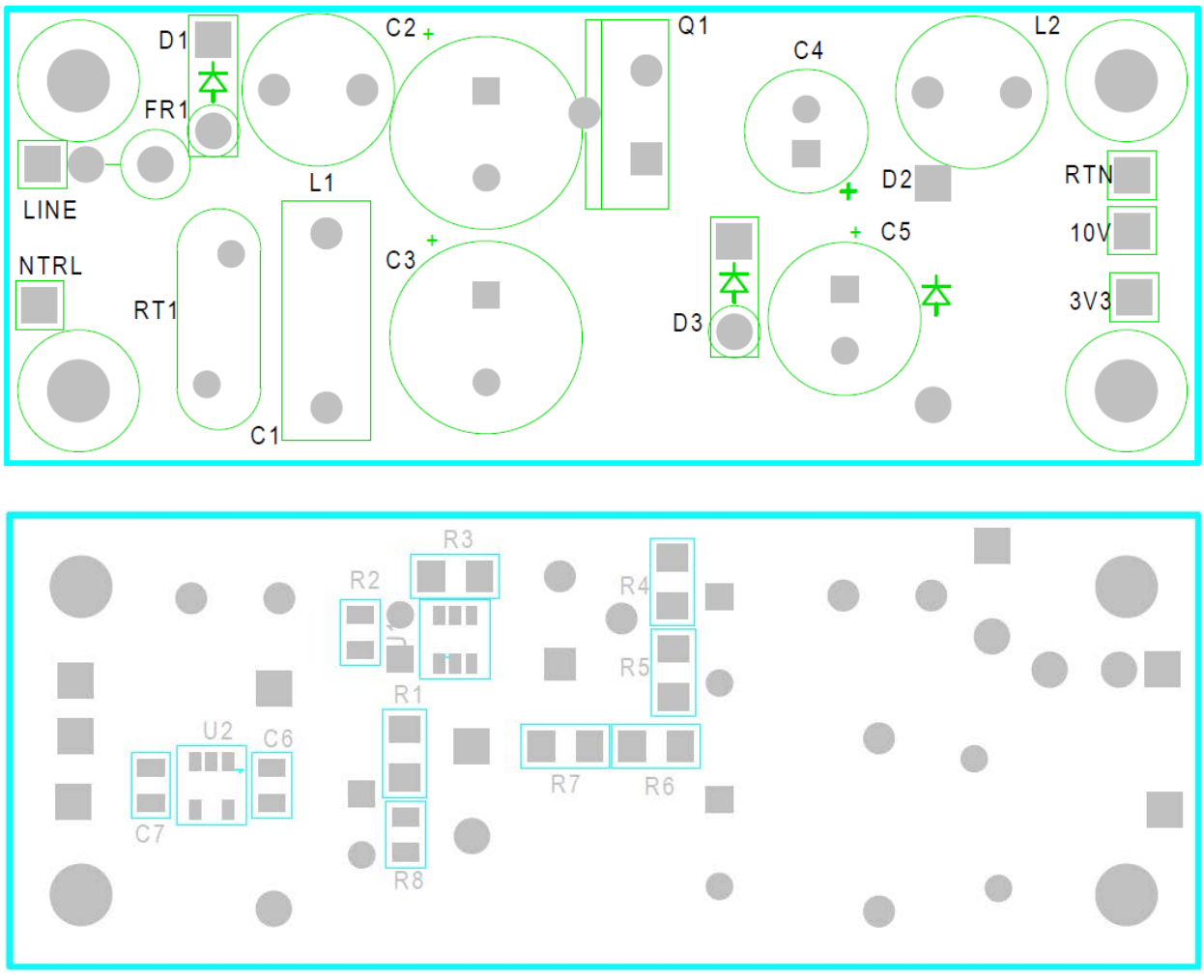
Equipment Used:

1. Isolated AC Source
2. High voltage DC source
3. Digital Oscilloscope
4. Multimeters
5. Electronic load

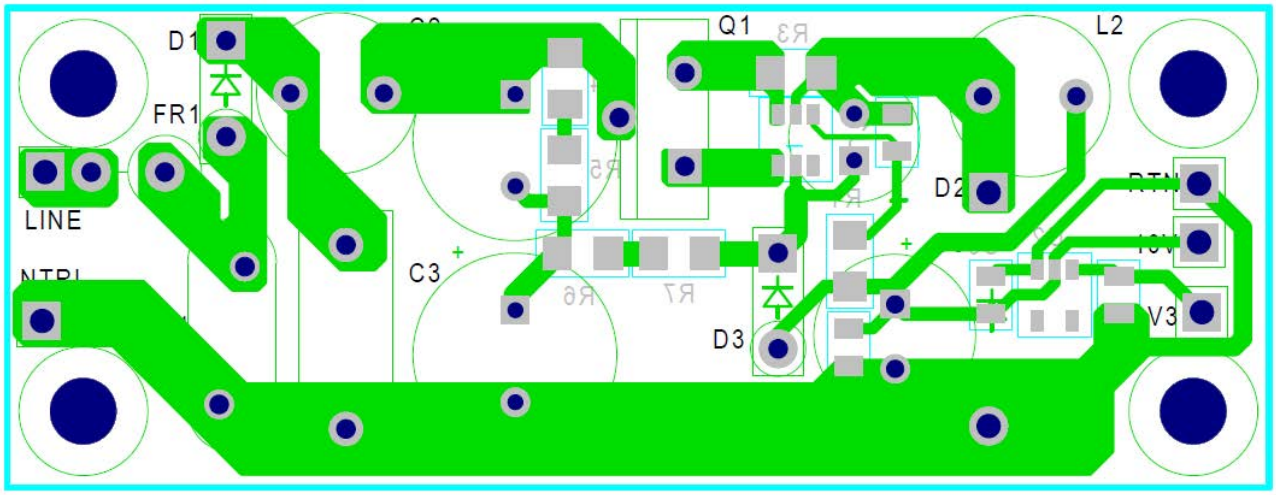
Procedure:

1. Connect input terminals of the PMP7668 reference board to the AC/DC Power Source.
2. Connect output terminals to electronic load, maintaining correct polarity.
3. Maintain minimum load of about 2mA.
4. Gradually increase the input voltage from 0V to turn on voltage of 80VAC.
5. Observe the startup conditions for smooth switching waveforms.

VI. BOARD ASSEMBLY DRAWINGS



VII. LAYOUT



VIII. EFFICIENCY AND REGULATION

a. Performance Data

AC Efficiency

Vin (VAC)	Pin (W)	VA	Vo (V)	Io (mA)	Po (W)	Efficiency (%)
80	1.29	2.77	9.51	100	0.95	73.5
100	2.01	4.29	9.52	150	1.43	71.0
110	2.84	6.04	9.53	200	1.91	67.2
130	2.77	6.03	9.53	200	1.91	68.7
150	2.73	6.24	9.53	200	1.91	69.9
170	2.70	6.51	9.53	200	1.91	70.5
190	2.69	6.80	9.53	200	1.91	70.9
210	2.68	7.09	9.53	200	1.91	71.0
230	2.68	7.37	9.53	200	1.91	71.0
250	2.68	7.64	9.53	200	1.91	71.0
275	2.69	7.95	9.53	200	1.91	70.8

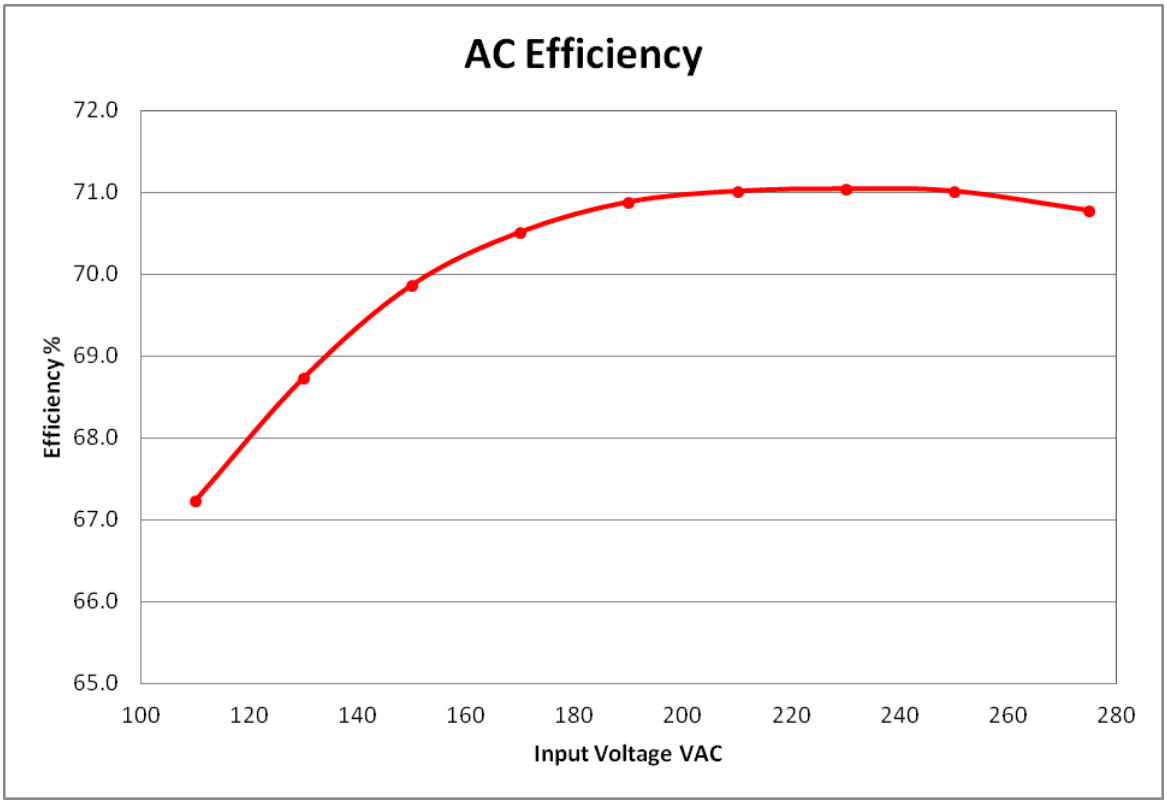
DC Efficiency

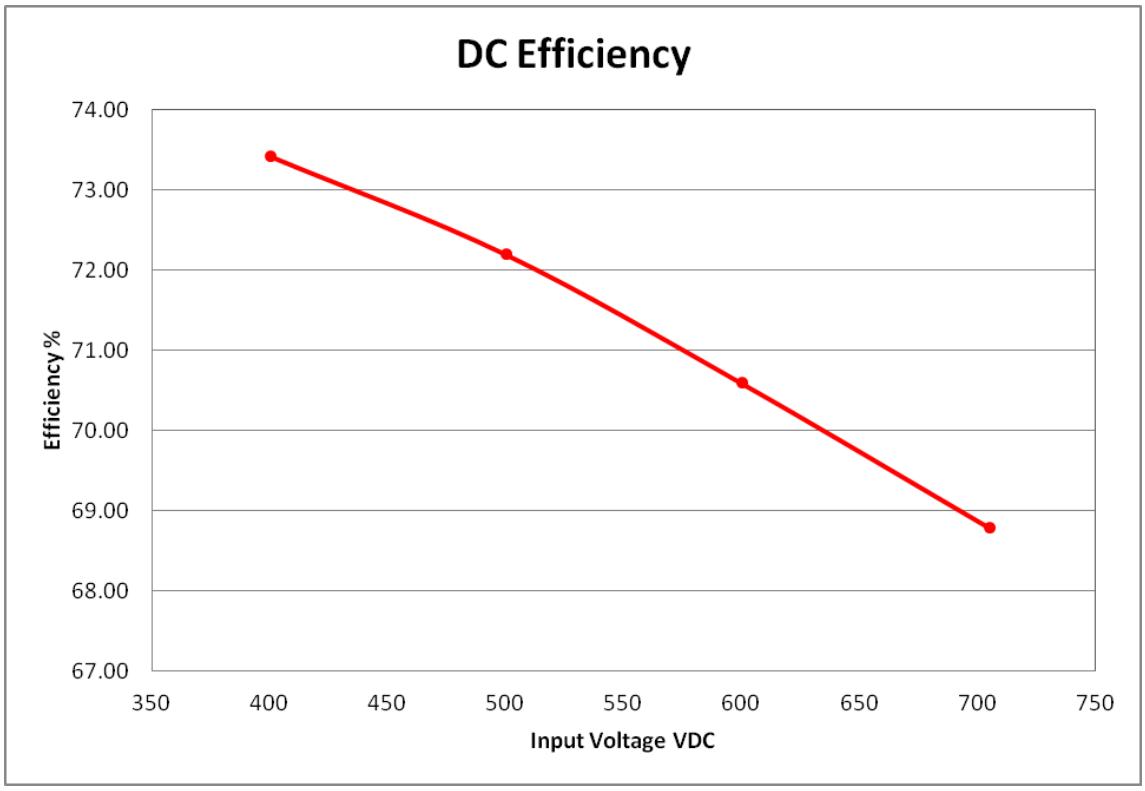
Vin (VDC)	Iin (mA)	Pin (W)	Vo (V)	Io (mA)	Po (W)	Efficiency (%)
400	6.49	2.60	9.53	200	1.91	73.42
500	5.28	2.64	9.53	200	1.91	72.20
600	4.50	2.70	9.53	200	1.91	70.59
705	3.93	2.77	9.53	200	1.91	68.79

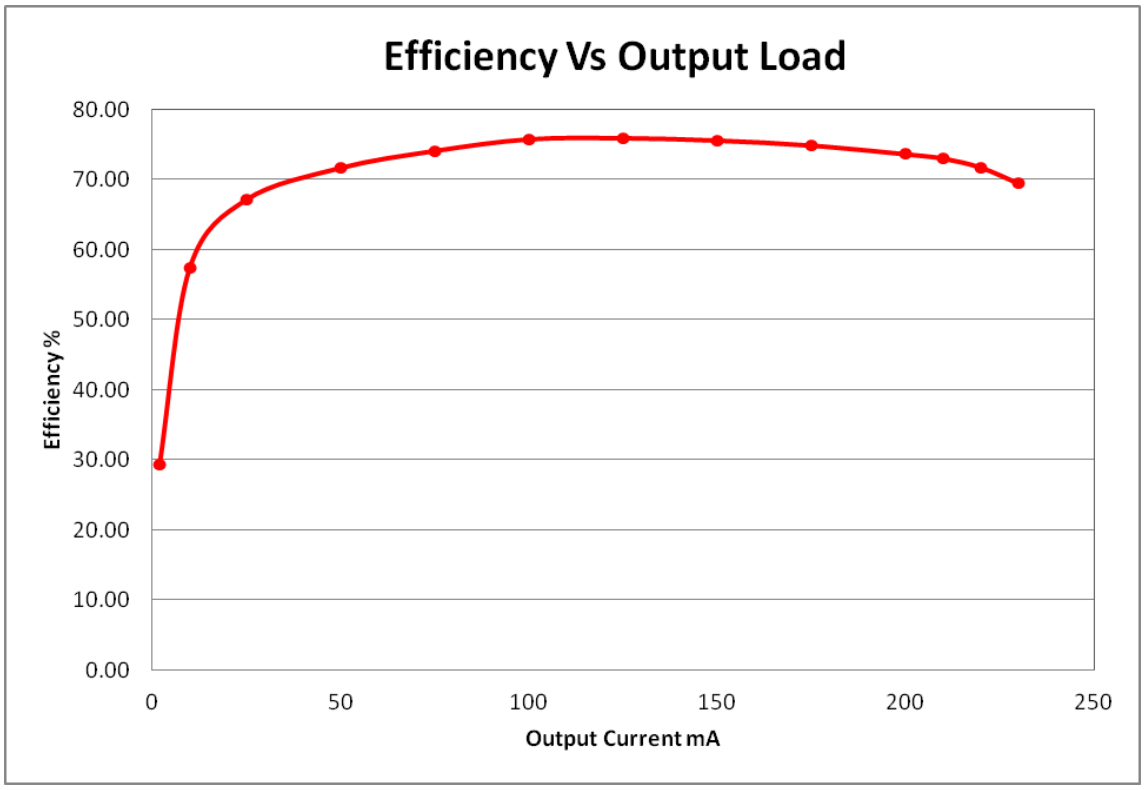
Regulation and Efficiency with output load

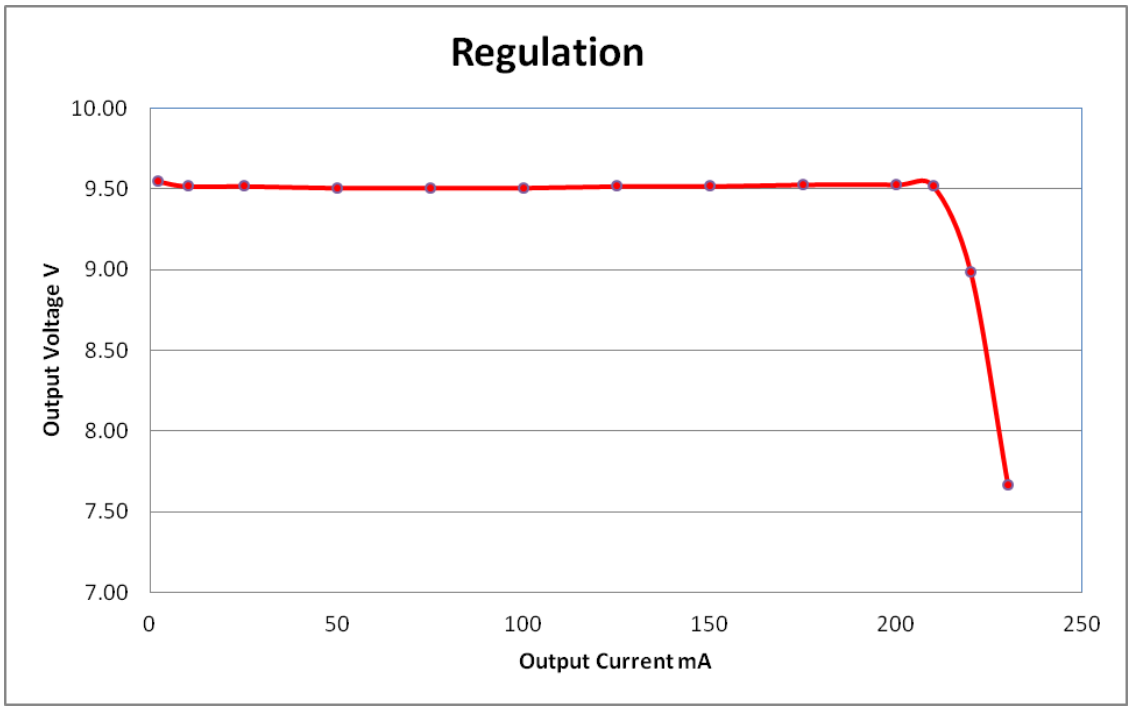
Vin (VDC)	Iin (mA)	Pin (W)	Vo (V)	Io (mA)	Po (W)	Efficiency (%)
325	0.20	0.07	9.55	2	0.02	29.38
325	0.51	0.17	9.52	10	0.10	57.44
325	1.09	0.35	9.52	25	0.24	67.18
325	2.04	0.66	9.51	50	0.48	71.72
325	2.96	0.96	9.51	75	0.71	74.14
325	3.86	1.25	9.51	100	0.95	75.81
325	4.82	1.57	9.52	125	1.19	75.97
325	5.81	1.89	9.52	150	1.43	75.63
325	6.85	2.23	9.53	175	1.67	74.91
325	7.96	2.59	9.53	200	1.91	73.68
325	8.42	2.74	9.52	210	2.00	73.06
325	8.48	2.76	8.99	220	1.98	71.76
325	7.81	2.54	7.67	230	1.76	69.50

b. Plots




DC Efficiency
74.00
73.00
72.00
71.00
70.00
69.00
68.00
67.00
Efficiency %
350
400
450
500
550
600
650
700
750
Input Voltage VDC

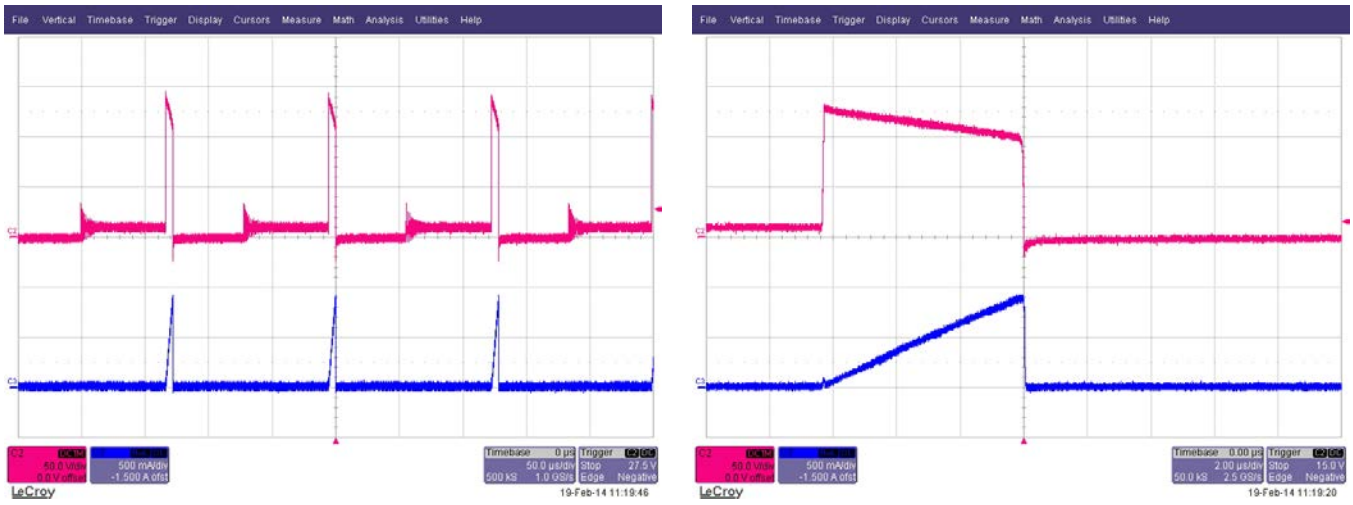

Efficiency Vs Output Load
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
Efficiency %
0
50
100
150
200
250
Output Current mA



IX. WAVEFORMS

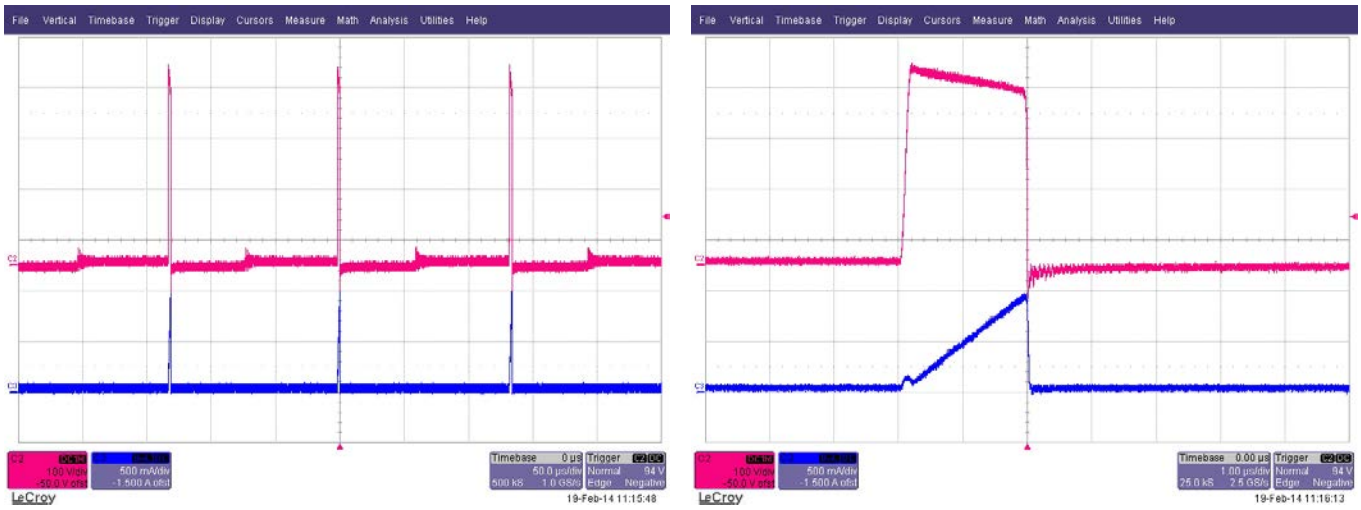
a. Switching Node Waveforms

Vin = 110VAC, Full Load



Red trace: Drain voltage, 50V/div; Blue trace: Drain current, 500mA/div

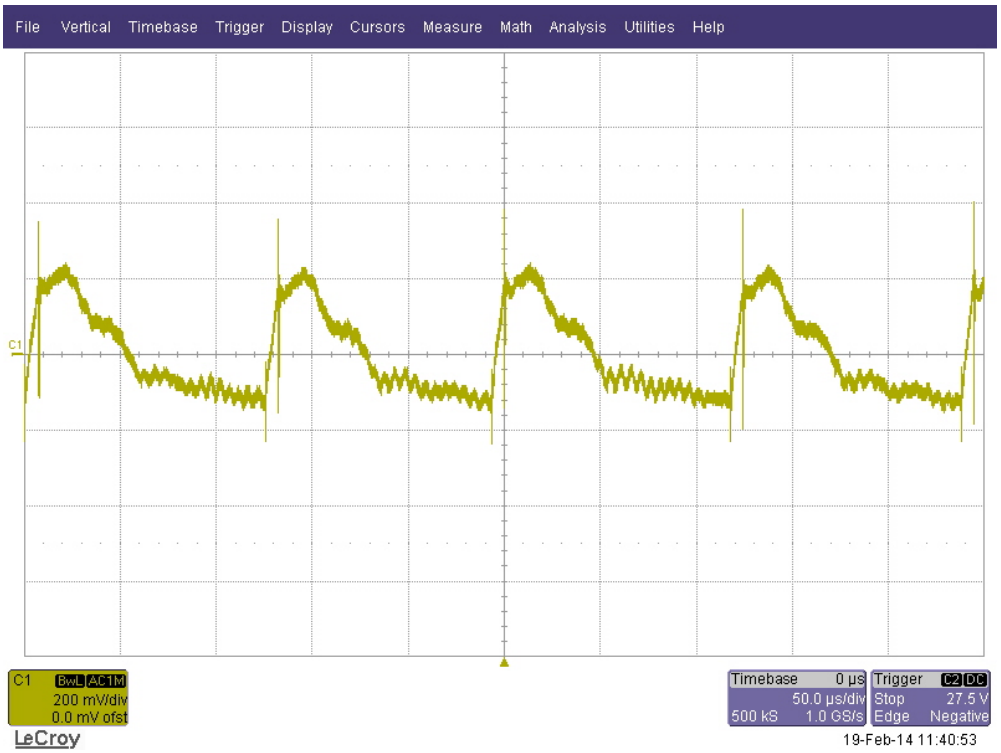
Vin = 275VAC, Full Load



Red trace: Drain voltage, 100V/div; Blue trace: Drain current, 500mA/div

b. Output Ripple

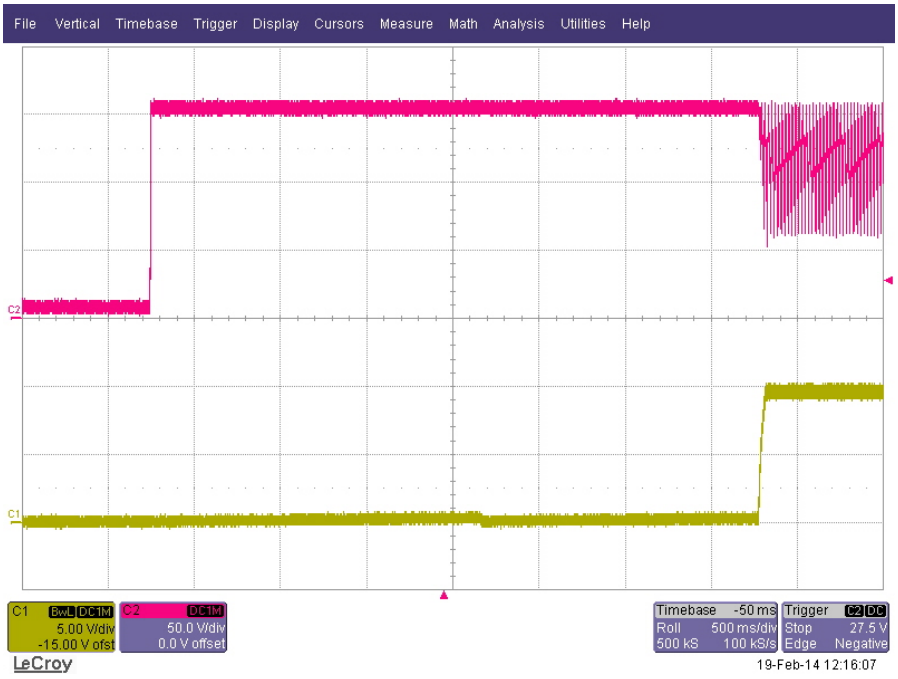
Vin = 110VAC, Full Load



Vin = 275VAC, Full Load

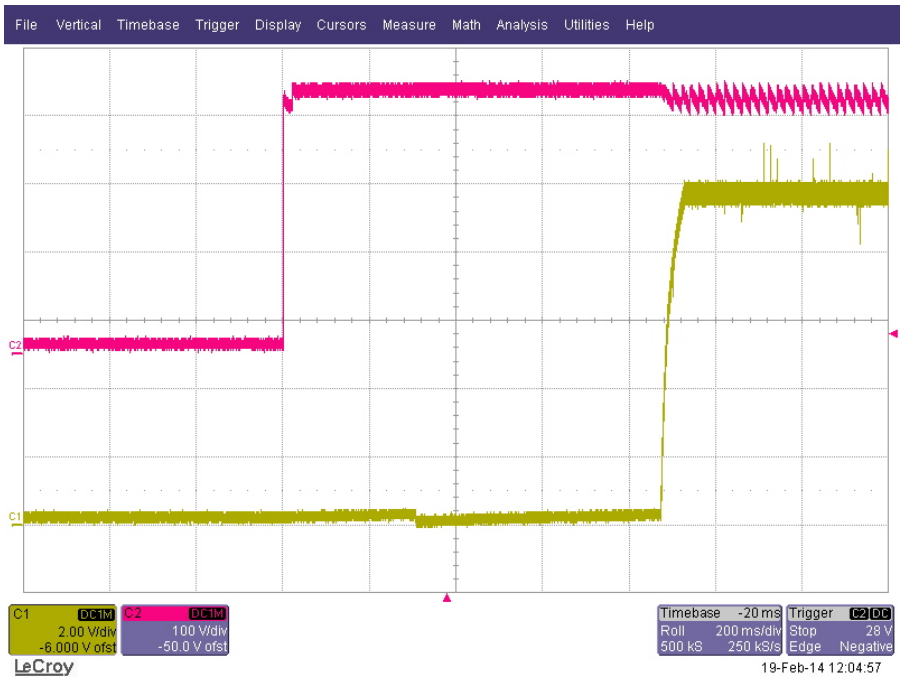
c. Turn On Characteristics

Vin = 110VAC, Full Load



Red trace: Input DC bus, 50V/div; Yellow trace: Output voltage, 5V/div

Vin = 275VAC, Full Load



Red trace: Input DC bus, 100V/div; Yellow trace: Output voltage, 2V/div

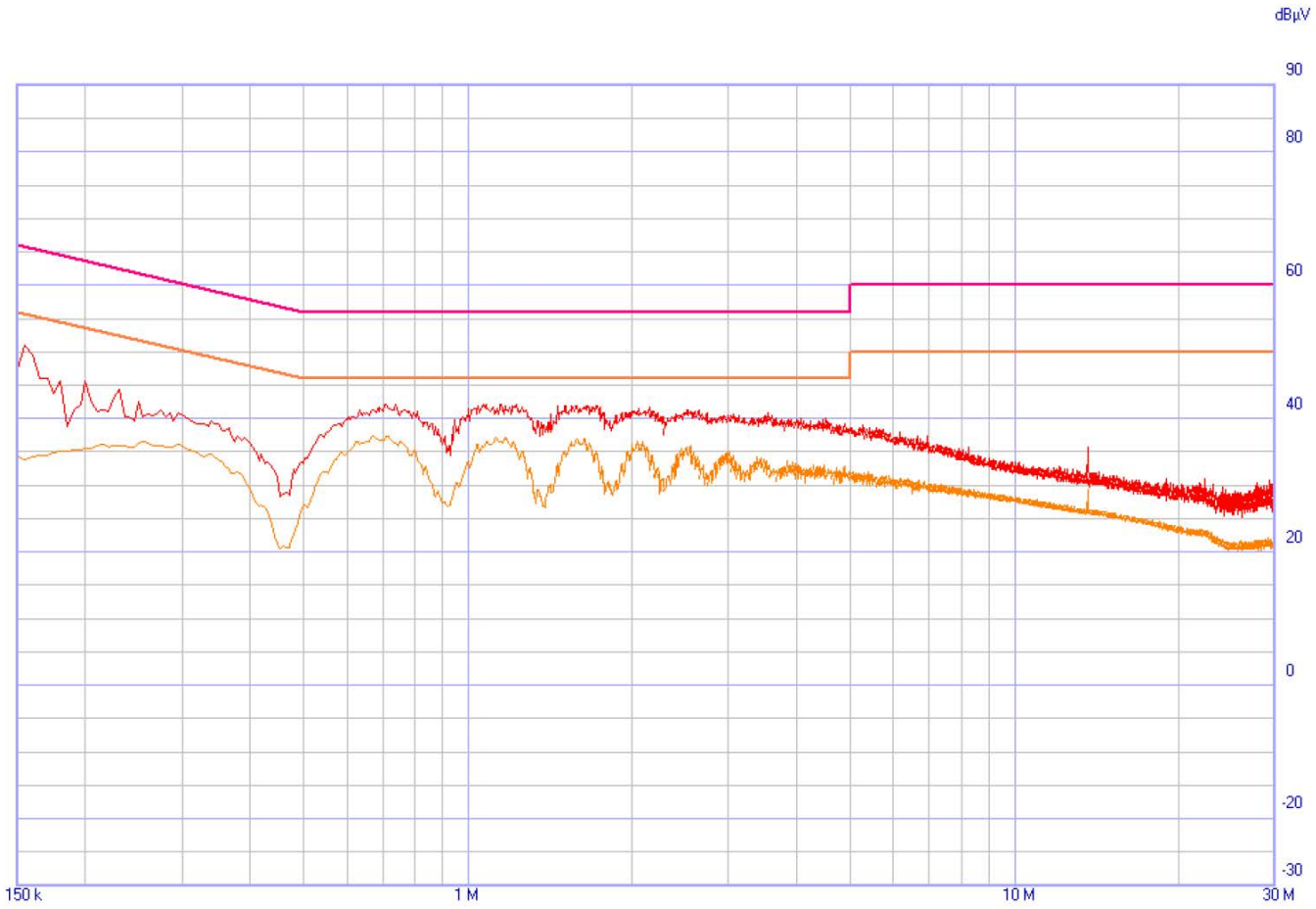
d. Transient response

Vin = 230VAC, Load transient from 2mA to 200mA

X. CONDUCTED EMISSIONS

230VAC Input, 200mA resistive load connected to PSU with short leads.

The conducted emissions in a pre-compliance test set-up were compared against EN55022 class B limits and found to be meeting them comfortably.



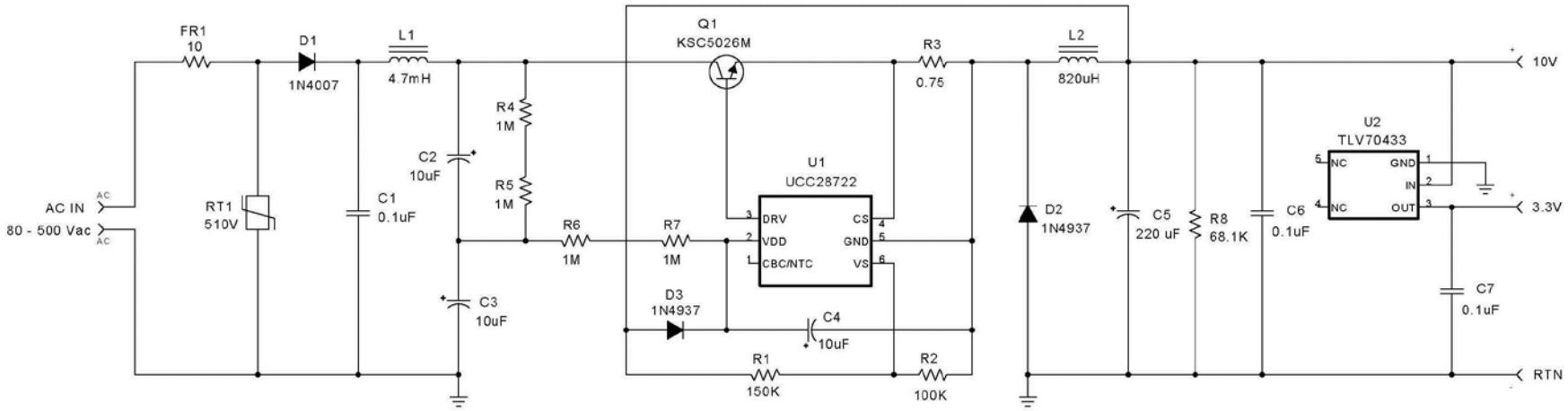
	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	0.15	30	AUTO (5 kHz)	P A 55022bqp 55022bav	15 ms	9 kHz	10	OFF	OFF	...	L1, L2

Pulse Limiter ON
Ancillary = L2 7010

Factors:
ambient-fac150kh-1mhz
ambient-fac150kh-1mhz

Peak
Avg

XI. SCHEMATIC



Schematic for PMP7668 Reference Design

XII. BILL OF MATERIALS

PMP7668 BOM Revision B							
Item	Qty	Reference	Value	Description	Part Number	Manufacturer	Size
1	1	C1	0.1uF	Capacitor, Leaded, 760 VDC, ±10%	PHE840MA6100KA04R17	Kemet	0.157 x 0.512 inch
2	2	C2, C3	10uF	Capacitor, Alum Electrolytic 400V, ±20%	UCA2G100MPD1TD	Nichicon	10.00 mm Dia
3	1	C4	10uF	Capacitor, Alum Elect, 25V, ±20%	Std	Std	5 x 11 mm
4	1	C5	220 uF	Capacitor, Alum Electrolytic, 25V, ±20%	25YXG220MEFC8X11.5	Rubycon	8 x 11.5 mm
5	2	C6, C7	0.1uF	Capacitor, Ceramic Chip, X7R, 50V, ±10%	Std	Std	805
6	1	D1	1N4007	Diode, Rectifier, 1000V, 1A	1N4007	Diodes	DO-41
7	2	D2, D3	1N4937	Diode, Fast, 600V, 1A	1N4937	Fairchild	DO-41
8	1	FR1	10	Fusible resistor, 0.5W	NFR25H0001009J	Vishay	2.5 x 7.5 mm
9	1	L1	4.7mH	Inductor, 150mA, 25ohm	744741472	Wurth Elektronik	8.5 x 5.5mm
10	1	L2	820uH	Inductor, 0.7A, 1.56ohm	7447728215	Wurth Elektronik	7.8 x 9.5mm
11	1	Q1	KSC5026M	Trans, NPN Medium Power, 800V, 1.5A	KSC5026MOS	Fairchild	TO-126
12	1	R1	150K	Resistor, Chip, 1/4W, 1%	Std	Std	1206
13	1	R2	100K	Resistor, Chip, 1/8W, 1%	Std	Std	805
14	1	R3	0.75	Resistor, Chip, 1/2W, 5%	CRL1206-FW-R750ELF	Bourns	1206
15	4	R4, R5, R6, R7	1M	Resistor, Chip, 1/4W, 5%	Std	Std	1206
16	1	R8	68.1K	Resistor, Chip, 1/8W, 1%	Std	Std	805
17	1	RT1	510V	MOV, 510VAC	MOV-10D821KTR	Bourns	10mm dia
18	1	U1	UCC28722	IC, CV/CC PWM With Primary Side Regulation	UCC28722DBV	TI	SOT-23
19	1	U2	TLV70433	IC, 24-V Input, 150 mA, Utralow IQ LDO Regulator	TLV70433DBV	TI	SOT-23

XIII. CONCLUSION

The board is tested against the specifications given in section IV and found to meet them including an overall efficiency of >65% and a board form factor of <1800mm^2. Also, the emission test performed in section X shows that this reference design is in compliance with EN55022 class B limits.

XIV. APPENDIX

EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

For Feasibility Evaluation Only, in Laboratory/Development Environments. The EVM is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.

Certain Instructions. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output ranges are maintained at nominal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be indentified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

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