TI Designs

Small Form Factor, 2-Wire, 4- to 20-mA Current-Loop, RTD Temperature Transmitter

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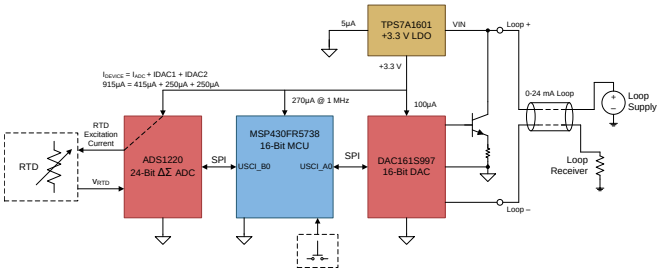
TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00165	Tool Folder Containing Design Files
ADS1220IRVA	Product Folder
DAC161S997RGH	Product Folder
MSP430FR5738IRGE	Product Folder
TPS7A1601DRB	Product Folder



Design Features

- Small Form Factor (L × W): 71.12 mm × 6 mm
- Sensor Input Compatible with 2-, 3- or 4-Wire Resistance Temperature Detector (RTD) Probes
- Connects to any RTD from PT100 to PT1000
- RTD Temperature Range -200°C to 850°C
- Output resolution: 0.76 µA
- Input Power Supply Range: 10-V to 33-V DC
- 4- to 20-mA Current-Loop Output Signal
- Maximum Measured Error: 0.2°C
- Implements Ratiometric Measurement
- Designed to Meet IEC 61000 Requirements
- Operating Temperature Range -40°C to 85°C

Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instruments

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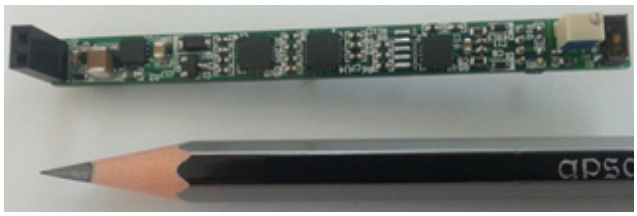

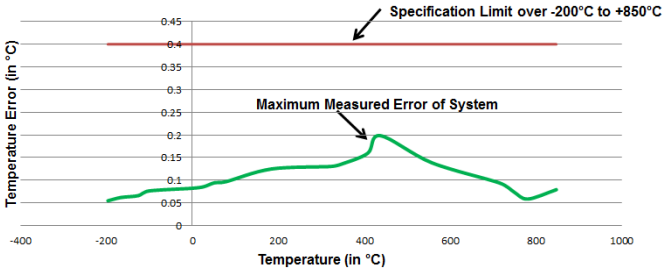

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1 Introduction

The sole objective of this reference design is to focus on the design of a robust, low-power, precise, long-term stable, 2-wire, loop-powered, 4- to 20-mA current-output temperature transmitter by making best use of signal chain, power and computing solutions. This reference design uses a RTD-temperature sensor with a 4- to 20-mA current-loop transmitter.

This design explains sensor signal conditioning, ratiometric measurement technique, recommended software flow, calibration, sensor linearization, printed circuit board (PCB) layout, and other practical design considerations. Furthermore, external-protection circuitry is deployed in-place for compliance with regulatory IEC61000-4 standards — electrical fast transient (EFT), electrostatic discharge (ESD), and electrical surge requirements. Electromagnetic compatibility (EMC) compliance to IEC61000-4 is necessary to ensure that the design not only survives but also performs as intended in a harsh and noisy industrial environment. All the relevant design files such as schematics, Bill of Materials (BOM), layer plots, Altium files, Gerber files, and MSP430 microcontroller unit (MCU) software are provided.

2 Key System Specifications

The reference design targets the specifications and features shown in Table 1.

Table 1. Key System Specifications

PARAMETERS	SPECIFICATIONS AND FEATURES
Sensor type	2-, 3-, and 4-wire PT100 to PT1000 RTD probes (The MCU software developed supports PT100 RTD by default)
Temperature range	-200°C to 850°C
Output signal	2-wire 4- to 20-mA current loop
Measurement type	Ratiometric
Power supply voltage range on loop interface terminals	10-V to 33-V DC
Supply current consumption	< 3.3 mA (To power all the functional blocks of transmitter)
Maximum load (including wiring resistance)	(Loop Supply Voltage – 10 V)/24 mA
Error output currents	Low: 3.375 mA (typical) High: 21.75 mA (typical)
Reverse polarity protection	Yes, on power input
Temperature resolution	0.0341°C (Noise free or flicker free resolution of analog front end)
Output current resolution	0.76 µA
Power supply influence on output	0.3 µA
System accuracy or maximum measured error (Excluding sensor errors)	Better than 0.2°C (-200°C to 850°C temperature range)
Calibration	Offset and gain calibration for analog-to-digital converter (ADC) and digital-to-analog converter (DAC)
RTD temperature linearization	–200°C to 850°C look-up table with 1°C resolution implemented in the MSP430 firmware to resolve nonlinearity of RTD or the Callendar-Van Dusen relationship between resistance and temperature
Surge transient immunity	IEC 61000-4-5: ±1 kV line-line (DM)
Operating temperature	-40°C to 85°C
Interface connector(s)	Two-pin TH connector for loop interface Four-pin RA TH connector for external RTD sensor probe Four pin RA SMD connector for Spy-bi-wire interface
Form factor (L × W)	71.12 mm × 6 mm

3 System Description

4- to 20-mA current loops are very popular world-wide. 4- to 20-mA current loops are a standard for transmitting remote sensor information to programmable logic controllers over long distances in industrial process monitoring, control, and automation applications.

This reference design uses a very small industrial form factor to provide a low-power, high-performance, and cost-effective 4- to 20-mA, temperature-transmitter solution. Low power consumption is a key requirement for industrial 2-wire sensor transmitters which are powered by loop power supply. To meet these requirements, the selected devices for the signal chain offer most of the functionality integrated on-chip, consume low power, and come in a small foot-print.

The compact sensor transmitters which are available in the market today come with an integrated probe and an industry-standard M12 connector for loop interface. To showcase the suitability of devices with respect to size and performance for such compact designs, a 6-mm wide PCB has been used. The 6-mm wide PCB enables the entire PCB assembly to fit inside a hollow cylindrical housing of similar diameter as the connector. The design also provides the two break-out sections for fast prototyping. Top level hardware architecture is shown in Figure 1, which has major blocks identified as ADC, DAC, MCU and LDO.

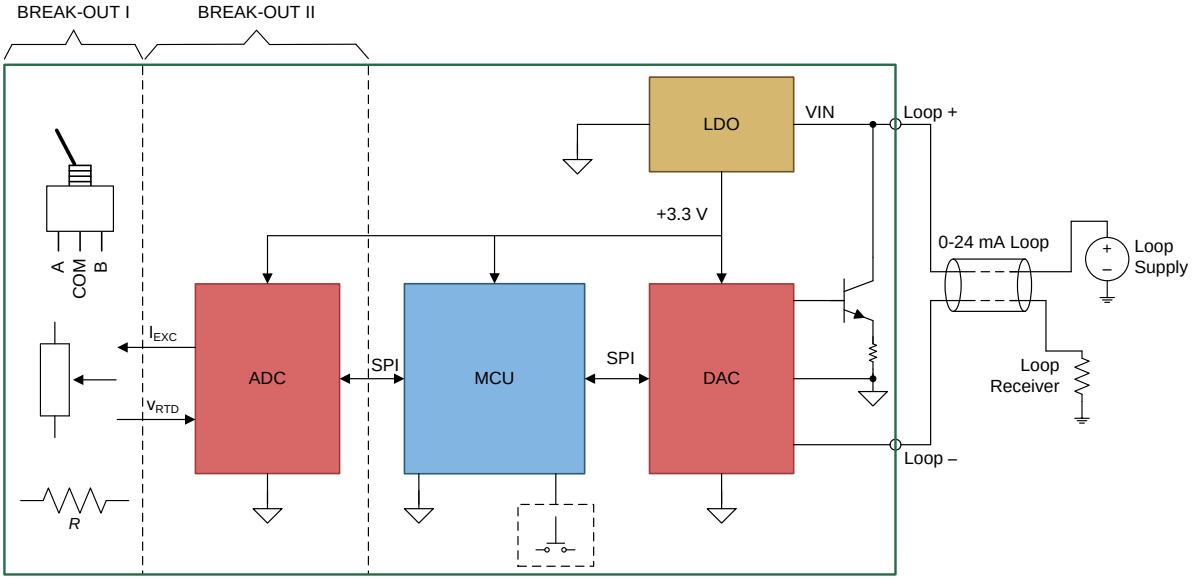


Figure 1. Top Level Hardware Architecture of Current Loop Temperature Transmitter

Before starting the design and layout of the actual system, carefully examine all the captured system requirements and features. Use a top-down approach to translate the design requirements into subsystem level requirements. Some of subsystem level requirements are as follows.

3.1 ADC Requirements

- The ADC should be a single chip sensor analog front-end for DC-sensing application. The intention of this design is to use as few external components as possible around the ADC.
- The ADC should have an integrated, dual-matched, programmable-current source for sensor excitation which can be routed to any of the analog pins through a flexible-input multiplexer. This integration helps in implementing a current-chopping technique in order to compensate for any mismatch that exists between current sources.
- The ADC should have an integrated, low-noise and high-input impedance, programmable-gain amplifier (PGA).
- The ADC should have an integrated 50 Hz or 60 Hz rejection filter in order to attenuate line frequency pick-up by long leads of temperature sensor running in a harsh or noisy factory environment.
- The ADC should have a serial peripheral interface (SPI) as a digital interface to the MCU.
- Target resolution should be 10 times lower than the overall system accuracy of 0.4°C from -200°C to

850°C.

- The ADC should accept external reference voltage for implementing ratiometric measurement.
- From a layout and routing perspective, the ADC should have a small package not exceeding 4.25 mm to fit into a 6-mm wide PCB.
- The ADC should have low current consumption so that additional current is available for the remaining portion of the system. The total current supply drawn by the ADC and other companion devices must stay well within 3.3 mA.

3.2 DAC Requirements

- The DAC should convert the digital code to an equivalent analog output current over a 4- to 20-mA loop.
- The DAC should be a single-chip solution with no precision-external components.
- The DAC should have an SPI as the digital interface to the MCU.
- Target resolution should be 10 times lower than the overall system accuracy of 0.4°C from -200°C to 850°C.
- From a layout and routing perspective, the DAC should have a small package not exceeding 4.25 mm to fit into a 6-mm wide PCB.
- The DAC should have low current consumption so that additional current is available for the remaining portion of the system. The total current supply drawn by the DAC and other companion devices must stay well within 3.3 mA.

3.3 MCU Requirements

- The MCU must have at least one SPI to interface with the ADC and the DAC. Ideally, the MCU should have two SPIs for easy routing as the ADC and the DAC will be placed on the opposite sides of the MCU (there is no other choice).
- The MCU should have enough internal memory to store application software, the entire RTD loop-table, and calibration data.
- The MCU should be capable of performing functions like arithmetic algorithms, gain and offset calibration routines, sensor linearization using look-up tables, and scaling ADC output to DAC input code.
- The MCU must have a small interface for debugging and programming.
- From a layout and routing perspective, the MCU should have a small package not exceeding 4.25 mm to fit into a 6-mm wide PCB.
- The MCU should have low current consumption so that additional current is available for the remaining portion of the system. The total current supply drawn by the MCU and other companion devices must stay well within 3.3 mA.

3.4 LDO Requirements

- The low-dropout (LDO) regulator should have a wide input range not only to withstand, but also to maintain, well regulation during the input voltage transient events.
- The LDO should generate 3.3-V output.
- The LDO should have low noise and low quiescent current.
- The LDO should have a small package with high thermal performance to ensure that the junction temperature stays within safe limits all the time during operation.

4 Component Selection and Block Diagram

4.1 ADC Selection

The delta-sigma ADCs are mainly preferred for measurement of weak and slow analog signals like temperature signals. These temperature signals are not expected to change rapidly and require a high signal-to-noise-ratio (SNR) and wide dynamic range. The primary challenge of sensing in an industrial environment is the conditioning of low signal levels in presence of high noise. Figure 2 shows various real world physical quantities for sensing with respect to resolution required and the bandwidth of these physical quantities.

If a successive approximation register (SAR) ADC is chosen for a DC sensing application, the SAR ADC would require an analog gain stage and a complete anti-aliasing filter. The external signal conditioning circuit adds a small error to the transducer signal. However, the delta-sigma ADC does not require the external functions (an analog gain stage and a complete anti-aliasing filter).

The delta-sigma ADC has many of the required signal conditioning functions designed within the ADC chip. The delta-sigma ADC performs these signal conditioning functions in the digital domain. The delta-sigma ADC can nearly be considered as a system-on-a-chip (SoC). Therefore, delta-sigma converter applications have fewer components when compared to SAR ADC circuits.

While in operation, the delta-sigma ADC continuously oversamples an input-voltage signal. The ADC then applies a digital filter on these samples to achieve a multi-bit, low-noise digital output. The byproduct of this algorithm is a higher dynamic range and lower output speeds.

Many delta-sigma ADCs include input buffers and programmable gain amplifiers (PGAs). An input buffer increases the input impedance to allow direct connection to high-source impedance signals. A PGA increases the converter's resolution when measuring small signals. Delta-sigma ADCs are inherently oversampling converters, which relaxes the baseband antialiasing filter requirements (an added benefit for this type of architecture).

Delta-sigma ADCs offer all these features in a small package. Therefore, these features of delta-sigma converters allow the designer to eliminate external analog circuitry in low-frequency signal chains. Figure 3 and Figure 4 show a clear picture why delta-sigma ADCs are a better choice for low-analog, signal-sensing applications by comparing different ADC architectures.

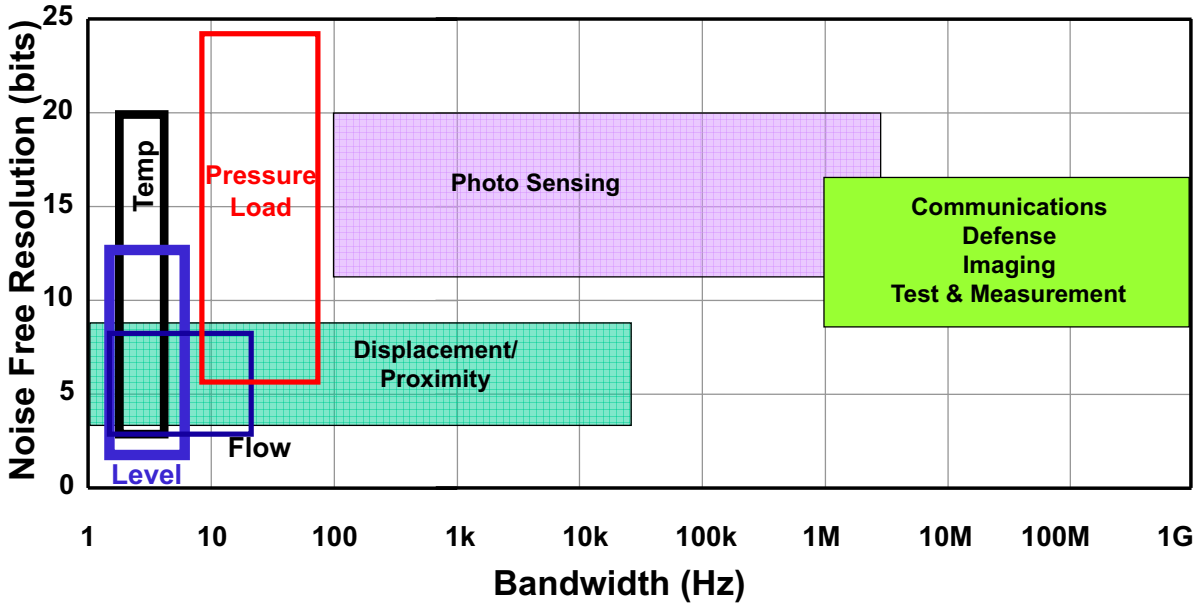


Figure 2. Real World versus Bandwidth

Characteristic	Pipelined	SAR	Delta Sigma
Throughput (samples/sec)	++	+	0/+
Resolution (ENOB)	0	+	++
Latency (Sample-to-Output)	+	++	0
Suitability for converting Multiple Signals per ADC	+	++	0
Capability to convert non-periodic multiplexed signals	+	++	-
Power Consumption	Scales with Sample Rate or Constant	Scales with Sample Rate	Constant

Figure 3. Comparisons of Different ADC Architectures

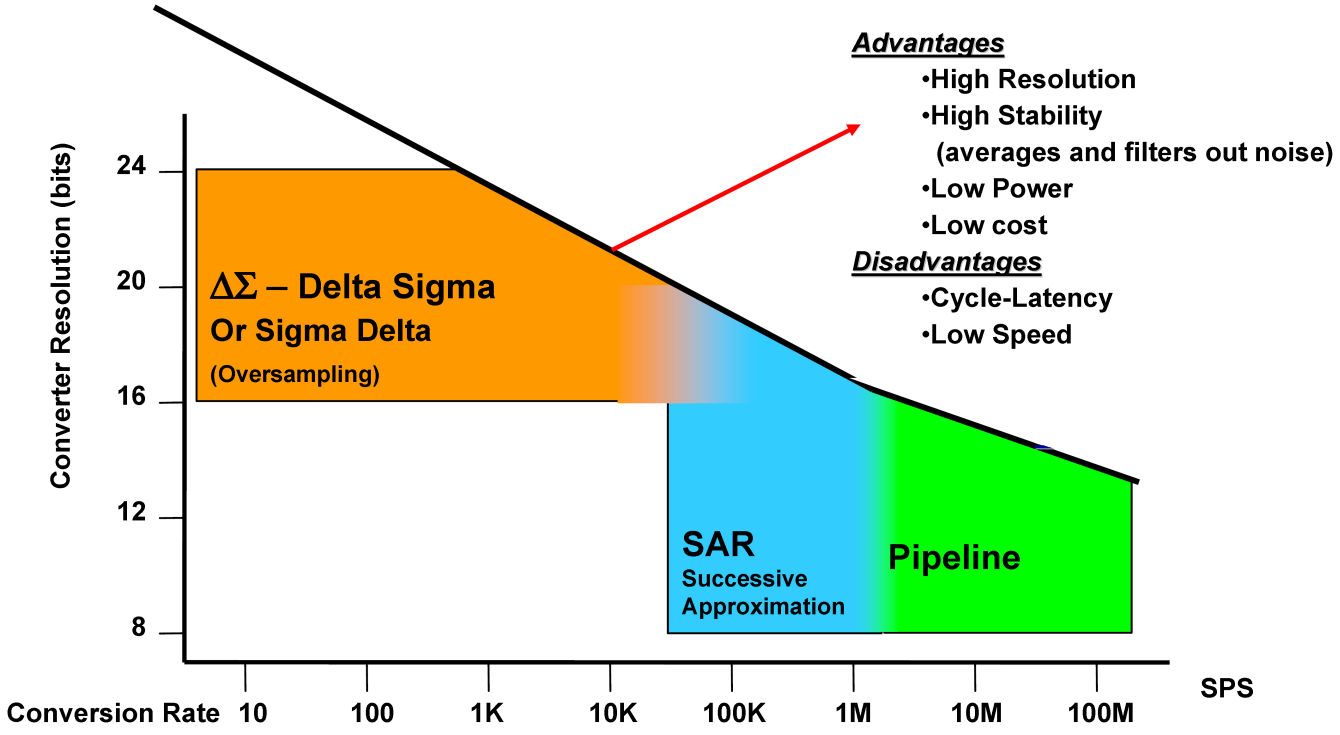


Figure 4. ADC Resolution versus Conversion Rate

A parametric comparison between different delta-sigma ADCs is given in Figure 5. The ADC selected for this application is ADS1220 which is a low-power, low-noise, 24-bit, delta-sigma ADC for small signal sensors. The high integration and small package size of ADS1220 enables the use of ADS1220 in space-sensitive applications. ADS1220 has the exact numbers of pins required for connecting with 2-, 3- or 4-wire RTD probes used in ratiometric technique.

Some of the highlighted features of ADS1220 are as follows.

- Low current consumption is approximately 415 µA (in normal mode)
- Programmable gain: 1 V/V to 128 V/V
- Programmable data rates up to 2000 SPS
- 50 Hz and 60 Hz line frequency rejection at 20 SPS
- Low noise PGA: 90 nVRMS at 20 SPS
- Dual-matched, programmable current sources for sensor excitation: 10 µA to 1.5 mA
- Two differential or four single-ended inputs
- Highly flexible input multiplexer
- Two burn-out current sources for sensor open-circuit detection
- Internal offset calibration by shorting PGA inputs using register setting
- SPI-compatible interface
- 3.5 mm × 3.5 mm 16-pin quad-flat no-leads (QFN) package

Compare Parts	ADS1148	ADS1248	ADS1220	ADS1118
Resolution (Bits)	16	24	24	16
Sample Rate (max) (SPS)	2kSPS	2kSPS	2kSPS	860SPS
# Input Channels	7	7	4	4
Power Consumption (Typ) (mW)	2.3	2.3	0.4	0.3
Architecture	Delta-Sigma	Delta-Sigma	Delta-Sigma	Delta-Sigma
Interface	Serial SPI	Serial SPI	Serial SPI	Serial SPI
Analog Voltage AV/DD (Min) (V)	2.7	2.7	2.3	2
Analog Voltage AV/DD (Max) (V)	5.25	5.25	5.5	5.5
Reference Mode	Ext Int	Ext Int	Ext Int Supply	Int
Rating	Catalog	Catalog	Catalog	Catalog
Operating Temperature Range (C)	-40 to 105	-40 to 105	-40 to 125	-40 to 125
Package Group	TSSOP VQFN	TSSOP	TSSOP VQFN	VSSOP X2QFN
Estimated Footprint (mm^2)	[pf]32VQFN[/pf]: 5 W 5 L: 25 mm2 [pf]28TSSOP[/pf]: 4.4 W 9.7 L: 51 mm2	[pf]28TSSOP[/pf]: 4.4 W 9.7 L: 51 mm2	[pf]16VQFN[/pf]: 3.5 W 3.5 L: 12 mm2 [pf]16TSSOP[/pf]: 4.4 W 5 L: 31 mm2	[pf]10X2QFN[/pf]: 2 W 1.5 L: 3 mm2 [pf]10VSSOP[/pf]: 3 W 3 L: 15 mm2
Integrated Features	PGA Dual matched Current Sources Internal Reference Oscillator 50/60 Hz rejection Single Cycle Settling Temp Sensor GPIOs	PGA Dual matched Current Sources Internal Reference Oscillator 50/60 Hz rejection Single Cycle Settling Temp Sensor GPIOs	PGA Dual matched Current Sources Internal Reference Oscillator 50/60 Hz rejection Single Cycle Settling Temp Sensor	PGA Oscillator Internal Reference Temp. Sensor
INL (+/-) (Max) (%)	0.0015	0.0015	0.0015	0.0015
PGA	PGA	PGA	PGA	

Figure 5. Compare Different Delta-Sigma ADCs

4.2 DAC Selection

Compare Parts	DAC8760	DAC161S997	DAC161P997
Architecture		Delta-Sigma	Delta-Sigma
DAC: Channels	1	1	1
Output Type	Current Voltage	Current	Current
Resolution (Bits)	16	16	16
INL (Max) (+/-LSB)		9	9
DNL (Max) (+/-LSB)	1	0.5	0.5
Offset Error (Max) (%)	0.1		
Gain Error (Max) (%FSR)	0.07	0.22	0.22
Total Unadjusted Error (Max) (%FSR)	0.1		
Output Range Max. (V or mA)	24	24	24
Analog Supply (Min) (V)	10	2.7	2.7
Analog Supply (Max) (V)	36	3.6	3.6
Power Consumption (Typ) (mW)	135	0.33	0.5
Interface	Serial SPI	Serial SPI	Single-Wire
Operating Temperature Range (C)	-40 to 125	-40 to 105	-40 to 105
Package Group	HTSSOP VQFN	WQFN	WQFN
Status	ACTIVE	ACTIVE	ACTIVE

Figure 6. Compare Different DACs

A parametric comparison between different DACs is given in Figure 6. The DAC selected for this application is DAC161S997. DAC161S997 is a 16-bit DAC and an obvious choice, as DAC161S997 was designed specifically for industry standard 4- to 20-mA current loops. DAC161S997 is an ideal choice for sensor nodes limited to 3.3 mA power consumption.

Some of the highlighted features of DAC161S997 are as follows.

- 16-bit resolution
- Very low power supply current < 125 µA (max)
- Pin-programmable, power-up condition
- Loop error detection and reporting
- Programmable output current error levels
- Ultra-low power internal reference and internal oscillator
- SPI-compatible interface
- No external precision components
- Integrating all precision elements on-chip in small 4 mm × 4mm 16-pin QFN package

4.3 MCU Selection

A 4- to 20-mA loop powered sensor transmitter application that requires continuous monitoring at low power consumption, MSP430™ MCUs with ferroelectric random-access memory (FRAM) are superior to typical flash memory based microcontrollers. The MSP430FR57xx family with FRAM introduces the market to a new generation of superior non-volatile memory devices.

Some of the benefits of MSP430FR57xx family with FRAM are as follows.

- Non-volatile memory — data state is retained even when power is turned-off
- Fast writing speed — 160 times faster than flash and >400 times lower energy on memory-write operations
- Unlimited write endurance — over 10^{15} write cycles
- Guaranteed completion of write operation in case of low power
- No pre-erase cycle required before writing
- Unified memory offers flexible code and data partitioning — the designer can dynamically partition the device memory into code space or data space, as needed

The selected MSP430 MCU with FRAM for this application is MSP430FR5738. MSP430FR5738 has 16 KB of FRAM, 1 KB of static random-access memory (SRAM), supports up to a 24-MHz system clock, two SPIs, 17 input/output pins (I/Os), and available in a 24-pin QFN package. A functional block diagram of MSP430FR5738 MCU is shown in Figure 7.

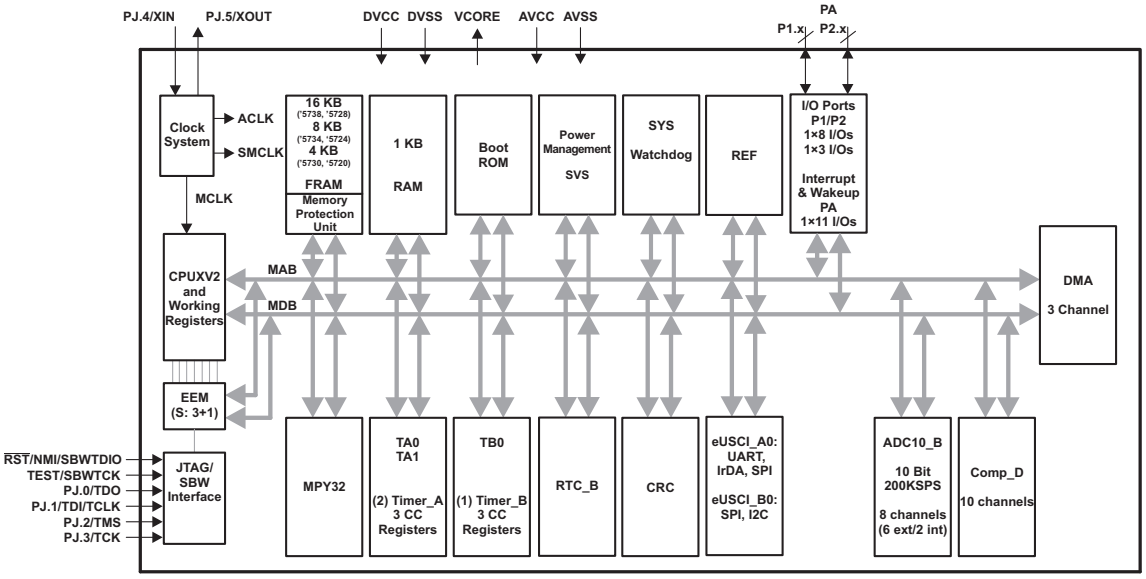


Figure 7. Functional Block Diagram of MSP430FR5738 MCU

4.4 LDO Selection

A wide input range is often required in industrial environments to protect large transients from damaging the LDO. The wide-input rating relaxes the design of external protection circuitry and minimizes protection circuitry cost and space. LDOs with wide-input range safely regulate the output-power supply rail at adesired 3.3 V, even when encountering high voltage transients at the input. These high-voltage transients cause high heat. Therefore, a proper package needs to be selected to dissipate heat. An LDO with low quiescent current is the best choice for a 4- to 20-mA loop-powered sensor transmitter. Quiescent current is needed to control internal circuitry that calibrates performance. A parametric comparison between different LDOs is given in Figure 9. The LDO device selected for this application is TPS7A1601DRB.

TPS7A1601DRB offers the following features.

- Wide input range 3 V to 60 V
- High accuracy — approximately 2%
- Low drop-out voltage — approximately 60 mV at 20 mA
- Power supply rejection ratio (PSRR) of 50 dB at 100 Hz
- Ultra-low quiescent current — approximately 5 µA
- Stable with any ceramic capacitor from 2.2 µF to 100 µF
- High thermal performance package

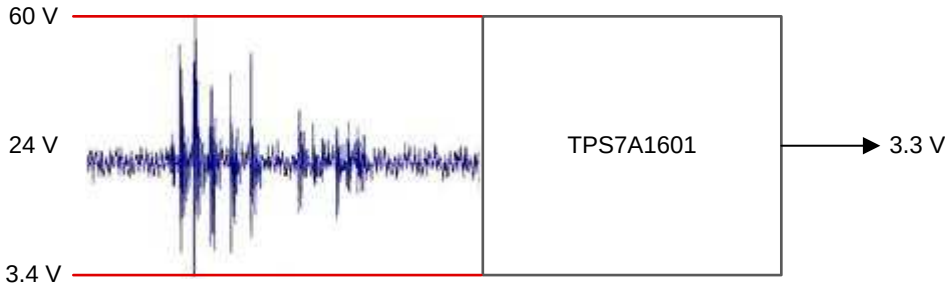


Figure 8. Wide Input Range of TPS7A1601 LDO

Compare Parts	TPS7A1601	TPS7A6601-Q1	TPS7A4001	TPS7A4101	TPS7A4901
Output Options	Adjustable Output	Adjustable Output	Adjustable Output	Adjustable Output	Adjustable Output
Iout (Max) (A)	0.1	0.15	0.05	0.05	0.15
Vin (Min) (V)	3	5.5	7	7	3
Vin (Max) (V)	60	40	100	50	36
Vout (Min) (V)	1.2	1.5	1.2	1.2	1.2
Vout (Max) (V)	18.5	5	90	48	33
Additional Features	PG Enable Over Current Protection Thermal Shutdown	Enable Over Current Protection PG Soft Start Thermal Shutdown	Enable Over Current Protection Thermal Shutdown	Enable Over Current Protection Thermal Shutdown	Over Current Protection Thermal Shutdown Enable Soft Start
Rating	Catalog	Automotive	Catalog	Catalog	Catalog
Operating Temperature Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Package Group	MSOP-PowerPAD SON	MSOP-PowerPAD	MSOP-PowerPAD	MSOP-PowerPAD	MSOP-PowerPAD
Estimated Footprint (mm^2)	[pf]8SON[/pf]: 3 W 3 L: 9 mm2 [pf]8MSOP-PowerPAD[/pf]: 3 W 3 L: 15 mm2	[pf]8MSOP-PowerPAD[/pf]: 3 W 3 L: 15 mm2	[pf]8MSOP-PowerPAD[/pf]: 3 W 3 L: 15 mm2	[pf]8MSOP-PowerPAD[/pf]: 3 W 3 L: 15 mm2	[pf]8MSOP-PowerPAD[/pf]: 3 W 3 L: 15 mm2
Iq (Typ) (mA)	0.005	0.012	0.02	0.02	0.06
Accuracy (%)	2	2	2.5	2.5	2.5
Vdo (Typ) (mV)	60	180	290	290	260
PSRR @ 100KHz (dB)	26	40	38	38	54
Regulated Outputs (#)	1	1	1	1	1
Output Capacitor Type	Ceramic	Ceramic	Ceramic	Ceramic	Ceramic

Figure 9. Compare Different LDO Devices

4.5 Block Diagram

This reference design has two hearts (ADS1220 and DAC161S997), one brain (MSP430FR5738), and one pacemaker (TPS7A1601). ADS1220 together with MSP430FR5738, DAC161S997 and TPS7A1601 uses less than 3.3 mA budget for a loop-powered sensor transmitter solution. The four selected integrated circuits complete the 4- to 20-mA transmitter signal chain. The detailed block diagram of the Small Form Factor 2-Wire 4- to 20-mA Current Loop RTD Temperature Transmitter is shown in Figure 10. The total current consumption by the selected devices is given in Equation 1 through .

$$I_{TOTAL} = I_{DAC1} + I_{DAC2} + I_{ADS1220} + I_{MSP430\ at\ 1MHz} + I_{DAC161S997} + I_{GND\_TPS7A1601} \quad (1)$$

At 25°C:

$$I_{TOTAL} \leq 250\mu A + 250\mu A + 415\mu A + 270\mu A + 100\mu A + 5\mu A \quad (2)$$

$$I_{TOTAL} \leq 1.29mA \text{ (Typical)}$$

Over -40°C to 85°C temperature range (worst condition):

$$I_{TOTAL} \leq 250\mu A + 250\mu A + 600\mu A + 730\mu A + 125\mu A + 10\mu A \quad (3)$$

$$I_{TOTAL} \leq 1.965mA \text{ (Maximum)}$$

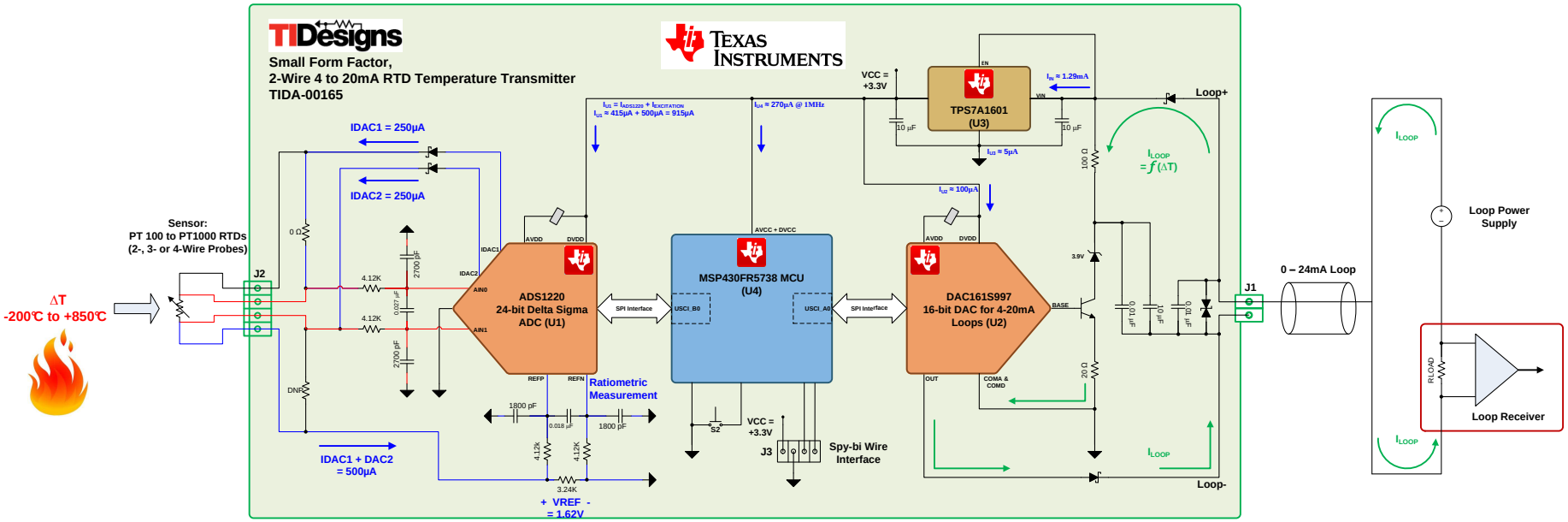


Figure 10. Conceptual Schematic Diagram of 2-Wire 4- to 20-mA Current Loop RTD Temperature Transmitter

5 System Design Theory

5.1 4- to 20-mA Current Loop – At a Glance

A typical current-loop system basically consists of four components as shown in Figure 11.

- Sensor (In this case, RTD temperature sensor)
- 4- to 20-mA Current Loop Sensor Transmitter
- Loop power supply
- Loop receiver

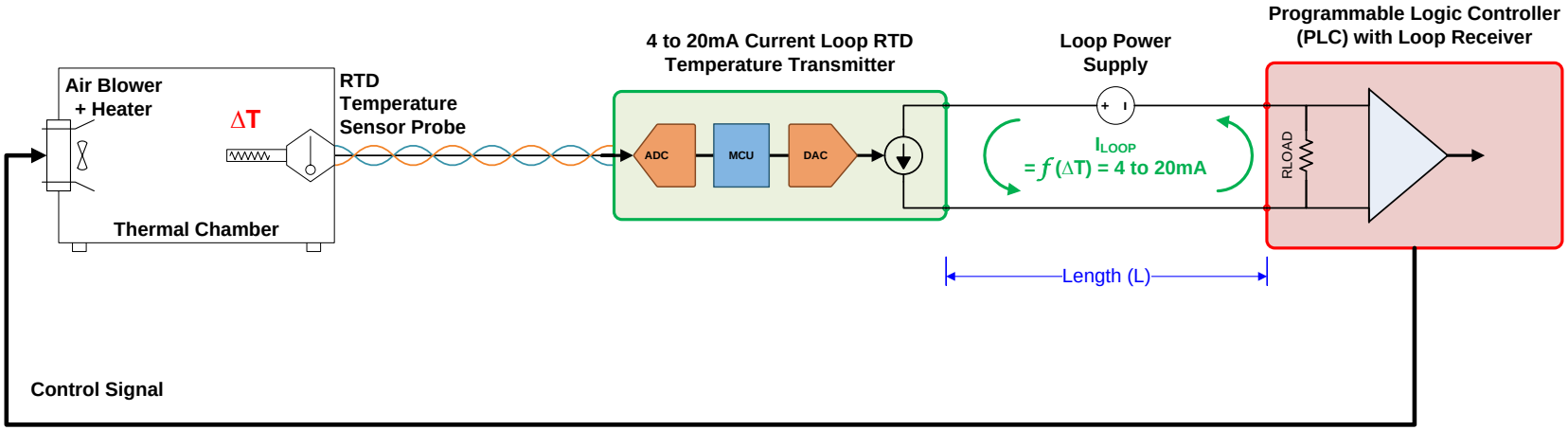


Figure 11. Typical Block Diagram of a Current Loop System

The sensor converts a physical parameter (in this case, temperature) to an equivalent voltage output. By regulating the current supplied by loop power supply, the transmitter converts the sensor's output to a proportional 4- to 20-mA DC current. The zero-value process variable, that is -200°C, is represented by 4 mA. The full scale process variable, that is 850°C, is represented by 20 mA. Therefore, a 16-mA span is available to represent the entire measurement information range. The current returns back to the power supply after flowing through a precision-load resistor of the loop receiver. As no system can measure the current directly, the receiver first converts 4- to 20-mA loop current into a voltage which is easily measured by the analog-input module of the programmable logic controller (PLC) system and processed further.

Choosing current over voltage as an information carrier is generally preferred due to the following reasons.

- Current loops have inherent immunity against noise.
- Transmitting current signal over long distances does produce the voltage drop (also known as voltage loss or loop drop) across the loop due to wiring resistance. However, the magnitude of signaling is not affected as long as the loop power supply is high enough to compensate for these losses and still meets the compliance voltage requirement at the transmitter for the transmitter's proper operation. Basic circuit theory shows that current is the same along the signal line, which means the same amount of current supplied by loop power supply always returns back to the source.
- The residual 4-mA current at zero-point allows easy detection of a wire-break condition. The residual 4-mA current at zero-point also allows the transmitter to be powered up if the current requirement is within 4 mA. The current will exceed 20 mA for a short-circuit condition. Therefore, current loops are self-monitoring.
- Choosing current over voltage minimizes the cost and simplifies the installation, since signal current and transmitter power-supply current share the same pair of conductors.
- Choosing current over voltage ensures safer operation in hazardous areas by limiting the energy available for ignition. Lower currents and voltage levels also ensure personnel safety.

The complete loop power supply voltage does not appear across the transmitter as all the devices in a 2-wire loop-powered system are connected in series. Therefore, it important to ensure that the loop-power supply is large enough to supply the minimum voltage at the transmitter while the maximum-expected loop current has taken care of the other drops in the loop. For detailed calculations of minimum loop power supply voltage, refer to Section 5.5.2 of this design guide.

5.2 RTD Overview and the Callendar-Van Dusen Equation

An RTD is a sensing element made of a metal with predictable resistance characteristics over temperature. Therefore, the temperature of an RTD is calculated by measuring the RTD's resistance. RTD sensors offer wide temperature ranges, good linearity, and excellent long-term stability and repeatability. These features make RTD sensors suitable for many precision applications.

Most RTD applications use a current source as excitation for the RTD element. By driving a known current through the RTD, a voltage potential is developed that is proportional to the resistance of the RTD and the excitation current. This voltage potential is amplified and then fed to the inputs of an ADC. The ADC converts the voltage into a digital output code that can be used to calculate the RTD resistance. A simplified circuit for an RTD measurement application is shown in Figure 12.

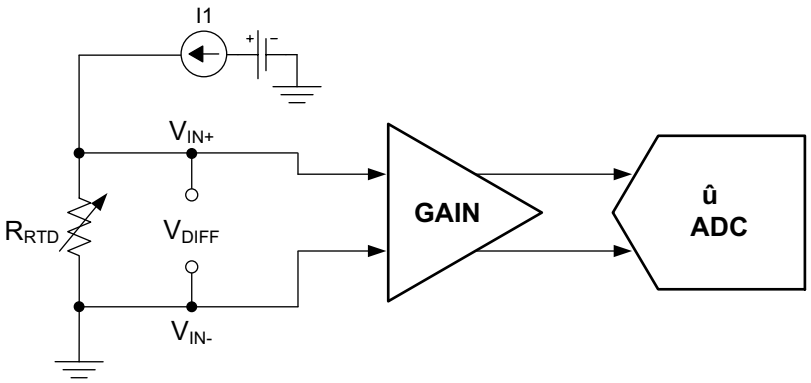


Figure 12. Simplified RTD Application Circuit

The basic principle for RTD operation is that all the metals have a positive change in resistance with increase in temperature. Metals which have high resistivity, high melting point, and high corrosion resistance are generally preferred for making RTDs. These characteristics allow using less amount of material to achieve high-nominal resistance value. By far, platinum is the best material for RTDs because of platinum's high resistivity and long term stability. Platinum follows a very linear resistance-temperature relationship compared to other metals. As a noble (chemically inert) metal, platinum is less susceptible to contamination. Platinum is one of the leading choices for metal for temperature measurement applications. PT100 RTD has an impedance of 100 Ω at 0°C and approximately 0.385 Ω of resistance change per 1°C change in temperature. This impedance results in 18.52 Ω at –200°C and 390.481 Ω at 850°C. However, higher-valued RTDs such as PT200, PT500, or PT1000 can be used for increased sensitivity and resolution at small extra cost.

Class-A RTDs are a good choice for this application to provide good pre-calibration accuracy and long term stability. A Class-A RTD has less than 0.5°C of error at 100°C without calibration and the long-term stability makes accurate and infrequent calibration possible. Table 2 displays the tolerance, initial accuracy, and resulting error at 100°C for the five main classes of RTDs.

Table 2. RTD Class Tolerance Information

TOLERANCE CLASS (DIN-IEC 60751)	TOLERANCE VALUES (°C)	RESISTANCE AT 0°C (Ω)	ERROR AT 100°C (°C)
AAA[1]	±(0.03 + 0.0005 × T)	100 ± 0.012	±0.08
AA	±(0.01 + 0.0017 × T)	100 ± 0.04	±0.27
A	±(0.15 + 0.002 × T)	100 ± 0.06	±0.35
B	±(0.3 + 0.005 × T)	100 ± 0.12	±0.8
C	±(0.6 + 0.01 × T)	100 ± 0.24	±1.6

(1) AAA is not included in the DIN-IEC 60751 specification but is an industry accepted tolerance for performance demanding applications.

The relationship between the resistance and temperature of platinum RTD is defined by a nonlinear mathematical model known as the Callendar-Van Dusen (CVD) equation. The coefficients in the Callendar-Van Dusen equation are defined by the IEC-60751 standard.

For T > 0°C, the CVD equation is a second-order polynomial as given in Equation 4:

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2] \quad (4)$$

For T < 0°C, the CVD equation expands to a fourth-order polynomial as given in Equation 5:

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2 + C(T)^3 (T - 100)] \quad (5)$$

The linear approximation model is as follows:

$$RTD(T) = R_0 \times [1 + \alpha(T)]$$

where

- T = Temperature of RTD element in °C
- RTD (T) = resistance of RTD element as a function of temperature
- R_0 is the resistance of the RTD element at 0°C
- α = Sensitivity of RTD element = 0.00385 Ω/Ω/°C
- $A = 3.9083 \times 10^{-3}$ °C^{-1}
- $B = -5.7750 \times 10^{-7}$ °C^{-2}
- $C = -4.1830 \times 10^{-12}$ °C^{-4} (6)

The behavior of resistance for PT100 RTD from –200°C to 850°C is shown in Figure 13.

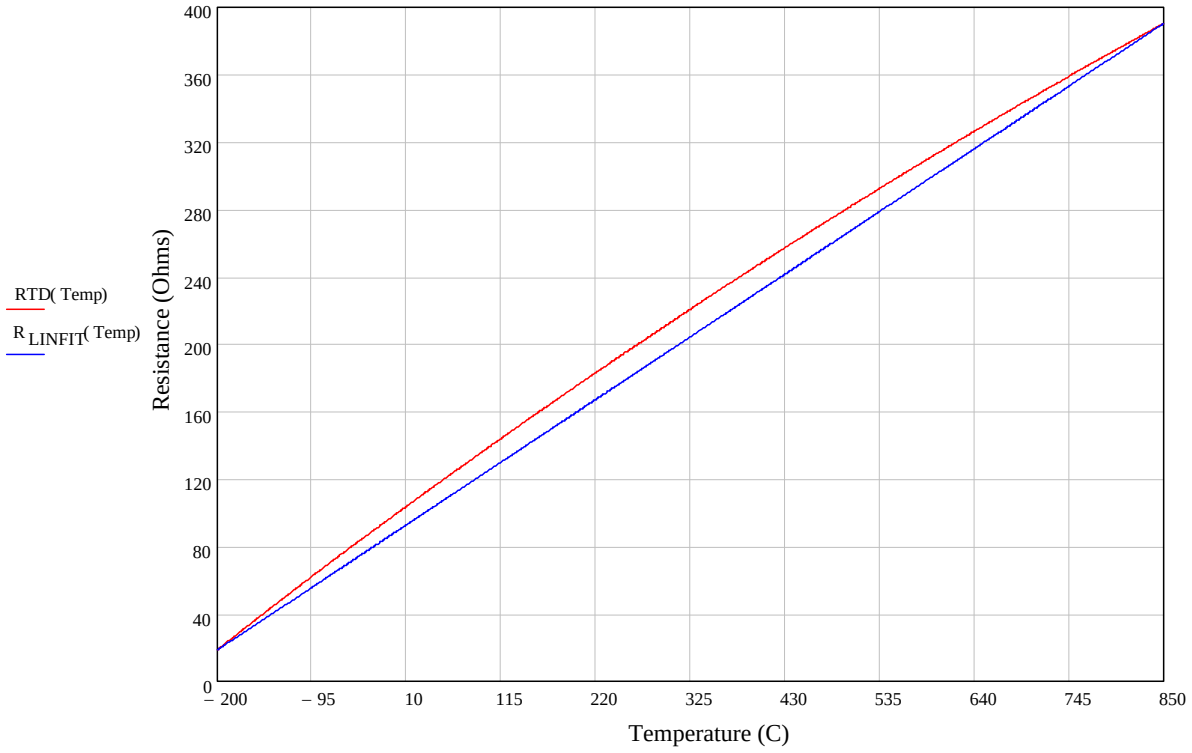


Figure 13. RTD Resistance and Linear Fit Line versus Temperature

The change in RTD resistance is piecewise linear over small temperature ranges. An end point curve fitting shows RTDs have second-order nonlinearity of approximately 0.375% as shown in Figure 14. Therefore, it is necessary to implement a digital linearization technique to correct this nonlinearity error. Table 3 compares three digital linearization techniques.

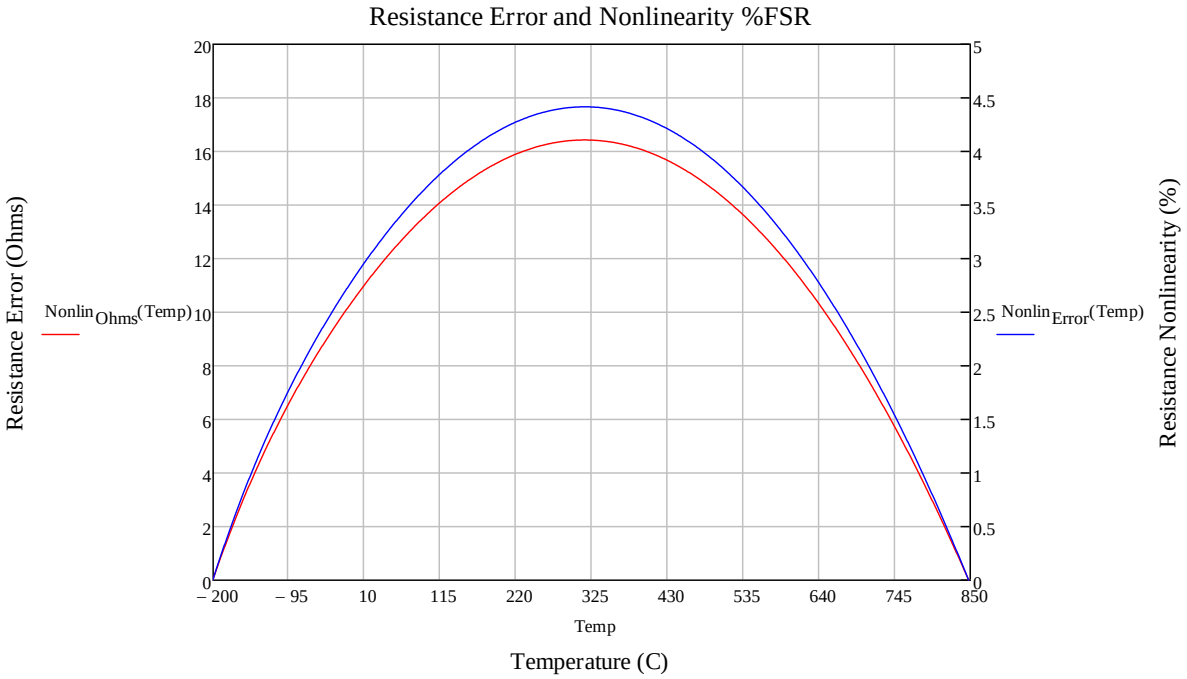


Figure 14. PT100 RTD Nonlinearity from –200°C to 850°C

Table 3. Comparison of Linear Approximation Methods

METHOD	ADVANTAGE	DISADVANTAGE	OTHER REMARKS
Simple Linear Approximation	Easy to implement Fast execution Accurate over small temperature ranges Smaller code size	Least accurate over wide temperature range	Simple method when memory size is limited and temperature range is smaller
Piecewise Linear Approximation	Accuracy depends on the entries in the lookup table Fast execution	High accuracy More entries in lookup table Bigger code size	Most practical method implement by most of the embedded systems
Callendar-Van Dusen equation	Most accurate	Extremely processor Intensive Time consuming Requires quare root and power functions on the processor	Not practical in most applications

In this reference design, a look-up table for the PT100 RTD with a resolution of 1°C is used for linear interpolation. The RTD value is computed after offset and gain calibration. Then, this RTD value is used in linear interpolation of the line segment involving two surrounding points in the PT100 RTD look-up table. If additional accuracy is desired, a table with more points with less than 1°C or more accurate curve fit can be stored as a look-up reference table.

5.3 ADC Operation (Three Wire RTD Measurement)

The first heart of this reference design is ADS1220. ADS1220 integrates all required features (such as dual-matched programmable current sources, buffered reference inputs, and PGA) to ease the implementation of ratiometric 2-, 3-, and 4-wire RTD measurements.

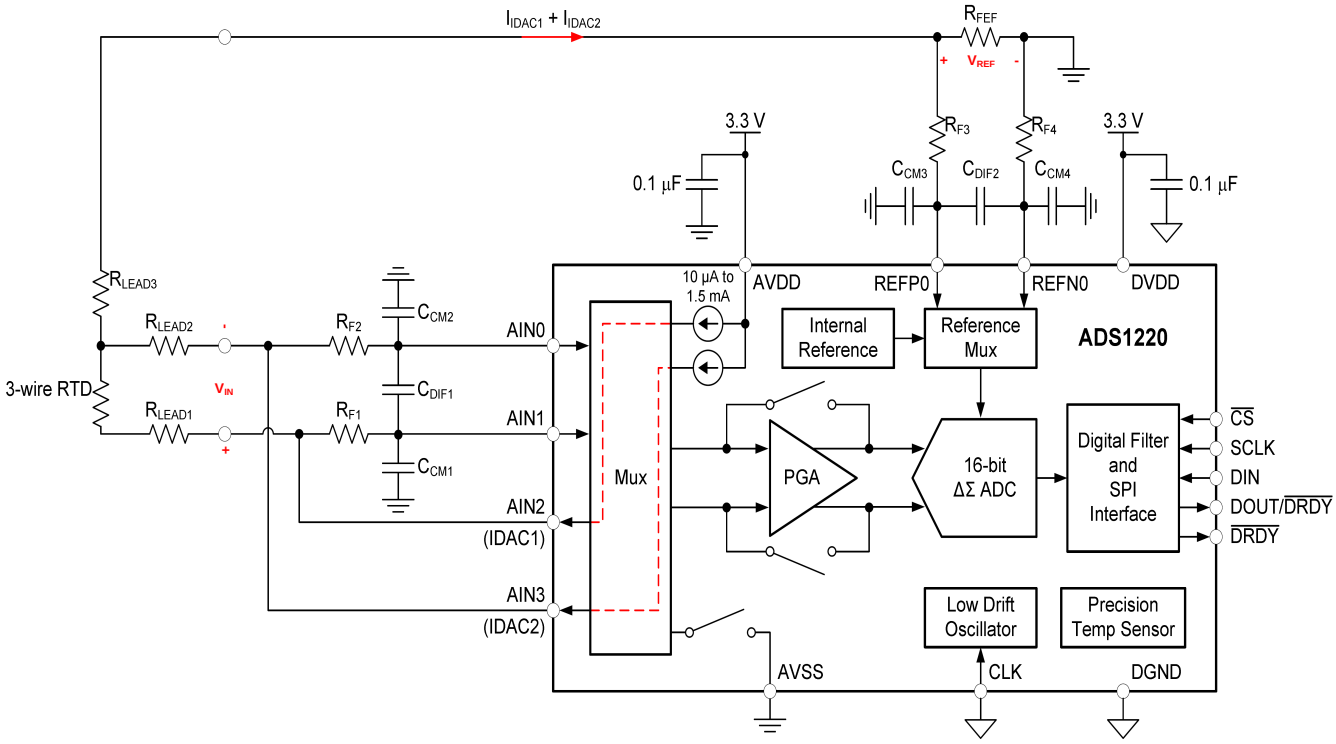


Figure 15. 3-Wire RTD Measurement

The circuit in Figure 15 employs a ratiometric measurement approach. In other words, the sensor signal (the voltage across the RTD) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise cancel out because these errors are common to both the sensor signal and the reference.

In order to implement a ratiometric 3-wire RTD measurement, ADS1220 provides two integrated digital-analog converter (IDAC) current sources capable of outputting currents from 10 µA to 1.5 mA. IDAC1 is routed to one of the excitation leads of the RTD. IDAC2 is routed to the second excitation lead as shown in Figure 15 by appropriate setting of I1MUX [2:0]: IDAC1 routing configuration bits and I2MUX [2:0]: IDAC2 routing configuration bits in the configuration register 3. Both currents have the same value, which is programmable by bits IDAC [2:0]: IDAC current setting in configuration register 2.

The design of the ADS1220 ensures that both IDAC values are closely matched, even across temperature. The excitation current of 1 mA or less is generally preferred for industrial applications in order to minimize the error due to self-heating. In this application, IDAC1 and IDAC2 programmed for 250 µA.

The sum of both currents, that is 500 µA, flows through a reference resistor, R_{REF}. The voltage developed across R_{REF} is fed into the positive and negative reference pins (REFP0 and REFN0) of the ADS1220 which is configured to use this external reference voltage V_{REF} for the analog-to-digital conversions. The R_{REF} resistor and excitation current are sized to produce an external reference of mid-supply (AVDD + AVSS)/2.

$$\text{ADC CODE } \alpha \frac{V_{RTD} \times PGA_{GAIN}}{V_{REF}} \quad (7)$$

$$\text{ADC CODE } \alpha \frac{R_{RTD} \text{ x } PGA_{GAIN}}{2 \times R_{REF}} \quad (8)$$

From Equation 8, it is obvious that the accuracy of the measurement depends on the reference resistor. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter. However, because the value of the reference resistor directly impacts the measurement result, the accuracy can be set to a higher level by choosing a high-precision, low-drift reference resistor R_{REF}.

5.3.1 Selecting R_{REF}

V_{REF} = (IDAC1 + IDAC2) X R_{REF} (9)

Because, IDAC1 = IDAC2 = IDAC = 250 µA

IDAC1 = IDAC2 = IDAC = 250µA (10)

If R_{REF} = 3.24 kΩ, ±0.1% tolerance or better, 25 PPM/°C drift or better, then

V_{REF} = 2 × IDAC × R_{REF} = 2 × 250 µA × 3.24 kΩ = 1.62 V, (11)

which is close to mid-supply voltage.

5.3.2 Selecting PGA Gain

The voltage produced across the RTD needs to be amplified by the PGA before it reaches ΔΣ ADC for conversion. The PGA gain should be chosen so that ADC input signal is still less than V_{REF} at maximum RTD temperature. The largest possible gain will yield the best resolution per °C.

R_{RTD} at 850°C = 390.48 Ω,

V_{RTD} at 850°C = 390.48 Ω X 250 µA = 97.62 mV,

$$PGA\_GAIN = \frac{V_{REF}}{V_{RTD} \text{ at } 850°C} = \frac{1.62 \text{ V}}{97.62 \text{ mV}} = 16.6 \text{ V / V} \quad (12)$$

The closest programmable gain option is 16V/V.

5.3.3 Common Mode Voltage Compliance Check

The allowed common-mode input voltage range is as highlighted in Figure 16.

ANALOG INPUTS			
Full-scale input voltage (V_{IN} = ADCINP – ADCINN)		$\pm V_{REF}/PGA$ (1)	V
Common-mode input range		AVSS + 0.2 V + $\frac{(V_{IN})(Gain)}{2}$ AVDD – 0.2 V – $\frac{(V_{IN})(Gain)}{2}$	V

Figure 16. Specification for Common Mode Input Range

$$0\,V + 0.2 + \frac{0.09762\,V \times 16\,V/V}{2} \le V_{CM} \le 3.3\,V - 0.2\,V - \frac{0.09762\,V \times 16\,V/V}{2} \quad (13)$$

0.981 V ≤ V_{CM} ≤ 2.32 V

The common-mode input voltage actually set by the design can be given as shown in Equation 14.

$$V_{CMI} = (IDAC \times R_{LEAD}) + \frac{IDAC \times R_{RTD}}{2} + 2 \times IDAC \times (R_{LEAD} + R_{REF}) \quad (14)$$

Assuming R_{LEAD} = 10 Ω,

V_{CMI} at R_{RTD} at -200°C ≤ VCMI ≤ V_{CMI} at R_{RTD} at 850°C (15)

1.63 V ≤ V_{CMI} ≤1.68 V

This result is well within the maximum allowed common-mode input voltage range.

5.3.4 Excitation Current Compliance Voltage Check

When designing the circuit, care should be taken to meet the compliance-voltage requirement of the IDACs. The IDACs require a minimum headroom of (AVDD – 0.9 V) in order to operate accurately.

EXCITATION CURRENT SOURCES (IDACs)			
Current settings		10, 50, 100, 250, 500, 1000, 1500	µA
Compliance voltage	All currents	AVDD – 0.9	V

Figure 17. Specification for Excitation Current Source Compliance Voltage

For IDAC1:

$$AVSS + [IDAC1 \times (R_{LEAD1} + R_{RTD})] + [(IDAC1+IDAC2) \times (R_{LEAD3}+R_{REF})] + V_{DIODE} \leq AVDD - 0.9\ V \quad (16)$$

$$2.12512\ V \leq 2.4\ V$$

For IDAC2:

$$AVSS + [IDAC2 \times (R_{LEAD2} + R_{RTD})] + [(IDAC1+IDAC2) \times (R_{LEAD3} + R_{REF})] + V_{DIODE} \leq AVDD - 0.9\ V \quad (17)$$

$$1.628\ V \leq 2.4\ V$$

This means that the excitation current compliance voltages for IDAC1 and IDAC2 are met.

5.3.5 Analog Input and Reference Low Pass Filter Design

RTD voltage output signal is typically in the millivolt range, which makes the signal susceptible to noise. First-order differential and common-mode RC filters (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) are placed on the ADC inputs, as well as on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and, C_{CM4}) to eliminate high-frequency noise in RTD measurements. The differential cut-off frequency of the analog-input filter must be chosen at least ten times higher than the ADC bandwidth at the selected data rate. The cut-off frequency chosen for this design is higher to account for a faster sampling rate. If the corner frequencies are not matched, noise appearing on analog input will be different from noise on the reference, which will not get cancelled in ratiometric measurement. For best performance, it is recommended to match the corner frequencies of the analog-input and reference low-pass filters. For more details on how to match corner frequencies of analog input and reference filters, refer to the following document: *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*, Application Report SBAA201.

5.3.6 Excitation Current Chopping

The two current sources must be perfectly matched to successfully cancel the lead resistance of the RTD wires. While initial matching of the current sources is important, any remaining mismatch in the two sources can be minimized by swapping (or chopping) the two current sources between the two inputs. Taking a measurement in both configurations and averaging the two readings will greatly reduce the effects of mismatched current sources (see Equation 18). Realizing current chopping technique could become possible by the use of an integrated, digitally-controlled, very-flexible input multiplexer inside ADS1220.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITATION CURRENT SOURCES (IDACs)					
Current settings			10, 50, 100, 250, 500, 1000, 1500		µA
Compliance voltage	All currents			AVDD – 0.9	V
Accuracy	All currents, each IDAC	–6%	±1%	6%	
Current match	Between IDACs (not valid for 10-µA setting)		±0.3%		
Temperature drift	Each IDAC (not valid for 10-µA setting)		50		ppm/°C
Temperature drift matching	Between IDACs (not valid for 10-µA setting)		10		ppm/°C

Figure 18. Specification for Excitation Current Source Mismatch and Temperature Drift

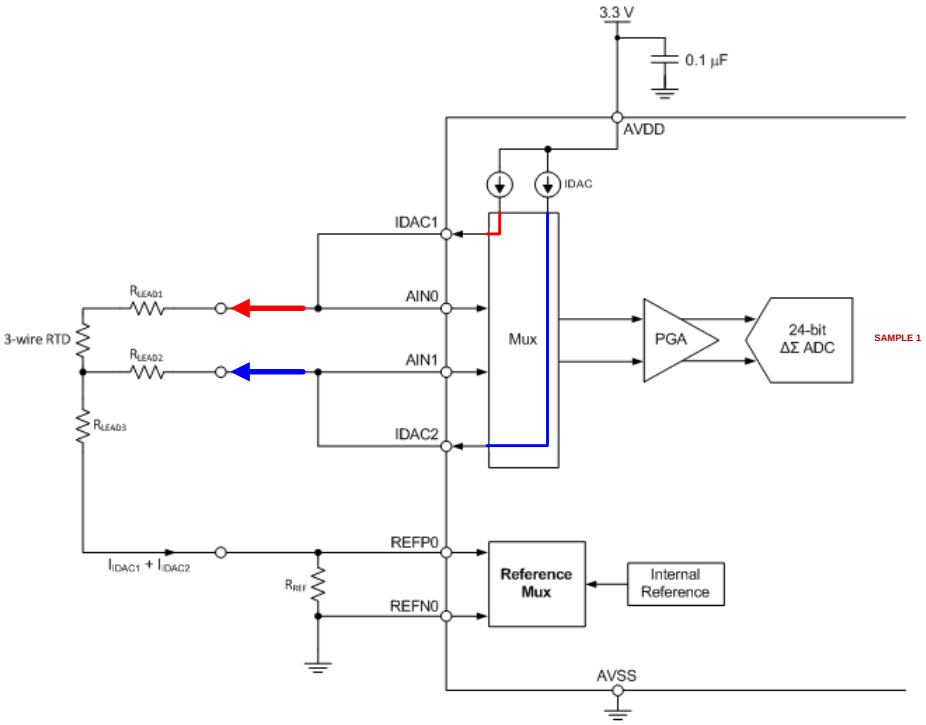


Figure 19. Measurement before Excitation Current Swap

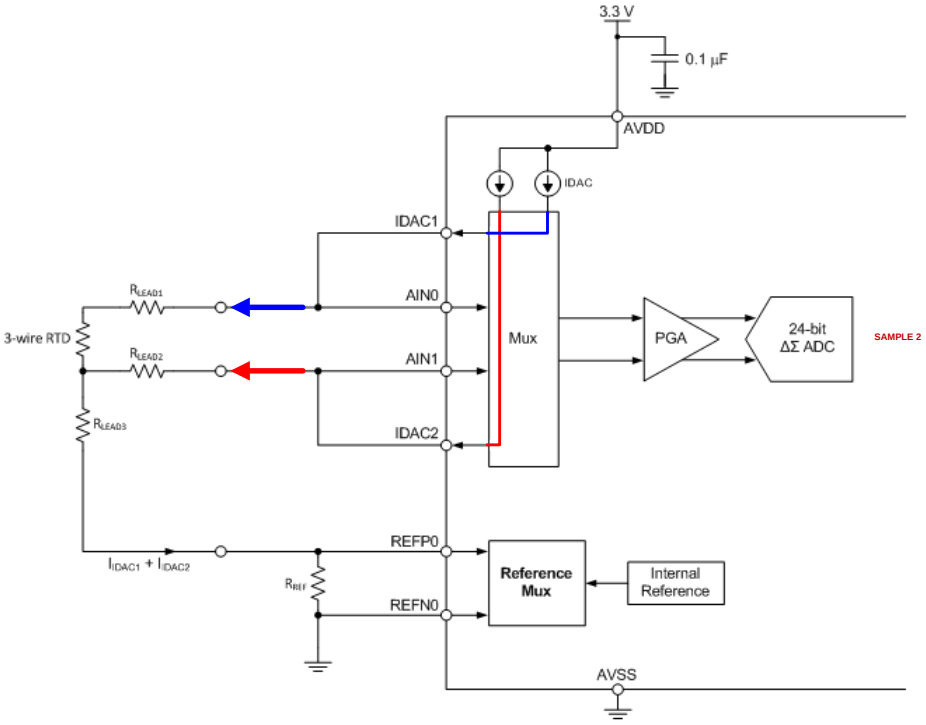


Figure 20. Measurement after Excitation Current Swap

$$\text{IDAC Mismatch Corrected Reading} = \frac{\text{SAMPLE 1} + \text{SAMPLE 2}}{2} \quad (18)$$

5.4 MCU Operation

MPS430FR5738 MCU is the brain of 2-wire 4- to 20-mA current loop RTD temperature transmitter. The intelligence required to perform all intended functions are coded in software which resides inside FRAM and runs from FRAM. The MCU interfaces with ADS1220 and DAC161S997 devices through two independent SPIs — USCI_B0 and USCI_A0, respectively. Immediately after power-up, the MCU performs necessary initializations required for itself, such as setting-up the system clock, I/O port setting, enables/disables interrupts, and initializes SPI engines to start communication with ADC and DAC. After self-initialization, the MCU initializes the internal registers of ADC and DAC as per the design requirements already captured and implemented in software.

The MCU gets the raw 24-bit code from the ADS1220 device that corresponds to the RTD temperature at the measurement point at that instance, applies offset and gain calibration, converts the ADC code to a resistance value, performs linear interpolation to convert resistance value into temperature using the RTD look-up table, converts this temperature value to the DAC input code, and after correcting for DAC gain and offset correction, applies the 16-bit code corresponding to loop current to the DAC161S997 device through SPI as shown in Figure 21.

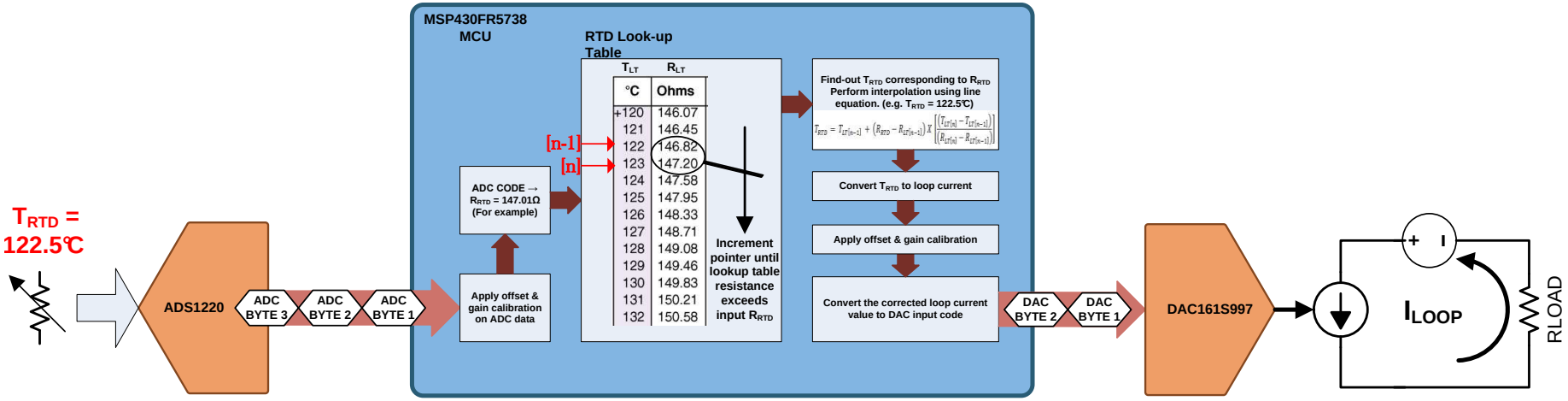


Figure 21. Data Flow Diagram

5.4.1 Converting ADC Output Code to RTD Resistance

ADS1220 provides 24-bit data in binary twos complement format. The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes are for signals that exceed full-scale (FS).

Table 4. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ +FS (2^{23} – 1) / 2^{23}	7FFFFFh
+FS / 2^{23}	000001h
0	0
–FS / 2^{23}	FFFFFFh
≤ –FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

$$1\ \text{LSB} = \frac{\text{Full Scale Range}}{(2^{24} - 1)} = \frac{2 \times \text{FS}}{(2^{24} - 1)} = \frac{2 \times V_{REF}}{\text{GAIN} \times (2^{24} - 1)} \tag{19}$$

In ratiometric measurement, $V_{IN} = R_{RTD} \times IDAC$ and $V_{REF} = 2 \times R_{REF}$ X IDAC, then

$$V_{IN} = 1\text{LSB} \times (\text{ADC\_CODE})_{DEC} = \frac{2 \times V_{REF} \times (\text{ADC\_CODE})_{DEC}}{\text{GAIN} \times (2^{24} - 1)} \tag{20}$$

$$R_{RTD} = \frac{4 \times R_{REF} \times (\text{ADC\_CODE})_{DEC}}{\text{GAIN} \times (2^{24} - 1)} \tag{21}$$

Where, R_{REF} = 3240 Ω and GAIN = 16V/V

5.4.2 Converting R_{RTD} to Equivalent Temperature (T_{RTD})

To perform a linear interpolation using a look-up table, first compare the measured R_{RTD} values with resistance values (R_{LT}) given in the look-up table, until the look-up table value exceeds the measured value that is being converted. Then, use Equation 22 to convert the measured R_{RTD} value to temperature value (T_{RTD}). This operation involves four additions, one multiplication, and one division step, respectively. This operation can be done easily on a 16-bit MSP340FR5738 MCU.

$$T_{RTD} = T_{LT[n-1]} + \left(R_{RTD} - R_{LT[n-1]}\right) \times \left[\frac{\left(T_{LT[n]} - T_{LT[n-1]}\right)}{\left(R_{LT[n]} - R_{LT[n-1]}\right)}\right] \tag{22}$$

5.4.3 Converting T_{RTD} to Equivalent DAC Input Code

First of all, convert the temperature value (T_{RTD}) to equivalent loop current using Equation 23 (see also Figure 23).

$$I_{LOOP} = 4\ \text{mA} + \left(T_{RTD} + 200°\text{C}\right) \times \left[\frac{16\ \text{mA}}{1050°\text{C}}\right] \tag{23}$$

Then, convert this loop current into the DAC input code using Equation 24.

$$I_{LOOP} = 24\ \text{mA} \times \left[\frac{\text{DAC\_CODE}}{2^{16}}\right] \tag{24}$$

To find out the relation between T_{RTD} and DAC_CODE, substitute the value of I_{LOOP} from Equation 23 in Equation 24,

$$DAC\_CODE = DEC2HEX\left[\frac{\left[4\,mA + (T_{RTD} + 200°C) \times \left[\frac{16\,mA}{1050°C}\right]\right] \times 2^{16}}{24\,mA}\right] \quad (25)$$

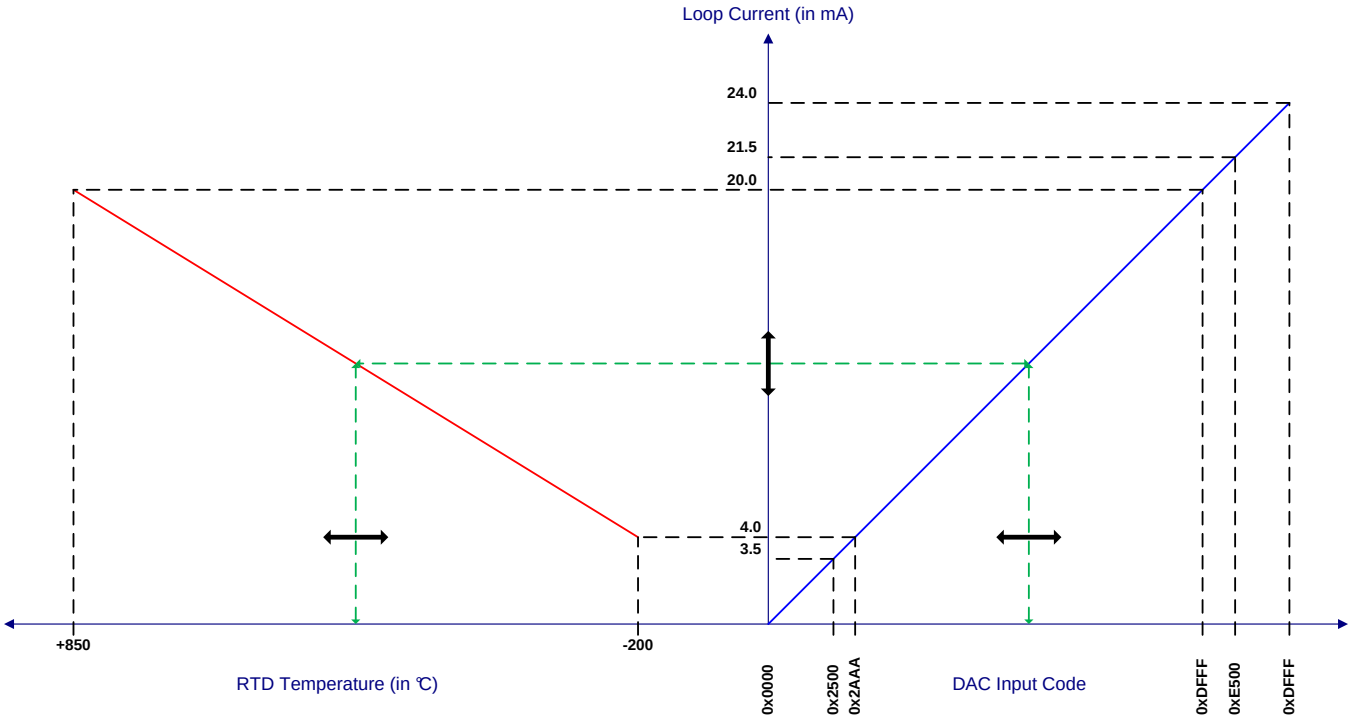


Figure 22. Mapping RTD Temperature to Loop Current to DAC Input Code

5.5 DAC Operation

The second heart of this reference design is DAC161S997, which converts a 16-bit input code in the DACCODE registers to an equivalent current output over the loop. The ΔΣ DAC output is a current pulse which is then filtered by a third-order RC low-pass filter and boosted to produce the loop current (I_{LOOP}) at the device OUT pin. Figure 23 shows the principle of operation of the DAC161S997 in the loop-powered transmitter. The I_{LOOP} has a number of component currents as given in Equation 26.

$$I_{LOOP} = I_{DAC} + I_D + I_A + I_E = 24\ mA \times \left[\frac{DAC\_CODE}{2^{16}}\right] \quad (26)$$

where

- I_{DAC} = f(DAC_CODE),
- I_D and I_A represent the supply currents of internal digital and analog blocks,
- I_{AUX} represents the supply current of companion devices present in the system,
- I_E is the only component which is regulated by the control loop to ensure that the actual loop current corresponds to the DAC input code applied by the MCU.

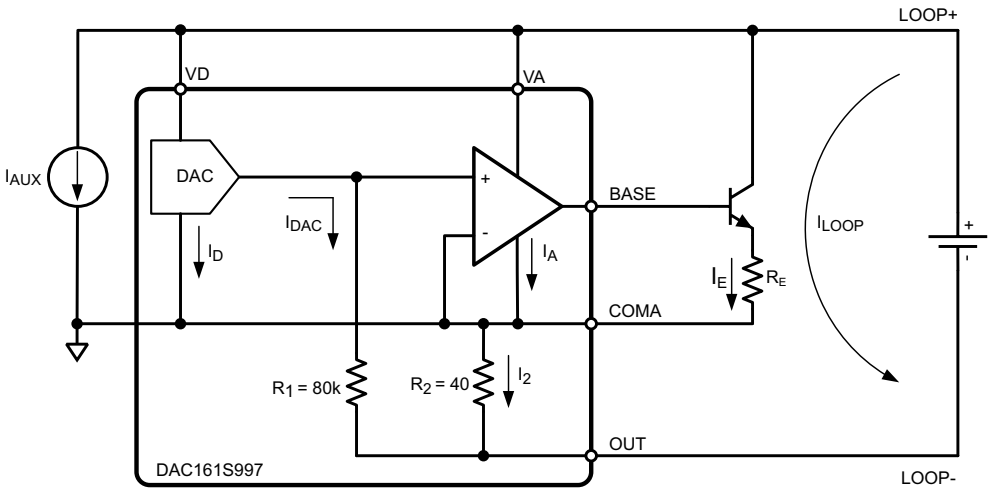


Figure 23. Loop Powered Transmitter

5.5.1 Reasons for Choosing a 3.9-V Zener Diode

The first and most important requirement for the proper functioning of the entire circuitry is a stable power supply. A good design ensures that the LDO gets the sufficient input voltage (V_{IN_LDO}) to generate a stable 3.3 V under minimum-loop, power-supply voltage and minimum-loop current conditions.

$$V_{IN\_LDO\ (MIN\ REQUIRED\ at\ 3.3\ mA)} = V_{CC} + V_{DO\ (MIN)} = 3.3\ V + 0.1\ V = 3.4\ V \quad (27)$$

From the circuit implementation, it is evident that the LDO input voltage V_{IN_LDO} is function of loop current and collector-emitter drop (V_{CE}) of the bipolar junction transistor (BJT). Apply Kirchhoff's Voltage Law (KVL) in the inner loop,

$$V_{(IN\_LDO)} = [(R_C \times I_{LOOP}) + V_{ZENER} + V_{CE} + (R_E \times I_{LOOP})] \quad (28)$$

At minimum loop power supply voltage, BJT operation is pushed towards saturation, which means that V_{CE} is approximately 0 V (minimum). Due to the stability considerations of the current control loop, the minimum output current ($I_{LOOP\ (MIN)}$) below 200 µA is not advised as shown in Figure 24.

$$V_{(IN\_LDO)}\ (\text{at minimum } V_{SUPPLY}\ \&\ \text{minimum } I_{LOOP}) = [(R_C \times I_{LOOP\ (MIN)}) + V_{ZENER} + V_{CE\ (MIN)} + (R_E \times I_{LOOP\ (MIN)})] \quad (29)$$

To ensure stable 3.3-V LDO output under these conditions, the following relation must be fulfilled.

$$V_{(IN\_LDO)}\ (\text{at minimum } V_{SUPPLY}\ \&\ \text{minimum } I_{LOOP}) > V_{IN\_LDO\ (MIN\ REQUIRED\ at\ 3.3\ mA)} \quad (30)$$

$$[(100\ \Omega \times 200\ \mu A) + V_{ZENER} + 0\ V + (20\ \Omega \times 200\ \mu A)] > 3.4V$$

$$[V_{ZENER} + 0.024\ V] > 3.4\ V$$

From Equation 30, it is clear that without having a zener diode, a voltage greater than 3.4 V at the input of the LDO cannot be ensured. Therefore, choose a zener diode having a zener voltage (V_{Zener}) greater than 3.4 V and able to handle power dissipation, $P_{DZ} = V_{Zener} \times I_{LOOP\ (MAX)}$. In this application, the design uses a 3.9-V, 500-mW zener diode.

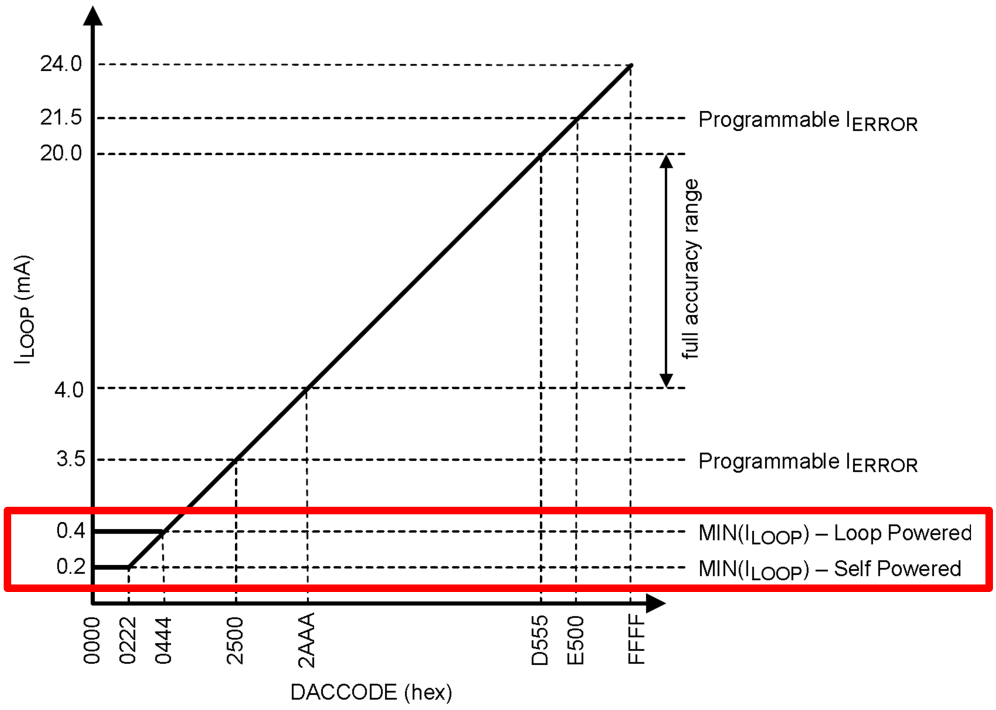


Figure 24. DAC DC Transfer Function

5.5.2 Loop Compliance Voltage

To calculate the minimum-loop, compliance-voltage (loop-power supply voltage), add all voltage drops in the loop at the maximum-expected loop current.

From a current control loop stability point of view, $V_{CE\ (MIN)}$ must stay greater than maximum $V_{CE\ (SAT)}$:

$V_{CE\ (MIN)} > 0.2\ V$

Applying Kirchhoff's Voltage Law in the outer loop, to find out the $V_{CE\ (MIN)}$:

$$V_{CE\ (MIN)} = V_{(SUPPLY\ (MIN)} – (2 \times V_{WIRE}) - (2 \times V_F) - V_{RC\ (MAX)} - V_{ZENER} - V_{RE\ (MAX)} – V_{SENSE(MAX)} – V_{LOAD\ (MAX)}$$

where

- $2 \times V_{WIRE}$ is voltage drop across system wiring. If system wiring runs over a length (L) along one way, wire resistance per unit length is ρ and current in the loop is I_{LOOP}, then the voltage drop for one conductor can be given as:
- $V_{WIRE\ (MAX)} = \rho \times L \times I_{LOOP\ (MAX)}$
- For example, a 24-AWG wire has resistance per unit length (ρ) of 0.026 Ω/ft or 0.0755 Ω/m.
- V_{LOAD} is the voltage drop caused by the internal resistance of the loop receiver. The internal resistance of the loop receiver may vary from 50 Ω to 250 Ω.
- $V_{LOAD\ (MAX)} = R_{LOAD} \times I_{LOOP\ (MAX)}$
- V_{SENSE} is the voltage drop across 40-Ω sense resistor internal to the DAC.
- V_F is the forward-voltage drop across the reverse polarity protection diode.
- V_F = 0.7 V at 30 mA forward current (from TVS data sheet, *SM6T39CA Data Sheet* SM6T39CA). (31)

Rewriting Equation 31,

$$V_{SUPPLY\ (MIN)} > 0.2\ V + (2 \times \rho \times L \times I_{LOOP(MAX)}) + (2 \times 0.7\ V) + (100\ \Omega \times I_{LOOP\ (MAX)}) + 3.9\ V + (20\ \Omega \times I_{LOOP\ (MAX)}) + (40\ \Omega \times I_{LOOP\ (MAX)}) + (R_{LOAD} \times I_{LOOP(MAX)}) + (40\ \Omega \times I_{LOOP(MAX)}) + (R_{LOAD} \times I_{LOOP(MAX)}) \quad (32)$$

The maximum output current that can be sourced out of the OUT pin by DAC161S997, $I_{LOOP\ (MAX)}$, is approximately 24 mA.

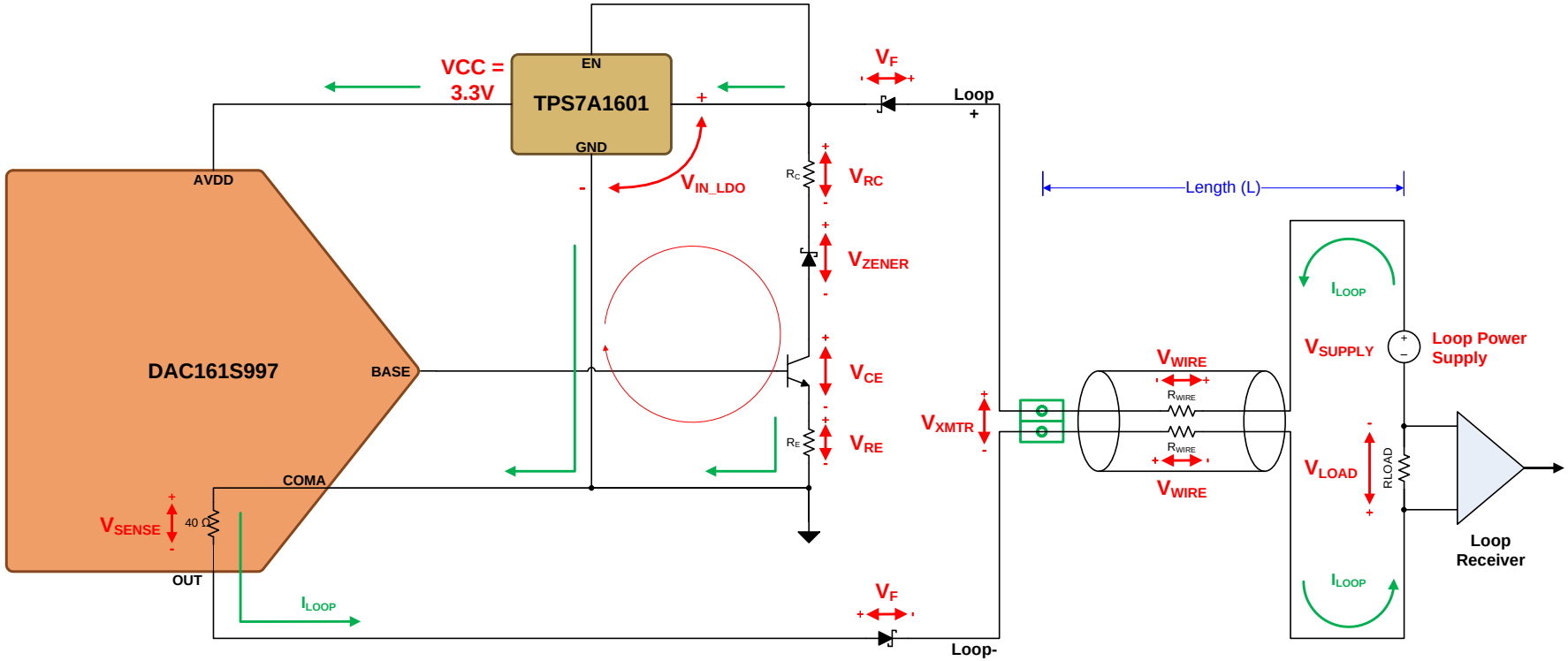


Figure 25. Series Voltage Drops in Current Loop System

LOOP CURRENT OUTPUT (OUT)				
I_{OUTMIN}	Minimum output current	Tested at DACCODE = 0x01C2 (7)	0.19	mA
I_{OUTMAX}	Maximum output current	Tested at DACCODE = 0xFFFF	23.95	mA
R_{OUT}	Output impedance		200	MΩ
	COMA to OUT voltage drop	I_{OUT} = 24 mA	960	mV

Figure 26. Specification for Loop Current Output

Next, examine what NAMUR NE43 has to say about loop current. NAMUR NE43 is an international association of process instrumentation user companies that have worked on improving the diagnostic coverage in 4- to 20-mA analog output transmitters to address associated safety issues. NAMUR NE43 provides the guideline for signaling-failure information to the safety-interlock systems over a 4- to 20-mA loop. NAMUR NE43 recommends using 3.8 mA to 20.5 mA as an extended measurement information range. NAMUR NE43 recommends using loop current below 3.6 mA or above 21 mA is in the diagnostic failure information range. Choose $I_{LOOP\ (MAX)}$ = 24 mA, depending upon DAC capability and also to comply with the NAMUR NE43 recommendation as shown in Figure 27.

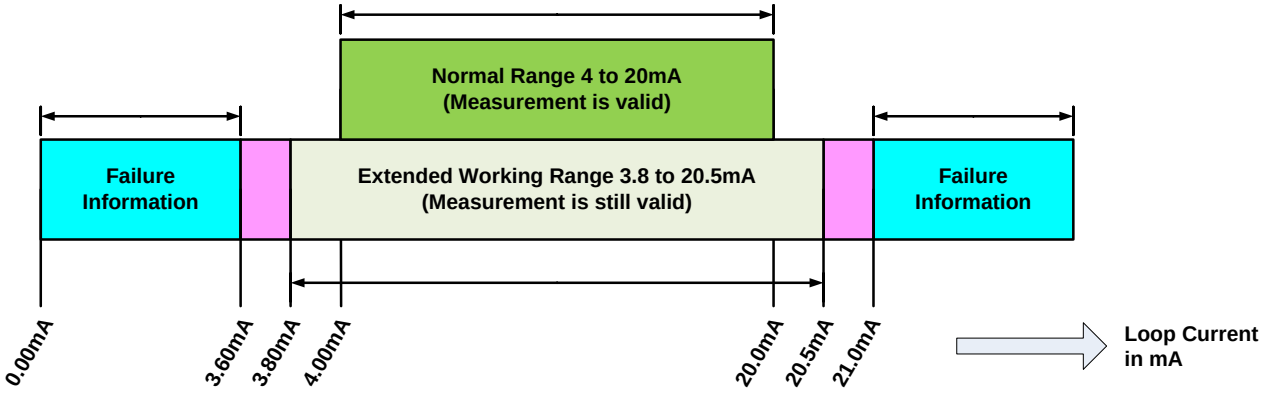


Figure 27. NAMUR NE43 Recommendation

Re-writing Equation 32,

$V_{SUPPLY\ (MIN)} > 0.2\ V + (2 \times \rho \times L \times 24\ mA) + (2 \times 0.7\ V) + (100\ \Omega \times 24\ mA) + 3.9\ V + (20\ \Omega \times 24\ mA) + (40\ \Omega \times 24\ mA) + (R_{LOAD} \times 24\ mA) + (40\ \Omega \times 24\ mA) + (R_{LOAD} \times 24\ mA)$ (33)

$V_{SUPPLY\ (MIN)} > 2 \times 0.026\ \Omega/ft \times L \times 24\ mA) + (R_{LOAD} \times 24\ mA) + 9.34\ V$ (34)

Figure 28 and Figure 29 give the loop supply voltages calculated using Equation 34 at different receiver load resistances and system wiring lengths.

System Wiring Length (in ft)

R_{LOAD}	2 X 50ft	2 X 500ft	2 X 1000ft	2 X 1500ft	2 X 2000ft
50Ω	10.6V	11.2V	11.8V	12.4V	13.1V
100Ω	11.8V	12.4V	13.0V	13.6V	14.3V
150Ω	13.0V	13.6V	14.2V	14.8V	15.5V
200Ω	14.2V	14.8V	15.4V	16.0V	16.7V
250Ω	15.4V	16.0V	16.6V	17.2V	17.9V

V_{SUPPLY} (vertical)

V_{SUPPLY} (horizontal)

Figure 28. Loop Power Supply Voltage for Different Loads and System Wiring length in Feet

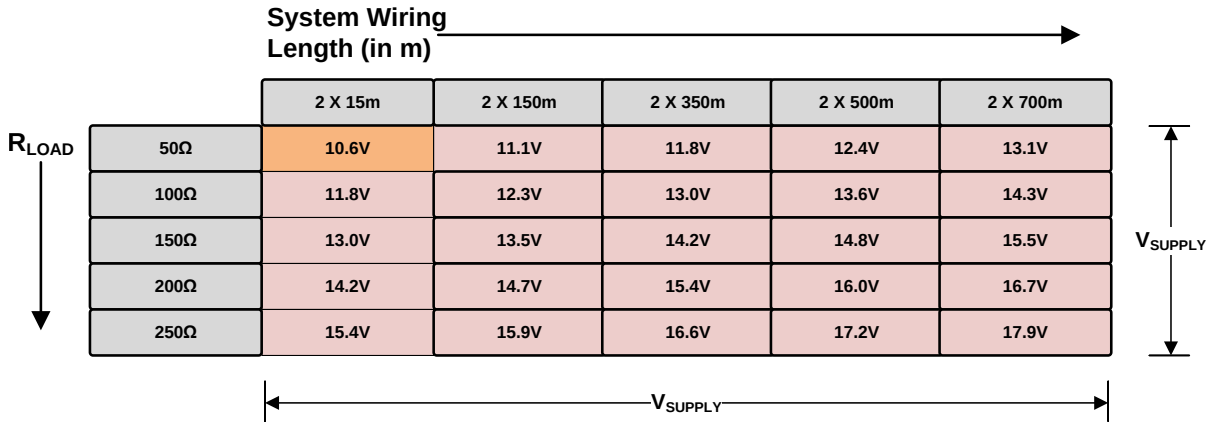


Figure 29. Loop Power Supply Voltage for Different Loads and System Wiring length in Meter

However, the maximum loop compliance voltage must not exceed the absolute maximum voltage rating of any device used in the loop. Therefore, select the device in order to meet the maximum loop compliance voltage requirement.

5.5.3 Selection of External BJT

DAC161S997 has been designed to use an external NPN transistor (BJT). Transistor Q1 conducts the majority of the signal-dependent, 4-20mA loop current. Using an external transistor avoids on-chip power dissipation and thermally-induced errors. Since the external transistor is part of a current control loop, the external transistor characteristics are not critical. Virtually any transistor with sufficient voltage, current and, power rating may be used. Basic requirements are as follows.

- V_{CEO} = 40 V minimum
- β = 40 minimum
- Must be able to handle power dissipation, $P_D = V_{CE\ (MAX)} \times I_{LOOP\ (MAX)}$

The NPN BJT should not be replaced with an N-channel Field Effect Transistor (FET) for the following reasons. Discrete FET's typically have high threshold voltages (V_{TH}), in the order of 1.5 V to 2 V, which is beyond the BASE output maximum range. Discrete FETs present higher load capacitance, which may degrade system stability margins. BASE output relies on the BJT's base current for biasing.

5.6 Power Design

The TPS7A16xx family of ultra-low power voltage regulators offers the benefit of ultra-low quiescent current, high-input voltage, and miniaturized, high-thermal performance packaging. The TPS7A16xx family LDOs accept a maximum input voltage of 60 V, which makes these LDOs ideal for use in industrial applications where high-voltage transients are present. The TPS7A1601 has an adjustable output voltage range from 1.194 V to 20 V. The nominal output of the device is set by two external resistors R_{14} and R_{18}, as shown in Figure 30. In order to set LDO output voltage, V_{CC} = 3.3 V, the resistor divider components are calculated using Equation 35.

$$R_{14} = R_{18} \times \left[\frac{V_{CC}}{V_{REF}} - 1 \right] \tag{35}$$

where

- V_{REF} = LDO Internal Reference Voltage = 1.193 V (typical)
- The selected values are R_{14} = 22.1 kΩ and R_{18} = 12.4 kΩ

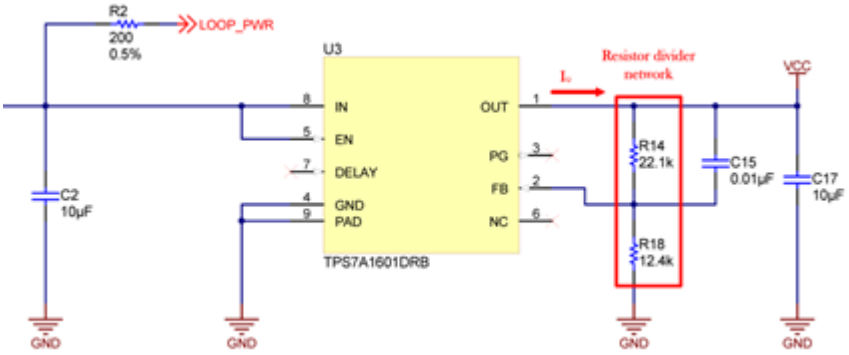


Figure 30. LDO Circuit with Feedback for Adjustable Output

The maximum power dissipation within the LDO is given by Equation 36.

$$P_D = (V_{IN\_LDO} - V_{CC}) \times I_Q \quad (36)$$

Assume a worst case scenario where the entire maximum loop power supply voltage, $V_{SUPPLY\ (MAX)}$ = 33 V, appears across the LDO input. The maximum allowed I_Q = 3.3 mA.

$$P_D = (33\ V - 3.3) \times 3.3\ mA = 98.01\ mW \quad (37)$$

The junction-to-ambient thermal resistance, θ_{JA}, of the TPS7A1601 device is 44.5°C/W.

For safe operation: $\theta_{JA} \times P_D + T_{A\ (MAX)} < T_{J\ (MAX)}$

The maximum junction temperature before the TPS7A1601 device shuts down is 170°C. From Equation 37, the worst case junction temperature of TPS7A1601 device is approximately 90°C, assuming an ambient temperature of 85°C. Therefore, a sufficient thermal-operating margin is available with the TPS7A1601 device, even accounting for the worse-case power dissipation.

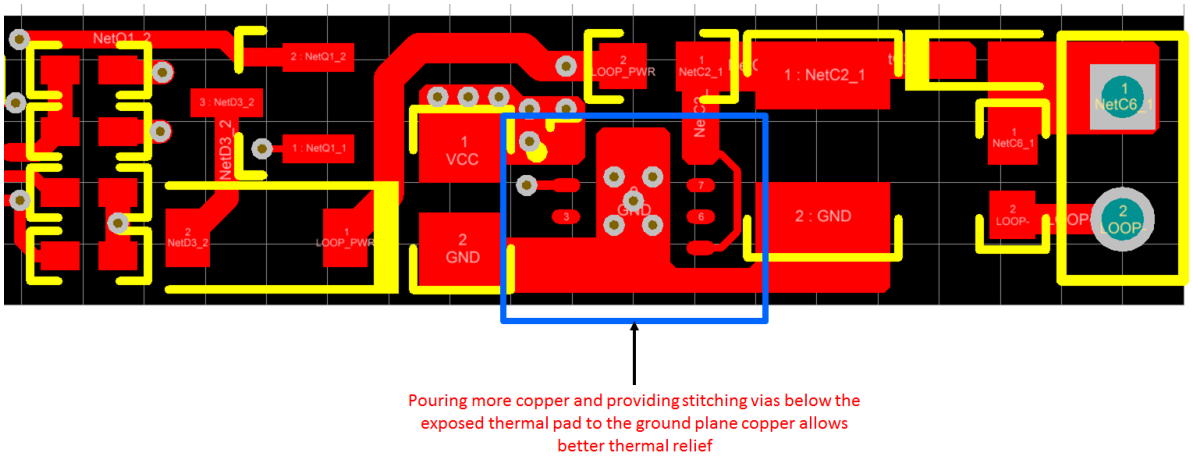


Figure 31. Layout for LDO Section

5.7 Protection

5.7.1 Protection for IEC61000-4

Primary Protection

The design uses a local transient-voltage suppressor (TVS) diode and a by-pass capacitor to reduce voltage spikes to lower, more manageable voltages to be in compliance with IEC61000-4 requirements.

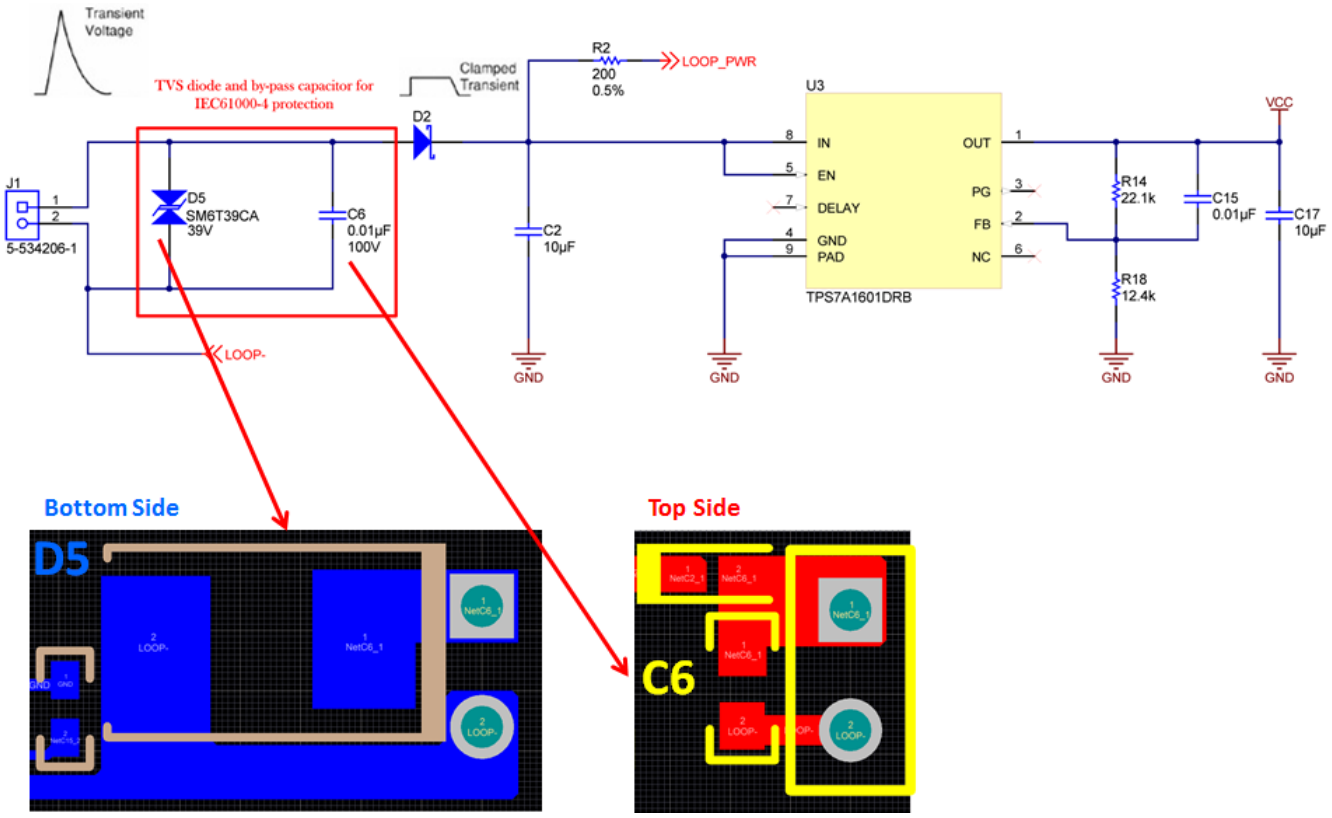


Figure 32. Protection Circuit and Layout

TVS Stand-off Voltage or Working Voltage (V_{RM})

Stand-off voltage or working voltage of the TVS diode, VRM, must be greater than the maximum continuous operating voltage, 33 V, at the place of intended protection in the circuit to prevent the TVS diode from conducting during normal operation.

Clamping Voltage (V_{CL}), Peak Pulse Current (I_{PP}) and Peak Pulse Power (P_{PP})

Most TVS diode manufacturers specify diode ratings with respect to conventional 10/1000 µs double exponential test pulse. However, the pulse used for the surge test is mostly 8/20 µs. In that case, the TVS manufacturer provides peak pulse power versus pulse time graph, which shows how the peak pulse power of the TVS is affected by a shorter or longer pulse duration. For shorter pulse widths, the TVS diode can withstand higher-peak pulse power.

The TPS7A1601 LDO can withstand a maximum transient input voltage up to 60 V. Therefore, the protection circuitry should be designed to handle ±1kV differential surge transient voltage (IEC 61000-4-5) safely and always clamp the surge transient voltage below 60 V, even at the higher ambient temperatures.

A few simple, but important mathematical equations must be solved for selecting the suitable TVS diode and to find out the application-specific TVS diode parameters. These equations are Equation 38 through Equation 43.

If R_D is given in the TVS data sheet, *SM6T39CA Data Sheet* SM6T39CA

$$V_{CL\ (MAX\ at\ 25°C)} = I_{PP} \times R_D + V_{BR(MAX\ at\ 25°C)} \quad (38)$$

If R_D is not given in the TVS data sheet, *SM6T39CA Data Sheet* SM6T39CA

$$V_{CL(MAX\ at\ 25°C)} = \frac{I_{PP}}{I_{PP(MAX)}}\left[V_{CL(MAX)} - V_{BR(MAX\ at\ 25°C)}\right] + V_{BR(MAX\ at\ 25°C)} \quad (39)$$

$$I_{PP} = \frac{(1000\ V - V_{CL})}{Z_S + R_S} \quad (40)$$

$$P_{PP} = V_{CL} \times I_{PP}$$

where

- R_D is the dynamic resistance
- V_{CL} is the application specific clamping voltage of the TVS diode at application-specific peak pulse current (I_{PP})
- Z_S is the source impedance of pulse generator and coupling/de-coupling network (CDN), Z_S = 42 Ω
- R_S is the external series resistance, R_S = 0 Ω (in this application) (41)

The TVS diode breakdown voltage (V_{BR}) has a positive voltage temperature coefficient (αT) specified in *SM6T39CA Data Sheet* SM6T39CA . To ensure that the requirements for circuit protection are met even at maximum ambient temperature of the application, it is important to take the voltage temperature coefficient (αT) into account while calculating the application specific clamping voltage.

$$\Delta V_{BR\ (MAX\ at\ Tamb)} = (\alpha T) \times (T_{amb} - 25°C) \times V_{BR\ (MAX\ at\ 25°C)}$$

where

- T_{amb} is ambient temperature which may go as high as 100°C in an industrial environment
- (αT) is voltage temperature coefficient (42)

The new equation for clamping voltage (Equation 43) at maximum ambient temperature can be given as follows.

$$V_{CL(MAX@T_{amb})} = \frac{I_{pp}}{I_{pp(MAX)}}\left[V_{CL(MAX@25°C)} - \left(V_{BR(MAX@25°C)} + \Delta V_{BR(MAX@T_{amb})}\right)\right] + \left[V_{BR(MAX@25°C)} + \Delta V_{BR(MAX@T_{amb})}\right] \quad (43)$$

The TVS diode selected for this design is SM6T39CA. The *SM6T39CA Data Sheet* SM6T39CA also specifies TVS diode parameters for 8/20 µs pulse. Some important TVS specifications at 25°C are as follows.

- $V_{RM\ (MAX)}$ = 33.3 V
- $V_{BR\ (MAX)}$ = 41 V
- $V_{CL\ (MAX)}$ = 69.7 V at $I_{PP\ (MAX)}$ = 57 A
- $P_{PP\ (MAX)}$ = 4000 Watts at 8/20 µs

Next, determine by some calculations if the SM6T39CA TVS diode is able to meet the requirements for 8/20 µs, 1 kV differential surge.

Using the TVS diode ratings, solve for I_{PP}, $V_{CL\ (MAX\ at\ 25°C)}$, P_{PP}, and $V_{CL\ (MAX\ at\ 100°C)}$.

I_{PP} equals approximately 22.6 A

$V_{CL\ (MAX\ at\ 25°C)}$ equals approximately 52.4 V, which is less than 60 V.

P_{PP} ≈ 1184.25 Watts (at 25°C), which is less 4000 watts with 8/20 µs pulse.

$V_{CL\ (MAX\ at\ 100°C)}$ equals approximately 54.22 V, which is still less than 60 V.

Secondary Protection

During the positive differential surge voltage, both the diodes (D2 and D6) are forward-biased. As a result, the clamped transient voltage appears across the transmitter's loop interface circuitry between the two traces as shown in Figure 34.

Before the feedback control loop reacts to the sudden and fast transient event in order to keep the loop current constant and soak the majority of the clamped transient voltage across collector-emitter of BJT, a high inrush current flows into the DAC's internal 40-Ω sense resistor (between OUT and COMA pins) via the C2 capacitor at the LDO input.

Most likely, a major portion of clamped transient voltage appears across OUT and COMA pins for a short time period. DAC may not be able to survive a voltage greater than 6 V between any two pins of the DAC.

In order to make sure the voltage between OUT and COMA pins does not exceed 6 V, it is worth adding a low-voltage, very low-leakage zener diode or a TVS-protection diode as secondary protection. A zener or TVS protection diode between the OUT and COMA pins ensures that the DAC survives the high voltage fast transient, but at the cost of reduced accuracy.

Therefore, selection of protection diode is very critical because the protection diode's leakage has a direct impact on the loop-current accuracy. The working voltage of the zener or TVS protection diode should be selected so that the working voltage does not affect the normal operation of the circuit.

$V_{BR} >> I_{LOOP\ (MAX)} \times 40\ \Omega$

$V_{BR} >> 24\ mA \times 40\ \Omega$

NOTE: This design does not have PCB pads to add the protection diode. However, to prove the concept, a 3.3 V/3 W zener diode was soldered manually and tested for 1-kV differential surge. For more details on surge testing, refer to Section 8.8.

ABSOLUTE MAXIMUM RATINGS(1)(2)

	MIN	MAX	UNIT
Supply voltage (VA, VD to COMA, COMD)	–0.3	6	V
Voltage between any two pins(3)		6	V
Current IN or OUT of any pin — except OUT pin(3)		5	mA

Figure 33. Absolute Maximum Rating for Voltage between Any Two Pins of DAC

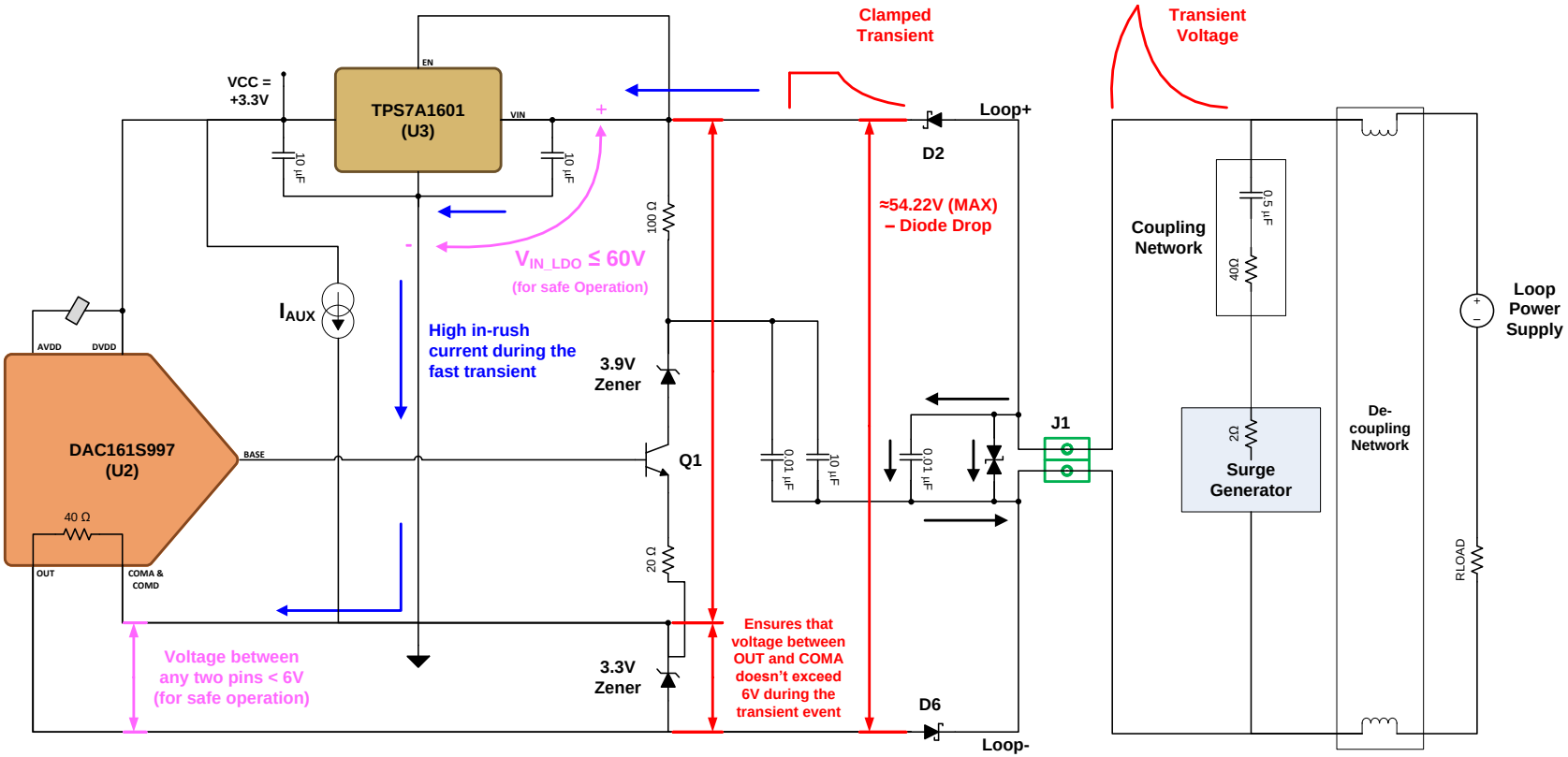


Figure 34. Circuit Protection during Positive Surge

During the negative differential surge voltage, both the diodes (D2 and D6) are reversed-biased as shown in Figure 35. As a result, the clamp transient voltage does not appear across the rest of the loop-interface circuitry. The pulse current is returned immediately through the front-end TVS diode and bypass capacitor back to the source.

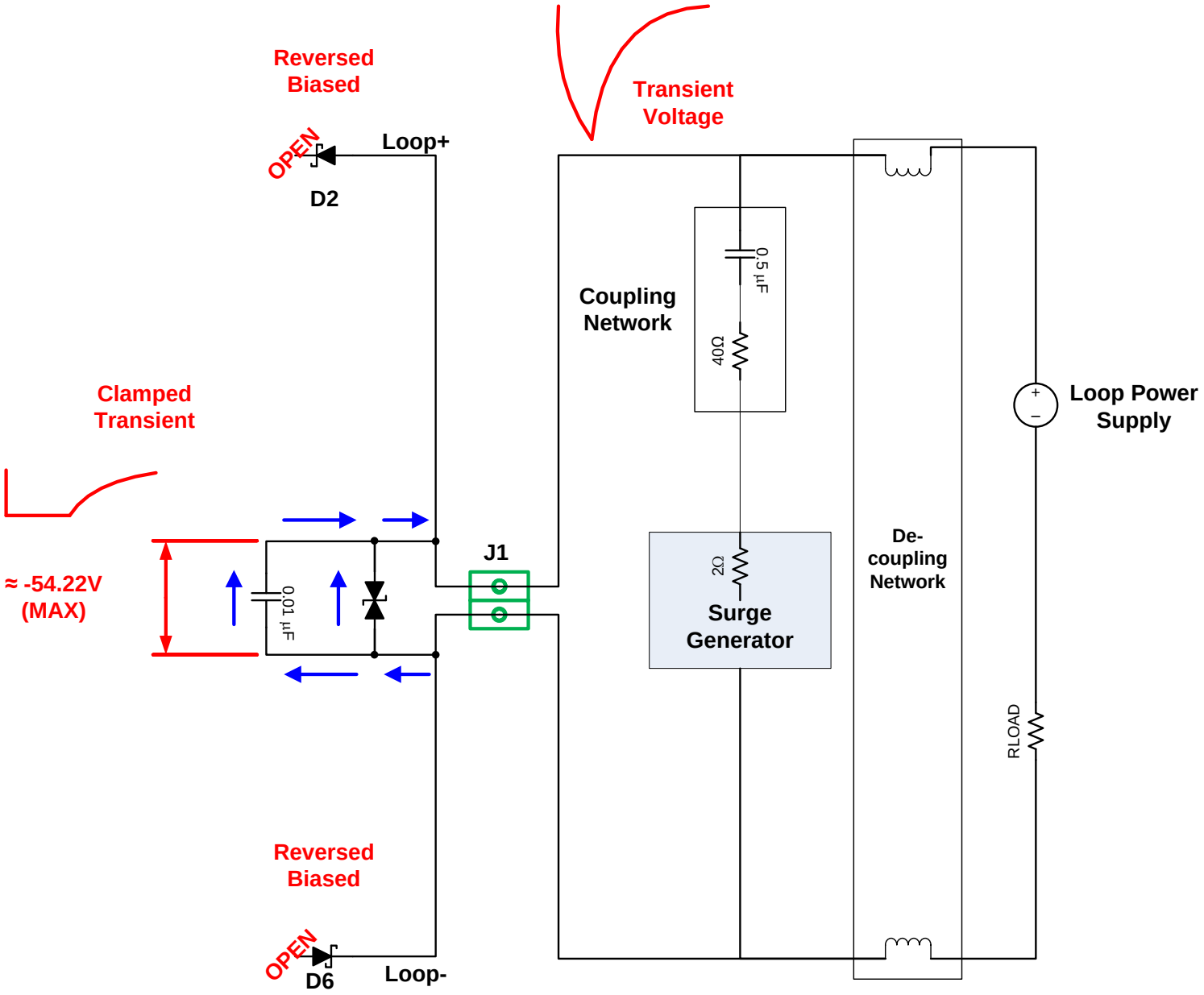


Figure 35. Circuit Protection during Negative Surge

5.7.2 Reverse Polarity Protection

To protect the system from accidently connecting the power to the board in reverse polarity, two protection diodes are used: one in the path of Loop+ and another in Loop– as shown in Figure 36. The diodes must have a reverse-voltage rating higher than the maximum clamping-voltage of the TVS in the event of high-voltage transient.

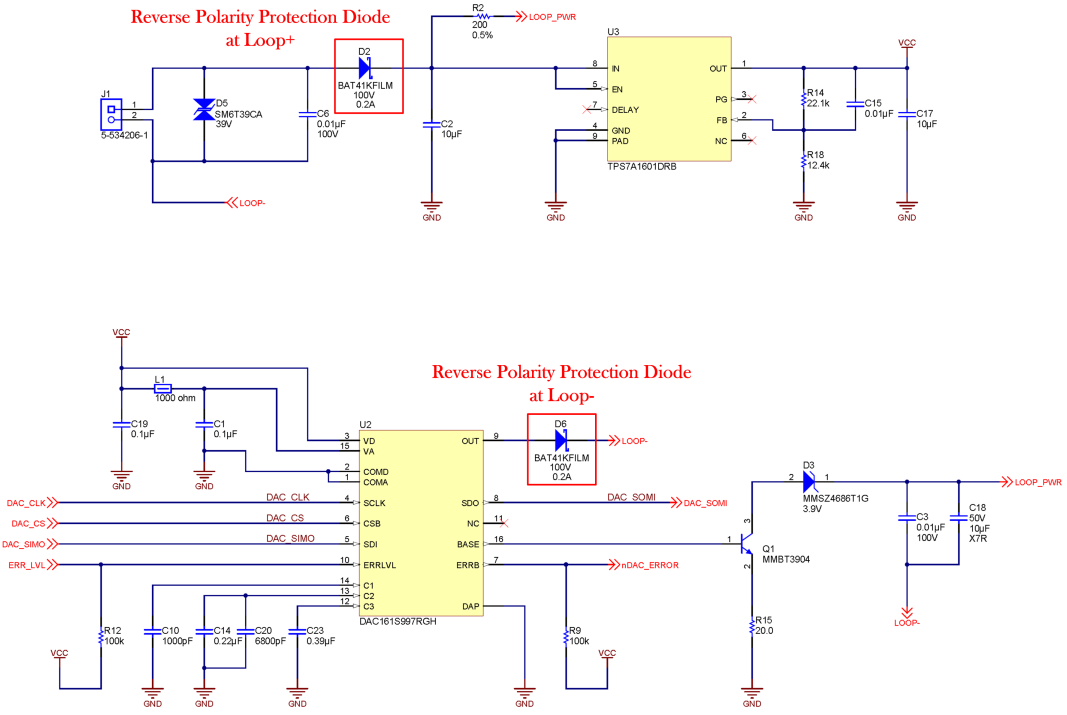


Figure 36. Reverse Polarity Protection using Schottky Diodes

6 Getting Started

6.1 Hardware Overview

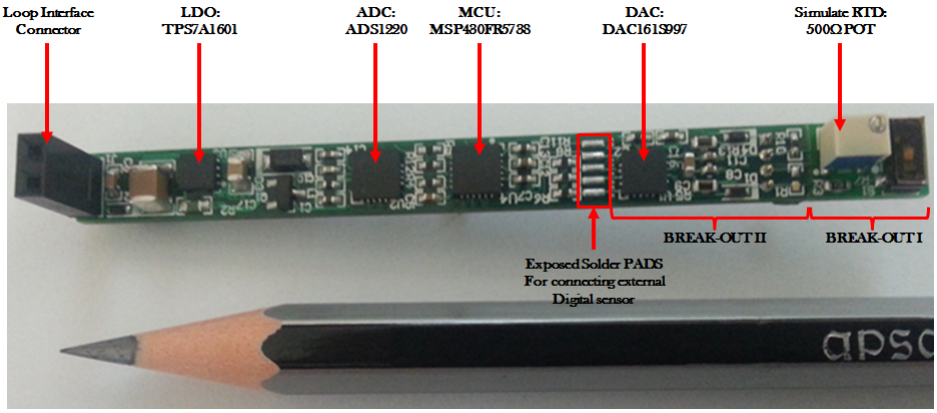


Figure 37. Top Side PCB Assembly View

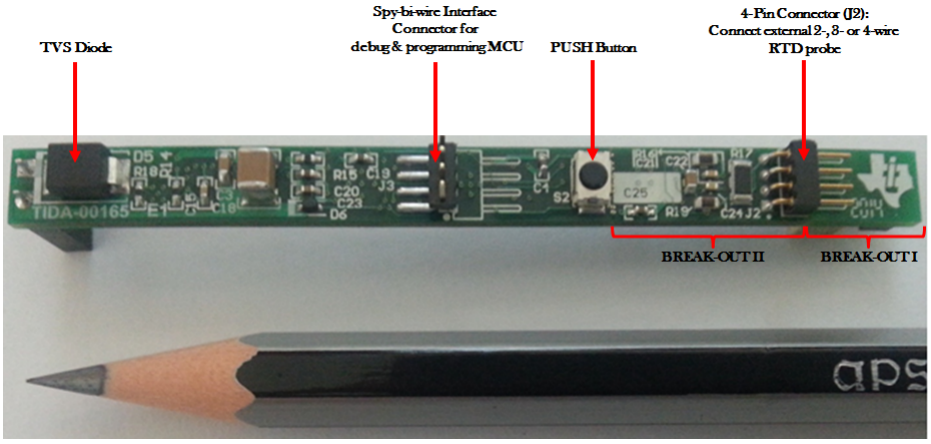


Figure 38. Bottom Side PCB Assembly View

6.2 Break-Out Options

The demo board has two break-out sections where the sensor signal chain can be interrupted for evaluation and prototyping purposes. Break-out I section contains one 500-Ω POT and one 300-Ω 0.1% resistor to simulate an actual RTD sensor. Break-out I section also contains a SPDT-slide switch to select either a POT or a 300-Ω resistor. Break-out II section contains a sensor analog front-end interface connector J2, a RC low-pass filter, and ADS1220. With break-out I and II sections intact, the TI design demo board is a complete 2-wire 4- to 20-mA current loop RTD temperature transmitter solution.

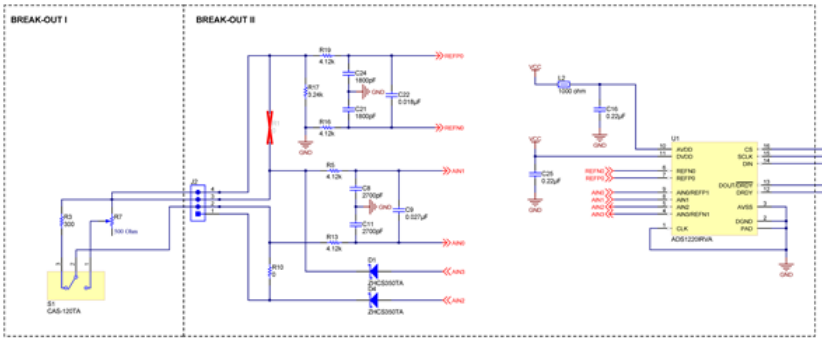


Figure 39. Break-out Section Options

6.3 Connecting Your Own RTD Sensor

To connect your own RTD sensor probe, separate the break-out I section from rest of the board. This removes the POT, the resistor and the SPDT switch. After breaking, the J2 connector can be used to interface with 2-, 3-, or 4-wire RTD sensor probes by populating R1 and R10 jumper resistor as per the instruction given in Figure 40.

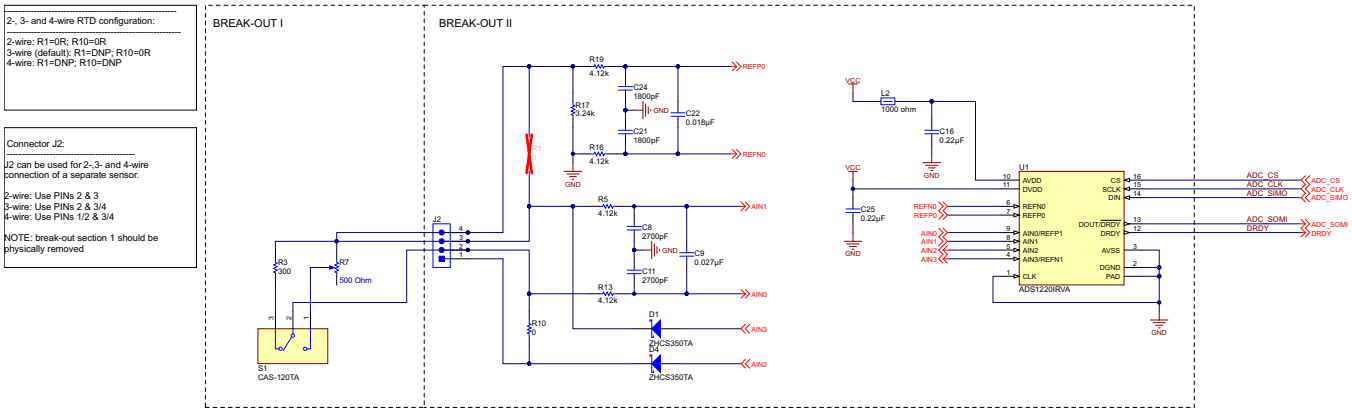
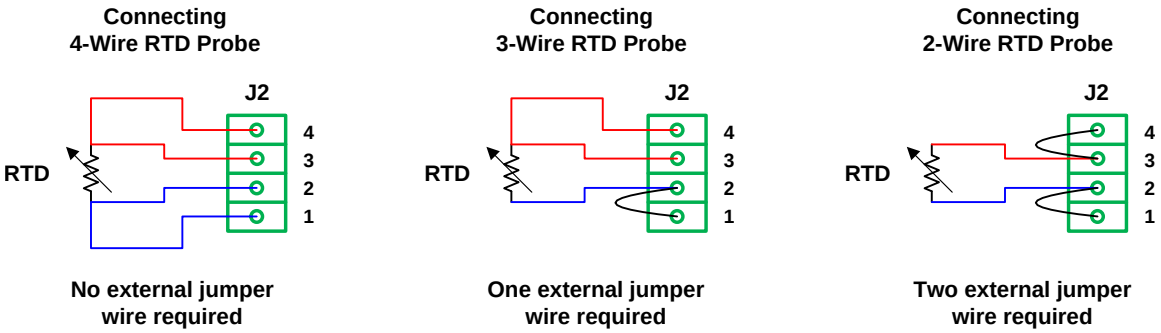


Figure 40. Connecting External 2-, 3- or 4-Wire RTD Sensor Probes using On-board Resistors

Another way of connecting a 2-, 3-, or 4-wire RTD sensor probe using external jumper wire is also illustrated in Figure 41.



*** Make sure R1 and R10 are DNP in all three cases**

Figure 41. Connecting External 2-, 3- or 4-Wire RTD Sensor Probes using External Jumper Wire

6.4 Connecting Your Own Digital Sensor

To connect your own digital sensor, both Break-out I and II sections must be first separated from rest of the board. This separation removes the J2 interface connector, the RC low-pass filters, and ADS1220. Now, five exposed pads on the PCB as shown in Figure 42 can be used to interface with an external digital sensor using the SPI/I2C interface from the MSP430FR5738 device. The SPI/I2C interface uses the eUSCI_B0 module of the MSP430FR5738 device. In SPI mode, the eUSCI_B0 module connects the device to an external sensor by way of four terminals: CS, UCB0CLK UCB0SIMO and UCB0SOMI. In I2C mode, the eUSCI_B0 module provides an interface between the MSP430FR5738 device and I2C-compatible sensors by way of two terminals: UCB0SDA and UCB0SCL.

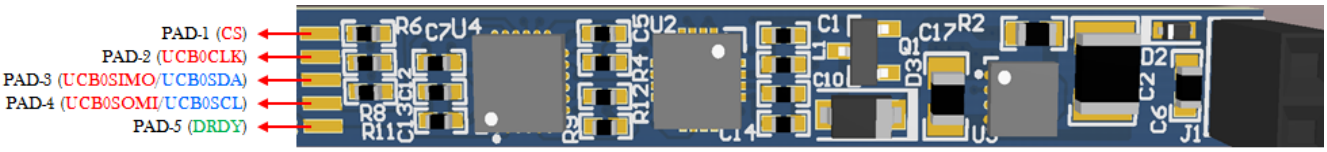


Figure 42. Exposed Pads for Connecting External Digital Sensor

WARNING

Please be careful breaking off the break-out sections. Due to the small form factor and small trace width, it is recommended to use a saw to remove the sections rather than breaking them away.

7 Software Update

The software code is designed to implement a temperature-transmitter application highlighting the ADS1220 to receive data from an RTD temperature probe and send out the temperature reading on a 4- to 20-mA signal using DAC161S997. The software code also addresses system level calibration — both offset and gain that can be implemented to improve ADC and DAC accuracy and also includes linear interpolation to address the nonlinearity of the RTD element.

For MSP430 firmware updates, Code Composer Studio™ (CCStudio) is recommended. CCStudio is an integrated development environment (IDE) for Texas Instruments embedded processor families. CCStudio comprises a suite of tools used to develop and debug embedded applications. CCStudio includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system, and many other features.

The intuitive IDE provides a single-user interface which takes the user through each step of the application development flow. For programming and debugging, the MSP430FR5738 implements an embedded emulation module (EEM). The EEM is accessed and controlled through either 4-wire JTAG mode or Spy-Bi-Wire mode. This reference design supports only the Spy-Bi-Wire mode. For more details on how the features of the EEM can be used together with CCStudio, see *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6*, Application Report SLAA393.

The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and the SBWTDIO (Spy-Bi-Wire test data input/output) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this SBWTCK pin is internally pulled to a ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For programming and debugging purposes, the SBWTCK, SBWTDIO, V_{CC} and GND from the Debugger need to be connected on J3.

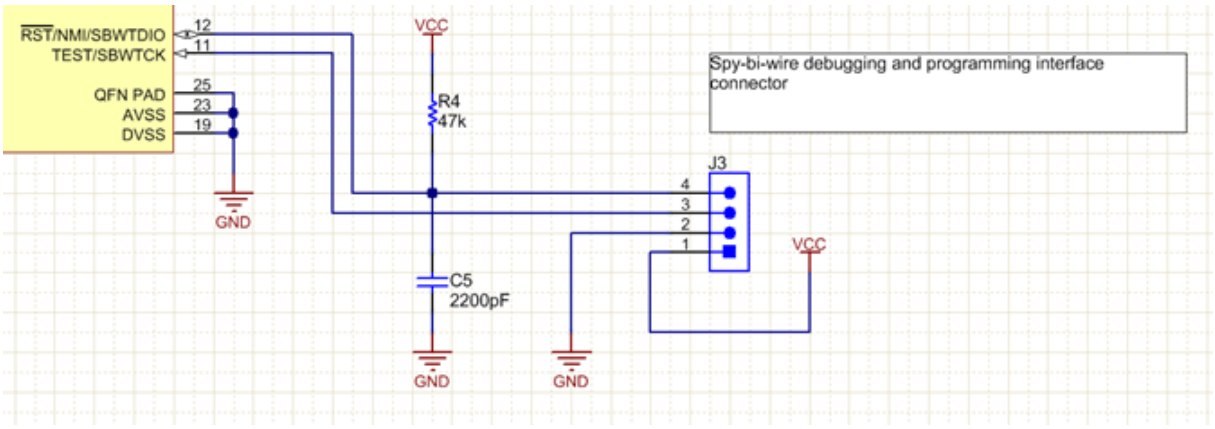


Figure 43. Spy-Bi-Wire Interface for Debugging and Programming of MCU

With the proper connections, a MSP430 debugger interface (such as the MSP-FET430UIF MSP-FET430UIF) can be used to program and debug code on the reference design.

Power during Debugging

WARNING

Special care should be taken during debug to avoid damages due to different power domain in conflicts (4-20mA loop power and debugger tools power), read following section carefully.

The TPS7A1601 supplies 3.3 V to the MSP430 if a voltage in the range of 10 V to 33 V is supplied to the 4- to 20-mA loop. Normally, the MSP430FR5738 is powered from this 3.3 V.

If this local 3.3-V supply from the TPS7A1601 is used during debugging, make sure that the VCC_Target pin from the debugger interface is connected to the V_{CC}. If there is no local power and the power from the debugger interface is used, make sure VCC_Tool pin from the debugger interface is connected to the V_{CC} and disconnect VCC_Target pin. Refer to Figure 44.

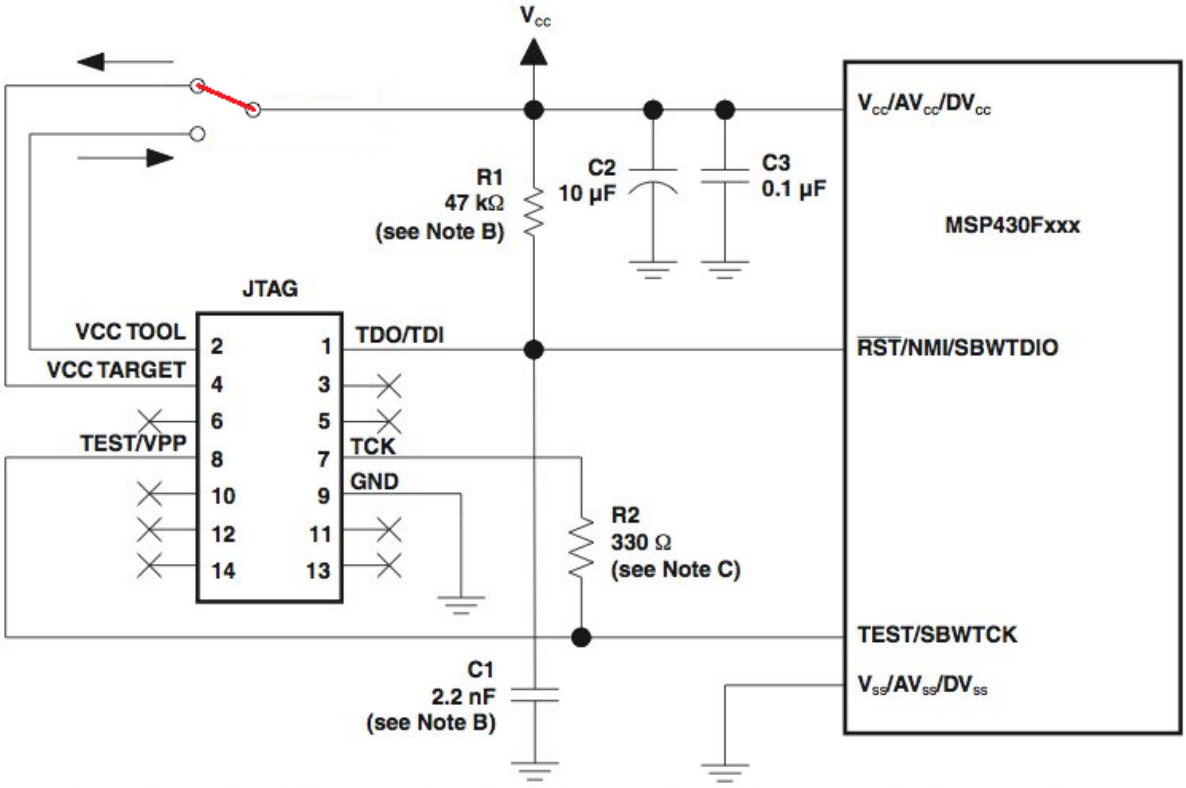


Figure 44. Power Supply Connection during Debugging

8 Test Data

The overall system performance is governed by ADC accuracy, DAC accuracy, and resolution. Section 8.2 characterizes the ADC for both resolution and error (adjusted for offset and gain calibration). The DAC is then characterized for both resolution and error (adjusted for offset and gain calibration). Finally, a full-system characterization is performed for maximum-measured error of the complete system.

NOTE: The test data in Section 8.1 through Section 8.8 was measured at room temperature using calibrated lab equipment, unless otherwise specified.

8.1 ADC Noise Histogram

The peak-to-peak noise of the acquisition system can be approximated from an ADC output code histogram. The RTD was replaced with a 390-Ω 0.01% tolerance, high-precision resistor to represent RTD resistance at full scale. ADS1220 was configured for continuous-conversion mode at a 20 SPS data rate in the software. Then, 1024 samples were recorded by the MSP430 MCU to generate the histogram plot shown in Figure 46.

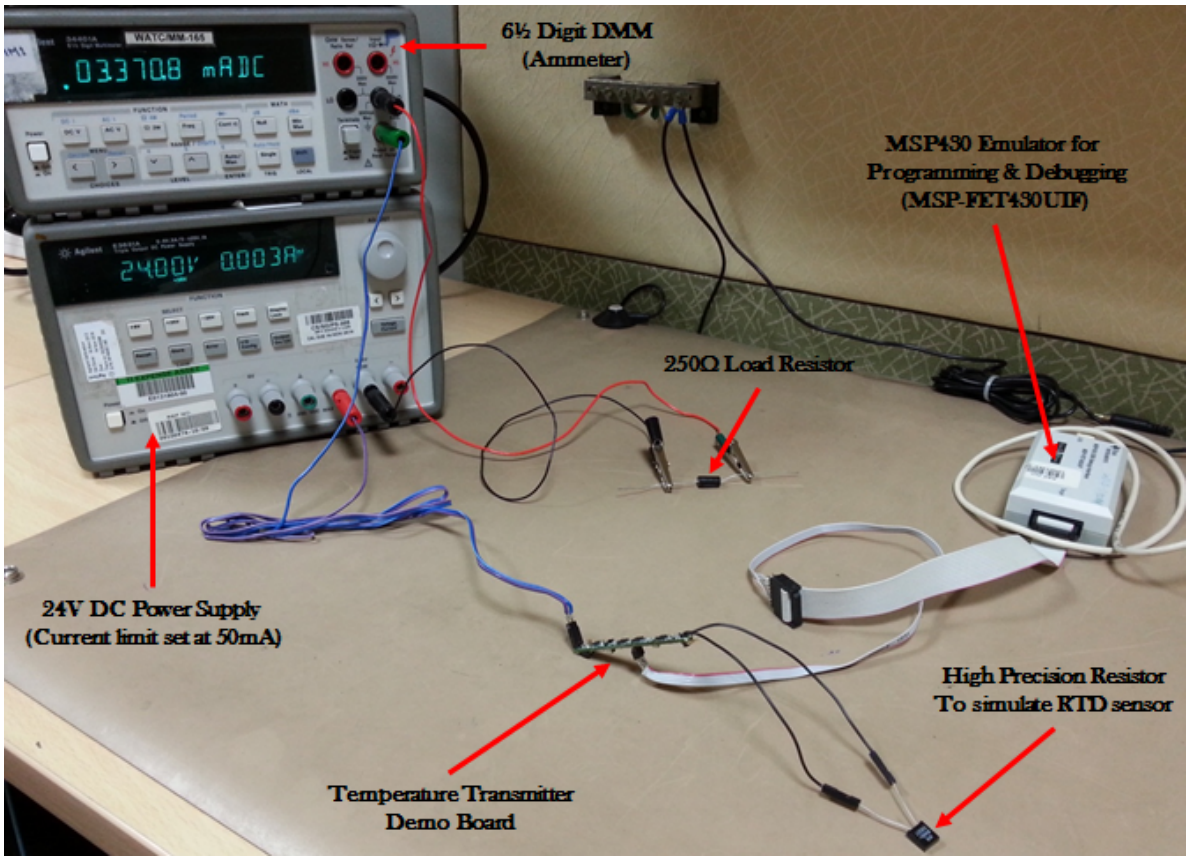


Figure 45. Basic Test Setup

The peak-to-peak spread of the codes in the histogram is around 282 codes. Equation 44 calculates the least-significant bit (LSB) size of the ADC, which is then used to translate the peak-to-peak noise voltage as given by Equation 44.

$$1\text{LSB} = \frac{2 \times V_{REF}}{\text{GAIN} \times (2^{24} - 1)} = \frac{2 \times 1.62\ \text{V}}{16 \times (2^{24} - 1)} = 12.07\text{nV} \quad (44)$$

Peak–to–Peak Noise = 1 LSB × ADC Code Spread = 12.07 nV × 282 = 3.41 μV_{PP} (45)

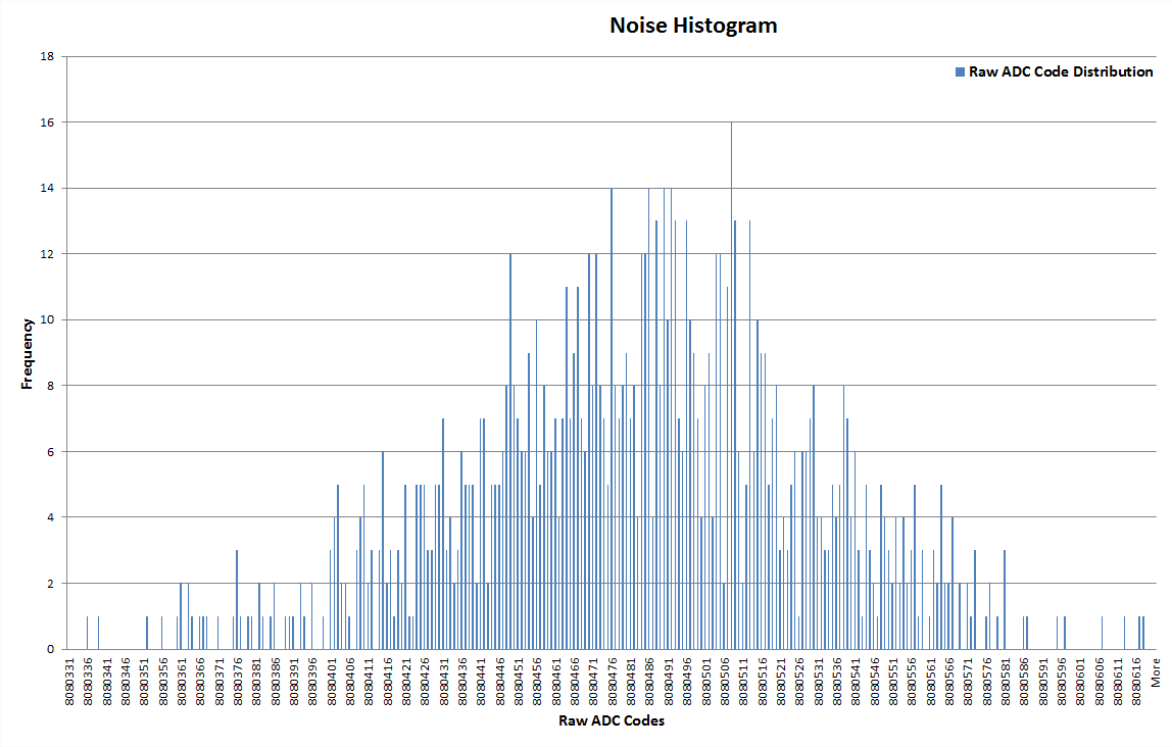


Figure 46. Raw ADC Code Distribution

The peak-to-peak noise can be used to calculate the total noise in degrees Celsius as given in Equation 46.

$$Noise\ (in\ °C) = \frac{Noise\ Voltage\ (in\ \mu V_{PP})}{PT100\ RTD\ Sensitivity\ X\ Excitation\ Current} = \frac{3.41 \mu V_{PP}}{0.385\ \frac{\Omega}{°C}\ X\ 250 \mu A} = 0.0354°C \quad (46)$$

The noise can be further reduced by implementing additional averaging or filtering in the software.

8.2 ADS1220 Error Characterization

To test the accuracy of the acquisition circuit alone, a series of high-precision discrete resistors were used as the input to the system. The offset error can be attributed largely due to the offset of the internal PGA and ADC, while the gain error can be attributed to the accuracy of the R_{REF} resistor and gain error of the internal PGA and ADC. The ADC error characterization includes corrections for any mismatch in excitation currents and offset and gain errors.

The following equipment was used for the testing.

- A 24-V DV power supply with current limit set to 50 mA.
- A 6½ digits multimeter, functional as a DC ammeter and connected in series with the power supply.
- Another 6½ digits multimeter to measure the high-precision resistors accurately using a 4-W resistance measurement method as shown in Figure 47.
- A MSP340 emulator (MSP-FET430UIF) for programming and debugging.
- A 250-Ω external-load resistor connected in series with the DC power supply and ammeter.

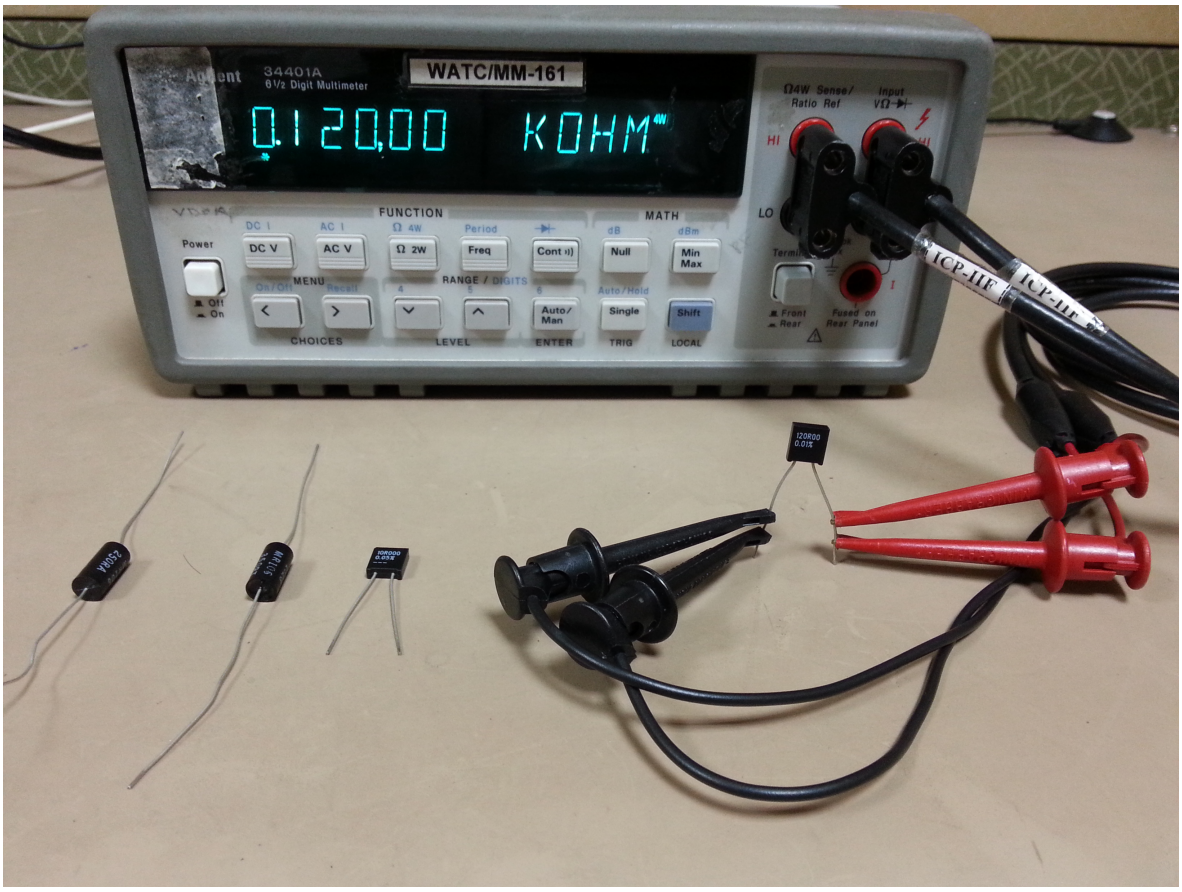


Figure 47. 4-Wire Resistance Measurement using 6½ Digits Multimeter

Use the following steps to carry out the testing.

1. Start with the smallest-value, precision resistor representing RTD resistance at the lowest scale. Measure the smallest-value, precision resistor's resistance using a 6½ digits multimeter in 4-W mode and record the measured value. Ensure that the measuring probes make a secure contact with resistor leads and avoid any human contact, since human contact may affect the resistance measurement.
2. Immediately connect the resistor already used in step 1. to the board.
3. Power-up the board.
4. Test software running in the MSP430 MCU to record the excitation-current and mismatch-corrected ADC code before and after offset calibration in the internal memory of the MSP430 MCU. The recorded samples are then exported to an Excel spreadsheet using CCS IDE on the PC. Preserve these samples safely in the Excel sheet for further calculations.
5. Repeat these steps until obtaining the highest-value precision resistor representing RTD resistance at full scale. Keep recording the sample in the Excel spreadsheet.
6. Gain calibration occurs when a full scale-precision resistor of 390 Ω is connected. A 390-Ω resistor corresponds to an approximately 848.36°C temperature, which is quite close to full scale temperature of 850°C. Then, the gain factor is determined by dividing the full-scale, reference-precision resistor with measured full-scale resistance after offset calibration. Finally, the gain correction is applied to all the measured resistances after offset calibration.

NOTE: Gain Calibration for the ADC: The MSP430 firmware algorithm averages a given number of measurements with offset correction applied to an expected result with a 390-Ω resistor connected to determine the gain calibration factor. To execute the algorithm, the S2 switch must be pressed with a 390-Ω resistor in place. If there is no previously stored gain calibration factor, a new one will be determined and stored in flash. Gain calibration should be performed after compensating for offset error.

Table 5. Gain Calibration for ADC

A	B	C	D	E	F = |B – E|	G	H	I = GAIN_FACTOR * H	J	K = |B – J|
Reference precision resistor value measured using 6½ digits multimeter in 4-W mode (in Ω)	Reference temperature corresponding to measured resistance, calculated using Callendar –Van Dusen Equation (in °C)	ADC output code with excitation current chopping (Without offset and gain calibration)	Measured resistance by ADC with excitation current chopping (Without offset and gain calibration)	Measured temperature by ADC with excitation current chopping (Without offset and gain calibration) (in °C)	Temperature error with excitation current chopping (Without offset and gain calibration) (in °C)	ADC output code with excitation current chopping and offset calibration (Without gain calibration)	Measured resistance with excitation current chopping and offset calibration (Without gain calibration) (in Ω)	Measured resistance with excitation current chopping, offset and gain calibration (in Ω)	Measured temperature with excitation current chopping, offset and gain calibration (in °C)	Temperature error with excitation current chopping, offset and gain calibration (in °C)
18.952	-199.58	387439	18.705	-199.571	0.009	387310	18.699	18.701	-199.58	4.64E-05
28.796	-176.15	595223	28.737	-176.138	0.012	595092	28.731	28.734	-176.145	0.004764
40.14	-149.14	830366	40.09	-149.12	0.02	830233	40.083	40.088	-149.124	0.015779
43.462	-141.88	892648	43.097	-141.882	0.002	892518	43.091	43.096	-141.885	0.004933
50.06	-125.33	1034108	49.926	-125.326	0.004	1033975	49.92	49.926	-125.327	0.003016
60.256	-100.74	1242014	59.964	-100.719	0.021	1241876	59.957	59.965	-100.718	0.022115
70.332	-75.89	1449494	69.981	-75.875	0.015	1449366	69.975	69.983	-75.8696	0.020408
100	-0.4	2068044	99.845	-0.397	0.003	2067916	99.839	99.85	-0.38291	0.017089
109.735	25.71	2278009	109.982	25.636	0.074	2277868	109.975	109.988	25.65176	0.058237
119.782	51.64	2485909	120.019	51.616	0.024	2485777	120.013	120.027	51.63601	0.003995
129.752	77.83	2693685	130.05	77.783	0.047	2693561	130.044	130.06	77.80792	0.022082
152.835	138.68	3170435	153.068	138.621	0.059	3170315	153.062	153.08	138.6536	0.026405
169.958	184.01	3519889	169.939	183.95	0.06	3519758	169.933	169.953	183.9868	0.023152
219.86	322.34	4555563	219.942	322.231	0.109	4555432	219.935	219.961	322.2865	0.053467
249.845	408.39	5177048	249.947	408.296	0.094	5176932	249.941	249.971	408.3649	0.025075
259.764	437.75	5385026	259.988	437.656	0.094	5384901	259.982	260.012	437.7285	0.021461
282.974	506.23	5861675	283	506.079	0.151	5861553	282.994	283.028	506.162	0.067979
349.92	715.45	7249585	350.008	715.287	0.163	7249449	350.002	350.043	715.3993	0.050681
359.725	747.84	7455099	359.93	747.676	0.164	7454974	359.924	359.967	747.7955	0.044507
368.508	776.84	7636855	368.706	776.654	0.186	7636737	368.7	368.743	776.7793	0.060749
389.896	848.63	8078743	390.04	848.493	0.137	8078627	390.034	390.08	848.6309	0.000948

Figure 48 shows temperature error before and after applying simple first order offset and gain calibration over a -200°C to 850°C temperature range. The temperature error still shows some variations, even after applying the offset and gain calibration. The temperature error is attributed mainly due to nonlinearity errors associated with the ADC and PT100 RTD look-up table. The nonlinearity errors are difficult to correct using a simple linear equation. Higher-order polynomial approximation may be used to correct the nonlinearity errors.

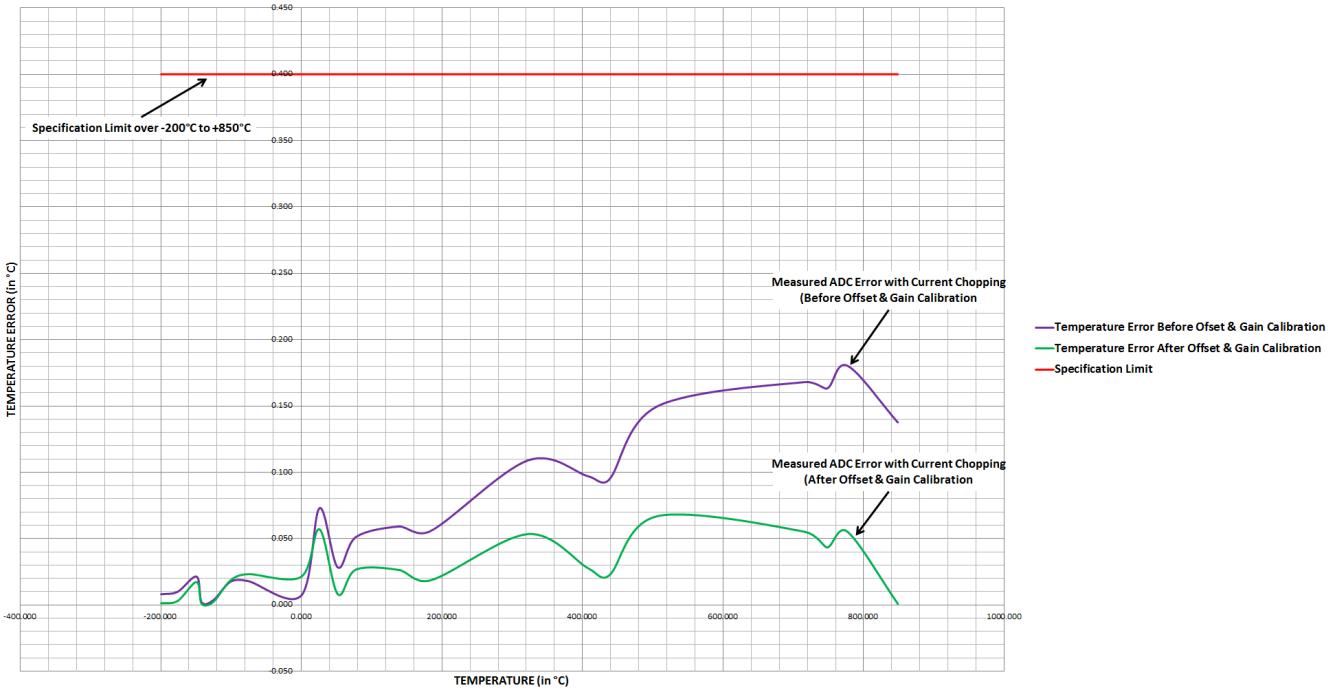


Figure 48. Measured ADC Error before and after Calibration

8.3 DAC Output Current Resolution

For this test, DAC output was programmed for a fixed 4-mA output current. More than 2500 samples were recorded over time using an 8½ digits multimeter. The minimum and maximum currents recorded were 4.00281 mA and 4.00375 mA, respectively. Therefore, the noise-free resolution in terms of output current is 0.76 µA.

8.4 DAC Error Characterization

To perform DAC error characterization, MSP430 MCU was programmed to generate the output-loop current from 4 mA to 20 mA in steps of 2 mA. The output current increased by 2 mA each time when the S2 switch was pressed. The output-loop current was measured using an 8½ digits multimeter.

Table 6. DAC Error Characterization

A	B	C = A – B	D	E = A – D
Ideal output loop current for ideal DAC value applied (in mA)	Output loop current measured using an 8½ digits multimeter before gain calibration (in mA)	Output current error before gain calibration (in mA)	Output loop current measured using an 8½ digits multimeter after gain calibration	Output current error after gain calibration (in mA)
4	4.00079	-0.00079	3.998563	0.001437
6	6.001443	-0.00144	5.998226	0.001774
8	8.002182	-0.00218	7.998213	0.001787
10	10.00314	-0.00314	9.997894	0.002106
12	12.00336	-0.00336	11.99704	0.00296
14	14.00434	-0.00434	13.99709	0.00291
16	16.00581	-0.00581	15.99776	0.00224
18	18.00755	-0.00755	17.9983	0.0017
20	20.00943	-0.00943	19.99915	0.00085

As shown in Figure 49, without gain calibration, negative gain error is seen in the loop current. This error increases linearly with loop current. A simple first order gain calibration implemented in the MSP430 fixes this error as shown in Figure 49. To increase DAC accuracy further, the MSP430 MCU can also further reduce the remaining error which is offset in nature.

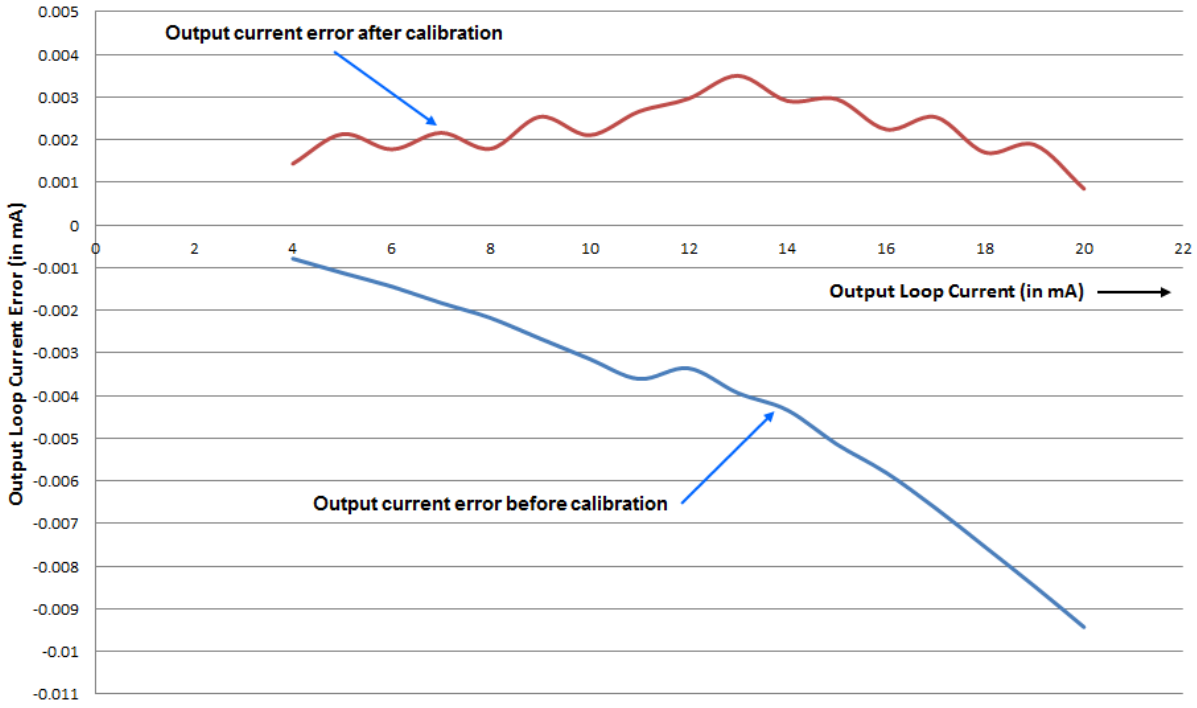


Figure 49. Measured Output Loop Current Error before and after Calibration

8.5 Maximum Measured Error of Complete System

After correcting the ADC and the DAC for gain and offset calibration, a complete system characterization was performed for maximum-measured error as given in Table 7 and Figure 50. In this setup, a power supply and a 8½ digits multimeter was used for loop-current measurement.

Table 7. Maximum Measured Error of Complete System after Offset and Gain Calibration of ADC and DAC

A	B	C	D	E	F = |B – E|
Reference precision resistor value measured using 6½ digits multimeter in 4-W mode (in °C)	Reference temperature corresponding to measured resistance, calculated using Callendar Van Dusen Equation (in °C)	Ideal loop current based on reference precision resistor (in mA)	Measured output loop current of the system for connected reference precision resistor (in mA)		Measured temperature error of complete system (in °C)
20	-196.57	4.052267	4.05143	-196.625	0.054906
33.027	-165.99	4.518248	4.5173	-166.052	0.062188
49.892	-125.41	5.13661	5.1356	-125.476	0.06625
59.927	-100.81	5.511467	5.5103	-100.887	0.076562
99.816	-0.47	7.040457	7.0392	-0.5525	0.0825
109.95	25.56	7.437105	7.4358	25.47438	0.085625
120	51.54	7.83299	7.83155	51.44547	0.094531
130.03	77.73	8.232076	8.2306	77.63313	0.096875
169.92	183.9	9.849905	9.848	183.775	0.125
219.94	322.23	11.95779	11.9558	322.0994	0.130625
229.99	350.78	12.39284	12.39075	350.643	0.137031
249.95	408.3	13.26933	13.2669	408.1403	0.159688
259.99	437.66	13.71672	13.7137	437.4616	0.198438
299.88	557.32	15.54011	15.538	557.1813	0.13875
350.02	715.32	17.94773	17.9463	715.2259	0.094062
360.07	748.1	18.44724	18.4461	748.0253	0.074687
369.98	780.89	18.9469	18.946	780.8313	0.05875
389.67	847.23	19.95779	19.959	847.3094	0.079375

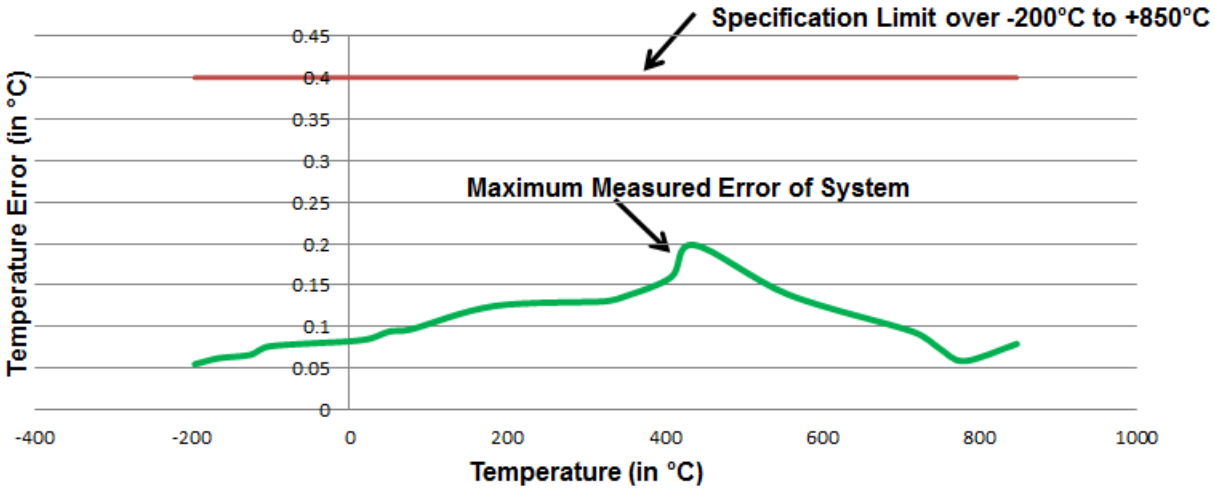


Figure 50. Maximum Measured Error of Complete System

8.6 Power Supply Influence

For the power-supply influence test, the power supply was vetted from 10 V to 33 V and the corresponding loop-current change was recorded. The DAC output was programmed for fixed 4-mA output current for this measurement. The total deviation of loop current across the power supply range was approximately 0.30 µA, as shown in Figure 51.

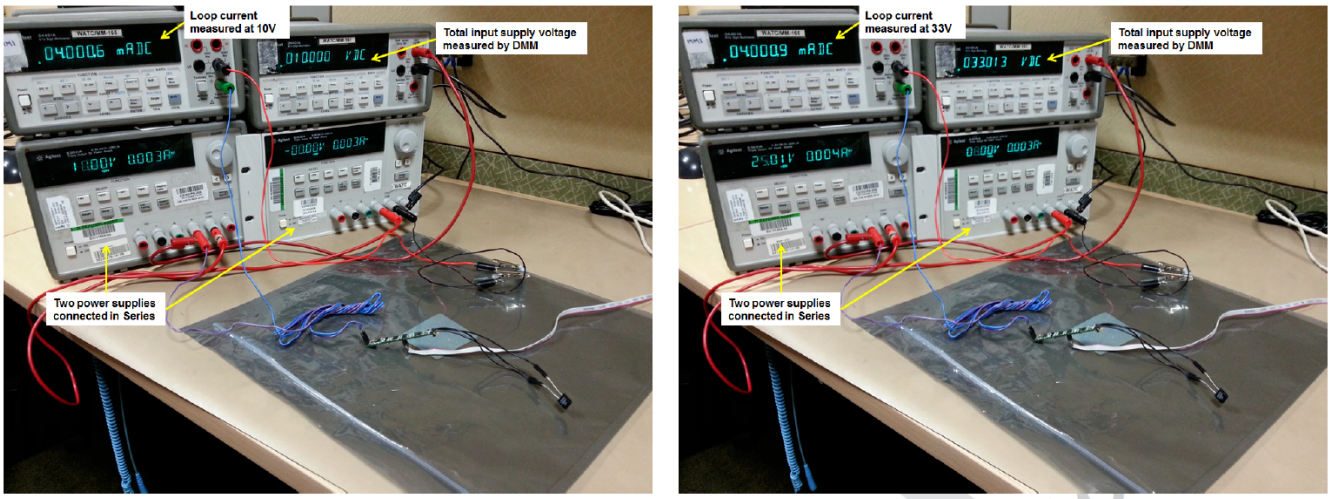


Figure 51. Power Supply Influence on the Output Loop Current

8.7 Reverse Polarity Test

For this test, a 24-V power supply was connected to the J1 loop interface connector in reverse polarity without any polarized capacitor, as shown in Figure 52. The leakage current drawn by the system recorded was only 0.2 µA.

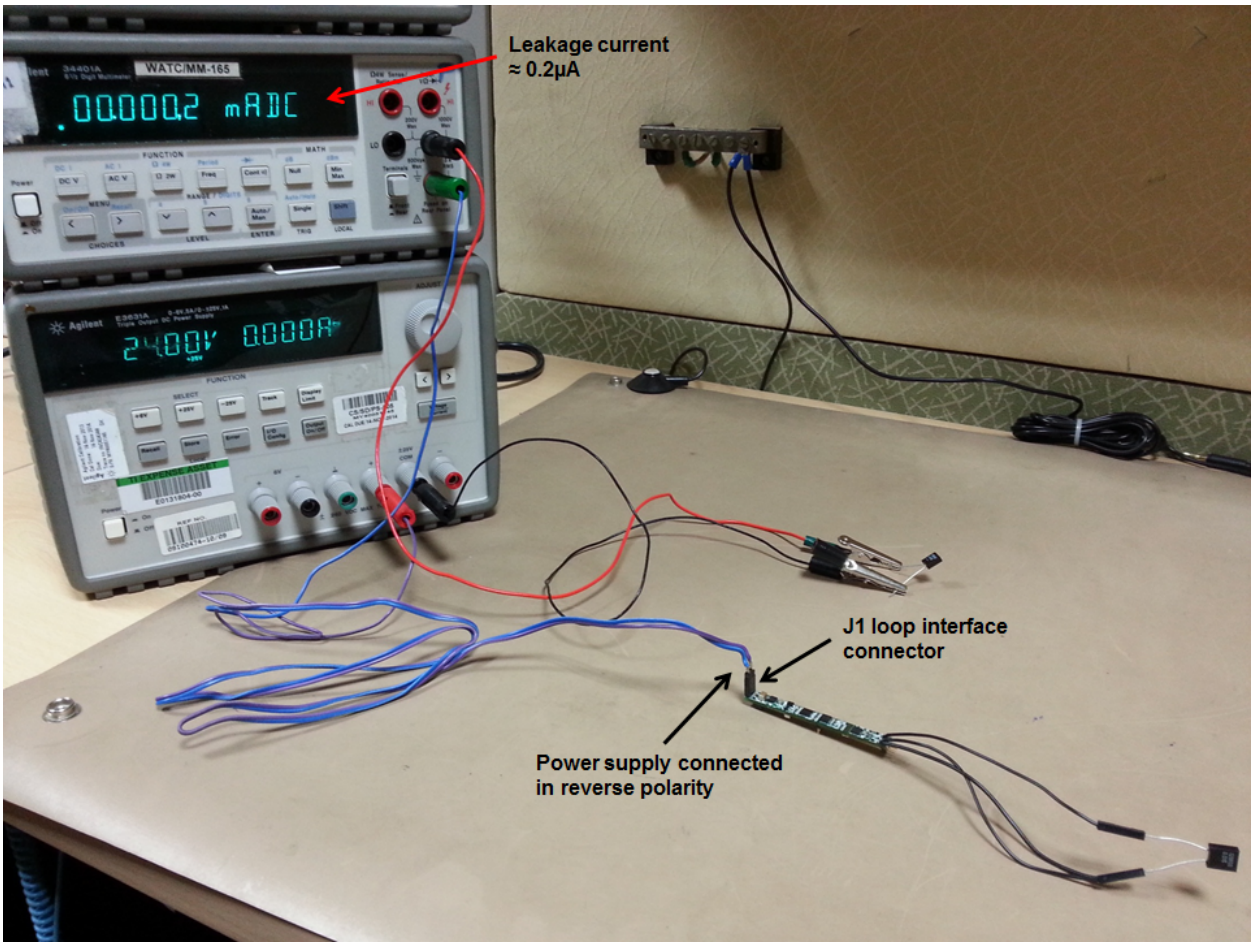


Figure 52. Reverse Polarity Protection Test Setup

8.8 Pre-compliance Surge Transient Immunity Test

The complete test setup and CDN clamp setting for pre-compliance surge transient immunity test are shown in Figure 53 and Figure 54, respectively.

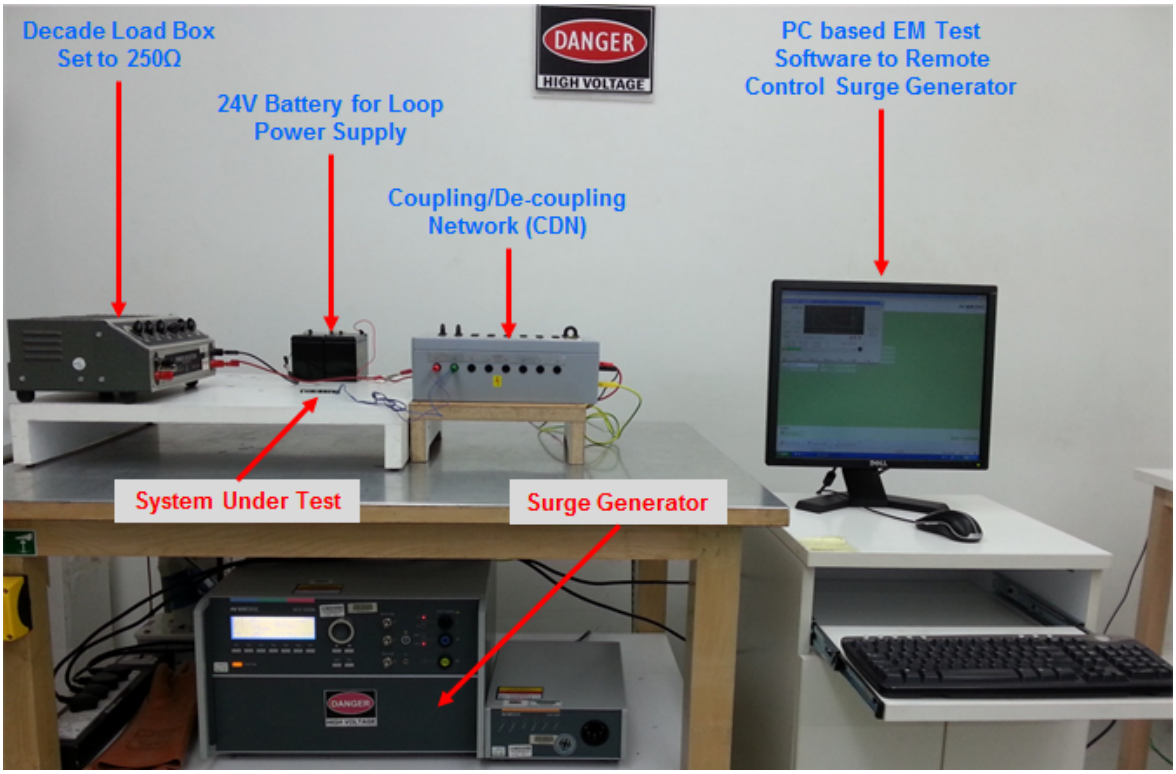


Figure 53. Surge Transient Immunity Test Setup

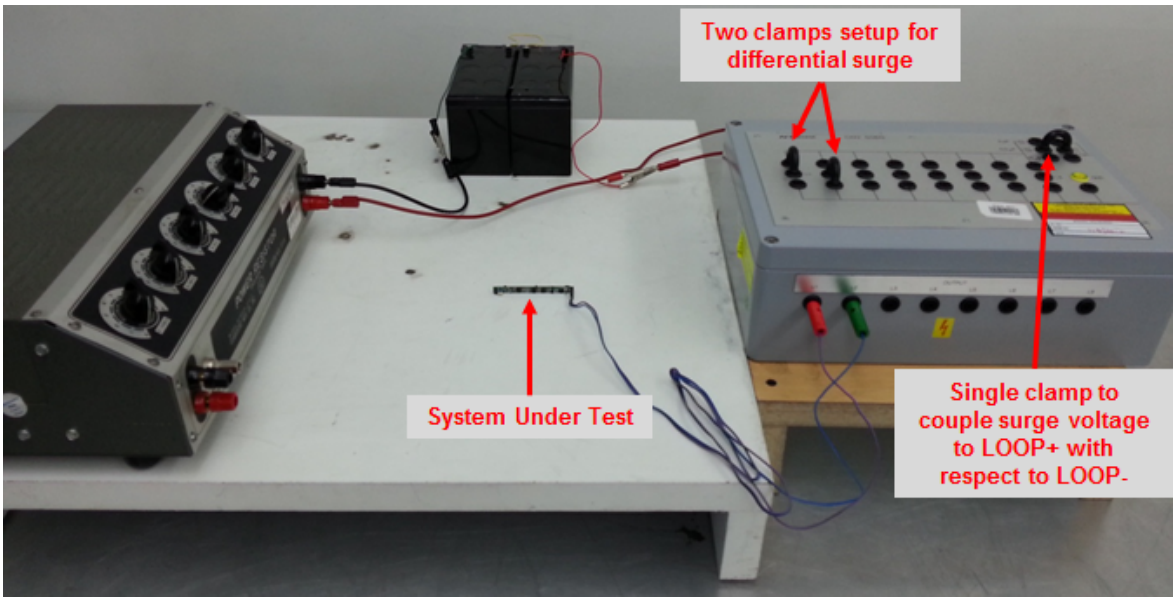


Figure 54. Clamp Setting on CDN for Differential Surge

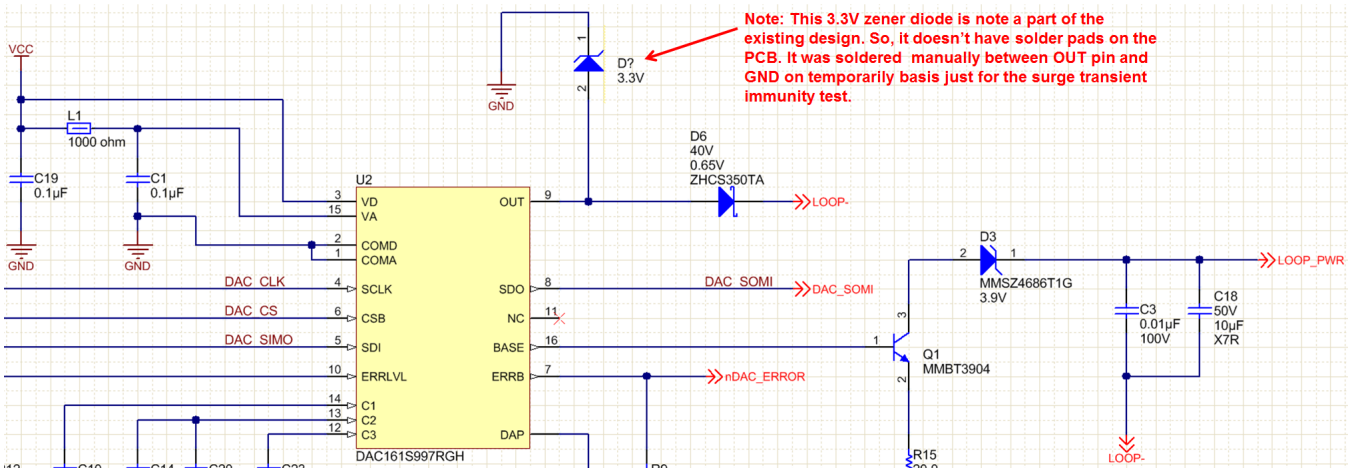


Figure 55. Additional 3.3–V Zener Required as Secondary Protection for DAC

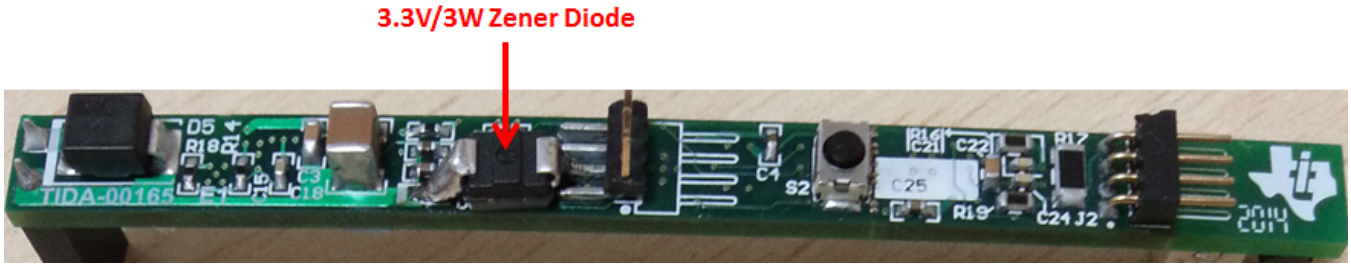


Figure 56. Mounting of 3.3–V Zener Diode for Surge Testing

For the surge transient immunity test, the 300-Ω resistor in the break-out I section was selected by switch S1 as a constant input to ADS1220, which makes DAC161S997 output fixed- loop current. The loop current was measured before and after the strike.

Table 8. IEC 61000-4 Test

IEC 61000-4 TEST	RESULT
IEC 61000-4-5: Surge transient immunity test; ±1kV line-line (DM) between loop power inputs (J1 connector). Five pulses of each polarity. Time between the two consecutive pulses was 60 seconds, 42-Ω coupling impedance, 8/20 µsec.	Meets category B. The system does not suffer any permanent damage and was found functional when monitored before and after the surge.

NOTE: The surge transient immunity test was performed only on loop-power input, that is, the J1 interface connector.

9 Design Files

9.1 Schematics

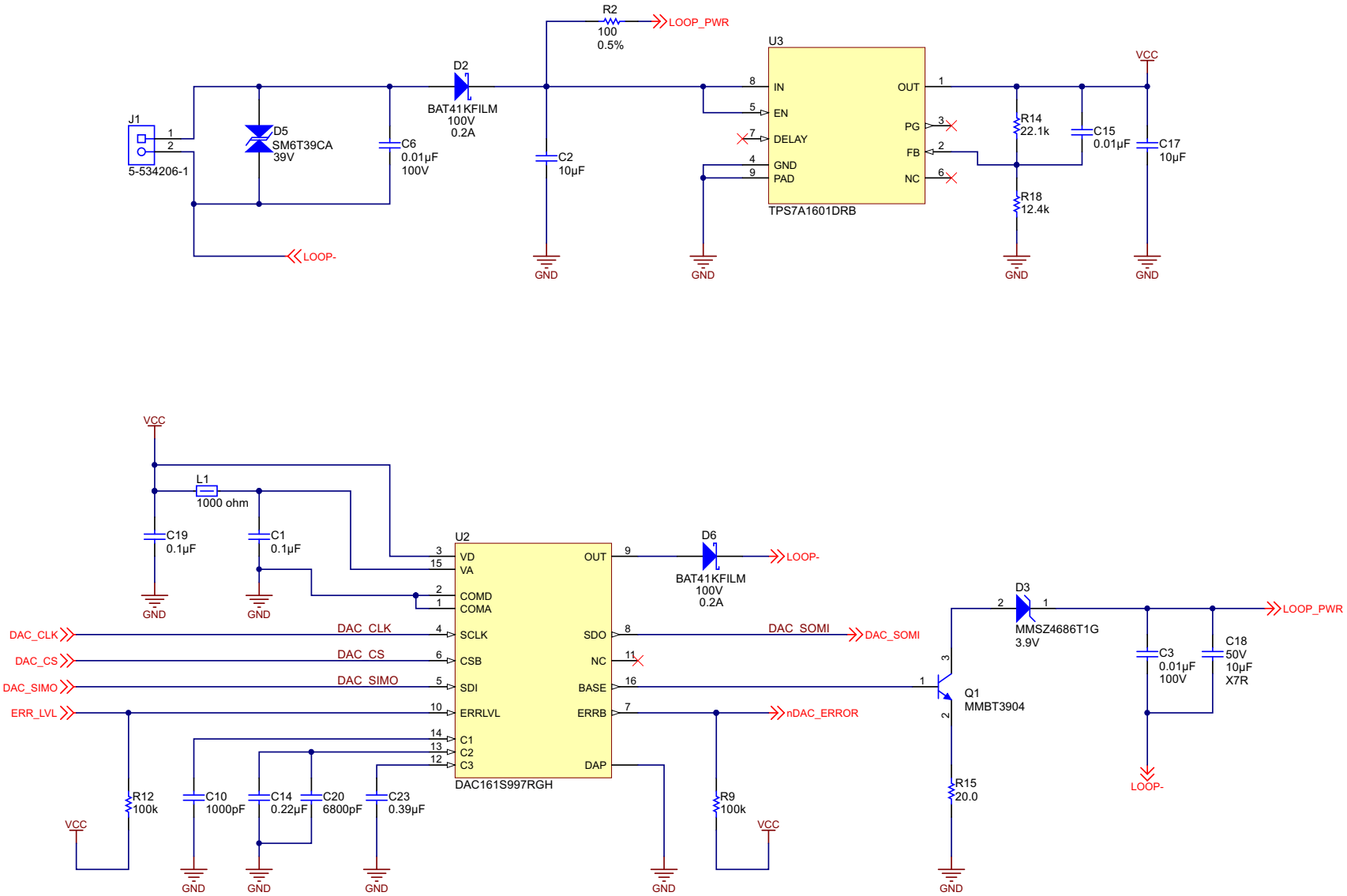


Figure 57. Schematics - Page 2

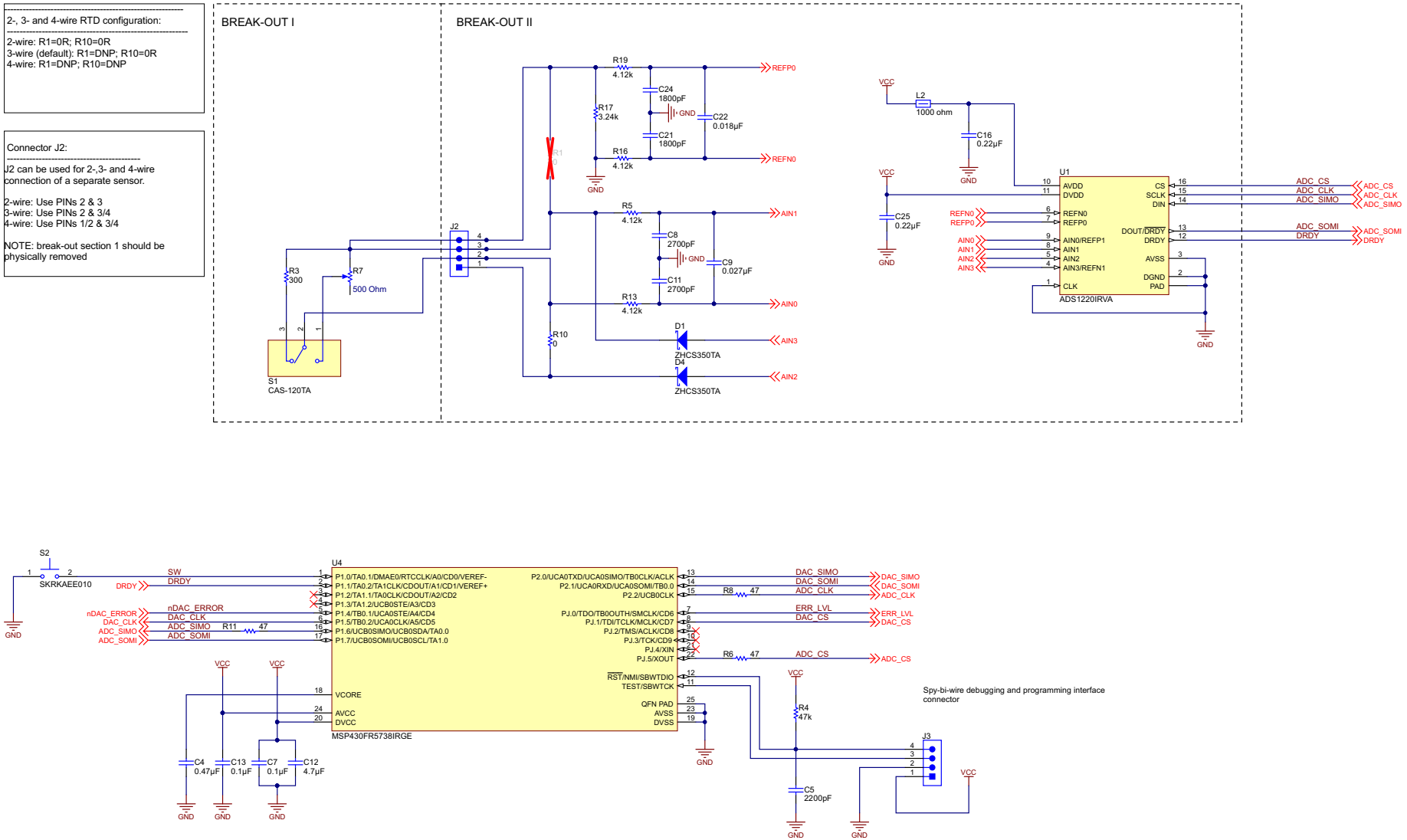


Figure 58. Schematics - Page 3

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00165.

Table 9. BOM

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QUANTITY	ROHS
Fitted	Printed Circuit Board	!PCB1		Any	TIDA-00165	1	O
Fitted	CAP, CERM, 0.1uF, 6.3V, +/-10%, X5R, 0402	C1, C7, C13, C19	0402	TDK	C1005X5R0J104K	4	Y
Fitted	CAP, CERM, 10uF, 50V, +/-10%, X7R, 1210	C2, C18	1210	MuRata	GRM32ER71H106KA12L	2	Y
Fitted	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	C3, C6	0603	TDK	C1608X7R2A103K	2	Y
Fitted	CAP, CERM, 0.47uF, 6.3V, +/-10%, X5R, 0402	C4	0402	MuRata	GRM155R60J474KE19D	1	Y
Fitted	CAP, CERM, 2200pF, 6.3V, +/-10%, X7R, 0402	C5	0402	MuRata	GRM155R70J222KA01D	1	Y
Fitted	CAP, CERM, 2700pF, 100V, +/-10%, X7R, 0402	C8, C11	0402S	MuRata	GRM155R72A272KA01D	2	Y
Fitted	CAP, CERM, 0.027uF, 100V, +/-10%, X7R, 0603	C9	0603S	Kemet	C0603C273K1RACTU	1	Y
Fitted	CAP, CERM, 1000pF, 6.3V, +/-10%, X5R, 0402	C10	0402	MuRata	GRM155R60J102KA01D	1	Y
Fitted	CAP, CERM, 4.7uF, 6.3V, +/-20%, X5R, 0402	C12	0402	TDK	C1005X5R0J475M050BC	1	Y
Fitted	CAP, CERM, 0.22uF, 6.3V, +/-10%, X5R, 0402	C14, C16, C25	0402	MuRata	GRM155R60J224KE01D	3	Y
Fitted	CAP, CERM, 0.01uF, 6.3V, +/-10%, X7R, 0402	C15	0402	MuRata	GRM155R70J103KA01D	1	Y
Fitted	CAP, CERM, 10uF, 6.3V, +/-10%, X7R, 0805	C17	0805_HV	MuRata	GRM21BR70J106KE76L	1	Y

Table 9. BOM (continued)

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QUANTITY	ROHS
Fitted	CAP, CERM, 6800pF, 25V, +/-10%, X7R, 0402	C20	0402	MuRata	GRM155R71E682KA01D	1	Y
Fitted	CAP, CERM, 1800pF, 100V, +/-10%, X7R, 0402	C21, C24	0402S	MuRata	GRM155R72A182KA01D	2	Y
Fitted	CAP, CERM, 0.018uF, 100V, +/-10%, X7R, 0603	C22	0603S	Kemet	C0603C183K1RACTU	1	Y
Fitted	CAP, CERM, 0.39uF, 10V, +/-10%, X5R, 0402	C23	0402	MuRata	GRM155R61A394KE15D	1	Y
Fitted	Diode, Schottky, 40V, 0.35A, SOD-523	D1, D4	SOD-523	Diodes Inc.	ZHCS350TA	2	Y
Fitted	DIODE SCHOTTKY 100V 0.2A SOD523	D2, D6	SOD-523	ST Microelectronics	BAT41KFILM	2	Y
Fitted	Diode, Zener, 3.9V, 500mW, SOD-123	D3	SOD-123	ON Semiconductor	MMSZ4686T1G	1	Y
Fitted	TVS DIODE 33.3VWM 69.7VC SMB	D5	SMB	STMicroelectronics	SM6T39CA	1	Y
Fitted	Connector, Receptacle, 100mil, 2x1, Gold plated, TH	J1	CONN_534206-1	TE Connectivity	5-534206-1	1	Y
Fitted	Header, 4x1, 50mil, R/A, TH	J2	Mill-Max_850-10-004-20-001000	Mill-Max	850-10-004-20-001000	1	Y
Fitted	Header, 4x1, 50mil, R/A, SMT	J3	Mill-max_850-10-004-40-001000	Mill-Max	850-10-004-40-001000	1	Y
Fitted	0.25A Ferrite Bead, 1000 ohm @ 100MHz, SMD	L1, L2	0402	MuRata	BLM15HG102SN1D	2	Y
Fitted	Transistor, NPN, 40V, 0.2A, SOT-23	Q1	SOT-23	Fairchild Semiconductor	MMBT3904	1	Y
Fitted	RES, 100 ohm, 0.5%, 0.1W, 0603	R2	0603	Yageo America	RT0603DRE07100RL	1	Y
Fitted	RES, 300 ohm, 0.1%, 0.1W, 0603	R3	0603S	Susumu Co Ltd	RG1608P-301-B-T5	1	Y
Fitted	RES, 47k ohm, 5%, 0.063W, 0402	R4	0402	Vishay-Dale	CRCW040247K0JNED	1	Y
Fitted	RES, 4.12k ohm, 0.1%, 0.1W, 0603	R5, R13, R16, R19	0603S	Susumu Co Ltd	RG1608P-4121-B-T5	4	Y

Table 9. BOM (continued)

FITTED	DESCRIPTION	DESIGNATOR	FOOTPRINT	MANUFACTURER	PARTNUMBER	QUANTITY	ROHS
Fitted	RES, 47 ohm, 5%, 0.063W, 0402	R6, R8, R11	0402	Vishay-Dale	CRCW040247R0JNED	3	Y
Fitted	TRIMMER 500 OHM 0.125W SMD	R7	Bourns_3223W	Bourns	3223W-1-501E	1	Y
Fitted	RES, 100k ohm, 5%, 0.063W, 0402	R9, R12	0402	Vishay-Dale	CRCW0402100KJNED	2	Y
Fitted	RES, 0 ohm, 5%, 0.063W, 0402	R10	0402	Vishay-Dale	CRCW04020000Z0ED	1	Y
Fitted	RES, 22.1k ohm, 1%, 0.063W, 0402	R14	0402	Vishay-Dale	CRCW040222K1FKED	1	Y
Fitted	RES, 20.0 ohm, 1%, 0.063W, 0402	R15	0402	Vishay-Dale	CRCW040220R0FKED	1	Y
Fitted	RES, 3.24k ohm, 0.1%, 0.333W, 1206	R17	1206L	TT Electronics/IRC	PFC-W1206R-12-3241-B	1	Y
Fitted	RES, 12.4k ohm, 1%, 0.063W, 0402	R18	0402	Vishay-Dale	CRCW040212K4FKED	1	Y
Fitted	Switch, Slide, SPDT 100mA, SMT	S1	SW_CAS-120TA	Copal Electronics	CAS-120TA	1	Y
Fitted	Switch, Push Button, SMD	S2	SW_SKRKAEE010	Alps	SKRKAEE010	1	Y
Fitted	Low-Power, Low-Noise, 24-Bit Analog-to-Digital Converter for Small Signal Sensors, RVA0016A	U1	RVA0016A	Texas Instruments	ADS1220IRVA	1	Y
Fitted	16-bit SPI Programmable DAC for 4-20mA Loops, RGH0016A	U2	RGH0016A	Texas Instruments	DAC161S997RGH	1	Y
Fitted	60-V, 5-µA IQ, 100-mA, Low-Dropout Voltage Regulator with Enable and Power-Good, DRB0008A	U3	DRB0008A	Texas Instruments	TPS7A1601DRB	1	Y
Fitted	24 MHz Mixed Signal Microcontroller, 1024 B SRAM and 17 GPIOs, -40 to 85 degC, RGE0024G	U4	RGE0024G	Texas Instruments	MSP430FR5738IRGE	1	Y
Not Fitted	RES, 0 ohm, 5%, 0.063W, 0402	R1	0402	Vishay-Dale	CRCW04020000Z0ED	0	Y

9.3 Layer Plots

To download the layer plots, see the design files at TIDA-00165.

NOTE: All artwork is viewed from the top side.

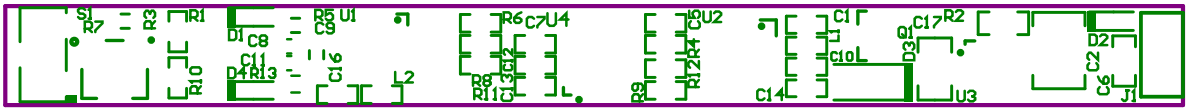


Figure 59. Top Overlay

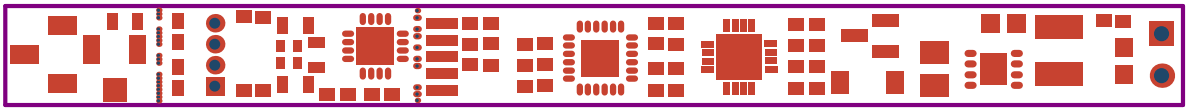


Figure 60. Top Solder Mask

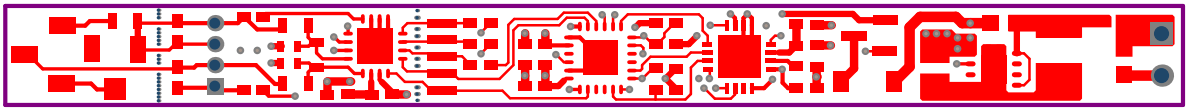


Figure 61. Top Electric (Top Layer)

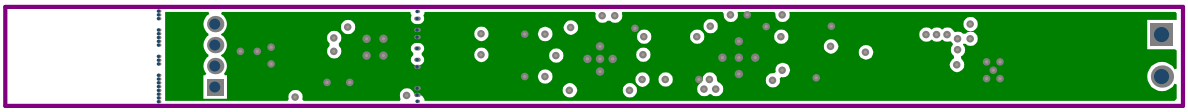


Figure 62. Ground Plane

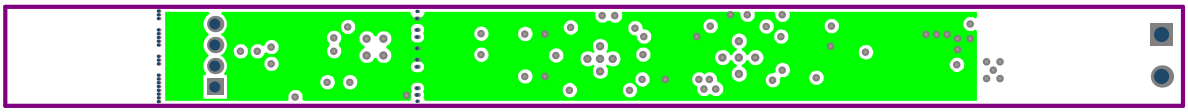


Figure 63. Power Plane (P2)

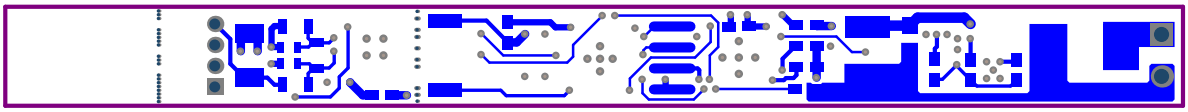


Figure 64. Bottom Electric (Bottom Layer)

Figure 65. Bottom Solder Mask

Figure 66. Bottom Overlay

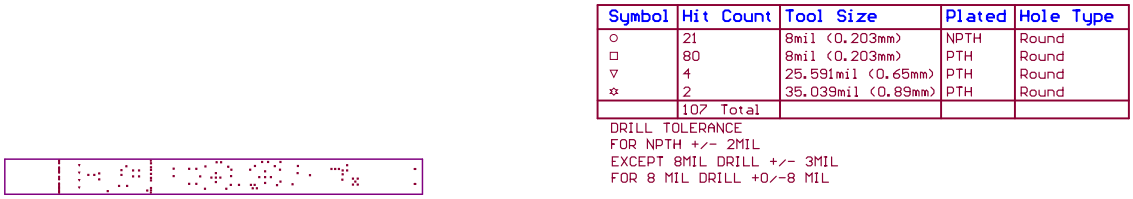


Figure 67. Drill Drawing

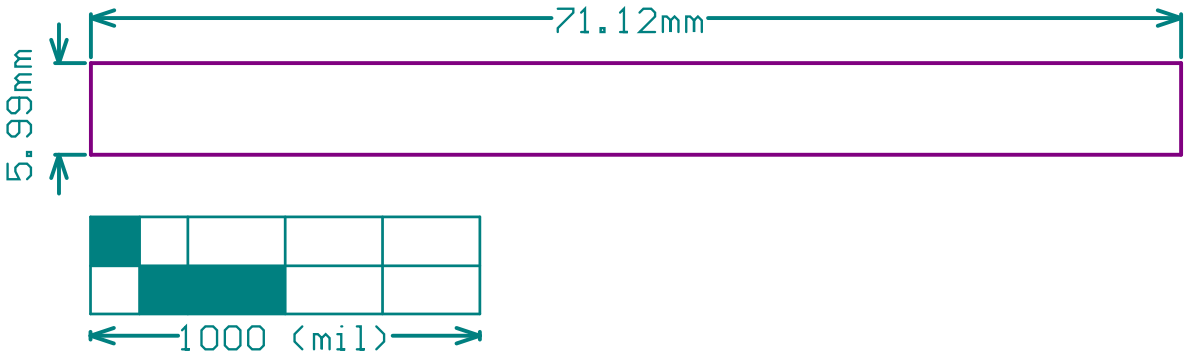


Figure 68. Layer Plot 10 - Board Dimensions

9.4 Assembly Drawings

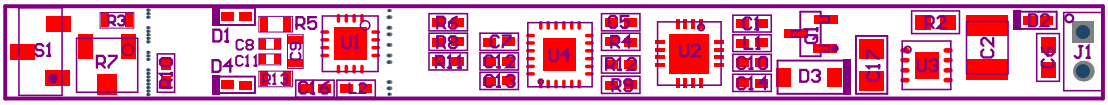


Figure 69. Top Assembly Drawing

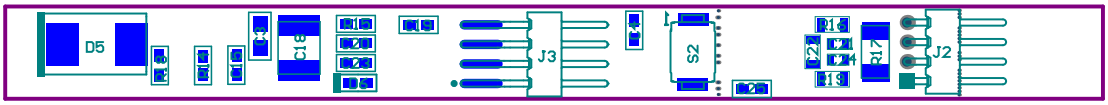


Figure 70. Bottom Assembly Drawing

9.5 Altium Project

To download the Altium project files, see the design files at TIDA-00165.

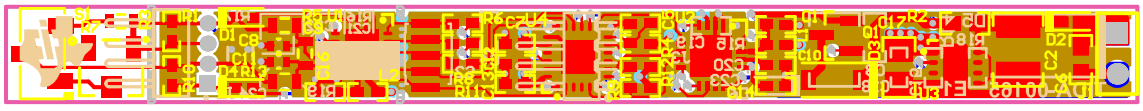


Figure 71. Altium All Layers

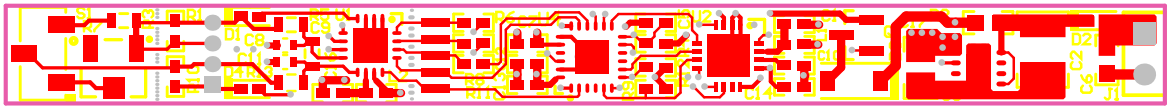


Figure 72. Altium Top Layer

9.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00165

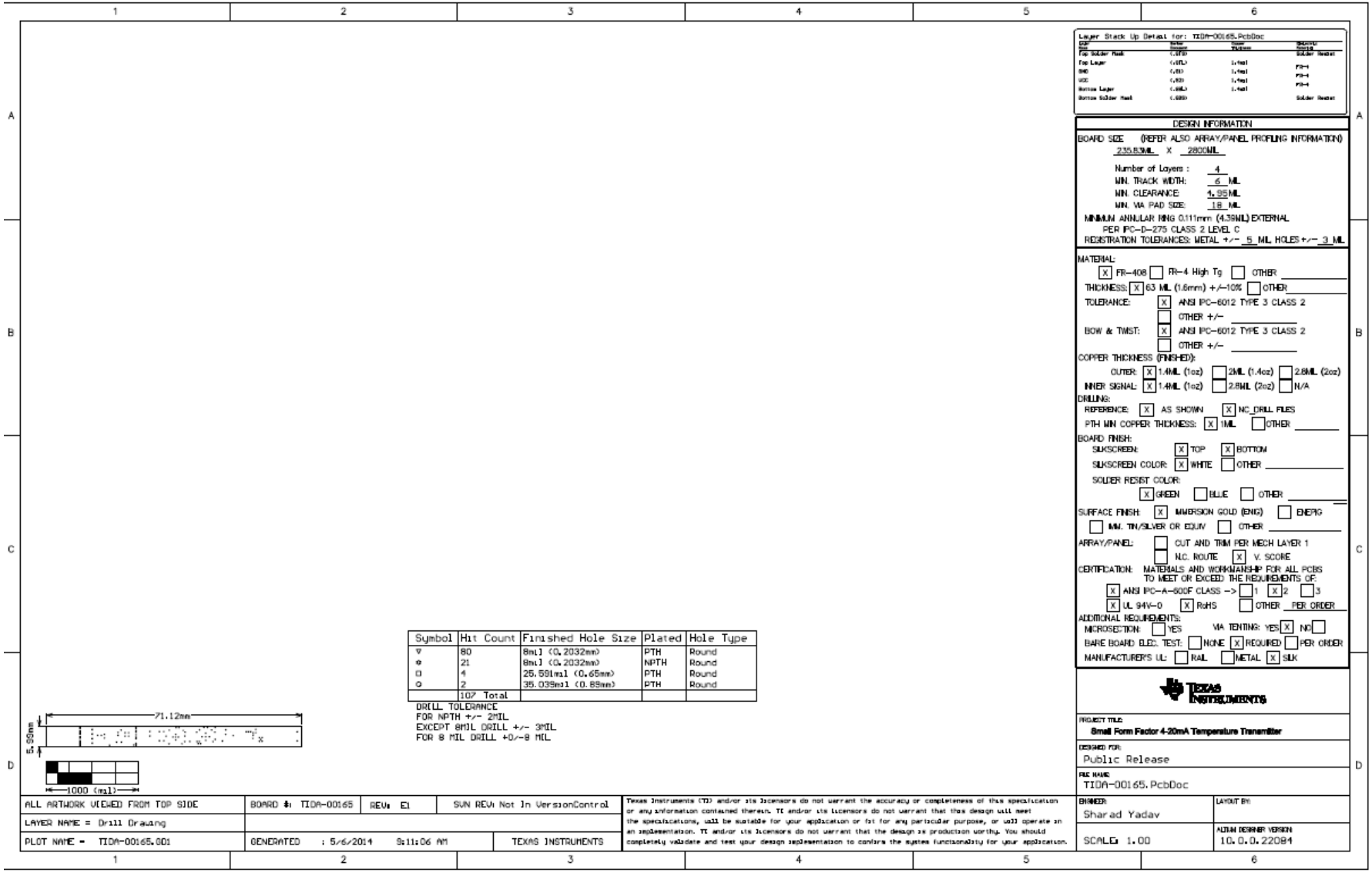


Figure 73. Fabrication Drawing

9.7 Software Files

To download the software files, see the design files at TIDA-00165.

10 References

1. *RTD Temperature Transmitter for 2-Wire, 4 to 20-mA Current Loop Systems*, Industrial Systems TI Design TIDU182
2. *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*, Application Report SBAA201
3. *Hardware-Compensated Ratiometric 3-Wire RTD System, 0°C – 100°C, 0.005°C Error*, TI Precision Design TIDU145
4. *3-Wire RTD Measurement System Reference Design, -200°C to 850°C*, TI Precision Design SLAU520
5. *Example Temperature Measurement Applications Using the ADS1247 and ADS1248*, Application Report SBAA180
6. *Signal Conditioning and Linearization of RTD Sensors 2011*, Texas Instruments Technology Day Presentation TIDU433
7. *Advanced Debugging Using the Enhanced Emulation Module (EEM) With Code Composer Studio Version 6*, Application Report SLAA393
8. *Namur NE43* Namur NE43
9. *Conversion of RTD Pt100* Conversion of RTD Pt100

11 About the Author

SHARAD YADAV is a Systems Engineer at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Sharad has eight years of experience in high-speed digital, mixed-signal boards, low-noise analog, and EMC protection circuit design.

TIDA-00165 Revision A History

Changes from Original (July 2014) to A Revision	Page
• Changed from TPA7A1601 to TPS7A1601	11
• Changed from TPA7A1601 to TPS7A1601	11
• Changed all instances of "NAUMAR" to "NAMUR"	27

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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