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TI High Speed Designs: Verified Design

High Performance Single Ended to Differential Active Interface for High Speed ADCs

TI High Speed Designs

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Circuit Description

The quad channel DEV-ADC34J22 board from Dallas Logic offers an example of a DC coupled single to differential channel using the THS4541 wideband Fully Differential Amplifier driving an ADC34J22. This type of circuit may be used in sensor front end, motor control, and test equipment applications. The amplifier circuit implemented on this EVM has a voltage gain of 2x. Applying a maximum 1Vpp ground centered input to one of the inputs, will result in a 2Vpp differential signal centered at 0.95V common mode at the ADC input pins. Included in this path is a low insertion loss 20MHz Bessel filter to limit the SNR degradation.

Design Resources

ADC34J22EVM	Product Folder
DEV-ADC34J22 EVM	Product Folder
ADC3XJXX Design	EVM Design Package

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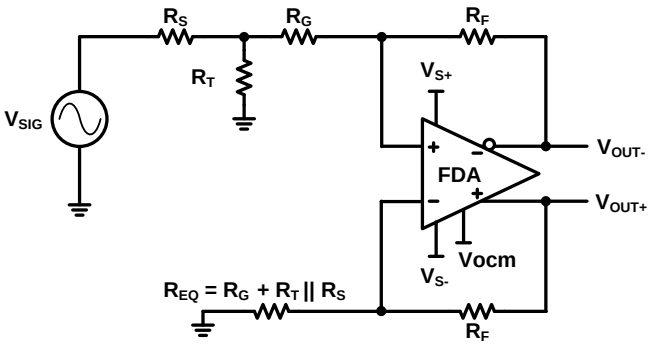

1 ADC34J22 and THS4541 Configuration

The DEV-ADC34J22 EVM from Dallas Logic has 4 channels: Channels 1 and 2 are transformer/AC coupled single-to-differential paths, while channels 3 and 4 are active DC coupled single-to-differential paths utilizing a THS4541 fully differential amplier. All 4 paths expect a 50 ohm source. For AC coupled passive performance the transformer paths should be used. In this document we will focus on the ADC34J22 + THS4541 implementation for simplicity sake – however the circuit applications are very similar for the entire ADC3XXXX family.

ADC Device	Interface	#channels	# bits	Max Msps
ADC3221	sLVDS	Dual	12	25
ADC3222			12	50
ADC3223			12	80
ADC3224			12	125
ADC3241			14	25
ADC3242			14	50
ADC3243			14	80
ADC3244			14	125
ADC3421	sLVDS	Quad	12	25
ADC3422			12	50
ADC3423			12	80
ADC3424			12	125
ADC3441			14	25
ADC3442			14	50
ADC3443			14	80
ADC3444			14	125
ADC32J22	JESD204B	Dual	12	50
ADC32J23			12	80
ADC32J24			12	125
ADC32J25			12	160
ADC32J42			14	50
ADC32J43			14	80
ADC32J44			14	125
ADC32J45			14	160
ADC34J22	JESD204B	Quad	12	50
ADC34J23			12	80
ADC34J24			12	125
ADC34J25			12	160
ADC34J42			14	50
ADC34J43			14	80
ADC34J44			14	125
ADC34J45			14	160

Table 1. List of available ADC3xxxx devices.

The block diagram of the DEV-ADC34J22 EVM is shown in figure 1. It is comprised of the ADC34J22, the THS4541 devices for the amplifier path, and the LMK04828B for clocking. The connection to the FPGA is through an HSMC connector. Configuration of the LMK04828B and the ADC34J22 is through the SPI interface through the HSMC connector from the FPGA. Refer to the Dallas Logic EVM link for details on ADC and LMK configuration.

Power for the ADC is provided from a TPS7A8101 LDO which regulates the 3.3V from the HSMC connector to 1.8V for the ADC.

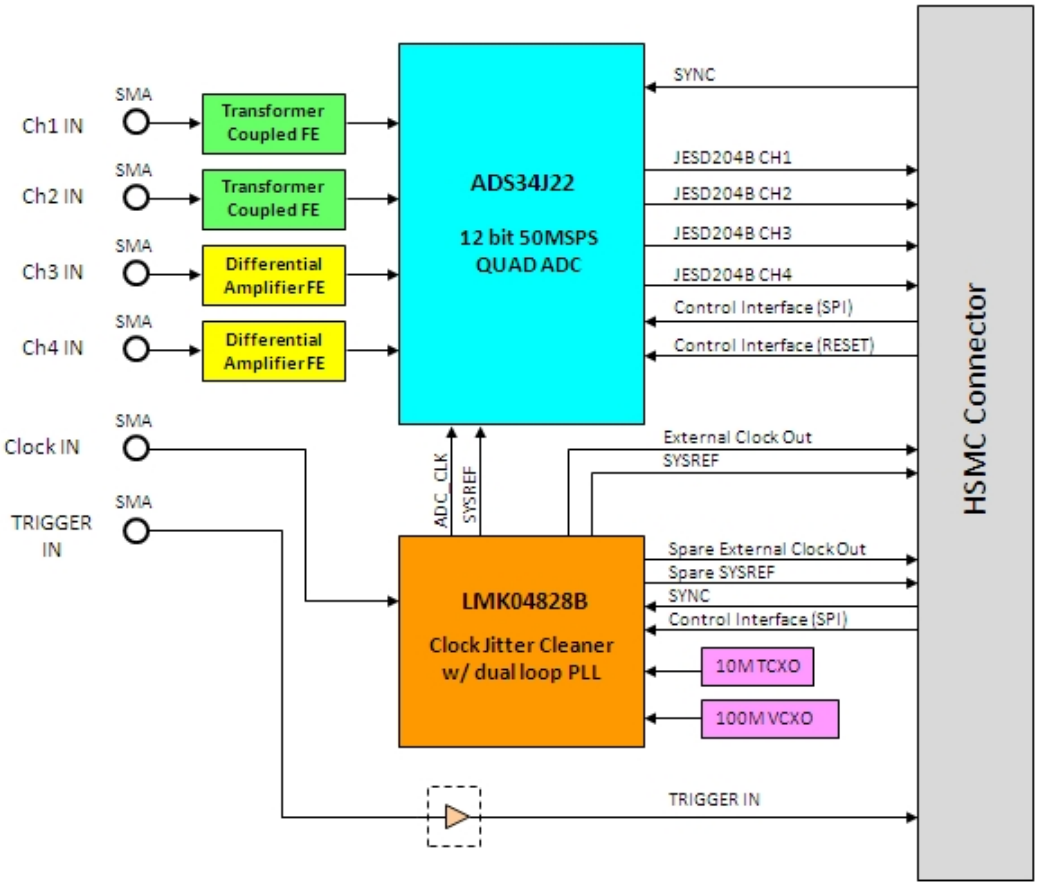

Figure 1. DEV-ADC34J22 block diagram.

2 Amplifier Power Supply

The power supply for the THS4541 circuit is provided by the 3.3V from the HSMC connector through a ferrite bead providing 3.3V and GND to the THS4541 device.

The amplifiers can also be put into a power down mode as needed through the PD control pin on the amplifier by asserting the PD pin to the negative supply. This can be controlled by installing a resistor on the DEV-ADC34J22 EVM (R62). PD is an active low signal.

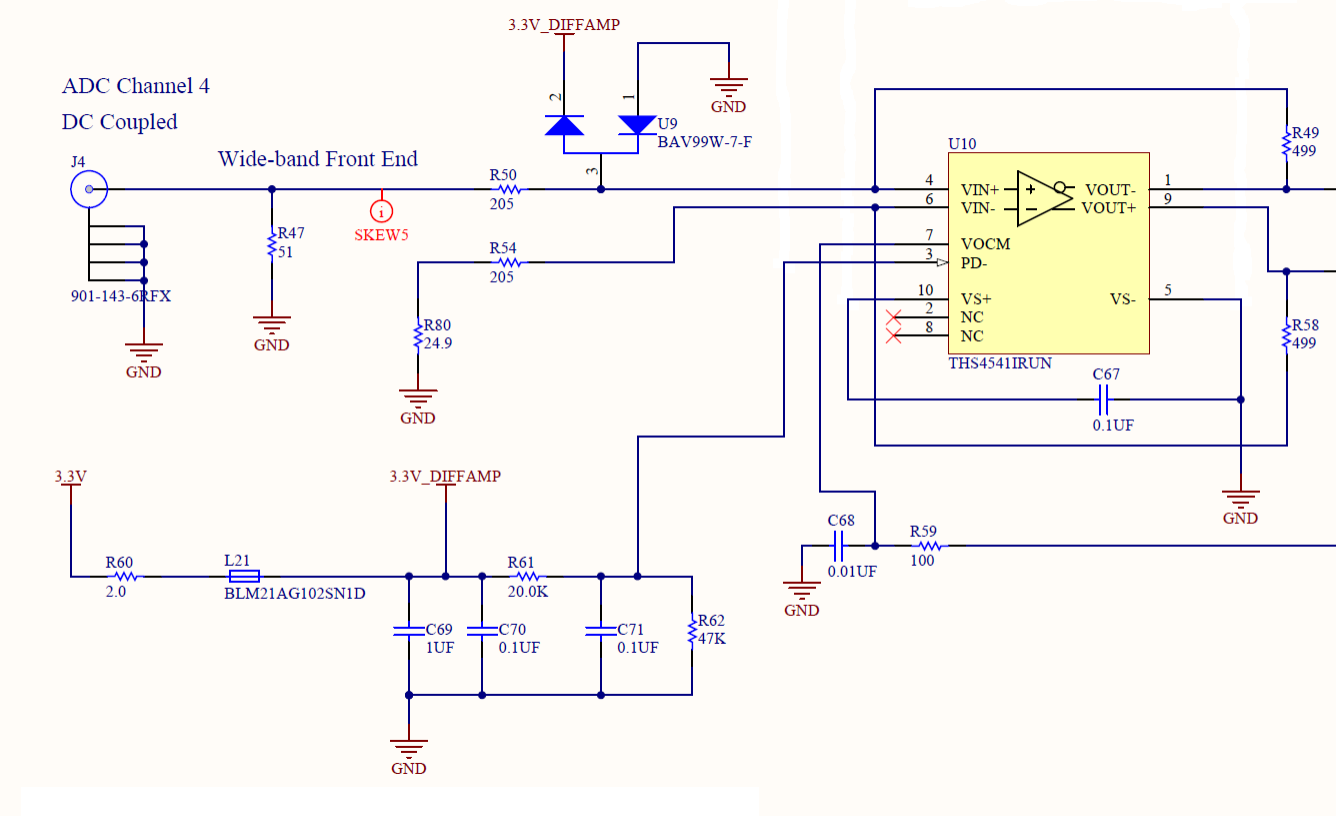

Figure 2. Amplifier Power Supply and Power Down option

3 Amplifier Circuit Configuration and Design

The Fully Differential Amplifier is configured in this case to have Single-Ended input with Differential outputs – assuming an off board source with 50 ohm impedance. An equivalent model is shown below.

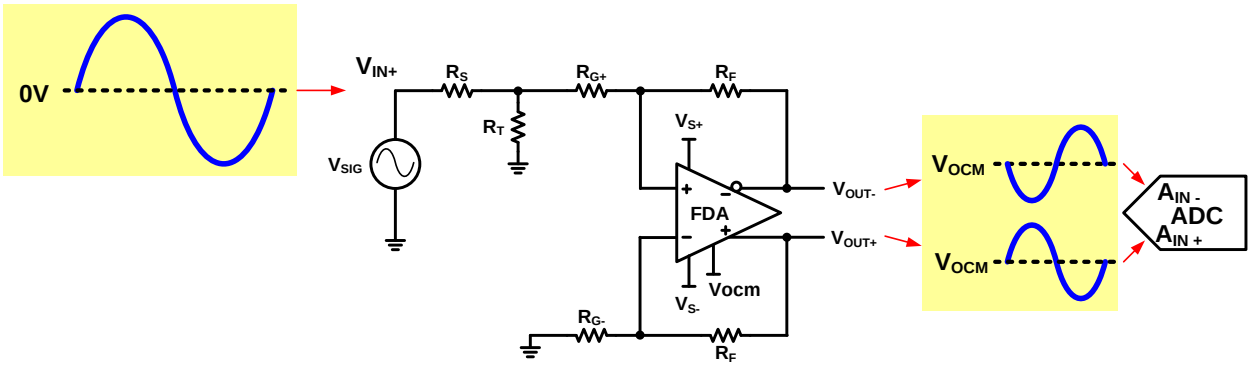

Figure 3. THS4541 circuit implementation model

The design equations for setting the resistors around an FDA to convert from a single ended input signal to differential output can be approached from several directions. Here, several critical assumptions will be made to simplify the results:

1. The feedback resistors will be selected first and set equal on the two sides
2. The DC and AC impedances from the summing junctions back to the signal source and ground (or a bias voltage on the non-signal input side) will be set equal to retain feedback divider balance on each side of the FDA.

Both of these assumptions are typical and aimed to delivering the best dynamic range through the FDA signal path.

Once the feedback resistor values are chosen, the aim here is to solve for the R_T (a termination resistor to ground on the signal input side), R_{G+} (the input gain resistor for the signal path), and R_{G-} (the matching gain resistor on the non – signal input side). The same resistor solutions can be applied to either AC or DC coupled paths. Adding blocking caps in the input signal chain is a simple option where adding it after the R_T element has the advantage of removing any DC currents in the feedback path from the output Vocm to ground.
Earlier approaches to the solutions for R_T , and R_{G+} (when the input needs to be matched to a source impedance, R_S) have followed an iterative approach. This complexity arises from the active input impedance looking into the R_{G+} element. When the FDA is used to convert a single ended signal to differential, the common mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the R_{G-} element (is one way to look at it). A more recent solution is shown as Eq. 1 where a quadratic in R_T can be solved for an exact required value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only inputs required are:

1. The selected R_F value
2. The target voltage gain (Av) from the input of R_T to the differential output voltage
3. The desired input impedance looking into R_T and R_{G+} to match R_S.

Solving this quadratic for R_T will start the solution sequence :

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_v^2\right)}{2R_F(2+A_v) - R_S A_v(4+A_v)} - \frac{2R_F R_S^2 A_v}{2R_F(2+A_v) - R_S A_v(4+A_v)} = 0 \qquad \text{Eq. 1}$$

Being a quadratic, there are limits to the range of solutions. Specifically, once R_F and R_S are chosen, there is physically a maximum gain beyond which this starts to solve for negative R_T values (if input matching is a requirement). With R_F selected, check Eq. 2 verifying the maximum gain is > than the desired gain.

$$Av_{\max} = \left(\frac{R_F}{R_S} - 2\right) * \left(1 + \sqrt{1 + \frac{4\frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right) \qquad \text{Eq. 2}$$

If the achievable Av_{MAX} is < than desired, increase the R_F value.
Once R_T is derived from Eq. 1, the R_{G+} element will be given by Eq. 3.

$$R_{G+} = \frac{2\frac{R_F}{Av} - R_S}{1 + \frac{R_S}{R_T}} \qquad \text{Eq. 3}$$

Then the simplest approach is to use a single $R_{G-} = R_T||R_S + R_{G+}$ on the non-signal input side. These are shown as separate elements here, but a single resistor to GND as given by Eq.4 is also acceptable. A direct solution for R_{G-} is given as eq. 4

$$R_{G-} = \frac{2\frac{R_F}{Av}}{1+\frac{R_S}{R_T}} \qquad \text{Eq. 4}$$

This design proceeds from a target input impedance matched to R_S, signal gain Av, and a selected R_F value. The nominal R_F value chosen for this THS4541 implementation was 499Ω. Going lower in R_F value improves noise and phase margin but reduces the total output load impedance possibly degrading harmonic distortion. Going higher increases the output noise and might reduce the loop phase margin due to the feedback pole to the parasitic input capacitance back to the input pins, but reduces the total loading on the outputs.

This design started with a 499Ω feedback resistor and designed for a DC coupled 50Ω input match providing a gain of 2.35V/V to the THS4541 output pins. The 3rd order interstage low pass filter provides a 20Mhz Bessel low pass response with a 0.85V/V insertion loss to the ADC giving a net gain of 2V/V from board edge to the ADC inputs. While the THS4541 can absorb overdrives, an added external protection element was added using the BAV99 low capacitance device shown in figure 3. For DC coupled testing, pins 1 to 2 are jumpered together. When the source is an AC coupled 50Ω source, pins 2 to 3 are jumpered to maintain differential balance. FFT testing normally uses a bandpass filter into the board – which would be an AC coupled source.

The results for this implementation using 1% standard resistor values:

Choose R_F=499, Assume R_S=50, A_V=2.35 V/V
Solve for R_T=59, $R_{G+=}$205, R_{G-}=232 (205+59//49.9 for balance)

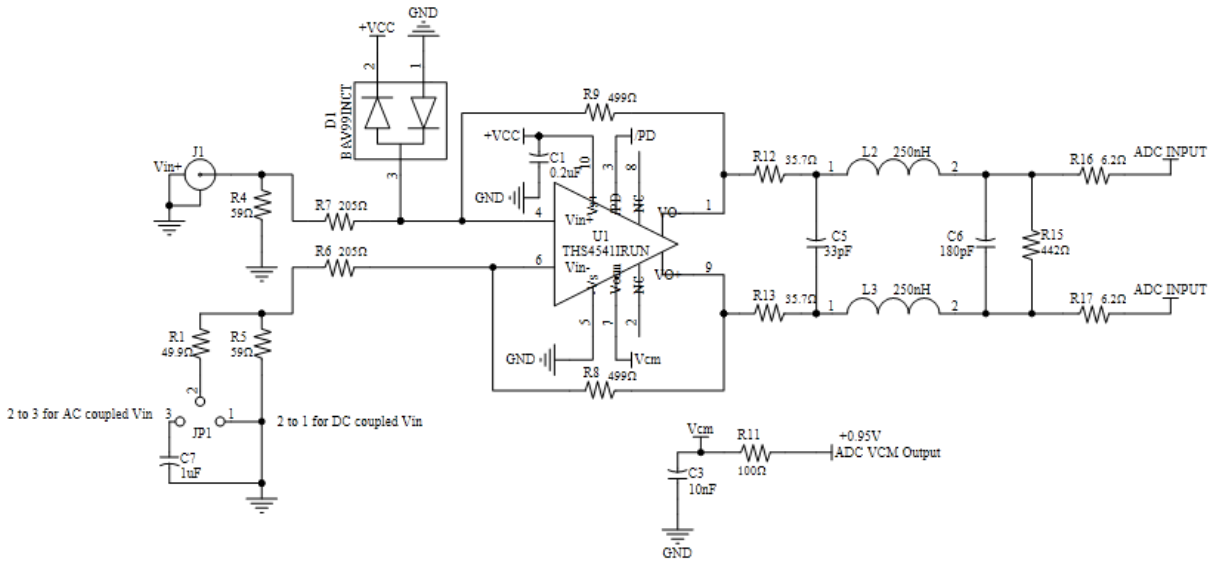

Figure 3. Example implementation of the THS4541 with 20MHz Low Pass interstage filter prior to ADC inputs.

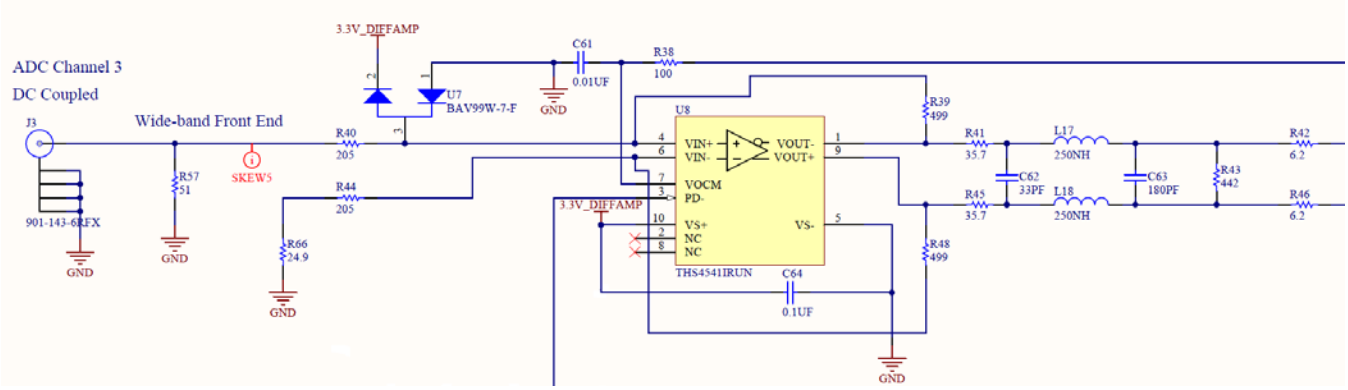

Figure 4. THS4541 circuit implementation with 20M Bessel LPF driving ADC34J22

4 Results on THS4541+ADC3244

The results for the implementation of the THS4541+ADC34J22 show very good combined response. In a simple test where a clean filtered signal is fed into the THS4541+ADC34J22 circuit, the SNR showed ~72dB which is only a slight degradation from the 72.4dB of the ADC3244 using a transformer interface. Also the exceptional HD of the THS4541 shows only a very slight impact to the ADC only SFDR performance of 96dB and a THD of 92.XdB. In summary a very clean active interface can be implemented using the THS4541 to drive the high performance requirements of the 12bit and 14bit ADC3xxxx data converter family. For applications below 5 MHz, the 1mA precision FDA – THS4521 should be considered. For applications above 50MHz, the 2.8 GHz low-noise FDA – LMH6554 would be a viable option.

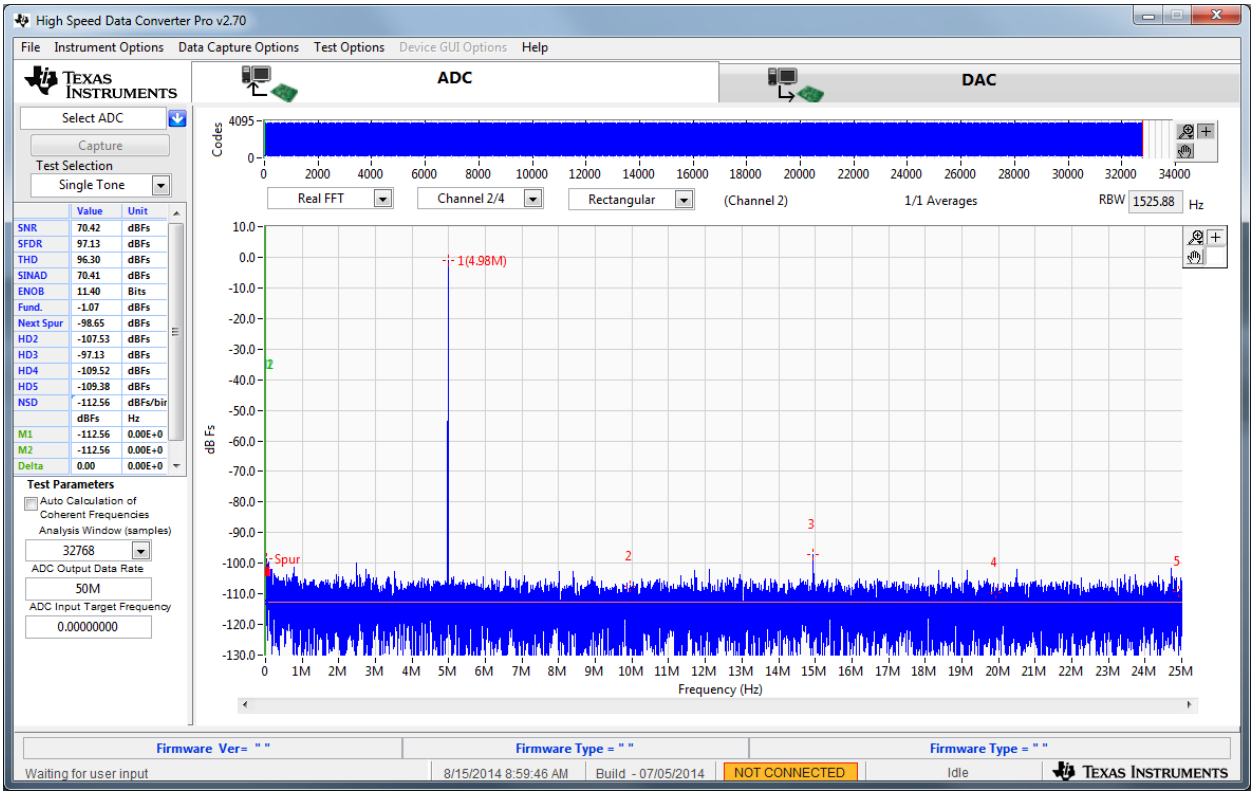

Figure 5. FFT performance of the ADC34J22 with transformer interface

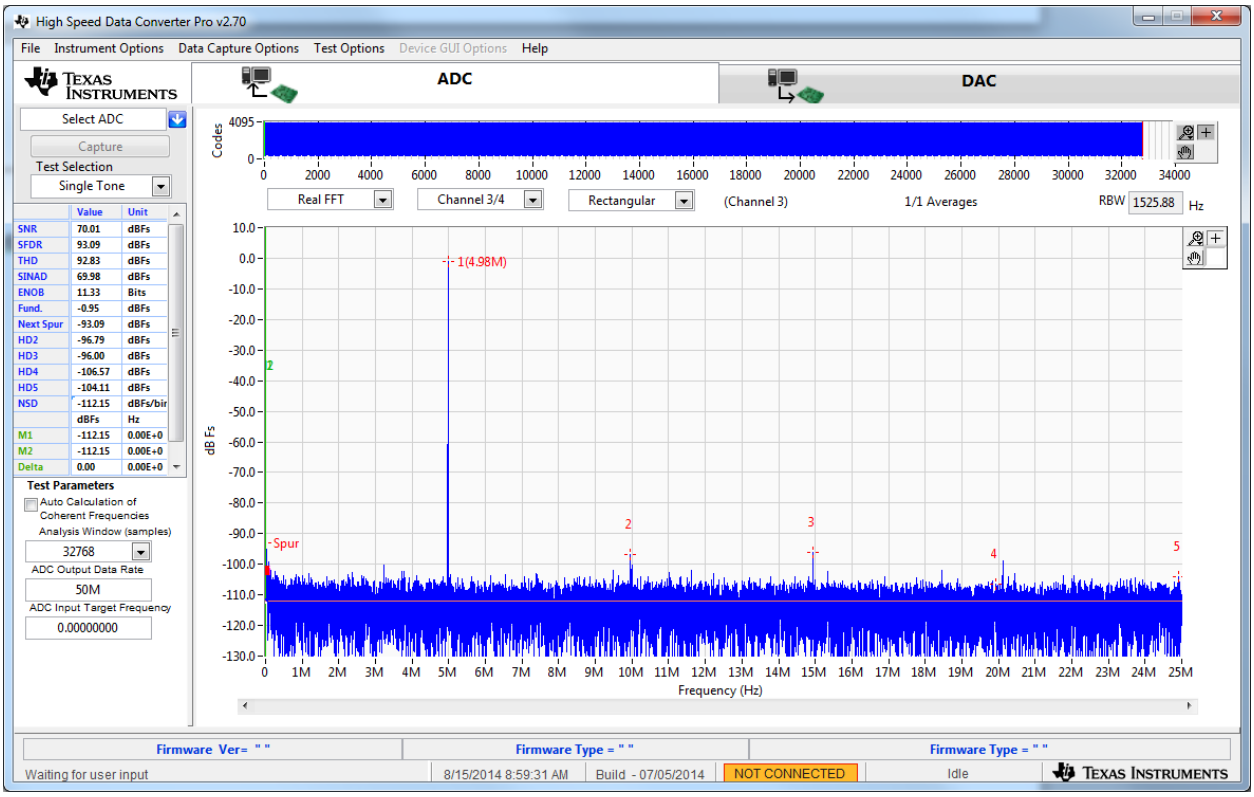

Figure 6. FFT performance of THS4541+ADC34J22 active interface

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