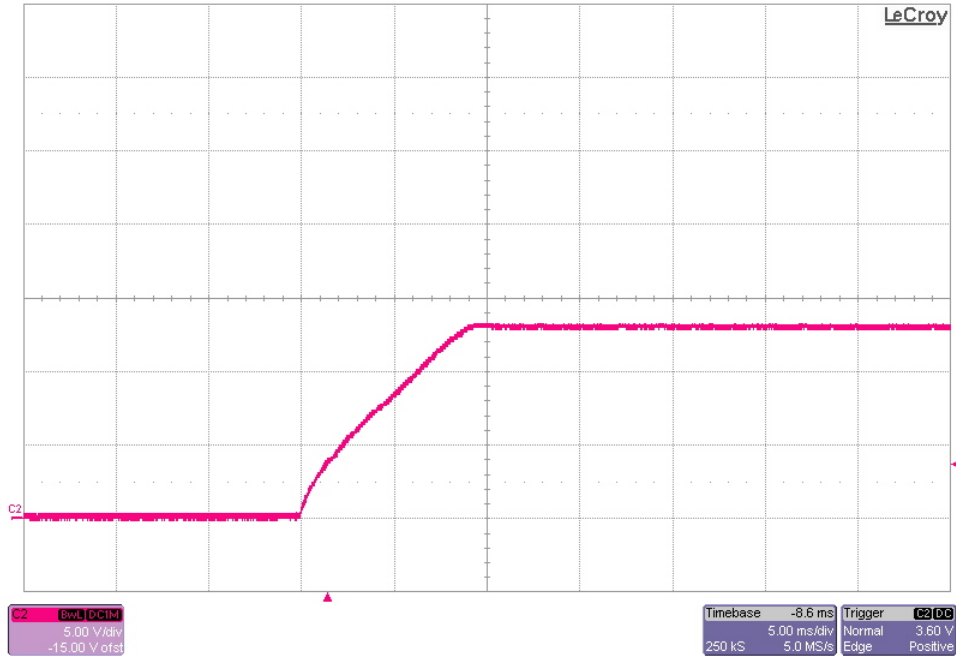
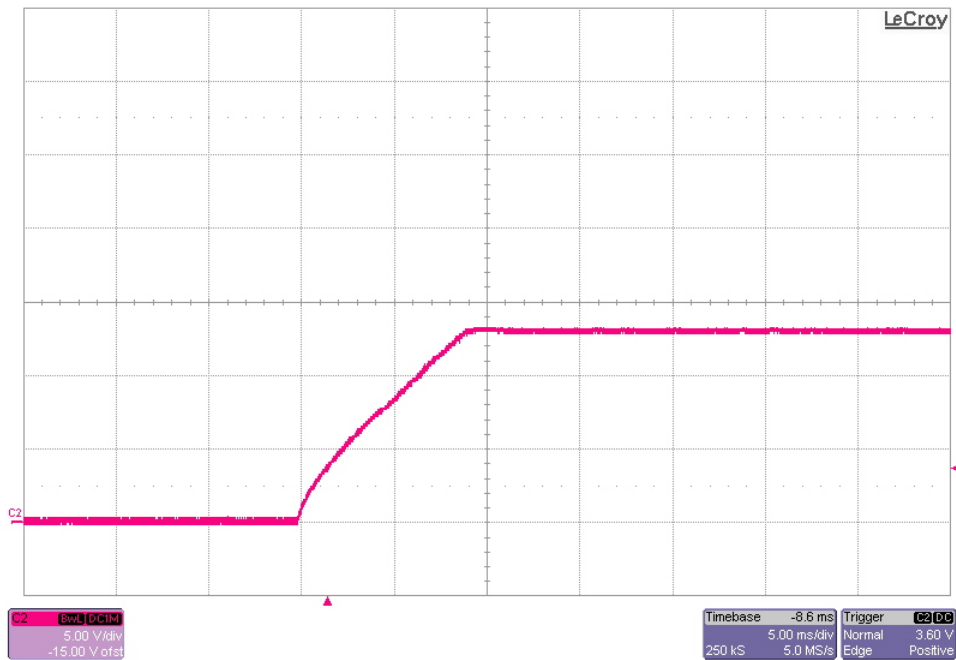


1 Startup

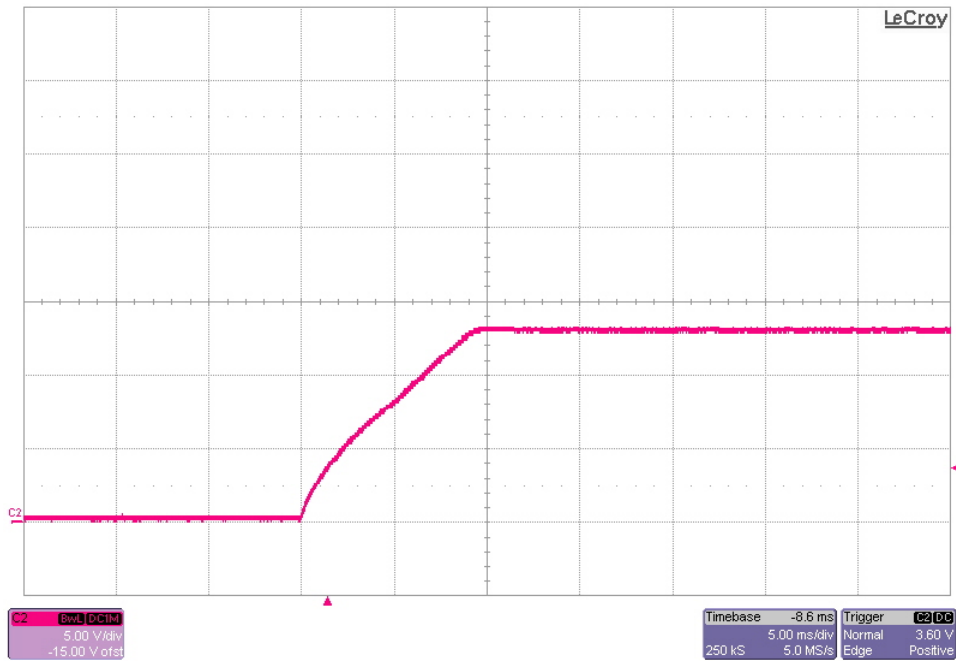
The photo below shows the output voltage startup waveform after the application of 16V in. The 13.2V output was loaded to 0A. (5V/DIV, 5mS/DIV)



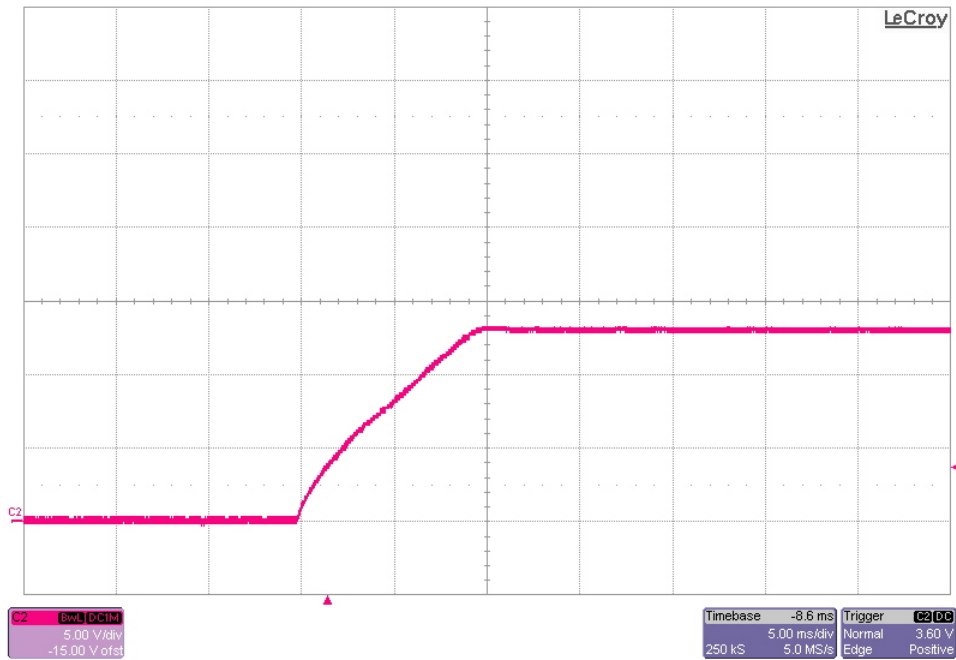
The photo below shows the output voltage startup waveform after the application of 16V in. The 13.2V output was loaded to 3A. (5V/DIV, 5mS/DIV)



The photo below shows the output voltage startup waveform after the application of 6V in. The 13.2V output was loaded to 0A. (5V/DIV, 5mS/DIV)

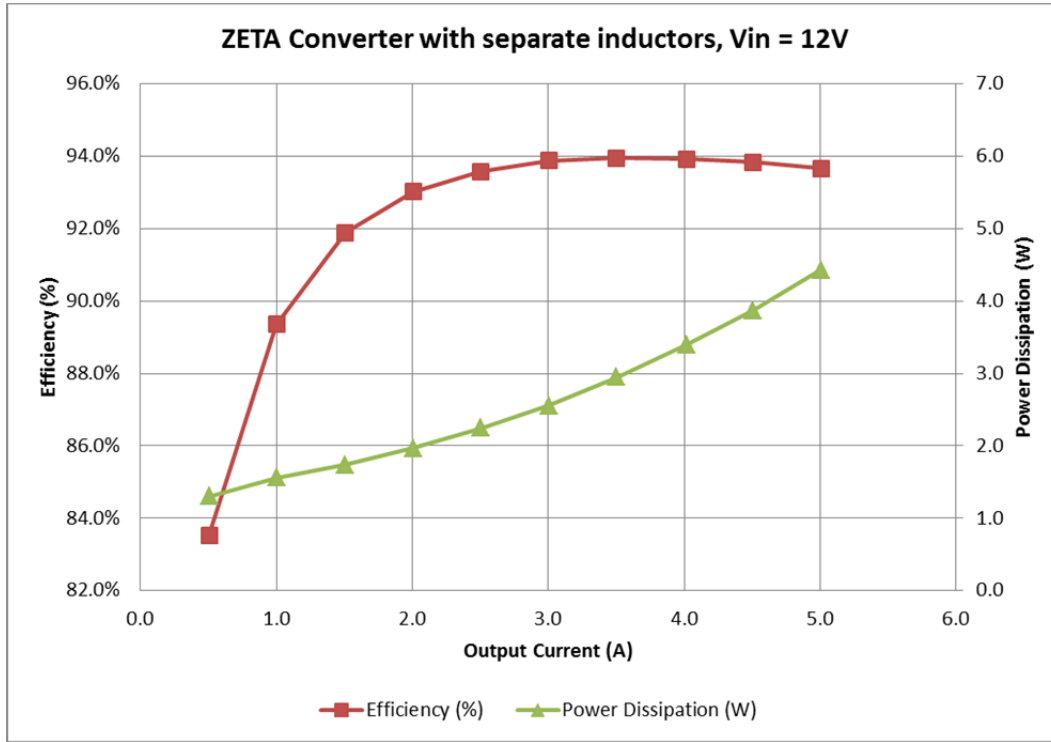


The photo below shows the output voltage startup waveform after the application of 6V in. The 13.2V output was loaded to 3A. (5V/DIV, 5mS/DIV)

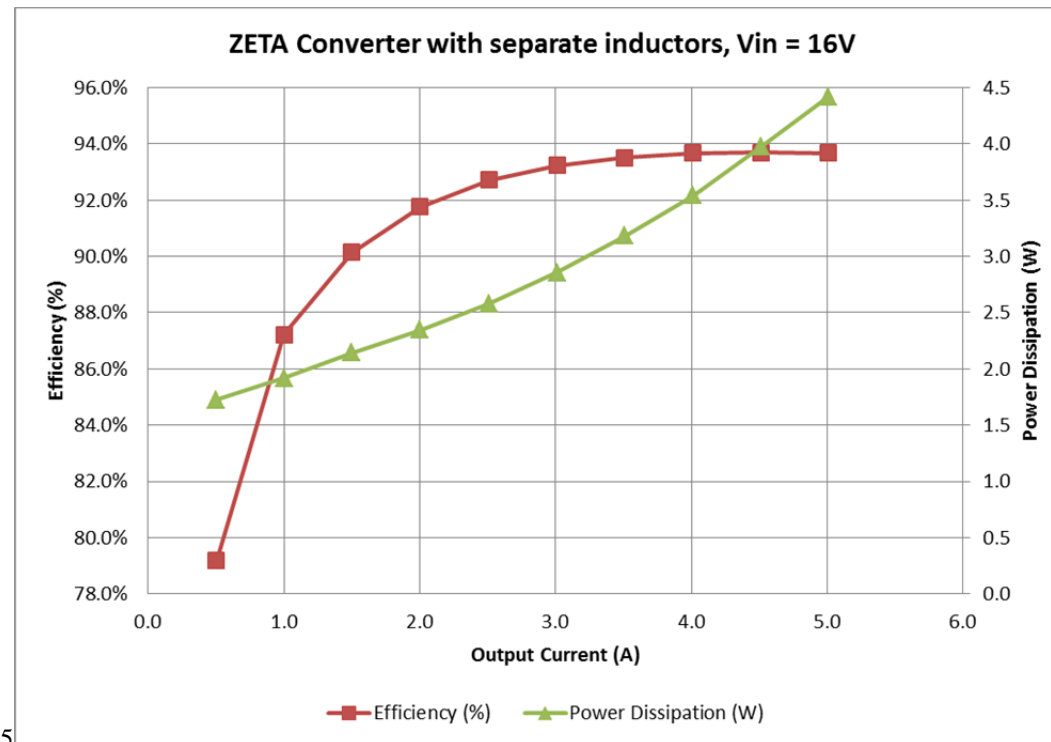


2 Efficiency

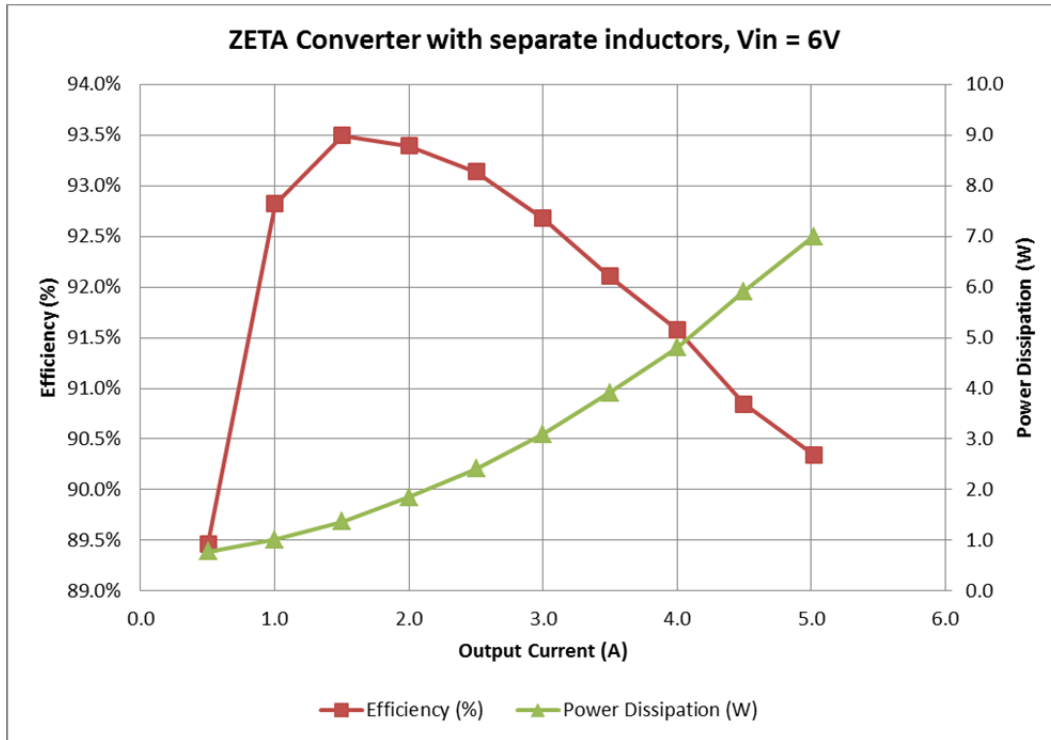
The converter efficiency is shown below for $V_{in} = 12V$ and $V_{out} = 13.2V$.



The converter efficiency is shown below for $V_{in} = 16V$ and $V_{out} = 13.2V$.

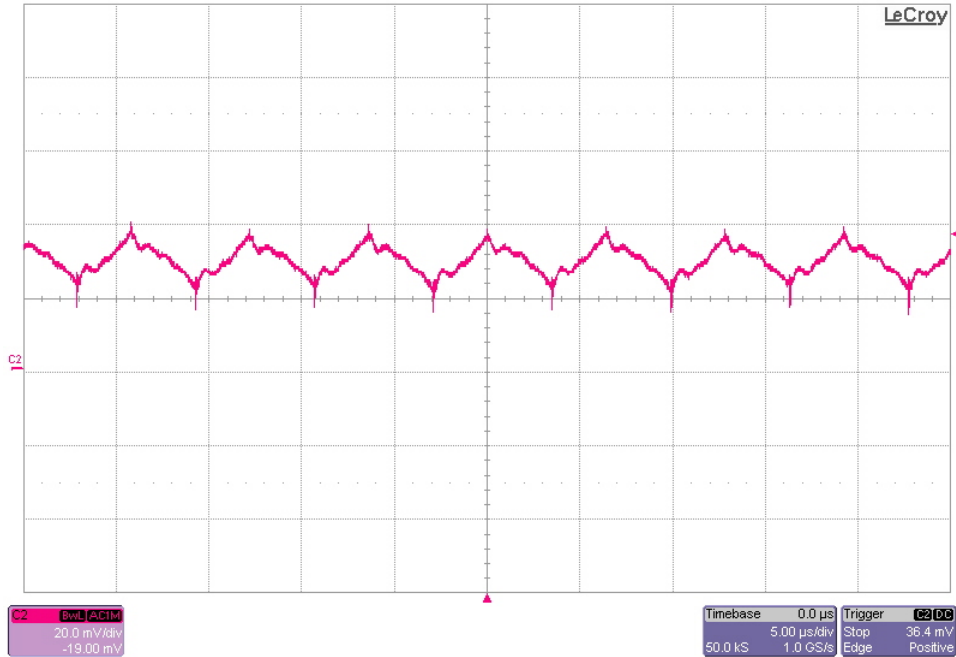


The converter efficiency is shown below for $V_{in} = 6V$ and $V_{out} = 13.2V$.

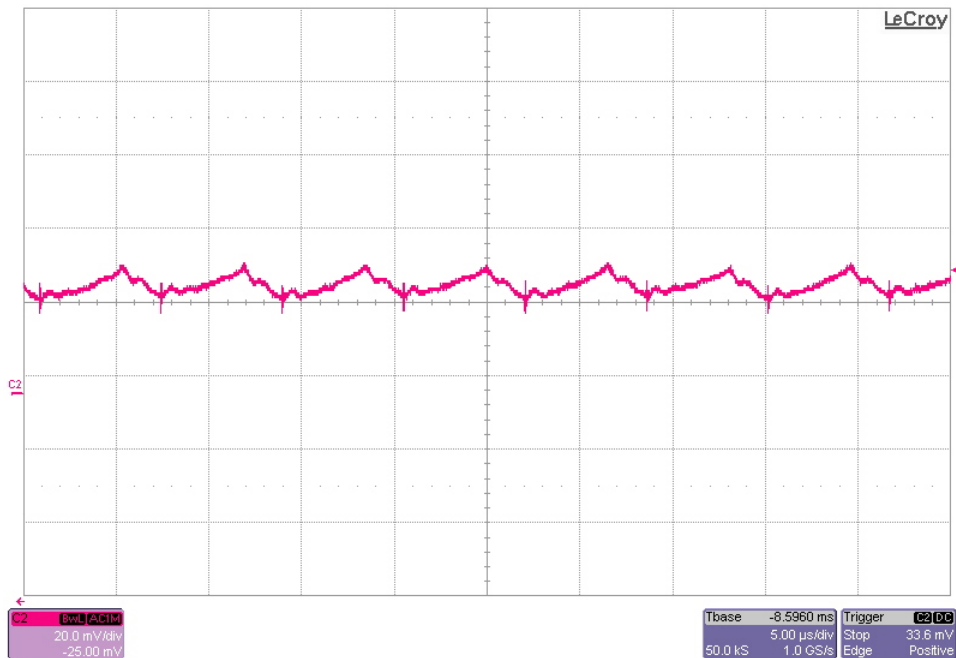


3 Output Ripple Voltage

The 13.2V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 3A. The input voltage is set to 16V. (20mV/DIV, 5uS/DIV)

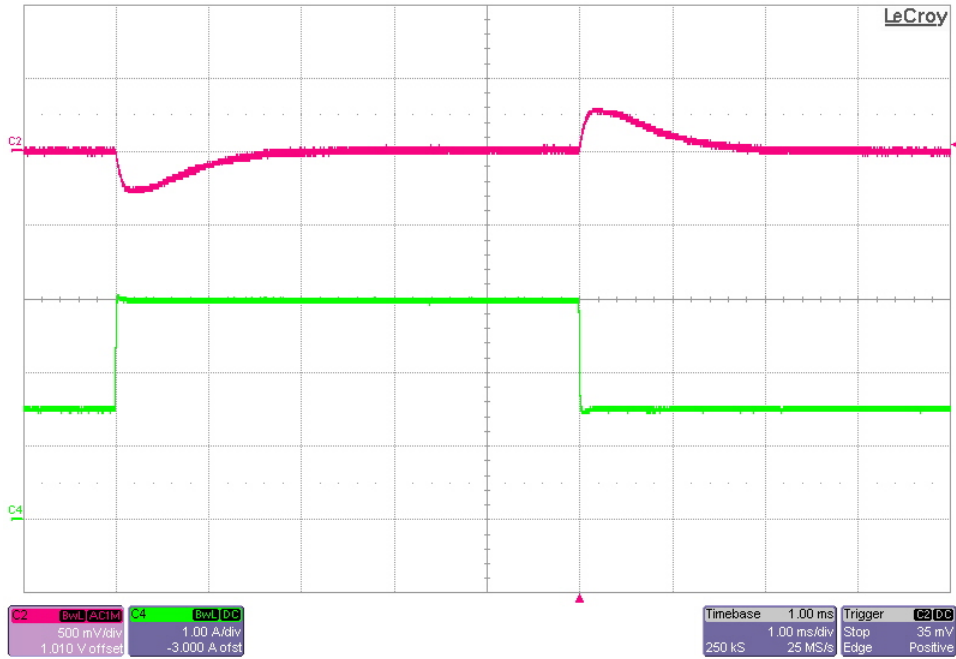


The 13.2V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 3A. The input voltage is set to 6V. (20mV/DIV, 5uS/DIV)

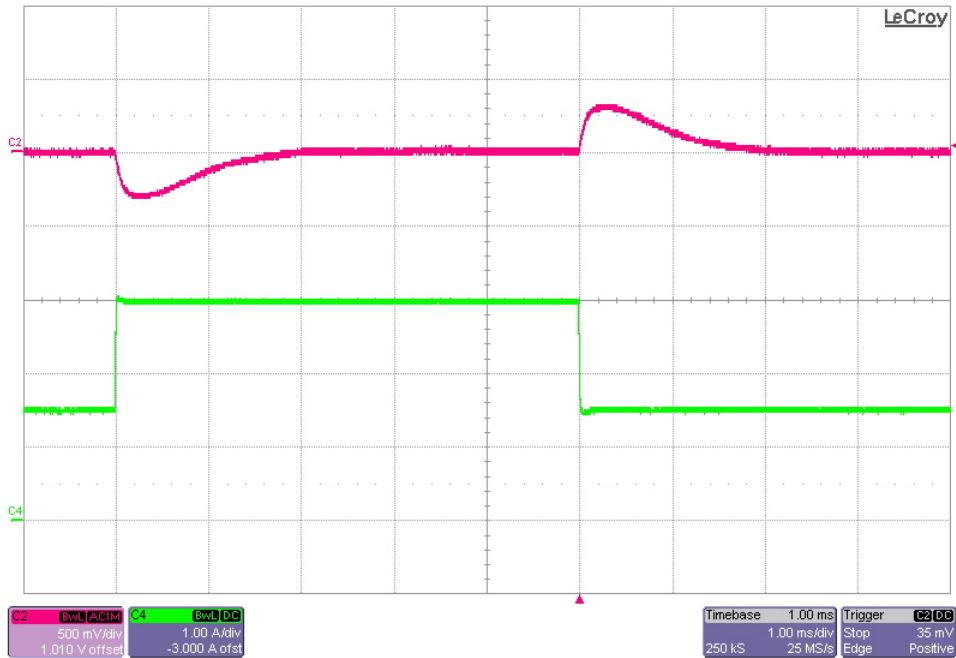


4 Load Transients

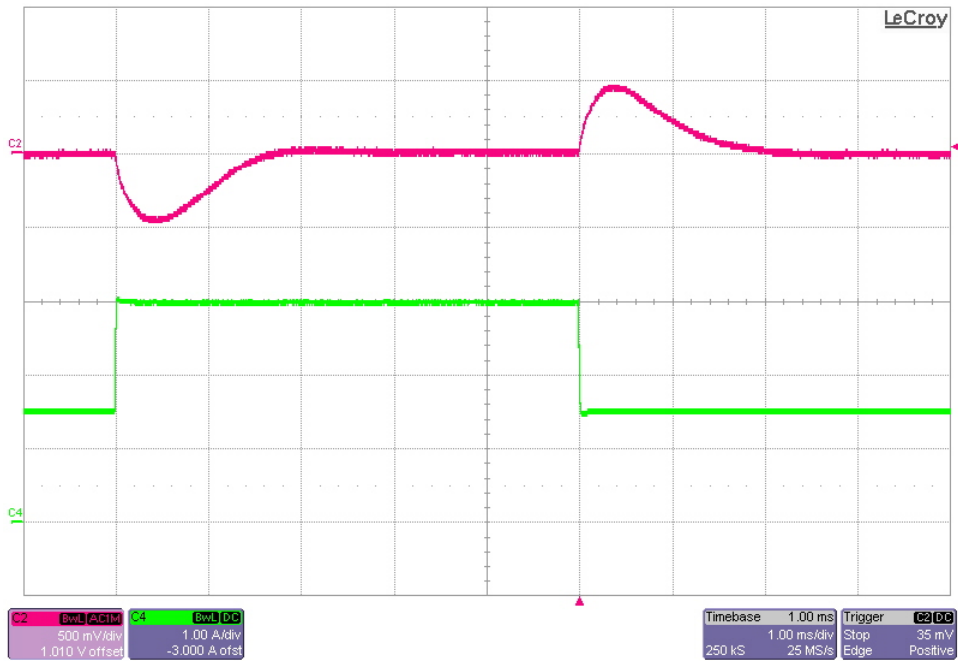
The photo below shows the 13.2V output voltage (ac coupled) when the load current is stepped between 1.5A and 3A. $V_{in} = 16V$. (500mV/DIV, 1A/DIV, 1mS/DIV)



The photo below shows the 13.2V output voltage (ac coupled) when the load current is stepped between 1.5A and 3A. $V_{in} = 12V$. (500mV/DIV, 1A/DIV, 1mS/DIV)

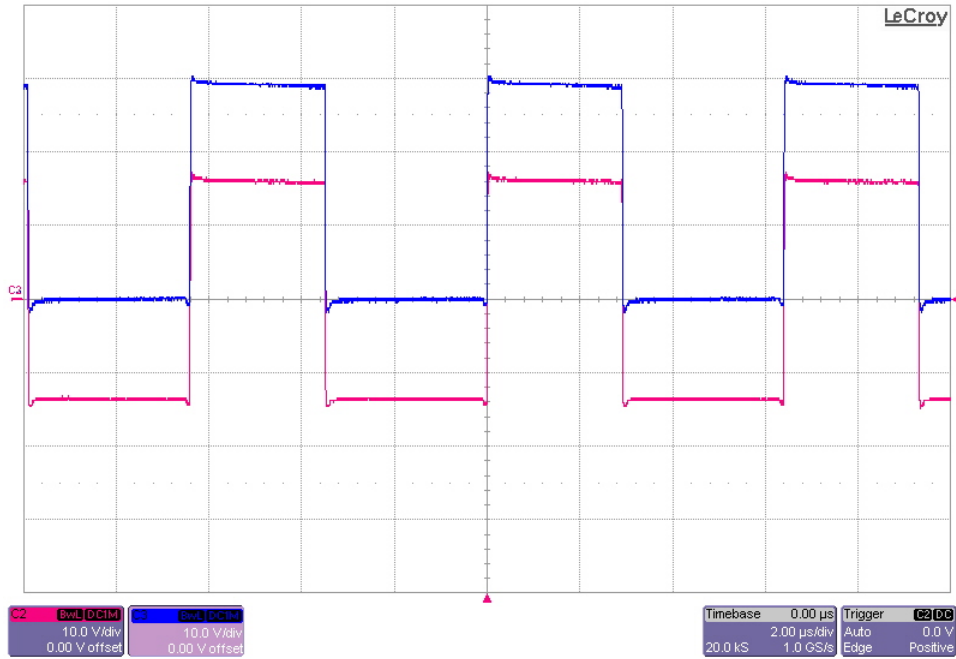


The photo below shows the 13.2V output voltage (ac coupled) when the load current is stepped between 1.5A and 3A. $V_{in} = 6V$. (500mV/DIV, 1A/DIV, 1mS/DIV)

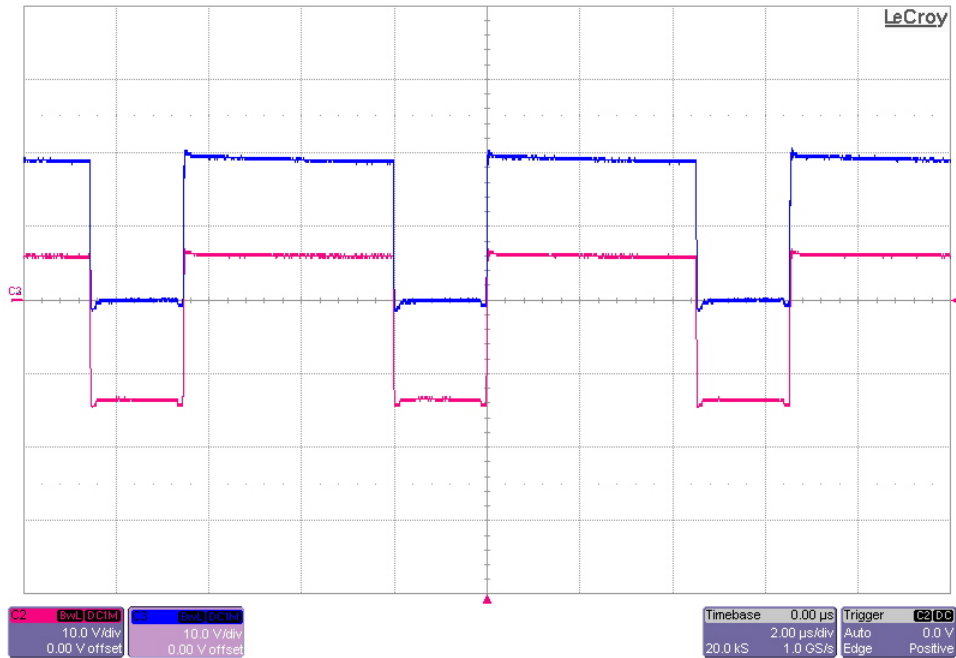


5 Switch Node Waveforms

The photo below shows the two switching node voltages for an input voltage of 16V and a 3A load. Blue is the bottom FET (TP7) and Red is the top FET (TP3). (10V/DIV, 2uS/DIV)



The photo below shows the two switching node voltages for an input voltage of 6V and a 3A load. Blue is the bottom FET (TP7) and Red is the top FET (TP3). (10V/DIV, 2uS/DIV)



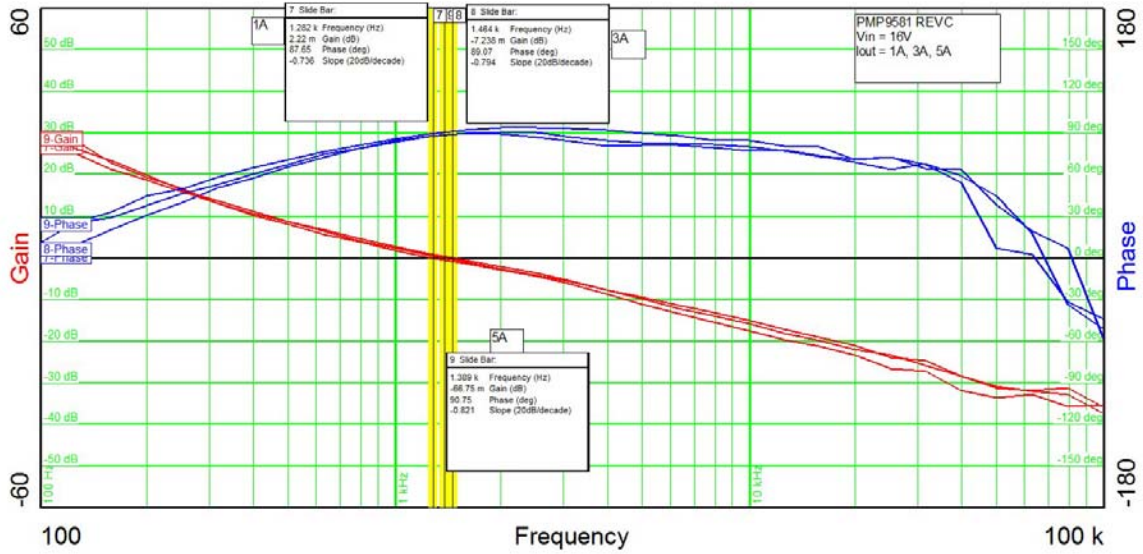
6 Loop Gain

The plot below shows the loop gain with the input voltage set to 16V and the output set to 1A, 3A, and 5A.

Loop Gain (Iout = 5A)
 Loop Gain (Iout = 3A)
 Loop Gain (Iout = 1A)

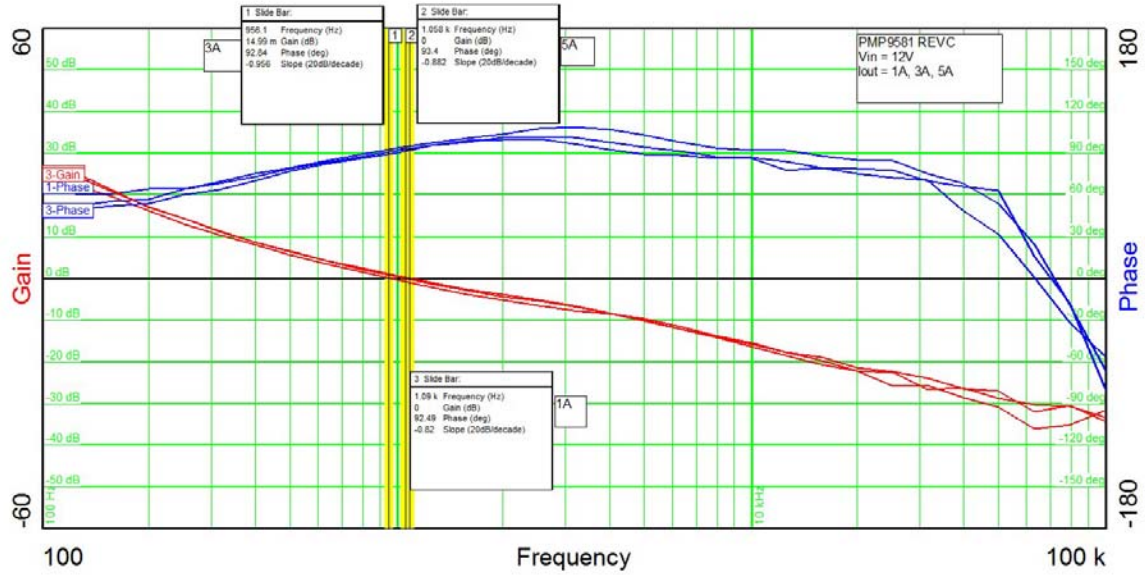
BW: 1.39KHz
 BW: 1.46KHz
 BW: 1.28KHz

PM: 91 degrees
 PM: 89 degrees
 PM: 88 degrees



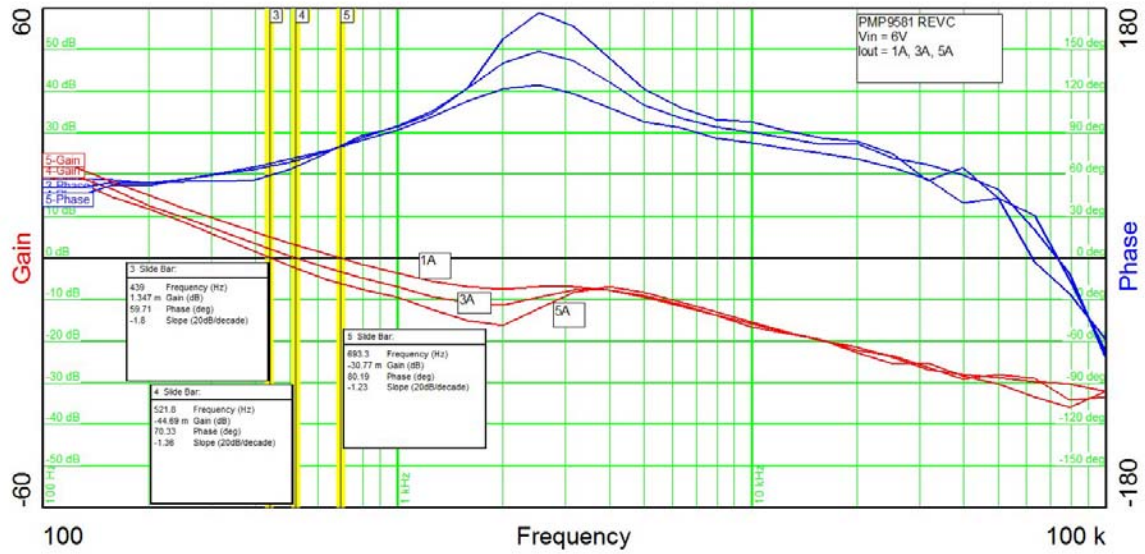
The plot below shows the loop gain with the input voltage set to 12V and the output set to 1A, 3A, and 5A.

Loop Gain (Iout = 5A)	BW: 1.06KHz	PM: 93 degrees
Loop Gain (Iout = 3A)	BW: 956Hz	PM: 93 degrees
Loop Gain (Iout = 1A)	BW: 1.09KHz	PM: 92 degrees



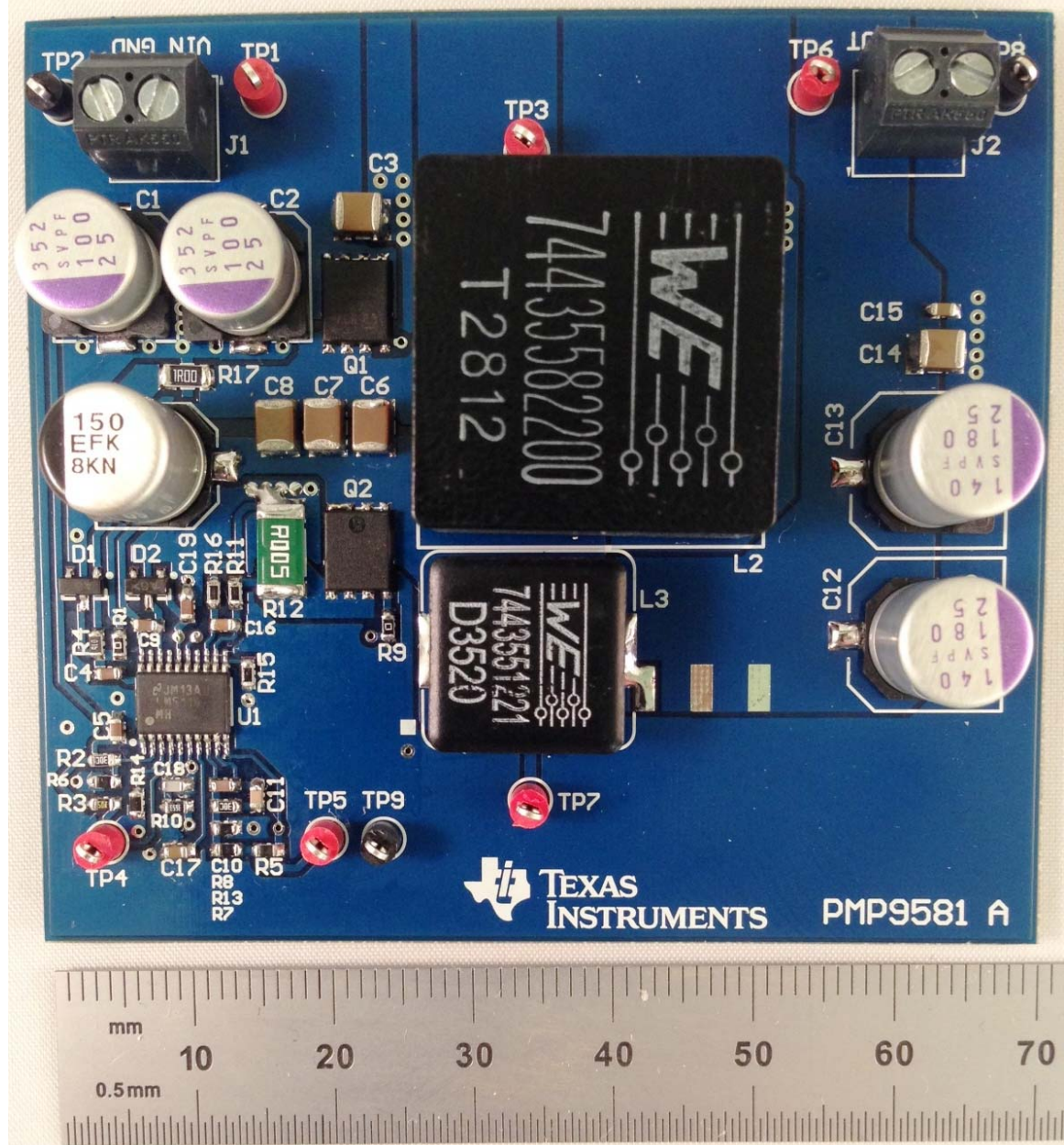
The plot below shows the loop gain with the input voltage set to 6V and the output set to 1A, 3A, and 5A.

Loop Gain (Iout = 5A)	BW: 439Hz	PM: 60 degrees
Loop Gain (Iout = 3A)	BW: 522Hz	PM: 70 degrees
Loop Gain (Iout = 1A)	BW: 693Hz	PM: 80 degrees



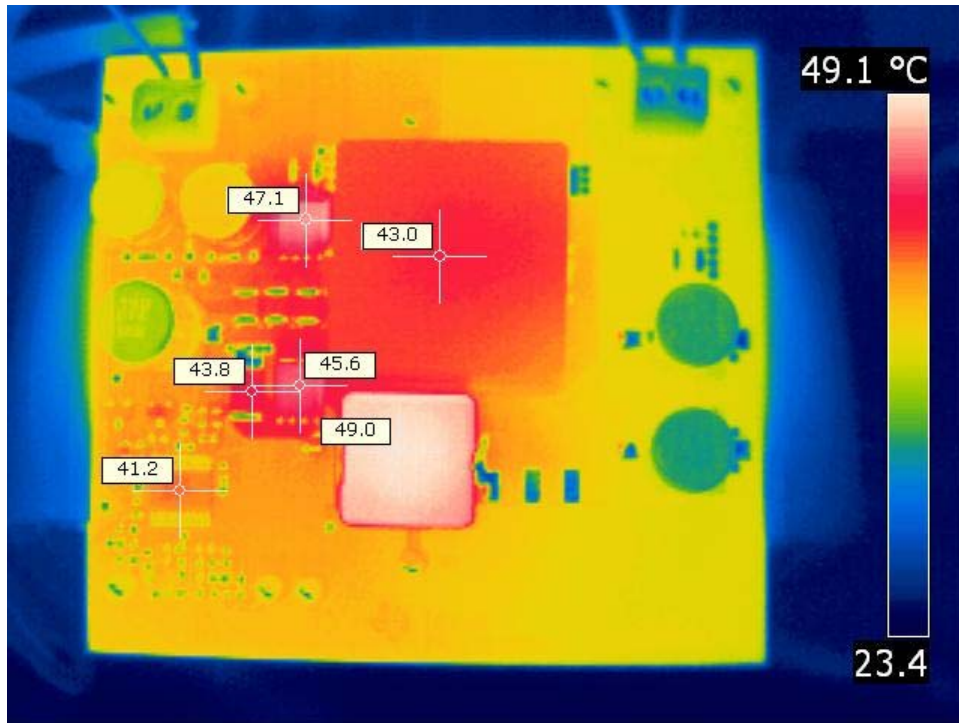
7 Photo

The photo below shows the PMP9581 REVC assy.

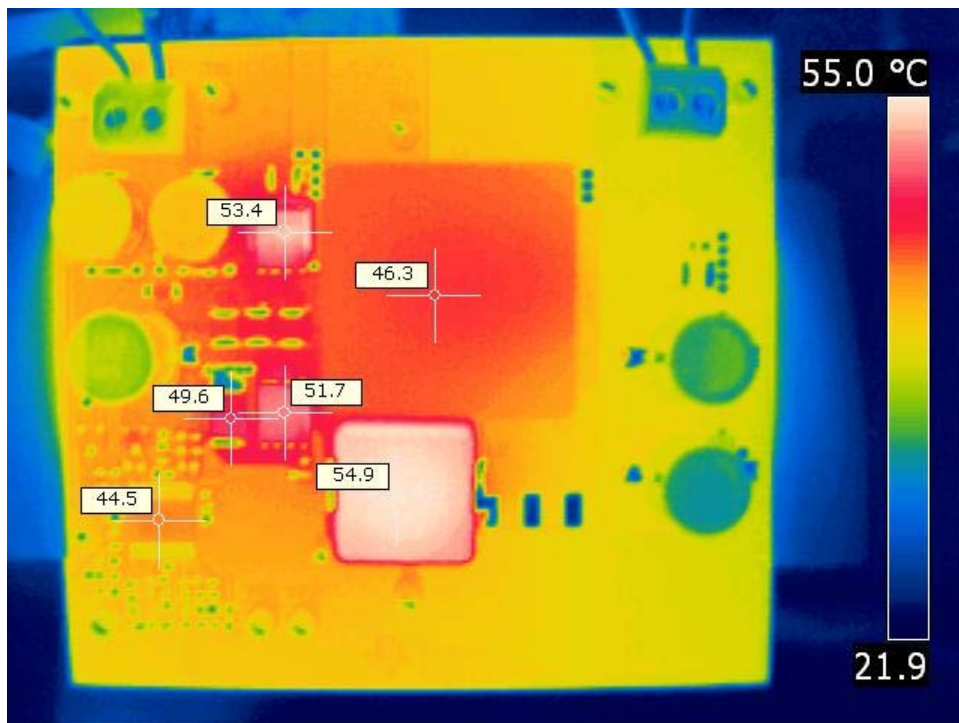


8 Thermal Image

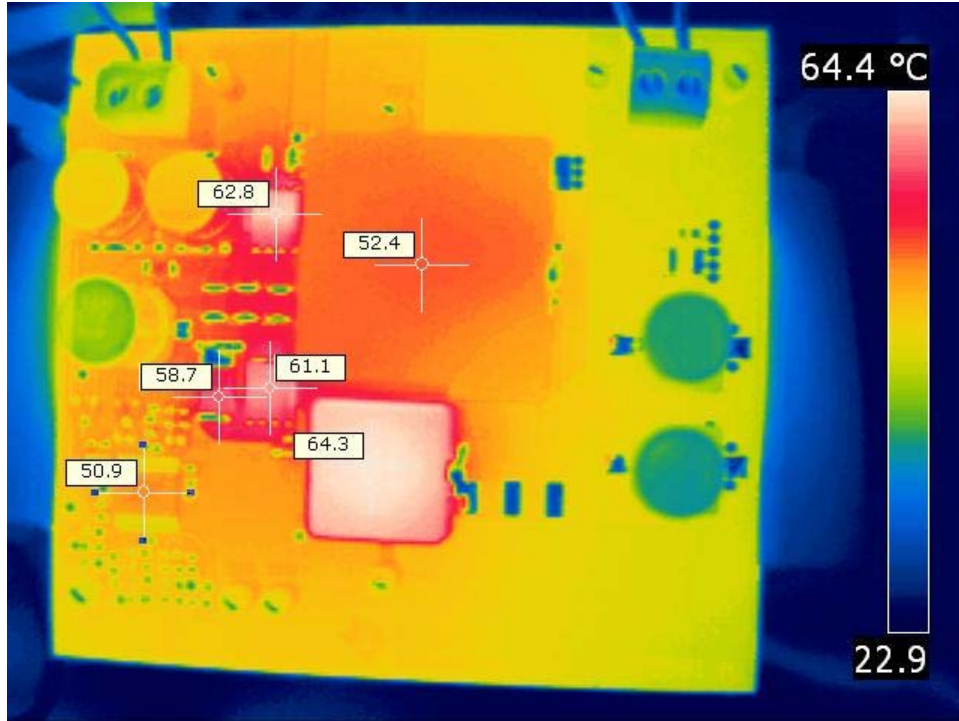
A thermal image is shown below operating at 12V input and 13.2V@3A output (room temp, no airflow).



A thermal image is shown below operating at 12V input and 13.2V@4A output (room temp, no airflow).



A thermal image is shown below operating at 12V input and 13.2V@5A output (room temp, no airflow).



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated