TI Designs

Shunt-Based Ground Fault Protection for Inverters Powered From 220-V AC Supply

Design Overview

This TI design provides a reference solution for detecting the ground fault in inverter-based drives. The inverter current is measured on both the DC positive and DC negative bus using shunt resistors. The current on the DC positive bus is measured using the INA170 device, which is powered by a low-side switched buck converter. The current on the DC negative bus is sensed using precision operational amplifiers (op-amps). The difference between the two measured currents is compared against a fixed threshold to determine the ground fault condition using high-speed comparators.

Design Resources

TIDA-00442	Tool Folder Containing Design Files
INA170	Product Folder
OPA2376	Product Folder
TLC372	Product Folder
REF2033	Product Folder
UCC28880	Product Folder
LM4040	Product Folder

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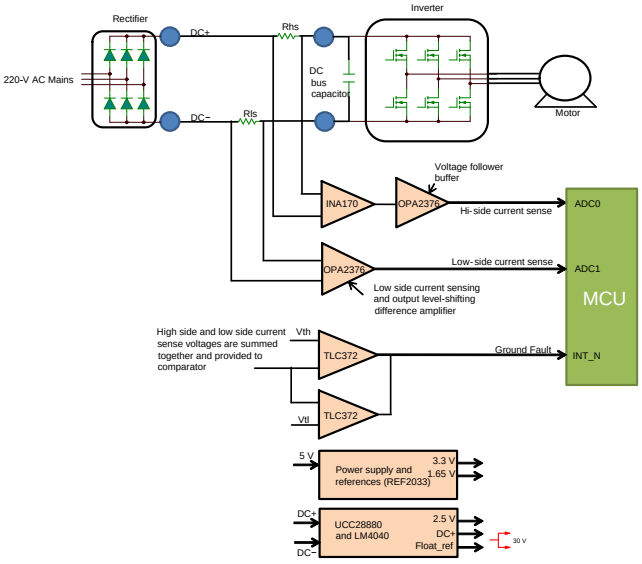
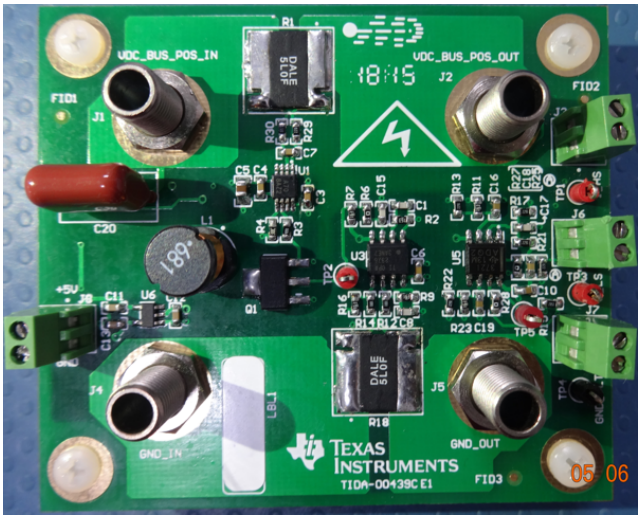
Design Features

- Shunt-Based Current Sensing for Inverter Control and Protection
- Rated to Measure DC Link Current of ±20A_{pk} (Design Tested for ±5 A)
- High-Side Current Sense Circuit With High Common Mode Voltage of 450 V Supporting 220-V AC Mains Powered Drives
- Calibrated High-Side and Low-Side Measurement Error Over Operating Temperature Range of −10°C to 55°C < 1.5%
- Ground Fault:
  - Minimum Fault Current Detection of 300 mA
  - Detection Time Less than 50 µs
- Designed to be Interfaced With Built-In 3.3-V Analog-to-Digital Converter (ADC) of Microcontroller (MCU)

Featured Applications

- Variable Speed Drives
- Consumer Appliances: Washing Machines, Refrigerators, Air Conditioners, and More





1 Introduction

Ground faults are one of the major causes of drive failures. Early detection of ground faults can avoid major drive damage, electrocution of personnel, and fire hazards. This TI design provides a reference solution to detect ground fault subsequently enabling shutdown of the inverter.

1.1 Ground Fault in Drives

A motor is considered to be a balanced three-phase load, which means that during normal operating condition of a drive system, the sum of the three-phase currents drawn from the source must be zero. Due to faults in the motor winding, faults in the cabling from the drive to the motor, or faults in the drive itself, current can leak into the earth through the chassis of the motor or drive and create ground fault. Current leak can cause hazardous situations and must be avoided.

Figure 1 shows an example ground fault condition. In a power distribution system the neutral wire is usually connected to the earth at the distribution transformer. In the motor drive system the chassis of the drive and motor are connected to the earth. Due to deterioration of the motor winding insulation, a resistance path is created between the winding and the chassis of the motor. This resistance path causes an earth leakage current to flow through the chassis into the earth and back into the neutral of the transformer, as Figure 1 shows.

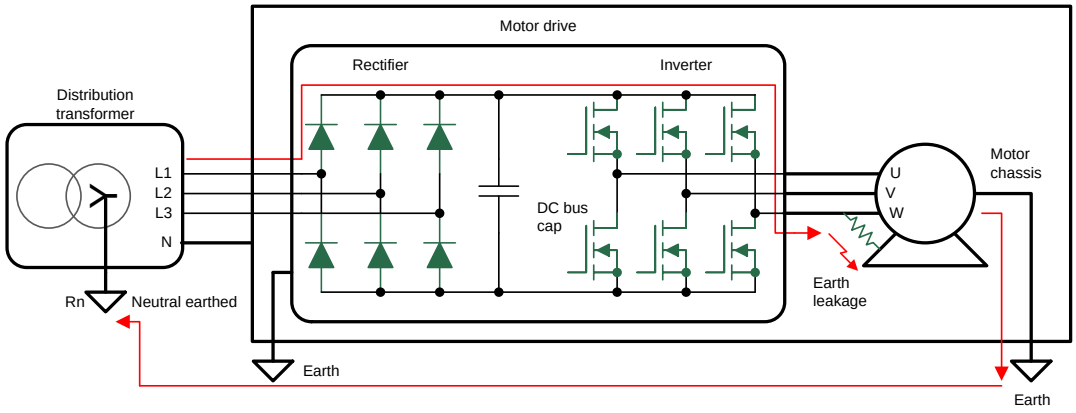


Figure 1. Ground Fault in Drive

1.2 Causes of Ground Fault

The main causes of ground fault are in the following list:

- **Faulty wiring**: During the installation of a motor drive system, the phase wire can be wrongly connected to the earth terminal of the motor or there could be a cut in the winding insulation that comes into contact with the motor chassis. This type of fault (dead short to earth) can result in high current flow into the earth wire upon starting the drive. This fault can be detected by fuses and circuit breakers in distribution systems where the transformer star point is connected to earth through low impedance. In case of high resistance earthing, where the fault current is limited, the user must utilize ground fault detection devices to detect the leakage current.
- **Insulation degradation**: The insulation of a motor phase winding to chassis degrades over time due to heating and aging. Current may start leaking from the phase into the earth through the degraded insulation.
- **Moist environment**: Moisture may condense onto the motor windings during the downtime. This moisture provides a path to earth and is one of the major causes of ground fault currents. Because of this hazard, fault protection is usually provided in moist operating environments such as water treatment plants, washdown areas of industrial plants, pumping applications, marine applications, and mining applications.

- **Dust**: Dust may provide a high resistance path to earth. Ground fault protection is usually provided to protect against dust in environments such as cement factories, mines, and gravel quarries.
- **Foreign object debris (FOD)**: During production conductive metal parts such as screws or metal pieces can enter into the motor during metal cutting or grinding. Mechanical vibrations can also cause screws, bolts, nuts, and washers to loosen and fall into the motor, which may lead to contact between the phase winding and chassis.

1.3 Required Use of Ground Fault Protection Devices

Motor drive systems are usually protected by fuses and circuit breakers for overcurrents. The trip levels of these protection mechanisms are usually set higher than the maximum current required by the system by a certain margin. Apart from a dead short between the inverter output and earth, even a high resistance path to earth can cause current leakage into the earth. Earth leakage currents through high resistance paths are smaller in magnitude and cannot be detected by overcurrent protection mechanisms.

Some of the hazards of ground leakage current are electrocution, arcing (which can pose fire hazards), and damage to the wiring insulation due to the continuous leakage of current through it. Ground currents also have an affect on the motor control algorithms if there is a current control loop involved. Ground currents are also an early indicator of insulation degradation. A ground fault protection circuit is required to avoid the possible hazards, prevent downtime, and inhibit loss due to a halt in production.

1.4 Ground Fault Sensitivity Levels

Ground fault protection devices have different sensitivity levels. A sensitivity level indicates the ground fault current at which the device responds. The sensitivity is expressed as the rated current difference, denoted as IΔn. Based on this rated current difference, the sensitivity levels can be categorized into the following groups:

- High sensitivity (HS): 6 to 10 to 30 mA (for direct-contact, life injury, and protection from electrocution)
- Medium sensitivity (MS): 100 to 300 to 500 to 1000 mA (for fire protection)
- Low sensitivity (LS): 3 to 10 to 30 A (for machine and device protection)

Choose a device with a a high, medium, or low sensitivity based on the application, required protection level, and environment.

2 System Description

A typical motor drive system powered from AC mains consists of an AC-DC converter and a DC-AC inverter along with a control circuit. Figure 2 shows the block diagram of the system. The mains supply can be single phase or three phase, 110-V AC or 220-V AC depending on the drive and the country in which the drive is to be used. The drive first converts the AC mains voltage into DC with the help of a power converter. The converter can be an active PFC or may be a simple bridge rectifier depending on the drive.

For 220-V AC mains powered drives, the nominal DC bus voltage is approximately 310-V DC. The maximum DC bus voltage in this design is rated up to 450-V DC. This rating accounts for the variation in the mains voltage as well the increase in the DC bus voltage due to motor regeneration.

In normal operating conditions, the current flowing from the DC bus positive into the inverter and the current flowing back from the inverter into the DC bus negative are equal. This current balance no longer holds true if earth leakage occurs. The TIDA-00442 ground fault detection circuit detects this unbalanced current. The circuit is inserted between the rectifier stage and the DC bus capacitor as Figure 2 shows.

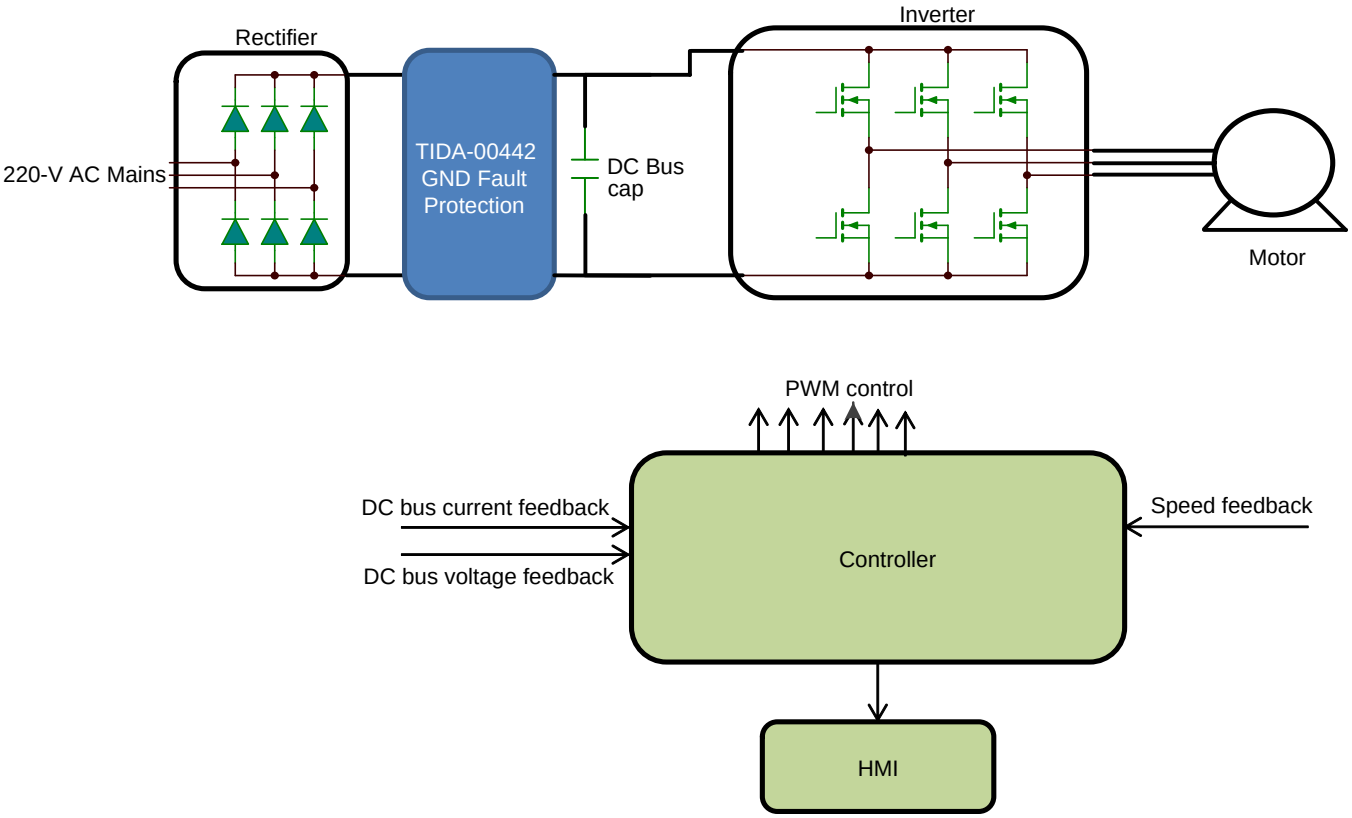


Figure 2. System Block Diagram

3 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
Drive AC input	220-V AC
DC bus voltage level maximum	450-V DC maximum
Maximum DC bus current	±20 A
Operating ambient temperature	–10°C to 55°C
Unbalanced current detection (GND fault current)	300 mA
Calibrated high-side and low-side current measurement error overtemperature range	< 1.5%
Features	Low-side and high-side current sense outputs designed to be interfaced to 3.3-V inbuilt ADCs of MCUs

4 Block Diagram

The ground fault detection block shown in Figure 2 is expanded in detail in Figure 3. The main sections are the shunt resistors, the low-side current sensing circuit, the high-side current sensing circuit, the GND fault detect comparator, and the low-side buck converter for generating the floating GND power supply for the INA170 device.

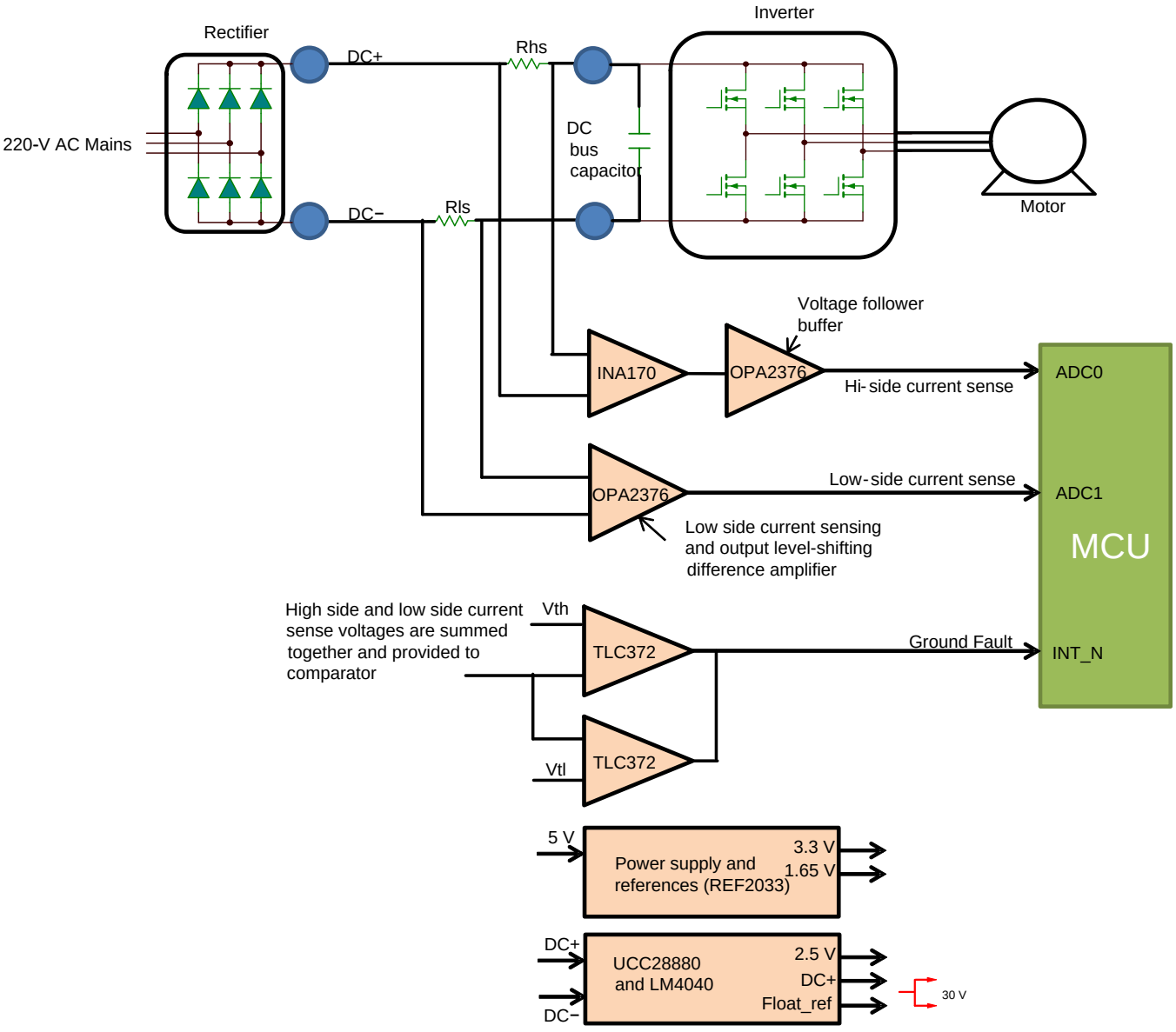


Figure 3. GND Fault Detection Circuit Block Diagram

The low-side current sensing circuit consists of a shunt resistor (RIs) and the OPA2376 op-amp. A difference amplifier implemented with the help of an OPA2376 op-amp has a level shift of 1.65 V, which allows the user to measure the bidirectional current. The OPA2376 op-amp is powered from a 3.3-V supply, which makes it compatible with the integrated ADCs of the MCU.

The high-side current sensing circuit consists of a shunt resistor (Rhs), current shunt monitor INA170, and the OPA2376 op-amp as a voltage follower buffer. The INA170 device is used along with a P-channel MOSFET on its output for blocking the high voltage and passing only the current output of the INA170 device. The high-side current sensing circuit also uses a floating GND reference, which enables it to measure current on the DC link with voltages up to 450 V.

The UCC28880 configured in the low-side buck converter topology is used to generate the floating GND. The LM4040 device is used to generate the 2.5-V reference with respect to the floating GND. The 2.5-V reference is used for level shifting the output of the INA170 device, enabling it to measure the bidirectional current.

The circuit is powered from 5-V DC, which is typically present in most industrial drives. The REF2033 reference is used to generate the 3.3-V supply and 1.65-V reference for the circuit.

The TLC372-based window comparator is used to detect ground faults. For better accuracy, the high-side and low-side current sense voltages can be acquired by an MCU and calibrated; then the ground fault current can be calculated.

4.1 Highlighted Products

The TIDA-00442 reference design features the following devices, which were selected based on their specifications. The following subsections detail the key features of the highlighted products.

For more information on each of these devices, see the respective product folders at www.ti.com or click on the links for the product folders on the first page of this reference design.

4.1.1 INA170—Current Output, High-Side, Bidirectional Current Shunt Monitor

The INA170 is a high-side, bidirectional current shunt monitor featuring a wide input common-mode voltage range, low quiescent current, and a tiny MSOP-8 package. Bidirectional current measurement is accomplished by output offsetting. The offset voltage level is set with an external resistor and voltage reference, which permits the measurement of a bidirectional shunt current while using a single supply for the INA170 device. The input common-mode and power-supply voltages are independent. The input voltage can range from 2.7 V to 60 V on any supply voltage from 2.7 V to 40 V. A low 10-µA input bias current adds minimal error to the shunt current. The INA170 device converts a differential input voltage to a current output. This current develops a voltage across an external load resistor, setting any gain from 1 to over 100. The INA170 device is available in an MSOP-8 package and is specified over the extended industrial temperature range, –40°C to +85°C with operation from –55°C to +125°C.

The INA170 device is chosen in the design for its bidirectional, current-shunt monitoring capabilities, a common-mode input voltage range that is independent of the supply voltage, and its current output stage. The current output stage enables the INA170 device to level shift the high voltage of the DC bus positive to the low voltage control stages using a voltage-blocking field effect transistor (FET), as Section 5.1.1 describes.

4.1.2 OPA2376—Low Noise, Low Quiescent Current, Precision Operation Amplifier

The OPA2376 is a low-noise, dual operational amplifier with e-trim that offers outstanding DC precision and AC performance. A Rail-to-rail input and output, low offset (25 µV max), low noise (7.5 nV/√Hz), quiescent current of 950 µA max, and a 5.5-MHz bandwidth make this part very suitable for precision applications. The integrated circuit (IC) is specified for operation from –40°C to +125°C.

The OPA2376 amplifier was chosen for its rail-to-rail input and output voltage ranges, very low input offset voltage, low offset voltage drift with temperature, low bias currents due to e-trim, and high bandwidth at a relatively low cost.

4.1.3 TLC372—TI LinCMOS™ Technology Dual Differential Comparator

The TLC372 is fabricated using TI's LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Each device features extremely high input impedance (typically greater than 10^{12}), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

The TLC372 device is chosen for the dual package, fast response time, and the open drain output so that the outputs can be ANDed with just a single pullup resistor.

4.1.4 REF2033—Low-Drift, Low-Power, Dual-Output V_{REF} and V_{REF} / 2-V Reference

Applications with only a positive supply voltage often require additional stable voltage in the middle of the ADC input range to bias input bipolar signals. The REF2033 reference provides a reference voltage for the ADC and a second highly accurate voltage that can be used to bias the input bipolar signals.

The REF2033 reference offers excellent temperature drift (8 ppm/°C, maximum) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 µA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (maximum) across the temperature range of –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Both the V_{REF} and V_{BIAS} have the same excellent specifications and can sink and source current equally well. Very long-term stability and low noise levels make these devices ideally-suited for high-precision industrial applications.

This device is chosen for its dual outputs in a very small package, a very low drift in the output with temperature, and for its V_{REF} and V_{BIAS} tracking for lower error.

4.1.5 UCC28880—700-V Lowest Quiescent Current Off-Line Switcher

The UCC28880 device integrates the controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling startup and operation directly from the rectified mains voltage. The low quiescent current of the device enables excellent efficiency. With the UCC28880 device, the most common converter topologies such as buck, buck-boost, and flyback can be built using a minimum number of external components. The UCC28880 device incorporates a soft-start feature for controlled startup of the power stage, which minimizes the stress on the power stage components.

The UCC28880 device was chosen for its integrated switching MOSFET and start-up current source, low standby power consumption (quiescent current consumption of less than 100 µA), and its internal current sense, which leads to a lower bill-of-materials (BOM) cost and board size.

4.1.6 LM4040—Precision Micropower Shunt Voltage Reference

The LM4040 series of shunt voltage references are versatile, easy-to-use references that cater to a vast array of applications. The two-pin fixed output device requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low dynamic impedance, low noise, and a low temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures. The LM4040 reference is packaged in space-saving SC70 and SOT23-3 packages and requires a minimum current of 45 µA (typical), which also makes it ideal for portable applications. The LM4040 device is characterized for operation over an ambient temperature range of –40°C to 85°C. This part is chosen for its small size and low reverse current requirement of 45 µA.

5 System Design Theory

The following subsections detail the design procedure for each of the circuit sections.

5.1 High-Side Current Measurement Solution

5.1.1 Design

The high-side current measurement circuit is designed to measure current on the DC positive bus, which can go up to 450-V DC. The 220-V AC powered drives have a nominal DC bus voltage of approximately 310-V DC. An extra margin of 100-V DC must be provided to accommodate the rise in DC bus voltage during the motor regeneration mode and the variations in the mains voltage.

The INA170 device has an input common-mode voltage range of 2.7 V to 60 V, which is independent of the supply voltage. To increase the common-mode voltage range of the INA170 device, the ground pin is floated to a high potential. The floating GND must always be at a voltage of less than 40 V from the DC bus voltage to ensure that the VCC of the INA170 device is within the specifications. This design uses a DC-DC converter to float the ground pin; however the ground pin of the INA170 device can also be floated to a high potential by using a Zener regulator. Both methods have their tradeoffs. The Zener regulator-based design is simple and inexpensive but the standby power dissipation is very high. The DC-DC converter-based solution is relatively complex and slightly more expensive, but the standby power dissipation is extremely low. The following subsections describe both designs. The printed circuit board (PCB) has been designed and tested with the DC-DC converter-based floating power supply.

Figure 4 shows the INA170-based, high-side current sense circuit with the floating GND reference.

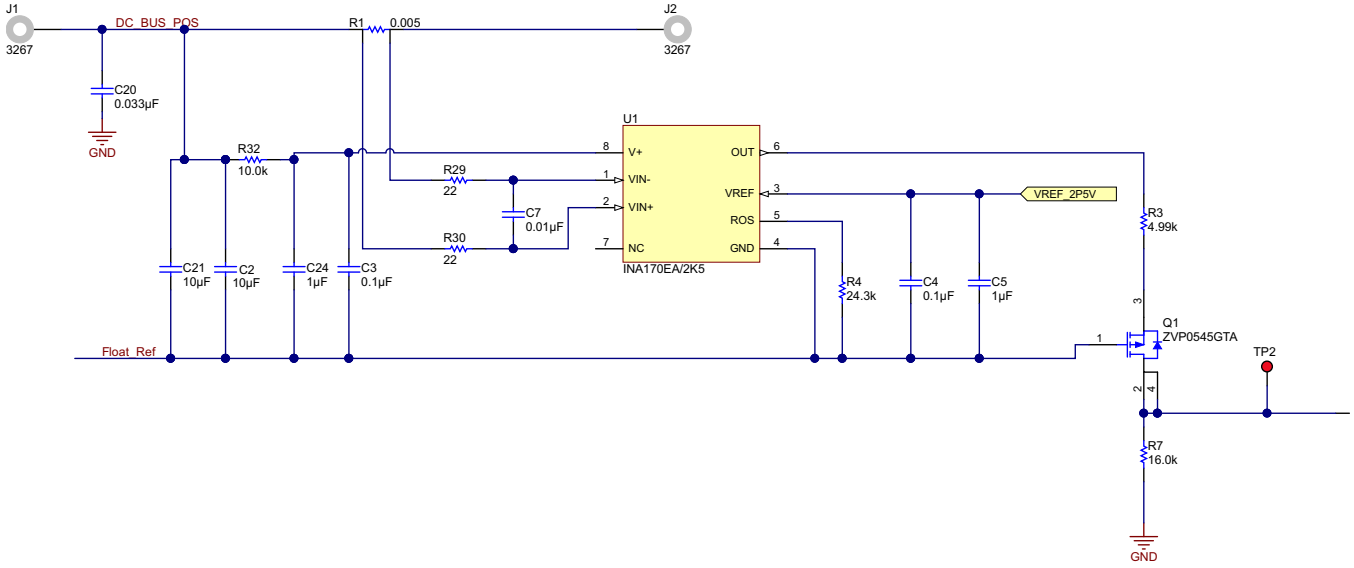


Figure 4. INA170 High-Side Current Sense Circuit

The DC bus positive is connected to the power supply pin of the INA170 device. The GND pin of the IC is floated to 30 V below the DC bus positive. A resistor-capacitor (RC) filter is used at the supply pin of the IC to filter the power supply noise. Resistor R32 is selected to be 10 KΩ and C24 is selected to be 1 µF, which gives the cutoff frequency of 15.91 Hz. Select a large value for C24 so that the voltage across this capacitor does not change much when supplying current to the IC.

The maximum specification for the DC link current for the TIDA-00442 design is ±20 Ap. The current shunt (R_1) inserted on DC positive bus is chosen such that the ±20 A generates a voltage of ±100 mV across current shunt resistor R1 (see Equation 1).

$$R_{HS\_sh} = \frac{V_{HS\_sh\_max}}{I_{DClink\_max}} = \frac{100\ m}{20} = 5\ m\Omega \quad (1)$$

Where R_{HS_sh} is the high side shunt resistance,
$V_{HS\_sh\_max}$ is the maximum voltage drop across the shunt,
I_{DClink_max} is the maximum current through the shunt

Equation 2 shows the calculation of the maximum power dissipated in the shunt.

$$P_{dissipated\_HS\_sh\_max} = I_{DClink\_max}^{2} \times R_{HS\_sh} = 20^{2} \times 5\ m = 2\ W \quad (2)$$

$P_{dissipated\_HS\_sh\_max}$ is the maximum power dissipated across the shunt resistor. For this design, a 5-mΩ shunt resistor is selected with a wattage rating of 3 W.

A differential filter is used between the shunt and the IC to reject any noise entering into the inputs. The voltage drop across the resistors due to the input bias current appears as an input offset voltage, which contributes to the measurement error; thus this voltage drop must be minimized. So, select low values for R29 and R30. The cutoff frequency is selected such that it allows the signal frequency to pass through but blocks all the noise. Capacitor C7 is chosen as 0.01 µF and resistors R29 and R30 as 22 Ω, which results in the following filter cutoff frequency in Equation 3:

$$f_c = \left(\frac{1}{(2\pi\ (R29 + R30)\ C7)} \right) = \left(\frac{1}{(2\pi \times 44 \times 0.01\ \mu)} \right) = 361.7\ KHz \quad (3)$$

The INA170 is a current output device. The output current is converted into voltage by passing it through resistor R7. The function of the P-channel MOSFET Q1 is to pass the output current of the INA170 device to R7 while blocking the high DC bus voltage from appearing across R7. A PNP transistor can be chosen instead of the PMOS due to the PNP transistor's smaller size and lower cost. The disadvantage of the bipolar junction transistor (BJT) is that the output of the INA170 device must supply the base current of the PNP BJT. Some of the output current is diverted into the base of the transistor, causing an error in the current through R7. For example, a PNP BJT with an H_{fe} of roughly 100 will have approximately 1% of the emitter current flowing out of the base. This reduction in collector current adds an error of about 1% on the voltage output. The H_{fe} of a PNP transistor also varies with temperature, which adds a temperature drift to the gain error. These errors are avoidable by using a P-channel MOSFET. The tradeoffs of using a P-channel MOSFET are a relatively larger size and cost. The important criteria for FET selection is that it must be able to withstand the maximum voltage of the DC bus. The ZVP0545GTA device is selected for this application as it can withstand a drain-to-source voltage of −450 V and has a continuous drain current rating of −75 mA.

The transfer function of the circuit in Figure 4 is given by the following Equation 4:

$$V_{out} = \left(\frac{Vref \times R7}{R4} \right) + \left(\frac{V_{R1} \times R7}{1\ k\Omega} \right) \quad (4)$$

Detecting the bidirectional current with an opamp powered from an unipolar supply requires an output offset. This offset voltage is equal to the following term from Equation 4:

$$\left(\frac{V_{REF} \times R7}{R4} \right)$$

where

- V_{REF} is chosen to be 2.5 V
- R7 is chosen as 16 kΩ
- R4 is equal to 24.3 kΩ

Substituting the preceding values in Equation 4 results in Equation 5:

$$V_{out} = 1.64609 + (16 \times V_{R1}) \quad (5)$$

The transimpedance gain of the circuit is given by the term R7 / 1 kΩ in Equation 4, which is equal to 16 in this design. The offset voltage is 1.64609 V.

When the DC link current varies from +20 A to −20 A, the voltage across shunt resistor R1 changes from 100 mV to −100 mV. Corresponding to this change, the output voltage changes from 3.24609 V to 0.04609 V.

An op-amp buffer stage succeeds the INA170 stage and is used to buffer the signal to the ADC (see Figure 5).

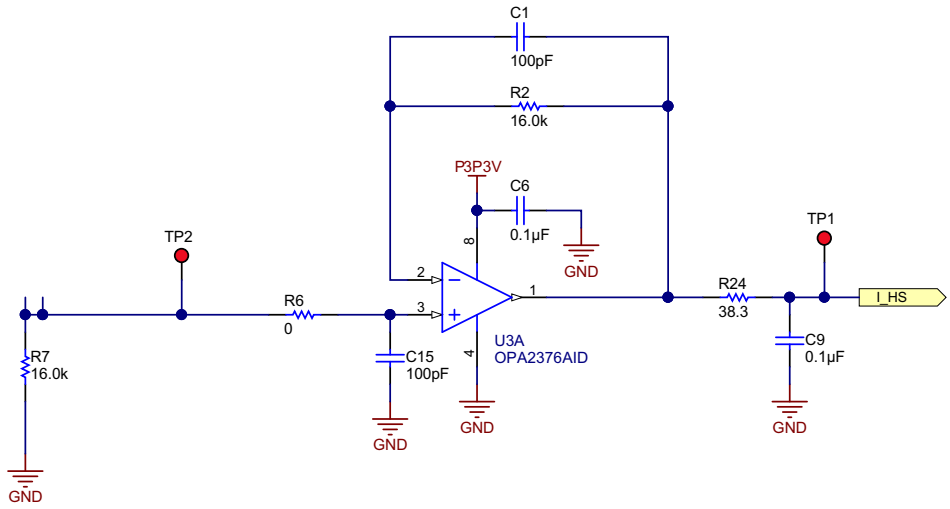


Figure 5. High-Side Current Sense Output Buffer

The resistor R2 is added to the feedback path of the voltage-follower buffer stage to cancel the input offset due to the op-amp input bias current that flows through R7.

5.1.2 Simulation Using TINA-TI™ Software From TI

The design is simulated in the TINA-TI software to verify the functionality of the circuit. All of the applicable SPICE models can be found on the respective device product folders on the TI website. The current through the shunt resistor R1 in Figure 6 is varied from −20 A to 20 A. This is done by keeping V_DC_BUS constant at 310 V and varying VG1 from 0 V to 620 V. By doing this the common mode to INA170 can be maintained constant at 310 V and the current through R1 can be varied from –20 A to 20 A if RL is selected to be 15.5 Ω. The floating power supply of 30 V is simulated with the help of V_Float supply and Rfl. The output of the INA170 and OPA2376 devices are monitored.

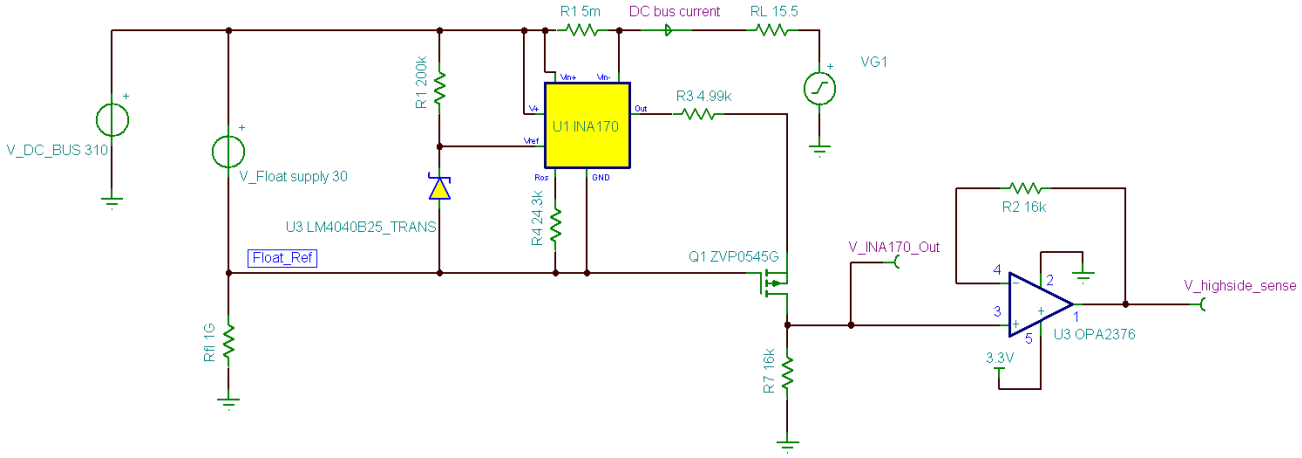


Figure 6. INA170 High-Side Current Sensing Simulation Model

The DC bus current is varied from –20 A to 20 A linearly from 5 ms to 15 ms; Figure 7 shows the variation of the INA170 and OPA2376 outputs.

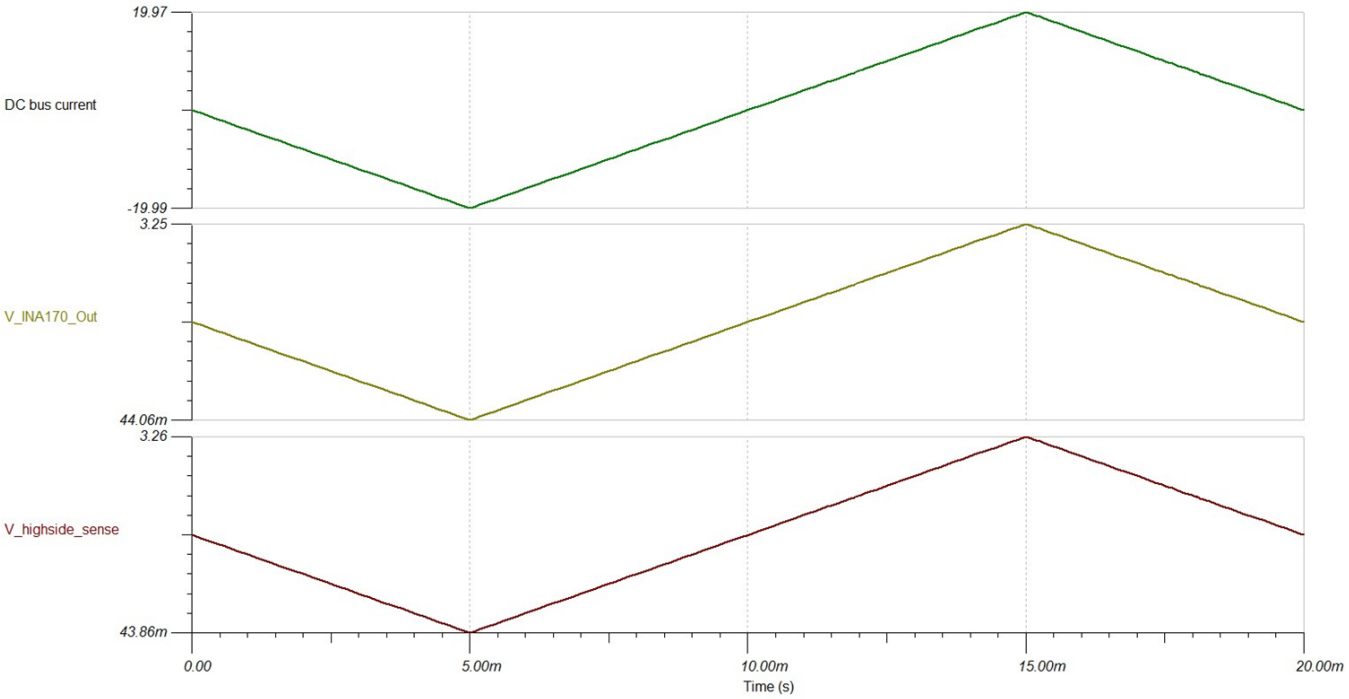


Figure 7. Simulation Results for INA170 High-Side Current Sense

5.1.3 DC-DC Converter-Based Power Supply for INA170

The standby power dissipation of the Zener regulator is about 0.430 W as Section 5.1.4 explains. The user can reduce this power dissipation by implementing a DC-DC converter-based solution. During testing, this power dissipation is measured to be less than 75 mW. This DC-DC converter must have a very low standby power consumption to improve the energy efficiency of the equipment. The UCC28880 part is chosen to implement a low-side switched buck converter to supply power to the INA170 device. This UCC28880 device offers a best-in-class operating current of less than 100 µA, which helps to reduce the standby-mode power consumption. The device is also self biased, so it does not require a power supply. The UCC28880 device also delivers robust operation by protecting the system during load short and inductor current runaway faults.

The controller has an integrated power MOSFET switch rated to 700-V drain-to-source voltage. The PWM signal generation is based on the maximum constant ON-time, minimum OFF-time concept, with the triggering of the ON-pulse depending on the feedback voltage level. The low-side buck converter generates a negative voltage with respect to the DC bus voltage. This pin is connected to the GND pin of the INA170 device and the DC bus voltage is connected to the INA170 supply pin to generate the floating power supply for the INA170 device.

Figure 8 shows the design of the low-side buck converter.

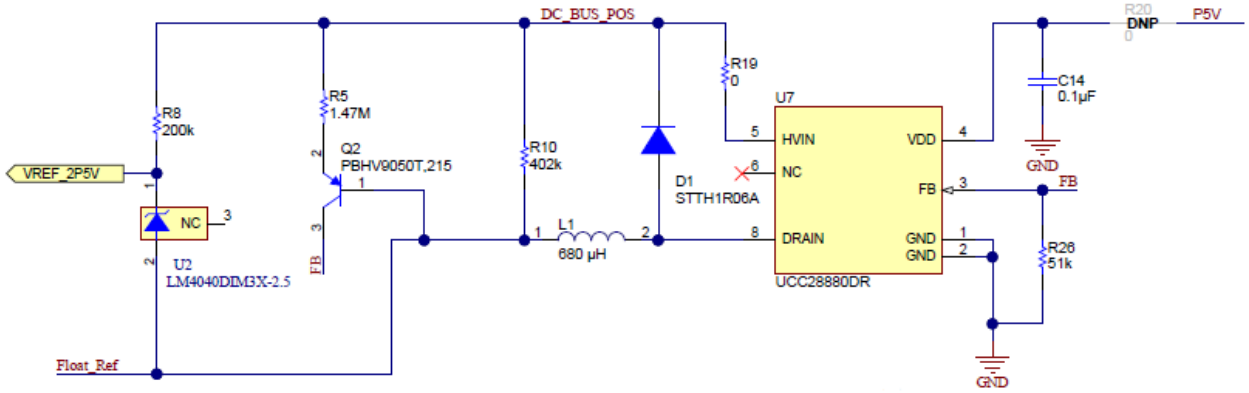


Figure 8. Low-Side Buck Converter Power Supply for INA170

The INA170 requires a 30-V power supply. For this supply, the GND pin of the INA170 device must be regulated to 30 V below the DC bus voltage. This is achieved with the help of direct level-shifted feedback using components R5, Q2, and R26. R5 sets the current through the feedback path and R26 sets the output voltage. Q2 acts as the level shifter and must be rated for high voltage. For this design, the PBHV9050T,215 PNP BJT is chosen for Q2 because of its small size (SOT23 package), low cost, and ease of availability. Determine the output voltage according to Equation 6:

$$V_{out} = \left(V_{FB\_TH} \times \frac{R5}{R26} \right) + V_{BE}$$

where

- V_{out} is the output voltage
- V_{FB_TH} is the FB pin voltage threshold
- V_{BE} is the base emitter saturation voltage of the external PNP transistor
- R5 is the external resistor setting the output voltage
- R26 is the external resistor setting the current through the external feedback path (6)

To minimize the power dissipated in the feedback path, select a low current of approximately 20 µA to flow through the external feedback path. To select the current to be 20 µA, select R26 according to Equation 7.

$$R26 = \frac{V_{FB\_TH}}{I_{FB}} = \frac{1}{20\ \mu A} = 50\ k\Omega \quad (7)$$

R26 is selected to be 51 kΩ which is close to the value calculated in Equation 7.

To regulate the output voltage to 30 V below the DC bus voltage, R5 must be selected according to Equation 8:

$$R5 = \frac{V_{out} - V_{BE}}{V_{FB\_TH}} \times R26 = \frac{30 - 0.5}{1} \times 51\ k\Omega = 1.505\ M\Omega \quad (8)$$

In Equation 9, select the standard resistor value of 1.47 MΩ, which gives a V_{out} equal to:

$$V_{out} = \left(V_{FB\_TH} \times \frac{R5}{R26} \right) + V_{BE} = \left(1 \times \frac{1.47\ M\Omega}{51\ k\Omega} \right) + 0.5 = 29.32\ V \quad (9)$$

The feedback current is always ON. To reduce the power dissipation, select a lower feedback current. The tradeoff for selecting a lower feedback current is that it results in a noise-sensitive feedback.

Load resistor (R10)

The user must choose the load resistor such that the output current in any standby or no-load condition is higher than the leakage current through the integrated power MOSFET. The maximum OFF state leakage current for the power MOSFET is specified to be 20 uA at V_{drain} = 400 V at junction temperature of T_j = 125°C. A load resistor is not required if the standby load current is ensured to be greater than the specified leakage current. The standby load current in the TIDA-00442 design (which consists of the quiescent supply current of the INA170 device and an offset setting current), is more than the leakage current of the power MOSFET. The R10 resistor is not fitted on the PCB and is provided as a provision.

Freewheeling diode (D1)

The user must select a freewheeling diode that can handle high voltage with a reverse recovery time that is as short as possible. A higher reverse recovery time leads to higher switching losses and lower efficiency.

Equation 10 shows the maximum reverse voltage that the diode experiences during normal operation.

$$V_{D1max} = V_{DCbusmax} = 450\ V \quad (10)$$

Consider a general margin of 20% for the maximum reverse voltage.

The freewheeling diode chosen for the TIDA-00442 design is the STTH1R06A, which is a 600-V rated device with a maximum reverse recovery time trr = 25 ns.

Regulator capacitor (C14)

This capacitor acts as the decoupling capacitor and storage capacitor for the internal regulator. A 100-nF ceramic capacitor is enough for proper operation of the device's internal low-dropout (LDO) regulator.

Output capacitor (C2)

The value of the output capacitor and its equivalent series resistor (ESR) impacts the output ripple voltage. A larger capacitance value results in a lesser output voltage ripple, but the start-up time increases. Selecting a capacitor with a low ESR value also reduces the ripple on the output voltage. This TIDA-00442 design uses an output capacitor of 20 µF.

Inductor (L1)

The selected inductance value for this design is 680 µH. The converter operates in burst mode because of the very low output load.

The LM4040-2.5 device is used to generate the 2.5-V reference for the INA170 output offsetting. The reverse current operating range is 60 µA to 15 mA. Resistor R8 functions to limit the current through the LM4040 device. R8 is selected to be 200 KΩ, which limits the current through U2 to 138 µA.

5.1.4 Zener Regulator Power Supply Option for INA170

If power dissipation is not a concern, the user can implement an inexpensive, simple solution with minimum BOM components to generate the floating power supply instead of the DC-DC converter. The solution that Figure 9 shows consists of a Zener diode D1 connected in series with resistors R5, R10, and U2 between the DC bus positive and the GND. The voltage drop across the Zener diode and U2 is the input power supply to the INA170 device. This supply is not referenced to GND but to the voltage drop across R5 and R10. The LM4040 IC is used to generate the reference voltage of 2.5 V for the INA170 device. The reference voltage is used to offset the output to enable bidirectional current measurement.

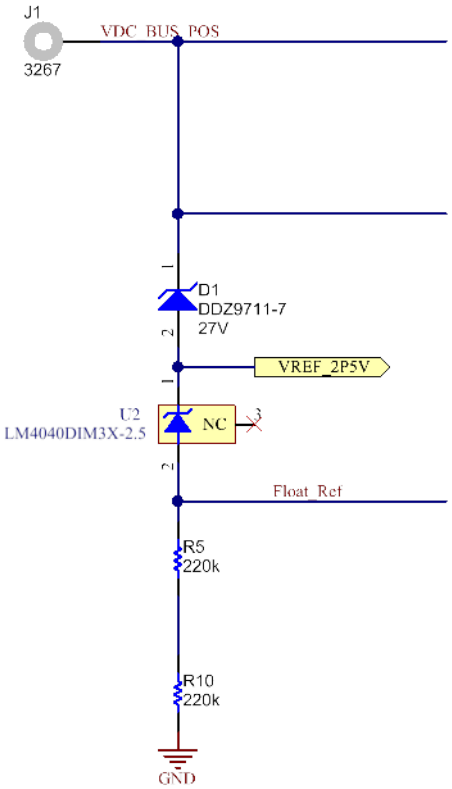


Figure 9. Zener Diode Floating Power Supply

This subsection addresses the design of a Zener regulator with an output voltage of 30 V. The Zener diodes used in series are DDZ9711-7 with V_z = 27 V and U2 with V_z = 2.5 V.

The following list defines the variables used throughout Equation 11 through Equation 16.

- R_{max} is the maximum series resistance allowed
- R_{min} is the minimum series resistance required
- V_{Rmin} is the minimum voltage drop across the series resistor
- V_{Rmax} is the maximum voltage drop across the series resistor
- V_{DCmin} is the minimum DC bus voltage = 280-V DC as in the case of 220-V AC drives (10% variation)
- V_{DCmax} is the maximum DC bus voltage = 450-V DC as in the case of 220-V AC drives
- V_{Zmax} is the maximum Zener voltage drop from the datasheet of DDZ9711-7
- V_{Zmin} is the minimum Zener voltage drop from the datasheet of DDZ9711-7
- I_{Zmin} is the minimum Zener current which is selected to be 100 µA
- I_{Zmax} is the maximum Zener current from the datasheet of DDZ9711-7
- I_{Lmax} is the maximum load current (required by INA170 when its output is fully loaded)
- I_{Lmin} is the minimum load current (quiescent current for INA170)

A minimum reverse current is required to flow through the Zener diodes D1 and U2 to enable their operation. This minimum reverse current limits the maximum series resistance. Equation 11 calculates the maximum permissible resistance:

$$R_{max} = \left(\frac{V_{Rmin}}{I_{Zmin} + I_{Lmax}} \right) = \left(\frac{V_{DCmin} - V_{Zmax}}{I_{Zmin} + I_{Lmax}} \right) = \left(\frac{280 - (28.35 + 2.525)}{100\mu + 350\ \mu} \right) = 553.61\ k\Omega \quad (11)$$

To limit the power dissipation across the Zener diode, the current that flows through the Zener diode must be limited. Equation 12 shows the minimum resistance required in series with the Zener diode to limit the current within safe limits.

$$R_{min} = \left(\frac{V_{Rmax}}{I_{Zmax} + I_{Lmin}} \right) = \left(\frac{V_{DCmax} - V_{Zmin}}{I_{Zmax} + I_{Lmin}} \right) = \left(\frac{450 - (25.65 + 2.475)}{10\ m + 125\mu} \right) = 41.67\ k\Omega \quad (12)$$

Select R = 440 kΩ (near the higher end of the limit) to reduce power dissipation. Two 500-V, 220-kΩ, 0.25-W resistors R5 and R10 are connected in series to share the 420-V drop across them as well as the power dissipated.

The following equations calculate the total power dissipation in the Zener diode-based regulator.

Equation 13 calculates the power dissipated in Zener diode D1:

$$P_{D1nom} = V_{D1nom} \times I_{ZD1} = V_{D1nom} \times \left(\frac{V_{DCmax} - V_{out}}{R_5 + R_{10}} \right) = 27 \times \left(\frac{450 - 29.5}{440\ k} \right) = 25.80\ mW \quad (13)$$

Equation 14 calculates the power dissipated in shunt reference IC U2:

$$P_{U2nom} = V_{U2nom} \times I_{ZU2} = V_{U2nom} \times \left(\frac{V_{DCmax} - V_{out}}{R_5 + R_{10}} \right) = 2.5 \times \left(\frac{450 - 29.5}{440\ k} \right) = 2.39\ mW \quad (14)$$

Equation 15 calculates the power dissipated in the series resistors:

$$P_{Rnom} = (R_5 + R_{10}) \times I_Z^2 = (R_5 + R_{10}) \times \left(\frac{V_{DCmax} - V_{Znom}}{(R_5 + R_{10})} \right)^2 = 440\ k \times \left(\frac{450 - 29.5}{440\ k} \right)^2 = 401.86\ mW \quad (15)$$

Equation 16 calculates the total power dissipated in the regulator:

$$P_{Dmax} = P_{D1nom} + P_{U2nom} + P_{Rnom} = 0.430\ W \quad (16)$$

5.2 Low-Side Current Measurement Solution

5.2.1 Design

Figure 10 shows the low-side current sensing circuit. The difference amplifier topology is used for measuring the voltage drop across the low-side shunt resistor R14.

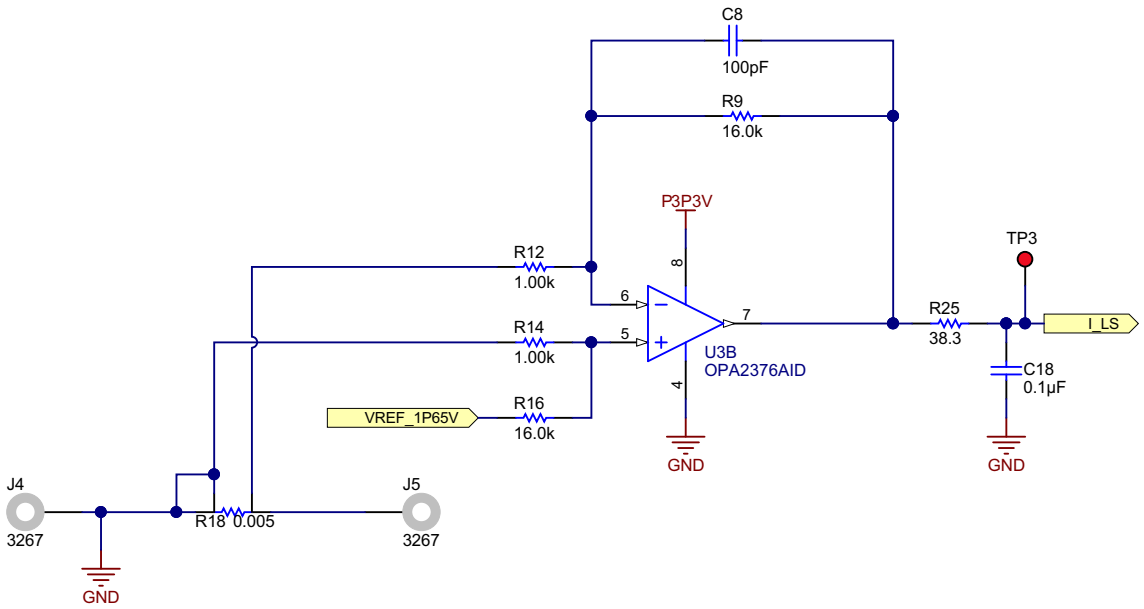


Figure 10. Low-Side Current Measurement Circuit

The criteria for selecting the low-side current sense resistor R18 is the same as the criteria for selecting the high-side current sense resistor. Thus the low-side current sense resistor is selected to be 5 mΩ with 3 W.

The transfer function of the difference amplifier is given by Equation 17. Refer to Figure 10 for the reference designators.

$$V_{out} = \left(\frac{R_{14}\left(R_{12} + R_9\right)}{R_{12}\left(R_{14} + R_{16}\right)}\right) V_{REF} + \left(\frac{R_{16}\left(R_{12} + R_9\right)}{\left(R_{14} + R_{16}\right) R_{12}}\right) V_{in\_p} - \left(\frac{R_9}{R_{12}}\right) V_{in\_n} \quad (17)$$

Using the following values where V_{REF} = 1.65 V, R14 = R12, and R16 = R9, Equation 17 simplifies to Equation 18:

$$V_{out} = V_{REF} + \left(\frac{R_9}{R_{12}}\right) V_{in\_p} - \left(\frac{R_9}{R_{12}}\right) V_{in\_n}$$

where

- V_{in_p} is the non-inverting input of the difference amplifier
- V_{in_n} is the inverting input of the difference amplifier (18)

$V_{in\_p} - V_{in\_n} = V_{R18}$ is the voltage drop across the low-side shunt resistor R18. V_{in_p} is connected to GND and V_{in_n} is connected across R14 with respect to GND to obtain the inverted output. Section 5.3 explains the reason for the inverted output. Equation 18 simplifies to Equation 19:

$$V_{out} = V_{REF} - V_{R18}\left(\frac{R_9}{R_{12}}\right) \quad (19)$$

The ±20-A current that flows through shunt resistor R18 creates a voltage drop of ±100 mV across the entire resistor. This range must be converted into a 0- to 3.3-V dynamic input range of the ADC. Using V_{REF}, the 0 A is level shifted to 1.65 V and a gain of 16 is selected to map ±100 mV to ±1.6 V around 1.65 V. Equation 19 simplifies to Equation 20:

$$V_{out} = 1.65 - \left(16 \times I_{DClink} \times R_{18}\right) \quad (20)$$

where

- I_{DClink} is the DC bus current

When the DC bus current changes from −20 A to +20 A, the output changes from 3.25 V to 50 mV. The OPA2376 output voltage swing is limited up to 20 mV from the rails and 40 mV overtemperature. Because of these limitations, the output voltage must be limited to 50 mV from the rails.

5.2.2 Simulation Results Using TINA-TI™ Software From TI

The DC bus current is simulated with the help of a current source, I_DC_BUS. The current that flows through shunt resistor R18 in Figure 11 is varied linearly and the output V_lowside_sense is monitored.

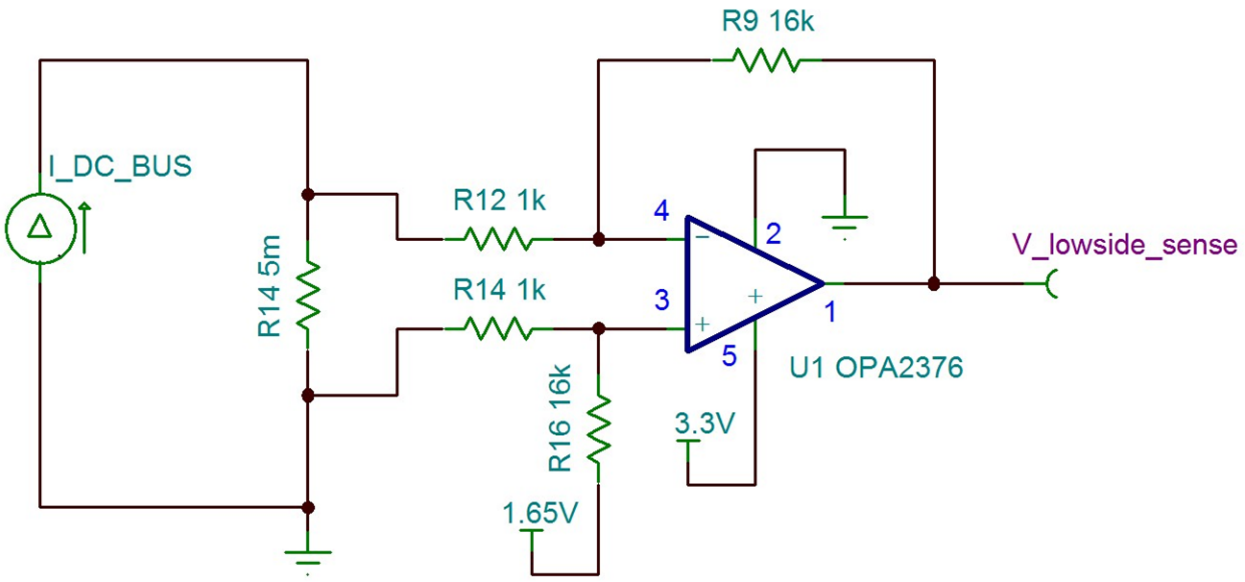


Figure 11. Low-Side Current Sense Amplifier

The DC bus current is varied from 20 A to −20 A linearly from 5 ms to 15 ms. Figure 12 shows the variation of low-side sense voltage.

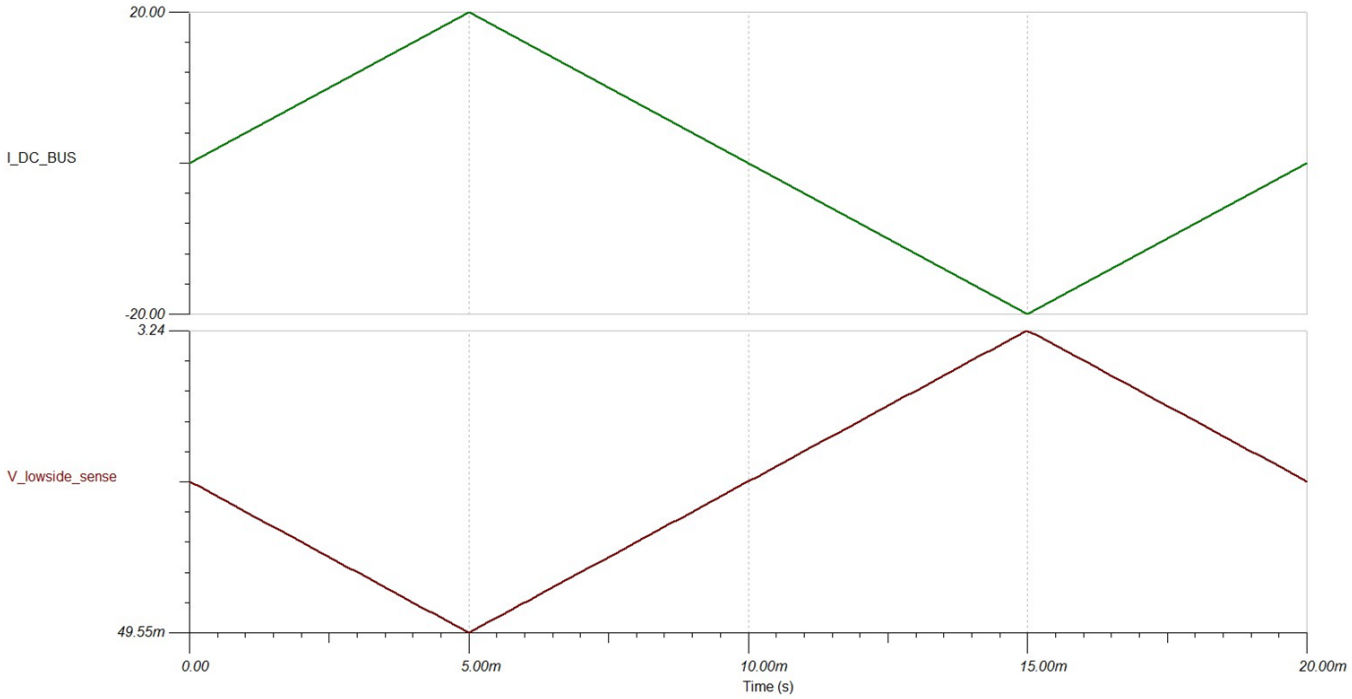


Figure 12. Simulation Results for Low-Side Current Sense Amplifier

5.3 Ground Fault Detect Comparator

Figure 13 shows the comparator circuit used to detect the ground fault. The comparator triggers when the difference between the high-side current and the low-side current is more than the set threshold (±300 mA in this case). Window comparators are used for this functionality. The upper comparator detects when the high-side current exceeds the low-side current by 300 mA and the lower comparator detects if the high-side current is less than the low-side current by 300 mA. The TIDA-00442 design uses the TLC372 device, which contains dual comparators in a single package, a fast response time, and an open-drain output, which helps to logic AND the outputs of the two comparators with the help of a single pullup resistor R20.

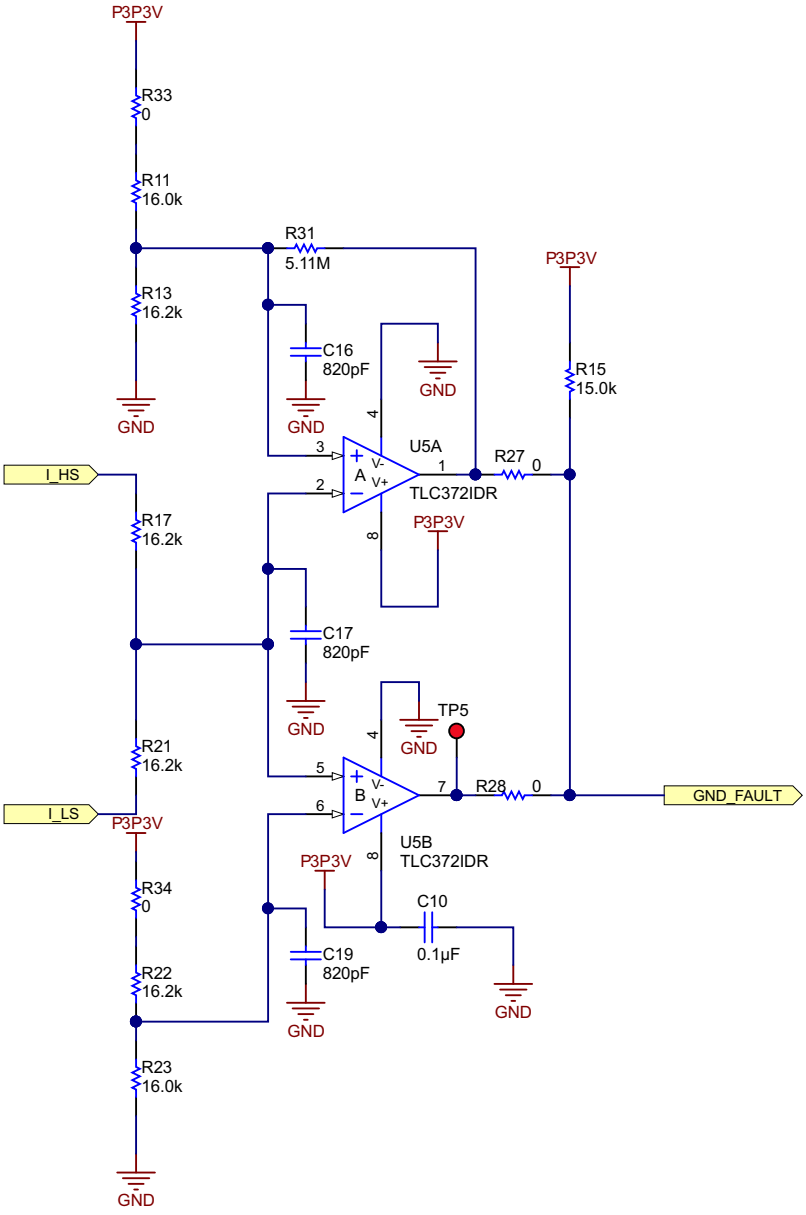


Figure 13. GND Fault Comparator Circuit

The average of the high-side and low-side current sense voltages (V_{mid}) is compared with the upper threshold voltage and lower threshold voltage. Select the threshold voltage using the following Equation 21.

$$\text{Threshold voltage} = \frac{\text{Ground fault current to be detected} \times \text{Shunt resistor} \times \text{Gain}}{2} \quad (21)$$

Insert the values for a 300-mA ground fault limit in Equation 21 to calculate Equation 22, Equation 23, and Equation 24:

$$\text{Threshold voltage} = \frac{300\ \text{mA} \times 5\ \text{m}\Omega \times 16}{2} = 0.012\ \text{V} \quad (22)$$

$$\text{Upper threshold} = V_{REF} + \text{Threshold voltage} = 1.65 + 0.012 = 1.662\ \text{V} \quad (23)$$

$$\text{Lower threshold} = V_{REF} - \text{Threshold voltage} = 1.65 - 0.012 = 1.638\ \text{V} \quad (24)$$

Resistor divider networks are used to generate the upper and lower threshold voltages from the 3.3-V supply. Resistors R11 and R13 generate the upper threshold voltage and R22 and R23 generate the lower threshold voltage. Use resisors R33 and R34 to finely calibrate the threshold voltage manually. R31 is the hysteresis setting resistor. The transfer functions of the high-side current sense circuit and the low-side current sense circuit have the same slope but different signs. The transfer function is set up this way so that the average of both circuits remain the same for any value of current flowing through them in the normal operating condition, as Equation 28 shows. The ideal average of the high-side and low-side current sense outputs is exactly 1.65 V, but due to offset and gain errors in both the signal paths, the actual average will deviate from this voltage. The threshold resistor values must be calibrated during the board testing. The comparator output provides indication of the earth fault, which can be connected to the interrupt of the MCU. On an interrupt, the MCU can acquire both the high-side and low-side current sense voltages, calibrate the sensed values, and estimate the accurate value of the ground fault current.

Equation 25 calculates the upper threshold voltage:

$$\text{Vuth} = 3.3 \times \left(\frac{R_{13}}{R_{13} + R_{11}}\right) = 3.3 \times \left(\frac{16.2\ \text{k}}{16.2\ \text{k} + 16\ \text{k}}\right) = 1.6602 \quad (25)$$

Equation 26 calculate the lower threshold voltage:

$$\text{Vlth} = 3.3 \times \left(\frac{R_{23}}{R_{23} + R_{22}}\right) = 3.3 \times \left(\frac{16\ \text{k}}{16\ \text{k} + 16.2\ \text{k}}\right) = 1.6398 \quad (26)$$

Equation 27 solves for V_{mid}, which is the voltage at the junction of resistors R13 and R17:

$$V_{mid} = \frac{(\text{I\_HS} \times R_{21}) + (\text{I\_LS} \times R_{17})}{(R_{17} + R_{21})} \quad (27)$$

If R17 = R21, then V_{mid} becomes the average of I_HS and I_LS (see Equation 28), which is ideally 1.65 V:

$$V_{mid} = \frac{(\text{I\_HS}) + (\text{I\_LS})}{2} \quad (28)$$

The TLC372 device has an open-drain output. In the normal operating condition, V_{mid} is between the upper and lower thresholds. In this case both the comparators are in the open-drain output condition and the outputs are tied together and pulled up to 3.3 V through R15. If the V_{mid} signal moves either above the upper threshold or below the lower threshold, the output of the respective comparator is pulled down to zero. Select R15 to be large enough to limit the power dissipation during this state.

5.4 Power Supply and Reference Section

In this application a bipolar signal (bidirectional DC link current) must be sensed using a unipolar power supply. To sense the bipolar signal using a unipolar power supply, the user must level shift the output of the signal conditioning stages to the midpoint of the power supply rail. A voltage reference is required to bias the signal conditioning stage outputs to the middle of the ADC dynamic range. The REF2033 IC provides both the 3.3-V supply to the op-amps as well as the 1.65-V reference voltage for biasing the signal to the middle of the ADC range. Both the outputs of the REF2033 IC can sink or source 20 mA. The tracking between the 3.3-V supply and 1.65-V supply is excellent and both the supplies are available in a single, tiny SOT23-5 package that reduces the BOM count and board size.

Figure 14 shows the power supply section.

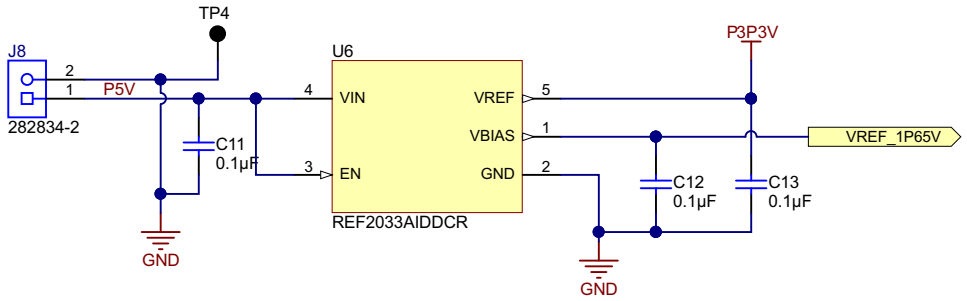


Figure 14. Power Supply and Reference Circuit

The IC is supplied with a 5-V power supply. The outputs are 3.3 V and 1.65 V. Place 0.1-µF noise decoupling capacitors close to the IC pins for a clean power input and output rails.

Table 2 shows the load on both the 3.3-V supply as well as the 1.65-V bias source.

Table 2. Power Supply Load Calculation for TIDA00442

SI NO	NAME OF IC OR COMPONENT	POWER SUPPLY OR REFERENCE USED	MAX CURRENT TAKEN BY THE IC (mA)	POWER CONSUMPTION (mW)	TOTAL OUTPUT CURRENT (mA)
1	OPA2376	3.3 V	2.29	7.557	3.115
2	TLC372	3.3 V	0.4	1.32	
3	Comparator output pullup resistor R15	3.3 V	0.22	0.726	
4	Comparator input references	3.3 V	0.205	0.6765	
5	OPA2376	1.65 V	0.097	0.16	0.097

The maximum load on a 3.3-V supply is 3.115 mA and the total load on a 1.65-V supply is 97 µA. The TIDA-00442 design uses a REF2033 IC with a sink and source capability of 20 mA.

6 Test Data

The TIDA-00442 board can be used with a DC bus voltage of up to 450-V DC. This specification includes 100-V AC or 110-V AC mains-powered drives as well as 220-V AC mains-powered drives. Therefore the board test results are split into two sections for the 310-V DC bus voltage (220-V AC mains-powered drives) as well as the 170-V DC bus voltage (110-V AC mains-powered drives).

The following tests are carried out on the design:

- High-side and low-side current measurement error
- Measurement error across different DC link voltages
- Measurement error across operating temperatures from −10°C to 55°C
- Detection of ground fault scenario and response time
- Testing on C2000 motor control kit for ground fault operation

6.1 Test Results for 310-V DC Bus Voltage (220-V AC Mains-Powered Drives)

6.1.1 High-Side and Low-Side Current Measurement Error

Figure 15 shows the test setup for measuring the error in high-side and low-side current measurement circuits. A variable load is connected to a high-voltage DC power supply through the TIDA-00442 board. An external DC power supply supplies the 5 V to power up the board. The high-voltage DC power supply (which simulates the DC bus voltage in the actual drive) is set to 310-V DC. The load is varied from −5 A to +5 A with the help of the variable electronic load and the high-side and low-side current measurement outputs are recorded.

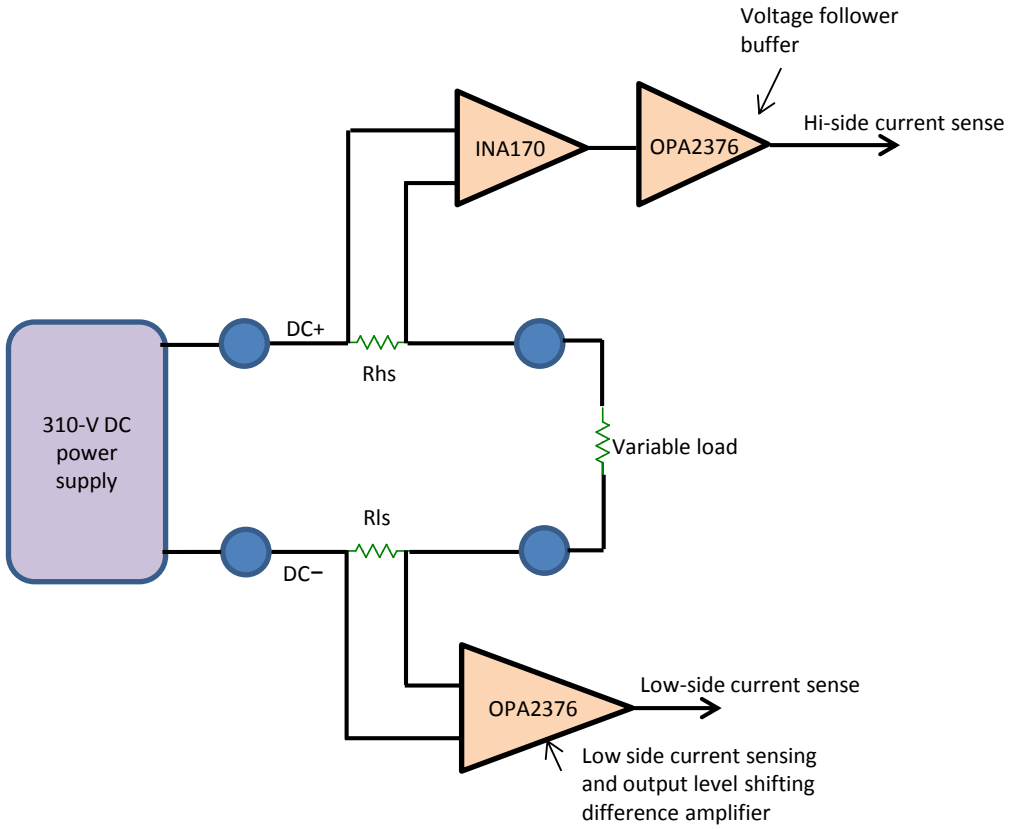


Figure 15. Test Setup for TIDA-00442 High-Side and Low-Side Current Measurement Error

Figure 16 shows a graph of the variation of current measurement error versus the DC bus current and Figure 17 shows the calibrated result. Table 3 shows the corresponding readings.

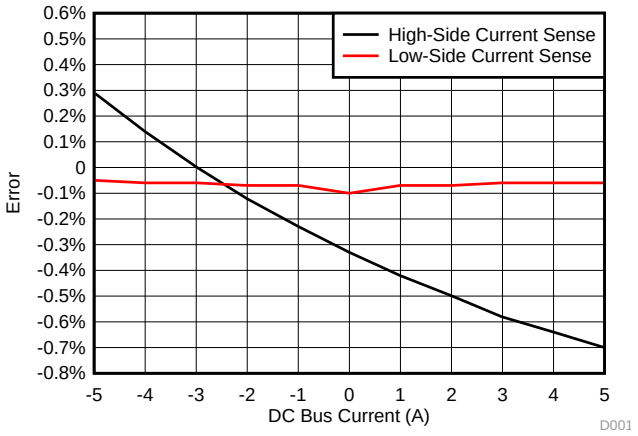


Figure 16. Current Sense Error Versus DC Bus Current (Non-Calibrated)

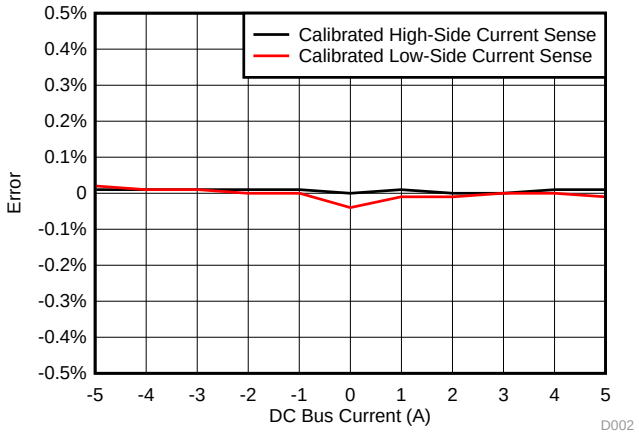


Figure 17. Current Sense Error Versus DC Bus Current (Calibrated)

Table 3. Current Sense Output and Error Versus DC Bus Current

DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE (V)	CALIBRATED HIGH-SIDE CURRENT SENSE VOLTAGE (V)	HIGH-SIDE CURRENT SENSE ERROR	CALIBRATED HIGH-SIDE CURRENT SENSE ERROR	LOW-SIDE CURRENT SENSE VOLTAGE (V)	CALIBRATED LOW-SIDE CURRENT SENSE VOLTAGE (V)	LOW-SIDE CURRENT SENSE ERROR	CALIBRATED LOW-SIDE CURRENT SENSE ERROR
–4.994	1.2454	1.2490	0.29%	0.01%	2.0517	2.0506	–0.05%	0.02%
–4.004	1.3245	1.3264	0.14%	0.01%	1.9723	1.9711	–0.06%	0.01%
–2.983	1.4065	1.4065	0.00%	0.01%	1.8902	1.889	–0.06%	0.01%
–2.014	1.4844	1.4826	–0.12%	0.01%	1.8121	1.8109	–0.07%	0.00%
–0.992	1.5664	1.5628	–0.23%	0.01%	1.7299	1.7287	–0.07%	0.00%
0.001	1.6460	1.6405	–0.33%	0.00%	1.6501	1.6484	–0.10%	–0.04%
0.993	1.7259	1.7187	–0.42%	0.01%	1.5700	1.5689	–0.07%	–0.01%
2.015	1.8079	1.7988	–0.50%	0.00%	1.4878	1.4868	–0.07%	–0.01%
2.984	1.8858	1.8749	–0.58%	0.00%	1.4097	1.4089	–0.06%	0.00%
4.005	1.9677	1.9551	–0.64%	0.01%	1.3276	1.3269	–0.06%	0.00%
4.994	2.0469	2.0325	–0.70%	0.01%	1.2483	1.2475	–0.06%	–0.01%

6.1.2 High-Side Measurement Error Across Different DC Link Voltages

Figure 18 shows the variation of high-side current measurement error with DC bus voltage and Table 4 shows the tabulated test results. The user can observe that there is little variation in the high-side error with variation in the DC bus voltage. This lack of variation is because the low-side, buck converter power supply for the INA170 device always maintains the floating reference 30 V below the DC bus. So although the DC bus voltage changes, the common-mode input observed by the INA170 inputs is constant.

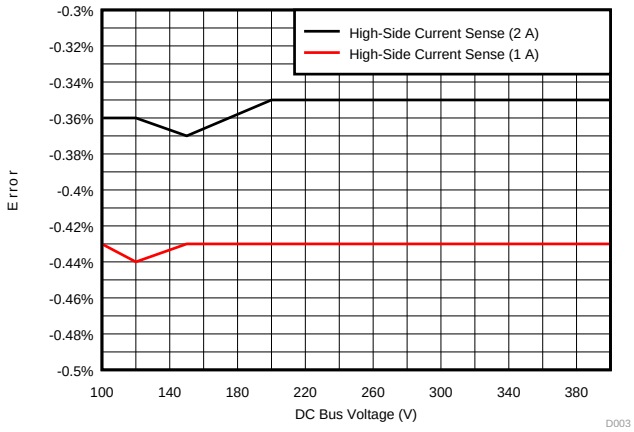


Figure 18. High-Side Current Measurement Error Versus DC Bus Voltage (Non-Calibrated)

Table 4. High-Side Current Sense Voltage and Error Versus DC Bus Voltage (V)

DC BUS VOLTAGE (V)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 1 A (V)	HIGH-SIDE CURRENT SENSE ERROR AT 1 A	HIGH-SIDE CURRENT SENSE VOLTAGE AT 2 A (V)	HIGH-SIDE CURRENT SENSE ERROR AT 2 A
100	1.7191	–0.36%	1.7993	–0.43%
120	1.7191	–0.36%	1.7993	–0.44%
150	1.719	–0.37%	1.7994	–0.43%
200	1.7192	–0.35%	1.7994	–0.43%
250	1.7193	–0.35%	1.7994	–0.43%
275	1.7193	–0.35%	1.7994	–0.43%
300	1.7193	–0.35%	1.7994	–0.43%
350	1.7194	–0.35%	1.7995	–0.43%
400	1.7194	–0.35%	1.7995	–0.43%

6.1.3 Measurement Error Versus Temperature

This test shows the variation of the signal-conditioning circuit output overtemperature. During this measurement, the board remains inside a temperature chamber and is tested at −10°C, 25°C, and 55°C. Figure 19 shows the variation of the high-side measurement error and Table 5 shows the corresponding results. Figure 20 shows the variation of the low-side measurement error and Table 6 shows the corresponding results.

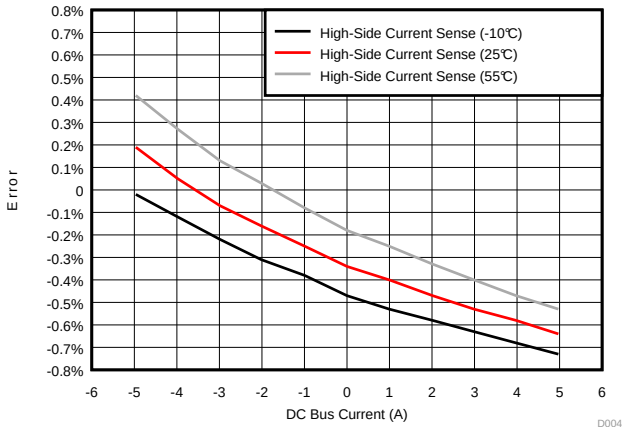


Figure 19. Graph of High-Side Current Measurement Error at −10°C, 25°C, and 55°C (Non-Calibrated)

Table 5. High-Side Current Sense Voltage and measurement error Versus DC Bus Current at −10°C, 25°C, and 55°C

−10°C			25°C			55°C		
DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT −10°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT −10°C	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 25°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT 25°C	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 55°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT 55°C
–4.965	1.2487	–0.02%	–4.994	1.249	0.19%	–5.027	1.2492	0.42%
–3.9783	1.3262	–0.12%	–4.004	1.3264	0.05%	–4.0359	1.3268	0.27%
–2.9866	1.404	–0.22%	–2.983	1.4065	–0.07%	–2.9861	1.4091	0.13%
–2.0163	1.4802	–0.31%	–2.014	1.4826	–0.16%	–2.0148	1.4853	0.03%
–0.9948	1.5605	–0.38%	–0.992	1.5628	–0.25%	–0.993	1.5654	–0.08%
0.0016	1.6385	–0.47%	0.001	1.6405	–0.34%	0.0016	1.6433	–0.18%
0.9936	1.7165	–0.53%	0.993	1.7187	–0.40%	0.9895	1.7209	–0.25%
2.0152	1.7968	–0.58%	2.015	1.7988	–0.47%	1.9744	1.7981	–0.33%
2.987	1.8732	–0.63%	2.984	1.8749	–0.53%	2.9937	1.878	–0.40%
3.9785	1.951	–0.68%	4.005	1.9551	–0.58%	4.025	1.9589	–0.47%
4.971	2.0288	–0.73%	4.994	2.0325	–0.64%	4.8943	2.0269	–0.53%

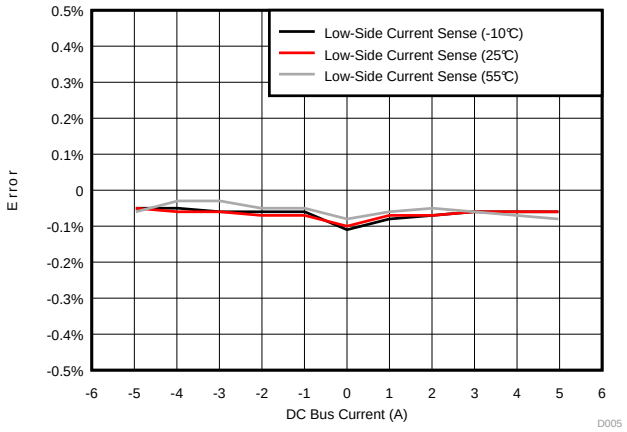


Figure 20. Graph of Low-Side Measurement Error at −10°C, 25°C, and 55°C (Non-Calibrated)

Table 6. Low-Side Current Sense Voltage and Measurement Error Versus DC Bus Current at −10°C, 25°C, and 55°C

–10°C			25°C			55°C		
DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT −10°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT −10°C	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 25°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT 25°C	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 55°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT 55°C
–4.965	2.0482	–0.05%	–4.994	2.0506	–0.05%	–5.027	2.0529	–0.06%
–3.9783	1.9688	–0.05%	–4.004	1.9711	–0.06%	–4.0359	1.974	–0.03%
–2.9866	1.8891	–0.06%	–2.983	1.889	–0.06%	–2.9861	1.8895	–0.03%
–2.0163	1.811	–0.06%	–2.014	1.8109	–0.07%	–2.0148	1.8113	–0.05%
–0.9948	1.7288	–0.06%	–0.992	1.7287	–0.07%	–0.993	1.7291	–0.05%
0.0016	1.6482	–0.11%	0.001	1.6484	–0.10%	0.0016	1.6486	–0.08%
0.9936	1.5689	–0.08%	0.993	1.5689	–0.07%	0.9895	1.5695	–0.06%
2.0152	1.4869	–0.07%	2.015	1.4868	–0.07%	1.9744	1.4903	–0.05%
2.987	1.4089	–0.06%	2.984	1.4089	–0.06%	2.9937	1.4084	–0.06%
3.9785	1.3293	–0.06%	4.005	1.3269	–0.06%	4.025	1.3252	–0.07%
4.971	1.2497	–0.06%	4.994	1.2475	–0.06%	4.8943	1.2554	–0.08%

6.1.4 Detection of GND Fault Scenario and Response Time

This section shows the detection of the GND fault scenario. Figure 21 shows the setup for simulating the GND fault. A constant electrical load is connected on the output of the TIDA-00442 board. One side of a variable electronic load is connected to the constant load and the other side is connected to DC− so that it bypasses the TIDA-00442 board. The variable electronic load is used to simulate the earth leakage fault current. The constant load is set to 86 mA in the test setup. The variable electronic load is a square wave of 100 Hz and has a 350-mA peak.

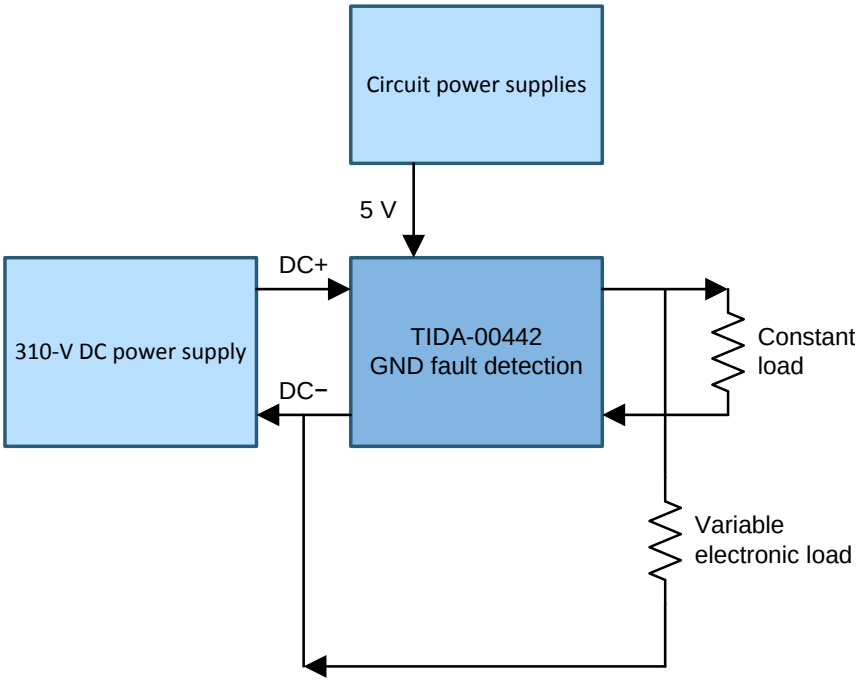


Figure 21. Setup for Creation of GND Fault Scenario

In Figure 22 the waveform in green is the earth leakage current, which is a square wave varying from 100 mA to 350 mA. This pulsed waveform is generated from the variable electronic load. The yellow waveform is the output of the GND fault detect comparator. The pink waveform is the average of the high-side and low-side current sense outputs and the blue waveform is the upper leakage detection threshold with hysteresis. The user can observe that, as the earth leakage current crosses 300 mA, the pink waveform crosses the upper threshold and the GND fault comparator output is pulled low.

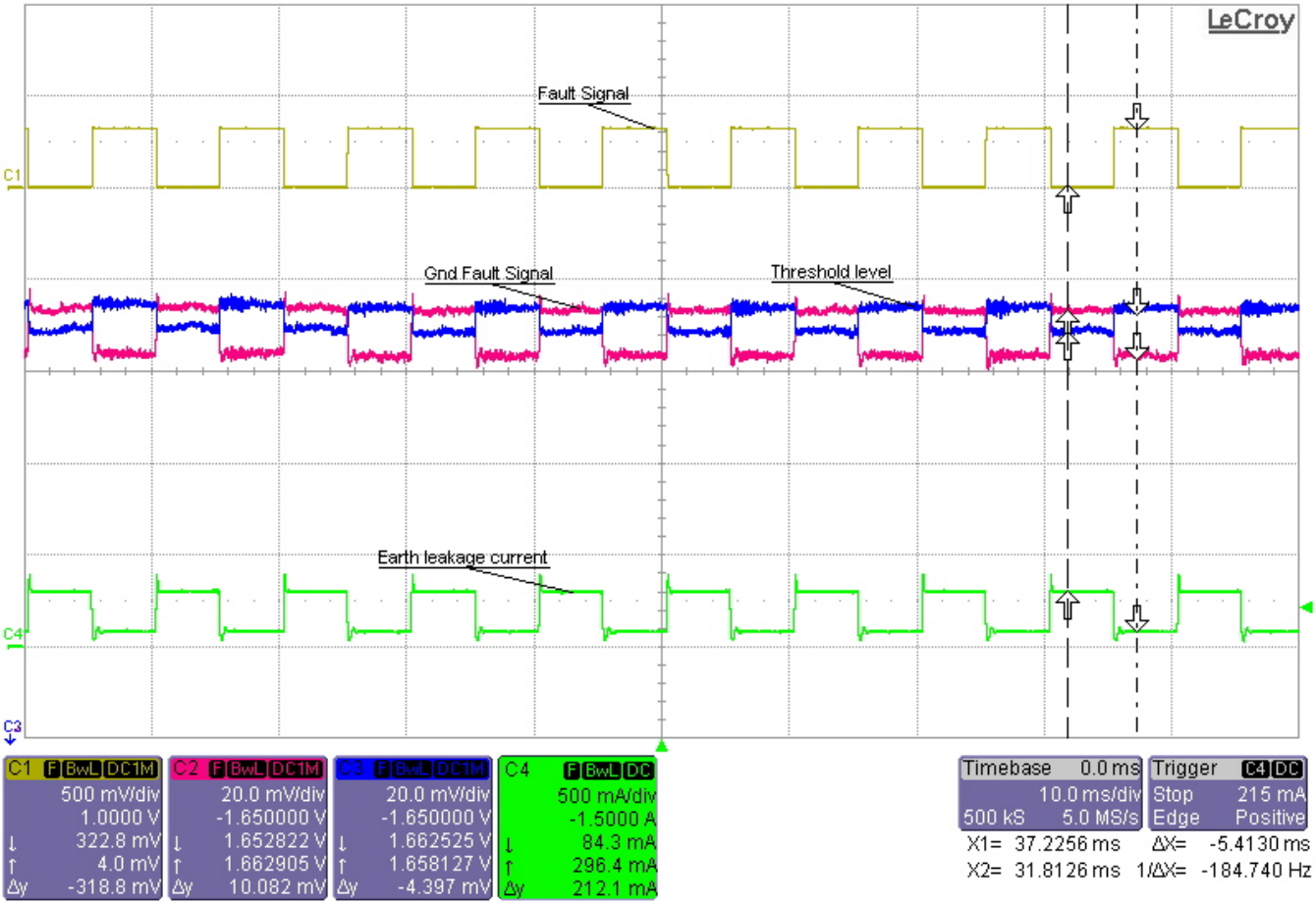


Figure 22. Detection of GND Fault

Figure 23 shows the response time to the GND fault. A zoomed-in version is also available so the user can read the response time. The response time in this scenario shows to be 32 µs.

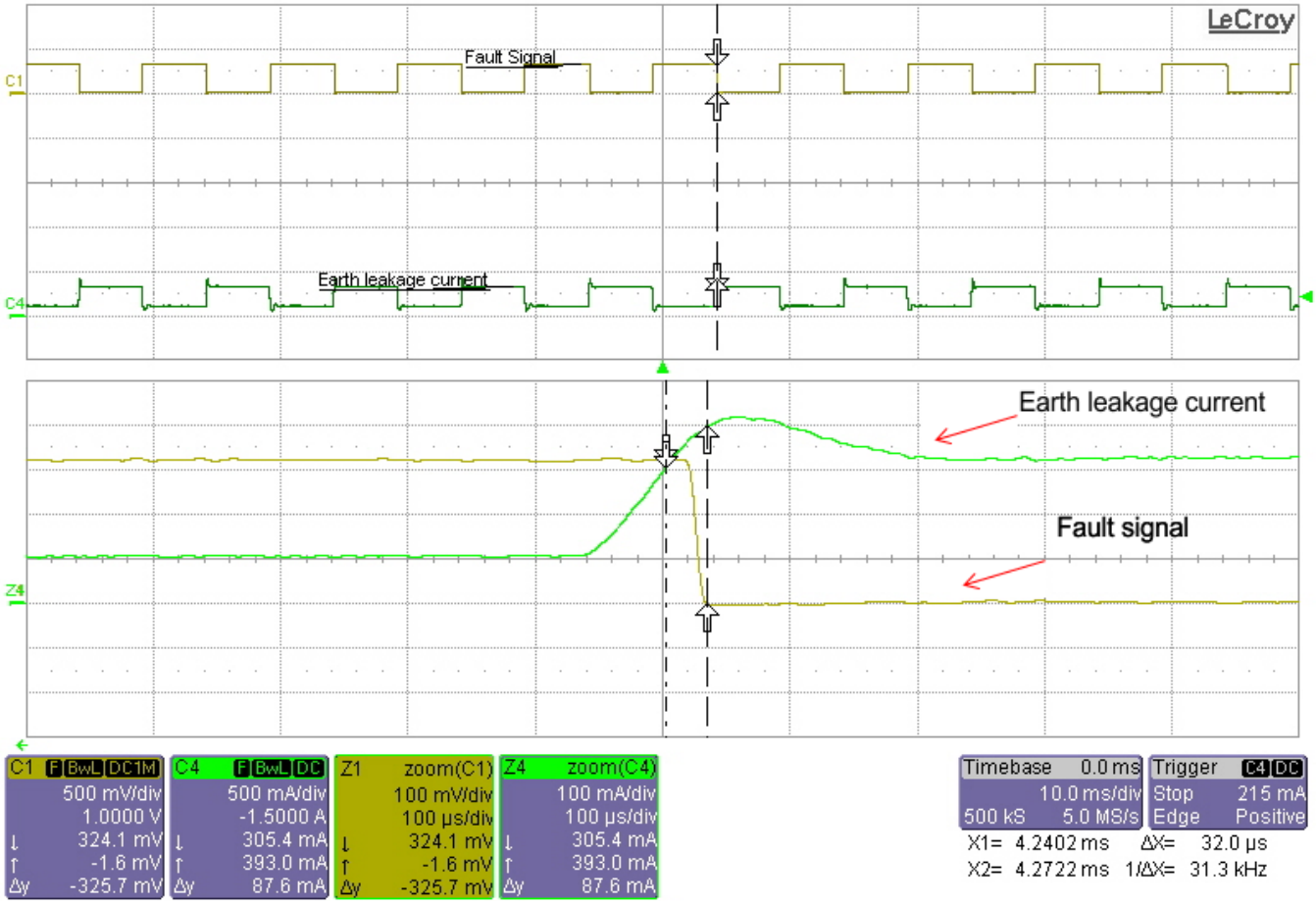


Figure 23. Response Time to GND Fault

6.1.5 Testing With C2000™ MCU-Based High-Voltage Motor Control Kit From TI to Detect GND Fault

This test uses the TIDA-00442 board to detect the GND fault on an actual motor drive. The C2000 application kit for high-voltage motor control applications is used as the motor driver. A three-phase AC induction motor is connected to the drive. Figure 24 shows a block diagram of the setup.

Figure 25 and Figure 26 show the actual setup images. The DC power supply is connected to the drive through the TIDA-00442 board. Figure 27 shows the graphical user interface (GUI), which is used to control the motor. Connect the PC to the motor control kit through a USB, power on the DC supply to the drive, select the motor type (either permanent magnet synchronous motor (PMSM) or AC induction motor (ACIM)), and enable the motor if none of the faults are flagged in the GUI software. Detailed information about the high-voltage motor control application kit and the GUI are available by downloading the TI controlSUITE™ software

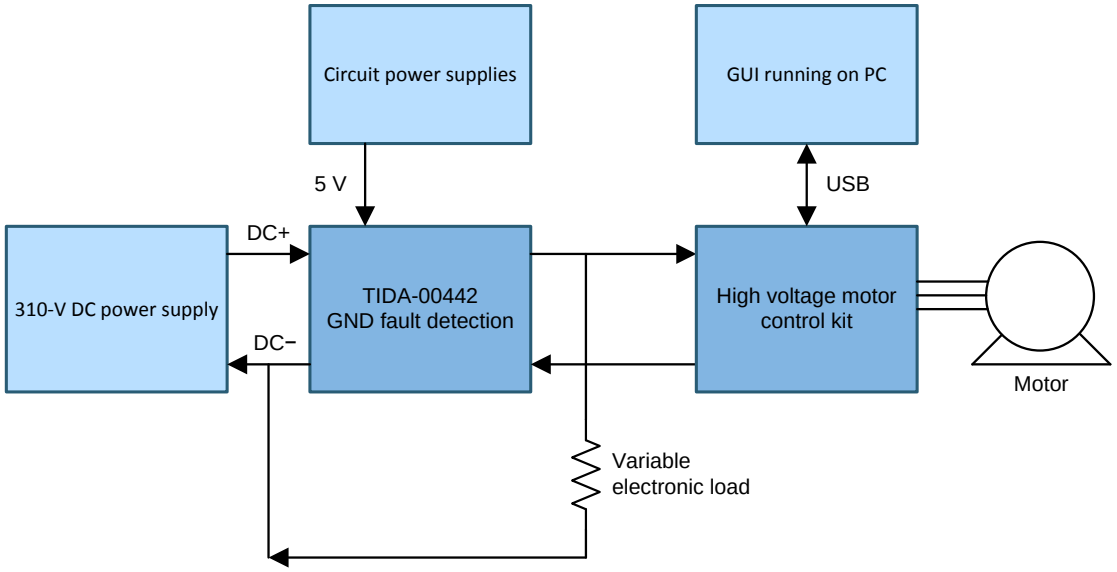


Figure 24. Block Diagram of C2000 High-Voltage Motor Drive Setup

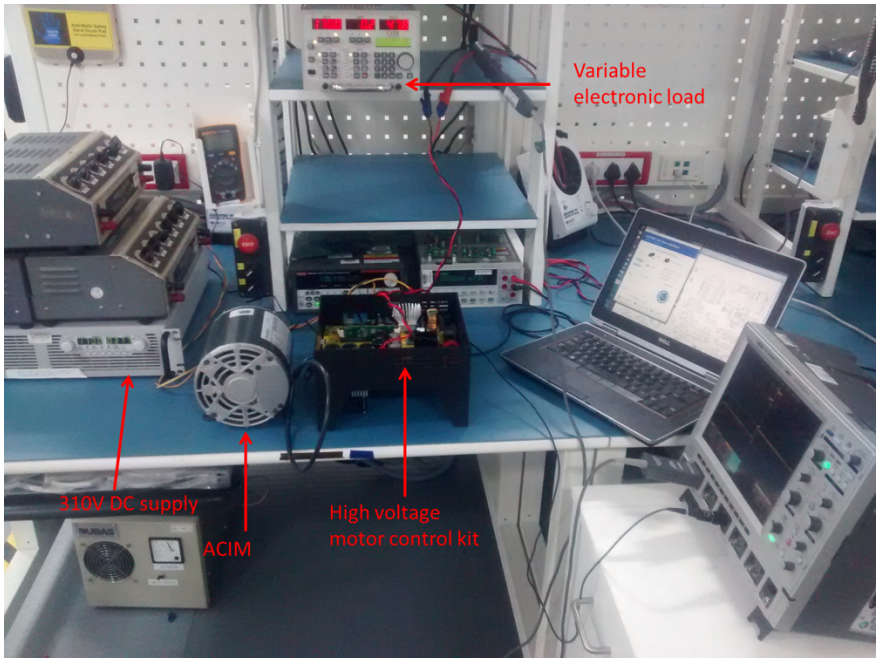


Figure 25. C2000 High-Voltage Motor Drive Setup

Figure 26. TIDA-00442 C2000™ MCU-Based High-Voltage Motor Control Kit From TI

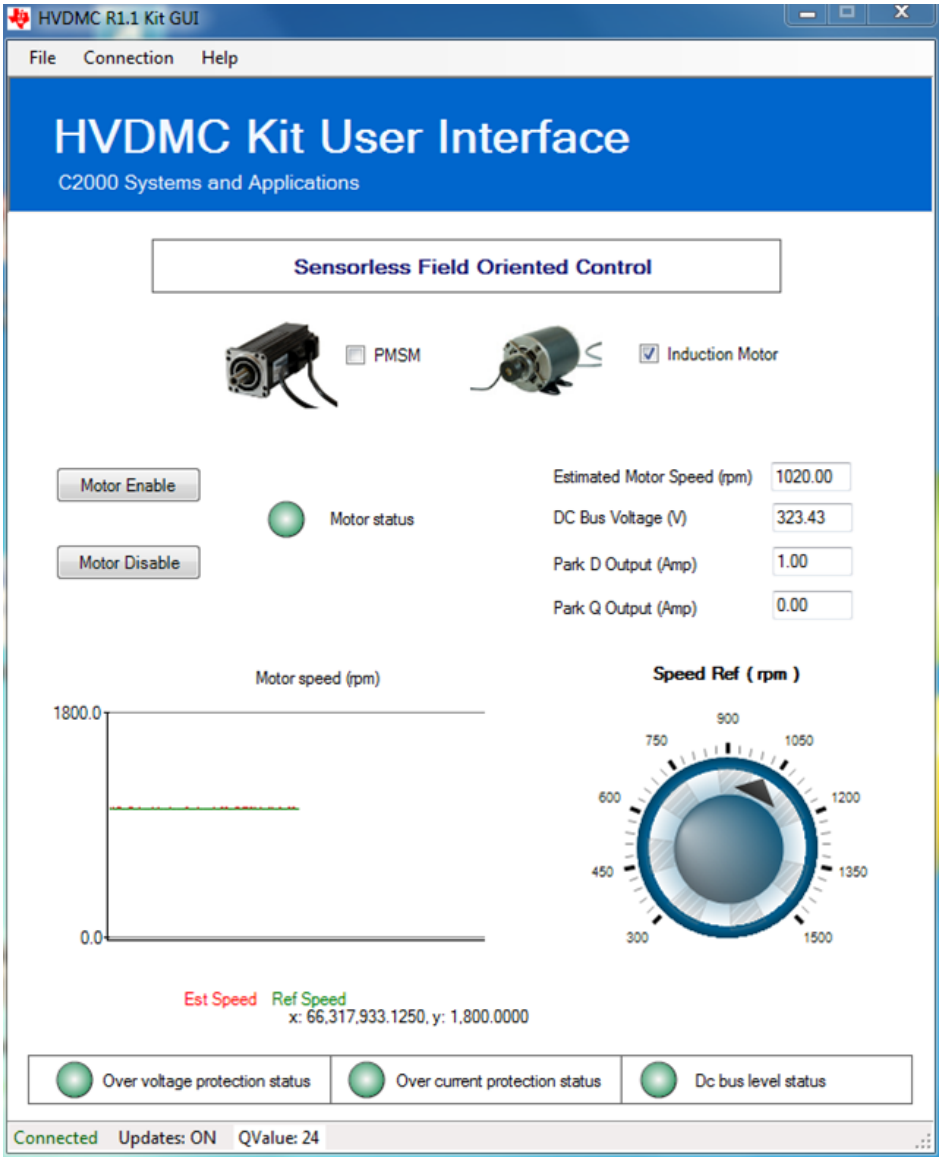


Figure 27. GUI to Control AC Motor

Figure 28 shows the test result. The yellow waveform is the earth leakage current with a frequency of 100 Hz and it varies from a 100- to 350-mA peak. The response time is 23.8 µs. The motor runs at 1000 rpm from a DC bus voltage of 310 V.

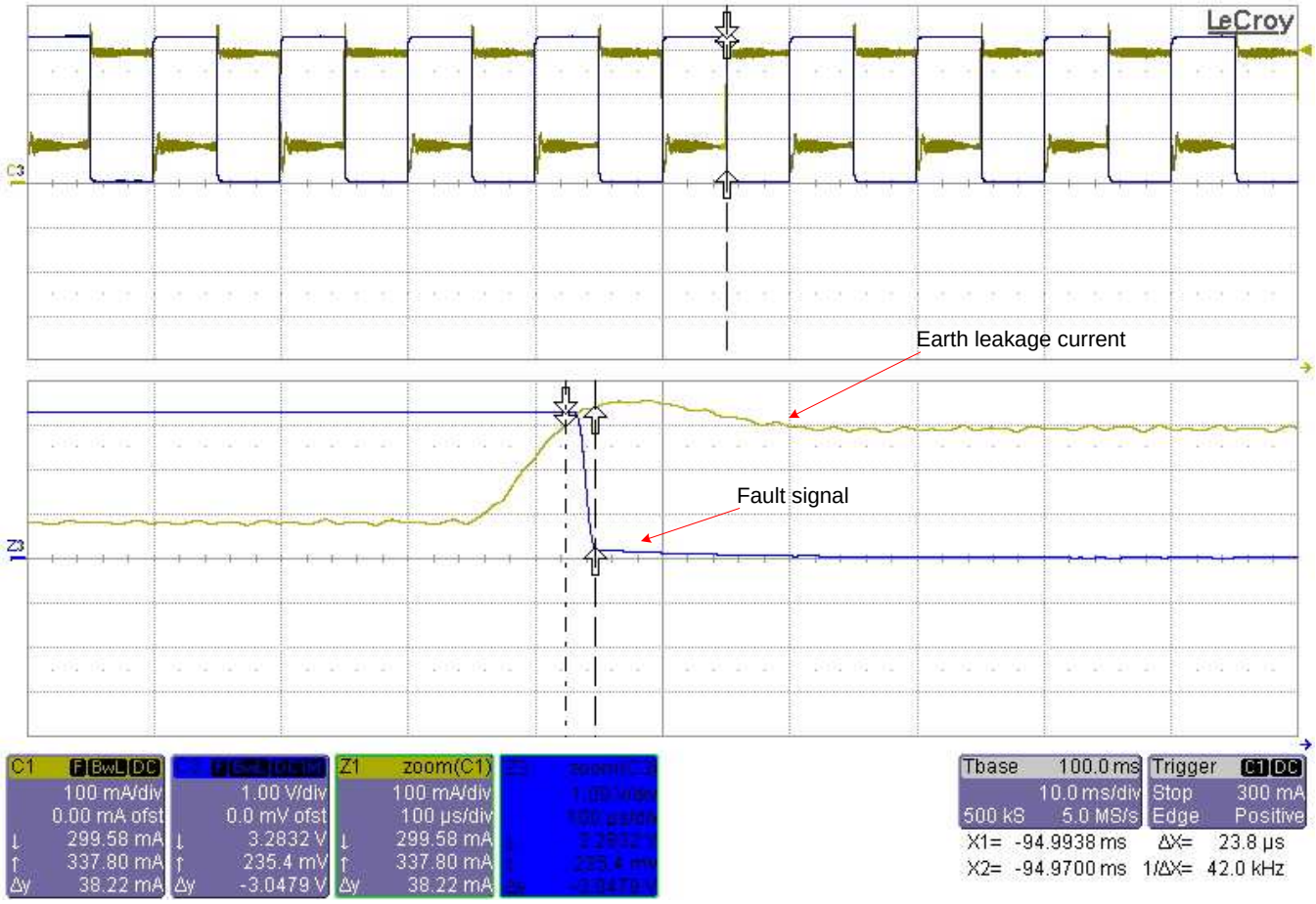


Figure 28. GND Fault Response Time

6.2 Test Results for 170-V DC Bus Voltage (110-V AC Mains-Powered Drives)

6.2.1 High-Side and Low-Side Current Measurement Error

Figure 29 shows the test setup for measuring the error of the high-side and low-side current measurement circuit. A variable load is connected to a high-voltage DC power supply through the TIDA-00442 board. An external DC power supply provides 5 V to power up the board. The high voltage DC power supply, which simulates the DC bus voltage in the actual drive, is set to 170-V DC. The load is varied from −5 A to 5 A with the help of the variable electronic load and the high-side and low-side current measurement outputs are recorded.

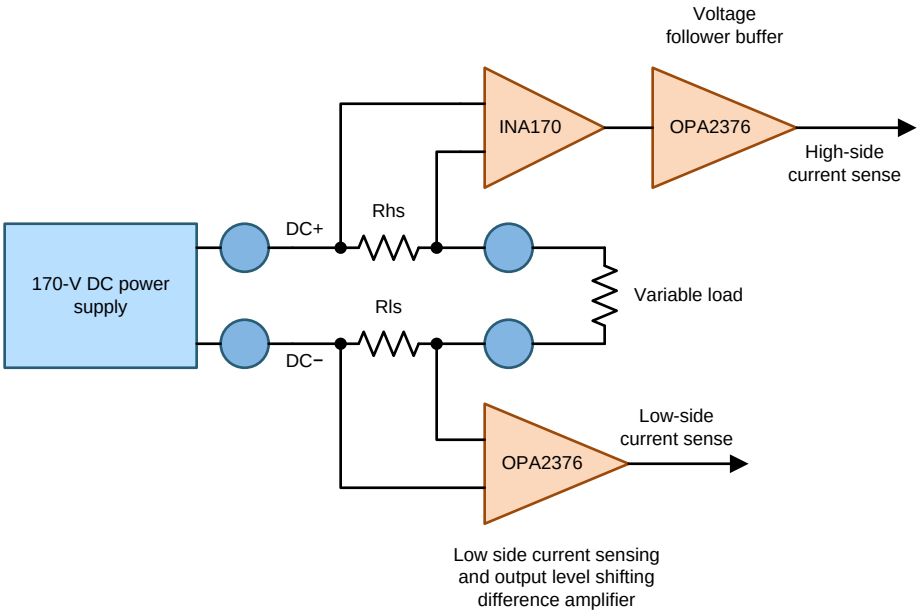


Figure 29. Test Setup for TIDA-00442 High-Side and Low-Side Current Measurement Error

Figure 30 shows a graph of the variation of current measurement error versus the DC bus current and Figure 31 shows the calibrated result. Table 7 shows the corresponding readings.

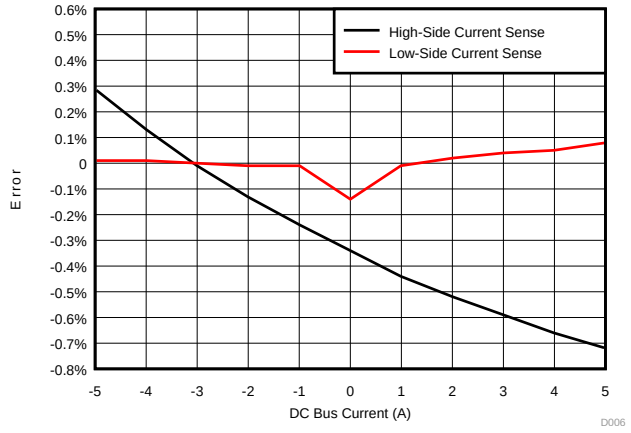


Figure 30. Current Sense error Versus DC Bus Current (Non-Calibrated)

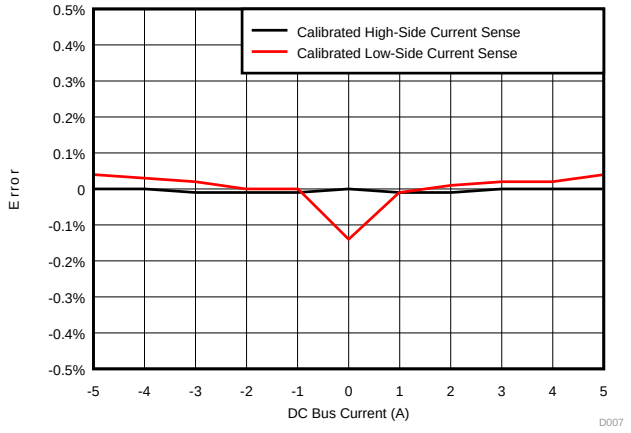


Figure 31. Current Sense Error Versus DC Bus Current (Calibrated)

Table 7. Current Sense Output and Measurement error Versus DC Bus Current

DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE (V)	CALIBRATED HIGH-SIDE CURRENT SENSE VOLTAGE (V)	HIGH-SIDE CURRENT SENSE ERROR (%)	CALIBRATED HIGH-SIDE CURRENT SENSE ERROR (%)	LOW-SIDE CURRENT SENSE VOLTAGE (V)	CALIBRATED LOW-SIDE CURRENT SENSE VOLTAGE (V)	LOW-SIDE CURRENT SENSE ERROR (%)	CALIBRATED LOW-SIDE CURRENT SENSE ERROR (%)
–5.01	1.2438	1.2475	0.29%	0.00%	2.0532	2.0535	0.01%	0.04%
–3.991	1.3256	1.3274	0.13%	0.00%	1.9712	1.9714	0.01%	0.03%
–3.003	1.4050	1.4049	–0.01%	–0.01%	1.8917	1.8917	0.00%	0.02%
–2.012	1.4845	1.4826	–0.13%	–0.01%	1.8119	1.8118	–0.01%	0.00%
–0.991	1.5666	1.5628	–0.24%	–0.01%	1.7297	1.7295	–0.01%	0.00%
0.001	1.6460	1.6405	–0.34%	0.00%	1.6500	1.6477	–0.14%	–0.14%
0.99	1.7257	1.7182	–0.44%	–0.01%	1.5702	1.5701	–0.01%	–0.01%
2.012	1.8079	1.7985	–0.52%	–0.01%	1.4878	1.4881	0.02%	0.01%
3.003	1.8875	1.8763	–0.59%	0.00%	1.4081	1.4086	0.04%	0.02%
3.991	1.9669	1.9539	–0.66%	0.00%	1.3285	1.3292	0.05%	0.02%
5.011	2.0487	2.0339	–0.72%	0.00%	1.2464	1.2474	0.08%	0.04%

6.2.2 Measurement Error Versus Temperature

This test identifies the variation of the signal-conditioning circuit measurement error overtemperature. The board remains inside a temperature chamber and is tested at −10°C, 25°C, and 55°C. Figure 32 shows the variation of the high-side measurement error and Table 8 shows the corresponding results.

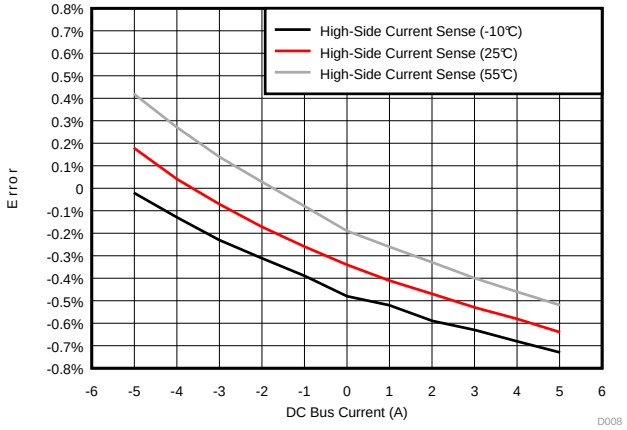


Figure 32. Graph of High-Side Current Measurement Error at −10°C, 25°C, and 55°C (Non-Calibrated)

Table 8. High-Side Current Sense Voltage and Measurement Error Versus DC Bus Current at −10°C, 25°C, and 55°C

−10°C			25°C			55°C		
DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT −10°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT −10°C (%)	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 25°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT 25°C (%)	DC BUS CURRENT (A)	HIGH-SIDE CURRENT SENSE VOLTAGE AT 55°C (V)	HIGH-SIDE CURRENT SENSE ERROR AT 55°C (%)
–5.0122	1.2449	–0.02%	–5.01	1.2475	0.18%	–5.0124	1.2503	0.42%
–3.993	1.3249	–0.13%	–3.991	1.3274	0.04%	–3.9932	1.3302	0.27%
–3.0045	1.4025	–0.23%	–3.003	1.4049	–0.07%	–3.0045	1.4077	0.14%
–2.014	1.4803	–0.31%	–2.012	1.4826	–0.17%	–2.0139	1.4854	0.03%
–0.992	1.5606	–0.39%	–0.991	1.5628	–0.26%	–0.9918	1.5655	–0.08%
0.0009	1.6383	–0.48%	0.00100	164.05%	–0.34%	0.0009	1.6431	–0.19%
0.9916	1.7164	–0.52%	0.99000	171.82%	–0.41%	0.9915	1.721	–0.26%
2.0137	1.7966	–0.59%	2.01200	179.85%	–0.47%	2.014	1.8012	–0.33%
3.0044	1.8745	–0.63%	3.00300	187.63%	–0.53%	3.0042	1.8789	–0.40%
3.9927	1.9521	–0.68%	3.99100	195.39%	–0.58%	3.9922	1.9564	–0.46%
5.0121	2.0321	–0.73%	5.01100	203.39%	–0.64%	5.011	2.0363	–0.52%

Figure 33 shows the variation of the low-side measurement error and Table 9 shows the corresponding results.

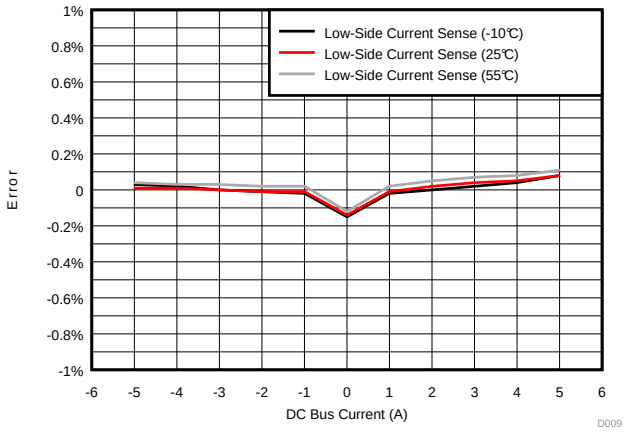


Figure 33. Graph of Low-Side Measurement Error Versus DC Bus Current at −10°C, 25°C, and 55°C (Non-Calibrated)

Table 9. Low-Side Current Sense Voltage and Measurement Error Versus DC Bus Current at −10°C, 25°C, and 55°C

−10°C			25°C			55°C		
DC BUS CURRENT (A)	LOW-SIDE CURRENT SENSE VOLTAGE AT −10°C (V)	LOW-SIDE CURRENT SENSE ERROR AT −10°C	DC BUS CURRENT (A)	LOW-SIDE CURRENT SENSE VOLTAGE AT 25°C (V)	LOW-SIDE CURRENT SENSE ERROR AT 25°C	DC BUS CURRENT (A)	LOW-SIDE CURRENT SENSE VOLTAGE AT 55°C (V)	LOW-SIDE CURRENT SENSE ERROR AT 55°C
–5.0122	2.0534	0.03%	–5.01	2.0535	0.01%	–5.0124	2.0542	0.04%
–3.993	1.9713	0.02%	–3.991	1.9714	0.01%	–3.9932	1.972	0.03%
–3.0045	1.8916	0.00%	–3.003	1.8917	0.00%	–3.0045	1.8923	0.03%
–2.014	1.8118	–0.01%	–2.012	1.8118	–0.01%	–2.0139	1.8125	0.02%
–0.992	1.7294	–0.02%	–0.991	1.7295	–0.01%	–0.9918	1.7301	0.02%
0.0009	1.6476	–0.15%	0.00100	1.6477	–0.14%	0.0009	1.6482	–0.12%
0.9916	1.57	–0.02%	0.99000	1.5701	–0.01%	0.9915	1.5706	0.02%
2.0137	1.4881	0.00%	2.01200	1.4881	0.02%	2.014	1.4885	0.05%
3.0044	1.4088	0.02%	3.00300	1.4086	0.04%	3.0042	1.4091	0.07%
3.9927	1.3296	0.04%	3.99100	1.3292	0.05%	3.9922	1.3298	0.08%
5.0121	1.248	0.08%	5.01100	1.2474	0.08%	5.011	1.2481	0.11%

6.2.3 Detection of GND Fault Scenario and Response Time

This section shows the detection of the GND fault scenario. Figure 34 shows the setup for simulating the GND fault. A constant electrical load is connected on the output of the TIDA-00442 board. One side of a variable electronic load is connected to the constant load and the other side is connected to the DC− so that it bypasses the TIDA-00442 board. The variable electronic load is used to simulate the earth leakage fault current. The constant load is set to 86 mA in this test setup. The variable electronic load is a square wave of 100 Hz and has a 350 mA peak.

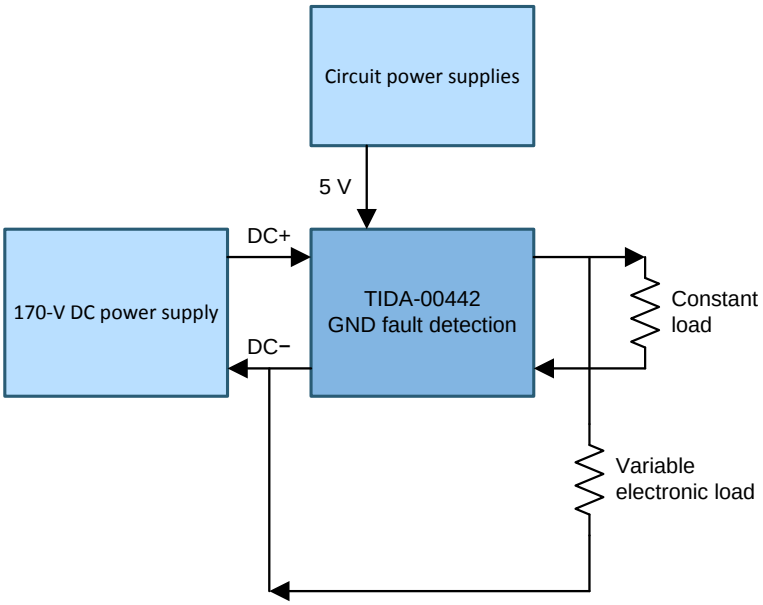


Figure 34. Setup for Creation of GND Fault Scenario

The green waveform in Figure 35 is the earth leakage current, which is a square wave that varies from 100 mA to 350 mA. This pulsed waveform is generated from the variable electronic load. The yellow waveform is the output of the GND fault detect comparator. The pink waveform is the average of the high-side and low-side current sense outputs and the blue waveform is the upper leakage detection threshold with hysteresis. The user can observe that, as the earth leakage current crosses 300 mA, the pink waveform crosses the upper threshold and the GND fault comparator output is pulled low.

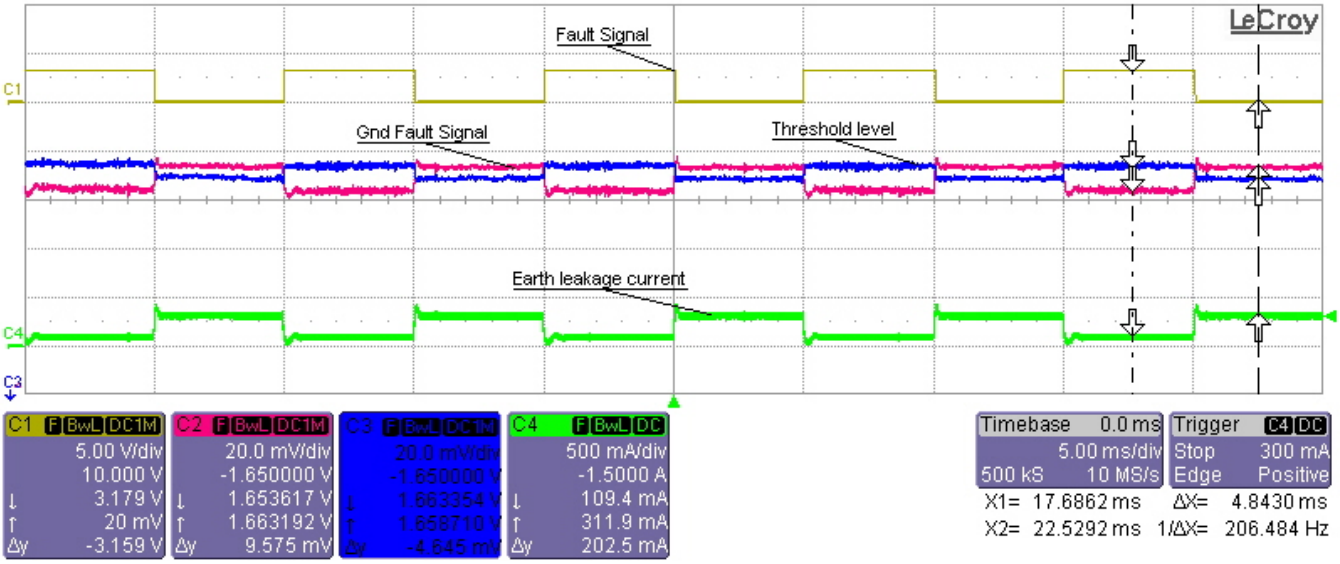


Figure 35. Detection of GND Fault

Figure 36 shows the response time to the GND fault. The yellow waveform is the output of the GND fault detect comparator. When the output is pulled down low, the yellow waveform indicates a GND fault. The green waveform is the earth leakage current, which has a frequency of 100 Hz and varies from 100 mA to 350 mA. A zoomed-in version is also available so the user can read the response time. The response time in this scenario shows to be 29.2 µs.

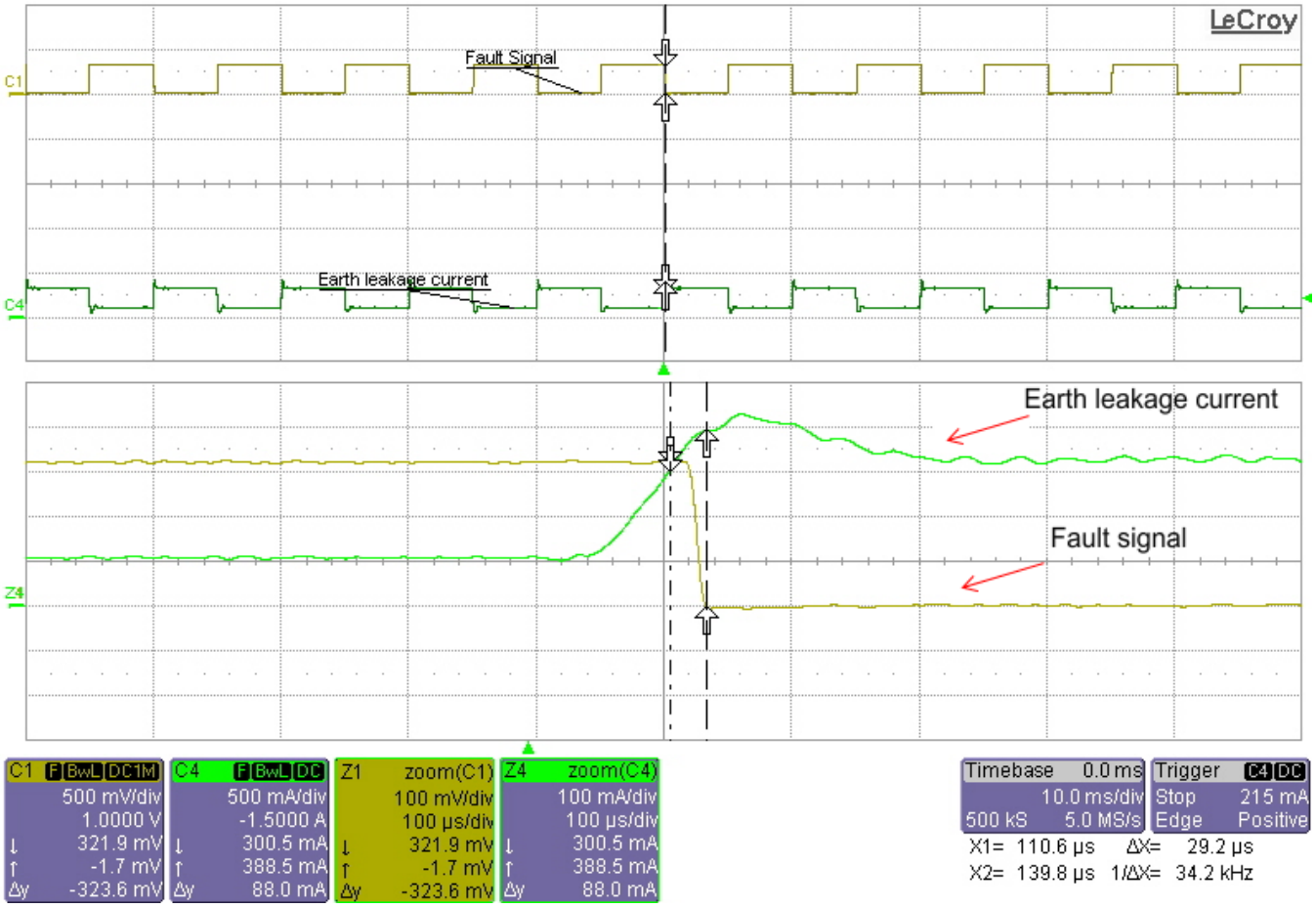


Figure 36. GND Fault Response Time

6.2.4 Testing With C2000™ MCU-Based High-Voltage Motor Control Kit From TI to Detect GND Fault

This test uses the TIDA-00442 board to detect the GND fault on an actual motor drive. The setup is similar to in the setup that Section 6.1.5 shows.

Figure 36 and Figure 38 show the test result. The yellow waveform is the earth leakage current with a frequency of 100 Hz and it varies from a 100-mA to 350-mA peak. The response time is 24.6 µs. The motor runs at 1000 rpm from a DC bus voltage of 170 V.

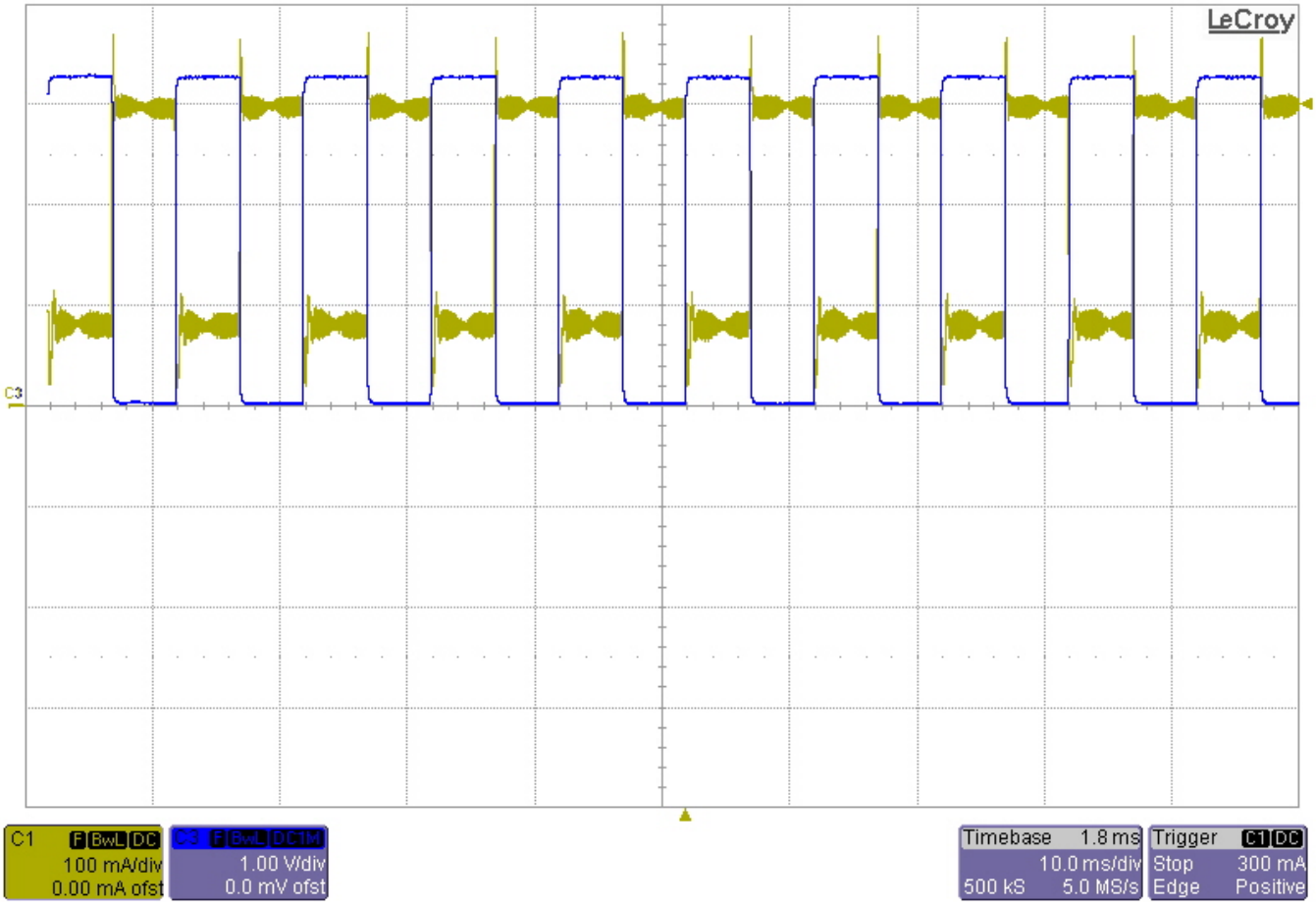


Figure 37. GND Fault Signal

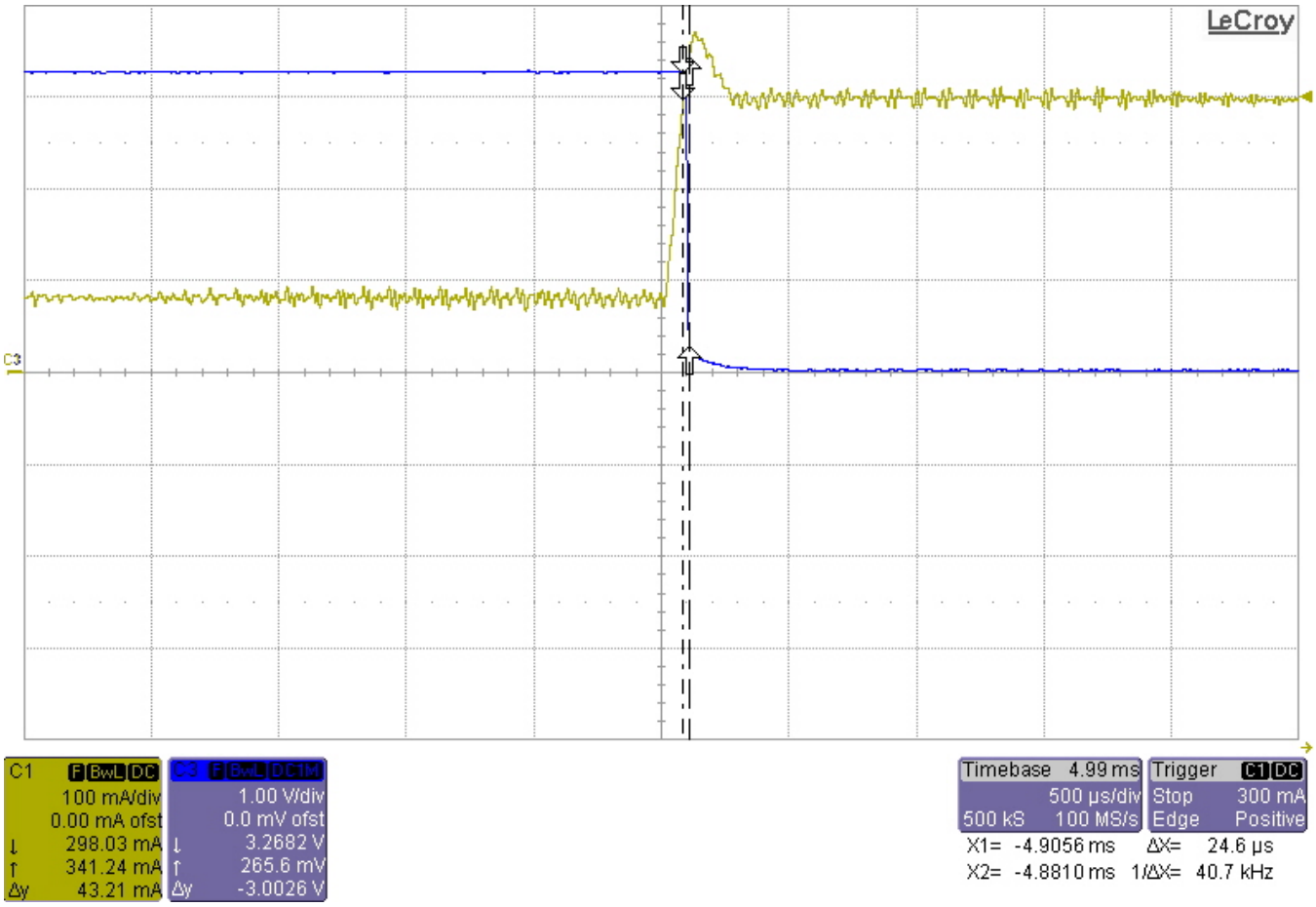


Figure 38. Zoomed-In GND Fault Signal Showing GND Fault Response Time

7 Design Files

7.1 Schematics

To download the schematics for each board, see the design files at TIDA-00442.

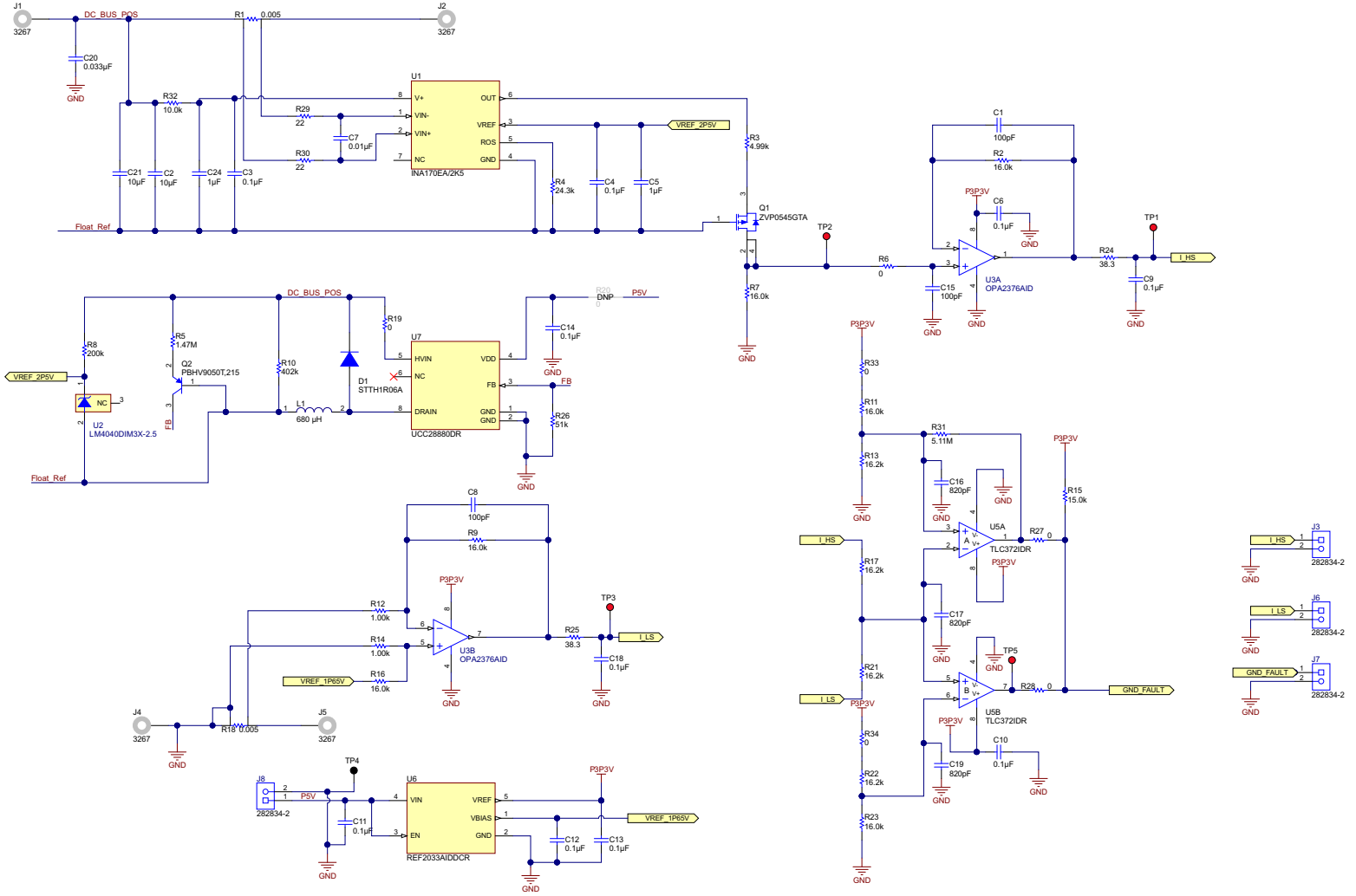


Figure 39. Current Sense and Signal Conditioning Schematic

7.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00442.

7.3 PCB Layout Recommendations

PCB placement and layout is very important to get the specified performance as mentioned in the datasheet. This board contains high voltage nets. Special care must be taken to provide sufficient spacing between high voltage nets and low voltage nets.

7.3.1 Layout Recommendations for High-Side Current Measurement Signal Chain

Figure 40 shows the layout for the INA170 current shunt monitor IC, which has the following layout recommendations:

- Use Kelvin connections for current sense resistor. The input differential filter between the shunt resistor and the INA170 sense inputs consists of R30, R29, and C7. The routing from the shunt resistor to the INA170 inputs through the differential filter should be symmetrical and as short as possible, place the differential filter capacitor C7 very close to the Vin+ and Vin– pins of INA170.
- The decoupling capacitor should be placed close to the power pin of INA170. The floating DC-DC converter power supply section can be placed farther away from the INA170 circuitry and the power then routed to INA170 through power planes.

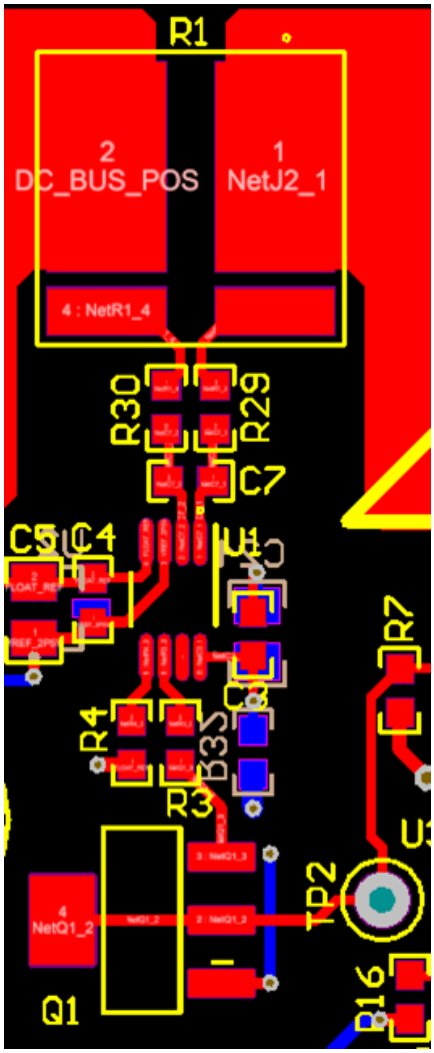


Figure 40. Layout Recommendations for INA170 Current Sense Circuit

- For the succeeding voltage-follower buffer stage keep the input nodes short to avoid noise getting coupled into the amplifier input. As Figure 41 shows, the trace length from R6 and C15 to pin 3 should be short, the trace length from R2 and C1 to pin 2 should also be short.

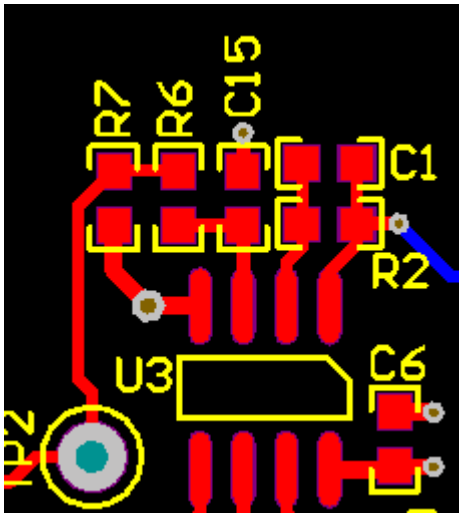


Figure 41. Layout Recommendations for OPA2376 Voltage Follower Buffer

7.3.2 Layout Recommendations for UCC28880-Based Low-Side Buck Converter

PCB placement and routing is very important for DC-DC switching converters for proper operation of the circuit and for minimum EMI/EMC. Special care is taken to minimize the switching loops and to control the flow of switching currents.

- The copper area of the switching node drain (pin 8 of U7) should be minimized to reduce EMI.
- There are two switching loops in the design. These loops should be minimized to a maximum extent possible to reduce EMI. The two switching loops are shown in Figure 42 and Figure 43. The first loop is when the inbuilt low side switch is ON. During this instant the current flows from the input bulk capacitor C20 through the output bulk capacitor C2, then into the inductor L1, into the drain (pin 8) of the UCC28880 IC through the inbuilt low-side switch, out of the GND pin of the IC (pin 1 and pin 2) and back into the input bulk capacitor C20. This loop has to be made as small as possible as Figure 42 shows.

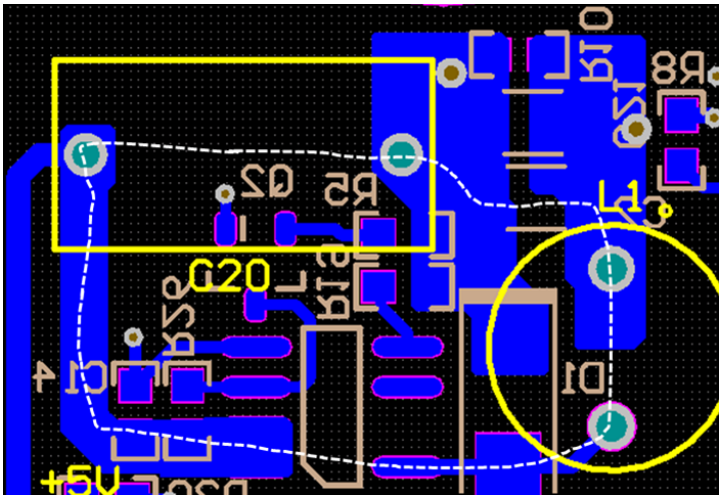


Figure 42. Switching Loop for UCC28880 Device When Low-Side Switch is ON

- Figure 43 shows the second switching loop. This switching loop happens when the inbuilt low side switch is OFF. Current flows through the output bulk capacitor C2, through the inductor L1 and back into the capacitor C2 through freewheeling diode D1. This loop has been minimized as much as possible in the layout.

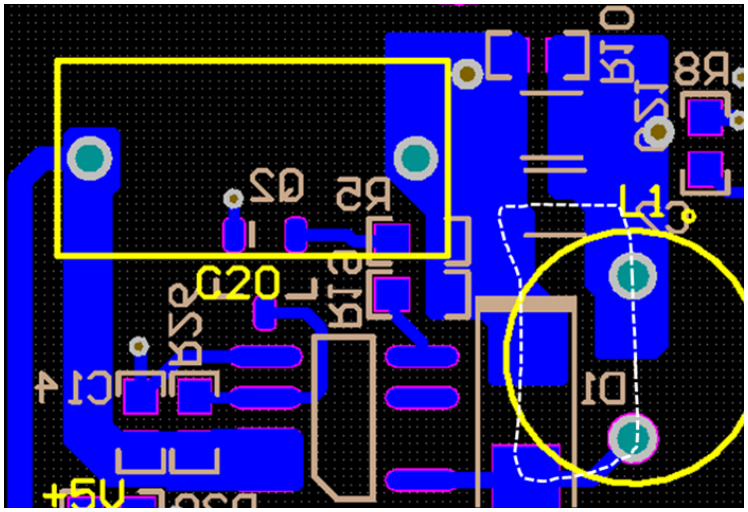


Figure 43. Switching Loop for UCC28880 Device When Low-Side Switch is OFF

- The floating output supply must be taken out from the output bulk capacitor C2 terminals.
- The feedback section consists of R26, Q2m and R5. The resistor R26 must be kept close to feedback pin of the IC.
- The decoupling capacitor C14 should be kept close to the power pin of the IC
- A star connection has to be done from the DC-DC converter GND to the main GND of the PCB as Figure 44 shows. This is done to ensure that none of the switching current passes through the main GND of the PCB thus avoiding GND noise issues.

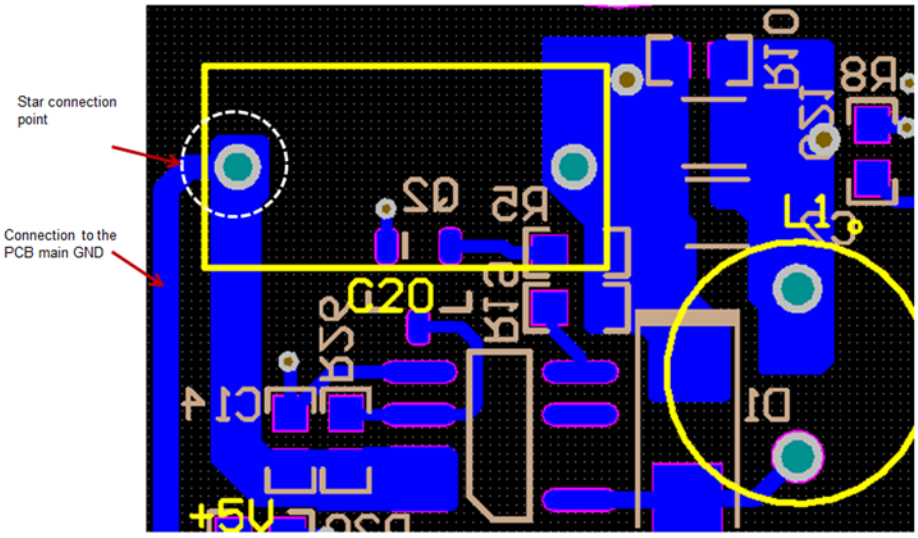


Figure 44. Star Connection to PCB Main GND

7.3.3 Layout Recommendations for Low-Side Current Monitor

Figure 45 shows the layout for the low-side current sense circuit. Be sure to utilize the following steps for this layout:

- Use Kelvin connections from the low-side current shunt resistor. Place the difference amplifier close to the shunt resistor and join it with short balanced traces to avoid offset voltages created due to input bias current of the op-amp and the trace parasitics.
- Keep all traces at the inverting and non-inverting nodes of the op-amp to be very short. Any noise coupled into these pins will be amplified and appear on the output.
- Place the power supply noise decoupling capacitor C6 very close to the power supply pin of the IC. The function of this capacitor is to decouple the noise from the rest of the circuit from entering the IC. Therefore during layout care should be taken that the power supply first enters the capacitor and then into the IC power pin, if this is not done the decoupling capacitor does not decouple the noise effectively. Also trace length from the decoupling capacitor to the IC power pin should be kept very short to minimize the trace stray parasitic inductance.

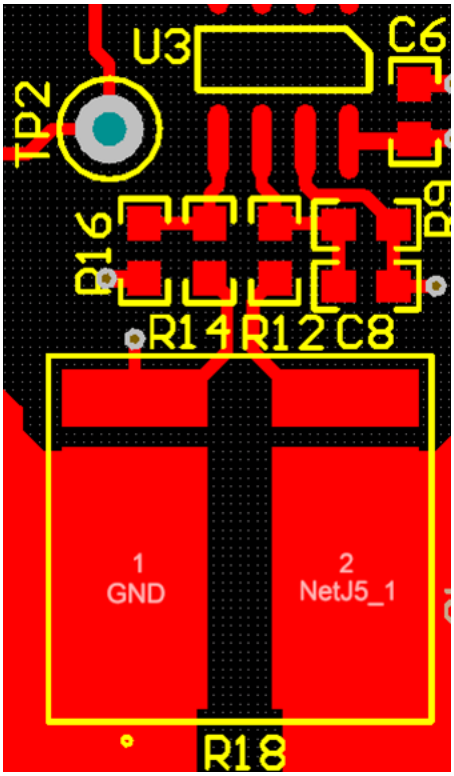


Figure 45. Layout Recommendations for Low-Side Current Sense Circuit

7.3.4 Low-Side and High-Side Sense Resistor Wiring (Kelvin Connections)

Figure 46 shows the layout for the low-side current sense circuit. Be sure to utilize the following steps for this layout:

- Current can be most precisely measured with the help of current shunt resistors. To make the power dissipation in these resistors negligible, very small values of current shunt resistors are used which are usually in the range of mΩ. At this range of resistance values the contact resistance and the termination resistance may be larger than the value of the resistor itself or may be a significant percentage in comparison to the value of the resistor. Therefore, if the voltage drop is measured across the resistor terminals, such as in Figure 46, the user is actually measuring the sum of the voltage drops across the resistor and the resistor contacts as well as a part of the high current carrying trace. This adds a significant error to the actual voltage drop across the resistor that the user intends to measure.
- This error can be avoided by using Kelvin sense connections Figure 46 shows. Now the sense connection is isolated from the actual current carrying path. The voltage drop measured is the actual voltage drop across the resistor.
- For very low values of shunt resistors, a four-terminal resistor along with a Kelvin connection must be used to obtain good accuracy.

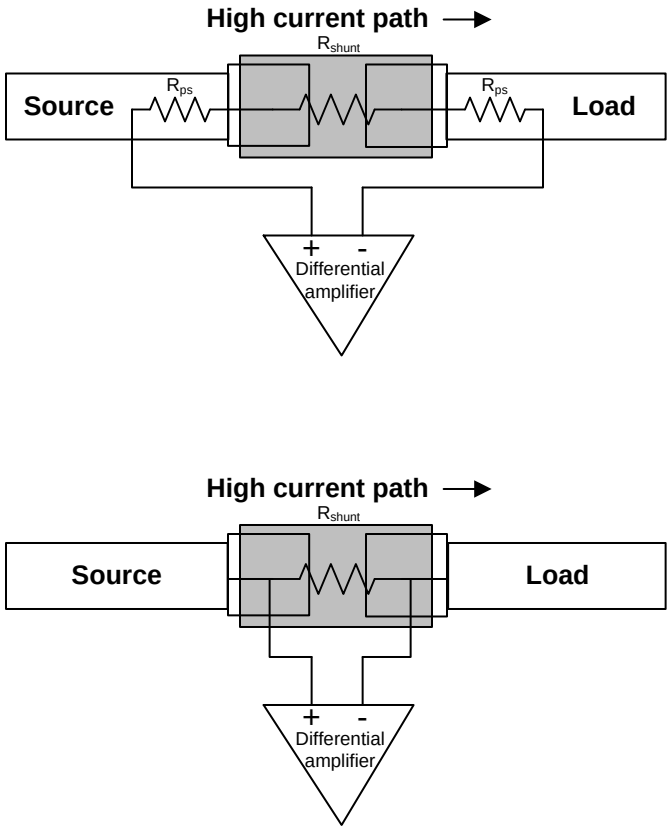


Figure 46. Non-Kelvin Connection Versus Kelvin Connection

7.3.5 Layout Prints

The size of the PCB is 71.12 mm × 62.23 mm. To download the layout prints for each board, see the design files at TIDA-00442.

7.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00442.

7.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00442.

7.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00442.

8 References

1. Texas Instruments, *High Voltage 1 2 V – 400 V DC Current Sense Reference Design*, Verified Design Guide (TIDU833)
2. Texas Instruments, *Using the UCC28880EVM-615*, UCC28880EVM-615 User's Guide (SLUUB57)
3. Texas Instruments, *High Voltage Digital Motor Control Kit (R1.1) Quick Start Guide*, (http://bit.ly/1J4rhaI)
4. Texas Instruments, *HVMotorCtrl + PFC (R1.1) Kit How t o Run Guide*, (http://bit.ly/1TVVSu5)
5. EETimes, *A Current Sensing Tutorial—Part IV: Layout and Troubleshooting Guidelines*, Design How-To (http://ubm.io/1LjBSiY)

9 About the Author

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