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Low Noise and Small Form Factor Power Management Reference Design for CC256X Bluetooth Controller

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Design Resources

TIDA-00598	http://www.ti.com/tool/tida-00598
LP5907	http://www.ti.com/product/lp5907
LP5900	http://www.ti.com/product/lp5900
CC256X	http://www.ti.com/product/CC2560

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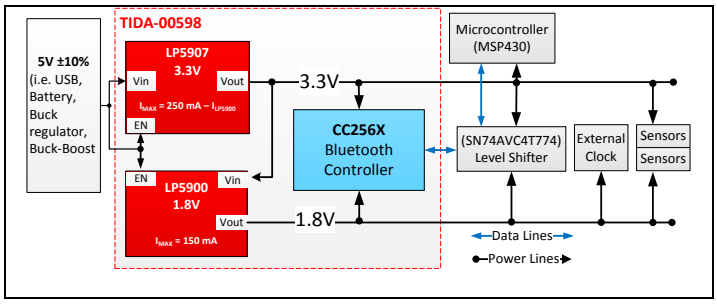
WEBENCH® Design Center

Block Diagram



Design Features

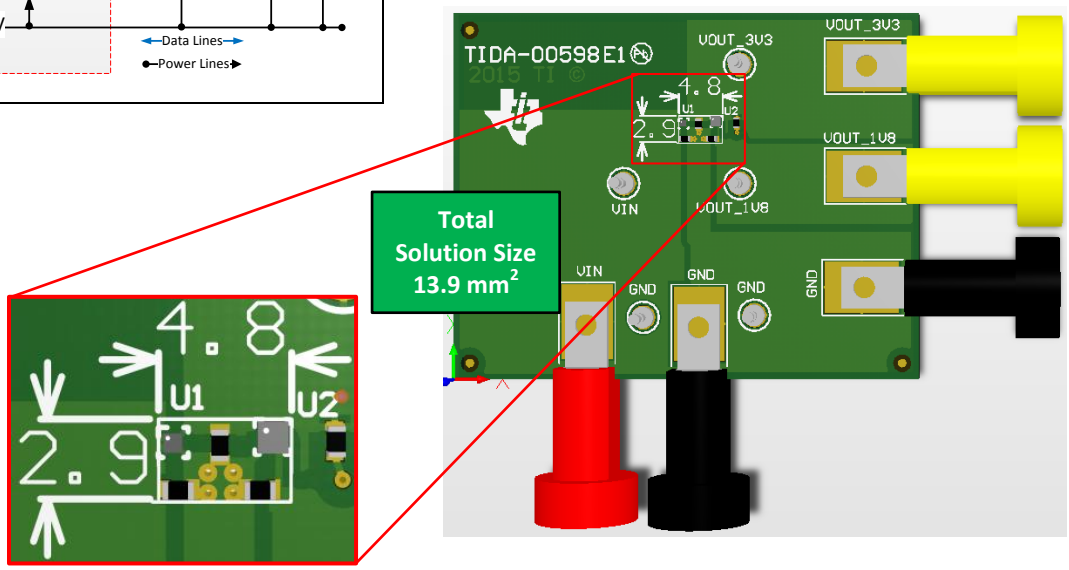
- Low noise power supply
  - Low Noise: >10 $\mu V_{RMS@}$ BW = 10 Hz to 100 kHz
  - High PSRR: >75dB @ f = 1 kHz
- Small footprint ICs with few decoupling capacitors
- Cost optimized voltage regulators
- Operating temperature range: -40°C to 85°C
- Low noise output voltage supply: 3.3V and 1.8V

Featured Applications

Bluetooth applications with board size constrains

- Households sensors and collector devices
- Key fobs (keyless entry)
- Proximity sensors
- HID keyboards and mice
- Remote display, remote unit control
- Barcode scanner Security tags
- Heart rate sensors
- Pedometers
- Smart Watch
- Blood pressure and glucose meters
- Weight scales
- Home Appliances

Board Image



1 Key Specifications

Table 1 System Specifications

ASPECTS	DESCRIPTION	DETAILS
Description of CC256X power requirements	Required Power Power sequence Shutdown—Static States	Section 4.1.2 and Section 5.1
Level shifter power requirements and description	Voltage requirements and device features	Section 4.1.2 and Section 5.2
Low noise power management design considerations	Passive component selection Thermal resistance Maximum system current supply	Section 5.3
Test setup and test results	Line and load transients, Power up timing, Thermal Image, PSRR and Noise Density	Section 6 and Section 7

2 System Description

The revolutionary CC256X Bluetooth® Controller is an integrated solution for Basic Rate (BR), Enhanced Data Rate (EDR) and Low Energy (LE) protocol. Easy to implement device reduces design effort and enable fast time to market.

The CC256X only requires two power sources to operate: VDD_IO 1.8V and VDD_IN 3.3V main power supply. The main 3.3V can be delivered directly from a battery or depending on the system main power supply a regulator may be required. It is crucial to select the right voltage regulator for the application; some applications may benefit for the high efficiency of a switch mode regulator at high input to output voltage difference. However space constrain applications with intermediate voltage difference and sensitive to voltage ripple and noise will benefit from a low noise and quiet power supply, a low dropout (LDO) linear regulator will be a perfect fit for the noise sensitive applications. An additional benefit of using LDOs is their low cost and small size with few decompiling capacitors.

The TIDA-00598 features a low noise and size optimized power management solution which regulates 5V to 3.3V and 1.8V required to operate the CC256X Bluetooth controller, these regulated voltage rails can be used to power other components in the system as microcontroller, level shifters and sensors.

Note

This design only provides guidelines and test data for the power management supply section of the CC256X. For additional information about CC256X functionality and application specific details please refer to section 9 of this document for resources.

3 Design Features and Benefits

Table 2 shows the design parameters and operation conditions.

Table 2 Design Parameters

PARAMETERS	VALUES
Operating temperature	-40 ^{O}C to 85 ^{O}C
Input voltage	(3.3 V – V_{DO}[(1)]) to 5.5 V
$I_{1.8VRail\_MAX}$	150 mA
$I_{3.3VRail\_MAX}$	250 mA - $I_{1.8VRail}$
Output noise	Noise Density: < 10 μV_{RMS} PSRR: 80 dB at 1 kHz
Total area	13.9 mm^2

(1) The dropout voltage of LP5907 is typically 50 mV at 100 mA and at 250 mA is typically 120.

Low noise

Quiet Power supply is vital for many applications for example when dealing with low frequency analog signals from audio transceivers or analog sensors which are susceptible to noise coupling from high speed signals in adjacent traces in the board or even by RFI or EMI radiation. In this design the low noise LDOs are used to filter the line ripple and regulate voltage to power the low tolerance CMOS core of the embedded devices in the system.

A low noise LDO regulator offers great noise filtering capability for power supply ripple which could be generated by the normal operation of switching mode regulators. Large discontinuous currents are generated by the power switches turn on and off. In a buck topology, large discontinuous currents are present at the input. The voltage ripple, created by those discontinuous currents, can couple into the rest of the system.

Small total solution area

Small size power management solution, the LP590X comes in a tiny DSBGA packages (<1mm), and only requires small ceramic input and output capacitor.

4 Block Diagram

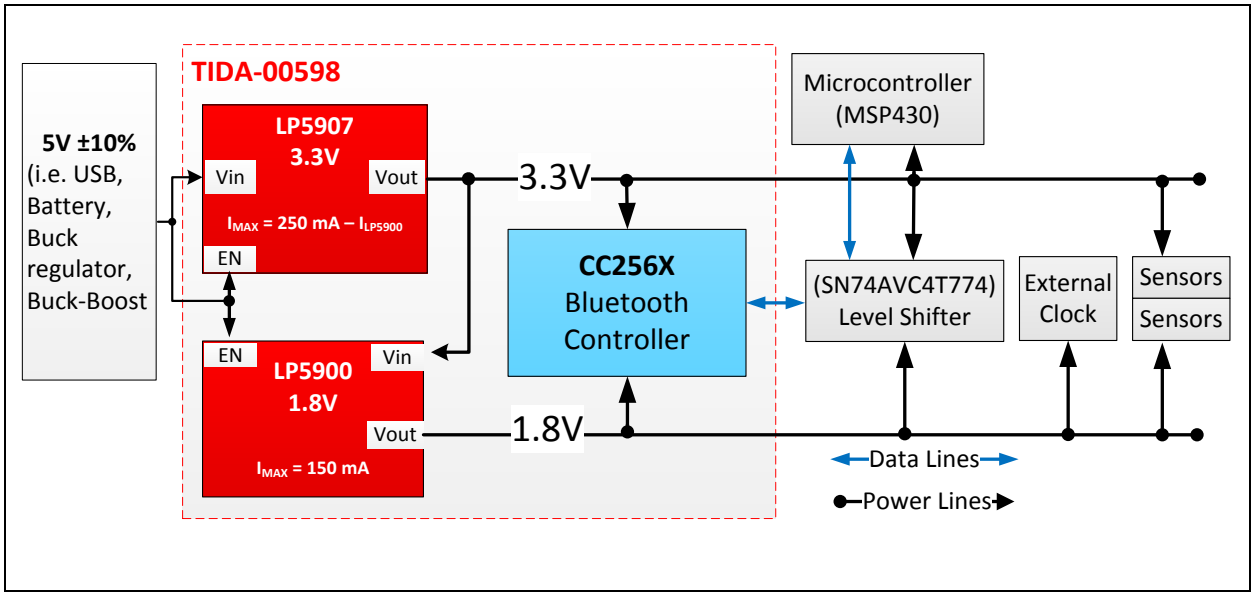


Figure 1 High Level Block Diagram of TIDA-00598 and Companion Devices

Figure 1 provides a high-level block diagram of the TIDA-00598 design. The red blocks represent the design emphasis on the power management components. The components in blue (CC256X) defined the voltage and current requirements of the design. The CC256X was not designed in the TIDA-00598 evaluation board, but its power requirements are described in section 5. The grey blocks represent other parts that were taken into account to approximate the total current requirements of the system.

4.1 Component Selection

Highlighted Components

- LP5907 3.3V LDO, 250 mA
- LP5900 1.8V LDO, 150 mA
- CC256X Bluetooth controller

Other TI Devices

- SN74AVC4T774RSV Level shifter
- MSP430 Low power microcontroller

4.1.1 Highlighted Components

LP5907

250mA, Ultra-Low Noise Low-Dropout Regulator Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor and has no load requirements the LP5900 will remain stable and in regulation with no external load.

The LP5907 is an ultra-low noise LDO, Any internal noise at the reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

- The LP5900 will remain stable and in regulation with no external load.
- Stable with 1-µF Ceramic Input and Output Capacitors
- –40°C to 125°C Junction Temperature Range for Operation
- Thermal-Overload and Short-Circuit Protection
- Low Output Voltage Noise: < 10 μV_{RMS}
- No Noise Bypass Capacitor Required
- Remote Output Capacitor Placement
- Input Voltage Range: 2.2 V to 5.5 V
- Virtually Zero IQ (Disabled): < 1 µA
- Output Voltage Tolerance: ±2%
- Low Dropout: 120 mV (typical)
- Very Low I_Q (Enabled): 12 µA
- Output Current: 250 mA
- PSRR: 82 dB at 1 kHz
- Start-up Time: 80 µs

Table 3 Key LP5907 Parameters

PARAMETERS	TYPICAL VALUES	
Package Size	0.675mm by 0.675 mm	
PSRR	>75 db @ 1 KHz	
Output Noise	I_{OUT} = 1 mA	10 μV_{RMS}
	I_{OUT} = 250 mA	6.5 μV_{RMS}
Load Transient IOUT = 250 mA to 1mA in 10 µs	40 mV	
IQ Quiescent current VEN =0.3 V (Disabled)	< 1 µA	

LP5900

150mA, Ultra-Low Noise Low-Dropout Regulator for RF/Analog Circuits Requires No Bypass Capacitor

- –40°C to 125°C Junction Temperature Range for Operation
- Stable with 0.47-µF Ceramic Input and Output Capacitors
- Thermal-Overload and Short-Circuit Protection
- Low Output Voltage Noise, 6.5 µVRMS
- No Noise Bypass Capacitor Required
- Input Voltage Range, 2.5 V to 5.5 V
- Virtually Zero IQ (Disabled), < 1 µA
- Output Voltage Tolerance, ±2%
- Very Low IQ (Enabled), 25 µA
- Low Dropout, 80 mV Typ.
- Output Current, 150 mA
- Logic Controlled Enable
- Start-up Time, 150 µs
- PSRR, 75 dB at 1 kHz

Table 4 Key LP5900 Parameters

PARAMETERS	TYPICAL VALUES	
Package Size	1.108 mm x 1.083 mm	
PSRR	>75 db @ 1 KHz	
Output Noise	I_{OUT} = 1 mA	10 μV_{RMS}
	I_{OUT} = 150 mA	6.5 μV_{RMS}
Load Transient IOUT = 150 mA to 1mA in 10 µs	50 mV	
IQ Quiescent current VEN =0.3 V (Disabled)	< 1 µA	

Alternative low noise LDOs

LP38798-ADJ: low noise LDO with higher I_{MAX} (800 mA), but bigger package size.

CC256X

The CC256x device is a complete Bluetooth BR/EDR/LE HCI solution that reduces design effort and enables fast time to market. Based on TI's 7th generation Bluetooth core, the device brings a product-proven solution that supports Bluetooth dual mode.

- Texas Instruments is now offering CC2560/64 in Bluetooth QFN devices.
- Dual mode support for Bluetooth + BLE and Bluetooth + ANT
- Flexible Bluetooth stacks supports more Profiles and MCUs
- Small package size: 7.83 mm x 8.10 mm: 63.4 mm^2

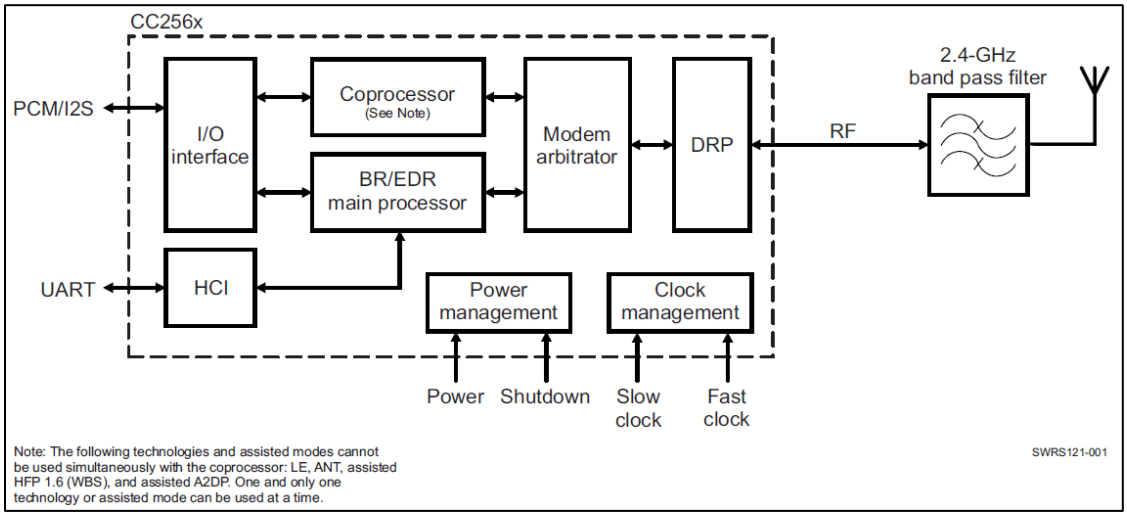


Figure 2 CC256X Functional Block Diagram

4.1.2 Other TI Devices

Level Translator: SN74AVC4T774

4-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs

- Each channel has an independent direction control pin (DIR) – Allows the channels' directional paths to be independently controlled from each other, thus have 16 possible transmitting and receiving patters.
- Complements the 500 V HBD protection of the CC256X with an embedded ESD-HBD protection of 8kV– No need for external ESD protection.
- Each port operates over the full 1.2V to 3.6V Power-Supply range – Allows the devices to interface with next-generation, power savvy processors as well as legacy peripherals
- Data rates up to 380Mbps – Allows the device to work with multiple types of interfaces

For alternative parts and more information on level translators please visit
http://www.ti.com/lsds/ti/interface/voltage-level-translation-overview.page

Microprocessor: MSP430 Family

MSP microcontrollers (MCUs) from Texas Instruments (TI) are 16-bit and 32-bit RISC-based, mixed-signal processors designed for ultra-low power. TI MCUs offer the lowest power consumption and the perfect mix of integrated peripherals for thousands of applications. TI also provides all of the hardware and software tools you need to get started. The new MSP432 Microcontrollers are 32-bit, RISC-based microcontrollers offering higher performance with a standardized ARM® core yet providing the low power benefits of MSP.
The MSP430 can be powered form the available 3.3V voltage rail and it only requires a few mA when is active most of the time is on a low power standby mode

For more information and family variant visit www.ti.com/msp

5 Design Considerations

5.1 CC256X Requirements

The main voltage supply (VDD_IN) for the module has higher tolerances than the 1.8 I/O ring voltage input (VDD_I/O), however the VDD_IN can only support a maximum voltage dip of 400 mV at a duration of 577 µs to 2.31 ms with a period of 4.6 msec.

The table below shows the input voltage requirement for the CC256X.

Table 5 CC256X Power Requirements

Power Pins	Nominal Voltage	Tolerance	Max Current	Max Power
VDD_IN	3.3 V	±30%	82.5 mA	297mW
VDD_IO	1.8 V	±5%	1 mA	1.8 mW

5.1.1 Input power pins designator and description

The figure below shows the pins designators of the CC256X, the input power pins are color coded and described in Table 4

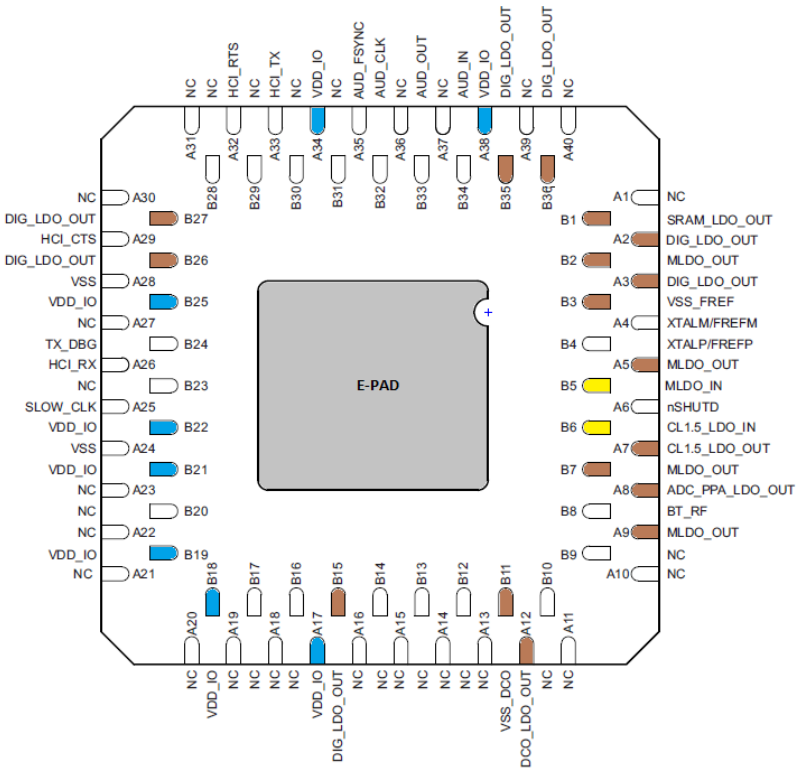


Figure 3 CC256X Pin designator

NAME	PIN NO.	FIGURE 3	DESCRIPTION
VDD_IO	A17, A34, A38, B18, B19, B21, B22, B25	Blue	I/O power supply (**1.8-V nominal**)
CL1.5_LDO_IN	B6	Yellow	Power amplifier (PA) (**3.3-V nominal**)
MLDO_IN	B5	Yellow	Main LDO input voltage (**3.3-V nominal**)
MLDO_OUT	A5, A9, B2, B7	Brown	Main LDO output Pins shorted together and connected to one 1uF cap to **GND**
DIG_LDO_OUT	A2, A3, B15, B26, B27, B35, B36	Brown	Digital LDO output QFN pin B26 or B27 must be shorted to other DIG_LDO_OUT pins on the PCB connected to two 0.47uF and one 0.1uF de-cap B36 should be isolated from the top layer GND (**GND**)
VSS_FREF	B3	Brown	Fast clock ground (Isolated and connected directly to layer 2 **GND**)
VSS_DCO	B11	Brown	DCO ground (Isolated from top layer **GND**)
DCO_LDO_OUT	A12	Brown	DCO LDO output (Cap isolated from top layer **GND**)
CL_1.5_LDO_OUT	A7	Brown	PA LDO output, connected to **GND** through a 0.1uF cap
SRAM_LDO_OUT	B1	Brown	SRAM LDO output, connected to **GND** through a 0.1uF cap
ADC_PPA_LDO_OUT	A8	Brown	ADC/PPA LDO output, connected to **GND** through a 0.1uF cap

Figure 4 CC256X Input Voltage Pins Description

5.1.2 Power Guidelines

1. Minimum trace width of at least 10 mils for the VDD and VIO traces for minimal resistance
2. Traces length must be as short as possible
3. Decoupling caps must be as close to QFN device as possible:
4. Solid GND plane in the second layer
5. Each capacitor's ground connection directly connected to solid ground layer (layer 2)
1. To minimize difference in potential the device and capacitors should be on the PCB same side
1. At least 13 vias on the thermal pad to minimize impedance for better thermal response

5.1.3 Power Sequence

The CC256X includes the following power-up requirements (see Figure 5):

- nSHUTD must be low. VDD_IN and VDD_IO are don't-care when nSHUTD is low. However, signals are not allowed on the I/O pins if I/O power is not supplied, because the I/Os are not fail-safe.
- Exceptions are SLOW_CLK_IN and AUD_xxx, which are fail-safe and can tolerate external voltages with no VDD_IO and VDD_IN.
- VDD_IO and VDD_IN must be stable before releasing nSHUTD.
- The fast clock must be stable within 20 ms of nSHUTD going high.
- The slow clock must be stable within 2 ms of nSHUTD going high.

The power-up sequence is complete by asserting RTS low, which occurs up to 100 ms after nSHUTD goes high. If RTS does not go low, the device is not powered up. In this case, ensure that the sequence and requirements are met.

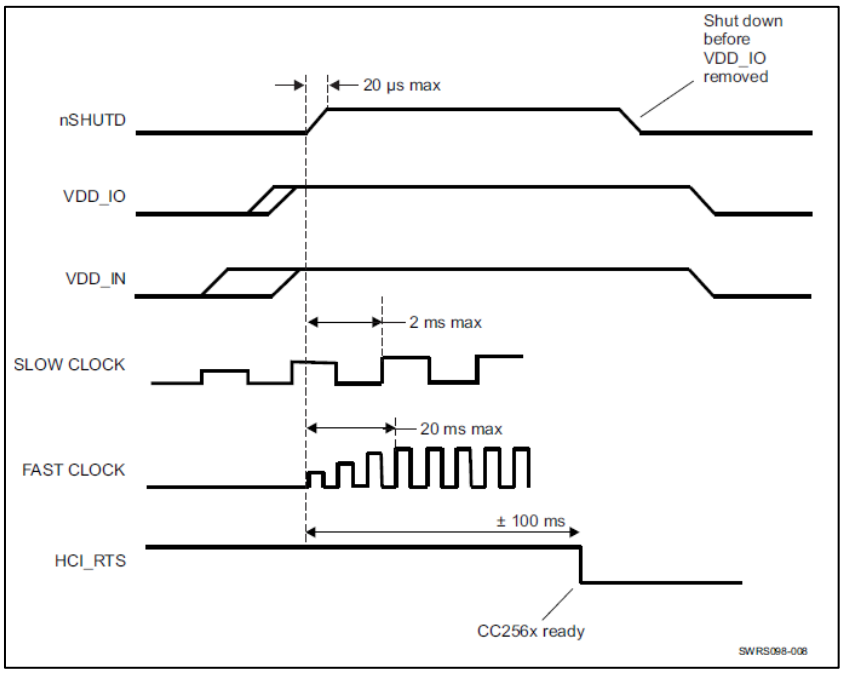


Figure 5 CC256X Power Requirements

Signal description:

HCI_RTS: HCI UART request to send the host is allowed to send data when HCI_RTS is low

nSHUTD: Shutdown input (active low)

Slow Clock: The external slow clock must be stable within 64 slow-clock cycles (2 ms) following the release of nSHUTD.

5.1.4 Shutdown—Static States

The nSHUTD signal puts the device in ultra-low power mode and performs an internal reset to the device.

The rise time for nSHUTD must not exceed 20 μ s; nSHUTD must be low for a minimum of 5 ms.

To prevent conflicts with external signals, all I/O pins are set to the high-impedance (Hi-Z) state during shutdown and power up of the device. The internal pull resistors are enabled on each I/O pin. The table below describes the static operation states.

Table 6 CC256X Power Modes

	VDD_IN(1)	VDD_IO(1)	nSHUTD(1)	PM_MODE	Comments
1	None	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
2	None	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
3	None	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
4	None	Present	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
5	Present	None	Asserted	Shut down	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
6	Present	None	Deasserted	Not allowed	I/O state is undefined. No I/O voltages are allowed on nonfail-safe pins.
7	Present	Present	Asserted	Shut down	I/Os are defined as 3-state with internal pullup or pulldown enabled.
8	Present	Present	Deasserted	Active	For I/O States in Various Power Mode, see SWRS121D

(1) The terms None or Asserted can imply any of the following conditions: directly pulled to ground or driven low, pulled to ground through a pulldown resistor, or left NC or floating (high-impedance output stage).

(2) Fail-safe means that the pins do not draw current from an external voltage applied to the pin when I/O power is not supplied to the device. External voltages are not allowed on these I/O pins when the I/O supply voltage is not supplied because of possible damage to the device

5.2 Low Noise Linear Regulators

5.2.1 Passive Component Selection

It is recommended to use at least Y5R class 2 ceramic capacitors, the dielectric for the ceramic capacitors have a maximum temperature variation of ±15% capacitance over the permissible temperature range of -55°C to +85°C. The capacitance must not be less than 0.5 µF over the full range of operating conditions.

The LP5907 is designed to work with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor, with a reasonable PCB layout, the single 1-µF ceramic output capacitor can be placed up to 10 cm away from the LP5907 package.
The LP5900 LDO can work with a nominal capacitance of 0.47 µF.

In both cases the capacitor must have an equivalent series resistance (ESR) in the range of 5 mΩ and 500 mΩ. In case that the main input voltage supply of 5V is not able to quickly source current based on the load demand it is recommended to use a big tantalum capacitor at the input of the LP5907-3.3V

5.2.2 Input Voltage

The LP5907 is directly connected to the main power rail which could be a battery, USB, buck regulator, boost or buck-boost regulator. Since the required output voltage is 3.3V the input voltage must be in the range of 3.3V+V_{DO} to 5.5V. The dropout voltage of the LP5907 is typically 50 mV with a load of 100 mA and at 250 mA load is typically 120 mV.

In addition to the benefits of low internal noise the LP5907 offers an active filtering with more than 60db input power supply rejection ratio in the range of 10Hz to 100 KHz, this is shown in **Figure 6**.

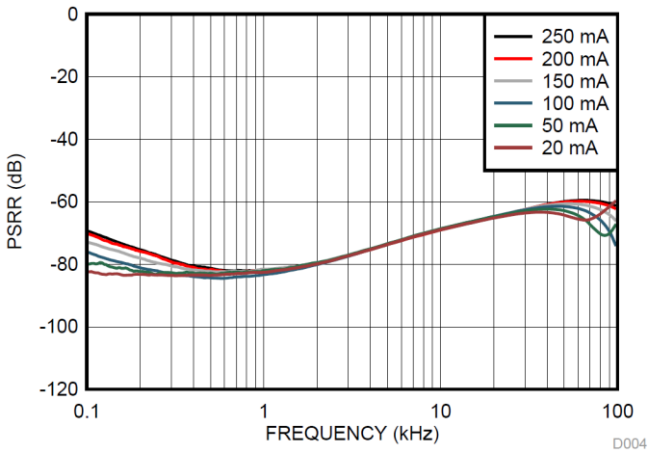


Figure 6 LP5907 PSRR 10 Hz to 100 kHz

5.2.3 Thermal Resistance

The permissible power dissipation for the LP5907 DSBGA package it's compared with other packages and devices by the capability of the device to pass heat from the power source and the junctions of the IC, to the ultimate heat sink the ambient environment. The power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The junction to ambient thermal resistance ($R_{\Theta JA}$) of the DSBGA package given in the datasheet is used to rate different packages in terms of thermal performance, but it should not be used to predict junction temperature, it may yield a wrong answer because $R_{\Theta JA}$ spec was calculated with a JEDEC 51-7 standard board which does not have an ideal layout or coper area to efficiently dissipate heat. The thermal performance is greatly influenced by the board design.

The junction to board characterization parameters (ψ_{JT}) found in the thermal metric table in the data sheet is a better way to predict the junction temperature independent of the board layers, layout, component placement etc.

Equation 1 can be used to estimate the junction temperature

$$T_J = \psi_{JT} \times P_{D\_MAX} + T_{CT} \quad (1)$$

Variables description:
T_J = Junction temperature. The maximum T_J is 125°C
T_{CT} = Case temperature (top)
P_D = Maximum power dissipation = (I_{OUT} x (V_{IN}- V_{OUT}))
ψ_{JT} = Junction to board characterization parameters

- LP5907 = 15 °C/W
- LP5900 = 5.8 °C/W

Equation 2 was used to calculate the power dissipated by the LDOs

$$P_D = P_{IN} - P_{OUT} \quad (2)$$

- LP5907 P_D: 425 mW regulating 5 V to 3.3 V at 250 mA load current.
- LP5900 P_D: 225 mW regulating 3.3V to 1.8 V at 150mA load current

With a good layout technique the LP5907 and LP5900 will be able to operate at the mentioned operating parameters without exceeding the thermal limits.

For more information about thermal metrics, Please refer to the IC Package Thermal Metrics application report SPRA953B

5.2.4 Maximum Output Current

In this design the LP5900 and LP5907 are connected in cascade the advantage is that the LP5900 will operate more efficiently due to smaller input-output voltage drop. In the other hand the LP5900 is considered a load for the LP5907. The output current of the LP5907 will be shared between LP5900 and other devices operating from the 3.3V voltage rail.

The maximum output current of the LP5900_1.8V ($I_{1.8VRail}$) is 150 mA. The maximum current available for the LP5907_3.3V is calculated with the equation below taking into account the LP5900 current demand.

$$I_{MAX(3.3VRail)} = 250mA - I_{1.8VRail} \quad (3)$$

Considering the above statement the absolute minimum current supply for the 3.3V voltage rail is 100mA.

5.2.5 Low I_Q Shutdown Mode

The LP5907_3.3V and LP5900_1.8V have a disable feature. The shutdown mode is controlled by an active low EN pin that can be controlled by a digital signal, a high voltage at this pin will enable the output voltage; inversely a low signal will disable the output voltage. The EN pin should not be left floating. In the case the disable mode is not required the EN pin should be connected to a high potential.

6 Test Setup and Results

Note

TIDA-00598 EVM is not available for purchase; however, reference design files can be downloaded at http://www.ti.com/tool/tida-00598.
Alternatively the LP5907 and LP5900 evaluation board can be purchase at their respective product folder at www.ti.com

Before applying power to the TIDA-00598 board, all external connections should be verified. The external power supply must be turned off before being connected, Confirm proper polarity to the 'VIN' and 'GND' terminals before turning the external power supply on. Under basic evaluation conditions all of the test points can be left open. The evaluation board will be in the normal operating mode when input power is applied.

6.1 Test Equipment

The following table shows the test equipment used in the upcoming sections.

Table 7 Test equipment

Test equipment	Part number
Oscilloscope	Agilent DPO4014B
Linear voltage supply	Agilent E3631A
Multimeter	Agilent E34401A
Network Analyzer	Agilent E5061B ENA

6.2 Load Transients and Regulation

This section shows that the transient response of TIDA-00598 power management solution is within the voltage tolerance and limits of the CC256X Bluetooth controller. The 3.3V VDD_IN does not exceed the maximum voltage dip of 400 mV requirements of the CC256X and also, complies with the additional requirements mentioned in section 5.1

Test parameters
LP5907 input voltage = 5V
LP5900 input voltage= 3.3V

LP5907 output voltage = 3.3V
LP5900 output voltage = 1.8V

$I_{LOAD\_3.3V}$ slew rate of 9 mA/µS
$I_{LOAD\_1.8V}$ Constant 110 mA
Maximum total load current: 200 mA

Scope shot = High resolution mode
Room Temperature 23° C

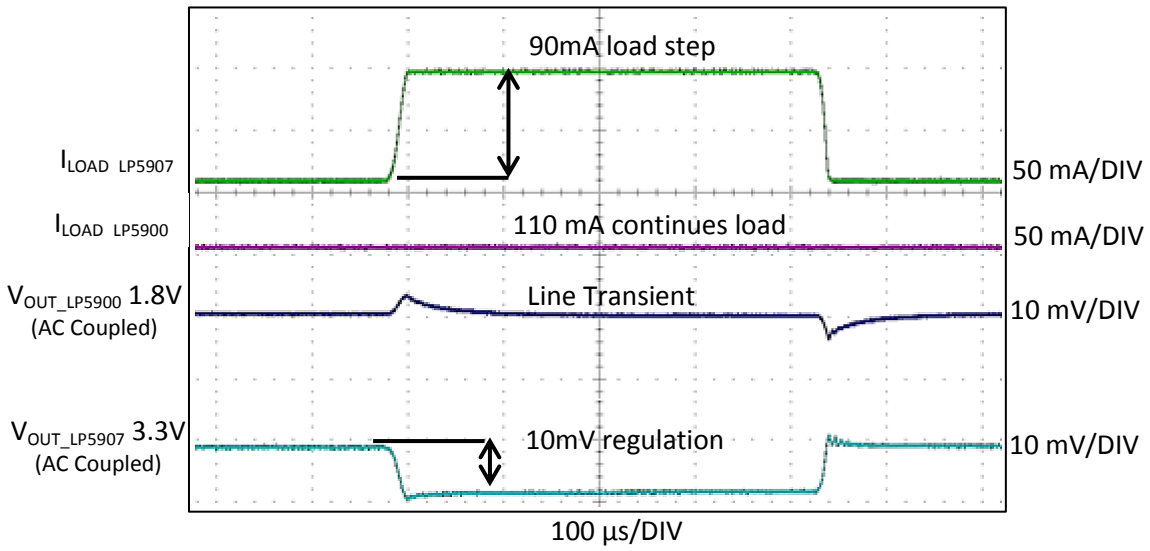


Figure 7: Load and Line Transients and Regulation of TIDA-00598

6.3 Line Transient and Regulation

The line regulation test is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Test parameters:

$C_{IN} = C_{OUT} = 1\mu F$

$V_{IN} = V_{OUT} + 1V$

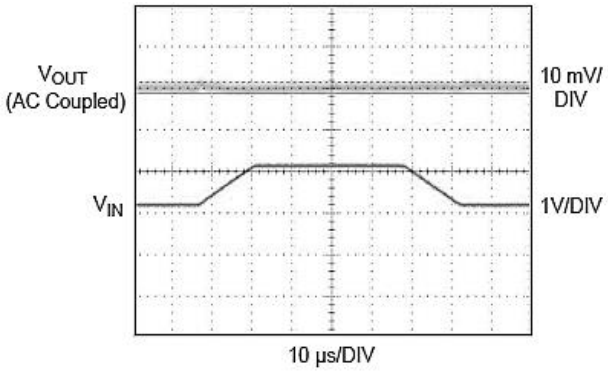


Figure 8 LP5907 Line Transient

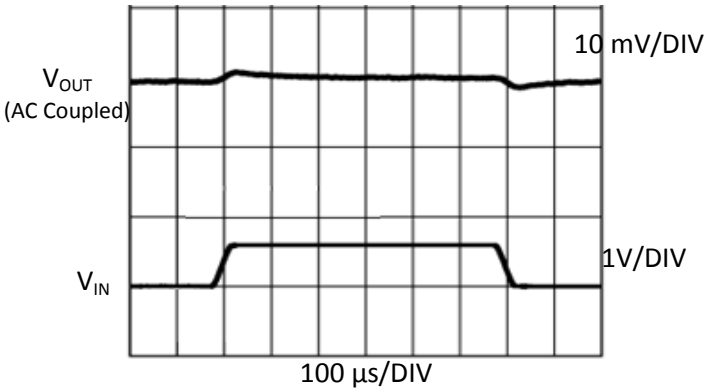


Figure 9 LP5900 Line Transient

6.4 Power Supply Ripple Rejection

The output voltage ripple rejection ratio is calculated by comparing the regulated output voltage of the device under test DUT with the input voltage ripple over a frequency range of 10Hz to 10MHz.

Test parameters:

$C_{IN} = C_{OUT} = 1\mu F$
$V_{IN} = V_{OUT} + 1V$
V_{IN_AC} = Sweep from 10Hz to 10MHz
Room Temperature = 23° C
EN pin tied to V_{IN}

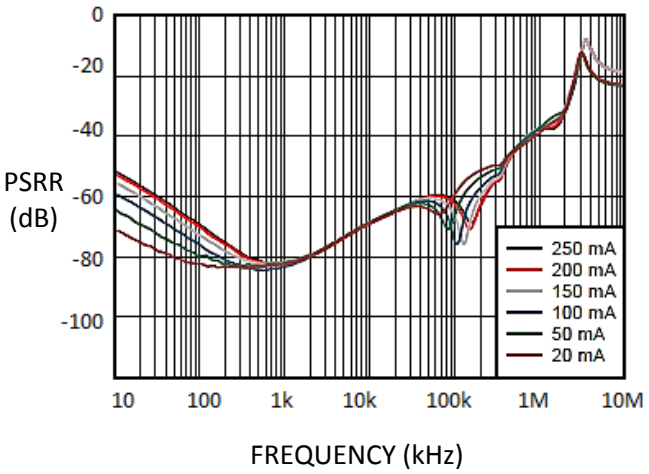


Figure 10 LP5907 PSRR

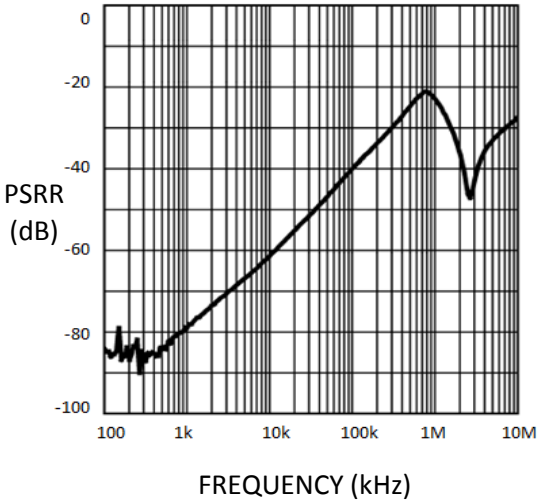


Figure 11 LP900 PSRR

6.5 Noise density

Output noise voltage is the root mean square (RMS) output noise voltage over a given range of frequencies (10 Hz to 100 kHz) under the conditions of a constant output current and a ripple-free input voltage.

Figure 12 and Figure 13 show the output noise of LP5907 and LP5900.

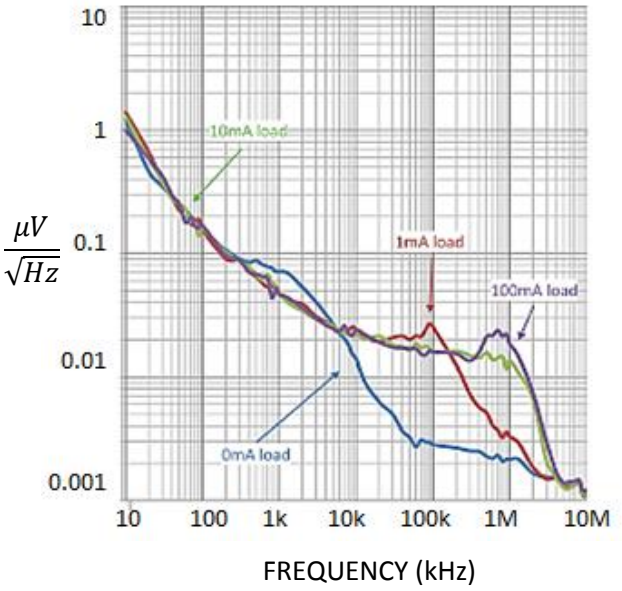


Figure 12 LP5907 Noise Density

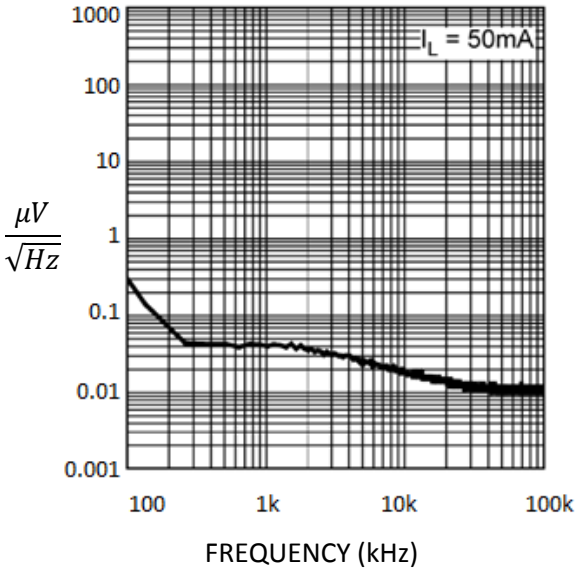


Figure 13 LP5900 Noise Density

6.6 Power up

Test parameters:
$C_{IN} = C_{OUT} = 1\mu F$
$V_{IN} = V_{OUT} + 1V$

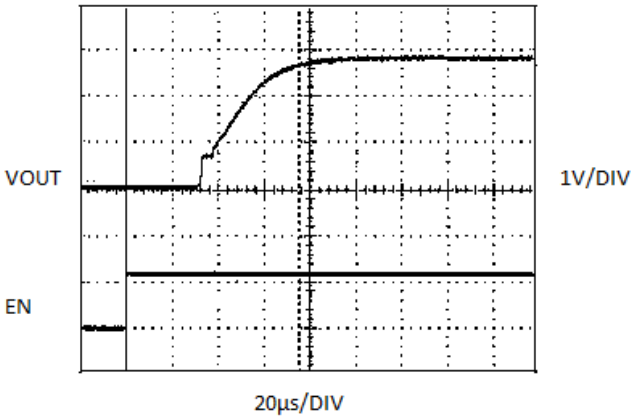


Figure 14 LP5907 Power-up

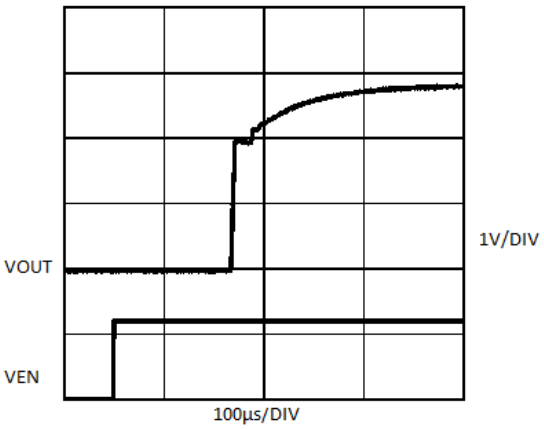


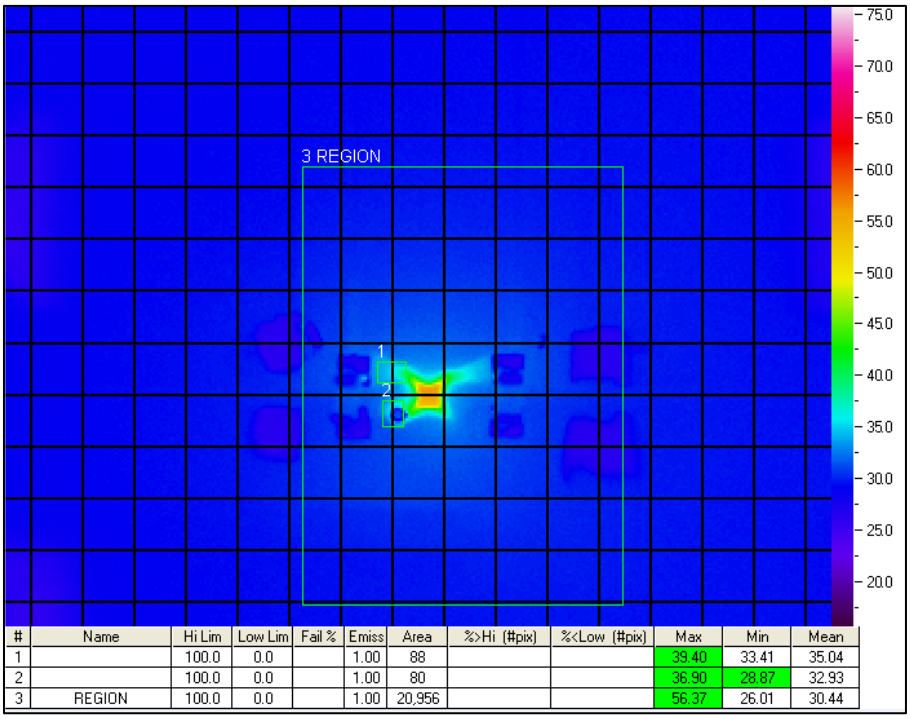
Figure 15 LP5900 Power-up

6.7 Thermals Resistance

Test Parameters:

- LP5907 Power dissipation (P_D) is 400 mV
- Room temperature 22°C
- Die Case temperature 56 °C
- Difference in temperature 56 - 25 = 31°C

In this particular board the approximate temperature increase per watt is 77.5 W/C



#	Name	Hi Lim	Low Lim	Fail %	Emiss	Area	%>Hi (#pix)	%<Low (#pix)	Max	Min	Mean
1		100.0	0.0		1.00	88			39.40	33.41	35.04
2		100.0	0.0		1.00	80			36.90	28.87	32.93
3	REGION	100.0	0.0		1.00	20,956			56.37	26.01	30.44

Figure 16 Thermal Camera Capture of LP5907UVX-3.3

The estimated junction temperature at 85°C ambient temperature is approximate 116°C which is well below the maximum junction temperature of 125°C

7 Design Files

7.1 Schematics

To download the Schematics for the board, see the design files at http://www.ti.com/tool/TIDA-00598

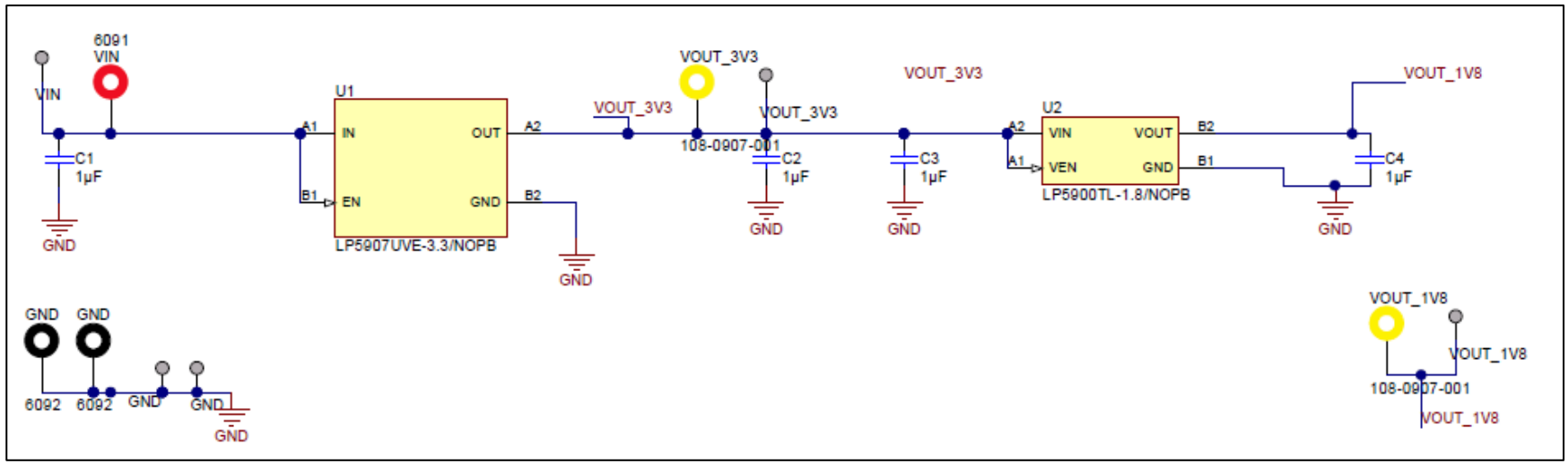


Figure 17 TIDA-00598 Schematic

7.1.1 Altium Project

To download the Altium project files, see the design files at http://www.ti.com/tool/TIDA-00598

- Gerber and NC-drills
- Bill of Materials (BOM)
- Schematic

7.2 Layout and Assembly TIPS

7.2.1 10.4 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Texas Instruments Application Note AN-1112, *DSBGA Wafer Level Chip Scale Package* (SNVA009). For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

7.2.2 10.5 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may cause incorrect operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device. Light with wavelengths in the red and infrared part of the spectrum have the most detrimental effect; thus, the fluorescent lighting used inside most buildings has very little effect on performance.

7.2.3 Layout Guidelines

Best performance is achieved by placing input and output caps on the same side of the PCB and as close as is practical to the package. The ground connections for the caps should be back to the LDO ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions

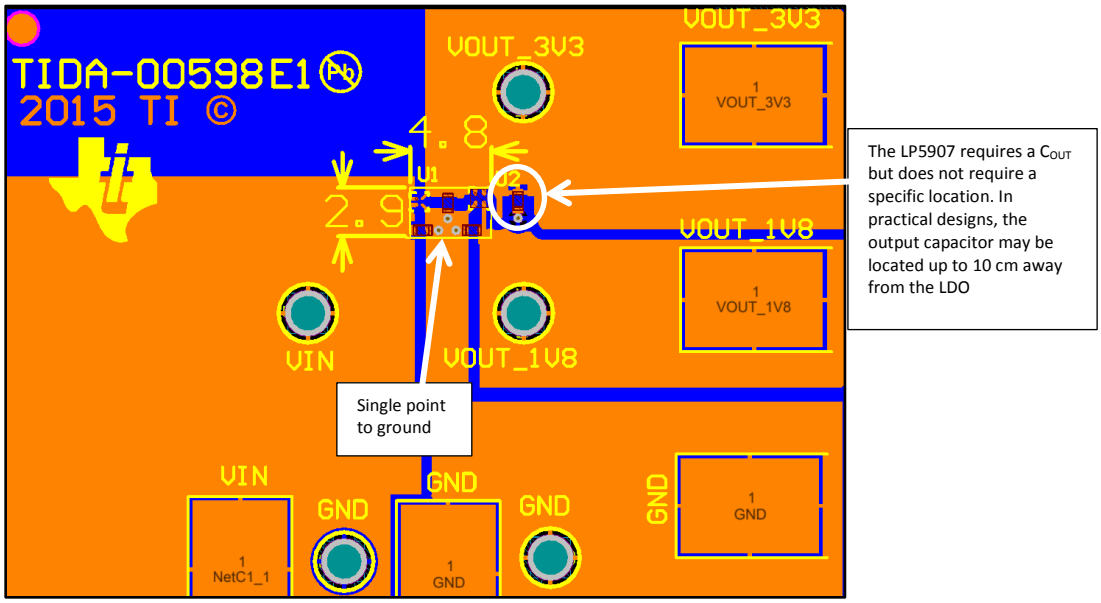


Figure 18 TIDA-00598 PCB Layout

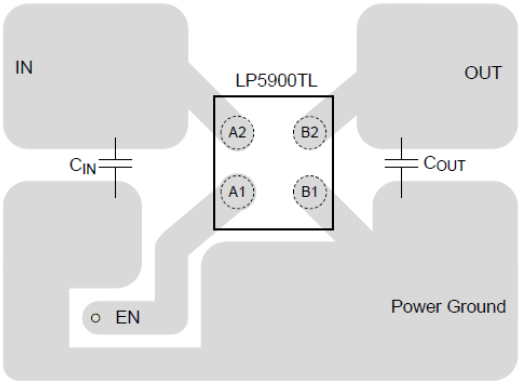


Figure 19 LP5900 Typical Layout

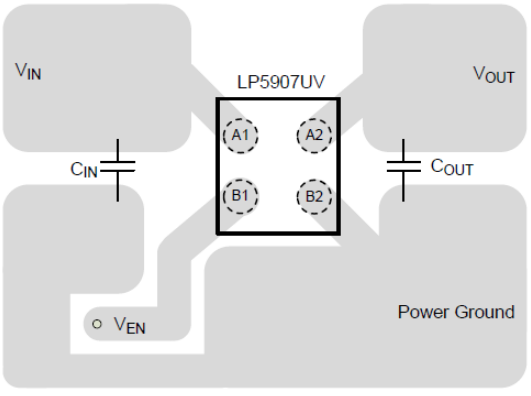


Figure 20 LP5907 Typical Layout

8 References

1. CC256X Schematic and Layout Checklist
   http://processors.wiki.ti.com/index.php/CC256x_Schematic_and_Layout_Checklist
2. CC256X system Design Guide
   http://processors.wiki.ti.com/index.php/CC256x_System_Design_Guide
3. CC256X Testing Guide
   http://processors.wiki.ti.com/index.php/CC256x_Testing_Guide
4. CC256X Data Sheet SWRS121D
   http://www.ti.com/lit/ds/symlink/cc2560.pdf
5. CC256X wiki page:
   http://processors.wiki.ti.com/index.php/CC256x

9 Terminology

TI Glossary: SLYZ022 This glossary lists and explains terms, acronyms, and definitions.

10 About the Author

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