TIDA-00588

TI Designs
Energy Harvester Booster Pack

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help you accelerate your time to market.

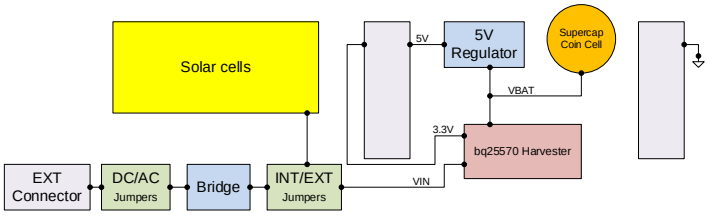
Design Resources

TIDA-00588	Design Folder
bq25570	Product Folder
TPS61220	Product Folder

Ask The Analog Experts

WEBENCH® Design Center

Block Diagram



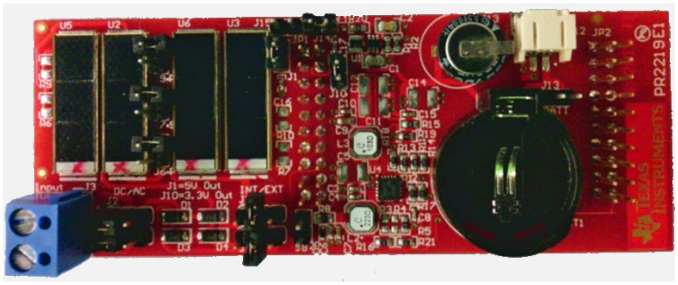
Design Features

- Energy harvesting booster pack designed for any low power Launchpad
- Converter/Charger that manages energy harvesting current sources
- Efficient nano-power buck converter
- Programmable Dynamic MPPT (Maximum Power Point Tracking)
- Super cap or coin cell storage to 50mA
- On board solar cells or external current source
- 3.3Vdc from the bq25570 to power the Launchpad
- 5V boost to power support circuitry
- Stackable design allows for creating a complete solution

Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instruments
- IoT (Internet of Things)

Board Image



1 Key System Specifications

bq25570	**Value**		**Description**
VINmins	0.33	Vdc	Minimum Startup input voltage
VINminr	0.1	Vdc	Minimum operating input voltage
I_INmin	280	uA	Minimum required current to startup the bq25570 with 5V boost
P_INmin	0.00009	W	Power to startup the bq25570 with the 5V regulator (there is no minimum power requirement to startup with the 5V regulator removed for operation)
VBAT_OK_on	3.51	Vdc	VBAT threshold Turn On
VBAT_OK_off	3.42	Vdc	VBAT threshold Turn Off
Vout_3	3.322	Vdc	Buck output of the bq25570
Iout_3_c	50	mA	Max current output of the regulator with a coin cell
Iout_3_s	0.8	mA	Max current output of the regulator with a super cap
V_ch	4.188	Vdc	Battery charge voltage
TPS61220			
Vout_5	5.09	Vdc	Boost output of the 5V regulator
Iout_5_c	10	mA	Max current output of the regulator with a coin cell
Iout_5_s	0.5	mA	Max current output of the regulator with a supercap
I_q	18	uA	Quiescent Current
I_std	4.7	uA	Standby current
Freq	1.25	MHZ	Idle current PWM frequency
LIR2032			
MAX_V	4.2	Vdc	Max charge voltage
NOM_V	3.6	Vdc	Nominal Voltage
MIN_V	2.8	Vdc	Minimum Voltage
CH_CUR	30	mA	Max charge current
C_rate	50	mA	Max continuous current
I_max	60	mA	Max peak current

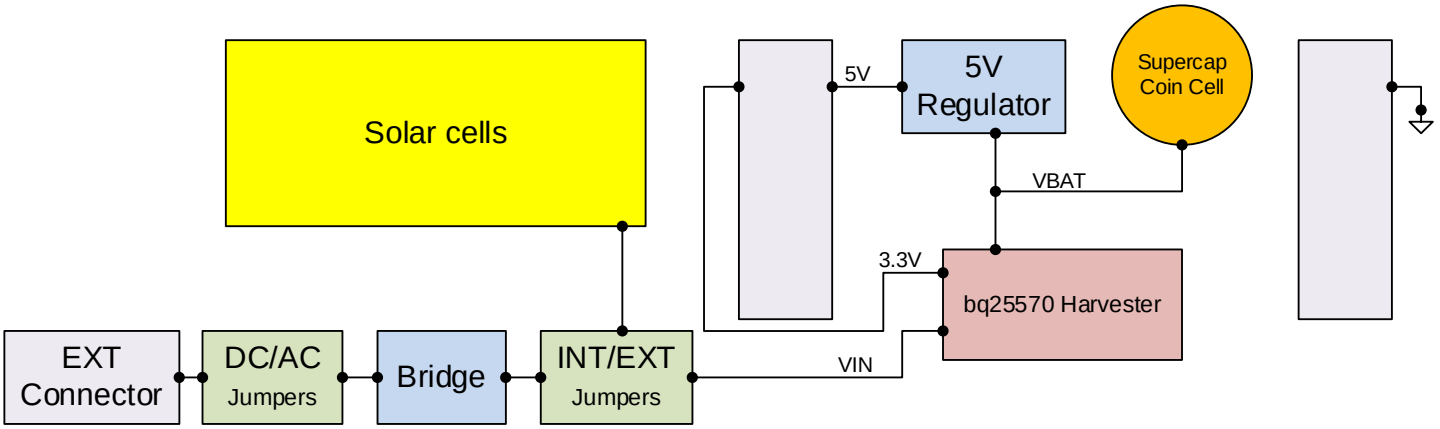
2 System Description

This is an Energy Harvester Booster Pack and is designed with the flexibility to support a variety of current source inputs and energy storage elements. Use this booster pack with your favorite TI Launchpad development board to power your design from a local source of energy.

There are jumpers on the board that will allow the use of the internal 4 cell solar array that can be operated in 4s or in a 2s2p parallel mode. The user can set the jumpers to use the internal or an external current source. There is a bridge diode to convert AC to DC if needed. Most systems will typically need some type of energy storage element such as a re-chargeable battery, super capacitor, or conventional capacitor. This system has an on board Super capacitor, a socket for an LIR2032 coin cell and a connector that can be used to add your own lithium storage element. To prevent damage to the storage element, both maximum and minimum voltages are monitored against the internally set under-voltage (UV) and user programmable over-voltage (OV) levels.

To further assist users in the strict management of their energy budgets, the bq25570 toggles the battery good (VBAT_OK) flag to signal an attached microprocessor when the voltage on an energy storage battery or capacitor has dropped below a pre-set critical level. This should trigger the reduction of load currents to prevent the system from entering an under voltage condition. There is also independent enable signals to allow the system to control when to run the regulated output or even put the whole IC into an ultra-low quiescent current sleep state.

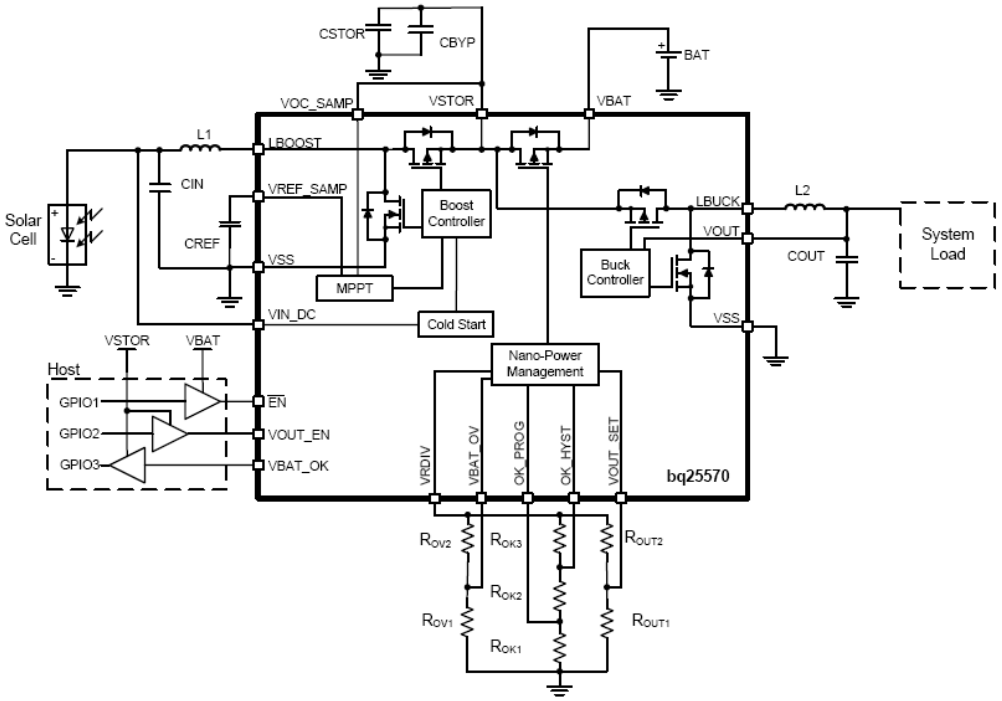
In addition to the boost charging front end, the bq25570 provides the system with an externally programmable regulated supply via the buck converter. The regulated output has been optimized to provide high efficiency across low output currents (< 10 µA) to high currents (~110 mA). The buck converter on the bq25570 will provide 3.3Vdc for the Launchpad power and an additional switching boost converter will supply 5V to run accessories.



2.1 Bq25570

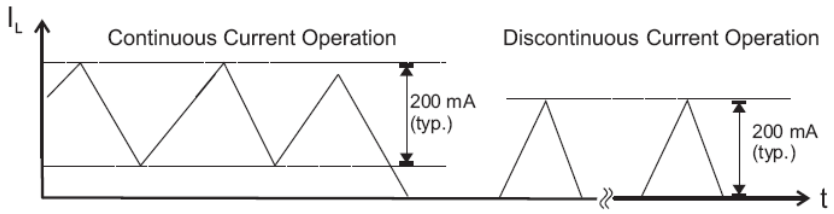
The bq25570 device is a highly integrated energy harvesting Nano-Power management solution that is well suited for meeting the special needs of ultra-low-power applications. The product is specifically designed to efficiently acquire and manage the microwatts (µW) to milliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. The main boost charger is powered from the boost output, VSTOR. Once the VSTOR voltage is above VSTOR_CHGEN (1.8 V typical), for example, after a partially discharged battery is attached to VBAT, the boost charger can effectively extract power from low voltage output harvesters such as TEGs or single or dual cell solar panels outputting voltages down to VIN(DC) (100 mV minimum). When starting from VSTOR=VBAT < 100 mV, the cold start circuit needs at least VIN(CS), 330 mV typical, to charge VSTOR up to 1.8 V.

The bq25570 also implements a programmable maximum power point tracking sampling network to optimize the transfer of power into the device. The fraction of open circuit voltage that is sampled and held can be controlled by pulling VOC_SAMP high or low (80% or 50% respectively) or by using external resistors. This sampled voltage is maintained via internal sampling circuitry and held with an external capacitor (CREF) on the VREF_SAMP pin. For example, solar cells typically operate with a maximum power point (MPP) of 80% of their open circuit voltage. Connecting VOC_SAMP to VSTOR sets the MPPT threshold to 80% and results in the IC regulating the voltage on the solar cell to ensure that the VIN_DC voltage does not fail below the voltage on CREF which equals 80% of the solar panel's open circuit voltage. Alternatively, an external reference voltage can be provided by a MCU to produce a more complex MPPT algorithm.

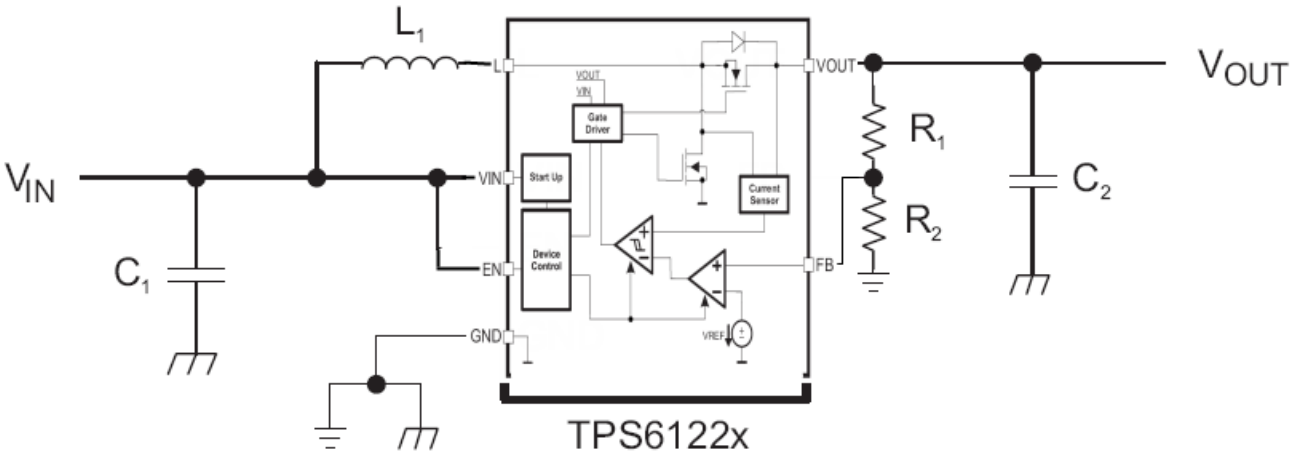


2.2 TI TPS61220

The TPS6122x is a high performance, high efficient family of switching boost converters. To achieve high efficiency, the power stage is realized as a synchronous-boost topology. For the power switching, two actively controlled low-RDSon power MOSFETs are implemented.
The device is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 200 mA and adjusting the offset of this inductor current depending on the output load. If the required average input current is lower than the average inductor current defined by this constant ripple current, the inductor current becomes discontinuous to keep the efficiency high under low-load conditions.



The output voltage VOUT is monitored via the feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly. In fixed output voltage devices, an internal feedback network is used to program the output voltage. In adjustable versions an external resistor divider is required. The self-oscillating hysteretic current mode architecture is inherently stable and allows fast response to load variations. This architecture also allows using a wide range of inductor and capacitor values.



3 Getting Started

The Energy Harvester Booster Pack can be a great addition to you design development. Having a good understanding of some of the key features is very important. Before you start, take the time to understand these important concepts.

3.1 Coin Cell

The coin cell is a LIR2032 Lithium Battery. The max charge current is 30mA. The max constant current is 50mA and the max peak current is 60mA. These specifications come from the battery manufacture. You should become familiar with this battery and it's limitations before using it in a design.

There is no adjustable current limit setting on the bq25570. This IC is capable of charging up to 100mA. It is up to the designer to measure and understand the capabilities of the current source they are using. For example the IXYS KXOB22-04X3L has a short circuit current of 15mA, and therefore will never be capable of charging at a current that is above the maximum current capability of the LIR2032. If you use an external current source that has more than 30mA short circuit current you may damage the coin cell battery. You may need to use an external battery that can handle the higher charge current.

3.2 Solar Cell

The solar cell is an IXYS KXOB22-04X3L. The typical efficiency is 22%. This cell has a very good response over a wide wavelength range and therefore can be used in both indoor and outdoor applications.

A standard desk lamp has a 400-800 LUX value. When using this solar cell indoors you can expect between 5uW to 40uW of power. This is not a lot of energy so when using any energy harvesting circuit create your design for low power and remember to use sleep mode techniques to minimize your power requirements and plan accordingly. When used properly energy harvesting can run you design for many years without needing batteries.

3.3 Super Capacitor

This circuit has a 47mF super capacitor on board. A simple low power circuit can run on this super cap without batteries. The biggest difference between a battery and a supercap besides the capacity is that a battery has a minimum charge voltage that is usually between 2.5Vdc and 3.0Vdc. This means that the battery will always have a small amount or energy stored at all times. The super cap does not have a minimum voltage and also has a high leakage current (usually a few micro amps, this is a lot compared to most batteries). What this means is that when starting your energy harvester the super cap voltage will most likely be zero volts. The bq25570 will start up with 300mV input from the current source and will charge the super cap in a reduced cold start mode until the supercap voltage reaches 1.8Vdc. The bq25570 will then begin normal charging. Under normal room lighting the light level can be 150-800 LUX. This means that the supercap has to be charged to 3.5Vdc before anything will turn on. This can take several hours to startup the super cap. This time can be reduced by increasing the light level. Sun light can start up the super cap in a few minutes. Using a super cap as your only method of storage is usually meant for very low power and intermittent circuits that never turn off and can afford the occasional long start up time.

Note: Having a battery in circuit will mean that your device will start up almost immediately if the battery voltage is above 3.4Vdc

3.4 External Battery

The use of an external battery is possible with the external battery connector supplied on the board. There are a few design concerns when using an external battery. First it is the responsibility of the designer to provide battery protection for your design. The max charge current from the bq25570 is 100mA and the max charge voltage is 4.2Vdc. The max charge voltage is resister programmable, so if you are using other battery chemistries you mush reprogram the bq25570 to meet the required manufactures specifications. With an external battery with a cRate above 200mAh the 3.3V regulator and the 5V regulator can supply up to 100mA each.

3.5 3.3V and 5.0V regulators

The bq25570 has an internal buck regulator. The output voltage is resister programmed for 3.3Vdc. This regulator can supply up to 100mA of current, however the coin cell can only supply 50mA, so it is up to the user to make sure that there circuit does not draw more than the maximum current that the battery can supply. The 5V regulator is a boost circuit. It runs off of the energy storage device (Super cap, coin cell or battery). The quiescent current of the 5V regulator is about 5uA.When starting a super cap from zero volts, and the light level is very low, the bq25570 start up current may be below the 5V regulator quiescent current and may never start up. It is recommended to disconnect the 5V regulator when using a super cap with low light levels. The 3.3Vdc buck will not turn on until the VBAT reaches 3.5Vdc. The quiescent current of the buck is about 450nA. Startup is possible with as little as 5uW of harvested input power.

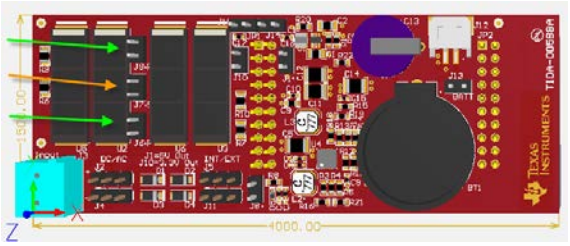
3.6 Jumpers

This section will help the user to set up and configure the energy harvester for basic and custom applications

3.6.1 Solar cells configuration

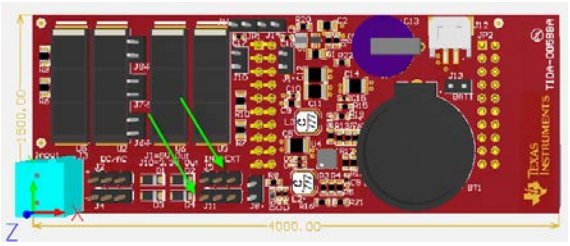
J6 and J9 (Green Arrows) will place the 4 solar cells into a 2s2p (2 cells in series and 2 series cell string in parallel. The benefit is a higher current in higher light levels.

J7 will place all of the solar cells in series. The benefit is a higher operating voltage in lower light level applications.



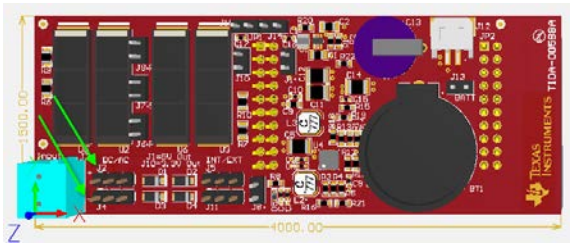
3.6.2 Internal and external current sources

J5 and J11 will allow the user to use the internal solar cells or use their own current source. (Solar, wind, heat, and vibration current sources will work on this unit)
Move both jumpers J5 (Positive) and J11 (Negative) to the left to use the onboard solar cells and move both jumpers to the right to use the input connector J3 to connect your own current source



3.6.3 DC\AC operations

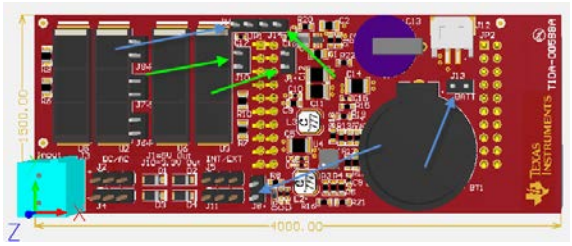
J2 (positive) and J4 (negative) jumpers will allow the user to connect a DC or AC current source to the energy harvester.



Move J2 and J4 to the left will bypass the bridge rectifier and for DC applications. Move J2 and J4 to the right for AC current sources (Wind generators and vibration current sources)

3.6.4 Regulators

J13 and J8 are test pins. They are the connectors with the blue arrows. Never place a jumper across these connectors as it will be a direct short.



J15 is a 2 pin ground connection used for connecting test equipment

J14 is the enable pin for the 5V Regulator. Remove this jumper and the 5V Regulator will not start up. (It will draw 5uA in quiescent current in this mode)

J1 will disconnect the output of the 5V regulator from the header pins. These pins can also be used to measure current out of the 5V regulator by adding a current shunt or meter in series

J10 will disconnect the output of the 3.3V regulator from the header pins. These pins can also be used to measure current out of the 3.3V regulator by adding a current shunt or meter in series.

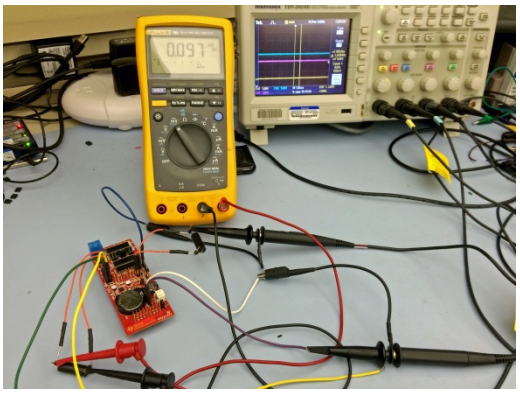
R22 is a zero Ohm resister and can be removed to fully disconnect the 5V input from the energy storage. This will also remove the quiescent current of the regulator. Add a current shunt or meter in series with the pads of this part to measure current in and out of the 5V regulator. To fully isolate the 5V regulator, also remove J1 and J14.

R23 is a zero Ohm resister and can be removed to isolate all of the storage devices. Add a current shunt or meter in series with the pads of this part to measure current in and out of the storage elements.

4 Test Setup

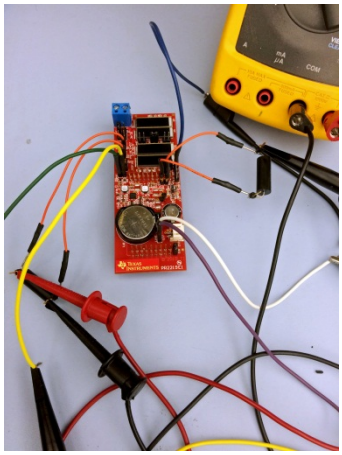
Description of the test setup

Test equipment:



- TDS2024B Tektronix Scope
- 189 Fluke Multi-meter
- 2400 Keithley Source Meter
- DI-158U Dataq Data Acquisition Module
- 2 - 1 Ohm 1% 5W Precision shunts

The use of a precision multi-meter along with a 1 Ohm shunt will make a great current measuring solution. Set the meter to the DC milli-volt scale and read the current as milli and micro Amps. Example: 1mV = 1mA



The source meter was used to supply a current limited source input for the startup cycles. This was better than attempting to find light sources that would provide the different currents needed to demonstrate startup at different currents.

The data acquisition module has an adjustable gain that will allow measuring in the micro volts range. 1 channel was used with the shunt to measure the input current and the other 3 channels were used to measure Voltage in, VBAT and VSTOR. After the cycle was finished the data was saved as a CSV file and imported into Excel for processing and plotting.

After the startup sequences all measured test results are in the Key System Specifications section of this document.

5 Test Data

The following description explains the test plots that show the process of a cold start from zero volts to the 1.8V threshold where the bq25570 changes over to charge mode thru the voltage out max setting of 4.2Vdc. This is the complete cycle. When starting at zero volts the bq25570 will enter into a cold start mode. The cold start circuit's goal is to charge VSTOR higher than VSTOR_CHGEN so that the main boost charger can operate. When a depleted storage element is initially attached to VBAT the harvester can provide a voltage > VIN(CS) and total power at least > PIN(CS), assuming no system load or leakage at VSTOR and VBAT, the cold start circuit can charge VSTOR above VSTOR_CHGEN. Once the VSTOR voltage reaches the VSTOR_CHGEN threshold, the IC goes thru the next three steps.

1. First it performs an initialization pulse on VRDIV to reset the feedback voltages,
2. Then disables the charger for 32 mS (typical) to allow the VIN_DC voltage to rise to the harvester's open circuit voltage which will be used as the input voltage regulation reference voltage until the next MPPT sampling cycle.
3. Lastly performs its first feedback sampling using VRDIV, approximately 64 mS after the initialization pulse.

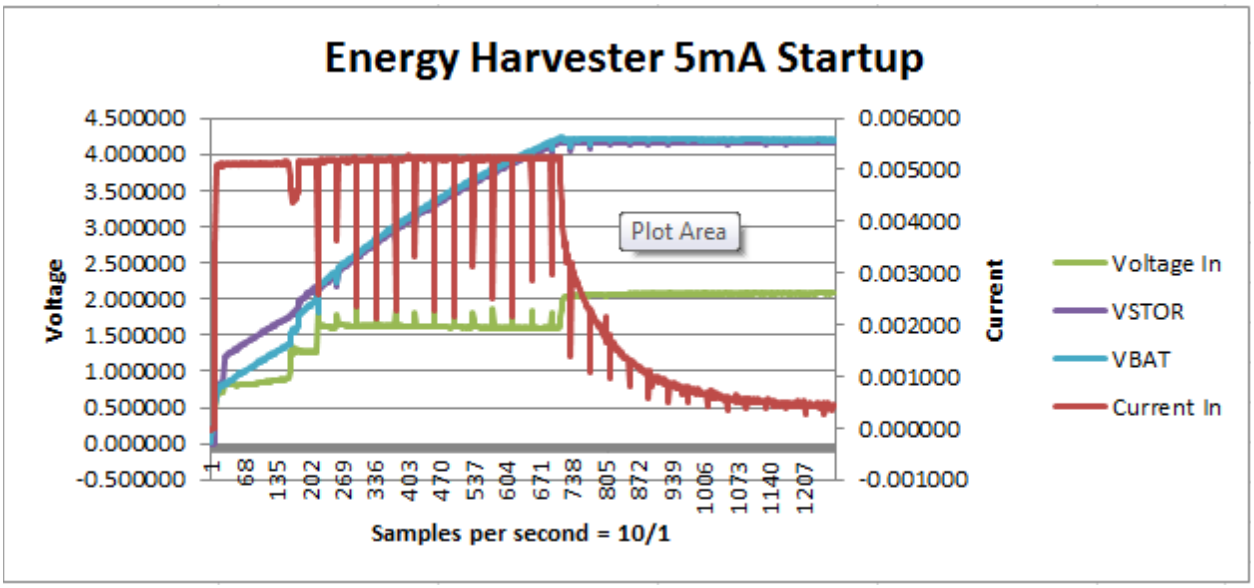
The energy harvester must supply sufficient power for the IC to exit cold start. Due to the body diode of the PFET connecting VSTOR and VBAT, the cold start circuit must charge both the capacitor on CSTOR up to the VSTOR_CHGEN

and the storage element connected to VBAT up to VSTOR_CHGEN less a diode drop. When a rechargeable battery with an open protector is attached, the initial charge time is typically short due to the minimum charge needed to close the battery's protector FETs. When large, discharged super capacitors with high DC leakage currents are attached, the initial charge time can be significant.
When the VSTOR voltage reaches VSTOR_CHGEN, the main boost charger starts up. When the VSTOR voltage rises to the VBAT_UV threshold, the PMOS switch between VSTOR and VBAT turns on. This provides additional loading on VSTOR and could result in the VSTOR voltage dropping below both the VBAT_UV threshold and the VSTOR_CHGEN voltage, especially if system loads on VSTOR or VBAT are active during this time. Therefore, it is not uncommon for the VSTOR voltage waveform to have incremental pulses (for example, stair steps) as the IC cycles between cold-start and main boost charger operation before eventually maintain VSTOR above VSTOR_CHGEN.

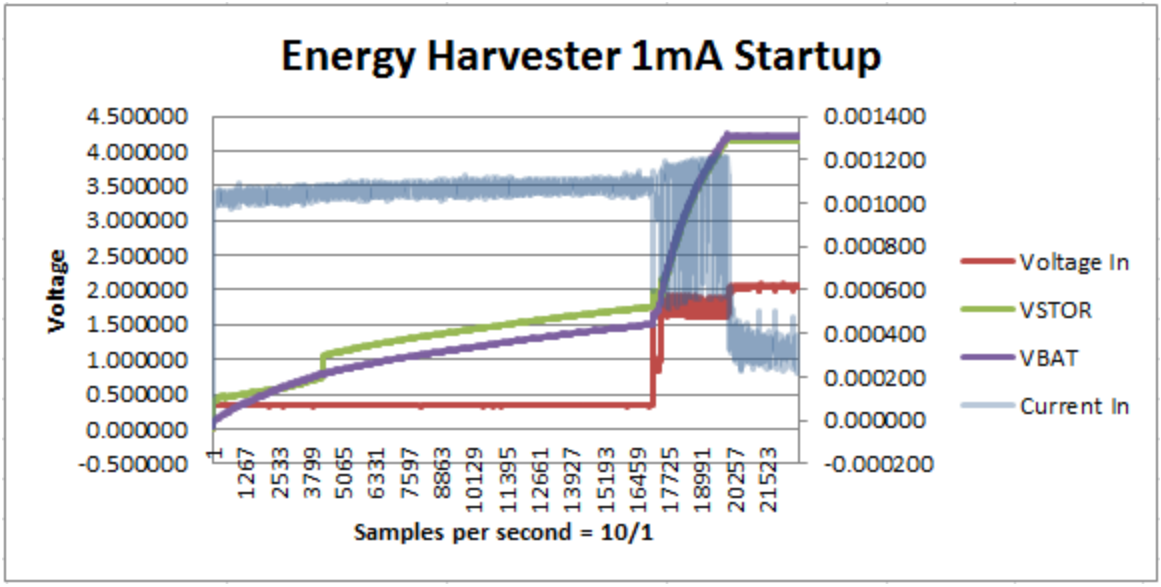
The last plot shows the proper turn on of the 3.3V and 5V supplies when the VBAT voltage reaches 3.5V. While discharging the VBAT_OK line will turn off when the VBAT voltage reaches 3.4V. This will prevent further discharging of the batter and the loss of regulation in the 3.3V supply.

Note: To maximize the use of the energy stored you can run your micro controller at a lower voltage2.8V – 3.0V. You can reprogram the bq25570 output regulator to provide 2.8V with a turn on of 3.0V and a turn off of 2.9V.

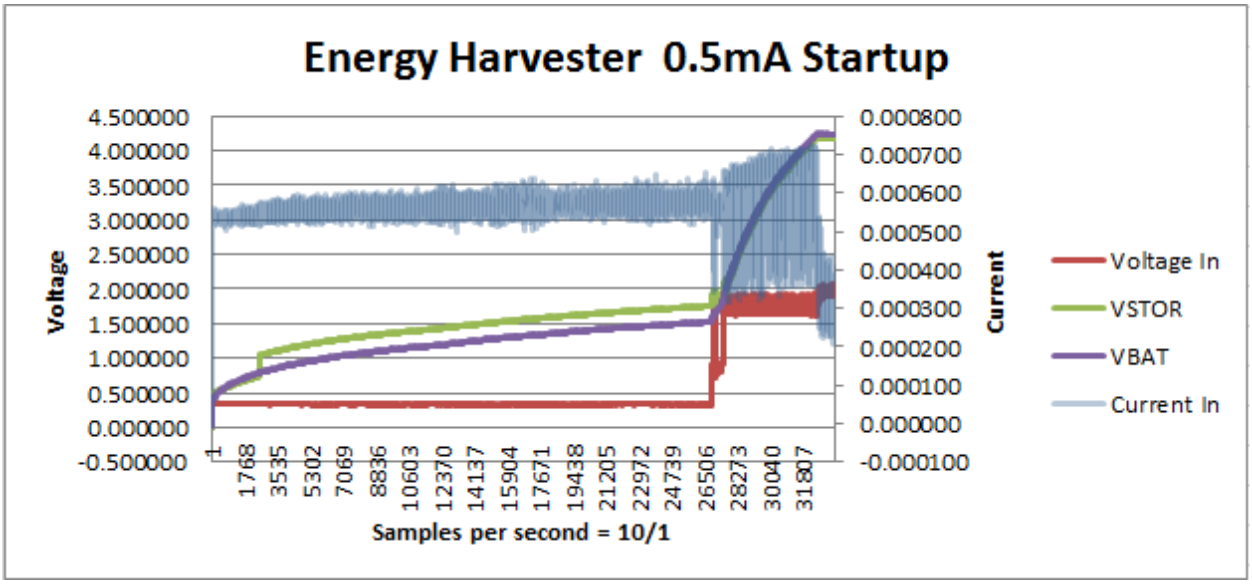
5.1 5mA start up



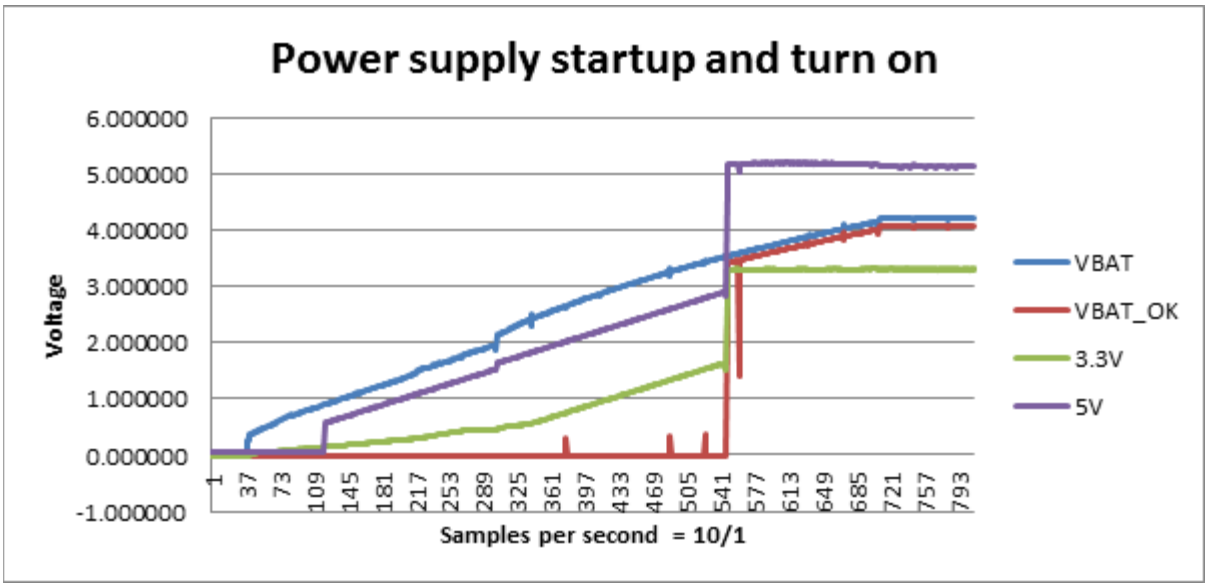
5.2 1mA start up



5.3 0.5mA start up



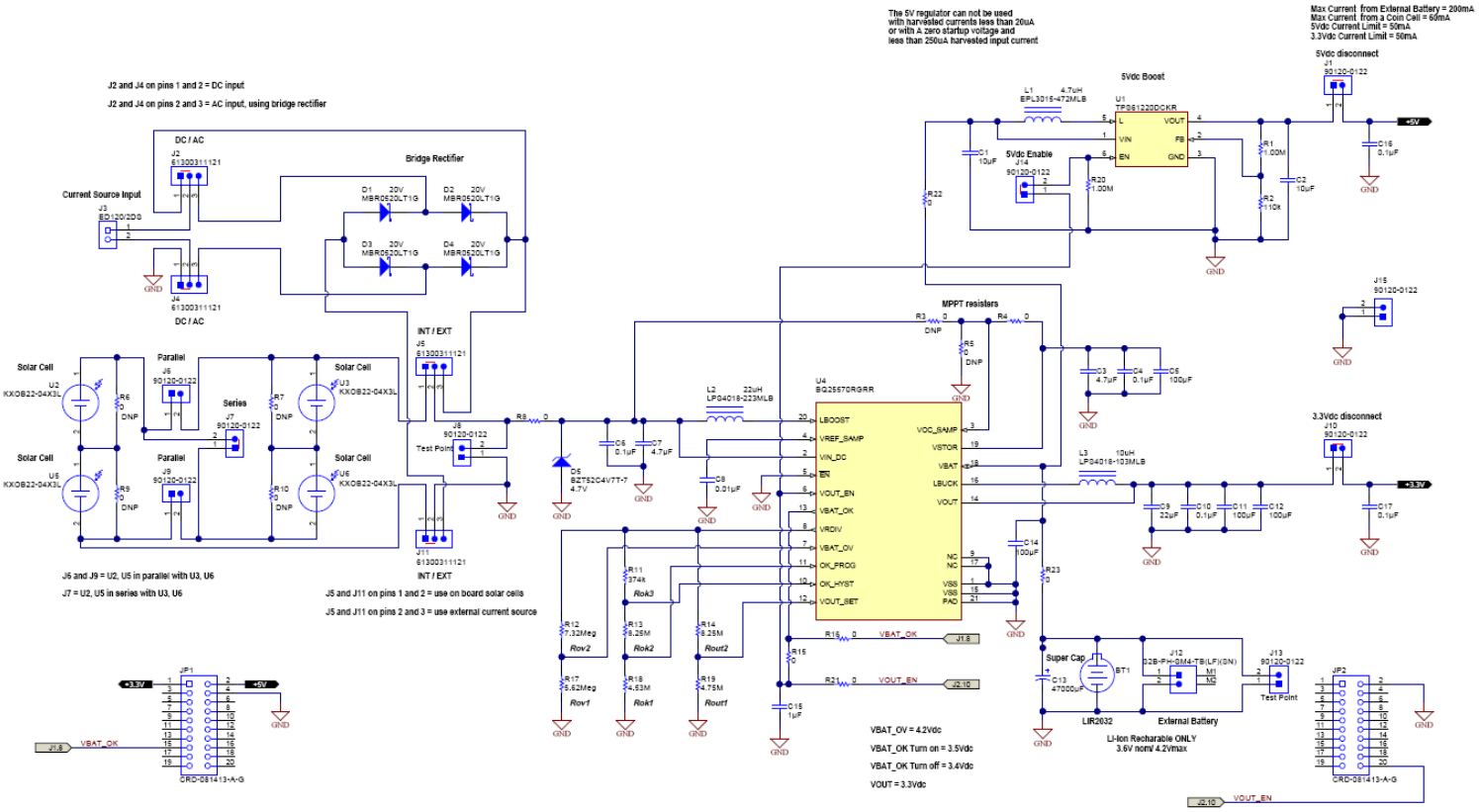
5.4 3.3V and 5V start up Plot



6 Design Files

6.1 Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/TIDA-00588



6.2 Bill of Materials

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TIDA-00588 REV A Bill of Materials

Item #	Designator	Quantity	Value	PartNumber	Manufacturer	Description	PackageReference
1	!PCB1	1		TIDA-00588	Any	Printed Circuit Board	
2	BT1	1		BS-7	Memory Protection Devices	Battery Holder, CR2032, Retainer clip, TH	CR2032 holder
3	C1, C2	2	10uF	GRM21BR61A106KE19L	MuRata	CAP, CERM, 10 µF, 10 V, +/- 10%, X5R, 0805	0805
4	C3, C7	2	4.7uF	C1005X5R0J475M050BC	TDK	CAP, CERM, 4.7 µF, 6.3 V, +/- 20%, X5R, 0402	0402
5	C4, C6, C10, C16, C17	5	0.1uF	GRM155R71A104KA01D	MuRata	CAP, CERM, 0.1 µF, 10 V, +/- 10%, X7R, 0402	0402
6	C8	1	0.01uF	GRM155R61A103KA01D	MuRata	CAP, CERM, 0.01 µF, 10 V, +/- 10%, X5R, 0402	0402
7	C9	1	22uF	CL10A226MP8NUNE	Samsung Electro-Mechanics	CAP, CERM, 22 µF, 10 V, +/- 20%, X5R, 0603	0603
8	C13	1	47000uF	DX-5R5H473U	Elna	CAP, Electric Double Layer, 47000 µF, 5.5 V, +80/-20%, TH	Horizontal D11.5x5mm
9	C15	1	1uF	C1005X5R0J105M	TDK	CAP, CERM, 1 µF, 6.3 V, +/- 20%, X5R, 0402	0402
10	D1, D2, D3, D4	4	20V	MBR0520LT1G	ON Semiconductor	Diode, Schottky, 20 V, 0.5 A, SOD-123	SOD-123
11	D5	1	4.7V	BZT52C4V7T-7	Diodes Inc.	Diode, Zener, 4.7 V, 300 mW, SOD-523	SOD-523
12	J1, J6, J7, J8, J9, J10, J13, J14, J15	9		90120-0122	Molex	Header, 100mil, 2x1, Tin, TH	Header 2x1
13	J2, J4, J5, J11	4		61300311121	Wurth Elektronik	Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH
14	J3	1		ED120/2DS	On-Shore Technology	TERMINAL BLOCK 5.08MM VERT 2POS, TH	TERM_BLK, 2pos, 5.08mm
15	J12	1		S2B-PH-SM4-TB(LF)(SN)	JST Manufacturing	Header (shrouded), 2mm, 2x1, R/A, SMT	Header, 2x1, 2mm, R/A
16	JP1, JP2	2		CRD-081413-A-G	Major League Electronics	Receptacle, 2.54 mm, 10x2, Gold, TH	Receptacle, 2.54 mm, 10x2, TH
17	L1	1	4.7uH	EPL3015-472MLB	Coilcraft	Inductor, Shielded, Ferrite, 4.7 µH, 1.2 A, 0.14 ohm, SMD	Inductor, 3x1.55x3mm
18	L2	1	22uH	LPS4018-223MLB	Coilcraft	Inductor, Shielded Drum Core, Ferrite, 22 µH, 0.83 A, 0.36 ohm, SMD	LPS4018
19	L3	1	10uH	LPS4018-103MLB	Coilcraft	Inductor, Shielded Drum Core, Ferrite, 10 µH, 1.25 A, 0.2 ohm, SMD	LPS4018
20	R1, R20	2	1.00Meg	CRCW06031M00FKEA	Vishay-Dale	RES, 1.00 M, 1%, 0.1 W, 0603	0603
21	R2	1	110k	CRCW0603110KFKEA	Vishay-Dale	RES, 110 k, 1%, 0.1 W, 0603	0603
22	R5, R8, R15, R16, R21, R22, R23	7	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
23	R11	1	374k	CRCW0603374KFKEA	Vishay-Dale	RES, 374 k, 1%, 0.1 W, 0603	0603
24	R12	1	7.32Meg	CRCW06037M32FKEA	Vishay-Dale	RES, 7.32 M, 1%, 0.1 W, 0603	0603
25	R13, R14	2	8.25Meg	CRCW06038M25FKEA	Vishay-Dale	RES, 8.25 M, 1%, 0.1 W, 0603	0603
26	R17	1	5.62Meg	CRCW06035M62FKEA	Vishay-Dale	RES, 5.62 M, 1%, 0.1 W, 0603	0603
27	R18	1	4.53Meg	CRCW06034M53FKEA	Vishay-Dale	RES, 4.53 M, 1%, 0.1 W, 0603	0603
28	R19	1	4.75Meg	CRCW06034M75FKEA	Vishay-Dale	RES, 4.75 M, 1%, 0.1 W, 0603	0603
29	SH-J1, SH-J2, SH-J4, SH-J5, SH-J6, SH-J7, SH-J9, SH-J10, SH-J11, SH-J14	10	1x2	969102-0000-DA	3M	Shunt, 100mil, Gold plated, Black	Shunt
30	U1	1		TPS61220DCKR	Texas Instruments	LOW INPUT VOLTAGE STEP-UP CONVERTER IN 6 PIN SC-70 PACKAGE, DCK0006A	DCK0006A
31	U2, U3, U5, U6	4	1.5V	KXOB22-04X3L	IXYS	MONOCRYSTALLINE SOLAR CELL, 22MM X 7MM, SMD	Solar Cell, 22x1.8x7mm
32	U4	1		BQ25570RGRR	Texas Instruments	Ultra Low Power Harvester Power Management IC with Boost Charger, and Nano-Powered Buck Converter, RGR0020A	RGR0020A
33	C5, C11, C12, C14	0	100uF	C1210C107M9PACTU	Kemet	CAP, CERM, 100 µF, 6.3 V, +/- 20%, X5R, 1210	1210
34	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	N/A
35	R3, R4	0	0	ERJ-3GEY0R00V	Panasonic	RES, 0, 5%, 0.1 W, 0603	0603
36	R6, R7, R9, R10	0	0	CRCW08050000Z0EA	Vishay-Dale	RES, 0, 5%, 0.125 W, 0805	0805

6.3 PCB Layout Recommendations

Layout Guidelines

As for all switching power supplies, the PCB layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost charger and buck converter could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitors as well as the inductors should be placed as close as possible to the IC. For the boost charger, first priority are the output capacitors, including the 0.1uF bypass capacitor (CBYP), followed by CSTOR, which should be placed as close as possible between VSTOR, pin 19, and VSS, pin 1. Next, the input capacitor, CIN, should be placed as close as possible between VIN_DC, pin 2, and VSS, pin 1. Last in priority is the boost charger's inductor, L1, which should be placed close to LBOOST, pin 20, and VIN_DC, pin 2. For the buck converter, the output capacitor COUT should be placed as close as possible between VOUT, pin 14, and VSS, pin 15. The buck converter inductor (L2) should be placed as close as possible between the switching node LBUCK, pin 16, and VOUT, pin 14. It is best to use vias and bottom traces for connecting the inductors to their respective pins instead of the capacitors.

To minimize noise pickup by the high impedance voltage setting nodes (VBAT_OV, OK_PROG, OK_HYST, VOUT_SET), the external resistors should be placed so that the traces connecting the midpoints of each divider to their respective pins are as short as possible. When laying out the non-power ground return paths (for example, from resistors and CREF), it is recommended to use short traces as well, separated from the power ground traces and connected to VSS pin 15. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. The PowerPAD should not be used as a power ground return path.

The remaining pins are either NC pins that should be connected to the PowerPAD as shown below or digital signals with minimal layout restrictions. See the EVM user's guide for an example layout (SLUUAA7).

In order to maximize efficiency at light load, the use of voltage level setting resistors > 1 MΩ is recommended. In addition, the sample and hold circuit output capacitor on VREF_SAMP must hold the voltage for 16s. During board assembly, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors/capacitors and/or from one end of a resistor/capacitor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed components. Therefore, it is highly recommended that no ground planes be poured near the voltage setting resistors or the sample and hold capacitor. In addition, the boards must be carefully cleaned, possibly rotated at least once during cleaning, and then rinsed with de-ionized water until the ionic contamination of that water is well above 50 MOhm. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced to at least 5X below the measured ionic contamination.

Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

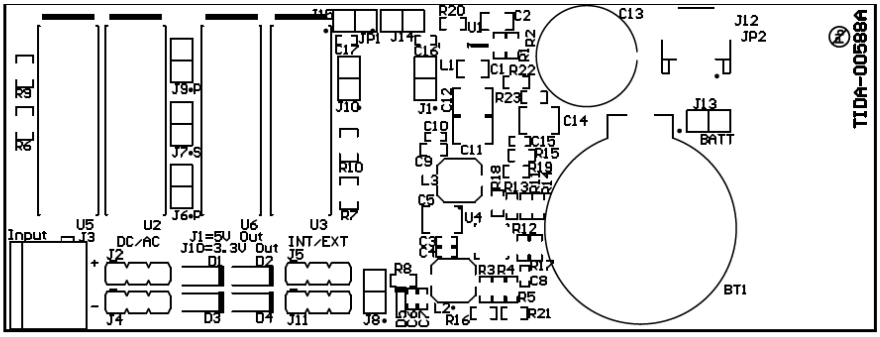
Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

6.4 Layout Prints

To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/TIDA-00588



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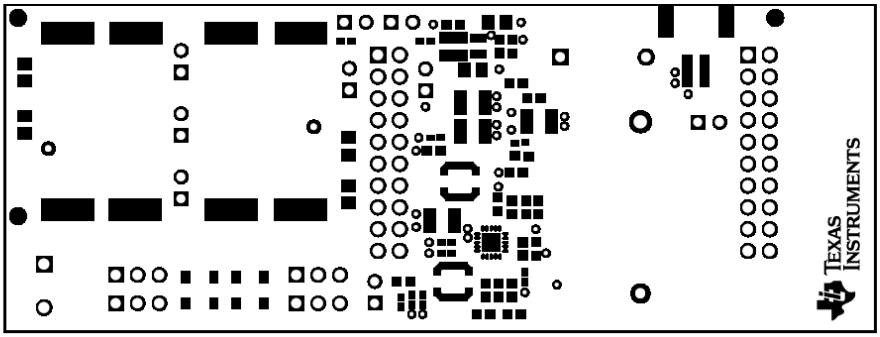
PLOT NAME = Top Overlay	GENERATED : 6/4/2015 8:36:42 AM		TEXAS INSTRUMENTS



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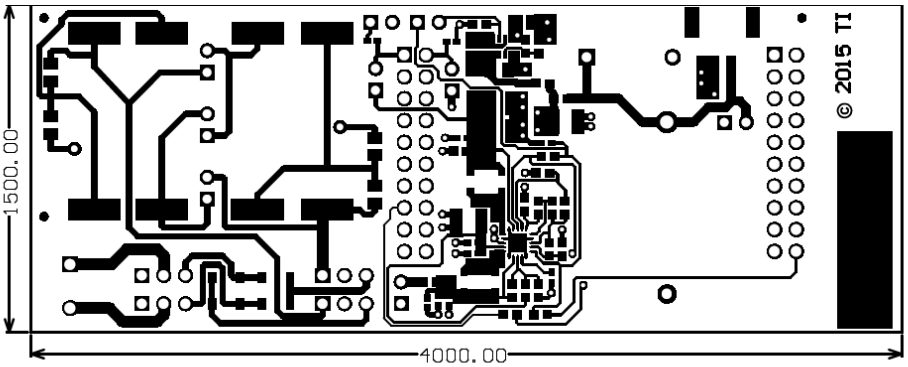

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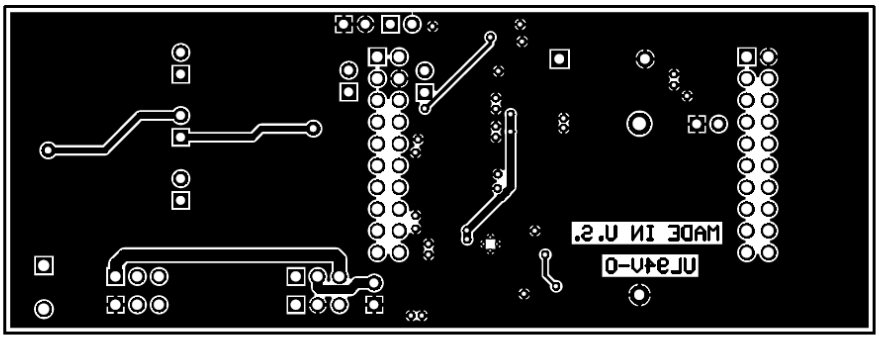

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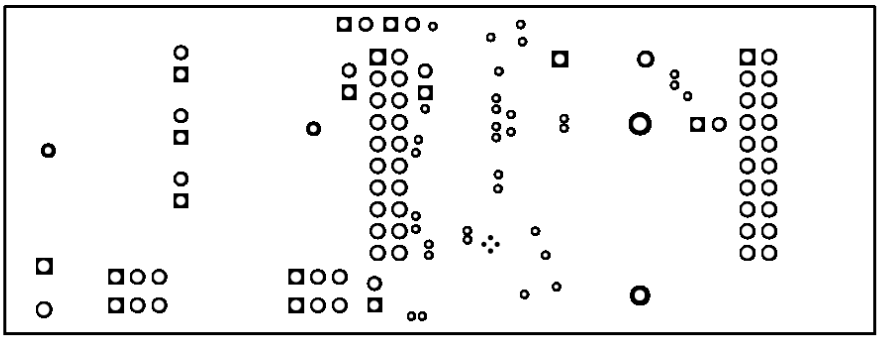

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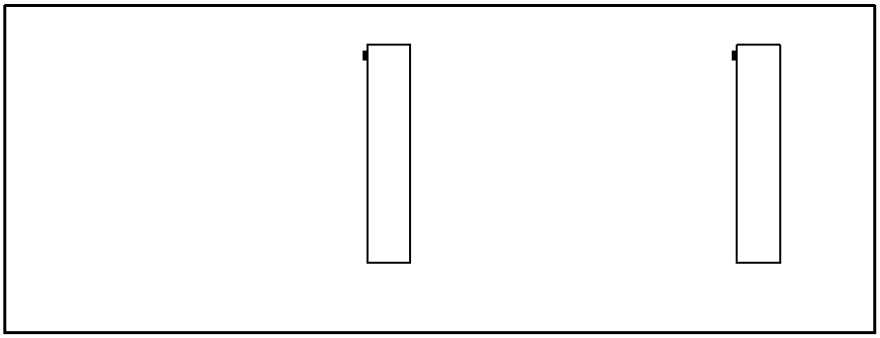

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PLOT NAME = Bottom Overlay	GENERATED : 6/4/2015 8:36:46 AM		TEXAS INSTRUMENTS

6.5 Booster Pack Pins

The Booster Pack pin configuration is in the table below

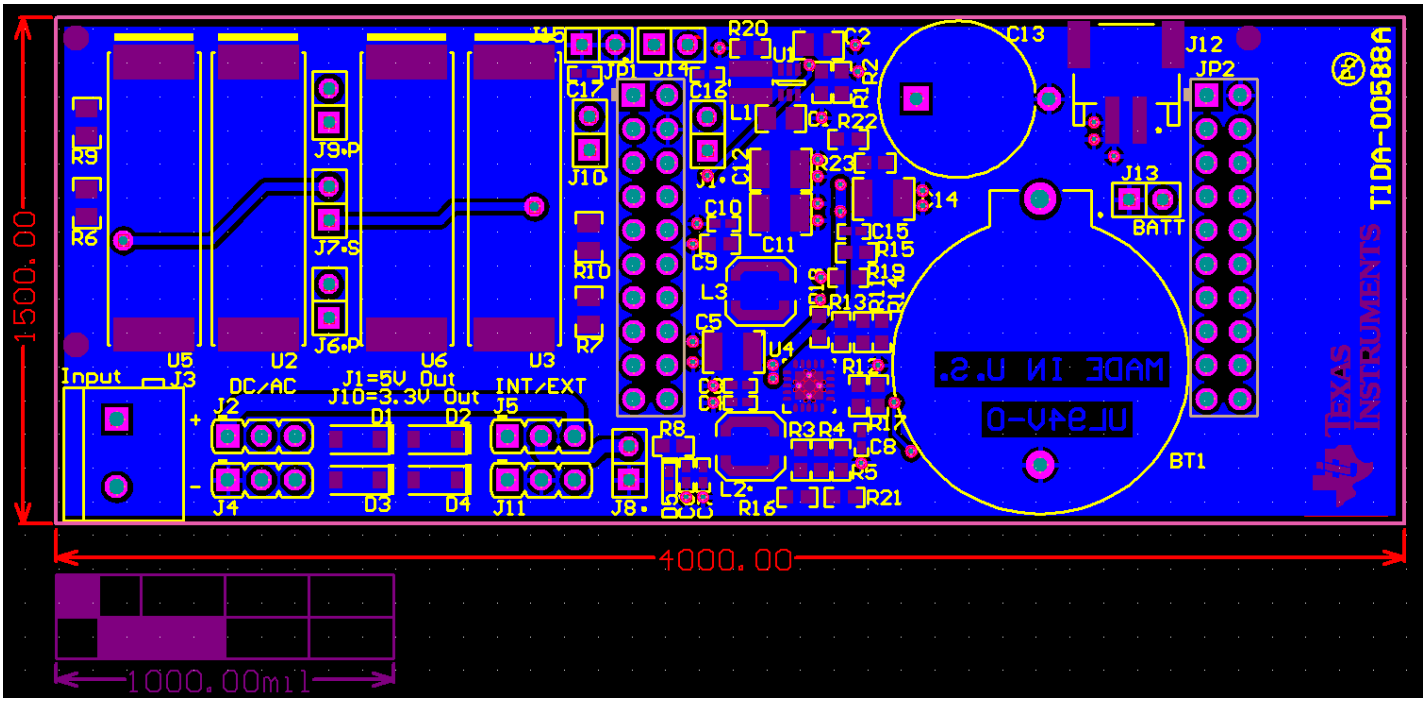
Energy Harvester Booster Pack 40Pin

Pin	J29	Pin Name	Function	IC Pin #	Pin	J29	Pin Name	Function	IC Pin #
1	A1	3.3V_Main			2	C1	5V		
3	A2	Analog In			4	C2	GND		
5	A3	UART/RX			6	C3			
7	A4	UART/TX			8	C4			
9	A5	GPIO			10	C5			
11	A6	Analog In			12	C6			
13	A7	SPI CLK			14	C7			
15	A8	GPIO	VBAT_OK		16	C8			
17	A9	I2C/SCL			18	C9			
19	A10	I2C/SDA			20	C10			

Pin	J30	Pin Name	Function	IC Pin #	Pin	J30	Pin Name	Function	IC Pin #
1	D20				2	B20	GND		
3	D19				4	B19	PWM/GPIO		
5	D18				6	B18	SPI CS/GPIO		
7	D17				8	B17	GPIO		
9	D16				10	B16	RESET	RST	
11	D15				12	B15	SPI/MOSI		
13	D14				14	B14	SPI/MISO		
15	D13				16	B13	SPI/CS/DISPLAY		
17	D12				18	B12	SPI/CS/Other		
19	D11				20	B11	GPIO	VOUT_EN	

6.6 Altium Project

To download the Altium project files for each board, see the design files at http://www.ti.com/tool/TIDA-00588



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