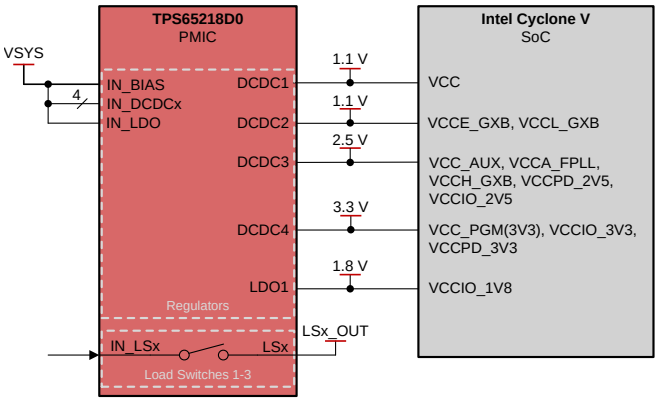
Test Report: TIDA-00606

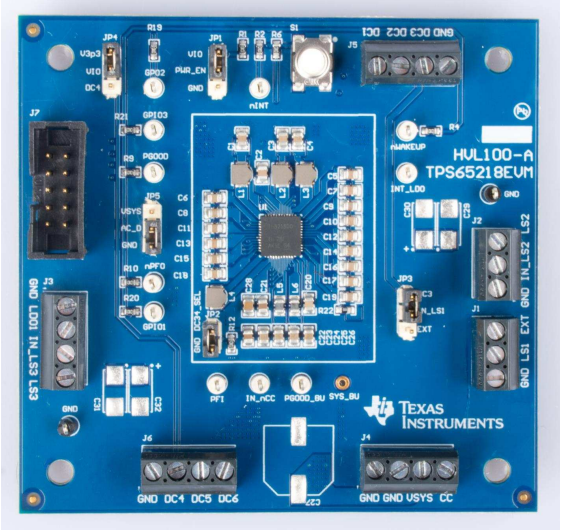
Powering the Intel® Cyclone® V SoC With Power Management IC Reference Design

Description

This TPS65218D0-based reference design is a compact, integrated power solution for the Intel® Cyclone® V (-E, -GX, and -GT) SoC. This design showcases TPS65218D0 as an all-in-one PMIC used to supply the five rails needed for powering the Cyclone® V SoC. The total board area needed for TPS65218D0, including passive components, to supply the five power rails to the Cyclone® V is just 1.594 in^2.

The TPS65218D0 has the flexibility to support either DDR3L or DDR3 memory. This power management IC can be run from a single 5-V supply or from a single cell Li-Ion battery. This design is ensured to operate across an industrial temperature range (-40°C to +105°C).





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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1 lists the names of the Cyclone V (-E, -GT, -GX) power supply rails, the voltage required for each rail, the maximum current capability of the TPS65218D0 for the corresponding rail, and the pin or rail name of the connection at the TPS65218D0 device.

Table 1. Voltage and Current Requirements

PARAMETER	VOLTAGE (V)	CURRENT (A)	TPS65218D0 PIN OR RAIL NAME
V_{IN}	3.3 – 5	—	IN_BIAS, IN_DCDCx, IN_LDO1
VCC	1.1	1.8	DCDC1
VCCE_GXB	1.1	1.8	DCDC2
VCCL_GXB	1.1		
VCC_AUX	2.5	1.8	DCDC3
VCCA_FPLL	2.5		
VCCH_GXB	2.5		
VCCPD_2V5	2.5		
VCCIO_2V5	2.5		
VCC_PGM(3V3)	3.3	1.6	DCDC4
VCCIO_3V3	3.3		
VCCPD_3V3	3.3		
VCC_IO1V8	1.8	0.4	LDO1

1.2 Required Equipment

- TPS65218EVM-100 evaluation module
- IPG-UI software
- TPS65218D0 sample IC
- BOOSTXL-TPS65218 socketed EVM (optional)

1.3 Design Considerations

The TPS65218D0 operates over a range of input voltages from 2.7 V to 5.5 V, such that the system can be powered from a 5-V, line-powered supply or from a nominal 3.6-V battery supply. Figure 1 shows the block diagram of the power connections in the system. The sequence order of each rail is circled in the diagram.

Figure 1. Cyclone V Power Supply Diagram

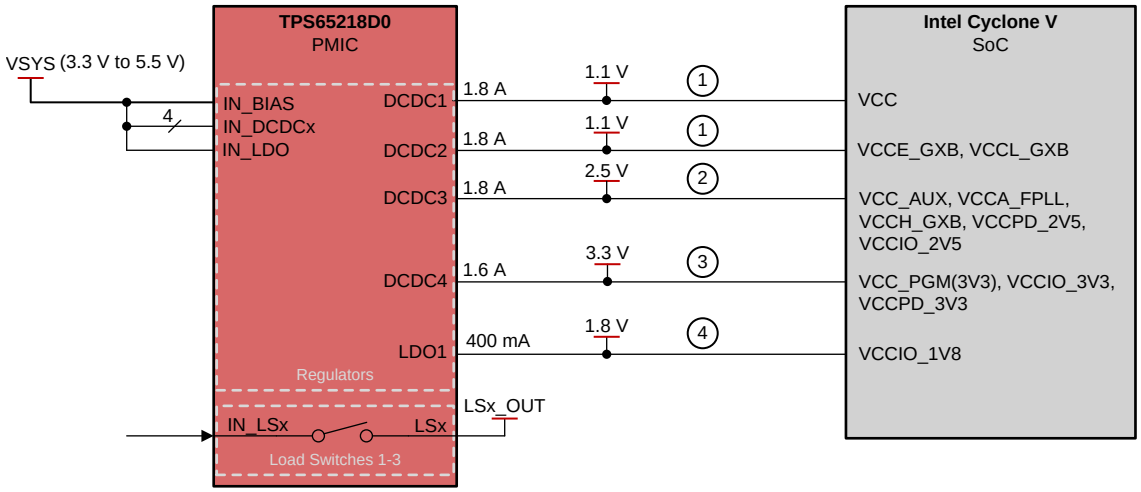


Table 2 lists the voltage settings required for the TPS65218D0 to power the Intel Cyclone V properly.

Table 2. Voltage Settings

Cyclone V Supply Rail(s)	TPS65218D0 Regulator	Voltage (V)	Register Address (Name)	Register Value
VCC	DCDC1	1.1	0x16 (DCDC1)	0x99
VCCE_GXB , VCCL_GXB	DCDC2	1.1	0x17 (DCDC2)	0x99
VCC_AUX, VCCA_FPLL, VCCH_GXB, VCCPD_2V5, VCCIO_2V5	DCDC3	2.5	0x18 (DCDC3)	0xAD
VCC_PGM(3V3), VCCPD_3V3, VCCIO_3V3	DCDC4	3.3	0x19 (DCDC4)	0xB2
VCC_IO1V8	LDO1	1.8	0x1B (LDO1)	0x1F

The same block diagram applies to a system using a nominal 3.6-V battery as the supply. The battery voltage can drop to less than 3.3 V, but DCDC4 can still generate 3.3 V because it is a buck-boost regulator.

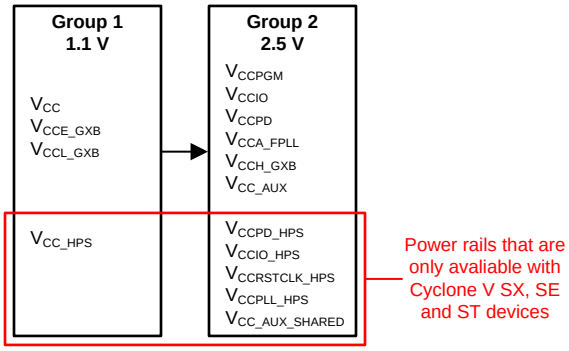
1.3.1 Intel® Cyclone® V Recommended Power Up/Down Sequencing

For reference, the sequencing requirements from the Intel Cyclone V data sheet and connection guideline documents are described in the following sections.

1.3.1.1 Cyclone V Power-On/Off Supply Sequencing

The recommended power-on sequencing is VCC, VCCE_GXB, VCCL_GXB together in the first group, then the other power rails as shown in Figure 2. Ramp up the power rails of Group 1 to 80% of their full rail before Group 2 starts.

Figure 2. Power-Up Sequencing for Cyclone V FPGAs



- Intel recommends connecting the VCC pins to a low-noise switching regulator. VCCE_GXBL and VCCL_GXBL can be supplied power from the same regulator as VCC with a proper isolation filter.
- Connect VCCA_PLL to a 2.5V low noise switching power supply through a proper isolation filter. Intel states that this rail may be shared with VCC_AUX and VCCH_GXBL pins.
  - With a proper isolation filter, these pins may be sourced from the same regulator as VCCIO, VCCPD, and VCCPGM when each of these power supplies require 2.5V.
- VCCIO pins can be connected to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, 3.0V or a 3.3V supply. If the pins have the same voltage requirements as VCCPD and VCCPGM, they can be tied to the same regulator.
- Intel recommends increasing VCCE_GXBL and VCCL_GXBL from 1.1V to 1.2V for systems which require full compliance to the CPRI 4.9G and PCI Express Gen 2 transmit jitter specification
- All Ground pins must be connected to the PCB ground plane.

Refer to the Intel Cyclone V Device Family Connection Guidelines for a detailed description of connection diagrams for various Cyclone V applications.

1.3.2 TPS65218D0 Wake-up and Power Sequencing

The TPS65218D0 has a pre-defined power-up / power-down sequence which may need to be adjusted for each different SoCs, processors, or FPGAs. Re-programming the nonvolatile EEPROM memory of the TPS65218D0 device with I^2C control allows the user to change the sequence order and timing to match the target SoC, processor, or FPGA.

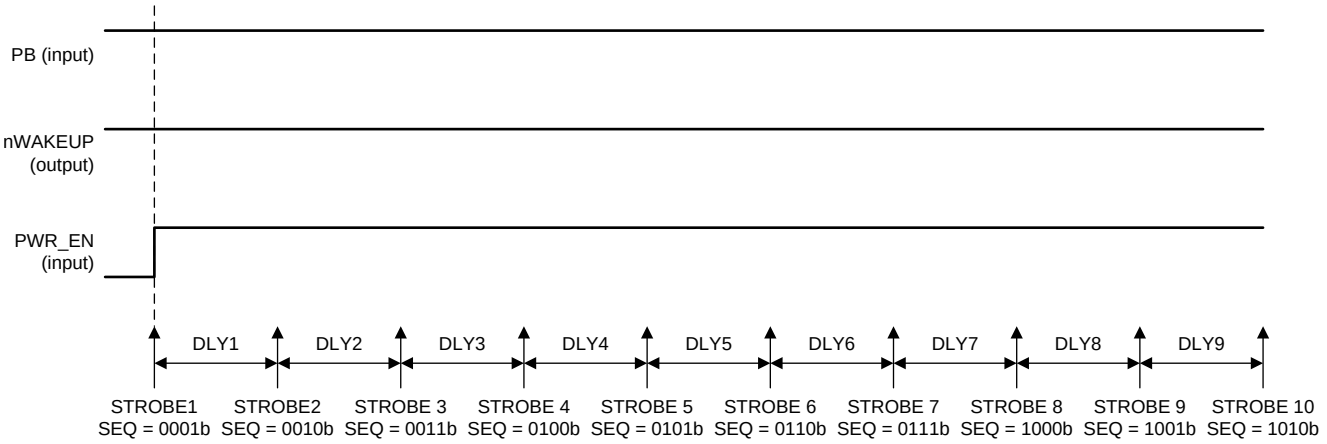
The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled. A rail can be assigned to only one strobe, but multiple rails can be assigned to the same strobe. The delay times in-between strobes are selectable between 2 ms and 5 ms.

1.3.2.1 General Power-Up Sequencing

When the power-up sequence initiates, STROBE1 occurs, and any rail assigned to this strobe is enabled.

After a delay time of DLY1, STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes occur and all DLYx times execute. Strobe assignments and delay times are defined in the SEQx registers, and are changed under I^2C control. Figure 3 shows a timing diagram detailing the power sequence when PWN_EN is the power-up event leaving the SUSPEND state. For further information on power up/down sequence, please consult the TPS65218D0 data sheet. Power-down sequencing follows the reverse order of power-up sequencing.

Figure 3. TPS65218D0 Power-Up from SUSPEND State (PWR_EN Set High)



1.3.2.2 TPS65218D0 Adjusted Sequencing for Intel® Cyclone® V

Table 3 lists the strobe assignments required for the TPS65218D0 to power the Intel Cyclone V properly. The delay (DLY1-9) between each strobe can also be adjusted in registers 0x20 (SEQ1) and 0x21 (SEQ2, bit 0) and multiplied by a factor of 1 or 10 (SEQ2, bit 7). Each bit in SEQ1 and bit 0 of SEQ2 can be set to 0b for a delay of 2 ms or set to 1b for a delay of 5 ms. Bit 7 of SEQ2 can be set to 0b for a factor of 1x or set to 1b for a factor of 10x. For this design, all delays will be kept at the defaults of 2 ms with a delay factor of 1x. As a result, the data in both registers, 0x20 and 0x21, will be 0x00.

Table 3. Strobe Assignments

Cyclone V Supply Rail(s)	TPS65218D0 Regulator	Strobe #	Register Address (Name)	Register Value
VCC	DCDC1	3	0x22 (SEQ3)	0x33
VCCE_GXB, VCCL_GXB	DCDC2	3		
VCC_AUX, VCCA_FPLL, VCCH_GXB, VCCPD_2V5, VCCIO_2V5	DCDC3	5	0x23 (SEQ4)	0x75
VCC_PGM(3V3), VCCPD_3V3, VCCIO_3V3	DCDC4	7		
VCC_IO1V8	LDO1	8	0x25 (SEQ6)	0xA8

2 Testing and Results

2.1 Efficiency Graphs

Figure 4 shows the efficiency curve for DCDC1, set to output a voltage of 1.1 V for the VCC rail.

Figure 5 shows the efficiency curve for DCDC2, set to output a voltage of 1.1 V for the VCCE_GXB and VCCL_GXB rails.

Figure 4. DCDC1 Efficiency vs Load Current, T_A = 25 °C

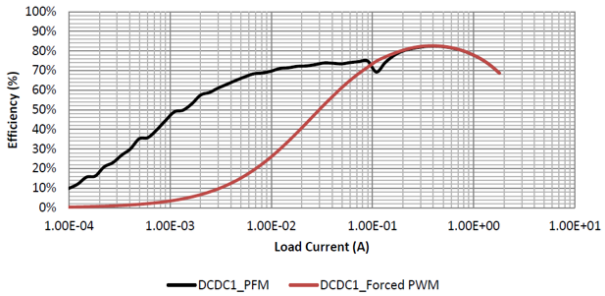


Figure 5. DCDC2 Efficiency vs Load Current, T_A = 25 °C

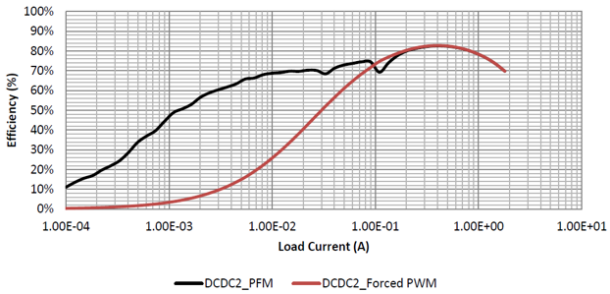


Figure 6 shows the efficiency curve for DCDC3, set to output a voltage of 2.5 V for the VCC_AUX, VCCA_FPLL, VCCH_GXB, VCCPD_2V5, and VCCIO_2V5 rails.

Figure 7 shows the efficiency curve for DCDC4, set to output a voltage of 3.3 V for the VCC_PGM, VCCPD_3V3, and VCCIO_3V3 rails.

Figure 6. DCDC3 Efficiency vs Load Current, T_A = 25 °C

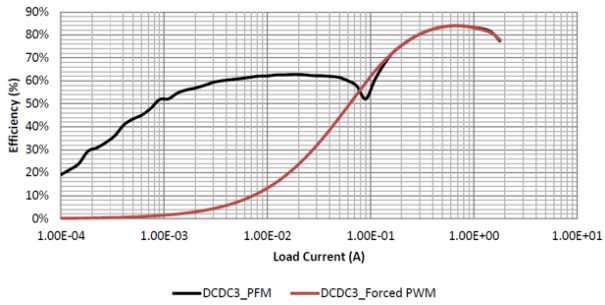
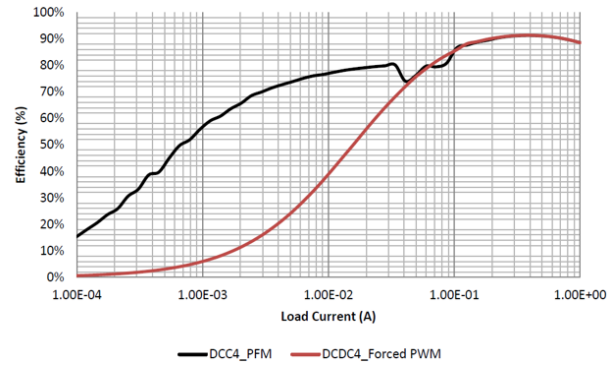


Figure 7. DCDC4 Efficiency vs Load Current, T_A = 25 °C



2.2 Load Regulation

Figure 8 shows the load regulation plot for DCDC1.

Figure 9 shows the load regulation plot for DCDC2.

Figure 8. DCDC1 Load Regulation, T_A = 25 °C

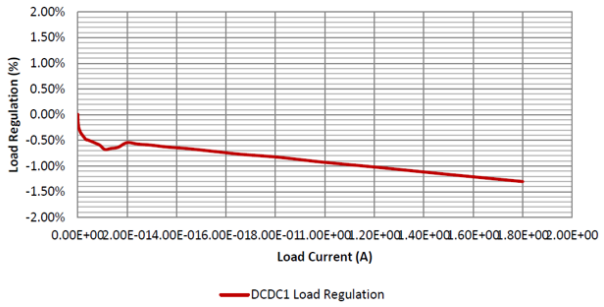


Figure 9. DCDC2 Load Regulation, T_A = 25 °C

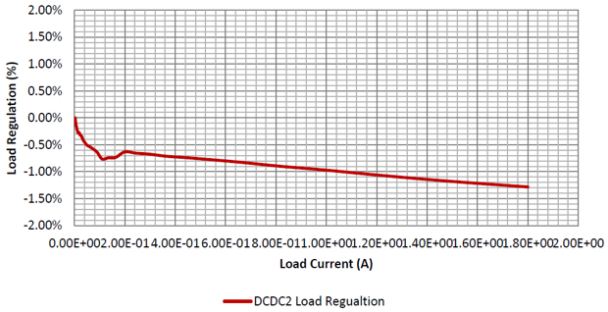


Figure 10 shows the load regulation plot for DCDC3.

Figure 11 shows the load regulation plot for DCDC4.

Figure 10. DCDC3 Load Regulation, T_A = 25 °C

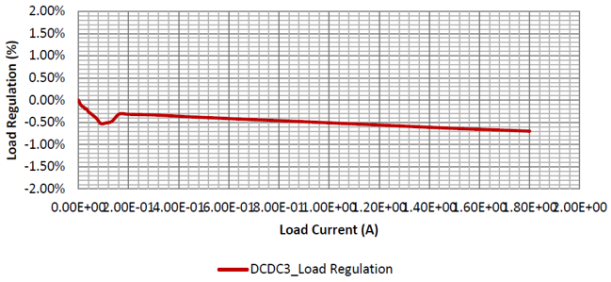
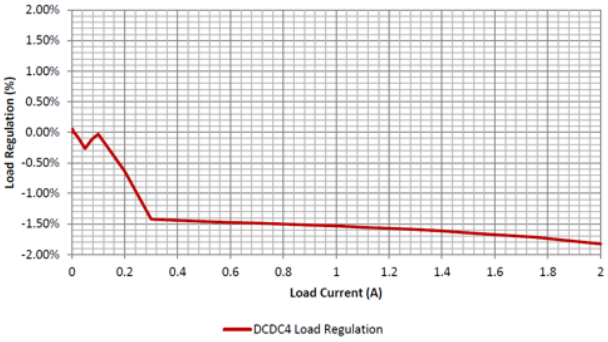


Figure 11. DCDC4 Load Regulation, T_A = 25 °C



3 Waveforms

3.1 Start-up Sequence

Figure 12 and Figure 13 show the start-up (or power-up) sequence of the TPS65218D0 rails programmed for the Cyclone V with no load applied.

Figure 12. Power-Up Sequence (No Load) Voltage and Timing Waveforms (1 of 2)

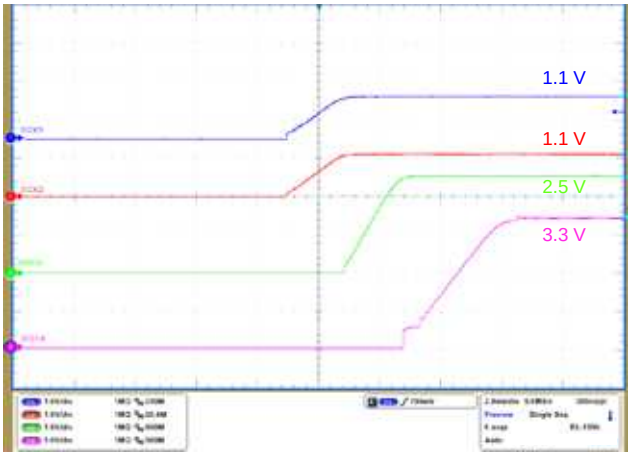
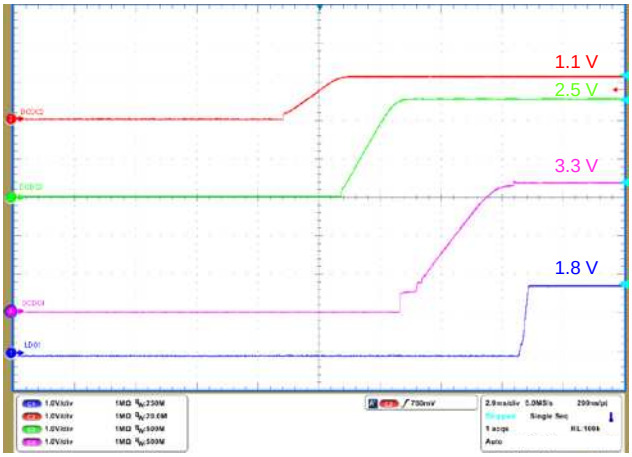


Figure 13. Power-Up Sequence (No Load) Voltage and Timing Waveforms (2 of 2)



3.2 Output Voltage Ripple

Figure 14 shows the measured output voltage ripple for DCDC1 at the maximum typical load (PWM mode) of the VCC rail. Figure 15 shows the measured output voltage ripple for DCDC1 in PFM mode with a light load applied.

Figure 14. DCDC1 Output Voltage Ripple (Max Load, PWM)

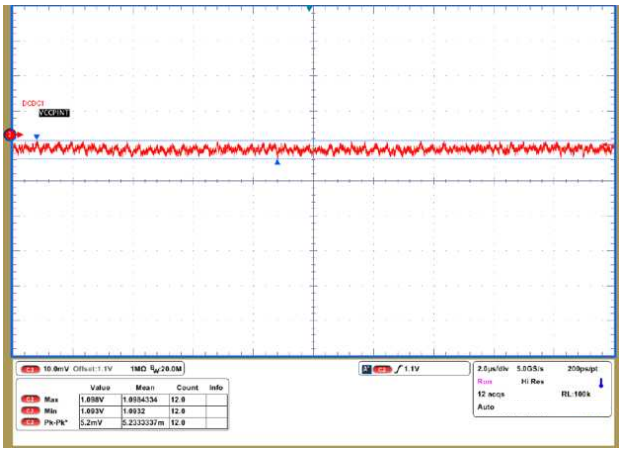


Figure 15. DCDC1 Output Voltage Ripple (Light Load, PFM)

Figure 16 shows the measured output voltage ripple for DCDC2 at the maximum typical load (PWM mode) of the VCCE_GXB and VCCL_GXB rails. Figure 17 shows the measured output voltage ripple for DCDC2 in PFM mode with a light load applied.

Figure 16. DCDC2 Output Voltage Ripple (Max Load, PWM)

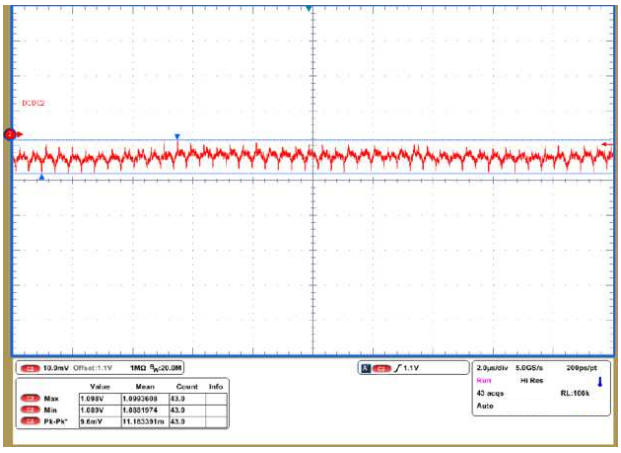


Figure 17. DCDC2 Output Voltage Ripple (Light Load, PFM)

Figure 18 shows the measured output voltage ripple for DCDC3 at the maximum typical load (PWM mode) of the VCC_AUX, VCCA_FPLL, VCCH_GXB, VCCPD_2V5, and VCCIO_2V5 rails. Figure 19 shows the measured output voltage ripple for DCDC3 in PFM mode with a light load applied.

Figure 18. DCDC3 Output Voltage Ripple (Max Load, PWM)

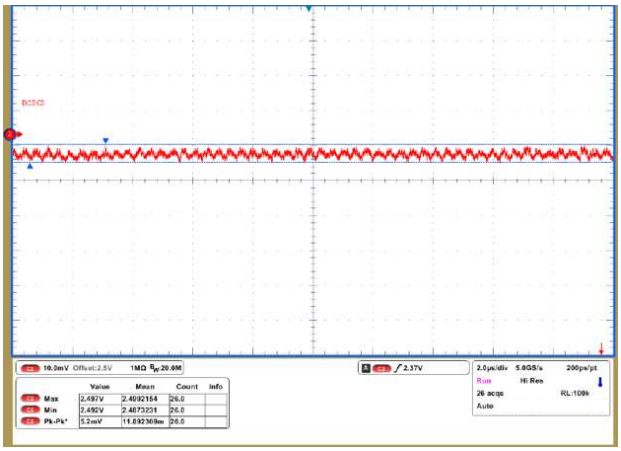


Figure 19. DCDC3 Output Voltage Ripple (Light Load, PFM)

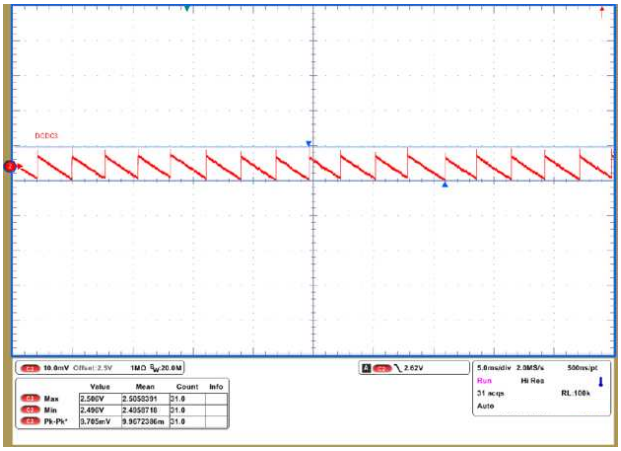
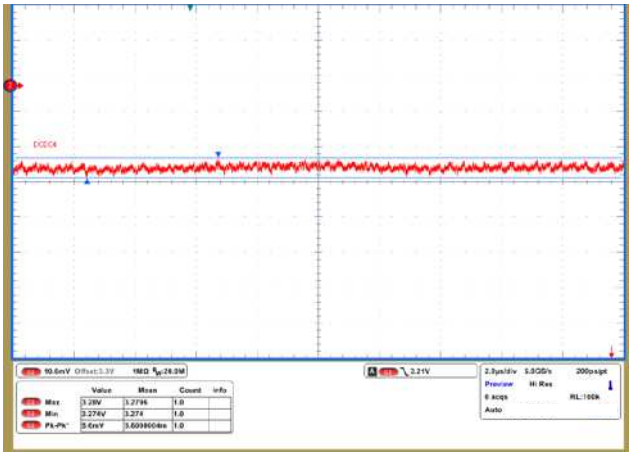


Figure 20 shows the measured output voltage ripple for DCDC4 at the maximum typical load (PWM mode) of theVCC_PGM, VCCPD_3V3, and VCCIO_3V3 rails.

Figure 20. DCDC4 Output Voltage Ripple (Max Load, PWM)



3.3 Load Transients

Figure 21 shows the measured load transient response for DCDC1 for a step from 10 mA to 850 mA.

Figure 22 shows the measured load transient response for DCDC2 for a step from 10 mA to 875 mA.

Figure 21. DCDC1 Load Transient Response (10 mA to 850 mA)

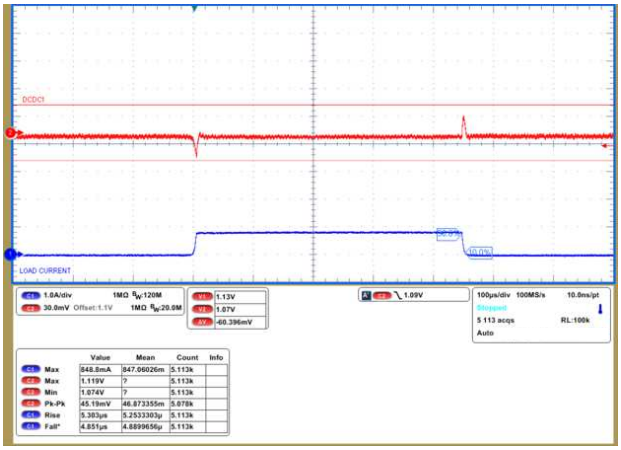


Figure 22. DCDC2 Load Transient Response (10 mA to 875 mA)

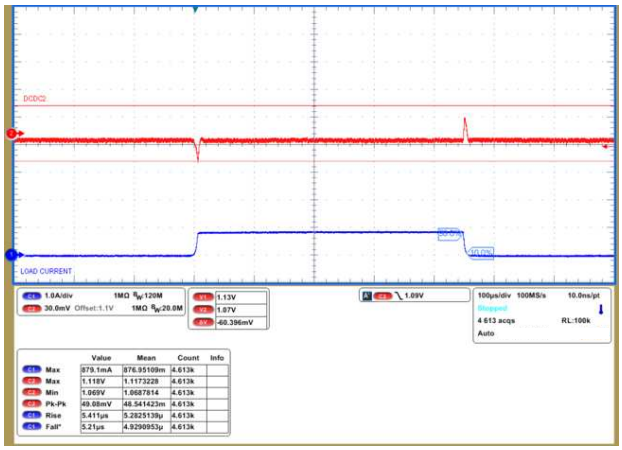
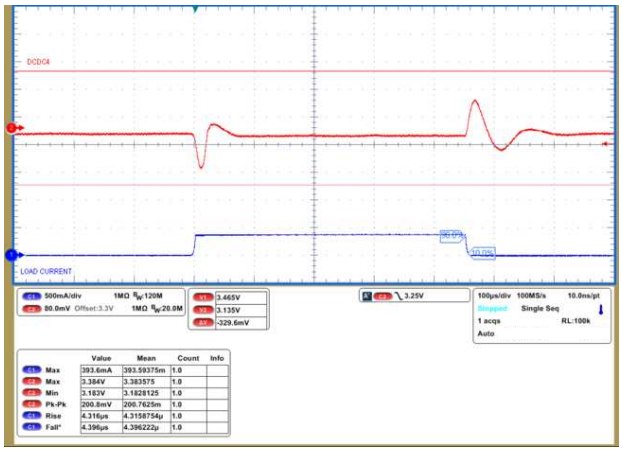


Figure 23 shows the measured load transient response for DCDC3 for a step from 10 mA to 975 mA.

Figure 24 shows the measured load transient response for DCDC4 for a step from 10 mA to 400 mA.

Figure 23. DCDC3 Load Transient Response (50 mA to 624 mA)

Figure 24. DCDC4 Load Transient Response (50 mA to 300 mA)



4 Next Steps

After reviewing this test report, the next steps towards building a design using the TPS65218D0 PMIC for a Intel Cyclone V SoC are simple. The EEPROM of TPS65218D0 samples can be re-programmed using a socketed BOOSTXL-TPS65218 BoosterPack EVM and an MSP430F5529 LaunchPad. The output voltage settings and sequencing outlined in this document are modified and re-programmed into the TPS65218D0 nonvolatile memory using the IPG-UI software.

The re-programmed TPS65218D0 sample is then soldered down onto the TPS65218EVM-100 board to evaluate the performance and obtain the same results captured in this documentation. If this documentation is sufficient to prove the TPS65218D0 PMIC will work in the final application, the re-programmed TPS65218D0 sample can be soldered directly into a prototype board and evaluated for use in the final application.

Although the scope of this document is limited to powering the Intel Cyclone V SoC, the TPS65218D0 device can be used to power a wide variety of SoCs, processors, and FPGAs using this same workflow.

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