TI Designs
Highly Integrated Power Reference Design for SSD's

TEXAS INSTRUMENTS

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Design Resources

TIDA-00719	Design Folder
LP8758	Product Folder

TI E2E™ Community

- Ask The Analog Experts
- Linear Regulators - Forum
- WEBENCH® Design Center

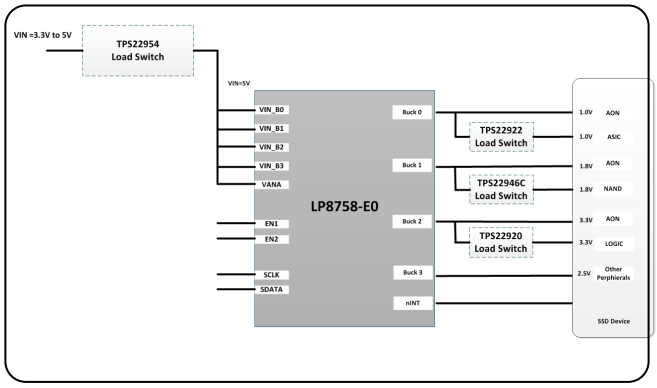
Design Features

- Programmable Output voltage ranges from 0.6V to 3.36V
- Four output voltage adjustable via I2C interface.
- Startup & Shutdown Programmable delays up to 15msec.
- Auto PWM-PFM and Forced-PWM
- Operations Maximum output current 4A per phase/output rail
- Output voltage Enable/Disable control

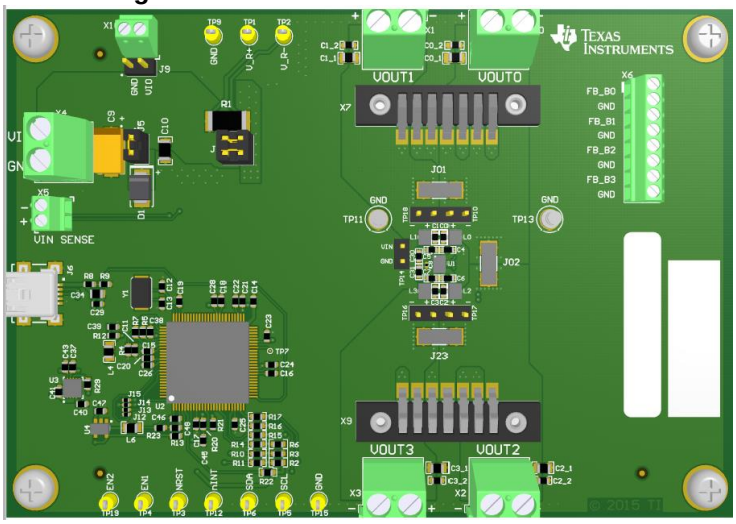
Featured Applications

- SSD Power Rails
- General DC-DC replacement
- Battery operated devices

High level Block Diagram



Board Image



1 System Description

This document features a highly configurable power management buck converter (LP8758-E0) showing the power rails for SSD's. The multi-buck solution shown can be easily reconfigured for other applications which need high output voltage accuracy and high peak currents.
The LP8758-E0 also allows startup and shutdown sequencing which is critical in terms of requirements from the SSD Application and also has the I2C control interface to disable/enable each of these rails independently.

In this design the output voltage is programmed for default output voltages of 1.0V,1.8V ,3.3V and 2.5V which are can be used to power different rails on the ASIC Core ,NAND Flash, ASIC Logic and other Peripherals. The maximum load current per rail can be as high as 4A each and the current limits can be as high as 5A.
This design also shows that load switches can be used if some of the rails need to be Always ON and can be powered via load switches such as TPS22946, TPS22922 etc.

Table 1 ASIC Voltages & Load Current Example

ASIC VOLTAGE	CURRENT LIMIT
1.0V	4A
1.8V	4A
3.3V	4A
2.5V	4A

1.1 TI Design Overview

This TI Design covers the ease of use power management solution for SSD ASIC Core and NAND Flash which needs multiple rails and has very tight requirements on the output voltage accuracy and ripple voltage.
Also the power rails require DVS method to reduce the average power consumption in embedded systems (i.e. ASICs, SoCs, processors/DSPs, FPGAs) this is accomplished by reducing the switching losses of the system by selectively reducing the core voltage based on the need of the system.

Table 2 Design Parameters

DESIGN PARAMETERS	VALUE
Input voltage	5V
Multiple Output voltages	1.0V,1.8V,3.3V,2.5V

Block Diagram

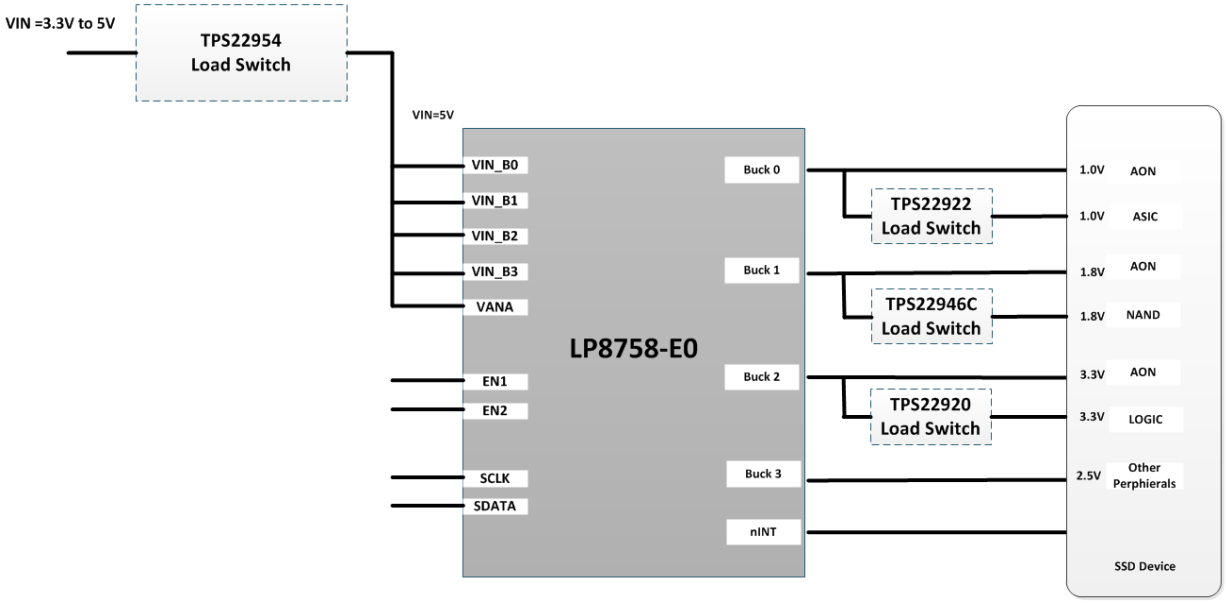


Figure 1 Comprehensive block diagram

2 Component Selection

This TI design has the following components

Power Management Buck Converter: LP8758-E0 Four Output Step down DC-DC Regulator

Parameters taken into account when selecting the buck regulator:

- Low Iq in Shutdown mode
- High accuracy in steady state
- Startup & Shutdown sequencing capability.
- Vout Range with DVS Control
- Small Solution Size
- Auto PWM-PFM and Forced-PWM Operations
- Programmable Output Voltage Slew-Rate from 30mV/µsec to 0.47mV/µsec

Alternative parts with similar functionality

- LP8754 similar functionality with additional phases

2.1 LP8758

The LP8758 is a high-efficiency, high-performance power supply device with four step-down DC-DC converter cores. The cores are configured for a four single-phase configuration. The device delivers 0.5-V to 3.36-V regulated voltage rails from 2.5-V to 5.5-V battery.

There are two modes of operation for the converter, depending on the output current required: Pulse-Width Modulation (PWM) and Pulse-Frequency Modulation (PFM). The converter operates in PWM mode at high load currents of approximately 400 mA or higher. Lighter output current loads will cause the converter to automatically switch into PFM mode for reduced current consumption and a longer battery life when Forced PWM mode is disabled.

Additional features include soft-start, under voltage lockout, overload protection, thermal warning, and thermal shutdown.

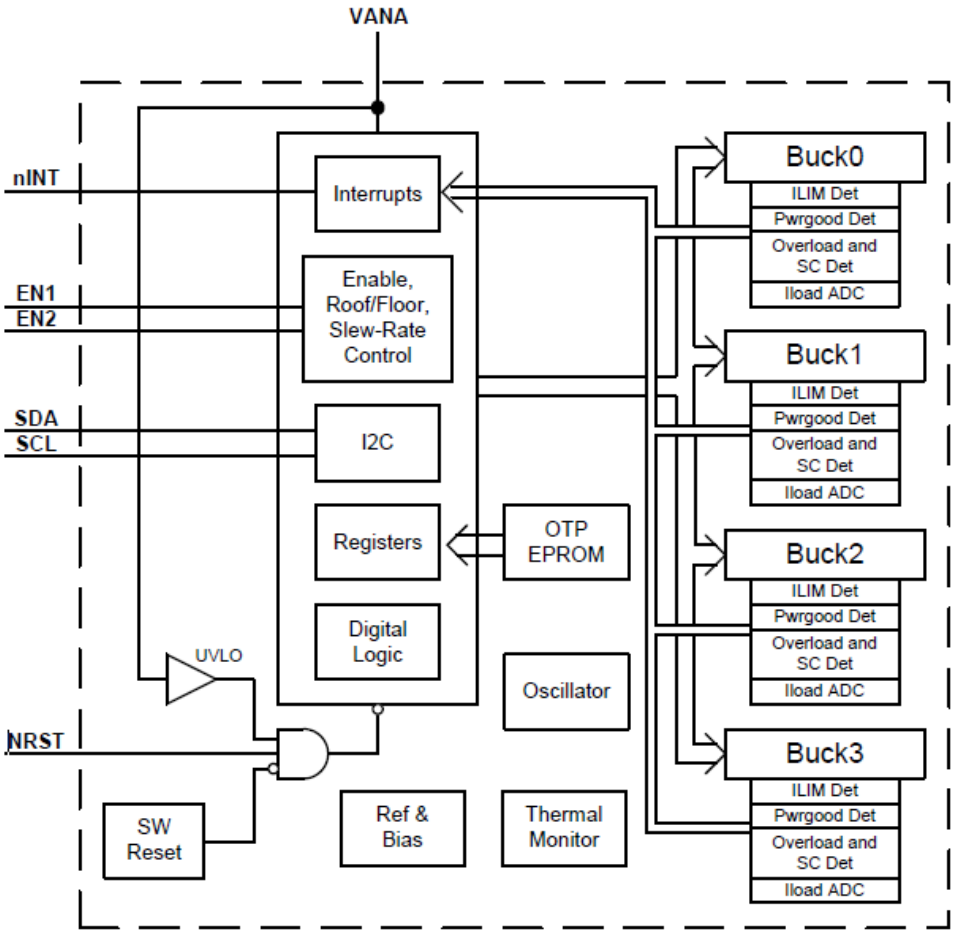


Figure 2: LP8758 Functional Block Diagram

3 System design and component selection

The following system considerations apply only for the conditions of this design. For different conditions it is essential to verify the ratings and operating conditions on the datasheets of the parts mentioned in this design. If the parameters does not fit the application consider one of the alternative parts on section 3 or perform and easy parametric search at http://www.ti.com

3.1 Input voltage consideration

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply should be well-regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition. The resistance of the input supply rail should be low enough that the input current transient does not cause too high drop in the LP8758 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP8758 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

3.2 Inductor & Input/output Capacitor selection consideration

3.2.1 Inductor Selection

DC bias current characteristics of inductors must be considered. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. DC bias curves should be requested from them as part of the inductor selection process. Minimum effective value of inductance to ensure good performance is 0.22 µH at 4 A bias current over the inductor's operating temperature range. The inductor's DC resistance should be less than 0.05 Ω for good efficiency at high current condition. The inductor AC loss (resistance) also affects conversion efficiency. Higher Q factor at switching frequency usually gives better efficiency at light load to middle loads

Table 3 Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	DIMENSIONS LxWxH (mm)	DCR (mΩ)
TOKO	DFE252010F-R33M	0.33 µH	2.5 x 2.0 x 1.0	16 (typ), 21 (max)
TDK	VLS252010HBX-R33M	0.33 µH	2.5 x 2.0 x 1.0	25 (typ), 31 (max)
TDK	VLS252010HBX-R47M	0.47 µH	2.5 x 2.0 x 1.0	29 (typ), 35 (max)
TDK	TFM2016GHM-0R47M	0.47 µH	2.0 x 1.6 x 1.0	46 (max)
TOKO	DFE322512C R47	0.47 µH	3.2 x 2.5 x 1.2	21 (typ), 31 (max)

3.2.2 Input Capacitor Selection

A ceramic input capacitor of 10 µF, 6.3 V is sufficient for most applications. Place the power input capacitor as close as possible to the VIN_Bx pin and PGND_Bx pin of the device. A larger value or higher voltage rating may be used to improve input voltage filtering. Use X7R or X5R types, do not use Y5V or F. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0402. Minimum effective input capacitance to ensure good performance is 1.9 µF per buck input at maximum input voltage DC bias including tolerances and over ambient temp range, assuming that there are at least 22 µF of additional capacitance common for all the power input pins on the system power rail.

Table 4 Recommended Power Input Capacitors (X5R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Murata	GRM188R60J106ME47	10 µF (20%)	0603	1.6 x 0.8 x 0.8	6.3 V

The input filter capacitor supplies current to the high-side FET switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low equivalent series resistance (ESR) provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with sufficient ripple current rating.
The VANA input is used to supply analog and digital circuits in the device. See recommended components from table below for VANA input supply filtering

Table 5 Recommended VANA Supply Filtering Components

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Samsung	CL03A104KP3NNNC	100 nF (10%)	0201	0.6 x 0.3 X 0.3	10 V
Murata	GRM033R61A104KE84	100 nF (10%)	0201	0.6 x 0.3 x 0.3	6.3 V

3.2.3 Output capacitors

Use ceramic capacitors, X7R or X5R types; do not use Y5V or F. DC bias voltage characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process. The output filter capacitor smooth's out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR and ESL to perform these functions. Minimum effective output capacitance to ensure good performance is 10 μ F per phase at the output voltage DC bias including tolerances and over ambient temp range. The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR}. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for selection process is at the switching frequency of the part.

A higher output capacitance improves the load step behavior and reduces the output voltage ripple as well as decreases the PFM switching frequency. For most 4-phase applications 4 x 22 μ F 0603 capacitors for COUT are suitable. Although a converter's loop compensation can be programmed to adapt to virtually several hundreds of microfarads C_{OUT}, it is preferable for C_{OUT} to be < 200 µF (4-phase configuration). Choosing higher than that is not necessarily of any benefit. Note that the output capacitor may be the limiting factor in the output voltage ramp, especially for very large (> 100 µF) output capacitors. For large output capacitors, the output voltage might be slower than the programmed ramp rate at voltage transitions, because of the higher energy stored on the output capacitance. Also at start-up, the time required to charge the output capacitor to target value might be
longer. At shutdown, if the output capacitor is discharged by the internal discharge resistor, more time is required to settle V_{OUT} down as a consequence of the increased time constant.

Table 6: Recommended Output Capacitors (X5R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	DIMENSIONS LxWxH (mm)	VOLTAGE RATING
Samsung	CL10A226MP8NUNE	22 µF (20%)	0603	1.6 x 0.8 x 0.8	10 V
Murata	GRM188R60J226MEA0	22 µF (20%)	0603	1.6 x 0.8 x 0.8	6.3 V

3.3 Output voltage configuration

The LP8758 is configured as 4 single phase buck regulator and the default output voltages are 1.0V, 1.8V, 3.3V and 2.5V.There is a startup delay of 0 msec set from the EN pin and this is for the following buck regulator 0 & 1 and 5 msec delay is set for buck regulator 2 & 3.The shutdown delay is set as 5 msec for buck regulator 0 & 1 and 0 msec for buck regulator 2 & 3.This can be modified as needed and the resolution of the delay is 1msec and maximum startup and shutdown delay is 15msec. In the LP8758-E0 Datasheet each buck has its independent control for current limit, slew rate, output voltage, startup and shutdown delay
The startup slew rate for the output voltage is set as 10mV/µsec and the current limits can be set from 1.5A to 5.0A according to the requirements from the SoC/Processor.

Table 7: Example Startup and Shutdown delay setting for Buck 0

Address: 0x12

D7	D6	D5	D4	D3	D2	D1	D0
BUCK0_SHUTDOWN_DELAY[3:0]				BUCK0_STARTUP_DELAY[3:0]			

Bits	Field	Type	Default	Description
7:4	BUCK0_ SHUTDOWN_ DELAY[3:0]	R/W	0000	Shutdown delay of BUCK0 from falling edge of ENx signal: 0000 - 0 ms 0001 - 1 ms ... 1111 - 15 ms
3:0	BUCK0_ STARTUP_ DELAY[3:0]	R/W	0000	Startup delay of BUCK0 from rising edge of ENx signal: 0000 - 0 ms 0001 - 1 ms ... 1111 - 15 ms

4 Power up Sequence

The power-up sequence for the LP8758 is as follows:

- VANA (and VIN_Bx) reach min recommended levels ($V_{(VANA)} > VANA_{UVLO}$).
- NRST is set to high level. This initiates Power-On-Reset (POR), OTP reading and enables the system I/O interface. The I2C host should allow at least 700 µs before writing or reading data to the LP8758.
- Device enters STANDBY-mode.
- The host can change the default register setting by I2C if needed.
- The regulator can be enabled/disabled by ENx pin(s) and by I2C interface

5 Layout guidelines

The high frequency and large switching currents of the LP8758 make the choice of layout important. Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation and can cause a good design to perform with less-than-expected results. With a range of output currents from milliamps to 10A and over, good power supply layout is much more difficult than most general PCB design. The following steps should be used as a reference to ensure the device is stable and maintains proper voltage and current regulation across its intended operating voltage and current range.

- Place CIN as close as possible to the VIN_Bx pin and the PGND_Bxx pin. Route the VIN trace wide and thick to avoid IR drops. The trace between the input capacitor's positive node and LP8758's VIN_Bx pin(s) as well as the trace between the input capacitor's negative node and power PGND_Bxx pin(s) must be kept as short as possible. The input capacitance provides a low-impedance voltage source for the switching converter. The inductance of the connection is the most important parameter of a local decoupling capacitor – parasitic inductance on these traces must be kept as tiny as possible for proper device operation.
- The output filter, consisting of Lx and COUTx, converts the switching signal at SW_Bx to the noiseless output voltage. It should be placed as close as possible to the device keeping the switch node small, for best EMI behavior. Route the traces between the LP8758's output capacitors and the load's input capacitors direct and wide to avoid losses due to the IR drop.
- Input for analog blocks (VANA and AGND) should be isolated from noisy signals. Connect VANA directly to a quiet system voltage node and AGND to a quiet ground point where no IR drop occurs. Place the decoupling capacitor as close to the VANA pin as possible. VANA must be connected to the same power node as VIN_Bx pins.
- If the processor load supports remote voltage sensing, connect the LP8758's feedback pins FB_Bx to the respective sense pins on the processor. The sense lines are susceptible to noise. They must be kept away from noisy signals such as PGND_Bxx, VIN_Bx, and SW_Bx, as well as high bandwidth signals such as the I2C. Avoid both capacitive as well as inductive coupling by keeping the sense lines short, direct and close

to each other. Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane if possible. Running the signal as a differential pair is recommended.

- PGND_Bxx, VIN_Bx and SW_Bx should be routed on thick layers. They must not surround inner signal layers which are not able to withstand interference from noisy PGND_Bxx, VIN_Bx and SW_Bx.
- Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. Proper PCB layout, focusing on thermal performance, results in lower die temperatures. Wide power traces come with the ability to sink dissipated heat. This can be improved further on multi-layer PCB designs with vias to different planes. This results in reduced junction-to-ambient (RθJA) and junction-to-board (RθJB) thermal resistances and thereby reduces the device junction temperature, TJ. Performing a careful system level 2D or full 3D dynamic thermal analysis at the beginning product design process is strongly recommended, using a thermal modeling analysis software

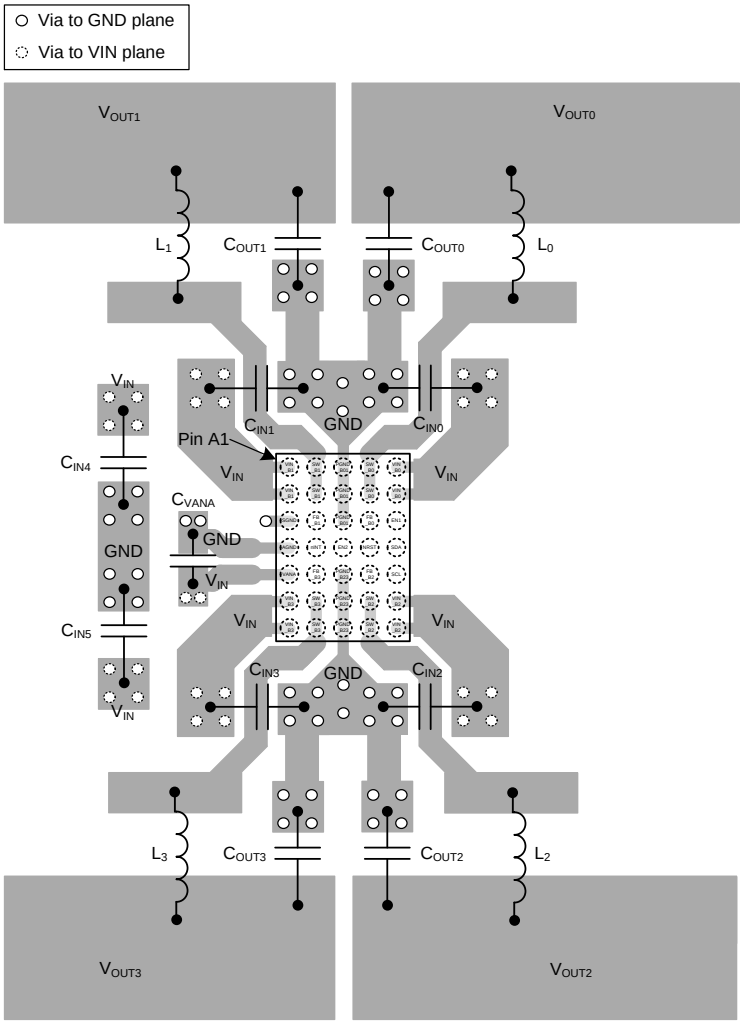


Figure 3: PCB layout example for LP8758-E0

6 Test Results

6.1 Equipment used

Table 8 is a list of the test equipment used in the preceding sections.

Table 8 Test equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Agilent DPO4014B
Voltage supply	Agilent E3631A
Multimeters	Agilent E34401A

6.2 Default output voltage at power up

Table 9 shows the example power up settings of the system.

Table 9 Default output voltage settings

BUCK OUTPUT	V_{OUT}	STARTUP DELAY	SHUTDOWN DELAY
Buck 0	1.0V	0 msec	0 msec
Buck 1	1.8V	5 msec	5 msec
Buck 2	3.3V	5 msec	0 msec
Buck 3	2.5V	5 msec	0 msec

6.3 Efficiency

The regulated output voltage remains stable at various input voltage levels. **Figure 4** shows the system output voltage efficiency at VIN of 3.3V

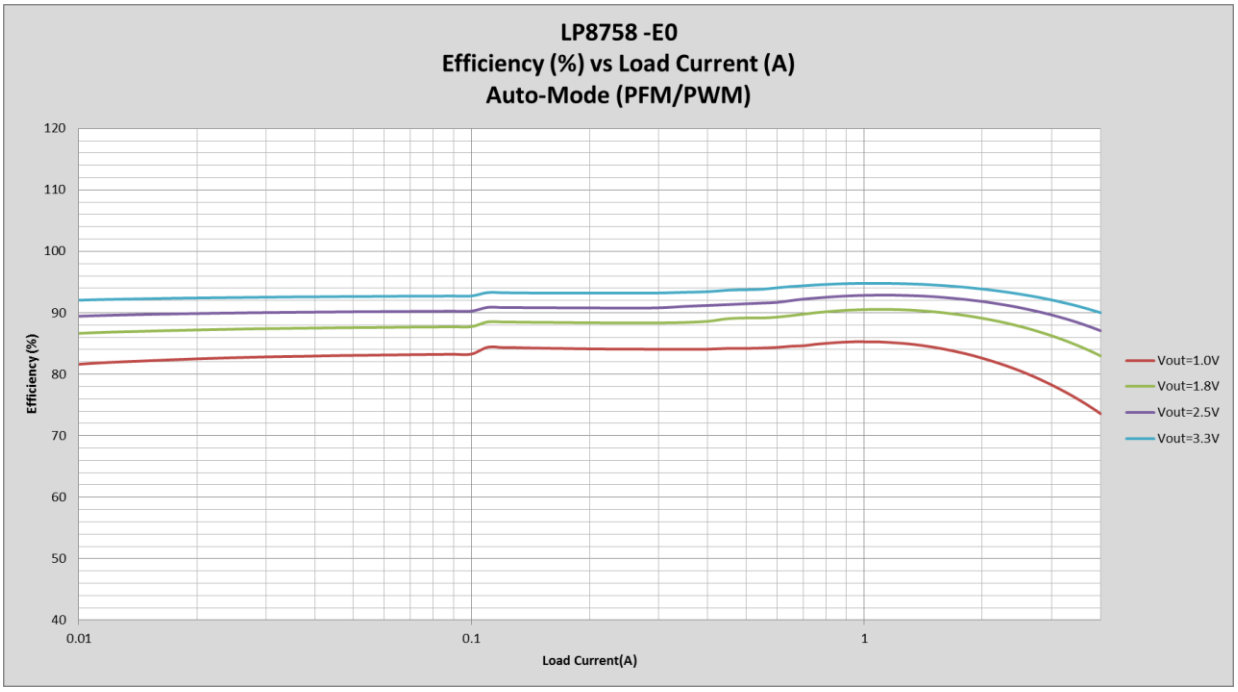


Figure 4: Output Voltage Efficiency in Auto Mode

6.4 Power up and Shutdown Sequence

Figure 5 & 6 show examples of the power up and power down sequence needed for the ASIC voltages of 1.0V and 1.8V. This can be controlled using the EN1 Pin on the LP8758. The delays are programmable from 0msec to 15msec in steps size of 1msec.

With the following design no external sequencer is needed and it reduces the overall BOM cost for the design and also makes it configurable across multiple reference platforms where different sequencing needs exist.

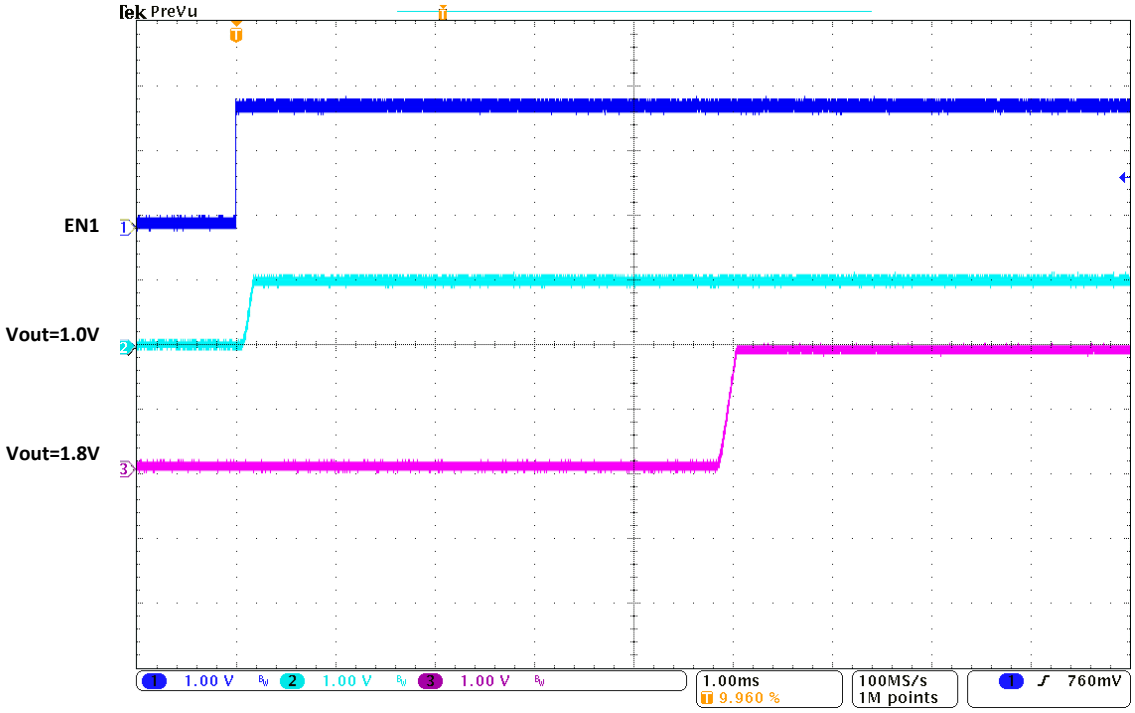


Figure 5 Measured Power up Sequence

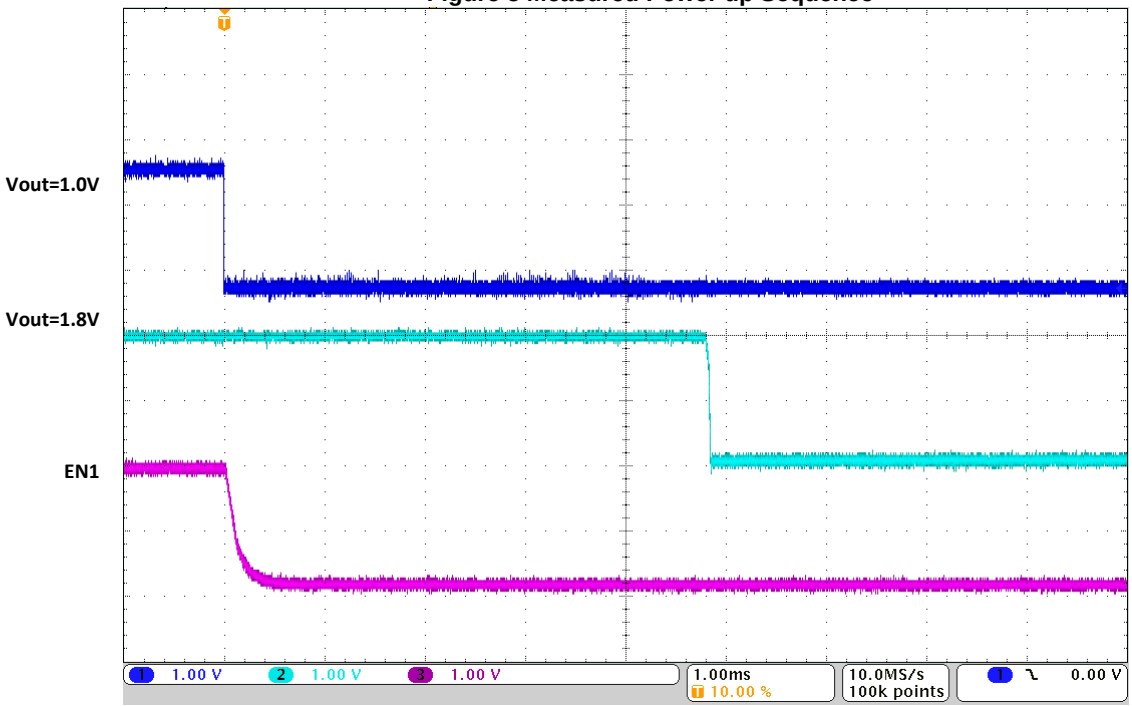


Figure 6 Measured Power down Sequence

6.5 Voltage Output accuracy

Figure 7 is a graphical representation of the computational results of the output voltage vs the load current to show that output voltage variation is within the 2% of the nominal expected voltage. The data shown below is in Forced PWM mode.

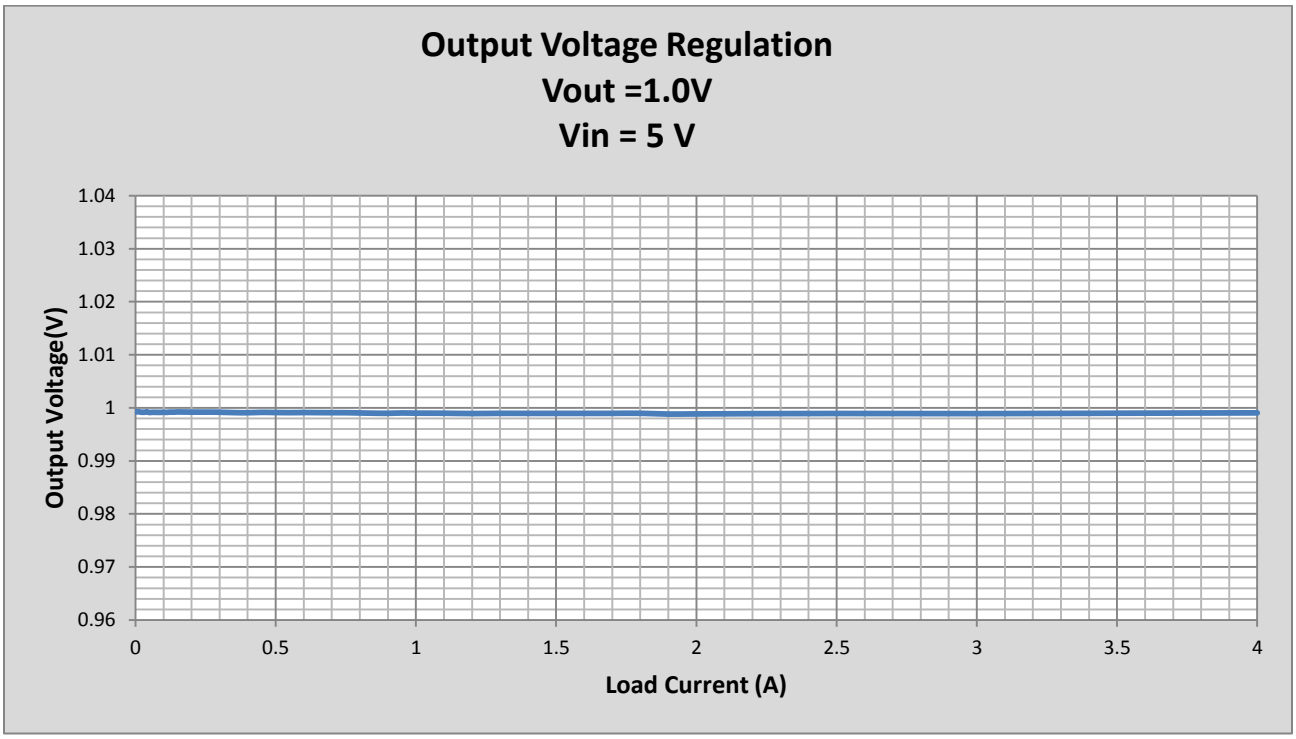


Figure 7 Output voltage vs Load Current

7 Design Files

7.1 Schematics

To download the Schematics, see the design files at http://www.ti.com/tool/TIDA-00719

7.2 Design Files

To download the design files, see the design files at http://www.ti.com/tool/TIDA-00719

- Bill of Materials
- Gerber Files
- Layout Prints

8 Terminology

TI Glossary: SLYZ022 This glossary lists and explains terms, acronyms, and definition

9 About the Author

Chintan Parekh Is an Applications & Systems Engineering Manager at Texas Instruments; he brings to this role experience in system-level analog, mixed-signal, and power management design.
Chintan earned his Bachelor of Engineering from University of Mumbai & Master of Science in Electrical Engineering from University of Southern California (USC).

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