TI Designs

Automotive Precision eFuse Reference Design

TI Designs

Fuses are used in many products to avoid current surges and the damage that overcurrent may cause. The traditional fuses used in the automotive space are low in accuracy and response time. The TIDA-00795 Automotive Precision eFuse reference design is a replacement to the traditional fuse, offering overcurrent protection with higher accuracy and features not found in traditional fuses. This TI Design can be used as a building block to implement a multichannel eFuse box. It can also be used in a body control module (BCM) and electronic control unit (ECU).

Design Resources

TIDA-00795	Design Folder
INA300-Q1	Product Folder
LM9036	Product Folder
LM74610-Q1	Product Folder

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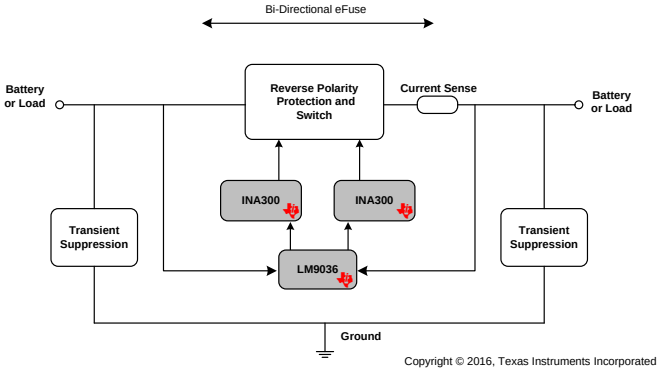
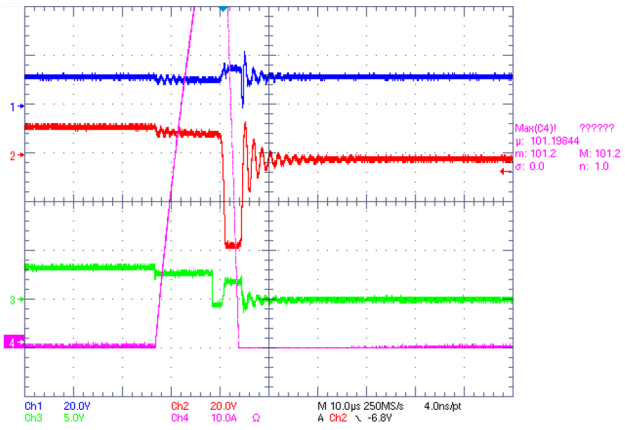
Design Features

- Overcurrent Limit: Up to 30 A (Scalable to > 100 A (1))
- Accuracy: > 97% (2)
- Response Time: Max 10 µs (Configurable)
- Configurable Delay Time to Accommodate Inrush Current for 10, 50, and 100 µs
- Target Quiescent Current: < 10 µA (3) / Channel
- Reverse Polarity Protection
- Compliance to 12-V Electrical Transients of ISO 7637-2
- Configurable Hysteresis for Accuracy
- Power off or Push Button to Reset Errors

Featured Applications

- Automotive eFuse Box
- Body Control Module
- High-Side Smart Switch





(1) Scalable solution based on selection of components
(2) Accuracy specified for 30-A current limit (configurable)
(3) Expected for single-channel eFuse in multichannel eFuse box

1 Key System Parameters

Table 1. Key System Parameters

PARAMETER	SPECIFICATION	MIN	TYP	MAX	UNIT
V_{INPUT}	DC input operating voltage	–28	—	28	V
I_{ON_TIME} Output current on time	Output load current: ≤ 30 A	2.2	3	3.5	ms
V_{ON_TIME} Output voltage on time	I_{LOAD} ≤ 30 A	—	2.24	—	ms
V_{OFF_TIME} Output voltage off time	I_{LOAD} = 30 A Input source off; output current less than 10 %	—	3	—	ms
Design accuracy	Based on selection of components Value specified for 30 A (see Section 3.1.5)	—	97.36%	—	—
Trip time	Trip current response time of eFuse Configured delay: 10 µs	—	13.8	—	µs
Trip error	Max current trip error (Measured at all current trip configurations)	—	2.82%	—	—
Resistance	Average measured turn on resistance of eFuse design	—	11.05	—	mΩ

2 System Description

Bidirectional automotive precision eFuse is a concept to replace typical fuses in cars. There is a need to look for novel methods to replace traditional fuses. Automotive fuses that are currently available in the market are slow in response and low in accuracy. The response time of a fuse is indirectly proportional to the safety of the system. Factors such as high delay time and high response time can foresee damage to loads and series path components (wiring, semiconductors, and connectors). To avoid such damages, manufacturers are forced to design the system with additional safety margins for components, which increases cost and weight (indirect fuel costs) of the car. An eFuse with high accuracy and low response time increases the safety of system and reduces the need to over design components.

Cars are flexible, but the fuse is not. The fuse rating for an application is fixed. If the load current is directly proportional to system performance, then the fuse rating has to be set at the maximum performance with additional tolerances. This setting can cause the fuse rating to be anywhere from 50% to 80% above the normal operating current of load, which compromises the safety of the system. Instead, this system needs a flexible eFuse, which can adapt for runtime system performance.

Traditional fuses are available with standard values. Sometimes, it is difficult to get fuses for required current limit values, which leads to compromising by choosing the nearing fuse value to protect the circuit. This compromise is a risk for the performance of the system. An automotive system requires an eFuse solution that is adaptable based on the application.

Frequent or long-running load operations lead to high power dissipation in series path components. The fuse will also heat up and will have a chance of failure while stressing at top load conditions. This damage is irreversible, forcing the customer to replace the fuse. Because early warnings are not possible to avoid these damages, a self-healing eFuse can prevent frequent service calls. An eFuse with the appropriate monitor and control circuits can adapt and inform its condition to avoid such damages.

Due to its internal characteristics and manufacturing quality, the operating current of the fuse has to be set far less than the rated fuse current (or melting current). At higher ambient temperatures, fuses blow faster, which means it melts well below the rated current; therefore, considering the temperature rerating parameter while selecting the fuse is required; refer to the following equation:

$$\text{Ideal fuse rating} = \frac{\text{Normal operating current}}{\text{Temperature rerating factor} \times 0.75}$$

A temperature rerating factor depends on the type of fuse manufacturer and material. Usually, this parameter varies from 12% to 40% based on the type of fuse. For an operating current of 15 A, if the temperature rerating factor is 0.85 (15% error), then required fuse rating is 23.52 A.

$$\text{Fuse rating} = \frac{15}{(0.85 \times 0.75)} = 23.52 \text{ A}$$

23.52 A is not the standard fuse rating; so, the nearest fuse to select is 25 A. For the given operating current of 15 A, the nearest possible fuse that can be fitted is 25 A, which is 66.67% higher. This difference leads to overdesigning the series path components and system. This overdesign adds cost and weight to the system. By selecting appropriate components, the eFuse reduces the delta between the operating current and trip current.

eFuses can be used in electronic control units to replace normal fuses, they can reset and offer runtime configurable solutions. Section 4 details the implementation of a multichannel eFuse box.

Key features expected from this eFuse design include:

- Accuracy
- Response time
- Flexible operation
- Self heal or trip
- Low turn-on resistance
- Scalable applications
- Reliability

This reference design uses the INA300-Q1 to build a bidirectional eFuse that can handle trip currents up to 30 A.

2.1 INA300-Q1

The INA300-Q1 is a high common-mode, current-sensing comparator that is configured to detect overcurrent conditions through measuring the voltage developed across a current sensing or shunt resistor. The device can measure this differential voltage signal on common-mode voltages that can vary from 0 V up to 36 V, independent of the supply voltage. The device features an adjustable threshold range that is set using a single external limit-setting resistor. A selectable hysteresis feature enables adjustable operation of the comparator to accommodate the wide input signal range of 0 to 250 mV.

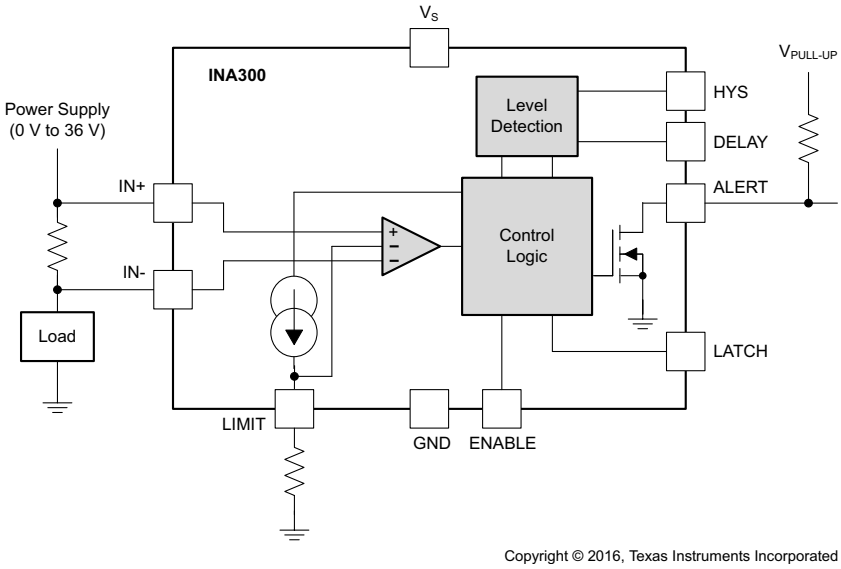


Figure 1. INA300-Q1 Block Diagram

Key features include:

- Selectable response times: 10, 50, and 100 μs
- Programmable threshold:
  - Resistor configurable
  - DAC output from 0 to 250 mV
- Adjustable hysteresis: 2, 4, and 8 mV
- Accuracy:
  - Very low offset voltage ≤ ±500 μV (varies for different delay times)
  - Very low voltage drift ≤ 0.5 μV/°C
  - Low bias current ≤ 5 μA
- Wide common-mode input voltage range 0 to 36 V

2.2 LM9036Q

The LM9036Q ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 25-μA ground pin current at a 0.1-mA load, the LM9036Q is ideally suited for automotive and other battery operated systems.

The LM9036Q retains all of the features that are common to low dropout regulators, including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM9036Q has a 40-V maximum operating voltage limit, a −40°C to 125°C operating temperature range, and ±5% output voltage tolerance over the entire output current, input voltage, and temperature range.

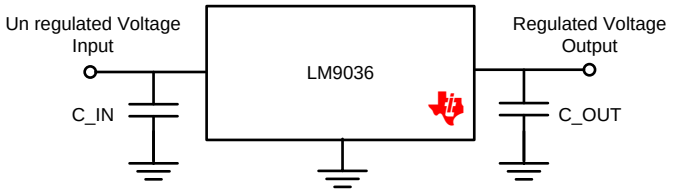


Figure 2. LM9036Q Block Diagram

Key features include:

- Ultra-low ground pin current (I_{GND} ≤ 25 μA for I_{OUT} = 0.1 mA)
- Low dropout voltage typically 200 mV at I_{OUT} = 50 mA
- Reverse transient protection for –45 V
- Short circuit current limit and thermal shutdown protection
- Output tolerance ±5% over line, load, and temperature

3 Block Diagram

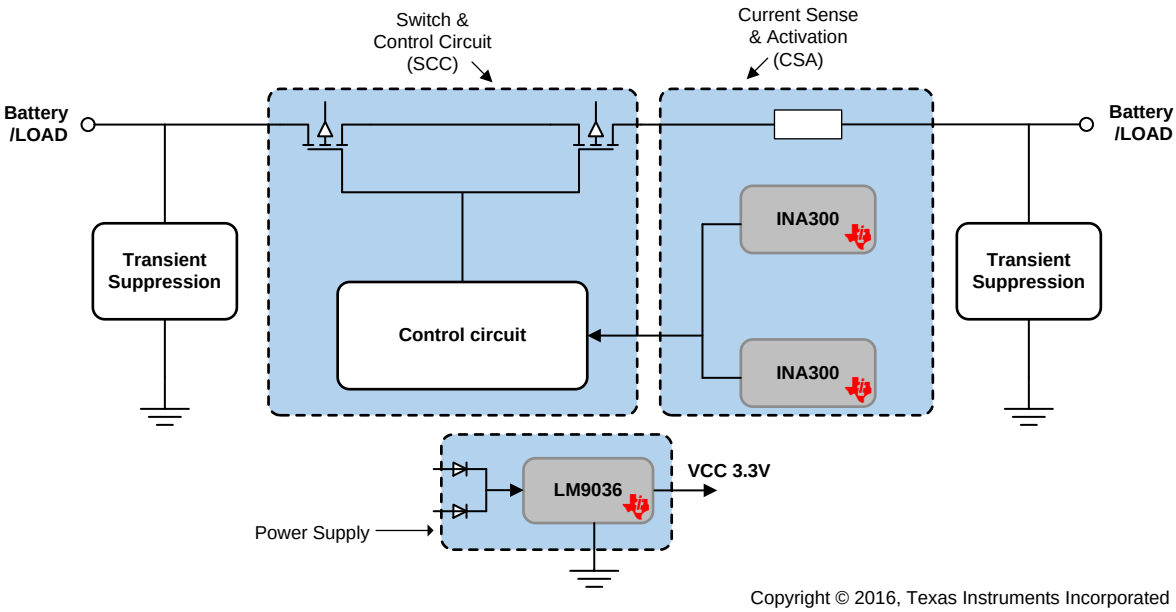


Figure 3. eFuse Block Diagram

Automotive eFuse design is categorized into the following subsections:

- Current Sense and Activation (CSA)
- Switch and Control Circuit (SCC)
- Power Supply and Protection (transient suppression)

3.1 Current Sense and Activation (CSA)

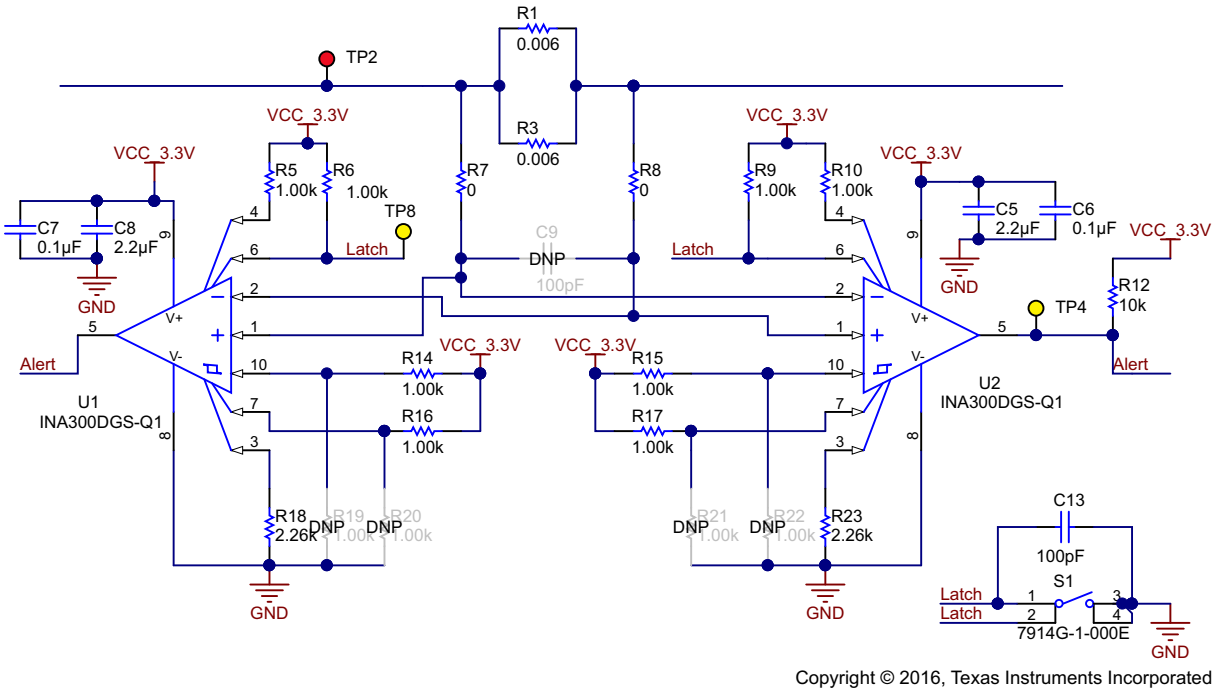


Figure 4. CSA Schematic

The CSA circuit plays an important role in the eFuse system design. 90% of the design remains constant, which can be scalable to multiple current sense values. Current limit value can be varied by two modes:

1. Shunt resistance
2. Current limit resistance

R_S is the equivalent shunt resistance and I_{TRIP} is the trip current to be set for eFuse. To calculate shunt resistance and in turn help calculate common-mode voltage:

$$R_S = \frac{R1 \times R2}{R1 + R2} \quad (1)$$

$$V_{CMTRIP} = R_S \times I_{TRIP} \quad (2)$$

As per Figure 4, R18 and R23 are current limiting resistors for U1 and U2, respectively. Consider R_X as the current limiting resistor for the INA300-Q1. A constant current is flown into R_X, which is a programmed threshold limit.

$$V_{LIMIT} = R_X \times I_{INA300\_LIMIT} \quad (3)$$

V_{LIMIT} is the programmed threshold limit set to the INA300-Q1. I_{INA300_LIMIT} is the current flowing in the INA300-Q1, which is 20 µA.

3.1.1 Recommendations to Set Current Trip Value for eFuse

1. There are very few choices for R_S shunt resistors. Finalize the R_S shunt resistor for the appropriate current with a given power dissipation and error budget. Calculate the V_{CM_TRIP} value, which is the common-mode voltage at which the INA300-Q1 has to trip.
2. There are quite good choices for R_X resistors. Selecting the limit resistor depends on the delay time configured for the INA300-Q1. The I_{INA300_LIMIT} is the current flowing from pin 3 of the INA300-Q1 device, which is typically 20 μA.

   For 50- and 100-μs delay times:
   $$R_X = \frac{V_{LIMIT}}{I_{INA300\_LIMIT}}$$

   For a 10-μs delay time:
   $$R_X = \frac{\left(V_{LIMIT} + NAF\right)}{I_{INA300\_LIMIT}}$$

The standard resistor value for R_X has to be chosen in such a way that the V_{LIMIT} value is close to the required V_{CM_TRIP} (the common-mode trip value of the INA300-Q1).

3.1.2 Delay Time

The delay time of the INA300-Q1 is configurable. It can be mapped with the functions of the eFuse. Inrush currents of the eFuse can be easily accommodated with the delay time configuration of the INA300-Q1. It can be set to three different values with two configurable resistors:

- 10 μs: Unpopulate R16, R20, R17, and R21
- 50 μs: Populate only R20 and R21
- 100 μs: Populate only R16 and R17

The delay time of the eFuse has to be set with a proper load analysis. A low delay time gives a faster response to any error conditions, but it will have less time for inrush currents. In other cases, if a high response time has been set for inrush currents, the series path components must be able to withstand during error conditions. Control unit loads with bulk capacitors must be set with an appropriate delay time to accommodate inrush currents. Resistive or inductive loads that have fewer inrush currents can be set with a low delay time.

Delay time is not required to be constant on both directions. In an eFuse circuit, delay times can be selected based on the type of load. In Figure 4, if TP2 is connected to the battery and R8 is connected to the load, U1 (INA300-Q1) supports for forward currents flowing from the source to the load, and U2 (INA300-Q1) works for reverse currents and kickback currents from inductive loads to source. There is a scope to configure different trip currents and delay times for U1 and U2 circuits.

3.1.3 Alert

The alert pin of the INA300-Q1 is an output after the comparator. Based on latch pin configuration, the alert pin responds to overload or short circuit errors. In transparent mode, the alert pin is pulled down only when there is an overcurrent across the shunt resistors. If the load current falls, the alert output will be cleared after the 10-μs configured delay time coupled with hysteresis set to its respective INA300-Q1. Output voltage will be back to 3.3 V in a short time (based on the MOSFET capacitance and pullup resistor). Take care when configuring such circuits; a delay when operating the control circuit may damage the series path components.

If the Latch pin is pulled up to VCC, the alert pin will hold the error state of the comparator. Once there is an overload or short circuit for the configured delay time, the alert pin will be pulled to low and stays in the same state until powered off or reset (pull down the latch pin for at least 200 ms).

3.1.4 Miscellaneous Functions

The CSA circuit can be configured appropriately based on the application. The enable pin can disable the INA300-Q1 to reduce the quiescent current of the system. Pull up the enable pin to activate the internal circuit of the INA300-Q1.

- Enable: Populate R5 and R10 for U1 and U2, respectively

Based on severity of the load, the load current monitoring circuit can be set to latch or transparent mode. This function provides the signal handling circuit a scope to adjust the loading behavior and bring the operating currents to a normal state without any interruptions. In this reference design, the latch pin is interfaced to a switch, which can be used to reset the eFuse. In transparent mode, there is a chance of high currents flowing in the circuit during SCG or overload conditions. Take care before opting for transparent mode.

- Latch Pin: Populate R6 and R9 for U1 and U2 to be in LATCH mode. Press the switch to reset circuit (only after clearing the error).

3.1.5 Error Calculation

Calculate circuit error before finalizing the components for current shunt and current limit resistors. To better understand the design, the following is an example in error calculation and component selection is shown for a 30-A current trip.

- R1 and R3: 6 mΩ ± 1%
- R_S: 3 mΩ ± 1%
- R18 and R23 (R_X): 4640 Ω ± 0.1% (close to required value with 0.1% tolerance)
- I_{INA300_LIMIT}: 20 µA ± 0.75% (taken from the INA300-Q1 datasheet)
- V_{OFFSET_MAX}: 650 µV (maximum offset voltage for a 10-µs delay)
- $CMRR_{MIN}$: 100 dB (10 µV/V)

1. Define the current limit value using $V_{LIMIT} = R_X \times I_{INA300\_LIMIT} \rightarrow V_{LIMIT} = 0.0928 \pm 0.85\%$.
2. Set the current limit value using $I_{TRIP} = V_{LIMIT} / R_S \rightarrow I_{TRIP} = 30.933 \pm 1.85\%$. Therefore, the trip error contributed by shunt and current limit resistors is $E_{TRIP} = 1.85\%$.
3. Find the input offset voltage of the INA300-Q1 using $E_{OFFSET} = \frac{V_{OFFSET\_MAX} \times 100}{V_{LIMIT}} = 0.7\%$.
4. Find the CMRR error with the INA300-Q1 using
   $E_{CMRR} = \frac{\left(V_{CM} - V_{CM\_SYS}\right) \times CMRR_{MIN} \times 100}{V_{LIMIT}} = 0.0652\%$.
   (V_{CM} = 12, V_{CM_SYS} =18, $CMRR_{MIN}$ =10 µV/V)
5. Find the PSRR error with the INA300-Q1 using
   $E_{PSRR} = \frac{\left(V_{CM} - V_{CM\_SYS}\right) \times PSRR_{INA300} \times 100}{V_{LIMIT}} = 0.0323\%$.
   (V_S = 3.3 V, V_{PS_SYS} = 3.5 (max), $PSRR_{INA300}$ = 150 µV/V)

Total error: $E_{TRIP} + E_{OFFSET} + E_{CMRR} + E_{PSRR} \rightarrow 2.64\%$ (approximately)

NOTE: Filter components need to be populated based on the application. As the eFuse is close to the battery, there is a small chance of a power supply ripple. To test with lab power supplies, populate the filter circuit to obtain better accuracy; however, this action introduces error because of input bias currents. For end designs, the INA300-Q1 can work accurately without any filter components. So, errors with bias currents coupled with filter resistors are not considered in error calculations.

3.2 Switch and Control Circuit (SCC)

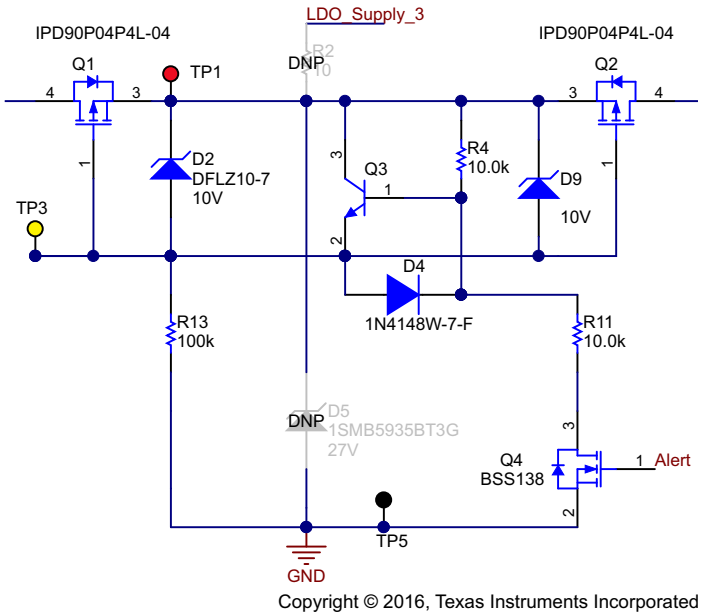


Figure 5. SCC Schematic

- Q1 and Q2 are P-channel MOSFETS, which are used for switch and reverse polarity functions.
- Q3 is used to switch and discharge the gate to source voltage of Q1 and Q2.
- Q4 is used to turn off the switch circuit by turning on Q3. Biasing components and input voltage play a role for this operation.
- R4, R11, and R13 are used to bias the circuit during the startup and operation phases.
- D4 is used to protect Q3.
- D2 and D9 are used to protect Q1 and Q2, respectively. Only one component can be used from D2 and D9; it depends on component placements and routing options available on the board.

Case 1: Forward conduction mode
The drain of Q1 is connected to the battery source, whereas the drain of Q2 is for load side connection. During normal operation, current flows through Power source → Q1 → Q2 → Series resistor → Load.

Q1 supports reverse polarity protection, whereas Q2 is used as a switch to turn off the load during overcurrent conditions.

Case 2: Reverse conduction mode
The drain of the Q2 side is connected to the battery source, whereas the drain of Q1 is connected to load. During normal operation, current flows through Power source → Series resistor → Q2 → Q1 → Load.

Q2 supports reverse polarity protection, whereas Q1 is used as a switch to turn off the load during overcurrent conditions.

3.2.1 Alert: High → Q4 is on

The alert pin is pulled to VCC3.3V by R12. During normal operation, when there is no error, the alert pin always stays high. Internal operation (biasing and control) of the SCC is common for both forward and reverse conduction modes.

- When the alert pin is pulled up, VCC3.3V is greater than V_{GS_TH} of the BSS138, which turns on Q4.
- When Q4 is turned on, current flows through R4, R11, and Q4 based on voltage at V_{TP1}

$$I_{Q4} = \frac{V_{TP1}}{R4 + R11 + R_{ON\_BSS138}}$$

- Voltage at V_{TP3} is important to operate Q1 and Q2. V_{TP3} mainly depends on the state of Q3 and V_{TP1} voltage.
- Voltage at the base of Q3 V_{B_Q3} depends on R11 and the state of Q4.
  As Q4 is turned ON: $V_{B\_Q3} = I_{Q4} \times \left(R11 + R_{ON\_BSS138}\right)$
- Voltage of $V_{TP3} = V_{B\_Q3} - V_{BE\_Q3}$; this is valid until $(V_{TP1} - V_{TP3}) < V_{Z\_D2}$ or V_{Z_D9}.
  V_{Z_D2} and V_{Z_D9} are the Zener breakdown voltages of D2 and D9, respectively.
- If $V_{TP3} - V_{TP1}$ is < V_{GSth_Q1} and V_{GSth_Q2} (Q1 and Q2 are P-MOSFET), then both Q1 and Q2 will turn on, which allows the eFuse to flow the current from the power source to the load.

3.2.2 Alert: Low → Q4 is off

The alert pin is pulled to ground by the INA300-Q1 (U1 or U2) when there is an overcurrent error. This error will be latched or transparent based on the configuration of the INA300 (U1 or U2). Turning off the operation (biasing and control) of the SCC is common for both forward and reverse conduction modes.

- When the alert pin is pulled down, voltage at the gate of Q4 is less than V_{GS_TH} of the BSS138, which leads to turning off Q4.
- When Q4 is turned off, leakage current flows through R4, R11, and Q4 based on voltage at V_{TP1}.
- Voltage at V_{TP3} is important to operate Q1 and Q2. V_{TP3} mainly depends on the state of Q3 and V_{TP1} voltage.
- Voltage at the base of Q3 V_{B_Q3} depends on R14, I_{LEAK_Q4} off-state leakage current of the BSS138 (Q4), and V_{TP1}.
  $V_{B\_Q3} = V_{TP1} - (I_{LEAK\_Q4} \times R4)$
  V_{B_Q3} is close to V_{TP1} as leakage current is very low.
- Voltage of $V_{TP3} = V_{B\_Q3} - V_{BE\_Q3}$
  V_{BE_Q3} is less than 0.7 V for Q3. So, $(V_{TP3} - V_{TP1}) > -1$ V.
- As long as the alert pin is pulled to ground, $V_{TP3} - V_{TP1}$ is always greater than V_{GSTH_Q1} and V_{GSTH_Q2} (gate-to-source threshold); as a result, both Q1 and Q2 will remain in an off state.

3.2.3 Startup: (V_{BATT} Rising from 0 to 10 V)

In forward conduction mode, voltage is applied at the drain of Q1 and the body diode of Q1 starts conducting. Voltage at TP1 follows the battery voltage along with the drop of the body diode.

$$V_{TP1} = V_{BATT} - V_{FD\_Q1} \quad (4)$$

where:

- V_{BATT} is battery voltage
- V_{FD_Q1} is forward voltage drop of Q1

VCC3.3V < V_{GSTH_Q4}
Q4 (BSS138) is a small signal MOSFET that stays in an off state until VCC reaches the V_{GS_TH} of the BSS138, which is 1.3 V (typical). Section 3.2.2 explains the behavior of the circuit when Q4 is OFF.

VCC3.3V > V_{GSTH_Q4}
When VCC is greater than V_{GSTH_Q4} (BSS138), Q4 turns on. When Q4 is turned on, circuit behavior is as explained in Section 3.2.1. Voltage at the base of Q3 (V_{B_Q3}) depends on the resistance of R4 and R11. In this case, the voltage of V_{TP3} depends on V_{B_Q3} and the voltage drop of the base to the emitter in Q3.

If Q4 is turned ON:

$$V_{B\_Q3} = \left(V_{TP1} \times \frac{R11 + R_{ON\_BSS138}}{R11 + R4 + R_{ON\_BSS138}} \right)$$

Selecting R4, R11, and R13 plays an important role for startup behavior. If Q4 is off, $V_{TP3} – V_{TP1}$ should be greater (Q1 and Q2 are P-MOSFET) than V_{GSTH_Q1} and V_{GSTH_Q1} in operating voltages of eFuse. This ensures the switches (Q1 and Q2) are turned off when Q4 is turned off as per the functionality of the eFuse.

If there is no overload or short circuit fault on the load: V_{TP1} follows the battery voltage, whereas the load does not see any voltage until Q4 is turned on. When Q4 is turned on, Q1 and Q2 turn on. Voltage at the load depends on the selection of series path components Q1, Q2, and R_S.

3.2.4 Operation: (Typical V_{BATT} 13.5 V)

- In Figure 5, if the battery voltage is greater than 10 V, D2 and D9 protect Q1 and Q2, respectively, from gate-to-source breakdown.
- If $V_{TP1} – V_{TP3}$ is greater than 10 V, the result is limited to 10 V and V_{TP3} follows V_{TP1} with a constant voltage drop. D4 is placed to protect Q3 from its maximum reverse breakdown voltage.
- Operation of the SCC follows the state of the alert pin. Response time of the switches upon activating Q4 depends on the selection of components. R4, R11, Q1, Q2, and Q3 play a significant role for the response time.

During normal operating conditions, the alert pin is pulled to VCC3.3V with R12 (10 kΩ). Q4 is turned on when the load current is less than the trip current. If the alert pin is pulled down to low due to an overload or short circuit, Q4 turns off, which effectively turns off Q1 and Q2. The turn-off response time of Q1 and Q2 depends on R4 and the gate-to-source capacitance (C_{GS_Q1}) of Q1 and Q2. The maximum delay time of the IPD90P04P4L-04 is 140 ns.

3.3 Power Supply and Protection

3.3.1 Power Supply

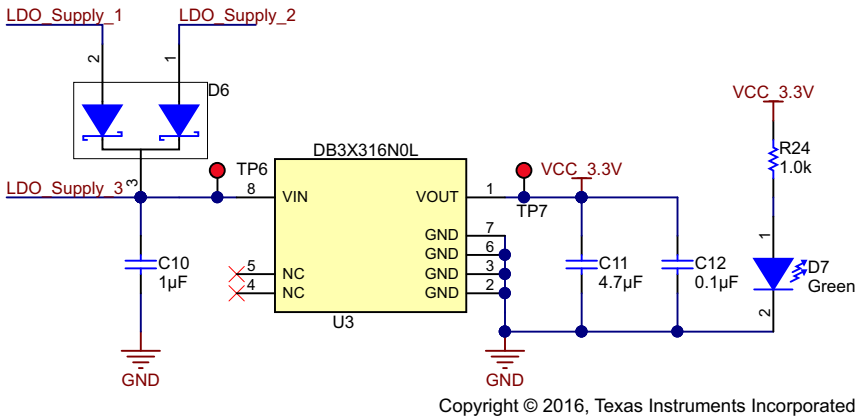


Figure 6. LDO Power Supply Schematic

The LM9036 (U3), a wide VIN LDO, is used to generate VCC3.3V. In a bidirectional eFuse, the power supply can be given from any side. D6 (schottky diode) is used to tap the signal from both directions and to supply the board. To save cost, the input supply can also be tapped from TP1, and R2 can be populated with low resistance and unpopulate D6. C10, C11, C12 are the bypass capacitors for the LM9036.

The operating characteristics of the LM9036-Q1 include:

- 0 V < V_{IN} < 2.5 V → V_{OUT} = 0 V (max 0.5 V)
- 2.5 V < V_{IN} < 3.3 V → V_{OUT} = V_{IN} – 0.1 V (max forward voltage drop)
- 3.3 V < V_{IN} < 40 V → V_{OUT} = 3.3 V (± 4%)

3.3.2 Protection

Automotive precision eFuse design can offer protection to ISO7637-2 power transients. Design also supports Jump start, Cold cranking and Reverse polarity. As shown in Figure 18, D1 and D3 bidirectional transient voltage suppression (TVS) 1.5SMC33CA-E3/57T is used to handle ISO7637-2 transients. D5 can only be populated to suppress Positive transients. Based on the requirement of the system; selection of D1, D3, and D5 can be decided.

Reverse Polarity protection can be achieved by SCC configuration. For any negative voltage gate to source voltage of Q1 and Q3 are greater than threshold limit. Both the switches will stay in OFF state, there will not be any conduction between source and load. Design of Internal circuits has to be taken care for any influences during reverse polarity.

4 Getting Started: Design

The Automotive Precision eFuse TI Design can compete with typical fuses available in the market. It can trip at specified currents in both directions. The design can be adapted easily to multiple current trip values. As of now, the design can support eFuse applications for a 12-V battery architecture. This TI Design can be easily portable to multichannel eFuse boxes. Selecting the series path components, current limit components can be done based on the type of load and application.

As mentioned in Section 2, a fuse box is a passive mechanical component in the cars. It interconnects the battery connections to loads with a melting fuse. In a multi-channel eFuse box, appropriate eFuse topologies can be used based on the type of load and application. Top level loads for batteries in an automotive environment are electronic control units, lamps, LEDs, relays, solenoids (switching), and motors. For electronic control units, lamps and LEDs have little to no kickback energy during their operation. A unidirectional eFuse with built-in reverse polarity protection works best for such applications.

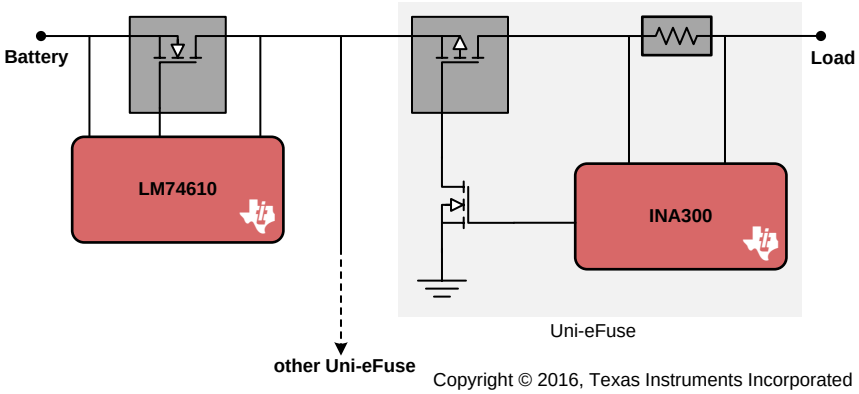


Figure 7. Unidirectional eFuse

The LM74610 ORing controller provides reverse polarity protection. It works for zero quiescent current of the module. The INA300-Q1 supports current sense and latch circuit. The uni-eFuse block can be replicated for multiple loads. The number of uni-eFuse blocks connected in parallel depends on the components selected for reverse polarity protection. The LM74610 turn on the MOSFET for 96% to 98% of time; it turns off for 2% to 4% of its duty cycle based on the capacitor selected. During the off-time of the LM74610, current flows through the body diode of the MOSFET. This leads to a dip in voltage based on the type of transistor selected. These dips can be filtered in electronic control units. The I_{LIMIT}, Enable, and Latch pins of the INA300-Q1 can be interfaced with a microcontroller. Interfacing with the controller increases the chances to improve diagnosis and system control. The quiescent current of a single channel in a unidirectional eFuse is around 3.5 µA (disable INA300-Q1).

Bidirectional eFuse topology is the typical choice for inductive loads. Kickback energy can be easily transferred to the battery based on the type of loads. Take care while designing the eFuse for high power inductive loads. When the high power inductive load is turned off, energy stored in the inductor tries to kickback to the battery. In such cases, selecting a relevant current limit and delay time avoids any unnecessary trip of the circuits.

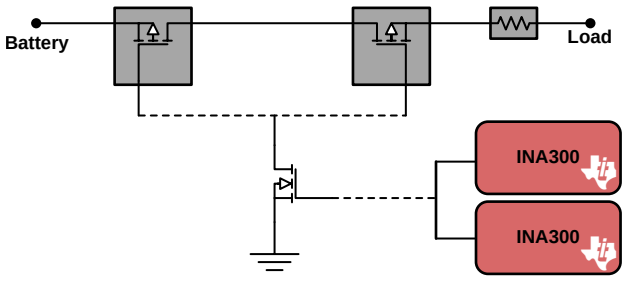


Figure 8. Bidirectional eFuse Block

A bidirectional eFuse circuit provides more flexibility to operate inductive loads. It also trips for overcurrent while operating in reverse conduction mode. The quiescent current of a bidirectional eFuse block module is around 7 µA (disable INA300-Q1). An intelligent multichannel eFuse box can be built by integrating unidirectional and bidirectional eFuses.

4.1 Multichannel eFuse Box

A multichannel eFuse box block diagram is shown in Figure 9. Appropriate selection of eFuse topologies can be chosen based on type of loads. Mixture of unidirectional and bidirectional eFuses can bring more value and reduce the overall costs of the system. The most important functions of eFuse are featured in the following subsections.

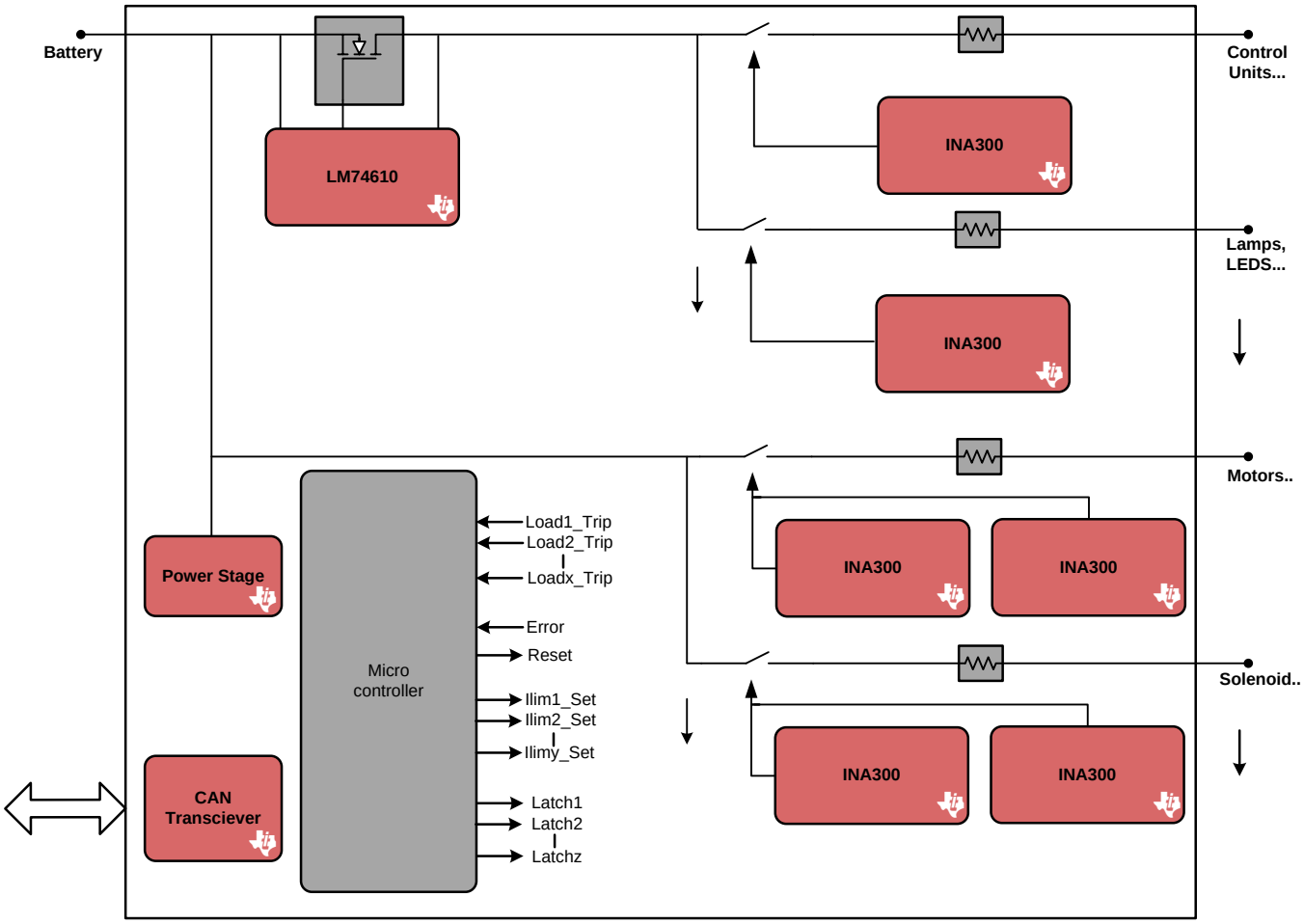


Figure 9. Multichannel eFuse Block Diagram

4.1.1 Inrush Current

The inrush current of the system can be handled in two ways in the multichannel eFuse. It can be changed by varying the current limit or delay time. Both methods have their own pros and cons in handling the system.

When the system is woken up by Immo or KL15, the microcontroller enables the INA300-Q1. Current limit resistors can be connected in a bridge configuration. Figure 10 shows an example configuration. The R_lim2 value is chosen to be at a higher current limit to accommodate inrush currents. If the microcontroller pulls the Inrush_Disable pin to high, then R_Lim1 will be parallel to R_Lim2, which reduces the current limit for the INA300-Q1. The value of R_Lim1 and R_Lim2 must be set based on the requirement of the system. The Inrush_Disable pin can be connected to multiple loads, so based on the type of loads and applications, a set of eFuses can be allowed to have a higher current limit.

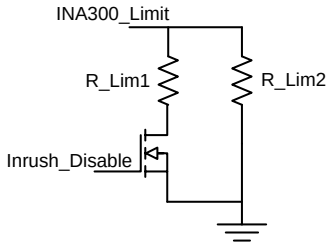


Figure 10. Current Limit Configuration → Inrush Current

Table 2. Current Limit Control for Inrush Currents

PARAMETER	RESISTANCE	COMMENT
Inrush_Disable → Low	R_Lim2	High current limit, supports inrush current
Inrush_Disable → High	R_Lim1 || R_Lim2	Actual load current limit

Inrush currents can also be handled with a delay time. Delay time configuration can change the runtime to support Inrush currents. The INA300-Q1 has three options to set the delay time: 10 μs, 50 μs, and 100 μs. This can be varied easily for two configurations (see Table 3). Figure 11 shows an example of changing the delay time of the INA300-Q1. Multiple eFuse delays can be configured by using a single pin from the microcontroller.

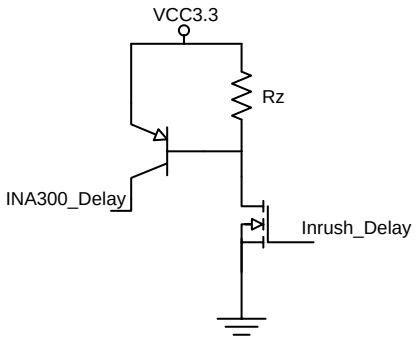


Figure 11. Delay Time Configuration → Inrush Current

Table 3. Delay Control for Inrush Currents

PARAMETER	DELAY SETTING	COMMENT
Inrush_Delay → High	INA300-Q1 delay pin pulled to VCC3.3	100-µs delay time is activated, supports high inrush currents
Inrush_Disable → Low	INA300-Q1 delay pin open	10-µs delay time is activated, supports normal eFuse operation

Possible configurations to handle inrush currents are not limited as shown in this design guide. They can be implemented with combinations of current limit and delay pins. These two pins offer many options to handle inrush currents based on the application.

It is also possible to handle inrush currents in the INA300-Q1 without varying the current limit and delay pins. The latch pins of the eFuse loads, which have a high inrush current, can be interfaced to the controller. The type of connection to the controller can be defined based on available resources and needs. The connections to the eFuse circuit must be there in such a way that by default, all latch pins must be pulled up to VCC. The controller's interface should allow the latch pin to pull it down for a short duration. During the startup phase of the system, pull the selected latch pins of the INA300-Q1 low for a predefined time to allow inrush currents.

When the system has settled or is within the predefined time, the controller can turn off the relevant circuit to allow the efuses to latch for any overcurrent events.

4.1.2 Power Supply Transients

Due to multiple reasons, transients are observed in power supply lines. Inductive loads are one of the main sources for the power supply transients. More details for the power supply transients are specified in ISO7637-2. The impact power supply transients have on electronics varies based on the type source, loads, and architecture. Most automotive manufacturers maintain their own internal specification for these power supply transients.

In the current system architecture, fuses are used as an overcurrent blow (OCB) application. Normal fuses do not support suppression of power supply transients. A multichannel eFuse system has a scope to handle power transients better.

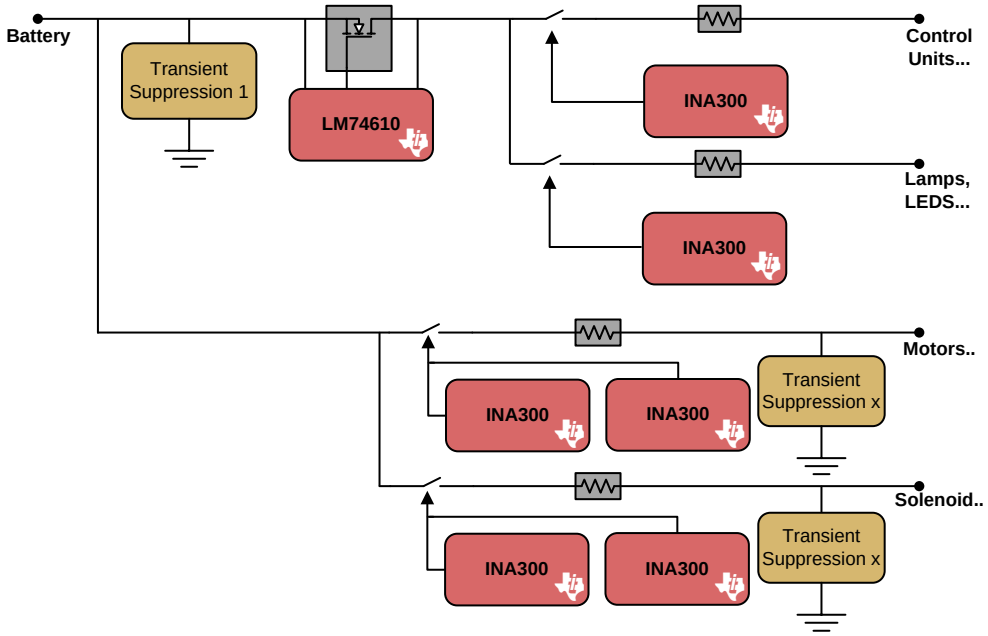


Figure 12. Transient Suppression Block Level

Transient suppression 1 (shown in Figure 12) can act as a central suppression circuit, which can safe guard most of the loads on a unidirectional eFuse. This can reduce or avoid the requirement of transient suppression in most of the electronics working under a unidirectional eFuse system. Save system costs by reducing the specification or avoiding individual transient suppressors in few loads.

Transient suppression x can be placed near inductive loads. Based on system requirements, transient suppressors can be placed in the multichannel eFuse box system. Components must be selected and placed appropriately to suppress the transients in bidirectional eFuse modules. Take care when handling the layout and interconnections required in the system.

NOTE: The connections shown in Figure 12 is only for reference. The actual wiring and routing of the system could be done to avoid or minimize the EMC interference in the system.

4.1.3 Diagnosis and Error Handling

The multichannel eFuse system offers much room for diagnosis and control of the loads and fuses. The alert pin of the INA300-Q1 can be taken as a system error. Based on the available resources, a system diagnosis can be further classified to find the exact root cause for error in the system. Based on the priority defined for the given error, the controller can take an action (error handling algorithm).

For example, a trip error was recorded for headlamps and LEDs. By resetting the error, the application is working fine. In such a case, only the trip error event is recorded and the system will be allowed to run normally without any interruption to the user (or driver). Due to external conditions such as overload or extreme temperatures, if the error repeats, the controller can check the influences that turn off the eFuse. Upon retry, if the eFuse of the lamp does not successfully turn on the lamp, the controller can increase the current limit by available methods and based on need (such as night time or low vision). If the lamp successfully turns on, it could solve the need and increase the scope of the system's functioning.

The parameters that led to failure can be logged. The controller and vehicle control systems can decide the next steps based on the importance of the function. If the eFuse starts functioning fine after resetting or by increasing the current limit, such instances can be noted, such as the frequency of resets, delta of current limit, temperature, and so forth. If the eFuse trips even after the current limit increases, the error will be logged and sent to other control units (BCU or cluster).

The flow chart that Figure 13 shows is an example of how to handle the errors in a multichannel eFuse system.

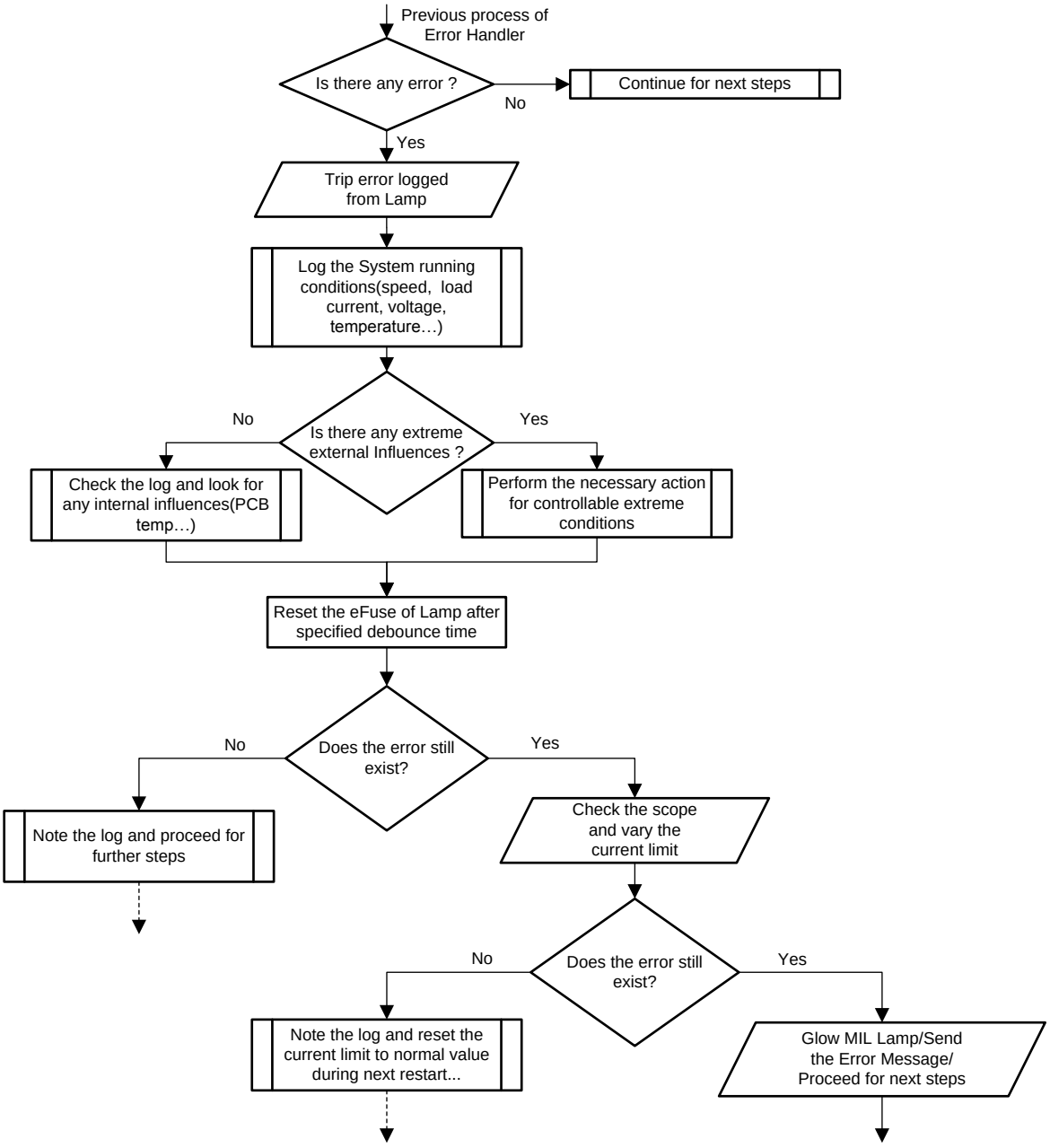


Figure 13. Flowchart of Error Handling in eFuse

The multichannel eFuse does not only improve the diagnosis of fuse box system. It can also handle errors occurring in other parts of the system, which completely depends on system architecture.

For example, in an automotive system a relay or load is connected to a battery with a fuse, and it is controlled by a low-side switch in control units as shown in Figure 14.

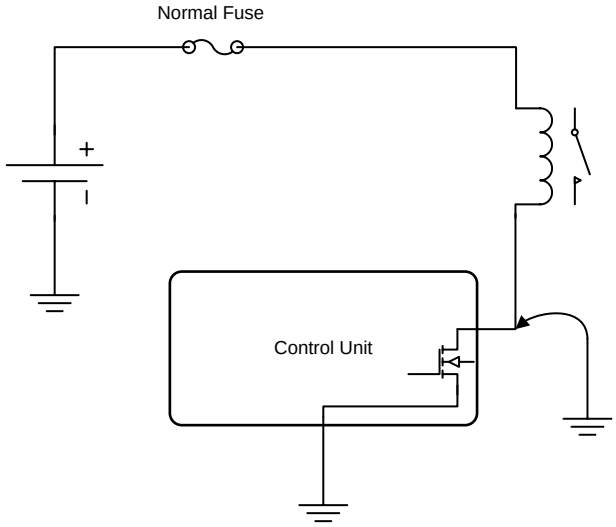


Figure 14. Normal Fuse SCG

Due to vibrations or faulty conditions, if the low side of the load is short circuit to GND (SCG), the fuse will not blow but the system will fail, which is not controllable by any electronics. These failures are be diagnosed and reported as errors, and the system will halt to avoid any damage, which inconveniences customers and increases service costs. To mitigate the risk, the system needs dual-side load control or other architecture, which will increase system cost.

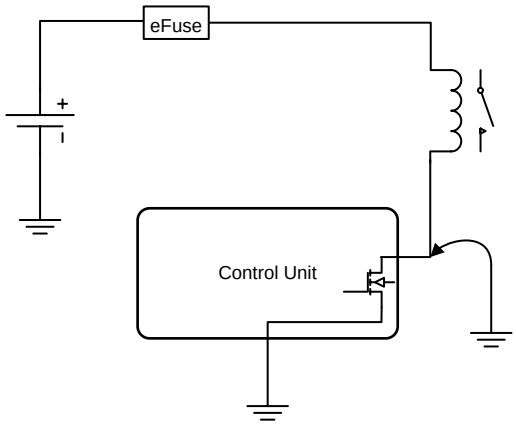


Figure 15. eFuse With SCG

In a multichannel eFuse system, if the relay or load has SCG at the low side, then the eFuse circuit can be turned off based on system demand (pre-configured for necessary eFuses). The eFuse can be used as a high-side switch and keep the system in a running state to avoid a complete system breakdown. The design of the subsystem can be handled at a low cost compared to other topology changes required for the system.

By deploying various load control options and diagnoses, the multichannel eFuse system improves the ASIL standards and safety in the automotive system.

4.1.4 Operating Current

As mentioned in Section 2, the operating current of the load is very high compared to the fuse rating. The fuse rating could be around 66% above the load current. This can be reduced to as low as 10% in the multichannel eFuse design. By selecting a shunt resistor with a low TCR, there is very little variance of resistance with respect to temperature. It will have an advantage of building an eFuse that has little impact due to changes in temperature.

The following factors improve the operating current of the eFuse in the multichannel system:

- Selecting switching components with low losses is necessary to reduce the power dissipation of the system, which also improves efficiency.
- Selecting a shunt resistor with low TCR offers a little variance in resistance for a change in ambient and body temperatures.
- Designing the layout with a necessary heat sink allows the design to extract heat from the PCB and series path components.

5 Getting Started: Hardware

To get started with the TIDA-00795 board, prepare the setup with an emphasis on safety.

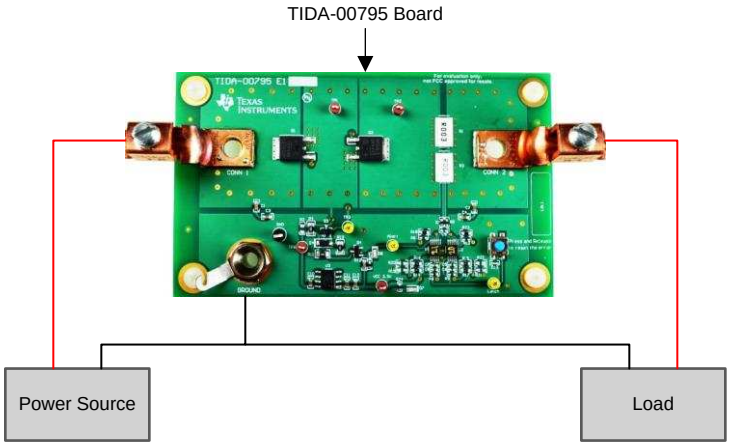


Figure 16. eFuse Setup

5.1 Setup Procedure and Precautions

1. Calculate the values of components for R1,R3 (shunt resistors) and R18, R23 for the desired current limit.
2. Check the desired hysteresis to be set for U1,U2 (INA300) and populate the components R14, R19, R15, and R22, accordingly.
3. Set the delay time of U1,U2 by the appropriate population of resistors R16, R20, R17, and R21.
4. Parameters such as current limit, hysteresis, and delay time can be chosen independently for U1 and U2.
5. Take care while selecting the wires. The current-carrying capability of the wires must be above the max current trip value set to U1 and U2. The ground line from the source to the load must always have a direct connection. The ground line to the TIDA-00795 eFuse is only for biasing. Be careful when wiring to avoid any damages to the TIDA-00795 eFuse boards.
6. Choose the power source and loads based on the type of tests planned on the TIDA-00795 eFuse.
7. If load or source does not have control switches to turn on or off the circuit, implement relevant switches in a series path to the TIDA-00795 eFuse board.
8. Connect the oscilloscope to necessary test points for voltage measurements. Place the current probe appropriately near to the source on either the positive or ground line.
9. Within the operating voltage range, set voltage in the power source. Based on the type of test, set the current limit value in power source.
10. Set the mode appropriately in the load based on the load current and type of test.
11. Use the push button switch on the TIDA-00795 board to reset the eFuse. *Do not press the push button continuously when a load current is more than the current trip value as this could damage components on the board and load.*
12. The latch pin of U1 and U2 is accessible to control by other circuits through test pin TP8. Reset U1 and U2 by pulling low for at least 20 μs. The pulse generated from the signal generator or microcontroller can be interfaced to latch pins through TP8.
13. Perform the necessary tests on the TIDA-00795 device. Take care with the setup and configuration while performing short circuit tests.

6 Test Setup

Initial tests of the automotive eFuse are done with the DC power supply and load. The eFuse is placed in between the power supply and load for a positive connection. Ground connection from the load is directly connected to the power source. For the eFuse internal components to function, a ground connection is placed between the power supply and eFuse. Be careful to avoid the ground current flowing through the PCB.

A lambda power supply has been chosen as the source. The current limit parameter in the source has been set to the maximum. Voltage of the source and current limit on the load has been varied to get the desired performance of eFuse. During the test, the current limit resistor (R_X) has been changed to get the performance details of the eFuse at different current trip values. DYNALOAD settings have been changed manually to introduce constant current limit, short circuit, and different loading behaviors.

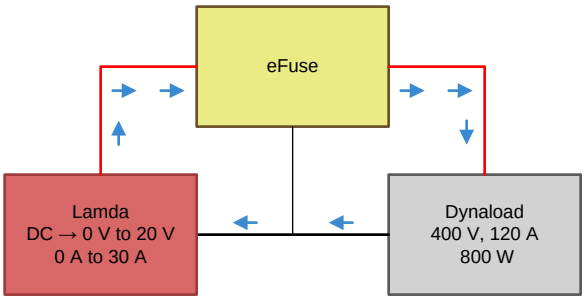


Figure 17. Test Setup

7 Test Data

Tests are conducted on the eFuse to note the performance and its behavior during normal and overload conditions. For better understanding, the test results are classified in the following subsections.

7.1 General Tests

7.1.1 Startup Behavior

Voltages at the source were increased in steps to closely monitor the behavior of circuit. Load is configured as a 5-A constant current.

Table 4. Startup Behavior

SOURCE	TP1 (SOURCE Q1 AND Q2)	TP2 (DRAIN OF Q2)	TP3 (GATE OF Q1 AND Q2)	VCC 3.3	COMMENT
1 V	737.7 mV	0 V	327 mV	0 V	Output OFF
1.5 V	1.231 V	0 V	732.7 mV	67.59 mV	Output OFF
2 V	1.777 V	0 V	1.309 V	254 mV	Output OFF
2.5 V	2.21 V	0 V	1.731V	398 mV	Output OFF
2.78 V	2.78 V	2.762 V	123.7mV	2.527 V	Output ON
4 V	3.919 V	3.829 V	361.3 mV	3.29 V	Output ON

The operating voltage of the LM9036 is 2.5 to 40 V. The LM9036 output stays low until the input voltage reaches 2.5 V. When battery voltage is 2.75 V (0.25-V Schottky diode, 2.5-V LM9036), the LM9036 turns on, which in turn supplies the internal circuit. Voltage at the VCC3.3V pin is above the threshold limits of Q4. If Q4 is on as explained in Section 3.2.1, both series path MOSFETs Q1 and Q2 will turn on.

The operating voltage of (V_{MIN} = 2.5 V) the LM9036 helps the eFuse to operate. When the LM9036 turns on, the battery voltage is greater than 2.5 V. The gate-to-source voltage of Q1 and Q2 is greater than 2.2 V, which is greater than the max gate-to-source threshold voltage of Q1 and Q2. In a short time, Q1 and Q2 are driven to saturation mode. This process avoids high power dissipation in the ohmic region of Q1 and Q2 along with load currents.

The minimum operating voltage of the INA300-Q1 is 2.7 V. Overcurrent limit protection is not activated below the minimum supply voltage. Be sure to consider this parameter in the design. In the multichannel eFuse system, the design of the power supply section must have relevant safety flags in place, which ensure flawless operation of circuits.

7.1.2 Run Behavior

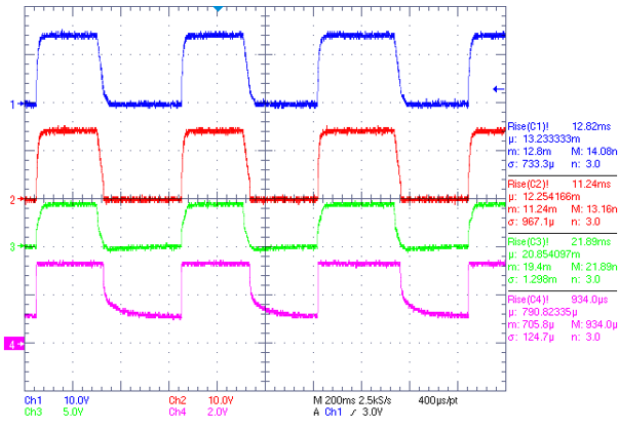


Figure 18. Run Behavior at 5 A

Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: VCC3.3
CH4: TP3 (Gate of Q1 and Q2)

The load is configured in a 5-A constant current mode.

NOTE: Source is turned on and off manually to check the behavior of the circuit.

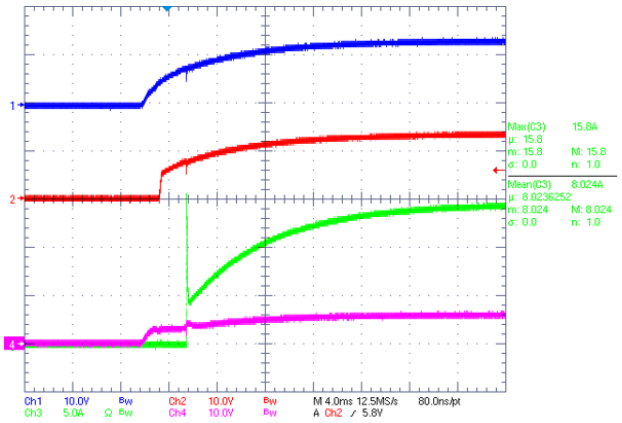
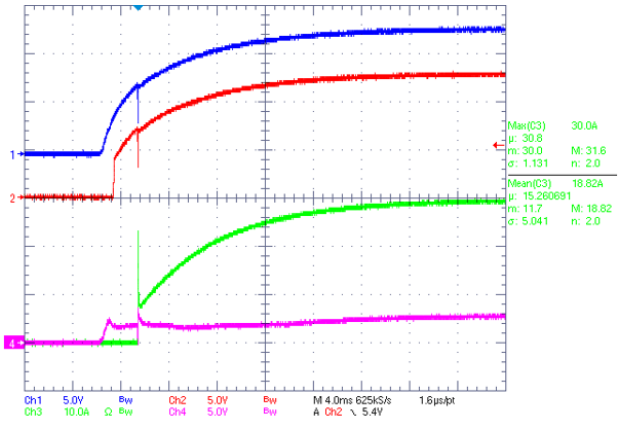


Figure 19. Startup Behavior at 15 A

Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

Configured trip current = 15.86 A
Load current = 15 A

NOTE: Startup behavior of the circuit for a load current of 15 A, peak input inrush current is 15.8 A.

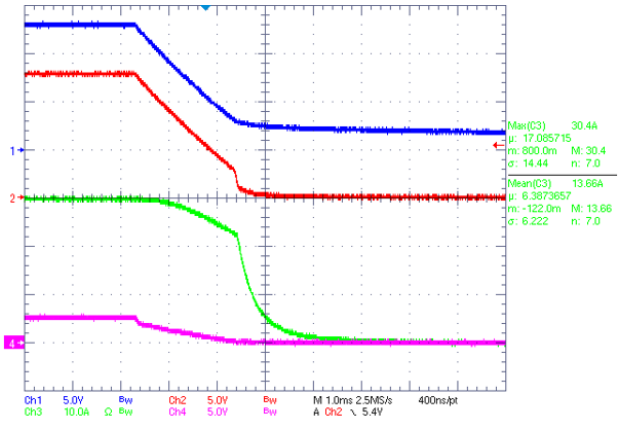


Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

Configured trip current = 31.6 A
Load current = 30 A

NOTE: Startup behavior of circuit for a load current of 30 A, peak input inrush current is 24 A.

Figure 20. Startup Behavior at 30 A



Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

NOTE: eFuse behavior when the source is turned off manually is 30 A.

Figure 21. Turned-off Behavior at 30 A

7.1.3 eFuse Characteristics

Electrical parameters of the eFuse series path components are checked by maintaining a constant voltage at the source and varying the load current. Table 5 shows the results:

Table 5. eFuse Behavior at Various Loads

CURRENT (A)	T1 INPUT (V)	TP1 (V)	TP2 (V)	T2 OUTPUT (V)	POWER DISSIPATION (W)
5	14.00	13.98	13.96	13.95	0.25
10	14.00	13.96	13.92	13.89	1.10
15	14.00	13.94	13.87	13.85	2.25
20	14.05	13.96	13.86	13.81	4.80
25	14.05	13.91	13.79	13.75	7.50
30	14.03	13.89	13.74	13.69	10.20

Figure 22 presents the data listed in Table 5.

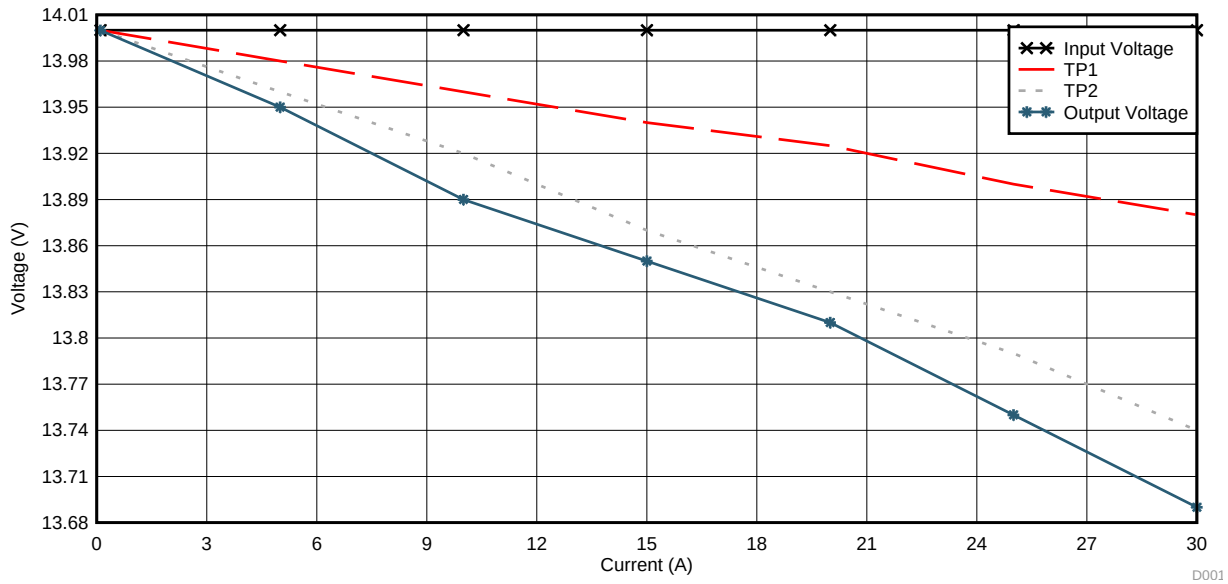


Figure 22. Internal Behavior at Various Load Currents

eFuse design resistance = 4.3 mΩ (Q1) + 4.3 mΩ (Q2) + 1.5 mΩ (shunt resistor) = 10.1 mΩ ± tolerances (design). The average eFuse resistance is 11.05 mΩ (measured).

There is a scope to reduce the series resistance by selecting appropriate components. This series resistance can be changed based on application and accuracy requirements.

7.2 Reliability Test

7.2.1 Reverse Polarity Test

Reverse polarity test was performed on the eFuse board. A positive connection of the power supply is connected to J1 (Ground), and a negative connection of the power supply is connected to T1.

- T1 versus Ground: –14.21 V
- TP1 versus Ground: –0.096 V
- TP3 versus Ground: 0.023 V
- TP6 versus Ground: –4.5 V
- VCC3.3 versus Ground: –0.425 V
- Alert versus Ground: –0.377 V

Observations:

- No damage to components.
- LED stays in off state.
- Output connections are overloaded to cross check the circuit tolerance.
- Output connections are shorted, no change in circuit behavior.
- Circuit performance met expectations.

The design performance of the eFuse is tested in the operating voltage range of the eFuse:

- Reverse voltage = –20 V
- Positive voltage = 40 V
- Load current = 5 A

Based on theory and practical tests on the eFuse board, bidirectional eFuse characteristics are plotted in Figure 23.

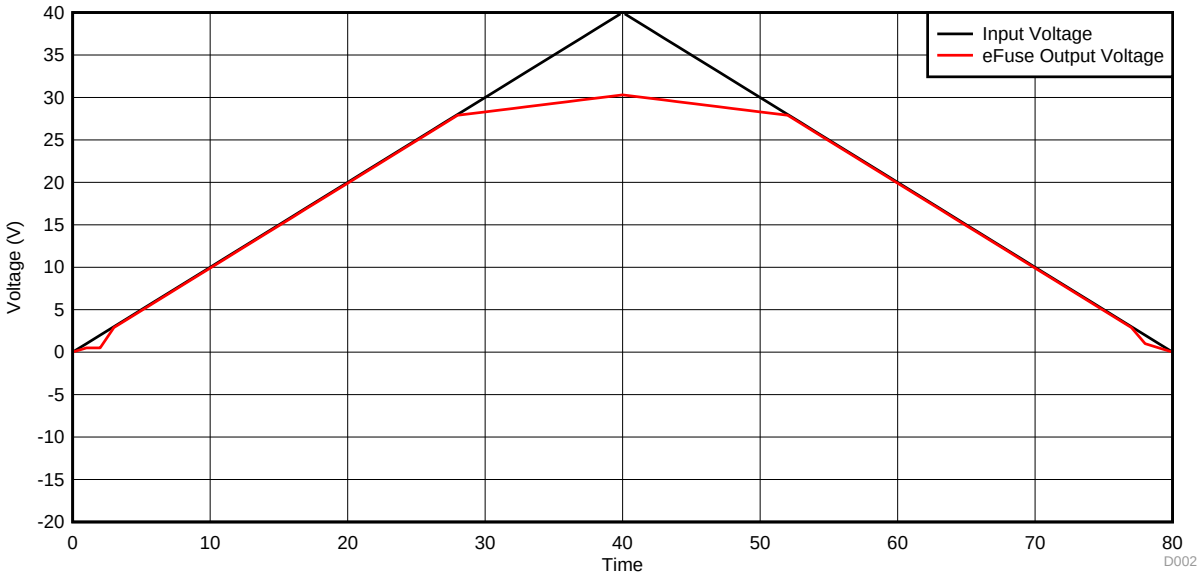
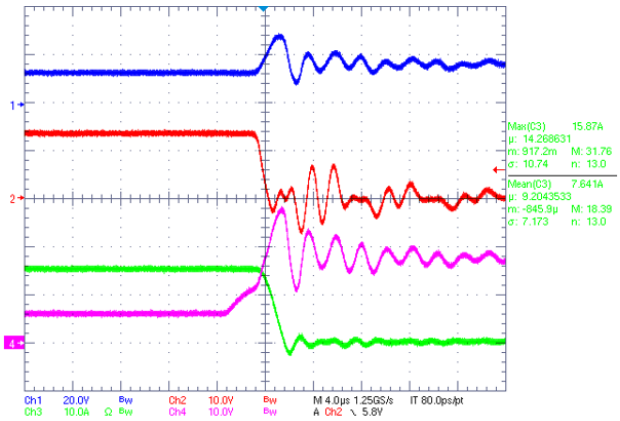


Figure 23. eFuse Performance Characteristics

NOTE: System performance may change by varying source and loading conditions.

7.2.2 Overload and Short Circuit Test



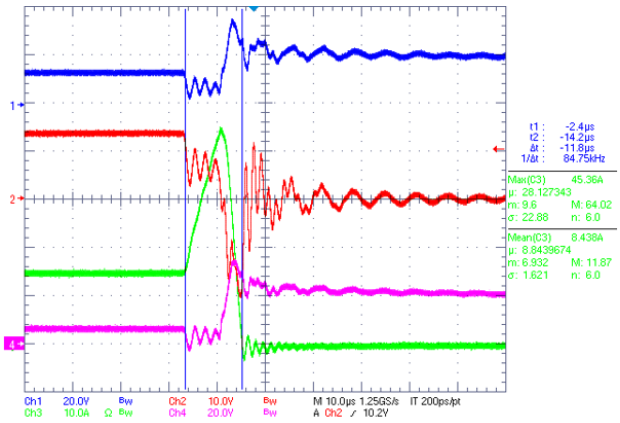
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 1185 Ω ± 0.1%

Configured trip current = 15.86 A
Actual trip current = 15.87 A

Error = 0.063%

Figure 24. Trip Behavior at 15 A



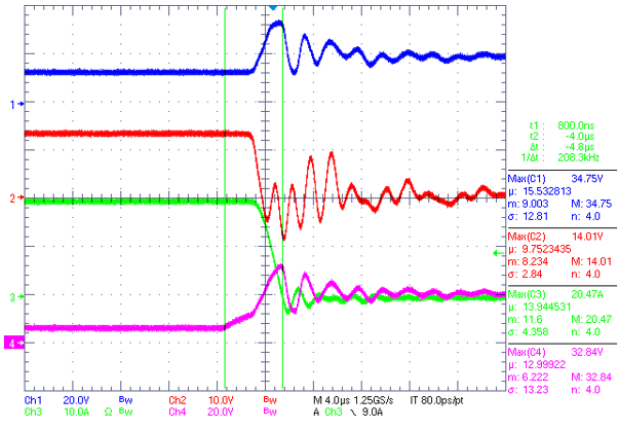
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 1185 Ω ± 0.1%

Configured trip current = 15.86 A

NOTE: Load short to ground during the eFuse running state.
Delay time = 11.8 us

Figure 25. Runtime Short Behavior at 15 A



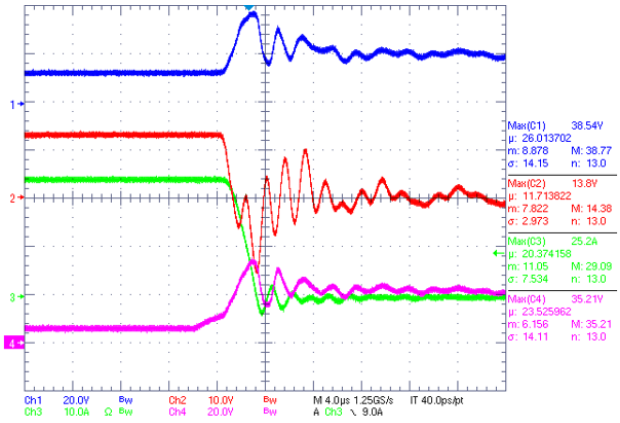
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 1580 Ω ± 0.1%

Configured trip current = 21.066 A
Actual trip current = 20.47 A

Error = 2.82%

Figure 26. Trip Behavior at 20 A



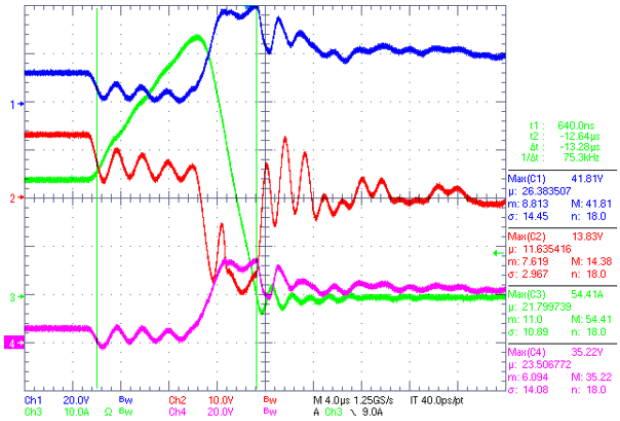
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 1975 Ω ± 0.1%

Configured trip current = 25.53 A
Actual trip current = 25.2 A

Error = 1.07%

Figure 27. Trip Behavior at 25 A



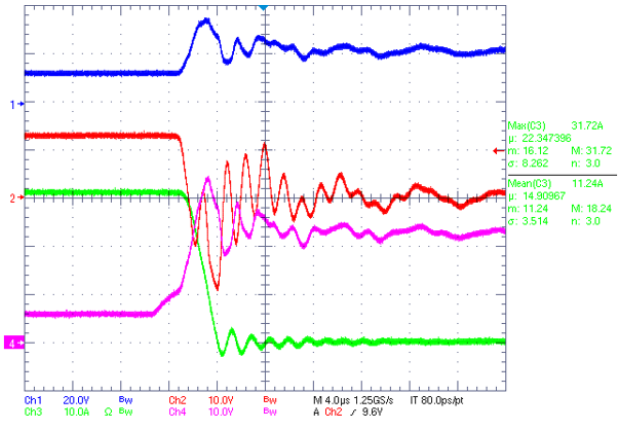
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 1975 Ω ± 0.1%

Configured trip current = 25.53 A

NOTE: Load is short to ground during the eFuse running state. Delay time ≤ 13.28 us

Figure 28. Runtime Short Behavior at 25 A



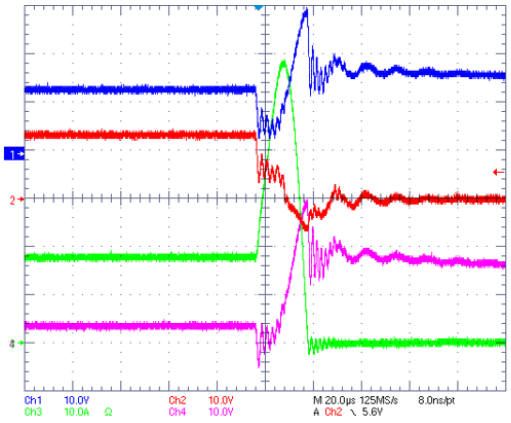
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 2370 Ω ± 0.1%

Configured trip current = 31.61 A
Actual trip current = 31.72 A

Error = 0.33%

Figure 29. Trip Behavior at 30 A



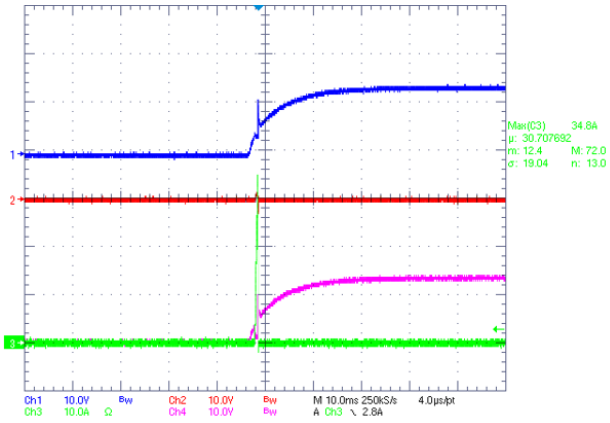
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 2370 Ω ± 0.1%

Configured trip current = 31.6133 A

NOTE: Load is short to ground during the eFuse running state.

Figure 30. Runtime Short Behavior at 30 A



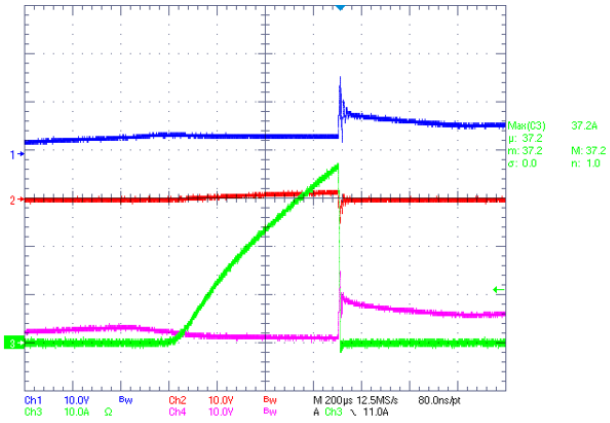
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 2370 Ω ± 0.1%

Configured trip current = 31.6133 A

NOTE: eFuse is turned on when load is short to ground; behavior of the eFuse is as expected.

Figure 31. eFuse Behavior at Load Short



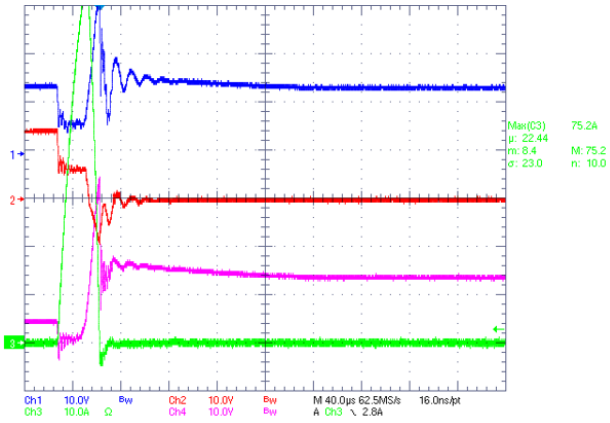
Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 2370 Ω ± 0.1%

Configured trip current = 31.6133 A

NOTE: eFuse is turned on when load is short to ground; behavior of the eFuse is as expected. (Zoomed picture)

Figure 32. eFuse Behavior at Load Short



Ch1: TP1 (Source of Q1 and Q2)
CH2: TP2 (Drain of Q2)
CH3: Load current
CH4: TP3 (Gate of Q1 and Q2)

R18 and R23 = 2370 Ω ± 0.1%

Configured trip current = 31.6133 A

NOTE: The eFuse load is short to ground while there is no load current; behavior of the eFuse is as expected.

Figure 33. Runtime Short Behavior at No Load

7.3 Battery Test

The test setup has been prepared to perform battery tests for the TIDA-00795. Take care while handling the battery and interconnections.

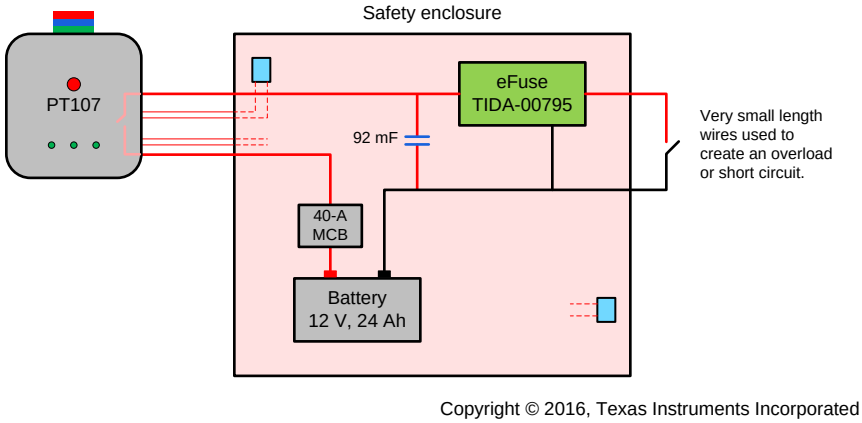


Figure 34. Battery Short Circuit Test

Safety of the operator and battery are given high priority for the entire setup. The PT107 has the intelligence to monitor and control the setup. The battery and eFuse are placed in a safety enclosure. Connections of the system are assembled as shown in Figure 34. A 12-V/24-Ah electric vehicle valve regulated lead acid (VRLA) battery (non-spillable) has been used to perform the test.

A capacitor of 92 mF was placed next to the eFuse along with shorter length wires to create overload and short-circuit conditions. Interlock signals of the safety enclosure is connected to the PT107. The device closes the battery connections only when the safety enclosure is properly closed.

A 40-A MCB is connected in series to the battery for additional protection and series switch. The eFuse (TIDA-00795) has been placed in series, just like any other fuse that breaks during overload and short-circuit conditions:

- Current limit: 30 A
- Delay time: 10 µs
- Hysteresis: 2 mV
- Alert pin: Latch mode

If the safety enclosure is connected and closed properly, the PT107 will close the battery connections. Once the PT107 is turned on, the eFuse will be powered up. The output terminal of eFuse can be referred as battery positive connection (Neglecting wire and eFuse series resistance). Positive connections from the safety enclosure and the ground connection of the battery are safe to handle electrical error conditions.

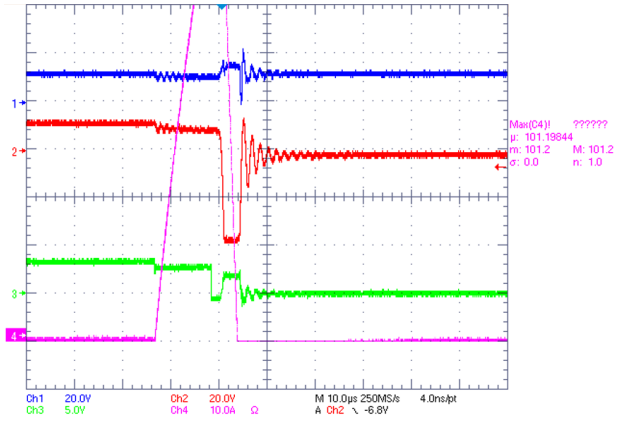


Figure 35. Battery Short 1

CH1: V_{IN} (Drain of Q1)
CH2: TP2 (Drain of Q2)
CH3: TP4 (Alert)
CH4: Load current

NOTE: Output terminals are shorted by using small cables. The eFuse has been tripped as per the design. The Alert pin turns OFF (pull down) close to 10 µs after the short circuit. Q2 turns OFF following the alert signal. The peak load current during the 10-µs delay time is > 100 A. The eFuse is functioning normal upon the reset.

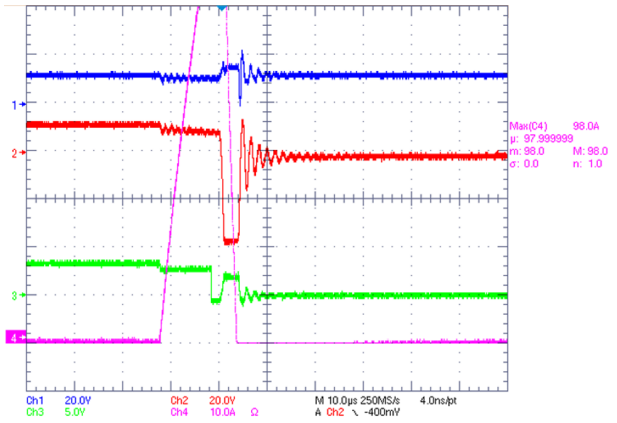


Figure 36. Battery Short 2

CH1: V_{IN} (Drain of Q1)
CH2: TP2 (Drain of Q2)
CH3: TP4 (Alert)
CH4: Load current

NOTE: Output terminals are shorted by using small cables. The eFuse has been tripped as per the design. The Alert pin turns OFF (pull down) close to 10 µs after the short circuit. Q2 turns OFF following the alert signal. The peak load current during the 10-µs delay time is > 98 A. The eFuse is functioning normal upon the reset.

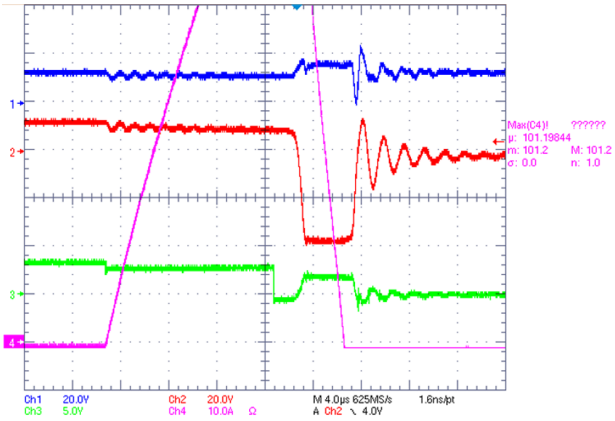


Figure 37. Battery Short 3

CH1: V_{IN} (Drain of Q1)
CH2: TP2 (Drain of Q2)
CH3: TP4 (Alert)
CH4: Load current

NOTE: Output terminals are shorted by using small cables. The eFuse has been tripped as per the design. When the load current is > 30 A, the Alert pin turns OFF (pull down) in 10 µs. Q2 turns OFF following the alert signal. The peak load current during the 10-µs delay time is > 100 A. The eFuse is functioning normal upon the reset.

Battery short circuit test results show the reliability of the eFuse. The response time and accuracy of the INA300-Q1 are advantageous to facilitate broad automotive protection applications from 5 to 15 A of high-side protection switches (eFuse) to 15 to 50 A of reliable independent eFuse.

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00795.

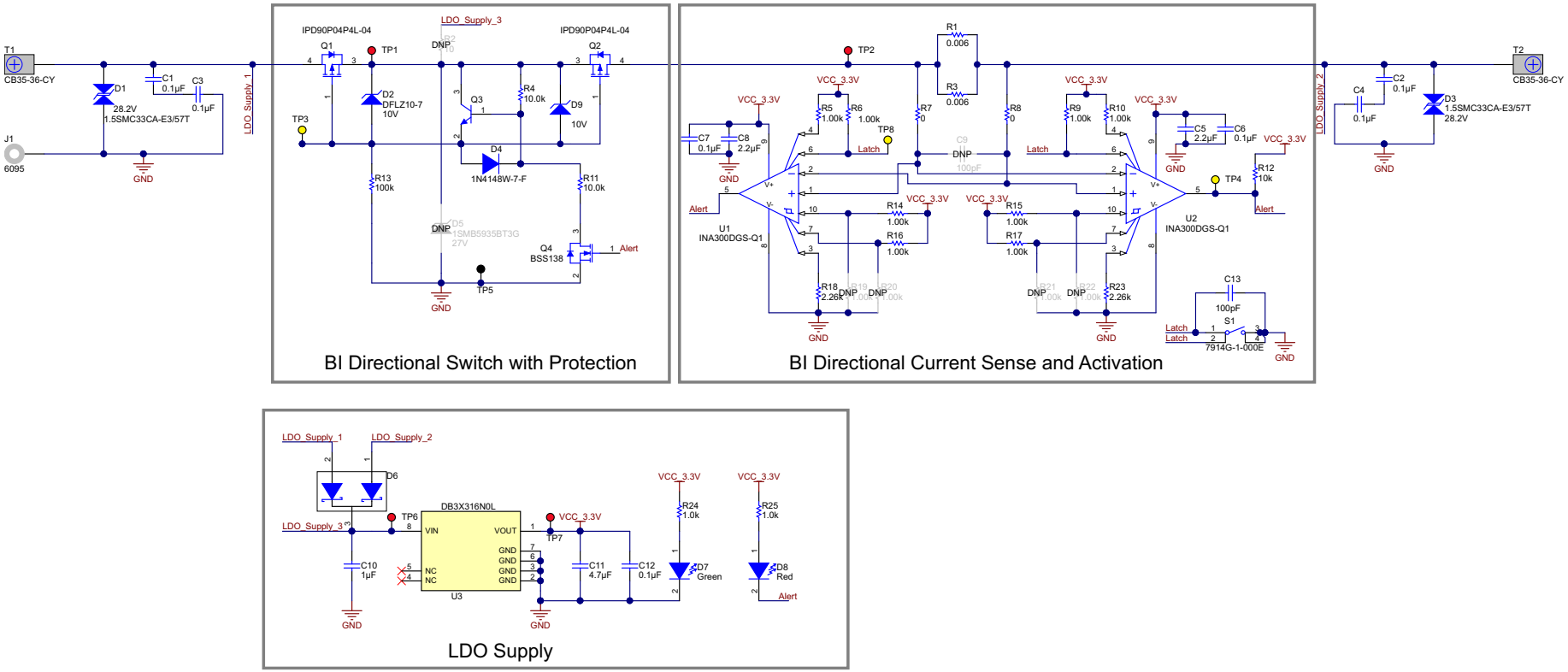


Figure 38. Automotive Precision eFuse Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00795.

Table 6. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PARTNUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		TIDA-00795	Any
C1, C2, C3, C12	4	0.1uF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R	603	GRM188R72A104KA35J	MuRata
C4	1	0.1uF	CAP, CERM, 0.1 µF, 6.3 V, +/- 10%, X7R,	603	GRM188R70J104KA01D	MuRata
C5, C8	2	2.2uF	CAP, CERM, 2.2 µF, 25 V, +/- 10%, X5	402	C1005X5R1E225K050BC	TDK
C6, C7	2	0.1uF	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1,	402	C0402C104K4RACAUTO	Kemet
C10	1	1uF	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R	603	UMK107AB7105KA-T	Taiyo Yuden
C11	1	4.7uF	CAP, CERM, 4.7 µF, 25 V, +/- 10%, X5R,	603	GRM188R61E475KE11D	MuRata
D1, D3	2	28.2V	Diode, TVS, Bi, 28.2 V, 1500 W, (no polarity)	DO-214AB (no polarity)	1.5SMC33CA-E3/57T	Vishay-Dale
D2, D9	2	10V	Diode, Zener, 10 V, 1 W	PowerDI123	DFLZ10-7	Diodes Inc.
D4	1	100V	Diode, Ultrafast, 100 V, 0.15 A	SOD-123	1N4148W-7-F	Diodes Inc.
D6	1	30V	Diode, Schottky, 30 V, 0.1 A	SOT-23	DB3X316N0L	Panasonic
D7	1	Yellow/green	LED, Yellow/green, SMD	0402 LED	SML-P12MTT86	Rohm
D8	1	Red	LED, Red, SMD	0.8x1.6mm	HSMC-C190	Avago
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Standard Banana Jack, Uninsulated	Keystone_6095	6095	Keystone
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
Q1, Q2	2	-40V	MOSFET, P-CH, -40 V, -90 A, AEC-Q101, DPAK	DPAK	IPD90P04P4L-04	Infineon Technologies
Q3	1	45 V	Transistor, NPN, 45 V, 0.5 A, SOT-23	SOT-23	BC817-16LT1G	ON Semiconductor
Q4	1	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R1, R3	2	0.003	RES, 0.003, 1%, 4 W, 3015 WIDE	3015 WIDE	KRL7638-C-R003-F-T1	Susumu Co Ltd
R4	1	40.0k	RES, 40.0k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	CRCW080540K0FKEA	Vishay-Dale
R5, R6, R9, R10	4	1.00k	RES, 1.00 k, 1%, 0.1 W, 0402	402	ERJ-2RKF1001X	Panasonic
R7, R8	2	0	RES, 0, 5%, 0.063 W, 0402	402	CRCW04020000Z0ED	Vishay-Dale
R11	1	10.0k	RES, 10.0 k, 1%, 0.125 W, 0805	805	CRCW080510K0FKEA	Vishay-Dale

Table 6. BOM (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PARTNUMBER	MANUFACTURER
R12	1	10k	RES, 10 k, 5%, 0.1 W, 0603	603	RC0603JR-0710KL	Yageo America
R13	1	100k	RES, 100 k, 1%, 0.125 W, 0805	805	CRCW0805100KFKEA	Vishay-Dale
R14, R15, R16, R17	4	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	603	CRCW06031K00FKEA	Vishay-Dale
R18, R23	2	2.26k	RES SMD 1.18KOHM 0.1% 1/10W, 0603	603	ERA-3AEB1181V	Panasonic
R24, R25	2	1.0k	RES, 1.0 k, 5%, 0.063 W, 0402	402	CRCW04021K00JNED	Vishay-Dale
S1	1		Switch, Tactile, SPST-NO, 0.1A, 16V, SMT	4.93x4.19x6.2 mm	7914G-1-000E	Bourns
T1, T2	2	50A	Terminal 50A Lug	CB35-36-CY	CB35-36-CY	Panduit
TP1, TP2, TP6, TP7	4	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP3, TP4	2	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP5	1	Black	Test Point, Compact, Black, TH	Black Compact Testpoint	5006	Keystone
U1, U2	2		High or Low Side, Bi-Directional Zerø-Drift Series CURRENT SENSE COMPARATOR, DSQ0010A	DSQ0010A	INA300AIDSQR	Texas Instruments
U3	1		Ultra-Low Quiescent Current Voltage Regulator, D0008A	D0008A	LM9036QMX-3.3/NOPB	Texas Instruments

8.3 PCB Layout Recommendations

The PCB layout has to be done with appropriate measures to ensure the smooth operation of eFuse functionality.

- Check the series path tracks for power dissipation, and set the layer thickness and area appropriately.
- Place vias appropriately to share the current on both sides of PCB.
- Place D1 and D3 very close to the connector.
- Place D2 and D9 close to Q1 and Q2 as shown in Figure 39:

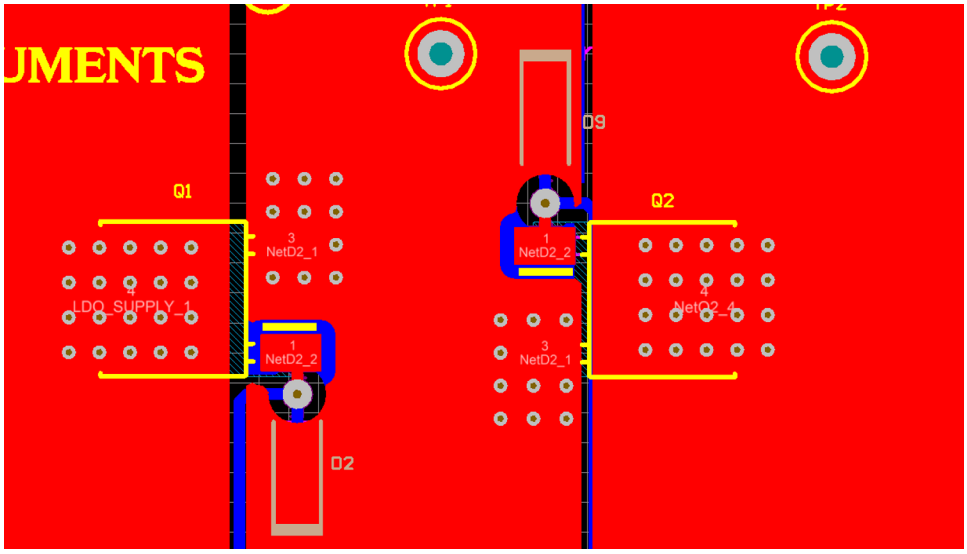


Figure 39. Positioning of Power MOSFETs

- Place decoupling capacitors near to ICs.
- Always ensure that the shunt resistor is Kelvin-connected to U1 and U2.

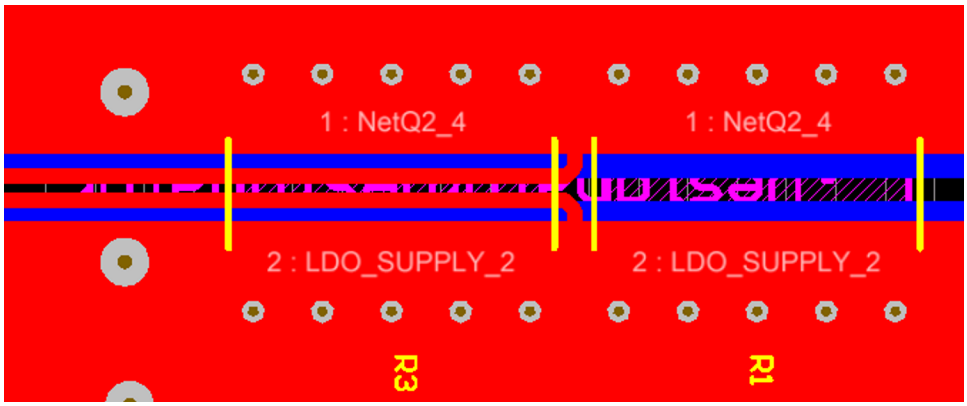


Figure 40. Kelvin Connections for Tapping Current Sense

- Keep shunt measurement traces as short as possible.
- Balance shunt measurement traces as much as possible.
- Place the current sensing device and shunt on the same side of the PCB.
- For U1 and U2, check the placement guidelines for the INA300. Place the R18 and R23 current sense resistors at U1 and U2. The ground connection from R18 and R23 should have less resistance to the ground connection of U1 and U2.

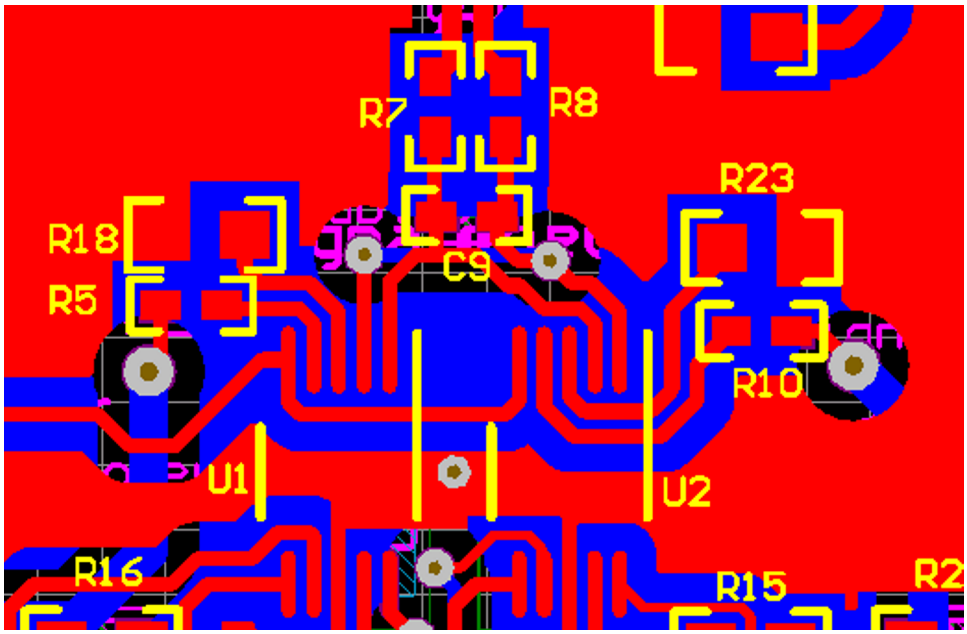


Figure 41. Placement of INA300-Q1

8.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00795.

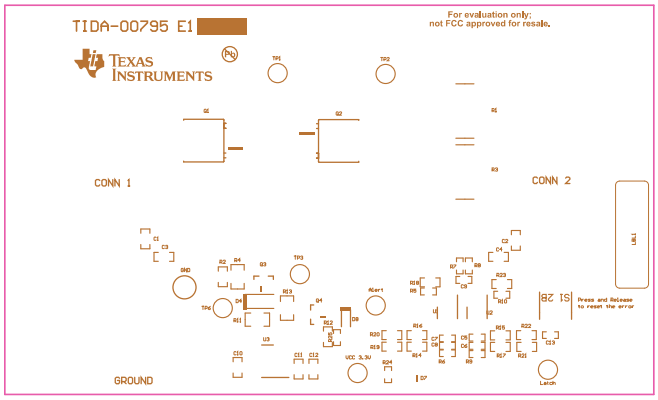


Figure 42. Top Overlay

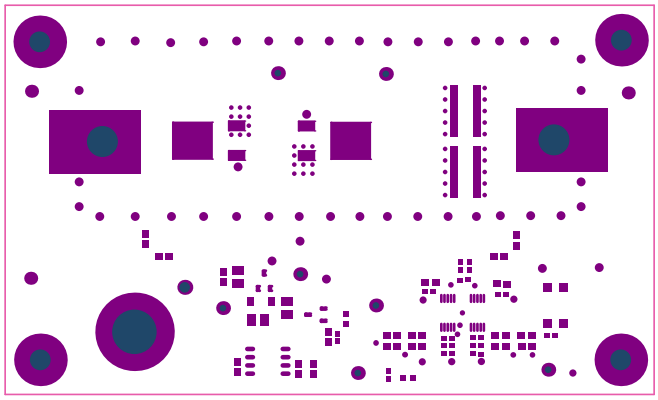


Figure 43. Top Solder Mask

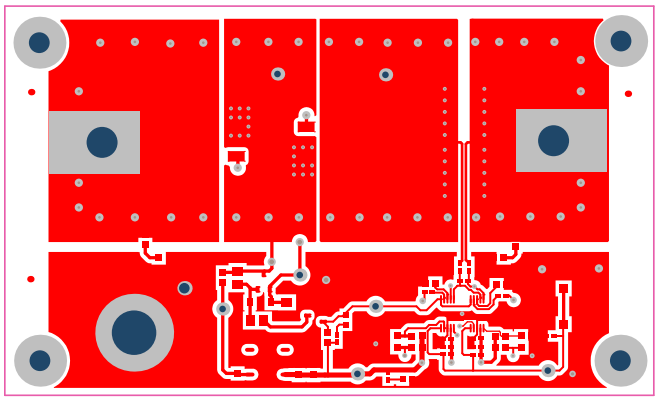


Figure 44. Top Layer

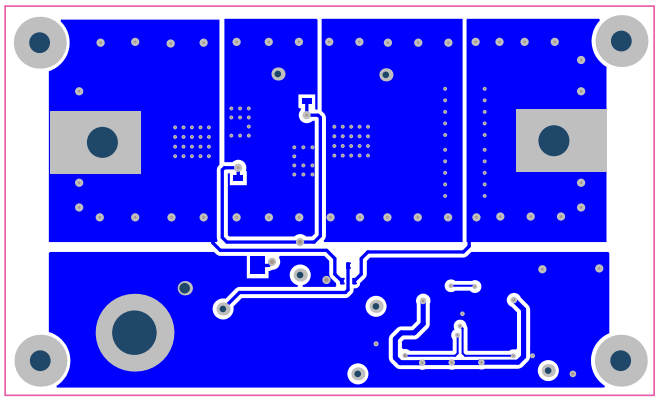


Figure 45. Bottom Layer

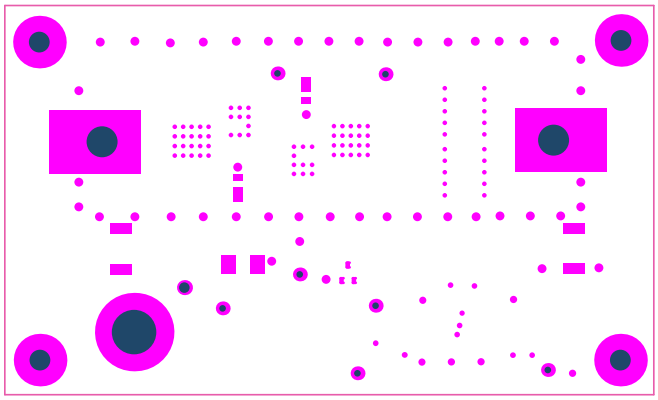


Figure 46. Bottom Solder Mask

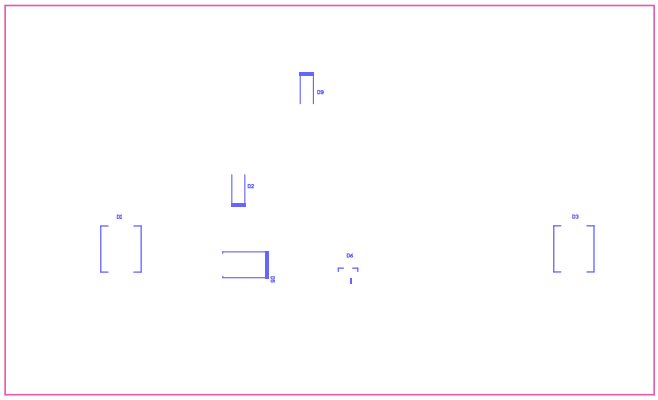


Figure 47. Bottom Overlay

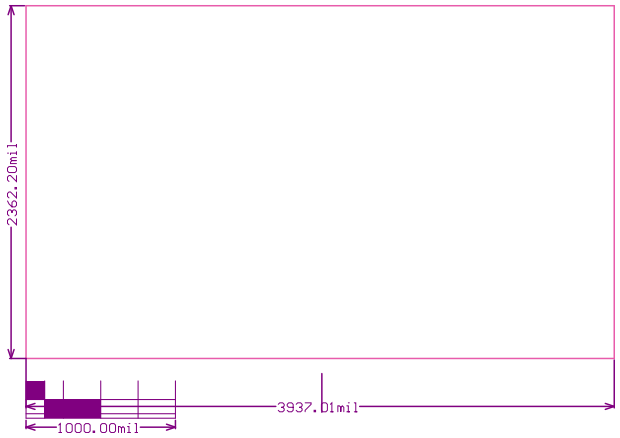


Figure 48. Mechanical Dimensions

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00795.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00795.

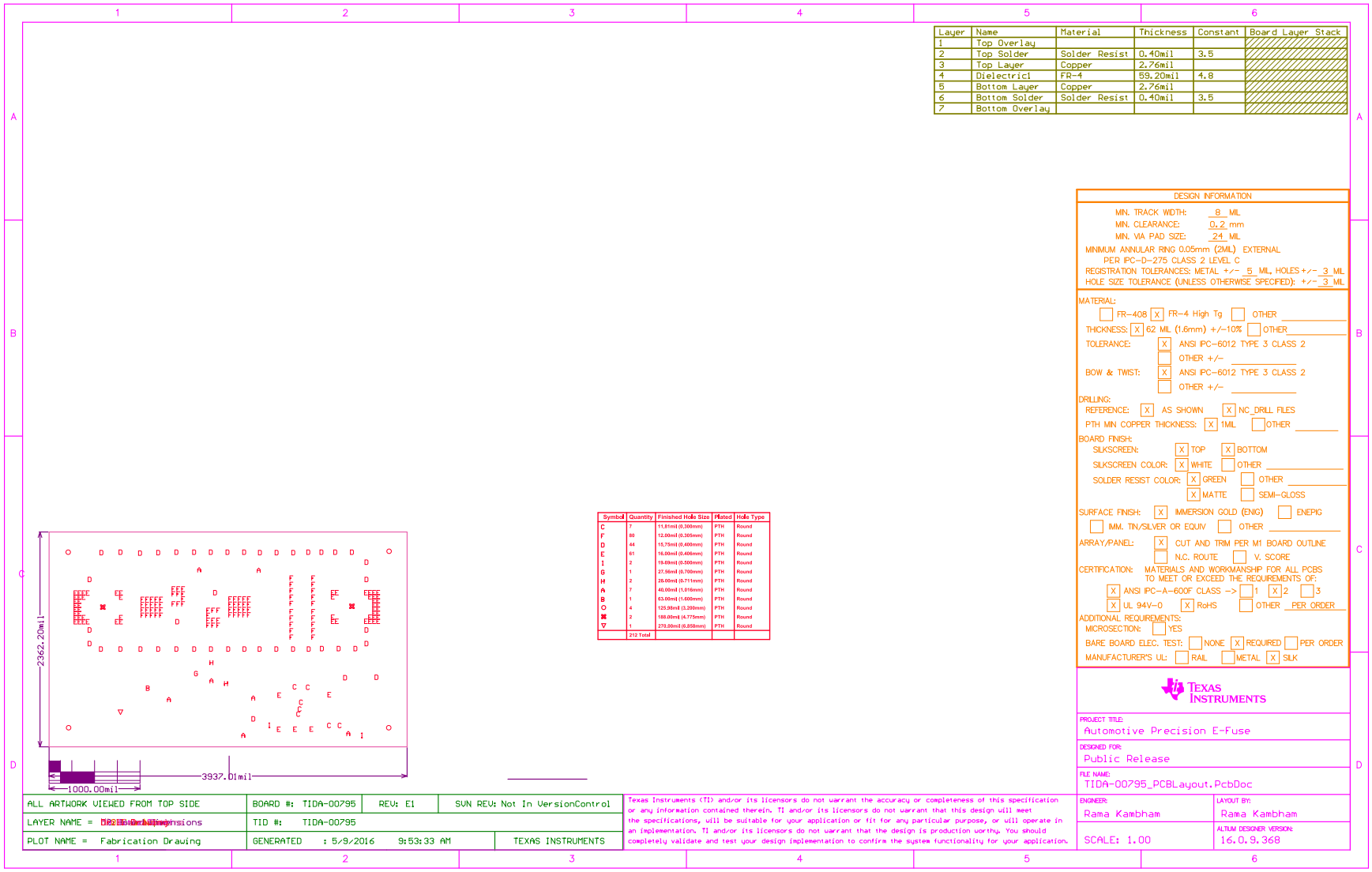


Figure 49. Fabrication Drawing

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00795.

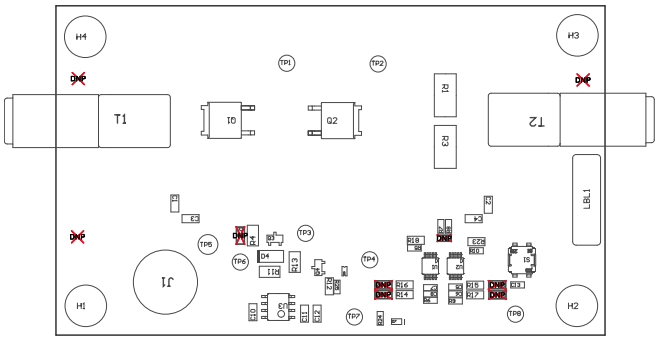


Figure 50. Top Assembly Drawing

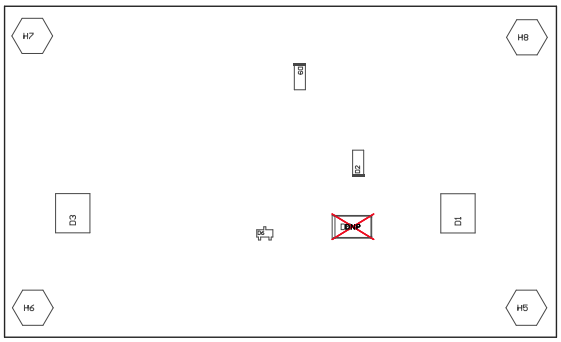


Figure 51. Bottom Assembly Drawing

9 References

1. Texas Instruments, *Introduction to optimized over-current detector INA300*, Video (Link)
2. Texas Instruments, *Current Shunt Monitors*, Brochure (SLYB194)

10 About the Author

RAMA KAMBHAM (Rama Chandra Reddy) is an automotive system engineer working in Texas Instruments Deutschland. Rama brings to this role his extensive experience in Battery Management Systems and Engine Management Systems in the automotive domain. Rama earned his bachelor of engineering degree from Osmania University Hyderabad, India.

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2016) to B Revision	Page
• Changed waveform	1
• Deleted High-Voltage EVM Disclaimer from translation	2
• Changed current limiting resistors for U1 and U2 from R18 and R19 to R18 and R23	7
• Changed information on eFuse topologies	14
• Changed title of Table 5	27
• Added Section 7.3	34
• Changed range from 1 to 5 A	36
• Changed range from 30 to 50 A	36

Revision A History

Changes from Original (April 2016) to A Revision	Page
• Changed from preview page	1

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