TI Designs

Optimized Automotive 1-MP Camera Module Design for Uncompressed Digital Video Over Coax

TEXAS INSTRUMENTS

Description

The TIDA-00262 reference design is a high-speed serial video interface to connect a remote automotive camera module to a display or machine vision processing system. It uses TI's FPD-Link III SerDes technology to transmit uncompressed megapixel video data, bidirectional control signals and power either over shielded twisted pair or coax cable.

Resources

|		
TIDA-00262	Camera Module	Design Folder
DS90UB913A-Q1	FPD-Link III Serializer	Product Folder
TPS62170-Q1	Buck Converter	Product Folder
TPS62231-Q1	Buck Converter	Product Folder
TPS3836E18-Q1	Voltage Supervisor	Product Folder

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Features

- Space-Optimized Design Fits on Single PCB 20×20 mm
- Power Supply Optimized for Small Size and High Efficiency
- 1-MP Image Sensor AR0140AT From ON Semiconductor Providing 10- or 12-Bit Raw Image Data
- Single Rosenberger Fakra Coax Connector for Digital Video, Power, Control and Diagnostics
- Diagnostic and Built-in Self-Test (BIST) for ASIL B Applications
- Includes Design Considerations and BOM Analysis

Applications

- ADAS Vision Systems
- Surround View Systems
- Rear Camera
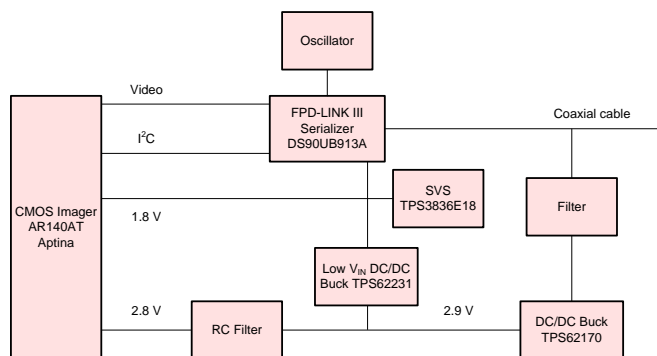
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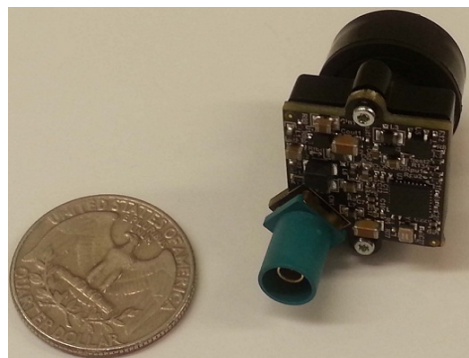
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1 System Overview

1.1 *System Description*

For many automotive safety systems, small cameras are required. This TI Design addresses these needs by combining a 1-megapixel imager with a 1.4-Gbit/s serializer and providing the necessary power supply for both. All of this functionality is contained on a 20×20-mm circuit card. The only connection required by the system is a single 50-Ω coaxial cable.
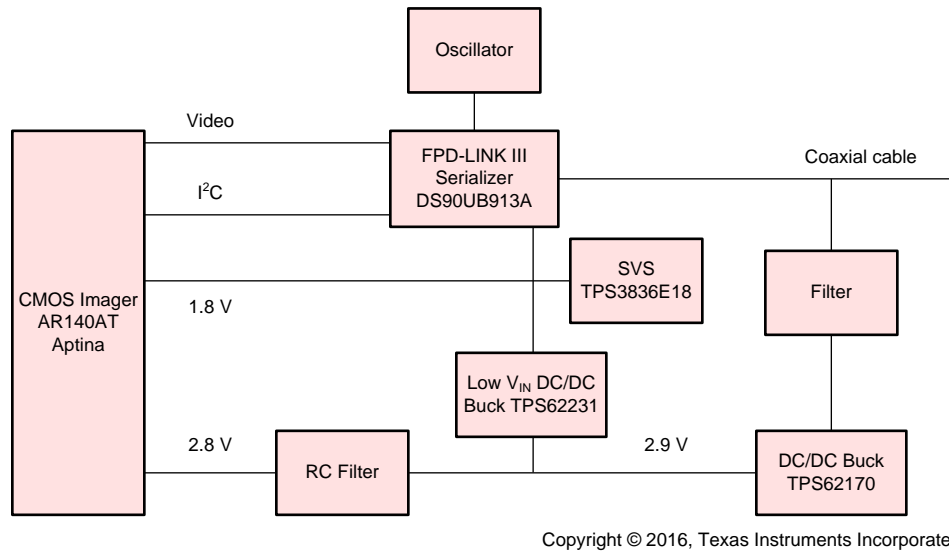

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Figure 1. Camera Block Diagram

A combined signal containing the DC power, the FPD-Link front and back channels enters the board through the FAKRA coax connector. The filter shown in Figure 2 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductors L4 and L5.
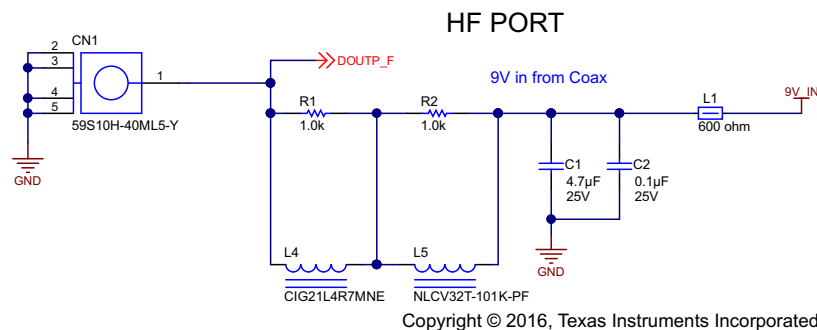

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Figure 2. FPD-Link III Signal Path

The DC portion is connected to the input of the TPS62170 buck converter to output 2.9 V. The other 1.8-V rail required by the serializer and the imager are created by TPS62231 buck converter.

The high frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control back channel will take between the serializer and deserializer.

The output of the CMOS imager is connected through a digital video port (DVP) to the serializer. This 10- or 12-bit video data (with two sync signals) is converted to a single high-speed serial stream that is transmitted over a single LVDS pair to the deserializer located on the other end of the coax cable.

On the same coax cable, there is separate low latency bidirectional control channel that transmits control information from an I²C port. This control channel is independent of video blanking period. It is used by the system microprocessor to configure and control the imager.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax	4	12	17	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V		0.6	1	W
F_{PCLK}	Pixel clock frequency		25		100	MHz

1.3 Highlighted Products

This design uses the following TI products:

- DS90UB913A-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer/deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU)
- TPS62170-Q1: an automotive qualified step-down DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response
- TPS62231-Q1: an automotive qualified fixed-output voltage, 500-mA step-down DC converter. The high switching frequency of up to 3.8 MHz allows for small inductors and a fast transient response
- TPS3836E18-Q1: a supply voltage supervisor that monitors supply voltage and keeps a device from powering on until a certain supply voltage threshold is reached. In this case, the supervisor keeps the PDB pin of the serializer in the low state until the supply reaches 1.71 V.

More information on each device and why they were chosen for this application follow in the next sections.

1.3.1 AR0140AT Imager

Available from the ON semiconductor, this imager is a ¼-inch 1.0 megapixel, a CMOS imager with high dynamic range (HDR). It is suitable for automotive systems and can provide a 10- or 12-bit parallel output. Some additional features of the imager are:

- Supports image sizes: 1280×800 and 720P (16:9) images
- Low power consumption
- Requires two voltage rails (1.8 V and 2.8 V)
- Can be configured using an I²C-compatible two-wire serial interface

1.3.2 DS90UB913A-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The parallel video input of the DS90UB913A-Q1 mates well with the 12-bit parallel video output of the AR0140AT imager. Once combined with the filters for the power over coax (POC), video, I²C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the application report *Cable Requirements for the DS90UB913A & DS90UB914A* (SNLA229).

1.3.3 TPS62170-Q1

To keep the camera small, the power supply must be small. It must also be power efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching power supply is more efficient than a linear regulator, but it can add noise to the system.

Camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This means that the TPS62170-Q1 switching regulator operating at 2.25 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

1.3.4 TPS62231-Q1

This device is simpler to design with since it is a fixed-voltage step down converter. The TPS6223x series features a switching frequency of up to 3.8 MHz, which avoids the AM radio band.

One additional feature of the TPS62231-Q1 not available on the TPS62170-Q1 is a MODE pin. By pulling this pin up, PWM mode can be forced across the full load range. However, with the typical load current of this system, the PWM mode option would provide any benefits.

1.3.5 TPS3836E18-Q1

The PDB pin of the serializer allows the device to be held in a power-down mode until the voltages in the rest of the system have stabilized. It is important that the ID(X) and MODE pins, supply rails, and oscillator of the serializer are stable when the device comes out of the reset.

The supply voltage supervisor manages a safe power-on of the serializer by monitoring the 1.8-V supply voltage rail. This device holds the PDB pin of the serializer in the low state, preventing the serializer from turning on, until the 1.8-V supply voltage rail reaches a threshold voltage, about 1.71 V in this case. Once this threshold voltage is reached, there is a hard 2-ms delay until the supervisor releases the serializer from reset.

2   System Design and Component Selection

This section discusses the considerations behind the design of each subsection of the system.

2.1   *PCB and Form Factor*

This design was not intended to fit any particular form-factor. The only goal of the design with regards to the PCB was to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.
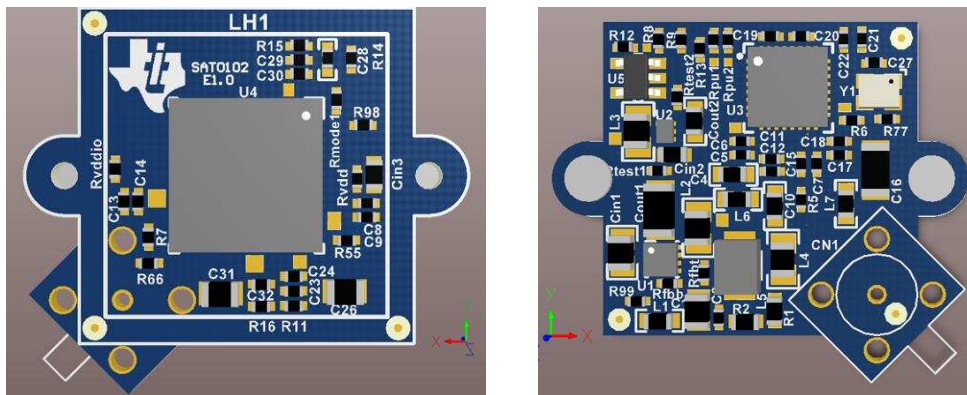

Figure 3. PCB Top and Bottom Views

2.2   *Power Supply Design*

2.2.1   Power Over Coax (POC) Filter

One of the most critical portions of a design which uses Power over Coax is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators, and
2. Protect the FPDLink communication channels from noise coupled backwards from the rest of the system

The DS90UB913/914 SerDes devices used in this system communicate over two carrier frequencies, 700 MHz at full speed ("forward channel") and a lower frequency between 1.75 and 3.25 MHz ("back channel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC. Luckily, by filtering the back channel frequency, this design also filters the frequencies from the switching power supplies on the board.

An ideal series 100-µH inductor could work as a low pass filter, with impedance >1 kΩ at frequencies starting at 1 MHz. However, due to parasitic capacitances, a real 100-µH inductor would cease to have high impedance around 70 MHz. To cover the higher frequency band, the design needs another series inductor. A 4.7-µH inductor ensures a high impedance up to frequencies well above the 700-MHz forward channel. See the application report *Sending Power Over Coax in DS90UB913A Designs* for more details (SNLA224).
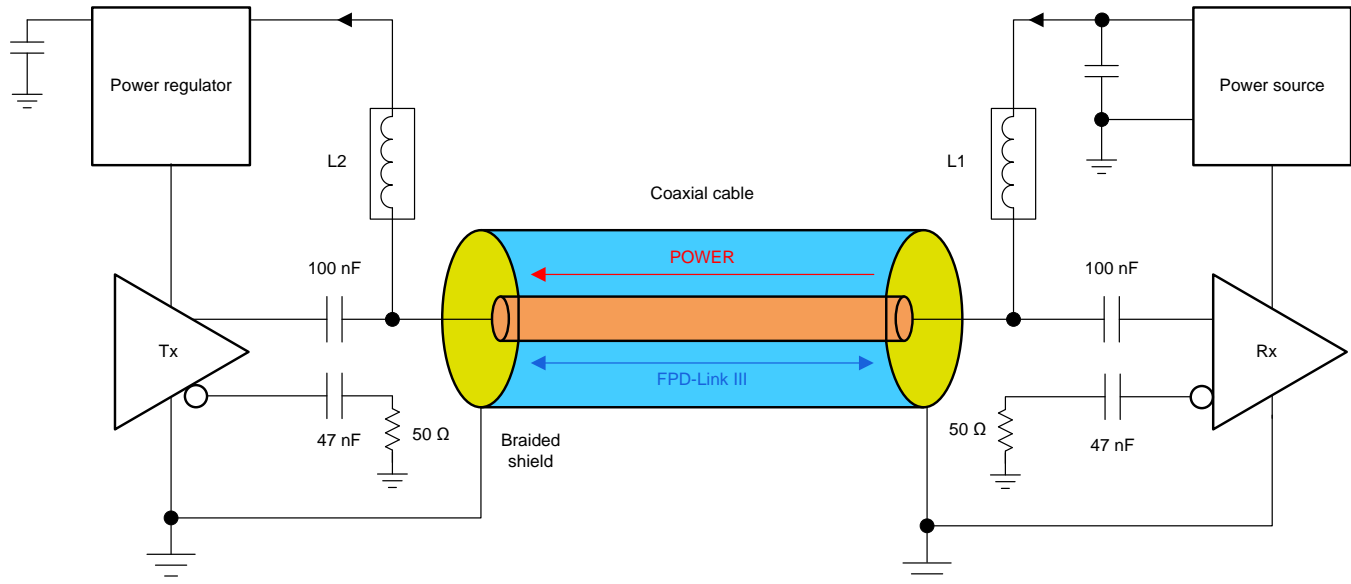
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Figure 4. Power Over Coax

This design needs to minimize the physical size of the inductors used, which is determined by the saturation current of the inductor. As discussed in Table 3 in Section 2.2.2, ideally the design would only be drawing 67.33 mA of current at 9 V to power the system.

However, consider a few non-idealities. First, the efficiency of our power supply is designed to be 77%, not 100%. Second, any voltage droop (due to various causes) from the supply causes the system to draw more current. Due to this, a conservative approach is to add saturation current headroom above what is needed (37% headroom used in this design). The ferrite bead is added for filtering out coupled electro-magnetic interference (EMI) in the coax cable. The capacitors are simply bulk capacitance to reduce current ripple to the input of the power supplies. Of course, these components affect the frequency response of the filter as well.

Table 2. Frequency Response of Filter

TOPOLOGY	–3-dB POINT (Hz)
As designed	9.28k
No ferrite bead	9.47k
Inductors only	160k

2.2.2   Power Supply Considerations

Because this design is targeted at automotive applications, there are few considerations that constrict design choices. In addition, there are few systems-level specifications that shaped the overall design:

- The total solution size needs to be minimized to meet our size requirement, which is less than 20 mm × 20mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate external circuitry.
- To avoid interference with the AM radio band, all switching frequencies need to be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this TI Designs looks at higher frequency switchers.
- All devices need to be AEC Q100 (-Q1) rated.
- Efficiency is important insofar as to keep the total power budget below 1 W to balance efficiency with size and cost, but also to keep this as a good number to stay below. Though the system will be quite low power anyway, it is also an extremely small board in a hot environment.

Before choosing parts, know the input voltage range, rails needed, and current required by each rail. In this case, the input voltage is a pre-regulated 9-V supply coming in over coax. The range is discussed later, but this is the nominal value. This system has only two main ICs, which will consume the majority of the power. The requirements for each supply on these devices are shown in Table 3:

Table 3. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (TYP) (A)	CURRENT (MAX) (A)	POWER (TYP) (W)	POWER (MAX) (W)
DS90UB913A-Q1					
VDDT	1.8	0.0610	0.080	0.1098	0.1440
VDDIO	1.8	0.0015	0.003	0.0027	0.0054
AR0140T					
VDD	1.8	0.1200	0.140	0.2160	0.2520
VDDIO	1.8	0.0180	0.025	0.0324	0.0450
VAA	2.8	0.0350	0.045	0.0980	0.1260
VAA_PIX	2.8	0.0030	0.004	0.0084	0.0112
VDD_PLL	2.8	0.0060	0.008	0.0168	0.0224
Rail total					
1.8-V rail	1.8	0.2005	0.248	0.3609	0.4464
2.8-V rail	2.8	0.0440	0.057	0.1232	0.1596
Overall total	4.6	0.2445	0.305	0.4841	0.6060

Summing these values, the 1.8-V rail requires ~248 mA and the 2.8-V requires 57 mA. If choosing to cascade these power supplies, then the 2.8-V regulator will actually need to source the current for the 1.8-V rail as well. This neglects the consumption of passive components, oscillator, IC quiescent currents, and so on, but this is a good ballpark number.

Since the input and output voltages, output current requirements, and total wattage consumption are known, calculate what the input currents will look like with Equation 1:

$$P_{OUT} = P_{IN} = I_{IN} \times V_{IN} \rightarrow 606 \text{ mW} = I_{IN} \times 9 \text{ V} \rightarrow I_{IN} = 67.33 \text{ mA (max)} \tag{1}$$

These numbers gives a good starting point for selecting the parts and topology for the regulators as well as inductor selections later on. However, this does not take into account the efficiencies of the power supplies.

As previously mentioned, the parts in the power supply need to be Q100 rated, switch outside the AM band, and satisfy the voltage and current requirements as listed. Because the input voltage is a regulated voltage that will always be greater than any of the power rail needs, only choose from step-down converters and LDOs.

The key feature of the system is the small size, so integration of external circuitry is a high priority. Integrating FETs, compensation networks, and sometimes feedback, can significantly reduce total solution size. Many of our buck regulators integrate everything but the input/output caps and the inductor into very small packages. High integration also loses a lot of efficiency across different operating points. However, This TI Design sacrifices some efficiency for size and simplicity reasons.

Ultimately, two device families are good candidates, the TPS621x0 (TPS62170 for the 2.9-V rail), TPS621x1 (possibly the TPS62171 as an option for the 1.8-V rail), and TPS6223x (TPS62231 is the fixed 1.8-V option).

Because there are only two rails, the TIDA-00262 could have either a parallel topology (both rails being fed by the input voltage) or a cascaded topology (one rail is fed by the input voltage, and then feeds the second rail). This design guide presents a few sample options, including buck regulator only (which is what the final design uses), buck+LDO, and LDO-only solutions.

Clearly the largest trade-off with using LDOs is that the efficiency drops significantly, raising the total power draw to over 1 W. This TI Design is a lower-power design; however, in some situations a designer may sacrifice the efficiency to avoid the inherent noise and EMI issues associated with switching power supplies. Another decision to make is parallel versus cascaded topologies. In this case, the parallel topology is actually the most efficient. However, it presents a few problems, especially in the case of the TPS62170+TPS62171 parallel combination. The first issue is that the TPS62170 would be running in discontinuous mode, which could potentially introduce noise into the system that is different from the typical switching frequency. The second issue is that the design now has two different regulators introducing noise backwards to the input. Because they have similar switching frequencies, this could cause low-frequency beat frequencies that are very difficult to filter out. This TI Design sacrifices efficiency to avoid these possible issues. Ultimately, the design uses the TPS62170 and TPS62231 cascaded topology. It is significantly more efficient than designs using LDOs, though not the most efficient design available. It is, however, lower cost than the more efficient options. Functionally, the cascaded topology means that the output current is sufficient such that neither device will operate in discontinuous mode, allowing better predictions and control of the switching noise produced by the devices, and operate with better efficiency.
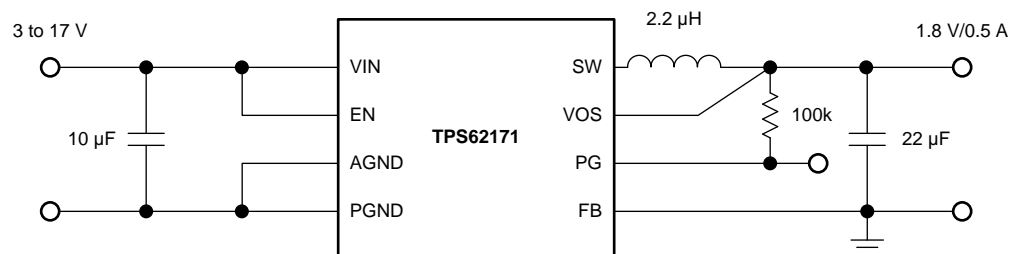
Figure 5. Typical Application Circuit

A lot of the component selection and design theory can be found in the Application Information section of the device's datasheet.

2.2.2.1 *Choosing the Output Inductor*

As mentioned in Section 2.2.2, the switching frequency of the converter must remain above 2 MHz. This means that the converter must always operate in continuous mode. Since input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using Equation 2:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2 \times V_{IN} \times I_{OUT} \times f} = \frac{3.3\,V\left(14\,V - 3.3\,V\right)}{2 \times 14\,V \times 0.12\,A \times 2.1\,MHz} = 5\,\mu H$$

(2)

Since 5 µH is between standard inductor values, the next higher value of 6.8 µH is chosen.

2.2.2.2 *Choosing the Output Capacitor*

Because the device is internally compensated, it is only stable for certain component values in the LC output filter. The application note on optimizing the output filter (SLVA463) has the chart of stable values shown in Table 4. 6.8 µH falls between 4.7 and 10 µH. This means that the user can use a 22-µF output capacitor and remain in the stable region of effective corner frequencies.

Table 4. Stability versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	EFFECTIVE CORNER FREQUENCIES (kHz)								
0.47 µH	151.4	103.8	70.0	47.9	32.8	23.2	16.4	11.6	8.2
1.00 µH	103.8	71.2	48.0	32.8	22.5	15.9	11.3	8.0	5.6
2.2 µH	70.0	48.0	32.4	22.1	15.2	10.7	7.6	5.4	3.8
3.3 µH	57.2	39.2	26.4	18.1	12.4	8.8	6.2	4.4	3.1
4.7 µH	47.9	32.8	22.1	15.1	10.4	7.3	5.2	3.7	2.6
10.0 µH	32.8	22.5	15.2	10.4	7.1	5.0	3.6	2.5	1.8

	Recommended for TPS6213x/4x/5x/6x/7x
	Recommended for TPS6213x/4x/5x only
	Stable without Cff (within recommended LC corner frequency range)
	Stable without Cff (outside recommended LC corner frequency range)
	Unstable

With our inductance value chosen, the design now needs an inductor with a proper saturation current. This is going to be the combination of the steady state supply current as well as the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current (from the datasheet) using Equation 3:

$$\Delta I_L = V_{OUT} \times \left(\frac{\left(1 - \dfrac{V_{OUT}}{V_{IN}} \right)}{L \times f_{SW}} \right)$$

(3)

Here are the parameters for our design using the TPS62170:

- V_{OUT} = 3.3 V
- V_{IN} = 14 V
- L = 6.8 µH
- f_{SW} = 2.25 MHz

which yields an inductor current of ΔI_L = 165 mA. The maximum current draw of the system through this regulator is 268 mA. Finally, Equation 4 gives us our minimum saturation:

$$L_{SAT} \geq \left(I_{MAX} + \frac{I_{RIPPLE}}{2} \right) \times 1.2 = \left(268\ mA + \frac{165\ mA}{2} \right) \times 1.2 = 420\ mA$$

(4)

The TIDA-00262 uses a Coilcraft XPL2010-682MLB, which has a saturation current of 450 mA with only a 10% drop in inductance. This part comes in a very small 1.9-mm square package.

The output voltage is determined by the resistor divider to the feedback pin. The following is the calculation for the output voltage, which is aimed for 3.3 V out, but wanted to work with readily available resistor values:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \rightarrow V_{OUT} = \left(\frac{R1}{R2} + 1 \right) \times V_{REF} = \left(\frac{316 k\Omega}{100 k\Omega} + 1 \right) \times 0.8\ V = 3.328\ V$$

(5)

This gives a close enough output voltage to the desired 3.3 V. For improved accuracy, all FB resistor dividers must use components with 1% or better tolerance.

2.2.3 TPS62231-Q1

This device is a bit easier than the TPS62170 because it is a simpler, fixed voltage device. However, the considerations are quite similar. Following the same procedure as the TPS62170, select the output LC filter for this supply. This converter is stable with a 1- or 2.2-µH inductor and a 4.7-µF capacitor. The larger inductance was chosen in this case in part to reduce ripple current (important for keeping the regulator in continuous mode), but also to use the same inductor for both regulators, reducing the unique BOM count. The previous equations can be used to find a minimum LSAT of 360 mA, which the inductor covers easily.

The only additional feature of this device not present on the TPS62170 is the mode select pin. Pulling this pin up forces PWM mode. With a typical load current, the PFM/PWM mode option would not provide additional efficiency benefits.

3 Getting Started Hardware

The TIDA-00262 needs only one connection to a system with a compatible deserializer. Simply connect the FAKRA connector on the coax cable between the serializer and deserializer.
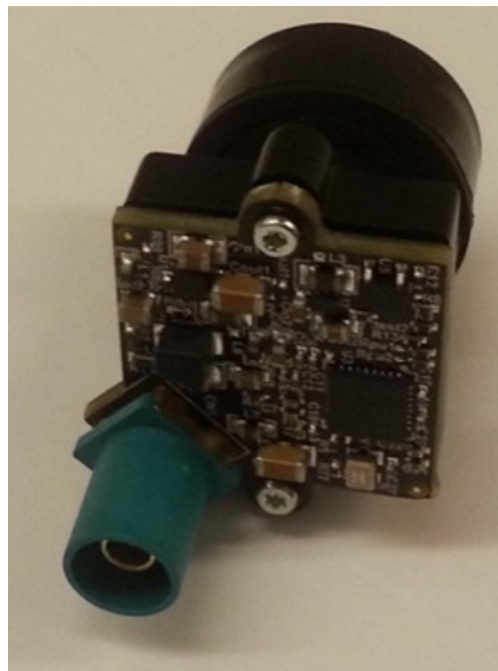
Figure 6. Getting Started With Board

4 Testing and Results

4.1 Test Setup

For the following tests, the camera was connected to a multiple camera surround view system.
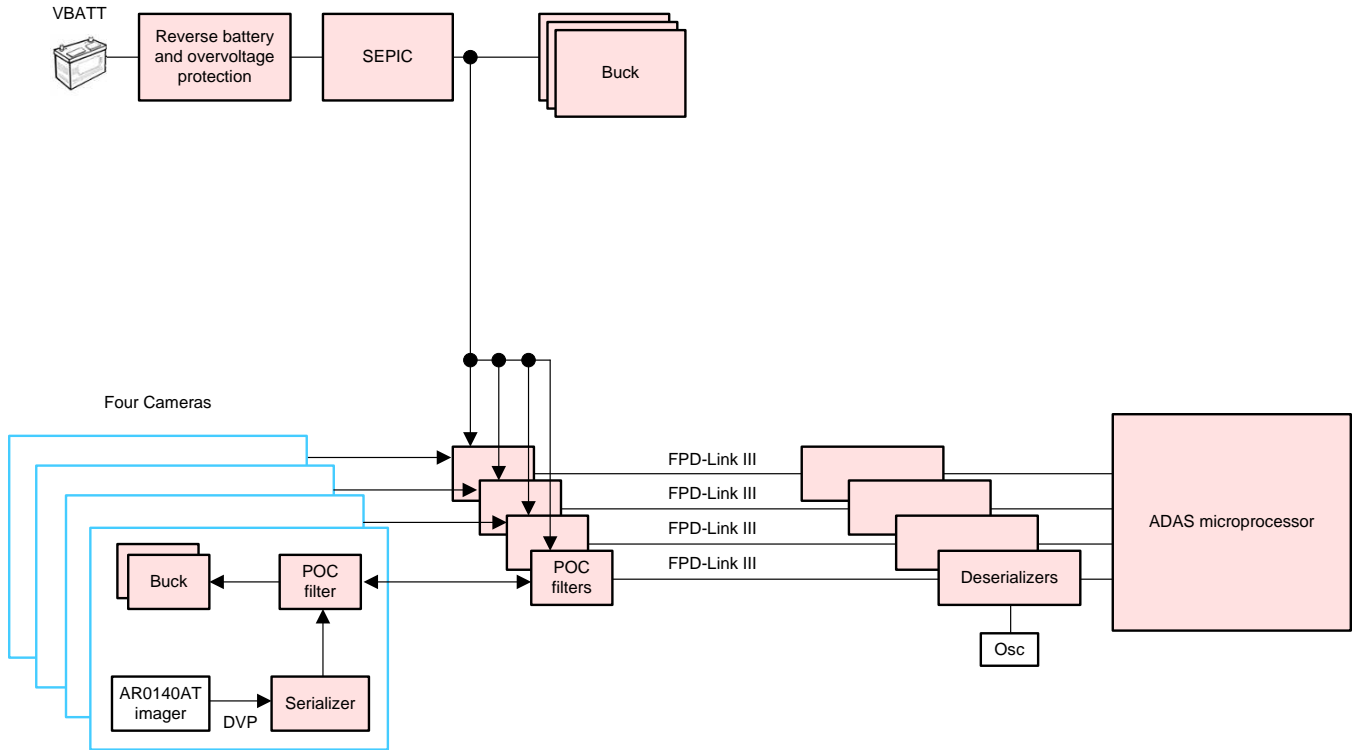
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Figure 7. Simplified Surround View Block Diagram

4.1.1 Setup for Verifying Power Supply Startup—1.8-V Rail and PDB
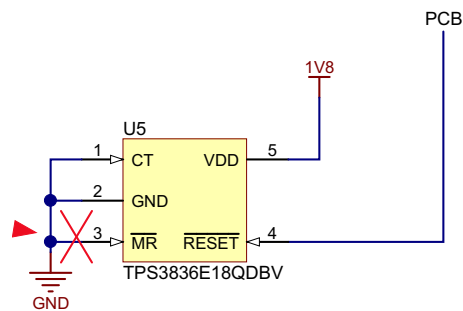
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Figure 8. Setup for Measuring All Power Rails

4.1.2   Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two busses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Make connections to both the clock and data lines of each bus.
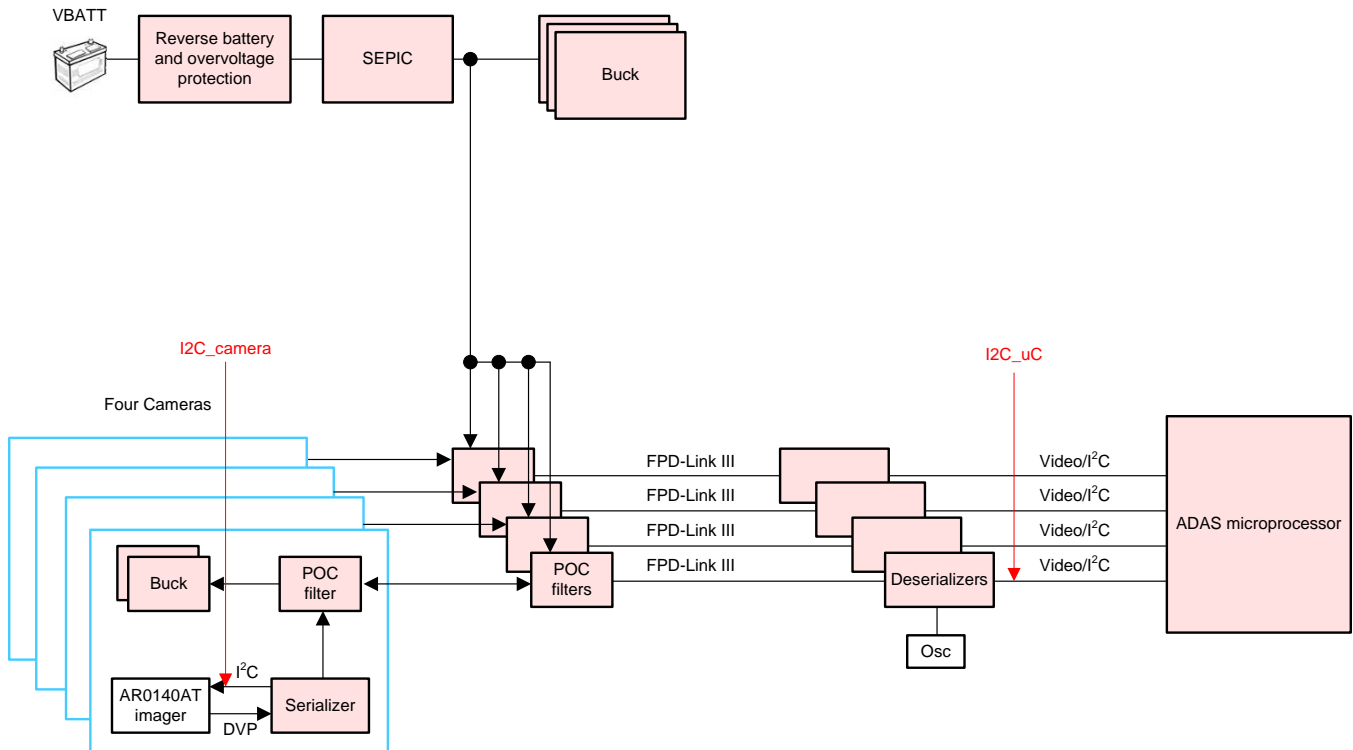
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Figure 9. Setup for Monitoring I²C Transactions

4.2   Test Data

The following sections show the test data from verifying the functionality of the camera design.

4.2.1   Power Supply Startup—1.8-V Rail and PDB

The only startup requirement is that the PDB pin of serializer remain low until the supply rails of the system stabilize at their final voltages. The power supply startup is shown in Figure 10.
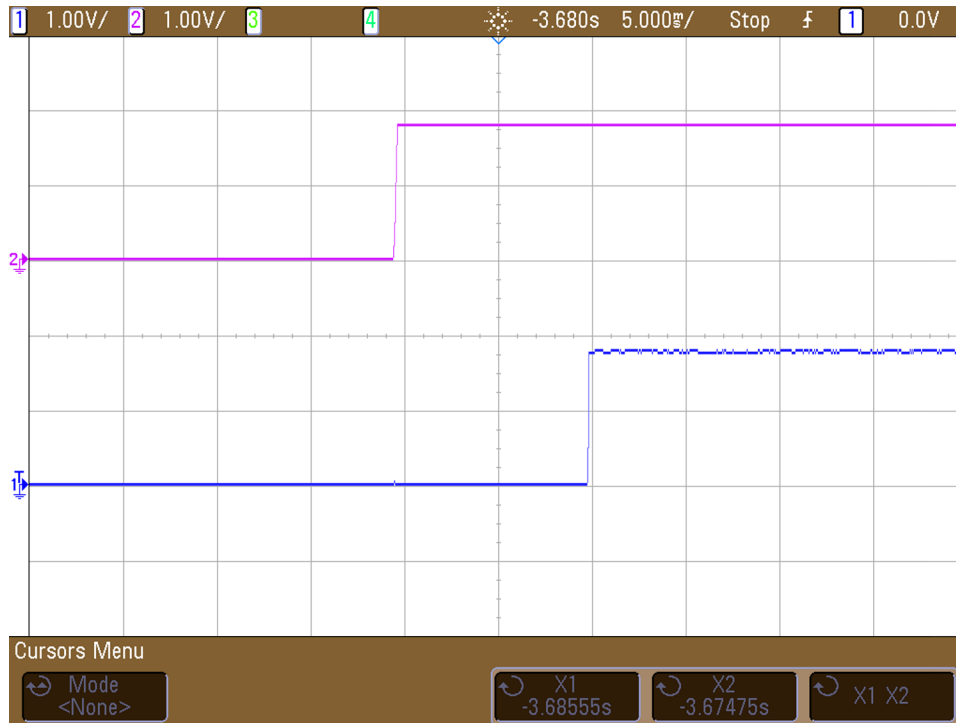
Figure 10. Serializer Power-Up Sequence

NOTE: Channel 1 (yellow) PDB; Channel 2 (green) VDDIO (1.8 V)

Figure 10 shows that PDB comes up roughly 10 ms after the 1.8-V rail has stabilized. This 10-ms delay is due to having the CT pin of the TPS3836E1 connected to ground.

4.2.2   I²C Communications

With the supplies up and running, now check the FPD-Link connection, the I²C aliasing, and the state of the AR0140AT imager in one step. Figure 11 shows a reset of logic. This occurs after the microprocessor configures the deserializer on the other end of the link. Because this communication starts on the ECU board and is acknowledged by the camera, this shows that the communication through the FPD-Link III is functioning properly.
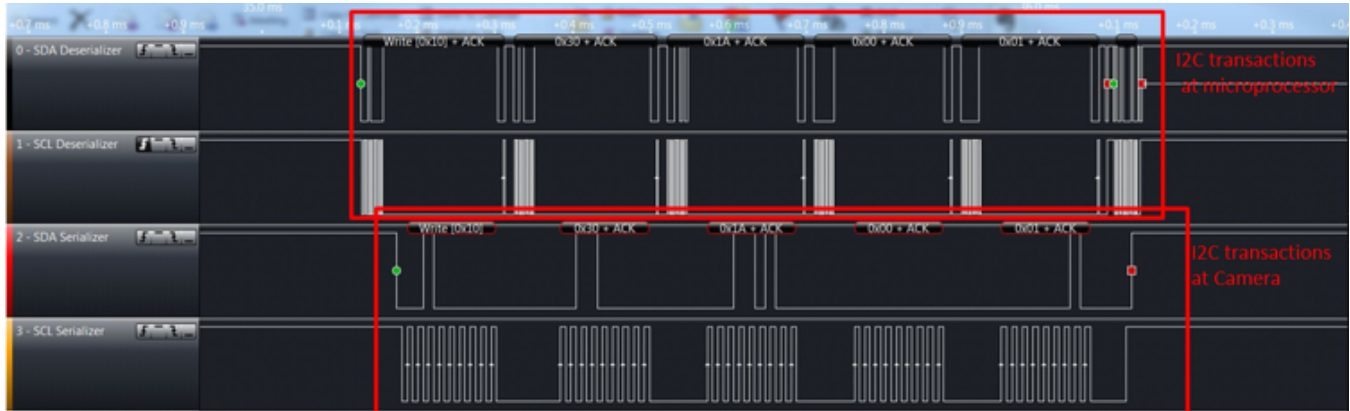
Figure 11. I²C Transactions

The top box contains the write from the microprocessor. It is addressed to slave alias address 0x10, the actual register address is 0x301A, and the data to be written is 0x0001. Since the address is 0x30, the logic on the deserializer passes this transaction to the camera. It is routed to the imager, and the address is aliased to 0x10.

The bottom box shows the same communication, slightly delayed. This is the communication present on the camera's I²C bus, measured at the imager.

By acknowledging the I²C write, the imager has confirmed that it is present and alive. Reading the status registers can confirm the status of the imager as well as verify that the correct imager was installed during assembly.

5   Design Files

5.1   Schematics

To download the schematics, see the design files at TIDA-00262.

5.2   Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00262.

5.3   PCB Layout Recommendations

5.3.1   Switching DC-DC Converters

During part placement and routing, it is helpful to always consider the path current will be taking through the circuit. The green line in Figure 12 shows the current path from the coax in through the power over coax filter, inductors L4 and L5 and capacitors C1 and C2, and then out to the ferrite bead, L1, input capacitor, Cin1, to U1, or the TPS62170-Q1. The yellow line follows the 2.9-V output of the switcher to the output inductor L2 and output capacitor Cout1. Any return currents from the input capacitor Cin1 or the output capacitor Cout1 are joined together at the top left of U1 before they are connected to the ground plane. This is shown inside the blue lines. This will reduce the amount of return currents, and thereby, voltage gradients in the ground plane. This may not be noticeable in the performance of the converter, but it will reduce its coupled noise into other devices.

Figure 12. Routing FB Traces Around SW Nodes

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5.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stack up recommendations. Since automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high speed signals and small PCBs.

- Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a 4-layer board, layer 2 must be a ground plane. Since most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers were used in this board to simplify BGA fan out and routing. Figure 13 shows the stackup used in this board:

Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - Signal	Signal	Copper	1.417		
Dielectric 3	Dielectric	Prepreg	16.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.417		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

Figure 13. Layer Stackup

5.3.3 Serializer Layout Recommendations

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

Figure 14 shows the supply current from C18 in yellow. The green line is the return path. The cross sectional area of this loop is very small. A similar sketch for C16 or C17 would show a larger loop.
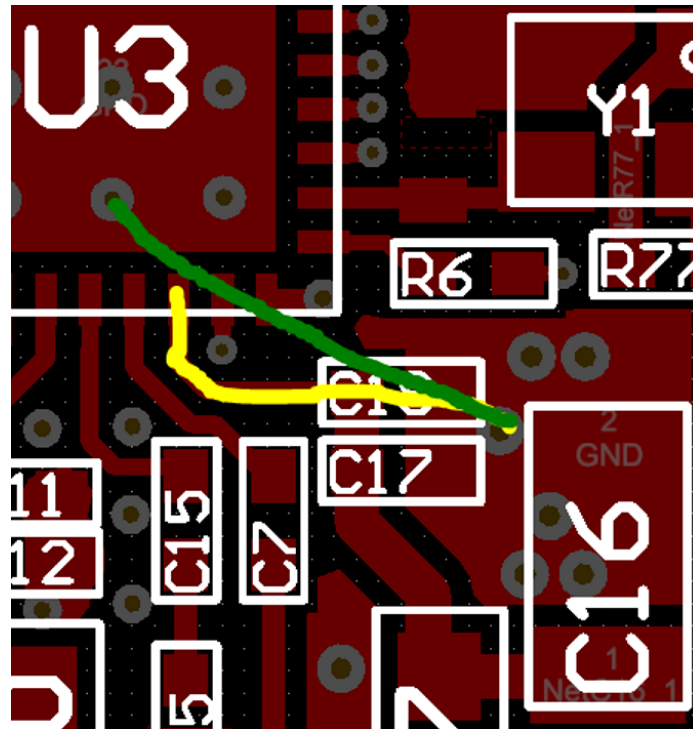
Figure 14. Decoupling Current Loop

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. The routing of the high-speed serial line is shown in Figure 15. It is highlighted by the yellow line. The total length of the yellow line is about ½ inch.
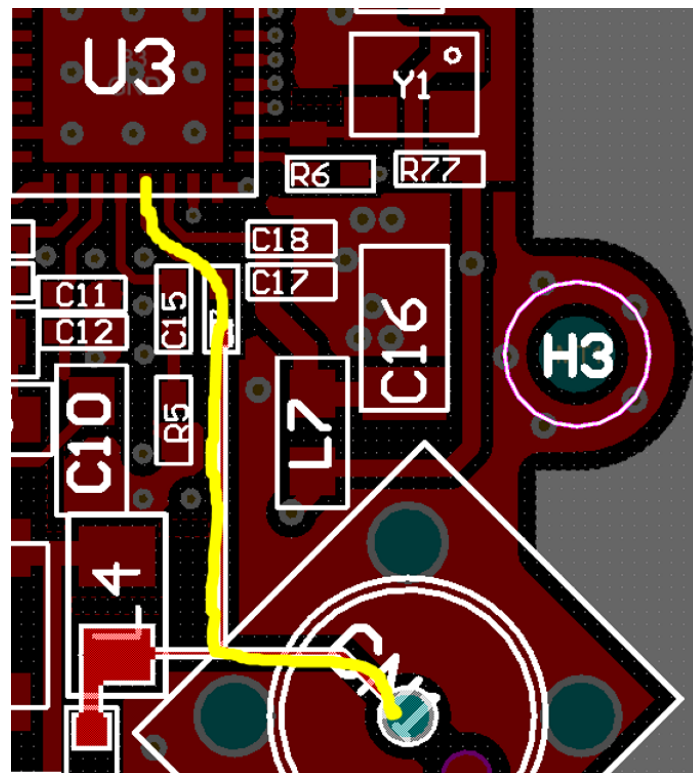
Figure 15. High-Speed Serial Trace

5.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-00262.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00262.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00262.

6 References

1. Texas Instruments, *DS90UB913A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer*, DS90UB913A-Q1 Datasheet (SNLS443)
2. Texas Instruments, *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™*, TPS62170-Q1 Datasheet (SLVSCK7)
3. Texas Instruments, *3-MHz Ultrasmall Stepdown Converter in 1x1.5 SON Package*, TPS62231-Q1 Datasheet (SLVSBV0)
4. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs*, Application Report (SNLA224)
5. Texas Instruments, *Cable Requirements for the DS90UB913A and DS90UB914A*, Application Report (SNLA229)
6. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter*, Application Report (SLVA463)

7 About the Author

BRIAN SHAFFER is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Brian focuses on ADAS (Advanced Driver Assistance Systems) end-equipments, creating reference designs for top automotive OEM and Tier 1 manufacturers. He brings to this role experience in high-reliability infrared cameras, power supplies for portable devices, cameras for automotive platforms, and embedded systems design. Brian earned his bachelor of science in electrical engineering from Kansas State University in Manhattan, KS.