TI Designs
Automatic Direction Control RS-485

Design Overview

This reference design allows for the direction of communication on an RS-485 bus to be set automatically when a node needs to transmit data. The transceiver enables the driver for a configurable length of time when data is sent to a transceiver device from a host microcontroller (MCU) or universal asynchronous-receiver transmitter (UART). This eliminates the need for manual control of the driver enable of the transceiver and the need for the receiver-enable controls, reducing the number of logic pins needed to implement the RS-485 interface.

Design Resources

TIDA-01090	Design Folder
SN65HVD3082E	Product Folder
NA555	Product Folder
RS-485 Design Guide	Application Report

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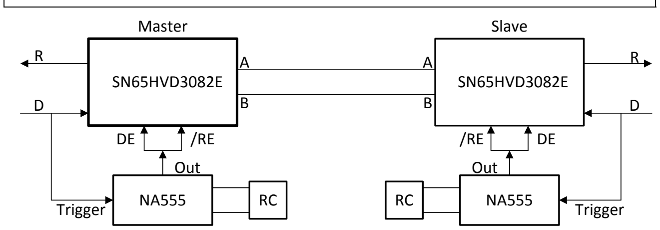
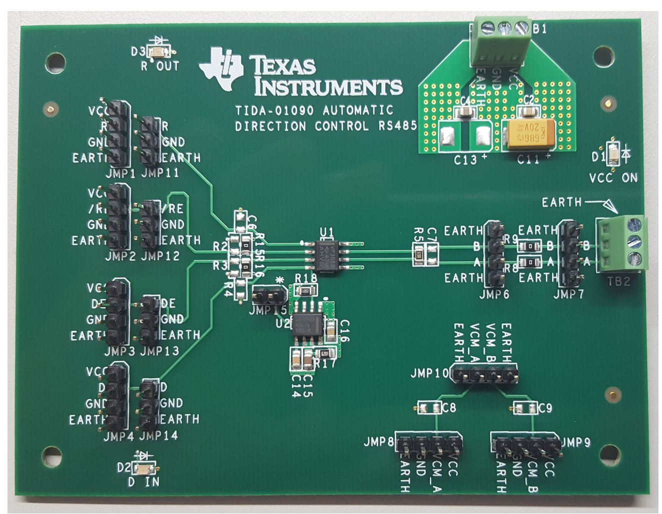


Design Features

- Auto-Direction Control for Half-Duplex RS-485 Master-Slave Communication
- Easy Time Setting When Using RC Networks

Featured Applications

- RS485 Repeaters
- E-Meters
- Industrial Automation
- Security and Surveillance Equipment
- Encoders and Decoders



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1 Key System Specifications

This reference design can be used in applications that require half-duplex RS-485 communication with fixed-packet lengths. The specifications required for the RS-485 bus (for example: data rate, number of nodes supported, communication distance, and transient immunity) vary from application to application and can be addressed through proper transceiver selection. This reference design works with any half-duplex RS-485 transceiver. The length of time that a node must stay enabled when transmitting a packet of data varies from application to application based on the packet length used. The length of time can be adjusted over a wide range through selection of different passive components (resistors and capacitors). This reference design is intended to interface to MCUs using 5-V logic levels, but can be adjusted to support 3.3-V logic levels by using alternate components or by introducing a level-translator stage.

2 System Description

The RS-485 communication protocol defines one of many physical-layer standards for differential signaling in half or full duplex-communication channels. In typical half-duplex communication, the direction of data flow is controlled by DE and $\overline{RE}$-control signals to the transceiver. Usually, these control signals are provided by a MCU and require a GPIO pin and software-implementation efforts to manage the direction of data flow. This design details the concept of automatic-direction control using TI's NA555 timer in mono-stable multivibrator mode to generate DE and $\overline{RE}$-control signals. The system uses the start bit of the data frame as the trigger and enables the driver of the SN65HVD3082 for the frame duration that is set by an RC circuit. The NA555 timer automatically disables the driver and enables the receiver as the set time elapses.

2.1 2.1 SN65HVD3082E

The SN65HVD3082E is a half-duplex RS-485 transceiver commonly used for asynchronous-data transmission (see Figure 1). The driver and receiver enable pins allow for the configuration of different operating modes.

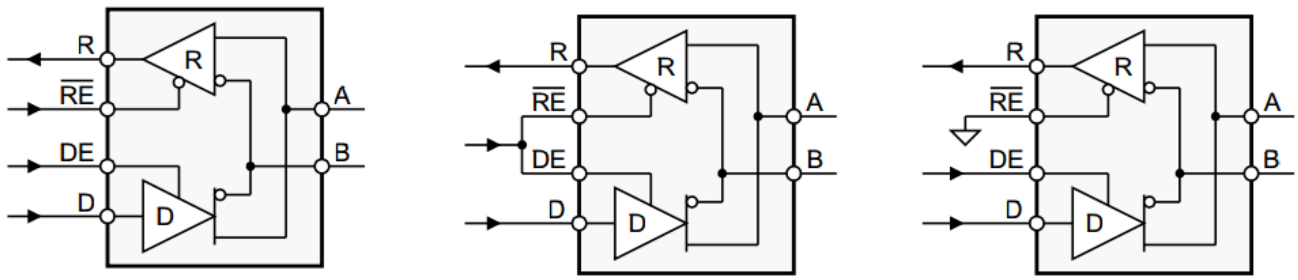

Figure 1. Half-Duplex Transceiver Configuration

Using independent-enable lines provides flexible control because it allows the driver and the receiver to be turned on and off individually. This configuration requires two control lines but still allows for selective listening into the bus traffic, whether the driver is transmitting data or not. Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. The transceiver operates as a driver when the direction-control line is high, and it operates as a receiver when the direction-control line is low. Only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this design, a node can send and receive data and verify that the correct data has been transmitted.

Although the second and third applications are able to reduce the number of control lines used, some manual control of the enable signals is still required. This reference design helps reduce the number of control-line connections needed to a MCU by making direction control automatic.

2.2 NA555

The NA555 device is a precision-timing circuit that can produce accurate time pulses. The time pulse is controlled by a single external resistor and capacitor network. An NA555 timer is used to detect the data being transmitted from a MCU and to produce the driver-enable signal to the RS485 transceiver for the predefined duration of the packet. The enable-signal duration is set by a resistor and capacitor network.

3 Block Diagram

Figure 2 shows the automatic-direction control RS485-block diagram.

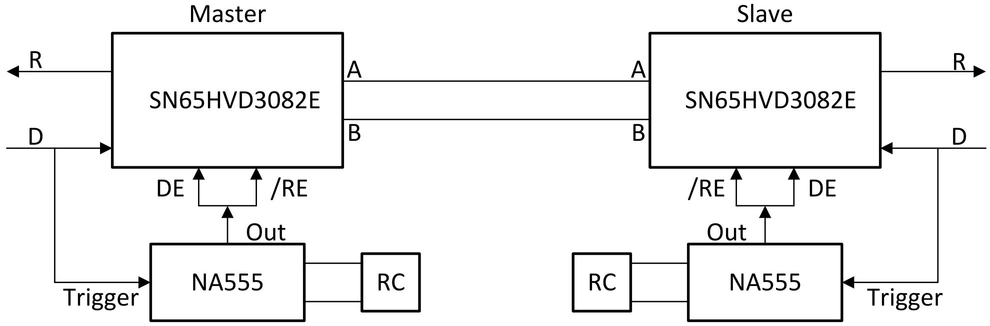

Figure 2. Automatic-Direction Control RS485-Block Diagram

3.1 *Highlighted Products*

3.1.1 SN65HVD3082E

The SNx5HVD308xE devices are half-duplex transceivers designed for RS-485 data-bus networks. Powered by a 5-V supply, the devices are fully compliant with the TIA/EIA-485A standard. These devices can transmit data through long twisted-pair cables with controlled-transition lines. The SN65HVD3082E and SN75HVD3082E devices are optimized for signaling rates of up to 200 kbps. The SN65HVD3085E device is suitable for data transmission of up to 1 Mbps, and the SN65HVD3088E device is suitable for applications that require signaling rates of up to 20 Mbps.

These devices are designed to operate with a low-supply current (0.3 mA) exclusive of the load. These devices are ideal for power-sensitive applications with nanoamps of current consumption during inactive-shutdown mode.

The wide common-mode range and high ESD-protection levels of the SNx5HVD308xE devices makes them suitable for demanding applications such as energy-meter networks, electrical inverters, status and command signals across telecom racks, cabled-chassis interconnects, and industrial-automation networks where noise tolerance is essential. These devices match the industry-standard footprint of the SN75176 device. Power-on-reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal-shutdown function protects the device from damage due to system-fault conditions. The SN75HVD3082E operates between 0°C and 70°C, and SN65HVD308xE devices operate from –40°C to 85°C air temperature.

3.1.2 NA555

The NA555 is a precision-timing circuit that can produce accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third of V_{CC}. These levels can be altered by using the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit can sink or source current of up to 200 mA. Operation is specified for supplies of 5 V to 15 V. Output levels are compatible with TTL inputs when using a 5-V power supply.

4 System Design Theory

The primary goal of the design is to detect the data transmission from a MCU and to generate accurate direction control to the transceiver. The design uses the falling edge of a start bit of a UART to implement auto-direction control. The falling edge triggers the timer of the NA555 that generates a driver-enable signal for the packet length that is predefined in the protocol. This duration is set by a single resistor and capacitor network.

4.1 Monostable Multivibrator

When a negative (0 V) pulse of the start bit is applied to the trigger input (pin 2) of the monostable-configured NA555-timer oscillator, the internal comparator detects this input and sets the state of the flip-flop, changing the output from a low state to a high state. This action turns off the discharge transistor connected to pin 7 and removes the short circuit across the external-timing capacitor (C1).

This action allows the timing capacitor to begin charging up through resistor R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of (2 ÷ 3) × V_{CC} that is set up by the internal voltage-divider network. The comparator output will go high and reset the flip-flop back to the original state; this activates the transistor and discharges the capacitor to ground through pin 7. The discharge causes the output to change its state back to the stable low value, awaiting another trigger pulse (start bit of next packet) to start the timing process again (see Figure 3 and Figure 4).

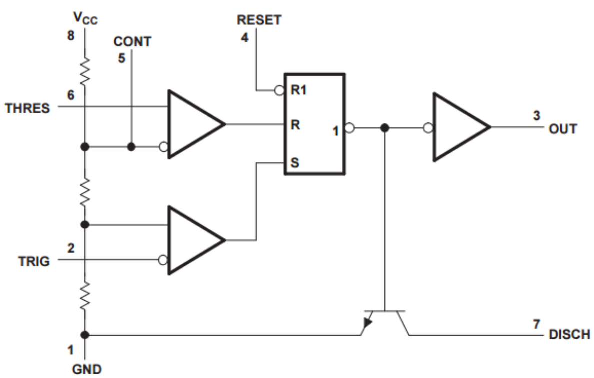

Figure 3. NA555

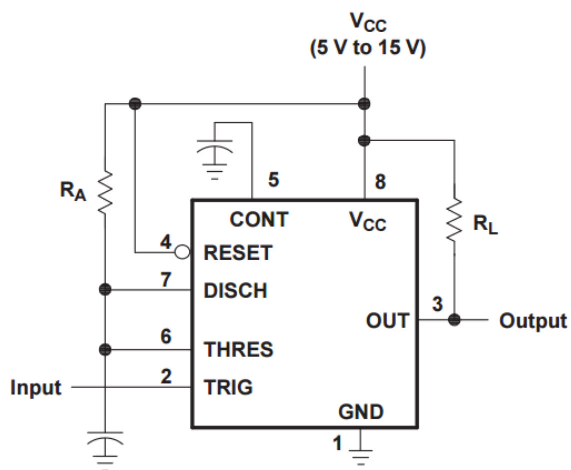

Figure 4. Monostable Multivibrator

4.2 Pulse-Duration Cancellation

The pulse width is predefined according to the packet length of the protocol. The resistor and capacitor value in the monostable-multivibrator configuration are chosen to enable the driver for the entire packet length using Equation 1, where τ is in seconds, R is in Ohms, and C is in Farads.

$$\tau = 1.1 \times R_1 \times C_1 \quad (1)$$

The tolerances of the resistor and the capacitor that is selected effects the enable pulse. Ensure the calculated resistor and capacitor values provide the required enable-pulse duration, even at the boundary value of the tolerance.

The time setting components in the reference schematic and layout files are designated as R17 and C15, respectively. While designing the system, care must be taken to provide at least 10 µs of space between consecutive packets to keep the trigger high long enough to overcome the comparator-storage time.

5 Getting Started Hardware

Users need two boards to evaluate both sides of the RS-485 connection. The design comes prepopulated with two of the TI devices with a resistor of 6.19 kΩ (R17) and a capacitor of 0.47 µF (C15) to produce 32 ms of driver-enable pulse.

The resistor and capacitor values on both boards need to be reworked based on the application. To rework the values on the boards, calculate the time period of the longest packet in the communications protocol using Equation 1 and replace R17 and C15 with the calculated values. Ensure a jumper is placed on JMP15.

V_{CC} and GND are connected at the top-right corner of the boards at terminal TB1. The driver-bus lines must be connected using a twisted-pair cable. The boards include a terminal block with screw heads to allow users to attach bus cables. Connect the master TX and RX on one side and the slave on the other side to evaluate the auto direction-control function.

Users can use the evaluation board as a normal RS-485 EVM (for example: with manual control of the driver- and receiver-enable lines through burg headers). The burg headers must be left open while evaluating the automatic direction-control functionality. If users need to evaluate the system without auto-direction control, remove the resistors on R15 and R16, or remove the jumper on JMP15.

6 Test Setup

The two boards must be properly powered (check the blue-status LED), connected together, and configured with the correct value of timing resistors and capacitors. In this test, the resistor is 6.19 kΩ and the capacitor is 0.47 µF to enable the driver for 32 ms.

The system is tested using two MSP430 MCUs, one is the master and one is the slave. In the test setup, the master sends a predefined packet of 30 bits at 9600 bps (3.12 ms of packet length). The slave compares the received-data packet with the expected-data packet and sends back the acknowledgment to the master. When the master receives the correct acknowledgment from the slave, the master marks the communication as successful by toggling an LED. This communication runs in a loop.

When the master encounters a communication error, it will no longer toggle the LED and switches the LED to the ON state.

To capture the test data, an oscilloscope was connected at the DE and $\overline{RE}$ signals on both the master and slave sides.

7 Test Data

7.1 Data Transmission and Direction Control

Figure 5 shows the plot of data transmission and the direction-control signal for a packet of 30 bits at 9.6 kbps.

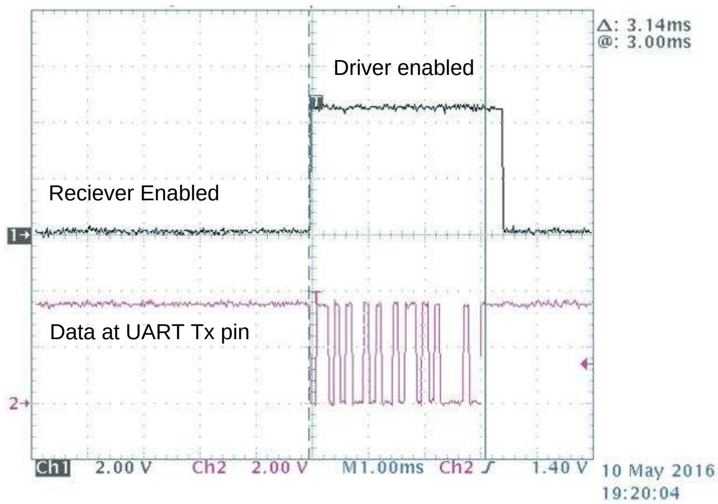

Figure 5. Plot of Data Transmission and Direction Control Signal

7.2 Delay Between UART-Start Bit and Driver-Enable Signal

Figure 6 shows the delay between the UART-start bit and the driver-enable signal.

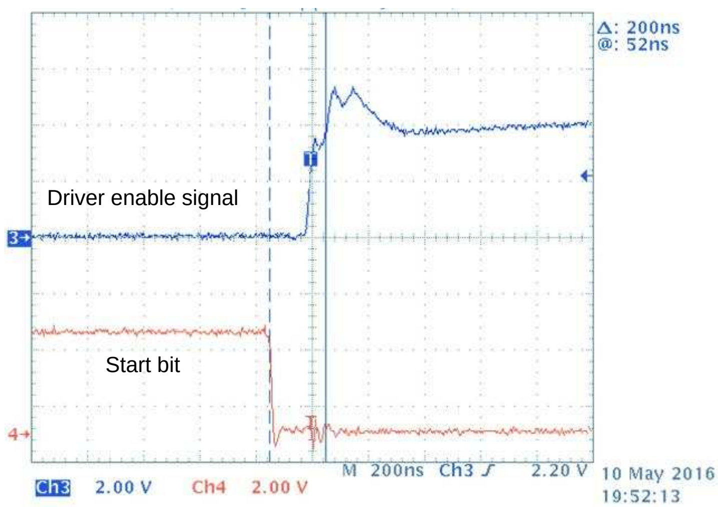

Figure 6. Delays

7.3 Master-Slave Communication

Figure 7 shows the master-slave communication and enable signals.

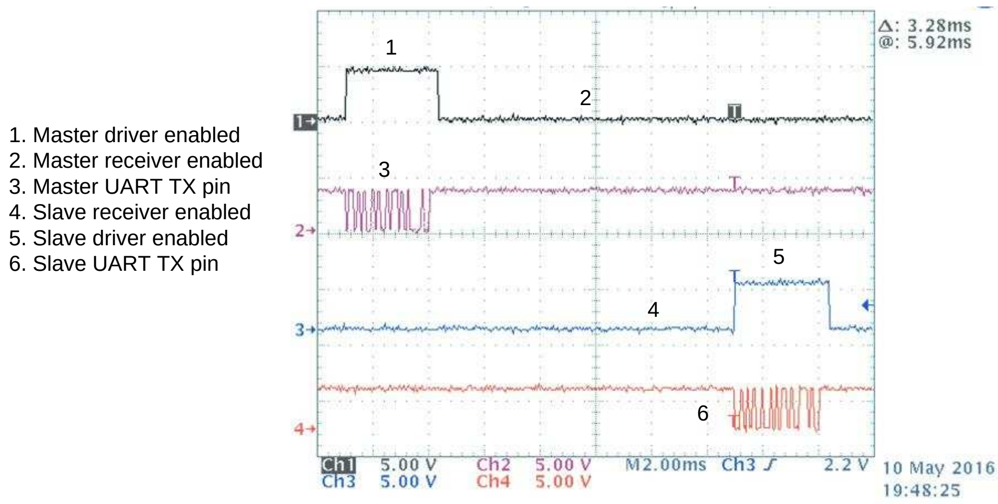

Figure 7. Master-Slave Communication

7.4 Data Rate

Figure 8 shows the receiver enabled, driver enabled, and data at UART TX pin for 200 kbps.

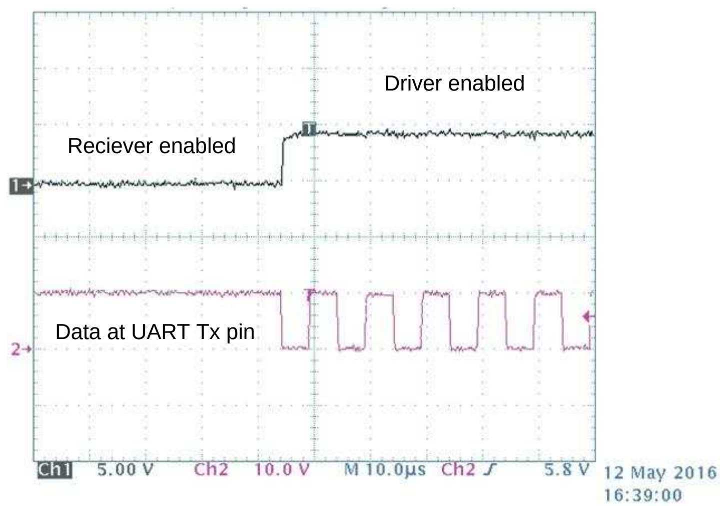

Figure 8. Enable Signal for 200 kbps

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-01090.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01090.

8.3 PCB Layout Recommendations

Place any protection circuitry close to the bus connector to prevent noise transients from entering the board. Use V_{CC} and ground planes to provide low-inductance and low-resistance power conditions. Apply 100- to 220-nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, and the control devices on the board. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective-via inductance.

8.4 Layout Prints

To download the layer plots, see the design files at TIDA-01090.

8.5 Allegro Project

To download the Allegro project files, see the design files at TIDA-01090.

8.6 Layout Guidelines

Provide bulk decoupling for C13, use local decoupling at each IC (C3 and C16), and match the bus-line length (see Figure 9).

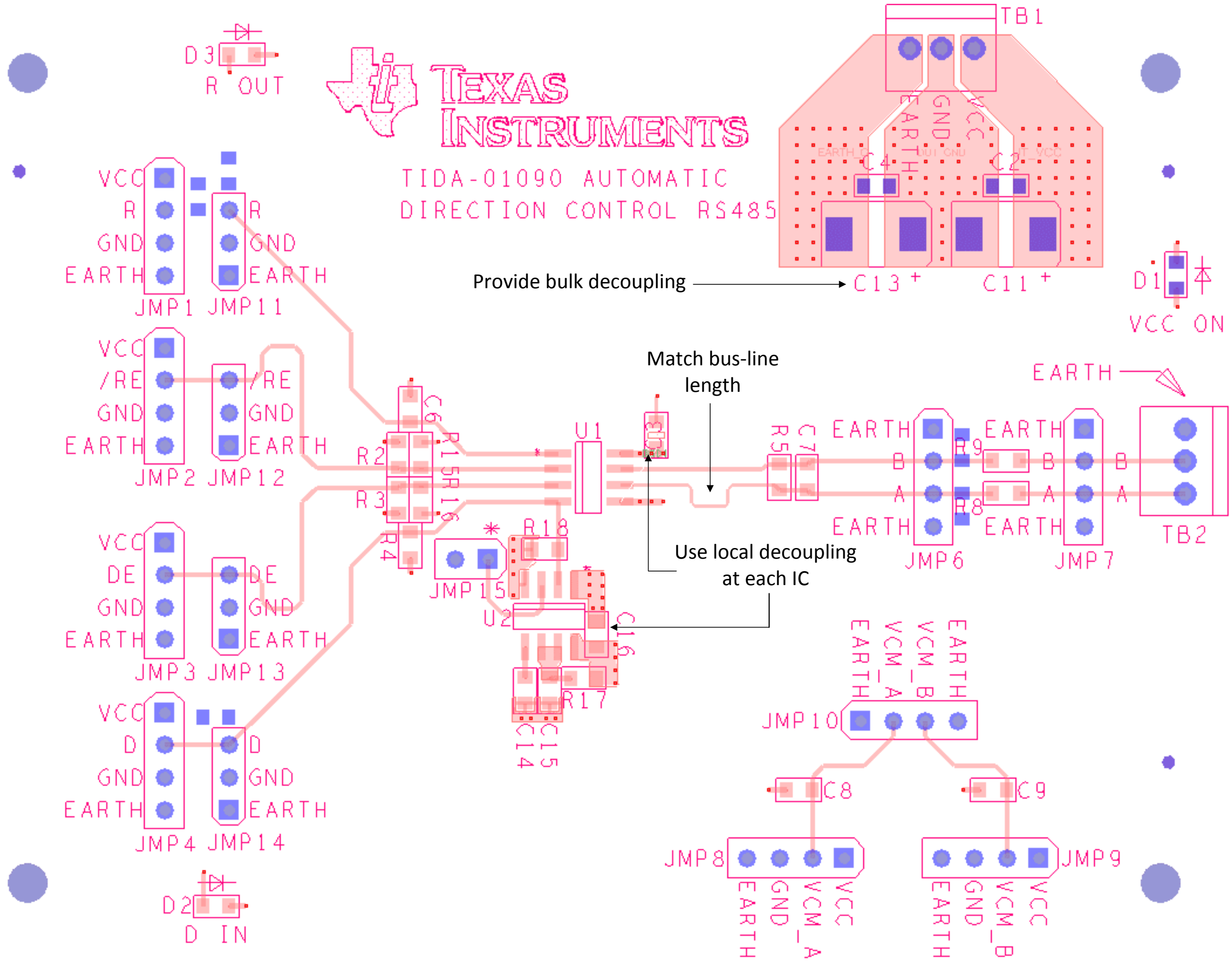

Figure 9. Layout Guidelines

8.7 Gerber Files

To download the Gerber files, see the design files at TIDA-01090.

8.8 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01090.

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