

TI Designs

RS-485 Bidirectional Fan-Out Hub With Automatic Direction Control Reference Design



Description

RS-485 is a bus communication scheme that implements point-to-point, multi-drop, and multi-point bus architectures. The TIA/EIA-485-A standard requires that a termination resistor matching the characteristic impedance of the transmission media be placed at the two farthest ends of the bus. This technique works well for linear, daisy-chained bus topologies but can become rather challenging in non-ideal bus topologies like stars, rings, and backbones with stars.

TIDA-01365 documents and tests an RS-485 fan-out hub design where 1:N and N:1 RS-485 signals are aggregated in and out of any bus topology. This TI Design also feature automatic direction control for reduced pin count on microcontrollers and a DC-to-DC converter using the 24-V DC rail typically seen in industrial applications.

Resources

TIDA-01365	Design Folder
SN65HVD3082E	Product Folder
NA555	Product Folder
SN74LV08A	Product Folder

Features

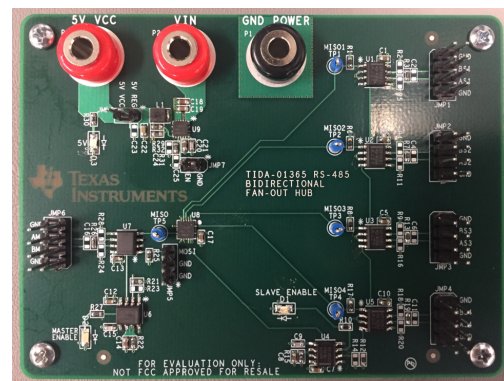
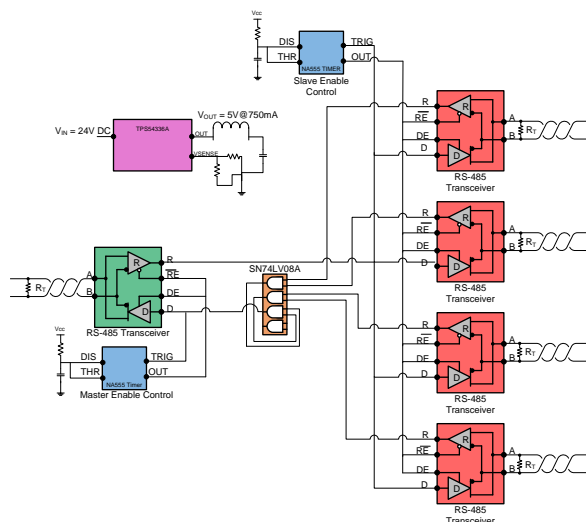
- One Master Node
- Four Slave Nodes
- Bidirectional Communication With Automatic Direction Control
- Configurable Data Rate and Packet Length Through RC Values on NA555 Timer
- Supports Cable Lengths >1000 m
- Supports 24-V Industrial DC Supplies

Applications

- [Building Automation](#)
 - HVAC Video
 - Surveillance
- [Factory Automation and Control](#)
- [Lighting](#)
 - Lighting Control



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1 System Overview

1.1 System Description

RS-485 is a bus communication scheme that implements point-to-point, multi-drop, or multi-point bus architectures. The TIA/EIA-485-A standard requires that a termination resistor matching the characteristic impedance of the transmission media be placed at the two farthest ends of the bus. Without the termination resistors the signal integrity could become compromised as reflections and standing waves begin to dominate the signal on the bus. The termination ensures that signal integrity is not compromised by dampening any reflections and standing waves that reside on the bus. This technique works well for linear, daisy-chained bus topologies but can become rather challenging in non-ideal bus topologies like stars, rings, and backbone with stars buses.

Figure 1 shows a non-inclusive list of the different types of bus topologies that could exist in RS-485 networks.

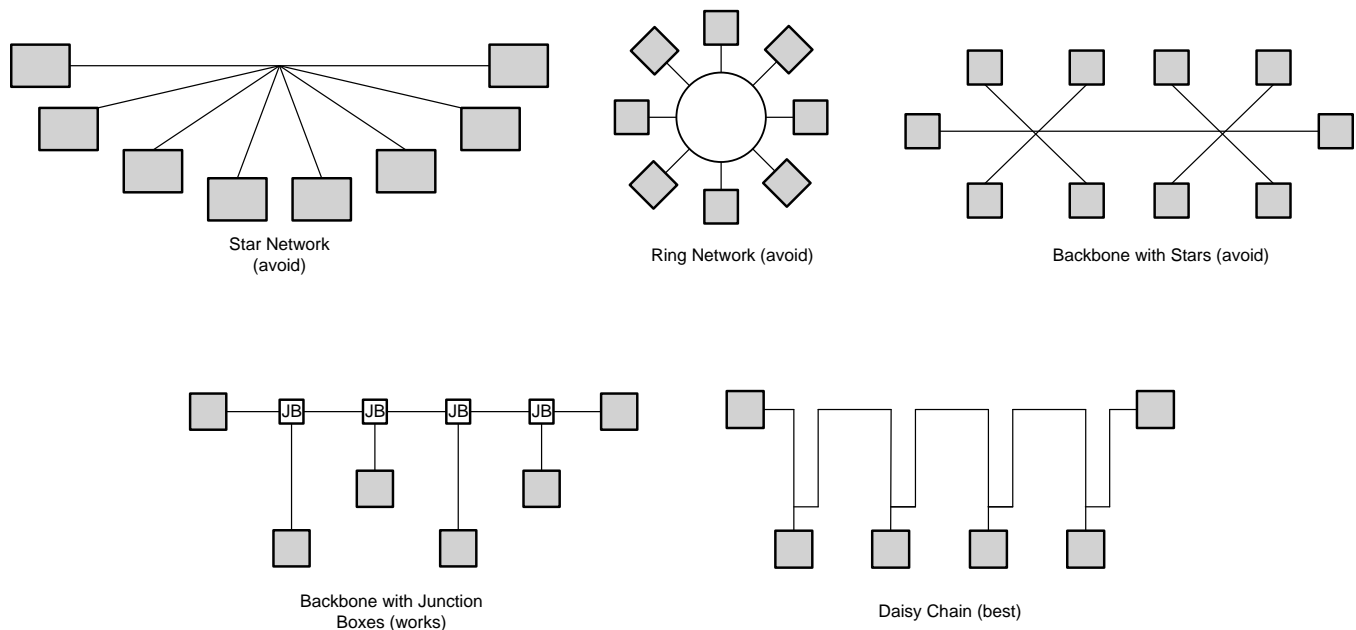


Figure 1. Network Topologies

TIDA-01365 documents the implementation of an RS-485 fan-out hub where one master nodes signal is fanned out to four slave nodes. This TI Design features automatic direction control through a precision-timing device and a DC-DC converter designed to work with common industrial supply voltages.

Building automation applications such as HVAC can benefit from this design. In an HVAC application there may be one master that handles the on and off controls of several different cooling zones in a building. The master could systematically poll the different zones requesting temperature data from the thermostats so that when needed the different zones could be activated or deactivated. Using this type of architecture allows for clusters of zones to be connected in to a main communication trunk similar to the backbone with stars architecture in Figure 1.

These same techniques can be applied to other applications such as video surveillance, factory automation and control, and lighting. In each of the above applications, there exists the possibility that a cluster of slave nodes must communicate with a master for diagnostic data, calibration, motion control, and motion sensing. In all of these applications the slave nodes can be numerous and remote where a traditional daisy chain architecture is not feasible. Using the design techniques described in this TI Design can make connecting to these slave nodes more manageable while using the 24-V industrial DC supply typically seen in these applications.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
24-V DC-DC converter	Step down converter for 24-V industrial supplies	See Section 1.4.2 and Section 2.1
RS-485 signaling	Communication interface up to 200 kbps	See Section 1.4.1 and Section 2.2
Automatic direction control	Configurable to packet length and data rate	See Section 1.4.3 and Section 2.4

1.3 Block Diagram

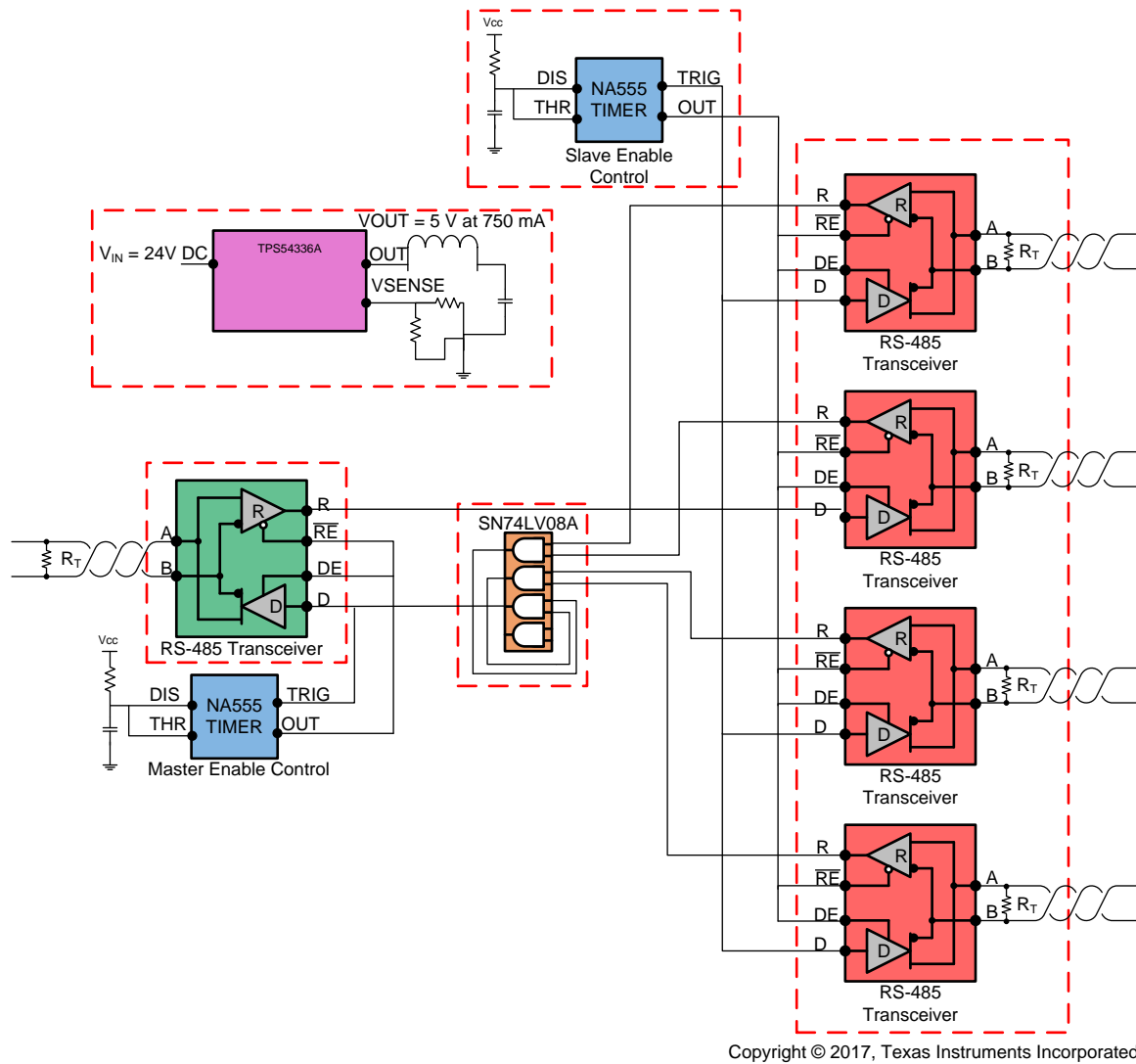


Figure 2. 24-V RS-485 Bidirectional Fan-Out Hub With Automatic Direction Control

1.4 Highlighted Products

This section highlights the Texas Instruments products used in this reference design. Each of the components is highlighted in [Figure 2](#).

1.4.1 SN65HVD3082

The SN65HVD3082E transceiver supports half-duplex operation and is designed for RS-485 data bus networks. This device is powered by a 5-V supply, supports data rates up to 200 kbps, and is fully compliant to the TIA/EIA-485-A standard.

1.4.2 TPS54336A

The TPS54336A DC-DC converter is a synchronous converter with an input-voltage range of 4.5 V to 28 V. This device has an integrated low-side switching FET that eliminates the requirement for an external diode.

1.4.3 NA555

The NA555 is a precision-timing circuit that can produce accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third of V_{CC} . These levels can be altered by using the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset, and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit can sink or source current of up to 200 mA. Operation is specified for supplies of 5 V to 15 V. Output levels are compatible with TTL inputs when using a 5-V power supply.

1.4.4 SN74LV08A

The SN74LV08A is a quad-channel, two-input positive-AND gate and is designed for 2-V to 5.5-V V_{CC} operation. The SN65LV08A device performs the Boolean AND function in positive logic. This device is fully specified for partial-power-down application using I_{off} . The I_{off} circuitry disables the outputs, which prevents damaging current backflow through the devices when they are powered down.

2 Getting Started Hardware

The TIDA-01365 TI Design includes a PCB, which is fully assembled with one SN65HVD3082E RS-485 transceiver as the master, four SN65HVD3082E RS-485 transceivers as the slaves, a TPS54336A DC-DC synchronous regulator, two NA555 precision-timing devices for separate enable controls of the master and slave devices, and a SN74LV08A quad-channel positive-AND for sending the four slave messages to the master.

2.1 Powering the PCB

V_{CC} and GND are applied to the board through the banana jack connectors P1, P2, and P3. When applying a 24-V DC source to the design, connector P2, V_{IN} , should be used, and JMP8 should be shorted using a shunt to connect the regulator output to the 5V_ V_{CC} power rail of the board. An application circuit for the TPS54336A is given in the data sheet to produce a 5-V, 3-A output from 8-V to 28-V supply, this circuit was implemented in this design to meet the 24-V V_{IN} 5-V V_{OUT} power requirements. See the *TPS5433xA 4.5-V to 28-V Input, 3-A Output, Synchronous Step-Down DC-DC Converter*[3] datasheet for more information on the performance and operating parameters of this DC-DC converter.

If 24-V is not being used during the test then a 5-V supply should be connected to P3, 5V_ V_{CC} , and JMP8 should be unshorted by removing the shunt. Because the TPS54336A is a synchronous regulator, there is an opportunity for the regulator to partially power up when connecting 5-V to its output, which is why removing the shunt is recommended.

2.2 RS-485 Signaling

During testing, the master RS-485 transceiver bus pins AM and BM, U7 and JMP6 should interface to an RS-485 bus like the main communication trunk in an RS-485 network. If this node is located at one of the farthest ends of the network then a 120- Ω termination resistor should be included. If the node falls somewhere in the middle of the bus then no termination resistor is required at the connection point. The RS-485 slave nodes (U1, U2, U3, and U5) all receive their driver input signals, D, from the master receiver output, R. JMP5 allows access for probing of the master receiver output signal, master out slave in (MOSI). The RS-485 slaves send the received master signal to their end equipments through their bus pins, A1, B1, A2, B2, A3, B3, A4, and B4. When a response is required from a slave node, the response is received through the bus pins on the slave device and driven from the receiver output, R or MISOx, to a quad-channel, positive-AND gate, which connects to the driver input, D, of the master. See the *SNx5HVD308xE Low-Power RS-485 Transceivers, Available in a Small MSOP-8 Package*[4] datasheet for more information regarding the performance of the transceiver.

2.3 Slave Receiver Output Combined

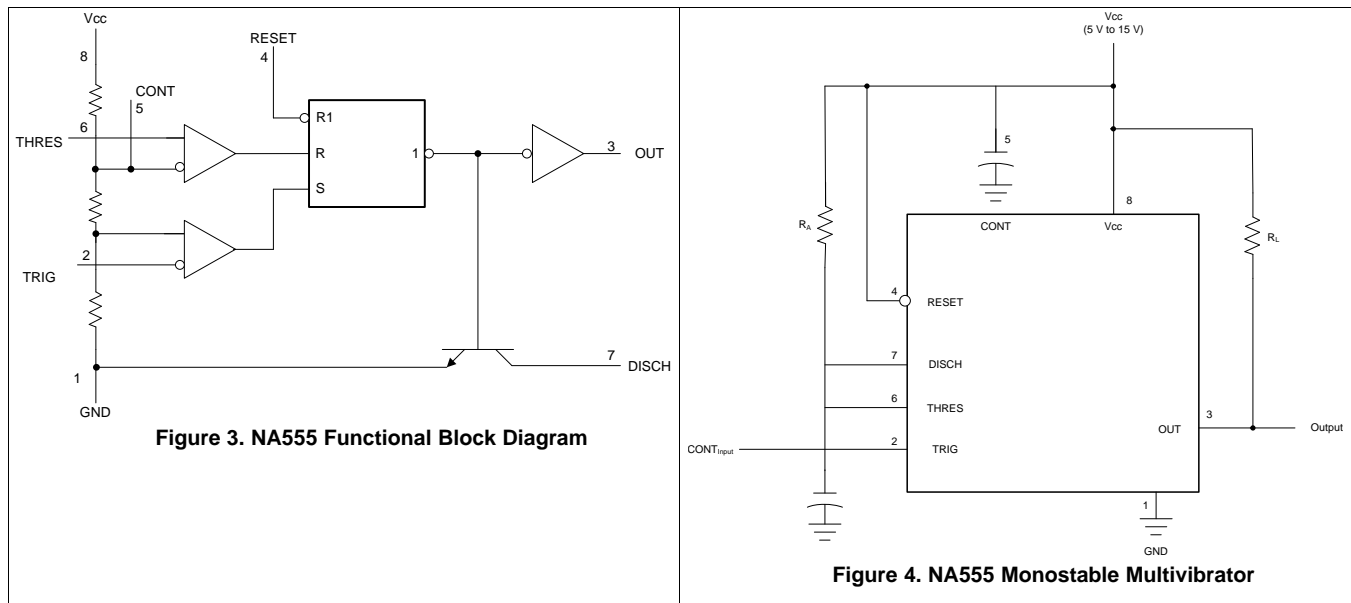
The SN74LV08A AND gate serves the purpose of combining the data from the four slave receiver outputs into a single driver input for the master. If more than one slave is communicating at a time, the data to the master will be corrupted due to collisions so care should be taken when designing the communication structure at the protocol level. A common method for this is time division multiple access (TDMA), which allocates different time slots on a bus for each node to transmit its data. Another simple method is a master-slave protocol in which slave nodes would only transmit data when it is requested by a master node. A third method would involve token passing, which means that permission to transmit is granted through a token to one node at a time, and each node sends the token to the next node in a ring after it completes transmission. See the *SN74LV08A Quadruple 2-Input Positive-AND Gates*[5] datasheet for more information on the operation parameters of this device.

2.4 Automatic Direction Control

TIDA-01365 also features separate NA555 precision timers to control the enable lines, /RE and DE, of the master and slave devices. When a negative (0 V) pulse of the start bit is applied to the trigger input (pin 2) of the monostable-configured NA555-timer oscillator, the internal comparator detects this input and sets the state of the flip-flop, which changes the output from a low state to a high state. This action turns off the discharge transistor connected to pin 7 and removes the short circuit across the external-timing capacitor (C1).

This action allows the timing capacitor to begin charging up through resistor R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of $(2/3) \times V_{CC}$ that is set up by the internal voltage-divider network. The comparator output will go high and reset the flip-flop back to the original state; this action activates the transistor and discharges the capacitor to ground through pin 7. The discharge causes the output to change its state back to the stable low value, which awaits another trigger pulse (start bit of next packet) to start the timing process again (see Figure 3 and Figure 4).

See the *xx555 Precision Timers* [6] datasheet for more information on the configuration and operation parameters.



2.5 Pulse-Duration Calculation

The pulse width is predefined according to the packet length of the protocol. The resistor and capacitor value in the monostable-multivibrator configuration are chosen to enable the driver for the entire packet length using Equation 1.

$$T = 1.1 \times R1 \times C1 \tag{1}$$

Where:

- T is in seconds
- R is in Ω
- C is in Farads

The tolerances of the selected resistor and capacitor affects the enable pulse. Ensure the calculated resistor and capacitor values provide the required enable-pulse duration, even at the boundary value of the tolerance.

The time setting components in the reference schematic and layout files for the slave nodes are designated as R15 and C8 and for the master node R22 and C14, respectively. At least 10 μ s of space between consecutive packets should be designed for to keep the trigger high for long enough to overcome the comparator-storage time.

3 Testing and Results

This section describes the test procedure and results for TIDA-01365.

3.1 TPS45366A 24-V to 5-V DC-DC Converter

The TPS54336A DC-DC regulator is good a choice for this application due to its wide input voltage range for industrial environments. The device's synchronous design eliminates the for an external diode, which reduces overall design component count. The regulator's pulse skipping mode for light loads further increases efficiency and power savings. [Figure 5](#) shows the TPS54336A output voltage ripple measurement and the switch node measurement. It can be seen that there is approximately 30 mV of output ripple on the 5-V supply and that the device is switching in a pulse skipping mode due to the load current being less than 500 mA. The maximum switching frequency under heavy load conditions for the TPS54336A is 340 kHz. When consuming less than 500 mA, the pulse skip mode operation activates, which improves overall system performance.

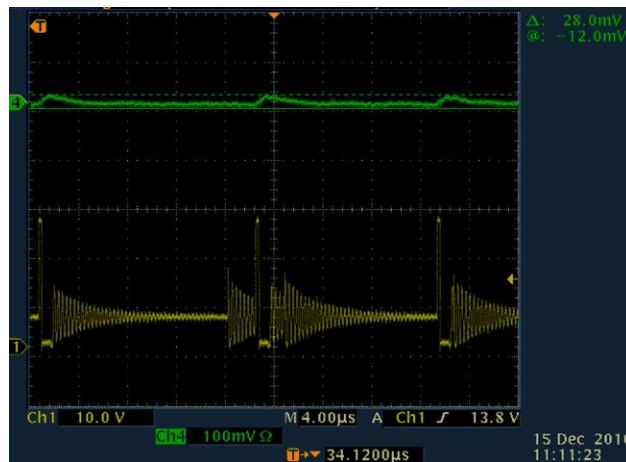


Figure 5. TPS54336A

3.2 RS-485 Bus Signaling and Automatic Direction Control

The SN65HVD3082 RS-485 transceiver was used for the TIDA-01365 reference design because of its robust system performance over long distances (>1000 m) across up to 256 RS-485 nodes, 200-kbps maximum supported data rate, and slew-rate-controlled edge transitions. Any half-duplex RS-485 transceiver from Texas Instruments could be substituted into this design to meet the design requirements of the intended application. See the full [RS-485 portfolio](#) on Texas Instruments' website for a list of products.

Figure 6 and Figure 7 show data communication at 50 kHz, a packet length ~3.5 ms (160 bits), and a ~600 μ s break in between packets allowing the trigger voltage on the NA555 timer to overcome the comparator-storage threshold time.

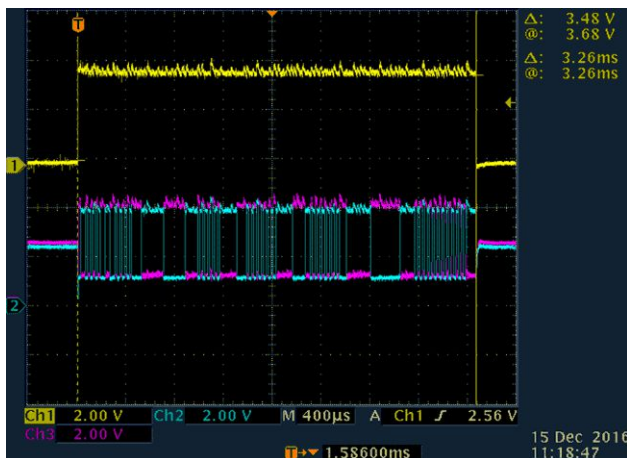


Figure 6. MOSI Zoomed

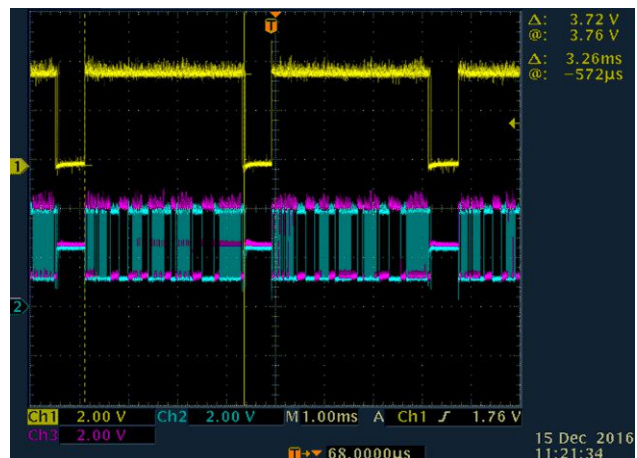


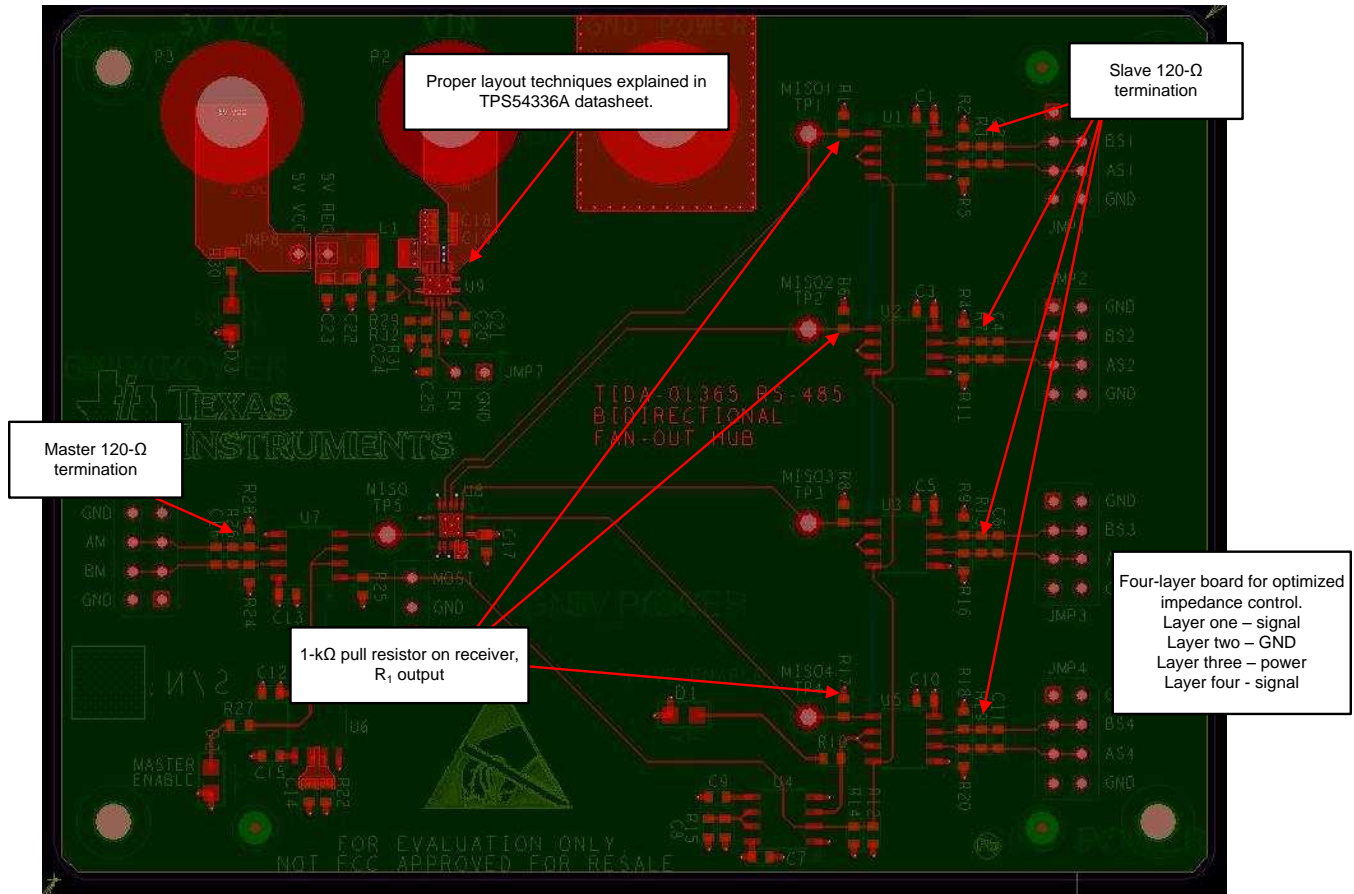
Figure 7. MOSI

The above data is fanned out from the master to the four slave devices for transmission to the end nodes. The communication works in the same manner from individual slaves back to the master although data will not pass from slave to slave. Because the receiver output on most modern transceivers is idle high, an AND gate was chosen to ensure the correct logic levels are transmitted back to the master from the slaves.

4.2 Bill of Materials

To download the BOM for each board, see the design files at [TIDA-01365](#)

4.3 PCB Layout Recommendations



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Figure 11. 24 V RS-485 Bidirectional Fan-Out Hub with Automatic Direction Control Layout Recommendations

4.3.1 Layout Prints

To download the Layout Prints for each board, see the design files at [TIDA-01365](#)

5 Related Documentation

1. Texas Instruments, [The RS-485 Design Guide](#), Application Report (SLLA272)
2. Texas Instruments, [Automatic Direction Control RS-485](#), TIDA-01090 TI Design (TIDUBW6)
3. Texas Instruments, [TPS5433xA 4.5-V to 28-V Input, 3-A Output, Synchronous Step-Down DC-DC Converter](#), TPS54335A, TPS54335-1A, TPS54336A Datasheet (SLVSCD5)
4. Texas Instruments, [SNx5HVD308xE Low-Power RS-485 Transceivers, Available in a Small MSOP-8 Package](#), SN65HVD3082E, SN75HVD3082E, SN65HVD3085E, SN65HVD3088E Datasheet (SLLS562)
5. Texas Instruments, [SN74LV08A Quadruple 2-Input Positive-AND Gates](#), SN74LV08A Datasheet (SCLS387)
6. Texas Instruments, [xx555 Precision Timers](#), NA555, NE555, SA555, SE555 Datasheet (SLFS002)

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6 About the Author

MICHAEL PEFFERS is an applications engineer at Texas Instruments supporting the RS-485, LVDS, PECL, CAN, LIN, IO-Link, and Profibus interface products. Michael is responsible for developing reference designs solutions for the industrial segment and direct customer support including onsite support as well as onsite training. Michael is also responsible for producing technical content such as application notes, datasheets, white papers, and is the author of a recurring blog on the Texas Instruments E2E forum called *Analog Wire: Get Connected*. Michael brings to this role his experience in high-speed SERDES applications as well as experience in the optical transceiver space. Michael earned his Bachelors of Science in Electrical Engineering (BSEE) from the University Of Central Florida (UCF).

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