

# **DAC39RF10 IBIS & IBIS-AMI Models**

## ***User's Guide***

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# 1 Introduction

This document describes the organization, structure, and proper usage of the TI DAC39RF10 IBIS-AMI/IBIS models (compiled and approved for external customer release), hereafter referred to as the “model” for short. The model is intended for use by the DAC39RF10 design team and by DAC39RF10 customers for system-level modeling and verification. This document assumes that you are familiar with the relevant IBIS-AMI modeling specifications. In these models the AAV package type is supported.

## 1.1 Formatting Conventions

The help readability, various formatting conventions are used throughout this document:

- Hyperlinks to material within and outside this document are marked in [blue](#).
- Courier font is used for file names, code, variables, structures, parameters, and terminal commands.

## 1.2 Charter of the SerDes IBIS-AMI models

The models are designed in accordance with the [IBIS-AMI standard](#) and attempt to model the significant characteristics of most components in the DAC39RF10. The models are not intended to be an exact representation of DAC39RF10 components implemented. Rather, the models seek to provide as high a degree of accuracy as is feasible outside of Spice-based models and simulations.

## 1.3 Is / Is Not Table

The following table describes the features and purposes of the models, as well as the limitations of the models.

Table 1: Model Is / Is Not Table

Is	Is Not
Compiled for 64-bit AMI EDA tool that run in Linux & Windows platform. The reference simulator is Keysight – ADS.	
Compliant to IBIS-AMI 6.0	Compliant to a more recent BIRD revisions, if they exist
Model of DAC39RF10 I/O functionality, non-idealities and I/O performance	Exact representation of implemented components

## 2 About This Release

### 2.1 IBIS Model Files

**Table 2: IBIS Model Files**

File Name	Type	Description
dac39rf10aav.ibs	IBIS	Marketing part# DAC39RF10AAV Package-type FCBGA #pins/pkg drawing 256-pin FCBGA

### 2.2 IBIS-AMI Model Files (ADS workspace)

**Table 3: IBIS-AMI files, ../data/**

File Name	Type	Description
DAC39RF10.ibs	IBIS	Top-level IBIS wrapper for AMI model.
DAC39RF10_Rx.ami	AMI	Parameter file for RX model as required by the IBIS-AMI standard
DAC39RF10_Rx_x64.dll DAC39RF10_Rx_x64.so	DLL, SO	Windows/Linux 64-bit compiled shared library for the RX model

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**Table 4: IBIS-AMI files, ../data/**

File Name	Type	Description
../data/ DAC39RF10_rxterm_nom.s4p DAC39RF10_rxterm_weak.s4p DAC39RF10_rxterm_strong.s4p	S4P	RX termination for 3 corner cases
xSRX.s4p	S4P	Package S4P single lanes (1SRX.s4p to 15SRX.s4p) Please note, the xSRX input lanes are AC coupled with a 22nF package capacitor.

**Table 5: additional data files, ../data/**

File Name	Type	Description
../data/ xSRX.s64p	S64P	Package 64port covering interlane coupling for all 16 input lanes. Please note, the xSRX input lanes are AC coupled with a 22nF package capacitor.
../data/ fr4_100mm.s4p fr4_150mm.s4p fr4_200mm.s4p	S4P	100/150/200mm FR4 line for test and example purposes

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## 2.3 IBIS file dac39rf10aav.ibs

### 2.3.1 Device conditions for IBIS corners

Table 7: IBIS corner conditions

Case	Silicon model	VDD18 supply	VDD10 supply	Temperature ambient
typ	nom	1.8V	1.0V	25degC
min	weak	1.71V	0.95V	125degC
max	strong	1.89V	1.05V	-55degC

### 2.3.2 Component configurations

Two different device component definitions are possible which affect the termination of following differential input pin:

M16, N16      SYSREF+-

1. DAC39RF10AAV\_PECL  
In this case the SYSREF inputs are terminated with 50Ohm to ground.
2. DAC39RF10AAV\_LVDS  
In this case a termination of typical 100Ohm between the differential SYSREF pins is defined.

### 3 IBIS-AMI Model Simulation

#### 3.1 IBIS-AMI Model Features

There are a couple of parameters in the AMI section which control the model behavior.

##### **anlg\_eql\_gaincode**

- 1 is Adaptive Equalization
- 0 is MAX Equalization for user specified setting
- 16 is No Equalization for user specified setting
- Default setting is -1

This parameter refers to EQLEVEL section in the LANE\_EQ register. Please note, the register setting defines the equalization strength in opposite order compared to the IBIS-AMI model.

##### **anlg\_eql\_zerocode**

- 0 is max zero frequency 365MHz
- 7 is min zero frequency 50MHz
- Default setting is 0

The DAC39RF10 is automatically determining the equalizer zero depending on the RATE field based on the table below. Please set anlg\_eql\_zerocode based on the desired RATE setting.

<b>RATE</b>	<b>anlg_eql_zerocode</b>	<b>zero frequency</b>
0x0	0	365 MHz
0x1	0	365 MHz
0x2	3	140 MHz
0x3	5	75 MHz

##### **anlg\_eql\_gainboost**

- 0 is gain boost turned off, EQBOOST = 0
- 1 is gain boost turned on, EQBOOST = 2
- Default setting is 0

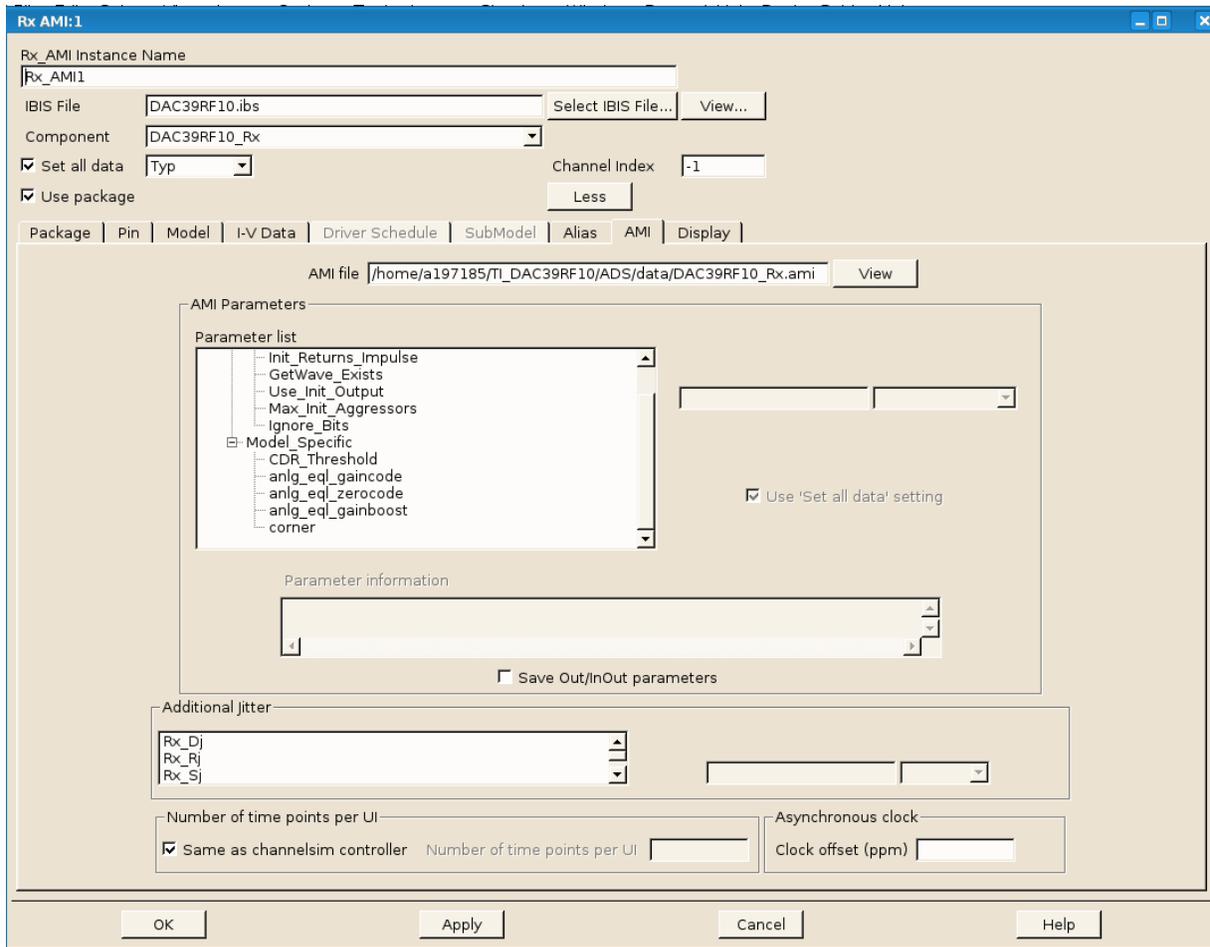
These settings map to values EQBOOST = 0, 2 in LANE\_EQ register. Please refer to device datasheet for more information.

##### **corner**

- typ, fast, slow corner definition
- 0 = typ, 1 = fast, 2 = slow
- Default setting is typ

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**Figure 1. AMI settings**

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## 3.2 Keysight ADS IBIS-AMI

### 3.2.1 IBIS-AMI basic set-up example

- Open basic set-up from ADS workspace: cell\_1\_4p – schematic
- BitRate = 12.8Gbps
- Select 1 out of 3 RX termination cases (here fast case, DAC39RF10\_rxterm\_fast.s4p, corner = fast)
- anlg\_eq\_l\_gaincode = 15 (manual setting)
- anlg\_eq\_l\_gainboost = 1
- corner = fast = 1
- all other options default

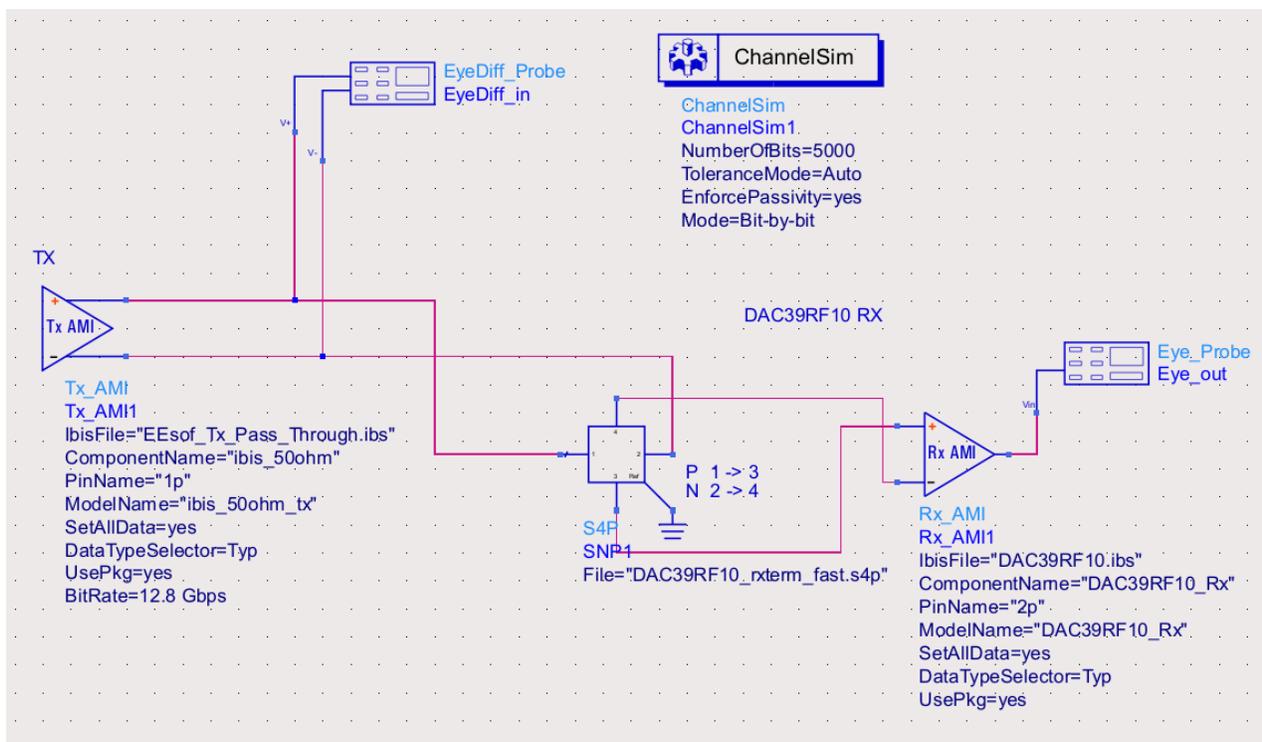
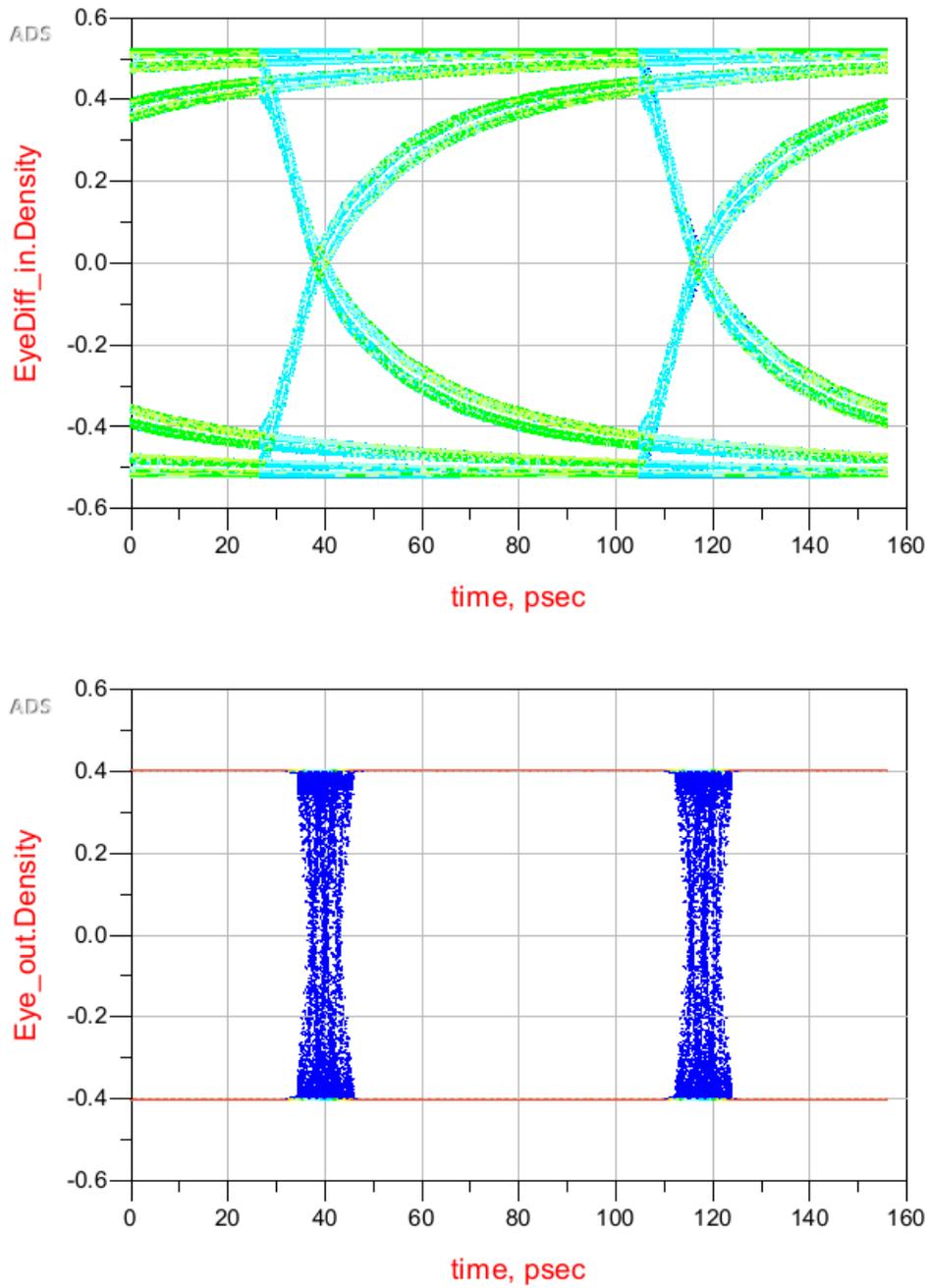


Figure 2. Basic set-up example

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**Figure 3. Eyeprobe input & output in ADS**

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### 3.2.2 IBIS-AMI basic set-up example including channel

- Open basic set-up from ADS workspace: cell\_1\_line\_4p – schematic
- Select 1 out of 3 RX termination cases (here typ case, DAC39RF10\_rxterm\_typ.s4p, corner = typ)
- Select input lane S4P data (here lane 15SRX, 15SRX.s4p)
- Add channel model (here 300mm FR4)
- all AMI settings default
- nom. case, 12.8Gbps

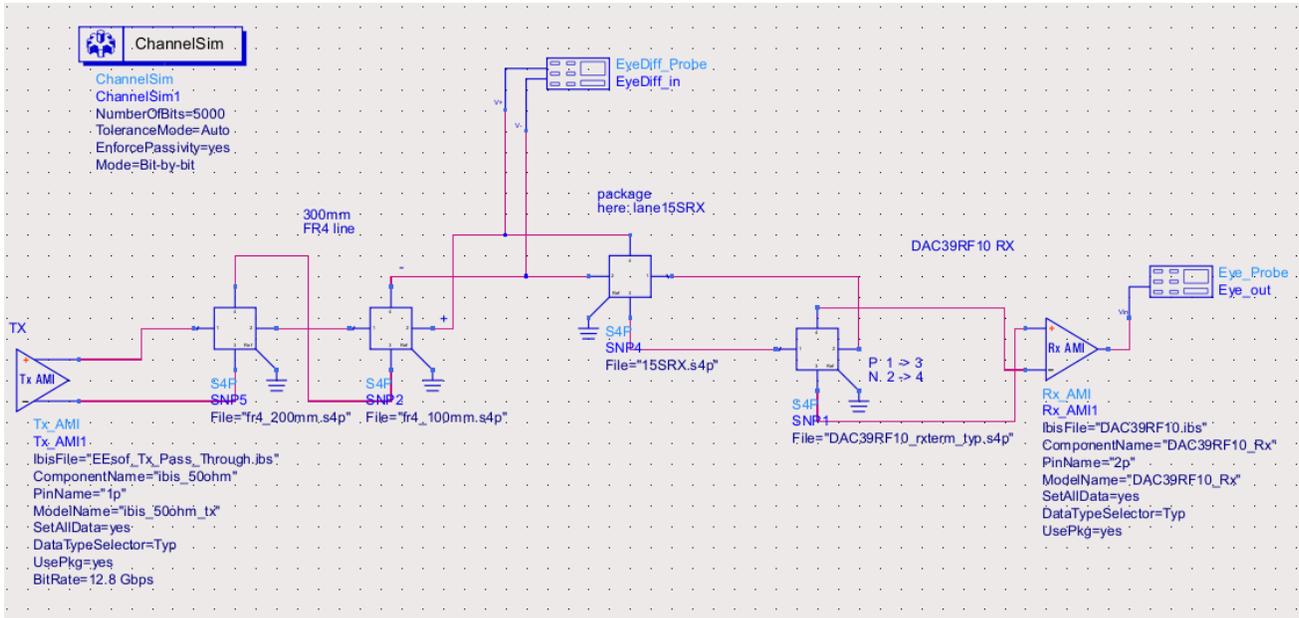
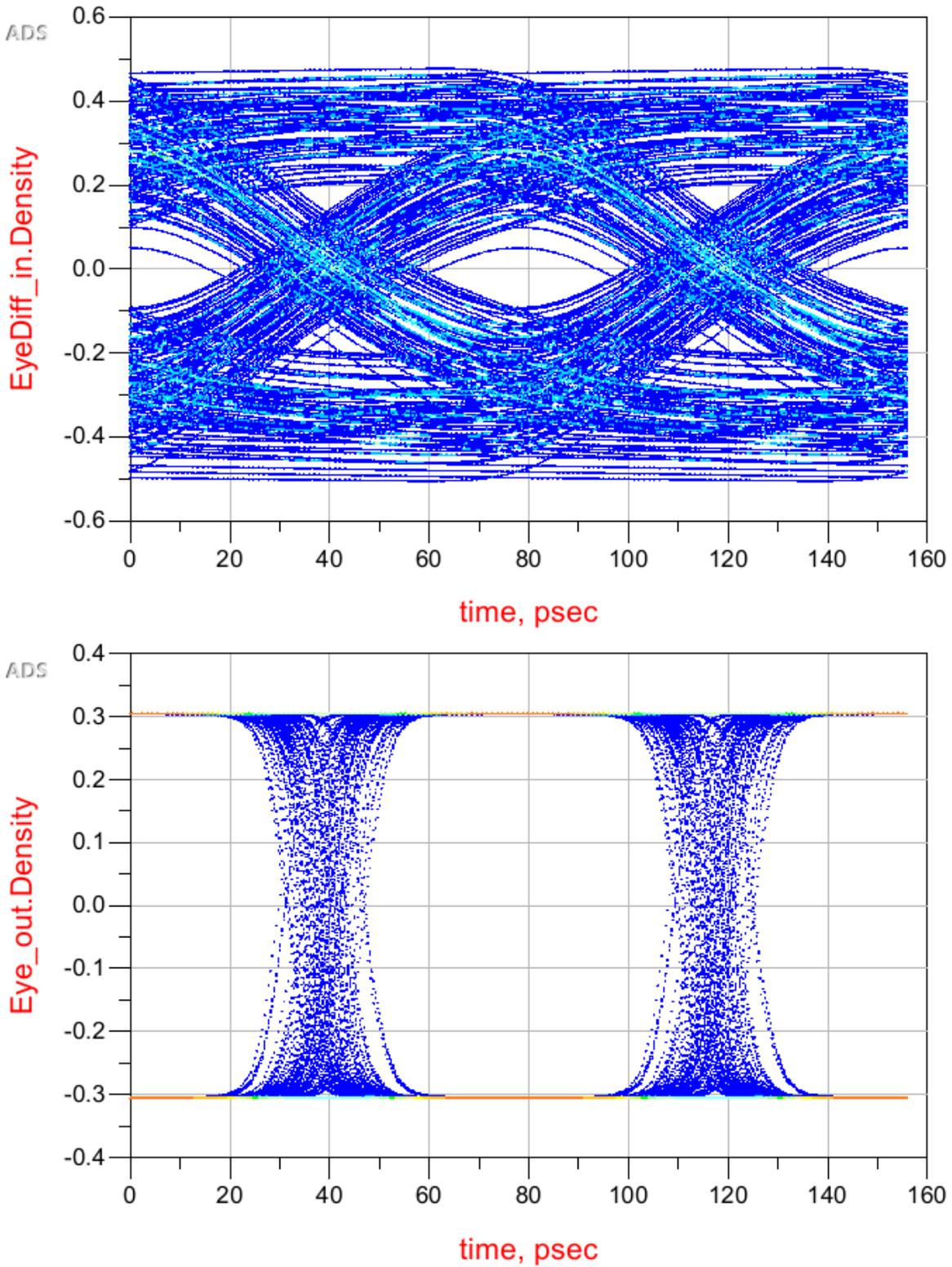


Figure 4. Basic IBIS-AMI schematic set-up in ADS

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**Figure 5. Eyeprobe input & output in ADS**

The TI IBIS-AMI models contain information on products that is based on high-level specifications. These may not accurately represent the product design in all cases. Please verify the accuracy of the models with TI before using the results.

### 3.2.3 IBIS-AMI example case with interlane coupling

The following application example in ADS can be found under cell\_2\_line\_s64p – schematic. A 300mm FR4 line is used as a channel here. In this example the xLRX.s64p package model is used. This model enables the simulation of interlane coupling.

The adaptive equalization feature is active and chooses gaincode = 12 as the optimum setting.

- IBIS-AMI 12.8Gbps
- Lane 15SRX
- 300mm FR4 channel attached
- all AMI settings default

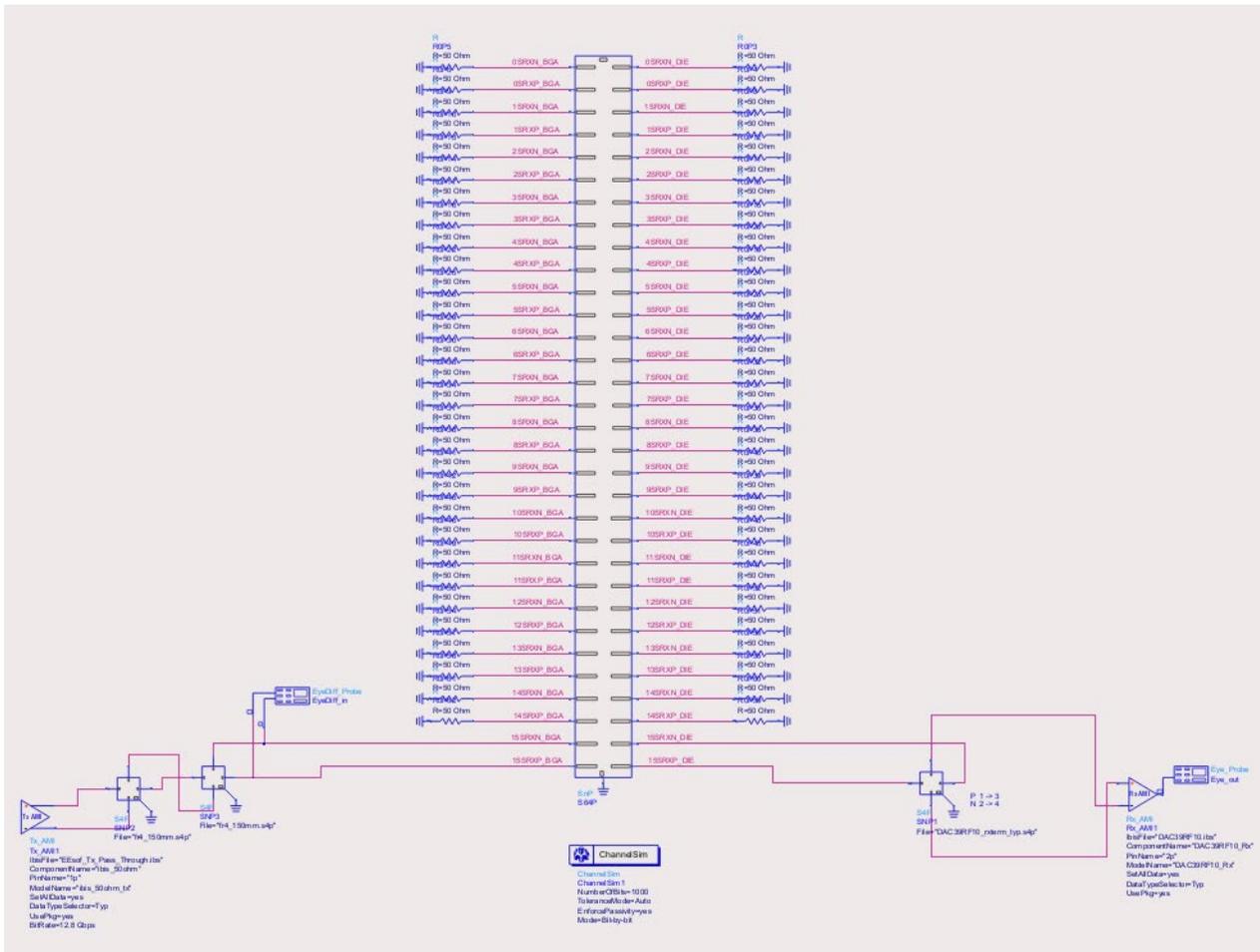
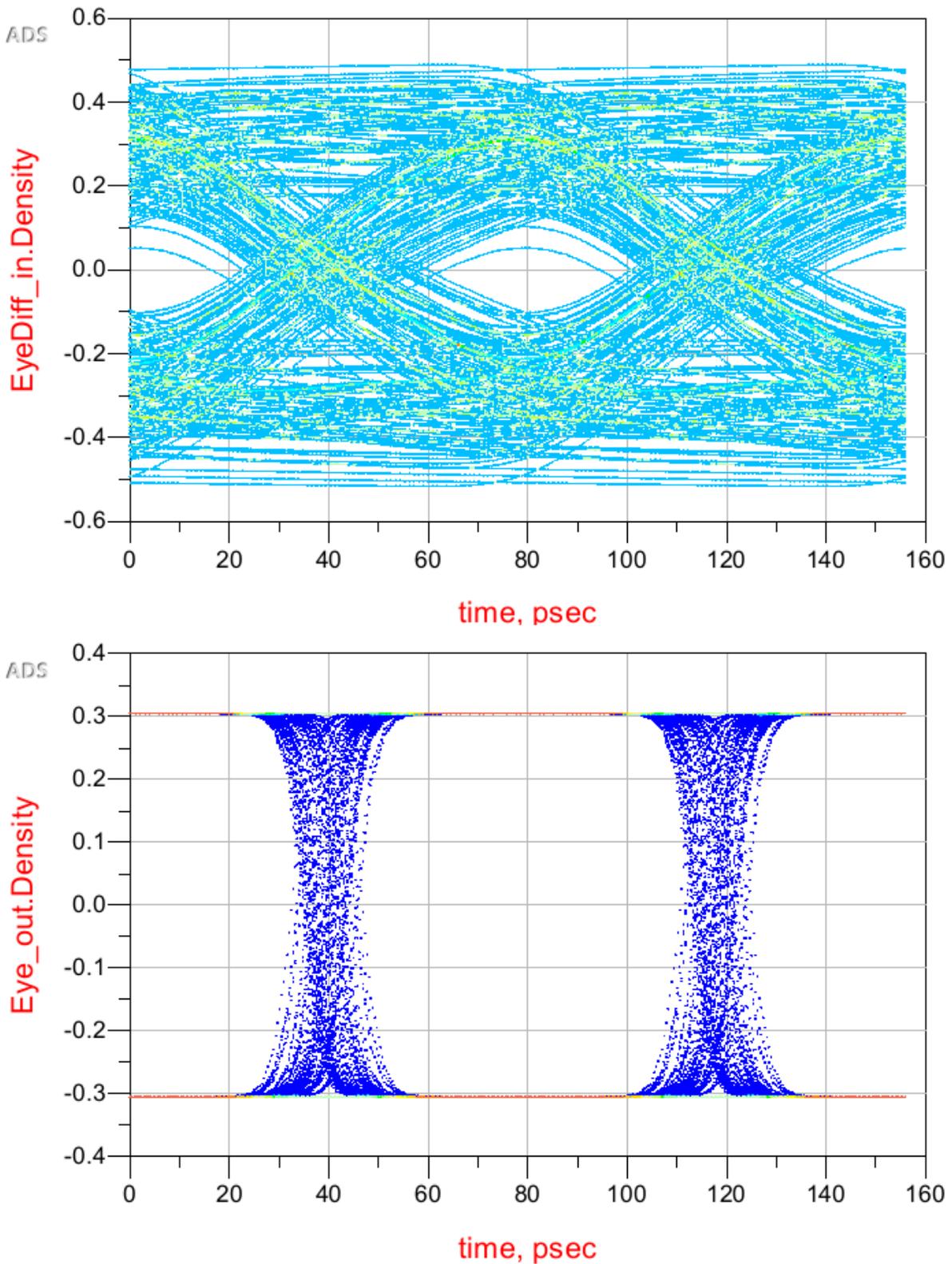


Figure 6. ADS channel example with 300mm FR4 line

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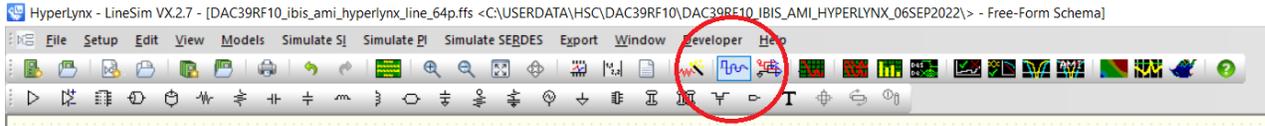
**Figure 7. ADS simulation output**

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### 3.3 HyperLynx IBIS-AMI Example

#### 3.3.1 IBIS-AMI basic set-up example

- Open **DAC39RF10\_ibis\_ami\_hyperlynx\_basic\_setup.ffe**
- Verify **Enable Lossy Simulation** is checked



- Select **Simulate SERDES/Run IBIS-AMI Channel Analysis ...**
- Select **New Settings**, click **Next**
- Select **Time domain**, click **Next**
- In Setup for Channel Characterization
  - **Transmitter probe: U1.1p/U1.1n (at die)**
  - **Receiver probe: U2.2p/U2.2n (at die)**
  - Click **Next**
- Assign and configure IBIS-AMI Models, click on **configure RX AMI...**
  - **anlg\_eql\_gaincode = 15 (manual setting)**
  - **anlg\_eql\_gainboost = 1**
  - corner = fast = 1
  - **all other options default**
  - **Save/Exit/Next**
- Optionally Sweep AMI-Model Parameters, click **Next**
- Add Jitter, click **Next**
- Define Stimulus for the Channel Analysis, **BitRate = 12.8Gbps**, click **Next**
- View Analysis Results, check **BER Plots**, click **Run**

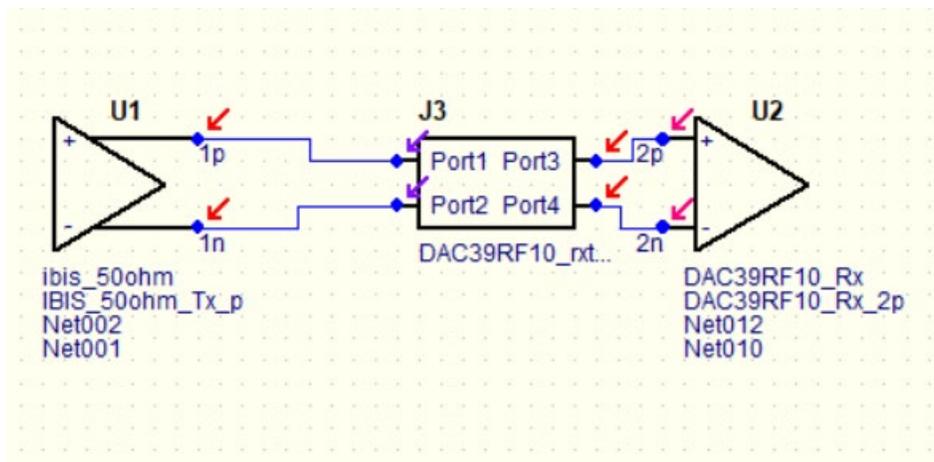
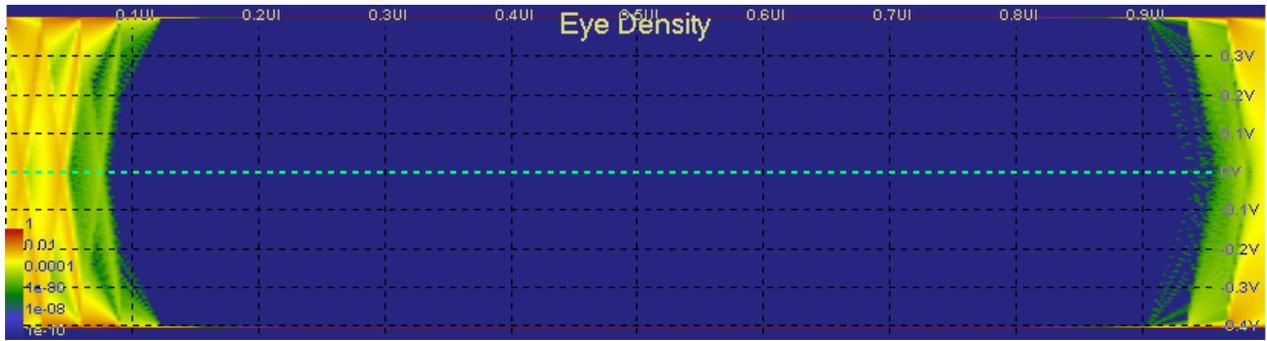


Figure 8. Basic set-up example

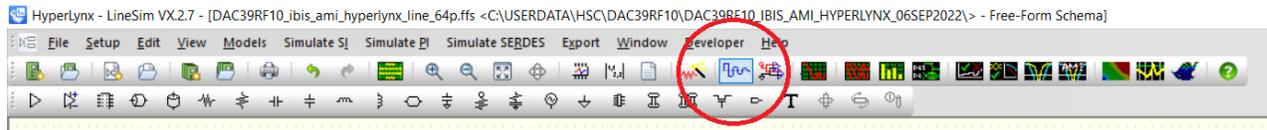
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**Figure 9. Reciever Eye in HyperLynx**

### 3.3.2 IBIS-AMI basic set-up example including channel

- Open **DAC39RF10\_ibis\_ami\_hyperlynx\_line\_4p.ffs**
- Verify **Enable Lossy Simulation** is checked



- Select **Simulate SERDES/Run IBIS-AMI Channel Analysis ...**
- Select **New Settings**, click **Next**
- Select **Time domain**, click **Next**
- In Setup for Channel Characterization
  - **Transmitter probe: U1.1p/U1.1n (at die)**
  - **Receiver probe: U2.2p/U2.2n (at die)**
  - Click **Next**
- Assign and configure IBIS-AMI Models, click on **configure RX AMI...** and keep default values
  - **anlg\_eql\_gaincode = -1 (adaptive setting)**
  - **anlg\_eql\_gainboost = 0**
  - corner = nominal = 0
  - **all other options default**
  - **Save/Exit/Next**
- Optionally Sweep AMI-Model Parameters, click **Next**
- Add Jitter, click **Next**
- Define Stimulus for the Channel Analysis, **BitRate = 12.8Gbps**, click **Next**
- View Analysis Results, check **BER Plots**, click **Run**

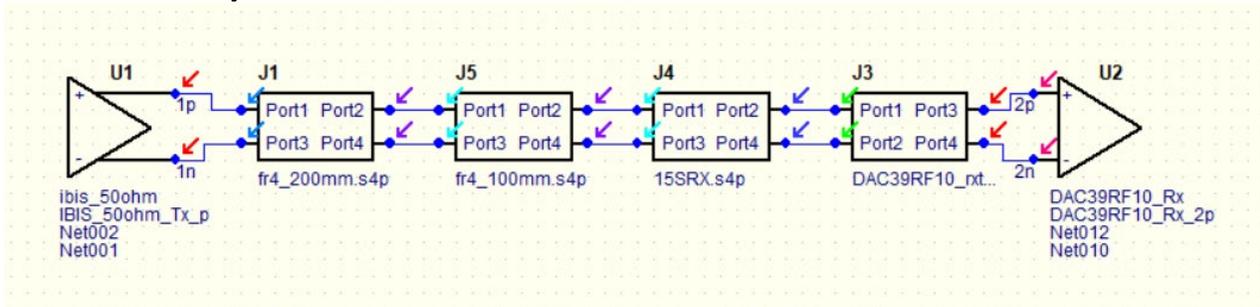
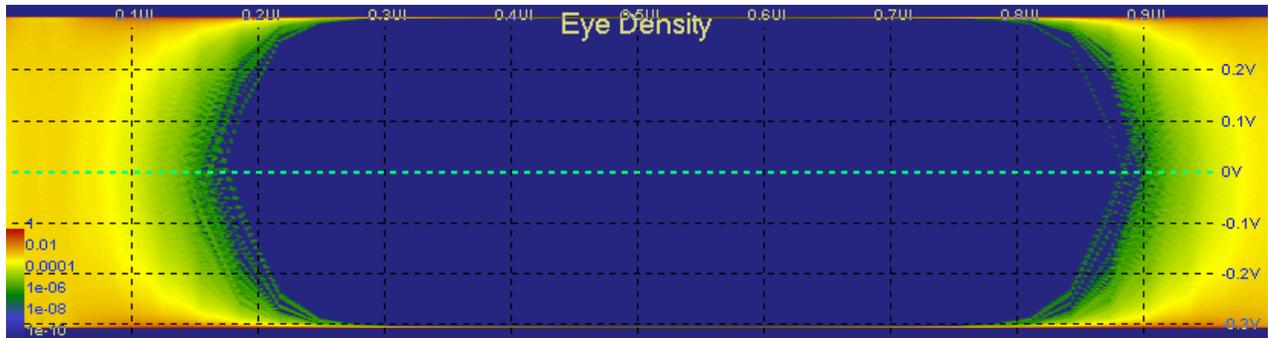


Figure 10. IBIS-AMI schematic set-up in HyperLynx

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**Figure 11. Receiver Eye in HyperLynx**

The adapted equalizer value (gain\_code) can be found in the file DAC38J48.adapt (this is a text file). The gain\_code is the second value listed, in this case it adapted to a value of 12.

```
0 , 12, -1.70196, -0.00392157, -1, -3, -1
```

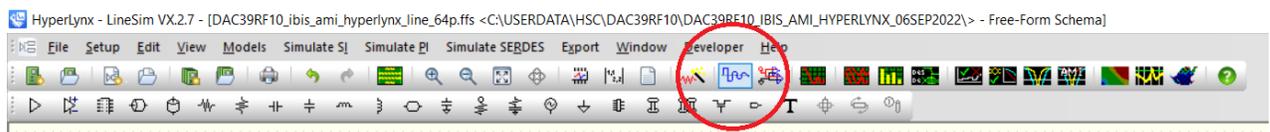
### 3.3.3 IBIS-AMI example case with interlane coupling

The following application example in Hyperlynx can be found in file DAC39RF10\_ibis\_ami\_hyperlynx\_line\_64p.ffs. A 300mm FR4 line is used as a channel here. In this example the xIRX.s64p package model is used. This model enables the simulation of interlane coupling.

The ports are defined as

```
Port[1] = 0SRXN_BGA
Port[2] = 0SRXN_DIE
Port[3] = 0SRXP_BGA
Port[4] = 0SRXP_DIE
Port[5] = 1SRXN_BGA
Port[6] = 1SRXN_DIE
Port[7] = 1SRXP_BGA
Port[8] = 1SRXP_DIE
...
```

- Open **DAC39RF10\_ibis\_ami\_hyperlynx\_line\_64p.ffs**
- Verify **Enable Lossy Simulation** is checked



- Select **Simulate SERDES/Run IBIS-AMI Channel Analysis ...**
- Select **New Settings**, click **Next**
- Select **Time domain**, click **Next**
- In Setup for Channel Characterization
  - **Transmitter probe: U1.1p/U1.1n (at die)**

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- Receiver probe: U2.2p/U2.2n (at die)
- Click **Next**
- Assign and configure IBIS-AMI Models, click on **configure RX AMI...** and keep default values
  - **anlg\_eq1\_gaincode = -1** (adaptive setting)
  - **anlg\_eq1\_gainboost = 0**
  - corner = nominal = 0
  - **all other options default**
  - **Save/Exit/Next**
- Optionally Sweep AMI-Model Parameters, click **Next**
- Add Jitter, click **Next**
- Define Stimulus for the Channel Analysis, **BitRate = 12.8Gbps**, click **Next**
- View Analysis Results, check **BER Plots**, click **Run**

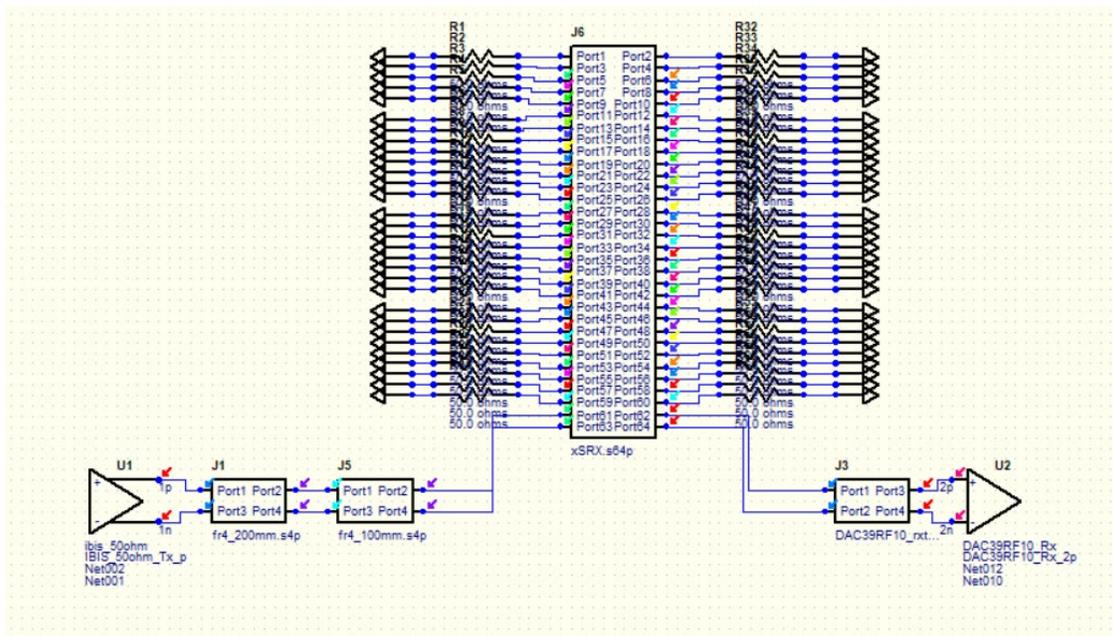


Figure 12. HyperLynx channel example with 300mm FR4 line



Figure 13. Receiver Eye in HyperLynx

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The adapted equalizer value (gain\_code) can be found in the file DAC38J48.adapt (this is a text file). The gain\_code is the second value listed, in this case it adapted to a value of 12.

0 , 12, 1e-16, 0, 0, 2, 0