REVISIONS		
REV #	DESCRIPTION	DATE
REV #	CCN #	DDMMYY

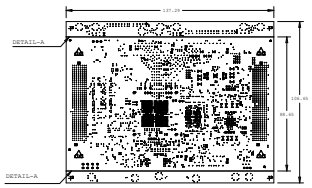
FABRICATION NOTES:

1. FABRICATE PCB IN ACCORDANCE WITH IPC-6012C, CLASS 2, PER IPC-4011.
   PCB SHALL BE MANUFACTURED USING IRULA 370HR OR EQUIVALENT.
2. MATERIALS:
   1. LAMINATE AND PREPREG (8-STAGE) TO BE IN ACCORDANCE WITH IPC-4101/126.
      (NEMA TO 180)
   2. COPPER FOIL TO BE IN ACCORDANCE WITH IPC-MF-150. UNLESS OTHERWISE SPECIFIED,
      ALL COPPER WEIGHT FOR INNER SIGNAL LAYERS TO BE 17.5UM (0.5 OZ.) AND INNER PLANE LAYERS TO BE 35UM (1 OZ.).
      FOR OUTER LAYERS 1.33 OZ. COPPER WEIGHT IS TO BE CONSIDERED "FINISHED".
      THE COPPER FOIL THICKNESS TOLERANCES SHALL BE AS PER IPC 4012B TABLE NO.3-7 AND 3-8.
3. ALL HOLES SHALL BE LOCATED WITHIN 0.13MM DIAMETER OF TRUE POSITION.
   LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.125MM.
4. NOR AND TRUST SHALL NOT EXCEED MORE THAN 2.75% OF THE DESIGN LENGTH.
5. CONDUCTOR WIDTH SHALL NOT BE LESS THAN 20% FROM ITS ORIGINAL DATA. INCASE FOR MATCHING
   IMPEDANCE MINIMAL SHALL APPROVE THE MODIFIED WIDTHS AND SPACING.
   TRACE WIDTH SHALL BE MEASURED ON THE SURFACE IN CONTACT WITH THE LAMINATE.
6. AUTOMATED OPTICAL INSPECTION OF ALL THE LAYERS IS REQUIRED.
7. PLATING:
   1. ALL EXPOSED CONDUCTIVE PATTERN AREAS NOT COVERED WITH SOLDER MASK OR OTHER PLATING SHALL BE ENIG,
      ELECTROLESS NICKEL/IMMERSION GOLD, ELECTROLESS NICKEL SHALL BE 3-6 MICRONS, TYPICAL IMMERSION GOLD
      THICKNESS SHALL BE 0.04-0.06 MICRONS OF SOLDERABLE IMMERSION GOLD SURFACE.
   2. APPLY LIQUID PHOTO IMAGEABLE SOLDER MASK PER IPC-SM-840, CLASS H, TO BOTH SIDES OF THE BOARD OVER BARE COPPER.
      VIA HOLES THAT HAVE MASK OPEN SHALL BE FILLED WITH NON CONDUCTIVE INK AND CAP PLATED.
      ALL OTHER VIA HOLES SHALL BE FILLED WITH NON CONDUCTIVE INK AND COVERED WITH SOLDER MASK.
      ONLY SOLDERMASK INKDES THAT ARE 0.08(0.003") PER SIDE SHALL BE REDUCED IF REQUIRED.
      ALL OTHER SOLDER MASK INKDES SHALL NOT BE ENLARGED. DEFAULT COLOUR OF SOLDER MASK SHALL BE GREEN.
   3. SILKSCREEN SHALL BE WHITE, PERMANENT, ORGANIC, NON-CONDUCTIVE INK. THERE SHALL BE
      NO SILKSCREEN ON ANY SOLDERABLE COMPONENT PAD. CLIPPING OF SILK SCREEN SHALL BE ALLOWED
      IF THE SILK SCREEN FALLS ON SOLDERABLE AREAS.
   4. SURFACE AND VIA HOLES FINISH SHALL NOT BE LESS THAN 20UM [0.0007"]; INCASE OF LASER
      VIA'S, BLIND VIA'S SHALL NOT BE LESS THAN 12UM [0.0014"]; AND BURIED VIA'S SHALL NOT BE LESS THAN 15UM [0.0006"].
   5. ALL HOLES SURROUNDED BY LAND <=0.010" SHALL BE COMPLIAN TO IPC6012, CLASS 2.
8. MARKING:
   1. BOARD SHALL MEET THE REQUIREMENTS OF UL-796E WITH FLAMMABILITY RATING OF MINIMUM 94V-0. UL LOGO,UL FILE NUMBER,
      MANUFACTURER'S IDENTIFICATION AND DATE CODE LETTER SHALL BE RENDERED IN SILKSCREEN.
9. TEST REQUIREMENTS:
   1. 100% NET LIST ELECTRICAL VERIFICATION USING NEUTRAL SUPPLIES IPC-D-356 NET LIST FOR OPENS AND SHORTS.
10. THIEVING IS ALLOWED ONLY IN THE PANEL FRAME, NOT IN THE CIRCUIT AREA.
11. TEAR DROPS SHALL BE ADDED ON INTERNAL AND EXTERNAL LAYER FOR ALL THE VIA'S AND THROUGH HOLE PADS.
12. FINISHED PCB THICKNESS SHALL BE 0.062" +/-10%.
13. MIN TRACE WIDTH/SPACING ON BOARD IS 0.003"/0.0032".
14. ALL THE IMPEDANCE SHALL BE MATCHED AS PER IMPEDANCE TABLE WITH +/-10% TOLERANCE.
15. ALL UNCONNECTED VIA'S SHALL BE SUPPRESSED IN INTERNAL LAYERS.
16. BACKDRILLING TO BE DONE FROM L01 TO L07.

MATERIALS: TOP to L7-PAR/BRD				
ALL UNITS ARE IN MILS				
MATERIAL	SIZE	TOLERANCE	PLATED	QTY
2	7.94	+3.0/-2.0	PLATED	24
		FOR LARGE	HOLE NOT ON	
		2:16 HOLE	LS	

NOTES:
- DRILL SIZES LISTED IN LARGEST
- NOT CONSIDERED FINISHED.
- DRILL SIZE IS ADJUSTED TO REJECT TOOLING FOR OVERDRILLING.
- LARGEST SIZE NOT SPECIFY DEPTH ZERO ALIGNMENT TOLERANCE LAYER.

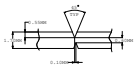
DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FINISHED	SIZE	TOLERANCE	PLATED	QTY
▲	7.94	+3.0/-2.0	PLATED	24
▲	7.99	+3.0/-2.0	PLATED	140
▲	8.0	+3.0/-2.0	PLATED	2738
▲	10.0	+3.0/-2.0	PLATED	658
▲	12.0	+3.0/-2.0	PLATED	67
◆	36.0	+3.0/-2.0	PLATED	3
◆	40.0	+2.0/-2.0	PLATED	6
◆	60.0	+3.0/-2.0	PLATED	2
◆	80.0	+3.0/-2.0	PLATED	12
◆	86.0	+2.0/-2.0	PLATED	3
■	36.0	+1.0/-1.0	NON-PLATED	2
■	62.0	+2.0/-2.0	NON-PLATED	6
■	38.0	+3.0/-3.0	NON-PLATED	6
■	86.0	+3.0/-3.0	NON-PLATED	6
■	108.0	+3.0/-3.0	NON-PLATED	6
▲	250.0	+3.0/-3.0	NON-PLATED	6



IMPEDANCE SPECIFICATIONS:

SL#	TYPE	LAYER	TRACEWIDTH(Mils)	SPACING(Mils)	IMPEDANCE(Ohms)	REF LAYER
01.	EDGE COUPLED MICROSTRIP	L1/L12	4.1	6.4	100	L2/L11
02.	EDGE COUPLED MICROSTRIP	L1/L12	5	5.5	90	L2/L11
03.	EDGE COUPLED MICROSTRIP	L1/L12	6	5.5	85	L2/L11
04.	MICROSTRIP	L1/L12	6.5	-	50	L2/L11
05.	MICROSTRIP	L1	10	-	40	L2
06.	MICROSTRIP	L1	8.9	-	38	L2
07.	EDGE COUPLED STRIPLINE	L8 L10	3.9	8.1	100	L7/L7 L9/L11
08.	EDGE COUPLED STRIPLINE	L8 L10	4.5	6.5	90	L7/L9 L9/L11
09.	EDGE COUPLED STRIPLINE	L8 L10	5	6.5	85	L7/L9 L9/L11
10.	EDGE COUPLED STRIPLINE	L3 L5	5.88	6.12	80	L2/L4 L4/L6
11.	EDGE COUPLED STRIPLINE	L10	6.35	5.65	76	L9/L11
12.	EDGE COUPLED MICROSTRIP	L1	7.2	8.3	120	L4
13.	STRIPLINE	L3,L5 L8,L10	4	-	50	L2/L4,L4/L6 L7/L9,L9/L11
14.	STRIPLINE	L3,L5,L8	6.45	-	40	L2/L4,L4/L6,L7/L9
15.	STRIPLINE	L10	7	-	38	L9/L11

LAYER STACKUP



DETAIL-A(V-GROOVE DETAILS)
SCALE:NTS

SIGNATURES	DATE
LAYOUT BY DAK/RA	010920
REVIEWED BY RA	020920
APPROVED BY AMG	020920

TEXAS INSTRUMENTS

PROC105E6

J7200X SOM 941x+8764x BRD

SIZE D | Rev 66

SCALE: NONE | SHEET 1 OF 19