# SK-AM68 Processor Starter Kit
# SoM Board

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Project :
J7 EVM

TEXAS INSTRUMENTS

Title
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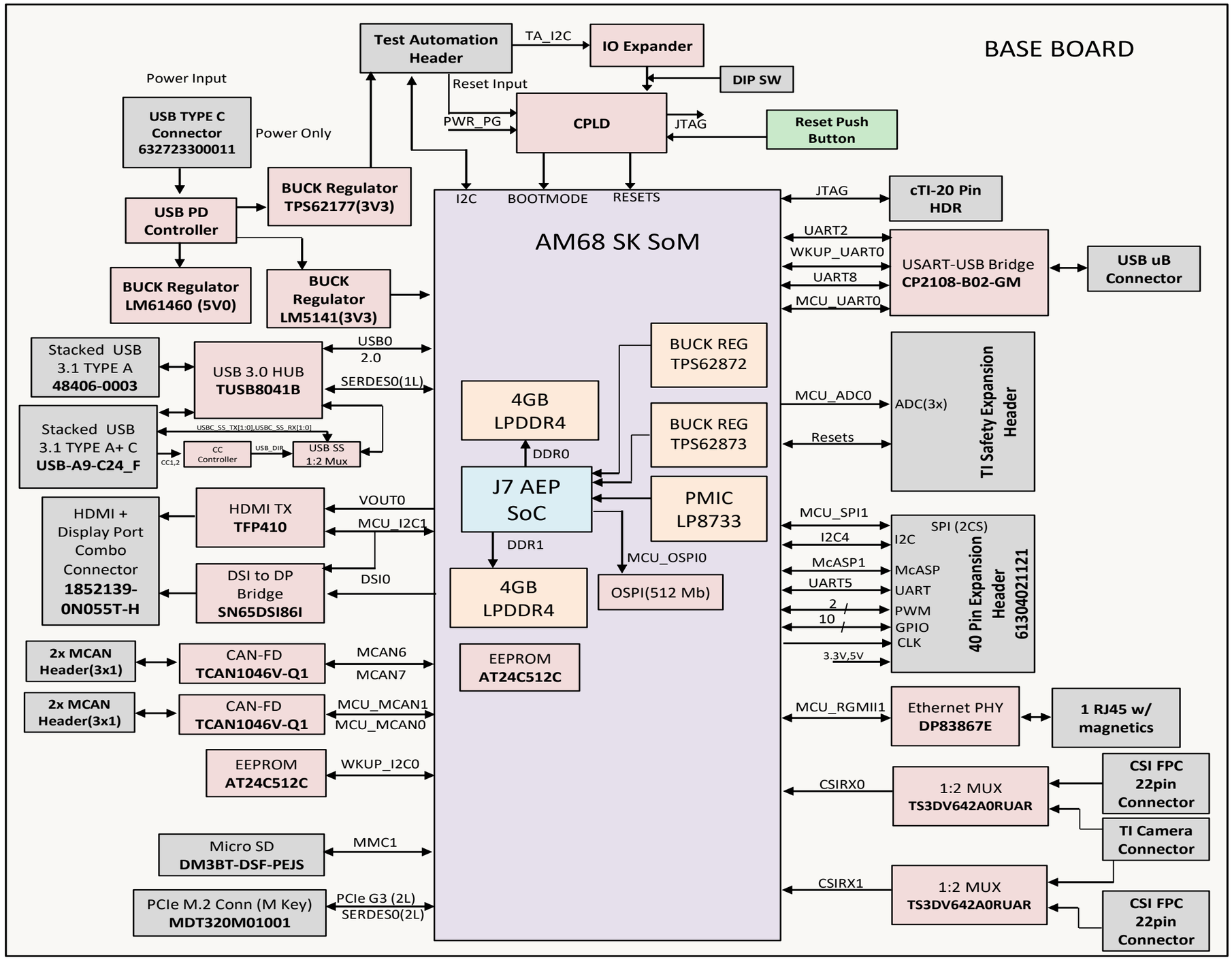
|---|---|---|
| C | PROC131 001 AM68 SK | E1 |
| Date: | Tuesday, October 04, 2022 | Sheet 1 of 21 |

# REVISION HISTORY

| REV # | DATE | DESCRIPTION OF CHANGES | AUTHOR | REVIEWED BY | APPROVED BY |
|---|---|---|---|---|---|
| E1 | 12-OCT-2021 | Initial Draft | Mistral Design Team | | |
| | 03-NOV-2021 | Updated for GPIO Assignment given by TI | Mistral Design Team | | |
| | 09-NOV-2021 | Updated for Power pins and rearranged signal pins in sodimm connector<br>Changed C1163 to 100uF and removed C1162 | Mistral Design Team | | |
| | 11-NOV-2021 | Updated variant list and added GND test points | Mistral Design Team | | |
| | 16-NOV-2021 | Updated to latest PDN v0.4 | Mistral Design Team | | |
| | 18-NOV-2021 | Swapped CSI signals on DIMM connector for routing ease<br>Updated GPIO mapping table | Mistral Design Team | | |
| | 24-NOV-2021 | Moved VSYS_IO_3V3 INA to Base board<br>Changed Board ID EEPROM to AT24C512C-MAHM-T device<br>Swapped SODIMM connectors for routing ease | Mistral Design Team | | |
| | 29-NOV-2021 | Added Mounting hole | Mistral Design Team | | |
| | 1-DEC-2021 | Updated Tripad capacitors footprint<br>Updated VSYS_IO_3V3 supply connection | Mistral Design Team | | |
| | 1-DEC-2021 | Changed U12 to TXS0102<br>Changed R119 to 10K | Mistral Design Team | | |
| | 5-AUG-2022 | Changed U12 to TXS0102 | Mistral Design Team | | |
| | 10-AUG-2022 | Updated SoC symbol | Mistral Design Team | | |
| | 17-AUG-2022 | DNI'd capacitors C67,C365, C351<br>Changed pin assignment for VDD_SD_DV | Mistral Design Team | | |
| | 19-AUG-2022 | Removed TP16 | Mistral Design Team | | |
| | 24-AUG-2022 | Updated PMIC part number | Mistral Design Team | | |
| | 29-AUG-2022 | Updated block diagrams<br>Updated DDR part number to MT53E2G32D4DE-046 AUT:C | Mistral Design Team | | |
| | 29-AUG-2022 | Updated for TI review comments | Mistral Design Team | | |
| | 12-SEP-2022 | Updated murata capacitors part numbers | Mistral Design Team | | |
| | 04-OCT-2022 | Updated Title block and board name | Mistral Design Team | | |

# SYSTEM BLOCK DIAGRAM




| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: BLOCK DIAGRAM |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
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# PDN

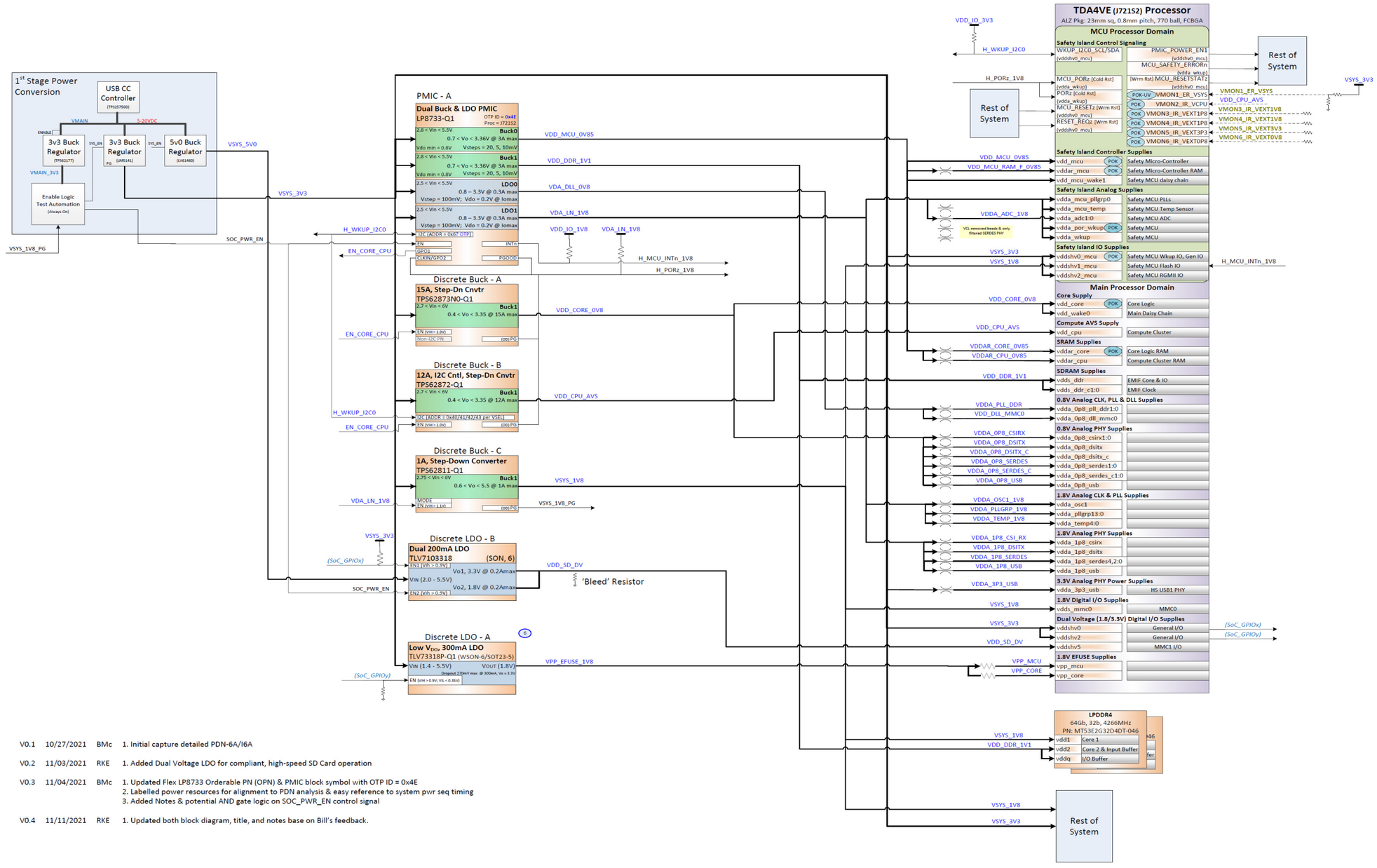
## J721S2 SK Edge AI - Flex + Tulip PDN-6B/I6B

(Power Rail & GPIO Mapping Overview)

Flex PMIC, PN LP87334ERHDR-Q1 (TI OTP ID = 4E)
Tulip Buck, PN TPS62873N0xxx-Q1
Tulip Buck, PN TPS62872??xxx-Q1 (TI OTP ID = ??)

### Features Supported :

1. J721S2 Superset Use-Case Performance with 2.0GHz clock and Peak Power est.
2. Supports J721S2 Junction Temperature (Tj) up to 105C
3. 32Gb LPDDR4 Memory, Dual 32b Interfaces at 4266MTs
4. Supports both 3.3V and 1.8V digital IO
5. Includes capacity on IO rails to support variety of peripherals (xSPI Flash, eMMC, etc)
6. Supports UHS-I compliant SD cards (Dual-Voltage IO)
7. High Secure/Field Securable Device Support
8. No Low/Partial Power Modes Support (MCU-only, Retention, etc)




| | | | |
|---|---|---|---|
| V0.1 | 10/27/2021 | BMc | 1. Initial capture detailed PDN-6A/I6A |
| V0.2 | 11/03/2021 | RKE | 1. Added Dual Voltage LDO for compliant, high-speed SD Card operation |
| V0.3 | 11/04/2021 | BMc | 1. Updated Flex LP8733 Orderable PN (OPN) & PMIC block symbol with OTP ID = 0x4E<br>2. Labelled power resources for alignment to PDN analysis & easy reference to system pwr seq timing<br>3. Added Notes & potential AND gate logic on SOC_PWR_EN control signal |
| V0.4 | 11/11/2021 | RKE | 1. Updated both block diagram, title, and notes base on Bill's feedback. |

Project : J7 EVM

Title: PDN

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|---|---|---|
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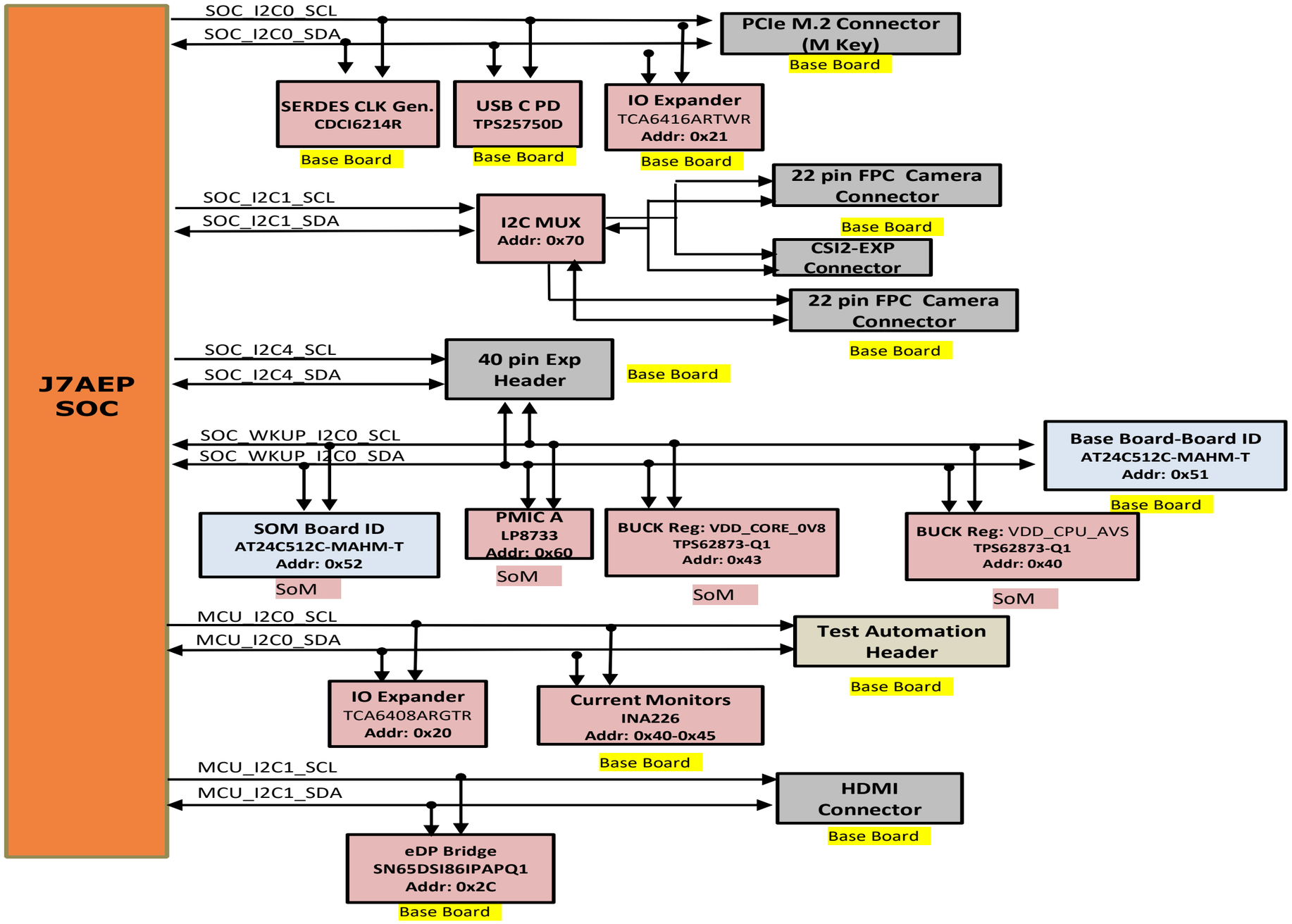
# SoM I2C TREE DIAGRAM

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|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SoM I2C TREE DIAGRAM |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
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# SoM I2C ADDRESS TABLE

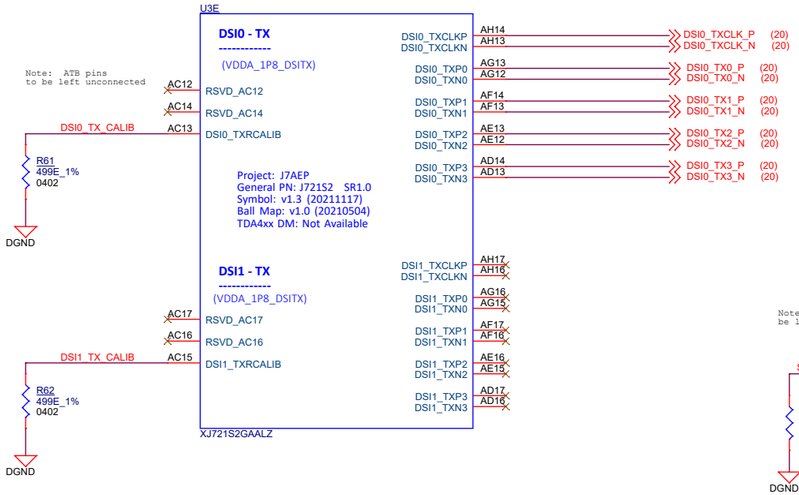
| Board | Interface name | Part# | Address | J7AEP Port mapping |
|---|---|---|---|---|
| EVM/SoM | Board ID EEPROM | CAV24C256WE-GT3 | 0x51 | WKUP_I2C0 |
| EVM/CPB | Board ID EEPROM | AT24C512C-MAHM-T | 0x52 | |
| EVM/CPB | 40 pin Expansion Header | | | |
| EVM/SoM | PMIC and BUCK's | PMIC A: LP7733 | 0x60 | |
| | | BUCK: TPS62873 | 0x40 | |
| | | BUCK: TPS62873 | 0x43 | |
| EVM/CPB | 16 bit I2C GPIO Expander | TCA6424ARGJR | 0X21 | Main I2C0 |
| EVM/CPB | SerDes Clock gen | CDCI6214 | Optional | |
| EVM/CPB | PCIe M.2 M Key | | | |
| EVM/CPB | USC C PD controller | TPS25750DRJKR | 0x20 | |
| EVM/CPB | I2C MUX | TCA9543APWR | 0x70 | Main I2C1 |
| EVM/CPB | CSI2 Expansion Connector | QSH-020-01-L-D-DP-A-K | | |
| EVM/CPB | CSI FPC Connector | 22_1734248 | | |
| EVM/CPB | 40 pin Expansion Header | | | Main I2C4 |
| EVM/SoM | CURRENT MONITORs | INA231AIYFDR | 0x40,0x41,0x41,0x43,0x44,0x45 | MCU I2C0 |
| EVM/CPB | Test automation header | | | |
| EVM/CPB | Bootmode IO Expander | TCA6408ARGTR | 0x20 | |
| EVM/CPB | eDP Bridge | SN65DSI86IPAPQ1 | 0x2C | MCU I2C1 |

# SoC GPIO MAPPING TABLE

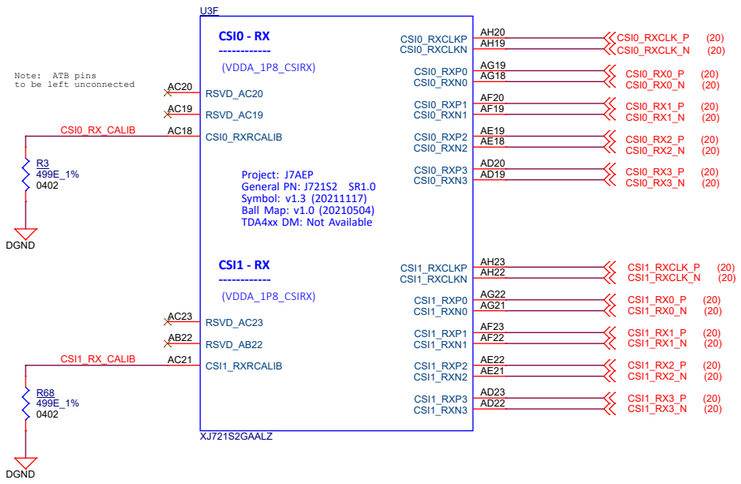
| J7x SoM - GPIO Mapping Table | | | | | | |
|---|---|---|---|---|---|---|
| **WKUP Domain** | | | | | | |
| **J7AEP Mapping** | | **Net name** | | | | |
| **Package Signal Name** | **GPIO Number** | | **Input/ Output** | **Default** | **State** | **Remarks** |
| MCU_OSPI0_CSn1 | WKUP_GPIO0_28 | EN_EFUSE_VPP | Output | PU | Active High | Enable pin for VPP_EFUSE supply |
| MCU_OSPI0_CSN2 | WKUP_GPIO0_29 | CPLD_TMS/USER_LED1 | Output | NA | NA | JTAG signals for CPLD & USER LED enable signal.<br>1:2 Mux on base board |
| MCU_OSPI1_CLK | WKUP_GPIO0_31 | CPLD_TCK/MCU_RGMII_INTz | Input | PD | NA | JTAG signals for CPLD & MCU_RGMII_INT signal.<br>1:2 Mux on base board |
| MCU_OSPI1_CSN0 | WKUP_GPIO0_38 | CSI_EXP_GPIO_4 | I/O | NA | NA | GPIO Signals for CSI expansion connector |
| MCU_OSPI1_CSN1 | WKUP_GPIO0_39 | PMIC_INTn_1V8 | Input | PU | Active low | Interrupt signal from PMIC |
| MCU_OSPI1_D0 | WKUP_GPIO0_34 | CPLD_TDI/ eDP_IRQ | Input | NA | NA | JTAG signals for CPLD & Interrupt signal from eDP bridge.<br>1:2 Mux on base board |
| MCU_OSPI1_D1 | WKUP_GPIO0_35 | CSI_EXP_GPIO_5 | I/O | NA | NA | GPIO Signals for CSI expansion connector |
| MCU_OSPI1_D2 | WKUP_GPIO0_36 | CSI_EXP_GPIO_2 | I/O | NA | NA | GPIO Signals for CSI expansion connector |
| MCU_OSPI1_D3 | WKUP_GPIO0_37 | CSI_EXP_GPIO_3 | I/O | NA | NA | GPIO Signals for CSI expansion connector |
| MCU_OSPI1_DQS | WKUP_GPIO0_33 | CPLD_TDO/ SOC_WAKE | Output | NA | NA | JTAG signals for CPLD |
| MCU_OSPI1_LBCLKO | WKUP_GPIO0_32 | CSI_EXP_GPIO_1 | I/O | NA | NA | GPIO Signals for CSI expansion connector |
| MCU_SPI0_CLK | WKUP_GPIO0_54 | WKUP_GPIO0_54 | Output | BOOTMODE | Active low | CPLD_JTAG/GPIOn_SEL.<br>Mux select signal for CPLD JTAG and GPIO's |
| MCU_SPI0_CS0 | WKUP_GPIO0_70 | WKUP_GPIO0_70 | I/O | BOOTMODE | NA | FPC Camera GPIO signals |
| MCU_SPI0_D1 | WKUP_GPIO0_69 | SYS_MCU_PWRDN | Output | BOOTMODE | Active High | System Power Down ('0' - normal operation,<br>'1' - system power down) |
| WKUP_GPIO0_10 | WKUP_GPIO0_10 | MCU_ADC_EXT_TRIGGER0/PCIE 1_M.2_CLKREQ# | | | | ADC external trigger from TI safety header(Default connection)/CLKREQ# |
| WKUP_GPIO0_11 | WKUP_GPIO0_11 | MCU_CLKOUT0 | Output | NA | NA | 25MHz reference clock for CSI expansion connector |
| WKUP_GPIO0_15 | WKUP_GPIO0_15 | MCU_SPI1_CS2 | Output | BOOTMODE | Active low | MCU SPI1 signals |
| WKUP_GPIO0_49 | WKUP_GPIO0_49 | WKUP_GPIO0_49 | I/O | NA | NA | GPIO signal for 40 pin expansion header |
| WKUP_GPIO0_57 | WKUP_GPIO0_57 | WKUP_GPIO0_57 | I/O | BOOTMODE | NA | GPIO signal for 40 pin expansion header |
| WKUP_GPIO0_56 | WKUP_GPIO0_56 | WKUP_GPIO0_56 | I/O | BOOTMODE | NA | GPIO signal for 40 pin expansion header |
| WKUP_GPIO0_66 | WKUP_GPIO0_66 | WKUP_GPIO0_66 | I/O | BOOTMODE | NA | GPIO signal for 40 pin expansion header |
| WKUP_GPIO0_67 | WKUP_GPIO0_67 | WKUP_GPIO0_67 | I/O | BOOTMODE | NA | GPIO signal for 40 pin expansion header |
| PMIC_POWER_EN1 | WKUP_GPIO0_88 | WKUP_GPIO0_88 | I/O | NA | NA | FPC Camera GPIO signals |
| MCU_ADC1_AIN0 | WKUP_GPIO0_79 | SOC_INT1z | Input | PU | Active low | Test automation INT signal |
| MCU_ADC1_AIN1 | WKUP_GPIO0_80 | SOC_INT2z | Input | PU | Active low | Test automation INT signal |
| | | | | | | |
| **Main Domain** | | | | | | |
| ECAP0_IN_APWM_OUT | GPIO0_49 | SEL_SDIO_3v3_1v8n | Output | PU | Active low | VDD_SD_DV 1.8V or 3.3V selection control |
| TIMER_IO0 | GPIO0_58 | MMC1_SDCD | Input | PU | Active low | SD card detect signal |
| TIMER_IO1 | GPIO0_59 | USB0_DRVVBUS | Output | NA | Active High | USB VBUS Drive signal |
| EXTINTN | GPIO0_0 | HDMI_HPD | Input | NA | Active High | HDMI hot plug detect signal |
| MCAN1_TX | GPIO0_27 | GPIO0_27 | I/O | NA | NA | GPIO signal for 40 pin expansion header |
| MCAN13_TX | GPIO0_3 | GPIO0_3 | I/O | NA | NA | GPIO signal for 40 pin expansion header |
| MCASP0_AXR8 | GPIO0_36 | GPIO0_36 | I/O | NA | NA | GPIO signal for 40 pin expansion header |
| MCASP0_AXR13 | GPIO0_41 | GPIO0_41/UART5_CTSn | I/O | NA | NA | GPIO signal for 40 pin expansion header/ UART5_CTS Signal |
| MCASP0_AXR14 | GPIO0_42 | GPIO0_42/UART5_RTSn | I/O | NA | NA | GPIO signal for 40 pin expansion header/ UART5_RTS Signal |
| **GPIO Expander on Base Board** | | | | | | |
| **Port NO** | | **I2C Instance** | **Input/Output** | **Default** | **State** | **Usage** |
| P00 | CSI_VIO_SEL | | Output | PD | Active High | Enable for VCC_CSI_IO supply generation load switch |
| P01 | CSI_SEL_FPC_EXPn | | Output | PD | Active High | CSI MUX selection |
| P02 | HDMI_PDn | | Output | PD | Active Low | Power down signal for HDMI Transmitter |
| P03 | HDMI_LS_OE | | Output | PU | Active High | HDMI current limit load switch enable |
| P04 | DP0_3V3_EN | | Output | PD | Active High | Enable signal for Display port load switch |
| P05 | BOARDID_EEPROM_WP | | Output | PD | Active High | Board id Eeeprom Write protect signal |
| P06 | CAN_STB | | Output | PD | Active High | Standby signals for MAIN & MCU domain<br>CAN Transceivers |
| P10 | GPIO_uSD_PWR_EN | | Output | PU | Active High | Micro SD card Load switch enable |
| P11 | eDP_ENABLE | | Output | PD | Active High | Used for Enable of DSI to eDP Bridge |
| P12 | IO_EXP_PCIe1_M.2_RTSz | | Output | NA | Active Low | PCIe Reset input to CPLD |
| P13 | IO_EXP_MCU_RGMII_RST# | | Output | NA | Active Low | MCU_RGMII reest input to CPLD |
| P14 | IO_EXP_CSI2_EXP_RSTz | | Output | PD | Active Low | CSI expansion connector reset |
| P16 | CSI0_B_GPIO1 | | Output | NA | NA | FPC Camera1 GPIO signal |
| P17 | CSI1_B_GPIO1 | **I2C0 ADDR: 0x21** | Output | NA | NA | FPC Camera2 GPIO signal |

| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SoC GPIO MAPPING TABLE<br>Size: C — PROC131 001 AM68 SK — Rev: E1<br>Date: Tuesday, October 04, 2022 — Sheet 7 of 21 |

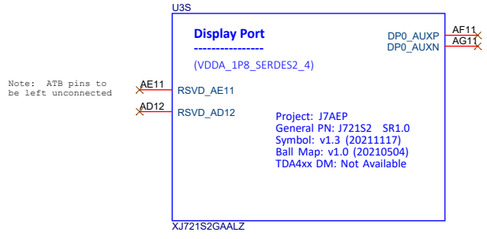
# DSI Interface



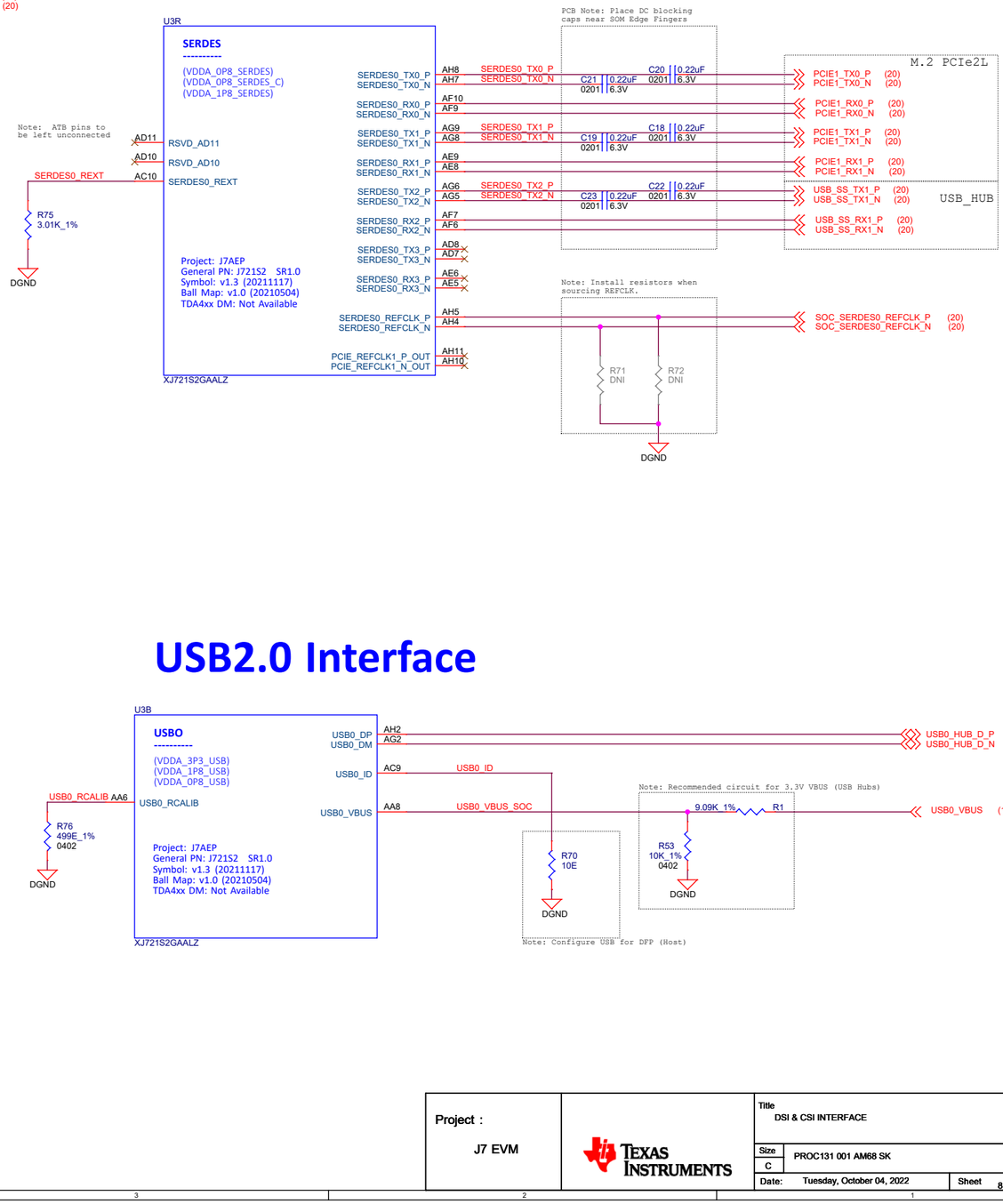

# CSI Interface




# DP Aux




# SERDES Interface (PCIE/USB)




# USB2.0 Interface




| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: DSI & CSI INTERFACE |
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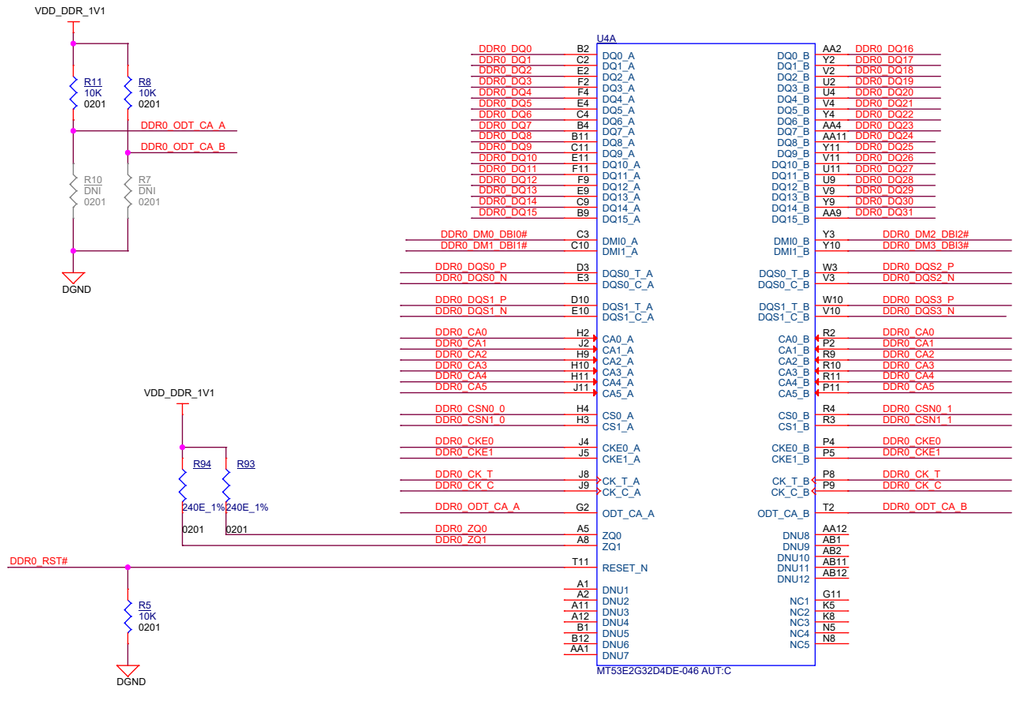
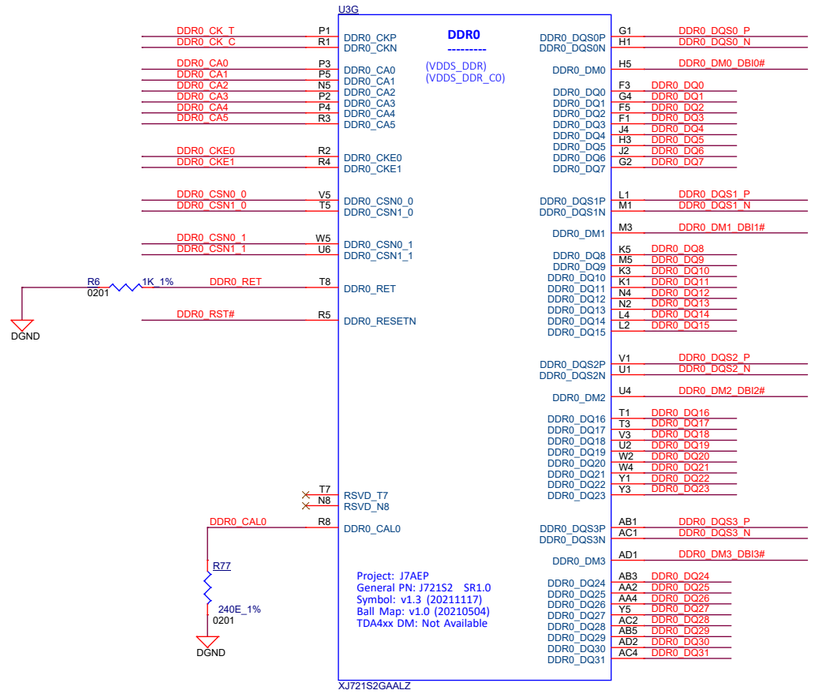
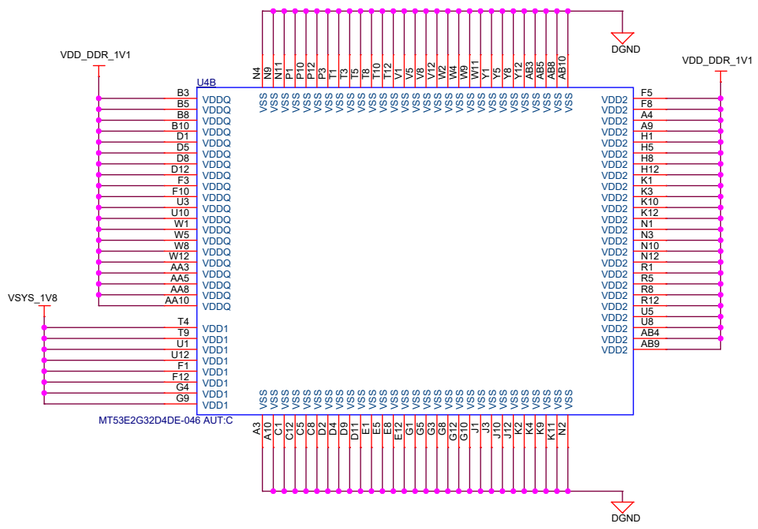
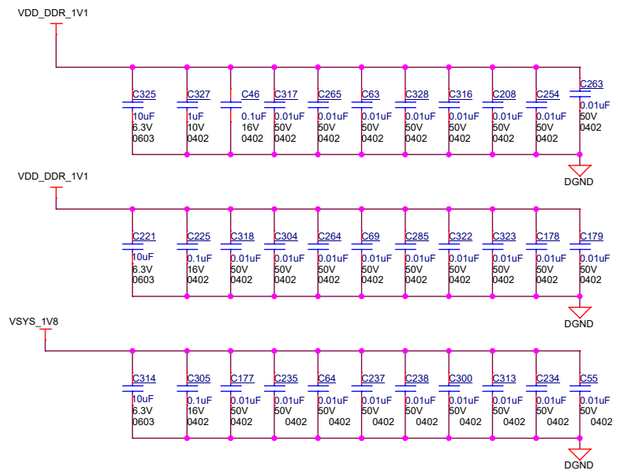
# LPDDR4 Inteface (Bank 0)




| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: LPDDDR4 INTERFACE - 1 |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
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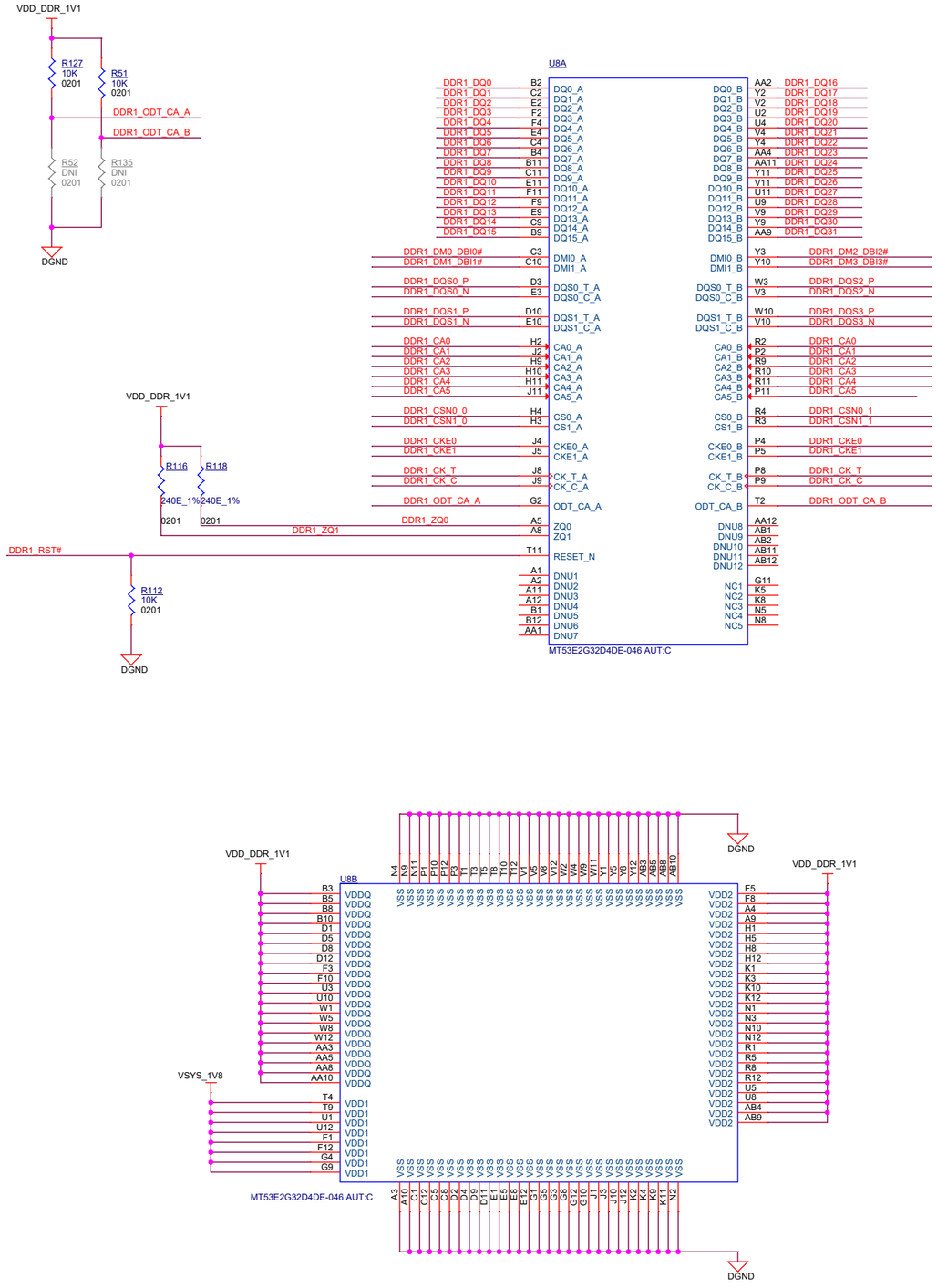
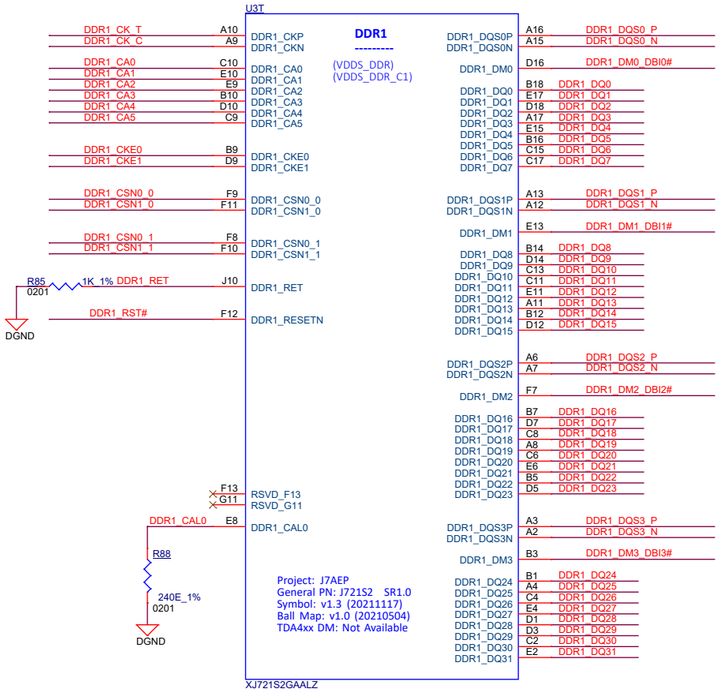
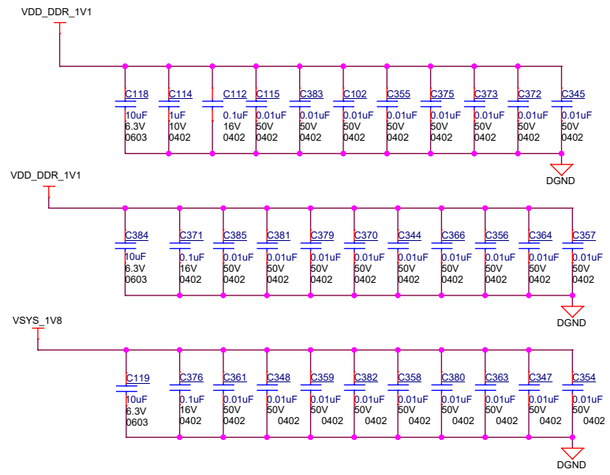
# LPDDR4 Interface (Bank 1)







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| Project : J7 EVM | TEXAS INSTRUMENTS | Title: LPDDR4 INTERFACE - 2 | |
| | | Size: C — PROC131 001 AM68 SK | Rev: E1 |
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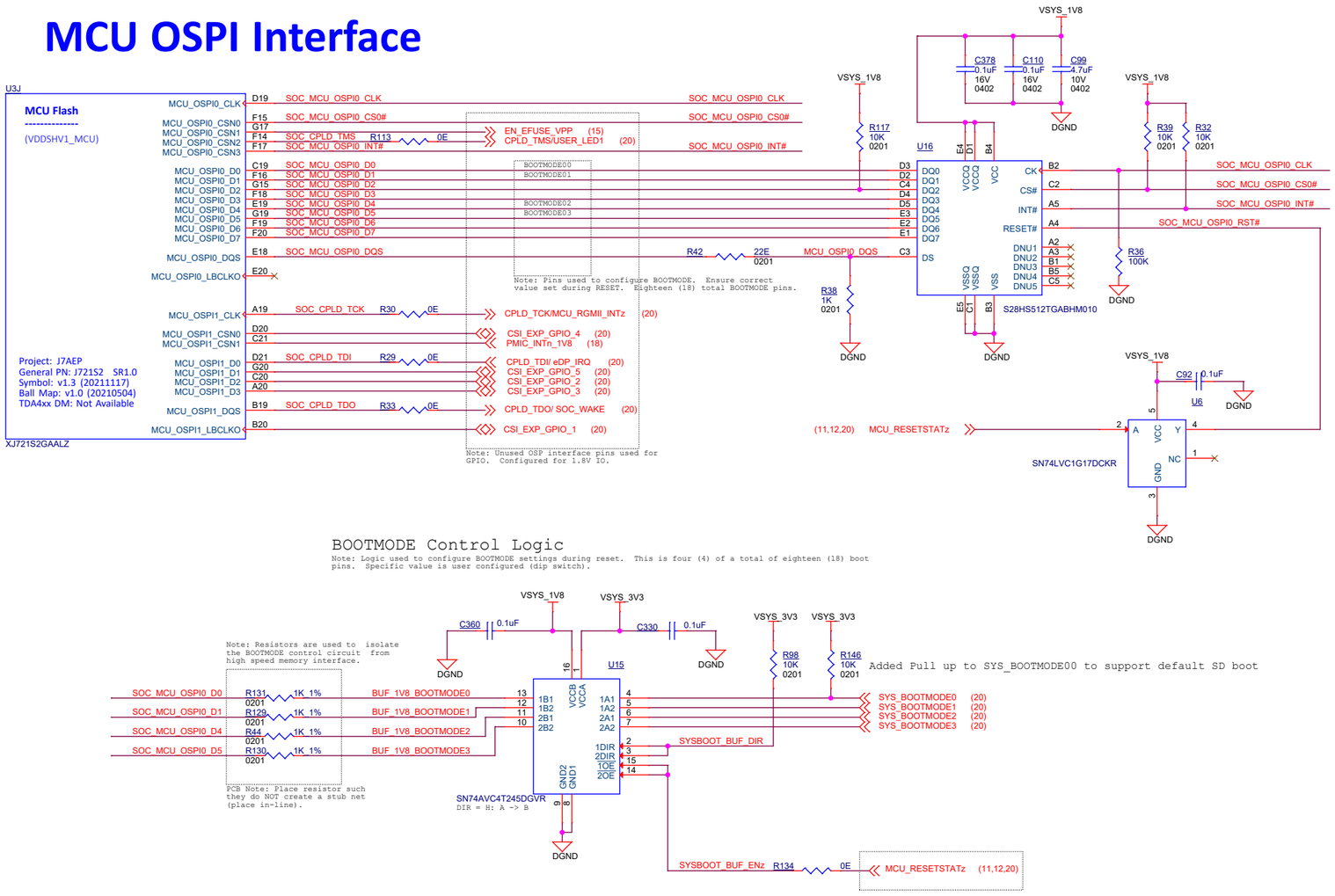
# MCU OSPI Interface

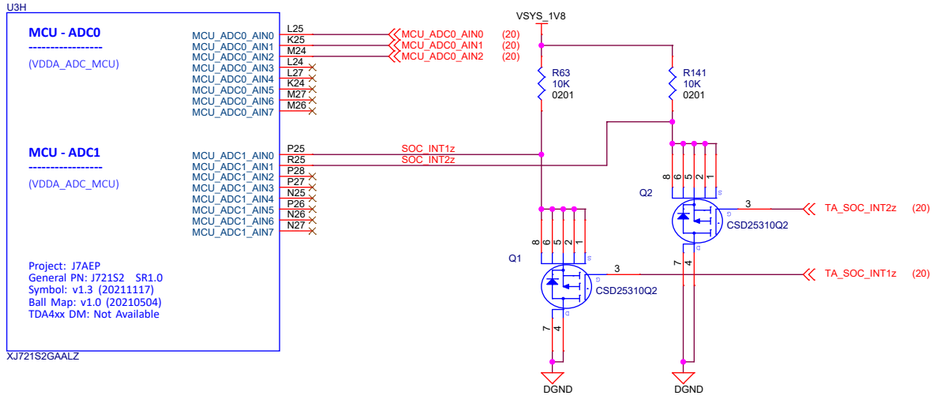



## BOOTMODE Control Logic

Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).




# MCU ADCs

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|---|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: MCU FLASH IF | |
| | | Size: C | PROC131 001 AM68 SK — Rev: E1 |
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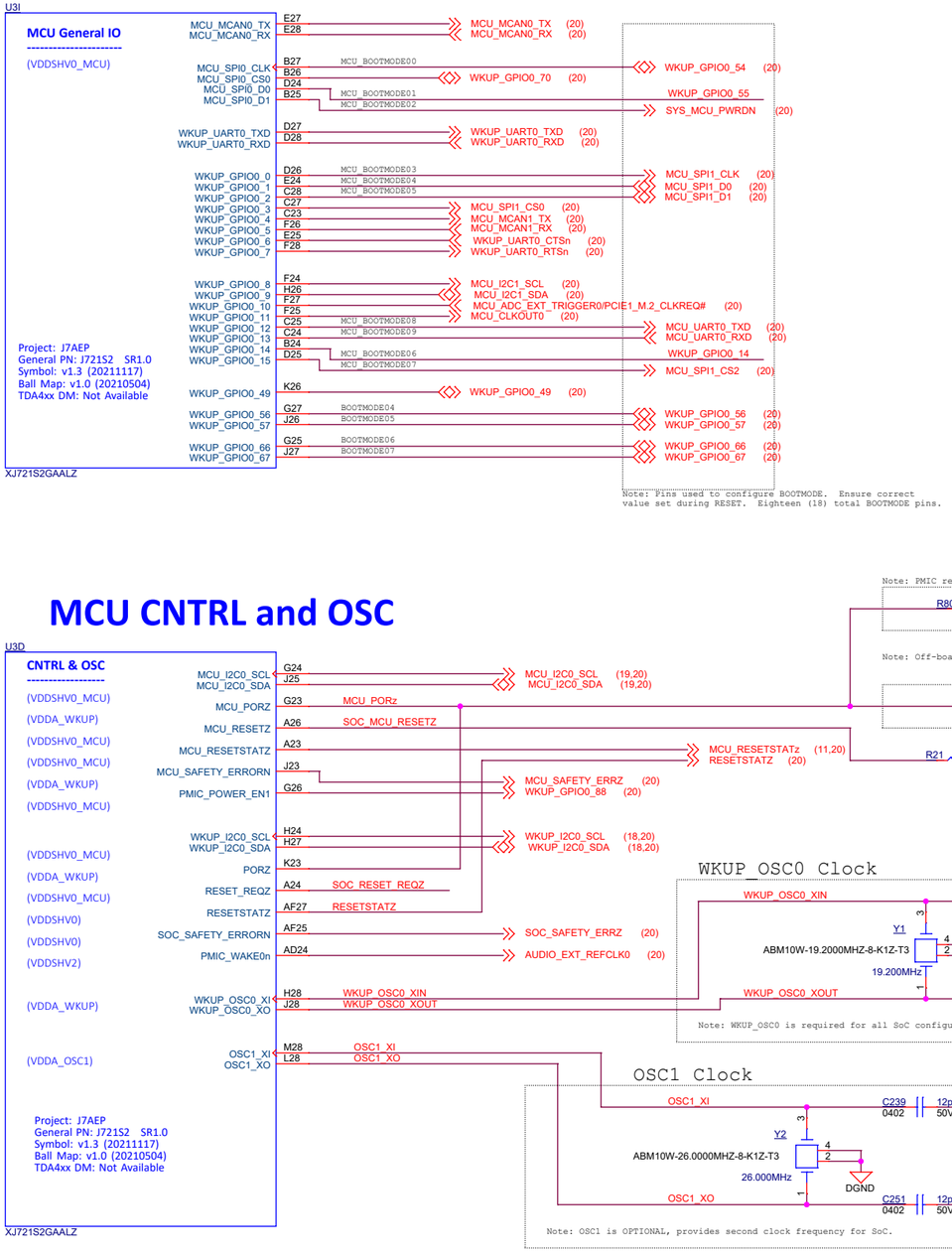
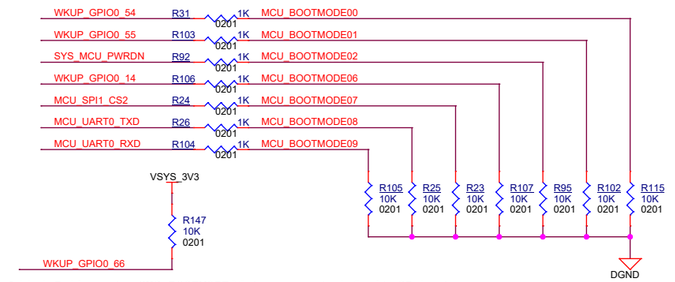
# MCU GENERAL IO




## BOOTMODE Control Logic

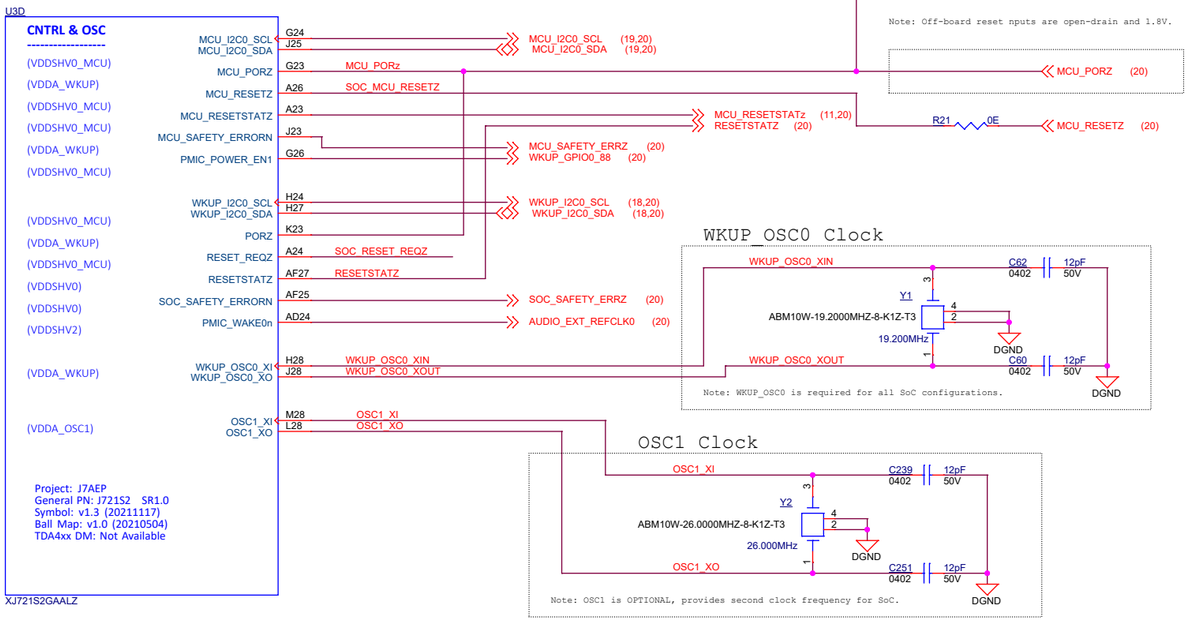
Note: Logic used to configure BOOTMODE settings during reset. This is seven(7) of a total of eighteen (18) boot pins. These settings configure for:

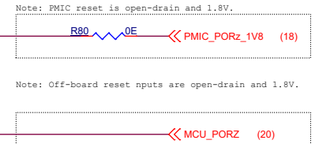
MCU_BOOTMODE[2:0] set '000' for WKUP_OSC0 of 19.2MHz
MCU_BOOTMODE[6] set '0' for Normal Boot
MCU_BOOTMODE[7] set '0' for Reserved
MCU_BOOTMODE[9:8] set '00' for LBIST + PBIST




Added Pull up to SYS_BOOTMODE06 to support default SD boot

# MCU CNTRL and OSC



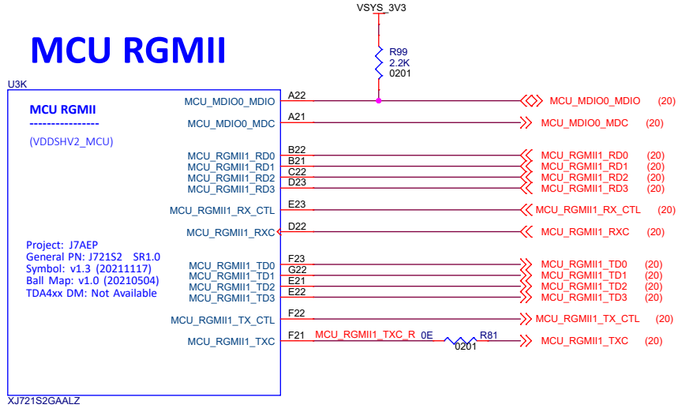

## WKUP_OSC0 Clock



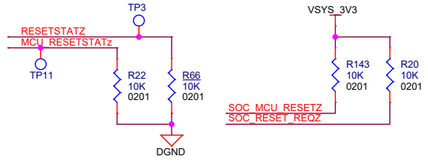

## OSC1 Clock



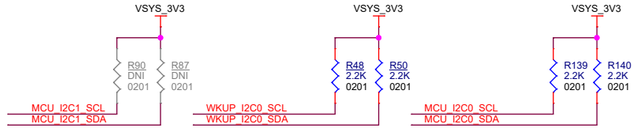

# MCU RGMII




## RESET Pull Resistors

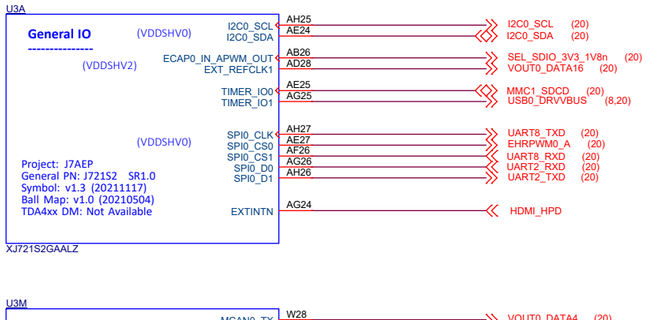


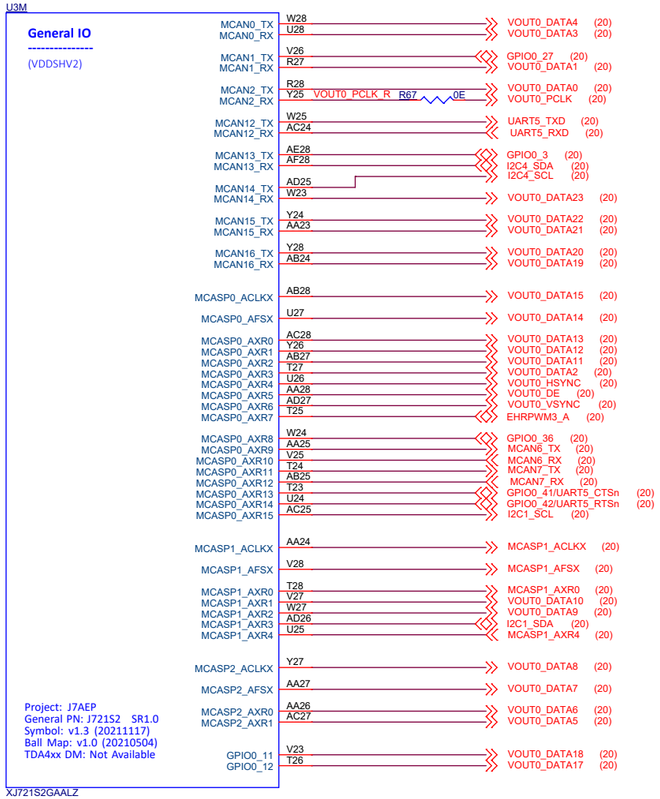

## MCU I2C Pull-Ups



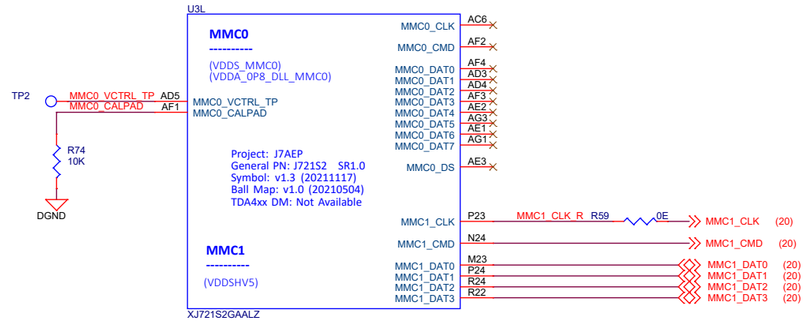

| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SOC_GENERAL&MCU_GENERAL |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 — Sheet 12 of 21 |

# GENERAL IO

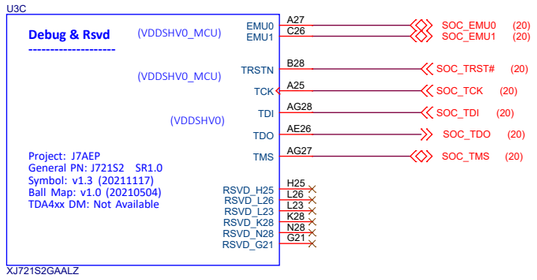


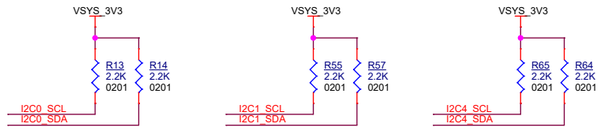

# MMC Interface




# DEBUG




## I2C Pull-Ups




Project : J7 EVM

TEXAS INSTRUMENTS

Title: SOC_GENERAL&MCU_GENERAL

| Size | PROC131 001 AM68 SK | Rev |
|---|---|---|
| C | | E1 |
| Date: Tuesday, October 04, 2022 | Sheet 13 of 21 | |

# ANALOG POWER 1

**Analog Power**

VDA_DLL_0V8

C326 10uF

PLL/DLL Filtering Scheme:
- No ferrite due to low noise LDO pwr source
-1x 1.0uF, SoC perimeter/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C192 0.1uF 6.3V 0201
C293 0.1uF 6.3V 0201
C332 10uF
C240 0.1uF 6.3V 0201

(VDD_PHYCORE_0V8)
VDD_CORE_0V8

FL3 120E — BLM18KG121TH1D
C15 4.7uF 16V 0805
C31 1uF 10V 0402

CSI/DSI PHY Filtering Scheme:
-1x Ferrite bead, common CORE buck
-1x 4.7uF & 1.0uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C163 0.1uF 6.3V 0201
C162 0.1uF 6.3V 0201

FL11 120E — BLM18KG121TH1D
C136 4.7uF 16V 0805
C14 1uF 10V 0402
C160 0.1uF 6.3V 0201
C161 0.1uF 6.3V 0201

FL1 120E — BLM18KG121TH1D
C7 22uF 6.3V 0805
C12 1uF 10V 0402

SERDES PHY Filtering Scheme:
-1x Ferrite bead, common CORE buck
-1x 22uF & 1.0uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C157 0.1uF 6.3V 0201
C164 0.1uF 6.3V 0201

FL8 120E — BLM18KG121TH1D
C129 22uF 6.3V 0805
C134 1uF 10V 0402
C170 0.1uF 6.3V 0201
C175 0.1uF 6.3V 0201

FL12 120E — BLM18KG121TH1D
C153 4.7uF 16V 0805
C150 1uF 10V 0402

USB2.0 PHY Filtering Scheme:
-1x Ferrite bead, common CORE buck
-1x 4.7uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C158 0.1uF 6.3V 0201

(VDD_PHY_1V8)
VDDA_1V8

FL4 120E — BLM18KG121TH1D
C132 4.7uF 16V 0805
C9 1uF 10V 0402

CSI/DSI PHY Filtering Scheme:
-1x Ferrite bead, common buck pwr
-1x 4.7uF & 1.0uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C173 0.1uF 6.3V 0201
C172 0.1uF 6.3V 0201

FL2 120E — BLM18KG121TH1D
C13 4.7uF 16V 0805
C32 1uF 10V 0402
C169 0.1uF 6.3V 0201
C168 0.1uF 6.3V 0201

FL10 120E — BLM18KG121TH1D
C135 22uF 6.3V 0805
C142 1uF 10V 0402

SERDES PHY Filtering Scheme:
-1x Ferrite bead, common buck pwr
-1x 22uF & 1.0uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C159 0.1uF 6.3V 0201
C171 0.1uF 6.3V 0201

FL9 120E — BLM18KG121TH1D
C130 4.7uF 16V 0805
C133 1uF 10V 0402

USB2.0 PHY Filtering Scheme:
-1x Ferrite bead, common buck pwr
-1x 4.7uF, bead/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C167 0.1uF 6.3V 0201

VSYS_IO_3V3

C29 1uF 10V 0402

PLL/DLL Filtering Scheme:
- No ferrite due to low noise LDO pwr source
-1x 1.0uF, SoC perimeter/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C165 0.1uF 6.3V 0201

U3N

| | | |
|---|---|---|
| VDA_DLL_0V8 | P10 | VDDA_0P8_PLL_DDR0 |
| VDA_DLL_0V8 | J14 | VDDA_0P8_PLL_DDR1 |
| | W7 | VDDA_0P8_DLL_MMC0 |
| VDDA_0P8_CSIRX | AB18 | VDDA_0P8_CSIRX0_1 |
| | AB17 | VDDA_0P8_CSIRX0_1 |
| VDDA_0P8_DSITX | AB14 | VDDA_0P8_DSITX |
| | AB15 | VDDA_0P8_DSITX_C |
| VDDA_0P8_SERDES | AB10 | VDDA_0P8_SERDES0_1 |
| VDDA_0P8_SERDES_C | AB11 | VDDA_0P8_SERDES0_1 |
| | AA10 | VDDA_0P8_SERDES_C0_1 |
| | AA11 | VDDA_0P8_SERDES_C0_1 |
| VDDA_0P8_USB | AB8 | VDDA_0P8_USB |
| VDDA_1P8_CSIRX | AA19 | VDDA_1P8_CSIRX0_1 |
| | AA17 | VDDA_1P8_CSIRX0_1 |
| VDDA_1P8_DSITX | AA14 | VDDA_1P8_DSITX |
| | AA15 | VDDA_1P8_DSITX |
| VDDA_1P8_SERDES | AA12 | VDDA_1P8_SERDES0_1 |
| | AB13 | VDDA_1P8_SERDES2_4 |
| VDDA_1P8_USB | AB7 | VDDA_1P8_USB |
| VDA_USB_3V3 | AB9 | VDDA_3P3_USB |

XJ721S2GAALZ

| | | |
|---|---|---|
| VDDA_MCU_PLLGRP0 | K22 | |
| VDDA_MCU_TEMP | J17 | |
| VDDA_ADC0 | J21 | |
| VDDA_ADC1 | K21 | |
| VDDA_WKUP | J22 | |
| VDDA_POR_WKUP | L20 | |
| VDDA_PLLGRP0 | U18 | |
| VDDA_PLLGRP1 | V19 | |
| VDDA_PLLGRP2 | Y11 | |
| VDDA_PLLGRP5 | N14 | |
| VDDA_PLLGRP6 | R12 | |
| VDDA_PLLGRP7 | R11 | |
| VDDA_PLLGRP8 | K12 | |
| VDDA_PLLGRP9 | T18 | |
| VDDA_PLLGRP10 | Y16 | |
| VDDA_PLLGRP12 | Y18 | |
| VDDA_PLLGRP13 | V12 | |
| VDDA_TEMP0 | U19 | |
| VDDA_TEMP1 | K10 | |
| VDDA_TEMP2 | T16 | |
| VDDA_TEMP3 | U10 | |
| VDDA_TEMP4 | Y14 | |
| VDDA_OSC1 | L21 | |

(VDA_MCU_1V8)
VDDA_1V8

C270 0.1uF 6.3V 0201
C276 0.1uF 6.3V 0201
C292 0.1uF 6.3V 0201
C286 0.1uF 6.3V 0201

PLL/DLL Filtering Scheme:
- No ferrite due to low noise LDO pwr source
-1x 1.0uF, SoC perimeter/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C74 1uF 10V 0402

VDDA_ADC_1V8

C287 0.1uF 6.3V 0201
C278 0.1uF 6.3V 0201

ADC 0 & 1 Filtering Scheme:
ADC Vref connected to VDD_ADCx supplies
-1x Ferrite bead to filter & reduce noise
-1x 1.0uF, SoC perimeter/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C71 1uF 10V 0402

FL5 120E — BLM18KG121TH1D

(VDA_PLL_1V8)
VDDA_1V8

C231 0.1uF 6.3V 0201
C184 0.1uF 6.3V 0201
C182 0.1uF 6.3V 0201
C187 0.1uF 6.3V 0201

PLL/DLL Filtering Scheme:
- No ferrite due to low noise LDO pwr source
-1x 1.0uF, SoC perimeter/near end
- 0.1uF per pwr ball, far end
(as area under SoC allows)

C321 1uF 10V 0402

C219 0.1uF 6.3V 0201
C216 0.1uF 6.3V 0201
C210 0.1uF 6.3V 0201
C183 0.1uF 6.3V 0201

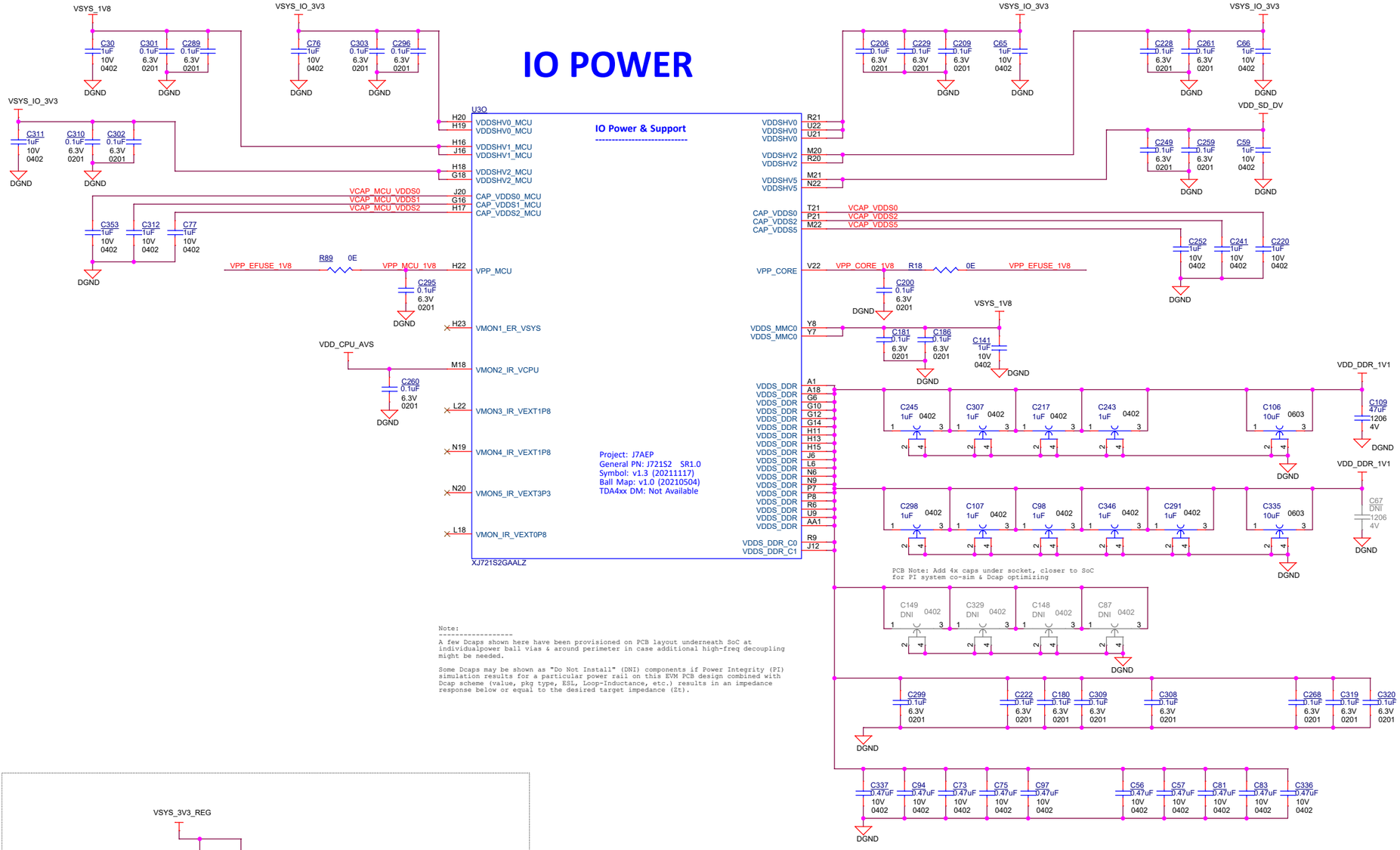
C248 0.1uF 6.3V 0201
C230 0.1uF 6.3V 0201
C282 0.1uF 6.3V 0201
C269 0.1uF 6.3V 0201
C211 0.1uF 6.3V 0201
C202 0.1uF 6.3V 0201

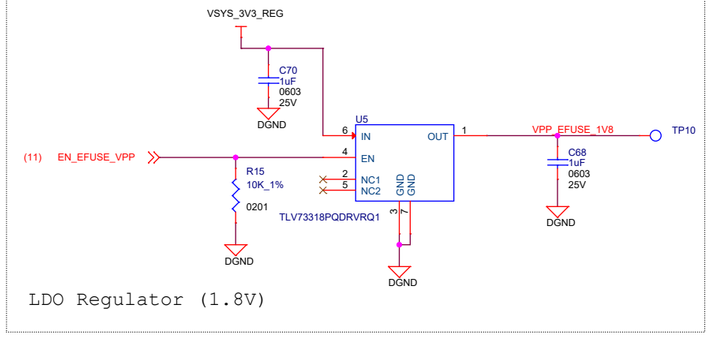
C273 0.1uF 6.3V 0201

Project: J7AEP
General PN: J721S2 SR1.0
Symbol: v1.3 (20211117)
Ball Map: v1.0 (20210504)
TDA4xx DM: Not Available

| | | | |
|---|---|---|---|
| Project : J7 EVM | | Title: SOC ANALOG POWER 1 | |
| | | Size: C | PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 | Sheet 14 of 21 |

# IO POWER




| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SOC DIGITAL IO & SUPPORT POWER 2 |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 — Sheet 15 of 21 |

# DIGITAL POWER

**Digital Power**

U3P

VDD_MCU_0V85 → K16, K18, L15, L17, L19 (VDD_MCU)

VDD_MCU_0V85 → J19 (VDD_MCU_WAKE1); C290 0.1uF 6.3V 0201 → DGND

K17, K19 (VDDAR_MCU) ← VDDAR_MCU_0V85

VDD_CORE_0V8 → J13, J15, M16, M19, N10, R17, R19, T10, T20, U8, U15, U17, P18, V7, V9, V14, V18, V20, W8, W10, W13, W15, W17, W19, W21, Y9, Y12, Y22, AA21, AB20 (VDD_CORE)

C53 22uF 1206 10V; C233 22uF 1206 10V; C232 22uF 1206 10V; C54 22uF 1206 10V

C198 10uF 0603; C49 10uF 0603; C48 10uF 0603; C199 10uF 0603; C215 10uF 0603; C52 10uF 0603; C214 10uF 0603; C51 10uF 0603 → DGND

PCB Note: Add 4x caps under socket, closer to SoC for PI system co-sim & Dcap optimizing

C201 1uF 0402; C193 1uF 0402; C203 1uF 0402; C166 1uF 0402; C190 1uF 0402; C188 1uF 0402; C227 1uF 0402; C196 1uF 0402; C191 1uF 0402; C189 1uF 0402; C47 DNI 0402; C50 DNI 0402; C213 DNI 0402; C197 DNI 0402 → DGND

C224 0.1uF 6.3V 0201; C218 0.1uF 6.3V 0201; C194 0.1uF 6.3V 0201; C288 0.1uF 6.3V 0201; C284 0.1uF 6.3V 0201; C253 0.1uF 6.3V 0201; C242 0.1uF 6.3V 0201; C174 0.47uF 10V 0402; C45 0.47uF 10V 0402; C176 0.47uF 10V 0402; C44 0.47uF 10V 0402 → DGND

VDD_CORE_0V8 → C246 0.1uF 6.3V 0201 → DGND

C257 0.1uF 6.3V 0201; C250 0.1uF 6.3V 0201; C207 0.1uF 6.3V 0201 → DGND

VDD_WAKE0 ← P20

VDDAR_CORE_0V85 ← N17, V11, V16, Y20 (VDDAR_CORE)

C247 0.1uF 6.3V 0201; C195 0.1uF 6.3V 0201; C185 0.1uF 6.3V 0201 → DGND

C90 4.7uF 16V 0805 → DGND

(VDD_RAM_0V85) VDD_MCU_0V85 ← 120E FL7 BLM18KG121TH1D

VDDAR_CPU_0V85 ← H9, K14, P11, P14, V13 (VDDAR_CPU)

C294 0.1uF 6.3V 0201; C275 0.1uF 6.3V 0201; C204 0.1uF 6.3V 0201 → DGND

C349 4.7uF 16V 0805 → DGND

120E FL13 BLM18KG121TH1D

VDD_CPU_AVS ← G8, H7, J8, K7, K9, K11, K13, L8, M7, M9, M14, N11, N15, P16, R13, R15, T12, T14, U11, U13 (VDD_CPU)

C6 22uF 10V 1206; C5 22uF 10V 1206; C127 22uF 10V 1206; C128 22uF 10V 1206

C140 10uF 0603; C28 10uF 0603; C27 10uF 0603; C139 10uF 0603; C26 10uF 0603; C138 10uF 0603; C267 10uF 0603; C33 10uF 0603; C144 10uF 0603; C236 10uF 0603 → DGND

PCB Note: Add 4x caps under socket, closer to SoC for PI system co-sim & Dcap optimizing

C212 1uF 0402; C223 1uF 0402; C283 1uF 0402; C272 1uF 0402; C306 1uF 0402; C244 1uF 0402; C256 1uF 0402; C151 DNI 0402; C37 DNI 0402; C34 DNI 0402; C146 DNI 0402 → DGND

C205 0.1uF 6.3V 0201; C226 0.1uF 6.3V 0201; C40 100uF 6.3V 1210; C154 100uF 6.3V 1210 → DGND

Project: J7AEP
General PN: J721S2 SR1.0
Symbol: v1.3 (20211117)
Ball Map: v1.0 (20210504)
TDA4xx DM: Not Available

XJ721S2GAALZ

Note:
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

VDD_MCU_0V85

PCB Note: Add 2x caps under socket, closer to SoC for PI system co-sim & Dcap optimizing

C334 10uF 0603; C271 1uF 0402; C333 1uF 0402; C78 DNI 0402; C338 DNI 0402 → DGND

C280 0.1uF 6.3V 0201; C262 0.1uF 6.3V 0201; C266 0.1uF 6.3V 0201 → DGND

C340 0.47uF 10V 0402; C339 0.47uF 10V 0402; C79 0.47uF 10V 0402; C80 0.47uF 10V 0402

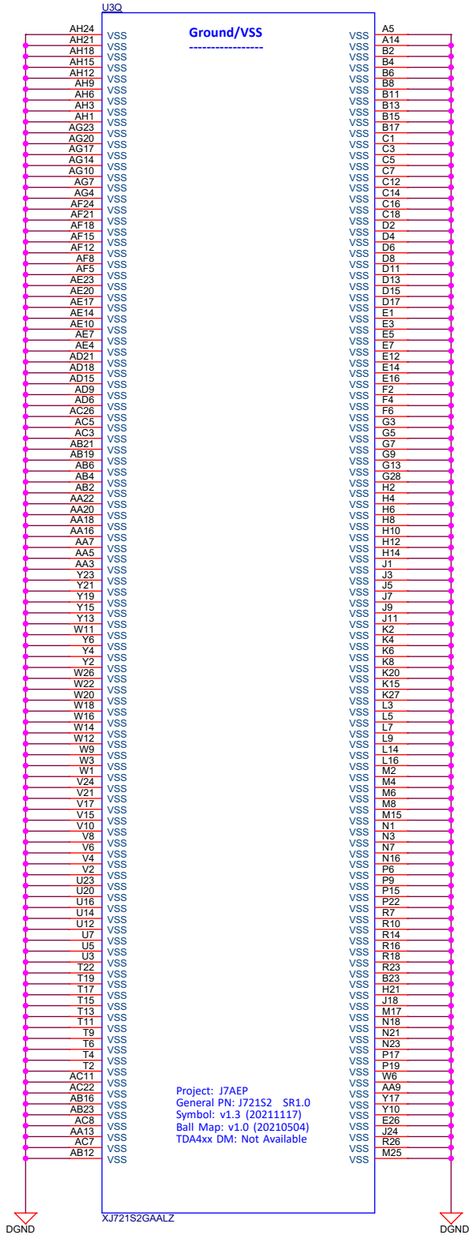
(VDD_MCU_RAM_0V85) VDD_MCU_0V85 ← FL6 120E BLM18KG121TH1D → VDDAR_MCU_0V85

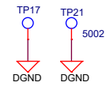
C84 4.7uF 16V 0805 → DGND

C274 0.1uF 6.3V 0201; C281 0.1uF 6.3V 0201 → DGND

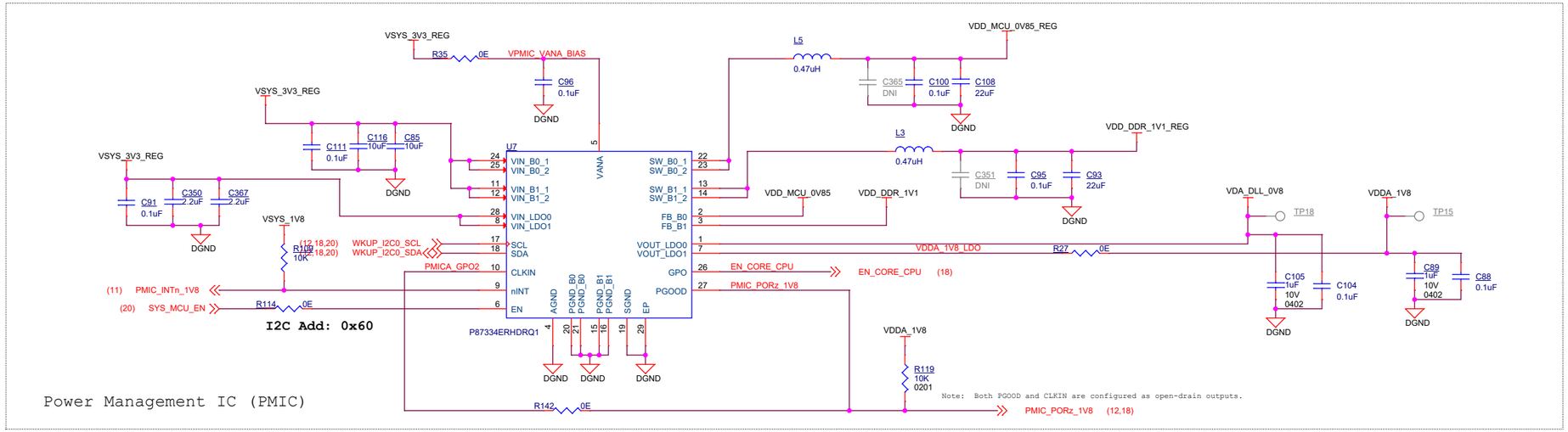
| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SOC DIGITAL POWER 3 |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 — Sheet 16 of 21 |

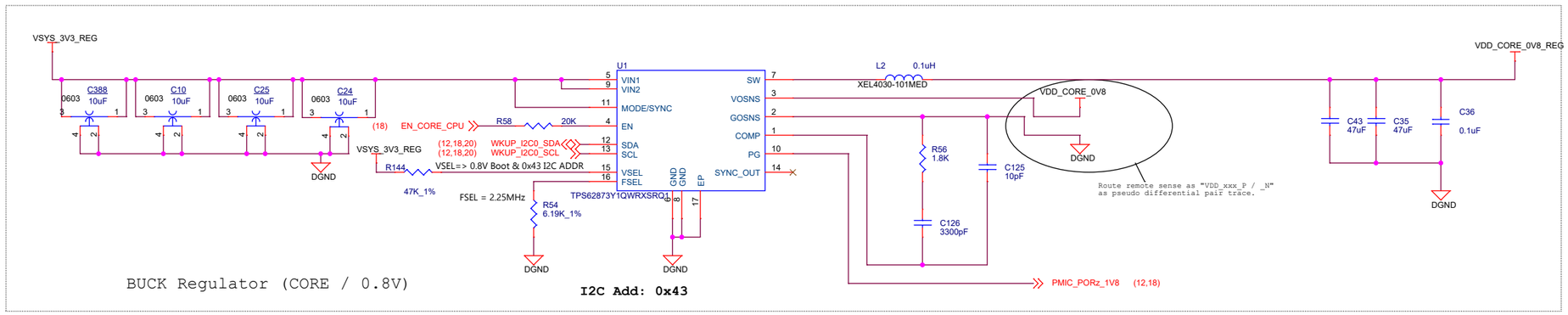
# SOC GROUND

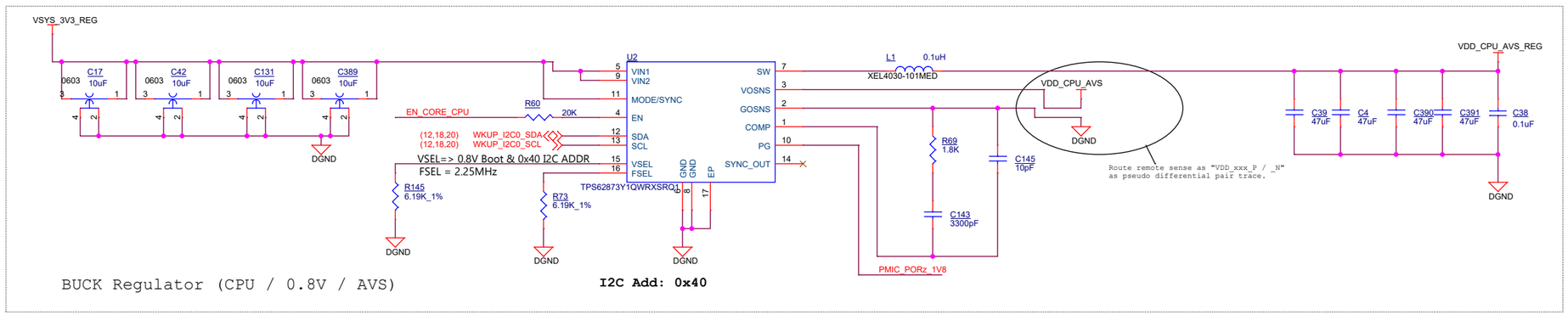


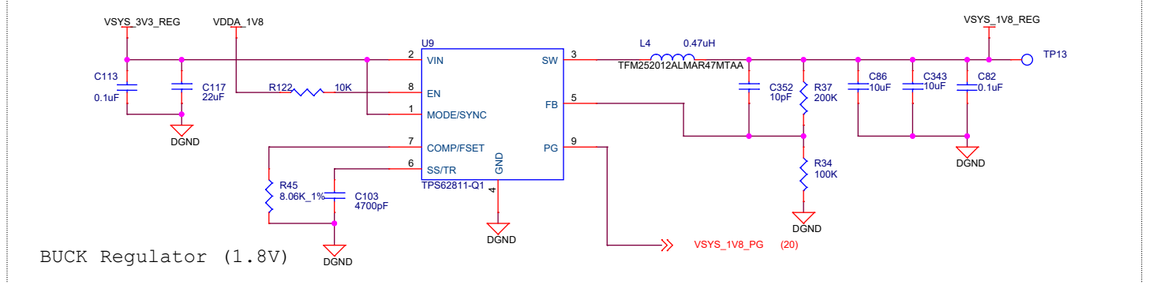




| | | | |
|---|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SOC GROUND | |
| | | Size: C | PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 | Sheet 17 of 21 |



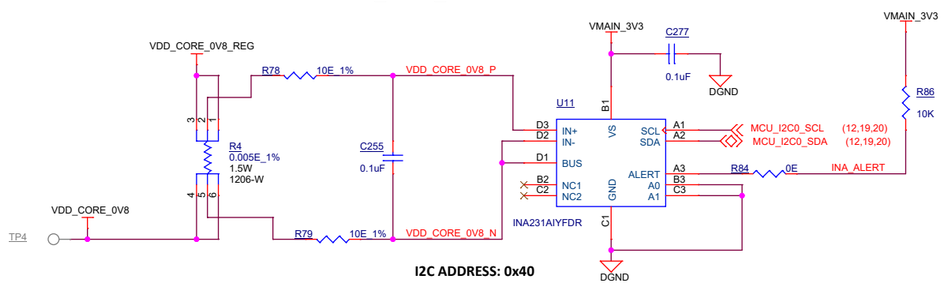




# POWER SUPPLY

| | | | |
|---|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: PMIC and Power Supply | |
| | | Size: C | PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 | Sheet 18 of 21 |

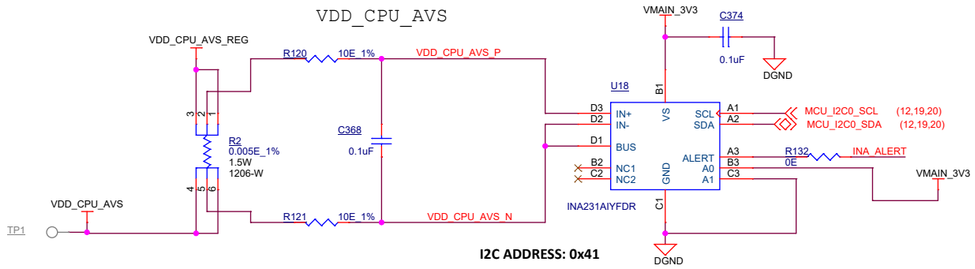
# CURRENT MONITOR

## VDD_CORE_0V8



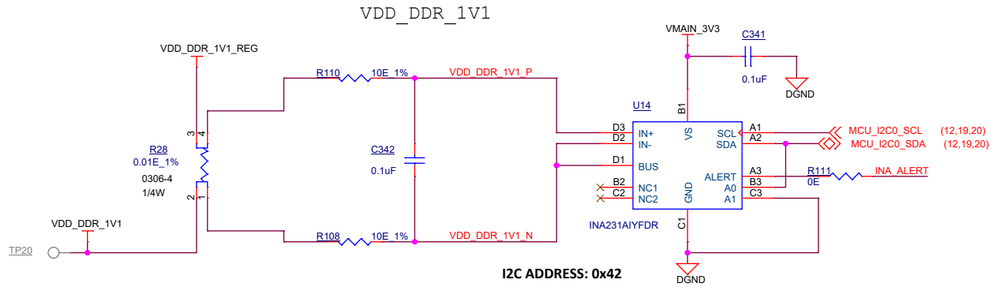

**I2C ADDRESS: 0x40**

## VDD_CPU_AVS



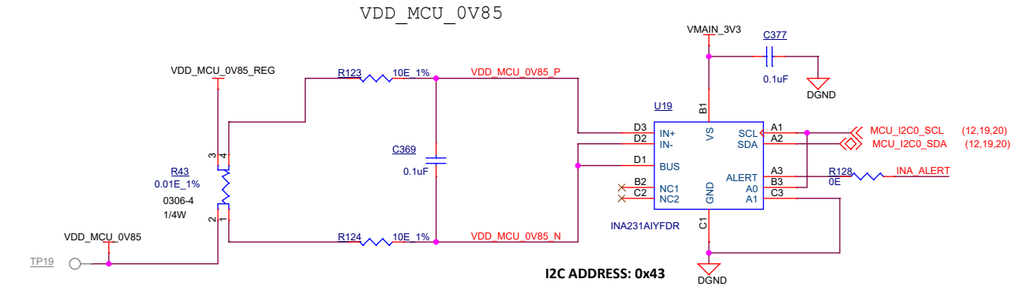

**I2C ADDRESS: 0x41**

## VDD_DDR_1V1



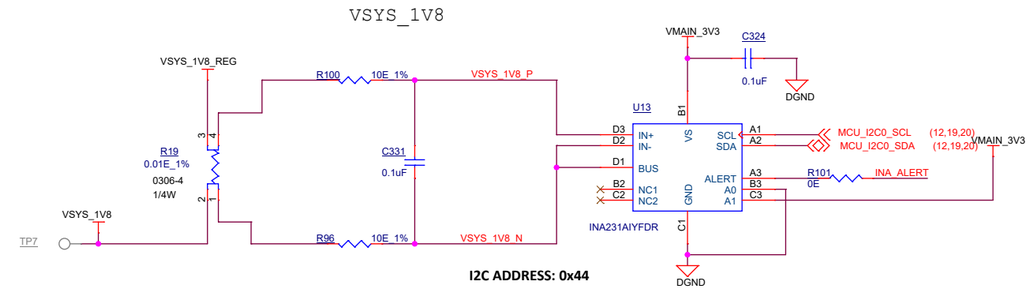

**I2C ADDRESS: 0x42**

## VDD_MCU_0V85



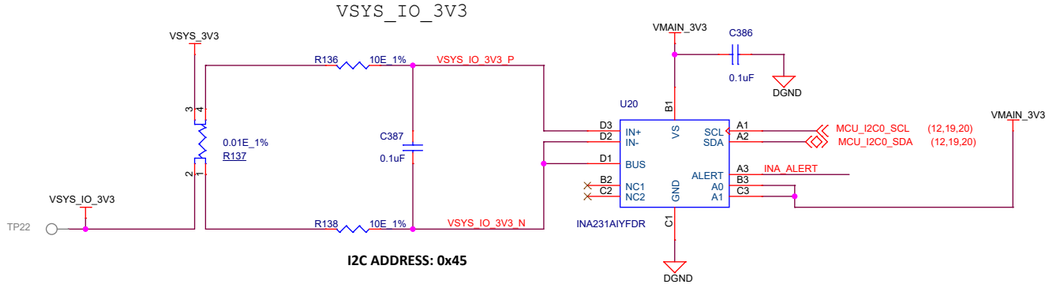

**I2C ADDRESS: 0x43**

## VSYS_1V8




**I2C ADDRESS: 0x44**

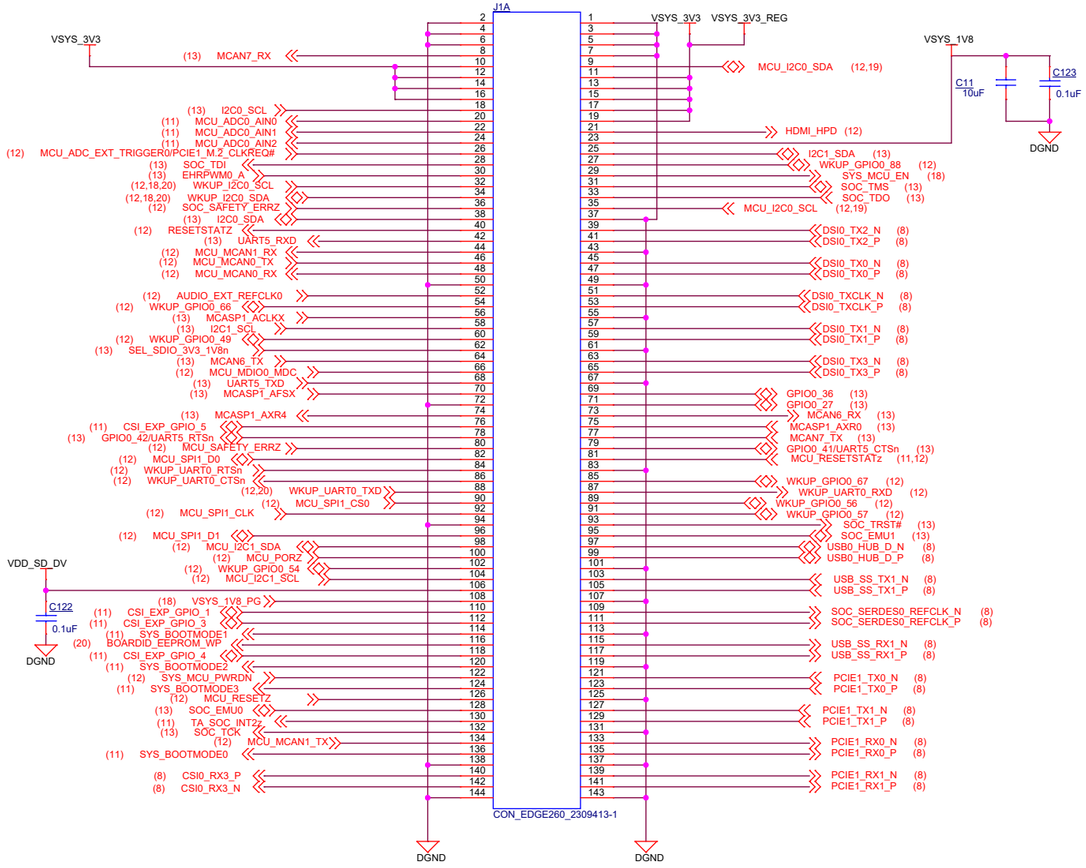
## VSYS_IO_3V3

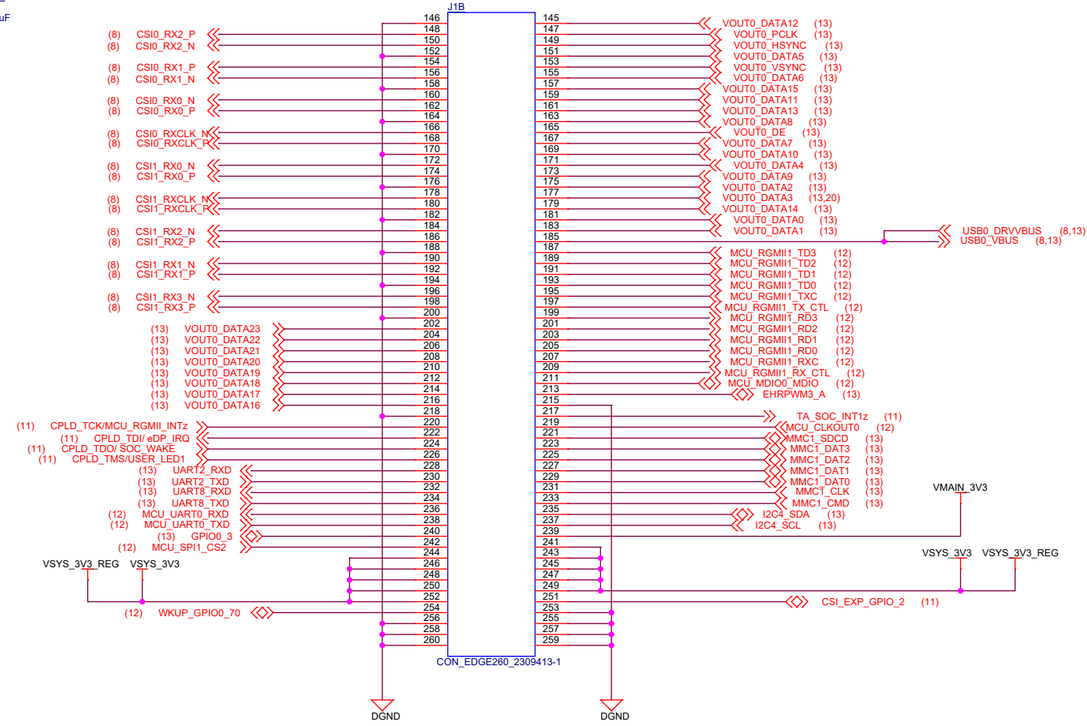


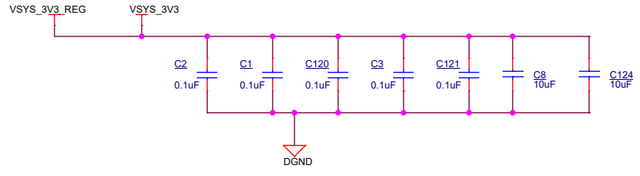

**I2C ADDRESS: 0x45**

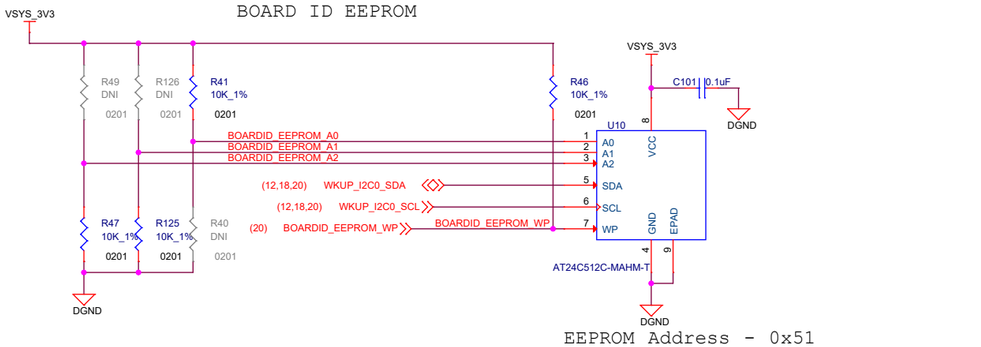
| | | |
|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: Current sense |
| | | Size: C — PROC131 001 AM68 SK — Rev: E1 |
| | | Date: Tuesday, October 04, 2022 — Sheet 19 of 21 |

# 260 PIN SODIMM CONNECTOR




| | | | |
|---|---|---|---|
| Project : J7 EVM | TEXAS INSTRUMENTS | Title: SODIMM 260 PIN EDGE FINGERS | |
| | | Size: C — PROC131 001 AM68 SK | Rev: E1 |
| | | Date: Tuesday, October 04, 2022 | Sheet 20 of 21 |

# NOTES, HW & LABELS

## ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

## FIDUCIALS

FID1 FID_40X80 | FID2 FID_40X80 | FID3 FID_40X80

FID4 FID_40X80 | FID5 FID_40X80 | FID6 FID_40X80

## BARE PCB

PCB1

PROC131E1

## LABELS

### Board Serial No.

LBL1

PCB LABEL

AM6-COMPROCEVM

### Assembly Revision.

LBL2

PCB LABEL

AM6-COMPROCEVM

**OPN: SK - AM68**

## LOGOs

PCB LOGO Texas Intruments — Texas Intruments

PCB LOGO For Evaluation only; not FCC approved for resale — For Evaluation only; not FCC approved for resale

PCB LOGO WEEE Mark — WEEE Mark

PCB LOGO CE Mark — CE Mark

PCB LOGO High Temperature — High Temperature

## STANDOFF,SCREW & WASHER FOR SOM

MH1 — MHOLE_PAN HEAD_M2_NPTH

MH2 — MHOLE_PAN HEAD_M2_NPTH

## HEATSINK AS ACCESSORIES

ACC1

374424B00035G

| | | |
|---|---|---|
| Project : J7 EVM | Title: Hardware Schematic | |
| | Size: C — PROC131 001 AM68 SK | Rev: E1 |
| | Date: Tuesday, October 04, 2022 | Sheet 21 of 21 |