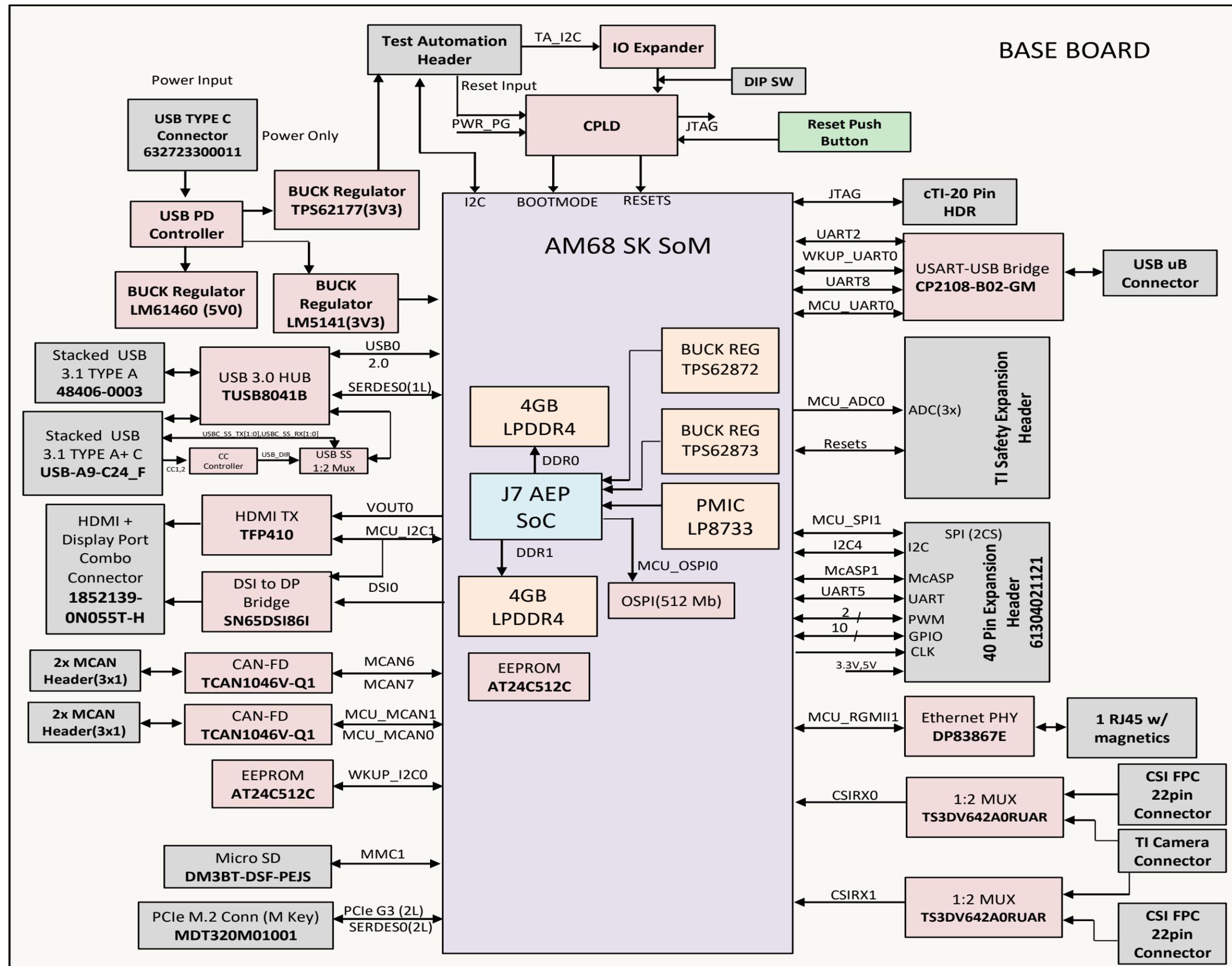


REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E1	12-OCT-2021	Initial Draft	Mistral Design Team		
	03-NOV-2021	Updated for GPIO Assignment given by TI	Mistral Design Team		
	09-NOV-2021	Updated for Power pins and rearranged signal pins in sodimm connector Changed C1163 to 100uF and removed C1162	Mistral Design Team		
	11-NOV-2021	Updated variant list and added GND test points	Mistral Design Team		
	16-NOV-2021	Updated to latest PDN v0.4	Mistral Design Team		
	18-NOV-2021	Swapped CSI signals on DIMM connector for routing ease Updated GPIO mapping table	Mistral Design Team		
	24-NOV-2021	Moved VSYS_IO_3V3 INA to Base board Changed Board ID EEPROM to AT24C512C-MAHM-T device Swapped SODIMM connectors for routing ease	Mistral Design Team		
	29-NOV-2021	Added Mounting hole	Mistral Design Team		
	1-DEC-2021	Updated Tripad capacitors footprint Updated VSYS_IO_3V3 supply connection	Mistral Design Team		
	1-DEC-2021	Changed U12 to TXS0102 Changed R119 to 10K	Mistral Design Team		
	5-AUG-2022	Changed U12 to TXS0102	Mistral Design Team		
	10-AUG-2022	Updated SoC symbol	Mistral Design Team		
	17-AUG-2022	DNI'd capacitors C67,C365, C351 Changed pin assignment for VDD_SD_DV	Mistral Design Team		
	19-AUG-2022	Removed TP16	Mistral Design Team		
	24-AUG-2022	Updated PMIC part number	Mistral Design Team		
	29-AUG-2022	Updated block diagrams Updated DDR part number to MT53E2G32D4DE-046 AUT:C	Mistral Design Team		
	29-AUG-2022	Updated for TI review comments	Mistral Design Team		
	12-SEP-2022	Updated murata capacitors part numbers	Mistral Design Team		
	04-OCT-2022	Updated Title block and board name	Mistral Design Team		
	E1A	16-JAN-2023	Updated schematic revision to E1A for HS SOC build Updated SOC symbol to XJ721S25AALZ Changed resistor R119 to 1K (Pull up resistor for PORz)	Mistral Design Team	
E2	19-JAN-2023	Updated schematic revision to E2 Updated FL7 & FL13 to BLM21SP111BH1D Changed C53, C54, C232, C33 to 47uF Changed C45, C174 to GCM32ED70G107MEC4 and deleted caps C44 & C176	Mistral Design Team		
	31-JAN-2023	Changed 0.01uF cap from C0402C103K5RACTU to GCM155R71H103KA55D	Mistral Design Team		
	06-FEB-2023	Added fan assembly components and assembled Baseboard as accessories	Mistral Design Team		
	27-MAR-2023	Changed C5, C6, 127 & 128 to 47uF - GCM31CD70G476ME02 Removed C39, C390 & C391	Mistral Design Team		

Project : J7 EVM				Title REVISION HISTORY	
Size C	PROC131 001 AM68 SK			Rev E2	
Date: Monday, March 27, 2023	Sheet 2 of 21				

SYSTEM BLOCK DIAGRAM



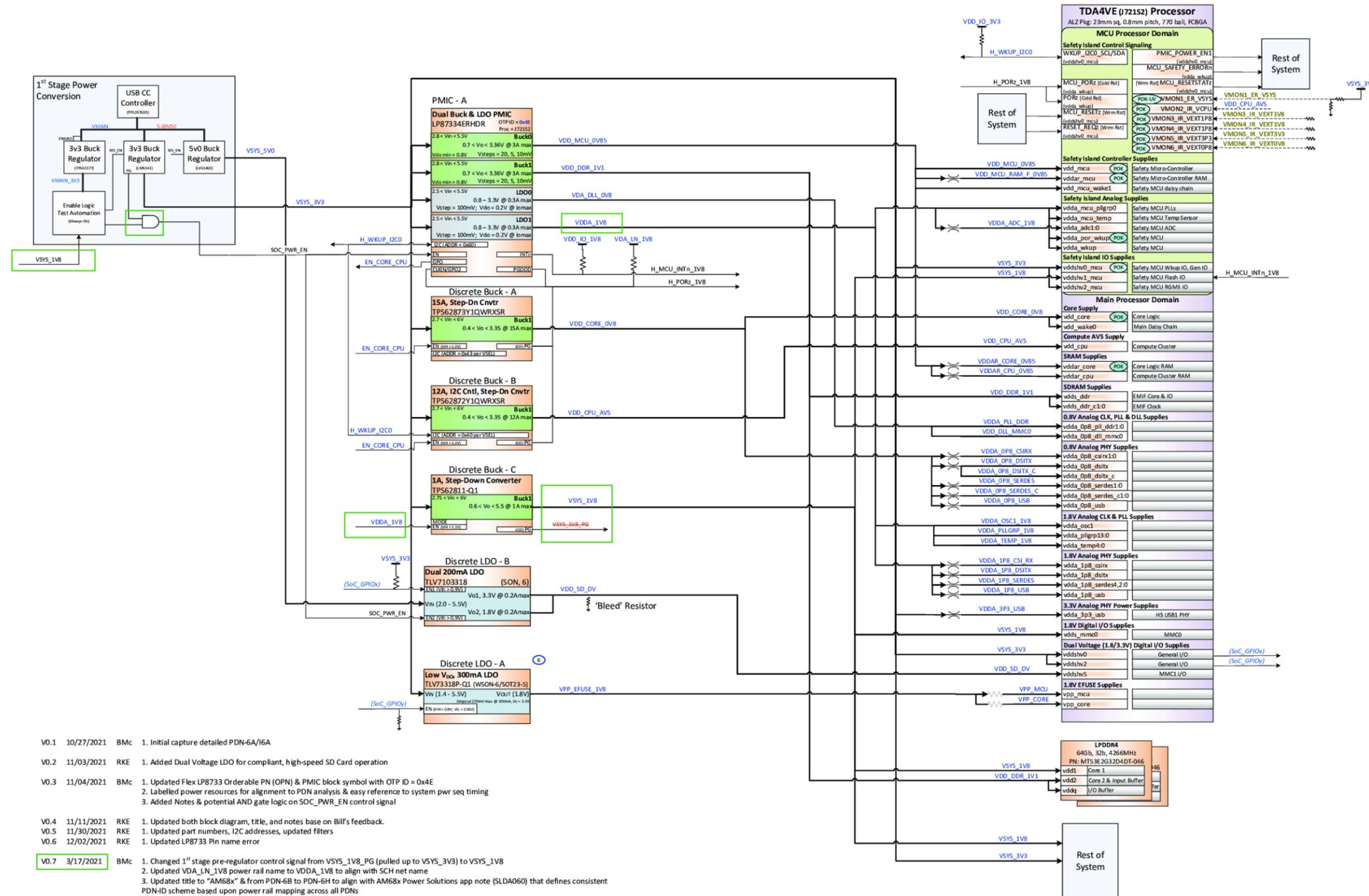
PDN

AM68x SK Edge AI - Flex + Tulip PDN-6H (Power Rail & GPIO Mapping Overview)

Flex PMIC, PN LP87334ERHDR-Q1 (TI OTP ID = 4E)
Tulip Buck, PN TPS62873Y1QWRXSR
Tulip Buck, PN TPS62872Y1QWRXSR

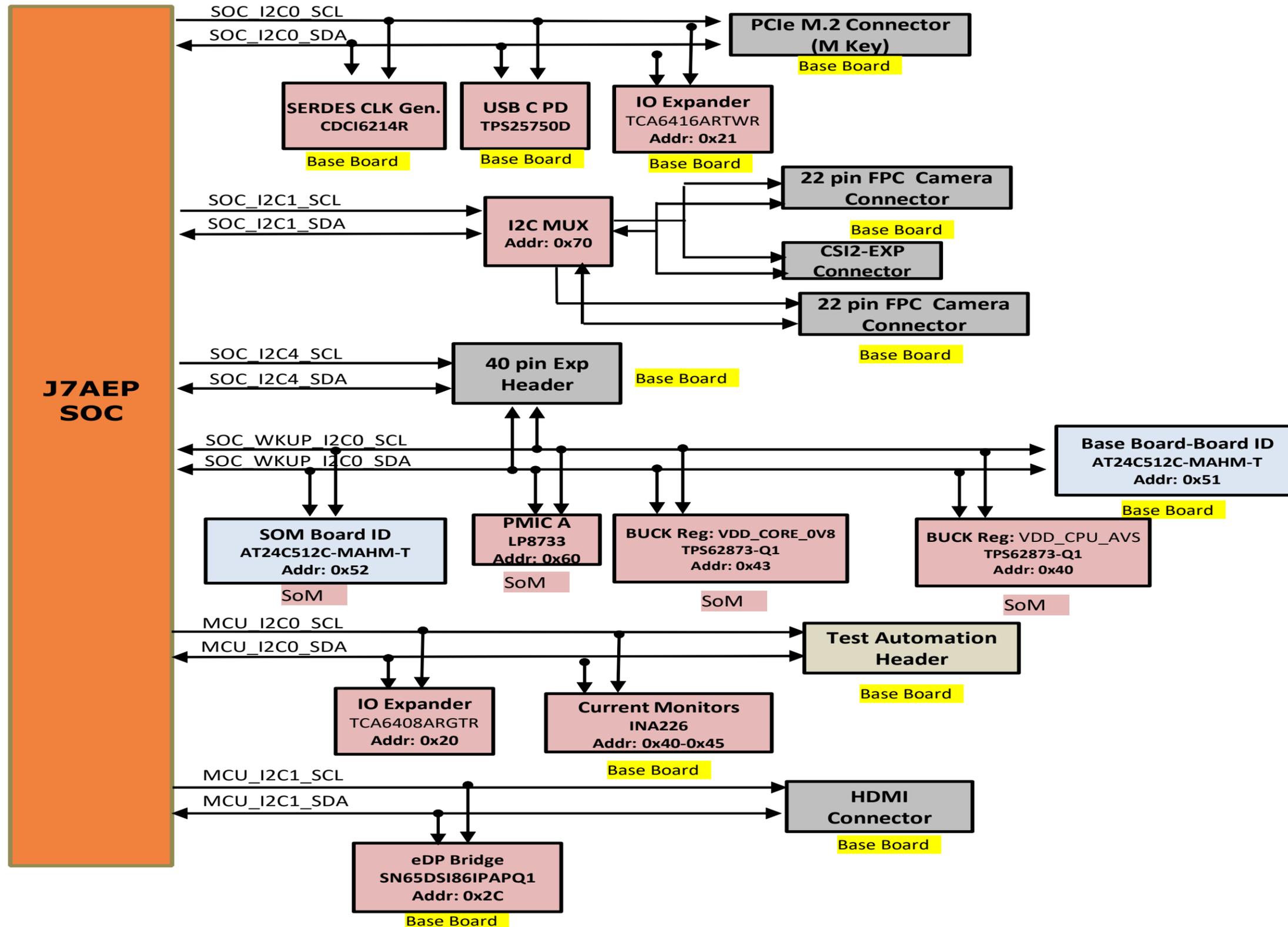
Features Supported :

1. J721S2 Superset Use-Case Performance with 2.0GHz clock and Peak Power est.
2. Supports J721S2 Junction Temperature (Tj) up to 105C
3. 32Gb LPDDR4 Memory, Dual 32b Interfaces at 4266MT/s
4. Supports both 3.3V and 1.8V digital IO
5. Includes capacity on IO rails to support variety of peripherals (xSPI Flash, eMMC, etc)
6. Supports UHS-I compliant SD cards (Dual-Voltage IO)
7. High Secure/Field Securable Device Support
8. No Low/Partial Power Modes Support (MCU-only, Retention, etc)



Project :	J7 EVM		Title	PDN
Size	C		PROC131 001 AM68 SK	Rev
Date:	Tuesday, March 21, 2023	Sheet	4	of 21

SoM I2C TREE DIAGRAM



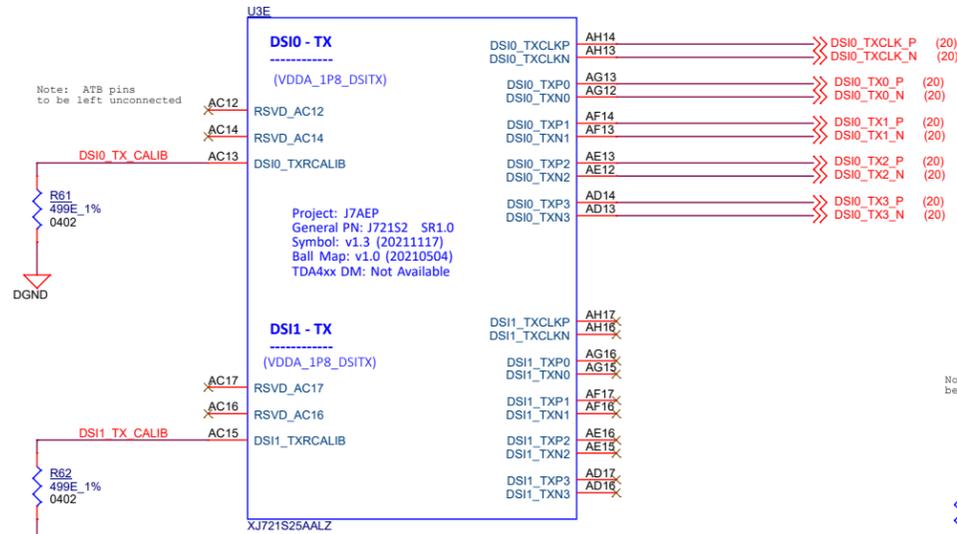
SoM I2C ADDRESS TABLE

Board	Interface name	Part#	Address	J7AEP Port mapping
EVM/SoM	Board ID EEPROM	CAV24C256WE-GT3	0x51	WKUP_I2C0
EVM/CPB	Board ID EEPROM	AT24C512C-MAHM-T	0x52	
EVM/CPB	40 pin Expansion Header			
EVM/SoM	PMIC and BUCK's	PMIC A: LP7733	0x60	
		BUCK: TPS62873	0x40	
		BUCK: TPS62873	0x43	
EVM/CPB	16 bit I2C GPIO Expander	TCA6424ARGJR	0X21	Main I2C0
EVM/CPB	SerDes Clock gen	CDCI6214	Optional	
EVM/CPB	PCIe M.2 M Key			
EVM/CPB	USC C PD controller	TPS25750DRJKR	0x20	
EVM/CPB	I2C MUX	TCA9543APWR	0x70	Main I2C1
EVM/CPB	CSI2 Expansion Connector	QSH-020-01-L-D-DP-A-K		
EVM/CPB	CSI FPC Connector	22_1734248		
EVM/CPB	40 pin Expansion Header			Main I2C4
EVM/SoM	CURRENT MONITORs	INA231AIYFDR	0x40,0x41,0x41,0x43,0x44,0x45	MCU I2C0
EVM/CPB	Test automation header			
EVM/CPB	Bootmode IO Expander	TCA6408ARGTR	0x20	
EVM/CPB	eDP Bridge	SN65DSI86IPAPQ1	0x2C	MCU I2C1

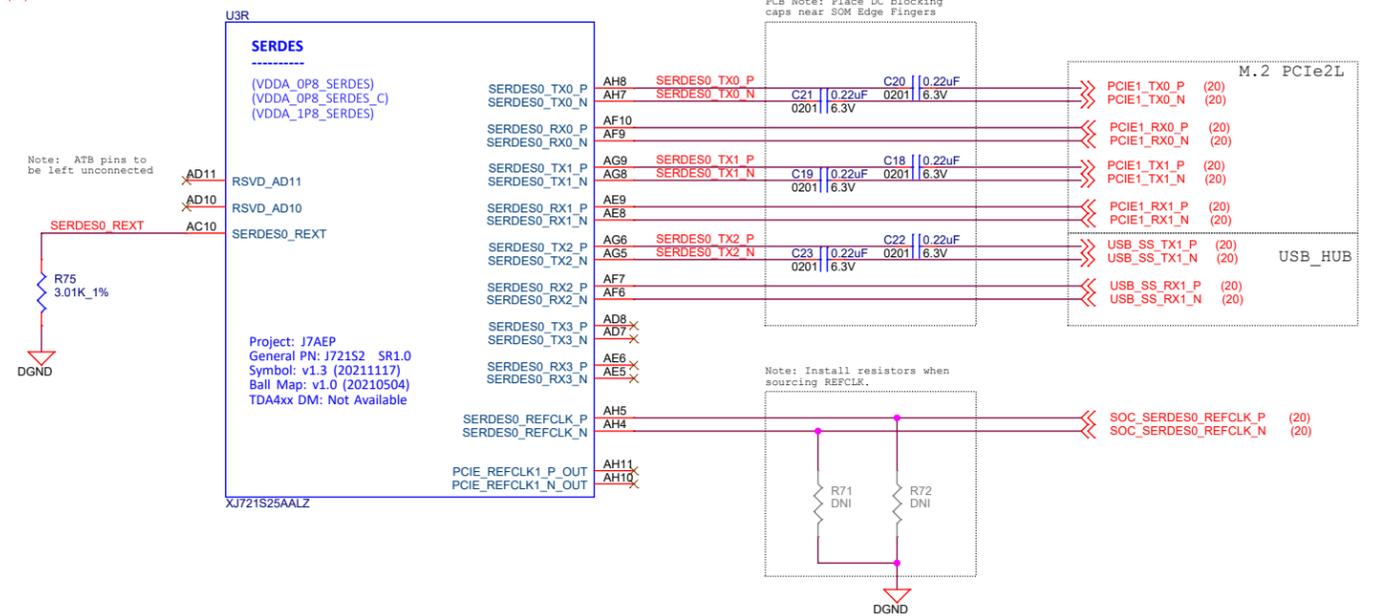
SoC GPIO MAPPING TABLE

J7x SoM - GPIO Mapping Table						
WKUP Domain						
J7AEP Mapping		Net name	Input/ Output	Default	State	Remarks
Package Signal Name	GPIO Number					
MCU_OSPI0_CSn1	WKUP_GPIO0_28	EN_EFUSE_VPP	Output	PU	Active High	Enable pin for VPP_EFUSE supply
MCU_OSPI0_CS2	WKUP_GPIO0_29	CPLD_TMS/USER_LED1	Output	NA	NA	JTAG signals for CPLD & USER LED enable signal. 1:2 Mux on base board
MCU_OSPI1_CLK	WKUP_GPIO0_31	CPLD_TCK/MCU_RGMII_INTz	Input	PD	NA	JTAG signals for CPLD & MCU_RGMII_INT signal. 1:2 Mux on base board
MCU_OSPI1_CSNO	WKUP_GPIO0_38	CSI_EXP_GPIO_4	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_CSN1	WKUP_GPIO0_39	PMIC_INTn_1V8	Input	PU	Active low	Interrupt signal from PMIC
MCU_OSPI1_D0	WKUP_GPIO0_34	CPLD_TDI/ eDP_IRQ	Input	NA	NA	JTAG signals for CPLD & Interrupt signal from eDP bridge. 1:2 Mux on base board
MCU_OSPI1_D1	WKUP_GPIO0_35	CSI_EXP_GPIO_5	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_D2	WKUP_GPIO0_36	CSI_EXP_GPIO_2	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_D3	WKUP_GPIO0_37	CSI_EXP_GPIO_3	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_OSPI1_DQS	WKUP_GPIO0_33	CPLD_TDO/ SOC_WAKE	Output	NA	NA	JTAG signals for CPLD
MCU_OSPI1_LBCLKO	WKUP_GPIO0_32	CSI_EXP_GPIO_1	I/O	NA	NA	GPIO Signals for CSI expansion connector
MCU_SPIO_CLK	WKUP_GPIO0_54	WKUP_GPIO0_54	Output	BOOTMODE	Active low	CPLD_JTAG/GPIOn_SEL. Mux select signal for CPLD JTAG and GPIO's
MCU_SPIO_CS0	WKUP_GPIO0_70	WKUP_GPIO0_70	I/O	BOOTMODE	NA	FPC Camera GPIO signals
MCU_SPIO_D1	WKUP_GPIO0_69	SYS_MCU_PWRDN	Output	BOOTMODE	Active High	System Power Down ('0' - normal operation, '1' - system power down)
WKUP_GPIO0_10	WKUP_GPIO0_10	MCU_ADC_EXT_TRIGGER0/PCIE_1_M.2_CLKREQ#				ADC external trigger from TI safety header(Default connection)/CLKREQ#
WKUP_GPIO0_11	WKUP_GPIO0_11	MCU_CLKOUT0	Output	NA	NA	25MHz reference clock for CSI expansion connector
WKUP_GPIO0_15	WKUP_GPIO0_15	MCU_SPI1_CS2	Output	BOOTMODE	Active low	MCU SPI1 signals
WKUP_GPIO0_49	WKUP_GPIO0_49	WKUP_GPIO0_49	I/O	NA	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_57	WKUP_GPIO0_57	WKUP_GPIO0_57	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_56	WKUP_GPIO0_56	WKUP_GPIO0_56	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_66	WKUP_GPIO0_66	WKUP_GPIO0_66	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
WKUP_GPIO0_67	WKUP_GPIO0_67	WKUP_GPIO0_67	I/O	BOOTMODE	NA	GPIO signal for 40 pin expansion header
PMIC_POWER_EN1	WKUP_GPIO0_88	WKUP_GPIO0_88	I/O	NA	NA	FPC Camera GPIO signals
MCU_ADC1_AIN0	WKUP_GPIO0_79	SOC_INT1z	Input	PU	Active low	Test automation INT signal
MCU_ADC1_AIN1	WKUP_GPIO0_80	SOC_INT2z	Input	PU	Active low	Test automation INT signal
Main Domain						
ECAPO_IN_APWM_OUT	GPIO0_49	SEL_SDIO_3v3_1v8n	Output	PU	Active low	VDD_SD_DV 1.8V or 3.3V selection control
TIMER_IO0	GPIO0_58	MMC1_SDCD	Input	PU	Active low	SD card detect signal
TIMER_IO1	GPIO0_59	USB0_DRVVBUS	Output	NA	Active High	USB VBUS Drive signal
EXTINTN	GPIO0_0	HDMI_HPD	Input	NA	Active High	HDMI hot plug detect signal
MCAN1_TX	GPIO0_27	GPIO0_27	I/O	NA	NA	GPIO signal for 40 pin expansion header
MCAN13_TX	GPIO0_3	GPIO0_3	I/O	NA	NA	GPIO signal for 40 pin expansion header
MCASPO_AXR8	GPIO0_36	GPIO0_36	I/O	NA	NA	GPIO signal for 40 pin expansion header
MCASPO_AXR13	GPIO0_41	GPIO0_41/UART5_CTSn	I/O	NA	NA	GPIO signal for 40 pin expansion header/ UART5_CTS Signal
MCASPO_AXR14	GPIO0_42	GPIO0_42/UART5_RTSn	I/O	NA	NA	GPIO signal for 40 pin expansion header/ UART5_RTS Signal
GPIO Expander on Base Board						
Port NO		I2C Instance	Input/O output	Default	State	Usage
P00	CSI_VIO_SEL	I2C0 ADDR: 0x21	Output	PD	Active High	Enable for VCC_CSI_IO supply generation load switch
P01	CSI_SEL_FPC_EXPn		Output	PD	Active High	CSI MUX selection
P02	HDMI_PDn		Output	PD	Active Low	Power down signal for HDMI Transmitter
P03	HDMI_LS_OE		Output	PU	Active High	HDMI current limit load switch enable
P04	DPO_3V3_EN		Output	PD	Active High	Enable signal for Display port load switch
P05	BOARDID_EEPROM_WP		Output	PD	Active High	Board id Eeeprom Write protect signal
P06	CAN_STB		Output	PD	Active High	Standby signals for MAIN & MCU domain CAN Transceivers
P10	GPIO_uSD_PWR_EN		Output	PU	Active High	Micro SD card Load switch enable
P11	eDP_ENABLE		Output	PD	Active High	Used for Enable of DSI to eDP Bridge
P12	IO_EXP_Pcie1_M.2_RTSz		Output	NA	Active Low	PCIe Reset input to CPLD
P13	IO_EXP_MCU_RGMII_RST#		Output	NA	Active Low	MCU_RGMII reest input to CPLD
P14	IO_EXP_CSI2_EXP_RSTz		Output	PD	Active Low	CSI expansion connector reset
P16	CSIO_B_GPIO1		Output	NA	NA	FPC Camera1 GPIO signal
P17	CSIO_B_GPIO1		Output	NA	NA	FPC Camera2 GPIO signal

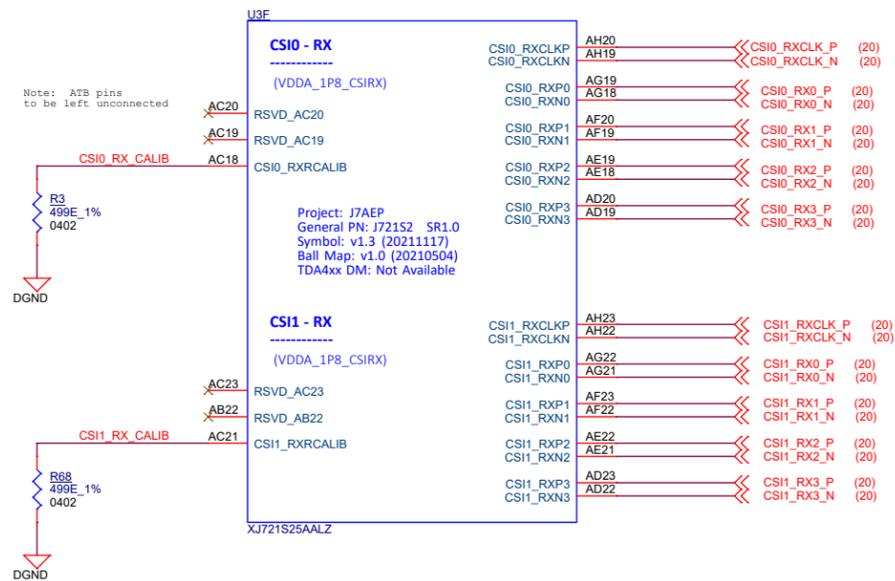
DSI Interface



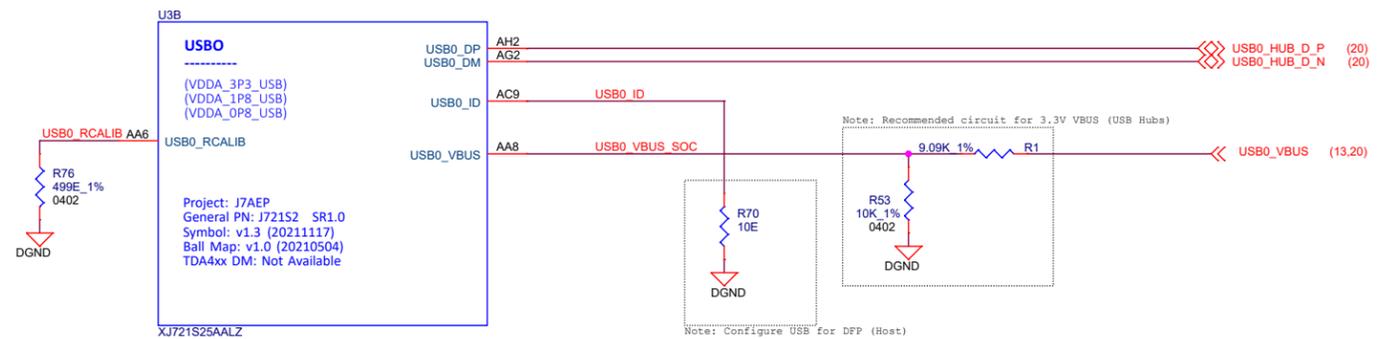
SERDES Interface (PCIE/USB)



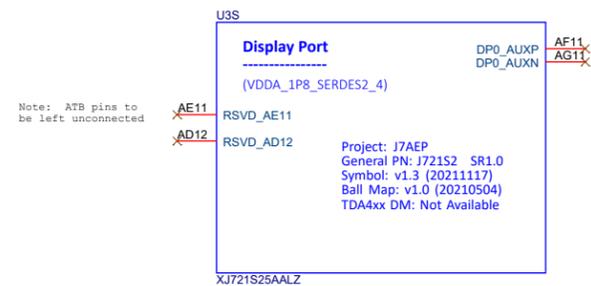
CSI Interface



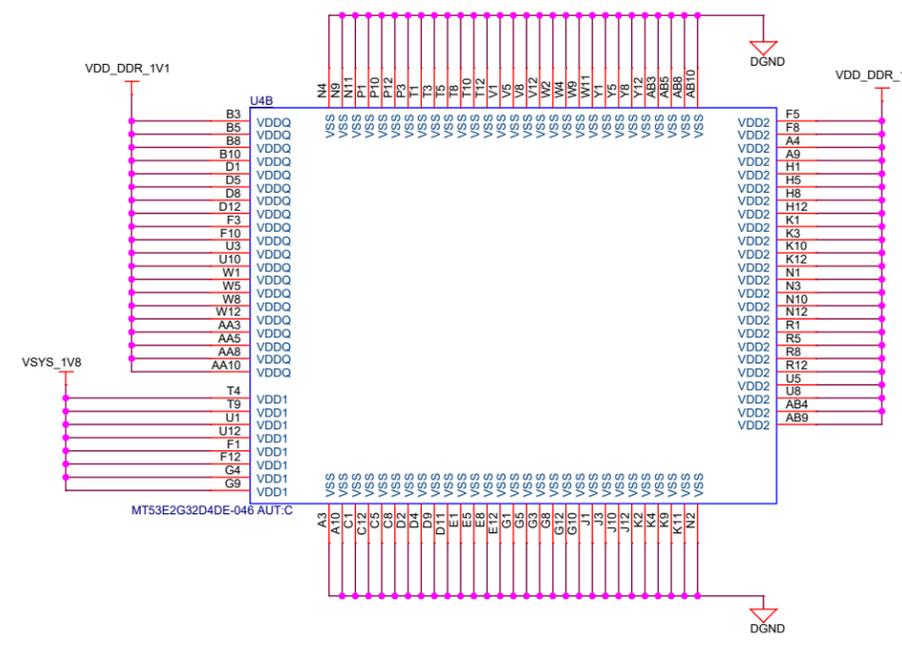
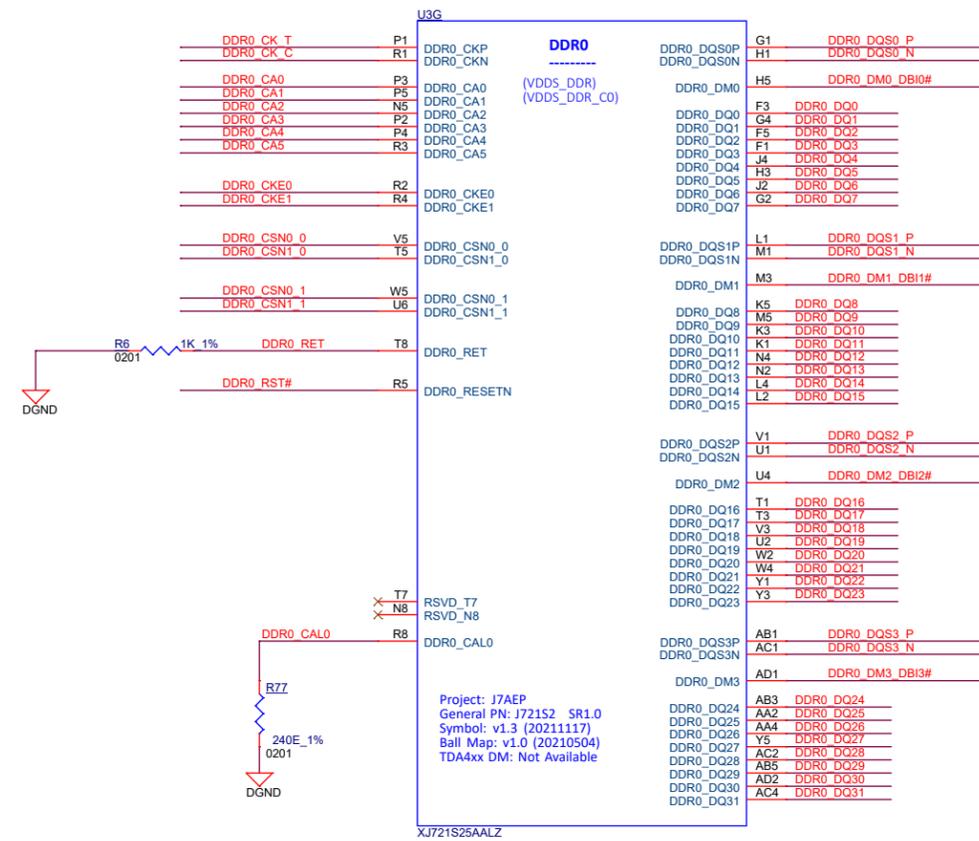
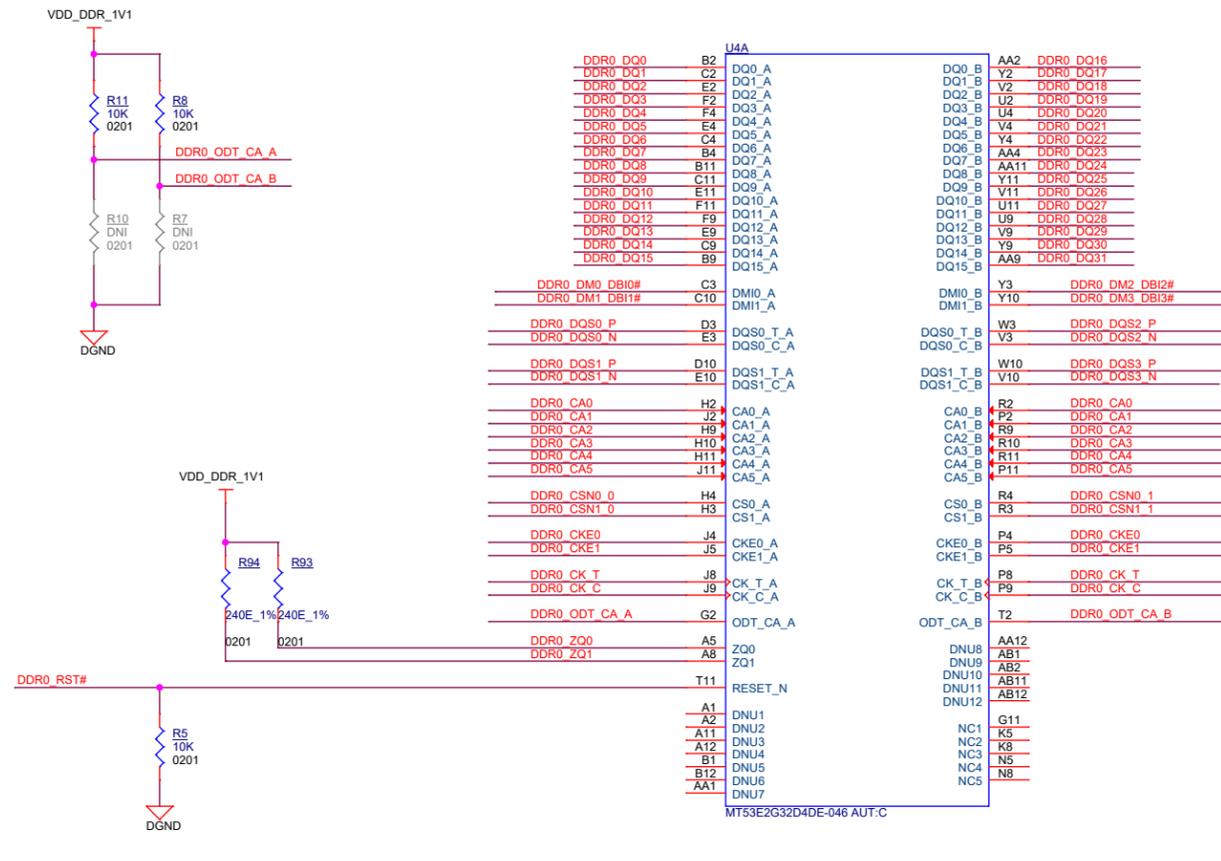
USB2.0 Interface



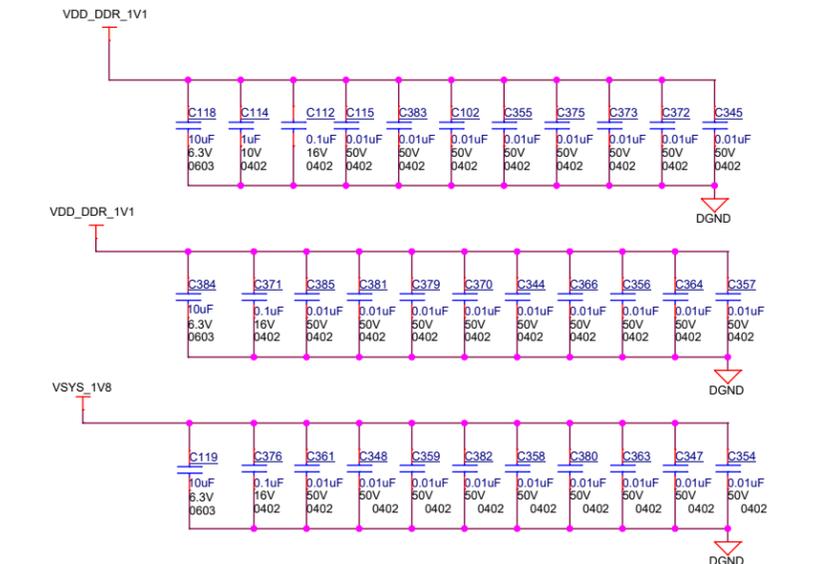
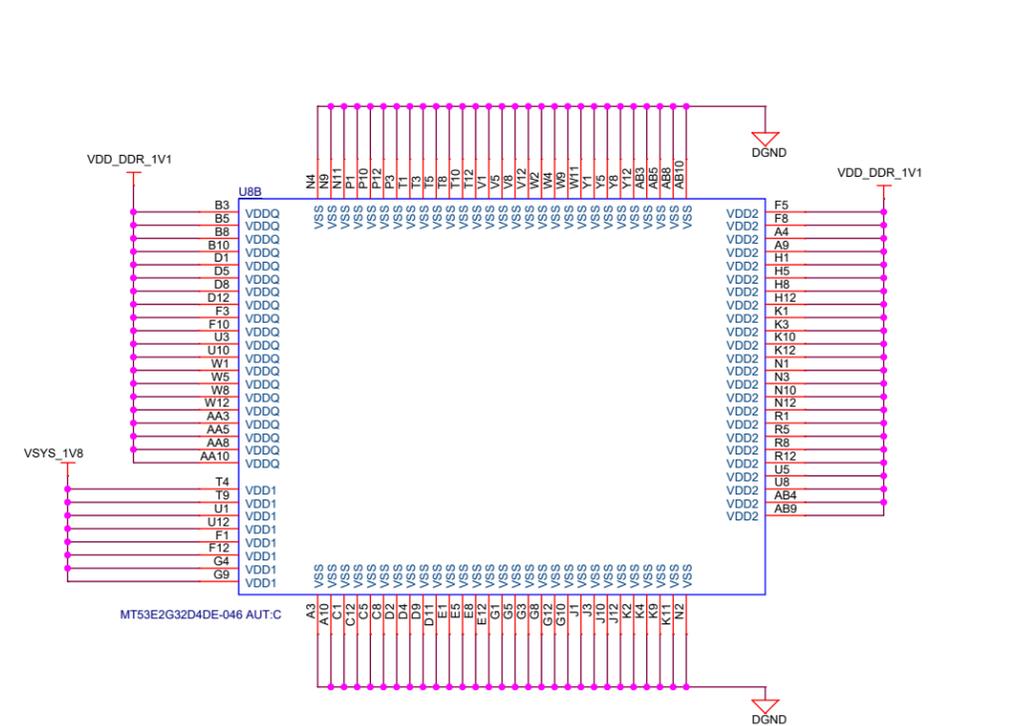
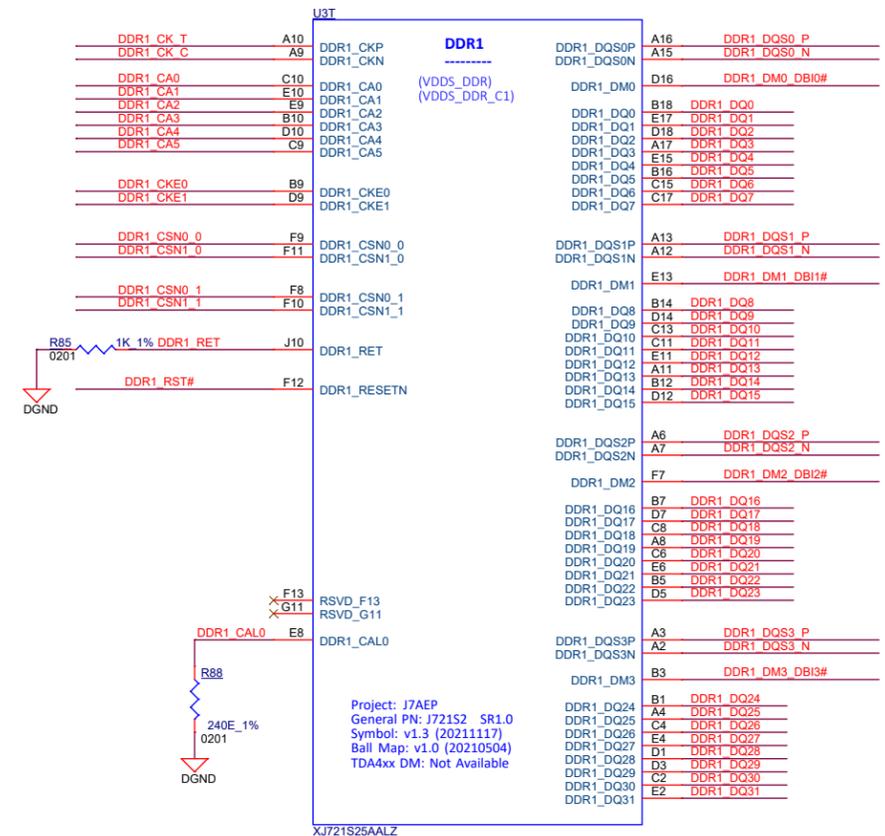
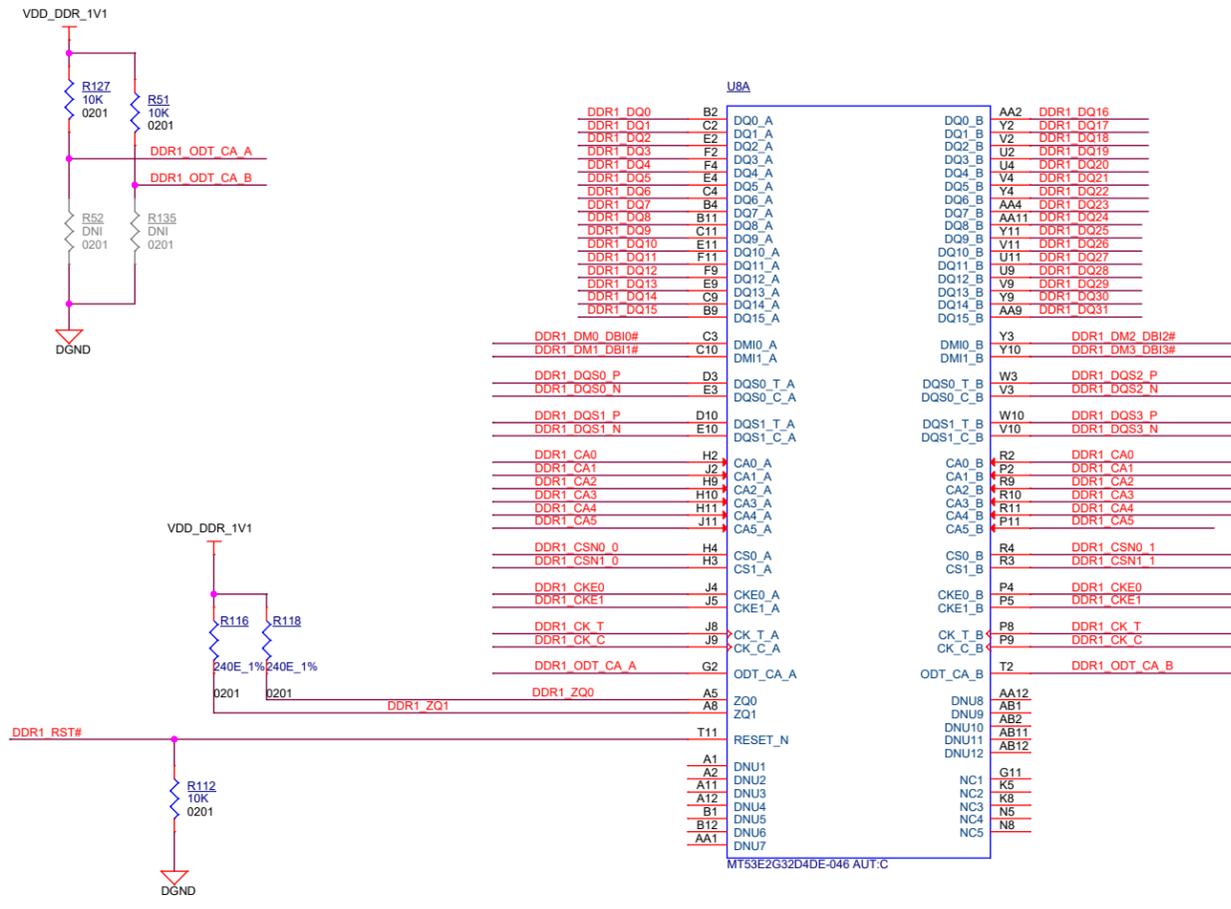
DP Aux



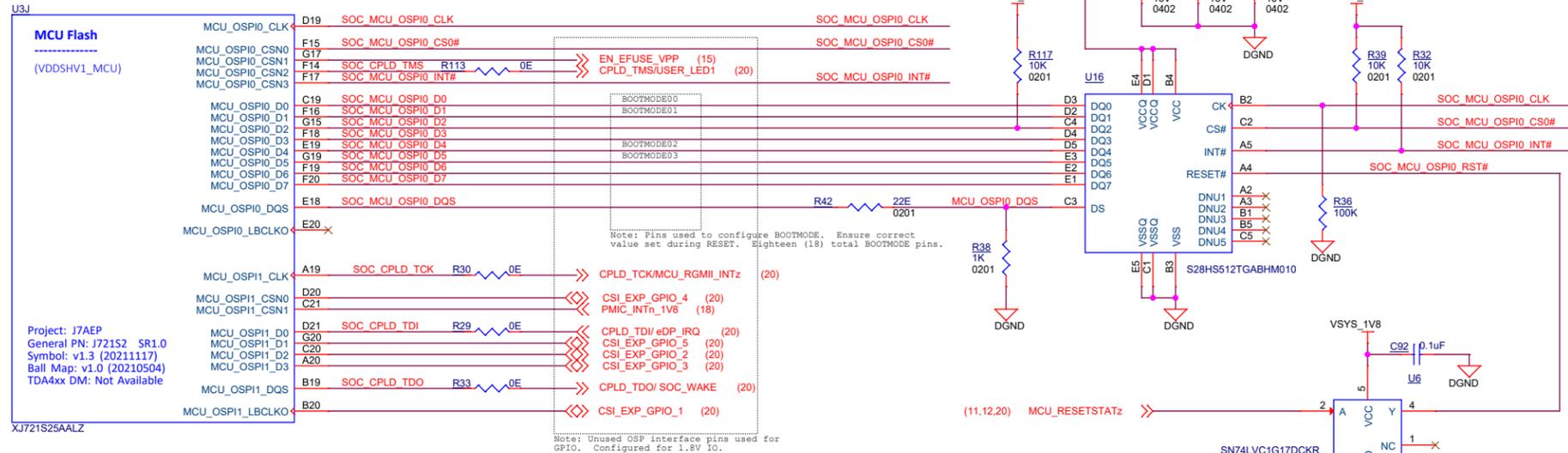
LPDDR4 Interface (Bank 0)



LPDDR4 Interface (Bank 1)

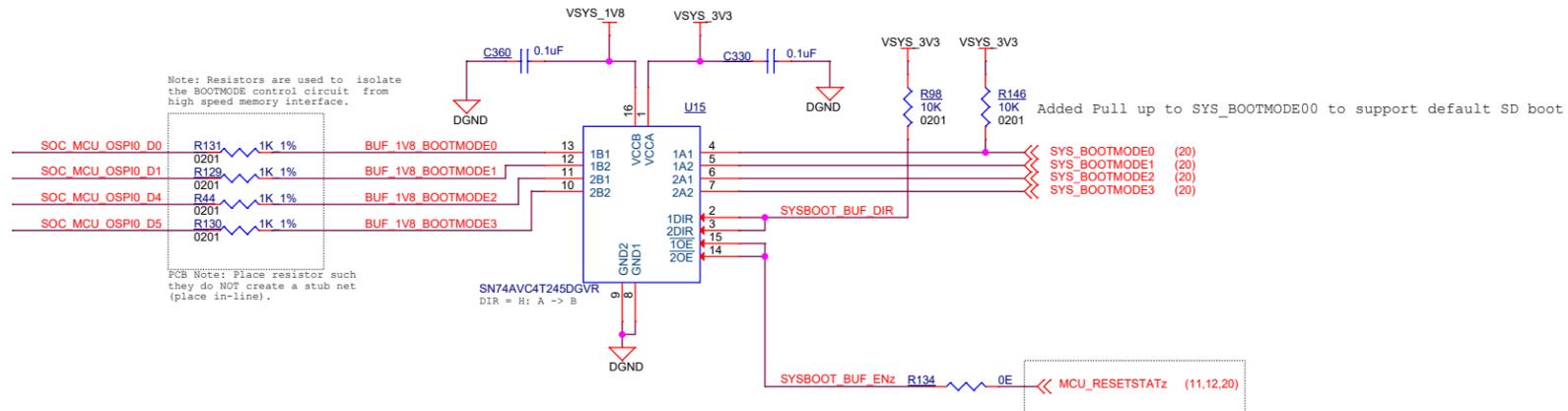


MCU OSPI Interface

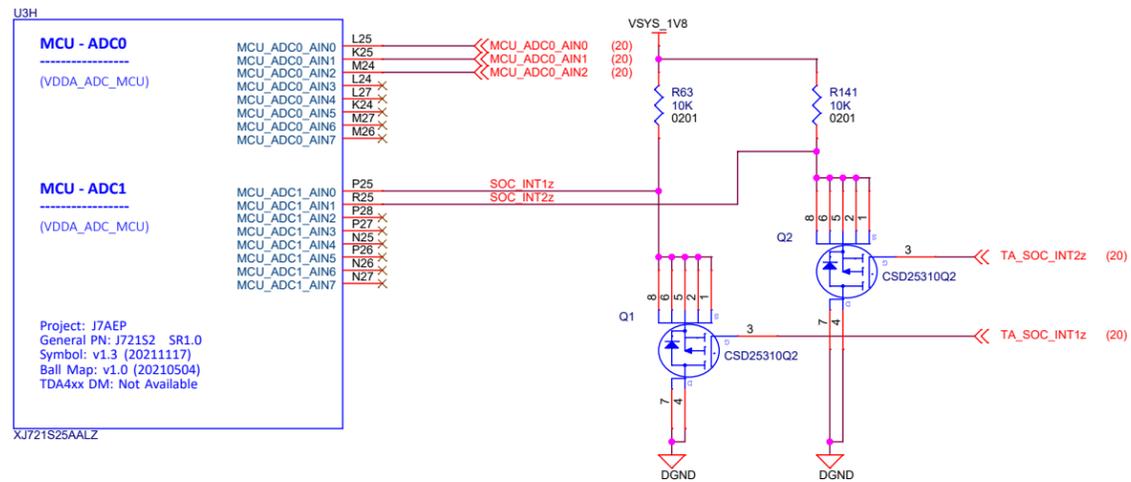


BOOTMODE Control Logic

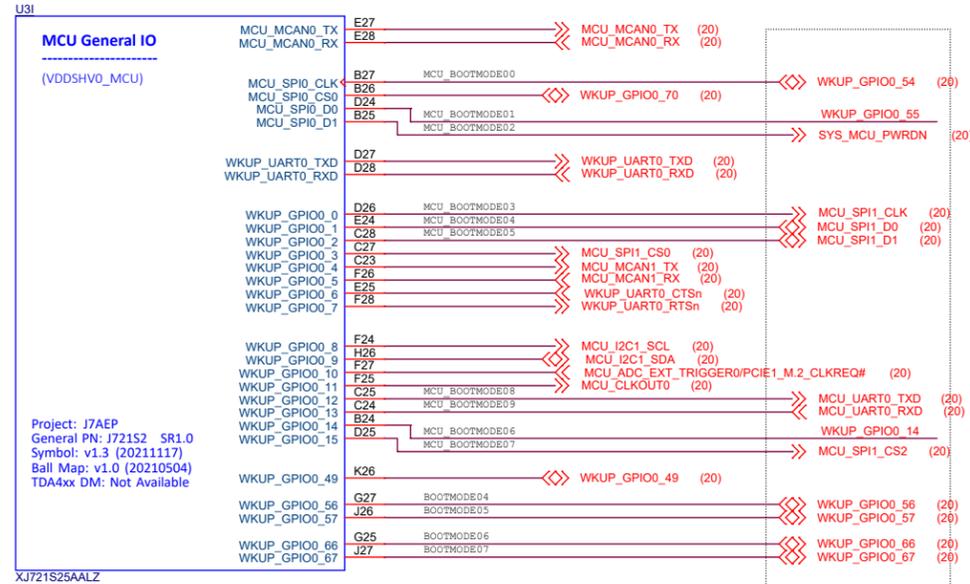
Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).



MCU ADCs



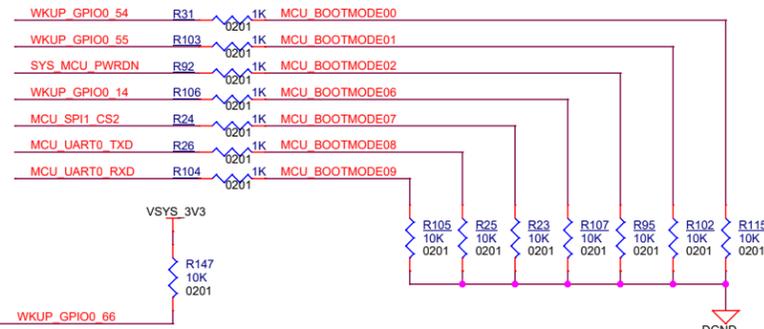
MCU GENERAL IO



BOOTMODE Control Logic

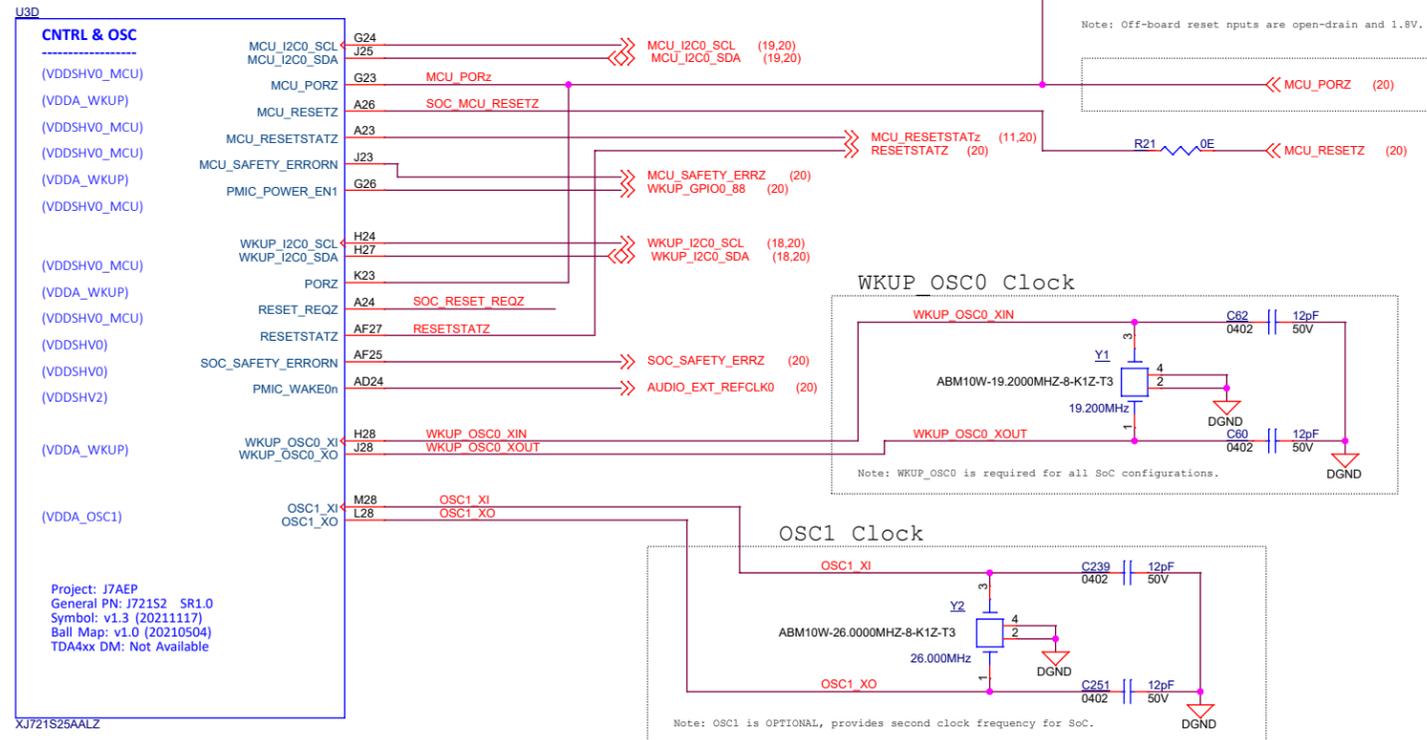
Note: Logic used to configure BOOTMODE settings during reset. This is seven(7) of a total of eighteen (18) boot pins. These settings configure for:

MCU_BOOTMODE[2:0] set '000' for WKUP_OSC0 of 19.2MHz
 MCU_BOOTMODE[6] set '0' for Normal Boot
 MCU_BOOTMODE[7] set '0' for Reserved
 MCU_BOOTMODE[9:8] set '00' for LBIST + FBIST

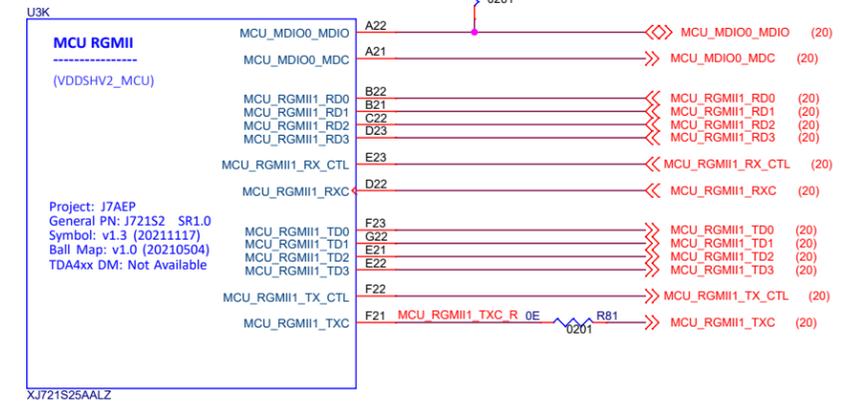


Note: Pins used to configure BOOTMODE. Ensure correct value set during RESET. Eighteen (18) total BOOTMODE pins.

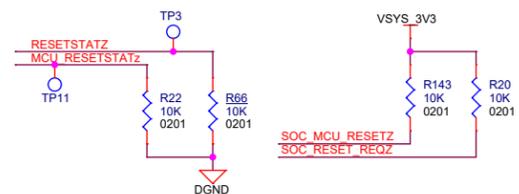
MCU CNTRL and OSC



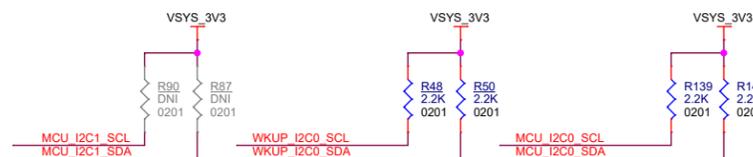
MCU RGMII



RESET Pull Resistors

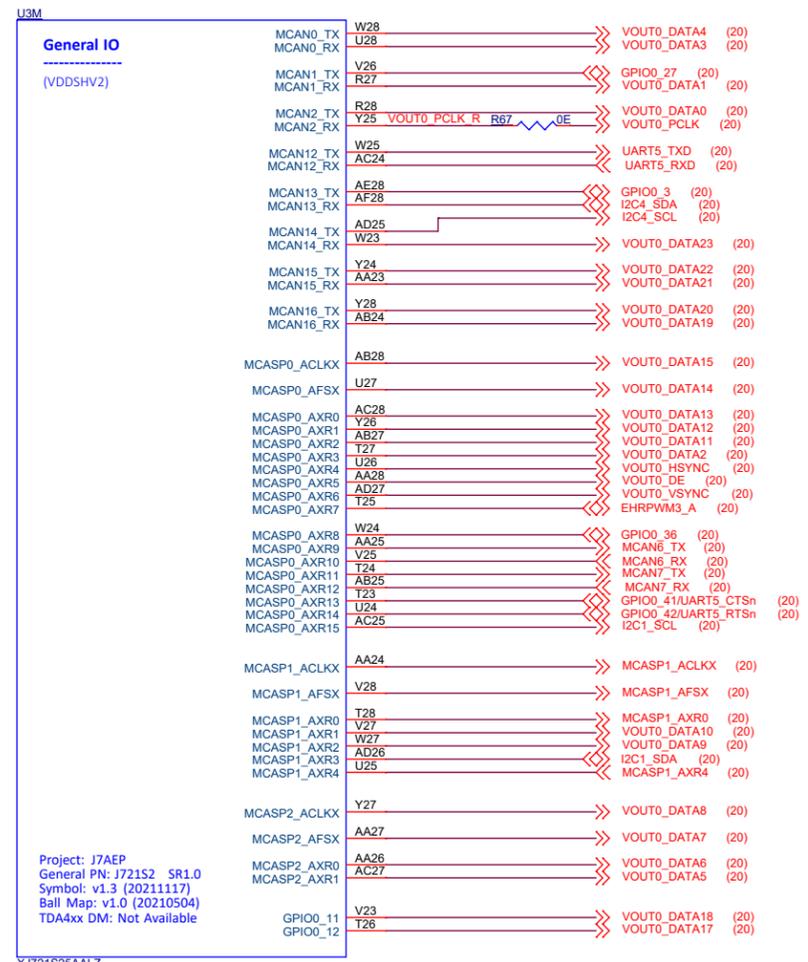
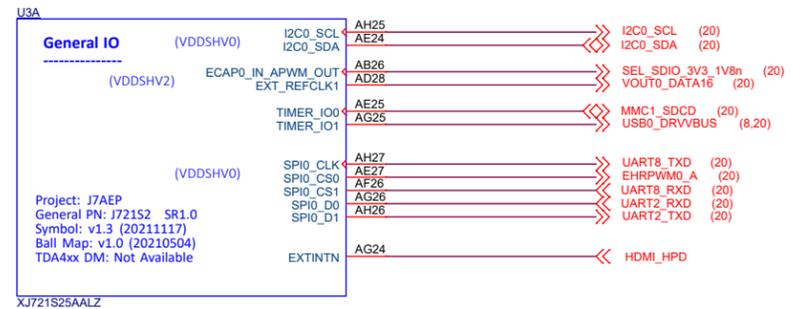


MCU I2C Pull-Ups

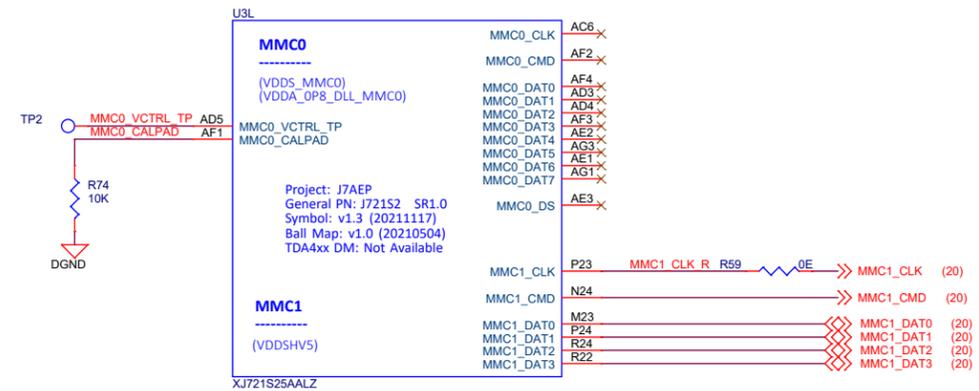


Project :	J7 EVM		Title	
			SOC_GENERAL&MCU_GENERAL	
Size	C	PROC131 001 AM68 SK	Rev	E2
Date:	Tuesday, March 21, 2023	Sheet	12	of 21

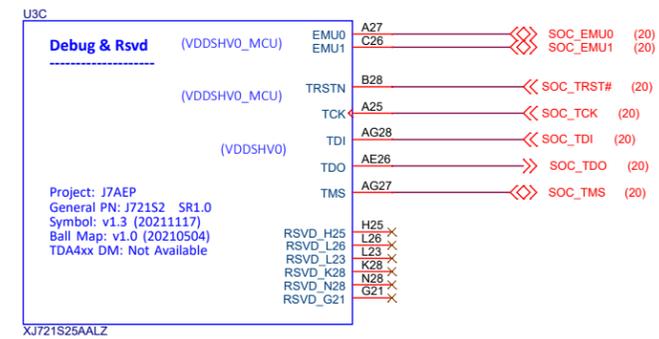
GENERAL IO



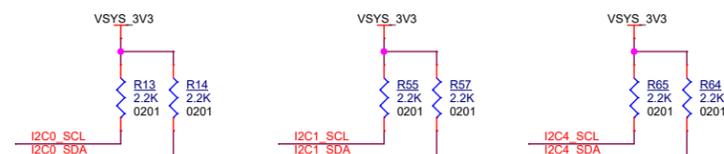
MMC Interface



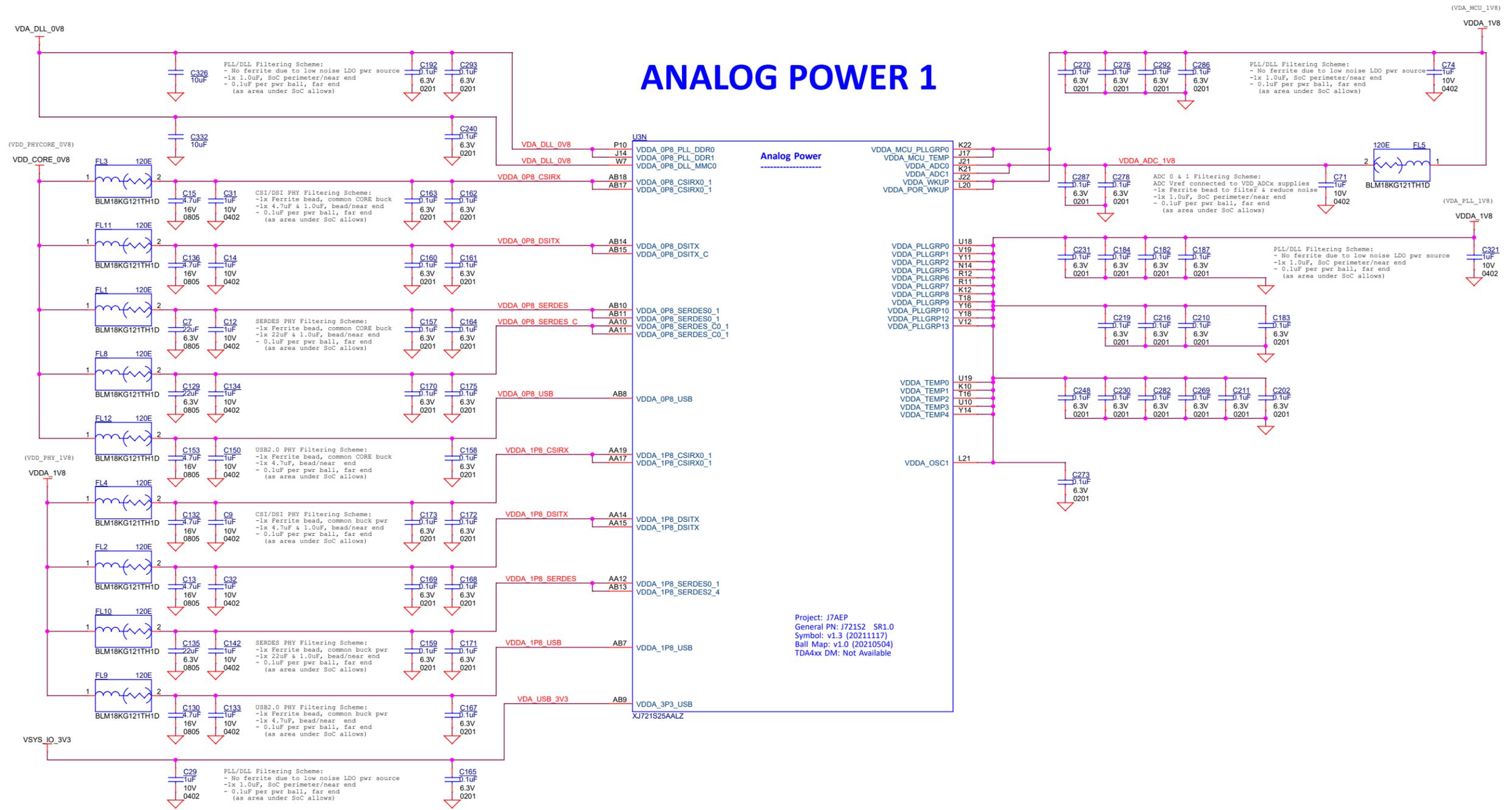
DEBUG



I2C Pull-Ups



ANALOG POWER 1

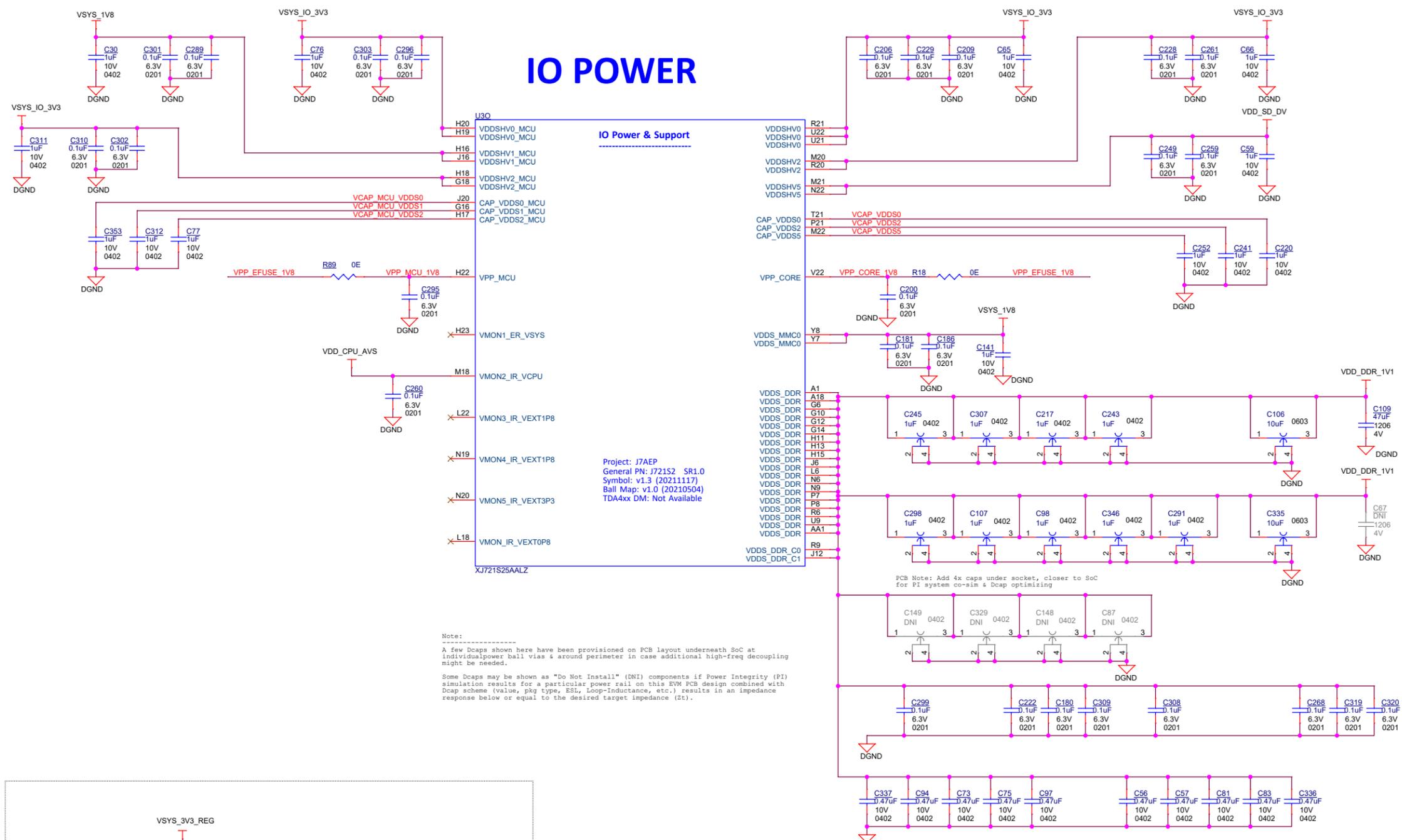


Analog Power

Project: J7AEP
 General PN: J721S2 SR1.0
 Symbol: v1.3 (20211117)
 Ball Map: v1.0 (20210504)
 TDA4xx DM: Not Available

Project : J7 EVM		Title SOC ANALOG POWER 1	
		Size C	Rev E2
Date: Tuesday, March 21, 2023		Sheet 14 of 21	

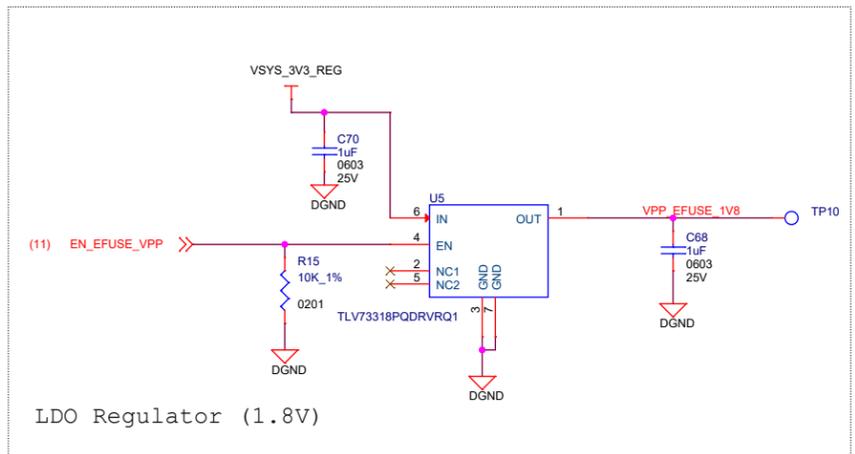
IO POWER



IO Power & Support

Project: J7AEP
 General PN: J721S2 SR1.0
 Symbol: v1.3 (20211117)
 Ball Map: v1.0 (20210504)
 TDA4xx DM: Not Available

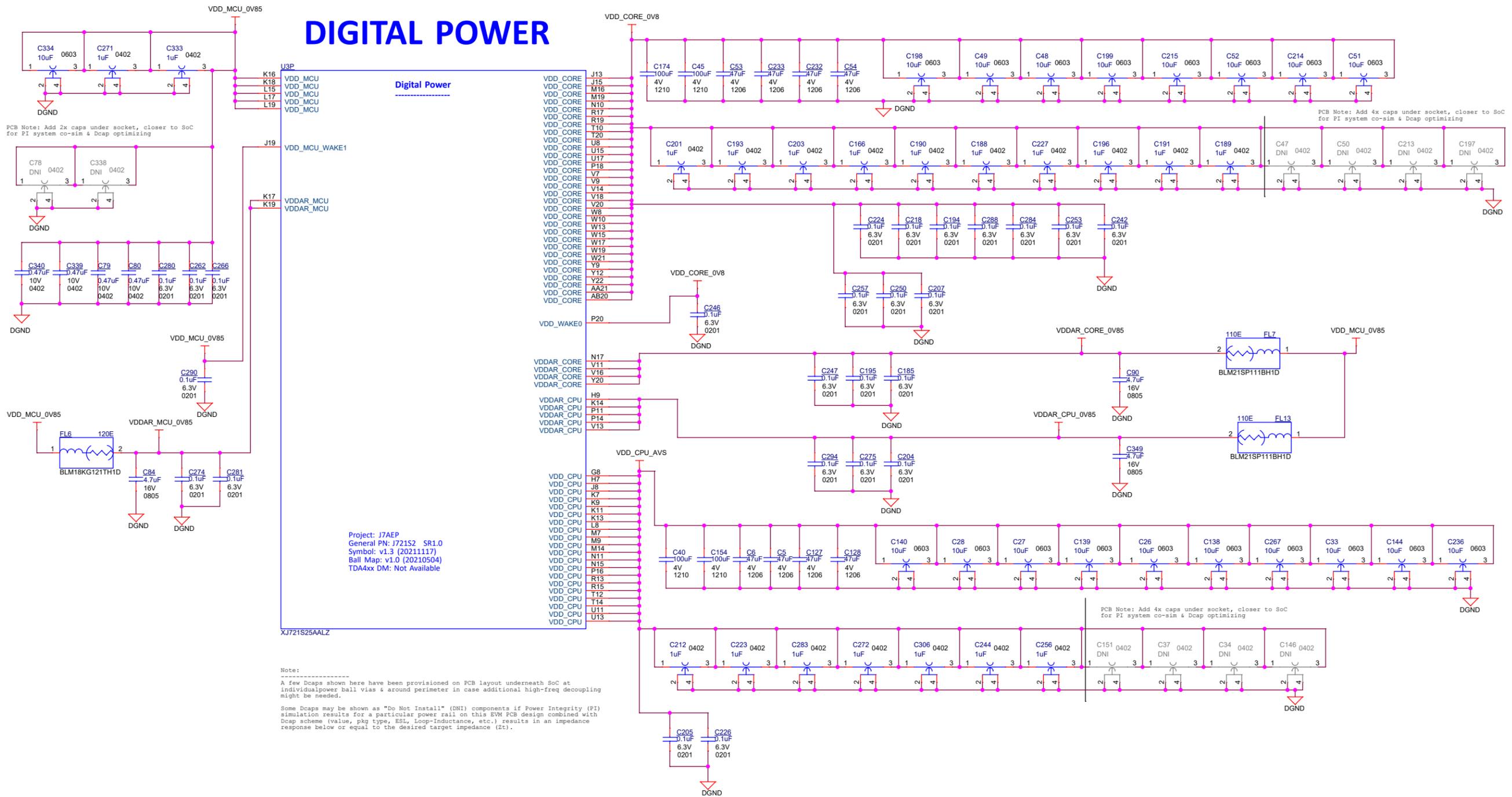
Note:
 A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.
 Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).



LDO Regulator (1.8V)

Project : J7 EVM		Title : SOC DIGITAL IO & SUPPORT POWER 2	
		Size : PROC131 001 AM68 SK	Rev : E2
		Date : Tuesday, March 21, 2023	Sheet 15 of 21

DIGITAL POWER



PCB Note: Add 2x caps under socket, closer to SoC for PI system co-sim & Dcap optimizing

PCB Note: Add 4x caps under socket, closer to SoC for PI system co-sim & Dcap optimizing

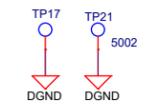
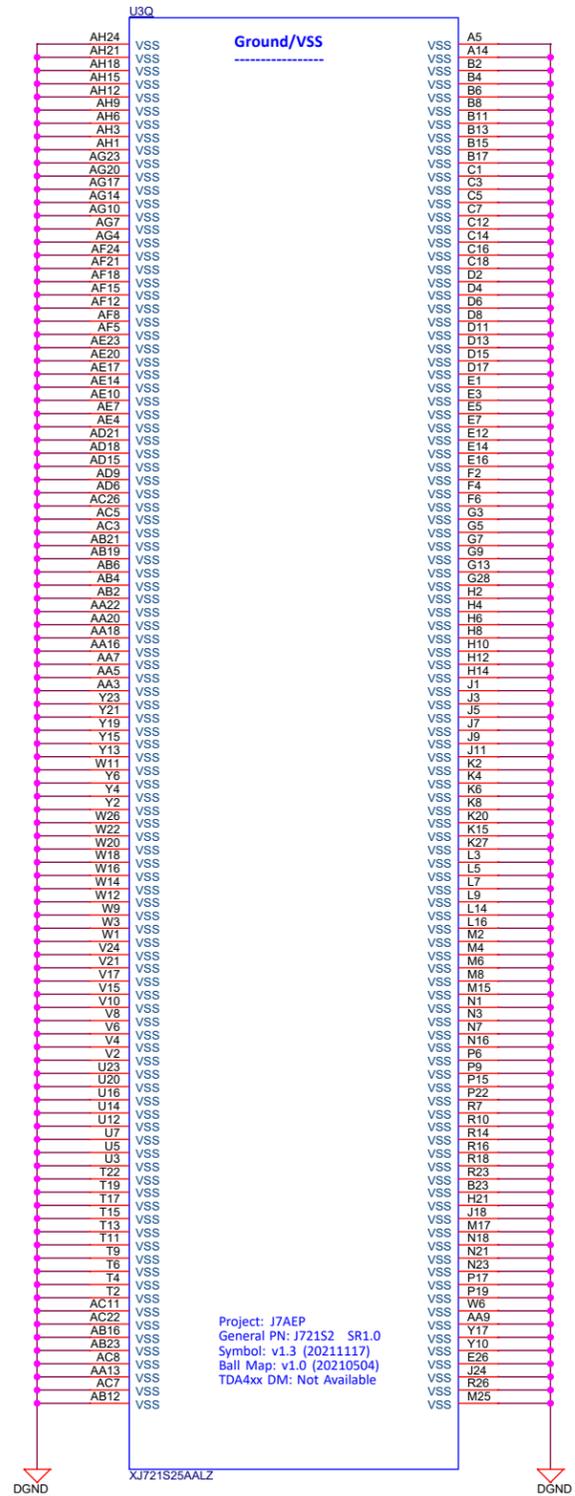
PCB Note: Add 4x caps under socket, closer to SoC for PI system co-sim & Dcap optimizing

Project: J7AEP
 General PN: J721S2 SR1.0
 Symbol: v1.3 (20211117)
 Ball Map: v1.0 (20210504)
 TDA4xx DM: Not Available

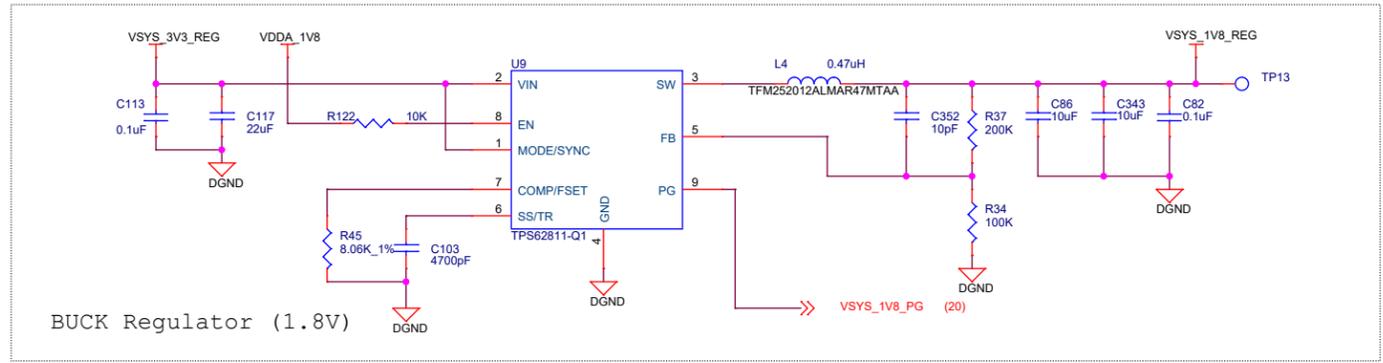
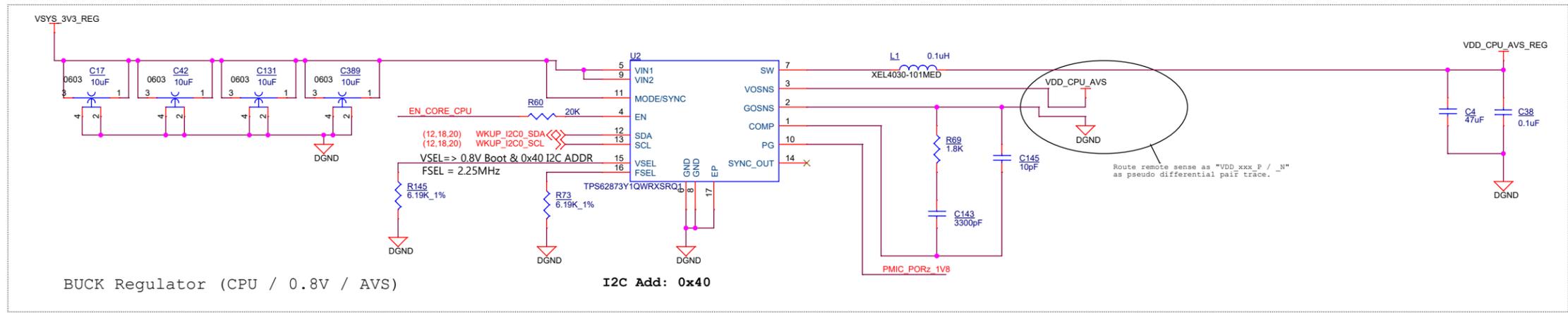
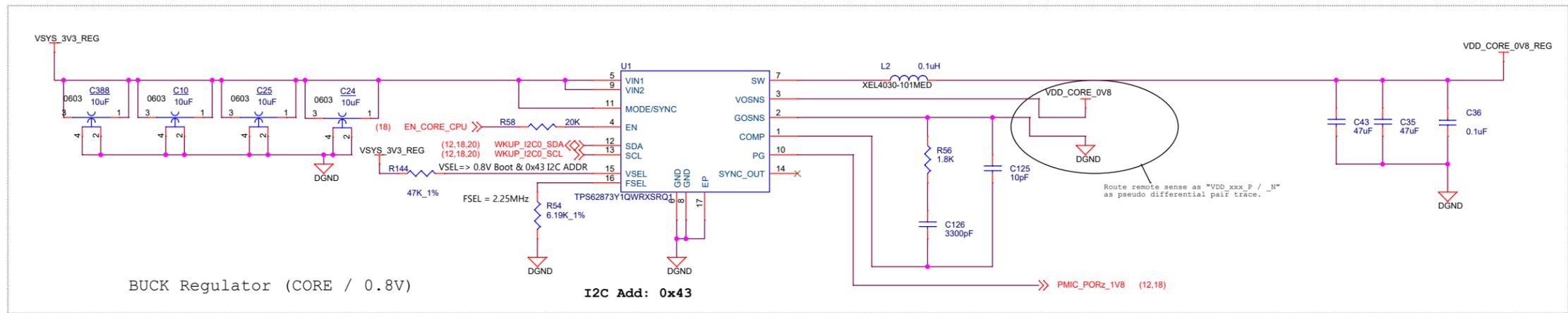
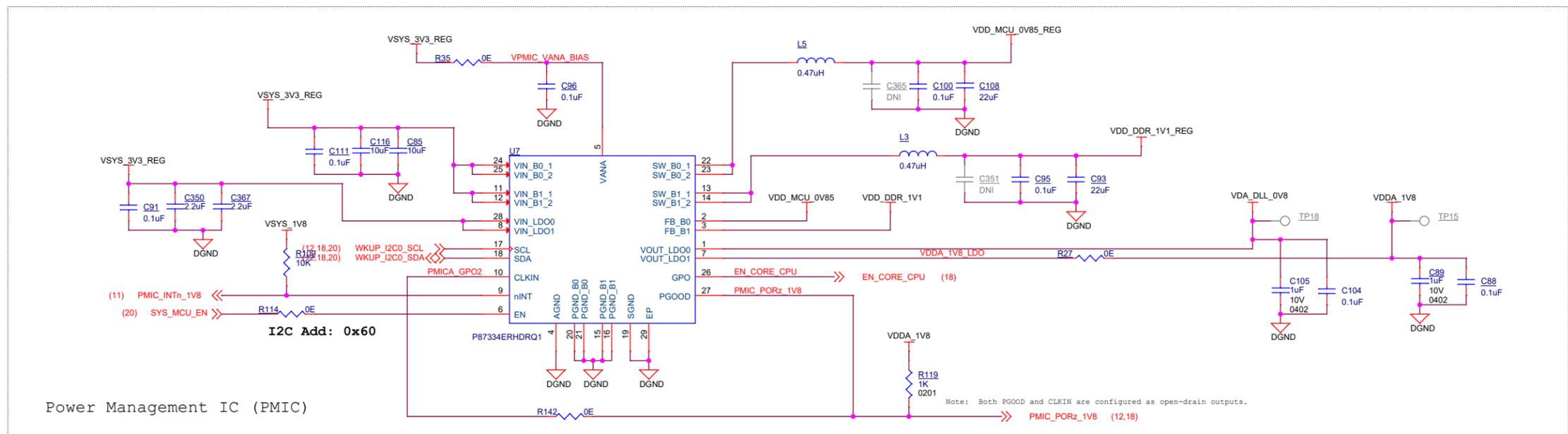
Note:
 A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.
 Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : J7 EVM		Title SOC DIGITAL POWER 3	
		Size C	Rev E2
Date: Tuesday, March 21, 2023		Sheet 16 of 21	

SOC GROUND



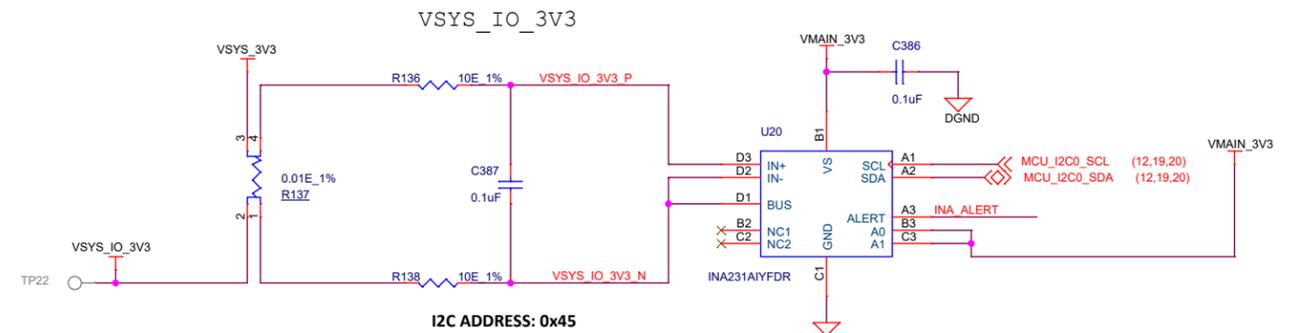
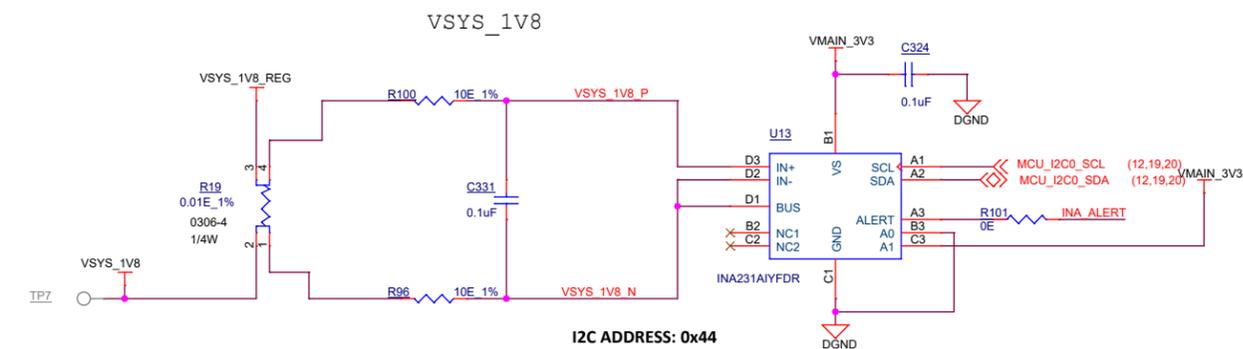
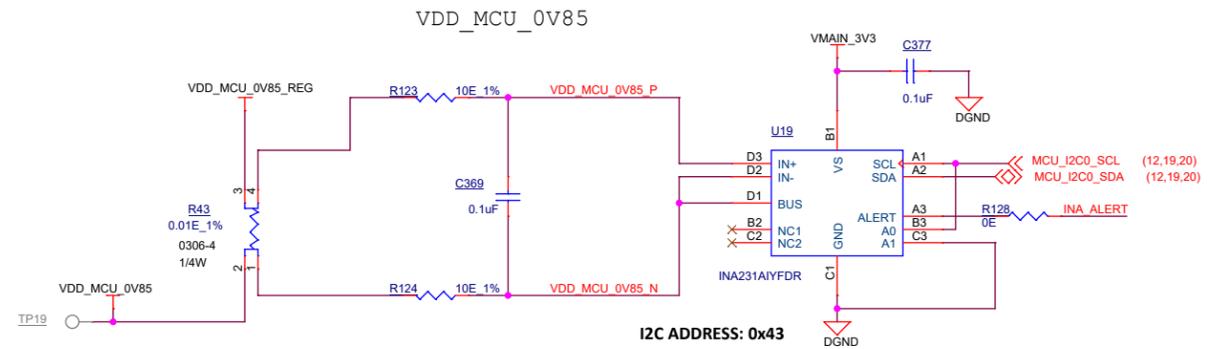
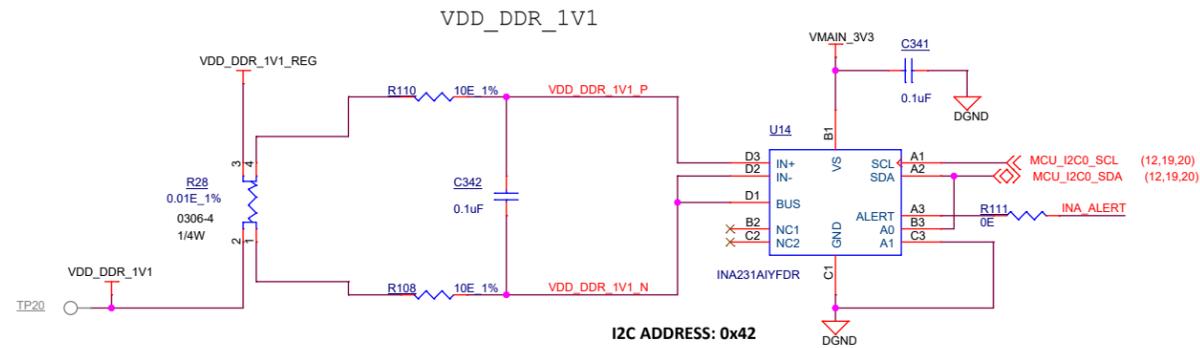
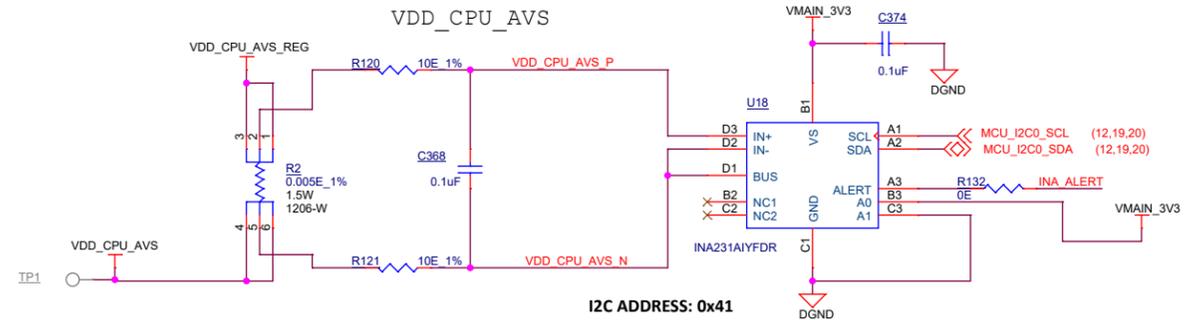
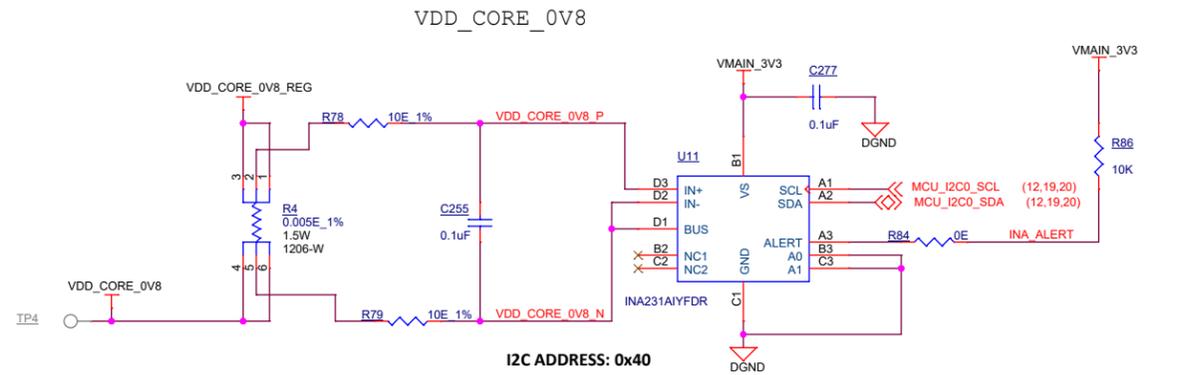
Project : J7 EVM		Title SOC GROUND	
		Size C	Rev E2
		Date: Tuesday, March 21, 2023	Sheet 17 of 21



POWER SUPPLY

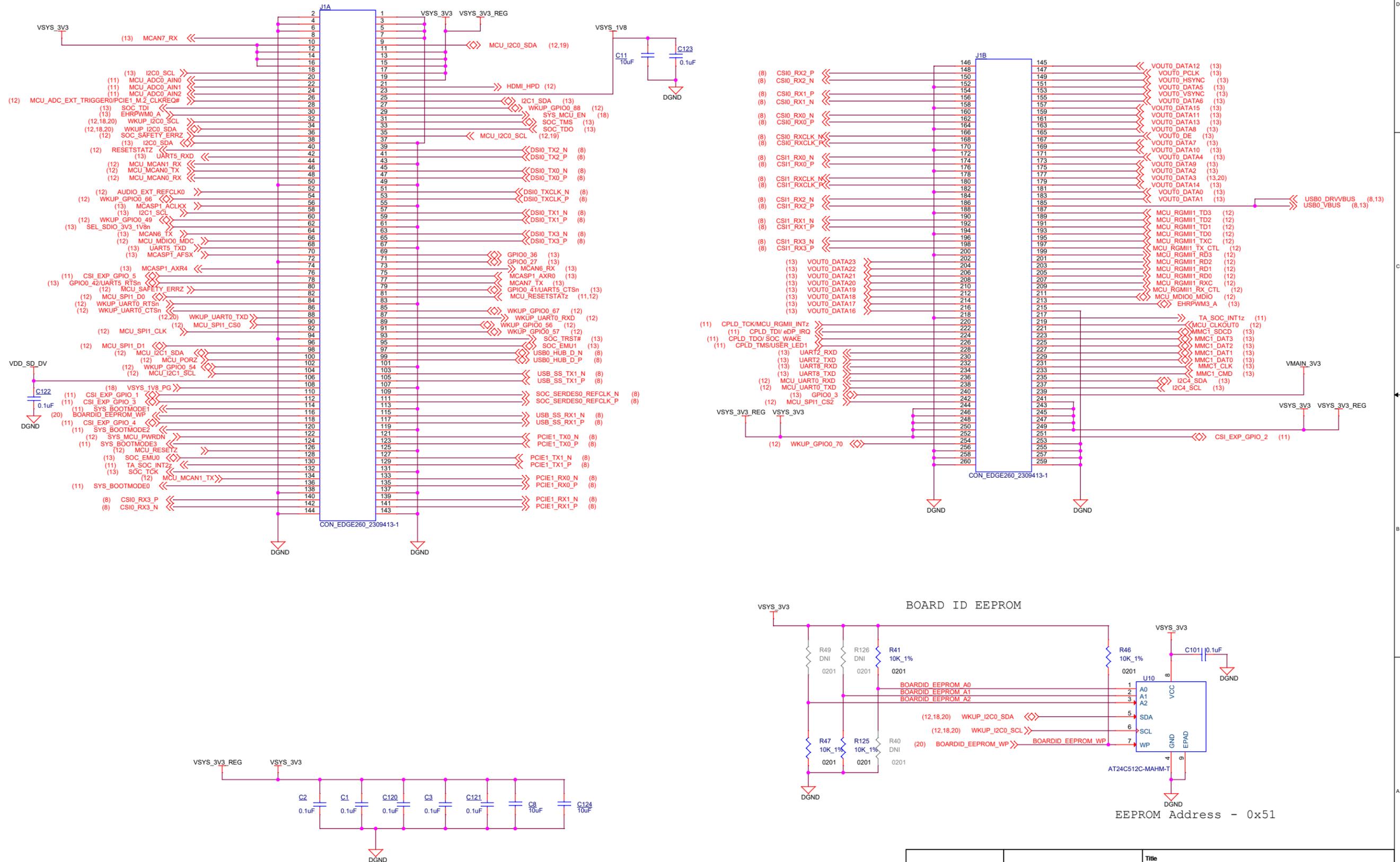
Project : J7 EVM		Title PMIC and Power Supply	
		Size C	Rev E2
Date: Monday, March 27, 2023		Sheet 18 of 21	

CURRENT MONITOR



Project :	J7 EVM		Title	
			Current sense	
Date:	Tuesday, March 21, 2023		Size	Rev
			C	PROC131 001 AM68 SK
			Sheet	19 of 21

260 PIN SODIMM CONNECTOR



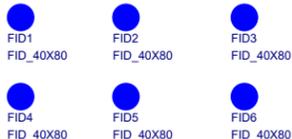
Project :	J7 EVM		Title	
			SODIMM 260 PIN EDGE FINGERS	
Date:	Tuesday, March 21, 2023		Size	PROC131 001 AM68 SK
			Rev	E2
Sheet			20	of 21

NOTES, HW & LABELS

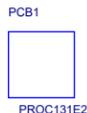
ASSEMBLY NOTES

- All MSL components should be baked as per JEDEC standard.
- PCB should be baked at 120 degree for 8 hours.
- Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- These assemblies are ESD sensitive, ESD precautions shall be observed.
- These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- Provide serial numbers to the assembled boards for identification.
- The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

FIDUCIALS



BARE PCB



AM68 SK ASSEMBLED BASEBOARD



LABELS

Board Serial No.



AM6-COMPROCEVM

Assembly Revision.



AM6-COMPROCEVM

OPN: SK - AM68

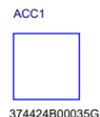
LOGOs



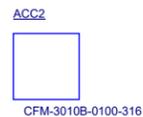
STANDOFF,SCREW & WASHER FOR SOM



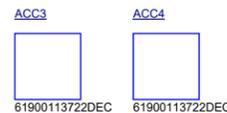
HEATSINK



FAN



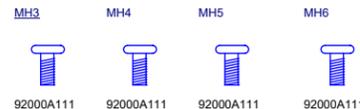
CRIMP PIN



CONN HOUSING



SCREW FOR FAN ASSEMBLY



Project : J7 EVM



Title Hardware Schematic	
Size C	Rev E2
Date: Tuesday, March 21, 2023	Sheet 21 of 21