

J721E DRA829/TDA4VM/AM68P Processors Silicon Revision 1.1 Texas Instruments Families of Products



1 Mailbox Registers

Table 1-2 lists the memory-mapped registers for the MAILBOX0. All register offset addresses not listed in Table 1-2 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. Mailbox Instances

Instance	Base Address
NAVSS0_MAILBOX0_REGS0	31F8 0000h
NAVSS0_MAILBOX0_REGS1	31F8 1000h
NAVSS0_MAILBOX0_REGS2	31F8 2000h
NAVSS0_MAILBOX0_REGS3	31F8 3000h
NAVSS0_MAILBOX0_REGS4	31F8 4000h
NAVSS0_MAILBOX0_REGS5	31F8 5000h
NAVSS0_MAILBOX0_REGS6	31F8 6000h
NAVSS0_MAILBOX0_REGS7	31F8 7000h
NAVSS0_MAILBOX0_REGS8	31F8 8000h
NAVSS0_MAILBOX0_REGS9	31F8 9000h
NAVSS0_MAILBOX0_REGS10	31F8 A000h
NAVSS0_MAILBOX0_REGS11	31F8 B000h

Table 1-2. Mailbox Registers

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS0 Physical Address	NAVSS0_MAILBOX0_REGS1 Physical Address
0h	MAILBOX_REVISION	Peripheral ID register	31F8 0000h	31F8 1000h
10h	MAILBOX_SYSCONFIG	Mailbox control register	31F8 0010h	31F8 1010h
40h + formula	MAILBOX_MESSAGE_y	Message Mailbox y	31F8 0040h + formula	31F8 1040h + formula
80h + formula	MAILBOX_FIFO_STATUS_y	FIFO status for Mailbox y	31F8 0080h + formula	31F8 1080h + formula
C0h + formula	MAILBOX_MSG_STATUS_y	Number of messages in Mailbox y	31F8 00C0h + formula	31F8 10C0h + formula
100h + formula	MAILBOX_IRQ_STATUS_RAW_j	Raw status for each event for user j	31F8 0100h + formula	31F8 1100h + formula
104h + formula	MAILBOX_IRQ_STATUS_CLR_j	Masked status for each event for user j	31F8 0104h + formula	31F8 1104h + formula
108h + formula	MAILBOX_IRQ_ENABLE_SET_j	Set interrupt enables user j	31F8 0108h + formula	31F8 1108h + formula
10Ch + formula	MAILBOX_IRQ_ENABLE_CLR_j	Clear interrupt enables user j	31F8 010Ch + formula	31F8 110Ch + formula
140h	MAILBOX_IRQ_EOI	End of interrupt register	31F8 0140h	31F8 1140h

Table 1-3. Mailbox Registers 2

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS2 Physical Address	NAVSS0_MAILBOX0_REGS3 Physical Address
0h	MAILBOX_REVISION	Peripheral ID register	31F8 2000h	31F8 3000h
10h	MAILBOX_SYSCONFIG	Mailbox control register	31F8 2010h	31F8 3010h
40h + formula	MAILBOX_MESSAGE_y	Message Mailbox y	31F8 2040h + formula	31F8 3040h + formula
80h + formula	MAILBOX_FIFO_STATUS_y	FIFO status for Mailbox y	31F8 2080h + formula	31F8 3080h + formula
C0h + formula	MAILBOX_MSG_STATUS_y	Number of messages in Mailbox y	31F8 20C0h + formula	31F8 30C0h + formula
100h + formula	MAILBOX_IRQ_STATUS_RAW_j	Raw status for each event for user j	31F8 2100h + formula	31F8 3100h + formula
104h + formula	MAILBOX_IRQ_STATUS_CLR_j	Masked status for each event for user j	31F8 2104h + formula	31F8 3104h + formula
108h + formula	MAILBOX_IRQ_ENABLE_SET_j	Set interrupt enables user j	31F8 2108h + formula	31F8 3108h + formula
10Ch + formula	MAILBOX_IRQ_ENABLE_CLR_j	Clear interrupt enables user j	31F8 210Ch + formula	31F8 310Ch + formula
140h	MAILBOX_IRQ_EOI	End of interrupt register	31F8 2140h	31F8 3140h

Table 1-4. Mailbox Registers 3

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS4 Physical Address	NAVSS0_MAILBOX0_REGS5 Physical Address
0h	MAILBOX_REVISION	Peripheral ID register	31F8 4000h	31F8 5000h
10h	MAILBOX_SYSCONFIG	Mailbox control register	31F8 4010h	31F8 5010h
40h + formula	MAILBOX_MESSAGE_y	Message Mailbox y	31F8 4040h + formula	31F8 5040h + formula
80h + formula	MAILBOX_FIFO_STATUS_y	FIFO status for Mailbox y	31F8 4080h + formula	31F8 5080h + formula
C0h + formula	MAILBOX_MSG_STATUS_y	Number of messages in Mailbox y	31F8 40C0h + formula	31F8 50C0h + formula
100h + formula	MAILBOX_IRQ_STATUS_RAW_j	Raw status for each event for user j	31F8 4100h + formula	31F8 5100h + formula
104h + formula	MAILBOX_IRQ_STATUS_CLR_j	Masked status for each event for user j	31F8 4104h + formula	31F8 5104h + formula
108h + formula	MAILBOX_IRQ_ENABLE_SET_j	Set interrupt enables user j	31F8 4108h + formula	31F8 5108h + formula
10Ch + formula	MAILBOX_IRQ_ENABLE_CLR_j	Clear interrupt enables user j	31F8 410Ch + formula	31F8 510Ch + formula
140h	MAILBOX_IRQ_EOI	End of interrupt register	31F8 4140h	31F8 5140h

Table 1-5. Mailbox Registers 4

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS6 Physical Address	NAVSS0_MAILBOX0_REGS7 Physical Address
0h	MAILBOX_REVISION	Peripheral ID register	31F8 6000h	31F8 7000h
10h	MAILBOX_SYSCONFIG	Mailbox control register	31F8 6010h	31F8 7010h
40h + formula	MAILBOX_MESSAGE_y	Message Mailbox y	31F8 6040h + formula	31F8 7040h + formula
80h + formula	MAILBOX_FIFO_STATUS_y	FIFO status for Mailbox y	31F8 6080h + formula	31F8 7080h + formula
C0h + formula	MAILBOX_MSG_STATUS_y	Number of messages in Mailbox y	31F8 60C0h + formula	31F8 70C0h + formula

Table 1-5. Mailbox Registers 4 (continued)

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS6 Physical Address	NAVSS0_MAILBOX0_REGS7 Physical Address
100h + formula	MAILBOX_IRQ_STATUS_RAW_j	Raw status for each event for user j	31F8 6100h + formula	31F8 7100h + formula
104h + formula	MAILBOX_IRQ_STATUS_CLR_j	Masked status for each event for user j	31F8 6104h + formula	31F8 7104h + formula
108h + formula	MAILBOX_IRQ_ENABLE_SET_j	Set interrupt enables user j	31F8 6108h + formula	31F8 7108h + formula
10Ch + formula	MAILBOX_IRQ_ENABLE_CLR_j	Clear interrupt enables user j	31F8 610Ch + formula	31F8 710Ch + formula
140h	MAILBOX_IRQ_EOI	End of interrupt register	31F8 6140h	31F8 7140h

Table 1-6. Mailbox Registers 5

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS8 Physical Address	NAVSS0_MAILBOX0_REGS9 Physical Address
0h	MAILBOX_REVISION	Peripheral ID register	31F8 8000h	31F8 9000h
10h	MAILBOX_SYSCONFIG	Mailbox control register	31F8 8010h	31F8 9010h
40h + formula	MAILBOX_MESSAGE_y	Message Mailbox y	31F8 8040h + formula	31F8 9040h + formula
80h + formula	MAILBOX_FIFO_STATUS_y	FIFO status for Mailbox y	31F8 8080h + formula	31F8 9080h + formula
C0h + formula	MAILBOX_MSG_STATUS_y	Number of messages in Mailbox y	31F8 80C0h + formula	31F8 90C0h + formula
100h + formula	MAILBOX_IRQ_STATUS_RAW_j	Raw status for each event for user j	31F8 8100h + formula	31F8 9100h + formula
104h + formula	MAILBOX_IRQ_STATUS_CLR_j	Masked status for each event for user j	31F8 8104h + formula	31F8 9104h + formula
108h + formula	MAILBOX_IRQ_ENABLE_SET_j	Set interrupt enables user j	31F8 8108h + formula	31F8 9108h + formula
10Ch + formula	MAILBOX_IRQ_ENABLE_CLR_j	Clear interrupt enables user j	31F8 810Ch + formula	31F8 910Ch + formula
140h	MAILBOX_IRQ_EOI	End of interrupt register	31F8 8140h	31F8 9140h

Table 1-7. Mailbox Registers 6

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_REGS10 Physical Address	NAVSS0_MAILBOX0_REGS11 Physical Address
0h	MAILBOX_REVISION	Peripheral ID register	31F8 A000h	31F8 B000h
10h	MAILBOX_SYSCONFIG	Mailbox control register	31F8 A010h	31F8 B010h
40h + formula	MAILBOX_MESSAGE_y	Message Mailbox y	31F8 A040h + formula	31F8 B040h + formula
80h + formula	MAILBOX_FIFO_STATUS_y	FIFO status for Mailbox y	31F8 A080h + formula	31F8 B080h + formula
C0h + formula	MAILBOX_MSG_STATUS_y	Number of messages in Mailbox y	31F8 A0C0h + formula	31F8 B0C0h + formula
100h + formula	MAILBOX_IRQ_STATUS_RAW_j	Raw status for each event for user j	31F8 A100h + formula	31F8 B100h + formula
104h + formula	MAILBOX_IRQ_STATUS_CLR_j	Masked status for each event for user j	31F8 A104h + formula	31F8 B104h + formula
108h + formula	MAILBOX_IRQ_ENABLE_SET_j	Set interrupt enables user j	31F8 A108h + formula	31F8 B108h + formula
10Ch + formula	MAILBOX_IRQ_ENABLE_CLR_j	Clear interrupt enables user j	31F8 A10Ch + formula	31F8 B10Ch + formula

Table 1-7. Mailbox Registers 6 (continued)

Offset	Acronym	Register Name	NAVSS0_MAILBOX0_ REGS10 Physical Address	NAVSS0_MAILBOX0_ REGS11 Physical Address
140h	MAILBOX_IRQ_EOI	End of interrupt register	31F8 A140h	31F8 B140h

1.1 MAILBOX_REVISION Register (Offset = 0h) [reset = Xh]

MAILBOX_REVISION is shown in [Figure 1-1](#) and described in [Table 1-9](#).

Return to [Summary Table](#).

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Reset = 66FC 7100h

Table 1-8. MAILBOX_REVISION Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0000h
NAVSS0_MAILBOX0_REGS1	31F8 1000h
NAVSS0_MAILBOX0_REGS2	31F8 2000h
NAVSS0_MAILBOX0_REGS3	31F8 3000h
NAVSS0_MAILBOX0_REGS4	31F8 4000h
NAVSS0_MAILBOX0_REGS5	31F8 5000h
NAVSS0_MAILBOX0_REGS6	31F8 6000h
NAVSS0_MAILBOX0_REGS7	31F8 7000h
NAVSS0_MAILBOX0_REGS8	31F8 8000h
NAVSS0_MAILBOX0_REGS9	31F8 9000h
NAVSS0_MAILBOX0_REGS10	31F8 A000h
NAVSS0_MAILBOX0_REGS11	31F8 B000h

Figure 1-1. MAILBOX_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNCTION									
R-1h				R-2h		R-6FCh									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_REV			CUSTOM		MINOR_REV					
R-Eh					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 1-9. MAILBOX_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used.
29-28	BU	R	2h	BU identifier
27-16	FUNCTION	R	6FCh	Module family.
15-11	RTL_VER	R	Eh	RTL version. R of X.Y.R.Z
10-8	MAJOR_REV	R	1h	Major revision. X of X.Y.R.Z
7-6	CUSTOM	R	0h	Special version number
5-0	MINOR_REV	R	0h	Minor revision. Y of X.Y.R.Z

1.2 MAILBOX_SYSCONFIG Register (Offset = 10h) [reset = X]

MAILBOX_SYSCONFIG is shown in [Figure 1-2](#) and described in [Table 1-11](#).

Return to [Summary Table](#).

This register contains parameters to control the whole Mailbox system. Provided for backwards compatibility with OMAP Mailbox. Only contains the soft reset.

Table 1-10. MAILBOX_SYSCONFIG Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0010h
NAVSS0_MAILBOX0_REGS1	31F8 1010h
NAVSS0_MAILBOX0_REGS2	31F8 2010h
NAVSS0_MAILBOX0_REGS3	31F8 3010h
NAVSS0_MAILBOX0_REGS4	31F8 4010h
NAVSS0_MAILBOX0_REGS5	31F8 5010h
NAVSS0_MAILBOX0_REGS6	31F8 6010h
NAVSS0_MAILBOX0_REGS7	31F8 7010h
NAVSS0_MAILBOX0_REGS8	31F8 8010h
NAVSS0_MAILBOX0_REGS9	31F8 9010h
NAVSS0_MAILBOX0_REGS10	31F8 A010h
NAVSS0_MAILBOX0_REGS11	31F8 B010h

Figure 1-2. MAILBOX_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							SOFT_RESET
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-11. MAILBOX_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	SOFT_RESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0. It has the same effect as the hardware reset. Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and empty all the mailboxes

1.3 MAILBOX_MESSAGE_y Register (Offset = 40h + formula) [reset = 0h]

MAILBOX_MESSAGE_y is shown in [Figure 1-3](#) and described in [Table 1-13](#).

Return to [Summary Table](#).

The message register stores the next to-be-read message of the mailbox. Read: Reads the next available message. Write: Add a message to this mailbox queue.

Offset = 40h + (y * 4h); where y = 0h to Fh

Table 1-12. MAILBOX_MESSAGE_y Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0040h + formula
NAVSS0_MAILBOX0_REGS1	31F8 1040h + formula
NAVSS0_MAILBOX0_REGS2	31F8 2040h + formula
NAVSS0_MAILBOX0_REGS3	31F8 3040h + formula
NAVSS0_MAILBOX0_REGS4	31F8 4040h + formula
NAVSS0_MAILBOX0_REGS5	31F8 5040h + formula
NAVSS0_MAILBOX0_REGS6	31F8 6040h + formula
NAVSS0_MAILBOX0_REGS7	31F8 7040h + formula
NAVSS0_MAILBOX0_REGS8	31F8 8040h + formula
NAVSS0_MAILBOX0_REGS9	31F8 9040h + formula
NAVSS0_MAILBOX0_REGS10	31F8 A040h + formula
NAVSS0_MAILBOX0_REGS11	31F8 B040h + formula

Figure 1-3. MAILBOX_MESSAGE_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-13. MAILBOX_MESSAGE_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALUE	R/W	0h	Message in Mailbox y

1.4 MAILBOX_FIFO_STATUS_y Register (Offset = 80h + formula) [reset = X]

MAILBOX_FIFO_STATUS_y is shown in [Figure 1-4](#) and described in [Table 1-15](#).

Return to [Summary Table](#).

The FIFO status register has the status of the Mailbox y FIFO

Offset = 80h + (y * 4h); where y = 0h to Fh

Table 1-14. MAILBOX_FIFO_STATUS_y Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0080h + formula
NAVSS0_MAILBOX0_REGS1	31F8 1080h + formula
NAVSS0_MAILBOX0_REGS2	31F8 2080h + formula
NAVSS0_MAILBOX0_REGS3	31F8 3080h + formula
NAVSS0_MAILBOX0_REGS4	31F8 4080h + formula
NAVSS0_MAILBOX0_REGS5	31F8 5080h + formula
NAVSS0_MAILBOX0_REGS6	31F8 6080h + formula
NAVSS0_MAILBOX0_REGS7	31F8 7080h + formula
NAVSS0_MAILBOX0_REGS8	31F8 8080h + formula
NAVSS0_MAILBOX0_REGS9	31F8 9080h + formula
NAVSS0_MAILBOX0_REGS10	31F8 A080h + formula
NAVSS0_MAILBOX0_REGS11	31F8 B080h + formula

Figure 1-4. MAILBOX_FIFO_STATUS_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							FULL
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 1-15. MAILBOX_FIFO_STATUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	FULL	R	0h	Full flag for Mailbox y

1.5 MAILBOX_MSG_STATUS_y Register (Offset = C0h + formula) [reset = X]

MAILBOX_MSG_STATUS_y is shown in [Figure 1-5](#) and described in [Table 1-17](#).

Return to [Summary Table](#).

The message status register has the status of the messages in Mailbox y

Offset = C0h + (y * 4h); where y = 0h to Fh

Table 1-16. MAILBOX_MSG_STATUS_y Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 00C0h + formula
NAVSS0_MAILBOX0_REGS1	31F8 10C0h + formula
NAVSS0_MAILBOX0_REGS2	31F8 20C0h + formula
NAVSS0_MAILBOX0_REGS3	31F8 30C0h + formula
NAVSS0_MAILBOX0_REGS4	31F8 40C0h + formula
NAVSS0_MAILBOX0_REGS5	31F8 50C0h + formula
NAVSS0_MAILBOX0_REGS6	31F8 60C0h + formula
NAVSS0_MAILBOX0_REGS7	31F8 70C0h + formula
NAVSS0_MAILBOX0_REGS8	31F8 80C0h + formula
NAVSS0_MAILBOX0_REGS9	31F8 90C0h + formula
NAVSS0_MAILBOX0_REGS10	31F8 A0C0h + formula
NAVSS0_MAILBOX0_REGS11	31F8 B0C0h + formula

Figure 1-5. MAILBOX_MSG_STATUS_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					NUM_MESSAGES		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 1-17. MAILBOX_MSG_STATUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2-0	NUM_MESSAGES	R	0h	Number of messages in Mailbox y

1.6 MAILBOX_IRQ_STATUS_RAW_j Register (Offset = 100h + formula) [reset = AAAAAAAAAh]

MAILBOX_IRQ_STATUS_RAW_j is shown in [Figure 1-6](#) and described in [Table 1-19](#).

Return to [Summary Table](#).

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user. Software may also write 1 to a given bit to set this bit to test interrupt generation. It will activate the status bit for two cycles. This may still be masked, however. Write 0 has no effect.

Offset = 100h + (j * 10h); where j = 0h to 3h

Table 1-18. MAILBOX_IRQ_STATUS_RAW_j Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0100h + formula
NAVSS0_MAILBOX0_REGS1	31F8 1100h + formula
NAVSS0_MAILBOX0_REGS2	31F8 2100h + formula
NAVSS0_MAILBOX0_REGS3	31F8 3100h + formula
NAVSS0_MAILBOX0_REGS4	31F8 4100h + formula
NAVSS0_MAILBOX0_REGS5	31F8 5100h + formula
NAVSS0_MAILBOX0_REGS6	31F8 6100h + formula
NAVSS0_MAILBOX0_REGS7	31F8 7100h + formula
NAVSS0_MAILBOX0_REGS8	31F8 8100h + formula
NAVSS0_MAILBOX0_REGS9	31F8 9100h + formula
NAVSS0_MAILBOX0_REGS10	31F8 A100h + formula
NAVSS0_MAILBOX0_REGS11	31F8 B100h + formula

Figure 1-6. MAILBOX_IRQ_STATUS_RAW_j Register

31	30	29	28	27	26	25	24
NOTFULLSTAT USMB15	NEWMSGSTAT USMB15	NOTFULLSTAT USMB14	NEWMSGSTAT USMB14	NOTFULLSTAT USMB13	NEWMSGSTAT USMB13	NOTFULLSTAT USMB12	NEWMSGSTAT USMB12
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h
23	22	21	20	19	18	17	16
NOTFULLSTAT USMB11	NEWMSGSTAT USMB11	NOTFULLSTAT USMB10	NEWMSGSTAT USMB10	NOTFULLSTAT USMB9	NEWMSGSTAT USMB9	NOTFULLSTAT USMB8	NEWMSGSTAT USMB8
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h
15	14	13	12	11	10	9	8
NOTFULLSTAT USMB7	NEWMSGSTAT USMB7	NOTFULLSTAT USMB6	NEWMSGSTAT USMB6	NOTFULLSTAT USMB5	NEWMSGSTAT USMB5	NOTFULLSTAT USMB4	NEWMSGSTAT USMB4
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h
7	6	5	4	3	2	1	0
NOTFULLSTAT USMB3	NEWMSGSTAT USMB3	NOTFULLSTAT USMB2	NEWMSGSTAT USMB2	NOTFULLSTAT USMB1	NEWMSGSTAT USMB1	NOTFULLSTAT USMB0	NEWMSGSTAT USMB0
R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-19. MAILBOX_IRQ_STATUS_RAW_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	1h	1 if Mailbox 15 is not full
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15
29	NOTFULLSTATUSMB14	R/W	1h	1 if Mailbox 14 is not full
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14

Table 1-19. MAILBOX_IRQ_STATUS_RAW_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NOTFULLSTATUSMB13	R/W	1h	1 if Mailbox 13 is not full
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13
25	NOTFULLSTATUSMB12	R/W	1h	1 if Mailbox 12 is not full
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12
23	NOTFULLSTATUSMB11	R/W	1h	1 if Mailbox 11 is not full
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11
21	NOTFULLSTATUSMB10	R/W	1h	1 if Mailbox 10 is not full
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10
19	NOTFULLSTATUSMB9	R/W	1h	1 if Mailbox 9 is not full
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9
17	NOTFULLSTATUSMB8	R/W	1h	1 if Mailbox 8 is not full
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8
15	NOTFULLSTATUSMB7	R/W	1h	1 if Mailbox 7 is not full
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7
13	NOTFULLSTATUSMB6	R/W	1h	1 if Mailbox 6 is not full
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6
11	NOTFULLSTATUSMB5	R/W	1h	1 if Mailbox 5 is not full
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5
9	NOTFULLSTATUSMB4	R/W	1h	1 if Mailbox 4 is not full
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4
7	NOTFULLSTATUSMB3	R/W	1h	1 if Mailbox 3 is not full
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3
5	NOTFULLSTATUSMB2	R/W	1h	1 if Mailbox 2 is not full
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2
3	NOTFULLSTATUSMB1	R/W	1h	1 if Mailbox 1 is not full
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1
1	NOTFULLSTATUSMB0	R/W	1h	1 if Mailbox 0 is not full
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0

1.7 MAILBOX_IRQ_STATUS_CLR_j Register (Offset = 104h + formula) [reset = 0h]

MAILBOX_IRQ_STATUS_CLR_j is shown in [Figure 1-7](#) and described in [Table 1-21](#).

Return to [Summary Table](#).

The interrupt status register has the status for each event that may be responsible for the generation of an interrupt to the corresponding user combined with the corresponding MASK information. Software may also write 1 to a given bit to clear this bit. However, if the hardware still has pending, enabled events, the interrupt will fire again in two cycles. Write 0 has no effect.

Offset = 104h + (j * 10h); where j = 0h to 3h

**Table 1-20. MAILBOX_IRQ_STATUS_CLR_j
Instances**

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0104h + formula
NAVSS0_MAILBOX0_REGS1	31F8 1104h + formula
NAVSS0_MAILBOX0_REGS2	31F8 2104h + formula
NAVSS0_MAILBOX0_REGS3	31F8 3104h + formula
NAVSS0_MAILBOX0_REGS4	31F8 4104h + formula
NAVSS0_MAILBOX0_REGS5	31F8 5104h + formula
NAVSS0_MAILBOX0_REGS6	31F8 6104h + formula
NAVSS0_MAILBOX0_REGS7	31F8 7104h + formula
NAVSS0_MAILBOX0_REGS8	31F8 8104h + formula
NAVSS0_MAILBOX0_REGS9	31F8 9104h + formula
NAVSS0_MAILBOX0_REGS10	31F8 A104h + formula
NAVSS0_MAILBOX0_REGS11	31F8 B104h + formula

Figure 1-7. MAILBOX_IRQ_STATUS_CLR_j Register

31	30	29	28	27	26	25	24
NOTFULLSTAT USMB15	NEWMSGSTAT USMB15	NOTFULLSTAT USMB14	NEWMSGSTAT USMB14	NOTFULLSTAT USMB13	NEWMSGSTAT USMB13	NOTFULLSTAT USMB12	NEWMSGSTAT USMB12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
NOTFULLSTAT USMB11	NEWMSGSTAT USMB11	NOTFULLSTAT USMB10	NEWMSGSTAT USMB10	NOTFULLSTAT USMB9	NEWMSGSTAT USMB9	NOTFULLSTAT USMB8	NEWMSGSTAT USMB8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
NOTFULLSTAT USMB7	NEWMSGSTAT USMB7	NOTFULLSTAT USMB6	NEWMSGSTAT USMB6	NOTFULLSTAT USMB5	NEWMSGSTAT USMB5	NOTFULLSTAT USMB4	NEWMSGSTAT USMB4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
NOTFULLSTAT USMB3	NEWMSGSTAT USMB3	NOTFULLSTAT USMB2	NEWMSGSTAT USMB2	NOTFULLSTAT USMB1	NEWMSGSTAT USMB1	NOTFULLSTAT USMB0	NEWMSGSTAT USMB0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-21. MAILBOX_IRQ_STATUS_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLSTATUSMB15	R/W	0h	1 if Mailbox 15 is not full and this interrupt bit is enabled
30	NEWMSGSTATUSMB15	R/W	0h	1 if there are messages present in Mailbox 15 and this interrupt bit is enabled

Table 1-21. MAILBOX_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	NOTFULLSTATUSMB14	R/W	0h	1 if Mailbox 14 is not full and this interrupt bit is enabled
28	NEWMSGSTATUSMB14	R/W	0h	1 if there are messages present in Mailbox 14 and this interrupt bit is enabled
27	NOTFULLSTATUSMB13	R/W	0h	1 if Mailbox 13 is not full and this interrupt bit is enabled
26	NEWMSGSTATUSMB13	R/W	0h	1 if there are messages present in Mailbox 13 and this interrupt bit is enabled
25	NOTFULLSTATUSMB12	R/W	0h	1 if Mailbox 12 is not full and this interrupt bit is enabled
24	NEWMSGSTATUSMB12	R/W	0h	1 if there are messages present in Mailbox 12 and this interrupt bit is enabled
23	NOTFULLSTATUSMB11	R/W	0h	1 if Mailbox 11 is not full and this interrupt bit is enabled
22	NEWMSGSTATUSMB11	R/W	0h	1 if there are messages present in Mailbox 11 and this interrupt bit is enabled
21	NOTFULLSTATUSMB10	R/W	0h	1 if Mailbox 10 is not full and this interrupt bit is enabled
20	NEWMSGSTATUSMB10	R/W	0h	1 if there are messages present in Mailbox 10 and this interrupt bit is enabled
19	NOTFULLSTATUSMB9	R/W	0h	1 if Mailbox 9 is not full and this interrupt bit is enabled
18	NEWMSGSTATUSMB9	R/W	0h	1 if there are messages present in Mailbox 9 and this interrupt bit is enabled
17	NOTFULLSTATUSMB8	R/W	0h	1 if Mailbox 8 is not full and this interrupt bit is enabled
16	NEWMSGSTATUSMB8	R/W	0h	1 if there are messages present in Mailbox 8 and this interrupt bit is enabled
15	NOTFULLSTATUSMB7	R/W	0h	1 if Mailbox 7 is not full and this interrupt bit is enabled
14	NEWMSGSTATUSMB7	R/W	0h	1 if there are messages present in Mailbox 7 and this interrupt bit is enabled
13	NOTFULLSTATUSMB6	R/W	0h	1 if Mailbox 6 is not full and this interrupt bit is enabled
12	NEWMSGSTATUSMB6	R/W	0h	1 if there are messages present in Mailbox 6 and this interrupt bit is enabled
11	NOTFULLSTATUSMB5	R/W	0h	1 if Mailbox 5 is not full and this interrupt bit is enabled
10	NEWMSGSTATUSMB5	R/W	0h	1 if there are messages present in Mailbox 5 and this interrupt bit is enabled
9	NOTFULLSTATUSMB4	R/W	0h	1 if Mailbox 4 is not full and this interrupt bit is enabled
8	NEWMSGSTATUSMB4	R/W	0h	1 if there are messages present in Mailbox 4 and this interrupt bit is enabled
7	NOTFULLSTATUSMB3	R/W	0h	1 if Mailbox 3 is not full and this interrupt bit is enabled
6	NEWMSGSTATUSMB3	R/W	0h	1 if there are messages present in Mailbox 3 and this interrupt bit is enabled
5	NOTFULLSTATUSMB2	R/W	0h	1 if Mailbox 2 is not full and this interrupt bit is enabled
4	NEWMSGSTATUSMB2	R/W	0h	1 if there are messages present in Mailbox 2 and this interrupt bit is enabled
3	NOTFULLSTATUSMB1	R/W	0h	1 if Mailbox 1 is not full and this interrupt bit is enabled
2	NEWMSGSTATUSMB1	R/W	0h	1 if there are messages present in Mailbox 1 and this interrupt bit is enabled
1	NOTFULLSTATUSMB0	R/W	0h	1 if Mailbox 0 is not full and this interrupt bit is enabled

Table 1-21. MAILBOX_IRQ_STATUS_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NEWMSGSTATUSMB0	R/W	0h	1 if there are messages present in Mailbox 0 and this interrupt bit is enabled

1.8 MAILBOX_IRQ_ENABLE_SET_j Register (Offset = 108h + formula) [reset = 0h]

MAILBOX_IRQ_ENABLE_SET_j is shown in [Figure 1-8](#) and described in [Table 1-23](#).

Return to [Summary Table](#).

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user j. Read value is the current enable bits for each interrupt source. Write 1 to a bit enables an interrupt source. Write 0 has no effect.

Offset = 108h + (j * 10h); where j = 0h to 3h

**Table 1-22. MAILBOX_IRQ_ENABLE_SET_j
Instances**

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0108h + formula
NAVSS0_MAILBOX0_REGS1	31F8 1108h + formula
NAVSS0_MAILBOX0_REGS2	31F8 2108h + formula
NAVSS0_MAILBOX0_REGS3	31F8 3108h + formula
NAVSS0_MAILBOX0_REGS4	31F8 4108h + formula
NAVSS0_MAILBOX0_REGS5	31F8 5108h + formula
NAVSS0_MAILBOX0_REGS6	31F8 6108h + formula
NAVSS0_MAILBOX0_REGS7	31F8 7108h + formula
NAVSS0_MAILBOX0_REGS8	31F8 8108h + formula
NAVSS0_MAILBOX0_REGS9	31F8 9108h + formula
NAVSS0_MAILBOX0_REGS10	31F8 A108h + formula
NAVSS0_MAILBOX0_REGS11	31F8 B108h + formula

Figure 1-8. MAILBOX_IRQ_ENABLE_SET_j Register

31	30	29	28	27	26	25	24
NOTFULLENA BLEMB15	NEWMSGENA BLEMB15	NOTFULLENA BLEMB14	NEWMSGENA BLEMB14	NOTFULLENA BLEMB13	NEWMSGENA BLEMB13	NOTFULLENA BLEMB12	NEWMSGENA BLEMB12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
NOTFULLENA BLEMB11	NEWMSGENA BLEMB11	NOTFULLENA BLEMB10	NEWMSGENA BLEMB10	NOTFULLENA BLEMB9	NEWMSGENA BLEMB9	NOTFULLENA BLEMB8	NEWMSGENA BLEMB8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
NOTFULLENA BLEMB7	NEWMSGENA BLEMB7	NOTFULLENA BLEMB6	NEWMSGENA BLEMB6	NOTFULLENA BLEMB5	NEWMSGENA BLEMB5	NOTFULLENA BLEMB4	NEWMSGENA BLEMB4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
NOTFULLENA BLEMB3	NEWMSGENA BLEMB3	NOTFULLENA BLEMB2	NEWMSGENA BLEMB2	NOTFULLENA BLEMB1	NEWMSGENA BLEMB1	NOTFULLENA BLEMB0	NEWMSGENA BLEMB0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-23. MAILBOX_IRQ_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
30	NEWMSGENABLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.

Table 1-23. MAILBOX_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.

Table 1-23. MAILBOX_IRQ_ENABLE_SET_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 enables the interrupt. Write 0 no action.

1.9 MAILBOX_IRQ_ENABLE_CLR_j Register (Offset = 10Ch + formula) [reset = 0h]

MAILBOX_IRQ_ENABLE_CLR_j is shown in [Figure 1-9](#) and described in [Table 1-25](#).

Return to [Summary Table](#).

The interrupt enable register allows software to mask/unmask the module internal source of interrupt for the user j. Read value is the current enable bits for each interrupt sourc. Write 1 to a bit disables an interrupt source. Write 0 has no effect.

Offset = 10Ch + (j * 10h); where j = 0h to 3h

**Table 1-24. MAILBOX_IRQ_ENABLE_CLR_j
Instances**

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 010Ch + formula
NAVSS0_MAILBOX0_REGS1	31F8 110Ch + formula
NAVSS0_MAILBOX0_REGS2	31F8 210Ch + formula
NAVSS0_MAILBOX0_REGS3	31F8 310Ch + formula
NAVSS0_MAILBOX0_REGS4	31F8 410Ch + formula
NAVSS0_MAILBOX0_REGS5	31F8 510Ch + formula
NAVSS0_MAILBOX0_REGS6	31F8 610Ch + formula
NAVSS0_MAILBOX0_REGS7	31F8 710Ch + formula
NAVSS0_MAILBOX0_REGS8	31F8 810Ch + formula
NAVSS0_MAILBOX0_REGS9	31F8 910Ch + formula
NAVSS0_MAILBOX0_REGS10	31F8 A10Ch + formula
NAVSS0_MAILBOX0_REGS11	31F8 B10Ch + formula

Figure 1-9. MAILBOX_IRQ_ENABLE_CLR_j Register

31	30	29	28	27	26	25	24
NOTFULLENA BLEMB15	NEWMSGENA BLEMB15	NOTFULLENA BLEMB14	NEWMSGENA BLEMB14	NOTFULLENA BLEMB13	NEWMSGENA BLEMB13	NOTFULLENA BLEMB12	NEWMSGENA BLEMB12
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
NOTFULLENA BLEMB11	NEWMSGENA BLEMB11	NOTFULLENA BLEMB10	NEWMSGENA BLEMB10	NOTFULLENA BLEMB9	NEWMSGENA BLEMB9	NOTFULLENA BLEMB8	NEWMSGENA BLEMB8
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
NOTFULLENA BLEMB7	NEWMSGENA BLEMB7	NOTFULLENA BLEMB6	NEWMSGENA BLEMB6	NOTFULLENA BLEMB5	NEWMSGENA BLEMB5	NOTFULLENA BLEMB4	NEWMSGENA BLEMB4
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
NOTFULLENA BLEMB3	NEWMSGENA BLEMB3	NOTFULLENA BLEMB2	NEWMSGENA BLEMB2	NOTFULLENA BLEMB1	NEWMSGENA BLEMB1	NOTFULLENA BLEMB0	NEWMSGENA BLEMB0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-25. MAILBOX_IRQ_ENABLE_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NOTFULLENA BLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
30	NEWMSGENA BLEMB15	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.

Table 1-25. MAILBOX_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	NOTFULLENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
28	NEWMSGENABLEMB14	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
27	NOTFULLENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
26	NEWMSGENABLEMB13	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
25	NOTFULLENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
24	NEWMSGENABLEMB12	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
23	NOTFULLENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
22	NEWMSGENABLEMB11	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
21	NOTFULLENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
20	NEWMSGENABLEMB10	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
19	NOTFULLENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
18	NEWMSGENABLEMB9	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
17	NOTFULLENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
16	NEWMSGENABLEMB8	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
15	NOTFULLENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
14	NEWMSGENABLEMB7	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
13	NOTFULLENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
12	NEWMSGENABLEMB6	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
11	NOTFULLENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.

Table 1-25. MAILBOX_IRQ_ENABLE_CLR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	NEWMSGENABLEMB5	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
9	NOTFULLENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
8	NEWMSGENABLEMB4	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
7	NOTFULLENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
6	NEWMSGENABLEMB3	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
5	NOTFULLENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
4	NEWMSGENABLEMB2	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
3	NOTFULLENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
2	NEWMSGENABLEMB1	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
1	NOTFULLENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.
0	NEWMSGENABLEMB0	R/W	0h	Read value is current enable state for this interrupt. Write 1 disables the interrupt. Write 0 no action.

1.10 MAILBOX_IRQ_EOI Register (Offset = 140h) [reset = X]

MAILBOX_IRQ_EOI is shown in [Figure 1-10](#) and described in [Table 1-27](#).

Return to [Summary Table](#).

This is the EOI register with which the software is enabled to do the interrupt clearance.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 1-26. MAILBOX_IRQ_EOI Instances

Instance	Physical Address
NAVSS0_MAILBOX0_REGS0	31F8 0140h
NAVSS0_MAILBOX0_REGS1	31F8 1140h
NAVSS0_MAILBOX0_REGS2	31F8 2140h
NAVSS0_MAILBOX0_REGS3	31F8 3140h
NAVSS0_MAILBOX0_REGS4	31F8 4140h
NAVSS0_MAILBOX0_REGS5	31F8 5140h
NAVSS0_MAILBOX0_REGS6	31F8 6140h
NAVSS0_MAILBOX0_REGS7	31F8 7140h
NAVSS0_MAILBOX0_REGS8	31F8 8140h
NAVSS0_MAILBOX0_REGS9	31F8 9140h
NAVSS0_MAILBOX0_REGS10	31F8 A140h
NAVSS0_MAILBOX0_REGS11	31F8 B140h

Figure 1-10. MAILBOX_IRQ_EOI Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED				EOI3	EOI2	EOI1	EOI0
W-X				W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 1-27. MAILBOX_IRQ_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	W	X	
3	EOI3	W	0h	Software EOI signal for the user 3 interrupt
2	EOI2	W	0h	Software EOI signal for the user 2 interrupt
1	EOI1	W	0h	Software EOI signal for the user 1 interrupt
0	EOI0	W	0h	Software EOI signal for the user 0 interrupt

2 Spinlock Registers

Table 2-2 lists the memory-mapped registers for the Spinlock. All register offset addresses not listed in Table 2-2 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. Spinlock Instances

Instance	Base Address
NAVSS0_SPINLOCK	30E0 0000h

Table 2-2. Spinlock Registers

Offset	Acronym	Register Name	NAVSS0_SPINLOCK Physical Address
0h	SPINLOCK_REVISION	Peripheral ID register	30E0 0000h
10h	SPINLOCK_SYSCONFIG	SpinLock top level configuration	30E0 0010h
14h	SPINLOCK_SYSTATUS	SpinLock top level status	30E0 0014h
800h + formula	SPINLOCK_LOCK_REG_y	Lock y register	30E0 0800h + formula

2.1 SPINLOCK_REVISION Register (Offset = 0h) [reset = Xh]

REVISION is shown in [Figure 2-1](#) and described in [Table 2-4](#).

Return to [Summary Table](#).

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Reset = 66FA 5100h

Table 2-3. SPINLOCK_REVISION Instances

Instance	Physical Address
NAVSS0_SPINLOCK	30E0 0000h

Figure 2-1. SPINLOCK_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		bu			FUNC										
R-1h			R-2h			R-6FAh									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R_RTL					X_MAJOR			CUSTOM		Y_MINOR					
R-Ah					R-1h			R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 2-4. SPINLOCK_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Used to distinguish which ID numbering scheme is used.
29-28	BU	R	2h	BU identifier
27-16	FUNC	R	6FAh	Module family.
15-11	R_RTL	R	Ah	RTL version.
10-8	X_MAJOR	R	1h	Major revision.
7-6	CUSTOM	R	0h	Special version number
5-0	Y_MINOR	R	0h	Minor revision.

2.2 SPINLOCK_SYSCONFIG Register (Offset = 10h) [reset = X]

SYSCONFIG is shown in [Figure 2-2](#) and described in [Table 2-6](#).

Return to [Summary Table](#).

Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock

Table 2-5. SPINLOCK_SYSCONFIG Instances

Instance	Physical Address
NAVSS0_SPINLOCK	30E0 0010h

Figure 2-2. SPINLOCK_SYSCONFIG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SOFTRESET	RESERVED
R/W-X						R/W-0h	R/W-X

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-6. SPINLOCK_SYSCONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SOFTRESET	R/W	0h	Module Software Reset The bit is automatically reset by the hardware. During reads, it always returns 0 It has the same effect as the hardware reset Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks
0	RESERVED	R/W	X	

2.3 SPINLOCK_SYSTATUS Register (Offset = 14h) [reset = X]

SYSTATUS is shown in [Figure 2-3](#) and described in [Table 2-8](#).

Return to [Summary Table](#).

Provides information about the Spinlock module

Table 2-7. SPINLOCK_SYSTATUS Instances

Instance	Physical Address
NAVSS0_SPINLOCK	30E0 0014h

Figure 2-3. SPINLOCK_SYSTATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NUMLOCKS								RESERVED							
R-8h								R-X							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								IU7	IU6	IU5	IU4	IU3	IU2	IU1	IU0
R-X								R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 2-8. SPINLOCK_SYSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	NUMLOCKS	R	8h	Module configuration parameter n, the total number of spinlocks divided by 32. e.g. For 256 spin locks, this will return the number 0x08
23-8	RESERVED	R	X	
7	IU7	R	0h	In-Use flag 7 covering lock registers 224 - 255. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 224 - 255 are in the Not Taken state Read 1 : At least one of the lock registers 224 - 255 are in the Taken state
6	IU6	R	0h	In-Use flag 6 covering lock registers 192 - 223. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 192 - 223 are in the Not Taken state Read 1 : At least one of the lock registers 192 - 223 are in the Taken state
5	IU5	R	0h	In-Use flag 5 covering lock registers 160 - 191. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 160 - 191 are in the Not Taken state Read 1 : At least one of the lock registers 160 - 191 are in the Taken state
4	IU4	R	0h	In-Use flag 4 covering lock registers 128 - 159. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 128 - 159 are in the Not Taken state Read 1 : At least one of the lock registers 128 - 159 are in the Taken state
3	IU3	R	0h	In-Use flag 3 covering lock registers 96 - 127. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 96 - 127 are in the Not Taken state Read 1 : At least one of the lock registers 96 - 127 are in the Taken state

Table 2-8. SPINLOCK_SYSTATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	IU2	R	0h	In-Use flag 2 covering lock registers 64 - 95. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 64 - 95 are in the Not Taken state Read 1 : At least one of the lock registers 64 - 95 are in the Taken state
1	IU1	R	0h	In-Use flag 1 covering lock registers 32 - 63. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 32 - 63 are in the Not Taken state Read 1 : At least one of the lock registers 32 - 63 are in the Taken state
0	IU0	R	0h	In-Use flag 0 covering lock registers 0 - 31. If no lock registers are implemented in this range, then this flag always reads as 0 Read 0 : All lock registers 0 - 31 are in the Not Taken state Read 1 : At least one of the lock registers 0 - 31 are in the Taken state

2.4 SPINLOCK_LOCK_REG_y Register (Offset = 800h + formula) [reset = X]

LOCK_REG_y is shown in [Figure 2-4](#) and described in [Table 2-10](#).

Return to [Summary Table](#).

The LOCK_REG_y register is read and written to perform lock and unlock operations on lock 'y'

Offset = 30E00800h + (y * 4h); where y = 0h to FFh

Table 2-9. SPINLOCK_LOCK_REG_y Instances

Instance	Physical Address
NAVSS0_SPINLOCK	30E0 0800h + formula

Figure 2-4. SPINLOCK_LOCK_REG_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TAKEN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-10. SPINLOCK_LOCK_REG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TAKEN	R/W	0h	Lock Status Read 0 : Lock was previously free. The reader now has been granted the lock. Read 1 : Lock was previously taken. The reader has not been granted the lock and must retry. Write 0 : Free the lock by setting TAKEN to zero. Write 1 : No effect

3 MSMC Registers

Table 3-2 lists the memory-mapped registers for the MSMC. All register offset addresses not listed in Table 3-2 should be considered as reserved locations and the register contents should not be modified.

Note

The MSMC configuration space supports 1-, 2-, 4- and 8-byte aligned reads and 4- and 8-byte aligned writes.

Table 3-1. MSMC Instances

Instance	Base Address
COMPUTE_CLUSTER0_MSMC_CFGS0	6E00 0000h

Table 3-2. MSMC Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_MSMC_CFGS0 Physical Address
0h	MSMC_PID	Peripheral ID Register	6E00 0000h
1000h	MSMC_CACHE_CTRL	Cache Control Register	6E00 1000h
1010h	MSMC_RT_WAY_SELECT	Real Time Way Select	6E00 1010h
1018h	MSMC_NRT_WAY_SELECT	Non Real Time Way Select	6E00 1018h
2048h	MSMC_COHCTRL	Coherence Control Register	6E00 2048h
3080h	MSMC_SMEDCC	Scrub Rate Register	6E00 3080h
5000h	MSMC_SMESTAT	Interrupt Enabled Status register	6E00 5000h
5008h	MSMC_SMIRSTAT	Interrupt raw status register	6E00 5008h
5008h	MSMC_SMIRWS	Set interrupt raw status register	6E00 5008h
5010h	MSMC_SMIRC	Interrupt clear register	6E00 5010h
5018h	MSMC_SMIESTAT	Interrupt raw status register	6E00 5018h
5018h	MSMC_SMIEWS	Set interrupt raw status register	6E00 5018h
5020h	MSMC_SMIEC	Interrupt clear register	6E00 5020h
6000h	MSMC_SBNDCOH0	Starvation Bound for Coherent Port 0	6E00 6000h
6008h	MSMC_SBNDCOH1	Starvation Bound for Coherent Port 1. Not used on this device.	6E00 6008h
6010h	MSMC_SBNDCOH2	Starvation Bound for Coherent Port 2. Not used on this device.	6E00 6010h
6018h	MSMC_SBNDCOH3	Starvation Bound for Coherent Port 3. Not used on this device.	6E00 6018h
6020h	MSMC_SBNDCOH4	Starvation Bound for Coherent Port 4	6E00 6020h
6028h	MSMC_SBNDCOH5	Starvation Bound for Coherent Port 5. Not used on this device.	6E00 6028h
6030h	MSMC_SBNDCOH6	Starvation Bound for Coherent Port 6. Not used on this device.	6E00 6030h
6038h	MSMC_SBNDCOH7	Starvation Bound for Coherent Port 7. Not used on this device.	6E00 6038h
6040h	MSMC_SBNDCOH8	Starvation Bound for Coherent Port 8. Not used on this device.	6E00 6040h
6048h	MSMC_SBNDCOH9	Starvation Bound for Coherent Port 9. Not used on this device.	6E00 6048h
6050h	MSMC_SBNDCOH10	Starvation Bound for Coherent Port 10. Not used on this device.	6E00 6050h
6058h	MSMC_SBNDCOH11	Starvation Bound for Coherent Port 11	6E00 6058h
6060h	MSMC_SBNDCOH12	Starvation Bound for Coherent Port 12	6E00 6060h
6100h	MSMC_SBNDDRU	Starvation Bound for Data Routing Unit	6E00 6100h

Table 3-2. MSMC Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0 _MSMC_CFGS0 Physical Address
6200h	MSMC_SBNDRESP	Starvation Bound for Read Response	6E00 6200h
7000h	MSMC_DBGTAGCTL	Debug Tag View Control	6E00 7000h
7080h	MSMC_DBGTAGVIEW	Debug Tag View Read	6E00 7080h
A000h	MSMC_NULL_SLV_STAT0	Null Slave Status 0	6E00 A000h
A008h	MSMC_NULL_SLV_STAT1	Null Slave Status 1	6E00 A008h
A018h	MSMC_NULL_SLV_CNT	Null Slave Error Count	6E00 A018h

3.1 MSMC_PID Register (Offset = 0h) [reset = 60240000h]

MSMC_PID is shown in [Figure 3-1](#) and described in [Table 3-4](#).

Return to [Summary Table](#).

Peripheral ID Register.

Table 3-3. MSMC_PID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 0000h

Figure 3-1. MSMC_PID Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																															
R-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-60240000h																															

LEGEND: R = Read Only; -n = value after reset

Table 3-4. MSMC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R	0h	Reserved
31-0	REVISION	R	60240000h	PID Revision

3.2 MSMC_CACHE_CTRL Register (Offset = 1000h) [reset = 0h]

MSMC_CACHE_CTRL is shown in [Figure 3-2](#) and described in [Table 3-6](#).

Return to [Summary Table](#).

Cache Control Register.

Table 3-5. MSMC_CACHE_CTRL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 1000h

Figure 3-2. MSMC_CACHE_CTRL Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					ALLOCATION_ POLICY	RESERVED	REPLACEM T_POLICY
R-0h					RW-0h	R-0h	RW-0h
7	6	5	4	3	2	1	0
RESERVED			SZ_TRANSITIO N	CACHE_SIZE			
R-0h			R-0h	RW-0h			

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-6. MSMC_CACHE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
63-11	RESERVED	R	0h	Reserved
10	ALLOCATION_POLICY	RW	0h	Allocation Policy
9	RESERVED	R	0h	Reserved
8	REPLACEMENT_POLICY	RW	0h	Replacement Policy
7-5	RESERVED	R	0h	Reserved

Table 3-6. MSMC_CACHE_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SZ_TRANSITION	R	0h	Cache Size Change in Progress
3-0	CACHE_SIZE	RW	0h	Cache Size Control

3.3 MSMC_RT_WAY_SELECT Register (Offset = 1010h) [reset = 3h]

MSMC_RT_WAY_SELECT is shown in [Figure 3-3](#) and described in [Table 3-8](#).

Return to [Summary Table](#).

Real Time Way Select.

Table 3-7. MSMC_RT_WAY_SELECT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 1010h

Figure 3-3. MSMC_RT_WAY_SELECT Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	OR_MASK		RESERVED			AND_MASK	
R-0h	RW-0h		R-0h			RW-3h	

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-8. MSMC_RT_WAY_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
63-7	RESERVED	R	0h	Reserved
6-5	OR_MASK	RW	0h	OR mask for way-select
4-2	RESERVED	R	0h	Reserved
1-0	AND_MASK	RW	3h	AND mask for way-select

3.4 MSMC_NRT_WAY_SELECT Register (Offset = 1018h) [reset = 3h]

MSMC_NRT_WAY_SELECT is shown in [Figure 3-4](#) and described in [Table 3-10](#).

Return to [Summary Table](#).

Non Real Time Way Select.

Table 3-9. MSMC_NRT_WAY_SELECT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 1018h

Figure 3-4. MSMC_NRT_WAY_SELECT Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	OR_MASK		RESERVED			AND_MASK	
R-0h	RW-0h		R-0h			RW-3h	

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-10. MSMC_NRT_WAY_SELECT Register Field Descriptions

Bit	Field	Type	Reset	Description
63-7	RESERVED	R	0h	Reserved
6-5	OR_MASK	RW	0h	OR mask for way-select
4-2	RESERVED	R	0h	Reserved
1-0	AND_MASK	RW	3h	AND mask for way-select

3.5 MSMC_COHCTRL Register (Offset = 2048h) [reset = 0h]

MSMC_COHCTRL is shown in [Figure 3-5](#) and described in [Table 3-12](#).

Return to [Summary Table](#).

Coherence Control Register.

Table 3-11. MSMC_COHCTRL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 2048h

Figure 3-5. MSMC_COHCTRL Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							BCM
R-0h							RW-0h

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-12. MSMC_COHCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	BCM	RW	0h	Broadcast Mode

3.6 MSMC_SMEDCC Register (Offset = 3080h) [reset = 80000000h]

MSMC_SMEDCC is shown in [Figure 3-6](#) and described in [Table 3-14](#).

Return to [Summary Table](#).

Scrub Rate Register.

Table 3-13. MSMC_SMEDCC Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 3080h

Figure 3-6. MSMC_SMEDCC Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
SEN	RESERVED						
RW-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
REFDEL							
RW-0h							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-14. MSMC_SMEDCC Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R	0h	Reserved
31	SEN	RW	1h	Scrub Engine Enable
30-8	RESERVED	R	0h	Reserved
7-0	REFDEL	RW	0h	Number of Clock Cycles Between Scrubs

3.7 MSMC_SMESTAT Register (Offset = 5000h) [reset = 0h]

MSMC_SMESTAT is shown in [Figure 3-7](#) and described in [Table 3-16](#).

Return to [Summary Table](#).

Interrupt Enabled Status register. ANDed value of MSMC_SMIRSTAT and MSMC_SMIESTAT.

Table 3-15. MSMC_SMESTAT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5000h

Figure 3-7. MSMC_SMESTAT Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 3-16. MSMC_SMESTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	R	0h	Null slave error is enabled and pending

3.8 MSMC_SMIRSTAT Register (Offset = 5008h) [reset = 0h]

MSMC_SMIRSTAT is shown in [Figure 3-8](#) and described in [Table 3-18](#).

Return to [Summary Table](#).

Interrupt raw status register.

Table 3-17. MSMC_SMIRSTAT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5008h

Figure 3-8. MSMC_SMIRSTAT Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 3-18. MSMC_SMIRSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	R	0h	Null slave error flagged

3.9 MSMC_SMIRWS Register (Offset = 5008h) [reset = 0h]

MSMC_SMIRWS is shown in [Figure 3-9](#) and described in [Table 3-20](#).

Return to [Summary Table](#).

Set interrupt raw status register.

Table 3-19. MSMC_SMIRWS Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5008h

Figure 3-9. MSMC_SMIRWS Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 3-20. MSMC_SMIRWS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	W	0h	Set software null slave error

3.10 MSMC_SMIRC Register (Offset = 5010h) [reset = 0h]

MSMC_SMIRC is shown in [Figure 3-10](#) and described in [Table 3-22](#).

Return to [Summary Table](#).

Interrupt clear register.

Table 3-21. MSMC_SMIRC Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5010h

Figure 3-10. MSMC_SMIRC Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 3-22. MSMC_SMIRC Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	W	0h	Clear null slave error flag

3.11 MSMC_SMIESTAT Register (Offset = 5018h) [reset = 0h]

MSMC_SMIESTAT is shown in [Figure 3-11](#) and described in [Table 3-24](#).

Return to [Summary Table](#).

Interrupt raw status register.

Table 3-23. MSMC_SMIESTAT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5018h

Figure 3-11. MSMC_SMIESTAT Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 3-24. MSMC_SMIESTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	R	0h	Null slave error interrupt is enabled

3.12 MSMC_SMIEWS Register (Offset = 5018h) [reset = 0h]

MSMC_SMIEWS is shown in [Figure 3-12](#) and described in [Table 3-26](#).

Return to [Summary Table](#).

Set interrupt raw status register.

Table 3-25. MSMC_SMIEWS Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5018h

Figure 3-12. MSMC_SMIEWS Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 3-26. MSMC_SMIEWS Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	W	0h	Enable null slave error

3.13 MSMC_SMIEC Register (Offset = 5020h) [reset = 0h]

MSMC_SMIEC is shown in [Figure 3-13](#) and described in [Table 3-28](#).

Return to [Summary Table](#).

Interrupt clear register.

Table 3-27. MSMC_SMIEC Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 5020h

Figure 3-13. MSMC_SMIEC Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							NULL_SLV
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 3-28. MSMC_SMIEC Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RESERVED	R	0h	Reserved
0	NULL_SLV	W	0h	clear null slave error interrupt enable

3.14 MSMC_SBNDCOH0 Register (Offset = 6000h) [reset = 3F003F003F003Fh]

MSMC_SBNDCOH0 is shown in [Figure 3-14](#) and described in [Table 3-30](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 0.

Table 3-29. MSMC_SBNDCOH0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6000h

Figure 3-14. MSMC_SBNDCOH0 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-30. MSMC_SBNDCOH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-30. MSMC_SBNDCOH0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.15 MSMC_SBNDCOH1 Register (Offset = 6008h) [reset = 3F003F003F0h]

MSMC_SBNDCOH1 is shown in [Figure 3-15](#) and described in [Table 3-32](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 1. Not used on this device.

Table 3-31. MSMC_SBNDCOH1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6008h

Figure 3-15. MSMC_SBNDCOH1 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-32. MSMC_SBNDCOH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-32. MSMC_SBNDCOH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.16 MSMC_SBNDCOH2 Register (Offset = 6010h) [reset = 3F003F003F0h]

MSMC_SBNDCOH2 is shown in [Figure 3-16](#) and described in [Table 3-34](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 2. Not used on this device.

Table 3-33. MSMC_SBNDCOH2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6010h

Figure 3-16. MSMC_SBNDCOH2 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-34. MSMC_SBNDCOH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-34. MSMC_SBNDCH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.17 MSMC_SBNDCOH3 Register (Offset = 6018h) [reset = 3F003F003F003Fh]

MSMC_SBNDCOH3 is shown in [Figure 3-17](#) and described in [Table 3-36](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 3. Not used on this device.

Table 3-35. MSMC_SBNDCOH3 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-17. MSMC_SBNDCOH3 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-36. MSMC_SBNDCOH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-36. MSMC_SBNDCOH3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.18 MSMC_SBNDCOH4 Register (Offset = 6018h) [reset = 3F003F003F003Fh]

MSMC_SBNDCOH4 is shown in [Figure 3-18](#) and described in [Table 3-38](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 4.

Table 3-37. MSMC_SBNDCOH4 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-18. MSMC_SBNDCOH4 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-38. MSMC_SBNDCOH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-38. MSMC_SBNDCH4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.19 MSMC_SBNDCOH5 Register (Offset = 6018h) [reset = 3F003F003F003Fh]

MSMC_SBNDCOH5 is shown in [Figure 3-19](#) and described in [Table 3-40](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 5. Not used on this device.

Table 3-39. MSMC_SBNDCOH5 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-19. MSMC_SBNDCOH5 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-40. MSMC_SBNDCOH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-40. MSMC_SBNDCH5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.20 MSMC_SBNDCOH6 Register (Offset = 6018h) [reset = 3F003F003F0h]

MSMC_SBNDCOH6 is shown in [Figure 3-20](#) and described in [Table 3-42](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 6. Not used on this device.

Table 3-41. MSMC_SBNDCOH6 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-20. MSMC_SBNDCOH6 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-42. MSMC_SBNDCOH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-42. MSMC_SBNDCH6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.21 MSMC_SBNDCOH7 Register (Offset = 6018h) [reset = 3F003F003F0h]

MSMC_SBNDCOH7 is shown in [Figure 3-21](#) and described in [Table 3-44](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 7. Not used on this device.

Table 3-43. MSMC_SBNDCOH7 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-21. MSMC_SBNDCOH7 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-44. MSMC_SBNDCOH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-44. MSMC_SBND7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.22 MSMC_SBNDCOH8 Register (Offset = 6018h) [reset = 3F003F003F0h]

MSMC_SBNDCOH8 is shown in [Figure 3-22](#) and described in [Table 3-46](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 8. Not used on this device.

Table 3-45. MSMC_SBNDCOH8 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-22. MSMC_SBNDCOH8 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-46. MSMC_SBNDCOH8 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-46. MSMC_SBNDCOH8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.23 MSMC_SBNDCOH9 Register (Offset = 6018h) [reset = 3F003F003F0h]

MSMC_SBNDCOH9 is shown in [Figure 3-23](#) and described in [Table 3-48](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 9. Not used on this device.

Table 3-47. MSMC_SBNDCOH9 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-23. MSMC_SBNDCOH9 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-48. MSMC_SBNDCOH9 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-48. MSMC_SBNDCOH9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.24 MSMC_SBNDCOH10 Register (Offset = 6018h) [reset = 3F003F003Fh]

MSMC_SBNDCOH10 is shown in [Figure 3-24](#) and described in [Table 3-50](#).

Return to [Summary Table](#).

Starvation Bound for Coherent Port 10. Not used on this device.

Table 3-49. MSMC_SBNDCOH10 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-24. MSMC_SBNDCOH10 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-50. MSMC_SBNDCOH10 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-50. MSMC_SBNDCOH10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.25 MSMC_SBNDCOH11 Register (Offset = 6018h) [reset = 3F003F003Fh]

MSMC_SBNDCOH11 is shown in [Figure 3-25](#) and described in [Table 3-52](#).

[Return to Summary Table.](#)

Starvation Bound for Coherent Port 11.

Table 3-51. MSMC_SBNDCOH11 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-25. MSMC_SBNDCOH11 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-52. MSMC_SBNDCOH11 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-52. MSMC_SBNDCOH11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.26 MSMC_SBNDCOH12 Register (Offset = 6018h) [reset = 3F003F003Fh]

MSMC_SBNDCOH12 is shown in [Figure 3-26](#) and described in [Table 3-54](#).

[Return to Summary Table.](#)

Starvation Bound for Coherent Port 12.

Table 3-53. MSMC_SBNDCOH12 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6018h

Figure 3-26. MSMC_SBNDCOH12 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-54. MSMC_SBNDCOH12 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-54. MSMC_SBNDCOH12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.27 MSMC_SBNDDRU Register (Offset = 6100h) [reset = 3F003F003Fh]

MSMC_SBNDDRU is shown in [Figure 3-27](#) and described in [Table 3-56](#).

Return to [Summary Table](#).

Starvation Bound for Data Routing Unit.

Table 3-55. MSMC_SBNDDRU Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6100h

Figure 3-27. MSMC_SBNDDRU Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-56. MSMC_SBNDDRU Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-56. MSMC_SBNDDRU Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.28 MSMC_SBNDRSP Register (Offset = 6200h) [reset = 3F003F003F0h]

MSMC_SBNDRSP is shown in [Figure 3-28](#) and described in [Table 3-58](#).

Return to [Summary Table](#).

Starvation Bound for Read Response.

Table 3-57. MSMC_SBNDRSP Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 6200h

Figure 3-28. MSMC_SBNDRSP Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
SBNDE_RT							
RW-3Fh							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
SBNDM_RT							
RW-3Fh							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SBNDE_NRT							
RW-3Fh							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SBNDM_NRT							
RW-3Fh							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-58. MSMC_SBNDRSP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	RESERVED	R	0h	Reserved
55-48	SBNDE_RT	RW	3Fh	Starvation Bound for Real-Time External Memory
47-40	RESERVED	R	0h	Reserved
39-32	SBNDM_RT	RW	3Fh	Starvation Bound for Real-Time On-Chip Memory
31-24	RESERVED	R	0h	Reserved
23-16	SBNDE_NRT	RW	3Fh	Starvation Bound for Non-Real-Time External Memory
15-8	RESERVED	R	0h	Reserved

Table 3-58. MSMC_SBNDRSP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	SBNDM_NRT	RW	3Fh	Starvation Bound for Non-Real-Time On-Chip Memory

3.29 MSMC_DBGTAGCTL Register (Offset = 7000h) [reset = 0h]

MSMC_DBGTAGCTL is shown in [Figure 3-29](#) and described in [Table 3-60](#).

Return to [Summary Table](#).

Debug Tag View Control.

Table 3-59. MSMC_DBGTAGCTL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 7000h

Figure 3-29. MSMC_DBGTAGCTL Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							L3CACHE
R-0h							RW-0h
39	38	37	36	35	34	33	32
RESERVED						BANK	
R-0h						RW-0h	
31	30	29	28	27	26	25	24
RESERVED		INDEX					
R-0h		RW-0h					
23	22	21	20	19	18	17	16
INDEX							
RW-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			WAY				
R-0h			RW-0h				

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-60. MSMC_DBGTAGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
63-41	RESERVED	R	0h	Reserved
40	L3CACHE	RW	0h	Level 3 Cache Tag Select
39-34	RESERVED	R	0h	Reserved
33-32	BANK	RW	0h	Physical Bank Select
31-30	RESERVED	R	0h	Reserved
29-16	INDEX	RW	0h	Index Select
15-5	RESERVED	R	0h	Reserved

Table 3-60. MSMC_DBGTAGCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	WAY	RW	0h	Way Select

3.30 MSMC_DBGTAGVIEW Register (Offset = 7080h) [reset = 0h]

MSMC_DBGTAGVIEW is shown in [Figure 3-30](#) and described in [Table 3-62](#).

Return to [Summary Table](#).

Debug Tag View Read.

Table 3-61. MSMC_DBGTAGVIEW Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 7080h

Figure 3-30. MSMC_DBGTAGVIEW Register

63	62	61	60	59	58	57	56
RESERVED					SF		
R-0h					R-0h		
55	54	53	52	51	50	49	48
SF		RESERVED	DIRTY	RESERVED	DATA_VALID	RESERVED	ADDR_VALID
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
47	46	45	44	43	42	41	40
ADDRESS							
R-0h							
39	38	37	36	35	34	33	32
ADDRESS							
R-0h							
31	30	29	28	27	26	25	24
ADDRESS							
R-0h							
23	22	21	20	19	18	17	16
ADDRESS							
R-0h							
15	14	13	12	11	10	9	8
ADDRESS							
R-0h							
7	6	5	4	3	2	1	0
ADDRESS							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 3-62. MSMC_DBGTAGVIEW Register Field Descriptions

Bit	Field	Type	Reset	Description
63-59	RESERVED	R	0h	Reserved
58-54	SF	R	0h	Snoop Filter
53	RESERVED	R	0h	Reserved
52	DIRTY	R	0h	Dirty
51	RESERVED	R	0h	Reserved
50	DATA_VALID	R	0h	Data Valid
49	RESERVED	R	0h	Reserved

Table 3-62. MSMC_DBGTAGVIEW Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
48	ADDR_VALID	R	0h	Address Valid
47-0	ADDRESS	R	0h	Tag Address

3.31 MSMC_NULL_SLV_STAT0 Register (Offset = A000h) [reset = 0h]

MSMC_NULL_SLV_STAT0 is shown in [Figure 3-31](#) and described in [Table 3-64](#).

Return to [Summary Table](#).

Null Slave Status 0.

Table 3-63. MSMC_NULL_SLV_STAT0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 A000h

Figure 3-31. MSMC_NULL_SLV_STAT0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 3-64. MSMC_NULL_SLV_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ADDR	R	0h	Address

3.32 MSMC_NULL_SLV_STAT1 Register (Offset = A008h) [reset = 0h]

MSMC_NULL_SLV_STAT1 is shown in [Figure 3-32](#) and described in [Table 3-66](#).

Return to [Summary Table](#).

Null Slave Status 1.

Table 3-65. MSMC_NULL_SLV_STAT1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 A008h

Figure 3-32. MSMC_NULL_SLV_STAT1 Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED		PRIV		RESERVED		SECURE	
R-0h		R-0h		R-0h		R-0h	
47	46	45	44	43	42	41	40
RESERVED			EMU	RESERVED		MEMTYPE	
R-0h			R-0h	R-0h		R-0h	
39	38	37	36	35	34	33	32
RESERVED		OPCODE					
R-0h		R-0h					
31	30	29	28	27	26	25	24
PRIVID							
R-0h							
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
ROUTEID				RESERVED		BYTECNT	
R-0h				R-0h		R-0h	
7	6	5	4	3	2	1	0
BYTECNT							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 3-66. MSMC_NULL_SLV_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-54	RESERVED	R	0h	Reserved
53-52	PRIV	R	0h	Privilege
51-49	RESERVED	R	0h	Reserved
48	SECURE	R	0h	Secure
47-45	RESERVED	R	0h	Reserved
44	EMU	R	0h	Emulation
43-42	RESERVED	R	0h	Reserved

Table 3-66. MSMC_NULL_SLV_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
41-40	MEMTYPE	R	0h	Memory Type
39-38	RESERVED	R	0h	Reserved
37-32	OPCODE	R	0h	Opcode
31-24	PRIVID	R	0h	Priv ID
23-12	ROUTEID	R	0h	Route ID
11-10	RESERVED	R	0h	Reserved
9-0	BYTECNT	R	0h	Byte Count

3.33 MSMC_NULL_SLV_CNT Register (Offset = A018h) [reset = 0h]

MSMC_NULL_SLV_CNT is shown in [Figure 3-33](#) and described in [Table 3-68](#).

Return to [Summary Table](#).

Null Slave Error Count.

Table 3-67. MSMC_NULL_SLV_CNT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MSMC_CFGS 0	6E00 A018h

Figure 3-33. MSMC_NULL_SLV_CNT Register

63	62	61	60	59	58	57	56
RESERVED							
R-0h							
55	54	53	52	51	50	49	48
RESERVED							
R-0h							
47	46	45	44	43	42	41	40
RESERVED							
R-0h							
39	38	37	36	35	34	33	32
RESERVED							
R-0h							
31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
COUNT							
RW-0h							

LEGEND: R = Read Only; RW = Read/Write; -n = value after reset

Table 3-68. MSMC_NULL_SLV_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
63-8	RESERVED	R	0h	Reserved
7-0	COUNT	RW	0h	Count

4 DDRSS Registers

4.1 DDR Subsystem Registers

Table 4-2 lists the memory-mapped registers for the DDR subsystem. All register offset addresses not listed in Table 4-2 should be considered as reserved locations and the register contents should not be modified.

Table 4-1. DDR Subsystem Instances

Instance	Base Address
COMPUTE_CLUSTER0_SS_CFG	0298 0000h

Table 4-2. DDR Subsystem Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_SS_CFG Physical Address
0h	DDRSS_SS_ID_REV_REG	Subsystem Revision Register	0298 0000h
4h	DDRSS_SS_CTL_REG	Subsystem Control Register	0298 0004h
20h	DDRSS_V2A_CTL_REG	MSMC2DDR Bridge Control Register	0298 0020h
24h	DDRSS_V2A_R1_MAT_REG	MSMC2DDR Bridge Range 1 Match Register	0298 0024h
28h	DDRSS_V2A_R2_MAT_REG	MSMC2DDR Bridge Range 2 Match Register	0298 0028h
2Ch	DDRSS_V2A_R3_MAT_REG	MSMC2DDR Bridge Range 3 Match Register	0298 002Ch
30h	DDRSS_V2A_LPT_DEF_PRI_MAP_REG	MSMC2DDR Bridge LPT Default Priority Mapping Register	0298 0030h
34h	DDRSS_V2A_LPT_R1_PRI_MAP_REG	MSMC2DDR Bridge LPT Range 1 Priority Map Register	0298 0034h
38h	DDRSS_V2A_LPT_R2_PRI_MAP_REG	MSMC2DDR Bridge LPT Range 2 Priority Map Register	0298 0038h
3Ch	DDRSS_V2A_LPT_R3_PRI_MAP_REG	MSMC2DDR Bridge LPT Range 3 Priority Map Register	0298 003Ch
4Ch	DDRSS_V2A_HPT_DEF_PRI_MAP_REG	MSMC2DDR Bridge HPT Default Priority Mapping Register	0298 004Ch
50h	DDRSS_V2A_HPT_R1_PRI_MAP_REG	MSMC2DDR Bridge HPT Range 1 Priority Map Register	0298 0050h
54h	DDRSS_V2A_HPT_R2_PRI_MAP_REG	MSMC2DDR Bridge HPT Range 2 Priority Map Register	0298 0054h
58h	DDRSS_V2A_HPT_R3_PRI_MAP_REG	MSMC2DDR Bridge HPT Range 3 Priority Map Register	0298 0058h
70h	DDRSS_V2A_AERR_LOG1_REG	MSMC2DDR Bridge Address Error Log 1 Register	0298 0070h
74h	DDRSS_V2A_AERR_LOG2_REG	MSMC2DDR Bridge Address Error Log 2 Register	0298 0074h
78h	DDRSS_V2A_OERR_LOG_REG	MSMC2DDR Bridge Opcode Error Log Register	0298 0078h
80h	DDRSS_V2A_1B_ERR_CNT_REG	MSMC2DDR Bridge 1-Bit EDC Error Count Register	0298 0080h
84h	DDRSS_V2A_1B_ERR_LOG1_REG	MSMC2DDR Bridge 1-Bit EDC Error Log 1 Register	0298 0084h
88h	DDRSS_V2A_1B_ERR_LOG2_REG	MSMC2DDR Bridge 1-Bit EDC Error Log 2 Register	0298 0088h
8Ch	DDRSS_V2A_2B_ERR_LOG1_REG	MSMC2DDR Bridge 2-Bit EDC Error Log 1 Register	0298 008Ch
90h	DDRSS_V2A_2B_ERR_LOG2_REG	MSMC2DDR Bridge 2-Bit EDC Error Log 2 Register	0298 0090h
9Ch	DDRSS_V2A_BUS_TO	MSMC2DDR Bridge Bus Timeout Register	0298 009Ch
A0h	DDRSS_V2A_INT_RAW_REG	MSMC2DDR Bridge Interrupt Raw Status Register	0298 00A0h
A4h	DDRSS_V2A_INT_STAT_REG	MSMC2DDR Bridge Interrupt Status Register	0298 00A4h
A8h	DDRSS_V2A_INT_SET_REG	MSMC2DDR Bridge Interrupt Enable Set Register	0298 00A8h

Table 4-2. DDR Subsystem Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_SS_CFG Physical Address
ACh	DDRSS_V2A_INT_CLR_REG	MSMC2DDR Bridge Interrupt Enable Clear Register	0298 00ACh
B0h	DDRSS_V2A_EOI_REG	MSMC2DDR Bridge End of Interrupt Register	0298 00B0h
100h	DDRSS_PERF_CNT_SEL_REG	Performance Counter Select Register	0298 0100h
104h	DDRSS_PERF_CNT1_REG	Performance Counter 1 Register	0298 0104h
108h	DDRSS_PERF_CNT2_REG	Performance Counter 2 Register	0298 0108h
10Ch	DDRSS_PERF_CNT3_REG	Performance Counter 3 Register	0298 010Ch
110h	DDRSS_PERF_CNT4_REG	Performance Counter 4 Register	0298 0110h
120h	DDRSS_ECC_CTRL_REG	ECC Control Register	0298 0120h
124h	DDRSS_ECC_RID_INDX_REG	ECC Cache RouteID Index Register	0298 0124h
128h	DDRSS_ECC_RID_VAL_REG	ECC Cache RouteID Write Value Register	0298 0128h
130h	DDRSS_ECC_R0_STR_ADDR_REG	ECC Range 0 Start Address Register	0298 0130h
134h	DDRSS_ECC_R0_END_ADDR_REG	ECC Range 0 End Address Register	0298 0134h
138h	DDRSS_ECC_R1_STR_ADDR_REG	ECC Range 1 Start Address Register	0298 0138h
13Ch	DDRSS_ECC_R1_END_ADDR_REG	ECC Range 1 End Address Register	0298 013Ch
140h	DDRSS_ECC_R2_STR_ADDR_REG	ECC Range 2 Start Address Register	0298 0140h
144h	DDRSS_ECC_R2_END_ADDR_REG	ECC Range 2 End Address Register	0298 0144h
150h	DDRSS_ECC_1B_ERR_CNT_REG	ECC 1-Bit Error Count Register	0298 0150h
154h	DDRSS_ECC_1B_ERR_THRSH_REG	ECC 1-Bit Error Threshold Register	0298 0154h
158h	DDRSS_ECC_1B_ERR_ADR_LOG_REG	ECC 1-Bit Error Address Log Register	0298 0158h
15Ch	DDRSS_ECC_1B_ERR_MSK_LOG_REG	ECC 1-Bit Error Mask Log Register	0298 015Ch
160h	DDRSS_ECC_2B_ERR_ADR_LOG_REG	ECC 2-Bit Error Address Log Register	0298 0160h
164h	DDRSS_ECC_2B_ERR_MSK_LOG_REG	ECC 2-Bit Error Mask Log Register	0298 0164h
180h	DDRSS_PHY_BIST_CTRL_REG	PHY BIST Control Register	0298 0180h

4.1.1 DDRSS_SS_ID_REV_REG Register (Offset = 0h) [reset = 68046900h]

DDRSS_SS_ID_REV_REG is shown in [Figure 4-1](#) and described in [Table 4-4](#).

Return to [Summary Table](#).

The Subsystem ID and Revision Register contains the module ID, major, and minor revisions for the subsystem.

Table 4-3. DDRSS_SS_ID_REV_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0000h

Figure 4-1. DDRSS_SS_ID_REV_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MOD_ID															
R-6804h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER				MAJ_REV				CUSTOM		MIN_REV					
R-Dh				R-1h				R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-4. DDRSS_SS_ID_REV_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MOD_ID	R	6804h	Module ID
15-11	RTL_VER	R	Dh	RTL version
10-8	MAJ_REV	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MIN_REV	R	0h	Minor revision

4.1.2 DDRSS_SS_CTL_REG Register (Offset = 4h) [reset = X]

DDRSS_SS_CTL_REG is shown in [Figure 4-2](#) and described in [Table 4-6](#).

Return to [Summary Table](#).

The Subsystem Control Register contains fields for control functions required for submodules in the subsystem.

Table 4-5. DDRSS_SS_CTL_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0004h

Figure 4-2. DDRSS_SS_CTL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_BYPASS
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-6. DDRSS_SS_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PHY_PLL_BYPASS	R/W	0h	PHY De-Skew PLL bypass. Write 1 to bypass PLL.

4.1.3 DDRSS_V2A_CTL_REG Register (Offset = 20h) [reset = X]

DDRSS_V2A_CTL_REG is shown in Figure 4-3 and described in Table 4-8.

Return to [Summary Table](#).

The MSMC2DDR Bridge Control register contains control functions required for the MSMC2DDR bridge submodule.

Table 4-7. DDRSS_V2A_CTL_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0020h

Figure 4-3. DDRSS_V2A_CTL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		WR_LO_BLK_THR				CRIT_THRESH	
R/W-X		R/W-18h				R/W-18h	
15	14	13	12	11	10	9	8
CRIT_THRESH				RESERVED	SDRAM_3QT	SDRAM_IDX	
R/W-18h				R/W-X	R/W-0h	R/W-13h	
7	6	5	4	3	2	1	0
SDRAM_IDX			REGION_IDX				
R/W-13h			R/W-13h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-8. DDRSS_V2A_CTL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-17	WR_LO_BLK_THR	R/W	18h	Write data threshold in 64 byte quantas. The MSMC2DDR bridge will block all Low Priority Thread writes to DDR when the total number of write data bytes sent to the controller is greater than this value. The reset value of this field is optimal however, it can be changed for better traffic shaping.
16-12	CRIT_THRESH	R/W	18h	Critical threshold. The MSMC2DDR bridge will block all Low Priority Thread traffic to DDR when the total number of commands sent to the controller is greater than this value. The reset value of this field is optimal however, it can be changed for better traffic shaping.
11	RESERVED	R/W	X	
10	SDRAM_3QT	R/W	0h	Setting this field to a 1 will modify SDRAM Index to be 3/4 its programmed value to support 3, 6, 12 and 24 GB sizes.

Table 4-8. DDRSS_V2A_CTL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-5	SDRAM_IDX	R/W	13h	<p>SDRAM Index = $\log_2(\text{connected SDRAM size}) - 16$.</p> <p>The <code>sdram_idx</code> describes the number of address bits minus 16 that are used to determine the mask used to detect memory rollover and prevent aliasing and false coherency issues.</p> <p>Max size supported is 8GB.</p> <p>A programmed value greater than 0x13 will result in this field being reset to 0x13.</p>
4-0	REGION_IDX	R/W	13h	<p>Region Index = $\log_2(\text{CBA region size}) - 16$.</p> <p>The <code>region_idx</code> describes the number of address bits minus 16 that are used to determine the mask used to detect memory rollover and prevent aliasing and false coherency issues.</p> <p>Max size supported is 8GB.</p> <p>A programmed value greater than 0x13 will result in this field being reset to 0x13.</p>

4.1.4 DDRSS_V2A_R1_MAT_REG Register (Offset = 24h) [reset = 0h]

DDRSS_V2A_R1_MAT_REG is shown in Figure 4-4 and described in Table 4-10.

Return to [Summary Table](#).

The Range 1 Match Register allows a single master to a range of masters to change their priority mapping. This allows selective masters to be increased or decreased in effective priority. Range 1 Match Register uses the associated Range 1 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

Table 4-9. DDRSS_V2A_R1_MAT_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0024h

Figure 4-4. DDRSS_V2A_R1_MAT_REG Register

31	30	29	28	27	26	25	24
RANGE1_RANGEEN_A	RANGE1_MASK_A			RANGE1_ROUTEID_A			
R/W-0h	R/W-0h			R/W-0h			
23	22	21	20	19	18	17	16
RANGE1_ROUTEID_A							
R/W-0h							
15	14	13	12	11	10	9	8
RANGE1_RANGEEN_B	RANGE1_MASK_B			RANGE1_ROUTEID_B			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
RANGE1_ROUTEID_B							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-10. DDRSS_V2A_R1_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE1_RANGEEN_A	R/W	0h	The range1_rangeen_a enables the RouteID AND'd with range1_mask_a to match the range1_routeid_a
30-28	RANGE1_MASK_A	R/W	0h	The range1_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a
27-16	RANGE1_ROUTEID_A	R/W	0h	The range1_routeid_a is the value that is compared to the RouteID arriving on the command interface
15	RANGE1_RANGEEN_B	R/W	0h	The range1_rangeen_b enables the RouteID AND'd with range1_mask_b to match the range1_routeid_b
14-12	RANGE1_MASK_B	R/W	0h	The range1_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b
11-0	RANGE1_ROUTEID_B	R/W	0h	The range1_routeid_b is the value that is compared to the RouteID arriving on the command interface

4.1.5 DDRSS_V2A_R2_MAT_REG Register (Offset = 28h) [reset = 0h]

DDRSS_V2A_R2_MAT_REG is shown in Figure 4-5 and described in Table 4-12.

Return to [Summary Table](#).

The Range 2 Match Register allows a single master to a range of masters to change their priority mapping. This allows selective masters to be increased or decreased in effective priority. Range 2 Match Register uses the associated Range 2 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

Table 4-11. DDRSS_V2A_R2_MAT_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0028h

Figure 4-5. DDRSS_V2A_R2_MAT_REG Register

31	30	29	28	27	26	25	24
RANGE2_RANGEEN_A	RANGE2_MASK_A			RANGE2_ROUTEID_A			
R/W-0h	R/W-0h			R/W-0h			
23	22	21	20	19	18	17	16
RANGE2_ROUTEID_A							
R/W-0h							
15	14	13	12	11	10	9	8
RANGE2_RANGEEN_B	RANGE2_MASK_B			RANGE2_ROUTEID_B			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
RANGE2_ROUTEID_B							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-12. DDRSS_V2A_R2_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE2_RANGEEN_A	R/W	0h	The range2_rangeen_a enables the RouteID AND'd with range2_mask_a to match the range2_routeid_a
30-28	RANGE2_MASK_A	R/W	0h	The range2_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a
27-16	RANGE2_ROUTEID_A	R/W	0h	The range2_routeid_a is the value that is compared to the RouteID arriving on the command interface
15	RANGE2_RANGEEN_B	R/W	0h	The range2_rangeen_b enables the RouteID AND'd with range2_mask_b to match the range2_routeid_b
14-12	RANGE2_MASK_B	R/W	0h	The range2_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b
11-0	RANGE2_ROUTEID_B	R/W	0h	The range2_routeid_b is the value that is compared to the RouteID arriving on the command interface

4.1.6 DDRSS_V2A_R3_MAT_REG Register (Offset = 2Ch) [reset = 0h]

DDRSS_V2A_R3_MAT_REG is shown in Figure 4-6 and described in Table 4-14.

Return to [Summary Table](#).

The Range 3 Match Register allows a single master to a range of masters to change their priority mapping. This allows selective masters to be increased or decreased in effective priority. Range 3 Match Register uses the associated Range 3 Priority Map Register. The highest Range Match Register will take priority and will be used in case of multiple range matches.

Table 4-13. DDRSS_V2A_R3_MAT_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 002Ch

Figure 4-6. DDRSS_V2A_R3_MAT_REG Register

31	30	29	28	27	26	25	24
RANGE3_RANGEEN_A	RANGE3_MASK_A			RANGE3_ROUTEID_A			
R/W-0h	R/W-0h			R/W-0h			
23	22	21	20	19	18	17	16
RANGE3_ROUTEID_A							
R/W-0h							
15	14	13	12	11	10	9	8
RANGE3_RANGEEN_B	RANGE3_MASK_B			RANGE3_ROUTEID_B			
R/W-0h	R/W-0h			R/W-0h			
7	6	5	4	3	2	1	0
RANGE3_ROUTEID_B							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-14. DDRSS_V2A_R3_MAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RANGE3_RANGEEN_A	R/W	0h	The range3_rangeen_a enables the RouteID AND'd with range3_mask_a to match the range3_routeid_a
30-28	RANGE3_MASK_A	R/W	0h	The range3_mask_a allows a number of least significant bits to be ignored prior to the match of the routeid_a
27-16	RANGE3_ROUTEID_A	R/W	0h	The range3_routeid_a is the value that is compared to the RouteID arriving on the command interface
15	RANGE3_RANGEEN_B	R/W	0h	The range3_rangeen_b enables the RouteID AND'd with range3_mask_b to match the range3_routeid_b
14-12	RANGE3_MASK_B	R/W	0h	The range3_mask_b allows a number of least significant bits to be ignored prior to the match of the routeid_b
11-0	RANGE3_ROUTEID_B	R/W	0h	The range3_routeid_b is the value that is compared to the RouteID arriving on the command interface

4.1.7 DDRSS_V2A_LPT_DEF_PRI_MAP_REG Register (Offset = 30h) [reset = X]

DDRSS_V2A_LPT_DEF_PRI_MAP_REG is shown in Figure 4-7 and described in Table 4-16.

Return to [Summary Table](#).

The LPT Default Priority Mapping Register is the default map for the inbound VBUSM.C priority on the Low Priority Thread to AXI priority.

Table 4-15. DDRSS_V2A_LPT_DEF_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0030h

Figure 4-7. DDRSS_V2A_LPT_DEF_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	LPT_PRIMAP0			RESERVED	LPT_PRIMAP1		
R/W-X	R/W-2h			R/W-X	R/W-3h		
23	22	21	20	19	18	17	16
RESERVED	LPT_PRIMAP2			RESERVED	LPT_PRIMAP3		
R/W-X	R/W-4h			R/W-X	R/W-5h		
15	14	13	12	11	10	9	8
RESERVED	LPT_PRIMAP4			RESERVED	LPT_PRIMAP5		
R/W-X	R/W-6h			R/W-X	R/W-6h		
7	6	5	4	3	2	1	0
RESERVED	LPT_PRIMAP6			RESERVED	LPT_PRIMAP7		
R/W-X	R/W-7h			R/W-X	R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-16. DDRSS_V2A_LPT_DEF_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	LPT_PRIMAP0	R/W	2h	The field contains AXI priority value for VBUSM.C priority 0. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	LPT_PRIMAP1	R/W	3h	The field contains AXI priority value for VBUSM.C priority 1. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	LPT_PRIMAP2	R/W	4h	The field contains AXI priority value for VBUSM.C priority 2. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	LPT_PRIMAP3	R/W	5h	The field contains AXI priority value for VBUSM.C priority 3. 0=highest priority. 7=lowest priority
15	RESERVED	R/W	X	
14-12	LPT_PRIMAP4	R/W	6h	The field contains AXI priority value for VBUSM.C priority 4. 0=highest priority. 7=lowest priority

Table 4-16. DDRSS_V2A_LPT_DEF_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RESERVED	R/W	X	
10-8	LPT_PRIMAP5	R/W	6h	The field contains AXI priority value for VBUSM.C priority 5. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	LPT_PRIMAP6	R/W	7h	The field contains AXI priority value for VBUSM.C priority 6. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	LPT_PRIMAP7	R/W	7h	The field contains AXI priority value for VBUSM.C priority 7. 0=highest priority. 7=lowest priority

4.1.8 DDRSS_V2A_LPT_R1_PRI_MAP_REG Register (Offset = 34h) [reset = X]

DDRSS_V2A_LPT_R1_PRI_MAP_REG is shown in Figure 4-8 and described in Table 4-18.

Return to [Summary Table](#).

The LPT Range 1 Priority Mapping Register is used to map the inbound VBUSM.C priority on the Low Priority Thread to AXI priority when a RouteID match 1 occurs. This allows the priority level to be changed from the LPT Default Priority Mapping value.

Table 4-17. DDRSS_V2A_LPT_R1_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0034h

Figure 4-8. DDRSS_V2A_LPT_R1_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	LPT_RANGE1_PRIMAP0			RESERVED	LPT_RANGE1_PRIMAP1		
R/W-X	R/W-2h			R/W-X	R/W-3h		
23	22	21	20	19	18	17	16
RESERVED	LPT_RANGE1_PRIMAP2			RESERVED	LPT_RANGE1_PRIMAP3		
R/W-X	R/W-4h			R/W-X	R/W-5h		
15	14	13	12	11	10	9	8
RESERVED	LPT_RANGE1_PRIMAP4			RESERVED	LPT_RANGE1_PRIMAP5		
R/W-X	R/W-6h			R/W-X	R/W-6h		
7	6	5	4	3	2	1	0
RESERVED	LPT_RANGE1_PRIMAP6			RESERVED	LPT_RANGE1_PRIMAP7		
R/W-X	R/W-7h			R/W-X	R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-18. DDRSS_V2A_LPT_R1_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	LPT_RANGE1_PRIMAP0	R/W	2h	The field contains AXI priority value for VBUSM.C priority 0 for range match 1. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	LPT_RANGE1_PRIMAP1	R/W	3h	The field contains AXI priority value for VBUSM.C priority 1 for range match 1. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	LPT_RANGE1_PRIMAP2	R/W	4h	The field contains AXI priority value for VBUSM.C priority 2 for range match 1. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	LPT_RANGE1_PRIMAP3	R/W	5h	The field contains AXI priority value for VBUSM.C priority 3 for range match 1. 0=highest priority. 7=lowest priority

Table 4-18. DDRSS_V2A_LPT_R1_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	X	
14-12	LPT_RANGE1_PRIMAP4	R/W	6h	The field contains AXI priority value for VBUSM.C priority 4 for range match 1. 0=highest priority. 7=lowest priority
11	RESERVED	R/W	X	
10-8	LPT_RANGE1_PRIMAP5	R/W	6h	The field contains AXI priority value for VBUSM.C priority 5 for range match 1. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	LPT_RANGE1_PRIMAP6	R/W	7h	The field contains AXI priority value for VBUSM.C priority 6 for range match 1. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	LPT_RANGE1_PRIMAP7	R/W	7h	The field contains AXI priority value for VBUSM.C priority 7 for range match 1. 0=highest priority. 7=lowest priority

4.1.9 DDRSS_V2A_LPT_R2_PRI_MAP_REG Register (Offset = 38h) [reset = X]

DDRSS_V2A_LPT_R2_PRI_MAP_REG is shown in Figure 4-9 and described in Table 4-20.

Return to [Summary Table](#).

The LPT Range 2 Priority Mapping Register is used to map the inbound VBUSM.C priority on the Low Priority Thread to AXI priority when a RouteID match 2 occurs. This allows the priority level to be changed from the LPT Default Priority Mapping value.

Table 4-19. DDRSS_V2A_LPT_R2_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0038h

Figure 4-9. DDRSS_V2A_LPT_R2_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	LPT_RANGE2_PRIMAP0			RESERVED	LPT_RANGE2_PRIMAP1		
R/W-X	R/W-2h			R/W-X	R/W-3h		
23	22	21	20	19	18	17	16
RESERVED	LPT_RANGE2_PRIMAP2			RESERVED	LPT_RANGE2_PRIMAP3		
R/W-X	R/W-4h			R/W-X	R/W-5h		
15	14	13	12	11	10	9	8
RESERVED	LPT_RANGE2_PRIMAP4			RESERVED	LPT_RANGE2_PRIMAP5		
R/W-X	R/W-6h			R/W-X	R/W-6h		
7	6	5	4	3	2	1	0
RESERVED	LPT_RANGE2_PRIMAP6			RESERVED	LPT_RANGE2_PRIMAP7		
R/W-X	R/W-7h			R/W-X	R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-20. DDRSS_V2A_LPT_R2_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	LPT_RANGE2_PRIMAP0	R/W	2h	The field contains AXI priority value for VBUSM.C priority 0 for range match 2. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	LPT_RANGE2_PRIMAP1	R/W	3h	The field contains AXI priority value for VBUSM.C priority 1 for range match 2. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	LPT_RANGE2_PRIMAP2	R/W	4h	The field contains AXI priority value for VBUSM.C priority 2 for range match 2. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	LPT_RANGE2_PRIMAP3	R/W	5h	The field contains AXI priority value for VBUSM.C priority 3 for range match 2. 0=highest priority. 7=lowest priority

Table 4-20. DDRSS_V2A_LPT_R2_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	X	
14-12	LPT_RANGE2_PRIMAP4	R/W	6h	The field contains AXI priority value for VBUSM.C priority 4 for range match 2. 0=highest priority. 7=lowest priority
11	RESERVED	R/W	X	
10-8	LPT_RANGE2_PRIMAP5	R/W	6h	The field contains AXI priority value for VBUSM.C priority 5 for range match 2. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	LPT_RANGE2_PRIMAP6	R/W	7h	The field contains AXI priority value for VBUSM.C priority 6 for range match 2. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	LPT_RANGE2_PRIMAP7	R/W	7h	The field contains AXI priority value for VBUSM.C priority 7 for range match 2. 0=highest priority. 7=lowest priority

4.1.10 DDRSS_V2A_LPT_R3_PRI_MAP_REG Register (Offset = 3Ch) [reset = X]

DDRSS_V2A_LPT_R3_PRI_MAP_REG is shown in Figure 4-10 and described in Table 4-22.

Return to [Summary Table](#).

The LPT Range 3 Priority Mapping Register is used to map the inbound VBUSM.C priority on the Low Priority Thread to AXI priority when a RouteID match 3 occurs. This allows the priority level to be changed from the LPT Default Priority Mapping value.

Table 4-21. DDRSS_V2A_LPT_R3_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 003Ch

Figure 4-10. DDRSS_V2A_LPT_R3_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	LPT_RANGE3_PRIMAP0			RESERVED	LPT_RANGE3_PRIMAP1		
R/W-X	R/W-2h			R/W-X	R/W-3h		
23	22	21	20	19	18	17	16
RESERVED	LPT_RANGE3_PRIMAP2			RESERVED	LPT_RANGE3_PRIMAP3		
R/W-X	R/W-4h			R/W-X	R/W-5h		
15	14	13	12	11	10	9	8
RESERVED	LPT_RANGE3_PRIMAP4			RESERVED	LPT_RANGE3_PRIMAP5		
R/W-X	R/W-6h			R/W-X	R/W-6h		
7	6	5	4	3	2	1	0
RESERVED	LPT_RANGE3_PRIMAP6			RESERVED	LPT_RANGE3_PRIMAP7		
R/W-X	R/W-7h			R/W-X	R/W-7h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-22. DDRSS_V2A_LPT_R3_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	LPT_RANGE3_PRIMAP0	R/W	2h	The field contains AXI priority value for VBUSM.C priority 0 for range match 3. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	LPT_RANGE3_PRIMAP1	R/W	3h	The field contains AXI priority value for VBUSM.C priority 1 for range match 3. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	LPT_RANGE3_PRIMAP2	R/W	4h	The field contains AXI priority value for VBUSM.C priority 2 for range match 3. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	LPT_RANGE3_PRIMAP3	R/W	5h	The field contains AXI priority value for VBUSM.C priority 3 for range match 3. 0=highest priority. 7=lowest priority

Table 4-22. DDRSS_V2A_LPT_R3_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	X	
14-12	LPT_RANGE3_PRIMAP4	R/W	6h	The field contains AXI priority value for VBUSM.C priority 4 for range match 3. 0=highest priority. 7=lowest priority
11	RESERVED	R/W	X	
10-8	LPT_RANGE3_PRIMAP5	R/W	6h	The field contains AXI priority value for VBUSM.C priority 5 for range match 3. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	LPT_RANGE3_PRIMAP6	R/W	7h	The field contains AXI priority value for VBUSM.C priority 6 for range match 3. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	LPT_RANGE3_PRIMAP7	R/W	7h	The field contains AXI priority value for VBUSM.C priority 7 for range match 3. 0=highest priority. 7=lowest priority

4.1.11 DDRSS_V2A_HPT_DEF_PRI_MAP_REG Register (Offset = 4Ch) [reset = X]

DDRSS_V2A_HPT_DEF_PRI_MAP_REG is shown in [Figure 4-11](#) and described in [Table 4-24](#).

Return to [Summary Table](#).

The HPT Default Priority Mapping Register is the default map for the inbound VBUSM.C priority on the High Priority Thread to the AXI priority.

Table 4-23. DDRSS_V2A_HPT_DEF_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 004Ch

Figure 4-11. DDRSS_V2A_HPT_DEF_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	HPT_PRIMAP0			RESERVED	HPT_PRIMAP1		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	HPT_PRIMAP2			RESERVED	HPT_PRIMAP3		
R/W-X	R/W-1h			R/W-X	R/W-1h		
15	14	13	12	11	10	9	8
RESERVED	HPT_PRIMAP4			RESERVED	HPT_PRIMAP5		
R/W-X	R/W-2h			R/W-X	R/W-3h		
7	6	5	4	3	2	1	0
RESERVED	HPT_PRIMAP6			RESERVED	HPT_PRIMAP7		
R/W-X	R/W-4h			R/W-X	R/W-5h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-24. DDRSS_V2A_HPT_DEF_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	HPT_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM.C priority 0. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	HPT_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM.C priority 1. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	HPT_PRIMAP2	R/W	1h	The field contains AXI priority value for VBUSM.C priority 2. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	HPT_PRIMAP3	R/W	1h	The field contains AXI priority value for VBUSM.C priority 3. 0=highest priority. 7=lowest priority
15	RESERVED	R/W	X	
14-12	HPT_PRIMAP4	R/W	2h	The field contains AXI priority value for VBUSM.C priority 4. 0=highest priority. 7=lowest priority

Table 4-24. DDRSS_V2A_HPT_DEF_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	RESERVED	R/W	X	
10-8	HPT_PRIMAP5	R/W	3h	The field contains AXI priority value for VBUSM.C priority 5. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	HPT_PRIMAP6	R/W	4h	The field contains AXI priority value for VBUSM.C priority 6. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	HPT_PRIMAP7	R/W	5h	The field contains AXI priority value for VBUSM.C priority 7. 0=highest priority. 7=lowest priority

4.1.12 DDRSS_V2A_HPT_R1_PRI_MAP_REG Register (Offset = 50h) [reset = X]

DDRSS_V2A_HPT_R1_PRI_MAP_REG is shown in Figure 4-12 and described in Table 4-26.

Return to [Summary Table](#).

The HPT Range 1 Priority Mapping Register is used to map the inbound VBUSM.C priority on the High Priority Thread to AXI priority when a RouteID match 1 occurs. This allows the priority level to be changed from the HPT Default Priority Mapping value.

Table 4-25. DDRSS_V2A_HPT_R1_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0050h

Figure 4-12. DDRSS_V2A_HPT_R1_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	HPT_RANGE1_PRIMAP0			RESERVED	HPT_RANGE1_PRIMAP1		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	HPT_RANGE1_PRIMAP2			RESERVED	HPT_RANGE1_PRIMAP3		
R/W-X	R/W-1h			R/W-X	R/W-1h		
15	14	13	12	11	10	9	8
RESERVED	HPT_RANGE1_PRIMAP4			RESERVED	HPT_RANGE1_PRIMAP5		
R/W-X	R/W-2h			R/W-X	R/W-3h		
7	6	5	4	3	2	1	0
RESERVED	HPT_RANGE1_PRIMAP6			RESERVED	HPT_RANGE1_PRIMAP7		
R/W-X	R/W-4h			R/W-X	R/W-5h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-26. DDRSS_V2A_HPT_R1_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	HPT_RANGE1_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM.C priority 0 for range match 1. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	HPT_RANGE1_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM.C priority 1 for range match 1. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	HPT_RANGE1_PRIMAP2	R/W	1h	The field contains AXI priority value for VBUSM.C priority 2 for range match 1. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	HPT_RANGE1_PRIMAP3	R/W	1h	The field contains AXI priority value for VBUSM.C priority 3 for range match 1. 0=highest priority. 7=lowest priority

Table 4-26. DDRSS_V2A_HPT_R1_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	X	
14-12	HPT_RANGE1_PRIMAP4	R/W	2h	The field contains AXI priority value for VBUSM.C priority 4 for range match 1. 0=highest priority. 7=lowest priority
11	RESERVED	R/W	X	
10-8	HPT_RANGE1_PRIMAP5	R/W	3h	The field contains AXI priority value for VBUSM.C priority 5 for range match 1. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	HPT_RANGE1_PRIMAP6	R/W	4h	The field contains AXI priority value for VBUSM.C priority 6 for range match 1. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	HPT_RANGE1_PRIMAP7	R/W	5h	The field contains AXI priority value for VBUSM.C priority 7 for range match 1. 0=highest priority. 7=lowest priority

4.1.13 DDRSS_V2A_HPT_R2_PRI_MAP_REG Register (Offset = 54h) [reset = X]

DDRSS_V2A_HPT_R2_PRI_MAP_REG is shown in Figure 4-13 and described in Table 4-28.

Return to [Summary Table](#).

The HPT Range 2 Priority Mapping Register is used to map the inbound VBUSM.C priority on the High Priority Thread to AXI priority when a RouteID match 2 occurs. This allows the priority level to be changed from the HPT Default Priority Mapping value.

Table 4-27. DDRSS_V2A_HPT_R2_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0054h

Figure 4-13. DDRSS_V2A_HPT_R2_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	HPT_RANGE2_PRIMAP0			RESERVED	HPT_RANGE2_PRIMAP1		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	HPT_RANGE2_PRIMAP2			RESERVED	HPT_RANGE2_PRIMAP3		
R/W-X	R/W-1h			R/W-X	R/W-1h		
15	14	13	12	11	10	9	8
RESERVED	HPT_RANGE2_PRIMAP4			RESERVED	HPT_RANGE2_PRIMAP5		
R/W-X	R/W-2h			R/W-X	R/W-3h		
7	6	5	4	3	2	1	0
RESERVED	HPT_RANGE2_PRIMAP6			RESERVED	HPT_RANGE2_PRIMAP7		
R/W-X	R/W-4h			R/W-X	R/W-5h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-28. DDRSS_V2A_HPT_R2_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	HPT_RANGE2_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM.C priority 0 for range match 2. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	HPT_RANGE2_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM.C priority 1 for range match 2. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	HPT_RANGE2_PRIMAP2	R/W	1h	The field contains AXI priority value for VBUSM.C priority 2 for range match 2. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	HPT_RANGE2_PRIMAP3	R/W	1h	The field contains AXI priority value for VBUSM.C priority 3 for range match 2. 0=highest priority. 7=lowest priority

Table 4-28. DDRSS_V2A_HPT_R2_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	X	
14-12	HPT_RANGE2_PRIMAP4	R/W	2h	The field contains AXI priority value for VBUSM.C priority 4 for range match 2. 0=highest priority. 7=lowest priority
11	RESERVED	R/W	X	
10-8	HPT_RANGE2_PRIMAP5	R/W	3h	The field contains AXI priority value for VBUSM.C priority 5 for range match 2. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	HPT_RANGE2_PRIMAP6	R/W	4h	The field contains AXI priority value for VBUSM.C priority 6 for range match 2. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	HPT_RANGE2_PRIMAP7	R/W	5h	The field contains AXI priority value for VBUSM.C priority 7 for range match 2. 0=highest priority. 7=lowest priority

4.1.14 DDRSS_V2A_HPT_R3_PRI_MAP_REG Register (Offset = 58h) [reset = X]

DDRSS_V2A_HPT_R3_PRI_MAP_REG is shown in Figure 4-14 and described in Table 4-30.

Return to [Summary Table](#).

The HPT Range 3 Priority Mapping Register is used to map the inbound VBUSM.C priority on the High Priority Thread to AXI priority when a RouteID match 3 occurs. This allows the priority level to be changed from the HPT Default Priority Mapping value.

Table 4-29. DDRSS_V2A_HPT_R3_PRI_MAP_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0058h

Figure 4-14. DDRSS_V2A_HPT_R3_PRI_MAP_REG Register

31	30	29	28	27	26	25	24
RESERVED	HPT_RANGE3_PRIMAP0			RESERVED	HPT_RANGE3_PRIMAP1		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	HPT_RANGE3_PRIMAP2			RESERVED	HPT_RANGE3_PRIMAP3		
R/W-X	R/W-1h			R/W-X	R/W-1h		
15	14	13	12	11	10	9	8
RESERVED	HPT_RANGE3_PRIMAP4			RESERVED	HPT_RANGE3_PRIMAP5		
R/W-X	R/W-2h			R/W-X	R/W-3h		
7	6	5	4	3	2	1	0
RESERVED	HPT_RANGE3_PRIMAP6			RESERVED	HPT_RANGE3_PRIMAP7		
R/W-X	R/W-4h			R/W-X	R/W-5h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-30. DDRSS_V2A_HPT_R3_PRI_MAP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	HPT_RANGE3_PRIMAP0	R/W	0h	The field contains AXI priority value for VBUSM.C priority 0 for range match 3. 0=highest priority. 7=lowest priority
27	RESERVED	R/W	X	
26-24	HPT_RANGE3_PRIMAP1	R/W	0h	The field contains AXI priority value for VBUSM.C priority 1 for range match 3. 0=highest priority. 7=lowest priority
23	RESERVED	R/W	X	
22-20	HPT_RANGE3_PRIMAP2	R/W	1h	The field contains AXI priority value for VBUSM.C priority 2 for range match 3. 0=highest priority. 7=lowest priority
19	RESERVED	R/W	X	
18-16	HPT_RANGE3_PRIMAP3	R/W	1h	The field contains AXI priority value for VBUSM.C priority 3 for range match 3. 0=highest priority. 7=lowest priority

Table 4-30. DDRSS_V2A_HPT_R3_PRI_MAP_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	X	
14-12	HPT_RANGE3_PRIMAP4	R/W	2h	The field contains AXI priority value for VBUSM.C priority 4 for range match 3. 0=highest priority. 7=lowest priority
11	RESERVED	R/W	X	
10-8	HPT_RANGE3_PRIMAP5	R/W	3h	The field contains AXI priority value for VBUSM.C priority 5 for range match 3. 0=highest priority. 7=lowest priority
7	RESERVED	R/W	X	
6-4	HPT_RANGE3_PRIMAP6	R/W	4h	The field contains AXI priority value for VBUSM.C priority 6 for range match 3. 0=highest priority. 7=lowest priority
3	RESERVED	R/W	X	
2-0	HPT_RANGE3_PRIMAP7	R/W	5h	The field contains AXI priority value for VBUSM.C priority 7 for range match 3. 0=highest priority. 7=lowest priority

4.1.15 DDRSS_V2A_AERR_LOG1_REG Register (Offset = 70h) [reset = X]

DDRSS_V2A_AERR_LOG1_REG is shown in [Figure 4-15](#) and described in [Table 4-32](#).

Return to [Summary Table](#).

The Address Error Log 1 register displays the RouteID and lsb of the address for the first VBUSM.C command that was outside the programmed addressing range. Writing a 0x1 will clear all fields. Writing any other value has no effect. The Address Error Log 2 register will also be cleared upon writing this register.

Table 4-31. DDRSS_V2A_AERR_LOG1_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0070h

Figure 4-15. DDRSS_V2A_AERR_LOG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AERR_ADDR_LSB															
R/W1C-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				AERR_ROUTE_ID											
R/W-X				R/W1C-0h											

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-32. DDRSS_V2A_AERR_LOG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	AERR_ADDR_LSB	R/W1C	0h	Address [15:0] of the VBUSM.C command
15-12	RESERVED	R/W	X	
11-0	AERR_ROUTE_ID	R/W1C	0h	RouteID of the VBUSM.C write command

4.1.16 DDRSS_V2A_AERR_LOG2_REG Register (Offset = 74h) [reset = 0h]

DDRSS_V2A_AERR_LOG2_REG is shown in [Figure 4-16](#) and described in [Table 4-34](#).

Return to [Summary Table](#).

The Address Error Log 2 registers displays the msb of the address for the first VBUSM.C command that was outside the programmed addressing range. This register will be cleared upon writing the Address Error Log 1 register.

**Table 4-33. DDRSS_V2A_AERR_LOG2_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0074h

Figure 4-16. DDRSS_V2A_AERR_LOG2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AERR_ADDR_MSB																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-34. DDRSS_V2A_AERR_LOG2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	AERR_ADDR_MSB	R	0h	Address[47:16] of the VBUSM.C command

4.1.17 DDRSS_V2A_OERR_LOG_REG Register (Offset = 78h) [reset = X]

DDRSS_V2A_OERR_LOG_REG is shown in [Figure 4-17](#) and described in [Table 4-36](#).

Return to [Summary Table](#).

The Opcode Error Log register displays the RouteID and opcode for the first VBUSM.C command that had an unsupported opcode. Writing a 0x1 will clear all fields. Writing any other value has no effect.

Table 4-35. DDRSS_V2A_OERR_LOG_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0078h

Figure 4-17. DDRSS_V2A_OERR_LOG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														OERR_OP_CODE	
R/W-X														R/W1C-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OERR_OP_CODE				OERR_ROUTE_ID											
R/W1C-0h				R/W1C-0h											

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-36. DDRSS_V2A_OERR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-12	OERR_OP_CODE	R/W1C	0h	Opcode of the VBUSM.C command
11-0	OERR_ROUTE_ID	R/W1C	0h	RouteID of the VBUSM.C command

4.1.18 DDRSS_V2A_1B_ERR_CNT_REG Register (Offset = 80h) [reset = X]

DDRSS_V2A_1B_ERR_CNT_REG is shown in [Figure 4-18](#) and described in [Table 4-38](#).

Return to [Summary Table](#).

MSMC2DDR Bridge 1-Bit EDC Error Count Register

**Table 4-37. DDRSS_V2A_1B_ERR_CNT_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0080h

Figure 4-18. DDRSS_V2A_1B_ERR_CNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EDC_1B_ERR_CNT															
R/W-X																R/W1C-0h															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-38. DDRSS_V2A_1B_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EDC_1B_ERR_CNT	R/W1C	0h	16-bit counter that displays number of 1-bit EDC errors on write data received on the VBUSM.C interface. Writing a 0x1 will clear this count. Writing any other value has no effect.

4.1.19 DDRSS_V2A_1B_ERR_LOG1_REG Register (Offset = 84h) [reset = X]

DDRSS_V2A_1B_ERR_LOG1_REG is shown in [Figure 4-19](#) and described in [Table 4-40](#).

Return to [Summary Table](#).

The 1-Bit EDC Error Log 1 register displays the RouteID and error position of the first VBUSM.C write that incurred 1-bit EDC error. Writing a 0x1 will clear all fields. Writing any other value has no effect. The 1-Bit EDC Error Log 2 register will also be cleared upon writing this register.

Table 4-39. DDRSS_V2A_1B_ERR_LOG1_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0084h

Figure 4-19. DDRSS_V2A_1B_ERR_LOG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								ERR_POS_1B							
R/W-X								R/W1C-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ROUTE_ID_1B							
R/W-X								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-40. DDRSS_V2A_1B_ERR_LOG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	ERR_POS_1B	R/W1C	0h	Bit error position
15-12	RESERVED	R/W	X	
11-0	ROUTE_ID_1B	R/W1C	0h	RouteID of the VBUSM.C write command

4.1.20 DDRSS_V2A_1B_ERR_LOG2_REG Register (Offset = 88h) [reset = X]

DDRSS_V2A_1B_ERR_LOG2_REG is shown in [Figure 4-20](#) and described in [Table 4-42](#).

Return to [Summary Table](#).

The 1-Bit EDC Error Log 2 registers displays the address of the first VBUSM.C write that incurred 1-bit EDC error. This register will be cleared upon writing the 1-Bit EDC Error Log 1 register.

**Table 4-41. DDRSS_V2A_1B_ERR_LOG2_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0088h

Figure 4-20. DDRSS_V2A_1B_ERR_LOG2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		ADDR_MSB_1B																													
R-X		R-0h																													

LEGEND: R = Read Only; -n = value after reset

Table 4-42. DDRSS_V2A_1B_ERR_LOG2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-0	ADDR_MSB_1B	R	0h	Address [34:5] of the VBUSM.C write command

4.1.21 DDRSS_V2A_2B_ERR_LOG1_REG Register (Offset = 8Ch) [reset = X]

DDRSS_V2A_2B_ERR_LOG1_REG is shown in [Figure 4-21](#) and described in [Table 4-44](#).

Return to [Summary Table](#).

The 2-Bit EDC Error Log 1 register displays the RouteID of the first VBUSM.C write that incurred 2-bit EDC error. Writing a 0x1 clear all fields. Writing any other value has no effect. The 2-Bit EDC Error Log 2 register will also be cleared upon writing this register.

Table 4-43. DDRSS_V2A_2B_ERR_LOG1_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 008Ch

Figure 4-21. DDRSS_V2A_2B_ERR_LOG1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ROUTE_ID_2B																			
R/W-X												R/W1C-0h																			

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-44. DDRSS_V2A_2B_ERR_LOG1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	ROUTE_ID_2B	R/W1C	0h	RouteID of the VBUSM.C write command

4.1.22 DDRSS_V2A_2B_ERR_LOG2_REG Register (Offset = 90h) [reset = X]

DDRSS_V2A_2B_ERR_LOG2_REG is shown in [Figure 4-22](#) and described in [Table 4-46](#).

Return to [Summary Table](#).

The 2-Bit EDC Error Log 1 register displays the address of the first VBUSM.C write that incurred 2-bit EDC error. This register will be cleared upon writing the 2-Bit EDC Error Log 1 register.

**Table 4-45. DDRSS_V2A_2B_ERR_LOG2_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0090h

Figure 4-22. DDRSS_V2A_2B_ERR_LOG2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		ADR_MSB_2B																													
R-X		R-0h																													

LEGEND: R = Read Only; -n = value after reset

Table 4-46. DDRSS_V2A_2B_ERR_LOG2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-0	ADR_MSB_2B	R	0h	Address [34:5] of the VBUSM.C write command

4.1.23 DDRSS_V2A_BUS_TO Register (Offset = 9Ch) [reset = X]

DDRSS_V2A_BUS_TO is shown in [Figure 4-23](#) and described in [Table 4-48](#).

Return to [Summary Table](#).

MSMC2DDR Bridge Bus Timeout Register

Table 4-47. DDRSS_V2A_BUS_TO Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 009Ch

Figure 4-23. DDRSS_V2A_BUS_TO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BUS_TIMER																							
R/W-X								R/W-00FFFFFFh																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-48. DDRSS_V2A_BUS_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	BUS_TIMER	R/W	00FFFFFFh	AXI bus timeout value. Number of DDR clock cycles after which the MSMC2DDR bridge times out if a hang on the controller AXI interface is detected. A value of N will be equal to N x 16 clocks. Writing a 0 will disable the timeout feature.

4.1.24 DDRSS_V2A_INT_RAW_REG Register (Offset = A0h) [reset = X]

DDRSS_V2A_INT_RAW_REG is shown in [Figure 4-24](#) and described in [Table 4-50](#).

Return to [Summary Table](#).

MSMC2DDR Bridge Interrupt Raw Status Register

Table 4-49. DDRSS_V2A_INT_RAW_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 00A0h

Figure 4-24. DDRSS_V2A_INT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	ECCM1BERR	ECC2BERR	ECC1BERR	TOERR	AERR	OERR	
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-50. DDRSS_V2A_INT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	ECCM1BERR	R/W1S	0h	Raw status of SDRAM ECC multi 1-bit errors in same SDRAM burst. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
4	ECC2BERR	R/W1S	0h	Raw status of SDRAM ECC 2-bit error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
3	ECC1BERR	R/W1S	0h	Raw status of SDRAM ECC 1-bit error. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
2	TOERR	R/W1S	0h	Raw status of MSMC2DDR bridge interrupt for controller AXI interface timeout. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
1	AERR	R/W1S	0h	Raw status of MSMC2DDR bridge interrupt for VBUSM.C address outside the programmed range. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.
0	OERR	R/W1S	0h	Raw status of MSMC2DDR bridge interrupt for VBUSM.C unsupported opcode. Write 1 to set the (raw) status, mostly for debug. Writing a 0 has no effect.

4.1.25 DDRSS_V2A_INT_STAT_REG Register (Offset = A4h) [reset = X]

DDRSS_V2A_INT_STAT_REG is shown in [Figure 4-25](#) and described in [Table 4-52](#).

Return to [Summary Table](#).

MSMC2DDR Bridge Interrupt Status Register

Table 4-51. DDRSS_V2A_INT_STAT_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 00A4h

Figure 4-25. DDRSS_V2A_INT_STAT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR	ECC2BERR	ECC1BERR	TOERR	AERR	OERR
R/W-X		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-52. DDRSS_V2A_INT_STAT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	ECCM1BERR	R/W1C	0h	Enabled status of SDRAM ECC multi 1-bit errors in same SDRAM burst. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
4	ECC2BERR	R/W1C	0h	Enabled status of SDRAM ECC 2-bit error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
3	ECC1BERR	R/W1C	0h	Enabled status of SDRAM ECC 1-bit error. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.
2	TOERR	R/W1C	0h	Enabled status of MSMC2DDR bridge interrupt for controller AXI interface timeout. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled). Writing a 0 has no effect.

Table 4-52. DDRSS_V2A_INT_STAT_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR	R/W1C	0h	<p>Enabled status of MSMC2DDR bridge interrupt for VBUSM.C address outside the programmed range.</p> <p>Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled).</p> <p>Writing a 0 has no effect.</p>
0	OERR	R/W1C	0h	<p>Enabled status of MSMC2DDR bridge interrupt for VBUSM.C unsupported opcode.</p> <p>Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, i.e. even if not enabled).</p> <p>Writing a 0 has no effect.</p>

4.1.26 DDRSS_V2A_INT_SET_REG Register (Offset = A8h) [reset = X]

DDRSS_V2A_INT_SET_REG is shown in [Figure 4-26](#) and described in [Table 4-54](#).

Return to [Summary Table](#).

MSMC2DDR Bridge Interrupt Enable Set Register

Table 4-53. DDRSS_V2A_INT_SET_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 00A8h

Figure 4-26. DDRSS_V2A_INT_SET_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR_EN	ECC2BERR_EN	ECC1BERR_EN	TOERR_EN	AERR_EN	OERR_EN
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-54. DDRSS_V2A_INT_SET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	ECCM1BERR_EN	R/W1S	0h	Enable set for SDRAM ECC multi 1-bit errors in same SDRAM burst. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
4	ECC2BERR_EN	R/W1S	0h	Enable set for SDRAM ECC 2-bit error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
3	ECC1BERR_EN	R/W1S	0h	Enable set for SDRAM ECC 1-bit error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.
2	TOERR_EN	R/W1S	0h	Enable set for MSMC2DDR bridge interrupt for controller AXI interface timeout. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

Table 4-54. DDRSS_V2A_INT_SET_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR_EN	R/W1S	0h	<p>Enable set for MSMC2DDR bridge interrupt for VBUSM.C address outside the programmed range.</p> <p>Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register.</p> <p>Writing a 0 has no effect.</p>
0	OERR_EN	R/W1S	0h	<p>Enable set for MSMC2DDR bridge interrupt for VBUSM.C unsupported opcode.</p> <p>Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register.</p> <p>Writing a 0 has no effect.</p>

4.1.27 DDRSS_V2A_INT_CLR_REG Register (Offset = ACh) [reset = X]

DDRSS_V2A_INT_CLR_REG is shown in Figure 4-27 and described in Table 4-56.

Return to [Summary Table](#).

MSMC2DDR Bridge Interrupt Enable Clear Register

Table 4-55. DDRSS_V2A_INT_CLR_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 00ACh

Figure 4-27. DDRSS_V2A_INT_CLR_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		ECCM1BERR_EN	ECC2BERR_EN	ECC1BERR_EN	TOERR_EN	AERR_EN	OERR_EN
R/W-X		R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-56. DDRSS_V2A_INT_CLR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	ECCM1BERR_EN	R/W1C	0h	Enable clear for SDRAM ECC multi 1-bit errors in same SDRAM burst. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
4	ECC2BERR_EN	R/W1C	0h	Enable clear for SDRAM ECC 2-bit error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
3	ECC1BERR_EN	R/W1C	0h	Enable clear for SDRAM ECC 1-bit error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
2	TOERR_EN	R/W1C	0h	Enable clear for MSMC2DDR bridge interrupt for controller AXI interface timeout. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

Table 4-56. DDRSS_V2A_INT_CLR_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AERR_EN	R/W1C	0h	Enable clear for MSMC2DDR bridge interrupt for VBUSM.C address outside the programmed range. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.
0	OERR_EN	R/W1C	0h	Enable clear for MSMC2DDR bridge interrupt for VBUSM.C unsupported opcode. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

4.1.28 DDRSS_V2A_EOI_REG Register (Offset = B0h) [reset = X]

DDRSS_V2A_EOI_REG is shown in [Figure 4-28](#) and described in [Table 4-58](#).

Return to [Summary Table](#).

MSMC2DDR Bridge End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-57. DDRSS_V2A_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 00B0h

Figure 4-28. DDRSS_V2A_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														EOI	
W-X														W-0h	

LEGEND: W = Write Only; -n = value after reset

Table 4-58. DDRSS_V2A_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	W	X	
1-0	EOI	W	0h	Software End Of Interrupt (EOI) control. Write 0 for aerr/oerr/toerr interrupt. Write 1 for ecc1b interrupt. Write 2 for ecc2b interrupt. This field always reads 0 (no EOI memory).

4.1.29 DDRSS_PERF_CNT_SEL_REG Register (Offset = 100h) [reset = X]

DDRSS_PERF_CNT_SEL_REG is shown in [Figure 4-29](#) and described in [Table 4-60](#).

Return to [Summary Table](#).

The Performance Counter Select register is used to select the statistic type to be counted in the corresponding Performance Counter register.

Table 4-59. DDRSS_PERF_CNT_SEL_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0100h

Figure 4-29. DDRSS_PERF_CNT_SEL_REG Register

31	30	29	28	27	26	25	24
RESERVED				CNT4_SEL			
R/W-X				R/W-3h			
23	22	21	20	19	18	17	16
RESERVED				CNT3_SEL			
R/W-X				R/W-2h			
15	14	13	12	11	10	9	8
RESERVED				CNT2_SEL			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
RESERVED				CNT1_SEL			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29-24	CNT4_SEL	R/W	3h	<p>Statistic select for Performance Counter 4 register.</p> <p>0x 0 = Counts every Write command.</p> <p>0x 1 = Counts every Read command.</p> <p>0x 2 = Counts every read as a result of a RMW command.</p> <p>0x 3 = Counts every Activate command.</p> <p>0x 4 = Counts every Precharge command.</p> <p>0x 5 = Counts every Precharge All command.</p> <p>0x 6 = Counts every Mode Register Read command.</p> <p>0x 7 = Counts every Mode Register Write command.</p> <p>0x 8 = Counts every Per Bank Refresh command.</p> <p>0x 9 = Counts every Auto Refresh command.</p> <p>0xA = Counts every ZQ Calib Long command.</p> <p>0xB = Counts every ZQ Calib Short command.</p> <p>0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around.</p> <p>0xD = Counts every Write-to-Write address collision.</p> <p>0xE = Counts every Write-to-Read address collision.</p> <p>0xF = Counts every Read-to-Write address collision.</p> <p>0x 10 = Counts every Read-to-Read address collision.</p> <p>0x 11 = Counts every exit from Power-Down Self-Refresh mode.</p> <p>0x 12 = Counts every entry into Power-Down Self-Refresh mode.</p> <p>0x 13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode.</p> <p>0x 14 = Counts every exit from Power-Down mode.</p> <p>0x 15 = Counts every entry into Power-Down mode.</p> <p>0x 16 = Counts every cycle for which the DDR Controller stays in Power-Down mode.</p> <p>0x 17 = Counts every exit from Self-Refresh mode.</p> <p>0x 18 = Counts every entry into Self-Refresh mode.</p> <p>0x 19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode.</p> <p>0x1A = Reserved</p> <p>0x1B = Reserved</p>

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x1C = Counts every cycle for which the DDR Controller command queue is full. 0x1D = Counts every cycle for which the DDR Controller info FIFO is full. 0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full. 0x1F = Counts every cycle for which the DDR Controller port command FIFO is full. 0x 20 = Counts every cycle for which the DDR Controller write response FIFO is full. 0x 21 = Counts every cycle for which the DDR Controller port write FIFO is full. 0x 22 = Counts every cycle for which the DDR Controller core read FIFO is full. 0x 23 = Counts every cycle for which the DDR Controller port read FIFO is full. 0x 24-0x2F = Reserved
23-22	RESERVED	R/W	X	

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	CNT3_SEL	R/W	2h	<p>Statistic select for Performance Counter 3 register.</p> <p>0x</p> <p>0 = Counts every Write command.</p> <p>0x</p> <p>1 = Counts every Read command.</p> <p>0x</p> <p>2 = Counts every read as a result of a RMW command.</p> <p>0x</p> <p>3 = Counts every Activate command.</p> <p>0x</p> <p>4 = Counts every Precharge command.</p> <p>0x</p> <p>5 = Counts every Precharge All command.</p> <p>0x</p> <p>6 = Counts every Mode Register Read command.</p> <p>0x</p> <p>7 = Counts every Mode Register Write command.</p> <p>0x</p> <p>8 = Counts every Per Bank Refresh command.</p> <p>0x</p> <p>9 = Counts every Auto Refresh command.</p> <p>0xA = Counts every ZQ Calib Long command.</p> <p>0xB = Counts every ZQ Calib Short command.</p> <p>0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around.</p> <p>0xD = Counts every Write-to-Write address collision.</p> <p>0xE = Counts every Write-to-Read address collision.</p> <p>0xF = Counts every Read-to-Write address collision.</p> <p>0x</p> <p>10 = Counts every Read-to-Read address collision.</p> <p>0x</p> <p>11 = Counts every exit from Power-Down Self-Refresh mode.</p> <p>0x</p> <p>12 = Counts every entry into Power-Down Self-Refresh mode.</p> <p>0x</p> <p>13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode.</p> <p>0x</p> <p>14 = Counts every exit from Power-Down mode.</p> <p>0x</p> <p>15 = Counts every entry into Power-Down mode.</p> <p>0x</p> <p>16 = Counts every cycle for which the DDR Controller stays in Power-Down mode.</p> <p>0x</p> <p>17 = Counts every exit from Self-Refresh mode.</p> <p>0x</p> <p>18 = Counts every entry into Self-Refresh mode.</p> <p>0x</p> <p>19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode.</p> <p>0x1A = Reserved</p> <p>0x1B = Reserved</p>

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>0x1C = Counts every cycle for which the DDR Controller command queue is full.</p> <p>0x1D = Counts every cycle for which the DDR Controller info FIFO is full.</p> <p>0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full.</p> <p>0x1F = Counts every cycle for which the DDR Controller port command FIFO is full.</p> <p>0x</p> <p>20 = Counts every cycle for which the DDR Controller write response FIFO is full.</p> <p>0x</p> <p>21 = Counts every cycle for which the DDR Controller port write FIFO is full.</p> <p>0x</p> <p>22 = Counts every cycle for which the DDR Controller core read FIFO is full.</p> <p>0x</p> <p>23 = Counts every cycle for which the DDR Controller port read FIFO is full.</p> <p>0x</p> <p>24-0x2F = Reserved</p>
15-14	RESERVED	R/W	X	

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-8	CNT2_SEL	R/W	1h	<p>Statistic select for Performance Counter 2 register.</p> <p>0x</p> <p>0 = Counts every Write command.</p> <p>0x</p> <p>1 = Counts every Read command.</p> <p>0x</p> <p>2 = Counts every read as a result of a RMW command.</p> <p>0x</p> <p>3 = Counts every Activate command.</p> <p>0x</p> <p>4 = Counts every Precharge command.</p> <p>0x</p> <p>5 = Counts every Precharge All command.</p> <p>0x</p> <p>6 = Counts every Mode Register Read command.</p> <p>0x</p> <p>7 = Counts every Mode Register Write command.</p> <p>0x</p> <p>8 = Counts every Per Bank Refresh command.</p> <p>0x</p> <p>9 = Counts every Auto Refresh command.</p> <p>0xA = Counts every ZQ Calib Long command.</p> <p>0xB = Counts every ZQ Calib Short command.</p> <p>0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around.</p> <p>0xD = Counts every Write-to-Write address collision.</p> <p>0xE = Counts every Write-to-Read address collision.</p> <p>0xF = Counts every Read-to-Write address collision.</p> <p>0x</p> <p>10 = Counts every Read-to-Read address collision.</p> <p>0x</p> <p>11 = Counts every exit from Power-Down Self-Refresh mode.</p> <p>0x</p> <p>12 = Counts every entry into Power-Down Self-Refresh mode.</p> <p>0x</p> <p>13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode.</p> <p>0x</p> <p>14 = Counts every exit from Power-Down mode.</p> <p>0x</p> <p>15 = Counts every entry into Power-Down mode.</p> <p>0x</p> <p>16 = Counts every cycle for which the DDR Controller stays in Power-Down mode.</p> <p>0x</p> <p>17 = Counts every exit from Self-Refresh mode.</p> <p>0x</p> <p>18 = Counts every entry into Self-Refresh mode.</p> <p>0x</p> <p>19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode.</p> <p>0x1A = Reserved</p> <p>0x1B = Reserved</p>

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>0x1C = Counts every cycle for which the DDR Controller command queue is full.</p> <p>0x1D = Counts every cycle for which the DDR Controller info FIFO is full.</p> <p>0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full.</p> <p>0x1F = Counts every cycle for which the DDR Controller port command FIFO is full.</p> <p>0x</p> <p>20 = Counts every cycle for which the DDR Controller write response FIFO is full.</p> <p>0x</p> <p>21 = Counts every cycle for which the DDR Controller port write FIFO is full.</p> <p>0x</p> <p>22 = Counts every cycle for which the DDR Controller core read FIFO is full.</p> <p>0x</p> <p>23 = Counts every cycle for which the DDR Controller port read FIFO is full.</p> <p>0x</p> <p>24-0x2F = Reserved</p>
7-6	RESERVED	R/W	X	

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	CNT1_SEL	R/W	0h	<p>Statistic select for Performance Counter 1 register.</p> <p>0x</p> <p>0 = Counts every Write command.</p> <p>0x</p> <p>1 = Counts every Read command.</p> <p>0x</p> <p>2 = Counts every read as a result of a RMW command.</p> <p>0x</p> <p>3 = Counts every Activate command.</p> <p>0x</p> <p>4 = Counts every Precharge command.</p> <p>0x</p> <p>5 = Counts every Precharge All command.</p> <p>0x</p> <p>6 = Counts every Mode Register Read command.</p> <p>0x</p> <p>7 = Counts every Mode Register Write command.</p> <p>0x</p> <p>8 = Counts every Per Bank Refresh command.</p> <p>0x</p> <p>9 = Counts every Auto Refresh command.</p> <p>0xA = Counts every ZQ Calib Long command.</p> <p>0xB = Counts every ZQ Calib Short command.</p> <p>0xC = Counts every Write-to-Read and Read-to-Write bus-turn-around.</p> <p>0xD = Counts every Write-to-Write address collision.</p> <p>0xE = Counts every Write-to-Read address collision.</p> <p>0xF = Counts every Read-to-Write address collision.</p> <p>0x</p> <p>10 = Counts every Read-to-Read address collision.</p> <p>0x</p> <p>11 = Counts every exit from Power-Down Self-Refresh mode.</p> <p>0x</p> <p>12 = Counts every entry into Power-Down Self-Refresh mode.</p> <p>0x</p> <p>13 = Counts every cycle for which the DDR Controller stays in Power-Down Self-Refresh mode.</p> <p>0x</p> <p>14 = Counts every exit from Power-Down mode.</p> <p>0x</p> <p>15 = Counts every entry into Power-Down mode.</p> <p>0x</p> <p>16 = Counts every cycle for which the DDR Controller stays in Power-Down mode.</p> <p>0x</p> <p>17 = Counts every exit from Self-Refresh mode.</p> <p>0x</p> <p>18 = Counts every entry into Self-Refresh mode.</p> <p>0x</p> <p>19 = Counts every cycle for which the DDR Controller stays in Self-Refresh mode.</p> <p>0x1A = Reserved</p> <p>0x1B = Reserved</p>

Table 4-60. DDRSS_PERF_CNT_SEL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				<p>0x1C = Counts every cycle for which the DDR Controller command queue is full.</p> <p>0x1D = Counts every cycle for which the DDR Controller info FIFO is full.</p> <p>0x1E = Counts every cycle for which the DDR Controller write latency FIFO is full.</p> <p>0x1F = Counts every cycle for which the DDR Controller port command FIFO is full.</p> <p>0x</p> <p>20 = Counts every cycle for which the DDR Controller write response FIFO is full.</p> <p>0x</p> <p>21 = Counts every cycle for which the DDR Controller port write FIFO is full.</p> <p>0x</p> <p>22 = Counts every cycle for which the DDR Controller core read FIFO is full.</p> <p>0x</p> <p>23 = Counts every cycle for which the DDR Controller port read FIFO is full.</p> <p>0x</p> <p>24-0x2F = Reserved</p>

4.1.30 DDRSS_PERF_CNT1_REG Register (Offset = 104h) [reset = 0h]

DDRSS_PERF_CNT1_REG is shown in [Figure 4-30](#) and described in [Table 4-62](#).

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Performance Counter 1 Register

Table 4-61. DDRSS_PERF_CNT1_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0104h

Figure 4-30. DDRSS_PERF_CNT1_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-62. DDRSS_PERF_CNT1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNT1	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register.

4.1.31 DDRSS_PERF_CNT2_REG Register (Offset = 108h) [reset = 0h]

DDRSS_PERF_CNT2_REG is shown in [Figure 4-31](#) and described in [Table 4-64](#).

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Performance Counter 2 Register

Table 4-63. DDRSS_PERF_CNT2_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0108h

Figure 4-31. DDRSS_PERF_CNT2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-64. DDRSS_PERF_CNT2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNT2	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register.

4.1.32 DDRSS_PERF_CNT3_REG Register (Offset = 10Ch) [reset = 0h]

DDRSS_PERF_CNT3_REG is shown in [Figure 4-32](#) and described in [Table 4-66](#).

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Performance Counter 3 Register

Table 4-65. DDRSS_PERF_CNT3_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 010Ch

Figure 4-32. DDRSS_PERF_CNT3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-66. DDRSS_PERF_CNT3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNT3	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register.

4.1.33 DDRSS_PERF_CNT4_REG Register (Offset = 110h) [reset = 0h]

DDRSS_PERF_CNT4_REG is shown in [Figure 4-33](#) and described in [Table 4-68](#).

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Performance Counter 4 Register

Table 4-67. DDRSS_PERF_CNT4_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0110h

Figure 4-33. DDRSS_PERF_CNT4_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT4																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-68. DDRSS_PERF_CNT4_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CNT4	R	0h	Soft 32-bit counter that can be configured as specified in the Performance Counter Select Register.

4.1.34 DDRSS_ECC_CTRL_REG Register (Offset = 120h) [reset = X]

DDRSS_ECC_CTRL_REG is shown in Figure 4-34 and described in Table 4-70.

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ECC Control Register

Table 4-69. DDRSS_ECC_CTRL_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0120h

Figure 4-34. DDRSS_ECC_CTRL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				COR_ECC_THRESH			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED			WR_ALLOC	RESERVED	ECC_CHK	RMW_EN	ECC_EN
R/W-X			R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-70. DDRSS_ECC_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12-8	COR_ECC_THRESH	R/W	0h	Threshold for 1-bit ECC errors in multiple data words in an SDRAM burst that create an uncorrected error fault indication. Value of 0/1 means 2 or more 1-bit errors in multiple data words will result in an uncorrected error fault indication, value of 2 means 3 or more 1-bit errors will result in an uncorrected error fault indication, and so on. Value of 16 or greater disables this feature. This field must always be kept at default, and only changed for debug.
7-5	RESERVED	R/W	X	
4	WR_ALLOC	R/W	0h	When set to 1, an unassigned ECC cache-line will be allocated for a write with routeID that do not match any of the mapped routeID's.
3	RESERVED	R/W	X	
2	ECC_CHK	R/W	0h	Set 1 to enable ECC verification for read accesses when ecc_en=1. The value of this field is ignored when ecc_en=0. This bit must be set and kept static before using DDR.

Table 4-70. DDRSS_ECC_CTRL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RMW_EN	R/W	0h	<p>Read modify write enable.</p> <p>Set 1 to enable RMW functionality for sub-quanta accesses when ecc_en=1.</p> <p>This bit must be set to 1 if ecc_en is set to a 1 to ensure subquanta accesses to DRAM do not result in ECC errors.</p> <p>This bit must be set and kept static before using DDR.</p>
0	ECC_EN	R/W	0h	<p>DRAM ECC enable.</p> <p>Setting a 1 causes ECC to be written to DRAM.</p> <p>This bit must be set and kept static before using DDR.</p>

4.1.35 DDRSS_ECC_RID_INDX_REG Register (Offset = 124h) [reset = X]

DDRSS_ECC_RID_INDX_REG is shown in [Figure 4-35](#) and described in [Table 4-72](#).

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ECC Cache RouteID Index Register

Table 4-71. DDRSS_ECC_RID_INDX_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0124h

Figure 4-35. DDRSS_ECC_RID_INDX_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									ECCRID_ADR						
R/W-X									R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-72. DDRSS_ECC_RID_INDX_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6-0	ECCRID_ADR	R/W	0h	This index specifies the ECC cache entry number that the eccrid_val is mapped to.

4.1.36 DDRSS_ECC_RID_VAL_REG Register (Offset = 128h) [reset = X]

DDRSS_ECC_RID_VAL_REG is shown in [Figure 4-36](#) and described in [Table 4-74](#).

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ECC Cache RouteID Write Value Register

Table 4-73. DDRSS_ECC_RID_VAL_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0128h

Figure 4-36. DDRSS_ECC_RID_VAL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
ECCRID_VAL_VLD	RESERVED			ECCRID_VAL			
R/W-0h	R/W-X			R/W-0h			
7	6	5	4	3	2	1	0
ECCRID_VAL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-74. DDRSS_ECC_RID_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	ECCRID_VAL_VLD	R/W	0h	A 1 in this field indicates that value in eccrid_val is valid.
14-12	RESERVED	R/W	X	
11-0	ECCRID_VAL	R/W	0h	RouteID value written or read.

4.1.37 DDRSS_ECC_R0_STR_ADDR_REG Register (Offset = 130h) [reset = X]

DDRSS_ECC_R0_STR_ADDR_REG is shown in [Figure 4-37](#) and described in [Table 4-76](#).

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ECC Range 0 Start Address Register

Table 4-75. DDRSS_ECC_R0_STR_ADDR_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0130h

Figure 4-37. DDRSS_ECC_R0_STR_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECC_STR_ADR_0																		
R/W-X													R/W-0007FFFFh																		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-76. DDRSS_ECC_R0_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-0	ECC_STR_ADR_0	R/W	0007FFFFh	Start address [34:16] for ECC range 0. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR.

4.1.38 DDRSS_ECC_R0_END_ADDR_REG Register (Offset = 134h) [reset = X]

DDRSS_ECC_R0_END_ADDR_REG is shown in Figure 4-38 and described in Table 4-78.

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ECC Range 0 End Address Register

**Table 4-77. DDRSS_ECC_R0_END_ADDR_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0134h

Figure 4-38. DDRSS_ECC_R0_END_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECC_END_ADR_0																		
R/W-X													R/W-0h																		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-78. DDRSS_ECC_R0_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-0	ECC_END_ADR_0	R/W	0h	End address [34:16] for ECC range 0. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR.

4.1.39 DDRSS_ECC_R1_STR_ADDR_REG Register (Offset = 138h) [reset = X]

DDRSS_ECC_R1_STR_ADDR_REG is shown in [Figure 4-39](#) and described in [Table 4-80](#).

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ECC Range 1 Start Address Register

Table 4-79. DDRSS_ECC_R1_STR_ADDR_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0138h

Figure 4-39. DDRSS_ECC_R1_STR_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECC_STR_ADR_1																		
R/W-X													R/W-0007FFFFh																		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-80. DDRSS_ECC_R1_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-0	ECC_STR_ADR_1	R/W	0007FFFFh	Start address [34:16] for ECC range 1. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR.

4.1.40 DDRSS_ECC_R1_END_ADDR_REG Register (Offset = 13Ch) [reset = X]

DDRSS_ECC_R1_END_ADDR_REG is shown in [Figure 4-40](#) and described in [Table 4-82](#).

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ECC Range 1 End Address Register

**Table 4-81. DDRSS_ECC_R1_END_ADDR_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 013Ch

Figure 4-40. DDRSS_ECC_R1_END_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECC_END_ADR_1																		
R/W-X													R/W-0h																		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-82. DDRSS_ECC_R1_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-0	ECC_END_ADR_1	R/W	0h	End address [34:16] for ECC range 1. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR.

4.1.41 DDRSS_ECC_R2_STR_ADDR_REG Register (Offset = 140h) [reset = X]

DDRSS_ECC_R2_STR_ADDR_REG is shown in [Figure 4-41](#) and described in [Table 4-84](#).

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ECC Range 2 Start Address Register

Table 4-83. DDRSS_ECC_R2_STR_ADDR_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0140h

Figure 4-41. DDRSS_ECC_R2_STR_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECC_STR_ADR_2																		
R/W-X													R/W-0007FFFFh																		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-84. DDRSS_ECC_R2_STR_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-0	ECC_STR_ADR_2	R/W	0007FFFFh	Start address [34:16] for ECC range 2. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR.

4.1.42 DDRSS_ECC_R2_END_ADDR_REG Register (Offset = 144h) [reset = X]

DDRSS_ECC_R2_END_ADDR_REG is shown in Figure 4-42 and described in Table 4-86.

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ECC Range 2 End Address Register

**Table 4-85. DDRSS_ECC_R2_END_ADDR_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0144h

Figure 4-42. DDRSS_ECC_R2_END_ADDR_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													ECC_END_ADR_2																		
R/W-X													R/W-0h																		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-86. DDRSS_ECC_R2_END_ADDR_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-0	ECC_END_ADR_2	R/W	0h	End address [34:16] for ECC range 2. Setting the start address greater than the end address disables the range. The range is inclusive of the start and end addresses. This field must be set and kept static before using DDR.

4.1.43 DDRSS_ECC_1B_ERR_CNT_REG Register (Offset = 150h) [reset = X]

DDRSS_ECC_1B_ERR_CNT_REG is shown in [Figure 4-43](#) and described in [Table 4-88](#).

Return to [Summary Table](#).

ECC 1-Bit Error Count Register

Table 4-87. DDRSS_ECC_1B_ERR_CNT_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0150h

Figure 4-43. DDRSS_ECC_1B_ERR_CNT_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_1B_ERR_CNT															
R/W-X																R/W1C-0h															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-88. DDRSS_ECC_1B_ERR_CNT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	ECC_1B_ERR_CNT	R/W1C	0h	16-bit counter that displays number of 1-bit ECC errors on SDRAM data. Writing a 0x1 will clear this count. Writing any other value has no effect.

4.1.44 DDRSS_ECC_1B_ERR_THRSH_REG Register (Offset = 154h) [reset = X]

DDRSS_ECC_1B_ERR_THRSH_REG is shown in [Figure 4-44](#) and described in [Table 4-90](#).

Return to [Summary Table](#).

ECC 1-Bit Error Threshold Register

**Table 4-89. DDRSS_ECC_1B_ERR_THRSH_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0154h

Figure 4-44. DDRSS_ECC_1B_ERR_THRSH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_1B_ERR_THRSH															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-90. DDRSS_ECC_1B_ERR_THRSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	ECC_1B_ERR_THRSH	R/W	0h	ECC 1-bit error threshold. The bridge will generate an interrupt when the ECC 1-bit error count is equal to or greater than this threshold. A value of 0 will disable the generation of interrupt.

4.1.45 DDRSS_ECC_1B_ERR_ADR_LOG_REG Register (Offset = 158h) [reset = X]

DDRSS_ECC_1B_ERR_ADR_LOG_REG is shown in [Figure 4-45](#) and described in [Table 4-92](#).

Return to [Summary Table](#).

ECC 1-Bit Error Address Log Register

Table 4-91. DDRSS_ECC_1B_ERR_ADR_LOG_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0158h

Figure 4-45. DDRSS_ECC_1B_ERR_ADR_LOG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVE D				ECC_1B_ERR_ADR																											
R/W-X				R/W1C-0h																											

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-92. DDRSS_ECC_1B_ERR_ADR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-0	ECC_1B_ERR_ADR	R/W1C	0h	<p>ECC</p> <p>1-bit error address.</p> <p>64-byte aligned address that had the</p> <p>1-bit ECC error.</p> <p>This field displays the first address logged in the 2 deep logging</p> <p>FIFO.</p> <p>Writing a 0x1 will pop the top element of the FIFO.</p> <p>Writing any other value has no effect.</p>

4.1.46 DDRSS_ECC_1B_ERR_MSK_LOG_REG Register (Offset = 15Ch) [reset = X]

DDRSS_ECC_1B_ERR_MSK_LOG_REG is shown in [Figure 4-46](#) and described in [Table 4-94](#).

Return to [Summary Table](#).

ECC 1-Bit Error Mask Log Register

Table 4-93. DDRSS_ECC_1B_ERR_MSK_LOG_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 015Ch

Figure 4-46. DDRSS_ECC_1B_ERR_MSK_LOG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_1B_ERR_MSK															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-94. DDRSS_ECC_1B_ERR_MSK_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ECC_1B_ERR_MSK	R	0h	<p>ECC</p> <p>1-bit error mask.</p> <p>Mask for the</p> <p>128-byte data block that had the</p> <p>1-bit ECC errors.</p> <p>Each bit represents an ECC quanta (8 bytes) in the</p> <p>128-byte data block starting at address specified by ecc_1b_err_adr.</p> <p>Value of 1 on the bit represents an error in that particular 8 bytes.</p> <p>This field displays the first mask logged in the 2 deep logging FIFO</p> <p>along with the ecc_1b_err_adr.</p> <p>The same mechanism used to pop ecc_1b_err_adr is used to pop</p> <p>this field.</p>

4.1.47 DDRSS_ECC_2B_ERR_ADR_LOG_REG Register (Offset = 160h) [reset = X]

DDRSS_ECC_2B_ERR_ADR_LOG_REG is shown in [Figure 4-47](#) and described in [Table 4-96](#).

Return to [Summary Table](#).

ECC 2-Bit Error Address Log Register

Table 4-95. DDRSS_ECC_2B_ERR_ADR_LOG_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0160h

Figure 4-47. DDRSS_ECC_2B_ERR_ADR_LOG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVE D		ECC_2B_ERR_ADR																													
R/W-X		R/W1C-0h																													

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-96. DDRSS_ECC_2B_ERR_ADR_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-0	ECC_2B_ERR_ADR	R/W1C	0h	ECC 2-bit error address. 64-byte aligned address that had the 2-bit ECC error. Writing a 0x1 will clear this field and the ecc_2b_err_msk field. Writing any other value has no effect.

4.1.48 DDRSS_ECC_2B_ERR_MSK_LOG_REG Register (Offset = 164h) [reset = X]

DDRSS_ECC_2B_ERR_MSK_LOG_REG is shown in [Figure 4-48](#) and described in [Table 4-98](#).

Return to [Summary Table](#).

ECC 2-Bit Error Mask Log Register

**Table 4-97. DDRSS_ECC_2B_ERR_MSK_LOG_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0164h

Figure 4-48. DDRSS_ECC_2B_ERR_MSK_LOG_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ECC_2B_ERR_MSK															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-98. DDRSS_ECC_2B_ERR_MSK_LOG_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ECC_2B_ERR_MSK	R	0h	ECC 2-bit error mask. Mask for the 128-byte data block that had the 2-bit ECC errors. Each bit represents an ECC quanta (8 bytes) in the 128-byte data block starting at address specified by ecc_2b_err_adr. Value of 1 on the bit represents an error in that particular 8 bytes.

4.1.49 DDRSS_PHY_BIST_CTRL_REG Register (Offset = 180h) [reset = X]

DDRSS_PHY_BIST_CTRL_REG is shown in [Figure 4-49](#) and described in [Table 4-100](#).

Return to [Summary Table](#).

PHY BIST Control Register

**Table 4-99. DDRSS_PHY_BIST_CTRL_REG
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_SS_CFG	0298 0180h

Figure 4-49. DDRSS_PHY_BIST_CTRL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BIST_TSEL_SELECT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-100. DDRSS_PHY_BIST_CTRL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	BIST_TSEL_SELECT	R/W	0h	This field controls the bist_tsel_select input of the PHY. For details please refer to the PHY specification.

4.2 DDR Controller Registers

Table 4-102 lists the memory-mapped registers for the DDR controller. All register offset addresses not listed in Table 4-102 should be considered as reserved locations and the register contents should not be modified.

Table 4-101. DDR Controller Instances

Instance	Base Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0000h

Table 4-102. DDR Controller Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
0h	DDRSS_CTL_0	DDR Controller Register 0	0299 0000h
4h	DDRSS_CTL_1	DDR Controller Register 1	0299 0004h
8h	DDRSS_CTL_2	DDR Controller Register 2	0299 0008h
Ch	DDRSS_CTL_3	DDR Controller Register 3	0299 000Ch
10h	DDRSS_CTL_4	DDR Controller Register 4	0299 0010h
14h	DDRSS_CTL_5	DDR Controller Register 5	0299 0014h
18h	DDRSS_CTL_6	DDR Controller Register 6	0299 0018h
1Ch	DDRSS_CTL_7	DDR Controller Register 7	0299 001Ch
20h	DDRSS_CTL_8	DDR Controller Register 8	0299 0020h
24h	DDRSS_CTL_9	DDR Controller Register 9	0299 0024h
28h	DDRSS_CTL_10	DDR Controller Register 10	0299 0028h
2Ch	DDRSS_CTL_11	DDR Controller Register 11	0299 002Ch
30h	DDRSS_CTL_12	DDR Controller Register 12	0299 0030h
34h	DDRSS_CTL_13	DDR Controller Register 13	0299 0034h
38h	DDRSS_CTL_14	DDR Controller Register 14	0299 0038h
3Ch	DDRSS_CTL_15	DDR Controller Register 15	0299 003Ch
40h	DDRSS_CTL_16	DDR Controller Register 16	0299 0040h
44h	DDRSS_CTL_17	DDR Controller Register 17	0299 0044h
48h	DDRSS_CTL_18	DDR Controller Register 18	0299 0048h
4Ch	DDRSS_CTL_19	DDR Controller Register 19	0299 004Ch
50h	DDRSS_CTL_20	DDR Controller Register 20	0299 0050h
54h	DDRSS_CTL_21	DDR Controller Register 21	0299 0054h
58h	DDRSS_CTL_22	DDR Controller Register 22	0299 0058h
5Ch	DDRSS_CTL_23	DDR Controller Register 23	0299 005Ch
60h	DDRSS_CTL_24	DDR Controller Register 24	0299 0060h
68h	DDRSS_CTL_26	DDR Controller Register 26	0299 0068h
6Ch	DDRSS_CTL_27	DDR Controller Register 27	0299 006Ch
70h	DDRSS_CTL_28	DDR Controller Register 28	0299 0070h
74h	DDRSS_CTL_29	DDR Controller Register 29	0299 0074h
78h	DDRSS_CTL_30	DDR Controller Register 30	0299 0078h
7Ch	DDRSS_CTL_31	DDR Controller Register 31	0299 007Ch
80h	DDRSS_CTL_32	DDR Controller Register 32	0299 0080h
84h	DDRSS_CTL_33	DDR Controller Register 33	0299 0084h
88h	DDRSS_CTL_34	DDR Controller Register 34	0299 0088h
8Ch	DDRSS_CTL_35	DDR Controller Register 35	0299 008Ch
90h	DDRSS_CTL_36	DDR Controller Register 36	0299 0090h
94h	DDRSS_CTL_37	DDR Controller Register 37	0299 0094h
98h	DDRSS_CTL_38	DDR Controller Register 38	0299 0098h
9Ch	DDRSS_CTL_39	DDR Controller Register 39	0299 009Ch

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
A0h	DDRSS_CTL_40	DDR Controller Register 40	0299 00A0h
A4h	DDRSS_CTL_41	DDR Controller Register 41	0299 00A4h
A8h	DDRSS_CTL_42	DDR Controller Register 42	0299 00A8h
ACh	DDRSS_CTL_43	DDR Controller Register 43	0299 00ACh
B0h	DDRSS_CTL_44	DDR Controller Register 44	0299 00B0h
B4h	DDRSS_CTL_45	DDR Controller Register 45	0299 00B4h
B8h	DDRSS_CTL_46	DDR Controller Register 46	0299 00B8h
BCh	DDRSS_CTL_47	DDR Controller Register 47	0299 00BCh
C0h	DDRSS_CTL_48	DDR Controller Register 48	0299 00C0h
C4h	DDRSS_CTL_49	DDR Controller Register 49	0299 00C4h
C8h	DDRSS_CTL_50	DDR Controller Register 50	0299 00C8h
CCh	DDRSS_CTL_51	DDR Controller Register 51	0299 00CCh
D0h	DDRSS_CTL_52	DDR Controller Register 52	0299 00D0h
D4h	DDRSS_CTL_53	DDR Controller Register 53	0299 00D4h
D8h	DDRSS_CTL_54	DDR Controller Register 54	0299 00D8h
DCh	DDRSS_CTL_55	DDR Controller Register 55	0299 00DCh
E0h	DDRSS_CTL_56	DDR Controller Register 56	0299 00E0h
E4h	DDRSS_CTL_57	DDR Controller Register 57	0299 00E4h
E8h	DDRSS_CTL_58	DDR Controller Register 58	0299 00E8h
ECh	DDRSS_CTL_59	DDR Controller Register 59	0299 00ECh
F0h	DDRSS_CTL_60	DDR Controller Register 60	0299 00F0h
F4h	DDRSS_CTL_61	DDR Controller Register 61	0299 00F4h
F8h	DDRSS_CTL_62	DDR Controller Register 62	0299 00F8h
FCh	DDRSS_CTL_63	DDR Controller Register 63	0299 00FCh
100h	DDRSS_CTL_64	DDR Controller Register 64	0299 0100h
104h	DDRSS_CTL_65	DDR Controller Register 65	0299 0104h
108h	DDRSS_CTL_66	DDR Controller Register 66	0299 0108h
10Ch	DDRSS_CTL_67	DDR Controller Register 67	0299 010Ch
110h	DDRSS_CTL_68	DDR Controller Register 68	0299 0110h
114h	DDRSS_CTL_69	DDR Controller Register 69	0299 0114h
118h	DDRSS_CTL_70	DDR Controller Register 70	0299 0118h
11Ch	DDRSS_CTL_71	DDR Controller Register 71	0299 011Ch
120h	DDRSS_CTL_72	DDR Controller Register 72	0299 0120h
124h	DDRSS_CTL_73	DDR Controller Register 73	0299 0124h
128h	DDRSS_CTL_74	DDR Controller Register 74	0299 0128h
12Ch	DDRSS_CTL_75	DDR Controller Register 75	0299 012Ch
130h	DDRSS_CTL_76	DDR Controller Register 76	0299 0130h
134h	DDRSS_CTL_77	DDR Controller Register 77	0299 0134h
138h	DDRSS_CTL_78	DDR Controller Register 78	0299 0138h
13Ch	DDRSS_CTL_79	DDR Controller Register 79	0299 013Ch
140h	DDRSS_CTL_80	DDR Controller Register 80	0299 0140h
144h	DDRSS_CTL_81	DDR Controller Register 81	0299 0144h
148h	DDRSS_CTL_82	DDR Controller Register 82	0299 0148h
14Ch	DDRSS_CTL_83	DDR Controller Register 83	0299 014Ch
150h	DDRSS_CTL_84	DDR Controller Register 84	0299 0150h
154h	DDRSS_CTL_85	DDR Controller Register 85	0299 0154h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
158h	DDRSS_CTL_86	DDR Controller Register 86	0299 0158h
15Ch	DDRSS_CTL_87	DDR Controller Register 87	0299 015Ch
160h	DDRSS_CTL_88	DDR Controller Register 88	0299 0160h
164h	DDRSS_CTL_89	DDR Controller Register 89	0299 0164h
168h	DDRSS_CTL_90	DDR Controller Register 90	0299 0168h
16Ch	DDRSS_CTL_91	DDR Controller Register 91	0299 016Ch
170h	DDRSS_CTL_92	DDR Controller Register 92	0299 0170h
178h	DDRSS_CTL_94	DDR Controller Register 94	0299 0178h
17Ch	DDRSS_CTL_95	DDR Controller Register 95	0299 017Ch
180h	DDRSS_CTL_96	DDR Controller Register 96	0299 0180h
184h	DDRSS_CTL_97	DDR Controller Register 97	0299 0184h
188h	DDRSS_CTL_98	DDR Controller Register 98	0299 0188h
18Ch	DDRSS_CTL_99	DDR Controller Register 99	0299 018Ch
190h	DDRSS_CTL_100	DDR Controller Register 100	0299 0190h
194h	DDRSS_CTL_101	DDR Controller Register 101	0299 0194h
198h	DDRSS_CTL_102	DDR Controller Register 102	0299 0198h
19Ch	DDRSS_CTL_103	DDR Controller Register 103	0299 019Ch
1A0h	DDRSS_CTL_104	DDR Controller Register 104	0299 01A0h
1A4h	DDRSS_CTL_105	DDR Controller Register 105	0299 01A4h
1A8h	DDRSS_CTL_106	DDR Controller Register 106	0299 01A8h
1ACh	DDRSS_CTL_107	DDR Controller Register 107	0299 01ACh
1B0h	DDRSS_CTL_108	DDR Controller Register 108	0299 01B0h
1B4h	DDRSS_CTL_109	DDR Controller Register 109	0299 01B4h
1B8h	DDRSS_CTL_110	DDR Controller Register 110	0299 01B8h
1BCh	DDRSS_CTL_111	DDR Controller Register 111	0299 01BCh
1C0h	DDRSS_CTL_112	DDR Controller Register 112	0299 01C0h
1C4h	DDRSS_CTL_113	DDR Controller Register 113	0299 01C4h
1C8h	DDRSS_CTL_114	DDR Controller Register 114	0299 01C8h
1CCh	DDRSS_CTL_115	DDR Controller Register 115	0299 01CCh
1D0h	DDRSS_CTL_116	DDR Controller Register 116	0299 01D0h
1D4h	DDRSS_CTL_117	DDR Controller Register 117	0299 01D4h
1D8h	DDRSS_CTL_118	DDR Controller Register 118	0299 01D8h
1DCh	DDRSS_CTL_119	DDR Controller Register 119	0299 01DCh
1E0h	DDRSS_CTL_120	DDR Controller Register 120	0299 01E0h
1E4h	DDRSS_CTL_121	DDR Controller Register 121	0299 01E4h
1E8h	DDRSS_CTL_122	DDR Controller Register 122	0299 01E8h
1ECh	DDRSS_CTL_123	DDR Controller Register 123	0299 01ECh
1F0h	DDRSS_CTL_124	DDR Controller Register 124	0299 01F0h
1F4h	DDRSS_CTL_125	DDR Controller Register 125	0299 01F4h
1F8h	DDRSS_CTL_126	DDR Controller Register 126	0299 01F8h
1FCh	DDRSS_CTL_127	DDR Controller Register 127	0299 01FCh
200h	DDRSS_CTL_128	DDR Controller Register 128	0299 0200h
204h	DDRSS_CTL_129	DDR Controller Register 129	0299 0204h
208h	DDRSS_CTL_130	DDR Controller Register 130	0299 0208h
20Ch	DDRSS_CTL_131	DDR Controller Register 131	0299 020Ch
210h	DDRSS_CTL_132	DDR Controller Register 132	0299 0210h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
214h	DDRSS_CTL_133	DDR Controller Register 133	0299 0214h
218h	DDRSS_CTL_134	DDR Controller Register 134	0299 0218h
21Ch	DDRSS_CTL_135	DDR Controller Register 135	0299 021Ch
220h	DDRSS_CTL_136	DDR Controller Register 136	0299 0220h
224h	DDRSS_CTL_137	DDR Controller Register 137	0299 0224h
228h	DDRSS_CTL_138	DDR Controller Register 138	0299 0228h
22Ch	DDRSS_CTL_139	DDR Controller Register 139	0299 022Ch
230h	DDRSS_CTL_140	DDR Controller Register 140	0299 0230h
234h	DDRSS_CTL_141	DDR Controller Register 141	0299 0234h
238h	DDRSS_CTL_142	DDR Controller Register 142	0299 0238h
23Ch	DDRSS_CTL_143	DDR Controller Register 143	0299 023Ch
240h	DDRSS_CTL_144	DDR Controller Register 144	0299 0240h
244h	DDRSS_CTL_145	DDR Controller Register 145	0299 0244h
248h	DDRSS_CTL_146	DDR Controller Register 146	0299 0248h
24Ch	DDRSS_CTL_147	DDR Controller Register 147	0299 024Ch
250h	DDRSS_CTL_148	DDR Controller Register 148	0299 0250h
254h	DDRSS_CTL_149	DDR Controller Register 149	0299 0254h
258h	DDRSS_CTL_150	DDR Controller Register 150	0299 0258h
25Ch	DDRSS_CTL_151	DDR Controller Register 151	0299 025Ch
260h	DDRSS_CTL_152	DDR Controller Register 152	0299 0260h
264h	DDRSS_CTL_153	DDR Controller Register 153	0299 0264h
268h	DDRSS_CTL_154	DDR Controller Register 154	0299 0268h
26Ch	DDRSS_CTL_155	DDR Controller Register 155	0299 026Ch
270h	DDRSS_CTL_156	DDR Controller Register 156	0299 0270h
274h	DDRSS_CTL_157	DDR Controller Register 157	0299 0274h
278h	DDRSS_CTL_158	DDR Controller Register 158	0299 0278h
27Ch	DDRSS_CTL_159	DDR Controller Register 159	0299 027Ch
280h	DDRSS_CTL_160	DDR Controller Register 160	0299 0280h
284h	DDRSS_CTL_161	DDR Controller Register 161	0299 0284h
288h	DDRSS_CTL_162	DDR Controller Register 162	0299 0288h
28Ch	DDRSS_CTL_163	DDR Controller Register 163	0299 028Ch
290h	DDRSS_CTL_164	DDR Controller Register 164	0299 0290h
294h	DDRSS_CTL_165	DDR Controller Register 165	0299 0294h
298h	DDRSS_CTL_166	DDR Controller Register 166	0299 0298h
29Ch	DDRSS_CTL_167	DDR Controller Register 167	0299 029Ch
2A0h	DDRSS_CTL_168	DDR Controller Register 168	0299 02A0h
2A4h	DDRSS_CTL_169	DDR Controller Register 169	0299 02A4h
2A8h	DDRSS_CTL_170	DDR Controller Register 170	0299 02A8h
2ACh	DDRSS_CTL_171	DDR Controller Register 171	0299 02ACh
2B0h	DDRSS_CTL_172	DDR Controller Register 172	0299 02B0h
2B4h	DDRSS_CTL_173	DDR Controller Register 173	0299 02B4h
2B8h	DDRSS_CTL_174	DDR Controller Register 174	0299 02B8h
2BCh	DDRSS_CTL_175	DDR Controller Register 175	0299 02BCh
2C0h	DDRSS_CTL_176	DDR Controller Register 176	0299 02C0h
2C4h	DDRSS_CTL_177	DDR Controller Register 177	0299 02C4h
2C8h	DDRSS_CTL_178	DDR Controller Register 178	0299 02C8h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
2CCh	DDRSS_CTL_179	DDR Controller Register 179	0299 02CCh
2D0h	DDRSS_CTL_180	DDR Controller Register 180	0299 02D0h
2D4h	DDRSS_CTL_181	DDR Controller Register 181	0299 02D4h
2D8h	DDRSS_CTL_182	DDR Controller Register 182	0299 02D8h
2DCh	DDRSS_CTL_183	DDR Controller Register 183	0299 02DCh
2E0h	DDRSS_CTL_184	DDR Controller Register 184	0299 02E0h
2E4h	DDRSS_CTL_185	DDR Controller Register 185	0299 02E4h
2E8h	DDRSS_CTL_186	DDR Controller Register 186	0299 02E8h
2ECh	DDRSS_CTL_187	DDR Controller Register 187	0299 02ECh
2F0h	DDRSS_CTL_188	DDR Controller Register 188	0299 02F0h
2F4h	DDRSS_CTL_189	DDR Controller Register 189	0299 02F4h
2F8h	DDRSS_CTL_190	DDR Controller Register 190	0299 02F8h
2FCh	DDRSS_CTL_191	DDR Controller Register 191	0299 02FCh
300h	DDRSS_CTL_192	DDR Controller Register 192	0299 0300h
304h	DDRSS_CTL_193	DDR Controller Register 193	0299 0304h
308h	DDRSS_CTL_194	DDR Controller Register 194	0299 0308h
30Ch	DDRSS_CTL_195	DDR Controller Register 195	0299 030Ch
310h	DDRSS_CTL_196	DDR Controller Register 196	0299 0310h
314h	DDRSS_CTL_197	DDR Controller Register 197	0299 0314h
318h	DDRSS_CTL_198	DDR Controller Register 198	0299 0318h
31Ch	DDRSS_CTL_199	DDR Controller Register 199	0299 031Ch
320h	DDRSS_CTL_200	DDR Controller Register 200	0299 0320h
324h	DDRSS_CTL_201	DDR Controller Register 201	0299 0324h
328h	DDRSS_CTL_202	DDR Controller Register 202	0299 0328h
32Ch	DDRSS_CTL_203	DDR Controller Register 203	0299 032Ch
330h	DDRSS_CTL_204	DDR Controller Register 204	0299 0330h
334h	DDRSS_CTL_205	DDR Controller Register 205	0299 0334h
338h	DDRSS_CTL_206	DDR Controller Register 206	0299 0338h
33Ch	DDRSS_CTL_207	DDR Controller Register 207	0299 033Ch
340h	DDRSS_CTL_208	DDR Controller Register 208	0299 0340h
344h	DDRSS_CTL_209	DDR Controller Register 209	0299 0344h
348h	DDRSS_CTL_210	DDR Controller Register 210	0299 0348h
34Ch	DDRSS_CTL_211	DDR Controller Register 211	0299 034Ch
350h	DDRSS_CTL_212	DDR Controller Register 212	0299 0350h
354h	DDRSS_CTL_213	DDR Controller Register 213	0299 0354h
358h	DDRSS_CTL_214	DDR Controller Register 214	0299 0358h
35Ch	DDRSS_CTL_215	DDR Controller Register 215	0299 035Ch
360h	DDRSS_CTL_216	DDR Controller Register 216	0299 0360h
364h	DDRSS_CTL_217	DDR Controller Register 217	0299 0364h
368h	DDRSS_CTL_218	DDR Controller Register 218	0299 0368h
36Ch	DDRSS_CTL_219	DDR Controller Register 219	0299 036Ch
370h	DDRSS_CTL_220	DDR Controller Register 220	0299 0370h
374h	DDRSS_CTL_221	DDR Controller Register 221	0299 0374h
378h	DDRSS_CTL_222	DDR Controller Register 222	0299 0378h
37Ch	DDRSS_CTL_223	DDR Controller Register 223	0299 037Ch
380h	DDRSS_CTL_224	DDR Controller Register 224	0299 0380h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
384h	DDRSS_CTL_225	DDR Controller Register 225	0299 0384h
388h	DDRSS_CTL_226	DDR Controller Register 226	0299 0388h
38Ch	DDRSS_CTL_227	DDR Controller Register 227	0299 038Ch
390h	DDRSS_CTL_228	DDR Controller Register 228	0299 0390h
394h	DDRSS_CTL_229	DDR Controller Register 229	0299 0394h
398h	DDRSS_CTL_230	DDR Controller Register 230	0299 0398h
39Ch	DDRSS_CTL_231	DDR Controller Register 231	0299 039Ch
3A0h	DDRSS_CTL_232	DDR Controller Register 232	0299 03A0h
3A4h	DDRSS_CTL_233	DDR Controller Register 233	0299 03A4h
3A8h	DDRSS_CTL_234	DDR Controller Register 234	0299 03A8h
3ACh	DDRSS_CTL_235	DDR Controller Register 235	0299 03ACh
3B0h	DDRSS_CTL_236	DDR Controller Register 236	0299 03B0h
3B4h	DDRSS_CTL_237	DDR Controller Register 237	0299 03B4h
3B8h	DDRSS_CTL_238	DDR Controller Register 238	0299 03B8h
3BCh	DDRSS_CTL_239	DDR Controller Register 239	0299 03BCh
3C0h	DDRSS_CTL_240	DDR Controller Register 240	0299 03C0h
3C4h	DDRSS_CTL_241	DDR Controller Register 241	0299 03C4h
3C8h	DDRSS_CTL_242	DDR Controller Register 242	0299 03C8h
3CCh	DDRSS_CTL_243	DDR Controller Register 243	0299 03CCh
3D0h	DDRSS_CTL_244	DDR Controller Register 244	0299 03D0h
3D4h	DDRSS_CTL_245	DDR Controller Register 245	0299 03D4h
3D8h	DDRSS_CTL_246	DDR Controller Register 246	0299 03D8h
3DCh	DDRSS_CTL_247	DDR Controller Register 247	0299 03DCh
3E0h	DDRSS_CTL_248	DDR Controller Register 248	0299 03E0h
3E4h	DDRSS_CTL_249	DDR Controller Register 249	0299 03E4h
3E8h	DDRSS_CTL_250	DDR Controller Register 250	0299 03E8h
3ECh	DDRSS_CTL_251	DDR Controller Register 251	0299 03ECh
3F0h	DDRSS_CTL_252	DDR Controller Register 252	0299 03F0h
3F4h	DDRSS_CTL_253	DDR Controller Register 253	0299 03F4h
3F8h	DDRSS_CTL_254	DDR Controller Register 254	0299 03F8h
3FCh	DDRSS_CTL_255	DDR Controller Register 255	0299 03FCh
400h	DDRSS_CTL_256	DDR Controller Register 256	0299 0400h
404h	DDRSS_CTL_257	DDR Controller Register 257	0299 0404h
408h	DDRSS_CTL_258	DDR Controller Register 258	0299 0408h
40Ch	DDRSS_CTL_259	DDR Controller Register 259	0299 040Ch
410h	DDRSS_CTL_260	DDR Controller Register 260	0299 0410h
414h	DDRSS_CTL_261	DDR Controller Register 261	0299 0414h
418h	DDRSS_CTL_262	DDR Controller Register 262	0299 0418h
41Ch	DDRSS_CTL_263	DDR Controller Register 263	0299 041Ch
420h	DDRSS_CTL_264	DDR Controller Register 264	0299 0420h
424h	DDRSS_CTL_265	DDR Controller Register 265	0299 0424h
428h	DDRSS_CTL_266	DDR Controller Register 266	0299 0428h
42Ch	DDRSS_CTL_267	DDR Controller Register 267	0299 042Ch
430h	DDRSS_CTL_268	DDR Controller Register 268	0299 0430h
434h	DDRSS_CTL_269	DDR Controller Register 269	0299 0434h
438h	DDRSS_CTL_270	DDR Controller Register 270	0299 0438h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG Physical Address
43Ch	DDRSS_CTL_271	DDR Controller Register 271	0299 043Ch
440h	DDRSS_CTL_272	DDR Controller Register 272	0299 0440h
444h	DDRSS_CTL_273	DDR Controller Register 273	0299 0444h
448h	DDRSS_CTL_274	DDR Controller Register 274	0299 0448h
44Ch	DDRSS_CTL_275	DDR Controller Register 275	0299 044Ch
450h	DDRSS_CTL_276	DDR Controller Register 276	0299 0450h
454h	DDRSS_CTL_277	DDR Controller Register 277	0299 0454h
458h	DDRSS_CTL_278	DDR Controller Register 278	0299 0458h
45Ch	DDRSS_CTL_279	DDR Controller Register 279	0299 045Ch
460h	DDRSS_CTL_280	DDR Controller Register 280	0299 0460h
464h	DDRSS_CTL_281	DDR Controller Register 281	0299 0464h
468h	DDRSS_CTL_282	DDR Controller Register 282	0299 0468h
46Ch	DDRSS_CTL_283	DDR Controller Register 283	0299 046Ch
470h	DDRSS_CTL_284	DDR Controller Register 284	0299 0470h
474h	DDRSS_CTL_285	DDR Controller Register 285	0299 0474h
478h	DDRSS_CTL_286	DDR Controller Register 286	0299 0478h
47Ch	DDRSS_CTL_287	DDR Controller Register 287	0299 047Ch
480h	DDRSS_CTL_288	DDR Controller Register 288	0299 0480h
484h	DDRSS_CTL_289	DDR Controller Register 289	0299 0484h
488h	DDRSS_CTL_290	DDR Controller Register 290	0299 0488h
48Ch	DDRSS_CTL_291	DDR Controller Register 291	0299 048Ch
490h	DDRSS_CTL_292	DDR Controller Register 292	0299 0490h
494h	DDRSS_CTL_293	DDR Controller Register 293	0299 0494h
498h	DDRSS_CTL_294	DDR Controller Register 294	0299 0498h
49Ch	DDRSS_CTL_295	DDR Controller Register 295	0299 049Ch
4A0h	DDRSS_CTL_296	DDR Controller Register 296	0299 04A0h
4A4h	DDRSS_CTL_297	DDR Controller Register 297	0299 04A4h
4A8h	DDRSS_CTL_298	DDR Controller Register 298	0299 04A8h
4ACh	DDRSS_CTL_299	DDR Controller Register 299	0299 04ACh
4B0h	DDRSS_CTL_300	DDR Controller Register 300	0299 04B0h
4B4h	DDRSS_CTL_301	DDR Controller Register 301	0299 04B4h
4B8h	DDRSS_CTL_302	DDR Controller Register 302	0299 04B8h
4BCh	DDRSS_CTL_303	DDR Controller Register 303	0299 04BCh
4C0h	DDRSS_CTL_304	DDR Controller Register 304	0299 04C0h
4C4h	DDRSS_CTL_305	DDR Controller Register 305	0299 04C4h
4C8h	DDRSS_CTL_306	DDR Controller Register 306	0299 04C8h
4CCh	DDRSS_CTL_307	DDR Controller Register 307	0299 04CCh
4D0h	DDRSS_CTL_308	DDR Controller Register 308	0299 04D0h
4D4h	DDRSS_CTL_309	DDR Controller Register 309	0299 04D4h
4D8h	DDRSS_CTL_310	DDR Controller Register 310	0299 04D8h
4DCh	DDRSS_CTL_311	DDR Controller Register 311	0299 04DCh
4E0h	DDRSS_CTL_312	DDR Controller Register 312	0299 04E0h
4E4h	DDRSS_CTL_313	DDR Controller Register 313	0299 04E4h
4E8h	DDRSS_CTL_314	DDR Controller Register 314	0299 04E8h
4ECh	DDRSS_CTL_315	DDR Controller Register 315	0299 04ECh
4F0h	DDRSS_CTL_316	DDR Controller Register 316	0299 04F0h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
4F4h	DDRSS_CTL_317	DDR Controller Register 317	0299 04F4h
4F8h	DDRSS_CTL_318	DDR Controller Register 318	0299 04F8h
4FCh	DDRSS_CTL_319	DDR Controller Register 319	0299 04FCh
500h	DDRSS_CTL_320	DDR Controller Register 320	0299 0500h
504h	DDRSS_CTL_321	DDR Controller Register 321	0299 0504h
508h	DDRSS_CTL_322	DDR Controller Register 322	0299 0508h
50Ch	DDRSS_CTL_323	DDR Controller Register 323	0299 050Ch
510h	DDRSS_CTL_324	DDR Controller Register 324	0299 0510h
514h	DDRSS_CTL_325	DDR Controller Register 325	0299 0514h
518h	DDRSS_CTL_326	DDR Controller Register 326	0299 0518h
51Ch	DDRSS_CTL_327	DDR Controller Register 327	0299 051Ch
520h	DDRSS_CTL_328	DDR Controller Register 328	0299 0520h
524h	DDRSS_CTL_329	DDR Controller Register 329	0299 0524h
528h	DDRSS_CTL_330	DDR Controller Register 330	0299 0528h
52Ch	DDRSS_CTL_331	DDR Controller Register 331	0299 052Ch
530h	DDRSS_CTL_332	DDR Controller Register 332	0299 0530h
534h	DDRSS_CTL_333	DDR Controller Register 333	0299 0534h
538h	DDRSS_CTL_334	DDR Controller Register 334	0299 0538h
53Ch	DDRSS_CTL_335	DDR Controller Register 335	0299 053Ch
540h	DDRSS_CTL_336	DDR Controller Register 336	0299 0540h
544h	DDRSS_CTL_337	DDR Controller Register 337	0299 0544h
548h	DDRSS_CTL_338	DDR Controller Register 338	0299 0548h
54Ch	DDRSS_CTL_339	DDR Controller Register 339	0299 054Ch
550h	DDRSS_CTL_340	DDR Controller Register 340	0299 0550h
554h	DDRSS_CTL_341	DDR Controller Register 341	0299 0554h
558h	DDRSS_CTL_342	DDR Controller Register 342	0299 0558h
55Ch	DDRSS_CTL_343	DDR Controller Register 343	0299 055Ch
560h	DDRSS_CTL_344	DDR Controller Register 344	0299 0560h
564h	DDRSS_CTL_345	DDR Controller Register 345	0299 0564h
568h	DDRSS_CTL_346	DDR Controller Register 346	0299 0568h
56Ch	DDRSS_CTL_347	DDR Controller Register 347	0299 056Ch
570h	DDRSS_CTL_348	DDR Controller Register 348	0299 0570h
574h	DDRSS_CTL_349	DDR Controller Register 349	0299 0574h
578h	DDRSS_CTL_350	DDR Controller Register 350	0299 0578h
57Ch	DDRSS_CTL_351	DDR Controller Register 351	0299 057Ch
580h	DDRSS_CTL_352	DDR Controller Register 352	0299 0580h
584h	DDRSS_CTL_353	DDR Controller Register 353	0299 0584h
588h	DDRSS_CTL_354	DDR Controller Register 354	0299 0588h
58Ch	DDRSS_CTL_355	DDR Controller Register 355	0299 058Ch
590h	DDRSS_CTL_356	DDR Controller Register 356	0299 0590h
594h	DDRSS_CTL_357	DDR Controller Register 357	0299 0594h
598h	DDRSS_CTL_358	DDR Controller Register 358	0299 0598h
59Ch	DDRSS_CTL_359	DDR Controller Register 359	0299 059Ch
5A0h	DDRSS_CTL_360	DDR Controller Register 360	0299 05A0h
5A4h	DDRSS_CTL_361	DDR Controller Register 361	0299 05A4h
5A8h	DDRSS_CTL_362	DDR Controller Register 362	0299 05A8h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG Physical Address
5ACh	DDRSS_CTL_363	DDR Controller Register 363	0299 05ACh
5B0h	DDRSS_CTL_364	DDR Controller Register 364	0299 05B0h
5B4h	DDRSS_CTL_365	DDR Controller Register 365	0299 05B4h
5B8h	DDRSS_CTL_366	DDR Controller Register 366	0299 05B8h
5BCh	DDRSS_CTL_367	DDR Controller Register 367	0299 05BCh
5C0h	DDRSS_CTL_368	DDR Controller Register 368	0299 05C0h
5C4h	DDRSS_CTL_369	DDR Controller Register 369	0299 05C4h
5C8h	DDRSS_CTL_370	DDR Controller Register 370	0299 05C8h
5CCh	DDRSS_CTL_371	DDR Controller Register 371	0299 05CCh
5D0h	DDRSS_CTL_372	DDR Controller Register 372	0299 05D0h
5D4h	DDRSS_CTL_373	DDR Controller Register 373	0299 05D4h
5D8h	DDRSS_CTL_374	DDR Controller Register 374	0299 05D8h
5DCh	DDRSS_CTL_375	DDR Controller Register 375	0299 05DCh
5E0h	DDRSS_CTL_376	DDR Controller Register 376	0299 05E0h
5E4h	DDRSS_CTL_377	DDR Controller Register 377	0299 05E4h
5E8h	DDRSS_CTL_378	DDR Controller Register 378	0299 05E8h
5ECh	DDRSS_CTL_379	DDR Controller Register 379	0299 05ECh
5F0h	DDRSS_CTL_380	DDR Controller Register 380	0299 05F0h
5F4h	DDRSS_CTL_381	DDR Controller Register 381	0299 05F4h
5F8h	DDRSS_CTL_382	DDR Controller Register 382	0299 05F8h
5FCh	DDRSS_CTL_383	DDR Controller Register 383	0299 05FCh
600h	DDRSS_CTL_384	DDR Controller Register 384	0299 0600h
604h	DDRSS_CTL_385	DDR Controller Register 385	0299 0604h
608h	DDRSS_CTL_386	DDR Controller Register 386	0299 0608h
60Ch	DDRSS_CTL_387	DDR Controller Register 387	0299 060Ch
610h	DDRSS_CTL_388	DDR Controller Register 388	0299 0610h
614h	DDRSS_CTL_389	DDR Controller Register 389	0299 0614h
618h	DDRSS_CTL_390	DDR Controller Register 390	0299 0618h
61Ch	DDRSS_CTL_391	DDR Controller Register 391	0299 061Ch
620h	DDRSS_CTL_392	DDR Controller Register 392	0299 0620h
624h	DDRSS_CTL_393	DDR Controller Register 393	0299 0624h
628h	DDRSS_CTL_394	DDR Controller Register 394	0299 0628h
62Ch	DDRSS_CTL_395	DDR Controller Register 395	0299 062Ch
630h	DDRSS_CTL_396	DDR Controller Register 396	0299 0630h
634h	DDRSS_CTL_397	DDR Controller Register 397	0299 0634h
638h	DDRSS_CTL_398	DDR Controller Register 398	0299 0638h
63Ch	DDRSS_CTL_399	DDR Controller Register 399	0299 063Ch
640h	DDRSS_CTL_400	DDR Controller Register 400	0299 0640h
644h	DDRSS_CTL_401	DDR Controller Register 401	0299 0644h
648h	DDRSS_CTL_402	DDR Controller Register 402	0299 0648h
64Ch	DDRSS_CTL_403	DDR Controller Register 403	0299 064Ch
650h	DDRSS_CTL_404	DDR Controller Register 404	0299 0650h
654h	DDRSS_CTL_405	DDR Controller Register 405	0299 0654h
658h	DDRSS_CTL_406	DDR Controller Register 406	0299 0658h
65Ch	DDRSS_CTL_407	DDR Controller Register 407	0299 065Ch
660h	DDRSS_CTL_408	DDR Controller Register 408	0299 0660h

Table 4-102. DDR Controller Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG Physical Address
664h	DDRSS_CTL_409	DDR Controller Register 409	0299 0664h
668h	DDRSS_CTL_410	DDR Controller Register 410	0299 0668h
66Ch	DDRSS_CTL_411	DDR Controller Register 411	0299 066Ch
670h	DDRSS_CTL_412	DDR Controller Register 412	0299 0670h
674h	DDRSS_CTL_413	DDR Controller Register 413	0299 0674h
678h	DDRSS_CTL_414	DDR Controller Register 414	0299 0678h
67Ch	DDRSS_CTL_415	DDR Controller Register 415	0299 067Ch
680h	DDRSS_CTL_416	DDR Controller Register 416	0299 0680h
684h	DDRSS_CTL_417	DDR Controller Register 417	0299 0684h
688h	DDRSS_CTL_418	DDR Controller Register 418	0299 0688h
68Ch	DDRSS_CTL_419	DDR Controller Register 419	0299 068Ch
690h	DDRSS_CTL_420	DDR Controller Register 420	0299 0690h
694h	DDRSS_CTL_421	DDR Controller Register 421	0299 0694h
698h	DDRSS_CTL_422	DDR Controller Register 422	0299 0698h
69Ch	DDRSS_CTL_423	DDR Controller Register 423	0299 069Ch
6A0h	DDRSS_CTL_424	DDR Controller Register 424	0299 06A0h
6A4h	DDRSS_CTL_425	DDR Controller Register 425	0299 06A4h
6A8h	DDRSS_CTL_426	DDR Controller Register 426	0299 06A8h
6ACh	DDRSS_CTL_427	DDR Controller Register 427	0299 06ACh
6B0h	DDRSS_CTL_428	DDR Controller Register 428	0299 06B0h
6B4h	DDRSS_CTL_429	DDR Controller Register 429	0299 06B4h
6B8h	DDRSS_CTL_430	DDR Controller Register 430	0299 06B8h
6D4h	DDRSS_CTL_437	DDR Controller Register 437	0299 06D4h
6D8h	DDRSS_CTL_438	DDR Controller Register 438	0299 06D8h
6DCh	DDRSS_CTL_439	DDR Controller Register 439	0299 06DCh
6E0h	DDRSS_CTL_440	DDR Controller Register 440	0299 06E0h
6E4h	DDRSS_CTL_441	DDR Controller Register 441	0299 06E4h
6E8h	DDRSS_CTL_442	DDR Controller Register 442	0299 06E8h
6ECh	DDRSS_CTL_443	DDR Controller Register 443	0299 06ECh
6F0h	DDRSS_CTL_444	DDR Controller Register 444	0299 06F0h
6FCh	DDRSS_CTL_447	DDR Controller Register 447	0299 06FCh
700h	DDRSS_CTL_448	DDR Controller Register 448	0299 0700h
704h	DDRSS_CTL_449	DDR Controller Register 449	0299 0704h
708h	DDRSS_CTL_450	DDR Controller Register 450	0299 0708h
71Ch	DDRSS_CTL_455	DDR Controller Register 455	0299 071Ch
720h	DDRSS_CTL_456	DDR Controller Register 456	0299 0720h
724h	DDRSS_CTL_457	DDR Controller Register 457	0299 0724h
728h	DDRSS_CTL_458	DDR Controller Register 458	0299 0728h

4.2.1 DDRSS_CTL_0 Register (Offset = 0h) [reset = X]

DDRSS_CTL_0 is shown in [Figure 4-50](#) and described in [Table 4-104](#).

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Table 4-103. DDRSS_CTL_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0000h

Figure 4-50. DDRSS_CTL_0 Register

31	30	29	28	27	26	25	24
CONTROLLER_ID							
R-1046h							
23	22	21	20	19	18	17	16
CONTROLLER_ID							
R-1046h							
15	14	13	12	11	10	9	8
RESERVED				DRAM_CLASS			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							START
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-104. DDRSS_CTL_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CONTROLLER_ID	R	1046h	Holds the controller product id number. READ-ONLY
15-12	RESERVED	R/W	X	
11-8	DRAM_CLASS	R/W	0h	Defines the class of DRAM memory which is connected to the controller. 7h - LPDDR3 Bh - LPDDR4 All other values reserved
7-1	RESERVED	R/W	X	
0	START	R/W	0h	Initiate command processing in the controller. Set to 1 to initiate.

4.2.2 DDRSS_CTL_1 Register (Offset = 4h) [reset = 54D5DA40h]

DDRSS_CTL_1 is shown in [Figure 4-51](#) and described in [Table 4-106](#).

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Table 4-105. DDRSS_CTL_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0004h

Figure 4-51. DDRSS_CTL_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROLLER_VERSION_0																															
R-54D5DA40h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-106. DDRSS_CTL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CONTROLLER_VERSION_0	R	54D5DA40h	Holds the controller version id. READ-ONLY

4.2.3 DDRSS_CTL_2 Register (Offset = 8h) [reset = 0C1865A1h]

DDRSS_CTL_2 is shown in [Figure 4-52](#) and described in [Table 4-108](#).

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Table 4-107. DDRSS_CTL_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0008h

Figure 4-52. DDRSS_CTL_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROLLER_VERSION_1																															
R-0C1865A1h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-108. DDRSS_CTL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CONTROLLER_VERSION_1	R	0C1865A1h	Holds the controller version id. READ-ONLY

4.2.4 DDRSS_CTL_3 Register (Offset = Ch) [reset = X]

DDRSS_CTL_3 is shown in [Figure 4-53](#) and described in [Table 4-110](#).

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Table 4-109. DDRSS_CTL_3 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 000Ch

Figure 4-53. DDRSS_CTL_3 Register

31	30	29	28	27	26	25	24
READ_DATA_FIFO_DEPTH							
R-40h							
23	22	21	20	19	18	17	16
RESERVED						MAX_CS_REG	
R-X						R-2h	
15	14	13	12	11	10	9	8
RESERVED				MAX_COL_REG			
R-X				R-Ch			
7	6	5	4	3	2	1	0
RESERVED			MAX_ROW_REG				
R-X			R-11h				

LEGEND: R = Read Only; -n = value after reset

Table 4-110. DDRSS_CTL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	READ_DATA_FIFO_DEPTH	R	40h	Reports the depth of the controller core read data queue. READ-ONLY
23-18	RESERVED	R	X	
17-16	MAX_CS_REG	R	2h	Holds the maximum number of chip selects available. READ-ONLY
15-12	RESERVED	R	X	
11-8	MAX_COL_REG	R	Ch	Holds the maximum width of column address in DRAMs. READ-ONLY
7-5	RESERVED	R	X	
4-0	MAX_ROW_REG	R	11h	Holds the maximum width of memory address bus. READ-ONLY

4.2.5 DDRSS_CTL_4 Register (Offset = 10h) [reset = X]

DDRSS_CTL_4 is shown in [Figure 4-54](#) and described in [Table 4-112](#).

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Table 4-111. DDRSS_CTL_4 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0010h

Figure 4-54. DDRSS_CTL_4 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
WRITE_DATA_FIFO_PTR_WIDTH							
R-5h							
15	14	13	12	11	10	9	8
WRITE_DATA_FIFO_DEPTH							
R-20h							
7	6	5	4	3	2	1	0
READ_DATA_FIFO_PTR_WIDTH							
R-6h							

LEGEND: R = Read Only; -n = value after reset

Table 4-112. DDRSS_CTL_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	WRITE_DATA_FIFO_PTR_WIDTH	R	5h	Reports the width of the controller core write data latency queue pointer. READ-ONLY
15-8	WRITE_DATA_FIFO_DEPTH	R	20h	Reports the depth of the controller core write data latency queue. READ-ONLY
7-0	READ_DATA_FIFO_PTR_WIDTH	R	6h	Reports the width of the controller core read data queue pointer. READ-ONLY

4.2.6 DDRSS_CTL_5 Register (Offset = 14h) [reset = 02050020h]

DDRSS_CTL_5 is shown in [Figure 4-55](#) and described in [Table 4-114](#).

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Table 4-113. DDRSS_CTL_5 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0014h

Figure 4-55. DDRSS_CTL_5 Register

31	30	29	28	27	26	25	24
ASYNC_CDC_STAGES							
R-2h							
23	22	21	20	19	18	17	16
MEMCD_RMODW_FIFO_PTR_WIDTH							
R-5h							
15	14	13	12	11	10	9	8
MEMCD_RMODW_FIFO_DEPTH							
R-20h							
7	6	5	4	3	2	1	0
MEMCD_RMODW_FIFO_DEPTH							
R-20h							

LEGEND: R = Read Only; -n = value after reset

Table 4-114. DDRSS_CTL_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	ASYNC_CDC_STAGES	R	2h	Reports the number of synchronizer delays specified for the asynchronous boundary crossings. READ-ONLY
23-16	MEMCD_RMODW_FIFO_PTR_WIDTH	R	5h	Reports the width of the controller core read/modify/write FIFO pointer. READ-ONLY
15-0	MEMCD_RMODW_FIFO_DEPTH	R	20h	Reports the depth of the controller core read/modify/write FIFO. READ-ONLY

4.2.7 DDRSS_CTL_6 Register (Offset = 18h) [reset = 03070101h]

DDRSS_CTL_6 is shown in [Figure 4-56](#) and described in [Table 4-116](#).

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Table 4-115. DDRSS_CTL_6 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0018h

Figure 4-56. DDRSS_CTL_6 Register

31	30	29	28	27	26	25	24
AXI0_WRCMD_PROC_FIFO_LOG2_DEPTH							
R-3h							
23	22	21	20	19	18	17	16
AXI0_WR_ARRAY_LOG2_DEPTH							
R-7h							
15	14	13	12	11	10	9	8
AXI0_RDFIFO_LOG2_DEPTH							
R-1h							
7	6	5	4	3	2	1	0
AXI0_CMDFIFO_LOG2_DEPTH							
R-1h							

LEGEND: R = Read Only; -n = value after reset

Table 4-116. DDRSS_CTL_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	AXI0_WRCMD_PROC_FIFO_LOG2_DEPTH	R	3h	Reports the depth of the AXI port 0 write command processing FIFO. Value is the log2 value of the depth. READ-ONLY
23-16	AXI0_WR_ARRAY_LOG2_DEPTH	R	7h	Reports the depth of the AXI port 0 write data array. Value is the log2 value of the depth. READ-ONLY
15-8	AXI0_RDFIFO_LOG2_DEPTH	R	1h	Reports the depth of the AXI port 0 read data FIFO. Value is the log2 value of the depth. READ-ONLY
7-0	AXI0_CMDFIFO_LOG2_DEPTH	R	1h	Reports the depth of the AXI port 0 command FIFO. Value is the log2 value of the depth. READ-ONLY

4.2.8 DDRSS_CTL_7 Register (Offset = 1Ch) [reset = X]

DDRSS_CTL_7 is shown in [Figure 4-57](#) and described in [Table 4-118](#).

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Table 4-117. DDRSS_CTL_7 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 001Ch

Figure 4-57. DDRSS_CTL_7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-118. DDRSS_CTL_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT_F0	R/W	0h	DRAM TINIT value for frequency copy 0 in cycles.

4.2.9 DDRSS_CTL_8 Register (Offset = 20h) [reset = X]

DDRSS_CTL_8 is shown in [Figure 4-58](#) and described in [Table 4-120](#).

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Table 4-119. DDRSS_CTL_8 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0020h

Figure 4-58. DDRSS_CTL_8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT3_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-120. DDRSS_CTL_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT3_F0	R/W	0h	DRAM TINIT3 value for frequency copy 0 in cycles.

4.2.10 DDRSS_CTL_9 Register (Offset = 24h) [reset = X]

DDRSS_CTL_9 is shown in [Figure 4-59](#) and described in [Table 4-122](#).

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Table 4-121. DDRSS_CTL_9 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0024h

Figure 4-59. DDRSS_CTL_9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT4_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-122. DDRSS_CTL_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT4_F0	R/W	0h	DRAM TINIT4 value for frequency copy 0 in cycles.

4.2.11 DDRSS_CTL_10 Register (Offset = 28h) [reset = X]

DDRSS_CTL_10 is shown in [Figure 4-60](#) and described in [Table 4-124](#).

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Table 4-123. DDRSS_CTL_10 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0028h

Figure 4-60. DDRSS_CTL_10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT5_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-124. DDRSS_CTL_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT5_F0	R/W	0h	DRAM TINIT5 value for frequency copy 0 in cycles.

4.2.12 DDRSS_CTL_11 Register (Offset = 2Ch) [reset = X]

DDRSS_CTL_11 is shown in [Figure 4-61](#) and described in [Table 4-126](#).

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Table 4-125. DDRSS_CTL_11 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 002Ch

Figure 4-61. DDRSS_CTL_11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-126. DDRSS_CTL_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT_F1	R/W	0h	DRAM TINIT value for frequency copy 1 in cycles.

4.2.13 DDRSS_CTL_12 Register (Offset = 30h) [reset = X]

DDRSS_CTL_12 is shown in [Figure 4-62](#) and described in [Table 4-128](#).

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Table 4-127. DDRSS_CTL_12 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0030h

Figure 4-62. DDRSS_CTL_12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT3_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-128. DDRSS_CTL_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT3_F1	R/W	0h	DRAM TINIT3 value for frequency copy 1 in cycles.

4.2.14 DDRSS_CTL_13 Register (Offset = 34h) [reset = X]

DDRSS_CTL_13 is shown in [Figure 4-63](#) and described in [Table 4-130](#).

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Table 4-129. DDRSS_CTL_13 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0034h

Figure 4-63. DDRSS_CTL_13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT4_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-130. DDRSS_CTL_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT4_F1	R/W	0h	DRAM TINIT4 value for frequency copy 1 in cycles.

4.2.15 DDRSS_CTL_14 Register (Offset = 38h) [reset = X]

DDRSS_CTL_14 is shown in [Figure 4-64](#) and described in [Table 4-132](#).

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Table 4-131. DDRSS_CTL_14 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0038h

Figure 4-64. DDRSS_CTL_14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT5_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-132. DDRSS_CTL_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT5_F1	R/W	0h	DRAM TINIT5 value for frequency copy 1 in cycles.

4.2.16 DDRSS_CTL_15 Register (Offset = 3Ch) [reset = X]

DDRSS_CTL_15 is shown in [Figure 4-65](#) and described in [Table 4-134](#).

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Table 4-133. DDRSS_CTL_15 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 003Ch

Figure 4-65. DDRSS_CTL_15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-134. DDRSS_CTL_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT_F2	R/W	0h	DRAM TINIT value for frequency copy 2 in cycles.

4.2.17 DDRSS_CTL_16 Register (Offset = 40h) [reset = X]

DDRSS_CTL_16 is shown in [Figure 4-66](#) and described in [Table 4-136](#).

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Table 4-135. DDRSS_CTL_16 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0040h

Figure 4-66. DDRSS_CTL_16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT3_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-136. DDRSS_CTL_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT3_F2	R/W	0h	DRAM TINIT3 value for frequency copy 2 in cycles.

4.2.18 DDRSS_CTL_17 Register (Offset = 44h) [reset = X]

DDRSS_CTL_17 is shown in [Figure 4-67](#) and described in [Table 4-138](#).

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Table 4-137. DDRSS_CTL_17 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0044h

Figure 4-67. DDRSS_CTL_17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TINIT4_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-138. DDRSS_CTL_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	TINIT4_F2	R/W	0h	DRAM TINIT4 value for frequency copy 2 in cycles.

4.2.19 DDRSS_CTL_18 Register (Offset = 48h) [reset = X]

DDRSS_CTL_18 is shown in [Figure 4-68](#) and described in [Table 4-140](#).

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Table 4-139. DDRSS_CTL_18 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0048h

Figure 4-68. DDRSS_CTL_18 Register

31	30	29	28	27	26	25	24
RESERVED							NO_AUTO_MR R_INIT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
TINIT5_F2							
R/W-0h							
15	14	13	12	11	10	9	8
TINIT5_F2							
R/W-0h							
7	6	5	4	3	2	1	0
TINIT5_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-140. DDRSS_CTL_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	NO_AUTO_MRR_INIT	R/W	0h	Disable MRR commands during initialization. Set to 1 to disable.
23-0	TINIT5_F2	R/W	0h	DRAM TINIT5 value for frequency copy 2 in cycles.

4.2.20 DDRSS_CTL_19 Register (Offset = 4Ch) [reset = X]

DDRSS_CTL_19 is shown in [Figure 4-69](#) and described in [Table 4-142](#).

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Table 4-141. DDRSS_CTL_19 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 004Ch

Figure 4-69. DDRSS_CTL_19 Register

31	30	29	28	27	26	25	24
RESERVED							ODT_VALUE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							NO_MRW_INIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							DFI_INV_DATA_CS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							MRR_ERROR_STATUS
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-142. DDRSS_CTL_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ODT_VALUE	R/W	0h	When using LPDDR4, this value will be driven out on the dfi_odt signal.
23-17	RESERVED	R/W	X	
16	NO_MRW_INIT	R/W	0h	Disable MRW commands during initialization. Set to 1 to disable.
15-9	RESERVED	R/W	X	
8	DFI_INV_DATA_CS	R/W	0h	Forces the inversion of the dfi_rddata_cs_n_X and dfi_wrdata_cs_n_X signals. Set to 1 to force inversion.
7-1	RESERVED	R/W	X	
0	MRR_ERROR_STATUS	R	0h	Indicates that an MRR was issued while in self-refresh. Value of 1 indicates a violation. READ-ONLY

4.2.21 DDRSS_CTL_20 Register (Offset = 50h) [reset = X]

DDRSS_CTL_20 is shown in [Figure 4-70](#) and described in [Table 4-144](#).

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Table 4-143. DDRSS_CTL_20 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0050h

Figure 4-70. DDRSS_CTL_20 Register

31	30	29	28	27	26	25	24
RESERVED						DFIBUS_FREQ_INIT	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED							PHY_INDEP_IN IT_MODE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED		TSREF2PHYMSTR					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_INDEP_T RAIN_MODE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-144. DDRSS_CTL_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	DFIBUS_FREQ_INIT	R/W	0h	Defines the initial DFI bus frequency.
23-17	RESERVED	R/W	X	
16	PHY_INDEP_INIT_MODE	R/W	0h	Enable PHY independent initialization mode commands during initialization. Set to 1 to enable.
15-14	RESERVED	R/W	X	
13-8	TSREF2PHYMSTR	R/W	0h	Specifies the minimum time after a self-refresh exit command on the DFI bus that the Controller will wait for the PHY to assert the dfi_phymstr_req signal, before completing other commands. Used when the low power control logic is expected to pass control to the PHY for training when exiting SREF.
7-1	RESERVED	R/W	X	
0	PHY_INDEP_TRAIN_MODE	R/W	0h	Enable PHY independent training mode commands during initialization. Set to 1 to enable.

4.2.22 DDRSS_CTL_21 Register (Offset = 54h) [reset = X]

DDRSS_CTL_21 is shown in [Figure 4-71](#) and described in [Table 4-146](#).

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Table 4-145. DDRSS_CTL_21 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0054h

Figure 4-71. DDRSS_CTL_21 Register

31	30	29	28	27	26	25	24
RESERVED				DFIBUS_FREQ_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				DFIBUS_FREQ_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				DFIBUS_FREQ_F0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED						DFIBUS_BOOT_FREQ	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-146. DDRSS_CTL_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	DFIBUS_FREQ_F2	R/W	0h	Defines the DFI bus frequency for frequency copy 2.
23-21	RESERVED	R/W	X	
20-16	DFIBUS_FREQ_F1	R/W	0h	Defines the DFI bus frequency for frequency copy 1.
15-13	RESERVED	R/W	X	
12-8	DFIBUS_FREQ_F0	R/W	0h	Defines the DFI bus frequency for frequency copy 0.
7-2	RESERVED	R/W	X	
1-0	DFIBUS_BOOT_FREQ	R/W	0h	Defines the DFI bus boot frequency.

4.2.23 DDRSS_CTL_22 Register (Offset = 58h) [reset = X]

DDRSS_CTL_22 is shown in [Figure 4-72](#) and described in [Table 4-148](#).

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Table 4-147. DDRSS_CTL_22 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0058h

Figure 4-72. DDRSS_CTL_22 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						FREQ_CHANGE_TYPE_F2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						FREQ_CHANGE_TYPE_F1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						FREQ_CHANGE_TYPE_F0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-148. DDRSS_CTL_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	FREQ_CHANGE_TYPE_F2	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation.
15-10	RESERVED	R/W	X	
9-8	FREQ_CHANGE_TYPE_F1	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation.
7-2	RESERVED	R/W	X	
1-0	FREQ_CHANGE_TYPE_F0	R/W	0h	Defines the encoded frequency driven out on the cntrl_freq_change_req_type signal during a frequency change operation.

4.2.24 DDRSS_CTL_23 Register (Offset = 5Ch) [reset = 0h]

DDRSS_CTL_23 is shown in [Figure 4-73](#) and described in [Table 4-150](#).

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Table 4-149. DDRSS_CTL_23 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 005Ch

Figure 4-73. DDRSS_CTL_23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRST_PWRON																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-150. DDRSS_CTL_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TRST_PWRON	R/W	0h	Duration of memory reset during power-on initialization.

4.2.25 DDRSS_CTL_24 Register (Offset = 60h) [reset = 0h]

DDRSS_CTL_24 is shown in [Figure 4-74](#) and described in [Table 4-152](#).

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Table 4-151. DDRSS_CTL_24 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0060h

Figure 4-74. DDRSS_CTL_24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKE_INACTIVE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-152. DDRSS_CTL_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	CKE_INACTIVE	R/W	0h	Number of cycles after reset before CKE will be active.

4.2.26 DDRSS_CTL_26 Register (Offset = 68h) [reset = X]

DDRSS_CTL_26 is shown in [Figure 4-75](#) and described in [Table 4-154](#).

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Table 4-153. DDRSS_CTL_26 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0068h

Figure 4-75. DDRSS_CTL_26 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						DQS_OSC_ENABLE	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-154. DDRSS_CTL_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	DQS_OSC_ENABLE	R/W	0h	Enable DQS oscillator measurement function in DRAM. Set to 1 to enable.
15-8	RESERVED	R/W	0h	Reserved
7-0	RESERVED	R/W	0h	Reserved

4.2.27 DDRSS_CTL_27 Register (Offset = 6Ch) [reset = X]

DDRSS_CTL_27 is shown in [Figure 4-76](#) and described in [Table 4-156](#).

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Table 4-155. DDRSS_CTL_27 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 006Ch

Figure 4-76. DDRSS_CTL_27 Register

31	30	29	28	27	26	25	24
TOSCO_F0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				FUNC_VALID_CYCLES			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		DQS_OSC_PERIOD					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
DQS_OSC_PERIOD							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-156. DDRSS_CTL_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TOSCO_F0	R/W	0h	Number of cycles for tOSCO timing parameter for frequency copy 0. tOSCO is the time for the DQS Oscillator measurement to be available in the mode registers.
23-20	RESERVED	R/W	X	
19-16	FUNC_VALID_CYCLES	R/W	0h	Number of cycles to hold dfi_function_valid asserted.
15	RESERVED	R/W	X	
14-0	DQS_OSC_PERIOD	R/W	0h	Number of cycles to run the oscillator measurement. Must reflect cycles programmed into mode register.

4.2.28 DDRSS_CTL_28 Register (Offset = 70h) [reset = 0h]

DDRSS_CTL_28 is shown in [Figure 4-77](#) and described in [Table 4-158](#).

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Table 4-157. DDRSS_CTL_28 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0070h

Figure 4-77. DDRSS_CTL_28 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DQS_OSC_HIGH_THRESHOLD								DQS_OSC_NORM_THRESHOLD							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOSCO_F2								TOSCO_F1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-158. DDRSS_CTL_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	DQS_OSC_HIGH_THRES HOLD	R/W	0h	Number of long counts until the high priority request is asserted for DQS Oscillator.
23-16	DQS_OSC_NORM_THRE SHOLD	R/W	0h	Number of long counts until the normal priority request is asserted for DQS Oscillator.
15-8	TOSCO_F2	R/W	0h	Number of cycles for tOSCO timing parameter for frequency copy 2. tOSCO is the time for the DQS Oscillator measurement to be available in the mode registers.
7-0	TOSCO_F1	R/W	0h	Number of cycles for tOSCO timing parameter for frequency copy 1. tOSCO is the time for the DQS Oscillator measurement to be available in the mode registers.

4.2.29 DDRSS_CTL_29 Register (Offset = 74h) [reset = 0h]

DDRSS_CTL_29 is shown in [Figure 4-78](#) and described in [Table 4-160](#).

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Table 4-159. DDRSS_CTL_29 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0074h

Figure 4-78. DDRSS_CTL_29 Register

31	30	29	28	27	26	25	24
OSC_VARIANCE_LIMIT							
R/W-0h							
23	22	21	20	19	18	17	16
OSC_VARIANCE_LIMIT							
R/W-0h							
15	14	13	12	11	10	9	8
DQS_OSC_PROMOTE_THRESHOLD							
R/W-0h							
7	6	5	4	3	2	1	0
DQS_OSC_TIMEOUT							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-160. DDRSS_CTL_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OSC_VARIANCE_LIMIT	R/W	0h	Allowed difference between base value and DQS Oscillator measurement.
15-8	DQS_OSC_PROMOTE_THRESHOLD	R/W	0h	Number of long counts until a software request for the DQS Oscillator is promoted to high priority.
7-0	DQS_OSC_TIMEOUT	R/W	0h	Number of long counts until the timeout is asserted for DQS Oscillator.

4.2.30 DDRSS_CTL_30 Register (Offset = 78h) [reset = X]

DDRSS_CTL_30 is shown in [Figure 4-79](#) and described in [Table 4-162](#).

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Table 4-161. DDRSS_CTL_30 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0078h

Figure 4-79. DDRSS_CTL_30 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
OSC_BASE_VALUE_0_CS0							
R-0h							
15	14	13	12	11	10	9	8
OSC_BASE_VALUE_0_CS0							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DQS_OSC_REQUEST
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-162. DDRSS_CTL_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-8	OSC_BASE_VALUE_0_CS0	R	0h	Base value for device 0 on chip 0. READ-ONLY
7-1	RESERVED	R/W	X	
0	DQS_OSC_REQUEST	W	0h	Software request for DQS Oscillator measurement function in DRAM. WRITE-ONLY

4.2.31 DDRSS_CTL_31 Register (Offset = 7Ch) [reset = 0h]

DDRSS_CTL_31 is shown in [Figure 4-80](#) and described in [Table 4-164](#).

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Table 4-163. DDRSS_CTL_31 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 007Ch

Figure 4-80. DDRSS_CTL_31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSC_BASE_VALUE_2_CS0															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSC_BASE_VALUE_1_CS0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-164. DDRSS_CTL_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OSC_BASE_VALUE_2_CS0	R	0h	Base value for device 2 on chip 0. READ-ONLY
15-0	OSC_BASE_VALUE_1_CS0	R	0h	Base value for device 1 on chip 0. READ-ONLY

4.2.32 DDRSS_CTL_32 Register (Offset = 80h) [reset = 0h]

DDRSS_CTL_32 is shown in [Figure 4-81](#) and described in [Table 4-166](#).

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Table 4-165. DDRSS_CTL_32 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0080h

Figure 4-81. DDRSS_CTL_32 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSC_BASE_VALUE_0_CS1															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSC_BASE_VALUE_3_CS0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-166. DDRSS_CTL_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OSC_BASE_VALUE_0_CS1	R	0h	Base value for device 0 on chip 1. READ-ONLY
15-0	OSC_BASE_VALUE_3_CS0	R	0h	Base value for device 3 on chip 0. READ-ONLY

4.2.33 DDRSS_CTL_33 Register (Offset = 84h) [reset = 0h]

DDRSS_CTL_33 is shown in [Figure 4-82](#) and described in [Table 4-168](#).

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Table 4-167. DDRSS_CTL_33 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0084h

Figure 4-82. DDRSS_CTL_33 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OSC_BASE_VALUE_2_CS1															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSC_BASE_VALUE_1_CS1															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-168. DDRSS_CTL_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	OSC_BASE_VALUE_2_CS1	R	0h	Base value for device 2 on chip 1. READ-ONLY
15-0	OSC_BASE_VALUE_1_CS1	R	0h	Base value for device 1 on chip 1. READ-ONLY

4.2.34 DDRSS_CTL_34 Register (Offset = 88h) [reset = X]

DDRSS_CTL_34 is shown in [Figure 4-83](#) and described in [Table 4-170](#).

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Table 4-169. DDRSS_CTL_34 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0088h

Figure 4-83. DDRSS_CTL_34 Register

31	30	29	28	27	26	25	24
RESERVED	WRLAT_F0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	CASLAT_LIN_F0						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
OSC_BASE_VALUE_3_CS1							
R-0h							
7	6	5	4	3	2	1	0
OSC_BASE_VALUE_3_CS1							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-170. DDRSS_CTL_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	WRLAT_F0	R/W	0h	DRAM WRLAT value for frequency copy 0 in cycles.
23	RESERVED	R/W	X	
22-16	CASLAT_LIN_F0	R/W	0h	Sets latency from read command send to data receive from/to controller for frequency copy 0. Bit (0) is half-cycle increment and the upper bits define memory CAS latency for the controller.
15-0	OSC_BASE_VALUE_3_CS1	R	0h	Base value for device 3 on chip 1. READ-ONLY

4.2.35 DDRSS_CTL_35 Register (Offset = 8Ch) [reset = X]

DDRSS_CTL_35 is shown in [Figure 4-84](#) and described in [Table 4-172](#).

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Table 4-171. DDRSS_CTL_35 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 008Ch

Figure 4-84. DDRSS_CTL_35 Register

31	30	29	28	27	26	25	24
RESERVED	WRLAT_F2						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	CASLAT_LIN_F2						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	WRLAT_F1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	CASLAT_LIN_F1						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-172. DDRSS_CTL_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	WRLAT_F2	R/W	0h	DRAM WRLAT value for frequency copy 2 in cycles.
23	RESERVED	R/W	X	
22-16	CASLAT_LIN_F2	R/W	0h	Sets latency from read command send to data receive from/to controller for frequency copy 2. Bit (0) is half-cycle increment and the upper bits define memory CAS latency for the controller.
15	RESERVED	R/W	X	
14-8	WRLAT_F1	R/W	0h	DRAM WRLAT value for frequency copy 1 in cycles.
7	RESERVED	R/W	X	
6-0	CASLAT_LIN_F1	R/W	0h	Sets latency from read command send to data receive from/to controller for frequency copy 1. Bit (0) is half-cycle increment and the upper bits define memory CAS latency for the controller.

4.2.36 DDRSS_CTL_36 Register (Offset = 90h) [reset = X]

DDRSS_CTL_36 is shown in [Figure 4-85](#) and described in [Table 4-174](#).

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Table 4-173. DDRSS_CTL_36 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0090h

Figure 4-85. DDRSS_CTL_36 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
TRRD_F0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				TCCD			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED					TBST_INT_INTERVAL		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-174. DDRSS_CTL_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	TRRD_F0	R/W	0h	DRAM TRRD value for frequency copy 0 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCCD	R/W	0h	DRAM CAS-to-CAS value in cycles.
7-3	RESERVED	R/W	X	
2-0	TBST_INT_INTERVAL	R/W	0h	DRAM burst interrupt interval value in cycles.

4.2.37 DDRSS_CTL_37 Register (Offset = 94h) [reset = X]

DDRSS_CTL_37 is shown in [Figure 4-86](#) and described in [Table 4-176](#).

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Table 4-175. DDRSS_CTL_37 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0094h

Figure 4-86. DDRSS_CTL_37 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		TWTR_F0						TRAS_MIN_F0							
R/W-X		R/W-0h						R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRC_F0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-176. DDRSS_CTL_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TWTR_F0	R/W	0h	DRAM TWTR value for frequency copy 0 in cycles.
23-16	TRAS_MIN_F0	R/W	0h	DRAM TRAS_MIN value for frequency copy 0 in cycles.
15-9	RESERVED	R/W	X	
8-0	TRC_F0	R/W	0h	DRAM TRC value for frequency copy 0 in cycles.

4.2.38 DDRSS_CTL_38 Register (Offset = 98h) [reset = X]

DDRSS_CTL_38 is shown in [Figure 4-87](#) and described in [Table 4-178](#).

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Table 4-177. DDRSS_CTL_38 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0098h

Figure 4-87. DDRSS_CTL_38 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRRD_F1								RESERVED							TFAW_F0
R/W-0h								R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFAW_F0								TRP_F0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-178. DDRSS_CTL_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TRRD_F1	R/W	0h	DRAM TRRD value for frequency copy 1 in cycles.
23-17	RESERVED	R/W	X	
16-8	TFAW_F0	R/W	0h	DRAM TFAW value for frequency copy 0 in cycles.
7-0	TRP_F0	R/W	0h	DRAM TRP value for frequency copy 0 in cycles.

4.2.39 DDRSS_CTL_39 Register (Offset = 9Ch) [reset = X]

DDRSS_CTL_39 is shown in [Figure 4-88](#) and described in [Table 4-180](#).

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Table 4-179. DDRSS_CTL_39 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 009Ch

Figure 4-88. DDRSS_CTL_39 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		TWTR_F1						TRAS_MIN_F1							
R/W-X		R/W-0h						R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRC_F1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-180. DDRSS_CTL_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TWTR_F1	R/W	0h	DRAM TWTR value for frequency copy 1 in cycles.
23-16	TRAS_MIN_F1	R/W	0h	DRAM TRAS_MIN value for frequency copy 1 in cycles.
15-9	RESERVED	R/W	X	
8-0	TRC_F1	R/W	0h	DRAM TRC value for frequency copy 1 in cycles.

4.2.40 DDRSS_CTL_40 Register (Offset = A0h) [reset = X]

DDRSS_CTL_40 is shown in [Figure 4-89](#) and described in [Table 4-182](#).

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Table 4-181. DDRSS_CTL_40 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00A0h

Figure 4-89. DDRSS_CTL_40 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRRD_F2								RESERVED							TFAW_F1
R/W-0h								R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFAW_F1								TRP_F1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-182. DDRSS_CTL_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TRRD_F2	R/W	0h	DRAM TRRD value for frequency copy 2 in cycles.
23-17	RESERVED	R/W	X	
16-8	TFAW_F1	R/W	0h	DRAM TFAW value for frequency copy 1 in cycles.
7-0	TRP_F1	R/W	0h	DRAM TRP value for frequency copy 1 in cycles.

4.2.41 DDRSS_CTL_41 Register (Offset = A4h) [reset = X]

DDRSS_CTL_41 is shown in [Figure 4-90](#) and described in [Table 4-184](#).

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Table 4-183. DDRSS_CTL_41 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00A4h

Figure 4-90. DDRSS_CTL_41 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		TWTR_F2						TRAS_MIN_F2							
R/W-X		R/W-0h						R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TRC_F2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-184. DDRSS_CTL_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TWTR_F2	R/W	0h	DRAM TWTR value for frequency copy 2 in cycles.
23-16	TRAS_MIN_F2	R/W	0h	DRAM TRAS_MIN value for frequency copy 2 in cycles.
15-9	RESERVED	R/W	X	
8-0	TRC_F2	R/W	0h	DRAM TRC value for frequency copy 2 in cycles.

4.2.42 DDRSS_CTL_42 Register (Offset = A8h) [reset = X]

DDRSS_CTL_42 is shown in [Figure 4-91](#) and described in [Table 4-186](#).

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Table 4-185. DDRSS_CTL_42 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00A8h

Figure 4-91. DDRSS_CTL_42 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		TCCDMW						RESERVED						TFAW_F2	
R/W-X		R/W-20h						R/W-X						R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TFAW_F2								TRP_F2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-186. DDRSS_CTL_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TCCDMW	R/W	20h	DRAM CAS-to-CAS masked write value in cycles.
23-17	RESERVED	R/W	X	
16-8	TFAW_F2	R/W	0h	DRAM TFAW value for frequency copy 2 in cycles.
7-0	TRP_F2	R/W	0h	DRAM TRP value for frequency copy 2 in cycles.

4.2.43 DDRSS_CTL_43 Register (Offset = ACh) [reset = X]

DDRSS_CTL_43 is shown in [Figure 4-92](#) and described in [Table 4-188](#).

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Table 4-187. DDRSS_CTL_43 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00ACh

Figure 4-92. DDRSS_CTL_43 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TMOD_F0								TMRD_F0								TRTP_F0							
R/W-X								R/W-0h								R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-188. DDRSS_CTL_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	TMOD_F0	R/W	0h	DRAM TMOD value for frequency copy 0 in cycles.
15-8	TMRD_F0	R/W	0h	DRAM TMRD value for frequency copy 0 in cycles.
7-0	TRTP_F0	R/W	0h	DRAM TRTP value for frequency copy 0 in cycles.

4.2.44 DDRSS_CTL_44 Register (Offset = B0h) [reset = X]

DDRSS_CTL_44 is shown in [Figure 4-93](#) and described in [Table 4-190](#).

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Table 4-189. DDRSS_CTL_44 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00B0h

Figure 4-93. DDRSS_CTL_44 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			TCKE_F0					RESERVED							TRAS_MAX_F0
R/W-X			R/W-0h					R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRAS_MAX_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-190. DDRSS_CTL_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCKE_F0	R/W	0h	Minimum CKE pulse width for frequency copy 0.
23-17	RESERVED	R/W	X	
16-0	TRAS_MAX_F0	R/W	0h	DRAM TRAS_MAX value for frequency copy 0 in cycles.

4.2.45 DDRSS_CTL_45 Register (Offset = B4h) [reset = 0h]

DDRSS_CTL_45 is shown in [Figure 4-94](#) and described in [Table 4-192](#).

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Table 4-191. DDRSS_CTL_45 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00B4h

Figure 4-94. DDRSS_CTL_45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TMOD_F1								TMRD_F1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRTP_F1								TCKESR_F0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-192. DDRSS_CTL_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TMOD_F1	R/W	0h	DRAM TMOD value for frequency copy 1 in cycles.
23-16	TMRD_F1	R/W	0h	DRAM TMRD value for frequency copy 1 in cycles.
15-8	TRTP_F1	R/W	0h	DRAM TRTP value for frequency copy 1 in cycles.
7-0	TCKESR_F0	R/W	0h	Minimum CKE low pulse width during a self-refresh for frequency copy 0.

4.2.46 DDRSS_CTL_46 Register (Offset = B8h) [reset = X]

DDRSS_CTL_46 is shown in [Figure 4-95](#) and described in [Table 4-194](#).

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Table 4-193. DDRSS_CTL_46 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00B8h

Figure 4-95. DDRSS_CTL_46 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			TCKE_F1					RESERVED							TRAS_MAX_F1
R/W-X			R/W-0h					R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRAS_MAX_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-194. DDRSS_CTL_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCKE_F1	R/W	0h	Minimum CKE pulse width for frequency copy 1.
23-17	RESERVED	R/W	X	
16-0	TRAS_MAX_F1	R/W	0h	DRAM TRAS_MAX value for frequency copy 1 in cycles.

4.2.47 DDRSS_CTL_47 Register (Offset = BCh) [reset = 0h]

DDRSS_CTL_47 is shown in [Figure 4-96](#) and described in [Table 4-196](#).

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Table 4-195. DDRSS_CTL_47 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00BCh

Figure 4-96. DDRSS_CTL_47 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TMOD_F2								TMRD_F2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRTP_F2								TCKESR_F1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-196. DDRSS_CTL_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TMOD_F2	R/W	0h	DRAM TMOD value for frequency copy 2 in cycles.
23-16	TMRD_F2	R/W	0h	DRAM TMRD value for frequency copy 2 in cycles.
15-8	TRTP_F2	R/W	0h	DRAM TRTP value for frequency copy 2 in cycles.
7-0	TCKESR_F1	R/W	0h	Minimum CKE low pulse width during a self-refresh for frequency copy 1.

4.2.48 DDRSS_CTL_48 Register (Offset = C0h) [reset = X]

DDRSS_CTL_48 is shown in [Figure 4-97](#) and described in [Table 4-198](#).

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Table 4-197. DDRSS_CTL_48 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00C0h

Figure 4-97. DDRSS_CTL_48 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			TCKE_F2					RESERVED							TRAS_MAX_F2
R/W-X			R/W-0h					R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRAS_MAX_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-198. DDRSS_CTL_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCKE_F2	R/W	0h	Minimum CKE pulse width for frequency copy 2.
23-17	RESERVED	R/W	X	
16-0	TRAS_MAX_F2	R/W	0h	DRAM TRAS_MAX value for frequency copy 2 in cycles.

4.2.49 DDRSS_CTL_49 Register (Offset = C4h) [reset = X]

DDRSS_CTL_49 is shown in [Figure 4-98](#) and described in [Table 4-200](#).

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Table 4-199. DDRSS_CTL_49 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00C4h

Figure 4-98. DDRSS_CTL_49 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TPPD				TCKESR_F2							
R/W-X				R/W-4h				R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-200. DDRSS_CTL_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	RESERVED	R/W	0h	Reserved
23-19	RESERVED	R/W	X	
18-16	RESERVED	R/W	0h	Reserved
15-11	RESERVED	R/W	X	
10-8	TPPD	R/W	4h	DRAM TPPD value in cycles.
7-0	TCKESR_F2	R/W	0h	Minimum CKE low pulse width during a self-refresh for frequency copy 2.

4.2.50 DDRSS_CTL_50 Register (Offset = C8h) [reset = X]

DDRSS_CTL_50 is shown in [Figure 4-99](#) and described in [Table 4-202](#).

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Table 4-201. DDRSS_CTL_50 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00C8h

Figure 4-99. DDRSS_CTL_50 Register

31	30	29	28	27	26	25	24
TRCD_F1							
R/W-0h							
23	22	21	20	19	18	17	16
TWR_F0							
R/W-0h							
15	14	13	12	11	10	9	8
TRCD_F0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							WRITEINTERP
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-202. DDRSS_CTL_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TRCD_F1	R/W	0h	DRAM TRCD value for frequency copy 1 in cycles.
23-16	TWR_F0	R/W	0h	DRAM TWR value for frequency copy 0 in cycles.
15-8	TRCD_F0	R/W	0h	DRAM TRCD value for frequency copy 0 in cycles.
7-1	RESERVED	R/W	X	
0	WRITEINTERP	R/W	0h	Allow controller to interrupt a write burst to the DRAMs with a read command. Set to 1 to allow interruption.

4.2.51 DDRSS_CTL_51 Register (Offset = CCh) [reset = X]

DDRSS_CTL_51 is shown in [Figure 4-100](#) and described in [Table 4-204](#).

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Table 4-203. DDRSS_CTL_51 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00CCh

Figure 4-100. DDRSS_CTL_51 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TMRR				TWR_F2				TRCD_F2				TWR_F1															
R/W-X				R/W-0h				R/W-0h				R/W-0h				R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-204. DDRSS_CTL_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TMRR	R/W	0h	DRAM TMRR value in cycles.
23-16	TWR_F2	R/W	0h	DRAM TWR value for frequency copy 2 in cycles.
15-8	TRCD_F2	R/W	0h	DRAM TRCD value for frequency copy 2 in cycles.
7-0	TWR_F1	R/W	0h	DRAM TWR value for frequency copy 1 in cycles.

4.2.52 DDRSS_CTL_52 Register (Offset = D0h) [reset = X]

DDRSS_CTL_52 is shown in [Figure 4-101](#) and described in [Table 4-206](#).

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Table 4-205. DDRSS_CTL_52 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00D0h

Figure 4-101. DDRSS_CTL_52 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		TCAMRD						RESERVED						TCAENT	
R/W-X		R/W-0h						R/W-X						R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TCAENT								RESERVED				TCKACKEL			
R/W-0h								R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-206. DDRSS_CTL_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	TCAMRD	R/W	0h	DRAM TCAMRD value in cycles.
23-18	RESERVED	R/W	X	
17-8	TCAENT	R/W	0h	DRAM TCAENT value in cycles.
7-5	RESERVED	R/W	X	
4-0	TCKACKEL	R/W	0h	DRAM TCKACKEL value in cycles.

4.2.53 DDRSS_CTL_53 Register (Offset = D4h) [reset = X]

DDRSS_CTL_53 is shown in [Figure 4-102](#) and described in [Table 4-208](#).

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Table 4-207. DDRSS_CTL_53 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00D4h

Figure 4-102. DDRSS_CTL_53 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TMRZ_F1				RESERVED				TMRZ_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCACHEH				RESERVED				TCAEXT			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-208. DDRSS_CTL_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TMRZ_F1	R/W	0h	DRAM TMRZ value for frequency copy 1 in cycles.
23-21	RESERVED	R/W	X	
20-16	TMRZ_F0	R/W	0h	DRAM TMRZ value for frequency copy 0 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCACHEH	R/W	0h	DRAM TCACHEH value in cycles.
7-5	RESERVED	R/W	X	
4-0	TCAEXT	R/W	0h	DRAM TCAEXT value in cycles.

4.2.54 DDRSS_CTL_54 Register (Offset = D8h) [reset = X]

DDRSS_CTL_54 is shown in [Figure 4-103](#) and described in [Table 4-210](#).

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Table 4-209. DDRSS_CTL_54 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00D8h

Figure 4-103. DDRSS_CTL_54 Register

31	30	29	28	27	26	25	24
RESERVED							TRAS_LOCKOUT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							CONCURRENT AP
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							AP
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED			TMRZ_F2				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-210. DDRSS_CTL_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	TRAS_LOCKOUT	R/W	0h	IF the DRAM supports it, this allows the controller to execute auto pre-charge commands before the TRAS_MIN parameter expires. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	CONCURRENTAP	R/W	0h	IF the DRAM supports it, this allows the controller to issue commands to other banks while a bank is in auto pre-charge. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	AP	R/W	0h	Enable auto pre-charge mode of controller. Set to 1 to enable.
7-5	RESERVED	R/W	X	
4-0	TMRZ_F2	R/W	0h	DRAM TMRZ value for frequency copy 2 in cycles.

4.2.55 DDRSS_CTL_55 Register (Offset = DCh) [reset = X]

DDRSS_CTL_55 is shown in [Figure 4-104](#) and described in [Table 4-212](#).

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Table 4-211. DDRSS_CTL_55 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00DCh

Figure 4-104. DDRSS_CTL_55 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				BSTLEN				TDAL_F2							
R/W-X				R/W-2h				R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDAL_F1								TDAL_F0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-212. DDRSS_CTL_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	BSTLEN	R/W	2h	Encoded burst length sent to DRAMs during initialization. Program to 1 for BL2, program to 2 for BL4, program to 3 for BL8, program to 4 for BL16, or program to 5 for BL32. All other settings are reserved.
23-16	TDAL_F2	R/W	0h	DRAM TDAL value for frequency copy 2 in cycles.
15-8	TDAL_F1	R/W	0h	DRAM TDAL value for frequency copy 1 in cycles.
7-0	TDAL_F0	R/W	0h	DRAM TDAL value for frequency copy 0 in cycles.

4.2.56 DDRSS_CTL_56 Register (Offset = E0h) [reset = 0h]

DDRSS_CTL_56 is shown in [Figure 4-105](#) and described in [Table 4-214](#).

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Table 4-213. DDRSS_CTL_56 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00E0h

Figure 4-105. DDRSS_CTL_56 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRP_AB_F0_1								TRP_AB_F2_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP_AB_F1_0								TRP_AB_F0_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-214. DDRSS_CTL_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TRP_AB_F0_1	R/W	0h	DRAM TRP all bank value for frequency copy 0 in cycles for chip select 1.
23-16	TRP_AB_F2_0	R/W	0h	DRAM TRP all bank value for frequency copy 2 in cycles for chip select 0.
15-8	TRP_AB_F1_0	R/W	0h	DRAM TRP all bank value for frequency copy 1 in cycles for chip select 0.
7-0	TRP_AB_F0_0	R/W	0h	DRAM TRP all bank value for frequency copy 0 in cycles for chip select 0.

4.2.57 DDRSS_CTL_57 Register (Offset = E4h) [reset = X]

DDRSS_CTL_57 is shown in [Figure 4-106](#) and described in [Table 4-216](#).

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Table 4-215. DDRSS_CTL_57 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00E4h

Figure 4-106. DDRSS_CTL_57 Register

31	30	29	28	27	26	25	24
RESERVED						RESERVED	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED							REG_DIMM_ENABLE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
TRP_AB_F2_1							
R/W-0h							
7	6	5	4	3	2	1	0
TRP_AB_F1_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-216. DDRSS_CTL_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	REG_DIMM_ENABLE	R/W	0h	Enable registered DIMM operation of the controller. Set to 1 to enable.
15-8	TRP_AB_F2_1	R/W	0h	DRAM TRP all bank value for frequency copy 2 in cycles for chip select 1.
7-0	TRP_AB_F1_1	R/W	0h	DRAM TRP all bank value for frequency copy 1 in cycles for chip select 1.

4.2.58 DDRSS_CTL_58 Register (Offset = E8h) [reset = X]

DDRSS_CTL_58 is shown in [Figure 4-107](#) and described in [Table 4-218](#).

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Table 4-217. DDRSS_CTL_58 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00E8h

Figure 4-107. DDRSS_CTL_58 Register

31	30	29	28	27	26	25	24
RESERVED							NO_MEMORY_DM
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							OPTIMAL_RM_ODW_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-218. DDRSS_CTL_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	NO_MEMORY_DM	R/W	0h	Indicates that the external DRAM does not support DM masking. Set to 1 for no DM masking at the DRAM.
23-17	RESERVED	R/W	X	
16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	OPTIMAL_RMODW_EN	R/W	0h	Enables optimized RMODW logic in the controller. A value of 1 enables optimized RMODW operation. All RMODW operations are still supported in a non-optimal manner when the value is 0.
7	RESERVED	R/W	X	
6-0	RESERVED	R/W	0h	Reserved

4.2.59 DDRSS_CTL_59 Register (Offset = ECh) [reset = X]

DDRSS_CTL_59 is shown in [Figure 4-108](#) and described in [Table 4-220](#).

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Table 4-219. DDRSS_CTL_59 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00ECh

Figure 4-108. DDRSS_CTL_59 Register

31	30	29	28	27	26	25	24
RESERVED					RESERVED		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							TREF_ENABLE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							AREF_STATUS
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED							AREFRESH
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-220. DDRSS_CTL_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	TREF_ENABLE	R/W	0h	Issue auto-refresh commands to the DRAMs at the interval defined in the TREF parameter. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	AREF_STATUS	R	0h	Indicates a SR error associated with the AREF interrupt. Value of 1 indicates a violation. READ-ONLY
7-1	RESERVED	R/W	X	
0	AREFRESH	W	0h	Initiate auto-refresh at the end of the current burst boundary. Set to 1 to trigger. WRITE-ONLY

4.2.60 DDRSS_CTL_60 Register (Offset = F0h) [reset = X]

DDRSS_CTL_60 is shown in [Figure 4-109](#) and described in [Table 4-222](#).

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Table 4-221. DDRSS_CTL_60 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00F0h

Figure 4-109. DDRSS_CTL_60 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						TRFC_F0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
TRFC_F0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		CS_COMPARISON_FOR_REFRESH_DEPTH					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-222. DDRSS_CTL_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	TRFC_F0	R/W	0h	DRAM TRFC value for frequency copy 0 in cycles.
7-6	RESERVED	R/W	X	
5-0	CS_COMPARISON_FOR_REFRESH_DEPTH	R/W	0h	Defines the number of entries of the command queue that the refresh logic will consider for sending a refresh command. A non-zero value limits the decode to a subset of the full command pipeline.

4.2.61 DDRSS_CTL_61 Register (Offset = F4h) [reset = X]

DDRSS_CTL_61 is shown in [Figure 4-110](#) and described in [Table 4-224](#).

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Table 4-223. DDRSS_CTL_61 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00F4h

Figure 4-110. DDRSS_CTL_61 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TREF_F0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-224. DDRSS_CTL_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	TREF_F0	R/W	0h	DRAM TREF value for frequency copy 0 in cycles.

4.2.62 DDRSS_CTL_62 Register (Offset = F8h) [reset = X]

DDRSS_CTL_62 is shown in [Figure 4-111](#) and described in [Table 4-226](#).

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Table 4-225. DDRSS_CTL_62 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00F8h

Figure 4-111. DDRSS_CTL_62 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						TRFC_F1															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-226. DDRSS_CTL_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TRFC_F1	R/W	0h	DRAM TRFC value for frequency copy 1 in cycles.

4.2.63 DDRSS_CTL_63 Register (Offset = FCh) [reset = X]

DDRSS_CTL_63 is shown in [Figure 4-112](#) and described in [Table 4-228](#).

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Table 4-227. DDRSS_CTL_63 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 00FCh

Figure 4-112. DDRSS_CTL_63 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TREF_F1																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-228. DDRSS_CTL_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	TREF_F1	R/W	0h	DRAM TREF value for frequency copy 1 in cycles.

4.2.64 DDRSS_CTL_64 Register (Offset = 100h) [reset = X]

DDRSS_CTL_64 is shown in [Figure 4-113](#) and described in [Table 4-230](#).

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Table 4-229. DDRSS_CTL_64 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0100h

Figure 4-113. DDRSS_CTL_64 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						TRFC_F2															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-230. DDRSS_CTL_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TRFC_F2	R/W	0h	DRAM TRFC value for frequency copy 2 in cycles.

4.2.65 DDRSS_CTL_65 Register (Offset = 104h) [reset = X]

DDRSS_CTL_65 is shown in [Figure 4-114](#) and described in [Table 4-232](#).

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Table 4-231. DDRSS_CTL_65 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0104h

Figure 4-114. DDRSS_CTL_65 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TREF_F2																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-232. DDRSS_CTL_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	TREF_F2	R/W	0h	DRAM TREF value for frequency copy 2 in cycles.

4.2.66 DDRSS_CTL_66 Register (Offset = 108h) [reset = X]

DDRSS_CTL_66 is shown in [Figure 4-115](#) and described in [Table 4-234](#).

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Table 4-233. DDRSS_CTL_66 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0108h

Figure 4-115. DDRSS_CTL_66 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TREF_INTERVAL																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-234. DDRSS_CTL_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	TREF_INTERVAL	R/W	0h	Defines the cycles between refreshes to different chip selects.

4.2.67 DDRSS_CTL_67 Register (Offset = 10Ch) [reset = X]

DDRSS_CTL_67 is shown in [Figure 4-116](#) and described in [Table 4-236](#).

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Table 4-235. DDRSS_CTL_67 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 010Ch

Figure 4-116. DDRSS_CTL_67 Register

31	30	29	28	27	26	25	24
RESERVED						TRFC_PB_F0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
TRFC_PB_F0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PBR_NUMERICAL_ORDER	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PBR_EN	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-236. DDRSS_CTL_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TRFC_PB_F0	R/W	0h	DRAM TRFC_PB value for frequency copy 0 in cycles.
15-9	RESERVED	R/W	X	
8	PBR_NUMERICAL_ORDER	R/W	0h	Enables the PBR to run REFpb commands in numeric bank order (0,1,2,3, etc.) When disabled, the order may be modified if supported by the memory type. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	PBR_EN	R/W	0h	Enables the per-bank refresh feature. Set to 1 to enable.

4.2.68 DDRSS_CTL_68 Register (Offset = 110h) [reset = X]

DDRSS_CTL_68 is shown in [Figure 4-117](#) and described in [Table 4-238](#).

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Table 4-237. DDRSS_CTL_68 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0110h

Figure 4-117. DDRSS_CTL_68 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TRFC_PB_F1										TREFI_PB_F0															
R/W-X						R/W-0h										R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-238. DDRSS_CTL_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TRFC_PB_F1	R/W	0h	DRAM TRFC_PB value for frequency copy 1 in cycles.
15-0	TREFI_PB_F0	R/W	0h	DRAM TREFI_PB value for frequency copy 0 in cycles.

4.2.69 DDRSS_CTL_69 Register (Offset = 114h) [reset = X]

DDRSS_CTL_69 is shown in [Figure 4-118](#) and described in [Table 4-240](#).

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Table 4-239. DDRSS_CTL_69 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0114h

Figure 4-118. DDRSS_CTL_69 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TRFC_PB_F2										TREFI_PB_F1															
R/W-X						R/W-0h										R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-240. DDRSS_CTL_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TRFC_PB_F2	R/W	0h	DRAM TRFC_PB value for frequency copy 2 in cycles.
15-0	TREFI_PB_F1	R/W	0h	DRAM TREFI_PB value for frequency copy 1 in cycles.

4.2.70 DDRSS_CTL_70 Register (Offset = 118h) [reset = 0h]

DDRSS_CTL_70 is shown in [Figure 4-119](#) and described in [Table 4-242](#).

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Table 4-241. DDRSS_CTL_70 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0118h

Figure 4-119. DDRSS_CTL_70 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PBR_MAX_BANK_WAIT															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TREFI_PB_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-242. DDRSS_CTL_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PBR_MAX_BANK_WAIT	R/W	0h	Defines the maximum number of cycles that the PBR module will wait for Strategy to release the target bank until the PBR will assert the inhibit and close the target bank.
15-0	TREFI_PB_F2	R/W	0h	DRAM TREFI_PB value for frequency copy 2 in cycles.

4.2.71 DDRSS_CTL_71 Register (Offset = 11Ch) [reset = X]

DDRSS_CTL_71 is shown in Figure 4-120 and described in Table 4-244.

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Table 4-243. DDRSS_CTL_71 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 011Ch

Figure 4-120. DDRSS_CTL_71 Register

31	30	29	28	27	26	25	24
RESERVED				AREF_PBR_CONT_DIS_THRESHOLD			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				AREF_PBR_CONT_EN_THRESHOLD			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PBR_CONT_REQ_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				PBR_BANK_SELECT_DELAY			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-244. DDRSS_CTL_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	AREF_PBR_CONT_DIS_THRESHOLD	R/W	0h	Sets the auto-refresh request count threshold when the PBR continuous refresh request enable will be deasserted.
23-21	RESERVED	R/W	X	
20-16	AREF_PBR_CONT_EN_THRESHOLD	R/W	0h	Sets the auto-refresh request count threshold when the PBR continuous refresh request enable will be asserted.
15-9	RESERVED	R/W	X	
8	PBR_CONT_REQ_EN	R/W	0h	Enables the per-bank refresh continuous request feature. Set to 1 to enable.
7-4	RESERVED	R/W	X	
3-0	PBR_BANK_SELECT_DELAY	R/W	0h	Defines the PBR bank select to command delay, the time from bank selection to when the command queue bank selection logic is guaranteed to have blocked the bank.

4.2.72 DDRSS_CTL_72 Register (Offset = 120h) [reset = 0h]

DDRSS_CTL_72 is shown in [Figure 4-121](#) and described in [Table 4-246](#).

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Table 4-245. DDRSS_CTL_72 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0120h

Figure 4-121. DDRSS_CTL_72 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPDEX_F1																TPDEX_F0															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-246. DDRSS_CTL_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TPDEX_F1	R/W	0h	DRAM TPDEX value for frequency copy 1 in cycles.
15-0	TPDEX_F0	R/W	0h	DRAM TPDEX value for frequency copy 0 in cycles.

4.2.73 DDRSS_CTL_73 Register (Offset = 124h) [reset = 0h]

DDRSS_CTL_73 is shown in [Figure 4-122](#) and described in [Table 4-248](#).

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Table 4-247. DDRSS_CTL_73 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0124h

Figure 4-122. DDRSS_CTL_73 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRRI_F1								TMRRI_F0								TPDEX_F2															
R/W-0h								R/W-0h								R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-248. DDRSS_CTL_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TMRRI_F1	R/W	0h	DRAM TMRRI value for frequency copy 1 in cycles.
23-16	TMRRI_F0	R/W	0h	DRAM TMRRI value for frequency copy 0 in cycles.
15-0	TPDEX_F2	R/W	0h	DRAM TPDEX value for frequency copy 2 in cycles.

4.2.74 DDRSS_CTL_74 Register (Offset = 128h) [reset = X]

DDRSS_CTL_74 is shown in [Figure 4-123](#) and described in [Table 4-250](#).

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Table 4-249. DDRSS_CTL_74 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0128h

Figure 4-123. DDRSS_CTL_74 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TCKEHCS_F0				RESERVED				TCKELCS_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCSCKE_F0				TMRRI_F2							
R/W-X				R/W-0h				R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-250. DDRSS_CTL_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCKEHCS_F0	R/W	0h	DRAM TCKEHCS value for frequency copy 0 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCKELCS_F0	R/W	0h	DRAM TCKELCS value for frequency copy 0 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCSCKE_F0	R/W	0h	DRAM TCSCKE value for frequency copy 0 in cycles.
7-0	TMRRI_F2	R/W	0h	DRAM TMRRI value for frequency copy 2 in cycles.

4.2.75 DDRSS_CTL_75 Register (Offset = 12Ch) [reset = X]

DDRSS_CTL_75 is shown in [Figure 4-124](#) and described in [Table 4-252](#).

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Table 4-251. DDRSS_CTL_75 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 012Ch

Figure 4-124. DDRSS_CTL_75 Register

31	30	29	28	27	26	25	24
RESERVED				TCSCKE_F1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							CA_DEFAULT_VAL_F0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				TZQCKE_F0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				TMRWCKEL_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-252. DDRSS_CTL_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCSCKE_F1	R/W	0h	DRAM TCSCKE value for frequency copy 1 in cycles.
23-17	RESERVED	R/W	X	
16	CA_DEFAULT_VAL_F0	R/W	0h	Defines how unused address/command bits are driven for frequency copy 0. Set to 1 to use last value or clear to 0 to drive low.
15-12	RESERVED	R/W	X	
11-8	TZQCKE_F0	R/W	0h	DRAM TZQCKE value for frequency copy 0 in cycles.
7-5	RESERVED	R/W	X	
4-0	TMRWCKEL_F0	R/W	0h	DRAM TMRWCKEL value for frequency copy 0 in cycles.

4.2.76 DDRSS_CTL_76 Register (Offset = 130h) [reset = X]

DDRSS_CTL_76 is shown in [Figure 4-125](#) and described in [Table 4-254](#).

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Table 4-253. DDRSS_CTL_76 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0130h

Figure 4-125. DDRSS_CTL_76 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TZQCKE_F1				RESERVED				TMRWCKEL_F1			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKEHCS_F1				RESERVED				TCKELCS_F1			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-254. DDRSS_CTL_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TZQCKE_F1	R/W	0h	DRAM TZQCKE value for frequency copy 1 in cycles.
23-21	RESERVED	R/W	X	
20-16	TMRWCKEL_F1	R/W	0h	DRAM TMRWCKEL value for frequency copy 1 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKEHCS_F1	R/W	0h	DRAM TCKEHCS value for frequency copy 1 in cycles.
7-5	RESERVED	R/W	X	
4-0	TCKELCS_F1	R/W	0h	DRAM TCKELCS value for frequency copy 1 in cycles.

4.2.77 DDRSS_CTL_77 Register (Offset = 134h) [reset = X]

DDRSS_CTL_77 is shown in [Figure 4-126](#) and described in [Table 4-256](#).

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Table 4-255. DDRSS_CTL_77 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0134h

Figure 4-126. DDRSS_CTL_77 Register

31	30	29	28	27	26	25	24
RESERVED				TCKEHCS_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				TCKELCS_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				TCSCKE_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							CA_DEFAULT_VAL_F1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-256. DDRSS_CTL_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCKEHCS_F2	R/W	0h	DRAM TCKEHCS value for frequency copy 2 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCKELCS_F2	R/W	0h	DRAM TCKELCS value for frequency copy 2 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCSCKE_F2	R/W	0h	DRAM TCSCKE value for frequency copy 2 in cycles.
7-1	RESERVED	R/W	X	
0	CA_DEFAULT_VAL_F1	R/W	0h	Defines how unused address/command bits are driven for frequency copy 1. Set to 1 to use last value or clear to 0 to drive low.

4.2.78 DDRSS_CTL_78 Register (Offset = 138h) [reset = X]

DDRSS_CTL_78 is shown in [Figure 4-127](#) and described in [Table 4-258](#).

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Table 4-257. DDRSS_CTL_78 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0138h

Figure 4-127. DDRSS_CTL_78 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							CA_DEFAULT_VAL_F2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				TZQCKE_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED			TMRWCKEL_F2				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-258. DDRSS_CTL_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	CA_DEFAULT_VAL_F2	R/W	0h	Defines how unused address/command bits are driven for frequency copy 2. Set to 1 to use last value or clear to 0 to drive low.
15-12	RESERVED	R/W	X	
11-8	TZQCKE_F2	R/W	0h	DRAM TZQCKE value for frequency copy 2 in cycles.
7-5	RESERVED	R/W	X	
4-0	TMRWCKEL_F2	R/W	0h	DRAM TMRWCKEL value for frequency copy 2 in cycles.

4.2.79 DDRSS_CTL_79 Register (Offset = 13Ch) [reset = 0h]

DDRSS_CTL_79 is shown in [Figure 4-128](#) and described in [Table 4-260](#).

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Table 4-259. DDRSS_CTL_79 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 013Ch

Figure 4-128. DDRSS_CTL_79 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXSNR_F0																TXSR_F0															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-260. DDRSS_CTL_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TXSNR_F0	R/W	0h	DRAM TXSNR value for frequency copy 0 in cycles.
15-0	TXSR_F0	R/W	0h	DRAM TXSR value for frequency copy 0 in cycles.

4.2.80 DDRSS_CTL_80 Register (Offset = 140h) [reset = 0h]

DDRSS_CTL_80 is shown in [Figure 4-129](#) and described in [Table 4-262](#).

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Table 4-261. DDRSS_CTL_80 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0140h

Figure 4-129. DDRSS_CTL_80 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXSNR_F1																TXSR_F1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-262. DDRSS_CTL_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TXSNR_F1	R/W	0h	DRAM TXSNR value for frequency copy 1 in cycles.
15-0	TXSR_F1	R/W	0h	DRAM TXSR value for frequency copy 1 in cycles.

4.2.81 DDRSS_CTL_81 Register (Offset = 144h) [reset = 0h]

DDRSS_CTL_81 is shown in [Figure 4-130](#) and described in [Table 4-264](#).

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Table 4-263. DDRSS_CTL_81 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0144h

Figure 4-130. DDRSS_CTL_81 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXSNR_F2																TXSR_F2															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-264. DDRSS_CTL_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TXSNR_F2	R/W	0h	DRAM TXSNR value for frequency copy 2 in cycles.
15-0	TXSR_F2	R/W	0h	DRAM TXSR value for frequency copy 2 in cycles.

4.2.82 DDRSS_CTL_82 Register (Offset = 148h) [reset = X]

DDRSS_CTL_82 is shown in [Figure 4-131](#) and described in [Table 4-266](#).

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Table 4-265. DDRSS_CTL_82 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0148h

Figure 4-131. DDRSS_CTL_82 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSR_F0								RESERVED				TCKCKEL_F0			
R/W-0h								R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKEHCMD_F0				RESERVED				TCKELCMD_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-266. DDRSS_CTL_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TSR_F0	R/W	0h	DRAM TSR value for frequency copy 0 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCKCKEL_F0	R/W	0h	DRAM TCKCKEL value for frequency copy 0 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKEHCMD_F0	R/W	0h	DRAM TCKEHCMD value for frequency copy 0 in cycles.
7-5	RESERVED	R/W	X	
4-0	TCKELCMD_F0	R/W	0h	DRAM TCKELCMD value for frequency copy 0 in cycles.

4.2.83 DDRSS_CTL_83 Register (Offset = 14Ch) [reset = X]

DDRSS_CTL_83 is shown in [Figure 4-132](#) and described in [Table 4-268](#).

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Table 4-267. DDRSS_CTL_83 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 014Ch

Figure 4-132. DDRSS_CTL_83 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TCMDCKE_F0				RESERVED				TCSCKEH_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKELPD_F0				RESERVED				TESCKE_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-268. DDRSS_CTL_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCMDCKE_F0	R/W	0h	DRAM TCMDCKE value for frequency copy 0 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCSCKEH_F0	R/W	0h	DRAM TCSCKEH value for frequency copy 0 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKELPD_F0	R/W	0h	DRAM TCKELPD value for frequency copy 0 in cycles.
7-3	RESERVED	R/W	X	
2-0	TESCKE_F0	R/W	0h	DRAM TESCKE value for frequency copy 0 in cycles.

4.2.84 DDRSS_CTL_84 Register (Offset = 150h) [reset = X]

DDRSS_CTL_84 is shown in [Figure 4-133](#) and described in [Table 4-270](#).

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Table 4-269. DDRSS_CTL_84 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0150h

Figure 4-133. DDRSS_CTL_84 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSR_F1								RESERVED				TCKCKEL_F1			
R/W-0h								R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKEHCMF1				RESERVED				TCKELCMD_F1			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-270. DDRSS_CTL_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TSR_F1	R/W	0h	DRAM TSR value for frequency copy 1 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCKCKEL_F1	R/W	0h	DRAM TCKCKEL value for frequency copy 1 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKEHCMF1	R/W	0h	DRAM TCKEHCMF1 value for frequency copy 1 in cycles.
7-5	RESERVED	R/W	X	
4-0	TCKELCMD_F1	R/W	0h	DRAM TCKELCMD value for frequency copy 1 in cycles.

4.2.85 DDRSS_CTL_85 Register (Offset = 154h) [reset = X]

DDRSS_CTL_85 is shown in [Figure 4-134](#) and described in [Table 4-272](#).

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Table 4-271. DDRSS_CTL_85 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0154h

Figure 4-134. DDRSS_CTL_85 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TCMDCKE_F1				RESERVED				TCSCKEH_F1			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKELPD_F1				RESERVED				TESCKE_F1			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-272. DDRSS_CTL_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCMDCKE_F1	R/W	0h	DRAM TCMDCKE value for frequency copy 1 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCSCKEH_F1	R/W	0h	DRAM TCSCKEH value for frequency copy 1 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKELPD_F1	R/W	0h	DRAM TCKELPD value for frequency copy 1 in cycles.
7-3	RESERVED	R/W	X	
2-0	TESCKE_F1	R/W	0h	DRAM TESCKE value for frequency copy 1 in cycles.

4.2.86 DDRSS_CTL_86 Register (Offset = 158h) [reset = X]

DDRSS_CTL_86 is shown in [Figure 4-135](#) and described in [Table 4-274](#).

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Table 4-273. DDRSS_CTL_86 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0158h

Figure 4-135. DDRSS_CTL_86 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSR_F2								RESERVED				TCKCKEL_F2			
R/W-0h								R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKEHCMF2				RESERVED				TCKELCMD_F2			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-274. DDRSS_CTL_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TSR_F2	R/W	0h	DRAM TSR value for frequency copy 2 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCKCKEL_F2	R/W	0h	DRAM TCKCKEL value for frequency copy 2 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKEHCMF2	R/W	0h	DRAM TCKEHCMF2 value for frequency copy 2 in cycles.
7-5	RESERVED	R/W	X	
4-0	TCKELCMD_F2	R/W	0h	DRAM TCKELCMD value for frequency copy 2 in cycles.

4.2.87 DDRSS_CTL_87 Register (Offset = 15Ch) [reset = X]

DDRSS_CTL_87 is shown in [Figure 4-136](#) and described in [Table 4-276](#).

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Table 4-275. DDRSS_CTL_87 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 015Ch

Figure 4-136. DDRSS_CTL_87 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TCMDCKE_F2				RESERVED				TCSCKEH_F2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKELPD_F2				RESERVED				TESCKE_F2			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-276. DDRSS_CTL_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCMDCKE_F2	R/W	0h	DRAM TCMDCKE value for frequency copy 2 in cycles.
23-21	RESERVED	R/W	X	
20-16	TCSCKEH_F2	R/W	0h	DRAM TCSCKEH value for frequency copy 2 in cycles.
15-13	RESERVED	R/W	X	
12-8	TCKELPD_F2	R/W	0h	DRAM TCKELPD value for frequency copy 2 in cycles.
7-3	RESERVED	R/W	X	
2-0	TESCKE_F2	R/W	0h	DRAM TESCKE value for frequency copy 2 in cycles.

4.2.88 DDRSS_CTL_88 Register (Offset = 160h) [reset = X]

DDRSS_CTL_88 is shown in [Figure 4-137](#) and described in [Table 4-278](#).

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Table 4-277. DDRSS_CTL_88 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0160h

Figure 4-137. DDRSS_CTL_88 Register

31	30	29	28	27	26	25	24
RESERVED					CKE_DELAY		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED						ENABLE_QUICK_SREFRESH	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						RESERVED	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PWRUP_SREFRESH_EXIT	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-278. DDRSS_CTL_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	CKE_DELAY	R/W	0h	Additional cycles to delay CKE for status reporting.
23-17	RESERVED	R/W	X	
16	ENABLE_QUICK_SREFRESH	R/W	0h	Allow user to interrupt memory initialization to enter self-refresh mode. Set to 1 to allow interruption.
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	PWRUP_SREFRESH_EXIT	R/W	0h	Allow powerup via self-refresh instead of full memory initialization. Set to 1 to enable.

4.2.89 DDRSS_CTL_89 Register (Offset = 164h) [reset = X]

DDRSS_CTL_89 is shown in [Figure 4-138](#) and described in [Table 4-280](#).

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Table 4-279. DDRSS_CTL_89 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0164h

Figure 4-138. DDRSS_CTL_89 Register

31	30	29	28	27	26	25	24
RESERVED							DFS_CALVL_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							DFS_ZQ_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						DFS_STATUS	
R/W-X						R-0h	
7	6	5	4	3	2	1	0
RESERVED			RESERVED				
R/W-X			W-0h				

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-280. DDRSS_CTL_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DFS_CALVL_EN	R/W	0h	Enables CA training during a DFS exit. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	DFS_ZQ_EN	R/W	0h	Enables ZQ calibration during a DFS exit. Set to 1 to enable.
15-10	RESERVED	R/W	X	
9-8	DFS_STATUS	R	0h	Holds the error associated with the DFS interrupt. Bit (0) set indicates an illegal command and bit (1) set indicates that a shutdown occurred during DFS. READ-ONLY
7-5	RESERVED	R/W	X	
4-0	RESERVED	W	0h	Reserved

4.2.90 DDRSS_CTL_90 Register (Offset = 168h) [reset = X]

DDRSS_CTL_90 is shown in [Figure 4-139](#) and described in [Table 4-282](#).

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Table 4-281. DDRSS_CTL_90 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0168h

Figure 4-139. DDRSS_CTL_90 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							DFS_RDLVL_GATE_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							DFS_RDLVL_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							DFS_WRLVL_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-282. DDRSS_CTL_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	DFS_RDLVL_GATE_EN	R/W	0h	Enables read gate training during a DFS exit. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	DFS_RDLVL_EN	R/W	0h	Enables read data eye training during a DFS exit. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	DFS_WRLVL_EN	R/W	0h	Enables write leveling during a DFS exit. Set to 1 to enable.

4.2.91 DDRSS_CTL_91 Register (Offset = 16Ch) [reset = 0h]

DDRSS_CTL_91 is shown in [Figure 4-140](#) and described in [Table 4-284](#).

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Table 4-283. DDRSS_CTL_91 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 016Ch

Figure 4-140. DDRSS_CTL_91 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DFS_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFS_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-284. DDRSS_CTL_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DFS_PROMOTE_THRES HOLD_F1	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 1. Applies to SW and HW DFS commands.
15-0	DFS_PROMOTE_THRES HOLD_F0	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 0. Applies to SW and HW DFS commands.

4.2.92 DDRSS_CTL_92 Register (Offset = 170h) [reset = X]

DDRSS_CTL_92 is shown in [Figure 4-141](#) and described in [Table 4-286](#).

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Table 4-285. DDRSS_CTL_92 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0170h

Figure 4-141. DDRSS_CTL_92 Register

31	30	29	28	27	26	25	24
RESERVED					RESERVED		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					ZQ_STATUS_LOG		
R/W-X					R-0h		
15	14	13	12	11	10	9	8
DFS_PROMOTE_THRESHOLD_F2							
R/W-0h							
7	6	5	4	3	2	1	0
DFS_PROMOTE_THRESHOLD_F2							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-286. DDRSS_CTL_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	RESERVED	R/W	0h	Reserved
23-19	RESERVED	R/W	X	
18-16	ZQ_STATUS_LOG	R	0h	Indicates what kind of ZQ command was terminated without execution that caused the ZQ status interrupt to assert. Bit (0) correlates to a ZQ cal init, reset, short or long command. Bit (1) correlates to a ZQ cal start command. Bit (2) correlates to a ZQ cal latch command. Value of 1 indicates that that type of command was received, but terminated without execution. READ_ONLY
15-0	DFS_PROMOTE_THRES HOLD_F2	R/W	0h	DFS promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and HW DFS commands.

4.2.93 DDRSS_CTL_94 Register (Offset = 178h) [reset = 0h]

DDRSS_CTL_94 is shown in [Figure 4-142](#) and described in [Table 4-288](#).

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Table 4-287. DDRSS_CTL_94 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0178h

Figure 4-142. DDRSS_CTL_94 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_CTRLUPD_HIGH_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_CTRLUPD_NORM_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-288. DDRSS_CTL_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_CTRLUPD_HIGH_THRESHOLD_F0	R/W	0h	DFI control update number of long counts until the high priority request is asserted for frequency copy 0.
15-0	UPD_CTRLUPD_NORM_THRESHOLD_F0	R/W	0h	DFI control update number of long counts until the normal priority request is asserted for frequency copy 0.

4.2.94 DDRSS_CTL_95 Register (Offset = 17Ch) [reset = 0h]

DDRSS_CTL_95 is shown in [Figure 4-143](#) and described in [Table 4-290](#).

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Table 4-289. DDRSS_CTL_95 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 017Ch

Figure 4-143. DDRSS_CTL_95 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_CTRLUPD_TIMEOUT_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-290. DDRSS_CTL_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F0	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted for frequency copy 0.
15-0	UPD_CTRLUPD_TIMEOUT_F0	R/W	0h	DFI control update number of long counts until the timeout is asserted for frequency copy 0.

4.2.95 DDRSS_CTL_96 Register (Offset = 180h) [reset = 0h]

DDRSS_CTL_96 is shown in [Figure 4-144](#) and described in [Table 4-292](#).

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Table 4-291. DDRSS_CTL_96 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0180h

Figure 4-144. DDRSS_CTL_96 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_CTRLUPD_NORM_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-292. DDRSS_CTL_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_CTRLUPD_NORM_THRESHOLD_F1	R/W	0h	DFI control update number of long counts until the normal priority request is asserted for frequency copy 1.
15-0	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F0	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted for frequency copy 0.

4.2.96 DDRSS_CTL_97 Register (Offset = 184h) [reset = 0h]

DDRSS_CTL_97 is shown in [Figure 4-145](#) and described in [Table 4-294](#).

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Table 4-293. DDRSS_CTL_97 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0184h

Figure 4-145. DDRSS_CTL_97 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_CTRLUPD_TIMEOUT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_CTRLUPD_HIGH_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-294. DDRSS_CTL_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_CTRLUPD_TIMEOUT_F1	R/W	0h	DFI control update number of long counts until the timeout is asserted for frequency copy 1.
15-0	UPD_CTRLUPD_HIGH_THRESHOLD_F1	R/W	0h	DFI control update number of long counts until the high priority request is asserted for frequency copy 1.

4.2.97 DDRSS_CTL_98 Register (Offset = 188h) [reset = 0h]

DDRSS_CTL_98 is shown in [Figure 4-146](#) and described in [Table 4-296](#).

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Table 4-295. DDRSS_CTL_98 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0188h

Figure 4-146. DDRSS_CTL_98 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-296. DDRSS_CTL_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted for frequency copy 1.
15-0	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F1	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted for frequency copy 1.

4.2.98 DDRSS_CTL_99 Register (Offset = 18Ch) [reset = 0h]

DDRSS_CTL_99 is shown in [Figure 4-147](#) and described in [Table 4-298](#).

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Table 4-297. DDRSS_CTL_99 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 018Ch

Figure 4-147. DDRSS_CTL_99 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_CTRLUPD_HIGH_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_CTRLUPD_NORM_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-298. DDRSS_CTL_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_CTRLUPD_HIGH_THRESHOLD_F2	R/W	0h	DFI control update number of long counts until the high priority request is asserted for frequency copy 2.
15-0	UPD_CTRLUPD_NORM_THRESHOLD_F2	R/W	0h	DFI control update number of long counts until the normal priority request is asserted for frequency copy 2.

4.2.99 DDRSS_CTL_100 Register (Offset = 190h) [reset = 0h]

DDRSS_CTL_100 is shown in [Figure 4-148](#) and described in [Table 4-300](#).

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Table 4-299. DDRSS_CTL_100 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0190h

Figure 4-148. DDRSS_CTL_100 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_CTRLUPD_TIMEOUT_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-300. DDRSS_CTL_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	UPD_CTRLUPD_SW_PROMOTE_THRESHOLD_F2	R/W	0h	DFI control update SW promotion number of long counts until the high priority request is asserted for frequency copy 2.
15-0	UPD_CTRLUPD_TIMEOUT_F2	R/W	0h	DFI control update number of long counts until the timeout is asserted for frequency copy 2.

4.2.100 DDRSS_CTL_101 Register (Offset = 194h) [reset = X]

DDRSS_CTL_101 is shown in [Figure 4-149](#) and described in [Table 4-302](#).

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Table 4-301. DDRSS_CTL_101 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0194h

Figure 4-149. DDRSS_CTL_101 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-302. DDRSS_CTL_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	UPD_PHYUPD_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	DFI PHY update DFI promotion number of long counts until the high priority request is asserted for frequency copy 2.

4.2.101 DDRSS_CTL_102 Register (Offset = 198h) [reset = 0h]

DDRSS_CTL_102 is shown in [Figure 4-150](#) and described in [Table 4-304](#).

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Table 4-303. DDRSS_CTL_102 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0198h

Figure 4-150. DDRSS_CTL_102 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-304. DDRSS_CTL_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_F0	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack, for frequency copy 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.102 DDRSS_CTL_103 Register (Offset = 19Ch) [reset = 0h]

DDRSS_CTL_103 is shown in [Figure 4-151](#) and described in [Table 4-306](#).

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Table 4-305. DDRSS_CTL_103 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 019Ch

Figure 4-151. DDRSS_CTL_103 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-306. DDRSS_CTL_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE0_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0, for frequency copy 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.103 DDRSS_CTL_104 Register (Offset = 1A0h) [reset = 0h]

DDRSS_CTL_104 is shown in [Figure 4-152](#) and described in [Table 4-308](#).

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Table 4-307. DDRSS_CTL_104 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01A0h

Figure 4-152. DDRSS_CTL_104 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-308. DDRSS_CTL_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE1_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1, for frequency copy 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.104 DDRSS_CTL_105 Register (Offset = 1A4h) [reset = 0h]

DDRSS_CTL_105 is shown in [Figure 4-153](#) and described in [Table 4-310](#).

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Table 4-309. DDRSS_CTL_105 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01A4h

Figure 4-153. DDRSS_CTL_105 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-310. DDRSS_CTL_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE2_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2, for frequency copy 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.105 DDRSS_CTL_106 Register (Offset = 1A8h) [reset = 0h]

DDRSS_CTL_106 is shown in [Figure 4-154](#) and described in [Table 4-312](#).

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Table 4-311. DDRSS_CTL_106 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01A8h

Figure 4-154. DDRSS_CTL_106 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-312. DDRSS_CTL_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE3_F0	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3, for frequency copy 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.106 DDRSS_CTL_107 Register (Offset = 1ACh) [reset = X]

DDRSS_CTL_107 is shown in [Figure 4-155](#) and described in [Table 4-314](#).

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Table 4-313. DDRSS_CTL_107 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01ACh

Figure 4-155. DDRSS_CTL_107 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-314. DDRSS_CTL_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F0	R/W	0h	Defines the DFI(4.0 and 4.0v2) PHY master request promotion number of regular (not long) counts until the high priority request is asserted for frequency copy 0.

4.2.107 DDRSS_CTL_108 Register (Offset = 1B0h) [reset = X]

DDRSS_CTL_108 is shown in [Figure 4-156](#) and described in [Table 4-316](#).

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Table 4-315. DDRSS_CTL_108 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01B0h

Figure 4-156. DDRSS_CTL_108 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TDFI_PHYMSTR_RESP_F0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-316. DDRSS_CTL_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	TDFI_PHYMSTR_RESP_F0	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion, for frequency copy 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) to be set to 1 in the PHYMSTR_ERROR_STATUS parameter.

4.2.108 DDRSS_CTL_109 Register (Offset = 1B4h) [reset = 0h]

DDRSS_CTL_109 is shown in [Figure 4-157](#) and described in [Table 4-318](#).

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Table 4-317. DDRSS_CTL_109 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01B4h

Figure 4-157. DDRSS_CTL_109 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-318. DDRSS_CTL_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_F1	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack, for frequency copy 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.109 DDRSS_CTL_110 Register (Offset = 1B8h) [reset = 0h]

DDRSS_CTL_110 is shown in [Figure 4-158](#) and described in [Table 4-320](#).

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Table 4-319. DDRSS_CTL_110 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01B8h

Figure 4-158. DDRSS_CTL_110 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-320. DDRSS_CTL_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE0_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0, for frequency copy 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.110 DDRSS_CTL_111 Register (Offset = 1BCh) [reset = 0h]

DDRSS_CTL_111 is shown in [Figure 4-159](#) and described in [Table 4-322](#).

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Table 4-321. DDRSS_CTL_111 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01BCh

Figure 4-159. DDRSS_CTL_111 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-322. DDRSS_CTL_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE1_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1, for frequency copy 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.111 DDRSS_CTL_112 Register (Offset = 1C0h) [reset = 0h]

DDRSS_CTL_112 is shown in [Figure 4-160](#) and described in [Table 4-324](#).

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Table 4-323. DDRSS_CTL_112 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01C0h

Figure 4-160. DDRSS_CTL_112 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-324. DDRSS_CTL_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE2_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2, for frequency copy 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.112 DDRSS_CTL_113 Register (Offset = 1C4h) [reset = 0h]

DDRSS_CTL_113 is shown in [Figure 4-161](#) and described in [Table 4-326](#).

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Table 4-325. DDRSS_CTL_113 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01C4h

Figure 4-161. DDRSS_CTL_113 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-326. DDRSS_CTL_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE3_F1	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3, for frequency copy 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.113 DDRSS_CTL_114 Register (Offset = 1C8h) [reset = X]

DDRSS_CTL_114 is shown in [Figure 4-162](#) and described in [Table 4-328](#).

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Table 4-327. DDRSS_CTL_114 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01C8h

Figure 4-162. DDRSS_CTL_114 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-328. DDRSS_CTL_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F1	R/W	0h	Defines the DFI(4.0 and 4.0v2) PHY master request promotion number of regular (not long) counts until the high priority request is asserted for frequency copy 1.

4.2.114 DDRSS_CTL_115 Register (Offset = 1CCh) [reset = X]

DDRSS_CTL_115 is shown in [Figure 4-163](#) and described in [Table 4-330](#).

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Table 4-329. DDRSS_CTL_115 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01CCh

Figure 4-163. DDRSS_CTL_115 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TDFI_PHYMSTR_RESP_F1																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-330. DDRSS_CTL_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	TDFI_PHYMSTR_RESP_F1	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion, for frequency copy 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) to be set to 1 in the PHYMSTR_ERROR_STATUS parameter.

4.2.115 DDRSS_CTL_116 Register (Offset = 1D0h) [reset = 0h]

DDRSS_CTL_116 is shown in [Figure 4-164](#) and described in [Table 4-332](#).

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Table 4-331. DDRSS_CTL_116 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01D0h

Figure 4-164. DDRSS_CTL_116 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-332. DDRSS_CTL_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_F2	R/W	0h	Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack, for frequency copy 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.116 DDRSS_CTL_117 Register (Offset = 1D4h) [reset = 0h]

DDRSS_CTL_117 is shown in [Figure 4-165](#) and described in [Table 4-334](#).

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Table 4-333. DDRSS_CTL_117 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01D4h

Figure 4-165. DDRSS_CTL_117 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE0_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-334. DDRSS_CTL_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE0_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=0, for frequency copy 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.117 DDRSS_CTL_118 Register (Offset = 1D8h) [reset = 0h]

DDRSS_CTL_118 is shown in [Figure 4-166](#) and described in [Table 4-336](#).

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Table 4-335. DDRSS_CTL_118 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01D8h

Figure 4-166. DDRSS_CTL_118 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE1_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-336. DDRSS_CTL_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE1_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=1, for frequency copy 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.118 DDRSS_CTL_119 Register (Offset = 1DCh) [reset = 0h]

DDRSS_CTL_119 is shown in [Figure 4-167](#) and described in [Table 4-338](#).

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Table 4-337. DDRSS_CTL_119 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01DCh

Figure 4-167. DDRSS_CTL_119 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE2_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-338. DDRSS_CTL_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE2_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=2, for frequency copy 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.119 DDRSS_CTL_120 Register (Offset = 1E0h) [reset = 0h]

DDRSS_CTL_120 is shown in [Figure 4-168](#) and described in [Table 4-340](#).

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Table 4-339. DDRSS_CTL_120 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01E0h

Figure 4-168. DDRSS_CTL_120 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYMSTR_MAX_TYPE3_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-340. DDRSS_CTL_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYMSTR_MAX_T YPE3_F2	R/W	0h	Defines the DFI 4.0v2 tPHYMSTR_MAX_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req can be asserted following the assertion of dfi_phymstr_ack for dfi_phymstr_type=3, for frequency copy 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PHYMSTR_ERROR_STATUS parameter.

4.2.120 DDRSS_CTL_121 Register (Offset = 1E4h) [reset = X]

DDRSS_CTL_121 is shown in [Figure 4-169](#) and described in [Table 4-342](#).

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Table 4-341. DDRSS_CTL_121 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01E4h

Figure 4-169. DDRSS_CTL_121 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-342. DDRSS_CTL_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHYMSTR_DFI4_PROMOTE_THRESHOLD_F2	R/W	0h	Defines the DFI(4.0 and 4.0v2) PHY master request promotion number of regular (not long) counts until the high priority request is asserted for frequency copy 2.

4.2.121 DDRSS_CTL_122 Register (Offset = 1E8h) [reset = X]

DDRSS_CTL_122 is shown in [Figure 4-170](#) and described in [Table 4-344](#).

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Table 4-343. DDRSS_CTL_122 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01E8h

Figure 4-170. DDRSS_CTL_122 Register

31	30	29	28	27	26	25	24
RESERVED							PHYMSTR_NO_AREF
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				TDFI_PHYMSTR_RESP_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
TDFI_PHYMSTR_RESP_F2							
R/W-0h							
7	6	5	4	3	2	1	0
TDFI_PHYMSTR_RESP_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-344. DDRSS_CTL_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHYMSTR_NO_AREF	R/W	0h	Disables refreshes during the PHY master interface sequence. Set to 1 to disable. Refreshes during reset are only supported for DFI 4.0 and this parameter may be set or cleared for DFI 4.0. For all other DFI versions, this parameter must be set to 1.
23-20	RESERVED	R/W	X	
19-0	TDFI_PHYMSTR_RESP_F2	R/W	0h	Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion, for frequency copy 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) to be set to 1 in the PHYMSTR_ERROR_STATUS parameter.

4.2.122 DDRSS_CTL_123 Register (Offset = 1ECh) [reset = X]

DDRSS_CTL_123 is shown in [Figure 4-171](#) and described in [Table 4-346](#).

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Table 4-345. DDRSS_CTL_123 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01ECh

Figure 4-171. DDRSS_CTL_123 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHYMSTR_TRAIN_AFTER_INIT_COMPLETE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHYMSTR_DFI_VERSION_4P0V1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PHYMSTR_ERROR_STATUS	
R/W-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-346. DDRSS_CTL_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHYMSTR_TRAIN_AFTER_INIT_COMPLETE	R/W	0h	Defines how the PHY will use the PHY Master Interface for training. Clear to 0 to perform training without the PHY Master Interface, or set to 1 to use the PHY Master Interface to gain control over the DFI bus after the dfi_init_complete signal assertion for the initial training. Default is cleared to 0.
15-9	RESERVED	R/W	X	
8	PHYMSTR_DFI_VERSION_4P0V1	R/W	0h	Defines the version of the DFI 4.0 specification supported. Clear to 0 for DFI 4.0 version 2 PHY Master Interface, or set to 1 for DFI 4.0 version 1 PHY Master Interface. Default is cleared to 0 for version 2.
7-2	RESERVED	R/W	X	
1-0	PHYMSTR_ERROR_STATUS	R	0h	Identifies the source of any DFI PHY Master Interface errors. Value of 1 indicates a timing violation of the associated timing parameter. Bit (0) set indicates a TDFI_PHYMSTR_MAX or TDFI_PHYMSTR_TYPEn_MAX parameter violation and bit (1) set indicates a TDFI_PHYMSTR_RESP parameter violation. READ-ONLY

4.2.123 DDRSS_CTL_124 Register (Offset = 1F0h) [reset = 0h]

DDRSS_CTL_124 is shown in [Figure 4-172](#) and described in [Table 4-348](#).

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Table 4-347. DDRSS_CTL_124 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01F0h

Figure 4-172. DDRSS_CTL_124 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-348. DDRSS_CTL_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRR_TEMPCHK_HIGH_THRESHOLD_F0	R/W	0h	MRR temp check number of long counts until the high priority request is asserted for frequency copy 0.
15-0	MRR_TEMPCHK_NORM_THRESHOLD_F0	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted for frequency copy 0.

4.2.124 DDRSS_CTL_125 Register (Offset = 1F4h) [reset = 0h]

DDRSS_CTL_125 is shown in [Figure 4-173](#) and described in [Table 4-350](#).

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Table 4-349. DDRSS_CTL_125 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01F4h

Figure 4-173. DDRSS_CTL_125 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRR_TEMPCHK_NORM_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-350. DDRSS_CTL_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRR_TEMPCHK_NORM_THRESHOLD_F1	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted for frequency copy 1.
15-0	MRR_TEMPCHK_TIMEOUT_F0	R/W	0h	MRR temp check number of long counts until the timeout is asserted for frequency copy 0.

4.2.125 DDRSS_CTL_126 Register (Offset = 1F8h) [reset = 0h]

DDRSS_CTL_126 is shown in [Figure 4-174](#) and described in [Table 4-352](#).

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Table 4-351. DDRSS_CTL_126 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01F8h

Figure 4-174. DDRSS_CTL_126 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRR_TEMPCHK_TIMEOUT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRR_TEMPCHK_HIGH_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-352. DDRSS_CTL_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRR_TEMPCHK_TIMEOUT_F1	R/W	0h	MRR temp check number of long counts until the timeout is asserted for frequency copy 1.
15-0	MRR_TEMPCHK_HIGH_THRESHOLD_F1	R/W	0h	MRR temp check number of long counts until the high priority request is asserted for frequency copy 1.

4.2.126 DDRSS_CTL_127 Register (Offset = 1FCh) [reset = 0h]

DDRSS_CTL_127 is shown in [Figure 4-175](#) and described in [Table 4-354](#).

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Table 4-353. DDRSS_CTL_127 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 01FCh

Figure 4-175. DDRSS_CTL_127 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRR_TEMPCHK_HIGH_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRR_TEMPCHK_NORM_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-354. DDRSS_CTL_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRR_TEMPCHK_HIGH_THRESHOLD_F2	R/W	0h	MRR temp check number of long counts until the high priority request is asserted for frequency copy 2.
15-0	MRR_TEMPCHK_NORM_THRESHOLD_F2	R/W	0h	MRR temp check number of long counts until the normal priority request is asserted for frequency copy 2.

4.2.127 DDRSS_CTL_128 Register (Offset = 200h) [reset = X]

DDRSS_CTL_128 is shown in [Figure 4-176](#) and described in [Table 4-356](#).

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Table 4-355. DDRSS_CTL_128 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0200h

Figure 4-176. DDRSS_CTL_128 Register

31	30	29	28	27	26	25	24
RESERVED					PPR_COMMAND		
R/W-X					W-0h		
23	22	21	20	19	18	17	16
RESERVED						PPR_CONTROL	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
MRR_TEMPCHK_TIMEOUT_F2							
R/W-0h							
7	6	5	4	3	2	1	0
MRR_TEMPCHK_TIMEOUT_F2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-356. DDRSS_CTL_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PPR_COMMAND	W	0h	Specifies the type of PPR command. Program to 1 for pre-charge all, program to 2 for MRW, program to 3 for activate, or program to 5 for write. All other values are reserved. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PPR_CONTROL	R/W	0h	Enables the post-package repair feature. Set to 1 to enable. This parameter may only be programmed before initialization begins.
15-0	MRR_TEMPCHK_TIMEOUT_F2	R/W	0h	MRR temp check number of long counts until the timeout is asserted for frequency copy 2.

4.2.128 DDRSS_CTL_129 Register (Offset = 204h) [reset = X]

DDRSS_CTL_129 is shown in [Figure 4-177](#) and described in [Table 4-358](#).

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Table 4-357. DDRSS_CTL_129 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0204h

Figure 4-177. DDRSS_CTL_129 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PPR_ROW_ADDRESS							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPR_ROW_ADDRESS								PPR_COMMAND_MRW							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-358. DDRSS_CTL_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-8	PPR_ROW_ADDRESS	R/W	0h	Specifies the encoded row address to be repaired.
7-0	PPR_COMMAND_MRW	R/W	0h	Specifies the mode register to be used. Clear to 0 for MRW0 or program to 4 for MRW4. All other values are reserved.

4.2.129 DDRSS_CTL_130 Register (Offset = 208h) [reset = X]

DDRSS_CTL_130 is shown in [Figure 4-178](#) and described in [Table 4-360](#).

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Table 4-359. DDRSS_CTL_130 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0208h

Figure 4-178. DDRSS_CTL_130 Register

31	30	29	28	27	26	25	24
RESERVED							FM_OVRIDE_C ONTROL
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PPR_STATUS	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED							PPR_CS_ADD RESS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					PPR_BANK_ADDRESS		
R/W-X					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-360. DDRSS_CTL_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FM_OVRIDE_CONTROL	R/W	0h	Enables the FM Override feature. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PPR_STATUS	R	0h	Reports the status of the PPR operation. Bit (0) set indicates that PPR operations are now allowed and bit (1) set indicates if the last PPR command is complete. READ-ONLY
15-9	RESERVED	R/W	X	
8	PPR_CS_ADDRESS	R/W	0h	Specifies the chip select for the row to be repaired.
7-3	RESERVED	R/W	X	
2-0	PPR_BANK_ADDRESS	R/W	0h	Specifies the bank for the row to be repaired.

4.2.130 DDRSS_CTL_131 Register (Offset = 20Ch) [reset = X]

DDRSS_CTL_131 is shown in [Figure 4-179](#) and described in [Table 4-362](#).

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Table 4-361. DDRSS_CTL_131 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 020Ch

Figure 4-179. DDRSS_CTL_131 Register

31	30	29	28	27	26	25	24
CKSRE_F1							
R/W-0h							
23	22	21	20	19	18	17	16
CKSRX_F0							
R/W-0h							
15	14	13	12	11	10	9	8
CKSRE_F0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						LOWPOWER_REFRESH_ENABLE	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-362. DDRSS_CTL_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	CKSRE_F1	R/W	0h	Clock hold delay on self-refresh entry for frequency copy 1.
23-16	CKSRX_F0	R/W	0h	Clock stable delay on self-refresh exit for frequency copy 0.
15-8	CKSRE_F0	R/W	0h	Clock hold delay on self-refresh entry for frequency copy 0.
7-2	RESERVED	R/W	X	
1-0	LOWPOWER_REFRESH_ENABLE	R/W	0h	Enable refreshes while in low power mode. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to disable.

4.2.131 DDRSS_CTL_132 Register (Offset = 210h) [reset = X]

DDRSS_CTL_132 is shown in [Figure 4-180](#) and described in [Table 4-364](#).

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Table 4-363. DDRSS_CTL_132 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0210h

Figure 4-180. DDRSS_CTL_132 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE SE RV ED	LP_CMD							CKSRX_F2							CKSRE_F2							CKSRX_F1									
R/ W- X	W-0h							R/W-0h							R/W-0h							R/W-0h									

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-364. DDRSS_CTL_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	LP_CMD	W	0h	Low power software command request interface. Bit (0) controls exit, bit (1) controls entry, bits (4:2) define the low power state, bit (5) controls memory clock gating, bit (6) controls controller clock gating, and bit (7) controls lock. WRITE-ONLY
23-16	CKSRX_F2	R/W	0h	Clock stable delay on self-refresh exit for frequency copy 2.
15-8	CKSRE_F2	R/W	0h	Clock hold delay on self-refresh entry for frequency copy 2.
7-0	CKSRX_F1	R/W	0h	Clock stable delay on self-refresh exit for frequency copy 1.

4.2.132 DDRSS_CTL_133 Register (Offset = 214h) [reset = X]

DDRSS_CTL_133 is shown in [Figure 4-181](#) and described in [Table 4-366](#).

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Table 4-365. DDRSS_CTL_133 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0214h

Figure 4-181. DDRSS_CTL_133 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SR_LONG_WAKEUP_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_SHORT_WAKEUP_F0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_CTRL_IDLE_WAKEUP_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-366. DDRSS_CTL_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh long with memory and controller clock gating state, for frequency copy 0.
23-20	RESERVED	R/W	X	
19-16	LPI_SR_LONG_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh long state (with or without memory clock gating) for frequency copy 0.
15-12	RESERVED	R/W	X	
11-8	LPI_SR_SHORT_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when LPDDR4 memory is in the self-refresh short state (with or without memory clock gating) for frequency copy 0. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted.
7-4	RESERVED	R/W	X	
3-0	LPI_CTRL_IDLE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when controller is idle for frequency copy 0.

4.2.133 DDRSS_CTL_134 Register (Offset = 218h) [reset = X]

DDRSS_CTL_134 is shown in [Figure 4-182](#) and described in [Table 4-368](#).

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Table 4-367. DDRSS_CTL_134 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0218h

Figure 4-182. DDRSS_CTL_134 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SRPD_LONG_WAKEUP_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SRPD_SHORT_WAKEUP_F0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_PD_WAKEUP_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-368. DDRSS_CTL_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state, for frequency copy 0.
23-20	RESERVED	R/W	X	
19-16	LPI_SRPD_LONG_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down long state (with or without memory clock gating), for frequency copy 0.
15-12	RESERVED	R/W	X	
11-8	LPI_SRPD_SHORT_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down short state (with or without memory clock gating), for frequency copy 0.
7-4	RESERVED	R/W	X	
3-0	LPI_PD_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in any of the power-down states (with or without memory clock gating) for frequency copy 0.

4.2.134 DDRSS_CTL_135 Register (Offset = 21Ch) [reset = X]

DDRSS_CTL_135 is shown in [Figure 4-183](#) and described in [Table 4-370](#).

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Table 4-369. DDRSS_CTL_135 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 021Ch

Figure 4-183. DDRSS_CTL_135 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_LONG_WAKEUP_F1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SR_SHORT_WAKEUP_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_CTRL_IDLE_WAKEUP_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_TIMER_WAKEUP_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-370. DDRSS_CTL_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LPI_SR_LONG_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh long state (with or without memory clock gating) for frequency copy 1.
23-20	RESERVED	R/W	X	
19-16	LPI_SR_SHORT_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when LPDDR4 memory is in the self-refresh short state (with or without memory clock gating) for frequency copy 1. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted.
15-12	RESERVED	R/W	X	
11-8	LPI_CTRL_IDLE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when controller is idle for frequency copy 1.
7-4	RESERVED	R/W	X	
3-0	LPI_TIMER_WAKEUP_F0	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when the LPI timer expires for frequency copy 0.

4.2.135 DDRSS_CTL_136 Register (Offset = 220h) [reset = X]

DDRSS_CTL_136 is shown in [Figure 4-184](#) and described in [Table 4-372](#).

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Table 4-371. DDRSS_CTL_136 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0220h

Figure 4-184. DDRSS_CTL_136 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_LONG_WAKEUP_F1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_SRPD_SHORT_WAKEUP_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_PD_WAKEUP_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-372. DDRSS_CTL_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LPI_SRPD_LONG_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down long state (with or without memory clock gating), for frequency copy 1.
23-20	RESERVED	R/W	X	
19-16	LPI_SRPD_SHORT_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down short state (with or without memory clock gating), for frequency copy 1.
15-12	RESERVED	R/W	X	
11-8	LPI_PD_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in any of the power-down states (with or without memory clock gating) for frequency copy 1.
7-4	RESERVED	R/W	X	
3-0	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh long with memory and controller clock gating state, for frequency copy 1.

4.2.136 DDRSS_CTL_137 Register (Offset = 224h) [reset = X]

DDRSS_CTL_137 is shown in [Figure 4-185](#) and described in [Table 4-374](#).

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Table 4-373. DDRSS_CTL_137 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0224h

Figure 4-185. DDRSS_CTL_137 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SR_SHORT_WAKEUP_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_CTRL_IDLE_WAKEUP_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_TIMER_WAKEUP_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-374. DDRSS_CTL_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LPI_SR_SHORT_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when LPDDR4 memory is in the self-refresh short state (with or without memory clock gating) for frequency copy 2. For LPDDR4, SR_SHORT is used to send few commands so this wakeup time must be cleared to ZERO and no LPI request needs to be asserted.
23-20	RESERVED	R/W	X	
19-16	LPI_CTRL_IDLE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when controller is idle for frequency copy 2.
15-12	RESERVED	R/W	X	
11-8	LPI_TIMER_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when the LPI timer expires for frequency copy 1.
7-4	RESERVED	R/W	X	
3-0	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F1	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state, for frequency copy 1.

4.2.137 DDRSS_CTL_138 Register (Offset = 228h) [reset = X]

DDRSS_CTL_138 is shown in [Figure 4-186](#) and described in [Table 4-376](#).

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Table 4-375. DDRSS_CTL_138 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0228h

Figure 4-186. DDRSS_CTL_138 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_SRPD_SHORT_WAKEUP_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_PD_WAKEUP_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SR_LONG_MCCLK_GATE_WAKEUP_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SR_LONG_WAKEUP_F2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-376. DDRSS_CTL_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LPI_SRPD_SHORT_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down short state (with or without memory clock gating), for frequency copy 2.
23-20	RESERVED	R/W	X	
19-16	LPI_PD_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in any of the power-down states (with or without memory clock gating) for frequency copy 2.
15-12	RESERVED	R/W	X	
11-8	LPI_SR_LONG_MCCLK_GATE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh long with memory and controller clock gating state, for frequency copy 2.
7-4	RESERVED	R/W	X	
3-0	LPI_SR_LONG_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh long state (with or without memory clock gating) for frequency copy 2.

4.2.138 DDRSS_CTL_139 Register (Offset = 22Ch) [reset = X]

DDRSS_CTL_139 is shown in [Figure 4-187](#) and described in [Table 4-378](#).

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Table 4-377. DDRSS_CTL_139 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 022Ch

Figure 4-187. DDRSS_CTL_139 Register

31	30	29	28	27	26	25	24
RESERVED				LPI_WAKEUP_EN			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LPI_TIMER_WAKEUP_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				LPI_SRPD_LONG_WAKEUP_F2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-378. DDRSS_CTL_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	LPI_WAKEUP_EN	R/W	0h	Enables the various low power state wakeup parameters for LPI request uses. Bit (0) enables controller idle wakeup, bit (1) enables power-down wakeup, bit (2) enables either self-refresh short, self-refresh long with or without mem clk gating, either self-refresh power-down short, or self-refresh power-down long with or without mem clk gating, bit (3) enables self-refresh long with mem and ctr clk gating or self-refresh power-down long with mem and ctr clk gating, bit (4) enables the LPI timer expiry wakeup, and bit (5) is reserved. Set each bit to 1 to enable the respective LP_WAKEUP value for the LPI request.
23-20	RESERVED	R/W	X	
19-16	LPI_TIMER_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when the LPI timer expires for frequency copy 2.
15-12	RESERVED	R/W	X	
11-8	LPI_SRPD_LONG_MCCLK_GATE_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down long with memory and controller clock gating state, for frequency copy 2.
7-4	RESERVED	R/W	X	
3-0	LPI_SRPD_LONG_WAKEUP_F2	R/W	0h	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in the self-refresh power-down long state (with or without memory clock gating), for frequency copy 2.

4.2.139 DDRSS_CTL_140 Register (Offset = 230h) [reset = X]

DDRSS_CTL_140 is shown in [Figure 4-188](#) and described in [Table 4-380](#).

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Table 4-379. DDRSS_CTL_140 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0230h

Figure 4-188. DDRSS_CTL_140 Register

31	30	29	28	27	26	25	24
RESERVED						TDFI_LP_RESP	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						LPI_WAKEUP_TIMEOUT	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
LPI_WAKEUP_TIMEOUT							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							LPI_CTRL_REQ_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-380. DDRSS_CTL_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	TDFI_LP_RESP	R/W	0h	Defines the DFI tLP_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_lp_req assertion and a dfi_lp_ack assertion.
23-20	RESERVED	R/W	X	
19-8	LPI_WAKEUP_TIMEOUT	R/W	0h	Defines the LPI timeout time, the maximum cycles between a dfi_lp_req de-assertion and a dfi_lp_ack de-assertion. If this value is exceeded, an interrupt will occur.
7-1	RESERVED	R/W	X	
0	LPI_CTRL_REQ_EN	R/W	0h	Enables the dfi_lpi_ctrl_req signal for the LPI. This signal is only relevant for DFI versions 3.1 and beyond. Set to 1 to enable or clear to 0 to disable.

4.2.140 DDRSS_CTL_141 Register (Offset = 234h) [reset = X]

DDRSS_CTL_141 is shown in [Figure 4-189](#) and described in [Table 4-382](#).

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Table 4-381. DDRSS_CTL_141 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0234h

Figure 4-189. DDRSS_CTL_141 Register

31	30	29	28	27	26	25	24
RESERVED				LP_AUTO_EXIT_EN			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				LP_AUTO_ENTRY_EN			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		LP_STATE_CS1					
R/W-X		R-40h					
7	6	5	4	3	2	1	0
RESERVED		LP_STATE_CS0					
R/W-X		R-40h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-382. DDRSS_CTL_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	LP_AUTO_EXIT_EN	R/W	0h	Enable auto exit from each of the low power states when a read or write command enters the command queue. Bit (0) controls power-down, bit (1) controls self-refresh long or self-refresh power-down long, bit (2) controls self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating, and bit (3) controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable.
23-20	RESERVED	R/W	X	
19-16	LP_AUTO_ENTRY_EN	R/W	0h	Enable auto entry into each of the low power states when the associated idle timer expires. Bit (0) controls power-down, bit (1) controls self-refresh long or self-refresh power-down long, bit (2) controls self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating, and bit (3) controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable.
15	RESERVED	R/W	X	
14-8	LP_STATE_CS1	R	40h	Low power state status parameter for chip select 1. Bits (5:0) indicate the current low power state and bit (6) set indicates that status bits are valid. READ-ONLY
7	RESERVED	R/W	X	

Table 4-382. DDRSS_CTL_141 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-0	LP_STATE_CS0	R	40h	<p>Low power state status parameter for chip select 0.</p> <p>Bits (5:0) indicate the current low power state and bit (6) set indicates that status bits are valid.</p> <p>READ-ONLY</p>

4.2.141 DDRSS_CTL_142 Register (Offset = 238h) [reset = X]

DDRSS_CTL_142 is shown in [Figure 4-190](#) and described in [Table 4-384](#).

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Table 4-383. DDRSS_CTL_142 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0238h

Figure 4-190. DDRSS_CTL_142 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				LP_AUTO_PD_IDLE			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
LP_AUTO_PD_IDLE							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					LP_AUTO_MEM_GATE_EN		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-384. DDRSS_CTL_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	LP_AUTO_PD_IDLE	R/W	0h	Defines the idle time (in controller clocks) until the controller will automatically issue an entry into one of the power-down low power states.
7-3	RESERVED	R/W	X	
2-0	LP_AUTO_MEM_GATE_EN	R/W	0h	Enable memory clock gating when entering a low power state via the auto low power counters. Bit (0) controls power-down, bit (1) controls self-refresh long or self-refresh power-down long, and bit (2) controls self-refresh short or self-refresh power-down short. Set each bit to 1 to enable.

4.2.142 DDRSS_CTL_143 Register (Offset = 23Ch) [reset = X]

DDRSS_CTL_143 is shown in [Figure 4-191](#) and described in [Table 4-386](#).

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Table 4-385. DDRSS_CTL_143 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 023Ch

Figure 4-191. DDRSS_CTL_143 Register

31	30	29	28	27	26	25	24
LP_AUTO_SR_LONG_MC_GATE_IDLE							
R/W-0h							
23	22	21	20	19	18	17	16
LP_AUTO_SR_LONG_IDLE							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				LP_AUTO_SR_SHORT_IDLE			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
LP_AUTO_SR_SHORT_IDLE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-386. DDRSS_CTL_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	LP_AUTO_SR_LONG_M C_GATE_IDLE	R/W	0h	Defines the idle time (in long counts) until the controller will automatically issue an entry into the self-refresh long with memory and controller clock gating or self-refresh power-down long with memory and controller clock gating low power states.
23-16	LP_AUTO_SR_LONG_ID LE	R/W	0h	Defines the idle time (in long counts) until the controller will automatically issue an entry into the self-refresh long or self-refresh power-down long (with or without memory clock gating) low power states.
15-12	RESERVED	R/W	X	
11-0	LP_AUTO_SR_SHORT_I DLE	R/W	0h	Defines the idle time (in controller clocks) until the controller will automatically issue an entry into the self-refresh short or self-refresh power-down short (with or without memory clock gating) low power states.

4.2.143 DDRSS_CTL_144 Register (Offset = 240h) [reset = 0h]

DDRSS_CTL_144 is shown in [Figure 4-192](#) and described in [Table 4-388](#).

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Table 4-387. DDRSS_CTL_144 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0240h

Figure 4-192. DDRSS_CTL_144 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HW_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-388. DDRSS_CTL_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HW_PROMOTE_THRES HOLD_F1	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted for frequency copy 1.
15-0	HW_PROMOTE_THRES HOLD_F0	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted for frequency copy 0.

4.2.144 DDRSS_CTL_145 Register (Offset = 244h) [reset = 0h]

DDRSS_CTL_145 is shown in [Figure 4-193](#) and described in [Table 4-390](#).

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Table 4-389. DDRSS_CTL_145 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0244h

Figure 4-193. DDRSS_CTL_145 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPC_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HW_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-390. DDRSS_CTL_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	LPC_PROMOTE_THRES HOLD_F0	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 0. Applies to SW and auto low power commands.
15-0	HW_PROMOTE_THRES HOLD_F2	R/W	0h	HW interface promotion number of long counts until the high priority request is asserted for frequency copy 2.

4.2.145 DDRSS_CTL_146 Register (Offset = 248h) [reset = 0h]

DDRSS_CTL_146 is shown in [Figure 4-194](#) and described in [Table 4-392](#).

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Table 4-391. DDRSS_CTL_146 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0248h

Figure 4-194. DDRSS_CTL_146 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPC_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPC_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-392. DDRSS_CTL_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	LPC_PROMOTE_THRES HOLD_F2	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW and auto low power commands.
15-0	LPC_PROMOTE_THRES HOLD_F1	R/W	0h	LPC promotion number of long counts until the high priority request is asserted for frequency copy 1. Applies to SW and auto low power commands.

4.2.146 DDRSS_CTL_147 Register (Offset = 24Ch) [reset = X]

DDRSS_CTL_147 is shown in [Figure 4-195](#) and described in [Table 4-394](#).

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Table 4-393. DDRSS_CTL_147 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 024Ch

Figure 4-195. DDRSS_CTL_147 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							LPC_SR_PHY MSTR_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							LPC_SR_PHYU PD_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							LPC_SR_CTRL UPD_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-394. DDRSS_CTL_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	LPC_SR_PHYMSTR_EN	R/W	0h	Enable LPC to execute a DFI PHY Master request on a self-refresh exit sequence. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	LPC_SR_PHYUPD_EN	R/W	0h	Enable LPC to execute a DFI PHY update on a self-refresh exit sequence. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	LPC_SR_CTRLUPD_EN	R/W	0h	Enable LPC to execute a DFI control update on a self-refresh exit sequence. Set to 1 to enable.

4.2.147 DDRSS_CTL_148 Register (Offset = 250h) [reset = X]

DDRSS_CTL_148 is shown in [Figure 4-196](#) and described in [Table 4-396](#).

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Table 4-395. DDRSS_CTL_148 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0250h

Figure 4-196. DDRSS_CTL_148 Register

31	30	29	28	27	26	25	24
RESERVED		PCPCS_PD_EXIT_DEPTH					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PCPCS_PD_ENTER_DEPTH					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							PCPCS_PD_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							LPC_SR_ZQ_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-396. DDRSS_CTL_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PCPCS_PD_EXIT_DEPTH	R/W	0h	Defines the number of entries of the command queue that the PCPCS logic will consider for dynamic power-down exit decode. A non-zero value limits the decode to a subset of the full command pipeline.
23-22	RESERVED	R/W	X	
21-16	PCPCS_PD_ENTER_DEPTH	R/W	0h	Defines the number of entries of the command queue that the PCPCS logic will consider for dynamic power-down entry decode. A non-zero value limits the decode to a subset of the full command pipeline.
15-9	RESERVED	R/W	X	
8	PCPCS_PD_EN	R/W	0h	Enable dynamic PCPCS to allow chip selects to dynamically enter and exit power-down. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	LPC_SR_ZQ_EN	R/W	0h	Enable LPC to execute a ZQ calibration on a self-refresh exit sequence. Set to 1 to enable.

4.2.148 DDRSS_CTL_149 Register (Offset = 254h) [reset = X]

DDRSS_CTL_149 is shown in [Figure 4-197](#) and described in [Table 4-398](#).

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Table 4-397. DDRSS_CTL_149 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0254h

Figure 4-197. DDRSS_CTL_149 Register

31	30	29	28	27	26	25	24
RESERVED							DFS_ENABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PCPCS_PD_MASK	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PCPCS_PD_ENTER_TIMER							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-398. DDRSS_CTL_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DFS_ENABLE	R/W	0h	Enable hardware dynamic frequency scaling. Set to 1 to enable.
23-16	RESERVED	R/W	0h	Reserved
15-10	RESERVED	R/W	X	
9-8	PCPCS_PD_MASK	R/W	0h	Disables dynamic PCPCS power-down entry/exit for particular chip selects if the PCPCS_PD_EN parameter is set. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to disable the chip select from allowing dynamic PCPCS.
7-0	PCPCS_PD_ENTER_TIMER	R/W	0h	Sets the delay used by dynamic PCPCS from when the decode logic determines that a chip select has no outstanding transactions to when the power-down entry command is issued. A zero value disables the timer and issues the power-down entry immediately on decode.

4.2.149 DDRSS_CTL_150 Register (Offset = 258h) [reset = X]

DDRSS_CTL_150 is shown in [Figure 4-198](#) and described in [Table 4-400](#).

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Table 4-399. DDRSS_CTL_150 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0258h

Figure 4-198. DDRSS_CTL_150 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TDFI_INIT_START_F0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-400. DDRSS_CTL_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TDFI_INIT_COMPLETE_F0	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency copy 0, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY.
15-10	RESERVED	R/W	X	
9-0	TDFI_INIT_START_F0	R/W	0h	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency copy 0, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY.

4.2.150 DDRSS_CTL_151 Register (Offset = 25Ch) [reset = X]

DDRSS_CTL_151 is shown in [Figure 4-199](#) and described in [Table 4-402](#).

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Table 4-401. DDRSS_CTL_151 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 025Ch

Figure 4-199. DDRSS_CTL_151 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TDFI_INIT_START_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-402. DDRSS_CTL_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TDFI_INIT_COMPLETE_F1	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency copy 1, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY.
15-10	RESERVED	R/W	X	
9-0	TDFI_INIT_START_F1	R/W	0h	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency copy 1, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY.

4.2.151 DDRSS_CTL_152 Register (Offset = 260h) [reset = X]

DDRSS_CTL_152 is shown in [Figure 4-200](#) and described in [Table 4-404](#).

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Table 4-403. DDRSS_CTL_152 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0260h

Figure 4-200. DDRSS_CTL_152 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDFI_INIT_COMPLETE_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TDFI_INIT_START_F2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-404. DDRSS_CTL_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TDFI_INIT_COMPLETE_F2	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency copy 2, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY.
15-10	RESERVED	R/W	X	
9-0	TDFI_INIT_START_F2	R/W	0h	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency copy 2, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY.

4.2.152 DDRSS_CTL_153 Register (Offset = 264h) [reset = X]

DDRSS_CTL_153 is shown in [Figure 4-201](#) and described in [Table 4-406](#).

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Table 4-405. DDRSS_CTL_153 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0264h

Figure 4-201. DDRSS_CTL_153 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							DFS_PHY_REG_WRITE_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						CURRENT_REG_COPY	
R/W-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-406. DDRSS_CTL_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	DFS_PHY_REG_WRITE_EN	R/W	0h	Enable a register write to the PHY during a frequency change. Set to 1 to enable.
7-2	RESERVED	R/W	X	
1-0	CURRENT_REG_COPY	R	0h	Indicates the current copy of timing parameters that is in use by the controller. READ-ONLY

4.2.153 DDRSS_CTL_154 Register (Offset = 268h) [reset = 0h]

DDRSS_CTL_154 is shown in [Figure 4-202](#) and described in [Table 4-408](#).

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Table 4-407. DDRSS_CTL_154 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0268h

Figure 4-202. DDRSS_CTL_154 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_ADDR																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-408. DDRSS_CTL_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DFS_PHY_REG_WRITE_ADDR	R/W	0h	Register address which will be written during a frequency change. Must be a PHY register address.

4.2.154 DDRSS_CTL_155 Register (Offset = 26Ch) [reset = 0h]

DDRSS_CTL_155 is shown in [Figure 4-203](#) and described in [Table 4-410](#).

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Table 4-409. DDRSS_CTL_155 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 026Ch

Figure 4-203. DDRSS_CTL_155 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-410. DDRSS_CTL_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DFS_PHY_REG_WRITE_DATA_F0	R/W	0h	Register data which will be written during a frequency change for frequency copy 0.

4.2.155 DDRSS_CTL_156 Register (Offset = 270h) [reset = 0h]

DDRSS_CTL_156 is shown in [Figure 4-204](#) and described in [Table 4-412](#).

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Table 4-411. DDRSS_CTL_156 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0270h

Figure 4-204. DDRSS_CTL_156 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-412. DDRSS_CTL_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DFS_PHY_REG_WRITE_DATA_F1	R/W	0h	Register data which will be written during a frequency change for frequency copy 1.

4.2.156 DDRSS_CTL_157 Register (Offset = 274h) [reset = 0h]

DDRSS_CTL_157 is shown in [Figure 4-205](#) and described in [Table 4-414](#).

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Table 4-413. DDRSS_CTL_157 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0274h

Figure 4-205. DDRSS_CTL_157 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFS_PHY_REG_WRITE_DATA_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-414. DDRSS_CTL_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DFS_PHY_REG_WRITE_DATA_F2	R/W	0h	Register data which will be written during a frequency change for frequency copy 2.

4.2.157 DDRSS_CTL_158 Register (Offset = 278h) [reset = X]

DDRSS_CTL_158 is shown in [Figure 4-206](#) and described in [Table 4-416](#).

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Table 4-415. DDRSS_CTL_158 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0278h

Figure 4-206. DDRSS_CTL_158 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DFS_PHY_REG_WRITE_WAIT							
R/W-0h							
15	14	13	12	11	10	9	8
DFS_PHY_REG_WRITE_WAIT							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				DFS_PHY_REG_WRITE_MASK			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-416. DDRSS_CTL_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-8	DFS_PHY_REG_WRITE_WAIT	R/W	0h	Defines the number of DFI PHY clocks that the controller will wait after issuing the register write to the PHY during a frequency change.
7-4	RESERVED	R/W	X	
3-0	DFS_PHY_REG_WRITE_MASK	R/W	0h	Register mask which will be written during a frequency change.

4.2.158 DDRSS_CTL_159 Register (Offset = 27Ch) [reset = X]

DDRSS_CTL_159 is shown in [Figure 4-207](#) and described in [Table 4-418](#).

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Table 4-417. DDRSS_CTL_159 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 027Ch

Figure 4-207. DDRSS_CTL_159 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					WRITE_MODEREG																										
R/W-X					R/W-0h																										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-418. DDRSS_CTL_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	WRITE_MODEREG	R/W	0h	Write memory mode register data to the DRAMs. Bits (7:0) define the memory mode register number if bit (23) is set, bits (15:8) define the chip select if bit (24) is clear, bits (23:16) define which memory mode register/s to write, bit (24) defines whether all chip selects will be written, and bit (25) triggers the write.

4.2.159 DDRSS_CTL_160 Register (Offset = 280h) [reset = X]

DDRSS_CTL_160 is shown in [Figure 4-208](#) and described in [Table 4-420](#).

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Table 4-419. DDRSS_CTL_160 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0280h

Figure 4-208. DDRSS_CTL_160 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								READ_MODEREG							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_MODEREG								MRW_STATUS							
R/W-0h								R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-420. DDRSS_CTL_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-8	READ_MODEREG	R/W	0h	Read the specified memory mode register from specified chip when start bit set. Bits (7:0) define the memory mode register and bits (15:8) define the chip select. Set bit (16) to 1 to trigger.
7-0	MRW_STATUS	R	0h	Write memory mode register status. Bit (0) set indicates a WRITE_MODEREG parameter programming error. Bit (1) set indicates a PASR error. Bit (2) is Reserved. Bit (3) set indicates a self-refresh or deep power-down error. Bit (4) set indicates that a write to MR3 or MR11 was attempted (WRITE_MODEREG bit (25) was asserted with bit (17) set, or bit (23) was asserted with bits (7:0) defining MR3 or MR11) during tZQCAL after a ZQ calibration start command. READ-ONLY

4.2.160 DDRSS_CTL_161 Register (Offset = 284h) [reset = 0h]

DDRSS_CTL_161 is shown in [Figure 4-209](#) and described in [Table 4-422](#).

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Table 4-421. DDRSS_CTL_161 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0284h

Figure 4-209. DDRSS_CTL_161 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PERIPHERAL_MRR_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-422. DDRSS_CTL_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PERIPHERAL_MRR_DATA_0	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter. Bits (7:0) indicate the read data and bits (15:8) indicate the chip. READ-ONLY

4.2.161 DDRSS_CTL_162 Register (Offset = 288h) [reset = X]

DDRSS_CTL_162 is shown in [Figure 4-210](#) and described in [Table 4-424](#).

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Table 4-423. DDRSS_CTL_162 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0288h

Figure 4-210. DDRSS_CTL_162 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								AUTO_TEMPCHK_VAL_0							
R-X								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AUTO_TEMPCHK_VAL_0								PERIPHERAL_MRR_DATA_1							
R-0h								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-424. DDRSS_CTL_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-8	AUTO_TEMPCHK_VAL_0	R	0h	MR4 data for all devices on chip 0 accessed by automatic MRR commands. Bits (3:0) correlate to the device on the lower byte, bits (7:4) correlate to the devices on the 2nd byte etc. Value indicates the OP7, OP2, OP1 and OP0 bits. READ-ONLY
7-0	PERIPHERAL_MRR_DATA_1	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter. Bits (7:0) indicate the read data and bits (15:8) indicate the chip. READ-ONLY

4.2.162 DDRSS_CTL_163 Register (Offset = 28Ch) [reset = X]

DDRSS_CTL_163 is shown in [Figure 4-211](#) and described in [Table 4-426](#).

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Table 4-425. DDRSS_CTL_163 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 028Ch

Figure 4-211. DDRSS_CTL_163 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						DISABLE_UPD ATE_TVRCG	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
AUTO_TEMPCHK_VAL_1							
R-0h							
7	6	5	4	3	2	1	0
AUTO_TEMPCHK_VAL_1							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-426. DDRSS_CTL_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	DISABLE_UPDATE_TVR CG	R/W	0h	Bypass changing for TVRCG during a DFS operation. Set to 1 to skip TVRCG.
15-0	AUTO_TEMPCHK_VAL_1	R	0h	MR4 data for all devices on chip 1 accessed by automatic MRR commands. Bits (3:0) correlate to the device on the lower byte, bits (7:4) correlate to the devices on the 2nd byte etc. Value indicates the OP7, OP2, OP1 and OP0 bits. READ-ONLY

4.2.163 DDRSS_CTL_164 Register (Offset = 290h) [reset = X]

DDRSS_CTL_164 is shown in [Figure 4-212](#) and described in [Table 4-428](#).

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Table 4-427. DDRSS_CTL_164 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0290h

Figure 4-212. DDRSS_CTL_164 Register

31	30	29	28	27	26	25	24
RESERVED						TVRCG_ENABLE_F0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
TVRCG_ENABLE_F0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						MRW_DFS_UPDATE_FRC	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-428. DDRSS_CTL_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TVRCG_ENABLE_F0	R/W	0h	JEDEC TVRCG_ENABLE time.
15-2	RESERVED	R/W	X	
1-0	MRW_DFS_UPDATE_FRC	R/W	0h	Defines the frequency register set to use when doing a software MRW with WRITE_MODEREG bit (26).

4.2.164 DDRSS_CTL_165 Register (Offset = 294h) [reset = X]

DDRSS_CTL_165 is shown in [Figure 4-213](#) and described in [Table 4-430](#).

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Table 4-429. DDRSS_CTL_165 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0294h

Figure 4-213. DDRSS_CTL_165 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TFC_F0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TVRCG_DISABLE_F0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-430. DDRSS_CTL_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TFC_F0	R/W	0h	JEDEC TFC, the frequency set point switching time.
15-10	RESERVED	R/W	X	
9-0	TVRCG_DISABLE_F0	R/W	0h	JEDEC TVRCG_DISABLE time.

4.2.165 DDRSS_CTL_166 Register (Offset = 298h) [reset = X]

DDRSS_CTL_166 is shown in [Figure 4-214](#) and described in [Table 4-432](#).

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Table 4-431. DDRSS_CTL_166 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0298h

Figure 4-214. DDRSS_CTL_166 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TVREF_LONG_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKFSPX_F0				RESERVED				TCKFSPE_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-432. DDRSS_CTL_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TVREF_LONG_F0	R/W	0h	JEDEC TVREF, design will always use the long value.
15-13	RESERVED	R/W	X	
12-8	TCKFSPX_F0	R/W	0h	JEDEC TCKFSPX, the valid clock requirement before 1st valid command after FSP change.
7-5	RESERVED	R/W	X	
4-0	TCKFSPE_F0	R/W	0h	JEDEC TCKFSPE, the valid clock requirement after entering SDP change.

4.2.166 DDRSS_CTL_167 Register (Offset = 29Ch) [reset = X]

DDRSS_CTL_167 is shown in [Figure 4-215](#) and described in [Table 4-434](#).

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Table 4-433. DDRSS_CTL_167 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 029Ch

Figure 4-215. DDRSS_CTL_167 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TVRCG_DISABLE_F1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TVRCG_ENABLE_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-434. DDRSS_CTL_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TVRCG_DISABLE_F1	R/W	0h	JEDEC TVRCG_DISABLE time.
15-10	RESERVED	R/W	X	
9-0	TVRCG_ENABLE_F1	R/W	0h	JEDEC TVRCG_ENABLE time.

4.2.167 DDRSS_CTL_168 Register (Offset = 2A0h) [reset = X]

DDRSS_CTL_168 is shown in [Figure 4-216](#) and described in [Table 4-436](#).

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Table 4-435. DDRSS_CTL_168 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02A0h

Figure 4-216. DDRSS_CTL_168 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TCKFSPX_F1				RESERVED				TCKFSPE_F1			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TFC_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-436. DDRSS_CTL_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	TCKFSPX_F1	R/W	0h	JEDEC TCKFSPX, the valid clock requirement before 1st valid command after FSP change.
23-21	RESERVED	R/W	X	
20-16	TCKFSPE_F1	R/W	0h	JEDEC TCKFSPE, the valid clock requirement after entering SDP change.
15-10	RESERVED	R/W	X	
9-0	TFC_F1	R/W	0h	JEDEC TFC, the frequency set point switching time.

4.2.168 DDRSS_CTL_169 Register (Offset = 2A4h) [reset = X]

DDRSS_CTL_169 is shown in [Figure 4-217](#) and described in [Table 4-438](#).

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Table 4-437. DDRSS_CTL_169 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02A4h

Figure 4-217. DDRSS_CTL_169 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TVRCG_ENABLE_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TVREF_LONG_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-438. DDRSS_CTL_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TVRCG_ENABLE_F2	R/W	0h	JEDEC TVRCG_ENABLE time.
15-0	TVREF_LONG_F1	R/W	0h	JEDEC TVREF, design will always use the long value.

4.2.169 DDRSS_CTL_170 Register (Offset = 2A8h) [reset = X]

DDRSS_CTL_170 is shown in [Figure 4-218](#) and described in [Table 4-440](#).

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Table 4-439. DDRSS_CTL_170 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02A8h

Figure 4-218. DDRSS_CTL_170 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TFC_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TVRCG_DISABLE_F2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-440. DDRSS_CTL_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TFC_F2	R/W	0h	JEDEC TFC, the frequency set point switching time.
15-10	RESERVED	R/W	X	
9-0	TVRCG_DISABLE_F2	R/W	0h	JEDEC TVRCG_DISABLE time.

4.2.170 DDRSS_CTL_171 Register (Offset = 2ACh) [reset = X]

DDRSS_CTL_171 is shown in [Figure 4-219](#) and described in [Table 4-442](#).

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Table 4-441. DDRSS_CTL_171 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02ACh

Figure 4-219. DDRSS_CTL_171 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TVREF_LONG_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TCKFSPX_F2				RESERVED				TCKFSPE_F2			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-442. DDRSS_CTL_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TVREF_LONG_F2	R/W	0h	JEDEC TVREF, design will always use the long value.
15-13	RESERVED	R/W	X	
12-8	TCKFSPX_F2	R/W	0h	JEDEC TCKFSPX, the valid clock requirement before 1st valid command after FSP change.
7-5	RESERVED	R/W	X	
4-0	TCKFSPE_F2	R/W	0h	JEDEC TCKFSPE, the valid clock requirement after entering SDP change.

4.2.171 DDRSS_CTL_172 Register (Offset = 2B0h) [reset = 0h]

DDRSS_CTL_172 is shown in [Figure 4-220](#) and described in [Table 4-444](#).

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Table 4-443. DDRSS_CTL_172 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02B0h

Figure 4-220. DDRSS_CTL_172 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRR_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRR_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-444. DDRSS_CTL_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRR_PROMOTE_THRES HOLD_F1	R/W	0h	MRR promotion number of long counts until the high priority request is asserted for frequency copy 1. Applies to SW MRR commands.
15-0	MRR_PROMOTE_THRES HOLD_F0	R/W	0h	MRR promotion number of long counts until the high priority request is asserted for frequency copy 0. Applies to SW MRR commands.

4.2.172 DDRSS_CTL_173 Register (Offset = 2B4h) [reset = 0h]

DDRSS_CTL_173 is shown in [Figure 4-221](#) and described in [Table 4-446](#).

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Table 4-445. DDRSS_CTL_173 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02B4h

Figure 4-221. DDRSS_CTL_173 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRW_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRR_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-446. DDRSS_CTL_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRW_PROMOTE_THRESHOLD_F0	R/W	0h	MRW promotion number of long counts until the high priority request is asserted for frequency copy 0. Applies to SW MRW commands.
15-0	MRR_PROMOTE_THRESHOLD_F2	R/W	0h	MRR promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW MRR commands.

4.2.173 DDRSS_CTL_174 Register (Offset = 2B8h) [reset = 0h]

DDRSS_CTL_174 is shown in [Figure 4-222](#) and described in [Table 4-448](#).

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Table 4-447. DDRSS_CTL_174 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02B8h

Figure 4-222. DDRSS_CTL_174 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MRW_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MRW_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-448. DDRSS_CTL_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MRW_PROMOTE_THRESHOLD_F2	R/W	0h	MRW promotion number of long counts until the high priority request is asserted for frequency copy 2. Applies to SW MRW commands.
15-0	MRW_PROMOTE_THRESHOLD_F1	R/W	0h	MRW promotion number of long counts until the high priority request is asserted for frequency copy 1. Applies to SW MRW commands.

4.2.174 DDRSS_CTL_175 Register (Offset = 2BCh) [reset = 0h]

DDRSS_CTL_175 is shown in [Figure 4-223](#) and described in [Table 4-450](#).

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Table 4-449. DDRSS_CTL_175 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02BCh

Figure 4-223. DDRSS_CTL_175 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR2_DATA_F1_0								MR1_DATA_F1_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR2_DATA_F0_0								MR1_DATA_F0_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-450. DDRSS_CTL_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR2_DATA_F1_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency copy 1.
23-16	MR1_DATA_F1_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency copy 1.
15-8	MR2_DATA_F0_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency copy 0.
7-0	MR1_DATA_F0_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency copy 0.

4.2.175 DDRSS_CTL_176 Register (Offset = 2C0h) [reset = 0h]

DDRSS_CTL_176 is shown in [Figure 4-224](#) and described in [Table 4-452](#).

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Table 4-451. DDRSS_CTL_176 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02C0h

Figure 4-224. DDRSS_CTL_176 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR3_DATA_F0_0								MRSINGLE_DATA_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR2_DATA_F2_0								MR1_DATA_F2_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-452. DDRSS_CTL_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR3_DATA_F0_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency copy 0.
23-16	MRSINGLE_DATA_0	R/W	0h	Data to program into memory mode register single write to chip select 0.
15-8	MR2_DATA_F2_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency copy 2.
7-0	MR1_DATA_F2_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency copy 2.

4.2.176 DDRSS_CTL_177 Register (Offset = 2C4h) [reset = 0h]

DDRSS_CTL_177 is shown in [Figure 4-225](#) and described in [Table 4-454](#).

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Table 4-453. DDRSS_CTL_177 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02C4h

Figure 4-225. DDRSS_CTL_177 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR4_DATA_F1_0								MR4_DATA_F0_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR3_DATA_F2_0								MR3_DATA_F1_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-454. DDRSS_CTL_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR4_DATA_F1_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency copy 1.
23-16	MR4_DATA_F0_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency copy 0.
15-8	MR3_DATA_F2_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency copy 2.
7-0	MR3_DATA_F1_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency copy 1.

4.2.177 DDRSS_CTL_178 Register (Offset = 2C8h) [reset = 0h]

DDRSS_CTL_178 is shown in [Figure 4-226](#) and described in [Table 4-456](#).

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Table 4-455. DDRSS_CTL_178 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02C8h

Figure 4-226. DDRSS_CTL_178 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR11_DATA_F1_0								MR11_DATA_F0_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR8_DATA_0								MR4_DATA_F2_0							
R-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-456. DDRSS_CTL_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR11_DATA_F1_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency copy 1.
23-16	MR11_DATA_F0_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency copy 0.
15-8	MR8_DATA_0	R	0h	Data read from MR8 for chip select 0. READ-ONLY
7-0	MR4_DATA_F2_0	R/W	0h	Data to program into memory mode register 4 for chip select 0 for frequency copy 2.

4.2.178 DDRSS_CTL_179 Register (Offset = 2CCh) [reset = 0h]

DDRSS_CTL_179 is shown in [Figure 4-227](#) and described in [Table 4-458](#).

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Table 4-457. DDRSS_CTL_179 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02CCh

Figure 4-227. DDRSS_CTL_179 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR12_DATA_F2_0								MR12_DATA_F1_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR12_DATA_F0_0								MR11_DATA_F2_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-458. DDRSS_CTL_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR12_DATA_F2_0	R/W	0h	Data to program into memory mode register 12 for chip select 0.
23-16	MR12_DATA_F1_0	R/W	0h	Data to program into memory mode register 12 for chip select 0.
15-8	MR12_DATA_F0_0	R/W	0h	Data to program into memory mode register 12 for chip select 0.
7-0	MR11_DATA_F2_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency copy 2.

4.2.179 DDRSS_CTL_180 Register (Offset = 2D0h) [reset = 0h]

DDRSS_CTL_180 is shown in [Figure 4-228](#) and described in [Table 4-460](#).

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Table 4-459. DDRSS_CTL_180 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02D0h

Figure 4-228. DDRSS_CTL_180 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR14_DATA_F2_0								MR14_DATA_F1_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR14_DATA_F0_0								MR13_DATA_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-460. DDRSS_CTL_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR14_DATA_F2_0	R/W	0h	Data to program into memory mode register 14 for chip select 0.
23-16	MR14_DATA_F1_0	R/W	0h	Data to program into memory mode register 14 for chip select 0.
15-8	MR14_DATA_F0_0	R/W	0h	Data to program into memory mode register 14 for chip select 0.
7-0	MR13_DATA_0	R/W	0h	Data to program into memory mode register 13 for chip select 0.

4.2.180 DDRSS_CTL_181 Register (Offset = 2D4h) [reset = 0h]

DDRSS_CTL_181 is shown in [Figure 4-229](#) and described in [Table 4-462](#).

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Table 4-461. DDRSS_CTL_181 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02D4h

Figure 4-229. DDRSS_CTL_181 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR22_DATA_F0_0								MR20_DATA_0							
R/W-0h								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR17_DATA_0								MR16_DATA_0							
R/W-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-462. DDRSS_CTL_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR22_DATA_F0_0	R/W	0h	Data to program into memory mode register 22 for chip select 0.
23-16	MR20_DATA_0	R	0h	Data read from MR20 for chip select 0. READ-ONLY
15-8	MR17_DATA_0	R/W	0h	Data to program into memory mode register 17 for chip select 0.
7-0	MR16_DATA_0	R/W	0h	Data to program into memory mode register 16 for chip select 0.

4.2.181 DDRSS_CTL_182 Register (Offset = 2D8h) [reset = 0h]

DDRSS_CTL_182 is shown in [Figure 4-230](#) and described in [Table 4-464](#).

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Table 4-463. DDRSS_CTL_182 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02D8h

Figure 4-230. DDRSS_CTL_182 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR2_DATA_F0_1								MR1_DATA_F0_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR22_DATA_F2_0								MR22_DATA_F1_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-464. DDRSS_CTL_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR2_DATA_F0_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency copy 0.
23-16	MR1_DATA_F0_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency copy 0.
15-8	MR22_DATA_F2_0	R/W	0h	Data to program into memory mode register 22 for chip select 0.
7-0	MR22_DATA_F1_0	R/W	0h	Data to program into memory mode register 22 for chip select 0.

4.2.182 DDRSS_CTL_183 Register (Offset = 2DCh) [reset = 0h]

DDRSS_CTL_183 is shown in [Figure 4-231](#) and described in [Table 4-466](#).

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Table 4-465. DDRSS_CTL_183 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02DCh

Figure 4-231. DDRSS_CTL_183 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR2_DATA_F2_1								MR1_DATA_F2_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR2_DATA_F1_1								MR1_DATA_F1_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-466. DDRSS_CTL_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR2_DATA_F2_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency copy 2.
23-16	MR1_DATA_F2_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency copy 2.
15-8	MR2_DATA_F1_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency copy 1.
7-0	MR1_DATA_F1_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency copy 1.

4.2.183 DDRSS_CTL_184 Register (Offset = 2E0h) [reset = 0h]

DDRSS_CTL_184 is shown in [Figure 4-232](#) and described in [Table 4-468](#).

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Table 4-467. DDRSS_CTL_184 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02E0h

Figure 4-232. DDRSS_CTL_184 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR3_DATA_F2_1								MR3_DATA_F1_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR3_DATA_F0_1								MRSINGLE_DATA_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-468. DDRSS_CTL_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR3_DATA_F2_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency copy 2.
23-16	MR3_DATA_F1_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency copy 1.
15-8	MR3_DATA_F0_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency copy 0.
7-0	MRSINGLE_DATA_1	R/W	0h	Data to program into memory mode register single write to chip select 1.

4.2.184 DDRSS_CTL_185 Register (Offset = 2E4h) [reset = 0h]

DDRSS_CTL_185 is shown in [Figure 4-233](#) and described in [Table 4-470](#).

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Table 4-469. DDRSS_CTL_185 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02E4h

Figure 4-233. DDRSS_CTL_185 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR8_DATA_1								MR4_DATA_F2_1							
R-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR4_DATA_F1_1								MR4_DATA_F0_1							
R/W-0h								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-470. DDRSS_CTL_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR8_DATA_1	R	0h	Data read from MR8 for chip select 1. READ-ONLY
23-16	MR4_DATA_F2_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency copy 2.
15-8	MR4_DATA_F1_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency copy 1.
7-0	MR4_DATA_F0_1	R/W	0h	Data to program into memory mode register 4 for chip select 1 for frequency copy 0.

4.2.185 DDRSS_CTL_186 Register (Offset = 2E8h) [reset = 0h]

DDRSS_CTL_186 is shown in [Figure 4-234](#) and described in [Table 4-472](#).

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Table 4-471. DDRSS_CTL_186 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02E8h

Figure 4-234. DDRSS_CTL_186 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR12_DATA_F0_1								MR11_DATA_F2_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR11_DATA_F1_1								MR11_DATA_F0_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-472. DDRSS_CTL_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR12_DATA_F0_1	R/W	0h	Data to program into memory mode register 12 for chip select 1.
23-16	MR11_DATA_F2_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency copy 2.
15-8	MR11_DATA_F1_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency copy 1.
7-0	MR11_DATA_F0_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency copy 0.

4.2.186 DDRSS_CTL_187 Register (Offset = 2ECh) [reset = 0h]

DDRSS_CTL_187 is shown in [Figure 4-235](#) and described in [Table 4-474](#).

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Table 4-473. DDRSS_CTL_187 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02ECh

Figure 4-235. DDRSS_CTL_187 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR14_DATA_F0_1								MR13_DATA_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR12_DATA_F2_1								MR12_DATA_F1_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-474. DDRSS_CTL_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR14_DATA_F0_1	R/W	0h	Data to program into memory mode register 14 for chip select 1.
23-16	MR13_DATA_1	R/W	0h	Data to program into memory mode register 13 for chip select 1.
15-8	MR12_DATA_F2_1	R/W	0h	Data to program into memory mode register 12 for chip select 1.
7-0	MR12_DATA_F1_1	R/W	0h	Data to program into memory mode register 12 for chip select 1.

4.2.187 DDRSS_CTL_188 Register (Offset = 2F0h) [reset = 0h]

DDRSS_CTL_188 is shown in [Figure 4-236](#) and described in [Table 4-476](#).

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Table 4-475. DDRSS_CTL_188 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02F0h

Figure 4-236. DDRSS_CTL_188 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR17_DATA_1								MR16_DATA_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR14_DATA_F2_1								MR14_DATA_F1_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-476. DDRSS_CTL_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR17_DATA_1	R/W	0h	Data to program into memory mode register 17 for chip select 1.
23-16	MR16_DATA_1	R/W	0h	Data to program into memory mode register 16 for chip select 1.
15-8	MR14_DATA_F2_1	R/W	0h	Data to program into memory mode register 14 for chip select 1.
7-0	MR14_DATA_F1_1	R/W	0h	Data to program into memory mode register 14 for chip select 1.

4.2.188 DDRSS_CTL_189 Register (Offset = 2F4h) [reset = 0h]

DDRSS_CTL_189 is shown in [Figure 4-237](#) and described in [Table 4-478](#).

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Table 4-477. DDRSS_CTL_189 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02F4h

Figure 4-237. DDRSS_CTL_189 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MR22_DATA_F2_1								MR22_DATA_F1_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MR22_DATA_F0_1								MR20_DATA_1							
R/W-0h								R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-478. DDRSS_CTL_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	MR22_DATA_F2_1	R/W	0h	Data to program into memory mode register 22 for chip select 1.
23-16	MR22_DATA_F1_1	R/W	0h	Data to program into memory mode register 22 for chip select 1.
15-8	MR22_DATA_F0_1	R/W	0h	Data to program into memory mode register 22 for chip select 1.
7-0	MR20_DATA_1	R	0h	Data read from MR20 for chip select 1. READ-ONLY

4.2.189 DDRSS_CTL_190 Register (Offset = 2F8h) [reset = X]

DDRSS_CTL_190 is shown in [Figure 4-238](#) and described in [Table 4-480](#).

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Table 4-479. DDRSS_CTL_190 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02F8h

Figure 4-238. DDRSS_CTL_190 Register

31	30	29	28	27	26	25	24
RESERVED							MR_FSP_DATA_VALID_F2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							MR_FSP_DATA_VALID_F1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							MR_FSP_DATA_VALID_F0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
MR23_DATA							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-480. DDRSS_CTL_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	MR_FSP_DATA_VALID_F2	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter(s). Value of 1 means memory was trained.
23-17	RESERVED	R/W	X	
16	MR_FSP_DATA_VALID_F1	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter(s). Value of 1 means memory was trained.
15-9	RESERVED	R/W	X	
8	MR_FSP_DATA_VALID_F0	R/W	0h	Indicates that, at this frequency, memory was trained and the associated data has been loaded into the MRx_DATA parameter(s). Value of 1 means memory was trained.
7-0	MR23_DATA	R/W	0h	Data to program into memory mode register 23.

4.2.190 DDRSS_CTL_191 Register (Offset = 2FCh) [reset = X]

DDRSS_CTL_191 is shown in [Figure 4-239](#) and described in [Table 4-482](#).

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Table 4-481. DDRSS_CTL_191 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 02FCh

Figure 4-239. DDRSS_CTL_191 Register

31	30	29	28	27	26	25	24
RESERVED							FSP_PHY_UPD ATE_MRW
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R/W-X							R-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED						RL3_SUPPORT_EN	
R/W-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-482. DDRSS_CTL_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FSP_PHY_UPDATE_MR W	R/W	0h	Identifies the logic responsible for updating MR12 and MR14 in memory. Clear to 0 for the controller, or set to 1 for the PHY or PI.
23-17	RESERVED	R/W	X	
16	RESERVED	R	0h	Reserved
15-9	RESERVED	R/W	X	
8	RESERVED	R	0h	Reserved
7-2	RESERVED	R/W	X	
1-0	RL3_SUPPORT_EN	R	0h	Indicates if RL3 is supported by a connected LPDDR3 memory. Data read from MR0 bit 7. READ-ONLY

4.2.191 DDRSS_CTL_192 Register (Offset = 300h) [reset = X]

DDRSS_CTL_192 is shown in [Figure 4-240](#) and described in [Table 4-484](#).

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Table 4-483. DDRSS_CTL_192 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0300h

Figure 4-240. DDRSS_CTL_192 Register

31	30	29	28	27	26	25	24
RESERVED							FSP_WR_CURRENT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							FSP_OP_CURRENT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							FSP_STATUS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							DFS_ALWAYS_WRITE_FSP
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-484. DDRSS_CTL_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	FSP_WR_CURRENT	R/W	0h	Reports which FSP set the memory will target with write commands.
23-17	RESERVED	R/W	X	
16	FSP_OP_CURRENT	R/W	0h	Reports which FSP set the memory is currently using.
15-9	RESERVED	R/W	X	
8	FSP_STATUS	R/W	0h	Indicates that a DFS event caused the FSP mode registers to be updated. Value of 1 means that the FSP mode registers were changed.
7-1	RESERVED	R/W	X	
0	DFS_ALWAYS_WRITE_FSP	R/W	0h	Forces all FSP mode registers to be written by the controller during a DFS event. Set to 1 to force the write.

4.2.192 DDRSS_CTL_193 Register (Offset = 304h) [reset = X]

DDRSS_CTL_193 is shown in [Figure 4-241](#) and described in [Table 4-486](#).

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Table 4-485. DDRSS_CTL_193 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0304h

Figure 4-241. DDRSS_CTL_193 Register

31	30	29	28	27	26	25	24
RESERVED						FSP1_FRC	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						FSP0_FRC	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						FSP1_FRC_VALID	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						FSP0_FRC_VALID	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-486. DDRSS_CTL_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	FSP1_FRC	R/W	0h	Identifies which of the controller's frequency copy is associated with FSP1.
23-18	RESERVED	R/W	X	
17-16	FSP0_FRC	R/W	0h	Identifies which of the controller's frequency copy is associated with FSP0.
15-9	RESERVED	R/W	X	
8	FSP1_FRC_VALID	R/W	0h	Specifies whether the FSP set defined in the FSP1_FRC parameter reflects the frequency used to program the FSP1 registers.
7-1	RESERVED	R/W	X	
0	FSP0_FRC_VALID	R/W	0h	Specifies whether the FSP set defined in the FSP0_FRC parameter reflects the frequency used to program the FSP0 registers.

4.2.193 DDRSS_CTL_194 Register (Offset = 308h) [reset = X]

DDRSS_CTL_194 is shown in [Figure 4-242](#) and described in [Table 4-488](#).

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Table 4-487. DDRSS_CTL_194 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0308h

Figure 4-242. DDRSS_CTL_194 Register

31	30	29	28	27	26	25	24
RESERVED							BIST_DATA_CHECK
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		ADDR_SPACE					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED						BIST_RESULT	
R/W-X						R-0h	
7	6	5	4	3	2	1	0
RESERVED							BIST_GO
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-488. DDRSS_CTL_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	BIST_DATA_CHECK	R/W	0h	Enable data checking with BIST operation. Set to 1 to enable.
23-22	RESERVED	R/W	X	
21-16	ADDR_SPACE	R/W	0h	Sets the number of address bits to check during BIST operation.
15-10	RESERVED	R/W	X	
9-8	BIST_RESULT	R	0h	BIST operation status (pass/fail). Bit (0) indicates data check status and bit (1) indicates address check status. Value of 1 is a passing result. READ-ONLY
7-1	RESERVED	R/W	X	
0	BIST_GO	W	0h	Initiate a BIST operation. Set to 1 to trigger. WRITE-ONLY

4.2.194 DDRSS_CTL_195 Register (Offset = 30Ch) [reset = X]

DDRSS_CTL_195 is shown in [Figure 4-243](#) and described in [Table 4-490](#).

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Table 4-489. DDRSS_CTL_195 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 030Ch

Figure 4-243. DDRSS_CTL_195 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							BIST_ADDR_CHECK
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-490. DDRSS_CTL_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	BIST_ADDR_CHECK	R/W	0h	Enable address checking with BIST operation. Set to 1 to enable.

4.2.195 DDRSS_CTL_196 Register (Offset = 310h) [reset = 0h]

DDRSS_CTL_196 is shown in [Figure 4-244](#) and described in [Table 4-492](#).

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Table 4-491. DDRSS_CTL_196 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0310h

Figure 4-244. DDRSS_CTL_196 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_START_ADDRESS_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-492. DDRSS_CTL_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_START_ADDRESS_0	R/W	0h	Start BIST checking at this address.

4.2.196 DDRSS_CTL_197 Register (Offset = 314h) [reset = X]

DDRSS_CTL_197 is shown in [Figure 4-245](#) and described in [Table 4-494](#).

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Table 4-493. DDRSS_CTL_197 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0314h

Figure 4-245. DDRSS_CTL_197 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					BIST_START_ADDRESS_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-494. DDRSS_CTL_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	BIST_START_ADDRESS_1	R/W	0h	Start BIST checking at this address.

4.2.197 DDRSS_CTL_198 Register (Offset = 318h) [reset = 0h]

DDRSS_CTL_198 is shown in [Figure 4-246](#) and described in [Table 4-496](#).

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Table 4-495. DDRSS_CTL_198 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0318h

Figure 4-246. DDRSS_CTL_198 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_DATA_MASK_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-496. DDRSS_CTL_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_DATA_MASK_0	R/W	0h	Mask applied to data for BIST error checking. Bit (0) controls memory data path bit (0), bit (1) controls memory data path bit (1), etc. Set each bit to 1 to mask.

4.2.198 DDRSS_CTL_199 Register (Offset = 31Ch) [reset = 0h]

DDRSS_CTL_199 is shown in [Figure 4-247](#) and described in [Table 4-498](#).

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Table 4-497. DDRSS_CTL_199 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 031Ch

Figure 4-247. DDRSS_CTL_199 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_DATA_MASK_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-498. DDRSS_CTL_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_DATA_MASK_1	R/W	0h	Mask applied to data for BIST error checking. Bit (0) controls memory data path bit (0), bit (1) controls memory data path bit (1), etc. Set each bit to 1 to mask.

4.2.199 DDRSS_CTL_200 Register (Offset = 320h) [reset = X]

DDRSS_CTL_200 is shown in [Figure 4-248](#) and described in [Table 4-500](#).

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Table 4-499. DDRSS_CTL_200 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0320h

Figure 4-248. DDRSS_CTL_200 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					BIST_TEST_MODE		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-500. DDRSS_CTL_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	BIST_TEST_MODE	R/W	0h	Sets the BIST test mode. Value of 0 specifies standard BIST operation, value of 1 specifies a reduced BIST operation, value of 2 specifies a self-refresh retention test, value of 3 specifies an idle retention test, and value of 4 specifies memory initialization function. All other values are reserved.

4.2.200 DDRSS_CTL_201 Register (Offset = 324h) [reset = 0h]

DDRSS_CTL_201 is shown in [Figure 4-249](#) and described in [Table 4-502](#).

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Table 4-501. DDRSS_CTL_201 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0324h

Figure 4-249. DDRSS_CTL_201 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-502. DDRSS_CTL_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_DATA_PATTERN_0	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4.

4.2.201 DDRSS_CTL_202 Register (Offset = 328h) [reset = 0h]

DDRSS_CTL_202 is shown in [Figure 4-250](#) and described in [Table 4-504](#).

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Table 4-503. DDRSS_CTL_202 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0328h

Figure 4-250. DDRSS_CTL_202 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-504. DDRSS_CTL_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_DATA_PATTERN_1	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4.

4.2.202 DDRSS_CTL_203 Register (Offset = 32Ch) [reset = 0h]

DDRSS_CTL_203 is shown in [Figure 4-251](#) and described in [Table 4-506](#).

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Table 4-505. DDRSS_CTL_203 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 032Ch

Figure 4-251. DDRSS_CTL_203 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-506. DDRSS_CTL_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_DATA_PATTERN_2	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4.

4.2.203 DDRSS_CTL_204 Register (Offset = 330h) [reset = 0h]

DDRSS_CTL_204 is shown in [Figure 4-252](#) and described in [Table 4-508](#).

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Table 4-507. DDRSS_CTL_204 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0330h

Figure 4-252. DDRSS_CTL_204 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_DATA_PATTERN_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-508. DDRSS_CTL_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_DATA_PATTERN_3	R/W	0h	Data pattern to be used when the BIST_TEST_MODE parameter is programmed to 1, 2, 3 or 4.

4.2.204 DDRSS_CTL_205 Register (Offset = 334h) [reset = X]

DDRSS_CTL_205 is shown in [Figure 4-253](#) and described in [Table 4-510](#).

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Table 4-509. DDRSS_CTL_205 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0334h

Figure 4-253. DDRSS_CTL_205 Register

31	30	29	28	27	26	25	24
RESERVED				BIST_ERR_STOP			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
BIST_ERR_STOP							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							BIST_RET_STATE
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED							BIST_RET_STATE_EXIT
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-510. DDRSS_CTL_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	BIST_ERR_STOP	R/W	0h	Defines the maximum number of error occurrences allowed prior to quitting when the BIST_TEST_MODE parameter is programmed to 1, 2 or 3. A value of 0 will allow the test to run to completion.
15-9	RESERVED	R/W	X	
8	BIST_RET_STATE	R	0h	Indicates if BIST is in a retention wait state, used when the BIST_TEST_MODE parameter is programmed to 2 or 3. Value of 1 indicates BIST is waiting. READ-ONLY
7-1	RESERVED	R/W	X	
0	BIST_RET_STATE_EXIT	W	0h	Exit self-refresh or idle retention state, used when the BIST_TEST_MODE parameter is programmed to 2 or 3. Set to 1 to trigger. WRITE-ONLY

4.2.205 DDRSS_CTL_206 Register (Offset = 338h) [reset = X]

DDRSS_CTL_206 is shown in [Figure 4-254](#) and described in [Table 4-512](#).

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Note

The ECC Engine block of the DDR controller is not supported.

Table 4-511. DDRSS_CTL_206 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0338h

Figure 4-254. DDRSS_CTL_206 Register

31	30	29	28	27	26	25	24
RESERVED					INLINE_ECC_BANK_OFFSET		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					ECC_ENABLE		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED				BIST_ERR_COUNT			
R/W-X				R-0h			
7	6	5	4	3	2	1	0
BIST_ERR_COUNT							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-512. DDRSS_CTL_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	INLINE_ECC_BANK_OFFSET	R/W	0h	Inline ECC Bank Offset defines the bank shift between data and ECC commands associated with the same sequence the bank is offset to prevent inefficiencies due to opening an closing the pages on the same bank during transition between data and ECC commands.
23-18	RESERVED	R/W	X	
17-16	ECC_ENABLE	R/W	0h	ECC error checking and correcting control register. Clear to 0 to fully disable ECC, program to 1 to enable ECC with no error detection or error correction, program to 2 to enable ECC with error detection without error correction, or program to 3 to enable ECC with both error detection and error correction.
15-12	RESERVED	R/W	X	
11-0	BIST_ERR_COUNT	R	0h	Indicates the number of BIST errors found when the BIST_TEST_MODE parameter is programmed to 1, 2 or 3. READ-ONLY

4.2.206 DDRSS_CTL_207 Register (Offset = 33Ch) [reset = X]

DDRSS_CTL_207 is shown in [Figure 4-255](#) and described in [Table 4-514](#).

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Table 4-513. DDRSS_CTL_207 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 033Ch

Figure 4-255. DDRSS_CTL_207 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							ECC_WRITE_C OMBINING_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							ECC_READ_C ACHING_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-514. DDRSS_CTL_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	ECC_WRITE_COMBINING_EN	R/W	0h	Allows ECC write data within a given ECC buffer to be combined across commands so that in certain cases where we see multiple ECC writes to the same ECC address, the controller may end up only issuing one final ECC write command to memory.
7-1	RESERVED	R/W	X	
0	ECC_READ_CACHING_EN	R/W	0h	Allows ECC read data already in one of the ECC buffers to be used when possible in place of issuing an ECC read command to memory. This implies that some ECC read commands will be dropped in the command queue when it can pull the read data from the buffer instead.

4.2.207 DDRSS_CTL_208 Register (Offset = 340h) [reset = X]

DDRSS_CTL_208 is shown in [Figure 4-256](#) and described in [Table 4-516](#).

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Table 4-515. DDRSS_CTL_208 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0340h

Figure 4-256. DDRSS_CTL_208 Register

31	30	29	28	27	26	25	24
RESERVED							ECC_WRITEBACK_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
XOR_CHECK_BITS							
R/W-0h							
15	14	13	12	11	10	9	8
XOR_CHECK_BITS							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							FWC
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-516. DDRSS_CTL_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ECC_WRITEBACK_EN	R/W	0h	ECC writeback will occur on detection of single bit errors for reads. The ECC_ENABLE parameter must be programmed to 3 for this to take any effect. Note that no writebacks will be issued during BIST.
23-8	XOR_CHECK_BITS	R/W	0h	Value to xor with generated ECC codes for forced write check.
7-1	RESERVED	R/W	X	
0	FWC	R/W	0h	Force a write check. Xor the XOR_CHECK_BITS parameter with the ECC code and write to memory. Set to 1 to trigger.

4.2.208 DDRSS_CTL_209 Register (Offset = 344h) [reset = X]

DDRSS_CTL_209 is shown in [Figure 4-257](#) and described in [Table 4-518](#).

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Table 4-517. DDRSS_CTL_209 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0344h

Figure 4-257. DDRSS_CTL_209 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ECC_DISABLE_W_UC_ERR
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-518. DDRSS_CTL_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ECC_DISABLE_W_UC_ERR	R/W	0h	Controls auto-corruption of ECC when un-correctable errors occur in R/M/W operations. Set to 1 to disable corruption.

4.2.209 DDRSS_CTL_210 Register (Offset = 348h) [reset = 0h]

DDRSS_CTL_210 is shown in [Figure 4-258](#) and described in [Table 4-520](#).

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Table 4-519. DDRSS_CTL_210 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0348h

Figure 4-258. DDRSS_CTL_210 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_U_ADDR_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-520. DDRSS_CTL_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_U_ADDR_0	R	0h	Address of uncorrectable ECC event. READ-ONLY

4.2.210 DDRSS_CTL_211 Register (Offset = 34Ch) [reset = X]

DDRSS_CTL_211 is shown in [Figure 4-259](#) and described in [Table 4-522](#).

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Table 4-521. DDRSS_CTL_211 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 034Ch

Figure 4-259. DDRSS_CTL_211 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
ECC_U_SYND							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_U_ADDR_1		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 4-522. DDRSS_CTL_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	ECC_U_SYND	R	0h	Syndrome for uncorrectable ECC event. READ-ONLY
7-3	RESERVED	R	X	
2-0	ECC_U_ADDR_1	R	0h	Address of uncorrectable ECC event. READ-ONLY

4.2.211 DDRSS_CTL_212 Register (Offset = 350h) [reset = 0h]

DDRSS_CTL_212 is shown in [Figure 4-260](#) and described in [Table 4-524](#).

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Table 4-523. DDRSS_CTL_212 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0350h

Figure 4-260. DDRSS_CTL_212 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_U_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-524. DDRSS_CTL_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_U_DATA_0	R	0h	Data associated with uncorrectable ECC event. READ-ONLY

4.2.212 DDRSS_CTL_213 Register (Offset = 354h) [reset = 0h]

DDRSS_CTL_213 is shown in [Figure 4-261](#) and described in [Table 4-526](#).

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Table 4-525. DDRSS_CTL_213 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0354h

Figure 4-261. DDRSS_CTL_213 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_U_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-526. DDRSS_CTL_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_U_DATA_1	R	0h	Data associated with uncorrectable ECC event. READ-ONLY

4.2.213 DDRSS_CTL_214 Register (Offset = 358h) [reset = 0h]

DDRSS_CTL_214 is shown in [Figure 4-262](#) and described in [Table 4-528](#).

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Table 4-527. DDRSS_CTL_214 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0358h

Figure 4-262. DDRSS_CTL_214 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_C_ADDR_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-528. DDRSS_CTL_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_C_ADDR_0	R	0h	Address of correctable ECC event. READ-ONLY

4.2.214 DDRSS_CTL_215 Register (Offset = 35Ch) [reset = X]

DDRSS_CTL_215 is shown in [Figure 4-263](#) and described in [Table 4-530](#).

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Table 4-529. DDRSS_CTL_215 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 035Ch

Figure 4-263. DDRSS_CTL_215 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
ECC_C_SYND							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ECC_C_ADDR_1		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 4-530. DDRSS_CTL_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	ECC_C_SYND	R	0h	Syndrome for correctable ECC event. READ-ONLY
7-3	RESERVED	R	X	
2-0	ECC_C_ADDR_1	R	0h	Address of correctable ECC event. READ-ONLY

4.2.215 DDRSS_CTL_216 Register (Offset = 360h) [reset = 0h]

DDRSS_CTL_216 is shown in [Figure 4-264](#) and described in [Table 4-532](#).

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Table 4-531. DDRSS_CTL_216 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0360h

Figure 4-264. DDRSS_CTL_216 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_C_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-532. DDRSS_CTL_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_C_DATA_0	R	0h	Data associated with correctable ECC event. READ-ONLY

4.2.216 DDRSS_CTL_217 Register (Offset = 364h) [reset = 0h]

DDRSS_CTL_217 is shown in [Figure 4-265](#) and described in [Table 4-534](#).

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Table 4-533. DDRSS_CTL_217 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0364h

Figure 4-265. DDRSS_CTL_217 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_C_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-534. DDRSS_CTL_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_C_DATA_1	R	0h	Data associated with correctable ECC event. READ-ONLY

4.2.217 DDRSS_CTL_218 Register (Offset = 368h) [reset = X]

DDRSS_CTL_218 is shown in [Figure 4-266](#) and described in [Table 4-536](#).

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Table 4-535. DDRSS_CTL_218 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0368h

Figure 4-266. DDRSS_CTL_218 Register

31	30	29	28	27	26	25	24
RESERVED	NON_ECC_REGION_START_ADDR_0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
NON_ECC_REGION_START_ADDR_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	ECC_C_ID						
R/W-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED	ECC_U_ID						
R/W-X	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-536. DDRSS_CTL_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	NON_ECC_REGION_START_ADDR_0	R/W	0h	Set the base address of the soft-designated non-ECC region 0. The address written is 1Mbyte aligned.
15-14	RESERVED	R/W	X	
13-8	ECC_C_ID	R	0h	Source ID associated with correctable ECC event. READ-ONLY
7-6	RESERVED	R/W	X	
5-0	ECC_U_ID	R	0h	Source ID associated with the uncorrectable ECC event. READ-ONLY

4.2.218 DDRSS_CTL_219 Register (Offset = 36Ch) [reset = X]

DDRSS_CTL_219 is shown in [Figure 4-267](#) and described in [Table 4-538](#).

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Table 4-537. DDRSS_CTL_219 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 036Ch

Figure 4-267. DDRSS_CTL_219 Register

31	30	29	28	27	26	25	24
RESERVED	NON_ECC_REGION_START_ADDR_1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
NON_ECC_REGION_START_ADDR_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	NON_ECC_REGION_END_ADDR_0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
NON_ECC_REGION_END_ADDR_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-538. DDRSS_CTL_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	NON_ECC_REGION_START_ADDR_1	R/W	0h	Set the base address of the soft-designated non-ECC region 1. The address written is 1Mbyte aligned.
15	RESERVED	R/W	X	
14-0	NON_ECC_REGION_END_ADDR_0	R/W	0h	Set the base address of the soft-designated non-ECC region 0. The address written is 1Mbyte aligned.

4.2.219 DDRSS_CTL_220 Register (Offset = 370h) [reset = X]

DDRSS_CTL_220 is shown in [Figure 4-268](#) and described in [Table 4-540](#).

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Table 4-539. DDRSS_CTL_220 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0370h

Figure 4-268. DDRSS_CTL_220 Register

31	30	29	28	27	26	25	24
RESERVED	NON_ECC_REGION_START_ADDR_2						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
NON_ECC_REGION_START_ADDR_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	NON_ECC_REGION_END_ADDR_1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
NON_ECC_REGION_END_ADDR_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-540. DDRSS_CTL_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	NON_ECC_REGION_START_ADDR_2	R/W	0h	Set the base address of the soft-designated non-ECC region 2. The address written is 1Mbyte aligned.
15	RESERVED	R/W	X	
14-0	NON_ECC_REGION_END_ADDR_1	R/W	0h	Set the base address of the soft-designated non-ECC region 1. The address written is 1Mbyte aligned.

4.2.220 DDRSS_CTL_221 Register (Offset = 374h) [reset = X]

DDRSS_CTL_221 is shown in [Figure 4-269](#) and described in [Table 4-542](#).

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Table 4-541. DDRSS_CTL_221 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0374h

Figure 4-269. DDRSS_CTL_221 Register

31	30	29	28	27	26	25	24
RESERVED							ECC_SCRUB_START
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED					NON_ECC_REGION_ENABLE		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED	NON_ECC_REGION_END_ADDR_2						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
NON_ECC_REGION_END_ADDR_2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-542. DDRSS_CTL_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ECC_SCRUB_START	W	0h	ECC scrubbing control. Set to 1 to kick start the scrubbing operation. WRITE-ONLY
23-19	RESERVED	R/W	X	
18-16	NON_ECC_REGION_ENABLE	R/W	0h	Enables each soft-designated non-ECC region. Bit (0) correlates to region 0, bit (1) correlates to region 1, etc. Set each bit to 1 to enable.
15	RESERVED	R/W	X	
14-0	NON_ECC_REGION_END_ADDR_2	R/W	0h	Set the base address of the soft-designated non-ECC region 2. The address written is 1Mbyte aligned.

4.2.221 DDRSS_CTL_222 Register (Offset = 378h) [reset = X]

DDRSS_CTL_222 is shown in [Figure 4-270](#) and described in [Table 4-544](#).

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Table 4-543. DDRSS_CTL_222 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0378h

Figure 4-270. DDRSS_CTL_222 Register

31	30	29	28	27	26	25	24
RESERVED							ECC_SCRUB_MODE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				ECC_SCRUB_LEN			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
ECC_SCRUB_LEN							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							ECC_SCRUB_IN_PROGRESS
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-544. DDRSS_CTL_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ECC_SCRUB_MODE	R/W	0h	Defines how often ECC scrubbing operations will occur. Clear to 0 to scrub at regular intervals as dictated by the ECC_SCRUB_INTERVAL parameter, or set to 1 to scrub only when the controller is idle.
23-20	RESERVED	R/W	X	
19-8	ECC_SCRUB_LEN	R/W	0h	Defines the length of the ECC scrubbing read command that the controller will issue.
7-1	RESERVED	R/W	X	
0	ECC_SCRUB_IN_PROGRESS	R	0h	Reports the scrubbing operation status. A value of 1 indicates that the controller is in the process of performing a scrubbing operation. READ-ONLY

4.2.222 DDRSS_CTL_223 Register (Offset = 37Ch) [reset = 0h]

DDRSS_CTL_223 is shown in [Figure 4-271](#) and described in [Table 4-546](#).

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Table 4-545. DDRSS_CTL_223 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 037Ch

Figure 4-271. DDRSS_CTL_223 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECC_SCRUB_IDLE_CNT															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_SCRUB_INTERVAL															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-546. DDRSS_CTL_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ECC_SCRUB_IDLE_CNT	R/W	0h	The number of controller clock cycles that the scrubbing engine will wait in controller idle state before starting scrubbing operations. Valid when the ECC_SCRUB_MODE parameter is set to 1.
15-0	ECC_SCRUB_INTERVAL	R/W	0h	The minimum interval between two ECC scrubbing commands in number of controller clock cycles. Valid when the ECC_SCRUB_MODE parameter is cleared to 0.

4.2.223 DDRSS_CTL_224 Register (Offset = 380h) [reset = 0h]

DDRSS_CTL_224 is shown in [Figure 4-272](#) and described in [Table 4-548](#).

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Table 4-547. DDRSS_CTL_224 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0380h

Figure 4-272. DDRSS_CTL_224 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_SCRUB_START_ADDR_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-548. DDRSS_CTL_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_SCRUB_START_ADDR_0	R/W	0h	The starting address from where scrubbing operations will begin.

4.2.224 DDRSS_CTL_225 Register (Offset = 384h) [reset = X]

DDRSS_CTL_225 is shown in [Figure 4-273](#) and described in [Table 4-550](#).

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Table 4-549. DDRSS_CTL_225 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0384h

Figure 4-273. DDRSS_CTL_225 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					ECC_SCRUB_START_ADDR_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-550. DDRSS_CTL_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	ECC_SCRUB_START_ADDR_1	R/W	0h	The starting address from where scrubbing operations will begin.

4.2.225 DDRSS_CTL_226 Register (Offset = 388h) [reset = 0h]

DDRSS_CTL_226 is shown in [Figure 4-274](#) and described in [Table 4-552](#).

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Table 4-551. DDRSS_CTL_226 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0388h

Figure 4-274. DDRSS_CTL_226 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECC_SCRUB_END_ADDR_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-552. DDRSS_CTL_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ECC_SCRUB_END_ADDR_0	R/W	0h	The end address where scrubbing operations will wrap around to the start address. If this parameter is cleared to 0, the maximum physical address will be considered as the end address.

4.2.226 DDRSS_CTL_227 Register (Offset = 38Ch) [reset = X]

DDRSS_CTL_227 is shown in [Figure 4-275](#) and described in [Table 4-554](#).

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Table 4-553. DDRSS_CTL_227 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 038Ch

Figure 4-275. DDRSS_CTL_227 Register

31	30	29	28	27	26	25	24
RESERVED				AREF_HIGH_THRESHOLD			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				AREF_NORM_THRESHOLD			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				LONG_COUNT_MASK			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED					ECC_SCRUB_END_ADDR_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-554. DDRSS_CTL_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	AREF_HIGH_THRESHOLD	R/W	0h	AREF number of pending refreshes until the high priority request is asserted.
23-21	RESERVED	R/W	X	
20-16	AREF_NORM_THRESHOLD	R/W	0h	AREF number of pending refreshes until the normal priority request is asserted.
15-13	RESERVED	R/W	X	
12-8	LONG_COUNT_MASK	R/W	0h	Reduces the length of the long counter from 1024 cycles. The only supported values are 0x00 (1024 cycles), 0x10 (512 clocks), 0x18 (256 clocks), 0x1C (128 clocks), 0x1E (64 clocks) and 0x1F (32 clocks).
7-3	RESERVED	R/W	X	
2-0	ECC_SCRUB_END_ADDR_1	R/W	0h	The end address where scrubbing operations will wrap around to the start address. If this parameter is cleared to 0, the maximum physical address will be considered as the end address.

4.2.227 DDRSS_CTL_228 Register (Offset = 390h) [reset = X]

DDRSS_CTL_228 is shown in [Figure 4-276](#) and described in [Table 4-556](#).

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Table 4-555. DDRSS_CTL_228 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0390h

Figure 4-276. DDRSS_CTL_228 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				AREF_CMD_MAX_PER_TREFI			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				AREF_MAX_CREDIT			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AREF_MAX_DEFICIT			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-556. DDRSS_CTL_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	AREF_CMD_MAX_PER_TREFI	R/W	0h	Sets the maximum number of auto-refreshes that will be executed in a TREFI period - both normal and high priority. This does not prevent refreshes generated by sub-task requests such as a self-refresh exit and enter.
15-13	RESERVED	R/W	X	
12-8	AREF_MAX_CREDIT	R/W	0h	AREF number of posted refreshes until the maximum number of refresh credits has been reached.
7-5	RESERVED	R/W	X	
4-0	AREF_MAX_DEFICIT	R/W	0h	AREF number of pending refreshes until the maximum number of refreshes has been exceeded.

4.2.228 DDRSS_CTL_229 Register (Offset = 394h) [reset = 0h]

DDRSS_CTL_229 is shown in [Figure 4-277](#) and described in [Table 4-558](#).

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Table 4-557. DDRSS_CTL_229 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0394h

Figure 4-277. DDRSS_CTL_229 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALSTART_HIGH_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALSTART_NORM_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-558. DDRSS_CTL_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALSTART_HIGH_THRESHOLD_F0	R/W	0h	ZQ START number of long counts until the high priority request is asserted for frequency copy 0.
15-0	ZQ_CALSTART_NORM_THRESHOLD_F0	R/W	0h	ZQ START number of long counts until the normal priority request is asserted for frequency copy 0. This value should be scaled based on the number of ranks (chip selects) the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be.

4.2.229 DDRSS_CTL_230 Register (Offset = 398h) [reset = 0h]

DDRSS_CTL_230 is shown in [Figure 4-278](#) and described in [Table 4-560](#).

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Table 4-559. DDRSS_CTL_230 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0398h

Figure 4-278. DDRSS_CTL_230 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CS_NORM_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALLATCH_HIGH_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-560. DDRSS_CTL_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CS_NORM_THRESH OLD_F0	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted for frequency copy 0.
15-0	ZQ_CALLATCH_HIGH_T HRESHOLD_F0	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted for frequency copy 0.

4.2.230 DDRSS_CTL_231 Register (Offset = 39Ch) [reset = 0h]

DDRSS_CTL_231 is shown in [Figure 4-279](#) and described in [Table 4-562](#).

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Table 4-561. DDRSS_CTL_231 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 039Ch

Figure 4-279. DDRSS_CTL_231 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALSTART_TIMEOUT_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CS_HIGH_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-562. DDRSS_CTL_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALSTART_TIMEOUT_F0	R/W	0h	ZQ START number of long counts until the timeout is asserted for frequency copy 0.
15-0	ZQ_CS_HIGH_THRESHOLD_F0	R/W	0h	ZQ CS number of long counts until the high priority request is asserted for frequency copy 0.

4.2.231 DDRSS_CTL_232 Register (Offset = 3A0h) [reset = 0h]

DDRSS_CTL_232 is shown in [Figure 4-280](#) and described in [Table 4-564](#).

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Table 4-563. DDRSS_CTL_232 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03A0h

Figure 4-280. DDRSS_CTL_232 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CS_TIMEOUT_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALLATCH_TIMEOUT_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-564. DDRSS_CTL_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CS_TIMEOUT_F0	R/W	0h	ZQ CS number of long counts until the timeout is asserted for frequency copy 0.
15-0	ZQ_CALLATCH_TIMEO T_F0	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted for frequency copy 0.

4.2.232 DDRSS_CTL_233 Register (Offset = 3A4h) [reset = 0h]

DDRSS_CTL_233 is shown in [Figure 4-281](#) and described in [Table 4-566](#).

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Table 4-565. DDRSS_CTL_233 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03A4h

Figure 4-281. DDRSS_CTL_233 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALSTART_NORM_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-566. DDRSS_CTL_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALSTART_NORM_THRESHOLD_F1	R/W	0h	ZQ START number of long counts until the normal priority request is asserted for frequency copy 1. This value should be scaled based on the number of ranks (chip selects) the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be.
15-0	ZQ_PROMOTE_THRESHOLD_F0	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted for frequency copy 0.

4.2.233 DDRSS_CTL_234 Register (Offset = 3A8h) [reset = 0h]

DDRSS_CTL_234 is shown in [Figure 4-282](#) and described in [Table 4-568](#).

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Table 4-567. DDRSS_CTL_234 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03A8h

Figure 4-282. DDRSS_CTL_234 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALLATCH_HIGH_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALSTART_HIGH_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-568. DDRSS_CTL_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALLATCH_HIGH_THRESHOLD_F1	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted for frequency copy 1.
15-0	ZQ_CALSTART_HIGH_THRESHOLD_F1	R/W	0h	ZQ START number of long counts until the high priority request is asserted for frequency copy 1.

4.2.234 DDRSS_CTL_235 Register (Offset = 3ACh) [reset = 0h]

DDRSS_CTL_235 is shown in [Figure 4-283](#) and described in [Table 4-570](#).

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Table 4-569. DDRSS_CTL_235 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03ACh

Figure 4-283. DDRSS_CTL_235 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CS_HIGH_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CS_NORM_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-570. DDRSS_CTL_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CS_HIGH_THRESHOLD_F1	R/W	0h	ZQ CS number of long counts until the high priority request is asserted for frequency copy 1.
15-0	ZQ_CS_NORM_THRESHOLD_F1	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted for frequency copy 1.

4.2.235 DDRSS_CTL_236 Register (Offset = 3B0h) [reset = 0h]

DDRSS_CTL_236 is shown in [Figure 4-284](#) and described in [Table 4-572](#).

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Table 4-571. DDRSS_CTL_236 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03B0h

Figure 4-284. DDRSS_CTL_236 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALLATCH_TIMEOUT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALSTART_TIMEOUT_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-572. DDRSS_CTL_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALLATCH_TIMEOUT_F1	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted for frequency copy 1.
15-0	ZQ_CALSTART_TIMEOUT_F1	R/W	0h	ZQ START number of long counts until the timeout is asserted for frequency copy 1.

4.2.236 DDRSS_CTL_237 Register (Offset = 3B4h) [reset = 0h]

DDRSS_CTL_237 is shown in [Figure 4-285](#) and described in [Table 4-574](#).

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Table 4-573. DDRSS_CTL_237 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03B4h

Figure 4-285. DDRSS_CTL_237 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CS_TIMEOUT_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-574. DDRSS_CTL_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_PROMOTE_THRESH OLD_F1	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted for frequency copy 1.
15-0	ZQ_CS_TIMEOUT_F1	R/W	0h	ZQ CS number of long counts until the timeout is asserted for frequency copy 1.

4.2.237 DDRSS_CTL_238 Register (Offset = 3B8h) [reset = 0h]

DDRSS_CTL_238 is shown in [Figure 4-286](#) and described in [Table 4-576](#).

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Table 4-575. DDRSS_CTL_238 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03B8h

Figure 4-286. DDRSS_CTL_238 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALSTART_HIGH_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALSTART_NORM_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-576. DDRSS_CTL_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALSTART_HIGH_THRESHOLD_F2	R/W	0h	ZQ START number of long counts until the high priority request is asserted for frequency copy 2.
15-0	ZQ_CALSTART_NORM_THRESHOLD_F2	R/W	0h	ZQ START number of long counts until the normal priority request is asserted for frequency copy 2. This value should be scaled based on the number of ranks (chip selects) the controller handles. The more chip selects there are, the more rotations there are to go through, and the smaller this threshold should be.

4.2.238 DDRSS_CTL_239 Register (Offset = 3BCh) [reset = 0h]

DDRSS_CTL_239 is shown in [Figure 4-287](#) and described in [Table 4-578](#).

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Table 4-577. DDRSS_CTL_239 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03BCh

Figure 4-287. DDRSS_CTL_239 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CS_NORM_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALLATCH_HIGH_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-578. DDRSS_CTL_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CS_NORM_THRESH OLD_F2	R/W	0h	ZQ CS number of long counts until the normal priority request is asserted for frequency copy 2.
15-0	ZQ_CALLATCH_HIGH_T HRESHOLD_F2	R/W	0h	ZQ LATCH number of long counts until the high priority request is asserted for frequency copy 2.

4.2.239 DDRSS_CTL_240 Register (Offset = 3C0h) [reset = 0h]

DDRSS_CTL_240 is shown in [Figure 4-288](#) and described in [Table 4-580](#).

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Table 4-579. DDRSS_CTL_240 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03C0h

Figure 4-288. DDRSS_CTL_240 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CALSTART_TIMEOUT_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CS_HIGH_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-580. DDRSS_CTL_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CALSTART_TIMEOUT_F2	R/W	0h	ZQ START number of long counts until the timeout is asserted for frequency copy 2.
15-0	ZQ_CS_HIGH_THRESHOLD_F2	R/W	0h	ZQ CS number of long counts until the high priority request is asserted for frequency copy 2.

4.2.240 DDRSS_CTL_241 Register (Offset = 3C4h) [reset = 0h]

DDRSS_CTL_241 is shown in [Figure 4-289](#) and described in [Table 4-582](#).

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Table 4-581. DDRSS_CTL_241 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03C4h

Figure 4-289. DDRSS_CTL_241 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ZQ_CS_TIMEOUT_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_CALLATCH_TIMEOUT_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-582. DDRSS_CTL_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ZQ_CS_TIMEOUT_F2	R/W	0h	ZQ CS number of long counts until the timeout is asserted for frequency copy 2.
15-0	ZQ_CALLATCH_TIMEO T_F2	R/W	0h	ZQ LATCH number of long counts until the timeout is asserted for frequency copy 2.

4.2.241 DDRSS_CTL_242 Register (Offset = 3C8h) [reset = X]

DDRSS_CTL_242 is shown in [Figure 4-290](#) and described in [Table 4-584](#).

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Table 4-583. DDRSS_CTL_242 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03C8h

Figure 4-290. DDRSS_CTL_242 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RESERVED			
R/W-X												R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZQ_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-584. DDRSS_CTL_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	RESERVED	R/W	0h	Reserved
15-0	ZQ_PROMOTE_THRESH OLD_F2	R/W	0h	ZQ SW promotion number of long counts until the high priority request is asserted for frequency copy 2.

4.2.242 DDRSS_CTL_243 Register (Offset = 3CCh) [reset = 0h]

DDRSS_CTL_243 is shown in [Figure 4-291](#) and described in [Table 4-586](#).

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Table 4-585. DDRSS_CTL_243 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03CCh

Figure 4-291. DDRSS_CTL_243 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_BUS_ARB_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_TASK_ARB_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-586. DDRSS_CTL_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_BUS_ARB_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.
15-0	WATCHDOG_THRESHOLD_TASK_ARB_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.

4.2.243 DDRSS_CTL_244 Register (Offset = 3D0h) [reset = 0h]

DDRSS_CTL_244 is shown in [Figure 4-292](#) and described in [Table 4-588](#).

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Table 4-587. DDRSS_CTL_244 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03D0h

Figure 4-292. DDRSS_CTL_244 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_SPLIT_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_PORT0_CMD_ARB_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-588. DDRSS_CTL_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_SPLIT_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.
15-0	WATCHDOG_THRESHOLD_PORT0_CMD_ARB_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.

4.2.244 DDRSS_CTL_245 Register (Offset = 3D4h) [reset = 0h]

DDRSS_CTL_245 is shown in [Figure 4-293](#) and described in [Table 4-590](#).

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Table 4-589. DDRSS_CTL_245 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03D4h

Figure 4-293. DDRSS_CTL_245 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_PORT_TO_STRATEGY_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_STRATEGY_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-590. DDRSS_CTL_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_PORT_TO_STRATEGY_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.
15-0	WATCHDOG_THRESHOLD_STRATEGY_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.

4.2.245 DDRSS_CTL_246 Register (Offset = 3D8h) [reset = 0h]

DDRSS_CTL_246 is shown in [Figure 4-294](#) and described in [Table 4-592](#).

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Table 4-591. DDRSS_CTL_246 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03D8h

Figure 4-294. DDRSS_CTL_246 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_WRITE_DATA_FIFO_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_READ_DATA_FIFO0_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-592. DDRSS_CTL_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_WRITE_DATA_FIFO_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.
15-0	WATCHDOG_THRESHOLD_READ_DATA_FIFO0_F0	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 0.

4.2.246 DDRSS_CTL_247 Register (Offset = 3DCh) [reset = 0h]

DDRSS_CTL_247 is shown in [Figure 4-295](#) and described in [Table 4-594](#).

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Table 4-593. DDRSS_CTL_247 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03DCh

Figure 4-295. DDRSS_CTL_247 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_BUS_ARB_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_TASK_ARB_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-594. DDRSS_CTL_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_BUS_ARB_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.
15-0	WATCHDOG_THRESHOLD_TASK_ARB_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.

4.2.247 DDRSS_CTL_248 Register (Offset = 3E0h) [reset = 0h]

DDRSS_CTL_248 is shown in [Figure 4-296](#) and described in [Table 4-596](#).

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Table 4-595. DDRSS_CTL_248 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03E0h

Figure 4-296. DDRSS_CTL_248 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_SPLIT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_PORT0_CMD_ARB_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-596. DDRSS_CTL_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_SPLIT_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.
15-0	WATCHDOG_THRESHOLD_PORT0_CMD_ARB_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.

4.2.248 DDRSS_CTL_249 Register (Offset = 3E4h) [reset = 0h]

DDRSS_CTL_249 is shown in [Figure 4-297](#) and described in [Table 4-598](#).

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Table 4-597. DDRSS_CTL_249 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03E4h

Figure 4-297. DDRSS_CTL_249 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_PORT_TO_STRATEGY_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_STRATEGY_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-598. DDRSS_CTL_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_PORT_TO_STRATEGY_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.
15-0	WATCHDOG_THRESHOLD_STRATEGY_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.

4.2.249 DDRSS_CTL_250 Register (Offset = 3E8h) [reset = 0h]

DDRSS_CTL_250 is shown in [Figure 4-298](#) and described in [Table 4-600](#).

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Table 4-599. DDRSS_CTL_250 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03E8h

Figure 4-298. DDRSS_CTL_250 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_WRITE_DATA_FIFO_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_READ_DATA_FIFO0_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-600. DDRSS_CTL_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_WRITE_DATA_FIFO_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.
15-0	WATCHDOG_THRESHOLD_READ_DATA_FIFO0_F1	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 1.

4.2.250 DDRSS_CTL_251 Register (Offset = 3ECh) [reset = 0h]

DDRSS_CTL_251 is shown in [Figure 4-299](#) and described in [Table 4-602](#).

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Table 4-601. DDRSS_CTL_251 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03ECh

Figure 4-299. DDRSS_CTL_251 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_BUS_ARB_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_TASK_ARB_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-602. DDRSS_CTL_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_BUS_ARB_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.
15-0	WATCHDOG_THRESHOLD_TASK_ARB_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.

4.2.251 DDRSS_CTL_252 Register (Offset = 3F0h) [reset = 0h]

DDRSS_CTL_252 is shown in [Figure 4-300](#) and described in [Table 4-604](#).

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Table 4-603. DDRSS_CTL_252 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03F0h

Figure 4-300. DDRSS_CTL_252 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_SPLIT_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_PORT0_CMD_ARB_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-604. DDRSS_CTL_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_SPLIT_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.
15-0	WATCHDOG_THRESHOLD_PORT0_CMD_ARB_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.

4.2.252 DDRSS_CTL_253 Register (Offset = 3F4h) [reset = 0h]

DDRSS_CTL_253 is shown in [Figure 4-301](#) and described in [Table 4-606](#).

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Table 4-605. DDRSS_CTL_253 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03F4h

Figure 4-301. DDRSS_CTL_253 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_PORT_TO_STRATEGY_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_STRATEGY_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-606. DDRSS_CTL_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_PORT_TO_STRATEGY_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.
15-0	WATCHDOG_THRESHOLD_STRATEGY_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.

4.2.253 DDRSS_CTL_254 Register (Offset = 3F8h) [reset = 0h]

DDRSS_CTL_254 is shown in [Figure 4-302](#) and described in [Table 4-608](#).

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Table 4-607. DDRSS_CTL_254 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03F8h

Figure 4-302. DDRSS_CTL_254 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WATCHDOG_THRESHOLD_WRITE_DATA_FIFO_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_THRESHOLD_READ_DATA_FIFO0_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-608. DDRSS_CTL_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WATCHDOG_THRESHOLD_WRITE_DATA_FIFO_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.
15-0	WATCHDOG_THRESHOLD_READ_DATA_FIFO0_F2	R/W	0h	When watchdog's counter reaches this threshold, it will assert an error when using frequency copy 2.

4.2.254 DDRSS_CTL_255 Register (Offset = 3FCh) [reset = X]

DDRSS_CTL_255 is shown in [Figure 4-303](#) and described in [Table 4-610](#).

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Table 4-609. DDRSS_CTL_255 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 03FCh

Figure 4-303. DDRSS_CTL_255 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WATCHDOG_DIAGNOSTIC_MODE								WATCHDOG_RELOAD							
R/W-0h								W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-610. DDRSS_CTL_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	WATCHDOG_DIAGNOSTIC_MODE	R/W	0h	Used to test watchdog timers or to force a failure. There is one bit for each watchdog timer. Under normal operation, a watchdog timer will increment its counter after every long counter cycle. To aid in generating watchdog faults for testing, a watchdog's counter can increment every controller clock cycle instead by setting the corresponding bit in this register to 1.
7-0	WATCHDOG_RELOAD	W	0h	Forces reload to assert on all watchdog timers, effectively restarting all watchdog counters and clearing any existing watchdog error assertions. WRITE-ONLY

4.2.255 DDRSS_CTL_256 Register (Offset = 400h) [reset = X]

DDRSS_CTL_256 is shown in [Figure 4-304](#) and described in [Table 4-612](#).

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Table 4-611. DDRSS_CTL_256 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0400h

Figure 4-304. DDRSS_CTL_256 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TIMEOUT_TIMER_LOG																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 4-612. DDRSS_CTL_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-0	TIMEOUT_TIMER_LOG	R	0h	<p>Reflects which timers experienced a timeout error (or had an uncleared error) when the timeout interrupt fired.</p> <p>Task arbiter watchdog error is reflected in bit 0.</p> <p>Bus arbiter watchdog error is reflected in bit 1.</p> <p>Port 0 command arbiter watchdog error is reflected in bit 2.</p> <p>Split watchdog error is reflected in bit 3.</p> <p>Strategy watchdog error is reflected in bit 4.</p> <p>Port to strategy watchdog error is reflected in bit 5.</p> <p>Write data FIFO watchdog error is reflected in bit 7.</p> <p>ZQ calstart FM timeout is reflected in bit 9.</p> <p>ZQ callatch FM timeout is reflected in bit 10.</p> <p>ZQ cal init, cs, cl, or reset FM timeout is reflected in bit 8.</p> <p>Read leveling FM timeout is reflected in bit 11.</p> <p>Read gate leveling FM timeout is reflected in bit 12.</p> <p>Write leveling FM timeout is reflected in bit 13.</p> <p>CA training FM timeout is reflected in bit 14.</p> <p>DQS oscillator FM timeout is reflected in bit 16.</p> <p>MRR temperature check FM timeout is reflected in bit 15.</p> <p>DFI update FM timeout is reflected in bit 17.</p> <p>Low power interface wakeup timeout is reflected in bit 18.</p> <p>Auto refresh max deficit timeout is reflected in bit 19.</p> <p>READ-ONLY</p>

4.2.256 DDRSS_CTL_257 Register (Offset = 404h) [reset = X]

DDRSS_CTL_257 is shown in [Figure 4-305](#) and described in [Table 4-614](#).

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Table 4-613. DDRSS_CTL_257 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0404h

Figure 4-305. DDRSS_CTL_257 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				ZQCL_F0											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ZQINIT_F0											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-614. DDRSS_CTL_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	ZQCL_F0	R/W	0h	Number of cycles needed for a ZQCL command for frequency copy 0.
15-12	RESERVED	R/W	X	
11-0	ZQINIT_F0	R/W	0h	Number of cycles needed for a ZQINIT command for frequency copy 0.

4.2.257 DDRSS_CTL_258 Register (Offset = 408h) [reset = X]

DDRSS_CTL_258 is shown in [Figure 4-306](#) and described in [Table 4-616](#).

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Table 4-615. DDRSS_CTL_258 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0408h

Figure 4-306. DDRSS_CTL_258 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TZQCAL_F0											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ZQCS_F0											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-616. DDRSS_CTL_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	TZQCAL_F0	R/W	0h	Holds the DRAM ZQCAL value for frequency copy 0 in cycles.
15-12	RESERVED	R/W	X	
11-0	ZQCS_F0	R/W	0h	Number of cycles needed for a ZQCS command for frequency copy 0.

4.2.258 DDRSS_CTL_259 Register (Offset = 40Ch) [reset = X]

DDRSS_CTL_259 is shown in [Figure 4-307](#) and described in [Table 4-618](#).

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Table 4-617. DDRSS_CTL_259 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 040Ch

Figure 4-307. DDRSS_CTL_259 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				ZQINIT_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
ZQINIT_F1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	TZQLAT_F0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-618. DDRSS_CTL_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	ZQINIT_F1	R/W	0h	Number of cycles needed for a ZQINIT command for frequency copy 1.
7	RESERVED	R/W	X	
6-0	TZQLAT_F0	R/W	0h	Holds the DRAM ZQLAT value for frequency copy 0 in cycles.

4.2.259 DDRSS_CTL_260 Register (Offset = 410h) [reset = X]

DDRSS_CTL_260 is shown in [Figure 4-308](#) and described in [Table 4-620](#).

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Table 4-619. DDRSS_CTL_260 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0410h

Figure 4-308. DDRSS_CTL_260 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				ZQCS_F1											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ZQCL_F1											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-620. DDRSS_CTL_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	ZQCS_F1	R/W	0h	Number of cycles needed for a ZQCS command for frequency copy 1.
15-12	RESERVED	R/W	X	
11-0	ZQCL_F1	R/W	0h	Number of cycles needed for a ZQCL command for frequency copy 1.

4.2.260 DDRSS_CTL_261 Register (Offset = 414h) [reset = X]

DDRSS_CTL_261 is shown in [Figure 4-309](#) and described in [Table 4-622](#).

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Table 4-621. DDRSS_CTL_261 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0414h

Figure 4-309. DDRSS_CTL_261 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									TZQLAT_F1						
R/W-X									R/W-0h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TZQCAL_F1											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-622. DDRSS_CTL_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	TZQLAT_F1	R/W	0h	Holds the DRAM ZQLAT value for frequency copy 1 in cycles.
15-12	RESERVED	R/W	X	
11-0	TZQCAL_F1	R/W	0h	Holds the DRAM ZQCAL value for frequency copy 1 in cycles.

4.2.261 DDRSS_CTL_262 Register (Offset = 418h) [reset = X]

DDRSS_CTL_262 is shown in [Figure 4-310](#) and described in [Table 4-624](#).

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Table 4-623. DDRSS_CTL_262 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0418h

Figure 4-310. DDRSS_CTL_262 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				ZQCL_F2											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ZQINIT_F2											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-624. DDRSS_CTL_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	ZQCL_F2	R/W	0h	Number of cycles needed for a ZQCL command for frequency copy 2.
15-12	RESERVED	R/W	X	
11-0	ZQINIT_F2	R/W	0h	Number of cycles needed for a ZQINIT command for frequency copy 2.

4.2.262 DDRSS_CTL_263 Register (Offset = 41Ch) [reset = X]

DDRSS_CTL_263 is shown in [Figure 4-311](#) and described in [Table 4-626](#).

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Table 4-625. DDRSS_CTL_263 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 041Ch

Figure 4-311. DDRSS_CTL_263 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TZQCAL_F2											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ZQCS_F2											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-626. DDRSS_CTL_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	TZQCAL_F2	R/W	0h	Holds the DRAM ZQCAL value for frequency copy 2 in cycles.
15-12	RESERVED	R/W	X	
11-0	ZQCS_F2	R/W	0h	Number of cycles needed for a ZQCS command for frequency copy 2.

4.2.263 DDRSS_CTL_264 Register (Offset = 420h) [reset = X]

DDRSS_CTL_264 is shown in [Figure 4-312](#) and described in [Table 4-628](#).

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Table 4-627. DDRSS_CTL_264 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0420h

Figure 4-312. DDRSS_CTL_264 Register

31	30	29	28	27	26	25	24
RESERVED							ZQ_REQ_PENDING
R/W-X							R-0h
23	22	21	20	19	18	17	16
RESERVED				ZQ_REQ			
R/W-X				W-0h			
15	14	13	12	11	10	9	8
RESERVED							ZQ_SW_REQ_START_LATCH_MAP
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED	TZQLAT_F2						
R/W-X	R/W-0h						

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-628. DDRSS_CTL_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ZQ_REQ_PENDING	R	0h	Indicates that a ZQ command is currently in progress or waiting to run. Value of 1 indicates command in progress or waiting to run. When this is asserted, no writes to ZQ_REQ should occur. READ-ONLY
23-20	RESERVED	R/W	X	
19-16	ZQ_REQ	W	0h	User request to initiate a ZQ calibration. Program to 1 for ZQ Short (ZQCS), program to 2 for ZQ Long (ZQCL), program to 3 for ZQ Start, program to 4 for ZQ Initialization (ZQINIT), program to 5 for ZQ Latch, or program to 8 for ZQ Reset. Clearing to 0 will not trigger any ZQ command. This parameter should only be written when the ZQ_REQ_PENDING parameter is cleared to 0. WRITE-ONLY
15-10	RESERVED	R/W	X	
9-8	ZQ_SW_REQ_START_LATCH_MAP	R/W	0h	Specifies which chip selects will simultaneously receive a ZQ start or latch command once the ZQ_REQ parameter is written with a ZQ Start or ZQ Latch command.
7	RESERVED	R/W	X	
6-0	TZQLAT_F2	R/W	0h	Holds the DRAM ZQLAT value for frequency copy 2 in cycles.

4.2.264 DDRSS_CTL_265 Register (Offset = 424h) [reset = X]

DDRSS_CTL_265 is shown in [Figure 4-313](#) and described in [Table 4-630](#).

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Table 4-629. DDRSS_CTL_265 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0424h

Figure 4-313. DDRSS_CTL_265 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				ZQRESET_F1											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				ZQRESET_F0											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-630. DDRSS_CTL_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	ZQRESET_F1	R/W	0h	Number of cycles needed for a ZQRESET command for frequency copy 1.
15-12	RESERVED	R/W	X	
11-0	ZQRESET_F0	R/W	0h	Number of cycles needed for a ZQRESET command for frequency copy 0.

4.2.265 DDRSS_CTL_266 Register (Offset = 428h) [reset = X]

DDRSS_CTL_266 is shown in [Figure 4-314](#) and described in [Table 4-632](#).

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Table 4-631. DDRSS_CTL_266 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0428h

Figure 4-314. DDRSS_CTL_266 Register

31	30	29	28	27	26	25	24
RESERVED							ZQCS_ROTATE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							NO_ZQ_INIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				ZQRESET_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
ZQRESET_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-632. DDRSS_CTL_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ZQCS_ROTATE	R/W	0h	For non-LPDDR4 memories, selects whether a ZQCS command will calibrate just one chip select or all chip selects. When rotation is off, all chip selects will be calibrated, requiring a longer time frame, but ZQ calibration will need to be performed less frequently. Set to 1 for rotating CS. For LPDDR4 memories, this parameter is ignored.
23-17	RESERVED	R/W	X	
16	NO_ZQ_INIT	R/W	0h	Disable ZQ operations during initialization. Set to 1 to disable.
15-12	RESERVED	R/W	X	
11-0	ZQRESET_F2	R/W	0h	Number of cycles needed for a ZQRESET command for frequency copy 2.

4.2.266 DDRSS_CTL_267 Register (Offset = 42Ch) [reset = X]

DDRSS_CTL_267 is shown in [Figure 4-315](#) and described in [Table 4-634](#).

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Table 4-633. DDRSS_CTL_267 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 042Ch

Figure 4-315. DDRSS_CTL_267 Register

31	30	29	28	27	26	25	24
RESERVED						ZQ_CAL_LATCH_MAP_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						ZQ_CAL_START_MAP_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						ZQ_CAL_LATCH_MAP_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						ZQ_CAL_START_MAP_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-634. DDRSS_CTL_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	ZQ_CAL_LATCH_MAP_1	R/W	0h	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands.
23-18	RESERVED	R/W	X	
17-16	ZQ_CAL_START_MAP_1	R/W	0h	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands.
15-10	RESERVED	R/W	X	
9-8	ZQ_CAL_LATCH_MAP_0	R/W	0h	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands.
7-2	RESERVED	R/W	X	
1-0	ZQ_CAL_START_MAP_0	R/W	0h	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands.

4.2.267 DDRSS_CTL_268 Register (Offset = 430h) [reset = X]

DDRSS_CTL_268 is shown in [Figure 4-316](#) and described in [Table 4-636](#).

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Table 4-635. DDRSS_CTL_268 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0430h

Figure 4-316. DDRSS_CTL_268 Register

31	30	29	28	27	26	25	24
RESERVED						ROW_DIFF_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						ROW_DIFF_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						BANK_DIFF_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						BANK_DIFF_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-636. DDRSS_CTL_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	ROW_DIFF_1	R/W	0h	Difference between number of address pins available and number being used for chip select 1.
23-19	RESERVED	R/W	X	
18-16	ROW_DIFF_0	R/W	0h	Difference between number of address pins available and number being used for chip select 0.
15-10	RESERVED	R/W	X	
9-8	BANK_DIFF_1	R/W	0h	Encoded number of banks on the DRAM for chip select 1.
7-2	RESERVED	R/W	X	
1-0	BANK_DIFF_0	R/W	0h	Encoded number of banks on the DRAM for chip select 0.

4.2.268 DDRSS_CTL_269 Register (Offset = 434h) [reset = X]

DDRSS_CTL_269 is shown in [Figure 4-317](#) and described in [Table 4-638](#).

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Table 4-637. DDRSS_CTL_269 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0434h

Figure 4-317. DDRSS_CTL_269 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CS_VAL_LOWER_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				COL_DIFF_1				RESERVED				COL_DIFF_0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-638. DDRSS_CTL_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CS_VAL_LOWER_0	R/W	0h	Lower bound address for chip select 0.
15-12	RESERVED	R/W	X	
11-8	COL_DIFF_1	R/W	0h	Difference between number of column pins available and number being used for chip select 1.
7-4	RESERVED	R/W	X	
3-0	COL_DIFF_0	R/W	0h	Difference between number of column pins available and number being used for chip select 0.

4.2.269 DDRSS_CTL_270 Register (Offset = 438h) [reset = X]

DDRSS_CTL_270 is shown in [Figure 4-318](#) and described in [Table 4-640](#).

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Table 4-639. DDRSS_CTL_270 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0438h

Figure 4-318. DDRSS_CTL_270 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				ROW_START_VAL_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
CS_VAL_UPPER_0							
R/W-0h							
7	6	5	4	3	2	1	0
CS_VAL_UPPER_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-640. DDRSS_CTL_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	ROW_START_VAL_0	R/W	0h	Row start value for chip select 0.
15-0	CS_VAL_UPPER_0	R/W	0h	Upper bound address for chip select 0.

4.2.270 DDRSS_CTL_271 Register (Offset = 43Ch) [reset = 0h]

DDRSS_CTL_271 is shown in [Figure 4-319](#) and described in [Table 4-642](#).

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Table 4-641. DDRSS_CTL_271 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 043Ch

Figure 4-319. DDRSS_CTL_271 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS_VAL_UPPER_1																CS_VAL_LOWER_1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-642. DDRSS_CTL_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CS_VAL_UPPER_1	R/W	0h	Upper bound address for chip select 1.
15-0	CS_VAL_LOWER_1	R/W	0h	Lower bound address for chip select 1.

4.2.271 DDRSS_CTL_272 Register (Offset = 440h) [reset = X]

DDRSS_CTL_272 is shown in [Figure 4-320](#) and described in [Table 4-644](#).

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Table 4-643. DDRSS_CTL_272 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0440h

Figure 4-320. DDRSS_CTL_272 Register

31	30	29	28	27	26	25	24
CS_MSK_0							
R/W-0h							
23	22	21	20	19	18	17	16
CS_MSK_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						CS_MAP_NON_POW2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED					ROW_START_VAL_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-644. DDRSS_CTL_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CS_MSK_0	R/W	0h	Mask applied to the address decode for chip select 0.
15-10	RESERVED	R/W	X	
9-8	CS_MAP_NON_POW2	R/W	0h	Defines which chip selects are non-power-of-2 memory sizes.
7-3	RESERVED	R/W	X	
2-0	ROW_START_VAL_1	R/W	0h	Row start value for chip select 1.

4.2.272 DDRSS_CTL_273 Register (Offset = 444h) [reset = X]

DDRSS_CTL_273 is shown in [Figure 4-321](#) and described in [Table 4-646](#).

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Table 4-645. DDRSS_CTL_273 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0444h

Figure 4-321. DDRSS_CTL_273 Register

31	30	29	28	27	26	25	24
RESERVED				RESERVED			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							CS_LOWER_A DDR_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
CS_MSK_1							
R/W-0h							
7	6	5	4	3	2	1	0
CS_MSK_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-646. DDRSS_CTL_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	CS_LOWER_ADDR_EN	R/W	0h	Enables moving the CS field to lower in the address map. When set to 1, the memory address map will be changed to ROW_CS_BANK. Please refer to the limitations before setting this bit.
15-0	CS_MSK_1	R/W	0h	Mask applied to the address decode for chip select 1.

4.2.273 DDRSS_CTL_274 Register (Offset = 448h) [reset = X]

DDRSS_CTL_274 is shown in [Figure 4-322](#) and described in [Table 4-648](#).

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Table 4-647. DDRSS_CTL_274 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0448h

Figure 4-322. DDRSS_CTL_274 Register

31	30	29	28	27	26	25	24
COMMAND_AGE_COUNT							
R/W-0h							
23	22	21	20	19	18	17	16
AGE_COUNT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				APREBIT			
R/W-X				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-648. DDRSS_CTL_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	COMMAND_AGE_COUNT	R/W	0h	Initial value of individual command aging counters for command aging.
23-16	AGE_COUNT	R/W	0h	Initial value of master aging-rate counter for command aging.
15-13	RESERVED	R/W	X	
12-8	APREBIT	R/W	Ah	Location of the auto pre-charge bit in the DRAM address.
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.2.274 DDRSS_CTL_275 Register (Offset = 44Ch) [reset = X]

DDRSS_CTL_275 is shown in [Figure 4-323](#) and described in [Table 4-650](#).

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Table 4-649. DDRSS_CTL_275 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 044Ch

Figure 4-323. DDRSS_CTL_275 Register

31	30	29	28	27	26	25	24
RESERVED							PLACEMENT_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							BANK_SPLIT_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							ADDR_COLLISION_MPM_DIS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							ADDR_CMP_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-650. DDRSS_CTL_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PLACEMENT_EN	R/W	0h	Enable placement logic for command queue. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	BANK_SPLIT_EN	R/W	0h	Enable bank splitting as a rule for command queue placement. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	ADDR_COLLISION_MPM_DIS	R/W	0h	Disable address collision detection extension using micro page mask for command queue placement and selection. Set to 1 to disable.
7-1	RESERVED	R/W	X	
0	ADDR_CMP_EN	R/W	0h	Enable address collision detection as a rule for command queue placement. Set to 1 to enable.

4.2.275 DDRSS_CTL_276 Register (Offset = 450h) [reset = X]

DDRSS_CTL_276 is shown in [Figure 4-324](#) and described in [Table 4-652](#).

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Table 4-651. DDRSS_CTL_276 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0450h

Figure 4-324. DDRSS_CTL_276 Register

31	30	29	28	27	26	25	24
RESERVED							CS_SAME_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RW_SAME_PAGE_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RW_SAME_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PRIORITY_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-652. DDRSS_CTL_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	CS_SAME_EN	R/W	0h	Enable chip select grouping when read/write grouping as a rule for command queue placement. This is only valid when the RW_SAME_EN parameter is set. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	RW_SAME_PAGE_EN	R/W	0h	Enable page grouping when read/write grouping as a rule for command queue placement. This is only valid when the RW_SAME_EN parameter is set. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	RW_SAME_EN	R/W	0h	Enable read/write grouping as a rule for command queue placement. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	PRIORITY_EN	R/W	0h	Enable priority as a rule for command queue placement. Set to 1 to enable.

4.2.276 DDRSS_CTL_277 Register (Offset = 454h) [reset = X]

DDRSS_CTL_277 is shown in [Figure 4-325](#) and described in [Table 4-654](#).

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Table 4-653. DDRSS_CTL_277 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0454h

Figure 4-325. DDRSS_CTL_277 Register

31	30	29	28	27	26	25	24
RESERVED							SWAP_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED			NUM_Q_ENTRIES_ACT_DISABLE				
R/W-X			R/W-0h				
15	14	13	12	11	10	9	8
RESERVED						DISABLE_RW_GROUP_W_BNK_CONFLICT	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							W2R_SPLIT_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-654. DDRSS_CTL_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SWAP_EN	R/W	0h	Enable command swapping logic in execution unit. Set to 1 to enable. If inline ECC is enabled (if the ECC_ENABLE parameter is programmed to 1, 2 or 3), the SWAP_EN parameter must be cleared to 0 because these two features are not supported together.
23-21	RESERVED	R/W	X	
20-16	NUM_Q_ENTRIES_ACT_DISABLE	R/W	0h	Number of queue entries in which ACT requests will be disabled. Programming to X will disable ACT requests from the X entries lowest in the command queue.
15-10	RESERVED	R/W	X	
9-8	DISABLE_RW_GROUP_W_BNK_CONFLICT	R/W	0h	Disables placement to read/write group when grouping creates a bank collision. Bit (0) controls placement next to bank conflict command and bit (1) controls placement 2 away from bank conflict command. Set each bit to 1 to disable.
7-1	RESERVED	R/W	X	
0	W2R_SPLIT_EN	R/W	0h	Enable splitting of commands to the same chip select from a write to a read command as a rule for command queue placement.

4.2.277 DDRSS_CTL_278 Register (Offset = 458h) [reset = X]

DDRSS_CTL_278 is shown in [Figure 4-326](#) and described in [Table 4-656](#).

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Table 4-655. DDRSS_CTL_278 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0458h

Figure 4-326. DDRSS_CTL_278 Register

31	30	29	28	27	26	25	24
RESERVED							REDUC
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							CS_MAP
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							INHIBIT_DRAM_CMD
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							DISABLE_RD_INTERLEAVE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-656. DDRSS_CTL_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	REDUC	R/W	0h	Enable the half datapath feature of the controller. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	CS_MAP	R/W	0h	Defines which chip selects are active.
15-10	RESERVED	R/W	X	
9-8	INHIBIT_DRAM_CMD	R/W	0h	Inhibit command types from being executed from the command queue. Clear to 0 to enable any command, program to 1 to inhibit read/write and bank commands, program to 2 to inhibit MRR and peripheral MRR commands, or program to 3 to inhibit MRR and read/write commands.
7-1	RESERVED	R/W	X	
0	DISABLE_RD_INTERLEAVE	R/W	0h	Disable read data interleaving for commands from the same port, regardless of the requestor ID. If inline ECC is enabled (if the ECC_ENABLE parameter is programmed to either of 1, 2 or 3), the DISABLE_RD_INTERLEAVE parameter must be cleared to 0 because these two features are not supported together.

4.2.278 DDRSS_CTL_279 Register (Offset = 45Ch) [reset = X]

DDRSS_CTL_279 is shown in [Figure 4-327](#) and described in [Table 4-658](#).

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Table 4-657. DDRSS_CTL_279 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 045Ch

Figure 4-327. DDRSS_CTL_279 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														FAULT_FIFO_PROTECTION_EN	
R/W-X														R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_FIFO_PROTECTION_EN															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-658. DDRSS_CTL_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	FAULT_FIFO_PROTECTION_EN	R/W	0h	Enables fault fifo protection features. Set to 1 to enable.

4.2.279 DDRSS_CTL_280 Register (Offset = 460h) [reset = X]

DDRSS_CTL_280 is shown in [Figure 4-328](#) and described in [Table 4-660](#).

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Table 4-659. DDRSS_CTL_280 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0460h

Figure 4-328. DDRSS_CTL_280 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														FAULT_FIFO_PROTECTION_STATUS	
R-X														R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAULT_FIFO_PROTECTION_STATUS															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-660. DDRSS_CTL_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	FAULT_FIFO_PROTECTION_STATUS	R	0h	Status of fault fifo protection modules. Value of 1 indicates an error occurred. READ ONLY

4.2.280 DDRSS_CTL_281 Register (Offset = 464h) [reset = X]

DDRSS_CTL_281 is shown in [Figure 4-329](#) and described in [Table 4-662](#).

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Table 4-661. DDRSS_CTL_281 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0464h

Figure 4-329. DDRSS_CTL_281 Register

31	30	29	28	27	26	25	24
RESERVED							WRITE_ADDR_CHAN_PARITY_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						FAULT_FIFO_PROTECTION_INJECTION_EN	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
FAULT_FIFO_PROTECTION_INJECTION_EN							
R/W-0h							
7	6	5	4	3	2	1	0
FAULT_FIFO_PROTECTION_INJECTION_EN							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-662. DDRSS_CTL_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	WRITE_ADDR_CHAN_PARITY_EN	R/W	0h	Enables parity checking on the AXI write command (address) channel. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-0	FAULT_FIFO_PROTECTION_INJECTION_EN	R/W	0h	Triggers error injection for fault fifo protection modules. Set to 1 to trigger.

4.2.281 DDRSS_CTL_282 Register (Offset = 468h) [reset = X]

DDRSS_CTL_282 is shown in [Figure 4-330](#) and described in [Table 4-664](#).

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Table 4-663. DDRSS_CTL_282 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0468h

Figure 4-330. DDRSS_CTL_282 Register

31	30	29	28	27	26	25	24
RESERVED							READ_DATA_CHAN_PARITY_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							READ_ADDR_CHAN_PARITY_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							WRITE_RESP_CHAN_PARITY_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						WRITE_DATA_CHAN_PARITY_EN	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-664. DDRSS_CTL_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	READ_DATA_CHAN_PARITY_EN	R/W	0h	Enables parity checking on the AXI read data channel. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	READ_ADDR_CHAN_PARITY_EN	R/W	0h	Enables parity checking on the AXI read command (address) channel. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	WRITE_RESP_CHAN_PARITY_EN	R/W	0h	Enables parity checking on the AXI write response channel. Set to 1 to enable.
7-2	RESERVED	R/W	X	
1-0	WRITE_DATA_CHAN_PARITY_EN	R/W	0h	Enables parity checking on the AXI write data channel. Bit (0) controls the write data bus and bit (1) controls the write strobe and last signals. Set each bit to 1 to enable.

4.2.282 DDRSS_CTL_283 Register (Offset = 46Ch) [reset = X]

DDRSS_CTL_283 is shown in [Figure 4-331](#) and described in [Table 4-666](#).

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Table 4-665. DDRSS_CTL_283 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 046Ch

Figure 4-331. DDRSS_CTL_283 Register

31	30	29	28	27	26	25	24
RESERVED							READ_PARITY_ERR_RRESP_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							WRITE_PARITY_ERR_BRESP_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-666. DDRSS_CTL_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	READ_PARITY_ERR_RRESP_EN	R/W	0h	Enables AXI ERROR responses on the AXI read data channel for any parity errors that occurred on the read command (address) channel. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	WRITE_PARITY_ERR_BRESP_EN	R/W	0h	Enables AXI ERROR responses on the AXI write response channel for any parity errors that occurred on either the write command (address) or write data channels. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.2.283 DDRSS_CTL_284 Register (Offset = 470h) [reset = X]

DDRSS_CTL_284 is shown in [Figure 4-332](#) and described in [Table 4-668](#).

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Table 4-667. DDRSS_CTL_284 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0470h

Figure 4-332. DDRSS_CTL_284 Register

31	30	29	28	27	26	25	24
RESERVED							READ_ADDR_CHAN_TRIGGER_PARITY_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							WRITE_RESP_CHAN_CORRUPT_PARITY_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							WRITE_DATA_CHAN_TRIGGER_PARITY_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							WRITE_ADDR_CHAN_TRIGGER_PARITY_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-668. DDRSS_CTL_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	READ_ADDR_CHAN_TRIGGER_PARITY_EN	R/W	0h	Triggers a parity error on the AXI read command (address) channel. Set to 1 to introduce an error.
23-17	RESERVED	R/W	X	
16	WRITE_RESP_CHAN_CORRUPT_PARITY_EN	R/W	0h	Corrupts the parity on the AXI write response channel. Set to 1 to introduce an error.
15-9	RESERVED	R/W	X	
8	WRITE_DATA_CHAN_TRIGGER_PARITY_EN	R/W	0h	Triggers a parity error on the AXI write data channel. Set to 1 to introduce an error.
7-1	RESERVED	R/W	X	
0	WRITE_ADDR_CHAN_TRIGGER_PARITY_EN	R/W	0h	Triggers a parity error on the AXI write command (address) channel. Set to 1 to introduce an error.

4.2.284 DDRSS_CTL_285 Register (Offset = 474h) [reset = X]

DDRSS_CTL_285 is shown in [Figure 4-333](#) and described in [Table 4-670](#).

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Table 4-669. DDRSS_CTL_285 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0474h

Figure 4-333. DDRSS_CTL_285 Register

31	30	29	28	27	26	25	24
RESERVED							ENHANCED_PARITY_PROTECTION_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							WRITE_PARITY_ERROR_CORRUPT_ECC_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							ECC_AXI_ERROR_RESPONSE_INHIBIT
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							READ_DATA_CHANNEL_CORRUPT_PARITY_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-670. DDRSS_CTL_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	ENHANCED_PARITY_PROTECTION_EN	R/W	0h	Enable byte parity implementation on addr/data channels.
23-17	RESERVED	R/W	X	
16	WRITE_PARITY_ERROR_CORRUPT_ECC_EN	R/W	0h	Enables corruption of ECC code if an AXI parity error is detected. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	ECC_AXI_ERROR_RESPONSE_INHIBIT	R/W	0h	Inhibits AXI ERROR responses when an ECC error occurs on the AXI read data channel. Set to 1 to inhibit errors.
7-1	RESERVED	R/W	X	
0	READ_DATA_CHANNEL_CORRUPT_PARITY_EN	R/W	0h	Corrupts the parity on the AXI read data channel. Set to 1 to introduce an error.

4.2.285 DDRSS_CTL_286 Register (Offset = 478h) [reset = X]

DDRSS_CTL_286 is shown in [Figure 4-334](#) and described in [Table 4-672](#).

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Table 4-671. DDRSS_CTL_286 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0478h

Figure 4-334. DDRSS_CTL_286 Register

31	30	29	28	27	26	25	24
RESERVED				DEVICE2_BYTE0_CS0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				DEVICE1_BYTE0_CS0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				DEVICE0_BYTE0_CS0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED					MEMDATA_RATIO_0		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-672. DDRSS_CTL_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	DEVICE2_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 2 on chip 0. Used for MRRs to identify where data will be returned.
23-20	RESERVED	R/W	X	
19-16	DEVICE1_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 1 on chip 0. Used for MRRs to identify where data will be returned.
15-12	RESERVED	R/W	X	
11-8	DEVICE0_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 0 on chip 0. Used for MRRs to identify where data will be returned.
7-3	RESERVED	R/W	X	
2-0	MEMDATA_RATIO_0	R/W	0h	Defines the ratio of the DRAM device size on chip select 0 to the memory data width. Program with the log2 ratio of the memory data width to the device data width.

4.2.286 DDRSS_CTL_287 Register (Offset = 47Ch) [reset = X]

DDRSS_CTL_287 is shown in [Figure 4-335](#) and described in [Table 4-674](#).

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Table 4-673. DDRSS_CTL_287 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 047Ch

Figure 4-335. DDRSS_CTL_287 Register

31	30	29	28	27	26	25	24
RESERVED				DEVICE1_BYTE0_CS1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				DEVICE0_BYTE0_CS1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					MEMDATA_RATIO_1		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED				DEVICE3_BYTE0_CS0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-674. DDRSS_CTL_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	DEVICE1_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 1 on chip 1. Used for MRRs to identify where data will be returned.
23-20	RESERVED	R/W	X	
19-16	DEVICE0_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 0 on chip 1. Used for MRRs to identify where data will be returned.
15-11	RESERVED	R/W	X	
10-8	MEMDATA_RATIO_1	R/W	0h	Defines the ratio of the DRAM device size on chip select 1 to the memory data width. Program with the log2 ratio of the memory data width to the device data width.
7-4	RESERVED	R/W	X	
3-0	DEVICE3_BYTE0_CS0	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 3 on chip 0. Used for MRRs to identify where data will be returned.

4.2.287 DDRSS_CTL_288 Register (Offset = 480h) [reset = X]

DDRSS_CTL_288 is shown in [Figure 4-336](#) and described in [Table 4-676](#).

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Table 4-675. DDRSS_CTL_288 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0480h

Figure 4-336. DDRSS_CTL_288 Register

31	30	29	28	27	26	25	24
RESERVED							IN_ORDER_ACCEPT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				Q_FULLNESS			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				DEVICE3_BYTE0_CS1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				DEVICE2_BYTE0_CS1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-676. DDRSS_CTL_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	IN_ORDER_ACCEPT	R/W	0h	Forces the controller to accept commands in the order in which they are placed in the command queue. If inline ECC is enabled (if the ECC_ENABLE parameter is programmed to 1, 2 or 3), the IN_ORDER_ACCEPT parameter must be set to 1.
23-21	RESERVED	R/W	X	
20-16	Q_FULLNESS	R/W	0h	Quantity that determines command queue almost full assertion(q_almost_full). When set to 0 then q_almost_full will be set to 0 irrespective of number of entries in command queue.
15-12	RESERVED	R/W	X	
11-8	DEVICE3_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 3 on chip 1. Used for MRRs to identify where data will be returned.
7-4	RESERVED	R/W	X	
3-0	DEVICE2_BYTE0_CS1	R/W	0h	Defines the byte location of byte0 in the memory datapath for device 2 on chip 1. Used for MRRs to identify where data will be returned.

4.2.288 DDRSS_CTL_289 Register (Offset = 484h) [reset = X]

DDRSS_CTL_289 is shown in [Figure 4-337](#) and described in [Table 4-678](#).

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Table 4-677. DDRSS_CTL_289 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0484h

Figure 4-337. DDRSS_CTL_289 Register

31	30	29	28	27	26	25	24
RESERVED							CTRLUPD_REQ_PER_AREF_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							CTRLUPD_REQ
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							CONTROLLER_BUSY
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED						WR_ORDER_REQ	
R/W-X						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-678. DDRSS_CTL_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	CTRLUPD_REQ_PER_AREF_EN	R/W	0h	Enable an automatic controller-initiated update (dfi_ctrlupd_req) after every refresh. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	CTRLUPD_REQ	W	0h	Assert the DFI controller-initiated update request signal dfi_ctrlupd_req. Set to 1 to trigger. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	CONTROLLER_BUSY	R	0h	Indicator that the controller is processing a command. Evaluates all ports for outstanding transactions. Value of 1 indicates controller busy. READ-ONLY
7-2	RESERVED	R/W	X	
1-0	WR_ORDER_REQ	R/W	0h	Determines if the controller can re-order write commands from the same source ID and/or the same port. Bit (0) controls source ID usage and bit (1) controls port ID usage. Set each bit to 1 to enable usage in placement logic.

4.2.289 DDRSS_CTL_290 Register (Offset = 488h) [reset = X]

DDRSS_CTL_290 is shown in [Figure 4-338](#) and described in [Table 4-680](#).

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Table 4-679. DDRSS_CTL_290 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0488h

Figure 4-338. DDRSS_CTL_290 Register

31	30	29	28	27	26	25	24
RESERVED						PREAMBLE_SUPPORT_F2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PREAMBLE_SUPPORT_F1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PREAMBLE_SUPPORT_F0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						CTRLUPD_AREF_HP_ENABLE	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-680. DDRSS_CTL_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PREAMBLE_SUPPORT_F2	R/W	0h	Selection of one or two cycle preamble for read and write burst transfers for frequency copy 2.
23-18	RESERVED	R/W	X	
17-16	PREAMBLE_SUPPORT_F1	R/W	0h	Selection of one or two cycle preamble for read and write burst transfers for frequency copy 1.
15-10	RESERVED	R/W	X	
9-8	PREAMBLE_SUPPORT_F0	R/W	0h	Selection of one or two cycle preamble for read and write burst transfers for frequency copy 0.
7-1	RESERVED	R/W	X	
0	CTRLUPD_AREF_HP_ENABLE	R/W	0h	Enable an automatic controller-initiated update (dfi_ctrlupd_req) after every high priority refresh when executing as a subtask request. Set to 1 to enable.

4.2.290 DDRSS_CTL_291 Register (Offset = 48Ch) [reset = X]

DDRSS_CTL_291 is shown in [Figure 4-339](#) and described in [Table 4-682](#).

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Table 4-681. DDRSS_CTL_291 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 048Ch

Figure 4-339. DDRSS_CTL_291 Register

31	30	29	28	27	26	25	24
RESERVED				DFI_ERROR			
R/W-X				R-0h			
23	22	21	20	19	18	17	16
RESERVED							RD_DBI_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							WR_DBI_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RD_PREAMBL E_TRAINING_E N
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-682. DDRSS_CTL_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	DFI_ERROR	R	0h	Indicates that the DFI error flag has been asserted. READ-ONLY
23-17	RESERVED	R/W	X	
16	RD_DBI_EN	R/W	0h	Enables controller support of DRAM DBI feature for read data with DDR4 devices. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	WR_DBI_EN	R/W	0h	Enables controller support of DRAM DBI feature for write data with DDR4 devices. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	RD_PREAMBLE_TRAINING_EN	R/W	0h	Enable read preamble training during gate training. Set to 1 to enable.

4.2.291 DDRSS_CTL_292 Register (Offset = 490h) [reset = X]

DDRSS_CTL_292 is shown in [Figure 4-340](#) and described in [Table 4-684](#).

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Table 4-683. DDRSS_CTL_292 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0490h

Figure 4-340. DDRSS_CTL_292 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED				DFI_ERROR_INFO			
R/W-X				R-0h			
15	14	13	12	11	10	9	8
DFI_ERROR_INFO							
R-0h							
7	6	5	4	3	2	1	0
DFI_ERROR_INFO							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-684. DDRSS_CTL_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	W	0h	Reserved
23-20	RESERVED	R/W	X	
19-0	DFI_ERROR_INFO	R	0h	Holds the encoded DFI error type associated with the DFI_ERROR parameter assertion. READ-ONLY

4.2.292 DDRSS_CTL_293 Register (Offset = 494h) [reset = 0h]

DDRSS_CTL_293 is shown in [Figure 4-341](#) and described in [Table 4-686](#).

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Table 4-685. DDRSS_CTL_293 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0494h

Figure 4-341. DDRSS_CTL_293 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_STATUS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-686. DDRSS_CTL_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INT_STATUS_0	R	0h	Status of interrupt features in the controller. READ-ONLY

4.2.293 DDRSS_CTL_294 Register (Offset = 498h) [reset = X]

DDRSS_CTL_294 is shown in [Figure 4-342](#) and described in [Table 4-688](#).

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Table 4-687. DDRSS_CTL_294 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0498h

Figure 4-342. DDRSS_CTL_294 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			INT_STATUS_1												
R-X																			R-0h												

LEGEND: R = Read Only; -n = value after reset

Table 4-688. DDRSS_CTL_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	X	
12-0	INT_STATUS_1	R	0h	Status of interrupt features in the controller. READ-ONLY

4.2.294 DDRSS_CTL_295 Register (Offset = 49Ch) [reset = 0h]

DDRSS_CTL_295 is shown in [Figure 4-343](#) and described in [Table 4-690](#).

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Table 4-689. DDRSS_CTL_295 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 049Ch

Figure 4-343. DDRSS_CTL_295 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_ACK_0																															
W-0h																															

LEGEND: W = Write Only; -n = value after reset

Table 4-690. DDRSS_CTL_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INT_ACK_0	W	0h	Clear mask of the INT_STATUS parameter. WRITE-ONLY

4.2.295 DDRSS_CTL_296 Register (Offset = 4A0h) [reset = X]

DDRSS_CTL_296 is shown in [Figure 4-344](#) and described in [Table 4-692](#).

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Table 4-691. DDRSS_CTL_296 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04A0h

Figure 4-344. DDRSS_CTL_296 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RESERVED																				INT_ACK_1															
W-X																				W-0h															

LEGEND: W = Write Only; -n = value after reset

Table 4-692. DDRSS_CTL_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	W	X	
11-0	INT_ACK_1	W	0h	Clear mask of the INT_STATUS parameter. WRITE-ONLY

4.2.296 DDRSS_CTL_297 Register (Offset = 4A4h) [reset = 0h]

DDRSS_CTL_297 is shown in [Figure 4-345](#) and described in [Table 4-694](#).

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Table 4-693. DDRSS_CTL_297 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04A4h

Figure 4-345. DDRSS_CTL_297 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_MASK_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-694. DDRSS_CTL_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	INT_MASK_0	R/W	0h	Mask for the controller_int signal from the INT_STATUS parameter.

4.2.297 DDRSS_CTL_298 Register (Offset = 4A8h) [reset = X]

DDRSS_CTL_298 is shown in [Figure 4-346](#) and described in [Table 4-696](#).

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Table 4-695. DDRSS_CTL_298 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04A8h

Figure 4-346. DDRSS_CTL_298 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																INT_MASK_1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-696. DDRSS_CTL_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12-0	INT_MASK_1	R/W	0h	Mask for the controller_int signal from the INT_STATUS parameter.

4.2.298 DDRSS_CTL_299 Register (Offset = 4ACh) [reset = 0h]

DDRSS_CTL_299 is shown in [Figure 4-347](#) and described in [Table 4-698](#).

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Table 4-697. DDRSS_CTL_299 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04ACh

Figure 4-347. DDRSS_CTL_299 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT_OF_RANGE_ADDR_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-698. DDRSS_CTL_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	OUT_OF_RANGE_ADDR_0	R	0h	Address of command that caused an out-of-range interrupt. READ-ONLY

4.2.299 DDRSS_CTL_300 Register (Offset = 4B0h) [reset = X]

DDRSS_CTL_300 is shown in [Figure 4-348](#) and described in [Table 4-700](#).

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Table 4-699. DDRSS_CTL_300 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04B0h

Figure 4-348. DDRSS_CTL_300 Register

31	30	29	28	27	26	25	24
RESERVED	OUT_OF_RANGE_TYPE						
R-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED				OUT_OF_RANGE_LENGTH			
R-X				R-0h			
15	14	13	12	11	10	9	8
OUT_OF_RANGE_LENGTH							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					OUT_OF_RANGE_ADDR_1		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 4-700. DDRSS_CTL_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	X	
30-24	OUT_OF_RANGE_TYPE	R	0h	Type of command that caused an out-of-range interrupt. READ-ONLY
23-20	RESERVED	R	X	
19-8	OUT_OF_RANGE_LENGTH	R	0h	Length of command that caused an out-of-range interrupt. READ-ONLY
7-3	RESERVED	R	X	
2-0	OUT_OF_RANGE_ADDR_1	R	0h	Address of command that caused an out-of-range interrupt. READ-ONLY

4.2.300 DDRSS_CTL_301 Register (Offset = 4B4h) [reset = X]

DDRSS_CTL_301 is shown in [Figure 4-349](#) and described in [Table 4-702](#).

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Table 4-701. DDRSS_CTL_301 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04B4h

Figure 4-349. DDRSS_CTL_301 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED		OUT_OF_RANGE_SOURCE_ID					
R-X		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-702. DDRSS_CTL_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	X	
5-0	OUT_OF_RANGE_SOURCE_ID	R	0h	Source ID of command that caused an out-of-range interrupt. READ-ONLY

4.2.301 DDRSS_CTL_302 Register (Offset = 4B8h) [reset = 0h]

DDRSS_CTL_302 is shown in [Figure 4-350](#) and described in [Table 4-704](#).

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Table 4-703. DDRSS_CTL_302 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04B8h

Figure 4-350. DDRSS_CTL_302 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_EXP_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-704. DDRSS_CTL_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_EXP_DATA_0	R	0h	Expected data on BIST error. READ-ONLY

4.2.302 DDRSS_CTL_303 Register (Offset = 4BCh) [reset = 0h]

DDRSS_CTL_303 is shown in [Figure 4-351](#) and described in [Table 4-706](#).

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Table 4-705. DDRSS_CTL_303 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04BCh

Figure 4-351. DDRSS_CTL_303 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_EXP_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-706. DDRSS_CTL_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_EXP_DATA_1	R	0h	Expected data on BIST error. READ-ONLY

4.2.303 DDRSS_CTL_304 Register (Offset = 4C0h) [reset = 0h]

DDRSS_CTL_304 is shown in [Figure 4-352](#) and described in [Table 4-708](#).

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Table 4-707. DDRSS_CTL_304 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04C0h

Figure 4-352. DDRSS_CTL_304 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_EXP_DATA_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-708. DDRSS_CTL_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_EXP_DATA_2	R	0h	Expected data on BIST error. READ-ONLY

4.2.304 DDRSS_CTL_305 Register (Offset = 4C4h) [reset = 0h]

DDRSS_CTL_305 is shown in [Figure 4-353](#) and described in [Table 4-710](#).

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Table 4-709. DDRSS_CTL_305 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04C4h

Figure 4-353. DDRSS_CTL_305 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_EXP_DATA_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-710. DDRSS_CTL_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_EXP_DATA_3	R	0h	Expected data on BIST error. READ-ONLY

4.2.305 DDRSS_CTL_306 Register (Offset = 4C8h) [reset = 0h]

DDRSS_CTL_306 is shown in [Figure 4-354](#) and described in [Table 4-712](#).

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Table 4-711. DDRSS_CTL_306 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04C8h

Figure 4-354. DDRSS_CTL_306 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_FAIL_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-712. DDRSS_CTL_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_FAIL_DATA_0	R	0h	Actual data on BIST error. READ-ONLY

4.2.306 DDRSS_CTL_307 Register (Offset = 4CCh) [reset = 0h]

DDRSS_CTL_307 is shown in [Figure 4-355](#) and described in [Table 4-714](#).

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Table 4-713. DDRSS_CTL_307 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04CCh

Figure 4-355. DDRSS_CTL_307 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_FAIL_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-714. DDRSS_CTL_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_FAIL_DATA_1	R	0h	Actual data on BIST error. READ-ONLY

4.2.307 DDRSS_CTL_308 Register (Offset = 4D0h) [reset = 0h]

DDRSS_CTL_308 is shown in [Figure 4-356](#) and described in [Table 4-716](#).

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Table 4-715. DDRSS_CTL_308 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04D0h

Figure 4-356. DDRSS_CTL_308 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_FAIL_DATA_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-716. DDRSS_CTL_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_FAIL_DATA_2	R	0h	Actual data on BIST error. READ-ONLY

4.2.308 DDRSS_CTL_309 Register (Offset = 4D4h) [reset = 0h]

DDRSS_CTL_309 is shown in [Figure 4-357](#) and described in [Table 4-718](#).

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Table 4-717. DDRSS_CTL_309 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04D4h

Figure 4-357. DDRSS_CTL_309 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_FAIL_DATA_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-718. DDRSS_CTL_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_FAIL_DATA_3	R	0h	Actual data on BIST error. READ-ONLY

4.2.309 DDRSS_CTL_310 Register (Offset = 4D8h) [reset = 0h]

DDRSS_CTL_310 is shown in [Figure 4-358](#) and described in [Table 4-720](#).

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Table 4-719. DDRSS_CTL_310 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04D8h

Figure 4-358. DDRSS_CTL_310 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIST_FAIL_ADDR_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-720. DDRSS_CTL_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BIST_FAIL_ADDR_0	R	0h	Address of BIST error. READ-ONLY

4.2.310 DDRSS_CTL_311 Register (Offset = 4DCh) [reset = X]

DDRSS_CTL_311 is shown in [Figure 4-359](#) and described in [Table 4-722](#).

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Table 4-721. DDRSS_CTL_311 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04DCh

Figure 4-359. DDRSS_CTL_311 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					BIST_FAIL_ADDR_1		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 4-722. DDRSS_CTL_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2-0	BIST_FAIL_ADDR_1	R	0h	Address of BIST error. READ-ONLY

4.2.311 DDRSS_CTL_312 Register (Offset = 4E0h) [reset = 0h]

DDRSS_CTL_312 is shown in [Figure 4-360](#) and described in [Table 4-724](#).

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Table 4-723. DDRSS_CTL_312 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04E0h

Figure 4-360. DDRSS_CTL_312 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_CMD_ERROR_ADDR_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-724. DDRSS_CTL_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PORT_CMD_ERROR_ADDR_0	R	0h	Address of command that caused the PORT command error. READ-ONLY

4.2.312 DDRSS_CTL_313 Register (Offset = 4E4h) [reset = X]

DDRSS_CTL_313 is shown in [Figure 4-361](#) and described in [Table 4-726](#).

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Table 4-725. DDRSS_CTL_313 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04E4h

Figure 4-361. DDRSS_CTL_313 Register

31	30	29	28	27	26	25	24
RESERVED						ODT_RD_MAP_CS0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PORT_CMD_ERROR_TYPE	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED		PORT_CMD_ERROR_ID					
R/W-X		R-0h					
7	6	5	4	3	2	1	0
RESERVED						PORT_CMD_ERROR_ADDR_1	
R/W-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-726. DDRSS_CTL_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	ODT_RD_MAP_CS0	R/W	0h	Determines which chip(s) will have termination when a read occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a read.
23-18	RESERVED	R/W	X	
17-16	PORT_CMD_ERROR_TYPE	R	0h	Type of error and access type that caused the PORT command error. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	PORT_CMD_ERROR_ID	R	0h	Source ID of command that caused the PORT command error. READ-ONLY
7-3	RESERVED	R/W	X	
2-0	PORT_CMD_ERROR_ADDR_1	R	0h	Address of command that caused the PORT command error. READ-ONLY

4.2.313 DDRSS_CTL_314 Register (Offset = 4E8h) [reset = X]

DDRSS_CTL_314 is shown in [Figure 4-362](#) and described in [Table 4-728](#).

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Table 4-727. DDRSS_CTL_314 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04E8h

Figure 4-362. DDRSS_CTL_314 Register

31	30	29	28	27	26	25	24
TODTL_2CMD_F0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						ODT_WR_MAP_CS1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						ODT_RD_MAP_CS1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						ODT_WR_MAP_CS0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-728. DDRSS_CTL_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TODTL_2CMD_F0	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command.
23-18	RESERVED	R/W	X	
17-16	ODT_WR_MAP_CS1	R/W	0h	Determines which chip(s) will have termination when a write occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a write.
15-10	RESERVED	R/W	X	
9-8	ODT_RD_MAP_CS1	R/W	0h	Determines which chip(s) will have termination when a read occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a read.
7-2	RESERVED	R/W	X	
1-0	ODT_WR_MAP_CS0	R/W	0h	Determines which chip(s) will have termination when a write occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a write.

4.2.314 DDRSS_CTL_315 Register (Offset = 4ECh) [reset = X]

DDRSS_CTL_315 is shown in [Figure 4-363](#) and described in [Table 4-730](#).

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Table 4-729. DDRSS_CTL_315 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04ECh

Figure 4-363. DDRSS_CTL_315 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TODTH_WR_F1				TODTL_2CMD_F1							
R/W-X				R/W-0h				R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				TODTH_RD_F0				RESERVED				TODTH_WR_F0			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-730. DDRSS_CTL_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TODTH_WR_F1	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command.
23-16	TODTL_2CMD_F1	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command.
15-12	RESERVED	R/W	X	
11-8	TODTH_RD_F0	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command.
7-4	RESERVED	R/W	X	
3-0	TODTH_WR_F0	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command.

4.2.315 DDRSS_CTL_316 Register (Offset = 4F0h) [reset = X]

DDRSS_CTL_316 is shown in [Figure 4-364](#) and described in [Table 4-732](#).

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Table 4-731. DDRSS_CTL_316 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04F0h

Figure 4-364. DDRSS_CTL_316 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				TODTH_RD_F2				RESERVED				TODTH_WR_F2			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TODTL_2CMD_F2								RESERVED				TODTH_RD_F1			
R/W-0h								R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-732. DDRSS_CTL_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TODTH_RD_F2	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command.
23-20	RESERVED	R/W	X	
19-16	TODTH_WR_F2	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a write command.
15-8	TODTL_2CMD_F2	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command.
7-4	RESERVED	R/W	X	
3-0	TODTH_RD_F1	R/W	0h	Defines the DRAM minimum ODT high time after an ODT assertion for a read command.

4.2.316 DDRSS_CTL_317 Register (Offset = 4F4h) [reset = X]

DDRSS_CTL_317 is shown in [Figure 4-365](#) and described in [Table 4-734](#).

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Table 4-733. DDRSS_CTL_317 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04F4h

Figure 4-365. DDRSS_CTL_317 Register

31	30	29	28	27	26	25	24
RESERVED							EN_ODT_ASSERT_EXCEPT_RD
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							ODT_EN_F2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							ODT_EN_F1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							ODT_EN_F0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-734. DDRSS_CTL_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	EN_ODT_ASSERT_EXCEPT_RD	R/W	0h	Enable controller to assert ODT at all times except during reads. Assumes single ODT pin connected. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	ODT_EN_F2	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed.
15-9	RESERVED	R/W	X	
8	ODT_EN_F1	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed.
7-1	RESERVED	R/W	X	
0	ODT_EN_F0	R/W	0h	Enable support of DRAM ODT. When enabled, controller will assert and de-assert ODT output to DRAM as needed.

4.2.317 DDRSS_CTL_318 Register (Offset = 4F8h) [reset = X]

DDRSS_CTL_318 is shown in [Figure 4-366](#) and described in [Table 4-736](#).

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Table 4-735. DDRSS_CTL_318 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04F8h

Figure 4-366. DDRSS_CTL_318 Register

31	30	29	28	27	26	25	24
RESERVED				RD_TO_ODTH_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				WR_TO_ODTH_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				WR_TO_ODTH_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				WR_TO_ODTH_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-736. DDRSS_CTL_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	RD_TO_ODTH_F0	R/W	0h	Defines the delay from a read command to ODT assertion.
23-22	RESERVED	R/W	X	
21-16	WR_TO_ODTH_F2	R/W	0h	Defines the delay from a write command to ODT assertion.
15-14	RESERVED	R/W	X	
13-8	WR_TO_ODTH_F1	R/W	0h	Defines the delay from a write command to ODT assertion.
7-6	RESERVED	R/W	X	
5-0	WR_TO_ODTH_F0	R/W	0h	Defines the delay from a write command to ODT assertion.

4.2.318 DDRSS_CTL_319 Register (Offset = 4FCh) [reset = X]

DDRSS_CTL_319 is shown in [Figure 4-367](#) and described in [Table 4-738](#).

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Table 4-737. DDRSS_CTL_319 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 04FCh

Figure 4-367. DDRSS_CTL_319 Register

31	30	29	28	27	26	25	24
RESERVED				RW2MRW_DLY_F1			
R/W-X				R/W-8h			
23	22	21	20	19	18	17	16
RESERVED				RW2MRW_DLY_F0			
R/W-X				R/W-8h			
15	14	13	12	11	10	9	8
RESERVED				RD_TO_ODTH_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				RD_TO_ODTH_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-738. DDRSS_CTL_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	RW2MRW_DLY_F1	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system.
23-21	RESERVED	R/W	X	
20-16	RW2MRW_DLY_F0	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system.
15-14	RESERVED	R/W	X	
13-8	RD_TO_ODTH_F2	R/W	0h	Defines the delay from a read command to ODT assertion.
7-6	RESERVED	R/W	X	
5-0	RD_TO_ODTH_F1	R/W	0h	Defines the delay from a read command to ODT assertion.

4.2.319 DDRSS_CTL_320 Register (Offset = 500h) [reset = X]

DDRSS_CTL_320 is shown in [Figure 4-368](#) and described in [Table 4-740](#).

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Table 4-739. DDRSS_CTL_320 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0500h

Figure 4-368. DDRSS_CTL_320 Register

31	30	29	28	27	26	25	24
RESERVED				W2R_DIFFCS_DLY_F0			
R/W-X				R/W-1h			
23	22	21	20	19	18	17	16
RESERVED				R2W_DIFFCS_DLY_F0			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED				R2R_DIFFCS_DLY_F0			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
RESERVED				RW2MRW_DLY_F2			
R/W-X				R/W-8h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-740. DDRSS_CTL_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	W2R_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system.
23-21	RESERVED	R/W	X	
20-16	R2W_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value.
15-13	RESERVED	R/W	X	
12-8	R2R_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between reads to different chip selects. Allowed programming dependent on memory system.
7-5	RESERVED	R/W	X	
4-0	RW2MRW_DLY_F2	R/W	8h	Additional delay to insert between read or write and mode_reg_write. Allowed programming dependent on memory system.

4.2.320 DDRSS_CTL_321 Register (Offset = 504h) [reset = X]

DDRSS_CTL_321 is shown in [Figure 4-369](#) and described in [Table 4-742](#).

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Table 4-741. DDRSS_CTL_321 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0504h

Figure 4-369. DDRSS_CTL_321 Register

31	30	29	28	27	26	25	24
RESERVED				W2R_DIFFCS_DLY_F1			
R/W-X				R/W-1h			
23	22	21	20	19	18	17	16
RESERVED				R2W_DIFFCS_DLY_F1			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED				R2R_DIFFCS_DLY_F1			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
RESERVED				W2W_DIFFCS_DLY_F0			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-742. DDRSS_CTL_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	W2R_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system.
23-21	RESERVED	R/W	X	
20-16	R2W_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value.
15-13	RESERVED	R/W	X	
12-8	R2R_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between reads to different chip selects. Allowed programming dependent on memory system.
7-5	RESERVED	R/W	X	
4-0	W2W_DIFFCS_DLY_F0	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value.

4.2.321 DDRSS_CTL_322 Register (Offset = 508h) [reset = X]

DDRSS_CTL_322 is shown in [Figure 4-370](#) and described in [Table 4-744](#).

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Table 4-743. DDRSS_CTL_322 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0508h

Figure 4-370. DDRSS_CTL_322 Register

31	30	29	28	27	26	25	24
RESERVED				W2R_DIFFCS_DLY_F2			
R/W-X				R/W-1h			
23	22	21	20	19	18	17	16
RESERVED				R2W_DIFFCS_DLY_F2			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED				R2R_DIFFCS_DLY_F2			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
RESERVED				W2W_DIFFCS_DLY_F1			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-744. DDRSS_CTL_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	W2R_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between writes and reads to different chip selects. Allowed programming dependent on memory system.
23-21	RESERVED	R/W	X	
20-16	R2W_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between reads and writes to different chip selects. Program to a non-zero value.
15-13	RESERVED	R/W	X	
12-8	R2R_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between reads to different chip selects. Allowed programming dependent on memory system.
7-5	RESERVED	R/W	X	
4-0	W2W_DIFFCS_DLY_F1	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value.

4.2.322 DDRSS_CTL_323 Register (Offset = 50Ch) [reset = X]

DDRSS_CTL_323 is shown in [Figure 4-371](#) and described in [Table 4-746](#).

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Table 4-745. DDRSS_CTL_323 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 050Ch

Figure 4-371. DDRSS_CTL_323 Register

31	30	29	28	27	26	25	24
RESERVED				R2W_SAMECS_DLY_F1			
R/W-X				R/W-2h			
23	22	21	20	19	18	17	16
RESERVED				R2W_SAMECS_DLY_F0			
R/W-X				R/W-2h			
15	14	13	12	11	10	9	8
RESERVED				R2R_SAMECS_DLY			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				W2W_DIFFCS_DLY_F2			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-746. DDRSS_CTL_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	R2W_SAMECS_DLY_F1	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value.
23-21	RESERVED	R/W	X	
20-16	R2W_SAMECS_DLY_F0	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value.
15-13	RESERVED	R/W	X	
12-8	R2R_SAMECS_DLY	R/W	0h	Additional delay to insert between two reads to the same chip select. Any value including 0 supported.
7-5	RESERVED	R/W	X	
4-0	W2W_DIFFCS_DLY_F2	R/W	1h	Additional delay to insert between writes to different chip selects. Program to a non-zero value.

4.2.323 DDRSS_CTL_324 Register (Offset = 510h) [reset = X]

DDRSS_CTL_324 is shown in [Figure 4-372](#) and described in [Table 4-748](#).

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Table 4-747. DDRSS_CTL_324 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0510h

Figure 4-372. DDRSS_CTL_324 Register

31	30	29	28	27	26	25	24
RESERVED				TDQSCK_MAX_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				W2W_SAMECS_DLY			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				W2R_SAMECS_DLY			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				R2W_SAMECS_DLY_F2			
R/W-X				R/W-2h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-748. DDRSS_CTL_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TDQSCK_MAX_F0	R/W	0h	Additional delay needed for tDQSCK.
23-21	RESERVED	R/W	X	
20-16	W2W_SAMECS_DLY	R/W	0h	Additional delay to insert between two writes to the same chip select. Any value including 0 supported.
15-13	RESERVED	R/W	X	
12-8	W2R_SAMECS_DLY	R/W	0h	Additional delay to insert between writes and reads to the same chip select.
7-5	RESERVED	R/W	X	
4-0	R2W_SAMECS_DLY_F2	R/W	2h	Additional delay to insert between reads and writes to the same chip select. Program to a non-zero value.

4.2.324 DDRSS_CTL_325 Register (Offset = 514h) [reset = X]

DDRSS_CTL_325 is shown in [Figure 4-373](#) and described in [Table 4-750](#).

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Table 4-749. DDRSS_CTL_325 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0514h

Figure 4-373. DDRSS_CTL_325 Register

31	30	29	28	27	26	25	24
RESERVED				TDQSCK_MAX_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				TDQSCK_MIN_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				TDQSCK_MAX_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				TDQSCK_MIN_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-750. DDRSS_CTL_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TDQSCK_MAX_F2	R/W	0h	Additional delay needed for tDQSCK.
23-19	RESERVED	R/W	X	
18-16	TDQSCK_MIN_F1	R/W	0h	Additional delay needed for tDQSCK.
15-12	RESERVED	R/W	X	
11-8	TDQSCK_MAX_F1	R/W	0h	Additional delay needed for tDQSCK.
7-3	RESERVED	R/W	X	
2-0	TDQSCK_MIN_F0	R/W	0h	Additional delay needed for tDQSCK.

4.2.325 DDRSS_CTL_326 Register (Offset = 518h) [reset = X]

DDRSS_CTL_326 is shown in [Figure 4-374](#) and described in [Table 4-752](#).

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Table 4-751. DDRSS_CTL_326 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0518h

Figure 4-374. DDRSS_CTL_326 Register

31	30	29	28	27	26	25	24
RESERVED							SWLVL_START
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							SWLVL_LOAD
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED					SW_LEVELING_MODE		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED					TDQSCK_MIN_F2		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-752. DDRSS_CTL_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SWLVL_START	W	0h	User request to initiate software leveling of type in the SW_LEVELING_MODE parameter. Set to 1 to trigger. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	SWLVL_LOAD	W	0h	User request to load delays and execute software leveling. Set to 1 to trigger. WRITE-ONLY
15-11	RESERVED	R/W	X	
10-8	SW_LEVELING_MODE	R/W	0h	Defines the leveling operation for software leveling. Clear to 0 for none, program to 1 for write leveling, program to 2 for data eye training, or program to 3 for gate training.
7-3	RESERVED	R/W	X	
2-0	TDQSCK_MIN_F2	R/W	0h	Additional delay needed for tDQSCK.

4.2.326 DDRSS_CTL_327 Register (Offset = 51Ch) [reset = X]

DDRSS_CTL_327 is shown in [Figure 4-375](#) and described in [Table 4-754](#).

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Table 4-753. DDRSS_CTL_327 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 051Ch

Figure 4-375. DDRSS_CTL_327 Register

31	30	29	28	27	26	25	24
RESERVED							SWLVL_RESP_1
R/W-X							R-0h
23	22	21	20	19	18	17	16
RESERVED							SWLVL_RESP_0
R/W-X							R-0h
15	14	13	12	11	10	9	8
RESERVED							SWLVL_OP_DONE
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED							SWLVL_EXIT
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-754. DDRSS_CTL_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SWLVL_RESP_1	R	0h	Leveling response for data slice 1. READ-ONLY
23-17	RESERVED	R/W	X	
16	SWLVL_RESP_0	R	0h	Leveling response for data slice 0. READ-ONLY
15-9	RESERVED	R/W	X	
8	SWLVL_OP_DONE	R	0h	Signals that software leveling is currently in progress. Value of 1 indicates operation complete. READ-ONLY
7-1	RESERVED	R/W	X	
0	SWLVL_EXIT	W	0h	User request to exit software leveling. Set to 1 to exit. WRITE-ONLY

4.2.327 DDRSS_CTL_328 Register (Offset = 520h) [reset = X]

DDRSS_CTL_328 is shown in [Figure 4-376](#) and described in [Table 4-756](#).

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Table 4-755. DDRSS_CTL_328 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0520h

Figure 4-376. DDRSS_CTL_328 Register

31	30	29	28	27	26	25	24
RESERVED							WRLVL_REQ
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							PHYUPD_APP END_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							SWLVL_RESP_3
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED							SWLVL_RESP_2
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-756. DDRSS_CTL_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	WRLVL_REQ	W	0h	User request to initiate write leveling. Set to 1 to trigger. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PHYUPD_APPEND_EN	R/W	0h	Specifies if a PHY update will be run prior to completing a training sequence. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	SWLVL_RESP_3	R	0h	Leveling response for data slice 3. READ-ONLY
7-1	RESERVED	R/W	X	
0	SWLVL_RESP_2	R	0h	Leveling response for data slice 2. READ-ONLY

4.2.328 DDRSS_CTL_329 Register (Offset = 524h) [reset = X]

DDRSS_CTL_329 is shown in [Figure 4-377](#) and described in [Table 4-758](#).

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Table 4-757. DDRSS_CTL_329 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0524h

Figure 4-377. DDRSS_CTL_329 Register

31	30	29	28	27	26	25	24
RESERVED							WRLVL_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		WLMRD					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		WLDQSEN					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							WRLVL_CS
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-758. DDRSS_CTL_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	WRLVL_EN	R/W	0h	Enable the MC write leveling module. Set to 1 to enable.
23-22	RESERVED	R/W	X	
21-16	WLMRD	R/W	0h	Delay from issuing MRS to first write leveling strobe.
15-14	RESERVED	R/W	X	
13-8	WLDQSEN	R/W	0h	Delay from issuing MRS to first DQS strobe for write leveling.
7-1	RESERVED	R/W	X	
0	WRLVL_CS	R/W	0h	Specifies the target chip select for the write leveling operation initiated through the WRLVL_REQ parameter.

4.2.329 DDRSS_CTL_330 Register (Offset = 528h) [reset = X]

DDRSS_CTL_330 is shown in [Figure 4-378](#) and described in [Table 4-760](#).

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Table 4-759. DDRSS_CTL_330 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0528h

Figure 4-378. DDRSS_CTL_330 Register

31	30	29	28	27	26	25	24
RESERVED				WRLVL_RESP_MASK			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							WRLVL_ON_SREF_EXIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							WRLVL_PERIODIC
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							DFI_PHY_WRLVL_MODE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-760. DDRSS_CTL_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	WRLVL_RESP_MASK	R/W	0h	Mask for the dfi_wrlvl_resp signal during write leveling.
23-17	RESERVED	R/W	X	
16	WRLVL_ON_SREF_EXIT	R/W	0h	Enables automatic write leveling on a self-refresh exit. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	WRLVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during write leveling. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	DFI_PHY_WRLVL_MODE	R/W	0h	Specifies the PHY support for DFI write leveling. Set to 1 for supported.

4.2.330 DDRSS_CTL_331 Register (Offset = 52Ch) [reset = X]

DDRSS_CTL_331 is shown in [Figure 4-379](#) and described in [Table 4-762](#).

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Table 4-761. DDRSS_CTL_331 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 052Ch

Figure 4-379. DDRSS_CTL_331 Register

31	30	29	28	27	26	25	24
RESERVED					WRLVL_ERROR_STATUS		
R/W-X					R-0h		
23	22	21	20	19	18	17	16
RESERVED					WRLVL_CS_MAP		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						WRLVL_ROTATE	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						WRLVL_AREF_EN	
R/W-X						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-762. DDRSS_CTL_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	WRLVL_ERROR_STATUS	R	0h	Holds the error associated with the write level error interrupt. Bit (0) set indicates a TDFI_WRLVL_MAX parameter violation, bit (1) set indicates a TDFI_WRLVL_RESP parameter violation, bit (2) set indicates that a write leveling operation was attempted while memory was in self-refresh mode or self-refresh power-down mode. READ-ONLY
23-18	RESERVED	R/W	X	
17-16	WRLVL_CS_MAP	R/W	0h	Defines the chip select map for write leveling operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for write leveling.
15-9	RESERVED	R/W	X	
8	WRLVL_ROTATE	R/W	0h	Enables rotational CS for interval write leveling. Set to 1 for rotating CS.
7-1	RESERVED	R/W	X	
0	WRLVL_AREF_EN	R/W	0h	Enables refreshes and other non-data commands to execute in the middle of write leveling. Set to 1 to enable.

4.2.331 DDRSS_CTL_332 Register (Offset = 530h) [reset = 0h]

DDRSS_CTL_332 is shown in [Figure 4-380](#) and described in [Table 4-764](#).

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Table 4-763. DDRSS_CTL_332 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0530h

Figure 4-380. DDRSS_CTL_332 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_HIGH_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_NORM_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-764. DDRSS_CTL_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_HIGH_THRESHOLD_F0	R/W	0h	Write leveling high threshold number of long counts until the high priority request is asserted.
15-0	WRLVL_NORM_THRESHOLD_F0	R/W	0h	Write leveling normal threshold number of long counts until the normal priority request is asserted.

4.2.332 DDRSS_CTL_333 Register (Offset = 534h) [reset = 0h]

DDRSS_CTL_333 is shown in [Figure 4-381](#) and described in [Table 4-766](#).

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Table 4-765. DDRSS_CTL_333 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0534h

Figure 4-381. DDRSS_CTL_333 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_SW_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_TIMEOUT_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-766. DDRSS_CTL_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_SW_PROMOTE_THRESHOLD_F0	R/W	0h	Write leveling promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	WRLVL_TIMEOUT_F0	R/W	0h	Write leveling timeout number of long counts until the timeout is asserted.

4.2.333 DDRSS_CTL_334 Register (Offset = 538h) [reset = 0h]

DDRSS_CTL_334 is shown in [Figure 4-382](#) and described in [Table 4-768](#).

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Table 4-767. DDRSS_CTL_334 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0538h

Figure 4-382. DDRSS_CTL_334 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_NORM_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_DFI_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-768. DDRSS_CTL_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_NORM_THRESH OLD_F1	R/W	0h	Write leveling normal threshold number of long counts until the normal priority request is asserted.
15-0	WRLVL_DFI_PROMOTE_ THRESHOLD_F0	R/W	0h	Write leveling promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.334 DDRSS_CTL_335 Register (Offset = 53Ch) [reset = 0h]

DDRSS_CTL_335 is shown in [Figure 4-383](#) and described in [Table 4-770](#).

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Table 4-769. DDRSS_CTL_335 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 053Ch

Figure 4-383. DDRSS_CTL_335 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_TIMEOUT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_HIGH_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-770. DDRSS_CTL_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_TIMEOUT_F1	R/W	0h	Write leveling timeout number of long counts until the timeout is asserted.
15-0	WRLVL_HIGH_THRESHOLD_F1	R/W	0h	Write leveling high threshold number of long counts until the high priority request is asserted.

4.2.335 DDRSS_CTL_336 Register (Offset = 540h) [reset = 0h]

DDRSS_CTL_336 is shown in [Figure 4-384](#) and described in [Table 4-772](#).

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Table 4-771. DDRSS_CTL_336 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0540h

Figure 4-384. DDRSS_CTL_336 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_DFI_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_SW_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-772. DDRSS_CTL_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	Write leveling promotion number of long counts until the high priority request is asserted. Applies to DFI commands.
15-0	WRLVL_SW_PROMOTE_THRESHOLD_F1	R/W	0h	Write leveling promotion number of long counts until the high priority request is asserted. Applies to SW commands.

4.2.336 DDRSS_CTL_337 Register (Offset = 544h) [reset = 0h]

DDRSS_CTL_337 is shown in [Figure 4-385](#) and described in [Table 4-774](#).

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Table 4-773. DDRSS_CTL_337 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0544h

Figure 4-385. DDRSS_CTL_337 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_HIGH_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_NORM_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-774. DDRSS_CTL_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_HIGH_THRESHOLD_F2	R/W	0h	Write leveling high threshold number of long counts until the high priority request is asserted.
15-0	WRLVL_NORM_THRESHOLD_F2	R/W	0h	Write leveling normal threshold number of long counts until the normal priority request is asserted.

4.2.337 DDRSS_CTL_338 Register (Offset = 548h) [reset = 0h]

DDRSS_CTL_338 is shown in [Figure 4-386](#) and described in [Table 4-776](#).

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Table 4-775. DDRSS_CTL_338 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0548h

Figure 4-386. DDRSS_CTL_338 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRLVL_SW_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRLVL_TIMEOUT_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-776. DDRSS_CTL_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	WRLVL_SW_PROMOTE_THRESHOLD_F2	R/W	0h	Write leveling promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	WRLVL_TIMEOUT_F2	R/W	0h	Write leveling timeout number of long counts until the timeout is asserted.

4.2.338 DDRSS_CTL_339 Register (Offset = 54Ch) [reset = X]

DDRSS_CTL_339 is shown in [Figure 4-387](#) and described in [Table 4-778](#).

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Table 4-777. DDRSS_CTL_339 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 054Ch

Figure 4-387. DDRSS_CTL_339 Register

31	30	29	28	27	26	25	24
RESERVED							RDLVL_GATE_REQ
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							RDLVL_REQ
R/W-X							W-0h
15	14	13	12	11	10	9	8
WRLVL_DFI_PROMOTE_THRESHOLD_F2							
R/W-0h							
7	6	5	4	3	2	1	0
WRLVL_DFI_PROMOTE_THRESHOLD_F2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-778. DDRSS_CTL_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RDLVL_GATE_REQ	W	0h	User request to initiate gate training. Set to 1 to trigger. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	RDLVL_REQ	W	0h	User request to initiate data eye training. Set to 1 to trigger. WRITE-ONLY
15-0	WRLVL_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	Write leveling promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.339 DDRSS_CTL_340 Register (Offset = 550h) [reset = X]

DDRSS_CTL_340 is shown in [Figure 4-388](#) and described in [Table 4-780](#).

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Table 4-779. DDRSS_CTL_340 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0550h

Figure 4-388. DDRSS_CTL_340 Register

31	30	29	28	27	26	25	24
RESERVED							DFI_PHY_RDLVL_MODE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				RDLVL_GATE_SEQ_EN			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				RDLVL_SEQ_EN			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							RDLVL_CS
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-780. DDRSS_CTL_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	DFI_PHY_RDLVL_MODE	R/W	0h	Specifies the PHY support for DFI data eye training. Set to 1 for supported.
23-20	RESERVED	R/W	X	
19-16	RDLVL_GATE_SEQ_EN	R/W	0h	Specifies the pattern, format and MPR for gate training.
15-12	RESERVED	R/W	X	
11-8	RDLVL_SEQ_EN	R/W	0h	Specifies the pattern, format and MPR for data eye training.
7-1	RESERVED	R/W	X	
0	RDLVL_CS	R/W	0h	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ parameter or the gate training operation initiated through the RDLVL_GATE_REQ parameter.

4.2.340 DDRSS_CTL_341 Register (Offset = 554h) [reset = X]

DDRSS_CTL_341 is shown in [Figure 4-389](#) and described in [Table 4-782](#).

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Table 4-781. DDRSS_CTL_341 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0554h

Figure 4-389. DDRSS_CTL_341 Register

31	30	29	28	27	26	25	24
RESERVED							RDLVL_GATE_PERIODIC
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RDLVL_ON_SREF_EXIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RDLVL_PERIODIC
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							DFI_PHY_RDLVL_GATE_MODE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-782. DDRSS_CTL_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RDLVL_GATE_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during gate training. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	RDLVL_ON_SREF_EXIT	R/W	0h	Enables automatic data eye training on a self-refresh exit. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	RDLVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during data eye training. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	DFI_PHY_RDLVL_GATE_MODE	R/W	0h	Specifies the PHY support for DFI gate training. Set to 1 for supported.

4.2.341 DDRSS_CTL_342 Register (Offset = 558h) [reset = X]

DDRSS_CTL_342 is shown in [Figure 4-390](#) and described in [Table 4-784](#).

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Table 4-783. DDRSS_CTL_342 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0558h

Figure 4-390. DDRSS_CTL_342 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RDLVL_GATE_AREF_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RDLVL_AREF_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RDLVL_GATE_ON_SREF_EXIT
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-784. DDRSS_CTL_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	RDLVL_GATE_AREF_EN	R/W	0h	Enables refreshes and other non-data commands to execute in the middle of gate training. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	RDLVL_AREF_EN	R/W	0h	Enables refreshes and other non-data commands to execute in the middle of data eye training. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	RDLVL_GATE_ON_SREF_EXIT	R/W	0h	Enables automatic gate training on a self-refresh exit. Set to 1 to enable.

4.2.342 DDRSS_CTL_343 Register (Offset = 55Ch) [reset = X]

DDRSS_CTL_343 is shown in [Figure 4-391](#) and described in [Table 4-786](#).

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Table 4-785. DDRSS_CTL_343 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 055Ch

Figure 4-391. DDRSS_CTL_343 Register

31	30	29	28	27	26	25	24
RESERVED						RDLVL_GATE_CS_MAP	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						RDLVL_CS_MAP	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						RDLVL_GATE_ROTATE	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						RDLVL_ROTATE	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-786. DDRSS_CTL_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	RDLVL_GATE_CS_MAP	R/W	0h	Defines the chip select map for gate training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for gate training.
23-18	RESERVED	R/W	X	
17-16	RDLVL_CS_MAP	R/W	0h	Defines the chip select map for data eye training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for data eye training.
15-9	RESERVED	R/W	X	
8	RDLVL_GATE_ROTATE	R/W	0h	Enables rotational CS for interval gate training. Set to 1 for rotating CS.
7-1	RESERVED	R/W	X	
0	RDLVL_ROTATE	R/W	0h	Enables rotational CS for interval data eye training. Set to 1 for rotating CS.

4.2.343 DDRSS_CTL_344 Register (Offset = 560h) [reset = 0h]

DDRSS_CTL_344 is shown in [Figure 4-392](#) and described in [Table 4-788](#).

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Table 4-787. DDRSS_CTL_344 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0560h

Figure 4-392. DDRSS_CTL_344 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_HIGH_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_NORM_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-788. DDRSS_CTL_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_HIGH_THRESHOLD_F0	R/W	0h	Read leveling high threshold number of long counts until the high priority request is asserted.
15-0	RDLVL_NORM_THRESHOLD_F0	R/W	0h	Read leveling normal threshold number of long counts until the normal priority request is asserted.

4.2.344 DDRSS_CTL_345 Register (Offset = 564h) [reset = 0h]

DDRSS_CTL_345 is shown in [Figure 4-393](#) and described in [Table 4-790](#).

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Table 4-789. DDRSS_CTL_345 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0564h

Figure 4-393. DDRSS_CTL_345 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_SW_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_TIMEOUT_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-790. DDRSS_CTL_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_SW_PROMOTE_THRESHOLD_F0	R/W	0h	Read leveling promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	RDLVL_TIMEOUT_F0	R/W	0h	Read leveling timeout number of long counts until the timeout is asserted.

4.2.345 DDRSS_CTL_346 Register (Offset = 568h) [reset = 0h]

DDRSS_CTL_346 is shown in [Figure 4-394](#) and described in [Table 4-792](#).

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Table 4-791. DDRSS_CTL_346 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0568h

Figure 4-394. DDRSS_CTL_346 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_NORM_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_DFI_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-792. DDRSS_CTL_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_NORM_THRESHOLD_F0	R/W	0h	Gate training normal threshold number of long counts until the normal priority request is asserted.
15-0	RDLVL_DFI_PROMOTE_THRESHOLD_F0	R/W	0h	Read leveling promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.346 DDRSS_CTL_347 Register (Offset = 56Ch) [reset = 0h]

DDRSS_CTL_347 is shown in [Figure 4-395](#) and described in [Table 4-794](#).

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Table 4-793. DDRSS_CTL_347 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 056Ch

Figure 4-395. DDRSS_CTL_347 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_TIMEOUT_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_GATE_HIGH_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-794. DDRSS_CTL_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_TIMEOUT_F0	R/W	0h	Gate training timeout number of long counts until the timeout is asserted.
15-0	RDLVL_GATE_HIGH_THRESHOLD_F0	R/W	0h	Gate training high threshold number of long counts until the high priority request is asserted.

4.2.347 DDRSS_CTL_348 Register (Offset = 570h) [reset = 0h]

DDRSS_CTL_348 is shown in [Figure 4-396](#) and described in [Table 4-796](#).

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Table 4-795. DDRSS_CTL_348 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0570h

Figure 4-396. DDRSS_CTL_348 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_GATE_SW_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-796. DDRSS_CTL_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F0	R/W	0h	Gate training promotion number of long counts until the high priority request is asserted. Applies to DFI commands.
15-0	RDLVL_GATE_SW_PROMOTE_THRESHOLD_F0	R/W	0h	Gate training promotion number of long counts until the high priority request is asserted. Applies to SW commands.

4.2.348 DDRSS_CTL_349 Register (Offset = 574h) [reset = 0h]

DDRSS_CTL_349 is shown in [Figure 4-397](#) and described in [Table 4-798](#).

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Table 4-797. DDRSS_CTL_349 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0574h

Figure 4-397. DDRSS_CTL_349 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_HIGH_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_NORM_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-798. DDRSS_CTL_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_HIGH_THRESHOLD_F1	R/W	0h	Read leveling high threshold number of long counts until the high priority request is asserted.
15-0	RDLVL_NORM_THRESHOLD_F1	R/W	0h	Read leveling normal threshold number of long counts until the normal priority request is asserted.

4.2.349 DDRSS_CTL_350 Register (Offset = 578h) [reset = 0h]

DDRSS_CTL_350 is shown in [Figure 4-398](#) and described in [Table 4-800](#).

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Table 4-799. DDRSS_CTL_350 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0578h

Figure 4-398. DDRSS_CTL_350 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_SW_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_TIMEOUT_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-800. DDRSS_CTL_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_SW_PROMOTE_THRESHOLD_F1	R/W	0h	Read leveling promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	RDLVL_TIMEOUT_F1	R/W	0h	Read leveling timeout number of long counts until the timeout is asserted.

4.2.350 DDRSS_CTL_351 Register (Offset = 57Ch) [reset = 0h]

DDRSS_CTL_351 is shown in [Figure 4-399](#) and described in [Table 4-802](#).

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Table 4-801. DDRSS_CTL_351 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 057Ch

Figure 4-399. DDRSS_CTL_351 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_NORM_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_DFI_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-802. DDRSS_CTL_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_NORM_THRESHOLD_F1	R/W	0h	Gate training normal threshold number of long counts until the normal priority request is asserted.
15-0	RDLVL_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	Read leveling promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.351 DDRSS_CTL_352 Register (Offset = 580h) [reset = 0h]

DDRSS_CTL_352 is shown in [Figure 4-400](#) and described in [Table 4-804](#).

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Table 4-803. DDRSS_CTL_352 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0580h

Figure 4-400. DDRSS_CTL_352 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_TIMEOUT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_GATE_HIGH_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-804. DDRSS_CTL_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_TIMEOUT_F1	R/W	0h	Gate training timeout number of long counts until the timeout is asserted.
15-0	RDLVL_GATE_HIGH_THRESHOLD_F1	R/W	0h	Gate training high threshold number of long counts until the high priority request is asserted.

4.2.352 DDRSS_CTL_353 Register (Offset = 584h) [reset = 0h]

DDRSS_CTL_353 is shown in [Figure 4-401](#) and described in [Table 4-806](#).

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Table 4-805. DDRSS_CTL_353 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0584h

Figure 4-401. DDRSS_CTL_353 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_GATE_SW_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-806. DDRSS_CTL_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	Gate training promotion number of long counts until the high priority request is asserted. Applies to DFI commands.
15-0	RDLVL_GATE_SW_PROMOTE_THRESHOLD_F1	R/W	0h	Gate training promotion number of long counts until the high priority request is asserted. Applies to SW commands.

4.2.353 DDRSS_CTL_354 Register (Offset = 588h) [reset = 0h]

DDRSS_CTL_354 is shown in [Figure 4-402](#) and described in [Table 4-808](#).

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Table 4-807. DDRSS_CTL_354 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0588h

Figure 4-402. DDRSS_CTL_354 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_HIGH_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_NORM_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-808. DDRSS_CTL_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_HIGH_THRESHOLD_F2	R/W	0h	Read leveling high threshold number of long counts until the high priority request is asserted.
15-0	RDLVL_NORM_THRESHOLD_F2	R/W	0h	Read leveling normal threshold number of long counts until the normal priority request is asserted.

4.2.354 DDRSS_CTL_355 Register (Offset = 58Ch) [reset = 0h]

DDRSS_CTL_355 is shown in [Figure 4-403](#) and described in [Table 4-810](#).

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Table 4-809. DDRSS_CTL_355 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 058Ch

Figure 4-403. DDRSS_CTL_355 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_SW_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_TIMEOUT_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-810. DDRSS_CTL_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_SW_PROMOTE_THRESHOLD_F2	R/W	0h	Read leveling promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	RDLVL_TIMEOUT_F2	R/W	0h	Read leveling timeout number of long counts until the timeout is asserted.

4.2.355 DDRSS_CTL_356 Register (Offset = 590h) [reset = 0h]

DDRSS_CTL_356 is shown in [Figure 4-404](#) and described in [Table 4-812](#).

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Table 4-811. DDRSS_CTL_356 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0590h

Figure 4-404. DDRSS_CTL_356 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_NORM_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_DFI_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-812. DDRSS_CTL_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_NORM_THRESHOLD_F2	R/W	0h	Gate training normal threshold number of long counts until the normal priority request is asserted.
15-0	RDLVL_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	Read leveling promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.356 DDRSS_CTL_357 Register (Offset = 594h) [reset = 0h]

DDRSS_CTL_357 is shown in [Figure 4-405](#) and described in [Table 4-814](#).

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Table 4-813. DDRSS_CTL_357 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0594h

Figure 4-405. DDRSS_CTL_357 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_TIMEOUT_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_GATE_HIGH_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-814. DDRSS_CTL_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_TIMEOUT_F2	R/W	0h	Gate training timeout number of long counts until the timeout is asserted.
15-0	RDLVL_GATE_HIGH_THRESHOLD_F2	R/W	0h	Gate training high threshold number of long counts until the high priority request is asserted.

4.2.357 DDRSS_CTL_358 Register (Offset = 598h) [reset = 0h]

DDRSS_CTL_358 is shown in [Figure 4-406](#) and described in [Table 4-816](#).

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Table 4-815. DDRSS_CTL_358 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0598h

Figure 4-406. DDRSS_CTL_358 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDLVL_GATE_SW_PROMOTE_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-816. DDRSS_CTL_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	Gate training promotion number of long counts until the high priority request is asserted. Applies to DFI commands.
15-0	RDLVL_GATE_SW_PROMOTE_THRESHOLD_F2	R/W	0h	Gate training promotion number of long counts until the high priority request is asserted. Applies to SW commands.

4.2.358 DDRSS_CTL_359 Register (Offset = 59Ch) [reset = X]

DDRSS_CTL_359 is shown in [Figure 4-407](#) and described in [Table 4-818](#).

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Table 4-817. DDRSS_CTL_359 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 059Ch

Figure 4-407. DDRSS_CTL_359 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							CALVL_CS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CALVL_REQ
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-818. DDRSS_CTL_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	CALVL_CS	R/W	0h	Specifies the target chip select for the CA training operation initiated through the CALVL_REQ parameter.
7-1	RESERVED	R/W	X	
0	CALVL_REQ	W	0h	User request to initiate CA training. Set to 1 to trigger. WRITE-ONLY

4.2.359 DDRSS_CTL_360 Register (Offset = 5A0h) [reset = X]

DDRSS_CTL_360 is shown in [Figure 4-408](#) and described in [Table 4-820](#).

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Table 4-819. DDRSS_CTL_360 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05A0h

Figure 4-408. DDRSS_CTL_360 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_PAT_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-820. DDRSS_CTL_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_PAT_0	R/W	0h	CA Training pattern 0 driven on the CA bus during a calibration command.

4.2.360 DDRSS_CTL_361 Register (Offset = 5A4h) [reset = X]

DDRSS_CTL_361 is shown in [Figure 4-409](#) and described in [Table 4-822](#).

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Table 4-821. DDRSS_CTL_361 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05A4h

Figure 4-409. DDRSS_CTL_361 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_BG_PAT_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-822. DDRSS_CTL_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_BG_PAT_0	R/W	0h	CA Training pattern 0 driven on the CA bus before and after a calibration command.

4.2.361 DDRSS_CTL_362 Register (Offset = 5A8h) [reset = X]

DDRSS_CTL_362 is shown in [Figure 4-410](#) and described in [Table 4-824](#).

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Table 4-823. DDRSS_CTL_362 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05A8h

Figure 4-410. DDRSS_CTL_362 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_PAT_1																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-824. DDRSS_CTL_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_PAT_1	R/W	0h	CA Training pattern 1 driven on the CA bus during a calibration command.

4.2.362 DDRSS_CTL_363 Register (Offset = 5ACh) [reset = X]

DDRSS_CTL_363 is shown in [Figure 4-411](#) and described in [Table 4-826](#).

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Table 4-825. DDRSS_CTL_363 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05ACh

Figure 4-411. DDRSS_CTL_363 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_BG_PAT_1																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-826. DDRSS_CTL_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_BG_PAT_1	R/W	0h	CA Training pattern 1 driven on the CA bus before and after a calibration command.

4.2.363 DDRSS_CTL_364 Register (Offset = 5B0h) [reset = X]

DDRSS_CTL_364 is shown in [Figure 4-412](#) and described in [Table 4-828](#).

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Table 4-827. DDRSS_CTL_364 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05B0h

Figure 4-412. DDRSS_CTL_364 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_PAT_2																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-828. DDRSS_CTL_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_PAT_2	R/W	0h	CA Training pattern 2 driven on the CA bus during a calibration command.

4.2.364 DDRSS_CTL_365 Register (Offset = 5B4h) [reset = X]

DDRSS_CTL_365 is shown in [Figure 4-413](#) and described in [Table 4-830](#).

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Table 4-829. DDRSS_CTL_365 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05B4h

Figure 4-413. DDRSS_CTL_365 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_BG_PAT_2																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-830. DDRSS_CTL_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_BG_PAT_2	R/W	0h	CA Training pattern 2 driven on the CA bus before and after a calibration command.

4.2.365 DDRSS_CTL_366 Register (Offset = 5B8h) [reset = X]

DDRSS_CTL_366 is shown in [Figure 4-414](#) and described in [Table 4-832](#).

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Table 4-831. DDRSS_CTL_366 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05B8h

Figure 4-414. DDRSS_CTL_366 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CALVL_PAT_3																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-832. DDRSS_CTL_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	CALVL_PAT_3	R/W	0h	CA Training pattern 3 driven on the CA bus during a calibration command.

4.2.366 DDRSS_CTL_367 Register (Offset = 5BCh) [reset = X]

DDRSS_CTL_367 is shown in [Figure 4-415](#) and described in [Table 4-834](#).

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Table 4-833. DDRSS_CTL_367 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05BCh

Figure 4-415. DDRSS_CTL_367 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				CALVL_BG_PAT_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
CALVL_BG_PAT_3							
R/W-0h							
7	6	5	4	3	2	1	0
CALVL_BG_PAT_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-834. DDRSS_CTL_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-20	RESERVED	R/W	X	
19-0	CALVL_BG_PAT_3	R/W	0h	CA Training pattern 3 driven on the CA bus before and after a calibration command.

4.2.367 DDRSS_CTL_368 Register (Offset = 5C0h) [reset = X]

DDRSS_CTL_368 is shown in [Figure 4-416](#) and described in [Table 4-836](#).

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Table 4-835. DDRSS_CTL_368 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05C0h

Figure 4-416. DDRSS_CTL_368 Register

31	30	29	28	27	26	25	24
RESERVED							CALVL_PERIODIC
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							DFI_PHY_CALVL_MODE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						CALVL_SEQ_EN	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-836. DDRSS_CTL_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	CALVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during CA training. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	DFI_PHY_CALVL_MODE	R/W	0h	Specifies the PHY support for DFI CA training. Set to 1 for supported.
15-10	RESERVED	R/W	X	
9-8	CALVL_SEQ_EN	R/W	0h	Specifies which CA training patterns will be used. Clear to 0 for pattern 0 only, program to 1 for patterns 0 and 1, program to 2 for patterns 0, 1 and 2, or program to 3 for all patterns.
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.2.368 DDRSS_CTL_369 Register (Offset = 5C4h) [reset = X]

DDRSS_CTL_369 is shown in [Figure 4-417](#) and described in [Table 4-838](#).

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Table 4-837. DDRSS_CTL_369 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05C4h

Figure 4-417. DDRSS_CTL_369 Register

31	30	29	28	27	26	25	24
RESERVED						CALVL_CS_MAP	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						CALVL_ROTATE	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						CALVL_AREF_EN	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						CALVL_ON_SREF_EXIT	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-838. DDRSS_CTL_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	CALVL_CS_MAP	R/W	0h	Defines the chip select map for CA training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for CA training.
23-17	RESERVED	R/W	X	
16	CALVL_ROTATE	R/W	0h	Enables rotational CS for interval CA training. Set to 1 for rotating CS.
15-9	RESERVED	R/W	X	
8	CALVL_AREF_EN	R/W	0h	Enables refreshes and other non-data commands to execute in the middle of CA training. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	CALVL_ON_SREF_EXIT	R/W	0h	Enables automatic CA training on a self-refresh exit. Set to 1 to enable.

4.2.369 DDRSS_CTL_370 Register (Offset = 5C8h) [reset = 0h]

DDRSS_CTL_370 is shown in [Figure 4-418](#) and described in [Table 4-840](#).

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Table 4-839. DDRSS_CTL_370 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05C8h

Figure 4-418. DDRSS_CTL_370 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_HIGH_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_NORM_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-840. DDRSS_CTL_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_HIGH_THRESHOLD_F0	R/W	0h	CA training high threshold number of long counts until the high priority request is asserted.
15-0	CALVL_NORM_THRESHOLD_F0	R/W	0h	CA training normal threshold number of long counts until the normal priority request is asserted.

4.2.370 DDRSS_CTL_371 Register (Offset = 5CCh) [reset = 0h]

DDRSS_CTL_371 is shown in [Figure 4-419](#) and described in [Table 4-842](#).

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Table 4-841. DDRSS_CTL_371 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05CCh

Figure 4-419. DDRSS_CTL_371 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_SW_PROMOTE_THRESHOLD_F0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_TIMEOUT_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-842. DDRSS_CTL_371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_SW_PROMOTE_THRESHOLD_F0	R/W	0h	CA training promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	CALVL_TIMEOUT_F0	R/W	0h	CA training timeout number of long counts until the timeout is asserted.

4.2.371 DDRSS_CTL_372 Register (Offset = 5D0h) [reset = 0h]

DDRSS_CTL_372 is shown in [Figure 4-420](#) and described in [Table 4-844](#).

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Table 4-843. DDRSS_CTL_372 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05D0h

Figure 4-420. DDRSS_CTL_372 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_NORM_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_DFI_PROMOTE_THRESHOLD_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-844. DDRSS_CTL_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_NORM_THRESH OLD_F1	R/W	0h	CA training normal threshold number of long counts until the normal priority request is asserted.
15-0	CALVL_DFI_PROMOTE_ THRESHOLD_F0	R/W	0h	CA training promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.372 DDRSS_CTL_373 Register (Offset = 5D4h) [reset = 0h]

DDRSS_CTL_373 is shown in [Figure 4-421](#) and described in [Table 4-846](#).

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Table 4-845. DDRSS_CTL_373 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05D4h

Figure 4-421. DDRSS_CTL_373 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_TIMEOUT_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_HIGH_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-846. DDRSS_CTL_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_TIMEOUT_F1	R/W	0h	CA training timeout number of long counts until the timeout is asserted.
15-0	CALVL_HIGH_THRESHOLD_F1	R/W	0h	CA training high threshold number of long counts until the high priority request is asserted.

4.2.373 DDRSS_CTL_374 Register (Offset = 5D8h) [reset = 0h]

DDRSS_CTL_374 is shown in [Figure 4-422](#) and described in [Table 4-848](#).

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Table 4-847. DDRSS_CTL_374 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05D8h

Figure 4-422. DDRSS_CTL_374 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_DFI_PROMOTE_THRESHOLD_F1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_SW_PROMOTE_THRESHOLD_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-848. DDRSS_CTL_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_DFI_PROMOTE_THRESHOLD_F1	R/W	0h	CA training promotion number of long counts until the high priority request is asserted. Applies to DFI commands.
15-0	CALVL_SW_PROMOTE_THRESHOLD_F1	R/W	0h	CA training promotion number of long counts until the high priority request is asserted. Applies to SW commands.

4.2.374 DDRSS_CTL_375 Register (Offset = 5DCh) [reset = 0h]

DDRSS_CTL_375 is shown in [Figure 4-423](#) and described in [Table 4-850](#).

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Table 4-849. DDRSS_CTL_375 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05DCh

Figure 4-423. DDRSS_CTL_375 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_HIGH_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_NORM_THRESHOLD_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-850. DDRSS_CTL_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_HIGH_THRESHOLD_F2	R/W	0h	CA training high threshold number of long counts until the high priority request is asserted.
15-0	CALVL_NORM_THRESHOLD_F2	R/W	0h	CA training normal threshold number of long counts until the normal priority request is asserted.

4.2.375 DDRSS_CTL_376 Register (Offset = 5E0h) [reset = 0h]

DDRSS_CTL_376 is shown in [Figure 4-424](#) and described in [Table 4-852](#).

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Table 4-851. DDRSS_CTL_376 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05E0h

Figure 4-424. DDRSS_CTL_376 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CALVL_SW_PROMOTE_THRESHOLD_F2															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CALVL_TIMEOUT_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-852. DDRSS_CTL_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CALVL_SW_PROMOTE_THRESHOLD_F2	R/W	0h	CA training promotion number of long counts until the high priority request is asserted. Applies to SW commands.
15-0	CALVL_TIMEOUT_F2	R/W	0h	CA training timeout number of long counts until the timeout is asserted.

4.2.376 DDRSS_CTL_377 Register (Offset = 5E4h) [reset = X]

DDRSS_CTL_377 is shown in Figure 4-425 and described in Table 4-854.

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Table 4-853. DDRSS_CTL_377 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05E4h

Figure 4-425. DDRSS_CTL_377 Register

31	30	29	28	27	26	25	24
RESERVED							AXI0_FIXED_P ORT_PRIORIT Y_ENABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							AXI0_ALL_STR OBES_USED_ ENABLE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
CALVL_DFI_PROMOTE_THRESHOLD_F2							
R/W-0h							
7	6	5	4	3	2	1	0
CALVL_DFI_PROMOTE_THRESHOLD_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-854. DDRSS_CTL_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	AXI0_FIXED_PORT_PRIORITY_ENABLE	R/W	0h	Defines the priority control for AXI port 0 as per-port or per-command. Set to 1 for per-port with priority defined through the AXI4_R_PRIORITY and AXI4_W_PRIORITY parameters. Clear to 0 for per-command.
23-17	RESERVED	R/W	X	
16	AXI0_ALL_STROBES_USED_ENABLE	R/W	0h	Enables use of the AWALLSTRB signal for AXI port 0. Set to 1 to enable.
15-0	CALVL_DFI_PROMOTE_THRESHOLD_F2	R/W	0h	CA training promotion number of long counts until the high priority request is asserted. Applies to DFI commands.

4.2.377 DDRSS_CTL_378 Register (Offset = 5E8h) [reset = X]

DDRSS_CTL_378 is shown in [Figure 4-426](#) and described in [Table 4-856](#).

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Table 4-855. DDRSS_CTL_378 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05E8h

Figure 4-426. DDRSS_CTL_378 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED					AXI0_W_PRIORITY		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED					AXI0_R_PRIORITY		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-856. DDRSS_CTL_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-8	AXI0_W_PRIORITY	R/W	0h	Priority of write commands from AXI port 0. 0 is the highest priority. This may only be changed before initialization begins or when the controller is quiescent, there is no data in the port FIFOs, and the AXI0_FIXED_PORT_PRIORITY_ENABLE parameter is low.
7-3	RESERVED	R/W	X	
2-0	AXI0_R_PRIORITY	R/W	0h	Priority of read commands from AXI port 0. 0 is the highest priority. This may only be changed before initialization begins or when the controller is quiescent, there is no data in the port FIFOs, and the AXI0_FIXED_PORT_PRIORITY_ENABLE parameter is low.

4.2.378 DDRSS_CTL_379 Register (Offset = 5ECh) [reset = 0h]

DDRSS_CTL_379 is shown in [Figure 4-427](#) and described in [Table 4-858](#).

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Table 4-857. DDRSS_CTL_379 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05ECh

Figure 4-427. DDRSS_CTL_379 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARITY_ERROR_ADDRESS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-858. DDRSS_CTL_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PARITY_ERROR_ADDRESS_0	R	0h	Address of the AXI command that resulted in the parity error. READ-ONLY

4.2.379 DDRSS_CTL_380 Register (Offset = 5F0h) [reset = X]

DDRSS_CTL_380 is shown in [Figure 4-428](#) and described in [Table 4-860](#).

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Table 4-859. DDRSS_CTL_380 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05F0h

Figure 4-428. DDRSS_CTL_380 Register

31	30	29	28	27	26	25	24
RESERVED				PARITY_ERROR_BUS_CHANNEL			
R-X				R-0h			
23	22	21	20	19	18	17	16
PARITY_ERROR_BUS_CHANNEL							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		PARITY_ERROR_MASTER_ID					
R-X		R-0h					
7	6	5	4	3	2	1	0
RESERVED					PARITY_ERROR_ADDRESS_1		
R-X					R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 4-860. DDRSS_CTL_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	X	
28-16	PARITY_ERROR_BUS_CHANNEL	R	0h	Reports the AXI field that resulted in the parity error. Bit (0) specifies if the error was on the read channel (value of 0) or the write channel (value of 1). Subsequent bits specify the exact signal that had a parity error. Bit (1): ARADDR/AWADDR, Bit (2): ARID/AWID, Bit (3): ARLEN/AWLEN, Bit (4): ARSIZE/AWSIZE, Bit (5): ARBURST/AWBURST, Bit (6): ARQOS/AWQOS, Bit (7): Misc group signals, Bit (8): Reserved, Bit (9): Reserved, Bit (10): WDATA, Bit (11): (WLAST,WSTRB), and Bit (12): Reserved. READ-ONLY
15-14	RESERVED	R	X	
13-8	PARITY_ERROR_MASTER_ID	R	0h	Port ID and Master ID of the AXI command that resulted in the parity error. READ-ONLY
7-3	RESERVED	R	X	
2-0	PARITY_ERROR_ADDRESS_1	R	0h	Address of the AXI command that resulted in the parity error. READ-ONLY

4.2.380 DDRSS_CTL_381 Register (Offset = 5F4h) [reset = 0h]

DDRSS_CTL_381 is shown in [Figure 4-429](#) and described in [Table 4-862](#).

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Table 4-861. DDRSS_CTL_381 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05F4h

Figure 4-429. DDRSS_CTL_381 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARITY_ERROR_WRITE_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-862. DDRSS_CTL_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PARITY_ERROR_WRITE_DATA_0	R	0h	Write data of the AXI command that resulted in the parity error. READ-ONLY

4.2.381 DDRSS_CTL_382 Register (Offset = 5F8h) [reset = 0h]

DDRSS_CTL_382 is shown in [Figure 4-430](#) and described in [Table 4-864](#).

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Table 4-863. DDRSS_CTL_382 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05F8h

Figure 4-430. DDRSS_CTL_382 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARITY_ERROR_WRITE_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-864. DDRSS_CTL_382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PARITY_ERROR_WRITE_DATA_1	R	0h	Write data of the AXI command that resulted in the parity error. READ-ONLY

4.2.382 DDRSS_CTL_383 Register (Offset = 5FCh) [reset = 0h]

DDRSS_CTL_383 is shown in [Figure 4-431](#) and described in [Table 4-866](#).

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Table 4-865. DDRSS_CTL_383 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 05FCh

Figure 4-431. DDRSS_CTL_383 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARITY_ERROR_WRITE_DATA_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-866. DDRSS_CTL_383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PARITY_ERROR_WRITE_DATA_2	R	0h	Write data of the AXI command that resulted in the parity error. READ-ONLY

4.2.383 DDRSS_CTL_384 Register (Offset = 600h) [reset = 0h]

DDRSS_CTL_384 is shown in [Figure 4-432](#) and described in [Table 4-868](#).

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Table 4-867. DDRSS_CTL_384 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0600h

Figure 4-432. DDRSS_CTL_384 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARITY_ERROR_WRITE_DATA_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-868. DDRSS_CTL_384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PARITY_ERROR_WRITE_DATA_3	R	0h	Write data of the AXI command that resulted in the parity error. READ-ONLY

4.2.384 DDRSS_CTL_385 Register (Offset = 604h) [reset = X]

DDRSS_CTL_385 is shown in [Figure 4-433](#) and described in [Table 4-870](#).

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Table 4-869. DDRSS_CTL_385 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0604h

Figure 4-433. DDRSS_CTL_385 Register

31	30	29	28	27	26	25	24
RESERVED							MEM_RST_VALID
R-X							R-0h
23	22	21	20	19	18	17	16
RESERVED						CKE_STATUS	
R-X						R-0h	
15	14	13	12	11	10	9	8
PARITY_ERROR_WRITE_DATA_PARITY_VECTOR							
R-0h							
7	6	5	4	3	2	1	0
PARITY_ERROR_WRITE_DATA_PARITY_VECTOR							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-870. DDRSS_CTL_385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	X	
24	MEM_RST_VALID	R	0h	Register access to mem_rst_valid signal. READ-ONLY
23-18	RESERVED	R	X	
17-16	CKE_STATUS	R	0h	Register access to cke_status signal. READ-ONLY
15-0	PARITY_ERROR_WRITE_DATA_PARITY_VECTOR	R	0h	Write data parity vector associated with the AXI command that resulted in the parity error. READ-ONLY

4.2.385 DDRSS_CTL_386 Register (Offset = 608h) [reset = X]

DDRSS_CTL_386 is shown in [Figure 4-434](#) and described in [Table 4-872](#).

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Table 4-871. DDRSS_CTL_386 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0608h

Figure 4-434. DDRSS_CTL_386 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESE RVED	TDFI_PHY_WRLAT							DLL_RST_ADJ_DLY							
R/W-X	R-0h							R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLL_RST_DELAY															
R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-872. DDRSS_CTL_386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	TDFI_PHY_WRLAT	R	0h	Holds the calculated DFI tPHY_WRLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_en assertion. READ-ONLY
23-16	DLL_RST_ADJ_DLY	R/W	0h	Minimum cycles after setting master delay in DLL until the DLL reset signal dll_rst_n may be asserted. If this signal is not being used by the PHY, this parameter may be ignored.
15-0	DLL_RST_DELAY	R/W	0h	Minimum cycles required for DLL reset signal dll_rst_n to be held. If this signal is not being used by the PHY, this parameter may be ignored.

4.2.386 DDRSS_CTL_387 Register (Offset = 60Ch) [reset = X]

DDRSS_CTL_387 is shown in [Figure 4-435](#) and described in [Table 4-874](#).

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Table 4-873. DDRSS_CTL_387 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 060Ch

Figure 4-435. DDRSS_CTL_387 Register

31	30	29	28	27	26	25	24
RESERVED	TDFI_PHY_RDLAT_F2						
R/W-X	R/W-6h						
23	22	21	20	19	18	17	16
RESERVED	TDFI_PHY_RDLAT_F1						
R/W-X	R/W-6h						
15	14	13	12	11	10	9	8
RESERVED	TDFI_PHY_RDLAT_F0						
R/W-X	R/W-6h						
7	6	5	4	3	2	1	0
RESERVED	UPDATE_ERROR_STATUS						
R/W-X	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-874. DDRSS_CTL_387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	TDFI_PHY_RDLAT_F2	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion.
23	RESERVED	R/W	X	
22-16	TDFI_PHY_RDLAT_F1	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion.
15	RESERVED	R/W	X	
14-8	TDFI_PHY_RDLAT_F0	R/W	6h	Defines the DFI tPHY_RDLAT timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_rddata_en assertion and a dfi_rddata_valid assertion.
7	RESERVED	R/W	X	
6-0	UPDATE_ERROR_STATUS	R	0h	Identifies the source of any DFI MC-initiated or PHY-initiated update errors. Value of 1 indicates a timing violation of the associated timing parameter. READ-ONLY

4.2.387 DDRSS_CTL_388 Register (Offset = 610h) [reset = X]

DDRSS_CTL_388 is shown in [Figure 4-436](#) and described in [Table 4-876](#).

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Table 4-875. DDRSS_CTL_388 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0610h

Figure 4-436. DDRSS_CTL_388 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
TDFI_CTRLUPD_MIN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						DRAM_CLK_DISABLE	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	TDFI_RDDATA_EN						
R/W-X	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-876. DDRSS_CTL_388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	TDFI_CTRLUPD_MIN	R/W	0h	Defines the DFI tCTRLUPD_MIN timing parameter (in DFI clocks), the minimum cycles that dfi_ctrlupd_req must be asserted.
15-10	RESERVED	R/W	X	
9-8	DRAM_CLK_DISABLE	R/W	0h	Set value for the dfi_dram_clk_disable signal. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to disable.
7	RESERVED	R/W	X	
6-0	TDFI_RDDATA_EN	R	0h	Holds the calculated DFI tRDDATA_EN timing parameter (in DFI PHY clocks), the maximum cycles between a read command and a dfi_rddata_en assertion. READ-ONLY

4.2.388 DDRSS_CTL_389 Register (Offset = 614h) [reset = X]

DDRSS_CTL_389 is shown in [Figure 4-437](#) and described in [Table 4-878](#).

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Table 4-877. DDRSS_CTL_389 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0614h

Figure 4-437. DDRSS_CTL_389 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TDFI_CTRLUPD_MAX_F0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-878. DDRSS_CTL_389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-0	TDFI_CTRLUPD_MAX_F0	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the UPDATE_ERROR_STATUS parameter.

4.2.389 DDRSS_CTL_390 Register (Offset = 618h) [reset = 0h]

DDRSS_CTL_390 is shown in [Figure 4-438](#) and described in [Table 4-880](#).

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Table 4-879. DDRSS_CTL_390 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0618h

Figure 4-438. DDRSS_CTL_390 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-880. DDRSS_CTL_390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE0_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) set in the UPDATE_ERROR_STATUS parameter.

4.2.390 DDRSS_CTL_391 Register (Offset = 61Ch) [reset = 0h]

DDRSS_CTL_391 is shown in [Figure 4-439](#) and described in [Table 4-882](#).

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Table 4-881. DDRSS_CTL_391 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 061Ch

Figure 4-439. DDRSS_CTL_391 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE1_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-882. DDRSS_CTL_391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE1_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (2) set in the UPDATE_ERROR_STATUS parameter.

4.2.391 DDRSS_CTL_392 Register (Offset = 620h) [reset = 0h]

DDRSS_CTL_392 is shown in [Figure 4-440](#) and described in [Table 4-884](#).

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Table 4-883. DDRSS_CTL_392 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0620h

Figure 4-440. DDRSS_CTL_392 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE2_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-884. DDRSS_CTL_392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE2_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (3) set in the UPDATE_ERROR_STATUS parameter.

4.2.392 DDRSS_CTL_393 Register (Offset = 624h) [reset = 0h]

DDRSS_CTL_393 is shown in [Figure 4-441](#) and described in [Table 4-886](#).

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Table 4-885. DDRSS_CTL_393 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0624h

Figure 4-441. DDRSS_CTL_393 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-886. DDRSS_CTL_393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE3_F0	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit (4) set in the UPDATE_ERROR_STATUS parameter.

4.2.393 DDRSS_CTL_394 Register (Offset = 628h) [reset = X]

DDRSS_CTL_394 is shown in [Figure 4-442](#) and described in [Table 4-888](#).

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Table 4-887. DDRSS_CTL_394 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0628h

Figure 4-442. DDRSS_CTL_394 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TDFI_PHYUPD_RESP_F0																						
R/W-X									R/W-0h																						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-888. DDRSS_CTL_394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-0	TDFI_PHYUPD_RESP_F0	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit (5) set in the UPDATE_ERROR_STATUS parameter.

4.2.394 DDRSS_CTL_395 Register (Offset = 62Ch) [reset = 0h]

DDRSS_CTL_395 is shown in [Figure 4-443](#) and described in [Table 4-890](#).

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Table 4-889. DDRSS_CTL_395 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 062Ch

Figure 4-443. DDRSS_CTL_395 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-890. DDRSS_CTL_395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_CTRLUPD_INTERVAL_F0	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit (6) set in the UPDATE_ERROR_STATUS parameter.

4.2.395 DDRSS_CTL_396 Register (Offset = 630h) [reset = X]

DDRSS_CTL_396 is shown in [Figure 4-444](#) and described in [Table 4-892](#).

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Table 4-891. DDRSS_CTL_396 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0630h

Figure 4-444. DDRSS_CTL_396 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	WRLAT_ADJ_F0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	RDLAT_ADJ_F0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-892. DDRSS_CTL_396 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-8	WRLAT_ADJ_F0	R/W	0h	Adjustment value for PHY write timing.
7	RESERVED	R/W	X	
6-0	RDLAT_ADJ_F0	R/W	0h	Adjustment value for PHY read timing.

4.2.396 DDRSS_CTL_397 Register (Offset = 634h) [reset = X]

DDRSS_CTL_397 is shown in [Figure 4-445](#) and described in [Table 4-894](#).

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Table 4-893. DDRSS_CTL_397 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0634h

Figure 4-445. DDRSS_CTL_397 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											TDFI_CTRLUPD_MAX_F1																				
R/W-X											R/W-0h																				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-894. DDRSS_CTL_397 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-0	TDFI_CTRLUPD_MAX_F1	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the UPDATE_ERROR_STATUS parameter.

4.2.397 DDRSS_CTL_398 Register (Offset = 638h) [reset = 0h]

DDRSS_CTL_398 is shown in [Figure 4-446](#) and described in [Table 4-896](#).

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Table 4-895. DDRSS_CTL_398 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0638h

Figure 4-446. DDRSS_CTL_398 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-896. DDRSS_CTL_398 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE0_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) set in the UPDATE_ERROR_STATUS parameter.

4.2.398 DDRSS_CTL_399 Register (Offset = 63Ch) [reset = 0h]

DDRSS_CTL_399 is shown in [Figure 4-447](#) and described in [Table 4-898](#).

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Table 4-897. DDRSS_CTL_399 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 063Ch

Figure 4-447. DDRSS_CTL_399 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE1_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-898. DDRSS_CTL_399 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE1_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (2) set in the UPDATE_ERROR_STATUS parameter.

4.2.399 DDRSS_CTL_400 Register (Offset = 640h) [reset = 0h]

DDRSS_CTL_400 is shown in [Figure 4-448](#) and described in [Table 4-900](#).

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Table 4-899. DDRSS_CTL_400 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0640h

Figure 4-448. DDRSS_CTL_400 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE2_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-900. DDRSS_CTL_400 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE2_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (3) set in the UPDATE_ERROR_STATUS parameter.

4.2.400 DDRSS_CTL_401 Register (Offset = 644h) [reset = 0h]

DDRSS_CTL_401 is shown in [Figure 4-449](#) and described in [Table 4-902](#).

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Table 4-901. DDRSS_CTL_401 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0644h

Figure 4-449. DDRSS_CTL_401 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-902. DDRSS_CTL_401 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE3_F1	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit (4) set in the UPDATE_ERROR_STATUS parameter.

4.2.401 DDRSS_CTL_402 Register (Offset = 648h) [reset = X]

DDRSS_CTL_402 is shown in [Figure 4-450](#) and described in [Table 4-904](#).

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Table 4-903. DDRSS_CTL_402 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0648h

Figure 4-450. DDRSS_CTL_402 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TDFI_PHYUPD_RESP_F1																					
R/W-X										R/W-0h																					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-904. DDRSS_CTL_402 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-0	TDFI_PHYUPD_RESP_F1	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit (5) set in the UPDATE_ERROR_STATUS parameter.

4.2.402 DDRSS_CTL_403 Register (Offset = 64Ch) [reset = 0h]

DDRSS_CTL_403 is shown in [Figure 4-451](#) and described in [Table 4-906](#).

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Table 4-905. DDRSS_CTL_403 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 064Ch

Figure 4-451. DDRSS_CTL_403 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-906. DDRSS_CTL_403 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_CTRLUPD_INTERVAL_F1	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit (6) set in the UPDATE_ERROR_STATUS parameter.

4.2.403 DDRSS_CTL_404 Register (Offset = 650h) [reset = X]

DDRSS_CTL_404 is shown in [Figure 4-452](#) and described in [Table 4-908](#).

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Table 4-907. DDRSS_CTL_404 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0650h

Figure 4-452. DDRSS_CTL_404 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED	WRLAT_ADJ_F1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	RDLAT_ADJ_F1						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-908. DDRSS_CTL_404 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-15	RESERVED	R/W	X	
14-8	WRLAT_ADJ_F1	R/W	0h	Adjustment value for PHY write timing.
7	RESERVED	R/W	X	
6-0	RDLAT_ADJ_F1	R/W	0h	Adjustment value for PHY read timing.

4.2.404 DDRSS_CTL_405 Register (Offset = 654h) [reset = X]

DDRSS_CTL_405 is shown in [Figure 4-453](#) and described in [Table 4-910](#).

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Table 4-909. DDRSS_CTL_405 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0654h

Figure 4-453. DDRSS_CTL_405 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TDFI_CTRLUPD_MAX_F2																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-910. DDRSS_CTL_405 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-0	TDFI_CTRLUPD_MAX_F2	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the UPDATE_ERROR_STATUS parameter.

4.2.405 DDRSS_CTL_406 Register (Offset = 658h) [reset = 0h]

DDRSS_CTL_406 is shown in [Figure 4-454](#) and described in [Table 4-912](#).

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Table 4-911. DDRSS_CTL_406 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0658h

Figure 4-454. DDRSS_CTL_406 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE0_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-912. DDRSS_CTL_406 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE0_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) set in the UPDATE_ERROR_STATUS parameter.

4.2.406 DDRSS_CTL_407 Register (Offset = 65Ch) [reset = 0h]

DDRSS_CTL_407 is shown in [Figure 4-455](#) and described in [Table 4-914](#).

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Table 4-913. DDRSS_CTL_407 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 065Ch

Figure 4-455. DDRSS_CTL_407 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE1_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-914. DDRSS_CTL_407 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE1_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation will cause an interrupt and bit (2) set in the UPDATE_ERROR_STATUS parameter.

4.2.407 DDRSS_CTL_408 Register (Offset = 660h) [reset = 0h]

DDRSS_CTL_408 is shown in [Figure 4-456](#) and described in [Table 4-916](#).

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Table 4-915. DDRSS_CTL_408 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0660h

Figure 4-456. DDRSS_CTL_408 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE2_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-916. DDRSS_CTL_408 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE2_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation will cause an interrupt and bit (3) set in the UPDATE_ERROR_STATUS parameter.

4.2.408 DDRSS_CTL_409 Register (Offset = 664h) [reset = 0h]

DDRSS_CTL_409 is shown in [Figure 4-457](#) and described in [Table 4-918](#).

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Table 4-917. DDRSS_CTL_409 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0664h

Figure 4-457. DDRSS_CTL_409 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_PHYUPD_TYPE3_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-918. DDRSS_CTL_409 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_PHYUPD_TYPE3_F2	R/W	0h	Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation will cause an interrupt and bit (4) set in the UPDATE_ERROR_STATUS parameter.

4.2.409 DDRSS_CTL_410 Register (Offset = 668h) [reset = X]

DDRSS_CTL_410 is shown in [Figure 4-458](#) and described in [Table 4-920](#).

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Table 4-919. DDRSS_CTL_410 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0668h

Figure 4-458. DDRSS_CTL_410 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										TDFI_PHYUPD_RESP_F2																					
R/W-X										R/W-0h																					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-920. DDRSS_CTL_410 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-0	TDFI_PHYUPD_RESP_F2	R/W	0h	Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation will cause an interrupt and bit (5) set in the UPDATE_ERROR_STATUS parameter.

4.2.410 DDRSS_CTL_411 Register (Offset = 66Ch) [reset = 0h]

DDRSS_CTL_411 is shown in [Figure 4-459](#) and described in [Table 4-922](#).

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Table 4-921. DDRSS_CTL_411 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 066Ch

Figure 4-459. DDRSS_CTL_411 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_CTRLUPD_INTERVAL_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-922. DDRSS_CTL_411 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_CTRLUPD_INTERVAL_F2	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit (6) set in the UPDATE_ERROR_STATUS parameter.

4.2.411 DDRSS_CTL_412 Register (Offset = 670h) [reset = X]

DDRSS_CTL_412 is shown in [Figure 4-460](#) and described in [Table 4-924](#).

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Table 4-923. DDRSS_CTL_412 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0670h

Figure 4-460. DDRSS_CTL_412 Register

31	30	29	28	27	26	25	24
RESERVED				TDFI_CTRL_DELAY_F1			
R/W-X				R/W-2h			
23	22	21	20	19	18	17	16
RESERVED				TDFI_CTRL_DELAY_F0			
R/W-X				R/W-2h			
15	14	13	12	11	10	9	8
RESERVED		WRLAT_ADJ_F2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		RDLAT_ADJ_F2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-924. DDRSS_CTL_412 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	TDFI_CTRL_DELAY_F1	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks), the delay between a DFI command change and a memory command.
23-20	RESERVED	R/W	X	
19-16	TDFI_CTRL_DELAY_F0	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks), the delay between a DFI command change and a memory command.
15	RESERVED	R/W	X	
14-8	WRLAT_ADJ_F2	R/W	0h	Adjustment value for PHY write timing.
7	RESERVED	R/W	X	
6-0	RDLAT_ADJ_F2	R/W	0h	Adjustment value for PHY read timing.

4.2.412 DDRSS_CTL_413 Register (Offset = 674h) [reset = X]

DDRSS_CTL_413 is shown in [Figure 4-461](#) and described in [Table 4-926](#).

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Table 4-925. DDRSS_CTL_413 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0674h

Figure 4-461. DDRSS_CTL_413 Register

31	30	29	28	27	26	25	24
TDFI_WRLVL_EN							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				TDFI_DRAM_CLK_ENABLE			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				TDFI_DRAM_CLK_DISABLE			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				TDFI_CTRL_DELAY_F2			
R/W-X				R/W-2h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-926. DDRSS_CTL_413 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TDFI_WRLVL_EN	R/W	0h	Defines the DFI tWRLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_wrlvl_en assertion to the first dfi_wrlvl_strobe assertion.
23-20	RESERVED	R/W	X	
19-16	TDFI_DRAM_CLK_ENABLE	R/W	0h	Defines the DFI tDRAM_CLK_ENABLE timing parameter (in DFI clocks), the delay between a dfi_dram_clk_disable de-assertion and the memory clock enable.
15-12	RESERVED	R/W	X	
11-8	TDFI_DRAM_CLK_DISABLE	R/W	0h	Defines the DFI tDRAM_CLK_DISABLE timing parameter (in DFI clocks), the delay between a dfi_dram_clock_disable assertion and the memory clock disable.
7-4	RESERVED	R/W	X	
3-0	TDFI_CTRL_DELAY_F2	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks), the delay between a DFI command change and a memory command.

4.2.413 DDRSS_CTL_414 Register (Offset = 678h) [reset = X]

DDRSS_CTL_414 is shown in [Figure 4-462](#) and described in [Table 4-928](#).

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Table 4-927. DDRSS_CTL_414 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0678h

Figure 4-462. DDRSS_CTL_414 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TDFI_WRLVL_WW							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-928. DDRSS_CTL_414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TDFI_WRLVL_WW	R/W	0h	Defines the DFI tWRLVL_WW timing parameter (in DFI clocks), the minimum cycles between dfi_wrlvl_strobe assertions.

4.2.414 DDRSS_CTL_415 Register (Offset = 67Ch) [reset = 0h]

DDRSS_CTL_415 is shown in [Figure 4-463](#) and described in [Table 4-930](#).

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Table 4-929. DDRSS_CTL_415 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 067Ch

Figure 4-463. DDRSS_CTL_415 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_WRLVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-930. DDRSS_CTL_415 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_WRLVL_RESP	R/W	0h	Defines the DFI tWRLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_req assertion and a dfi_wrlvl_en assertion.

4.2.415 DDRSS_CTL_416 Register (Offset = 680h) [reset = 0h]

DDRSS_CTL_416 is shown in [Figure 4-464](#) and described in [Table 4-932](#).

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Table 4-931. DDRSS_CTL_416 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0680h

Figure 4-464. DDRSS_CTL_416 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_WRLVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-932. DDRSS_CTL_416 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_WRLVL_MAX	R/W	0h	Defines the DFI tWRLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_en assertion and a valid dfi_wrlvl_resp.

4.2.416 DDRSS_CTL_417 Register (Offset = 684h) [reset = X]

DDRSS_CTL_417 is shown in [Figure 4-465](#) and described in [Table 4-934](#).

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Table 4-933. DDRSS_CTL_417 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0684h

Figure 4-465. DDRSS_CTL_417 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														TDFI_RDLVL_R R	
R/W-X														R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_RDLVL_RR								TDFI_RDLVL_EN							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-934. DDRSS_CTL_417 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	TDFI_RDLVL_RR	R/W	0h	Defines the DFI tRDLVL_RR timing parameter (in DFI clocks), the minimum cycles between read commands.
7-0	TDFI_RDLVL_EN	R/W	0h	Defines the DFI tRDLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion to the first read or MRR.

4.2.417 DDRSS_CTL_418 Register (Offset = 688h) [reset = 0h]

DDRSS_CTL_418 is shown in [Figure 4-466](#) and described in [Table 4-936](#).

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Table 4-935. DDRSS_CTL_418 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0688h

Figure 4-466. DDRSS_CTL_418 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_RDLVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-936. DDRSS_CTL_418 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_RDLVL_RESP	R/W	0h	Defines the DFI tRDLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_rdlvl_req or dfi_rdlvl_gate_req assertion and a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion.

4.2.418 DDRSS_CTL_419 Register (Offset = 68Ch) [reset = X]

DDRSS_CTL_419 is shown in [Figure 4-467](#) and described in [Table 4-938](#).

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Table 4-937. DDRSS_CTL_419 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 068Ch

Figure 4-467. DDRSS_CTL_419 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						RDLVL_GATE_EN	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						RDLVL_EN	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RDLVL_RESP_MASK							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-938. DDRSS_CTL_419 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	RDLVL_GATE_EN	R/W	0h	Enable the MC gate training module. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	RDLVL_EN	R/W	0h	Enable the MC data eye training module. Set to 1 to enable.
7-0	RDLVL_RESP_MASK	R/W	0h	Mask for the dfi_rdlvl_resp signal during data eye training.

4.2.419 DDRSS_CTL_420 Register (Offset = 690h) [reset = 0h]

DDRSS_CTL_420 is shown in [Figure 4-468](#) and described in [Table 4-940](#).

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Table 4-939. DDRSS_CTL_420 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0690h

Figure 4-468. DDRSS_CTL_420 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_RDLVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-940. DDRSS_CTL_420 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_RDLVL_MAX	R/W	0h	Defines the DFI tRDLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion and a valid dfi_rdlvl_resp.

4.2.420 DDRSS_CTL_421 Register (Offset = 694h) [reset = X]

DDRSS_CTL_421 is shown in [Figure 4-469](#) and described in [Table 4-942](#).

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Table 4-941. DDRSS_CTL_421 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0694h

Figure 4-469. DDRSS_CTL_421 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
TDFI_CALVL_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					RDLVL_GATE_ERROR_STATUS		
R/W-X					R-0h		
7	6	5	4	3	2	1	0
RESERVED					RDLVL_ERROR_STATUS		
R/W-X					R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-942. DDRSS_CTL_421 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	TDFI_CALVL_EN	R/W	0h	Defines the DFI tCALVL_EN timing parameter (in DFI clocks), the minimum cycles between a dfi_calvl_en assertion and a dfi_cke de-assertion.
15-11	RESERVED	R/W	X	
10-8	RDLVL_GATE_ERROR_STATUS	R	0h	Holds the error associated with the read gate training error or gate training error interrupt. Bit (0) set indicates a TDFI_RDLVL_MAX parameter violation, bit (1) set indicates a TDFI_RDLVL_RESP parameter violation, and bit (2) set indicates a gate training operation was attempted while memory was in self-refresh mode or self-refresh power-down mode and therefore a false rdlvl_done was signaled to move the state machine back to idle state. READ-ONLY
7-3	RESERVED	R/W	X	
2-0	RDLVL_ERROR_STATUS	R	0h	Holds the error associated with the data eye training error or gate training error interrupt. Bit (0) set indicates a TDFI_RDLVL_MAX parameter violation, bit (1) set indicates a TDFI_RDLVL_RESP parameter violation, and bit (2) set indicates a read leveling operation was attempted while memory was in self-refresh mode or self-refresh power-down mode and therefore a false rdlvl_done was signaled to move the state machine back to idle state. READ-ONLY

4.2.421 DDRSS_CTL_422 Register (Offset = 698h) [reset = X]

DDRSS_CTL_422 is shown in [Figure 4-470](#) and described in [Table 4-944](#).

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Table 4-943. DDRSS_CTL_422 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0698h

Figure 4-470. DDRSS_CTL_422 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TDFI_CALVL_CAPTURE_F0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TDFI_CALVL_CC_F0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-944. DDRSS_CTL_422 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TDFI_CALVL_CAPTURE_F0	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the minimum cycles between a calibration command and a dfi_calvl_capture pulse.
15-10	RESERVED	R/W	X	
9-0	TDFI_CALVL_CC_F0	R/W	0h	Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the minimum cycles between calibration commands.

4.2.422 DDRSS_CTL_423 Register (Offset = 69Ch) [reset = X]

DDRSS_CTL_423 is shown in [Figure 4-471](#) and described in [Table 4-946](#).

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Table 4-945. DDRSS_CTL_423 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 069Ch

Figure 4-471. DDRSS_CTL_423 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TDFI_CALVL_CAPTURE_F1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TDFI_CALVL_CC_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-946. DDRSS_CTL_423 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TDFI_CALVL_CAPTURE_F1	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the minimum cycles between a calibration command and a dfi_calvl_capture pulse.
15-10	RESERVED	R/W	X	
9-0	TDFI_CALVL_CC_F1	R/W	0h	Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the minimum cycles between calibration commands.

4.2.423 DDRSS_CTL_424 Register (Offset = 6A0h) [reset = X]

DDRSS_CTL_424 is shown in [Figure 4-472](#) and described in [Table 4-948](#).

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Table 4-947. DDRSS_CTL_424 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06A0h

Figure 4-472. DDRSS_CTL_424 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TDFI_CALVL_CAPTURE_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TDFI_CALVL_CC_F2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-948. DDRSS_CTL_424 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TDFI_CALVL_CAPTURE_F2	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the minimum cycles between a calibration command and a dfi_calvl_capture pulse.
15-10	RESERVED	R/W	X	
9-0	TDFI_CALVL_CC_F2	R/W	0h	Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the minimum cycles between calibration commands.

4.2.424 DDRSS_CTL_425 Register (Offset = 6A4h) [reset = 0h]

DDRSS_CTL_425 is shown in [Figure 4-473](#) and described in [Table 4-950](#).

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Table 4-949. DDRSS_CTL_425 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06A4h

Figure 4-473. DDRSS_CTL_425 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_CALVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-950. DDRSS_CTL_425 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_CALVL_RESP	R/W	0h	Defines the DFI tCALVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_req assertion and a dfi_calvl_en assertion.

4.2.425 DDRSS_CTL_426 Register (Offset = 6A8h) [reset = 0h]

DDRSS_CTL_426 is shown in [Figure 4-474](#) and described in [Table 4-952](#).

Return to [Summary Table](#).

Table 4-951. DDRSS_CTL_426 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06A8h

Figure 4-474. DDRSS_CTL_426 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDFI_CALVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-952. DDRSS_CTL_426 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TDFI_CALVL_MAX	R/W	0h	Defines the DFI tCALVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_en assertion and a valid dfi_calvl_resp.

4.2.426 DDRSS_CTL_427 Register (Offset = 6ACh) [reset = X]

DDRSS_CTL_427 is shown in [Figure 4-475](#) and described in [Table 4-954](#).

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Table 4-953. DDRSS_CTL_427 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06ACh

Figure 4-475. DDRSS_CTL_427 Register

31	30	29	28	27	26	25	24
RESERVED					TDFI_PHY_WRDATA_F0		
R/W-X					R/W-1h		
23	22	21	20	19	18	17	16
RESERVED					CALVL_ERROR_STATUS		
R/W-X					R-0h		
15	14	13	12	11	10	9	8
RESERVED							CALVL_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							CALVL_RESP_MASK
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-954. DDRSS_CTL_427 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	TDFI_PHY_WRDATA_F0	R/W	1h	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.
23-20	RESERVED	R/W	X	
19-16	CALVL_ERROR_STATUS	R	0h	Holds the error associated with the CA training error interrupt. Bit (0) set indicates a TDFI_CALVL_MAX parameter violation, bit (1) set indicates a TDFI_CALVL_RESP parameter violation, and bit (2) set indicates that a CA leveling operation was attempted while memory was in self-refresh mode or self-refresh power-down mode. READ-ONLY
15-9	RESERVED	R/W	X	
8	CALVL_EN	R/W	0h	Enable the MC CA training module. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	CALVL_RESP_MASK	R/W	0h	Mask for the dfi_calvl_resp signal during CA training.

4.2.427 DDRSS_CTL_428 Register (Offset = 6B0h) [reset = X]

DDRSS_CTL_428 is shown in [Figure 4-476](#) and described in [Table 4-956](#).

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Table 4-955. DDRSS_CTL_428 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06B0h

Figure 4-476. DDRSS_CTL_428 Register

31	30	29	28	27	26	25	24
RESERVED	TDFI_WRCSLAT_F0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	TDFI_RDCSLAT_F0						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED					TDFI_PHY_WRDATA_F2		
R/W-X					R/W-1h		
7	6	5	4	3	2	1	0
RESERVED					TDFI_PHY_WRDATA_F1		
R/W-X					R/W-1h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-956. DDRSS_CTL_428 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	TDFI_WRCSLAT_F0	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_cs_n assertion.
23	RESERVED	R/W	X	
22-16	TDFI_RDCSLAT_F0	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a read command and a dfi_rddata_cs_n assertion.
15-11	RESERVED	R/W	X	
10-8	TDFI_PHY_WRDATA_F2	R/W	1h	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.
7-3	RESERVED	R/W	X	
2-0	TDFI_PHY_WRDATA_F1	R/W	1h	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.

4.2.428 DDRSS_CTL_429 Register (Offset = 6B4h) [reset = X]

DDRSS_CTL_429 is shown in [Figure 4-477](#) and described in [Table 4-958](#).

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Table 4-957. DDRSS_CTL_429 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06B4h

Figure 4-477. DDRSS_CTL_429 Register

31	30	29	28	27	26	25	24
RESERVED	TDFI_WRCSLAT_F2						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	TDFI_RDCSLAT_F2						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	TDFI_WRCSLAT_F1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	TDFI_RDCSLAT_F1						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-958. DDRSS_CTL_429 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	TDFI_WRCSLAT_F2	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_cs_n assertion.
23	RESERVED	R/W	X	
22-16	TDFI_RDCSLAT_F2	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a read command and a dfi_rddata_cs_n assertion.
15	RESERVED	R/W	X	
14-8	TDFI_WRCSLAT_F1	R/W	0h	Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_cs_n assertion.
7	RESERVED	R/W	X	
6-0	TDFI_RDCSLAT_F1	R/W	0h	Defines the DFI tPHY_RDCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a read command and a dfi_rddata_cs_n assertion.

4.2.429 DDRSS_CTL_430 Register (Offset = 6B8h) [reset = X]

DDRSS_CTL_430 is shown in [Figure 4-478](#) and described in [Table 4-960](#).

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Table 4-959. DDRSS_CTL_430 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06B8h

Figure 4-478. DDRSS_CTL_430 Register

31	30	29	28	27	26	25	24
RESERVED							BL_ON_FLY_ENABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							DISABLE_MEMORY_MASKED_WRITE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							EN_1T_TIMING
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
TDFI_WRDATA_DELAY							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-960. DDRSS_CTL_430 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	BL_ON_FLY_ENABLE	R/W	0h	Enables the burst length on the fly feature. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	DISABLE_MEMORY_MASKED_WRITE	R/W	0h	Restricts the controller from masked write commands. Set to 1 to not issue these commands. Only used if connected to an LPDDR4 device.
15-9	RESERVED	R/W	X	
8	EN_1T_TIMING	R/W	0h	Enable 1T timing in a system supporting both 1T and 2T timing. Set to 1 to enable.
7-0	TDFI_WRDATA_DELAY	R/W	0h	Defines the tWRDATA_DELAY timing parameter (in DFI PHY clocks), the maximum cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus.

4.2.430 DDRSS_CTL_437 Register (Offset = 6D4h) [reset = X]

DDRSS_CTL_437 is shown in [Figure 4-479](#) and described in [Table 4-962](#).

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Table 4-961. DDRSS_CTL_437 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06D4h

Figure 4-479. DDRSS_CTL_437 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GLOBAL_ERROR_INFO								RESERVED				RESERVED			
R/W-0h								R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-2h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-962. DDRSS_CTL_437 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GLOBAL_ERROR_INFO	R/W	0h	Indicates the source of DDR controller safety error interrupts. Write a 1 to a bit to clear the error.
23-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	2h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.2.431 DDRSS_CTL_438 Register (Offset = 6D8h) [reset = X]

DDRSS_CTL_438 is shown in [Figure 4-480](#) and described in [Table 4-964](#).

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Table 4-963. DDRSS_CTL_438 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06D8h

Figure 4-480. DDRSS_CTL_438 Register

31	30	29	28	27	26	25	24
NWR_F1							
R/W-28h							
23	22	21	20	19	18	17	16
NWR_F0							
R/W-28h							
15	14	13	12	11	10	9	8
RESERVED						AXI_PARITY_ERROR_STATUS	
R/W-X						R-0h	
7	6	5	4	3	2	1	0
GLOBAL_ERROR_MASK							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-964. DDRSS_CTL_438 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	NWR_F1	R/W	28h	DRAM NWR value in cycles for chip select 2.
23-16	NWR_F0	R/W	28h	DRAM NWR value in cycles for chip select 2.
15-10	RESERVED	R/W	X	
9-8	AXI_PARITY_ERROR_ST ATUS	R	0h	Specifies the source of the GLOBAL_ERROR_INFO bit (3) error. Bit (0) correlates to an overlapping write data parity error and bit (1) correlates to a write data parity error or an AXI command parity error. Value of 1 indicates that violation occurs. Both bits may be set simultaneously. READ-ONLY
7-0	GLOBAL_ERROR_MASK	R/W	0h	Mask for the DDR0_DDRSS_CONTROLLER_GLOBAL_ERROR_FATAL_0 and DDR0_DDRSS_CONTROLLER_GLOBAL_ERROR_NONFATAL_0 signals from the GLOBAL_ERROR_INFO parameter. Set each bit to 1 to mask interrupt from the output signal.

4.2.432 DDRSS_CTL_439 Register (Offset = 6DCh) [reset = X]

DDRSS_CTL_439 is shown in [Figure 4-481](#) and described in [Table 4-966](#).

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Table 4-965. DDRSS_CTL_439 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06DCh

Figure 4-481. DDRSS_CTL_439 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				REGPORT_PARAM_PARITY_PROTECTION_STATUS			
R/W-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
NWR_F2							
R/W-28h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-966. DDRSS_CTL_439 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	REGPORT_PARAM_PARITY_PROTECTION_STATUS	R	0h	Specifies the source of the GLOBAL_ERROR_INFO bit (5) error. Bit (0) correlates to an address parity error, bit (1) correlates to a write data mask parity error, bit (2) correlates to a write data parity error, bit (3) correlates to a read data parity error, and bit (4) correlates to a param register parity error. Value of 1 indicates a violation. READ-ONLY
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-0	NWR_F2	R/W	28h	DRAM NWR value in cycles for chip select 2.

4.2.433 DDRSS_CTL_440 Register (Offset = 6E0h) [reset = 0h]

DDRSS_CTL_440 is shown in [Figure 4-482](#) and described in [Table 4-968](#).

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Table 4-967. DDRSS_CTL_440 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06E0h

Figure 4-482. DDRSS_CTL_440 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC_PARITY_INJECTION_BYTE_ENABLE_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-968. DDRSS_CTL_440 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MC_PARITY_INJECTION_BYTE_ENABLE_0	R/W	0h	Enables a parity error injection on the associated byte. This parameter is a global parameter that affects all MC fault logic. To actually inject an error, the user would need to set this parameter and then set the logic injection enable parameter. Set each bit to 1 to enable the associated byte to have an error injected.

4.2.434 DDRSS_CTL_441 Register (Offset = 6E4h) [reset = 0h]

DDRSS_CTL_441 is shown in [Figure 4-483](#) and described in [Table 4-970](#).

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Table 4-969. DDRSS_CTL_441 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06E4h

Figure 4-483. DDRSS_CTL_441 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC_PARITY_INJECTION_BYTE_ENABLE_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-970. DDRSS_CTL_441 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MC_PARITY_INJECTION_BYTE_ENABLE_1	R/W	0h	Enables a parity error injection on the associated byte. This parameter is a global parameter that affects all MC fault logic. To actually inject an error, the user would need to set this parameter and then set the logic injection enable parameter. Set each bit to 1 to enable the associated byte to have an error injected.

4.2.435 DDRSS_CTL_442 Register (Offset = 6E8h) [reset = X]

DDRSS_CTL_442 is shown in [Figure 4-484](#) and described in [Table 4-972](#).

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Table 4-971. DDRSS_CTL_442 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06E8h

Figure 4-484. DDRSS_CTL_442 Register

31	30	29	28	27	26	25	24
RESERVED							REGPORT_WRITE_PARITY_PROTECTION_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							REGPORT_WRITE_MASK_PARITY_PROTECTION_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							REGPORT_ADDR_PARITY_PROTECTION_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							MC_PARITY_ERROR_TYPE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-972. DDRSS_CTL_442 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	REGPORT_WRITE_PARITY_PROTECTION_EN	R/W	0h	Enables regport write data parity checking from the regport to the param block. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	REGPORT_WRITE_MASK_PARITY_PROTECTION_EN	R/W	0h	Enables regport write data mask parity checking from the regport to the param block. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	REGPORT_ADDR_PARITY_PROTECTION_EN	R/W	0h	Enables regport address/command parity checking from the regport to the param block. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	MC_PARITY_ERROR_TYPE	R/W	0h	Defines if the parity error injected is a transient (one-time) or stuck-at (every time) error. Clear to 0 for transient or set to 1 for stuck-at.

4.2.436 DDRSS_CTL_443 Register (Offset = 6ECh) [reset = X]

DDRSS_CTL_443 is shown in [Figure 4-485](#) and described in [Table 4-974](#).

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Table 4-973. DDRSS_CTL_443 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06ECh

Figure 4-485. DDRSS_CTL_443 Register

31	30	29	28	27	26	25	24
RESERVED							REGPORT_WRITEMASK_PARITY_PROTECTION_INJECTION_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							REGPORT_ADDR_PARITY_PROTECTION_INJECTION_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PARAMREG_PARITY_PROTECTION_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							REGPORT_READ_PARITY_PROTECTION_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-974. DDRSS_CTL_443 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	REGPORT_WRITEMASK_PARITY_PROTECTION_INJECTION_EN	R/W	0h	Enables regport write mask data parity error injection from the regport to the param block. Set to 1 to enable. Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic. This parameter is only meaningful if the REGPORT_WRITEMASK_PARITY_PROTECTION_EN parameter is also set to 1.
23-17	RESERVED	R/W	X	

Table 4-974. DDRSS_CTL_443 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	REGPORT_ADDR_PARITY_PROTECTION_INJECTION_EN	R/W	0h	Enables regport address/command parity error injection from the regport to the param block. Set to 1 to enable. Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic. This parameter is only meaningful if the REGPORT_ADDR_PARITY_PROTECTION_EN parameter is also set to 1.
15-9	RESERVED	R/W	X	
8	PARAMREG_PARITY_PROTECTION_EN	R/W	0h	Enables parity checking on the param registers. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	REGPORT_READ_PARITY_PROTECTION_EN	R/W	0h	Enables regport read data parity checking from the param block to the regport. Set to 1 to enable.

4.2.437 DDRSS_CTL_444 Register (Offset = 6F0h) [reset = X]

DDRSS_CTL_444 is shown in [Figure 4-486](#) and described in [Table 4-976](#).

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Table 4-975. DDRSS_CTL_444 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06F0h

Figure 4-486. DDRSS_CTL_444 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PARAMREG_P ARITY_PROTE CTION_INJECT ION_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							REGPORT_RE AD_PARITY_P ROTECTION_I NJECTION_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							REGPORT_WR ITE_PARITY_P ROTECTION_I NJECTION_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-976. DDRSS_CTL_444 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PARAMREG_PARITY_PROTECTION_INJECTION_EN	R/W	0h	Enables parity error injection on the param registers. Set to 1 to enable. Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic. This parameter is only meaningful if the PARAMREG_PARITY_PROTECTION_EN parameter is also set to 1.
15-9	RESERVED	R/W	X	

Table 4-976. DDRSS_CTL_444 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	REGPORT_READ_PARITY_PROTECTION_INJECTION_EN	R/W	0h	<p>Enables regport read data parity error injection from the param block to the regport.</p> <p>Set to 1 to enable.</p> <p>Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic.</p> <p>This parameter is only meaningful if the REGPORT_READ_PARITY_PROTECTION_EN parameter is also set to 1.</p>
7-1	RESERVED	R/W	X	
0	REGPORT_WRITE_PARITY_PROTECTION_INJECTION_EN	R/W	0h	<p>Enables regport write data parity error injection from the regport to the param block.</p> <p>Set to 1 to enable.</p> <p>Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic.</p> <p>This parameter is only meaningful if the REGPORT_WRITE_PARITY_PROTECTION_EN parameter is also set to 1.</p>

4.2.438 DDRSS_CTL_447 Register (Offset = 6FCh) [reset = X]

DDRSS_CTL_447 is shown in [Figure 4-487](#) and described in [Table 4-978](#).

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Table 4-977. DDRSS_CTL_447 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 06FCh

Figure 4-487. DDRSS_CTL_447 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							PORT_TO_CORE_PROTECTION_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					RESERVED		
R/W-X					R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-978. DDRSS_CTL_447 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	PORT_TO_CORE_PROTECTION_EN	R/W	0h	Enables parity checking and logic replication protection from the port to the controller core. Set to 1 to enable.
7-3	RESERVED	R/W	X	
2-0	RESERVED	R	0h	Reserved

4.2.439 DDRSS_CTL_448 Register (Offset = 700h) [reset = 0h]

DDRSS_CTL_448 is shown in [Figure 4-488](#) and described in [Table 4-980](#).

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Table 4-979. DDRSS_CTL_448 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0700h

Figure 4-488. DDRSS_CTL_448 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_TO_CORE_PROTECTION_INJECTION_EN_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-980. DDRSS_CTL_448 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PORT_TO_CORE_PROTECTION_INJECTION_EN_0	R/W	0h	<p>Enables parity error injection from the port to the controller core. Set to 1 to enable.</p> <p>Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic.</p> <p>This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.</p>

4.2.440 DDRSS_CTL_449 Register (Offset = 704h) [reset = 0h]

DDRSS_CTL_449 is shown in [Figure 4-489](#) and described in [Table 4-982](#).

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Table 4-981. DDRSS_CTL_449 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0704h

Figure 4-489. DDRSS_CTL_449 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_TO_CORE_PROTECTION_INJECTION_EN_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-982. DDRSS_CTL_449 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PORT_TO_CORE_PROTECTION_INJECTION_EN_1	R/W	0h	Enables parity error injection from the port to the controller core. Set to 1 to enable. Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic. This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.

4.2.441 DDRSS_CTL_450 Register (Offset = 708h) [reset = X]

DDRSS_CTL_450 is shown in [Figure 4-490](#) and described in [Table 4-984](#).

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Table 4-983. DDRSS_CTL_450 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0708h

Figure 4-490. DDRSS_CTL_450 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					PORT_TO_CORE_PROTECTION_INJECTION_EN_2		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-984. DDRSS_CTL_450 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	PORT_TO_CORE_PROTECTION_INJECTION_EN_2	R/W	0h	Enables parity error injection from the port to the controller core. Set to 1 to enable. Only the bytes enabled in the MC_PARITY_INJECTION_BYTE_ENABLE parameter will be injected with an error on the next use of this signal/logic. This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.

4.2.442 DDRSS_CTL_455 Register (Offset = 71Ch) [reset = 0h]

DDRSS_CTL_455 is shown in [Figure 4-491](#) and described in [Table 4-986](#).

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Table 4-985. DDRSS_CTL_455 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 071Ch

Figure 4-491. DDRSS_CTL_455 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_TO_CORE_LR_ERR_INJ_EN_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-986. DDRSS_CTL_455 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PORT_TO_CORE_LR_ERR_INJ_EN_0	R/W	0h	Enables error injection from the port to the controller core. Set to 1 to enable. This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.

4.2.443 DDRSS_CTL_456 Register (Offset = 720h) [reset = 0h]

DDRSS_CTL_456 is shown in [Figure 4-492](#) and described in [Table 4-988](#).

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Table 4-987. DDRSS_CTL_456 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0720h

Figure 4-492. DDRSS_CTL_456 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_TO_CORE_LR_ERR_INJ_EN_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-988. DDRSS_CTL_456 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PORT_TO_CORE_LR_ERR_INJ_EN_1	R/W	0h	Enables error injection from the port to the controller core. Set to 1 to enable. This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.

4.2.444 DDRSS_CTL_457 Register (Offset = 724h) [reset = 0h]

DDRSS_CTL_457 is shown in [Figure 4-493](#) and described in [Table 4-990](#).

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Table 4-989. DDRSS_CTL_457 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0724h

Figure 4-493. DDRSS_CTL_457 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PORT_TO_CORE_LR_ERR_INJ_EN_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-990. DDRSS_CTL_457 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PORT_TO_CORE_LR_ERR_INJ_EN_2	R/W	0h	Enables error injection from the port to the controller core. Set to 1 to enable. This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.

4.2.445 DDRSS_CTL_458 Register (Offset = 728h) [reset = X]

DDRSS_CTL_458 is shown in [Figure 4-494](#) and described in [Table 4-992](#).

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Table 4-991. DDRSS_CTL_458 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG	0299 0728h

Figure 4-494. DDRSS_CTL_458 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PORT_TO_CORE_LR_ERR_INJ_EN_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-992. DDRSS_CTL_458 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PORT_TO_CORE_LR_ERR_INJ_EN_3	R/W	0h	Enables error injection from the port to the controller core. Set to 1 to enable. This parameter is only meaningful if the PORT_TO_CORE_PROTECTION_EN parameter is also set to 1.

4.3 PI Registers

Table 4-994 lists the memory-mapped registers for the PI. All register offset addresses not listed in Table 4-994 should be considered as reserved locations and the register contents should not be modified.

Table 4-993. PI Instances

Instance	Base Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 0000h

Table 4-994. PI Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PI Physical Address
2000h	DDRSS_PI_0	PI Register 0	0299 2000h
2004h	DDRSS_PI_1	PI Register 1	0299 2004h
2008h	DDRSS_PI_2	PI Register 2	0299 2008h
200Ch	DDRSS_PI_3	PI Register 3	0299 200Ch
2010h	DDRSS_PI_4	PI Register 4	0299 2010h
2014h	DDRSS_PI_5	PI Register 5	0299 2014h
2018h	DDRSS_PI_6	PI Register 6	0299 2018h
201Ch	DDRSS_PI_7	PI Register 7	0299 201Ch
2020h	DDRSS_PI_8	PI Register 8	0299 2020h
2024h	DDRSS_PI_9	PI Register 9	0299 2024h
2028h	DDRSS_PI_10	PI Register 10	0299 2028h
202Ch	DDRSS_PI_11	PI Register 11	0299 202Ch
2030h	DDRSS_PI_12	PI Register 12	0299 2030h
2034h	DDRSS_PI_13	PI Register 13	0299 2034h
2038h	DDRSS_PI_14	PI Register 14	0299 2038h
203Ch	DDRSS_PI_15	PI Register 15	0299 203Ch
2040h	DDRSS_PI_16	PI Register 16	0299 2040h
2044h	DDRSS_PI_17	PI Register 17	0299 2044h
2048h	DDRSS_PI_18	PI Register 18	0299 2048h
204Ch	DDRSS_PI_19	PI Register 19	0299 204Ch
2050h	DDRSS_PI_20	PI Register 20	0299 2050h
2054h	DDRSS_PI_21	PI Register 21	0299 2054h
2058h	DDRSS_PI_22	PI Register 22	0299 2058h
205Ch	DDRSS_PI_23	PI Register 23	0299 205Ch
2060h	DDRSS_PI_24	PI Register 24	0299 2060h
2064h	DDRSS_PI_25	PI Register 25	0299 2064h
2068h	DDRSS_PI_26	PI Register 26	0299 2068h
206Ch	DDRSS_PI_27	PI Register 27	0299 206Ch
2070h	DDRSS_PI_28	PI Register 28	0299 2070h
2074h	DDRSS_PI_29	PI Register 29	0299 2074h
2078h	DDRSS_PI_30	PI Register 30	0299 2078h
207Ch	DDRSS_PI_31	PI Register 31	0299 207Ch
2080h	DDRSS_PI_32	PI Register 32	0299 2080h
2084h	DDRSS_PI_33	PI Register 33	0299 2084h
2088h	DDRSS_PI_34	PI Register 34	0299 2088h
208Ch	DDRSS_PI_35	PI Register 35	0299 208Ch
2090h	DDRSS_PI_36	PI Register 36	0299 2090h
2094h	DDRSS_PI_37	PI Register 37	0299 2094h

Table 4-994. PI Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PI Physical Address
2098h	DDRSS_PI_38	PI Register 38	0299 2098h
209Ch	DDRSS_PI_39	PI Register 39	0299 209Ch
20A0h	DDRSS_PI_40	PI Register 40	0299 20A0h
20A4h	DDRSS_PI_41	PI Register 41	0299 20A4h
20A8h	DDRSS_PI_42	PI Register 42	0299 20A8h
20ACh	DDRSS_PI_43	PI Register 43	0299 20ACh
20B0h	DDRSS_PI_44	PI Register 44	0299 20B0h
20B4h	DDRSS_PI_45	PI Register 45	0299 20B4h
20B8h	DDRSS_PI_46	PI Register 46	0299 20B8h
20BCh	DDRSS_PI_47	PI Register 47	0299 20BCh
20C0h	DDRSS_PI_48	PI Register 48	0299 20C0h
20C4h	DDRSS_PI_49	PI Register 49	0299 20C4h
20C8h	DDRSS_PI_50	PI Register 50	0299 20C8h
20CCh	DDRSS_PI_51	PI Register 51	0299 20CCh
20D0h	DDRSS_PI_52	PI Register 52	0299 20D0h
20D4h	DDRSS_PI_53	PI Register 53	0299 20D4h
20D8h	DDRSS_PI_54	PI Register 54	0299 20D8h
20DCh	DDRSS_PI_55	PI Register 55	0299 20DCh
20E0h	DDRSS_PI_56	PI Register 56	0299 20E0h
20E4h	DDRSS_PI_57	PI Register 57	0299 20E4h
20E8h	DDRSS_PI_58	PI Register 58	0299 20E8h
20ECh	DDRSS_PI_59	PI Register 59	0299 20ECh
20F0h	DDRSS_PI_60	PI Register 60	0299 20F0h
20F4h	DDRSS_PI_61	PI Register 61	0299 20F4h
20F8h	DDRSS_PI_62	PI Register 62	0299 20F8h
20FCh	DDRSS_PI_63	PI Register 63	0299 20FCh
2100h	DDRSS_PI_64	PI Register 64	0299 2100h
2104h	DDRSS_PI_65	PI Register 65	0299 2104h
2108h	DDRSS_PI_66	PI Register 66	0299 2108h
210Ch	DDRSS_PI_67	PI Register 67	0299 210Ch
2110h	DDRSS_PI_68	PI Register 68	0299 2110h
2114h	DDRSS_PI_69	PI Register 69	0299 2114h
2118h	DDRSS_PI_70	PI Register 70	0299 2118h
211Ch	DDRSS_PI_71	PI Register 71	0299 211Ch
2120h	DDRSS_PI_72	PI Register 72	0299 2120h
2124h	DDRSS_PI_73	PI Register 73	0299 2124h
2128h	DDRSS_PI_74	PI Register 74	0299 2128h
212Ch	DDRSS_PI_75	PI Register 75	0299 212Ch
2130h	DDRSS_PI_76	PI Register 76	0299 2130h
2134h	DDRSS_PI_77	PI Register 77	0299 2134h
2138h	DDRSS_PI_78	PI Register 78	0299 2138h
213Ch	DDRSS_PI_79	PI Register 79	0299 213Ch
2140h	DDRSS_PI_80	PI Register 80	0299 2140h
2144h	DDRSS_PI_81	PI Register 81	0299 2144h
2148h	DDRSS_PI_82	PI Register 82	0299 2148h

Table 4-994. PI Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PI Physical Address
214Ch	DDRSS_PI_83	PI Register 83	0299 214Ch
2150h	DDRSS_PI_84	PI Register 84	0299 2150h
2154h	DDRSS_PI_85	PI Register 85	0299 2154h
2158h	DDRSS_PI_86	PI Register 86	0299 2158h
215Ch	DDRSS_PI_87	PI Register 87	0299 215Ch
2160h	DDRSS_PI_88	PI Register 88	0299 2160h
2164h	DDRSS_PI_89	PI Register 89	0299 2164h
2168h	DDRSS_PI_90	PI Register 90	0299 2168h
216Ch	DDRSS_PI_91	PI Register 91	0299 216Ch
2170h	DDRSS_PI_92	PI Register 92	0299 2170h
2174h	DDRSS_PI_93	PI Register 93	0299 2174h
2178h	DDRSS_PI_94	PI Register 94	0299 2178h
217Ch	DDRSS_PI_95	PI Register 95	0299 217Ch
2180h	DDRSS_PI_96	PI Register 96	0299 2180h
2184h	DDRSS_PI_97	PI Register 97	0299 2184h
2188h	DDRSS_PI_98	PI Register 98	0299 2188h
218Ch	DDRSS_PI_99	PI Register 99	0299 218Ch
2190h	DDRSS_PI_100	PI Register 100	0299 2190h
2194h	DDRSS_PI_101	PI Register 101	0299 2194h
2198h	DDRSS_PI_102	PI Register 102	0299 2198h
219Ch	DDRSS_PI_103	PI Register 103	0299 219Ch
21A0h	DDRSS_PI_104	PI Register 104	0299 21A0h
21A4h	DDRSS_PI_105	PI Register 105	0299 21A4h
21A8h	DDRSS_PI_106	PI Register 106	0299 21A8h
21ACh	DDRSS_PI_107	PI Register 107	0299 21ACh
21B0h	DDRSS_PI_108	PI Register 108	0299 21B0h
21B4h	DDRSS_PI_109	PI Register 109	0299 21B4h
21B8h	DDRSS_PI_110	PI Register 110	0299 21B8h
21BCh	DDRSS_PI_111	PI Register 111	0299 21BCh
21C0h	DDRSS_PI_112	PI Register 112	0299 21C0h
21C4h	DDRSS_PI_113	PI Register 113	0299 21C4h
21C8h	DDRSS_PI_114	PI Register 114	0299 21C8h
21CCh	DDRSS_PI_115	PI Register 115	0299 21CCh
21D0h	DDRSS_PI_116	PI Register 116	0299 21D0h
21D4h	DDRSS_PI_117	PI Register 117	0299 21D4h
21D8h	DDRSS_PI_118	PI Register 118	0299 21D8h
21DCh	DDRSS_PI_119	PI Register 119	0299 21DCh
21E0h	DDRSS_PI_120	PI Register 120	0299 21E0h
21E4h	DDRSS_PI_121	PI Register 121	0299 21E4h
21E8h	DDRSS_PI_122	PI Register 122	0299 21E8h
21ECh	DDRSS_PI_123	PI Register 123	0299 21ECh
21F0h	DDRSS_PI_124	PI Register 124	0299 21F0h
21F4h	DDRSS_PI_125	PI Register 125	0299 21F4h
21F8h	DDRSS_PI_126	PI Register 126	0299 21F8h
21FCh	DDRSS_PI_127	PI Register 127	0299 21FCh

Table 4-994. PI Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PI Physical Address
2200h	DDRSS_PI_128	PI Register 128	0299 2200h
2204h	DDRSS_PI_129	PI Register 129	0299 2204h
2208h	DDRSS_PI_130	PI Register 130	0299 2208h
220Ch	DDRSS_PI_131	PI Register 131	0299 220Ch
2210h	DDRSS_PI_132	PI Register 132	0299 2210h
2214h	DDRSS_PI_133	PI Register 133	0299 2214h
2218h	DDRSS_PI_134	PI Register 134	0299 2218h
221Ch	DDRSS_PI_135	PI Register 135	0299 221Ch
2220h	DDRSS_PI_136	PI Register 136	0299 2220h
2224h	DDRSS_PI_137	PI Register 137	0299 2224h
2228h	DDRSS_PI_138	PI Register 138	0299 2228h
222Ch	DDRSS_PI_139	PI Register 139	0299 222Ch
2230h	DDRSS_PI_140	PI Register 140	0299 2230h
2234h	DDRSS_PI_141	PI Register 141	0299 2234h
2238h	DDRSS_PI_142	PI Register 142	0299 2238h
223Ch	DDRSS_PI_143	PI Register 143	0299 223Ch
2240h	DDRSS_PI_144	PI Register 144	0299 2240h
2244h	DDRSS_PI_145	PI Register 145	0299 2244h
2248h	DDRSS_PI_146	PI Register 146	0299 2248h
224Ch	DDRSS_PI_147	PI Register 147	0299 224Ch
2250h	DDRSS_PI_148	PI Register 148	0299 2250h
2254h	DDRSS_PI_149	PI Register 149	0299 2254h
2258h	DDRSS_PI_150	PI Register 150	0299 2258h
225Ch	DDRSS_PI_151	PI Register 151	0299 225Ch
2260h	DDRSS_PI_152	PI Register 152	0299 2260h
2264h	DDRSS_PI_153	PI Register 153	0299 2264h
2268h	DDRSS_PI_154	PI Register 154	0299 2268h
226Ch	DDRSS_PI_155	PI Register 155	0299 226Ch
2270h	DDRSS_PI_156	PI Register 156	0299 2270h
2274h	DDRSS_PI_157	PI Register 157	0299 2274h
2278h	DDRSS_PI_158	PI Register 158	0299 2278h
227Ch	DDRSS_PI_159	PI Register 159	0299 227Ch
2280h	DDRSS_PI_160	PI Register 160	0299 2280h
2284h	DDRSS_PI_161	PI Register 161	0299 2284h
2288h	DDRSS_PI_162	PI Register 162	0299 2288h
228Ch	DDRSS_PI_163	PI Register 163	0299 228Ch
2290h	DDRSS_PI_164	PI Register 164	0299 2290h
2294h	DDRSS_PI_165	PI Register 165	0299 2294h
2298h	DDRSS_PI_166	PI Register 166	0299 2298h
229Ch	DDRSS_PI_167	PI Register 167	0299 229Ch
22A0h	DDRSS_PI_168	PI Register 168	0299 22A0h
22A4h	DDRSS_PI_169	PI Register 169	0299 22A4h
22A8h	DDRSS_PI_170	PI Register 170	0299 22A8h
22ACh	DDRSS_PI_171	PI Register 171	0299 22ACh
22B0h	DDRSS_PI_172	PI Register 172	0299 22B0h

Table 4-994. PI Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PI Physical Address
22B4h	DDRSS_PI_173	PI Register 173	0299 22B4h
22B8h	DDRSS_PI_174	PI Register 174	0299 22B8h
22BCh	DDRSS_PI_175	PI Register 175	0299 22BCh
22C0h	DDRSS_PI_176	PI Register 176	0299 22C0h
22C4h	DDRSS_PI_177	PI Register 177	0299 22C4h
22C8h	DDRSS_PI_178	PI Register 178	0299 22C8h
22CCh	DDRSS_PI_179	PI Register 179	0299 22CCh
22D0h	DDRSS_PI_180	PI Register 180	0299 22D0h
22D4h	DDRSS_PI_181	PI Register 181	0299 22D4h
22D8h	DDRSS_PI_182	PI Register 182	0299 22D8h
22DCh	DDRSS_PI_183	PI Register 183	0299 22DCh
22E0h	DDRSS_PI_184	PI Register 184	0299 22E0h
22E4h	DDRSS_PI_185	PI Register 185	0299 22E4h
22E8h	DDRSS_PI_186	PI Register 186	0299 22E8h
22ECh	DDRSS_PI_187	PI Register 187	0299 22ECh
22F0h	DDRSS_PI_188	PI Register 188	0299 22F0h
22F4h	DDRSS_PI_189	PI Register 189	0299 22F4h
22F8h	DDRSS_PI_190	PI Register 190	0299 22F8h
22FCh	DDRSS_PI_191	PI Register 191	0299 22FCh
2300h	DDRSS_PI_192	PI Register 192	0299 2300h
2304h	DDRSS_PI_193	PI Register 193	0299 2304h
2308h	DDRSS_PI_194	PI Register 194	0299 2308h
230Ch	DDRSS_PI_195	PI Register 195	0299 230Ch
2310h	DDRSS_PI_196	PI Register 196	0299 2310h
2314h	DDRSS_PI_197	PI Register 197	0299 2314h
2318h	DDRSS_PI_198	PI Register 198	0299 2318h
231Ch	DDRSS_PI_199	PI Register 199	0299 231Ch
2320h	DDRSS_PI_200	PI Register 200	0299 2320h
2324h	DDRSS_PI_201	PI Register 201	0299 2324h
2328h	DDRSS_PI_202	PI Register 202	0299 2328h
232Ch	DDRSS_PI_203	PI Register 203	0299 232Ch
2330h	DDRSS_PI_204	PI Register 204	0299 2330h
2334h	DDRSS_PI_205	PI Register 205	0299 2334h
2338h	DDRSS_PI_206	PI Register 206	0299 2338h
233Ch	DDRSS_PI_207	PI Register 207	0299 233Ch
2340h	DDRSS_PI_208	PI Register 208	0299 2340h
2344h	DDRSS_PI_209	PI Register 209	0299 2344h
2348h	DDRSS_PI_210	PI Register 210	0299 2348h
234Ch	DDRSS_PI_211	PI Register 211	0299 234Ch
2350h	DDRSS_PI_212	PI Register 212	0299 2350h
2354h	DDRSS_PI_213	PI Register 213	0299 2354h
2358h	DDRSS_PI_214	PI Register 214	0299 2358h
235Ch	DDRSS_PI_215	PI Register 215	0299 235Ch
2360h	DDRSS_PI_216	PI Register 216	0299 2360h
2364h	DDRSS_PI_217	PI Register 217	0299 2364h

Table 4-994. PI Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PI Physical Address
2368h	DDRSS_PI_218	PI Register 218	0299 2368h
236Ch	DDRSS_PI_219	PI Register 219	0299 236Ch
2370h	DDRSS_PI_220	PI Register 220	0299 2370h
2374h	DDRSS_PI_221	PI Register 221	0299 2374h
2378h	DDRSS_PI_222	PI Register 222	0299 2378h
237Ch	DDRSS_PI_223	PI Register 223	0299 237Ch
2380h	DDRSS_PI_224	PI Register 224	0299 2380h
2384h	DDRSS_PI_225	PI Register 225	0299 2384h
2388h	DDRSS_PI_226	PI Register 226	0299 2388h
238Ch	DDRSS_PI_227	PI Register 227	0299 238Ch
2390h	DDRSS_PI_228	PI Register 228	0299 2390h
2394h	DDRSS_PI_229	PI Register 229	0299 2394h
2398h	DDRSS_PI_230	PI Register 230	0299 2398h
239Ch	DDRSS_PI_231	PI Register 231	0299 239Ch
23A0h	DDRSS_PI_232	PI Register 232	0299 23A0h
23A4h	DDRSS_PI_233	PI Register 233	0299 23A4h
23A8h	DDRSS_PI_234	PI Register 234	0299 23A8h
23ACh	DDRSS_PI_235	PI Register 235	0299 23ACh
23B0h	DDRSS_PI_236	PI Register 236	0299 23B0h
23B4h	DDRSS_PI_237	PI Register 237	0299 23B4h
23B8h	DDRSS_PI_238	PI Register 238	0299 23B8h
23BCh	DDRSS_PI_239	PI Register 239	0299 23BCh
23C0h	DDRSS_PI_240	PI Register 240	0299 23C0h
23C4h	DDRSS_PI_241	PI Register 241	0299 23C4h
23C8h	DDRSS_PI_242	PI Register 242	0299 23C8h
23CCh	DDRSS_PI_243	PI Register 243	0299 23CCh
23D0h	DDRSS_PI_244	PI Register 244	0299 23D0h
23D4h	DDRSS_PI_245	PI Register 245	0299 23D4h
23D8h	DDRSS_PI_246	PI Register 246	0299 23D8h
23DCh	DDRSS_PI_247	PI Register 247	0299 23DCh
23E0h	DDRSS_PI_248	PI Register 248	0299 23E0h
23E4h	DDRSS_PI_249	PI Register 249	0299 23E4h
23E8h	DDRSS_PI_250	PI Register 250	0299 23E8h
23ECh	DDRSS_PI_251	PI Register 251	0299 23ECh
23F0h	DDRSS_PI_252	PI Register 252	0299 23F0h
23F4h	DDRSS_PI_253	PI Register 253	0299 23F4h
23F8h	DDRSS_PI_254	PI Register 254	0299 23F8h
23FCh	DDRSS_PI_255	PI Register 255	0299 23FCh
2400h	DDRSS_PI_256	PI Register 256	0299 2400h
2404h	DDRSS_PI_257	PI Register 257	0299 2404h
2408h	DDRSS_PI_258	PI Register 258	0299 2408h
240Ch	DDRSS_PI_259	PI Register 259	0299 240Ch
2410h	DDRSS_PI_260	PI Register 260	0299 2410h
2414h	DDRSS_PI_261	PI Register 261	0299 2414h
2418h	DDRSS_PI_262	PI Register 262	0299 2418h

Table 4-994. PI Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PI Physical Address
241Ch	DDRSS_PI_263	PI Register 263	0299 241Ch
2420h	DDRSS_PI_264	PI Register 264	0299 2420h
2424h	DDRSS_PI_265	PI Register 265	0299 2424h
2428h	DDRSS_PI_266	PI Register 266	0299 2428h
242Ch	DDRSS_PI_267	PI Register 267	0299 242Ch
2430h	DDRSS_PI_268	PI Register 268	0299 2430h
2434h	DDRSS_PI_269	PI Register 269	0299 2434h
2438h	DDRSS_PI_270	PI Register 270	0299 2438h
243Ch	DDRSS_PI_271	PI Register 271	0299 243Ch
2440h	DDRSS_PI_272	PI Register 272	0299 2440h
2444h	DDRSS_PI_273	PI Register 273	0299 2444h
2448h	DDRSS_PI_274	PI Register 274	0299 2448h
244Ch	DDRSS_PI_275	PI Register 275	0299 244Ch
2450h	DDRSS_PI_276	PI Register 276	0299 2450h
2454h	DDRSS_PI_277	PI Register 277	0299 2454h
2458h	DDRSS_PI_278	PI Register 278	0299 2458h
245Ch	DDRSS_PI_279	PI Register 279	0299 245Ch
2460h	DDRSS_PI_280	PI Register 280	0299 2460h
2464h	DDRSS_PI_281	PI Register 281	0299 2464h
2468h	DDRSS_PI_282	PI Register 282	0299 2468h
246Ch	DDRSS_PI_283	PI Register 283	0299 246Ch
2470h	DDRSS_PI_284	PI Register 284	0299 2470h
2474h	DDRSS_PI_285	PI Register 285	0299 2474h
2478h	DDRSS_PI_286	PI Register 286	0299 2478h
247Ch	DDRSS_PI_287	PI Register 287	0299 247Ch
2480h	DDRSS_PI_288	PI Register 288	0299 2480h
2484h	DDRSS_PI_289	PI Register 289	0299 2484h
2488h	DDRSS_PI_290	PI Register 290	0299 2488h
248Ch	DDRSS_PI_291	PI Register 291	0299 248Ch
2490h	DDRSS_PI_292	PI Register 292	0299 2490h
2494h	DDRSS_PI_293	PI Register 293	0299 2494h
2498h	DDRSS_PI_294	PI Register 294	0299 2498h
249Ch	DDRSS_PI_295	PI Register 295	0299 249Ch
24A0h	DDRSS_PI_296	PI Register 296	0299 24A0h
24A4h	DDRSS_PI_297	PI Register 297	0299 24A4h
24A8h	DDRSS_PI_298	PI Register 298	0299 24A8h
24ACh	DDRSS_PI_299	PI Register 299	0299 24ACh

4.3.1 DDRSS_PI_0 Register (Offset = 2000h) [reset = X]

DDRSS_PI_0 is shown in [Figure 4-495](#) and described in [Table 4-996](#).

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Table 4-995. DDRSS_PI_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2000h

Figure 4-495. DDRSS_PI_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				PI_DRAM_CLASS			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PI_START
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-996. DDRSS_PI_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-8	PI_DRAM_CLASS	R/W	0h	Defines the memory class for the PI. Bh - LPDDR4 All other values reserved
7-1	RESERVED	R/W	X	
0	PI_START	R/W	0h	Initiate command processing in the PI. Set to 1 to initiate.

4.3.2 DDRSS_PI_1 Register (Offset = 2004h) [reset = CB1E3F21h]

DDRSS_PI_1 is shown in [Figure 4-496](#) and described in [Table 4-998](#).

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Table 4-997. DDRSS_PI_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2004h

Figure 4-496. DDRSS_PI_1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_VERSION_0																															
R-CB1E3F21h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-998. DDRSS_PI_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_VERSION_0	R	CB1E3F21h	Holds the PI version number. This is a unique number for each PHY IP delivery. This will help in identifying different version of the PHY IP. READ-ONLY

4.3.3 DDRSS_PI_2 Register (Offset = 2008h) [reset = 078D9209h]

DDRSS_PI_2 is shown in [Figure 4-497](#) and described in [Table 4-1000](#).

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Table 4-999. DDRSS_PI_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2008h

Figure 4-497. DDRSS_PI_2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_VERSION_1																															
R-078D9209h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1000. DDRSS_PI_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_VERSION_1	R	078D9209h	Holds the PI version number. This is a unique number for each PHY IP delivery. This will help in identifying different version of the PHY IP. READ-ONLY

4.3.4 DDRSS_PI_3 Register (Offset = 200Ch) [reset = X]

DDRSS_PI_3 is shown in [Figure 4-498](#) and described in [Table 4-1002](#).

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Table 4-1001. DDRSS_PI_3 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 200Ch

Figure 4-498. DDRSS_PI_3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PI_ID															
R-X																R-1387h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1002. DDRSS_PI_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	PI_ID	R	1387h	Holds the PI ID number. This is a DDR PHY IP identifier. It is set to 0x1387. READ-ONLY

4.3.5 DDRSS_PI_4 Register (Offset = 2010h) [reset = 0h]

DDRSS_PI_4 is shown in [Figure 4-499](#) and described in [Table 4-1004](#).

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Table 4-1003. DDRSS_PI_4 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2010h

Figure 4-499. DDRSS_PI_4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_UNUSED_REG_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1004. DDRSS_PI_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_UNUSED_REG_0	R	0h	Unused register

4.3.6 DDRSS_PI_5 Register (Offset = 2014h) [reset = X]

DDRSS_PI_5 is shown in [Figure 4-500](#) and described in [Table 4-1006](#).

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Table 4-1005. DDRSS_PI_5 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2014h

Figure 4-500. DDRSS_PI_5 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PI_NOTCARE_PHYUPD
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_INIT_LVL_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_NORMAL_LVL_SEQ
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1006. DDRSS_PI_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PI_NOTCARE_PHYUPD	R/W	0h	Allow the PI to issue a master request to the controller if a phyupd_req from the PHY has been detected. Set to 1 to issue the master request.
15-9	RESERVED	R/W	X	
8	PI_INIT_LVL_EN	R/W	0h	Enables the initial leveling sequence after PI initialization procedure. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	PI_NORMAL_LVL_SEQ	R/W	0h	Enable the PI to finish all the pending leveling before releasing the DFI bus.

4.3.7 DDRSS_PI_6 Register (Offset = 2018h) [reset = X]

DDRSS_PI_6 is shown in [Figure 4-501](#) and described in [Table 4-1008](#).

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Table 4-1007. DDRSS_PI_6 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2018h

Figure 4-501. DDRSS_PI_6 Register

31	30	29	28	27	26	25	24
RESERVED							PI_TRAIN_ALL_FREQ_REQ
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							
R/W-64h							
15	14	13	12	11	10	9	8
PI_TCMD_GAP							
R/W-0h							
7	6	5	4	3	2	1	0
PI_TCMD_GAP							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1008. DDRSS_PI_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_TRAIN_ALL_FREQ_REQ	W	0h	Triggers training for all supported frequencies in PI_FREQ_MAP. Applies to LPDDR4 devices onlyh. Set to 1 to trigger. Only applicable after memory initialization has been completed. Can be used to train new frequencies that were not available at initialization time. WRITE-ONLY
23-16	RESERVED	R/W	64h	Reserved
15-0	PI_TCMD_GAP	R/W	0h	Specifies the minimum gap in DFI clocks between two commands. Used to guard the timing from the last command of MC and the first command of PI when MC hand over the control of DFI to PI.

4.3.8 DDRSS_PI_7 Register (Offset = 201Ch) [reset = X]

DDRSS_PI_7 is shown in [Figure 4-502](#) and described in [Table 4-1010](#).

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Table 4-1009. DDRSS_PI_7 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 201Ch

Figure 4-502. DDRSS_PI_7 Register

31	30	29	28	27	26	25	24
RESERVED							PI_DFI_PHYMS TR_STATE_SE L_R
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_DFI_PHYMS TR_CS_STATE _R
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PI_DFI_PHYMSTR_TYPE	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PI_DFI_VERSI ON
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1010. DDRSS_PI_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_DFI_PHYMSTR_STAT E_SEL_R	R/W	0h	DFI PHY Master State Select: Indication from the PHY to the MC whether the requested memory state is IDLE or Self refresh. 'b 0: indicates that the corresponding CS must be put into the IDLE state. 'b 1: indicates that the corresponding CS must be put into the Self refresh state.
23-17	RESERVED	R/W	X	
16	PI_DFI_PHYMSTR_CS_S TATE_R	R/W	0h	This signal indicates the state of the DRAM when the PHY becomes the master. 'b 0: The PHY specifies the required state, using the dfi_phymstr_state_sel signal. 'b 1: is reserved.
15-10	RESERVED	R/W	X	

Table 4-1010. DDRSS_PI_7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9-8	PI_DFI_PHYMSTR_TYPE	R/W	0h	DFI Master Request Type used for dfi 4.1 version: This signal indicates the required state of DRAM when PHY becomes the master. Each memory rank uses one bit. 1'b 0: IDLE. The MC should close all the pages. 1'b 1: IDLE or Self Refresh.
7-1	RESERVED	R/W	X	
0	PI_DFI_VERSION	R/W	0h	Define the DFI master version, set 1 for DFI4.1, set 0 for DFI4.0

4.3.9 DDRSS_PI_8 Register (Offset = 2020h) [reset = 0h]

DDRSS_PI_8 is shown in [Figure 4-503](#) and described in [Table 4-1012](#).

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Table 4-1011. DDRSS_PI_8 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2020h

Figure 4-503. DDRSS_PI_8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_PHYMSTR_MAX																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1012. DDRSS_PI_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_PHYMSTR_MAX	R	0h	Indicates the maximum number of DFI clock cycles registered while the dfi_phymstr_req signal is asserted and the dfi_phymstr_ack signal is asserted. READ-ONLY.

4.3.10 DDRSS_PI_9 Register (Offset = 2024h) [reset = X]

DDRSS_PI_9 is shown in [Figure 4-504](#) and described in [Table 4-1014](#).

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Table 4-1013. DDRSS_PI_9 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2024h

Figure 4-504. DDRSS_PI_9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PI_TDFI_PHYMSTR_RESP																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 4-1014. DDRSS_PI_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-0	PI_TDFI_PHYMSTR_RESP	R	0h	Indicates the maximum number of DFI clock cycles registered between a dfi_phymstr_req signal assertion and a dfi_phymstr_ack signal assertion. READ-ONLY

4.3.11 DDRSS_PI_10 Register (Offset = 2028h) [reset = X]

DDRSS_PI_10 is shown in [Figure 4-505](#) and described in [Table 4-1016](#).

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Table 4-1015. DDRSS_PI_10 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2028h

Figure 4-505. DDRSS_PI_10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PI_TDFI_PHYUPD_RESP																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 4-1016. DDRSS_PI_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-0	PI_TDFI_PHYUPD_RESP	R	0h	Indicates the maximum number of DFI clock cycles registered between a dfi_phyupd_req signal assertion and a dfi_phyupd_ack signal assertion. READ-ONLY.

4.3.12 DDRSS_PI_11 Register (Offset = 202Ch) [reset = 0h]

DDRSS_PI_11 is shown in [Figure 4-506](#) and described in [Table 4-1018](#).

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Table 4-1017. DDRSS_PI_11 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 202Ch

Figure 4-506. DDRSS_PI_11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_PHYUPD_MAX																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1018. DDRSS_PI_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_PHYUPD_MAX	R	0h	Indicates the maximum number of DFI clock cycles registered while the dfi_phyupd_req signal is asserted and the dfi_phy_ack signal is asserted. READ-ONLY.

4.3.13 DDRSS_PI_12 Register (Offset = 2030h) [reset = 0h]

DDRSS_PI_12 is shown in [Figure 4-507](#) and described in [Table 4-1020](#).

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Table 4-1019. DDRSS_PI_12 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2030h

Figure 4-507. DDRSS_PI_12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_FREQ_MAP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1020. DDRSS_PI_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_FREQ_MAP	R/W	0h	Frequency map for supported working frequencies. Each bit represents one supported frequency.

4.3.14 DDRSS_PI_13 Register (Offset = 2034h) [reset = X]

DDRSS_PI_13 is shown in [Figure 4-508](#) and described in [Table 4-1022](#).

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Table 4-1021. DDRSS_PI_13 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2034h

Figure 4-508. DDRSS_PI_13 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_SW_RST_N
R/W-X							R/W-1h
15	14	13	12	11	10	9	8
RESERVED							PI_INIT_DFS_C ALVL_ONLY
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED			PI_INIT_WORK_FREQ				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1022. DDRSS_PI_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	PI_SW_RST_N	R/W	1h	User request to reset the whole PI except the parameter modules. Set 0 to reset, set to 1 to release.
15-9	RESERVED	R/W	X	
8	PI_INIT_DFS_CALVL_ONLY	R/W	0h	Enables frequency training for CA leveling only. Other trainings are not performed.
7-5	RESERVED	R/W	X	
4-0	PI_INIT_WORK_FREQ	R/W	0h	Indicates the initial work frequency after initialization and initial leveling sequence.

4.3.15 DDRSS_PI_14 Register (Offset = 2038h) [reset = X]

DDRSS_PI_14 is shown in [Figure 4-509](#) and described in [Table 4-1024](#).

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Table 4-1023. DDRSS_PI_14 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2038h

Figure 4-509. DDRSS_PI_14 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TMRR			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PI_SRX_LVL_T ARGET_CS_E N
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PI_RANK_NUM_PER_CKE			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_CS_MAP			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1024. DDRSS_PI_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_TMRR	R/W	0h	DRAM tMRR value in memory clock cycles.
23-17	RESERVED	R/W	X	
16	PI_SRX_LVL_TARGET_CS_EN	R/W	0h	Defines self refresh exit trigger target rank/ranks training or all ranks training. 1: The rank/ranks exit from self refresh will trigger the corresponding rank/ranks training. Note: If multiple ranks exit from self refresh, current design only support the multiple ranks srx command issues at the same time. 0: Any rank/ranks exit from self refresh will trigger all ranks training
15-13	RESERVED	R/W	X	
12-8	PI_RANK_NUM_PER_CKE	R/W	0h	Defines the number of chip selects share one cke
7-4	RESERVED	R/W	X	
3-0	PI_CS_MAP	R/W	0h	Defines which chip selects are active.

4.3.16 DDRSS_PI_15 Register (Offset = 203Ch) [reset = X]

DDRSS_PI_15 is shown in [Figure 4-510](#) and described in [Table 4-1026](#).

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Table 4-1025. DDRSS_PI_15 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 203Ch

Figure 4-510. DDRSS_PI_15 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						RESERVED	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_MCAREF_FORWARD_ONLY	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_PREAMBLE_SUPPORT	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1026. DDRSS_PI_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	PI_MCAREF_FORWARD_ONLY	R/W	0h	Controls the generation of AREF from the PI module or forward the MC received value.
7-2	RESERVED	R/W	X	
1-0	PI_PREAMBLE_SUPPORT	R/W	0h	Defines the read and write preamble length. bit 0: Selection of one or two cycle preamble for read burst transfers. bit 1: Selection of one or two cycles write burst transfers for NON-DDR5, one or multi(up to four) cycles write burst transfers for DDR5.

4.3.17 DDRSS_PI_16 Register (Offset = 2040h) [reset = X]

DDRSS_PI_16 is shown in [Figure 4-511](#) and described in [Table 4-1028](#).

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Table 4-1027. DDRSS_PI_16 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2040h

Figure 4-511. DDRSS_PI_16 Register

31	30	29	28	27	26	25	24
RESERVED							PI_ON_DFIBUS
R/W-X							R-0h
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_INTERVAL			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_TREF_INTERVAL							
R/W-0h							
7	6	5	4	3	2	1	0
PI_TREF_INTERVAL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1028. DDRSS_PI_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_ON_DFIBUS	R	0h	Monitors the state of the PI controlling the DFI bus. 1 means PI is in control. READ-ONLY.
23-20	RESERVED	R/W	X	
19-0	PI_TREF_INTERVAL	R/W	0h	Defines the cycles between refreshes to different chip selects.

4.3.18 DDRSS_PI_17 Register (Offset = 2044h) [reset = X]

DDRSS_PI_17 is shown in [Figure 4-512](#) and described in [Table 4-1030](#).

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Table 4-1029. DDRSS_PI_17 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2044h

Figure 4-512. DDRSS_PI_17 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SW_WRLVL_RESP_0
R/W-X							R-0h
23	22	21	20	19	18	17	16
RESERVED							PI_SWLVL_OP_DONE
R/W-X							R-0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_LOAD
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_DATA_RETENTION
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1030. DDRSS_PI_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SW_WRLVL_RESP_0	R	0h	Write leveling response for data slice 0. READ-ONLY
23-17	RESERVED	R/W	X	
16	PI_SWLVL_OP_DONE	R	0h	Reports the status of the software leveling operation. Value of 1 indicates operation complete. READ-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_LOAD	W	0h	User request to load delays and execute software leveling. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_DATA_RETENTION	R	0h	Monitors the readiness for the PHY to be put into data retention mode after pi_sref_entry req parameter has been written. 1 means ready for data retention. READ-ONLY.

4.3.19 DDRSS_PI_18 Register (Offset = 2048h) [reset = X]

DDRSS_PI_18 is shown in [Figure 4-513](#) and described in [Table 4-1032](#).

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Table 4-1031. DDRSS_PI_18 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2048h

Figure 4-513. DDRSS_PI_18 Register

31	30	29	28	27	26	25	24
RESERVED						PI_SW_RDLVL_RESP_0	
R-X						R-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WRLVL_RESP_3	
R-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_SW_WRLVL_RESP_2	
R-X						R-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_SW_WRLVL_RESP_1	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-1032. DDRSS_PI_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-24	PI_SW_RDLVL_RESP_0	R	0h	Read leveling response for data slice 0. READ-ONLY
23-17	RESERVED	R	X	
16	PI_SW_WRLVL_RESP_3	R	0h	Write leveling response for data slice 3. READ-ONLY
15-9	RESERVED	R	X	
8	PI_SW_WRLVL_RESP_2	R	0h	Write leveling response for data slice 2. READ-ONLY
7-1	RESERVED	R	X	
0	PI_SW_WRLVL_RESP_1	R	0h	Write leveling response for data slice 1. READ-ONLY

4.3.20 DDRSS_PI_19 Register (Offset = 204Ch) [reset = X]

DDRSS_PI_19 is shown in [Figure 4-514](#) and described in [Table 4-1034](#).

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Table 4-1033. DDRSS_PI_19 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 204Ch

Figure 4-514. DDRSS_PI_19 Register

31	30	29	28	27	26	25	24
RESERVED						PI_SW_CALVL_RESP_0	
R-X						R-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_SW_RDLVL_RESP_3	
R-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_SW_RDLVL_RESP_2	
R-X						R-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_SW_RDLVL_RESP_1	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-1034. DDRSS_PI_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-24	PI_SW_CALVL_RESP_0	R	0h	CA leveling response for address slice 0. READ-ONLY
23-18	RESERVED	R	X	
17-16	PI_SW_RDLVL_RESP_3	R	0h	Read leveling response for data slice 3. READ-ONLY
15-10	RESERVED	R	X	
9-8	PI_SW_RDLVL_RESP_2	R	0h	Read leveling response for data slice 2. READ-ONLY
7-2	RESERVED	R	X	
1-0	PI_SW_RDLVL_RESP_1	R	0h	Read leveling response for data slice 1. READ-ONLY

4.3.21 DDRSS_PI_20 Register (Offset = 2050h) [reset = X]

DDRSS_PI_20 is shown in [Figure 4-515](#) and described in [Table 4-1036](#).

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Table 4-1035. DDRSS_PI_20 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2050h

Figure 4-515. DDRSS_PI_20 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_0
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_SWLVL_EXIT
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_START
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED					PI_SW_LEVELING_MODE		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1036. DDRSS_PI_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SWLVL_WR_SLICE_0	W	0h	SW leveling write command in WDQ training. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PI_SWLVL_EXIT	W	0h	User request to exit software leveling. Set to 1 to exit. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_START	W	0h	User request to initiate software leveling of type in the SW_LEVELING_MODE parameter. Set to 1 to trigger. WRITE-ONLY
7-3	RESERVED	R/W	X	
2-0	PI_SW_LEVELING_MODE	R/W	0h	Defines the leveling operation for software leveling. Set to 'b000 for DDR4 VREF training, set to b001 for write leveling, set to b010 for read data eye training, or set to b011 for read gate training, set to b100 for ca training, set to b101 for wdq training.

4.3.22 DDRSS_PI_21 Register (Offset = 2054h) [reset = X]

DDRSS_PI_21 is shown in [Figure 4-516](#) and described in [Table 4-1038](#).

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Table 4-1037. DDRSS_PI_21 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2054h

Figure 4-516. DDRSS_PI_21 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_1
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WDQLVL_RESP_0	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_0
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_0
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1038. DDRSS_PI_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SWLVL_WR_SLICE_1	W	0h	SW leveling write command in WDQ training. WRITE-ONLY
23-18	RESERVED	R/W	X	
17-16	PI_SW_WDQLVL_RESP_0	R	0h	Leveling response for data slice 0. READ-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_VREF_UPDATE_SLICE_0	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_SWLVL_RD_SLICE_0	W	0h	SW leveling read command in WDQ training. WRITE-ONLY

4.3.23 DDRSS_PI_22 Register (Offset = 2058h) [reset = X]

DDRSS_PI_22 is shown in [Figure 4-517](#) and described in [Table 4-1040](#).

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Table 4-1039. DDRSS_PI_22 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2058h

Figure 4-517. DDRSS_PI_22 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_2
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WDQLVL_RESP_1	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_1
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_1
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1040. DDRSS_PI_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SWLVL_WR_SLICE_2	W	0h	SW leveling write command in WDQ training. WRITE-ONLY
23-18	RESERVED	R/W	X	
17-16	PI_SW_WDQLVL_RESP_1	R	0h	Leveling response for data slice 1. READ-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_VREF_UPDATE_SLICE_1	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_SWLVL_RD_SLICE_1	W	0h	SW leveling read command in WDQ training. WRITE-ONLY

4.3.24 DDRSS_PI_23 Register (Offset = 205Ch) [reset = X]

DDRSS_PI_23 is shown in [Figure 4-518](#) and described in [Table 4-1042](#).

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Table 4-1041. DDRSS_PI_23 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 205Ch

Figure 4-518. DDRSS_PI_23 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_WR_SLICE_3
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED						PI_SW_WDQLVL_RESP_2	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_2
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_2
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1042. DDRSS_PI_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SWLVL_WR_SLICE_3	W	0h	SW leveling write command in WDQ training. WRITE-ONLY
23-18	RESERVED	R/W	X	
17-16	PI_SW_WDQLVL_RESP_2	R	0h	Leveling response for data slice 2. READ-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_VREF_UPDATE_SLICE_2	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_SWLVL_RD_SLICE_2	W	0h	SW leveling read command in WDQ training. WRITE-ONLY

4.3.25 DDRSS_PI_24 Register (Offset = 2060h) [reset = X]

DDRSS_PI_24 is shown in [Figure 4-519](#) and described in [Table 4-1044](#).

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Table 4-1043. DDRSS_PI_24 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2060h

Figure 4-519. DDRSS_PI_24 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SWLVL_SM2_START
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_SW_WDQLVL_RESP_3
R/W-X							R-0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_VREF_UPDATE_SLICE_3
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_RD_SLICE_3
R/W-X							W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1044. DDRSS_PI_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SWLVL_SM2_START	W	0h	SW leveling start command for stage 2. WRITE-ONLY
23-18	RESERVED	R/W	X	
17-16	PI_SW_WDQLVL_RESP_3	R	0h	Leveling response for data slice 3. READ-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_VREF_UPDATE_SLICE_3	W	0h	SW leveling vref update command in WDQ training. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_SWLVL_RD_SLICE_3	W	0h	SW leveling read command in WDQ training. WRITE-ONLY

4.3.26 DDRSS_PI_25 Register (Offset = 2064h) [reset = X]

DDRSS_PI_25 is shown in [Figure 4-520](#) and described in [Table 4-1046](#).

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Table 4-1045. DDRSS_PI_25 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2064h

Figure 4-520. DDRSS_PI_25 Register

31	30	29	28	27	26	25	24
RESERVED							PI_DFS_PERIOD_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_SEQUENTIAL_LVL_REQ
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_SWLVL_SM2_RD
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SWLVL_SM2_WR
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1046. DDRSS_PI_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_DFS_PERIOD_EN	R/W	0h	Enable the DFS triggered periodic leveling.
23-17	RESERVED	R/W	X	
16	PI_SEQUENTIAL_LVL_REQ	W	0h	User request to initiate all possible leveling sequences. Set to 1 to trigger. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	PI_SWLVL_SM2_RD	W	0h	SW leveling read command for stage 2. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_SWLVL_SM2_WR	W	0h	SW leveling write command for stage 2. WRITE-ONLY

4.3.27 DDRSS_PI_26 Register (Offset = 2068h) [reset = X]

DDRSS_PI_26 is shown in [Figure 4-521](#) and described in [Table 4-1048](#).

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Table 4-1047. DDRSS_PI_26 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2068h

Figure 4-521. DDRSS_PI_26 Register

31	30	29	28	27	26	25	24
RESERVED							PI_WRLVL_REQ
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_16BIT_DRAM_CONNECT
R/W-X							R/W-1h
15	14	13	12	11	10	9	8
RESERVED							PI_DFI40_POLARITY
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SRE_PERIOD_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1048. DDRSS_PI_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_WRLVL_REQ	W	0h	User request to initiate write leveling. Set to 1 to trigger. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PI_16BIT_DRAM_CONNECT	R/W	1h	Enable 16/32 bit DRAM configuration. 0: 16bit DRAM. 1: 32 bit DRAM.
15-9	RESERVED	R/W	X	
8	PI_DFI40_POLARITY	R/W	0h	Defines the polarity of the dfi_wrdata_cs_n/dfi_rddata_cs_n signals.
7-1	RESERVED	R/W	X	
0	PI_SRE_PERIOD_EN	R/W	0h	Enable the self refresh exit triggered periodic leveling.

4.3.28 DDRSS_PI_27 Register (Offset = 206Ch) [reset = X]

DDRSS_PI_27 is shown in [Figure 4-522](#) and described in [Table 4-1050](#).

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Table 4-1049. DDRSS_PI_27 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 206Ch

Figure 4-522. DDRSS_PI_27 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PI_WLMRD					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PI_WLDQSEN					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED						PI_WRLVL_CS	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1050. DDRSS_PI_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PI_WLMRD	R/W	0h	Delay from issuing MRS to first write leveling strobe.
15-14	RESERVED	R/W	X	
13-8	PI_WLDQSEN	R/W	0h	Delay from issuing MRS to first DQS strobe for write leveling.
7-2	RESERVED	R/W	X	
1-0	PI_WRLVL_CS	R/W	0h	Specifies the target chip select for the write leveling operation initiated through the WRLVL_REQ parameter.

4.3.29 DDRSS_PI_28 Register (Offset = 2070h) [reset = X]

DDRSS_PI_28 is shown in [Figure 4-523](#) and described in [Table 4-1052](#).

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Table 4-1051. DDRSS_PI_28 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2070h

Figure 4-523. DDRSS_PI_28 Register

31	30	29	28	27	26	25	24
RESERVED							PI_WRLVL_ON_SREF_EXIT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_WRLVL_PERIODIC
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PI_WRLVL_INTERVAL							
R/W-0h							
7	6	5	4	3	2	1	0
PI_WRLVL_INTERVAL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1052. DDRSS_PI_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_WRLVL_ON_SREF_EXIT	R/W	0h	Enables automatic write leveling on a self-refresh exit. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	PI_WRLVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during write leveling. Set to 1 to enable.
15-0	PI_WRLVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic write leveling commands.

4.3.30 DDRSS_PI_29 Register (Offset = 2074h) [reset = X]

DDRSS_PI_29 is shown in [Figure 4-524](#) and described in [Table 4-1054](#).

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Table 4-1053. DDRSS_PI_29 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2074h

Figure 4-524. DDRSS_PI_29 Register

31	30	29	28	27	26	25	24
RESERVED				PI_WRLVL_CS_MAP			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PI_WRLVL_ROTATE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PI_WRLVL_RESP_MASK			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PI_WRLVL_DISABLE_DFS
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1054. DDRSS_PI_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_WRLVL_CS_MAP	R/W	0h	Defines the chip select map for write leveling operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for write leveling.
23-17	RESERVED	R/W	X	
16	PI_WRLVL_ROTATE	R/W	0h	Enables rotational CS for counter triggered automatic write leveling. Set to 1, only one rank's write leveling will process, the rank number is rotational for each time that write leveling been triggered by counter expiring. Set to 0 or not a short pattern leveling (indicated by dfi_lvl_periodic), the counter expired write leveling will process all the ranks.
15-12	RESERVED	R/W	X	
11-8	PI_WRLVL_RESP_MASK	R/W	0h	Mask for the dfi_wrlvl_resp signal during write leveling.
7-1	RESERVED	R/W	X	
0	PI_WRLVL_DISABLE_DFS	R/W	0h	Disable automatic write leveling on freq change. Set to 1 to disable wrlvl on dfs, set 0 enable wrlvl on dfs.

4.3.31 DDRSS_PI_30 Register (Offset = 2078h) [reset = X]

DDRSS_PI_30 is shown in [Figure 4-525](#) and described in [Table 4-1056](#).

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Table 4-1055. DDRSS_PI_30 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2078h

Figure 4-525. DDRSS_PI_30 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_EN							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PI_WRLVL_ER ROR_STATUS
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1056. DDRSS_PI_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PI_TDFI_WRLVL_EN	R/W	0h	Defines the DFI tWRLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_wrlvl_en assertion to the first dfi_wrlvl_strobe assertion.
7-1	RESERVED	R/W	X	
0	PI_WRLVL_ERROR_STA TUS	R	0h	Holds the error associated with the write level error interrupt. Bit (0) set indicates a TDFI_WRLVL_MAX parameter violation and bit (1) set indicates a TDFI_WRLVL_RESP parameter violation. READ-ONLY

4.3.32 DDRSS_PI_31 Register (Offset = 207Ch) [reset = 0h]

DDRSS_PI_31 is shown in [Figure 4-526](#) and described in [Table 4-1058](#).

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Table 4-1057. DDRSS_PI_31 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 207Ch

Figure 4-526. DDRSS_PI_31 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1058. DDRSS_PI_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_WRLVL_RESP	R/W	0h	Defines the DFI tWRLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_req assertion and a dfi_wrlvl_en assertion.

4.3.33 DDRSS_PI_32 Register (Offset = 2080h) [reset = 0h]

DDRSS_PI_32 is shown in [Figure 4-527](#) and described in [Table 4-1060](#).

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Table 4-1059. DDRSS_PI_32 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2080h

Figure 4-527. DDRSS_PI_32 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_WRLVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1060. DDRSS_PI_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_WRLVL_MAX	R/W	0h	Defines the DFI tWRLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_en assertion and a valid dfi_wrlvl_resp.

4.3.34 DDRSS_PI_33 Register (Offset = 2084h) [reset = X]

DDRSS_PI_33 is shown in [Figure 4-528](#) and described in [Table 4-1062](#).

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Table 4-1061. DDRSS_PI_33 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2084h

Figure 4-528. DDRSS_PI_33 Register

31	30	29	28	27	26	25	24
RESERVED				PI_ODT_VALUE			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_TODTH_RD			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TODTH_WR			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_WRLVL_STROBE_NUM			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1062. DDRSS_PI_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_ODT_VALUE	R/W	0h	When using LPDDR4, this value will be driven out on the dfi_odt signal.
23-20	RESERVED	R/W	X	
19-16	PI_TODTH_RD	R/W	0h	Defines the minimum DRAM cycles of ODT high time for a read command, in memory clocks.
15-12	RESERVED	R/W	X	
11-8	PI_TODTH_WR	R/W	0h	Defines the minimum DRAM cycles of ODT high time for a write command, in memory clocks.
7-5	RESERVED	R/W	X	
4-0	PI_WRLVL_STROBE_NUM	R/W	0h	Defines the number of write leveling strobes generated.

4.3.35 DDRSS_PI_34 Register (Offset = 2088h) [reset = X]

DDRSS_PI_34 is shown in [Figure 4-529](#) and described in [Table 4-1064](#).

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Table 4-1063. DDRSS_PI_34 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2088h

Figure 4-529. DDRSS_PI_34 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_CS	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							PI_RDLVL_GATE_REQ
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_REQ
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1064. DDRSS_PI_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PI_RDLVL_CS	R/W	0h	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ parameter or the gate training operation initiated through the RDLVL_GATE_REQ parameter.
15-9	RESERVED	R/W	X	
8	PI_RDLVL_GATE_REQ	W	0h	User request to initiate gate training. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PI_RDLVL_REQ	W	0h	User request to initiate data eye training. Set to 1 to trigger. WRITE-ONLY

4.3.36 DDRSS_PI_35 Register (Offset = 208Ch) [reset = 0h]

DDRSS_PI_35 is shown in [Figure 4-530](#) and described in [Table 4-1066](#).

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Table 4-1065. DDRSS_PI_35 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 208Ch

Figure 4-530. DDRSS_PI_35 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1066. DDRSS_PI_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_0	R/W	0h	Non-default pattern 0 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.37 DDRSS_PI_36 Register (Offset = 2090h) [reset = 0h]

DDRSS_PI_36 is shown in [Figure 4-531](#) and described in [Table 4-1068](#).

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Table 4-1067. DDRSS_PI_36 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2090h

Figure 4-531. DDRSS_PI_36 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1068. DDRSS_PI_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_1	R/W	0h	Non-default pattern 1 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.38 DDRSS_PI_37 Register (Offset = 2094h) [reset = 0h]

DDRSS_PI_37 is shown in [Figure 4-532](#) and described in [Table 4-1070](#).

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Table 4-1069. DDRSS_PI_37 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2094h

Figure 4-532. DDRSS_PI_37 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1070. DDRSS_PI_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_2	R/W	0h	Non-default pattern 2 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.39 DDRSS_PI_38 Register (Offset = 2098h) [reset = 0h]

DDRSS_PI_38 is shown in [Figure 4-533](#) and described in [Table 4-1072](#).

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Table 4-1071. DDRSS_PI_38 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2098h

Figure 4-533. DDRSS_PI_38 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1072. DDRSS_PI_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_3	R/W	0h	Non-default pattern 3 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.40 DDRSS_PI_39 Register (Offset = 209Ch) [reset = 0h]

DDRSS_PI_39 is shown in [Figure 4-534](#) and described in [Table 4-1074](#).

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Table 4-1073. DDRSS_PI_39 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 209Ch

Figure 4-534. DDRSS_PI_39 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_4																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1074. DDRSS_PI_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_4	R/W	0h	Non-default pattern 4 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.41 DDRSS_PI_40 Register (Offset = 20A0h) [reset = 0h]

DDRSS_PI_40 is shown in [Figure 4-535](#) and described in [Table 4-1076](#).

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Table 4-1075. DDRSS_PI_40 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20A0h

Figure 4-535. DDRSS_PI_40 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_5																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1076. DDRSS_PI_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_5	R/W	0h	Non-default pattern 5 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.42 DDRSS_PI_41 Register (Offset = 20A4h) [reset = 0h]

DDRSS_PI_41 is shown in [Figure 4-536](#) and described in [Table 4-1078](#).

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Table 4-1077. DDRSS_PI_41 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20A4h

Figure 4-536. DDRSS_PI_41 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_6																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1078. DDRSS_PI_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_6	R/W	0h	Non-default pattern 6 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.43 DDRSS_PI_42 Register (Offset = 20A8h) [reset = 0h]

DDRSS_PI_42 is shown in [Figure 4-537](#) and described in [Table 4-1080](#).

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Table 4-1079. DDRSS_PI_42 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20A8h

Figure 4-537. DDRSS_PI_42 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_RDLVL_PAT_7																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1080. DDRSS_PI_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_RDLVL_PAT_7	R/W	0h	Non-default pattern 7 used for read data eye training of DDR4 or LPDDR4, and read dbi training of DDR4.

4.3.44 DDRSS_PI_43 Register (Offset = 20ACh) [reset = X]

DDRSS_PI_43 is shown in [Figure 4-538](#) and described in [Table 4-1082](#).

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Table 4-1081. DDRSS_PI_43 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20ACh

Figure 4-538. DDRSS_PI_43 Register

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_DISABLE_DFS
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_ON_SREF_EXIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_RDLVL_PERIODIC
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				PI_RDLVL_SEQ_EN			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1082. DDRSS_PI_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_RDLVL_DISABLE_DFS	R/W	0h	Disables automatic data eye training on freq change. Set to 1 to disable rdvl on dfs, Set to 0 to enable rdvl on dfs.
23-17	RESERVED	R/W	X	
16	PI_RDLVL_ON_SREF_EXIT	R/W	0h	Enables automatic data eye training on a self-refresh exit. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	PI_RDLVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during data eye training. Set to 1 to enable.
7-4	RESERVED	R/W	X	
3-0	PI_RDLVL_SEQ_EN	R/W	0h	Specifies the pattern, format and MPR for data eye training.

4.3.45 DDRSS_PI_44 Register (Offset = 20B0h) [reset = X]

DDRSS_PI_44 is shown in [Figure 4-539](#) and described in [Table 4-1084](#).

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Table 4-1083. DDRSS_PI_44 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20B0h

Figure 4-539. DDRSS_PI_44 Register

31	30	29	28	27	26	25	24
RESERVED							PI_RDLVL_ROTATE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_RDLVL_GATE_DISABLE_DFS
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_RDLVL_GATE_ON_SREF_EXIT
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_GATE_PERIODIC
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1084. DDRSS_PI_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_RDLVL_ROTATE	R/W	0h	Enables rotational CS for interval data eye training. Set to 1 for rotating CS.
23-17	RESERVED	R/W	X	
16	PI_RDLVL_GATE_DISABLE_DFS	R/W	0h	Disables automatic gate training on freq change. Set to 1 to disable rdvl_gate on dfs, Set to 0 to enable rdvl_gate on dfs.
15-9	RESERVED	R/W	X	
8	PI_RDLVL_GATE_ON_SREF_EXIT	R/W	0h	Enables automatic gate training on a self-refresh exit. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	PI_RDLVL_GATE_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during gate training. Set to 1 to enable.

4.3.46 DDRSS_PI_45 Register (Offset = 20B4h) [reset = X]

DDRSS_PI_45 is shown in [Figure 4-540](#) and described in [Table 4-1086](#).

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Table 4-1085. DDRSS_PI_45 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20B4h

Figure 4-540. DDRSS_PI_45 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PI_RDLVL_GATE_CS_MAP			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RDLVL_CS_MAP			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_GATE_ROTATE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1086. DDRSS_PI_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PI_RDLVL_GATE_CS_MAP	R/W	0h	Defines the chip select map for gate training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for gate training.
15-12	RESERVED	R/W	X	
11-8	PI_RDLVL_CS_MAP	R/W	0h	Defines the chip select map for data eye training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for data eye training.
7-1	RESERVED	R/W	X	
0	PI_RDLVL_GATE_ROTATE	R/W	0h	Enables rotational CS for interval gate training. Set to 1 for rotating CS.

4.3.47 DDRSS_PI_46 Register (Offset = 20B8h) [reset = X]

DDRSS_PI_46 is shown in [Figure 4-541](#) and described in [Table 4-1088](#).

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Table 4-1087. DDRSS_PI_46 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20B8h

Figure 4-541. DDRSS_PI_46 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TDFI_RDLVL_RR									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1088. DDRSS_PI_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PI_TDFI_RDLVL_RR	R/W	0h	Defines the DFI tRDLVL_RR timing parameter (in DFI clocks), the minimum cycles between read commands.

4.3.48 DDRSS_PI_47 Register (Offset = 20BCh) [reset = 0h]

DDRSS_PI_47 is shown in [Figure 4-542](#) and described in [Table 4-1090](#).

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Table 4-1089. DDRSS_PI_47 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20BCh

Figure 4-542. DDRSS_PI_47 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_RDLVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1090. DDRSS_PI_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_RDLVL_RESP	R/W	0h	Defines the DFI tRDLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_rdlvl_req or dfi_rdlvl_gate_req assertion and a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion.

4.3.49 DDRSS_PI_48 Register (Offset = 20C0h) [reset = X]

DDRSS_PI_48 is shown in [Figure 4-543](#) and described in [Table 4-1092](#).

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Table 4-1091. DDRSS_PI_48 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20C0h

Figure 4-543. DDRSS_PI_48 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PI_TDFI_RDLVL_EN							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PI_RDLVL_RESP_MASK			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1092. DDRSS_PI_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PI_TDFI_RDLVL_EN	R/W	0h	Defines the DFI tRDLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion to the first read or MRR. Set to 1 means the minium value(1 cycle), set to 0 means the maxium value
7-4	RESERVED	R/W	X	
3-0	PI_RDLVL_RESP_MASK	R/W	0h	Mask for the dfi_rdlvl_resp signal during data eye training.

4.3.50 DDRSS_PI_49 Register (Offset = 20C4h) [reset = 0h]

DDRSS_PI_49 is shown in [Figure 4-544](#) and described in [Table 4-1094](#).

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Table 4-1093. DDRSS_PI_49 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20C4h

Figure 4-544. DDRSS_PI_49 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_RDLVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1094. DDRSS_PI_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_RDLVL_MAX	R/W	0h	Defines the DFI tRDLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion and a valid dfi_rdlvl_resp.

4.3.51 DDRSS_PI_50 Register (Offset = 20C8h) [reset = X]

DDRSS_PI_50 is shown in [Figure 4-545](#) and described in [Table 4-1096](#).

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Table 4-1095. DDRSS_PI_50 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20C8h

Figure 4-545. DDRSS_PI_50 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PI_RDLVL_INTERVAL							
R/W-0h							
15	14	13	12	11	10	9	8
PI_RDLVL_INTERVAL							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PI_RDLVL_ER ROR_STATUS
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1096. DDRSS_PI_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-8	PI_RDLVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic data eye training commands.
7-1	RESERVED	R/W	X	
0	PI_RDLVL_ERROR_STAT US	R	0h	Holds the error associated with the data eye training error or gate training error interrupt. Uppermost bit set indicates a TDFI_RDLVL_RESP parameter violation. Next uppermost bit set indicates a TDFI_RDLVL_MAX parameter violation. Lower bits are reserved. READ-ONLY

4.3.52 DDRSS_PI_51 Register (Offset = 20CCh) [reset = X]

DDRSS_PI_51 is shown in [Figure 4-546](#) and described in [Table 4-1098](#).

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Table 4-1097. DDRSS_PI_51 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20CCh

Figure 4-546. DDRSS_PI_51 Register

31	30	29	28	27	26	25	24
RESERVED				PI_RDLVL_PATTERN_NUM			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_RDLVL_PATTERN_START			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_RDLVL_GATE_INTERVAL							
R/W-0h							
7	6	5	4	3	2	1	0
PI_RDLVL_GATE_INTERVAL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1098. DDRSS_PI_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_RDLVL_PATTERN_NUM	R/W	0h	Defines the number of pattern supported in read leveling.
23-20	RESERVED	R/W	X	
19-16	PI_RDLVL_PATTERN_START	R/W	0h	Defines the start pattern in read leveling.
15-0	PI_RDLVL_GATE_INTERVAL	R/W	0h	Number of long count sequences counted between automatic gate training commands.

4.3.53 DDRSS_PI_52 Register (Offset = 20D0h) [reset = X]

DDRSS_PI_52 is shown in [Figure 4-547](#) and described in [Table 4-1100](#).

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Table 4-1099. DDRSS_PI_52 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20D0h

Figure 4-547. DDRSS_PI_52 Register

31	30	29	28	27	26	25	24
RESERVED							PI_REG_DIMM_ENABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_RD_PREAMBLE_TRAINING_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED			PI_RDLVL_GATE_STROBE_NUM				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED			PI_RDLVL_STROBE_NUM				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1100. DDRSS_PI_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_REG_DIMM_ENABLE	R/W	0h	Enable registered DIMM operation. Set to 1 to enable.
23-17	RESERVED	R/W	X	
16	PI_RD_PREAMBLE_TRAINING_EN	R/W	0h	Enable read preamble training during gate training. Set to 1 to enable.
15-13	RESERVED	R/W	X	
12-8	PI_RDLVL_GATE_STROBE_NUM	R/W	0h	Defines the number of back to back MPC command in one read process in read gate training.
7-5	RESERVED	R/W	X	
4-0	PI_RDLVL_STROBE_NUM	R/W	0h	Defines the number of back to back MPC command in one read process in read eye training.

4.3.54 DDRSS_PI_53 Register (Offset = 20D4h) [reset = X]

DDRSS_PI_53 is shown in [Figure 4-548](#) and described in [Table 4-1102](#).

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Table 4-1101. DDRSS_PI_53 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20D4h

Figure 4-548. DDRSS_PI_53 Register

31	30	29	28	27	26	25	24
RESERVED						PI_CALVL_CS	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_CALVL_REQ	
R/W-X						W-0h	
15	14	13	12	11	10	9	8
RESERVED		PI_TDFI_PHY_WRLAT					
R/W-X		R-0h					
7	6	5	4	3	2	1	0
RESERVED		PI_TDFI_RDDATA_EN					
R/W-X		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1102. DDRSS_PI_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_CALVL_CS	R/W	0h	Specifies the target chip select for the CA training operation initiated through the CALVL_REQ parameter.
23-17	RESERVED	R/W	X	
16	PI_CALVL_REQ	W	0h	User request to initiate CA training. Set to 1 to trigger. WRITE-ONLY
15	RESERVED	R/W	X	
14-8	PI_TDFI_PHY_WRLAT	R	0h	Holds the calculated DFI tPHY_WRLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_en assertion. READ-ONLY
7	RESERVED	R/W	X	
6-0	PI_TDFI_RDDATA_EN	R	0h	Holds the calculated DFI tRDDATA_EN timing parameter (in DFI PHY clocks), the maximum cycles between a read command and a dfi_rddata_en assertion. READ-ONLY

4.3.55 DDRSS_PI_54 Register (Offset = 20D8h) [reset = X]

DDRSS_PI_54 is shown in [Figure 4-549](#) and described in [Table 4-1104](#).

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Table 4-1103. DDRSS_PI_54 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20D8h

Figure 4-549. DDRSS_PI_54 Register

31	30	29	28	27	26	25	24
RESERVED							PI_CALVL_PERIODIC
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_CALVL_SEQ_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1104. DDRSS_PI_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_CALVL_PERIODIC	R/W	0h	Enables the use of the dfi_lvl_periodic signal during CA training. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PI_CALVL_SEQ_EN	R/W	0h	Specifies which CA training patterns will be used. Set to 0 for pattern 0 only, set to 1 for patterns 0 and 1, set to 2 for patterns 0, 1 and 2, or set to 3 for all patterns.
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.3.56 DDRSS_PI_55 Register (Offset = 20DCh) [reset = X]

DDRSS_PI_55 is shown in [Figure 4-550](#) and described in [Table 4-1106](#).

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Table 4-1105. DDRSS_PI_55 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20DCh

Figure 4-550. DDRSS_PI_55 Register

31	30	29	28	27	26	25	24
RESERVED				PI_CALVL_CS_MAP			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PI_CALVL_ROTATE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_CALVL_DISABLE_DFS
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_CALVL_ON_SREF_EXIT
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1106. DDRSS_PI_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_CALVL_CS_MAP	R/W	0h	Defines the chip select map for CA training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set each bit to 1 to enable chip for CA training.
23-17	RESERVED	R/W	X	
16	PI_CALVL_ROTATE	R/W	0h	Enables rotational CS for interval CA training. Set to 1 for rotating CS.
15-9	RESERVED	R/W	X	
8	PI_CALVL_DISABLE_DFS	R/W	0h	Disables automatic CA training on freq change. Set to 1 to disable CA training on dfs, Set to 0 to enable CA training .
7-1	RESERVED	R/W	X	
0	PI_CALVL_ON_SREF_EXIT	R/W	0h	Enables automatic CA training on a self-refresh exit. Set to 1 to enable.

4.3.57 DDRSS_PI_56 Register (Offset = 20E0h) [reset = X]

DDRSS_PI_56 is shown in [Figure 4-551](#) and described in [Table 4-1108](#).

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Table 4-1107. DDRSS_PI_56 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20E0h

Figure 4-551. DDRSS_PI_56 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TDFI_CALVL_EN							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1108. DDRSS_PI_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	PI_TDFI_CALVL_EN	R/W	0h	Defines the DFI tCALVL_EN timing parameter (in DFI clocks), the minimum cycles between a dfi_calvl_en assertion and a dfi_cke de-assertion.

4.3.58 DDRSS_PI_57 Register (Offset = 20E4h) [reset = 0h]

DDRSS_PI_57 is shown in [Figure 4-552](#) and described in [Table 4-1110](#).

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Table 4-1109. DDRSS_PI_57 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20E4h

Figure 4-552. DDRSS_PI_57 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CALVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1110. DDRSS_PI_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_CALVL_RESP	R/W	0h	Defines the DFI tCALVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_req assertion and a dfi_calvl_en assertion.

4.3.59 DDRSS_PI_58 Register (Offset = 20E8h) [reset = 0h]

DDRSS_PI_58 is shown in [Figure 4-553](#) and described in [Table 4-1112](#).

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Table 4-1111. DDRSS_PI_58 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20E8h

Figure 4-553. DDRSS_PI_58 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CALVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1112. DDRSS_PI_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_CALVL_MAX	R/W	0h	Defines the DFI tCALVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_en assertion and a valid dfi_calvl_resp.

4.3.60 DDRSS_PI_59 Register (Offset = 20ECh) [reset = X]

DDRSS_PI_59 is shown in [Figure 4-554](#) and described in [Table 4-1114](#).

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Table 4-1113. DDRSS_PI_59 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20ECh

Figure 4-554. DDRSS_PI_59 Register

31	30	29	28	27	26	25	24
PI_CALVL_INTERVAL							
R/W-0h							
23	22	21	20	19	18	17	16
PI_CALVL_INTERVAL							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PI_CALVL_ERROR_STATUS	
R/W-X						R-0h	
7	6	5	4	3	2	1	0
RESERVED							PI_CALVL_RESP_MASK
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1114. DDRSS_PI_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PI_CALVL_INTERVAL	R/W	0h	Number of long count sequences counted between automatic CA training commands.
15-10	RESERVED	R/W	X	
9-8	PI_CALVL_ERROR_STATUS	R	0h	Holds the error associated with the CA training error interrupt. Bit (0) set indicates a TDFI_CALVL_RESP parameter violation and bit (1) set indicates a TDFI_CALVL_MAX parameter violation. READ-ONLY
7-1	RESERVED	R/W	X	
0	PI_CALVL_RESP_MASK	R/W	0h	Mask for the dfi_calvl_resp signal during CA training.

4.3.61 DDRSS_PI_60 Register (Offset = 20F0h) [reset = X]

DDRSS_PI_60 is shown in [Figure 4-555](#) and described in [Table 4-1116](#).

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Table 4-1115. DDRSS_PI_60 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20F0h

Figure 4-555. DDRSS_PI_60 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TCAEXT			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_TCAKEH			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TCAMRD			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_TCKEL			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1116. DDRSS_PI_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PI_TCAEXT	R/W	0h	DRAM tCAEXT value in memory cycles.
23-21	RESERVED	R/W	X	
20-16	PI_TCAKEH	R/W	0h	DRAM tCAKEH value in memory cycles.
15-14	RESERVED	R/W	X	
13-8	PI_TCAMRD	R/W	0h	DRAM tCAMRD value in memory cycles.
7-5	RESERVED	R/W	X	
4-0	PI_TCKEL	R/W	0h	DRAM tCKEL value in memory cycles.

4.3.62 DDRSS_PI_61 Register (Offset = 20F4h) [reset = X]

DDRSS_PI_61 is shown in [Figure 4-556](#) and described in [Table 4-1118](#).

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Table 4-1117. DDRSS_PI_61 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20F4h

Figure 4-556. DDRSS_PI_61 Register

31	30	29	28	27	26	25	24
PI_TDFI_INIT_START_MIN							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PI_CALVL_VREF_NORMAL_STEPSIZE			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_CALVL_VREF_INITIAL_STEPSIZE			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PI_CA_TRAIN_VREF_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1118. DDRSS_PI_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TDFI_INIT_START_MIN	R/W	0h	Minimum number of DFI clocks before dfi_init_start can be driven after a previous command/training event.
23-20	RESERVED	R/W	X	
19-16	PI_CALVL_VREF_NORMAL_STEPSIZE	R/W	0h	The adjust step for the post-initial Vref(ca) training.
15-12	RESERVED	R/W	X	
11-8	PI_CALVL_VREF_INITIAL_STEPSIZE	R/W	0h	The adjust step for the initial Vref(ca) training.
7-1	RESERVED	R/W	X	
0	PI_CA_TRAIN_VREF_EN	R/W	0h	Control for VREF training during CA training post power-on initialization. Set to enable VREF training.

4.3.63 DDRSS_PI_62 Register (Offset = 20F8h) [reset = X]

DDRSS_PI_62 is shown in [Figure 4-557](#) and described in [Table 4-1120](#).

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Table 4-1119. DDRSS_PI_62 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20F8h

Figure 4-557. DDRSS_PI_62 Register

31	30	29	28	27	26	25	24
RESERVED	PI_SW_CA_TRAIN_VREF						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED				PI_CALVL_STROBE_NUM			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TCKCKEH			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_MIN							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1120. DDRSS_PI_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_SW_CA_TRAIN_VREF	R/W	0h	The Vref value which is set for SW step by step CA training.
23-21	RESERVED	R/W	X	
20-16	PI_CALVL_STROBE_NUM	R/W	0h	The consecutive dfi_calvl_strobe number when updating the CA vref data.
15-12	RESERVED	R/W	X	
11-8	PI_TCKCKEH	R/W	0h	DRAM tCKELCK Clock and command valid before CKE HIGH.
7-0	PI_TDFI_INIT_COMPLETE_MIN	R/W	0h	Minimum number of DFI clocks from dfi_init_complete to a command/training event.

4.3.64 DDRSS_PI_63 Register (Offset = 20FCh) [reset = X]

DDRSS_PI_63 is shown in [Figure 4-558](#) and described in [Table 4-1122](#).

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Table 4-1121. DDRSS_PI_63 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 20FCh

Figure 4-558. DDRSS_PI_63 Register

31	30	29	28	27	26	25	24
RESERVED							PI_REFRESH_BETWEEN_SEGMENT_DISABLE
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
RESERVED							PI_DRAM_CLK_DISABLE_DEASSERT_SEL
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PI_INIT_STARTORCOMPLETE_2_CLKDISABLE							
R/W-0h							
7	6	5	4	3	2	1	0
PI_CLKDISABLE_2_INIT_START							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1122. DDRSS_PI_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_REFRESH_BETWEEN_SEGMENT_DISABLE	R/W	1h	Disable the refresh between CA first and second segment training. Set to 1 to disable.
23-17	RESERVED	R/W	X	
16	PI_DRAM_CLK_DISABLE_DEASSERT_SEL	R/W	0h	Indicate dfi_dram_clk_disable deassert following dfi_init_start deassert or dfi_init_complete assert. Set to 0: dfi_dram_clk_disable deassert following dfi_init_start deassert. Set to 1: dfi_dram_clk_disable deassert following dfi_init_complete assert.
15-8	PI_INIT_STARTORCOMPLETE_2_CLKDISABLE	R/W	0h	Defines the delay from deasserting of dfi_init_start or asserting of dfi_init_complete to deasserting of dfi_dram_clk_disable in DFI clock.
7-0	PI_CLKDISABLE_2_INIT_START	R/W	0h	Defines the delay from the asserting of dfi_dram_clk_disable to the asserting of dfi_init_start in DFI clock.

4.3.65 DDRSS_PI_64 Register (Offset = 2100h) [reset = X]

DDRSS_PI_64 is shown in [Figure 4-559](#) and described in [Table 4-1124](#).

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Table 4-1123. DDRSS_PI_64 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2100h

Figure 4-559. DDRSS_PI_64 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PI_FSM_ERROR_INFO_MASK							
R/W-0h							
15	14	13	12	11	10	9	8
PI_FSM_ERROR_INFO_MASK							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PI_MC_DFS_PI_SET_VREF_ENABLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1124. DDRSS_PI_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-8	PI_FSM_ERROR_INFO_MASK	R/W	0h	PI FSM Error Info MASK
7-1	RESERVED	R/W	X	
0	PI_MC_DFS_PI_SET_VREF_ENABLE	R/W	0h	Enable the PI to set VREF value after DFS issued by MC. MR12 and MR14 for LPDDR4. MR6 for DDR4. 1 means disable.

4.3.66 DDRSS_PI_65 Register (Offset = 2104h) [reset = 0h]

DDRSS_PI_65 is shown in [Figure 4-560](#) and described in [Table 4-1126](#).

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Table 4-1125. DDRSS_PI_65 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2104h

Figure 4-560. DDRSS_PI_65 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_FSM_ERROR_INFO															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_SC_FSM_ERROR_INFO_WOCLR															
W-0h															

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-1126. DDRSS_PI_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PI_FSM_ERROR_INFO	R	0h	Gather each fsm error bit. READ-ONLY.
15-0	PI_SC_FSM_ERROR_INF O_WOCLR	W	0h	PI FSM Error Info. WOCLR

4.3.67 DDRSS_PI_66 Register (Offset = 2108h) [reset = X]

DDRSS_PI_66 is shown in [Figure 4-561](#) and described in [Table 4-1128](#).

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Table 4-1127. DDRSS_PI_66 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2108h

Figure 4-561. DDRSS_PI_66 Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_ROTATE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PI_WDQLVL_RESP_MASK			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PI_WDQLVL_BST_NUM		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED							PI_WDQLVL_VREF_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1128. DDRSS_PI_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_WDQLVL_ROTATE	R/W	0h	Enables write DQ training rotate for interval training.
23-20	RESERVED	R/W	X	
19-16	PI_WDQLVL_RESP_MASK	R/W	0h	Write DQ training response mask. When set to 1, the dfi_wdqlvl_en of the slice is not asserted.
15-11	RESERVED	R/W	X	
10-8	PI_WDQLVL_BST_NUM	R/W	0h	Defines the number of write/read bursts issued at each step in write DQ training.
7-1	RESERVED	R/W	X	
0	PI_WDQLVL_VREF_EN	R/W	0h	Control for VREF training as part of non-initialization write DQ training.

4.3.68 DDRSS_PI_67 Register (Offset = 210Ch) [reset = X]

DDRSS_PI_67 is shown in [Figure 4-562](#) and described in [Table 4-1130](#).

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Table 4-1129. DDRSS_PI_67 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 210Ch

Figure 4-562. DDRSS_PI_67 Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_P ERIODIC
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED			PI_WDQLVL_VREF_NORMAL_STEPSIZE				
R/W-X			R/W-0h				
15	14	13	12	11	10	9	8
RESERVED			PI_WDQLVL_VREF_INITIAL_STEPSIZE				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED				PI_WDQLVL_CS_MAP			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1130. DDRSS_PI_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_WDQLVL_PERIODIC	R/W	0h	Enables periodic write DQ training.
23-21	RESERVED	R/W	X	
20-16	PI_WDQLVL_VREF_NOR MAL_STEPSIZE	R/W	0h	Write DQ training vref step size for post_initial training.
15-13	RESERVED	R/W	X	
12-8	PI_WDQLVL_VREF_INITI AL_STEPSIZE	R/W	0h	Write DQ training vref step size for initial training.
7-4	RESERVED	R/W	X	
3-0	PI_WDQLVL_CS_MAP	R/W	0h	Map of CS's included in write DQ training sequence.

4.3.69 DDRSS_PI_68 Register (Offset = 2110h) [reset = X]

DDRSS_PI_68 is shown in [Figure 4-563](#) and described in [Table 4-1132](#).

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Table 4-1131. DDRSS_PI_68 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2110h

Figure 4-563. DDRSS_PI_68 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PI_TDFI_WDQLVL_EN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PI_WDQLVL_CS	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PI_WDQLVL_REQ
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1132. DDRSS_PI_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PI_TDFI_WDQLVL_EN	R/W	0h	DFI timing param tWDQLVL_EN. Minimum number of DFI clocks required after the write DQ training enable signal is asserted until the first write command may be asserted.
15-10	RESERVED	R/W	X	
9-8	PI_WDQLVL_CS	R/W	0h	Write DQ training target chip select.
7-1	RESERVED	R/W	X	
0	PI_WDQLVL_REQ	W	0h	SW write to initiate Write DQ training request. WRITE-ONLY

4.3.70 DDRSS_PI_69 Register (Offset = 2114h) [reset = 0h]

DDRSS_PI_69 is shown in [Figure 4-564](#) and described in [Table 4-1134](#).

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Table 4-1133. DDRSS_PI_69 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2114h

Figure 4-564. DDRSS_PI_69 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RESP																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1134. DDRSS_PI_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_WDQLVL_RESP	R/W	0h	DFI timing param tWDQLVL_RESP. Maximum number of DFI clocks that may occur between a write DQ training request and the associated mode enable.

4.3.71 DDRSS_PI_70 Register (Offset = 2118h) [reset = 0h]

DDRSS_PI_70 is shown in [Figure 4-565](#) and described in [Table 4-1136](#).

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Table 4-1135. DDRSS_PI_70 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2118h

Figure 4-565. DDRSS_PI_70 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_MAX																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1136. DDRSS_PI_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_WDQLVL_MAX	R/W	0h	DFI timing param tWDQLVL_MAX. Maximum number of DFI clocks that the PI will wait for a response from the PHY.

4.3.72 DDRSS_PI_71 Register (Offset = 211Ch) [reset = X]

DDRSS_PI_71 is shown in [Figure 4-566](#) and described in [Table 4-1138](#).

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Table 4-1137. DDRSS_PI_71 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 211Ch

Figure 4-566. DDRSS_PI_71 Register

31	30	29	28	27	26	25	24
RESERVED							PI_WDQLVL_DISABLE_DFS
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_WDQLVL_ON_SREF_EXIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PI_WDQLVL_INTERVAL							
R/W-0h							
7	6	5	4	3	2	1	0
PI_WDQLVL_INTERVAL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1138. DDRSS_PI_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_WDQLVL_DISABLE_DFS	R/W	0h	Disable automatic write DQ training on freq change. Set to 1 to disable.
23-17	RESERVED	R/W	X	
16	PI_WDQLVL_ON_SREF_EXIT	R/W	0h	Issue a write DQ training command on self-refresh exit.
15-0	PI_WDQLVL_INTERVAL	R/W	0h	Sets the maximum number of long count sequences allowed between automatic write DQ training operations.

4.3.73 DDRSS_PI_72 Register (Offset = 2120h) [reset = X]

DDRSS_PI_72 is shown in [Figure 4-567](#) and described in [Table 4-1140](#).

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Table 4-1139. DDRSS_PI_72 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2120h

Figure 4-567. DDRSS_PI_72 Register

31	30	29	28	27	26	25	24
RESERVED							PI_PARALLEL_WDQLVL_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_DQS_OSC_PERIOD_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_WDQLVL_OSC_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PI_WDQLVL_ERROR_STATUS	
R/W-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1140. DDRSS_PI_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_PARALLEL_WDQLVL_EN	R/W	0h	Enable per rank parallel Write DQ training for LPDDR4, 1 = enabled.
23-17	RESERVED	R/W	X	
16	PI_DQS_OSC_PERIOD_EN	R/W	0h	Enable for DQS oscillator triggered periodic write DQ training, 1 = enabled.
15-9	RESERVED	R/W	X	
8	PI_WDQLVL_OSC_EN	R/W	0h	Enable for DQS oscillator triggered write DQ training, 1 = enabled.
7-2	RESERVED	R/W	X	
1-0	PI_WDQLVL_ERROR_STATUS	R	0h	Holds the error associated with the write dq level error interrupt. Bit (0) set indicates a PI_TDFI_WDQLVL_MAX parameter violation and bit (1) set indicates a PI_TDFI_WDQLVL_RESP parameter violation. READ-ONLY.

4.3.74 DDRSS_PI_73 Register (Offset = 2124h) [reset = X]

DDRSS_PI_73 is shown in [Figure 4-568](#) and described in [Table 4-1142](#).

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Table 4-1141. DDRSS_PI_73 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2124h

Figure 4-568. DDRSS_PI_73 Register

31	30	29	28	27	26	25	24
RESERVED				RESERVED			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_TCCD			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PI_ROW_DIFF		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED						PI_BANK_DIFF	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1142. DDRSS_PI_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	RESERVED	R/W	0h	Reserved
23-21	RESERVED	R/W	X	
20-16	PI_TCCD	R/W	0h	DRAM CAS-to-CAS value in cycles.
15-11	RESERVED	R/W	X	
10-8	PI_ROW_DIFF	R/W	0h	Difference between number of address pins available and number being used.
7-2	RESERVED	R/W	X	
1-0	PI_BANK_DIFF	R/W	0h	Difference between number of bank pins available and number being used.

4.3.75 DDRSS_PI_74 Register (Offset = 2128h) [reset = X]

DDRSS_PI_74 is shown in [Figure 4-569](#) and described in [Table 4-1144](#).

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Table 4-1143. DDRSS_PI_74 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2128h

Figure 4-569. DDRSS_PI_74 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-2h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-2h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1144. DDRSS_PI_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	RESERVED	R/W	2h	Reserved
23-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	2h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.3.76 DDRSS_PI_75 Register (Offset = 212Ch) [reset = X]

DDRSS_PI_75 is shown in [Figure 4-570](#) and described in [Table 4-1146](#).

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Table 4-1145. DDRSS_PI_75 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 212Ch

Figure 4-570. DDRSS_PI_75 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-1h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-1h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1146. DDRSS_PI_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	RESERVED	R/W	1h	Reserved
23-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	1h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.3.77 DDRSS_PI_76 Register (Offset = 2130h) [reset = X]

DDRSS_PI_76 is shown in [Figure 4-571](#) and described in [Table 4-1148](#).

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Table 4-1147. DDRSS_PI_76 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2130h

Figure 4-571. DDRSS_PI_76 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-1h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1148. DDRSS_PI_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	RESERVED	R/W	1h	Reserved
23-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	0h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.3.78 DDRSS_PI_77 Register (Offset = 2134h) [reset = X]

DDRSS_PI_77 is shown in [Figure 4-572](#) and described in [Table 4-1150](#).

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Table 4-1149. DDRSS_PI_77 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2134h

Figure 4-572. DDRSS_PI_77 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-2h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-2h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1150. DDRSS_PI_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	RESERVED	R/W	2h	Reserved
23-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	2h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.3.79 DDRSS_PI_78 Register (Offset = 2138h) [reset = X]

DDRSS_PI_78 is shown in [Figure 4-573](#) and described in [Table 4-1152](#).

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Table 4-1151. DDRSS_PI_78 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2138h

Figure 4-573. DDRSS_PI_78 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												RESERVED			
R/W-X												R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
R/W-X				R/W-2h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1152. DDRSS_PI_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-8	RESERVED	R/W	2h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.3.80 DDRSS_PI_79 Register (Offset = 213Ch) [reset = X]

DDRSS_PI_79 is shown in [Figure 4-574](#) and described in [Table 4-1154](#).

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Table 4-1153. DDRSS_PI_79 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 213Ch

Figure 4-574. DDRSS_PI_79 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PI_INT_STATUS																											
R-X				R-0h																											

LEGEND: R = Read Only; -n = value after reset

Table 4-1154. DDRSS_PI_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-0	PI_INT_STATUS	R	0h	Status of interrupt features in the PI. READ-ONLY

4.3.81 DDRSS_PI_80 Register (Offset = 2140h) [reset = X]

DDRSS_PI_80 is shown in [Figure 4-575](#) and described in [Table 4-1156](#).

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Table 4-1155. DDRSS_PI_80 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2140h

Figure 4-575. DDRSS_PI_80 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PI_INT_ACK																										
W-X					W-0h																										

LEGEND: W = Write Only; -n = value after reset

Table 4-1156. DDRSS_PI_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	W	X	
26-0	PI_INT_ACK	W	0h	Clear the corresponding interrupt bit of the PI_INT_STATUS parameter. WRITE-ONLY

4.3.82 DDRSS_PI_81 Register (Offset = 2144h) [reset = X]

DDRSS_PI_81 is shown in [Figure 4-576](#) and described in [Table 4-1158](#).

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Table 4-1157. DDRSS_PI_81 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2144h

Figure 4-576. DDRSS_PI_81 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PI_INT_MASK																											
R/W-X				R/W-0h																											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1158. DDRSS_PI_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-0	PI_INT_MASK	R/W	0h	Mask for PI_int signals from the PI_INT_STATUS parameter.

4.3.83 DDRSS_PI_82 Register (Offset = 2148h) [reset = 0h]

DDRSS_PI_82 is shown in [Figure 4-577](#) and described in [Table 4-1160](#).

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Table 4-1159. DDRSS_PI_82 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2148h

Figure 4-577. DDRSS_PI_82 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1160. DDRSS_PI_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_EXP_DATA_0	R	0h	Expected data on BIST error. READ-ONLY

4.3.84 DDRSS_PI_83 Register (Offset = 214Ch) [reset = 0h]

DDRSS_PI_83 is shown in [Figure 4-578](#) and described in [Table 4-1162](#).

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Table 4-1161. DDRSS_PI_83 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 214Ch

Figure 4-578. DDRSS_PI_83 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1162. DDRSS_PI_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_EXP_DATA_1	R	0h	Expected data on BIST error. READ-ONLY

4.3.85 DDRSS_PI_84 Register (Offset = 2150h) [reset = 0h]

DDRSS_PI_84 is shown in [Figure 4-579](#) and described in [Table 4-1164](#).

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Table 4-1163. DDRSS_PI_84 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2150h

Figure 4-579. DDRSS_PI_84 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1164. DDRSS_PI_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_EXP_DATA_2	R	0h	Expected data on BIST error. READ-ONLY

4.3.86 DDRSS_PI_85 Register (Offset = 2154h) [reset = 0h]

DDRSS_PI_85 is shown in [Figure 4-580](#) and described in [Table 4-1166](#).

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Table 4-1165. DDRSS_PI_85 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2154h

Figure 4-580. DDRSS_PI_85 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_EXP_DATA_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1166. DDRSS_PI_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_EXP_DATA_3	R	0h	Expected data on BIST error. READ-ONLY

4.3.87 DDRSS_PI_86 Register (Offset = 2158h) [reset = 0h]

DDRSS_PI_86 is shown in [Figure 4-581](#) and described in [Table 4-1168](#).

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Table 4-1167. DDRSS_PI_86 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2158h

Figure 4-581. DDRSS_PI_86 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1168. DDRSS_PI_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_FAIL_DATA_0	R	0h	Actual data on BIST error. READ-ONLY

4.3.88 DDRSS_PI_87 Register (Offset = 215Ch) [reset = 0h]

DDRSS_PI_87 is shown in [Figure 4-582](#) and described in [Table 4-1170](#).

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Table 4-1169. DDRSS_PI_87 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 215Ch

Figure 4-582. DDRSS_PI_87 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1170. DDRSS_PI_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_FAIL_DATA_1	R	0h	Actual data on BIST error. READ-ONLY

4.3.89 DDRSS_PI_88 Register (Offset = 2160h) [reset = 0h]

DDRSS_PI_88 is shown in [Figure 4-583](#) and described in [Table 4-1172](#).

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Table 4-1171. DDRSS_PI_88 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2160h

Figure 4-583. DDRSS_PI_88 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1172. DDRSS_PI_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_FAIL_DATA_2	R	0h	Actual data on BIST error. READ-ONLY

4.3.90 DDRSS_PI_89 Register (Offset = 2164h) [reset = 0h]

DDRSS_PI_89 is shown in [Figure 4-584](#) and described in [Table 4-1174](#).

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Table 4-1173. DDRSS_PI_89 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2164h

Figure 4-584. DDRSS_PI_89 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_FAIL_DATA_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1174. DDRSS_PI_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_FAIL_DATA_3	R	0h	Actual data on BIST error. READ-ONLY

4.3.91 DDRSS_PI_90 Register (Offset = 2168h) [reset = 0h]

DDRSS_PI_90 is shown in [Figure 4-585](#) and described in [Table 4-1176](#).

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Table 4-1175. DDRSS_PI_90 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2168h

Figure 4-585. DDRSS_PI_90 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_FAIL_ADDR_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1176. DDRSS_PI_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_FAIL_ADDR_0	R	0h	The burst aligned address of BIST error. READ-ONLY

4.3.92 DDRSS_PI_91 Register (Offset = 216Ch) [reset = X]

DDRSS_PI_91 is shown in [Figure 4-586](#) and described in [Table 4-1178](#).

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Table 4-1177. DDRSS_PI_91 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 216Ch

Figure 4-586. DDRSS_PI_91 Register

31	30	29	28	27	26	25	24
RESERVED							PI_CMD_SWAP_EN
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PI_LONG_COUNT_MASK			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_BSTLEN			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
RESERVED					PI_BIST_FAIL_ADDR_1		
R/W-X					R-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1178. DDRSS_PI_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_CMD_SWAP_EN	R/W	0h	Command pin swap function enable
23-21	RESERVED	R/W	X	
20-16	PI_LONG_COUNT_MASK	R/W	0h	Reduces the length of the long counter from 1024 cycles.
15-13	RESERVED	R/W	X	
12-8	PI_BSTLEN	R/W	2h	Encoded burst length sent to DRAMs during initialization.
7-3	RESERVED	R/W	X	
2-0	PI_BIST_FAIL_ADDR_1	R	0h	The burst aligned address of BIST error. READ-ONLY

4.3.93 DDRSS_PI_92 Register (Offset = 2170h) [reset = X]

DDRSS_PI_92 is shown in [Figure 4-587](#) and described in [Table 4-1180](#).

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Table 4-1179. DDRSS_PI_92 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2170h

Figure 4-587. DDRSS_PI_92 Register

31	30	29	28	27	26	25	24
RESERVED						PI_DATA_BYTE_SWAP_SLICE2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_DATA_BYTE_SWAP_SLICE1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_DATA_BYTE_SWAP_SLICE0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_DATA_BYTE_SWAP_EN	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1180. DDRSS_PI_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_DATA_BYTE_SWAP_SLICE2	R/W	0h	DATA pin 2 mux selector
23-18	RESERVED	R/W	X	
17-16	PI_DATA_BYTE_SWAP_SLICE1	R/W	0h	DATA pin 1 mux selector
15-10	RESERVED	R/W	X	
9-8	PI_DATA_BYTE_SWAP_SLICE0	R/W	0h	DATA pin 0 mux selector
7-1	RESERVED	R/W	X	
0	PI_DATA_BYTE_SWAP_EN	R/W	0h	DATA pin swap function enable

4.3.94 DDRSS_PI_93 Register (Offset = 2174h) [reset = X]

DDRSS_PI_93 is shown in [Figure 4-588](#) and described in [Table 4-1182](#).

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Table 4-1181. DDRSS_PI_93 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2174h

Figure 4-588. DDRSS_PI_93 Register

31	30	29	28	27	26	25	24
RESERVED						PI_UPDATE_ERROR_STATUS	
R/W-X						R-0h	
23	22	21	20	19	18	17	16
PI_TDFI_CTRLUPD_MIN							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PI_CTRLUPD_REQ_PER_AREF_EN	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_DATA_BYTE_SWAP_SLICE3	
R/W-X						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1182. DDRSS_PI_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_UPDATE_ERROR_STATUS	R	0h	Identifies the source of any DFI PI-initiated update errors. Value of 1 indicates a timing violation of the associated timing parameter. Bit 1- 0: ctrlupd_max_error, ctrlupd_interval_error. Bit 6- 2: reserved. READ-ONLY
23-16	PI_TDFI_CTRLUPD_MIN	R/W	0h	Reports the DFI tCTRLUPD_MIN timing parameter (in DFI clocks), the minimum cycles that dfi_ctrlupd_req must be asserted.
15-9	RESERVED	R/W	X	
8	PI_CTRLUPD_REQ_PER_AREF_EN	R/W	0h	Enable an automatic PI initiated update (dfi_ctrlupd_req) after every refresh. Set to 1 to enable.
7-2	RESERVED	R/W	X	
1-0	PI_DATA_BYTE_SWAP_SLICE3	R/W	0h	DATA pin 3 mux selector

4.3.95 DDRSS_PI_94 Register (Offset = 2178h) [reset = X]

DDRSS_PI_94 is shown in [Figure 4-589](#) and described in [Table 4-1184](#).

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Table 4-1183. DDRSS_PI_94 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2178h

Figure 4-589. DDRSS_PI_94 Register

31	30	29	28	27	26	25	24
RESERVED							PI_BIST_DATA_CHECK
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		PI_ADDR_SPACE					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							PI_BIST_RESULT
R/W-X							R-0h
7	6	5	4	3	2	1	0
RESERVED							PI_BIST_GO
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1184. DDRSS_PI_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_BIST_DATA_CHECK	R/W	0h	Enable data checking with BIST operation. Set to 1 to enable.
23-22	RESERVED	R/W	X	
21-16	PI_ADDR_SPACE	R/W	0h	Sets the number of address bits to check during BIST operation. The end address of BIST is start_address+(1 shifted up by PI_ADDR_SPACE)-1. The end address should not beyond the actual memory address range.
15-10	RESERVED	R/W	X	
9-8	PI_BIST_RESULT	R	0h	BIST operation status (pass/fail). Bit (0) indicates data check status and bit (1) indicates address check status. Value of 1 is a passing result. READ-ONLY
7-1	RESERVED	R/W	X	
0	PI_BIST_GO	R/W	0h	Initiate a BIST operation. Set to 1 to trigger.

4.3.96 DDRSS_PI_95 Register (Offset = 217Ch) [reset = X]

DDRSS_PI_95 is shown in [Figure 4-590](#) and described in [Table 4-1186](#).

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Table 4-1185. DDRSS_PI_95 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 217Ch

Figure 4-590. DDRSS_PI_95 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PI_BIST_ADDR_CHECK
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1186. DDRSS_PI_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PI_BIST_ADDR_CHECK	R/W	0h	Enable address checking with BIST operation. Set to 1 to enable.

4.3.97 DDRSS_PI_96 Register (Offset = 2180h) [reset = 0h]

DDRSS_PI_96 is shown in [Figure 4-591](#) and described in [Table 4-1188](#).

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Table 4-1187. DDRSS_PI_96 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2180h

Figure 4-591. DDRSS_PI_96 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_START_ADDRESS_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1188. DDRSS_PI_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_START_ADDRES_0	R/W	0h	Start BIST checking at this address.

4.3.98 DDRSS_PI_97 Register (Offset = 2184h) [reset = X]

DDRSS_PI_97 is shown in [Figure 4-592](#) and described in [Table 4-1190](#).

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Table 4-1189. DDRSS_PI_97 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2184h

Figure 4-592. DDRSS_PI_97 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PI_MBIST_INIT_PATTERN							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PI_BIST_START_ADDRESS_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1190. DDRSS_PI_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PI_MBIST_INIT_PATTERN	R/W	0h	PI mbist data check, random lfsr pattern mode init pattern seed.
7-3	RESERVED	R/W	X	
2-0	PI_BIST_START_ADDRESS_1	R/W	0h	Start BIST checking at this address.

4.3.99 DDRSS_PI_98 Register (Offset = 2188h) [reset = 0h]

DDRSS_PI_98 is shown in [Figure 4-593](#) and described in [Table 4-1192](#).

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Table 4-1191. DDRSS_PI_98 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2188h

Figure 4-593. DDRSS_PI_98 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_DATA_MASK_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1192. DDRSS_PI_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_DATA_MASK_0	R/W	0h	Mask applied to data for BIST error checking. Bit (0) controls memory data path bit (0), bit (1) controls memory data path bit (1), etc. The mask range is the data transfer size in each memory clock cycle (The data on a rising edge and a failing edge). Set each bit to 1 to mask.

4.3.100 DDRSS_PI_99 Register (Offset = 218Ch) [reset = 0h]

DDRSS_PI_99 is shown in [Figure 4-594](#) and described in [Table 4-1194](#).

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Table 4-1193. DDRSS_PI_99 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 218Ch

Figure 4-594. DDRSS_PI_99 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_DATA_MASK_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1194. DDRSS_PI_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_DATA_MASK_1	R/W	0h	Mask applied to data for BIST error checking. Bit (0) controls memory data path bit (0), bit (1) controls memory data path bit (1), etc. The mask range is the data transfer size in each memory clock cycle (The data on a rising edge and a failing edge). Set each bit to 1 to mask.

4.3.101 DDRSS_PI_100 Register (Offset = 2190h) [reset = X]

DDRSS_PI_100 is shown in [Figure 4-595](#) and described in [Table 4-1196](#).

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Table 4-1195. DDRSS_PI_100 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2190h

Figure 4-595. DDRSS_PI_100 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_BIST_ERR_STOP											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ERR_COUNT											
R/W-X				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1196. DDRSS_PI_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PI_BIST_ERR_STOP	R/W	0h	Defines the maximum number of error occurrences allowed prior to quitting when the BIST_TEST_MODE parameter is set to 1, 2 or 3. A value of 0 will allow the test to run to completion.
15-12	RESERVED	R/W	X	
11-0	PI_BIST_ERR_COUNT	R	0h	Indicates the number of BIST errors found when the BIST_TEST_MODE parameter is set to 1, 2 or 3. READ-ONLY

4.3.102 DDRSS_PI_101 Register (Offset = 2194h) [reset = 0h]

DDRSS_PI_101 is shown in [Figure 4-596](#) and described in [Table 4-1198](#).

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Table 4-1197. DDRSS_PI_101 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2194h

Figure 4-596. DDRSS_PI_101 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_0_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1198. DDRSS_PI_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_0_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.103 DDRSS_PI_102 Register (Offset = 2198h) [reset = X]

DDRSS_PI_102 is shown in [Figure 4-597](#) and described in [Table 4-1200](#).

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Table 4-1199. DDRSS_PI_102 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2198h

Figure 4-597. DDRSS_PI_102 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_0_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1200. DDRSS_PI_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_0_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.104 DDRSS_PI_103 Register (Offset = 219Ch) [reset = 0h]

DDRSS_PI_103 is shown in [Figure 4-598](#) and described in [Table 4-1202](#).

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Table 4-1201. DDRSS_PI_103 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 219Ch

Figure 4-598. DDRSS_PI_103 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_1_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1202. DDRSS_PI_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_1_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.105 DDRSS_PI_104 Register (Offset = 21A0h) [reset = X]

DDRSS_PI_104 is shown in [Figure 4-599](#) and described in [Table 4-1204](#).

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Table 4-1203. DDRSS_PI_104 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21A0h

Figure 4-599. DDRSS_PI_104 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_1_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1204. DDRSS_PI_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_1_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.106 DDRSS_PI_105 Register (Offset = 21A4h) [reset = 0h]

DDRSS_PI_105 is shown in [Figure 4-600](#) and described in [Table 4-1206](#).

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Table 4-1205. DDRSS_PI_105 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21A4h

Figure 4-600. DDRSS_PI_105 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_2_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1206. DDRSS_PI_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_2_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.107 DDRSS_PI_106 Register (Offset = 21A8h) [reset = X]

DDRSS_PI_106 is shown in [Figure 4-601](#) and described in [Table 4-1208](#).

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Table 4-1207. DDRSS_PI_106 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21A8h

Figure 4-601. DDRSS_PI_106 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_2_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1208. DDRSS_PI_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_2_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.108 DDRSS_PI_107 Register (Offset = 21ACh) [reset = 0h]

DDRSS_PI_107 is shown in [Figure 4-602](#) and described in [Table 4-1210](#).

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Table 4-1209. DDRSS_PI_107 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21ACh

Figure 4-602. DDRSS_PI_107 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_3_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1210. DDRSS_PI_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_3_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.109 DDRSS_PI_108 Register (Offset = 21B0h) [reset = X]

DDRSS_PI_108 is shown in [Figure 4-603](#) and described in [Table 4-1212](#).

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Table 4-1211. DDRSS_PI_108 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21B0h

Figure 4-603. DDRSS_PI_108 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_3_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1212. DDRSS_PI_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_3_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.110 DDRSS_PI_109 Register (Offset = 21B4h) [reset = 0h]

DDRSS_PI_109 is shown in [Figure 4-604](#) and described in [Table 4-1214](#).

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Table 4-1213. DDRSS_PI_109 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21B4h

Figure 4-604. DDRSS_PI_109 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_4_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1214. DDRSS_PI_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_4_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.111 DDRSS_PI_110 Register (Offset = 21B8h) [reset = X]

DDRSS_PI_110 is shown in [Figure 4-605](#) and described in [Table 4-1216](#).

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Table 4-1215. DDRSS_PI_110 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21B8h

Figure 4-605. DDRSS_PI_110 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_4_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1216. DDRSS_PI_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_4_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.112 DDRSS_PI_111 Register (Offset = 21BCh) [reset = 0h]

DDRSS_PI_111 is shown in [Figure 4-606](#) and described in [Table 4-1218](#).

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Table 4-1217. DDRSS_PI_111 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21BCh

Figure 4-606. DDRSS_PI_111 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_5_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1218. DDRSS_PI_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_5_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.113 DDRSS_PI_112 Register (Offset = 21C0h) [reset = X]

DDRSS_PI_112 is shown in [Figure 4-607](#) and described in [Table 4-1220](#).

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Table 4-1219. DDRSS_PI_112 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21C0h

Figure 4-607. DDRSS_PI_112 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_5_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1220. DDRSS_PI_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_5_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.114 DDRSS_PI_113 Register (Offset = 21C4h) [reset = 0h]

DDRSS_PI_113 is shown in [Figure 4-608](#) and described in [Table 4-1222](#).

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Table 4-1221. DDRSS_PI_113 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21C4h

Figure 4-608. DDRSS_PI_113 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_6_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1222. DDRSS_PI_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_6_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.115 DDRSS_PI_114 Register (Offset = 21C8h) [reset = X]

DDRSS_PI_114 is shown in [Figure 4-609](#) and described in [Table 4-1224](#).

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Table 4-1223. DDRSS_PI_114 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21C8h

Figure 4-609. DDRSS_PI_114 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_6_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1224. DDRSS_PI_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_6_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.116 DDRSS_PI_115 Register (Offset = 21CCh) [reset = 0h]

DDRSS_PI_115 is shown in [Figure 4-610](#) and described in [Table 4-1226](#).

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Table 4-1225. DDRSS_PI_115 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21CCh

Figure 4-610. DDRSS_PI_115 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_7_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1226. DDRSS_PI_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_7_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.117 DDRSS_PI_116 Register (Offset = 21D0h) [reset = X]

DDRSS_PI_116 is shown in [Figure 4-611](#) and described in [Table 4-1228](#).

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Table 4-1227. DDRSS_PI_116 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21D0h

Figure 4-611. DDRSS_PI_116 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_7_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1228. DDRSS_PI_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_7_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.118 DDRSS_PI_117 Register (Offset = 21D4h) [reset = 0h]

DDRSS_PI_117 is shown in [Figure 4-612](#) and described in [Table 4-1230](#).

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Table 4-1229. DDRSS_PI_117 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21D4h

Figure 4-612. DDRSS_PI_117 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_8_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1230. DDRSS_PI_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_8_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.119 DDRSS_PI_118 Register (Offset = 21D8h) [reset = X]

DDRSS_PI_118 is shown in [Figure 4-613](#) and described in [Table 4-1232](#).

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Table 4-1231. DDRSS_PI_118 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21D8h

Figure 4-613. DDRSS_PI_118 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_8_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1232. DDRSS_PI_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_8_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.120 DDRSS_PI_119 Register (Offset = 21DCh) [reset = 0h]

DDRSS_PI_119 is shown in [Figure 4-614](#) and described in [Table 4-1234](#).

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Table 4-1233. DDRSS_PI_119 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21DCh

Figure 4-614. DDRSS_PI_119 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_ADDR_MASK_9_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1234. DDRSS_PI_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_ADDR_MASK_9_0	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.121 DDRSS_PI_120 Register (Offset = 21E0h) [reset = X]

DDRSS_PI_120 is shown in Figure 4-615 and described in Table 4-1236.

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Table 4-1235. DDRSS_PI_120 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21E0h

Figure 4-615. DDRSS_PI_120 Register

31	30	29	28	27	26	25	24
RESERVED						PI_BIST_PAT_MODE	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_BIST_ADDR_MODE	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_BIST_MODE	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_ADDR_MASK_9_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1236. DDRSS_PI_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_BIST_PAT_MODE	R/W	0h	Sets the pattern mode of BIST. 'b00 indicates using built-in pattern. 'b01 indicates checkerboard pattern, each data transfer inverts the last data transfer based on the built-in pattern. 'b10 indicates using both user pattern and built-in pattern. 'b11 indicates using pi lfsr random pattern.
23-18	RESERVED	R/W	X	
17-16	PI_BIST_ADDR_MODE	R/W	0h	Sets the address traversing order of BIST. 'b00 indicates fast column order (burst-column-bank-row-rank). 'b01 indicates fast row order (burst-row-column-bank-rank). 'b10 indicates fast bank order (burst-bank-column-row-rank).
15-11	RESERVED	R/W	X	
10-8	PI_BIST_MODE	R/W	0h	Sets the BIST data checking mode. 'b00 indicates MOV113N mode. 'b01 indicates March C mode. 'b10 indicates GALPAT mode. 'b11 indicates PRBS mode. 'b100 indicates programmable March data check mode.
7-4	RESERVED	R/W	X	
3-0	PI_BIST_ADDR_MASK_9_1	R/W	0h	Defines an address to be masked during the BIST operation..

4.3.122 DDRSS_PI_121 Register (Offset = 21E4h) [reset = 0h]

DDRSS_PI_121 is shown in [Figure 4-616](#) and described in [Table 4-1238](#).

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Table 4-1237. DDRSS_PI_121 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21E4h

Figure 4-616. DDRSS_PI_121 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1238. DDRSS_PI_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_USER_PAT_0	R/W	0h	Sets the user-specified pattern of BIST.

4.3.123 DDRSS_PI_122 Register (Offset = 21E8h) [reset = 0h]

DDRSS_PI_122 is shown in [Figure 4-617](#) and described in [Table 4-1240](#).

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Table 4-1239. DDRSS_PI_122 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21E8h

Figure 4-617. DDRSS_PI_122 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1240. DDRSS_PI_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_USER_PAT_1	R/W	0h	Sets the user-specified pattern of BIST.

4.3.124 DDRSS_PI_123 Register (Offset = 21ECh) [reset = 0h]

DDRSS_PI_123 is shown in [Figure 4-618](#) and described in [Table 4-1242](#).

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Table 4-1241. DDRSS_PI_123 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21ECh

Figure 4-618. DDRSS_PI_123 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1242. DDRSS_PI_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_USER_PAT_2	R/W	0h	Sets the user-specified pattern of BIST.

4.3.125 DDRSS_PI_124 Register (Offset = 21F0h) [reset = 0h]

DDRSS_PI_124 is shown in [Figure 4-619](#) and described in [Table 4-1244](#).

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Table 4-1243. DDRSS_PI_124 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21F0h

Figure 4-619. DDRSS_PI_124 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_BIST_USER_PAT_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1244. DDRSS_PI_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_BIST_USER_PAT_3	R/W	0h	Sets the user-specified pattern of BIST.

4.3.126 DDRSS_PI_125 Register (Offset = 21F4h) [reset = X]

DDRSS_PI_125 is shown in [Figure 4-620](#) and described in [Table 4-1246](#).

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Table 4-1245. DDRSS_PI_125 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21F4h

Figure 4-620. DDRSS_PI_125 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_BIST_PAT_NUM			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1246. DDRSS_PI_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PI_BIST_PAT_NUM	R/W	0h	Sets the max used pattern number of BIST from a total of 8 built-in patterns. Ex. set to 3, The BIST would use pattern 1, 2 and 3.

4.3.127 DDRSS_PI_126 Register (Offset = 21F8h) [reset = X]

DDRSS_PI_126 is shown in [Figure 4-621](#) and described in [Table 4-1248](#).

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Table 4-1247. DDRSS_PI_126 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21F8h

Figure 4-621. DDRSS_PI_126 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_0																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1248. DDRSS_PI_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_0	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.128 DDRSS_PI_127 Register (Offset = 21FCh) [reset = X]

DDRSS_PI_127 is shown in [Figure 4-622](#) and described in [Table 4-1250](#).

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Table 4-1249. DDRSS_PI_127 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 21FCh

Figure 4-622. DDRSS_PI_127 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_1																													
R/W-X		R/W-0h																													

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1250. DDRSS_PI_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_1	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.129 DDRSS_PI_128 Register (Offset = 2200h) [reset = X]

DDRSS_PI_128 is shown in [Figure 4-623](#) and described in [Table 4-1252](#).

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Table 4-1251. DDRSS_PI_128 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2200h

Figure 4-623. DDRSS_PI_128 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_2																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1252. DDRSS_PI_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_2	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.130 DDRSS_PI_129 Register (Offset = 2204h) [reset = X]

DDRSS_PI_129 is shown in [Figure 4-624](#) and described in [Table 4-1254](#).

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Table 4-1253. DDRSS_PI_129 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2204h

Figure 4-624. DDRSS_PI_129 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE	RVED	PI_BIST_STAGE_3																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1254. DDRSS_PI_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_3	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.131 DDRSS_PI_130 Register (Offset = 2208h) [reset = X]

DDRSS_PI_130 is shown in [Figure 4-625](#) and described in [Table 4-1256](#).

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Table 4-1255. DDRSS_PI_130 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2208h

Figure 4-625. DDRSS_PI_130 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_4																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1256. DDRSS_PI_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_4	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.132 DDRSS_PI_131 Register (Offset = 220Ch) [reset = X]

DDRSS_PI_131 is shown in [Figure 4-626](#) and described in [Table 4-1258](#).

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Table 4-1257. DDRSS_PI_131 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 220Ch

Figure 4-626. DDRSS_PI_131 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_5																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1258. DDRSS_PI_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_5	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.133 DDRSS_PI_132 Register (Offset = 2210h) [reset = X]

DDRSS_PI_132 is shown in [Figure 4-627](#) and described in [Table 4-1260](#).

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Table 4-1259. DDRSS_PI_132 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2210h

Figure 4-627. DDRSS_PI_132 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_6																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1260. DDRSS_PI_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_6	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.134 DDRSS_PI_133 Register (Offset = 2214h) [reset = X]

DDRSS_PI_133 is shown in [Figure 4-628](#) and described in [Table 4-1262](#).

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Table 4-1261. DDRSS_PI_133 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2214h

Figure 4-628. DDRSS_PI_133 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE RVED		PI_BIST_STAGE_7																													
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1262. DDRSS_PI_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PI_BIST_STAGE_7	R/W	0h	Sets the programmable algorithm of each stage X when pi_bist_mmode = 'h4.

4.3.135 DDRSS_PI_134 Register (Offset = 2218h) [reset = X]

DDRSS_PI_134 is shown in [Figure 4-629](#) and described in [Table 4-1264](#).

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Table 4-1263. DDRSS_PI_134 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2218h

Figure 4-629. DDRSS_PI_134 Register

31	30	29	28	27	26	25	24
RESERVED							PI_SREFRESH_EXIT_NO_REFRESH
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_PWRUP_SREFRESH_EXIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_SELF_REFRESH_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				PI_COL_DIFF			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1264. DDRSS_PI_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_SREFRESH_EXIT_NO_REFRESH	R/W	0h	Disables the automatic refresh request associated with self-refresh exit. Set to 1 to disable.
23-17	RESERVED	R/W	X	
16	PI_PWRUP_SREFRESH_EXIT	R/W	0h	Allow powerup via self-refresh instead of full memory initialization. Set to 1 to enable.
15-9	RESERVED	R/W	X	
8	PI_SELF_REFRESH_EN	R/W	0h	Control for PI to enable self refresh mode. Set to 1 to enable.
7-4	RESERVED	R/W	X	
3-0	PI_COL_DIFF	R/W	0h	Difference between number of column pins available and number being used.

4.3.136 DDRSS_PI_135 Register (Offset = 221Ch) [reset = X]

DDRSS_PI_135 is shown in Figure 4-630 and described in Table 4-1266.

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Table 4-1265. DDRSS_PI_135 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 221Ch

Figure 4-630. DDRSS_PI_135 Register

31	30	29	28	27	26	25	24
RESERVED							PI_NO_PHY_IN D_TRAIN_INIT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_NO_MRW_I NIT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_NO_MRW_ BT_INIT
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_SREF_ENT RY_REQ
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1266. DDRSS_PI_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_NO_PHY_IND_TRAIN_INIT	R/W	0h	Disable PHY Independent Training during initialization. Set to 1 to disable.
23-17	RESERVED	R/W	X	
16	PI_NO_MRW_INIT	R/W	0h	Disable MRW commands after training during initialization. Set to 1 to disable.
15-9	RESERVED	R/W	X	
8	PI_NO_MRW_BT_INIT	R/W	0h	Disable MRW commands before training during initialization. Set to 1 to disable.
7-1	RESERVED	R/W	X	
0	PI_SREF_ENTRY_REQ	W	0h	In PI power up data retention, PI can issued sref entry command. WRITE-ONLY

4.3.137 DDRSS_PI_136 Register (Offset = 2220h) [reset = X]

DDRSS_PI_136 is shown in [Figure 4-631](#) and described in [Table 4-1268](#).

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Table 4-1267. DDRSS_PI_136 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2220h

Figure 4-631. DDRSS_PI_136 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PI_NO_AUTO_MRR_INIT
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1268. DDRSS_PI_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PI_NO_AUTO_MRR_INIT	R/W	0h	Disable MRR commands during initialization. Set to 1 to disable.

4.3.138 DDRSS_PI_137 Register (Offset = 2224h) [reset = 0h]

DDRSS_PI_137 is shown in [Figure 4-632](#) and described in [Table 4-1270](#).

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Table 4-1269. DDRSS_PI_137 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2224h

Figure 4-632. DDRSS_PI_137 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRST_PWRON																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1270. DDRSS_PI_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TRST_PWRON	R/W	0h	Duration of memory reset during power-on initialization.

4.3.139 DDRSS_PI_138 Register (Offset = 2228h) [reset = 0h]

DDRSS_PI_138 is shown in [Figure 4-633](#) and described in [Table 4-1272](#).

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Table 4-1271. DDRSS_PI_138 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2228h

Figure 4-633. DDRSS_PI_138 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_CKE_INACTIVE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1272. DDRSS_PI_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_CKE_INACTIVE	R/W	0h	Number of cycles after reset before CKE will be active.

4.3.140 DDRSS_PI_139 Register (Offset = 222Ch) [reset = X]

DDRSS_PI_139 is shown in [Figure 4-634](#) and described in [Table 4-1274](#).

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Table 4-1273. DDRSS_PI_139 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 222Ch

Figure 4-634. DDRSS_PI_139 Register

31	30	29	28	27	26	25	24
PI_DLL_RST_DELAY							
R/W-0h							
23	22	21	20	19	18	17	16
PI_DLL_RST_DELAY							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PI_DRAM_INIT_EN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_DLL_RST
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1274. DDRSS_PI_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PI_DLL_RST_DELAY	R/W	0h	Minimum cycles required for DLL reset signal dll_rst_n to be held.
15-9	RESERVED	R/W	X	
8	PI_DRAM_INIT_EN	R/W	0h	Control for the initialization of DRAM by the PI.
7-1	RESERVED	R/W	X	
0	PI_DLL_RST	R/W	0h	Enables use of the DLL reset (dll_rst_n).

4.3.141 DDRSS_PI_140 Register (Offset = 2230h) [reset = X]

DDRSS_PI_140 is shown in [Figure 4-635](#) and described in [Table 4-1276](#).

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Table 4-1275. DDRSS_PI_140 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2230h

Figure 4-635. DDRSS_PI_140 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_DLL_RST_ADJ_DLY							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1276. DDRSS_PI_140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	PI_DLL_RST_ADJ_DLY	R/W	0h	Minimum cycles after setting master delay in DLL until the DLL reset signal dll_rst_n may be asserted.

4.3.142 DDRSS_PI_141 Register (Offset = 2234h) [reset = X]

DDRSS_PI_141 is shown in [Figure 4-636](#) and described in [Table 4-1278](#).

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Table 4-1277. DDRSS_PI_141 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2234h

Figure 4-636. DDRSS_PI_141 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_WRITE_MODEREG																									
R/W-X						R/W-0h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1278. DDRSS_PI_141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-0	PI_WRITE_MODEREG	R/W	0h	Write memory mode register data to the DRAMs. Bits (7:0) define the memory mode register number if bit (23) is set, bits (15:8) define the chip select if bit (24) is clear, bits (23:16) define which memory mode register/s to write, bit (24) defines whether all chip selects will be written, and bit (25) triggers the write.

4.3.143 DDRSS_PI_142 Register (Offset = 2238h) [reset = X]

DDRSS_PI_142 is shown in [Figure 4-637](#) and described in [Table 4-1280](#).

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Table 4-1279. DDRSS_PI_142 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2238h

Figure 4-637. DDRSS_PI_142 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PI_READ_MODEREG							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_READ_MODEREG								PI_MRW_STATUS							
R/W-0h								R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1280. DDRSS_PI_142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-8	PI_READ_MODEREG	R/W	0h	Read the specified memory mode register from specified chip when start bit set. Bits (7:0) define the memory mode register and bits (15:8) define the chip select. Set bit (16) to 1 to trigger.
7-0	PI_MRW_STATUS	R	0h	Write memory mode register status. Bit (0) set indicates a WRITE_MODEREG parameter programming error. Bit (1) set indicates a PASR error. Bit (2) is Reserved. Bit (3) set indicates a self refresh or deep power down error. Bit (4) set indicates that a write to MR3 or MR11 was attempted (write_modereg bit (25) was asserted with bit (17) set, or bit (23) was asserted with bits (7:0) defining MR3 or MR11) during tZQCAL after a ZQ calibration start command. READ-ONLY

4.3.144 DDRSS_PI_143 Register (Offset = 223Ch) [reset = X]

DDRSS_PI_143 is shown in [Figure 4-638](#) and described in [Table 4-1282](#).

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Table 4-1281. DDRSS_PI_143 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 223Ch

Figure 4-638. DDRSS_PI_143 Register

31	30	29	28	27	26	25	24
RESERVED							PI_NO_ZQ_INIT
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PI_PERIPHERAL_MRR_DATA_0							
R-0h							
15	14	13	12	11	10	9	8
PI_PERIPHERAL_MRR_DATA_0							
R-0h							
7	6	5	4	3	2	1	0
PI_PERIPHERAL_MRR_DATA_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1282. DDRSS_PI_143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_NO_ZQ_INIT	R/W	0h	Disable ZQ operations during initialization. Set to 1 to disable.
23-0	PI_PERIPHERAL_MRR_DATA_0	R	0h	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter, Bits (15:0) indicate the MRR data, (23:16) indicate the chip select. READ-ONLY

4.3.145 DDRSS_PI_144 Register (Offset = 2240h) [reset = X]

DDRSS_PI_144 is shown in [Figure 4-639](#) and described in [Table 4-1284](#).

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Table 4-1283. DDRSS_PI_144 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2240h

Figure 4-639. DDRSS_PI_144 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_ZQ_REQ_P ENDING
R/W-X							R-0h
15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R/W-X				W-0h			
7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1284. DDRSS_PI_144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	PI_ZQ_REQ_PENDING	R	0h	Indicates that a ZQ command is currently in progress or waiting to run. When this is asserted, no writes to ZQ_REQ should occur. READ-ONLY
15-12	RESERVED	R/W	X	
11-8	RESERVED	W	0h	Reserved
7-4	RESERVED	R/W	X	
3-0	RESERVED	R/W	0h	Reserved

4.3.146 DDRSS_PI_145 Register (Offset = 2244h) [reset = X]

DDRSS_PI_145 is shown in [Figure 4-640](#) and described in [Table 4-1286](#).

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Table 4-1285. DDRSS_PI_145 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2244h

Figure 4-640. DDRSS_PI_145 Register

31	30	29	28	27	26	25	24
PI_MONITOR_0							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							PI_MONITOR_CAP_SEL_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PI_MONITOR_SRC_SEL_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED					RESERVED		
R/W-X					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1286. DDRSS_PI_145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MONITOR_0	R	0h	Monitor register 0. READ-ONLY.
23-17	RESERVED	R/W	X	
16	PI_MONITOR_CAP_SEL_0	R/W	0h	Selection of captures for pi_monitor_0.
15-12	RESERVED	R/W	X	
11-8	PI_MONITOR_SRC_SEL_0	R/W	0h	Selection of sources for pi_monitor_0.
7-3	RESERVED	R/W	X	
2-0	RESERVED	R/W	0h	Reserved

4.3.147 DDRSS_PI_146 Register (Offset = 2248h) [reset = X]

DDRSS_PI_146 is shown in [Figure 4-641](#) and described in [Table 4-1288](#).

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Table 4-1287. DDRSS_PI_146 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2248h

Figure 4-641. DDRSS_PI_146 Register

31	30	29	28	27	26	25	24
RESERVED				PI_MONITOR_SRC_SEL_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PI_MONITOR_1							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PI_MONITOR_CAP_SEL_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PI_MONITOR_SRC_SEL_1			
R/W-X				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1288. DDRSS_PI_146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_MONITOR_SRC_SEL_2	R/W	0h	Selection of sources for pi_monitor_2.
23-16	PI_MONITOR_1	R	0h	Monitor register 1. READ-ONLY.
15-9	RESERVED	R/W	X	
8	PI_MONITOR_CAP_SEL_1	R/W	0h	Selection of captures for pi_monitor_1.
7-4	RESERVED	R/W	X	
3-0	PI_MONITOR_SRC_SEL_1	R/W	0h	Selection of sources for pi_monitor_1.

4.3.148 DDRSS_PI_147 Register (Offset = 224Ch) [reset = X]

DDRSS_PI_147 is shown in [Figure 4-642](#) and described in [Table 4-1290](#).

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Table 4-1289. DDRSS_PI_147 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 224Ch

Figure 4-642. DDRSS_PI_147 Register

31	30	29	28	27	26	25	24
RESERVED							PI_MONITOR_CAP_SEL_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PI_MONITOR_SRC_SEL_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_MONITOR_2							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PI_MONITOR_CAP_SEL_2
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1290. DDRSS_PI_147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_MONITOR_CAP_SEL_3	R/W	0h	Selection of captures for pi_monitor_3.
23-20	RESERVED	R/W	X	
19-16	PI_MONITOR_SRC_SEL_3	R/W	0h	Selection of sources for pi_monitor_3.
15-8	PI_MONITOR_2	R	0h	Monitor register 2. READ-ONLY.
7-1	RESERVED	R/W	X	
0	PI_MONITOR_CAP_SEL_2	R/W	0h	Selection of captures for pi_monitor_2.

4.3.149 DDRSS_PI_148 Register (Offset = 2250h) [reset = X]

DDRSS_PI_148 is shown in [Figure 4-643](#) and described in [Table 4-1292](#).

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Table 4-1291. DDRSS_PI_148 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2250h

Figure 4-643. DDRSS_PI_148 Register

31	30	29	28	27	26	25	24
PI_MONITOR_4							
R-0h							
23	22	21	20	19	18	17	16
RESERVED						PI_MONITOR_CAP_SEL_4	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PI_MONITOR_SRC_SEL_4			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PI_MONITOR_3							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1292. DDRSS_PI_148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MONITOR_4	R	0h	Monitor register 4. READ-ONLY.
23-17	RESERVED	R/W	X	
16	PI_MONITOR_CAP_SEL_4	R/W	0h	Selection of captures for pi_monitor_4.
15-12	RESERVED	R/W	X	
11-8	PI_MONITOR_SRC_SEL_4	R/W	0h	Selection of sources for pi_monitor_4.
7-0	PI_MONITOR_3	R	0h	Monitor register 3. READ-ONLY.

4.3.150 DDRSS_PI_149 Register (Offset = 2254h) [reset = X]

DDRSS_PI_149 is shown in [Figure 4-644](#) and described in [Table 4-1294](#).

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Table 4-1293. DDRSS_PI_149 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2254h

Figure 4-644. DDRSS_PI_149 Register

31	30	29	28	27	26	25	24
RESERVED				PI_MONITOR_SRC_SEL_6			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PI_MONITOR_5							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PI_MONITOR_CAP_SEL_5	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PI_MONITOR_SRC_SEL_5			
R/W-X				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1294. DDRSS_PI_149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_MONITOR_SRC_SEL_6	R/W	0h	Selection of sources for pi_monitor_6.
23-16	PI_MONITOR_5	R	0h	Monitor register 5. READ-ONLY.
15-9	RESERVED	R/W	X	
8	PI_MONITOR_CAP_SEL_5	R/W	0h	Selection of captures for pi_monitor_5.
7-4	RESERVED	R/W	X	
3-0	PI_MONITOR_SRC_SEL_5	R/W	0h	Selection of sources for pi_monitor_5.

4.3.151 DDRSS_PI_150 Register (Offset = 2258h) [reset = X]

DDRSS_PI_150 is shown in [Figure 4-645](#) and described in [Table 4-1296](#).

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Table 4-1295. DDRSS_PI_150 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2258h

Figure 4-645. DDRSS_PI_150 Register

31	30	29	28	27	26	25	24
RESERVED							PI_MONITOR_CAP_SEL_7
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PI_MONITOR_SRC_SEL_7			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_MONITOR_6							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PI_MONITOR_CAP_SEL_6
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1296. DDRSS_PI_150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_MONITOR_CAP_SEL_7	R/W	0h	Selection of captures for pi_monitor_7.
23-20	RESERVED	R/W	X	
19-16	PI_MONITOR_SRC_SEL_7	R/W	0h	Selection of sources for pi_monitor_7.
15-8	PI_MONITOR_6	R	0h	Monitor register 6. READ-ONLY.
7-1	RESERVED	R/W	X	
0	PI_MONITOR_CAP_SEL_6	R/W	0h	Selection of captures for pi_monitor_6.

4.3.152 DDRSS_PI_151 Register (Offset = 225Ch) [reset = X]

DDRSS_PI_151 is shown in [Figure 4-646](#) and described in [Table 4-1298](#).

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Table 4-1297. DDRSS_PI_151 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 225Ch

Figure 4-646. DDRSS_PI_151 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_MONITOR_7							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1298. DDRSS_PI_151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	PI_MONITOR_7	R	0h	Monitor register 7. READ-ONLY.

4.3.153 DDRSS_PI_152 Register (Offset = 2260h) [reset = X]

DDRSS_PI_152 is shown in [Figure 4-647](#) and described in [Table 4-1300](#).

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Table 4-1299. DDRSS_PI_152 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2260h

Figure 4-647. DDRSS_PI_152 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_MONITOR_STROBE							
W-X								W-0h							

LEGEND: W = Write Only; -n = value after reset

Table 4-1300. DDRSS_PI_152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	W	X	
7-0	PI_MONITOR_STROBE	W	0h	Strobe the pi_monitor once. Every bit corresponds respectively with a pi_monitor. WRITE-ONLY

4.3.154 DDRSS_PI_153 Register (Offset = 2264h) [reset = X]

DDRSS_PI_153 is shown in [Figure 4-648](#) and described in [Table 4-1302](#).

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Table 4-1301. DDRSS_PI_153 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2264h

Figure 4-648. DDRSS_PI_153 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED			PI_FREQ_RETENTION_NUM				
R/W-X			R/W-0h				
15	14	13	12	11	10	9	8
RESERVED			PI_FREQ_NUMBER_STATUS				
R/W-X			R-0h				
7	6	5	4	3	2	1	0
RESERVED							PI_DLL_LOCK
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1302. DDRSS_PI_153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-21	RESERVED	R/W	X	
20-16	PI_FREQ_RETENTION_NUM	R/W	0h	Monitor active freq number in PI for data_retention
15-13	RESERVED	R/W	X	
12-8	PI_FREQ_NUMBER_STATUS	R	0h	Monitor active freq number in PI. READ-ONLY.
7-1	RESERVED	R/W	X	
0	PI_DLL_LOCK	R	0h	Monitor dfi_init_complete from PHY. READ-ONLY.

4.3.155 DDRSS_PI_154 Register (Offset = 2268h) [reset = X]

DDRSS_PI_154 is shown in [Figure 4-649](#) and described in [Table 4-1304](#).

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Table 4-1303. DDRSS_PI_154 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2268h

Figure 4-649. DDRSS_PI_154 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_POWER_RE DUC_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PI_PHYMSTR_TYPE	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1304. DDRSS_PI_154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	PI_POWER_REduc_EN	R/W	0h	PI Power reduction enable, 1 = enabled.
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-2	RESERVED	R/W	X	
1-0	PI_PHYMSTR_TYPE	R/W	0h	Defines how the controller should set the state of DRAM before turning control of the DFI bus over to the PI.

4.3.156 DDRSS_PI_155 Register (Offset = 226Ch) [reset = X]

DDRSS_PI_155 is shown in [Figure 4-650](#) and described in [Table 4-1306](#).

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Table 4-1305. DDRSS_PI_155 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 226Ch

Figure 4-650. DDRSS_PI_155 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1306. DDRSS_PI_155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.3.157 DDRSS_PI_156 Register (Offset = 2270h) [reset = X]

DDRSS_PI_156 is shown in [Figure 4-651](#) and described in [Table 4-1308](#).

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Table 4-1307. DDRSS_PI_156 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2270h

Figure 4-651. DDRSS_PI_156 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1308. DDRSS_PI_156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.3.158 DDRSS_PI_157 Register (Offset = 2274h) [reset = X]

DDRSS_PI_157 is shown in [Figure 4-652](#) and described in [Table 4-1310](#).

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Table 4-1309. DDRSS_PI_157 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2274h

Figure 4-652. DDRSS_PI_157 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1310. DDRSS_PI_157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.3.159 DDRSS_PI_158 Register (Offset = 2278h) [reset = X]

DDRSS_PI_158 is shown in [Figure 4-653](#) and described in [Table 4-1312](#).

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Table 4-1311. DDRSS_PI_158 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2278h

Figure 4-653. DDRSS_PI_158 Register

31	30	29	28	27	26	25	24
RESERVED							RESERVED
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							RESERVED
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1312. DDRSS_PI_158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RESERVED	R/W	0h	Reserved
23-17	RESERVED	R/W	X	
16	RESERVED	R/W	0h	Reserved
15-9	RESERVED	R/W	X	
8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	RESERVED	R/W	0h	Reserved

4.3.160 DDRSS_PI_159 Register (Offset = 227Ch) [reset = X]

DDRSS_PI_159 is shown in [Figure 4-654](#) and described in [Table 4-1314](#).

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Table 4-1313. DDRSS_PI_159 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 227Ch

Figure 4-654. DDRSS_PI_159 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PI_TRE FBW _THR
R/W-X															R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRE FBW _THR								PI_WRLVL_MAX_STROBE_PEND							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1314. DDRSS_PI_159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16-8	PI_TRE FBW _THR	R/W	0h	Threshold value to control the AREF command interval. When the number of pending AREF is over this value, the interval is expanded to be tREF/8.
7-0	PI_WRLVL_MAX_STROBE_PEND	R/W	0h	Defines the maximum number of wrvl_strobes that be accumulated before an AREF is prevented from being generated.

4.3.161 DDRSS_PI_160 Register (Offset = 2280h) [reset = X]

DDRSS_PI_160 is shown in [Figure 4-655](#) and described in [Table 4-1316](#).

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Table 4-1315. DDRSS_PI_160 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2280h

Figure 4-655. DDRSS_PI_160 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PI_FREQ_CHANGE_REG_COPY			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1316. DDRSS_PI_160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	PI_FREQ_CHANGE_REG_COPY	R/W	0h	In non-DFI 4.0 mode, contains the frequency copy value.

4.3.162 DDRSS_PI_161 Register (Offset = 2284h) [reset = X]

DDRSS_PI_161 is shown in Figure 4-656 and described in Table 4-1318.

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Table 4-1317. DDRSS_PI_161 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2284h

Figure 4-656. DDRSS_PI_161 Register

31	30	29	28	27	26	25	24
RESERVED				PI_CATR			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PI_PARALLEL_CALVL_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PI_FREQ_SEL_FROM_REGIF
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1318. DDRSS_PI_161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_CATR	R/W	0h	It indicates LP4 DRAM CA termination ON/OFF state. Each bit corresponds to each chip select. 1:ON 0:OFF. This parameter is active when PI_NO_CATR_READ==1. When PI_NO_CATR_READ==0, this param is inactive
23-17	RESERVED	R/W	X	
16	PI_PARALLEL_CALVL_EN	R/W	0h	Enable parallel channel CA training for LPDDR4. 1: All the channels in one rank do CA Training in parallel. 0: Each channel does CA Training in sequence
15-13	RESERVED	R/W	X	
12-8	RESERVED	R/W	0h	Reserved
7-1	RESERVED	R/W	X	
0	PI_FREQ_SEL_FROM_REGIF	R/W	0h	In non-DFI 4.0 mode, user select the frequency copies from pi_freq_change_reg_copy.

4.3.163 DDRSS_PI_162 Register (Offset = 2288h) [reset = X]

DDRSS_PI_162 is shown in [Figure 4-657](#) and described in [Table 4-1320](#).

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Table 4-1319. DDRSS_PI_162 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2288h

Figure 4-657. DDRSS_PI_162 Register

31	30	29	28	27	26	25	24
RESERVED							PI_NOTCARE_MC_INIT_START
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PI_DISCONNECT_MC
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PI_MASK_INIT_COMPLETE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PI_NO_CATR_READ
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1320. DDRSS_PI_162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_NOTCARE_MC_INIT_START	R/W	0h	Defines whether PI waits for the controller to initiate dfi_init_start before PI memory initialization, 1: wait for dfi_init_start
23-17	RESERVED	R/W	X	
16	PI_DISCONNECT_MC	R/W	0h	PI disconnects the controller from the PHY, 1: disconnect
15-9	RESERVED	R/W	X	
8	PI_MASK_INIT_COMPLETE	R/W	0h	Enable the masking of the dfi_init_complete signal back to the controller, 1: mask.
7-1	RESERVED	R/W	X	
0	PI_NO_CATR_READ	R/W	0h	Defines how the LPDDR4 termination status is determined. 1: PI use PI_CATR to get DRAM CA Termination status. 0: PI reads DRAM MR0.OP7 to get DRAM CA Termination status.

4.3.164 DDRSS_PI_163 Register (Offset = 228Ch) [reset = X]

DDRSS_PI_163 is shown in [Figure 4-658](#) and described in [Table 4-1322](#).

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Table 4-1321. DDRSS_PI_163 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 228Ch

Figure 4-658. DDRSS_PI_163 Register

31	30	29	28	27	26	25	24
PI_TSDO_F2							
R/W-0h							
23	22	21	20	19	18	17	16
PI_TSDO_F1							
R/W-0h							
15	14	13	12	11	10	9	8
PI_TSDO_F0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PI_TRACE_MC_MR13
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1322. DDRSS_PI_163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TSDO_F2	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 2, in PI clocks
23-16	PI_TSDO_F1	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 1, in PI clocks
15-8	PI_TSDO_F0	R/W	0h	The delay from the read preamble training MRS command to the data strobe drive out for frequency set 0, in PI clocks
7-1	RESERVED	R/W	X	
0	PI_TRACE_MC_MR13	R/W	0h	Defines whether PI monitors controller mr13 mrw or not. 1: monitor mc mr13 mrw and update the op7 and op6 in PI_MR13_DATA.

4.3.165 DDRSS_PI_164 Register (Offset = 2290h) [reset = X]

DDRSS_PI_164 is shown in [Figure 4-659](#) and described in [Table 4-1324](#).

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Table 4-1323. DDRSS_PI_164 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2290h

Figure 4-659. DDRSS_PI_164 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1324. DDRSS_PI_164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	PI_TDELAY_RDWR_2_B US_IDLE_F0	R/W	0h	The delay from read or write to bus idle for frequency set 0. Recommend setting is: delay time from read command issued to last read data received.

4.3.166 DDRSS_PI_165 Register (Offset = 2294h) [reset = X]

DDRSS_PI_165 is shown in [Figure 4-660](#) and described in [Table 4-1326](#).

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Table 4-1325. DDRSS_PI_165 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2294h

Figure 4-660. DDRSS_PI_165 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1326. DDRSS_PI_165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	PI_TDELAY_RDWR_2_B US_IDLE_F1	R/W	0h	The delay from read or write to bus idle for frequency set 1. Recommend setting is: delay time from read command issued to last read data received.

4.3.167 DDRSS_PI_166 Register (Offset = 2298h) [reset = X]

DDRSS_PI_166 is shown in [Figure 4-661](#) and described in [Table 4-1328](#).

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Table 4-1327. DDRSS_PI_166 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2298h

Figure 4-661. DDRSS_PI_166 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PI_ZQINIT_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_ZQINIT_F0							
R/W-0h							
7	6	5	4	3	2	1	0
PI_TDELAY_RDWR_2_BUS_IDLE_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1328. DDRSS_PI_166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	PI_ZQINIT_F0	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 0.
7-0	PI_TDELAY_RDWR_2_B US_IDLE_F2	R/W	0h	The delay from read or write to bus idle for frequency set 2. Recommend setting is: delay time from read command issued to last read data received.

4.3.168 DDRSS_PI_167 Register (Offset = 229Ch) [reset = X]

DDRSS_PI_167 is shown in [Figure 4-662](#) and described in [Table 4-1330](#).

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Table 4-1329. DDRSS_PI_167 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 229Ch

Figure 4-662. DDRSS_PI_167 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_ZQINIT_F2											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PI_ZQINIT_F1											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1330. DDRSS_PI_167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PI_ZQINIT_F2	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 2.
15-12	RESERVED	R/W	X	
11-0	PI_ZQINIT_F1	R/W	0h	Number of cycles needed for a ZQINIT command for frequency set 1.

4.3.169 DDRSS_PI_168 Register (Offset = 22A0h) [reset = X]

DDRSS_PI_168 is shown in [Figure 4-663](#) and described in [Table 4-1332](#).

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Table 4-1331. DDRSS_PI_168 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22A0h

Figure 4-663. DDRSS_PI_168 Register

31	30	29	28	27	26	25	24
RESERVED	PI_CASLAT_LIN_F1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WRLAT_F1						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PI_CASLAT_LIN_F0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	PI_WRLAT_F0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1332. DDRSS_PI_168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_CASLAT_LIN_F1	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 1. Bit (0) is half-cycle increment and the upper bits define memory CAS latency for the controller.
23	RESERVED	R/W	X	
22-16	PI_WRLAT_F1	R/W	0h	DRAM WRLAT value in cycles for frequency set 1.
15	RESERVED	R/W	X	
14-8	PI_CASLAT_LIN_F0	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 0. Bit (0) is half-cycle increment and the upper bits define memory CAS latency for the controller.
7	RESERVED	R/W	X	
6-0	PI_WRLAT_F0	R/W	0h	DRAM WRLAT value in cycles for frequency set 0.

4.3.170 DDRSS_PI_169 Register (Offset = 22A4h) [reset = X]

DDRSS_PI_169 is shown in [Figure 4-664](#) and described in [Table 4-1334](#).

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Table 4-1333. DDRSS_PI_169 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22A4h

Figure 4-664. DDRSS_PI_169 Register

31	30	29	28	27	26	25	24
RESERVED						PI_TRFC_F0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PI_TRFC_F0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PI_CASLAT_LIN_F2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PI_WRLAT_F2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1334. DDRSS_PI_169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TRFC_F0	R/W	0h	DRAM tRFC value in memory clocks for frequency set 0.
15	RESERVED	R/W	X	
14-8	PI_CASLAT_LIN_F2	R/W	0h	Sets latency from read command sent to data received from/to controller for frequency set 2. Bit (0) is half-cycle increment and the upper bits define memory CAS latency for the controller.
7	RESERVED	R/W	X	
6-0	PI_WRLAT_F2	R/W	0h	DRAM WRLAT value in cycles for frequency set 2.

4.3.171 DDRSS_PI_170 Register (Offset = 22A8h) [reset = X]

DDRSS_PI_170 is shown in [Figure 4-665](#) and described in [Table 4-1336](#).

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Table 4-1335. DDRSS_PI_170 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22A8h

Figure 4-665. DDRSS_PI_170 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PI_TREF_F0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1336. DDRSS_PI_170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PI_TREF_F0	R/W	0h	DRAM tREF value in memory clocks for frequency set 0.

4.3.172 DDRSS_PI_171 Register (Offset = 22ACh) [reset = X]

DDRSS_PI_171 is shown in [Figure 4-666](#) and described in [Table 4-1338](#).

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Table 4-1337. DDRSS_PI_171 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22ACh

Figure 4-666. DDRSS_PI_171 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PI_TRFC_F1															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1338. DDRSS_PI_171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PI_TRFC_F1	R/W	0h	DRAM tRFC value in memory clocks for frequency set 1.

4.3.173 DDRSS_PI_172 Register (Offset = 22B0h) [reset = X]

DDRSS_PI_172 is shown in [Figure 4-667](#) and described in [Table 4-1340](#).

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Table 4-1339. DDRSS_PI_172 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22B0h

Figure 4-667. DDRSS_PI_172 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PI_TREF_F1																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1340. DDRSS_PI_172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PI_TREF_F1	R/W	0h	DRAM tREF value in memory clocks for frequency set 1.

4.3.174 DDRSS_PI_173 Register (Offset = 22B4h) [reset = X]

DDRSS_PI_173 is shown in [Figure 4-668](#) and described in [Table 4-1342](#).

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Table 4-1341. DDRSS_PI_173 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22B4h

Figure 4-668. DDRSS_PI_173 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PI_TRFC_F2															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1342. DDRSS_PI_173 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PI_TRFC_F2	R/W	0h	DRAM tRFC value in memory clocks for frequency set 2.

4.3.175 DDRSS_PI_174 Register (Offset = 22B8h) [reset = X]

DDRSS_PI_174 is shown in [Figure 4-669](#) and described in [Table 4-1344](#).

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Table 4-1343. DDRSS_PI_174 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22B8h

Figure 4-669. DDRSS_PI_174 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TDFI_CTRL_DELAY_F0			
R/W-X				R/W-2h			
23	22	21	20	19	18	17	16
RESERVED				PI_TREF_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_TREF_F2							
R/W-0h							
7	6	5	4	3	2	1	0
PI_TREF_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1344. DDRSS_PI_174 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_TDFI_CTRL_DELAY_F0	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks) for frequency set 0, the delay between a DFI command change and a memory command.
23-20	RESERVED	R/W	X	
19-0	PI_TREF_F2	R/W	0h	DRAM tREF value in memory clocks for frequency set 2.

4.3.176 DDRSS_PI_175 Register (Offset = 22BCh) [reset = X]

DDRSS_PI_175 is shown in Figure 4-670 and described in Table 4-1346.

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Table 4-1345. DDRSS_PI_175 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22BCh

Figure 4-670. DDRSS_PI_175 Register

31	30	29	28	27	26	25	24
RESERVED						PI_WRLVL_EN_F1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_WRLVL_EN_F0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CTRL_DELAY_F2			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
RESERVED				PI_TDFI_CTRL_DELAY_F1			
R/W-X				R/W-2h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1346. DDRSS_PI_175 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_WRLVL_EN_F1	R/W	0h	Enable the PI write leveling module for frequency set 1. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PI_WRLVL_EN_F0	R/W	0h	Enable the PI write leveling module for frequency set 0. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.
15-12	RESERVED	R/W	X	
11-8	PI_TDFI_CTRL_DELAY_F2	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks) for frequency set 2, the delay between a DFI command change and a memory command.
7-4	RESERVED	R/W	X	
3-0	PI_TDFI_CTRL_DELAY_F1	R/W	2h	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks) for frequency set 1, the delay between a DFI command change and a memory command.

4.3.177 DDRSS_PI_176 Register (Offset = 22C0h) [reset = X]

DDRSS_PI_176 is shown in [Figure 4-671](#) and described in [Table 4-1348](#).

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Table 4-1347. DDRSS_PI_176 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22C0h

Figure 4-671. DDRSS_PI_176 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WRLVL_WW_F0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PI_TDFI_WRLVL_WW_F0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PI_WRLVL_EN_F2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1348. DDRSS_PI_176 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PI_TDFI_WRLVL_WW_F0	R/W	0h	Defines the DFI tWRLVL_WW timing parameter (in DFI clocks) for frequency set 0, the minimum cycles between dfi_wrlvl_strobe assertions.
7-2	RESERVED	R/W	X	
1-0	PI_WRLVL_EN_F2	R/W	0h	Enable the PI write leveling module for frequency set 2. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.

4.3.178 DDRSS_PI_177 Register (Offset = 22C4h) [reset = X]

DDRSS_PI_177 is shown in [Figure 4-672](#) and described in [Table 4-1350](#).

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Table 4-1349. DDRSS_PI_177 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22C4h

Figure 4-672. DDRSS_PI_177 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WRLVL_WW_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TDFI_WRLVL_WW_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1350. DDRSS_PI_177 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_WRLVL_WW_F2	R/W	0h	Defines the DFI tWRLVL_WW timing parameter (in DFI clocks) for frequency set 2, the minimum cycles between dfi_wrlvl_strobe assertions.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_WRLVL_WW_F1	R/W	0h	Defines the DFI tWRLVL_WW timing parameter (in DFI clocks) for frequency set 1, the minimum cycles between dfi_wrlvl_strobe assertions.

4.3.179 DDRSS_PI_178 Register (Offset = 22C8h) [reset = X]

DDRSS_PI_178 is shown in [Figure 4-673](#) and described in [Table 4-1352](#).

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Table 4-1351. DDRSS_PI_178 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22C8h

Figure 4-673. DDRSS_PI_178 Register

31	30	29	28	27	26	25	24
RESERVED							PI_ODT_EN_F1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PI_TODTL_2CMD_F1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PI_ODT_EN_F0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PI_TODTL_2CMD_F0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1352. DDRSS_PI_178 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PI_ODT_EN_F1	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 1.
23-16	PI_TODTL_2CMD_F1	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 1.
15-9	RESERVED	R/W	X	
8	PI_ODT_EN_F0	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 0.
7-0	PI_TODTL_2CMD_F0	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 0.

4.3.180 DDRSS_PI_179 Register (Offset = 22CCh) [reset = X]

DDRSS_PI_179 is shown in Figure 4-674 and described in Table 4-1354.

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Table 4-1353. DDRSS_PI_179 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22CCh

Figure 4-674. DDRSS_PI_179 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TODTON_MIN_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_ODTLON_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PI_ODT_EN_F2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PI_TODTL_2CMD_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1354. DDRSS_PI_179 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_TODTON_MIN_F0	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 0.
23-20	RESERVED	R/W	X	
19-16	PI_ODTLON_F0	R/W	0h	Defines the latency from a CAS-2 command to the tODTon reference for frequency set 0.
15-9	RESERVED	R/W	X	
8	PI_ODT_EN_F2	R/W	0h	Enable support of DRAM ODT. When enabled, PI will assert and de-assert ODT output to DRAM as needed for frequency set 2.
7-0	PI_TODTL_2CMD_F2	R/W	0h	Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command for frequency set 2.

4.3.181 DDRSS_PI_180 Register (Offset = 22D0h) [reset = X]

DDRSS_PI_180 is shown in Figure 4-675 and described in Table 4-1356.

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Table 4-1355. DDRSS_PI_180 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22D0h

Figure 4-675. DDRSS_PI_180 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TODTON_MIN_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_ODTLON_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TODTON_MIN_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_ODTLON_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1356. DDRSS_PI_180 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_TODTON_MIN_F2	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 2.
23-20	RESERVED	R/W	X	
19-16	PI_ODTLON_F2	R/W	0h	Defines the latency from a CAS-2 command to the tODTOn reference for frequency set 2.
15-12	RESERVED	R/W	X	
11-8	PI_TODTON_MIN_F1	R/W	0h	Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on for frequency set 1.
7-4	RESERVED	R/W	X	
3-0	PI_ODTLON_F1	R/W	0h	Defines the latency from a CAS-2 command to the tODTOn reference for frequency set 1.

4.3.182 DDRSS_PI_181 Register (Offset = 22D4h) [reset = X]

DDRSS_PI_181 is shown in Figure 4-676 and described in Table 4-1358.

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Table 4-1357. DDRSS_PI_181 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22D4h

Figure 4-676. DDRSS_PI_181 Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_GATE_EN_F1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_EN_F1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_GATE_EN_F0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_EN_F0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1358. DDRSS_PI_181 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_RDLVL_GATE_EN_F1	R/W	0h	Enable the PI gate training module for frequency set 1. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PI_RDLVL_EN_F1	R/W	0h	Enable the PI data eye training module for frequency set 1. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.
15-10	RESERVED	R/W	X	
9-8	PI_RDLVL_GATE_EN_F0	R/W	0h	Enable the PI gate training module for frequency set 0. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.
7-2	RESERVED	R/W	X	
1-0	PI_RDLVL_EN_F0	R/W	0h	Enable the PI data eye training module for frequency set 0. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization. Set to 1 to enable.

4.3.183 DDRSS_PI_182 Register (Offset = 22D8h) [reset = X]

DDRSS_PI_182 is shown in Figure 4-677 and described in Table 4-1360.

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Table 4-1359. DDRSS_PI_182 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22D8h

Figure 4-677. DDRSS_PI_182 Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_RXCAL_EN_F0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_PAT0_EN_F0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_GATE_EN_F2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_EN_F2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1360. DDRSS_PI_182 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_RDLVL_RXCAL_EN_F0	R/W	0h	Enable RX Offset calibration (PATTERN 14,15) for read training for frequency set 0. bit1 for normal bit0 for initialization.
23-18	RESERVED	R/W	X	
17-16	PI_RDLVL_PAT0_EN_F0	R/W	0h	Enable PATTERN-0 for read training for frequency set 0. bit1 for normal bit0 for initialization.
15-10	RESERVED	R/W	X	
9-8	PI_RDLVL_GATE_EN_F2	R/W	0h	Enable the PI gate training module for frequency set 2. Bit(1) represents the support when non-initialization. Bit(0)represents the support when initialization. Set to 1 to enable.
7-2	RESERVED	R/W	X	
1-0	PI_RDLVL_EN_F2	R/W	0h	Enable the PI data eye training module for frequency set 2. Bit(1) represents the support when non-initialization. Bit(0)represents the support when initialization. Set to 1 to enable.

4.3.184 DDRSS_PI_183 Register (Offset = 22DCh) [reset = X]

DDRSS_PI_183 is shown in Figure 4-678 and described in Table 4-1362.

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Table 4-1361. DDRSS_PI_183 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22DCh

Figure 4-678. DDRSS_PI_183 Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_RXCAL_EN_F1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_PAT0_EN_F1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_MULTI_EN_F0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_DFE_EN_F0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1362. DDRSS_PI_183 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_RDLVL_RXCAL_EN_F1	R/W	0h	Enable RX Offset calibration (PATTERN 14,15) for read training for frequency set 1. bit1 for normal bit0 for initialization.
23-18	RESERVED	R/W	X	
17-16	PI_RDLVL_PAT0_EN_F1	R/W	0h	Enable PATTERN-0 for read training for frequency set 1. bit1 for normal bit0 for initialization.
15-10	RESERVED	R/W	X	
9-8	PI_RDLVL_MULTI_EN_F0	R/W	0h	Enable Multi-pattern (from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM) for read training for frequency set 0. bit1 for normal bit0 for initialization.
7-2	RESERVED	R/W	X	
1-0	PI_RDLVL_DFE_EN_F0	R/W	0h	Enable DFE (PATTERN 8,9) for read training for frequency set 0. bit1 for normal bit0 for initialization.

4.3.185 DDRSS_PI_184 Register (Offset = 22E0h) [reset = X]

DDRSS_PI_184 is shown in Figure 4-679 and described in Table 4-1364.

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Table 4-1363. DDRSS_PI_184 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22E0h

Figure 4-679. DDRSS_PI_184 Register

31	30	29	28	27	26	25	24
RESERVED						PI_RDLVL_RXCAL_EN_F2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PI_RDLVL_PAT0_EN_F2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_MULTI_EN_F1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_DFE_EN_F1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1364. DDRSS_PI_184 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_RDLVL_RXCAL_EN_F2	R/W	0h	Enable RX Offset calibration (PATTERN 14,15) for read training for frequency set 2. bit1 for normal bit0 for initialization.
23-18	RESERVED	R/W	X	
17-16	PI_RDLVL_PAT0_EN_F2	R/W	0h	Enable PATTERN-0 for read training for frequency set 2. bit1 for normal bit0 for initialization.
15-10	RESERVED	R/W	X	
9-8	PI_RDLVL_MULTI_EN_F1	R/W	0h	Enable Multi-pattern (from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM) for read training for frequency set 1. bit1 for normal bit0 for initialization.
7-2	RESERVED	R/W	X	
1-0	PI_RDLVL_DFE_EN_F1	R/W	0h	Enable DFE (PATTERN 8,9) for read training for frequency set 1. bit1 for normal bit0 for initialization.

4.3.186 DDRSS_PI_185 Register (Offset = 22E4h) [reset = X]

DDRSS_PI_185 is shown in Figure 4-680 and described in Table 4-1366.

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Table 4-1365. DDRSS_PI_185 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22E4h

Figure 4-680. DDRSS_PI_185 Register

31	30	29	28	27	26	25	24
RESERVED	PI_RDLAT_ADJ_F1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	PI_RDLAT_ADJ_F0						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED						PI_RDLVL_MULTI_EN_F2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_RDLVL_DFE_EN_F2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1366. DDRSS_PI_185 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_RDLAT_ADJ_F1	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 1.
23	RESERVED	R/W	X	
22-16	PI_RDLAT_ADJ_F0	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 0.
15-10	RESERVED	R/W	X	
9-8	PI_RDLVL_MULTI_EN_F2	R/W	0h	Enable Multi-pattern (from PI_RDLVL_PATTERN_START, total PI_RDLVL_PATTERN_NUM) for read training for frequency set 2. bit1 for normal bit0 for initialization.
7-2	RESERVED	R/W	X	
1-0	PI_RDLVL_DFE_EN_F2	R/W	0h	Enable DFE (PATTERN 8,9) for read training for frequency set 2. bit1 for normal bit0 for initialization.

4.3.187 DDRSS_PI_186 Register (Offset = 22E8h) [reset = X]

DDRSS_PI_186 is shown in [Figure 4-681](#) and described in [Table 4-1368](#).

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Table 4-1367. DDRSS_PI_186 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22E8h

Figure 4-681. DDRSS_PI_186 Register

31	30	29	28	27	26	25	24
RESERVED	PI_WRLAT_ADJ_F2						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WRLAT_ADJ_F1						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PI_WRLAT_ADJ_F0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	PI_RDLAT_ADJ_F2						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1368. DDRSS_PI_186 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_WRLAT_ADJ_F2	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 2.
23	RESERVED	R/W	X	
22-16	PI_WRLAT_ADJ_F1	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 1.
15	RESERVED	R/W	X	
14-8	PI_WRLAT_ADJ_F0	R/W	0h	Adjusts the relative timing in memory clocks between DFI write commands and the dfi_wrdata_en signal for frequency set 0.
7	RESERVED	R/W	X	
6-0	PI_RDLAT_ADJ_F2	R/W	0h	Adjusts the relative timing between DFI read commands and the dfi_rddata_en signal for frequency set 2.

4.3.188 DDRSS_PI_187 Register (Offset = 22ECh) [reset = X]

DDRSS_PI_187 is shown in [Figure 4-682](#) and described in [Table 4-1370](#).

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Table 4-1369. DDRSS_PI_187 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22ECh

Figure 4-682. DDRSS_PI_187 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PI_TDFI_PHY_WRDATA_F2			
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_PHY_WRDATA_F1			
R/W-X				R/W-1h			
7	6	5	4	3	2	1	0
RESERVED				PI_TDFI_PHY_WRDATA_F0			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1370. DDRSS_PI_187 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PI_TDFI_PHY_WRDATA_F2	R/W	1h	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks) for frequency set 2, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.
15-11	RESERVED	R/W	X	
10-8	PI_TDFI_PHY_WRDATA_F1	R/W	1h	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks) for frequency set 1, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.
7-3	RESERVED	R/W	X	
2-0	PI_TDFI_PHY_WRDATA_F0	R/W	1h	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks) for frequency set 0, the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.

4.3.189 DDRSS_PI_188 Register (Offset = 22F0h) [reset = X]

DDRSS_PI_188 is shown in [Figure 4-683](#) and described in [Table 4-1372](#).

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Table 4-1371. DDRSS_PI_188 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22F0h

Figure 4-683. DDRSS_PI_188 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_CALVL_CAPTURE_F0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TDFI_CALVL_CC_F0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1372. DDRSS_PI_188 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_CALVL_CAPTURE_F0	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks) for frequency set 0, the minimum cycles between a calibration command and a dfi_calvl_capture pulse.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_CALVL_CC_F0	R/W	0h	Defines the DFI tCALVL_CC timing parameter (in DFI clocks) for frequency set 0, the minimum cycles between calibration commands.

4.3.190 DDRSS_PI_189 Register (Offset = 22F4h) [reset = X]

DDRSS_PI_189 is shown in [Figure 4-684](#) and described in [Table 4-1374](#).

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Table 4-1373. DDRSS_PI_189 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22F4h

Figure 4-684. DDRSS_PI_189 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_CALVL_CAPTURE_F1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TDFI_CALVL_CC_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1374. DDRSS_PI_189 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_CALVL_CAPTURE_F1	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks) for frequency set 1, the minimum cycles between a calibration command and a dfi_calvl_capture pulse.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_CALVL_CC_F1	R/W	0h	Defines the DFI tCALVL_CC timing parameter (in DFI clocks) for frequency set 1, the minimum cycles between calibration commands.

4.3.191 DDRSS_PI_190 Register (Offset = 22F8h) [reset = X]

DDRSS_PI_190 is shown in [Figure 4-685](#) and described in [Table 4-1376](#).

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Table 4-1375. DDRSS_PI_190 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22F8h

Figure 4-685. DDRSS_PI_190 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_CALVL_CAPTURE_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TDFI_CALVL_CC_F2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1376. DDRSS_PI_190 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_CALVL_CAPTURE_F2	R/W	0h	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks) for frequency set 2, the minimum cycles between a calibration command and a dfi_calvl_capture pulse.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_CALVL_CC_F2	R/W	0h	Defines the DFI tCALVL_CC timing parameter (in DFI clocks) for frequency set 2, the minimum cycles between calibration commands.

4.3.192 DDRSS_PI_191 Register (Offset = 22FCh) [reset = X]

DDRSS_PI_191 is shown in [Figure 4-686](#) and described in [Table 4-1378](#).

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Table 4-1377. DDRSS_PI_191 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 22FCh

Figure 4-686. DDRSS_PI_191 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TMRZ_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PI_CALVL_EN_F2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_CALVL_EN_F1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED						PI_CALVL_EN_F0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1378. DDRSS_PI_191 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PI_TMRZ_F0	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 0.
23-18	RESERVED	R/W	X	
17-16	PI_CALVL_EN_F2	R/W	0h	Enable the PI CA training module. Bit(1) represents the support when non-initialization for frequency set 2. Bit(0) represents the support when initialization. Set to 1 to enable.
15-10	RESERVED	R/W	X	
9-8	PI_CALVL_EN_F1	R/W	0h	Enable the PI CA training module. Bit(1) represents the support when non-initialization for frequency set 1. Bit(0) represents the support when initialization. Set to 1 to enable.
7-2	RESERVED	R/W	X	
1-0	PI_CALVL_EN_F0	R/W	0h	Enable the PI CA training module. Bit(1) represents the support when non-initialization for frequency set 0. Bit(0) represents the support when initialization. Set to 1 to enable.

4.3.193 DDRSS_PI_192 Register (Offset = 2300h) [reset = X]

DDRSS_PI_192 is shown in [Figure 4-687](#) and described in [Table 4-1380](#).

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Table 4-1379. DDRSS_PI_192 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2300h

Figure 4-687. DDRSS_PI_192 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PI_TMRZ_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TCAENT_F0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PI_TCAENT_F0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1380. DDRSS_PI_192 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PI_TMRZ_F1	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 1.
15-14	RESERVED	R/W	X	
13-0	PI_TCAENT_F0	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 0.

4.3.194 DDRSS_PI_193 Register (Offset = 2304h) [reset = X]

DDRSS_PI_193 is shown in [Figure 4-688](#) and described in [Table 4-1382](#).

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Table 4-1381. DDRSS_PI_193 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2304h

Figure 4-688. DDRSS_PI_193 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PI_TMRZ_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED			PI_TCAENT_F1				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
PI_TCAENT_F1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1382. DDRSS_PI_193 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PI_TMRZ_F2	R/W	0h	Defines the delay between a MRW CA exit command and the DQ tristate in memory clocks for frequency set 2.
15-14	RESERVED	R/W	X	
13-0	PI_TCAENT_F1	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 1.

4.3.195 DDRSS_PI_194 Register (Offset = 2308h) [reset = X]

DDRSS_PI_194 is shown in [Figure 4-689](#) and described in [Table 4-1384](#).

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Table 4-1383. DDRSS_PI_194 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2308h

Figure 4-689. DDRSS_PI_194 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TDFI_CASEL_F0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_TDFI_CACSCA_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TCAENT_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PI_TCAENT_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1384. DDRSS_PI_194 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PI_TDFI_CASEL_F0	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 0.
23-21	RESERVED	R/W	X	
20-16	PI_TDFI_CACSCA_F0	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 0.
15-14	RESERVED	R/W	X	
13-0	PI_TCAENT_F2	R/W	0h	Defines the DRAM tCAENT term, in memory clocks for frequency set 2.

4.3.196 DDRSS_PI_195 Register (Offset = 230Ch) [reset = X]

DDRSS_PI_195 is shown in Figure 4-690 and described in Table 4-1386.

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Table 4-1385. DDRSS_PI_195 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 230Ch

Figure 4-690. DDRSS_PI_195 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TVREF_LONG_F0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TVREF_SHORT_F0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1386. DDRSS_PI_195 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TVREF_LONG_F0	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 0.
15-10	RESERVED	R/W	X	
9-0	PI_TVREF_SHORT_F0	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 0.

4.3.197 DDRSS_PI_196 Register (Offset = 2310h) [reset = X]

DDRSS_PI_196 is shown in Figure 4-691 and described in Table 4-1388.

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Table 4-1387. DDRSS_PI_196 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2310h

Figure 4-691. DDRSS_PI_196 Register

31	30	29	28	27	26	25	24
RESERVED						PI_TVREF_SHORT_F1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PI_TVREF_SHORT_F1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CASEL_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_TDFI_CACSCA_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1388. DDRSS_PI_196 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TVREF_SHORT_F1	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 1.
15-13	RESERVED	R/W	X	
12-8	PI_TDFI_CASEL_F1	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 1.
7-5	RESERVED	R/W	X	
4-0	PI_TDFI_CACSCA_F1	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 1.

4.3.198 DDRSS_PI_197 Register (Offset = 2314h) [reset = X]

DDRSS_PI_197 is shown in Figure 4-692 and described in Table 4-1390.

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Table 4-1389. DDRSS_PI_197 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2314h

Figure 4-692. DDRSS_PI_197 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TDFI_CASEL_F2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_TDFI_CACSCA_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PI_TVREF_LONG_F1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PI_TVREF_LONG_F1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1390. DDRSS_PI_197 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PI_TDFI_CASEL_F2	R/W	0h	Defines the DFI tcalvl_ca_sel timing parameter, the width of dfi_calvl_ca_sel in PHY DFI clock cycles for frequency set 2.
23-21	RESERVED	R/W	X	
20-16	PI_TDFI_CACSCA_F2	R/W	0h	Defines the DFI tcalvl_cs_ca timing parameter, the number of PHY DFI clocks from the assertion of dfi_calvl_ca_sel to the assertion of dfi_cs for frequency set 2.
15-10	RESERVED	R/W	X	
9-0	PI_TVREF_LONG_F1	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 1.

4.3.199 DDRSS_PI_198 Register (Offset = 2318h) [reset = X]

DDRSS_PI_198 is shown in Figure 4-693 and described in Table 4-1392.

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Table 4-1391. DDRSS_PI_198 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2318h

Figure 4-693. DDRSS_PI_198 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TVREF_LONG_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TVREF_SHORT_F2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1392. DDRSS_PI_198 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TVREF_LONG_F2	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter gt 1 for frequency set 2.
15-10	RESERVED	R/W	X	
9-0	PI_TVREF_SHORT_F2	R/W	0h	Defines the delay in PI clock cycles between the dfi_calvl_strobe to the next command if the pi_calvl_vref_stepsize parameter = 1 for frequency set 2.

4.3.200 DDRSS_PI_199 Register (Offset = 231Ch) [reset = X]

DDRSS_PI_199 is shown in Figure 4-694 and described in Table 4-1394.

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Table 4-1393. DDRSS_PI_199 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 231Ch

Figure 4-694. DDRSS_PI_199 Register

31	30	29	28	27	26	25	24
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F1						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PI_CALVL_VREF_INITIAL_STOP_POINT_F0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	PI_CALVL_VREF_INITIAL_START_POINT_F0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1394. DDRSS_PI_199 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_CALVL_VREF_INITIAL_STOP_POINT_F1	R/W	0h	The end point of initial training for the Vref(ca) training for frequency set 1 { vrefca_range, vref_ca_setting [5:0]}.
23	RESERVED	R/W	X	
22-16	PI_CALVL_VREF_INITIAL_START_POINT_F1	R/W	0h	The start point of initial training for the Vref(ca) training for frequency set 1 { vrefca_range, vref_ca_setting [5:0]}.
15	RESERVED	R/W	X	
14-8	PI_CALVL_VREF_INITIAL_STOP_POINT_F0	R/W	0h	The end point of initial training for the Vref(ca) training for frequency set 0 { vrefca_range, vref_ca_setting [5:0]}.
7	RESERVED	R/W	X	
6-0	PI_CALVL_VREF_INITIAL_START_POINT_F0	R/W	0h	The start point of initial training for the Vref(ca) training for frequency set 0 { vrefca_range, vref_ca_setting [5:0]}.

4.3.201 DDRSS_PI_200 Register (Offset = 2320h) [reset = X]

DDRSS_PI_200 is shown in Figure 4-695 and described in Table 4-1396.

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Table 4-1395. DDRSS_PI_200 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2320h

Figure 4-695. DDRSS_PI_200 Register

31	30	29	28	27	26	25	24
RESERVED				PI_CALVL_VREF_DELTA_F1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_CALVL_VREF_DELTA_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		PI_CALVL_VREF_INITIAL_STOP_POINT_F2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PI_CALVL_VREF_INITIAL_START_POINT_F2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1396. DDRSS_PI_200 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_CALVL_VREF_DELTA_F1	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 1.
23-20	RESERVED	R/W	X	
19-16	PI_CALVL_VREF_DELTA_F0	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 0.
15	RESERVED	R/W	X	
14-8	PI_CALVL_VREF_INITIAL_STOP_POINT_F2	R/W	0h	The end point of initial training for the Vref(ca) training for frequency set 2 { vrefca_range, vref_ca_setting [5:0]}.
7	RESERVED	R/W	X	
6-0	PI_CALVL_VREF_INITIAL_START_POINT_F2	R/W	0h	The start point of initial training for the Vref(ca) training for frequency set 2 { vrefca_range, vref_ca_setting [5:0]}.

4.3.202 DDRSS_PI_201 Register (Offset = 2324h) [reset = X]

DDRSS_PI_201 is shown in Figure 4-696 and described in Table 4-1398.

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Table 4-1397. DDRSS_PI_201 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2324h

Figure 4-696. DDRSS_PI_201 Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TXP_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CALVL_STROBE_F0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_CALVL_VREF_DELTA_F2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1398. DDRSS_PI_201 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TMRWCKEL_F0	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 0.
23-21	RESERVED	R/W	X	
20-16	PI_TXP_F0	R/W	0h	CKE assert to next valid command delay for frequency set 0.
15-12	RESERVED	R/W	X	
11-8	PI_TDFI_CALVL_STROBE_F0	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 0.
7-4	RESERVED	R/W	X	
3-0	PI_CALVL_VREF_DELTA_F2	R/W	0h	The delta fro the current CA vref for non-initial CA training for frequency set 2.

4.3.203 DDRSS_PI_202 Register (Offset = 2328h) [reset = X]

DDRSS_PI_202 is shown in [Figure 4-697](#) and described in [Table 4-1400](#).

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Table 4-1399. DDRSS_PI_202 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2328h

Figure 4-697. DDRSS_PI_202 Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F1							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TXP_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CALVL_STROBE_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_TCKELCK_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1400. DDRSS_PI_202 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TMRWCKEL_F1	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 1.
23-21	RESERVED	R/W	X	
20-16	PI_TXP_F1	R/W	0h	CKE assert to next valid command delay for frequency set 1.
15-12	RESERVED	R/W	X	
11-8	PI_TDFI_CALVL_STROBE_F1	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 1.
7-5	RESERVED	R/W	X	
4-0	PI_TCKELCK_F0	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 0.

4.3.204 DDRSS_PI_203 Register (Offset = 232Ch) [reset = X]

DDRSS_PI_203 is shown in [Figure 4-698](#) and described in [Table 4-1402](#).

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Table 4-1401. DDRSS_PI_203 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 232Ch

Figure 4-698. DDRSS_PI_203 Register

31	30	29	28	27	26	25	24
PI_TMRWCKEL_F2							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PI_TXP_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_TDFI_CALVL_STROBE_F2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_TCKELCK_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1402. DDRSS_PI_203 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TMRWCKEL_F2	R/W	0h	Valid Clock and CS Requirement before CKE deassert after MRW Command for frequency set 2.
23-21	RESERVED	R/W	X	
20-16	PI_TXP_F2	R/W	0h	CKE assert to next valid command delay for frequency set 2.
15-12	RESERVED	R/W	X	
11-8	PI_TDFI_CALVL_STROBE_F2	R/W	0h	Minimum number of DFI PHY clocks from dfi_calvl_data to dfi_calvl_strobe mode for frequency set 2.
7-5	RESERVED	R/W	X	
4-0	PI_TCKELCK_F1	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 1.

4.3.205 DDRSS_PI_204 Register (Offset = 2330h) [reset = X]

DDRSS_PI_204 is shown in [Figure 4-699](#) and described in [Table 4-1404](#).

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Table 4-1403. DDRSS_PI_204 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2330h

Figure 4-699. DDRSS_PI_204 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														PI_TDFI_INIT_START_F0	
R/W-X														R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_INIT_START_F0								RESERVED				PI_TCKELCK_F2			
R/W-0h								R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1404. DDRSS_PI_204 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PI_TDFI_INIT_START_F0	R/W	0h	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency set 0, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY.
7-5	RESERVED	R/W	X	
4-0	PI_TCKELCK_F2	R/W	0h	Valid Clock Requirement after CKE deassert for frequency set 2.

4.3.206 DDRSS_PI_205 Register (Offset = 2334h) [reset = X]

DDRSS_PI_205 is shown in [Figure 4-700](#) and described in [Table 4-1406](#).

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Table 4-1405. DDRSS_PI_205 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2334h

Figure 4-700. DDRSS_PI_205 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_INIT_START_F1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1406. DDRSS_PI_205 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_INIT_START_F1	R/W	0h	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency set 1, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY.
15-0	PI_TDFI_INIT_COMPLETE_F0	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency set 0, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY.

4.3.207 DDRSS_PI_206 Register (Offset = 2338h) [reset = X]

DDRSS_PI_206 is shown in [Figure 4-701](#) and described in [Table 4-1408](#).

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Table 4-1407. DDRSS_PI_206 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2338h

Figure 4-701. DDRSS_PI_206 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_INIT_START_F2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1408. DDRSS_PI_206 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_INIT_START_F2	R/W	0h	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency set 2, the maximum number of cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY.
15-0	PI_TDFI_INIT_COMPLETE_F1	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency set 1, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY.

4.3.208 DDRSS_PI_207 Register (Offset = 233Ch) [reset = X]

DDRSS_PI_207 is shown in [Figure 4-702](#) and described in [Table 4-1410](#).

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Table 4-1409. DDRSS_PI_207 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 233Ch

Figure 4-702. DDRSS_PI_207 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PI_TCKEHDQS_F0				
R/W-X											R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_INIT_COMPLETE_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1410. DDRSS_PI_207 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PI_TCKEHDQS_F0	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 0.
15-0	PI_TDFI_INIT_COMPLETE_F2	R/W	0h	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency set 2, the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY.

4.3.209 DDRSS_PI_208 Register (Offset = 2340h) [reset = X]

DDRSS_PI_208 is shown in [Figure 4-703](#) and described in [Table 4-1412](#).

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Table 4-1411. DDRSS_PI_208 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2340h

Figure 4-703. DDRSS_PI_208 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PI_TCKEHDQS_F1				
R/W-X											R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TFC_F0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1412. DDRSS_PI_208 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PI_TCKEHDQS_F1	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 1.
15-10	RESERVED	R/W	X	
9-0	PI_TFC_F0	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 0.

4.3.210 DDRSS_PI_209 Register (Offset = 2344h) [reset = X]

DDRSS_PI_209 is shown in [Figure 4-704](#) and described in [Table 4-1414](#).

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Table 4-1413. DDRSS_PI_209 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2344h

Figure 4-704. DDRSS_PI_209 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED										PI_TCKEHDQS_F2					
R/W-X										R/W-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PI_TFC_F1					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1414. DDRSS_PI_209 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PI_TCKEHDQS_F2	R/W	0h	The DRAM timing tCKEHDQS, minimum delay from CKE high to strobe high impedance for frequency set 2.
15-10	RESERVED	R/W	X	
9-0	PI_TFC_F1	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 1.

4.3.211 DDRSS_PI_210 Register (Offset = 2348h) [reset = X]

DDRSS_PI_210 is shown in [Figure 4-705](#) and described in [Table 4-1416](#).

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Table 4-1415. DDRSS_PI_210 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2348h

Figure 4-705. DDRSS_PI_210 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WDQLVL_WR_F0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TFC_F2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1416. DDRSS_PI_210 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_WDQLVL_WR_F0	R/W	0h	Switch time from write to read for frequency set 0.
15-10	RESERVED	R/W	X	
9-0	PI_TFC_F2	R/W	0h	The delay in PHY clock cycles from setting MR13.OP7 to any valid command for frequency set 2.

4.3.212 DDRSS_PI_211 Register (Offset = 234Ch) [reset = X]

DDRSS_PI_211 is shown in [Figure 4-706](#) and described in [Table 4-1418](#).

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Table 4-1417. DDRSS_PI_211 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 234Ch

Figure 4-706. DDRSS_PI_211 Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F0						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WDQLVL_RW_F0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RW_F0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1418. DDRSS_PI_211 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F0	R/W	0h	Write DQ training vref initial training stop value for frequency set 0.
23	RESERVED	R/W	X	
22-16	PI_WDQLVL_VREF_INITIAL_START_POINT_F0	R/W	0h	Write DQ training vref initial training start value for frequency set 0.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_WDQLVL_RW_F0	R/W	0h	Switch time from read to write for frequency set 0.

4.3.213 DDRSS_PI_212 Register (Offset = 2350h) [reset = X]

DDRSS_PI_212 is shown in [Figure 4-707](#) and described in [Table 4-1420](#).

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Table 4-1419. DDRSS_PI_212 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2350h

Figure 4-707. DDRSS_PI_212 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PI_NTP_TRAIN_EN_F0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_WDQLVL_EN_F0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PI_WDQLVL_VREF_DELTA_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1420. DDRSS_PI_212 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PI_NTP_TRAIN_EN_F0	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization.
15-10	RESERVED	R/W	X	
9-8	PI_WDQLVL_EN_F0	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 0. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization.
7-4	RESERVED	R/W	X	
3-0	PI_WDQLVL_VREF_DELTA_F0	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 0.

4.3.214 DDRSS_PI_213 Register (Offset = 2354h) [reset = X]

DDRSS_PI_213 is shown in [Figure 4-708](#) and described in [Table 4-1422](#).

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Table 4-1421. DDRSS_PI_213 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2354h

Figure 4-708. DDRSS_PI_213 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WDQLVL_RW_F1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PI_TDFI_WDQLVL_WR_F1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1422. DDRSS_PI_213 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PI_TDFI_WDQLVL_RW_F1	R/W	0h	Switch time from read to write for frequency set 1.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_WDQLVL_WR_F1	R/W	0h	Switch time from write to read for frequency set 1.

4.3.215 DDRSS_PI_214 Register (Offset = 2358h) [reset = X]

DDRSS_PI_214 is shown in [Figure 4-709](#) and described in [Table 4-1424](#).

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Table 4-1423. DDRSS_PI_214 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2358h

Figure 4-709. DDRSS_PI_214 Register

31	30	29	28	27	26	25	24
RESERVED						PI_WDQLVL_EN_F1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED				PI_WDQLVL_VREF_DELTA_F1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PI_WDQLVL_VREF_INITIAL_START_POINT_F1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1424. DDRSS_PI_214 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PI_WDQLVL_EN_F1	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 1. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization.
23-20	RESERVED	R/W	X	
19-16	PI_WDQLVL_VREF_DELTA_F1	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 1.
15	RESERVED	R/W	X	
14-8	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F1	R/W	0h	Write DQ training vref initial training stop value for frequency set 1.
7	RESERVED	R/W	X	
6-0	PI_WDQLVL_VREF_INITIAL_START_POINT_F1	R/W	0h	Write DQ training vref initial training start value for frequency set 1.

4.3.216 DDRSS_PI_215 Register (Offset = 235Ch) [reset = X]

DDRSS_PI_215 is shown in [Figure 4-710](#) and described in [Table 4-1426](#).

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Table 4-1425. DDRSS_PI_215 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 235Ch

Figure 4-710. DDRSS_PI_215 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PI_TDFI_WDQLVL_WR_F2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PI_TDFI_WDQLVL_WR_F2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PI_NTP_TRAIN_EN_F1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1426. DDRSS_PI_215 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PI_TDFI_WDQLVL_WR_F2	R/W	0h	Switch time from write to read for frequency set 2.
7-2	RESERVED	R/W	X	
1-0	PI_NTP_TRAIN_EN_F1	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization.

4.3.217 DDRSS_PI_216 Register (Offset = 2360h) [reset = X]

DDRSS_PI_216 is shown in [Figure 4-711](#) and described in [Table 4-1428](#).

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Table 4-1427. DDRSS_PI_216 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2360h

Figure 4-711. DDRSS_PI_216 Register

31	30	29	28	27	26	25	24
RESERVED	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED	PI_WDQLVL_VREF_INITIAL_START_POINT_F2						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED						PI_TDFI_WDQLVL_RW_F2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PI_TDFI_WDQLVL_RW_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1428. DDRSS_PI_216 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PI_WDQLVL_VREF_INITIAL_STOP_POINT_F2	R/W	0h	Write DQ training vref initial training stop value for frequency set 2.
23	RESERVED	R/W	X	
22-16	PI_WDQLVL_VREF_INITIAL_START_POINT_F2	R/W	0h	Write DQ training vref initial training start value for frequency set 2.
15-10	RESERVED	R/W	X	
9-0	PI_TDFI_WDQLVL_RW_F2	R/W	0h	Switch time from read to write for frequency set 2.

4.3.218 DDRSS_PI_217 Register (Offset = 2364h) [reset = X]

DDRSS_PI_217 is shown in Figure 4-712 and described in Table 4-1430.

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Table 4-1429. DDRSS_PI_217 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2364h

Figure 4-712. DDRSS_PI_217 Register

31	30	29	28	27	26	25	24
PI_TRTP_F0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						PI_NTP_TRAIN_EN_F2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PI_WDQLVL_EN_F2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PI_WDQLVL_VREF_DELTA_F2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1430. DDRSS_PI_217 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TRTP_F0	R/W	0h	DRAM tRTP value in cycles for frequency set 0.
23-18	RESERVED	R/W	X	
17-16	PI_NTP_TRAIN_EN_F2	R/W	0h	Indicates whether the no topology WDQ training is enabled. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization.
15-10	RESERVED	R/W	X	
9-8	PI_WDQLVL_EN_F2	R/W	0h	Indicates if Write DQ leveling is enabled for frequency set 2. Bit(1) represents the support when non-initialization. Bit(0) represents the support when initialization.
7-4	RESERVED	R/W	X	
3-0	PI_WDQLVL_VREF_DELTA_F2	R/W	0h	The delta from the current Write DQ vref adjustment for non-initial wdq training for frequency set 2.

4.3.219 DDRSS_PI_218 Register (Offset = 2368h) [reset = X]

DDRSS_PI_218 is shown in [Figure 4-713](#) and described in [Table 4-1432](#).

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Table 4-1431. DDRSS_PI_218 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2368h

Figure 4-713. DDRSS_PI_218 Register

31	30	29	28	27	26	25	24
PI_TWR_F0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED		PI_TWTR_F0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
PI_TRCD_F0							
R/W-0h							
7	6	5	4	3	2	1	0
PI_TRP_F0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1432. DDRSS_PI_218 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TWR_F0	R/W	0h	DRAM tWR value in cycles for frequency set 0.
23-22	RESERVED	R/W	X	
21-16	PI_TWTR_F0	R/W	0h	DRAM tWTR value in cycles for frequency set 0.
15-8	PI_TRCD_F0	R/W	0h	DRAM tRCD value in cycles for frequency set 0.
7-0	PI_TRP_F0	R/W	0h	DRAM tRP value in cycles for frequency set 0.

4.3.220 DDRSS_PI_219 Register (Offset = 236Ch) [reset = X]

DDRSS_PI_219 is shown in [Figure 4-714](#) and described in [Table 4-1434](#).

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Table 4-1433. DDRSS_PI_219 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 236Ch

Figure 4-714. DDRSS_PI_219 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_TRAS_MIN_F0								RESERVED							PI_TRAS_MAX_F0
R/W-0h								R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRAS_MAX_F0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1434. DDRSS_PI_219 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TRAS_MIN_F0	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 0.
23-17	RESERVED	R/W	X	
16-0	PI_TRAS_MAX_F0	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 0.

4.3.221 DDRSS_PI_220 Register (Offset = 2370h) [reset = X]

DDRSS_PI_220 is shown in [Figure 4-715](#) and described in [Table 4-1436](#).

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Table 4-1435. DDRSS_PI_220 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2370h

Figure 4-715. DDRSS_PI_220 Register

31	30	29	28	27	26	25	24
PI_TMRD_F0							
R/W-0h							
23	22	21	20	19	18	17	16
PI_TSR_F0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PI_TCCDMW_F0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED				PI_TDQSCK_MAX_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1436. DDRSS_PI_220 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TMRD_F0	R/W	0h	DRAM tMRD value in cycles for frequency set 0.
23-16	PI_TSR_F0	R/W	0h	Min cycles from sref entry to sref exit for frequency set 0.
15-14	RESERVED	R/W	X	
13-8	PI_TCCDMW_F0	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 0.
7-4	RESERVED	R/W	X	
3-0	PI_TDQSCK_MAX_F0	R/W	0h	Additional delay needed for tDQSCK for frequency set 0.

4.3.222 DDRSS_PI_221 Register (Offset = 2374h) [reset = 0h]

DDRSS_PI_221 is shown in [Figure 4-716](#) and described in [Table 4-1438](#).

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Table 4-1437. DDRSS_PI_221 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2374h

Figure 4-716. DDRSS_PI_221 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_TRCD_F1								PI_TRP_F1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRTP_F1								PI_TMRW_F0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1438. DDRSS_PI_221 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TRCD_F1	R/W	0h	DRAM tRCD value in cycles for frequency set 1.
23-16	PI_TRP_F1	R/W	0h	DRAM tRP value in cycles for frequency set 1.
15-8	PI_TRTP_F1	R/W	0h	DRAM tRTP value in cycles for frequency set 1.
7-0	PI_TMRW_F0	R/W	0h	DRAM tMRW value in cycles for frequency set 0.

4.3.223 DDRSS_PI_222 Register (Offset = 2378h) [reset = X]

DDRSS_PI_222 is shown in [Figure 4-717](#) and described in [Table 4-1440](#).

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Table 4-1439. DDRSS_PI_222 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2378h

Figure 4-717. DDRSS_PI_222 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PI_TWR_F1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PI_TWTR_F1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1440. DDRSS_PI_222 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PI_TWR_F1	R/W	0h	DRAM tWR value in cycles for frequency set 1.
7-6	RESERVED	R/W	X	
5-0	PI_TWTR_F1	R/W	0h	DRAM tWTR value in cycles for frequency set 1.

4.3.224 DDRSS_PI_223 Register (Offset = 237Ch) [reset = X]

DDRSS_PI_223 is shown in [Figure 4-718](#) and described in [Table 4-1442](#).

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Table 4-1441. DDRSS_PI_223 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 237Ch

Figure 4-718. DDRSS_PI_223 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_TRAS_MIN_F1								RESERVED							PI_TRAS_MAX_F1
R/W-0h								R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRAS_MAX_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1442. DDRSS_PI_223 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TRAS_MIN_F1	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 1.
23-17	RESERVED	R/W	X	
16-0	PI_TRAS_MAX_F1	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 1.

4.3.225 DDRSS_PI_224 Register (Offset = 2380h) [reset = X]

DDRSS_PI_224 is shown in [Figure 4-719](#) and described in [Table 4-1444](#).

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Table 4-1443. DDRSS_PI_224 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2380h

Figure 4-719. DDRSS_PI_224 Register

31	30	29	28	27	26	25	24
PI_TMRD_F1							
R/W-0h							
23	22	21	20	19	18	17	16
PI_TSR_F1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PI_TCCDMW_F1					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED				PI_TDQSCK_MAX_F1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1444. DDRSS_PI_224 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TMRD_F1	R/W	0h	DRAM tMRD value in cycles for frequency set 1.
23-16	PI_TSR_F1	R/W	0h	Min cycles from sref entry to sref exit for frequency set 1.
15-14	RESERVED	R/W	X	
13-8	PI_TCCDMW_F1	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 1.
7-4	RESERVED	R/W	X	
3-0	PI_TDQSCK_MAX_F1	R/W	0h	Additional delay needed for tDQSCK for frequency set 1.

4.3.226 DDRSS_PI_225 Register (Offset = 2384h) [reset = 0h]

DDRSS_PI_225 is shown in [Figure 4-720](#) and described in [Table 4-1446](#).

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Table 4-1445. DDRSS_PI_225 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2384h

Figure 4-720. DDRSS_PI_225 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_TRCD_F2								PI_TRP_F2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRTP_F2								PI_TMRW_F1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1446. DDRSS_PI_225 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TRCD_F2	R/W	0h	DRAM tRCD value in cycles for frequency set 2.
23-16	PI_TRP_F2	R/W	0h	DRAM tRP value in cycles for frequency set 2.
15-8	PI_TRTP_F2	R/W	0h	DRAM tRTP value in cycles for frequency set 2.
7-0	PI_TMRW_F1	R/W	0h	DRAM tMRW value in cycles for frequency set 1.

4.3.227 DDRSS_PI_226 Register (Offset = 2388h) [reset = X]

DDRSS_PI_226 is shown in [Figure 4-721](#) and described in [Table 4-1448](#).

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Table 4-1447. DDRSS_PI_226 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2388h

Figure 4-721. DDRSS_PI_226 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PI_TWR_F2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PI_TWTR_F2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1448. DDRSS_PI_226 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PI_TWR_F2	R/W	0h	DRAM tWR value in cycles for frequency set 2.
7-6	RESERVED	R/W	X	
5-0	PI_TWTR_F2	R/W	0h	DRAM tWTR value in cycles for frequency set 2.

4.3.228 DDRSS_PI_227 Register (Offset = 238Ch) [reset = X]

DDRSS_PI_227 is shown in [Figure 4-722](#) and described in [Table 4-1450](#).

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Table 4-1449. DDRSS_PI_227 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 238Ch

Figure 4-722. DDRSS_PI_227 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_TRAS_MIN_F2								RESERVED							PI_TRAS_MAX_F2
R/W-0h								R/W-X							R/W-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TRAS_MAX_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1450. DDRSS_PI_227 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TRAS_MIN_F2	R/W	0h	DRAM tRAS_MIN value in cycles for frequency set 2.
23-17	RESERVED	R/W	X	
16-0	PI_TRAS_MAX_F2	R/W	0h	DRAM tRAS_MAX value in cycles for frequency set 2.

4.3.229 DDRSS_PI_228 Register (Offset = 2390h) [reset = X]

DDRSS_PI_228 is shown in [Figure 4-723](#) and described in [Table 4-1452](#).

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Table 4-1451. DDRSS_PI_228 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2390h

Figure 4-723. DDRSS_PI_228 Register

31	30	29	28	27	26	25	24
PI_TMRD_F2							
R/W-0h							
23	22	21	20	19	18	17	16
PI_TSR_F2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PI_TCCDMW_F2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED				PI_TDQSCK_MAX_F2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1452. DDRSS_PI_228 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_TMRD_F2	R/W	0h	DRAM tMRD value in cycles for frequency set 2.
23-16	PI_TSR_F2	R/W	0h	Min cycles from sref entry to sref exit for frequency set 2.
15-14	RESERVED	R/W	X	
13-8	PI_TCCDMW_F2	R/W	0h	LPDDR4 DRAM tCCDMW in cycles for frequency set 2.
7-4	RESERVED	R/W	X	
3-0	PI_TDQSCK_MAX_F2	R/W	0h	Additional delay needed for tDQSCK for frequency set 2.

4.3.230 DDRSS_PI_229 Register (Offset = 2394h) [reset = X]

DDRSS_PI_229 is shown in [Figure 4-724](#) and described in [Table 4-1454](#).

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Table 4-1453. DDRSS_PI_229 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2394h

Figure 4-724. DDRSS_PI_229 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_TDFI_CTRLUPD_MAX_F0											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MAX_F0								PI_TMRW_F2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1454. DDRSS_PI_229 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-8	PI_TDFI_CTRLUPD_MAX_F0	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks) for frequency set 0, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) set in the PI_UPDATE_ERROR_STATUS parameter.
7-0	PI_TMRW_F2	R/W	0h	DRAM tMRW value in cycles for frequency set 2.

4.3.231 DDRSS_PI_230 Register (Offset = 2398h) [reset = 0h]

DDRSS_PI_230 is shown in [Figure 4-725](#) and described in [Table 4-1456](#).

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Table 4-1455. DDRSS_PI_230 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2398h

Figure 4-725. DDRSS_PI_230 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1456. DDRSS_PI_230 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_CTRLUPD_INTERVAL_F0	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks) for frequency set 0, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PI_UPDATE_ERROR_STATUS parameter.

4.3.232 DDRSS_PI_231 Register (Offset = 239Ch) [reset = X]

DDRSS_PI_231 is shown in [Figure 4-726](#) and described in [Table 4-1458](#).

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Table 4-1457. DDRSS_PI_231 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 239Ch

Figure 4-726. DDRSS_PI_231 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PI_TDFI_CTRLUPD_MAX_F1				
R/W-X											R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MAX_F1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1458. DDRSS_PI_231 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-0	PI_TDFI_CTRLUPD_MAX_F1	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks) for frequency set 1, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) set in the PI_UPDATE_ERROR_STATUS parameter.

4.3.233 DDRSS_PI_232 Register (Offset = 23A0h) [reset = 0h]

DDRSS_PI_232 is shown in [Figure 4-727](#) and described in [Table 4-1460](#).

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Table 4-1459. DDRSS_PI_232 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23A0h

Figure 4-727. DDRSS_PI_232 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1460. DDRSS_PI_232 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_CTRLUPD_INTERVAL_F1	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks) for frequency set 1, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PI_UPDATE_ERROR_STATUS parameter.

4.3.234 DDRSS_PI_233 Register (Offset = 23A4h) [reset = X]

DDRSS_PI_233 is shown in [Figure 4-728](#) and described in [Table 4-1462](#).

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Table 4-1461. DDRSS_PI_233 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23A4h

Figure 4-728. DDRSS_PI_233 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PI_TDFI_CTRLUPD_MAX_F2				
R/W-X											R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_MAX_F2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1462. DDRSS_PI_233 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-0	PI_TDFI_CTRLUPD_MAX_F2	R/W	0h	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks) for frequency set 2, the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation will cause an interrupt and bit (1) set in the PI_UPDATE_ERROR_STATUS parameter.

4.3.235 DDRSS_PI_234 Register (Offset = 23A8h) [reset = 0h]

DDRSS_PI_234 is shown in [Figure 4-729](#) and described in [Table 4-1464](#).

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Table 4-1463. DDRSS_PI_234 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23A8h

Figure 4-729. DDRSS_PI_234 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TDFI_CTRLUPD_INTERVAL_F2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1464. DDRSS_PI_234 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PI_TDFI_CTRLUPD_INTERVAL_F2	R/W	0h	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks) for frequency set 2, the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation will cause an interrupt and bit (0) set in the PI_UPDATE_ERROR_STATUS parameter.

4.3.236 DDRSS_PI_235 Register (Offset = 23ACh) [reset = 0h]

DDRSS_PI_235 is shown in [Figure 4-730](#) and described in [Table 4-1466](#).

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Table 4-1465. DDRSS_PI_235 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23ACh

Figure 4-730. DDRSS_PI_235 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_TXSR_F1																PI_TXSR_F0															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1466. DDRSS_PI_235 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PI_TXSR_F1	R/W	0h	DRAM TXSR value for frequency set 1 in cycles.
15-0	PI_TXSR_F0	R/W	0h	DRAM TXSR value for frequency set 0 in cycles.

4.3.237 DDRSS_PI_236 Register (Offset = 23B0h) [reset = X]

DDRSS_PI_236 is shown in [Figure 4-731](#) and described in [Table 4-1468](#).

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Table 4-1467. DDRSS_PI_236 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23B0h

Figure 4-731. DDRSS_PI_236 Register

31	30	29	28	27	26	25	24
RESERVED				PI_TEXCKE_F1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_TEXCKE_F0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PI_TXSR_F2							
R/W-0h							
7	6	5	4	3	2	1	0
PI_TXSR_F2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1468. DDRSS_PI_236 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PI_TEXCKE_F1	R/W	0h	DRAM CKE low after SREF command timing for frequency set 1.
23-22	RESERVED	R/W	X	
21-16	PI_TEXCKE_F0	R/W	0h	DRAM CKE low after SREF command timing for frequency set 0.
15-0	PI_TXSR_F2	R/W	0h	DRAM TXSR value for frequency set 2 in cycles.

4.3.238 DDRSS_PI_237 Register (Offset = 23B4h) [reset = X]

DDRSS_PI_237 is shown in [Figure 4-732](#) and described in [Table 4-1470](#).

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Table 4-1469. DDRSS_PI_237 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23B4h

Figure 4-732. DDRSS_PI_237 Register

31	30	29	28	27	26	25	24
PI_TINIT_F0							
R/W-0h							
23	22	21	20	19	18	17	16
PI_TINIT_F0							
R/W-0h							
15	14	13	12	11	10	9	8
PI_TINIT_F0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PI_TEXCKE_F2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1470. DDRSS_PI_237 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	PI_TINIT_F0	R/W	0h	DRAM tINIT value for frequency set 0 in cycles.
7-6	RESERVED	R/W	X	
5-0	PI_TEXCKE_F2	R/W	0h	DRAM CKE low after SREF command timing for frequency set 2.

4.3.239 DDRSS_PI_238 Register (Offset = 23B8h) [reset = X]

DDRSS_PI_238 is shown in [Figure 4-733](#) and described in [Table 4-1472](#).

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Table 4-1471. DDRSS_PI_238 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23B8h

Figure 4-733. DDRSS_PI_238 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT3_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1472. DDRSS_PI_238 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT3_F0	R/W	0h	DRAM tINIT3 value for frequency set 0 in cycles.

4.3.240 DDRSS_PI_239 Register (Offset = 23BCh) [reset = X]

DDRSS_PI_239 is shown in [Figure 4-734](#) and described in [Table 4-1474](#).

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Table 4-1473. DDRSS_PI_239 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23BCh

Figure 4-734. DDRSS_PI_239 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT4_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1474. DDRSS_PI_239 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT4_F0	R/W	0h	DRAM tINIT4 value for frequency set 0 in cycles.

4.3.241 DDRSS_PI_240 Register (Offset = 23C0h) [reset = X]

DDRSS_PI_240 is shown in [Figure 4-735](#) and described in [Table 4-1476](#).

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Table 4-1475. DDRSS_PI_240 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23C0h

Figure 4-735. DDRSS_PI_240 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT5_F0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1476. DDRSS_PI_240 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT5_F0	R/W	0h	DRAM tINIT5 value for frequency set 0 in cycles.

4.3.242 DDRSS_PI_241 Register (Offset = 23C4h) [reset = X]

DDRSS_PI_241 is shown in [Figure 4-736](#) and described in [Table 4-1478](#).

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Table 4-1477. DDRSS_PI_241 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23C4h

Figure 4-736. DDRSS_PI_241 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PI_TXSNR_F0															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1478. DDRSS_PI_241 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PI_TXSNR_F0	R/W	0h	DRAM tXSNR value for frequency set 0 in cycles.

4.3.243 DDRSS_PI_242 Register (Offset = 23C8h) [reset = X]

DDRSS_PI_242 is shown in [Figure 4-737](#) and described in [Table 4-1480](#).

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Table 4-1479. DDRSS_PI_242 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23C8h

Figure 4-737. DDRSS_PI_242 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1480. DDRSS_PI_242 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT_F1	R/W	0h	DRAM tINIT value for frequency set 1 in cycles.

4.3.244 DDRSS_PI_243 Register (Offset = 23CCh) [reset = X]

DDRSS_PI_243 is shown in [Figure 4-738](#) and described in [Table 4-1482](#).

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Table 4-1481. DDRSS_PI_243 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23CCh

Figure 4-738. DDRSS_PI_243 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT3_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1482. DDRSS_PI_243 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT3_F1	R/W	0h	DRAM tINIT3 value for frequency set 1 in cycles.

4.3.245 DDRSS_PI_244 Register (Offset = 23D0h) [reset = X]

DDRSS_PI_244 is shown in [Figure 4-739](#) and described in [Table 4-1484](#).

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Table 4-1483. DDRSS_PI_244 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23D0h

Figure 4-739. DDRSS_PI_244 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT4_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1484. DDRSS_PI_244 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT4_F1	R/W	0h	DRAM tINIT4 value for frequency set 1 in cycles.

4.3.246 DDRSS_PI_245 Register (Offset = 23D4h) [reset = X]

DDRSS_PI_245 is shown in [Figure 4-740](#) and described in [Table 4-1486](#).

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Table 4-1485. DDRSS_PI_245 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23D4h

Figure 4-740. DDRSS_PI_245 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT5_F1																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1486. DDRSS_PI_245 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT5_F1	R/W	0h	DRAM tINIT5 value for frequency set 1 in cycles.

4.3.247 DDRSS_PI_246 Register (Offset = 23D8h) [reset = X]

DDRSS_PI_246 is shown in [Figure 4-741](#) and described in [Table 4-1488](#).

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Table 4-1487. DDRSS_PI_246 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23D8h

Figure 4-741. DDRSS_PI_246 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PI_TXSNR_F1															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1488. DDRSS_PI_246 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PI_TXSNR_F1	R/W	0h	DRAM tXSNR value for frequency set 1 in cycles.

4.3.248 DDRSS_PI_247 Register (Offset = 23DCh) [reset = X]

DDRSS_PI_247 is shown in [Figure 4-742](#) and described in [Table 4-1490](#).

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Table 4-1489. DDRSS_PI_247 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23DCh

Figure 4-742. DDRSS_PI_247 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1490. DDRSS_PI_247 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT_F2	R/W	0h	DRAM tINIT value for frequency set 2 in cycles.

4.3.249 DDRSS_PI_248 Register (Offset = 23E0h) [reset = X]

DDRSS_PI_248 is shown in [Figure 4-743](#) and described in [Table 4-1492](#).

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Table 4-1491. DDRSS_PI_248 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23E0h

Figure 4-743. DDRSS_PI_248 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT3_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1492. DDRSS_PI_248 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT3_F2	R/W	0h	DRAM tINIT3 value for frequency set 2 in cycles.

4.3.250 DDRSS_PI_249 Register (Offset = 23E4h) [reset = X]

DDRSS_PI_249 is shown in [Figure 4-744](#) and described in [Table 4-1494](#).

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Table 4-1493. DDRSS_PI_249 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23E4h

Figure 4-744. DDRSS_PI_249 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT4_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1494. DDRSS_PI_249 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT4_F2	R/W	0h	DRAM tINIT4 value for frequency set 2 in cycles.

4.3.251 DDRSS_PI_250 Register (Offset = 23E8h) [reset = X]

DDRSS_PI_250 is shown in [Figure 4-745](#) and described in [Table 4-1496](#).

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Table 4-1495. DDRSS_PI_250 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23E8h

Figure 4-745. DDRSS_PI_250 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PI_TINIT5_F2																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1496. DDRSS_PI_250 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PI_TINIT5_F2	R/W	0h	DRAM tINIT5 value for frequency set 2 in cycles.

4.3.252 DDRSS_PI_251 Register (Offset = 23ECh) [reset = X]

DDRSS_PI_251 is shown in [Figure 4-746](#) and described in [Table 4-1498](#).

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Table 4-1497. DDRSS_PI_251 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23ECh

Figure 4-746. DDRSS_PI_251 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED								PI_TXSNR_F2															
R/W-X								R/W-0h								R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1498. DDRSS_PI_251 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	RESERVED	R/W	0h	Reserved
15-0	PI_TXSNR_F2	R/W	0h	DRAM tXSNR value for frequency set 2 in cycles.

4.3.253 DDRSS_PI_252 Register (Offset = 23F0h) [reset = X]

DDRSS_PI_252 is shown in [Figure 4-747](#) and described in [Table 4-1500](#).

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Table 4-1499. DDRSS_PI_252 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23F0h

Figure 4-747. DDRSS_PI_252 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_TZQCAL_F0											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1500. DDRSS_PI_252 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PI_TZQCAL_F0	R/W	0h	Holds the DRAM ZQCAL value for frequency set 0 in cycles.
15-12	RESERVED	R/W	X	
11-0	RESERVED	R/W	0h	Reserved

4.3.254 DDRSS_PI_253 Register (Offset = 23F4h) [reset = X]

DDRSS_PI_253 is shown in [Figure 4-748](#) and described in [Table 4-1502](#).

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Table 4-1501. DDRSS_PI_253 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23F4h

Figure 4-748. DDRSS_PI_253 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1502. DDRSS_PI_253 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	X	
6-0	PI_TZQLAT_F0	R/W	0h	Holds the DRAM ZQLAT value for frequency set 0 in cycles.

4.3.255 DDRSS_PI_254 Register (Offset = 23F8h) [reset = X]

DDRSS_PI_254 is shown in [Figure 4-749](#) and described in [Table 4-1504](#).

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Table 4-1503. DDRSS_PI_254 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23F8h

Figure 4-749. DDRSS_PI_254 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_TZQCAL_F1											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1504. DDRSS_PI_254 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PI_TZQCAL_F1	R/W	0h	Holds the DRAM ZQCAL value for frequency set 1 in cycles.
15-12	RESERVED	R/W	X	
11-0	RESERVED	R/W	0h	Reserved

4.3.256 DDRSS_PI_255 Register (Offset = 23FCh) [reset = X]

DDRSS_PI_255 is shown in [Figure 4-750](#) and described in [Table 4-1506](#).

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Table 4-1505. DDRSS_PI_255 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 23FCh

Figure 4-750. DDRSS_PI_255 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F1						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1506. DDRSS_PI_255 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	X	
6-0	PI_TZQLAT_F1	R/W	0h	Holds the DRAM ZQLAT value for frequency set 1 in cycles.

4.3.257 DDRSS_PI_256 Register (Offset = 2400h) [reset = X]

DDRSS_PI_256 is shown in [Figure 4-751](#) and described in [Table 4-1508](#).

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Table 4-1507. DDRSS_PI_256 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2400h

Figure 4-751. DDRSS_PI_256 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_TZQCAL_F2											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1508. DDRSS_PI_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PI_TZQCAL_F2	R/W	0h	Holds the DRAM ZQCAL value for frequency set 2 in cycles.
15-12	RESERVED	R/W	X	
11-0	RESERVED	R/W	0h	Reserved

4.3.258 DDRSS_PI_257 Register (Offset = 2404h) [reset = X]

DDRSS_PI_257 is shown in [Figure 4-752](#) and described in [Table 4-1510](#).

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Table 4-1509. DDRSS_PI_257 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2404h

Figure 4-752. DDRSS_PI_257 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				RESERVED			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PI_TZQLAT_F2						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1510. DDRSS_PI_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	X	
6-0	PI_TZQLAT_F2	R/W	0h	Holds the DRAM ZQLAT value for frequency set 2 in cycles.

4.3.259 DDRSS_PI_258 Register (Offset = 2408h) [reset = X]

DDRSS_PI_258 is shown in [Figure 4-753](#) and described in [Table 4-1512](#).

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Table 4-1511. DDRSS_PI_258 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2408h

Figure 4-753. DDRSS_PI_258 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED											
R/W-X				R/W-0h											

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1512. DDRSS_PI_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	RESERVED	R/W	0h	Reserved
15-12	RESERVED	R/W	X	
11-0	RESERVED	R/W	0h	Reserved

4.3.260 DDRSS_PI_259 Register (Offset = 240Ch) [reset = X]

DDRSS_PI_259 is shown in Figure 4-754 and described in Table 4-1514.

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Table 4-1513. DDRSS_PI_259 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 240Ch

Figure 4-754. DDRSS_PI_259 Register

31	30	29	28	27	26	25	24
PI_MR13_DATA_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_WDQ_OSC_DELTA_INDEX_F0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1514. DDRSS_PI_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR13_DATA_0	R/W	0h	Data to program into memory mode register 13 for chip select 0.
23-20	RESERVED	R/W	X	
19-16	PI_WDQ_OSC_DELTA_INDEX_F2	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 2. If the value is n, the delay is $2^n/512$ cycle.
15-12	RESERVED	R/W	X	
11-8	PI_WDQ_OSC_DELTA_INDEX_F1	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 1. If the value is n, the delay is $2^n/512$ cycle.
7-4	RESERVED	R/W	X	
3-0	PI_WDQ_OSC_DELTA_INDEX_F0	R/W	0h	WDQ DQS delay delta index for OSC triggered periodic training for frequency set 0. If the value is n, the delay is $2^n/512$ cycle.

4.3.261 DDRSS_PI_260 Register (Offset = 2410h) [reset = 0h]

DDRSS_PI_260 is shown in [Figure 4-755](#) and described in [Table 4-1516](#).

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Table 4-1515. DDRSS_PI_260 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2410h

Figure 4-755. DDRSS_PI_260 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR20_DATA_0								PI_MR17_DATA_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR16_DATA_0								PI_MR15_DATA_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1516. DDRSS_PI_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR20_DATA_0	R/W	0h	Data to program into memory mode register 20 for chip select 0.
23-16	PI_MR17_DATA_0	R/W	0h	Data to program into memory mode register 17 for chip select 0.
15-8	PI_MR16_DATA_0	R/W	0h	Data to program into memory mode register 16 for chip select 0.
7-0	PI_MR15_DATA_0	R/W	0h	Data to program into memory mode register 15 for chip select 0.

4.3.262 DDRSS_PI_261 Register (Offset = 2414h) [reset = 0h]

DDRSS_PI_261 is shown in [Figure 4-756](#) and described in [Table 4-1518](#).

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Table 4-1517. DDRSS_PI_261 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2414h

Figure 4-756. DDRSS_PI_261 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR15_DATA_1								PI_MR13_DATA_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR40_DATA_0								PI_MR32_DATA_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1518. DDRSS_PI_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR15_DATA_1	R/W	0h	Data to program into memory mode register 15 for chip select 1.
23-16	PI_MR13_DATA_1	R/W	0h	Data to program into memory mode register 13 for chip select 1.
15-8	PI_MR40_DATA_0	R/W	0h	Data to program into memory mode register 40 for chip select 0.
7-0	PI_MR32_DATA_0	R/W	0h	Data to program into memory mode register 32 for chip select 0.

4.3.263 DDRSS_PI_262 Register (Offset = 2418h) [reset = 0h]

DDRSS_PI_262 is shown in [Figure 4-757](#) and described in [Table 4-1520](#).

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Table 4-1519. DDRSS_PI_262 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2418h

Figure 4-757. DDRSS_PI_262 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR32_DATA_1								PI_MR20_DATA_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR17_DATA_1								PI_MR16_DATA_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1520. DDRSS_PI_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR32_DATA_1	R/W	0h	Data to program into memory mode register 32 for chip select 1.
23-16	PI_MR20_DATA_1	R/W	0h	Data to program into memory mode register 20 for chip select 1.
15-8	PI_MR17_DATA_1	R/W	0h	Data to program into memory mode register 17 for chip select 1.
7-0	PI_MR16_DATA_1	R/W	0h	Data to program into memory mode register 16 for chip select 1.

4.3.264 DDRSS_PI_263 Register (Offset = 241Ch) [reset = 0h]

DDRSS_PI_263 is shown in [Figure 4-758](#) and described in [Table 4-1522](#).

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Table 4-1521. DDRSS_PI_263 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 241Ch

Figure 4-758. DDRSS_PI_263 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR16_DATA_2								PI_MR15_DATA_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR13_DATA_2								PI_MR40_DATA_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1522. DDRSS_PI_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR16_DATA_2	R/W	0h	Data to program into memory mode register 16 for chip select 2.
23-16	PI_MR15_DATA_2	R/W	0h	Data to program into memory mode register 15 for chip select 2.
15-8	PI_MR13_DATA_2	R/W	0h	Data to program into memory mode register 13 for chip select 2.
7-0	PI_MR40_DATA_1	R/W	0h	Data to program into memory mode register 40 for chip select 1.

4.3.265 DDRSS_PI_264 Register (Offset = 2420h) [reset = 0h]

DDRSS_PI_264 is shown in [Figure 4-759](#) and described in [Table 4-1524](#).

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Table 4-1523. DDRSS_PI_264 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2420h

Figure 4-759. DDRSS_PI_264 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR40_DATA_2								PI_MR32_DATA_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR20_DATA_2								PI_MR17_DATA_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1524. DDRSS_PI_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR40_DATA_2	R/W	0h	Data to program into memory mode register 40 for chip select 2.
23-16	PI_MR32_DATA_2	R/W	0h	Data to program into memory mode register 32 for chip select 2.
15-8	PI_MR20_DATA_2	R/W	0h	Data to program into memory mode register 20 for chip select 2.
7-0	PI_MR17_DATA_2	R/W	0h	Data to program into memory mode register 17 for chip select 2.

4.3.266 DDRSS_PI_265 Register (Offset = 2424h) [reset = 0h]

DDRSS_PI_265 is shown in [Figure 4-760](#) and described in [Table 4-1526](#).

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Table 4-1525. DDRSS_PI_265 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2424h

Figure 4-760. DDRSS_PI_265 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR17_DATA_3								PI_MR16_DATA_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR15_DATA_3								PI_MR13_DATA_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1526. DDRSS_PI_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR17_DATA_3	R/W	0h	Data to program into memory mode register 17 for chip select 3.
23-16	PI_MR16_DATA_3	R/W	0h	Data to program into memory mode register 16 for chip select 3.
15-8	PI_MR15_DATA_3	R/W	0h	Data to program into memory mode register 15 for chip select 3.
7-0	PI_MR13_DATA_3	R/W	0h	Data to program into memory mode register 13 for chip select 3.

4.3.267 DDRSS_PI_266 Register (Offset = 2428h) [reset = X]

DDRSS_PI_266 is shown in [Figure 4-761](#) and described in [Table 4-1528](#).

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Table 4-1527. DDRSS_PI_266 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2428h

Figure 4-761. DDRSS_PI_266 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_CKE_MUX_0				PI_MR40_DATA_3							
R/W-X				R/W-0h				R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR32_DATA_3								PI_MR20_DATA_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1528. DDRSS_PI_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_CKE_MUX_0	R/W	0h	Command pin CKE_0 mux selector
23-16	PI_MR40_DATA_3	R/W	0h	Data to program into memory mode register 40 for chip select 3.
15-8	PI_MR32_DATA_3	R/W	0h	Data to program into memory mode register 32 for chip select 3.
7-0	PI_MR20_DATA_3	R/W	0h	Data to program into memory mode register 20 for chip select 3.

4.3.268 DDRSS_PI_267 Register (Offset = 242Ch) [reset = X]

DDRSS_PI_267 is shown in [Figure 4-762](#) and described in [Table 4-1530](#).

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Table 4-1529. DDRSS_PI_267 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 242Ch

Figure 4-762. DDRSS_PI_267 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PI_CS_MUX_0				RESERVED				PI_CKE_MUX_3			
R/W-X				R/W-0h				R/W-X				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PI_CKE_MUX_2				RESERVED				PI_CKE_MUX_1			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1530. DDRSS_PI_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_CS_MUX_0	R/W	0h	Command pin CS_0 mux selector
23-20	RESERVED	R/W	X	
19-16	PI_CKE_MUX_3	R/W	0h	Command pin CKE_3 mux selector
15-12	RESERVED	R/W	X	
11-8	PI_CKE_MUX_2	R/W	0h	Command pin CKE_2 mux selector
7-4	RESERVED	R/W	X	
3-0	PI_CKE_MUX_1	R/W	0h	Command pin CKE_1 mux selector

4.3.269 DDRSS_PI_268 Register (Offset = 2430h) [reset = X]

DDRSS_PI_268 is shown in [Figure 4-763](#) and described in [Table 4-1532](#).

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Table 4-1531. DDRSS_PI_268 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2430h

Figure 4-763. DDRSS_PI_268 Register

31	30	29	28	27	26	25	24
RESERVED				PI_RESET_N_MUX_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PI_CS_MUX_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_CS_MUX_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_CS_MUX_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1532. DDRSS_PI_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_RESET_N_MUX_0	R/W	0h	Command pin RESET_N_0 mux selector
23-20	RESERVED	R/W	X	
19-16	PI_CS_MUX_3	R/W	0h	Command pin CS_3 mux selector
15-12	RESERVED	R/W	X	
11-8	PI_CS_MUX_2	R/W	0h	Command pin CS_2 mux selector
7-4	RESERVED	R/W	X	
3-0	PI_CS_MUX_1	R/W	0h	Command pin CS_1 mux selector

4.3.270 DDRSS_PI_269 Register (Offset = 2434h) [reset = X]

DDRSS_PI_269 is shown in [Figure 4-764](#) and described in [Table 4-1534](#).

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Table 4-1533. DDRSS_PI_269 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2434h

Figure 4-764. DDRSS_PI_269 Register

31	30	29	28	27	26	25	24
PI_MRSINGLE_DATA_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PI_RESET_N_MUX_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PI_RESET_N_MUX_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PI_RESET_N_MUX_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1534. DDRSS_PI_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MRSINGLE_DATA_0	R/W	0h	Data to program into memory mode register single write to chip select 0.
23-20	RESERVED	R/W	X	
19-16	PI_RESET_N_MUX_3	R/W	0h	Command pin RESET_N_3 mux selector
15-12	RESERVED	R/W	X	
11-8	PI_RESET_N_MUX_2	R/W	0h	Command pin RESET_N_2 mux selector
7-4	RESERVED	R/W	X	
3-0	PI_RESET_N_MUX_1	R/W	0h	Command pin RESET_N_1 mux selector

4.3.271 DDRSS_PI_270 Register (Offset = 2438h) [reset = X]

DDRSS_PI_270 is shown in [Figure 4-765](#) and described in [Table 4-1536](#).

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Table 4-1535. DDRSS_PI_270 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2438h

Figure 4-765. DDRSS_PI_270 Register

31	30	29	28	27	26	25	24
RESERVED				PI_ZQ_CAL_START_MAP_0			
R/W-X				R/W-1h			
23	22	21	20	19	18	17	16
PI_MRSINGLE_DATA_3							
R/W-0h							
15	14	13	12	11	10	9	8
PI_MRSINGLE_DATA_2							
R/W-0h							
7	6	5	4	3	2	1	0
PI_MRSINGLE_DATA_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1536. DDRSS_PI_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_ZQ_CAL_START_MAP_0	R/W	1h	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands.
23-16	PI_MRSINGLE_DATA_3	R/W	0h	Data to program into memory mode register single write to chip select 3.
15-8	PI_MRSINGLE_DATA_2	R/W	0h	Data to program into memory mode register single write to chip select 2.
7-0	PI_MRSINGLE_DATA_1	R/W	0h	Data to program into memory mode register single write to chip select 1.

4.3.272 DDRSS_PI_271 Register (Offset = 243Ch) [reset = X]

DDRSS_PI_271 is shown in [Figure 4-766](#) and described in [Table 4-1538](#).

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Table 4-1537. DDRSS_PI_271 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 243Ch

Figure 4-766. DDRSS_PI_271 Register

31	30	29	28	27	26	25	24
RESERVED				PI_ZQ_CAL_START_MAP_2			
R/W-X				R/W-4h			
23	22	21	20	19	18	17	16
RESERVED				PI_ZQ_CAL_LATCH_MAP_1			
R/W-X				R/W-2h			
15	14	13	12	11	10	9	8
RESERVED				PI_ZQ_CAL_START_MAP_1			
R/W-X				R/W-2h			
7	6	5	4	3	2	1	0
RESERVED				PI_ZQ_CAL_LATCH_MAP_0			
R/W-X				R/W-1h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1538. DDRSS_PI_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PI_ZQ_CAL_START_MAP_2	R/W	4h	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 2 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands.
23-20	RESERVED	R/W	X	
19-16	PI_ZQ_CAL_LATCH_MAP_1	R/W	2h	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands.
15-12	RESERVED	R/W	X	
11-8	PI_ZQ_CAL_START_MAP_1	R/W	2h	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands.
7-4	RESERVED	R/W	X	
3-0	PI_ZQ_CAL_LATCH_MAP_0	R/W	1h	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands.

4.3.273 DDRSS_PI_272 Register (Offset = 2440h) [reset = X]

DDRSS_PI_272 is shown in [Figure 4-767](#) and described in [Table 4-1540](#).

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Table 4-1539. DDRSS_PI_272 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2440h

Figure 4-767. DDRSS_PI_272 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PI_ZQ_CAL_LATCH_MAP_3			
R/W-X				R/W-8h			
15	14	13	12	11	10	9	8
RESERVED				PI_ZQ_CAL_START_MAP_3			
R/W-X				R/W-8h			
7	6	5	4	3	2	1	0
RESERVED				PI_ZQ_CAL_LATCH_MAP_2			
R/W-X				R/W-4h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1540. DDRSS_PI_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PI_ZQ_CAL_LATCH_MAP_3	R/W	8h	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 3 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands.
15-12	RESERVED	R/W	X	
11-8	PI_ZQ_CAL_START_MAP_3	R/W	8h	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 3 of the ZQ START initialization and periodic command sequences. Clear to all zeros for no ZQ START commands.
7-4	RESERVED	R/W	X	
3-0	PI_ZQ_CAL_LATCH_MAP_2	R/W	4h	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 2 of the ZQ LATCH initialization and periodic command sequences. Clear to all zeros for no ZQ LATCH commands.

4.3.274 DDRSS_PI_273 Register (Offset = 2444h) [reset = 0h]

DDRSS_PI_273 is shown in [Figure 4-768](#) and described in [Table 4-1542](#).

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Table 4-1541. DDRSS_PI_273 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2444h

Figure 4-768. DDRSS_PI_273 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_DQS_OSC_BASE_VALUE_1_0															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_DQS_OSC_BASE_VALUE_0_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1542. DDRSS_PI_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PI_DQS_OSC_BASE_VALUE_1_0	R/W	0h	Base value for comparison of oscillator measurement for device 1 of rank 0
15-0	PI_DQS_OSC_BASE_VALUE_0_0	R/W	0h	Base value for comparison of oscillator measurement for device 0 of rank 0

4.3.275 DDRSS_PI_274 Register (Offset = 2448h) [reset = 0h]

DDRSS_PI_274 is shown in [Figure 4-769](#) and described in [Table 4-1544](#).

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Table 4-1543. DDRSS_PI_274 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2448h

Figure 4-769. DDRSS_PI_274 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_DQS_OSC_BASE_VALUE_1_1															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_DQS_OSC_BASE_VALUE_0_1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1544. DDRSS_PI_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PI_DQS_OSC_BASE_VALUE_1_1	R/W	0h	Base value for comparison of oscillator measurement for device 1 of rank 1
15-0	PI_DQS_OSC_BASE_VALUE_0_1	R/W	0h	Base value for comparison of oscillator measurement for device 0 of rank 1

4.3.276 DDRSS_PI_275 Register (Offset = 244Ch) [reset = 0h]

DDRSS_PI_275 is shown in [Figure 4-770](#) and described in [Table 4-1546](#).

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Table 4-1545. DDRSS_PI_275 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 244Ch

Figure 4-770. DDRSS_PI_275 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F0_0								PI_MR3_DATA_F0_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_0								PI_MR1_DATA_F0_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1546. DDRSS_PI_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F0_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 0.
23-16	PI_MR3_DATA_F0_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 0.
15-8	PI_MR2_DATA_F0_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 0.
7-0	PI_MR1_DATA_F0_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 0.

4.3.277 DDRSS_PI_276 Register (Offset = 2450h) [reset = 0h]

DDRSS_PI_276 is shown in [Figure 4-771](#) and described in [Table 4-1548](#).

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Table 4-1547. DDRSS_PI_276 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2450h

Figure 4-771. DDRSS_PI_276 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F0_0								PI_MR22_DATA_F0_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F0_0								PI_MR12_DATA_F0_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1548. DDRSS_PI_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F0_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 0.
23-16	PI_MR22_DATA_F0_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 0.
15-8	PI_MR14_DATA_F0_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 0.
7-0	PI_MR12_DATA_F0_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 0.

4.3.278 DDRSS_PI_277 Register (Offset = 2454h) [reset = 0h]

DDRSS_PI_277 is shown in [Figure 4-772](#) and described in [Table 4-1550](#).

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Table 4-1549. DDRSS_PI_277 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2454h

Figure 4-772. DDRSS_PI_277 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F1_0								PI_MR3_DATA_F1_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F1_0								PI_MR1_DATA_F1_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1550. DDRSS_PI_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F1_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 1.
23-16	PI_MR3_DATA_F1_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 1.
15-8	PI_MR2_DATA_F1_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 1.
7-0	PI_MR1_DATA_F1_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 1.

4.3.279 DDRSS_PI_278 Register (Offset = 2458h) [reset = 0h]

DDRSS_PI_278 is shown in [Figure 4-773](#) and described in [Table 4-1552](#).

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Table 4-1551. DDRSS_PI_278 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2458h

Figure 4-773. DDRSS_PI_278 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F1_0								PI_MR22_DATA_F1_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F1_0								PI_MR12_DATA_F1_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1552. DDRSS_PI_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F1_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 1.
23-16	PI_MR22_DATA_F1_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 1.
15-8	PI_MR14_DATA_F1_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 1.
7-0	PI_MR12_DATA_F1_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 1.

4.3.280 DDRSS_PI_279 Register (Offset = 245Ch) [reset = 0h]

DDRSS_PI_279 is shown in [Figure 4-774](#) and described in [Table 4-1554](#).

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Table 4-1553. DDRSS_PI_279 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 245Ch

Figure 4-774. DDRSS_PI_279 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F2_0								PI_MR3_DATA_F2_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_0								PI_MR1_DATA_F2_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1554. DDRSS_PI_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F2_0	R/W	0h	Data to program into memory mode register 11 for chip select 0 for frequency set 2.
23-16	PI_MR3_DATA_F2_0	R/W	0h	Data to program into memory mode register 3 for chip select 0 for frequency set 2.
15-8	PI_MR2_DATA_F2_0	R/W	0h	Data to program into memory mode register 2 for chip select 0 for frequency set 2.
7-0	PI_MR1_DATA_F2_0	R/W	0h	Data to program into memory mode register 1 for chip select 0 for frequency set 2.

4.3.281 DDRSS_PI_280 Register (Offset = 2460h) [reset = 0h]

DDRSS_PI_280 is shown in [Figure 4-775](#) and described in [Table 4-1556](#).

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Table 4-1555. DDRSS_PI_280 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2460h

Figure 4-775. DDRSS_PI_280 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F2_0								PI_MR22_DATA_F2_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F2_0								PI_MR12_DATA_F2_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1556. DDRSS_PI_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F2_0	R/W	0h	Data to program into memory mode register 23 for chip select 0 for frequency set 2.
23-16	PI_MR22_DATA_F2_0	R/W	0h	Data to program into memory mode register 22 for chip select 0 for frequency set 2.
15-8	PI_MR14_DATA_F2_0	R/W	0h	Data to program into memory mode register 14 for chip select 0 for frequency set 2.
7-0	PI_MR12_DATA_F2_0	R/W	0h	Data to program into memory mode register 12 for chip select 0 for frequency set 2.

4.3.282 DDRSS_PI_281 Register (Offset = 2464h) [reset = 0h]

DDRSS_PI_281 is shown in [Figure 4-776](#) and described in [Table 4-1558](#).

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Table 4-1557. DDRSS_PI_281 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2464h

Figure 4-776. DDRSS_PI_281 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F0_1								PI_MR3_DATA_F0_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_1								PI_MR1_DATA_F0_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1558. DDRSS_PI_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F0_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 0.
23-16	PI_MR3_DATA_F0_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 0.
15-8	PI_MR2_DATA_F0_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 0.
7-0	PI_MR1_DATA_F0_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 0.

4.3.283 DDRSS_PI_282 Register (Offset = 2468h) [reset = 0h]

DDRSS_PI_282 is shown in [Figure 4-777](#) and described in [Table 4-1560](#).

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Table 4-1559. DDRSS_PI_282 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2468h

Figure 4-777. DDRSS_PI_282 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F0_1								PI_MR22_DATA_F0_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F0_1								PI_MR12_DATA_F0_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1560. DDRSS_PI_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F0_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 0.
23-16	PI_MR22_DATA_F0_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 0.
15-8	PI_MR14_DATA_F0_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 0.
7-0	PI_MR12_DATA_F0_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 0.

4.3.284 DDRSS_PI_283 Register (Offset = 246Ch) [reset = 0h]

DDRSS_PI_283 is shown in [Figure 4-778](#) and described in [Table 4-1562](#).

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Table 4-1561. DDRSS_PI_283 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 246Ch

Figure 4-778. DDRSS_PI_283 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F1_1								PI_MR3_DATA_F1_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F1_1								PI_MR1_DATA_F1_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1562. DDRSS_PI_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F1_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 1.
23-16	PI_MR3_DATA_F1_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 1.
15-8	PI_MR2_DATA_F1_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 1.
7-0	PI_MR1_DATA_F1_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 1.

4.3.285 DDRSS_PI_284 Register (Offset = 2470h) [reset = 0h]

DDRSS_PI_284 is shown in [Figure 4-779](#) and described in [Table 4-1564](#).

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Table 4-1563. DDRSS_PI_284 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2470h

Figure 4-779. DDRSS_PI_284 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F1_1								PI_MR22_DATA_F1_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F1_1								PI_MR12_DATA_F1_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1564. DDRSS_PI_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F1_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 1.
23-16	PI_MR22_DATA_F1_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 1.
15-8	PI_MR14_DATA_F1_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 1.
7-0	PI_MR12_DATA_F1_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 1.

4.3.286 DDRSS_PI_285 Register (Offset = 2474h) [reset = 0h]

DDRSS_PI_285 is shown in [Figure 4-780](#) and described in [Table 4-1566](#).

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Table 4-1565. DDRSS_PI_285 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2474h

Figure 4-780. DDRSS_PI_285 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F2_1								PI_MR3_DATA_F2_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_1								PI_MR1_DATA_F2_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1566. DDRSS_PI_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F2_1	R/W	0h	Data to program into memory mode register 11 for chip select 1 for frequency set 2.
23-16	PI_MR3_DATA_F2_1	R/W	0h	Data to program into memory mode register 3 for chip select 1 for frequency set 2.
15-8	PI_MR2_DATA_F2_1	R/W	0h	Data to program into memory mode register 2 for chip select 1 for frequency set 2.
7-0	PI_MR1_DATA_F2_1	R/W	0h	Data to program into memory mode register 1 for chip select 1 for frequency set 2.

4.3.287 DDRSS_PI_286 Register (Offset = 2478h) [reset = 0h]

DDRSS_PI_286 is shown in [Figure 4-781](#) and described in [Table 4-1568](#).

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Table 4-1567. DDRSS_PI_286 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2478h

Figure 4-781. DDRSS_PI_286 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F2_1								PI_MR22_DATA_F2_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F2_1								PI_MR12_DATA_F2_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1568. DDRSS_PI_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F2_1	R/W	0h	Data to program into memory mode register 23 for chip select 1 for frequency set 2.
23-16	PI_MR22_DATA_F2_1	R/W	0h	Data to program into memory mode register 22 for chip select 1 for frequency set 2.
15-8	PI_MR14_DATA_F2_1	R/W	0h	Data to program into memory mode register 14 for chip select 1 for frequency set 2.
7-0	PI_MR12_DATA_F2_1	R/W	0h	Data to program into memory mode register 12 for chip select 1 for frequency set 2.

4.3.288 DDRSS_PI_287 Register (Offset = 247Ch) [reset = 0h]

DDRSS_PI_287 is shown in [Figure 4-782](#) and described in [Table 4-1570](#).

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Table 4-1569. DDRSS_PI_287 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 247Ch

Figure 4-782. DDRSS_PI_287 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F0_2								PI_MR3_DATA_F0_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_2								PI_MR1_DATA_F0_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1570. DDRSS_PI_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F0_2	R/W	0h	Data to program into memory mode register 11 for chip select 2 for frequency set 0.
23-16	PI_MR3_DATA_F0_2	R/W	0h	Data to program into memory mode register 3 for chip select 2 for frequency set 0.
15-8	PI_MR2_DATA_F0_2	R/W	0h	Data to program into memory mode register 2 for chip select 2 for frequency set 0.
7-0	PI_MR1_DATA_F0_2	R/W	0h	Data to program into memory mode register 1 for chip select 2 for frequency set 0.

4.3.289 DDRSS_PI_288 Register (Offset = 2480h) [reset = 0h]

DDRSS_PI_288 is shown in [Figure 4-783](#) and described in [Table 4-1572](#).

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Table 4-1571. DDRSS_PI_288 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2480h

Figure 4-783. DDRSS_PI_288 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F0_2								PI_MR22_DATA_F0_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F0_2								PI_MR12_DATA_F0_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1572. DDRSS_PI_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F0_2	R/W	0h	Data to program into memory mode register 23 for chip select 2 for frequency set 0.
23-16	PI_MR22_DATA_F0_2	R/W	0h	Data to program into memory mode register 22 for chip select 2 for frequency set 0.
15-8	PI_MR14_DATA_F0_2	R/W	0h	Data to program into memory mode register 14 for chip select 2 for frequency set 0.
7-0	PI_MR12_DATA_F0_2	R/W	0h	Data to program into memory mode register 12 for chip select 2 for frequency set 0.

4.3.290 DDRSS_PI_289 Register (Offset = 2484h) [reset = 0h]

DDRSS_PI_289 is shown in [Figure 4-784](#) and described in [Table 4-1574](#).

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Table 4-1573. DDRSS_PI_289 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2484h

Figure 4-784. DDRSS_PI_289 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F1_2								PI_MR3_DATA_F1_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F1_2								PI_MR1_DATA_F1_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1574. DDRSS_PI_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F1_2	R/W	0h	Data to program into memory mode register 11 for chip select 2 for frequency set 1.
23-16	PI_MR3_DATA_F1_2	R/W	0h	Data to program into memory mode register 3 for chip select 2 for frequency set 1.
15-8	PI_MR2_DATA_F1_2	R/W	0h	Data to program into memory mode register 2 for chip select 2 for frequency set 1.
7-0	PI_MR1_DATA_F1_2	R/W	0h	Data to program into memory mode register 1 for chip select 2 for frequency set 1.

4.3.291 DDRSS_PI_290 Register (Offset = 2488h) [reset = 0h]

DDRSS_PI_290 is shown in [Figure 4-785](#) and described in [Table 4-1576](#).

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Table 4-1575. DDRSS_PI_290 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2488h

Figure 4-785. DDRSS_PI_290 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F1_2								PI_MR22_DATA_F1_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F1_2								PI_MR12_DATA_F1_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1576. DDRSS_PI_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F1_2	R/W	0h	Data to program into memory mode register 23 for chip select 2 for frequency set 1.
23-16	PI_MR22_DATA_F1_2	R/W	0h	Data to program into memory mode register 22 for chip select 2 for frequency set 1.
15-8	PI_MR14_DATA_F1_2	R/W	0h	Data to program into memory mode register 14 for chip select 2 for frequency set 1.
7-0	PI_MR12_DATA_F1_2	R/W	0h	Data to program into memory mode register 12 for chip select 2 for frequency set 1.

4.3.292 DDRSS_PI_291 Register (Offset = 248Ch) [reset = 0h]

DDRSS_PI_291 is shown in [Figure 4-786](#) and described in [Table 4-1578](#).

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Table 4-1577. DDRSS_PI_291 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 248Ch

Figure 4-786. DDRSS_PI_291 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F2_2								PI_MR3_DATA_F2_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_2								PI_MR1_DATA_F2_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1578. DDRSS_PI_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F2_2	R/W	0h	Data to program into memory mode register 11 for chip select 2 for frequency set 2.
23-16	PI_MR3_DATA_F2_2	R/W	0h	Data to program into memory mode register 3 for chip select 2 for frequency set 2.
15-8	PI_MR2_DATA_F2_2	R/W	0h	Data to program into memory mode register 2 for chip select 2 for frequency set 2.
7-0	PI_MR1_DATA_F2_2	R/W	0h	Data to program into memory mode register 1 for chip select 2 for frequency set 2.

4.3.293 DDRSS_PI_292 Register (Offset = 2490h) [reset = 0h]

DDRSS_PI_292 is shown in [Figure 4-787](#) and described in [Table 4-1580](#).

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Table 4-1579. DDRSS_PI_292 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2490h

Figure 4-787. DDRSS_PI_292 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F2_2								PI_MR22_DATA_F2_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F2_2								PI_MR12_DATA_F2_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1580. DDRSS_PI_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F2_2	R/W	0h	Data to program into memory mode register 23 for chip select 2 for frequency set 2.
23-16	PI_MR22_DATA_F2_2	R/W	0h	Data to program into memory mode register 22 for chip select 2 for frequency set 2.
15-8	PI_MR14_DATA_F2_2	R/W	0h	Data to program into memory mode register 14 for chip select 2 for frequency set 2.
7-0	PI_MR12_DATA_F2_2	R/W	0h	Data to program into memory mode register 12 for chip select 2 for frequency set 2.

4.3.294 DDRSS_PI_293 Register (Offset = 2494h) [reset = 0h]

DDRSS_PI_293 is shown in [Figure 4-788](#) and described in [Table 4-1582](#).

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Table 4-1581. DDRSS_PI_293 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2494h

Figure 4-788. DDRSS_PI_293 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F0_3								PI_MR3_DATA_F0_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F0_3								PI_MR1_DATA_F0_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1582. DDRSS_PI_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F0_3	R/W	0h	Data to program into memory mode register 11 for chip select 3 for frequency set 0.
23-16	PI_MR3_DATA_F0_3	R/W	0h	Data to program into memory mode register 3 for chip select 3 for frequency set 0.
15-8	PI_MR2_DATA_F0_3	R/W	0h	Data to program into memory mode register 2 for chip select 3 for frequency set 0.
7-0	PI_MR1_DATA_F0_3	R/W	0h	Data to program into memory mode register 1 for chip select 3 for frequency set 0.

4.3.295 DDRSS_PI_294 Register (Offset = 2498h) [reset = 0h]

DDRSS_PI_294 is shown in [Figure 4-789](#) and described in [Table 4-1584](#).

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Table 4-1583. DDRSS_PI_294 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 2498h

Figure 4-789. DDRSS_PI_294 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F0_3								PI_MR22_DATA_F0_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F0_3								PI_MR12_DATA_F0_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1584. DDRSS_PI_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F0_3	R/W	0h	Data to program into memory mode register 23 for chip select 3 for frequency set 0.
23-16	PI_MR22_DATA_F0_3	R/W	0h	Data to program into memory mode register 22 for chip select 3 for frequency set 0.
15-8	PI_MR14_DATA_F0_3	R/W	0h	Data to program into memory mode register 14 for chip select 3 for frequency set 0.
7-0	PI_MR12_DATA_F0_3	R/W	0h	Data to program into memory mode register 12 for chip select 3 for frequency set 0.

4.3.296 DDRSS_PI_295 Register (Offset = 249Ch) [reset = 0h]

DDRSS_PI_295 is shown in [Figure 4-790](#) and described in [Table 4-1586](#).

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Table 4-1585. DDRSS_PI_295 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 249Ch

Figure 4-790. DDRSS_PI_295 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F1_3								PI_MR3_DATA_F1_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F1_3								PI_MR1_DATA_F1_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1586. DDRSS_PI_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F1_3	R/W	0h	Data to program into memory mode register 11 for chip select 3 for frequency set 1.
23-16	PI_MR3_DATA_F1_3	R/W	0h	Data to program into memory mode register 3 for chip select 3 for frequency set 1.
15-8	PI_MR2_DATA_F1_3	R/W	0h	Data to program into memory mode register 2 for chip select 3 for frequency set 1.
7-0	PI_MR1_DATA_F1_3	R/W	0h	Data to program into memory mode register 1 for chip select 3 for frequency set 1.

4.3.297 DDRSS_PI_296 Register (Offset = 24A0h) [reset = 0h]

DDRSS_PI_296 is shown in [Figure 4-791](#) and described in [Table 4-1588](#).

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Table 4-1587. DDRSS_PI_296 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 24A0h

Figure 4-791. DDRSS_PI_296 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F1_3								PI_MR22_DATA_F1_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F1_3								PI_MR12_DATA_F1_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1588. DDRSS_PI_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F1_3	R/W	0h	Data to program into memory mode register 23 for chip select 3 for frequency set 1.
23-16	PI_MR22_DATA_F1_3	R/W	0h	Data to program into memory mode register 22 for chip select 3 for frequency set 1.
15-8	PI_MR14_DATA_F1_3	R/W	0h	Data to program into memory mode register 14 for chip select 3 for frequency set 1.
7-0	PI_MR12_DATA_F1_3	R/W	0h	Data to program into memory mode register 12 for chip select 3 for frequency set 1.

4.3.298 DDRSS_PI_297 Register (Offset = 24A4h) [reset = 0h]

DDRSS_PI_297 is shown in [Figure 4-792](#) and described in [Table 4-1590](#).

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Table 4-1589. DDRSS_PI_297 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 24A4h

Figure 4-792. DDRSS_PI_297 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR11_DATA_F2_3								PI_MR3_DATA_F2_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR2_DATA_F2_3								PI_MR1_DATA_F2_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1590. DDRSS_PI_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR11_DATA_F2_3	R/W	0h	Data to program into memory mode register 11 for chip select 3 for frequency set 2.
23-16	PI_MR3_DATA_F2_3	R/W	0h	Data to program into memory mode register 3 for chip select 3 for frequency set 2.
15-8	PI_MR2_DATA_F2_3	R/W	0h	Data to program into memory mode register 2 for chip select 3 for frequency set 2.
7-0	PI_MR1_DATA_F2_3	R/W	0h	Data to program into memory mode register 1 for chip select 3 for frequency set 2.

4.3.299 DDRSS_PI_298 Register (Offset = 24A8h) [reset = 0h]

DDRSS_PI_298 is shown in [Figure 4-793](#) and described in [Table 4-1592](#).

Return to [Summary Table](#).

Table 4-1591. DDRSS_PI_298 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 24A8h

Figure 4-793. DDRSS_PI_298 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PI_MR23_DATA_F2_3								PI_MR22_DATA_F2_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PI_MR14_DATA_F2_3								PI_MR12_DATA_F2_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1592. DDRSS_PI_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PI_MR23_DATA_F2_3	R/W	0h	Data to program into memory mode register 23 for chip select 3 for frequency set 2.
23-16	PI_MR22_DATA_F2_3	R/W	0h	Data to program into memory mode register 22 for chip select 3 for frequency set 2.
15-8	PI_MR14_DATA_F2_3	R/W	0h	Data to program into memory mode register 14 for chip select 3 for frequency set 2.
7-0	PI_MR12_DATA_F2_3	R/W	0h	Data to program into memory mode register 12 for chip select 3 for frequency set 2.

4.3.300 DDRSS_PI_299 Register (Offset = 24ACh) [reset = X]

DDRSS_PI_299 is shown in [Figure 4-794](#) and described in [Table 4-1594](#).

Return to [Summary Table](#).

Table 4-1593. DDRSS_PI_299 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PI	0299 24ACh

Figure 4-794. DDRSS_PI_299 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PI_PARITY_ERROR_REGIF										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1594. DDRSS_PI_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	PI_PARITY_ERROR_REGIF	R/W	0h	Inject parity error to regisster interface signals for PI. WRITE-ONLY

4.4 DDR PHY Registers

Table 4-1596 lists the memory-mapped registers for the DDR PHY. All register offset addresses not listed in Table 4-1596 should be considered as reserved locations and the register contents should not be modified.

Table 4-1595. DDR PHY Instances

Instance	Base Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 0000h

Table 4-1596. DDR PHY Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PHY Physical Address
4000h	DDRSS_PHY_0	DDR PHY Register 0	0299 4000h
4004h	DDRSS_PHY_1	DDR PHY Register 1	0299 4004h
4008h	DDRSS_PHY_2	DDR PHY Register 2	0299 4008h
400Ch	DDRSS_PHY_3	DDR PHY Register 3	0299 400Ch
4010h	DDRSS_PHY_4	DDR PHY Register 4	0299 4010h
4014h	DDRSS_PHY_5	DDR PHY Register 5	0299 4014h
4018h	DDRSS_PHY_6	DDR PHY Register 6	0299 4018h
401Ch	DDRSS_PHY_7	DDR PHY Register 7	0299 401Ch
4020h	DDRSS_PHY_8	DDR PHY Register 8	0299 4020h
4024h	DDRSS_PHY_9	DDR PHY Register 9	0299 4024h
4028h	DDRSS_PHY_10	DDR PHY Register 10	0299 4028h
402Ch	DDRSS_PHY_11	DDR PHY Register 11	0299 402Ch
4030h	DDRSS_PHY_12	DDR PHY Register 12	0299 4030h
4034h	DDRSS_PHY_13	DDR PHY Register 13	0299 4034h
4038h	DDRSS_PHY_14	DDR PHY Register 14	0299 4038h
403Ch	DDRSS_PHY_15	DDR PHY Register 15	0299 403Ch
4040h	DDRSS_PHY_16	DDR PHY Register 16	0299 4040h
4044h	DDRSS_PHY_17	DDR PHY Register 17	0299 4044h
4048h	DDRSS_PHY_18	DDR PHY Register 18	0299 4048h
404Ch	DDRSS_PHY_19	DDR PHY Register 19	0299 404Ch
4050h	DDRSS_PHY_20	DDR PHY Register 20	0299 4050h
4054h	DDRSS_PHY_21	DDR PHY Register 21	0299 4054h
4058h	DDRSS_PHY_22	DDR PHY Register 22	0299 4058h
405Ch	DDRSS_PHY_23	DDR PHY Register 23	0299 405Ch
4060h	DDRSS_PHY_24	DDR PHY Register 24	0299 4060h
4064h	DDRSS_PHY_25	DDR PHY Register 25	0299 4064h
4068h	DDRSS_PHY_26	DDR PHY Register 26	0299 4068h
406Ch	DDRSS_PHY_27	DDR PHY Register 27	0299 406Ch
4070h	DDRSS_PHY_28	DDR PHY Register 28	0299 4070h
4074h	DDRSS_PHY_29	DDR PHY Register 29	0299 4074h
4078h	DDRSS_PHY_30	DDR PHY Register 30	0299 4078h
407Ch	DDRSS_PHY_31	DDR PHY Register 31	0299 407Ch
4080h	DDRSS_PHY_32	DDR PHY Register 32	0299 4080h
4084h	DDRSS_PHY_33	DDR PHY Register 33	0299 4084h
4088h	DDRSS_PHY_34	DDR PHY Register 34	0299 4088h
408Ch	DDRSS_PHY_35	DDR PHY Register 35	0299 408Ch
4090h	DDRSS_PHY_36	DDR PHY Register 36	0299 4090h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4094h	DDRSS_PHY_37	DDR PHY Register 37	0299 4094h
4098h	DDRSS_PHY_38	DDR PHY Register 38	0299 4098h
409Ch	DDRSS_PHY_39	DDR PHY Register 39	0299 409Ch
40A0h	DDRSS_PHY_40	DDR PHY Register 40	0299 40A0h
40A4h	DDRSS_PHY_41	DDR PHY Register 41	0299 40A4h
40A8h	DDRSS_PHY_42	DDR PHY Register 42	0299 40A8h
40ACh	DDRSS_PHY_43	DDR PHY Register 43	0299 40ACh
40B0h	DDRSS_PHY_44	DDR PHY Register 44	0299 40B0h
40B4h	DDRSS_PHY_45	DDR PHY Register 45	0299 40B4h
40B8h	DDRSS_PHY_46	DDR PHY Register 46	0299 40B8h
40BCh	DDRSS_PHY_47	DDR PHY Register 47	0299 40BCh
40C0h	DDRSS_PHY_48	DDR PHY Register 48	0299 40C0h
40C4h	DDRSS_PHY_49	DDR PHY Register 49	0299 40C4h
40C8h	DDRSS_PHY_50	DDR PHY Register 50	0299 40C8h
40CCh	DDRSS_PHY_51	DDR PHY Register 51	0299 40CCh
40D0h	DDRSS_PHY_52	DDR PHY Register 52	0299 40D0h
40D4h	DDRSS_PHY_53	DDR PHY Register 53	0299 40D4h
40D8h	DDRSS_PHY_54	DDR PHY Register 54	0299 40D8h
40DCh	DDRSS_PHY_55	DDR PHY Register 55	0299 40DCh
40E0h	DDRSS_PHY_56	DDR PHY Register 56	0299 40E0h
40E4h	DDRSS_PHY_57	DDR PHY Register 57	0299 40E4h
40E8h	DDRSS_PHY_58	DDR PHY Register 58	0299 40E8h
40ECh	DDRSS_PHY_59	DDR PHY Register 59	0299 40ECh
40F0h	DDRSS_PHY_60	DDR PHY Register 60	0299 40F0h
40F4h	DDRSS_PHY_61	DDR PHY Register 61	0299 40F4h
40F8h	DDRSS_PHY_62	DDR PHY Register 62	0299 40F8h
40FCh	DDRSS_PHY_63	DDR PHY Register 63	0299 40FCh
4100h	DDRSS_PHY_64	DDR PHY Register 64	0299 4100h
4104h	DDRSS_PHY_65	DDR PHY Register 65	0299 4104h
4108h	DDRSS_PHY_66	DDR PHY Register 66	0299 4108h
410Ch	DDRSS_PHY_67	DDR PHY Register 67	0299 410Ch
4110h	DDRSS_PHY_68	DDR PHY Register 68	0299 4110h
4114h	DDRSS_PHY_69	DDR PHY Register 69	0299 4114h
4118h	DDRSS_PHY_70	DDR PHY Register 70	0299 4118h
411Ch	DDRSS_PHY_71	DDR PHY Register 71	0299 411Ch
4120h	DDRSS_PHY_72	DDR PHY Register 72	0299 4120h
4124h	DDRSS_PHY_73	DDR PHY Register 73	0299 4124h
4128h	DDRSS_PHY_74	DDR PHY Register 74	0299 4128h
412Ch	DDRSS_PHY_75	DDR PHY Register 75	0299 412Ch
4130h	DDRSS_PHY_76	DDR PHY Register 76	0299 4130h
4134h	DDRSS_PHY_77	DDR PHY Register 77	0299 4134h
4138h	DDRSS_PHY_78	DDR PHY Register 78	0299 4138h
413Ch	DDRSS_PHY_79	DDR PHY Register 79	0299 413Ch
4140h	DDRSS_PHY_80	DDR PHY Register 80	0299 4140h
4144h	DDRSS_PHY_81	DDR PHY Register 81	0299 4144h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4148h	DDRSS_PHY_82	DDR PHY Register 82	0299 4148h
414Ch	DDRSS_PHY_83	DDR PHY Register 83	0299 414Ch
4150h	DDRSS_PHY_84	DDR PHY Register 84	0299 4150h
4154h	DDRSS_PHY_85	DDR PHY Register 85	0299 4154h
4158h	DDRSS_PHY_86	DDR PHY Register 86	0299 4158h
415Ch	DDRSS_PHY_87	DDR PHY Register 87	0299 415Ch
4160h	DDRSS_PHY_88	DDR PHY Register 88	0299 4160h
4164h	DDRSS_PHY_89	DDR PHY Register 89	0299 4164h
4168h	DDRSS_PHY_90	DDR PHY Register 90	0299 4168h
416Ch	DDRSS_PHY_91	DDR PHY Register 91	0299 416Ch
4170h	DDRSS_PHY_92	DDR PHY Register 92	0299 4170h
4174h	DDRSS_PHY_93	DDR PHY Register 93	0299 4174h
4178h	DDRSS_PHY_94	DDR PHY Register 94	0299 4178h
417Ch	DDRSS_PHY_95	DDR PHY Register 95	0299 417Ch
4180h	DDRSS_PHY_96	DDR PHY Register 96	0299 4180h
4184h	DDRSS_PHY_97	DDR PHY Register 97	0299 4184h
4188h	DDRSS_PHY_98	DDR PHY Register 98	0299 4188h
418Ch	DDRSS_PHY_99	DDR PHY Register 99	0299 418Ch
4190h	DDRSS_PHY_100	DDR PHY Register 100	0299 4190h
4194h	DDRSS_PHY_101	DDR PHY Register 101	0299 4194h
4198h	DDRSS_PHY_102	DDR PHY Register 102	0299 4198h
419Ch	DDRSS_PHY_103	DDR PHY Register 103	0299 419Ch
41A0h	DDRSS_PHY_104	DDR PHY Register 104	0299 41A0h
41A4h	DDRSS_PHY_105	DDR PHY Register 105	0299 41A4h
41A8h	DDRSS_PHY_106	DDR PHY Register 106	0299 41A8h
41ACh	DDRSS_PHY_107	DDR PHY Register 107	0299 41ACh
41B0h	DDRSS_PHY_108	DDR PHY Register 108	0299 41B0h
41B4h	DDRSS_PHY_109	DDR PHY Register 109	0299 41B4h
41B8h	DDRSS_PHY_110	DDR PHY Register 110	0299 41B8h
41BCh	DDRSS_PHY_111	DDR PHY Register 111	0299 41BCh
41C0h	DDRSS_PHY_112	DDR PHY Register 112	0299 41C0h
41C4h	DDRSS_PHY_113	DDR PHY Register 113	0299 41C4h
41C8h	DDRSS_PHY_114	DDR PHY Register 114	0299 41C8h
41CCh	DDRSS_PHY_115	DDR PHY Register 115	0299 41CCh
41D0h	DDRSS_PHY_116	DDR PHY Register 116	0299 41D0h
41D4h	DDRSS_PHY_117	DDR PHY Register 117	0299 41D4h
41D8h	DDRSS_PHY_118	DDR PHY Register 118	0299 41D8h
41DCh	DDRSS_PHY_119	DDR PHY Register 119	0299 41DCh
41E0h	DDRSS_PHY_120	DDR PHY Register 120	0299 41E0h
41E4h	DDRSS_PHY_121	DDR PHY Register 121	0299 41E4h
41E8h	DDRSS_PHY_122	DDR PHY Register 122	0299 41E8h
41ECh	DDRSS_PHY_123	DDR PHY Register 123	0299 41ECh
41F0h	DDRSS_PHY_124	DDR PHY Register 124	0299 41F0h
41F4h	DDRSS_PHY_125	DDR PHY Register 125	0299 41F4h
41F8h	DDRSS_PHY_126	DDR PHY Register 126	0299 41F8h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
41FCh	DDRSS_PHY_127	DDR PHY Register 127	0299 41FCh
4200h	DDRSS_PHY_128	DDR PHY Register 128	0299 4200h
4204h	DDRSS_PHY_129	DDR PHY Register 129	0299 4204h
4208h	DDRSS_PHY_130	DDR PHY Register 130	0299 4208h
420Ch	DDRSS_PHY_131	DDR PHY Register 131	0299 420Ch
4210h	DDRSS_PHY_132	DDR PHY Register 132	0299 4210h
4214h	DDRSS_PHY_133	DDR PHY Register 133	0299 4214h
4218h	DDRSS_PHY_134	DDR PHY Register 134	0299 4218h
421Ch	DDRSS_PHY_135	DDR PHY Register 135	0299 421Ch
4220h	DDRSS_PHY_136	DDR PHY Register 136	0299 4220h
4224h	DDRSS_PHY_137	DDR PHY Register 137	0299 4224h
4228h	DDRSS_PHY_138	DDR PHY Register 138	0299 4228h
422Ch	DDRSS_PHY_139	DDR PHY Register 139	0299 422Ch
4400h	DDRSS_PHY_256	DDR PHY Register 256	0299 4400h
4404h	DDRSS_PHY_257	DDR PHY Register 257	0299 4404h
4408h	DDRSS_PHY_258	DDR PHY Register 258	0299 4408h
440Ch	DDRSS_PHY_259	DDR PHY Register 259	0299 440Ch
4410h	DDRSS_PHY_260	DDR PHY Register 260	0299 4410h
4414h	DDRSS_PHY_261	DDR PHY Register 261	0299 4414h
4418h	DDRSS_PHY_262	DDR PHY Register 262	0299 4418h
441Ch	DDRSS_PHY_263	DDR PHY Register 263	0299 441Ch
4420h	DDRSS_PHY_264	DDR PHY Register 264	0299 4420h
4424h	DDRSS_PHY_265	DDR PHY Register 265	0299 4424h
4428h	DDRSS_PHY_266	DDR PHY Register 266	0299 4428h
442Ch	DDRSS_PHY_267	DDR PHY Register 267	0299 442Ch
4430h	DDRSS_PHY_268	DDR PHY Register 268	0299 4430h
4434h	DDRSS_PHY_269	DDR PHY Register 269	0299 4434h
4438h	DDRSS_PHY_270	DDR PHY Register 270	0299 4438h
443Ch	DDRSS_PHY_271	DDR PHY Register 271	0299 443Ch
4440h	DDRSS_PHY_272	DDR PHY Register 272	0299 4440h
4444h	DDRSS_PHY_273	DDR PHY Register 273	0299 4444h
4448h	DDRSS_PHY_274	DDR PHY Register 274	0299 4448h
444Ch	DDRSS_PHY_275	DDR PHY Register 275	0299 444Ch
4450h	DDRSS_PHY_276	DDR PHY Register 276	0299 4450h
4454h	DDRSS_PHY_277	DDR PHY Register 277	0299 4454h
4458h	DDRSS_PHY_278	DDR PHY Register 278	0299 4458h
445Ch	DDRSS_PHY_279	DDR PHY Register 279	0299 445Ch
4460h	DDRSS_PHY_280	DDR PHY Register 280	0299 4460h
4464h	DDRSS_PHY_281	DDR PHY Register 281	0299 4464h
4468h	DDRSS_PHY_282	DDR PHY Register 282	0299 4468h
446Ch	DDRSS_PHY_283	DDR PHY Register 283	0299 446Ch
4470h	DDRSS_PHY_284	DDR PHY Register 284	0299 4470h
4474h	DDRSS_PHY_285	DDR PHY Register 285	0299 4474h
4478h	DDRSS_PHY_286	DDR PHY Register 286	0299 4478h
447Ch	DDRSS_PHY_287	DDR PHY Register 287	0299 447Ch

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CTL_CFG_PHY Physical Address
4480h	DDRSS_PHY_288	DDR PHY Register 288	0299 4480h
4484h	DDRSS_PHY_289	DDR PHY Register 289	0299 4484h
4488h	DDRSS_PHY_290	DDR PHY Register 290	0299 4488h
448Ch	DDRSS_PHY_291	DDR PHY Register 291	0299 448Ch
4490h	DDRSS_PHY_292	DDR PHY Register 292	0299 4490h
4494h	DDRSS_PHY_293	DDR PHY Register 293	0299 4494h
4498h	DDRSS_PHY_294	DDR PHY Register 294	0299 4498h
449Ch	DDRSS_PHY_295	DDR PHY Register 295	0299 449Ch
44A0h	DDRSS_PHY_296	DDR PHY Register 296	0299 44A0h
44A4h	DDRSS_PHY_297	DDR PHY Register 297	0299 44A4h
44A8h	DDRSS_PHY_298	DDR PHY Register 298	0299 44A8h
44ACh	DDRSS_PHY_299	DDR PHY Register 299	0299 44ACh
44B0h	DDRSS_PHY_300	DDR PHY Register 300	0299 44B0h
44B4h	DDRSS_PHY_301	DDR PHY Register 301	0299 44B4h
44B8h	DDRSS_PHY_302	DDR PHY Register 302	0299 44B8h
44BCh	DDRSS_PHY_303	DDR PHY Register 303	0299 44BCh
44C0h	DDRSS_PHY_304	DDR PHY Register 304	0299 44C0h
44C4h	DDRSS_PHY_305	DDR PHY Register 305	0299 44C4h
44C8h	DDRSS_PHY_306	DDR PHY Register 306	0299 44C8h
44CCh	DDRSS_PHY_307	DDR PHY Register 307	0299 44CCh
44D0h	DDRSS_PHY_308	DDR PHY Register 308	0299 44D0h
44D4h	DDRSS_PHY_309	DDR PHY Register 309	0299 44D4h
44D8h	DDRSS_PHY_310	DDR PHY Register 310	0299 44D8h
44DCh	DDRSS_PHY_311	DDR PHY Register 311	0299 44DCh
44E0h	DDRSS_PHY_312	DDR PHY Register 312	0299 44E0h
44E4h	DDRSS_PHY_313	DDR PHY Register 313	0299 44E4h
44E8h	DDRSS_PHY_314	DDR PHY Register 314	0299 44E8h
44ECh	DDRSS_PHY_315	DDR PHY Register 315	0299 44ECh
44F0h	DDRSS_PHY_316	DDR PHY Register 316	0299 44F0h
44F4h	DDRSS_PHY_317	DDR PHY Register 317	0299 44F4h
44F8h	DDRSS_PHY_318	DDR PHY Register 318	0299 44F8h
44FCh	DDRSS_PHY_319	DDR PHY Register 319	0299 44FCh
4500h	DDRSS_PHY_320	DDR PHY Register 320	0299 4500h
4504h	DDRSS_PHY_321	DDR PHY Register 321	0299 4504h
4508h	DDRSS_PHY_322	DDR PHY Register 322	0299 4508h
450Ch	DDRSS_PHY_323	DDR PHY Register 323	0299 450Ch
4510h	DDRSS_PHY_324	DDR PHY Register 324	0299 4510h
4514h	DDRSS_PHY_325	DDR PHY Register 325	0299 4514h
4518h	DDRSS_PHY_326	DDR PHY Register 326	0299 4518h
451Ch	DDRSS_PHY_327	DDR PHY Register 327	0299 451Ch
4520h	DDRSS_PHY_328	DDR PHY Register 328	0299 4520h
4524h	DDRSS_PHY_329	DDR PHY Register 329	0299 4524h
4528h	DDRSS_PHY_330	DDR PHY Register 330	0299 4528h
452Ch	DDRSS_PHY_331	DDR PHY Register 331	0299 452Ch
4530h	DDRSS_PHY_332	DDR PHY Register 332	0299 4530h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4534h	DDRSS_PHY_333	DDR PHY Register 333	0299 4534h
4538h	DDRSS_PHY_334	DDR PHY Register 334	0299 4538h
453Ch	DDRSS_PHY_335	DDR PHY Register 335	0299 453Ch
4540h	DDRSS_PHY_336	DDR PHY Register 336	0299 4540h
4544h	DDRSS_PHY_337	DDR PHY Register 337	0299 4544h
4548h	DDRSS_PHY_338	DDR PHY Register 338	0299 4548h
454Ch	DDRSS_PHY_339	DDR PHY Register 339	0299 454Ch
4550h	DDRSS_PHY_340	DDR PHY Register 340	0299 4550h
4554h	DDRSS_PHY_341	DDR PHY Register 341	0299 4554h
4558h	DDRSS_PHY_342	DDR PHY Register 342	0299 4558h
455Ch	DDRSS_PHY_343	DDR PHY Register 343	0299 455Ch
4560h	DDRSS_PHY_344	DDR PHY Register 344	0299 4560h
4564h	DDRSS_PHY_345	DDR PHY Register 345	0299 4564h
4568h	DDRSS_PHY_346	DDR PHY Register 346	0299 4568h
456Ch	DDRSS_PHY_347	DDR PHY Register 347	0299 456Ch
4570h	DDRSS_PHY_348	DDR PHY Register 348	0299 4570h
4574h	DDRSS_PHY_349	DDR PHY Register 349	0299 4574h
4578h	DDRSS_PHY_350	DDR PHY Register 350	0299 4578h
457Ch	DDRSS_PHY_351	DDR PHY Register 351	0299 457Ch
4580h	DDRSS_PHY_352	DDR PHY Register 352	0299 4580h
4584h	DDRSS_PHY_353	DDR PHY Register 353	0299 4584h
4588h	DDRSS_PHY_354	DDR PHY Register 354	0299 4588h
458Ch	DDRSS_PHY_355	DDR PHY Register 355	0299 458Ch
4590h	DDRSS_PHY_356	DDR PHY Register 356	0299 4590h
4594h	DDRSS_PHY_357	DDR PHY Register 357	0299 4594h
4598h	DDRSS_PHY_358	DDR PHY Register 358	0299 4598h
459Ch	DDRSS_PHY_359	DDR PHY Register 359	0299 459Ch
45A0h	DDRSS_PHY_360	DDR PHY Register 360	0299 45A0h
45A4h	DDRSS_PHY_361	DDR PHY Register 361	0299 45A4h
45A8h	DDRSS_PHY_362	DDR PHY Register 362	0299 45A8h
45ACh	DDRSS_PHY_363	DDR PHY Register 363	0299 45ACh
45B0h	DDRSS_PHY_364	DDR PHY Register 364	0299 45B0h
45B4h	DDRSS_PHY_365	DDR PHY Register 365	0299 45B4h
45B8h	DDRSS_PHY_366	DDR PHY Register 366	0299 45B8h
45BCh	DDRSS_PHY_367	DDR PHY Register 367	0299 45BCh
45C0h	DDRSS_PHY_368	DDR PHY Register 368	0299 45C0h
45C4h	DDRSS_PHY_369	DDR PHY Register 369	0299 45C4h
45C8h	DDRSS_PHY_370	DDR PHY Register 370	0299 45C8h
45CCh	DDRSS_PHY_371	DDR PHY Register 371	0299 45CCh
45D0h	DDRSS_PHY_372	DDR PHY Register 372	0299 45D0h
45D4h	DDRSS_PHY_373	DDR PHY Register 373	0299 45D4h
45D8h	DDRSS_PHY_374	DDR PHY Register 374	0299 45D8h
45DCh	DDRSS_PHY_375	DDR PHY Register 375	0299 45DCh
45E0h	DDRSS_PHY_376	DDR PHY Register 376	0299 45E0h
45E4h	DDRSS_PHY_377	DDR PHY Register 377	0299 45E4h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
45E8h	DDRSS_PHY_378	DDR PHY Register 378	0299 45E8h
45ECh	DDRSS_PHY_379	DDR PHY Register 379	0299 45ECh
45F0h	DDRSS_PHY_380	DDR PHY Register 380	0299 45F0h
45F4h	DDRSS_PHY_381	DDR PHY Register 381	0299 45F4h
45F8h	DDRSS_PHY_382	DDR PHY Register 382	0299 45F8h
45FCh	DDRSS_PHY_383	DDR PHY Register 383	0299 45FCh
4600h	DDRSS_PHY_384	DDR PHY Register 384	0299 4600h
4604h	DDRSS_PHY_385	DDR PHY Register 385	0299 4604h
4608h	DDRSS_PHY_386	DDR PHY Register 386	0299 4608h
460Ch	DDRSS_PHY_387	DDR PHY Register 387	0299 460Ch
4610h	DDRSS_PHY_388	DDR PHY Register 388	0299 4610h
4614h	DDRSS_PHY_389	DDR PHY Register 389	0299 4614h
4618h	DDRSS_PHY_390	DDR PHY Register 390	0299 4618h
461Ch	DDRSS_PHY_391	DDR PHY Register 391	0299 461Ch
4620h	DDRSS_PHY_392	DDR PHY Register 392	0299 4620h
4624h	DDRSS_PHY_393	DDR PHY Register 393	0299 4624h
4628h	DDRSS_PHY_394	DDR PHY Register 394	0299 4628h
462Ch	DDRSS_PHY_395	DDR PHY Register 395	0299 462Ch
4800h	DDRSS_PHY_512	DDR PHY Register 512	0299 4800h
4804h	DDRSS_PHY_513	DDR PHY Register 513	0299 4804h
4808h	DDRSS_PHY_514	DDR PHY Register 514	0299 4808h
480Ch	DDRSS_PHY_515	DDR PHY Register 515	0299 480Ch
4810h	DDRSS_PHY_516	DDR PHY Register 516	0299 4810h
4814h	DDRSS_PHY_517	DDR PHY Register 517	0299 4814h
4818h	DDRSS_PHY_518	DDR PHY Register 518	0299 4818h
481Ch	DDRSS_PHY_519	DDR PHY Register 519	0299 481Ch
4820h	DDRSS_PHY_520	DDR PHY Register 520	0299 4820h
4824h	DDRSS_PHY_521	DDR PHY Register 521	0299 4824h
4828h	DDRSS_PHY_522	DDR PHY Register 522	0299 4828h
482Ch	DDRSS_PHY_523	DDR PHY Register 523	0299 482Ch
4830h	DDRSS_PHY_524	DDR PHY Register 524	0299 4830h
4834h	DDRSS_PHY_525	DDR PHY Register 525	0299 4834h
4838h	DDRSS_PHY_526	DDR PHY Register 526	0299 4838h
483Ch	DDRSS_PHY_527	DDR PHY Register 527	0299 483Ch
4840h	DDRSS_PHY_528	DDR PHY Register 528	0299 4840h
4844h	DDRSS_PHY_529	DDR PHY Register 529	0299 4844h
4848h	DDRSS_PHY_530	DDR PHY Register 530	0299 4848h
484Ch	DDRSS_PHY_531	DDR PHY Register 531	0299 484Ch
4850h	DDRSS_PHY_532	DDR PHY Register 532	0299 4850h
4854h	DDRSS_PHY_533	DDR PHY Register 533	0299 4854h
4858h	DDRSS_PHY_534	DDR PHY Register 534	0299 4858h
485Ch	DDRSS_PHY_535	DDR PHY Register 535	0299 485Ch
4860h	DDRSS_PHY_536	DDR PHY Register 536	0299 4860h
4864h	DDRSS_PHY_537	DDR PHY Register 537	0299 4864h
4868h	DDRSS_PHY_538	DDR PHY Register 538	0299 4868h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
486Ch	DDRSS_PHY_539	DDR PHY Register 539	0299 486Ch
4870h	DDRSS_PHY_540	DDR PHY Register 540	0299 4870h
4874h	DDRSS_PHY_541	DDR PHY Register 541	0299 4874h
4878h	DDRSS_PHY_542	DDR PHY Register 542	0299 4878h
487Ch	DDRSS_PHY_543	DDR PHY Register 543	0299 487Ch
4880h	DDRSS_PHY_544	DDR PHY Register 544	0299 4880h
4884h	DDRSS_PHY_545	DDR PHY Register 545	0299 4884h
4888h	DDRSS_PHY_546	DDR PHY Register 546	0299 4888h
488Ch	DDRSS_PHY_547	DDR PHY Register 547	0299 488Ch
4890h	DDRSS_PHY_548	DDR PHY Register 548	0299 4890h
4894h	DDRSS_PHY_549	DDR PHY Register 549	0299 4894h
4898h	DDRSS_PHY_550	DDR PHY Register 550	0299 4898h
489Ch	DDRSS_PHY_551	DDR PHY Register 551	0299 489Ch
48A0h	DDRSS_PHY_552	DDR PHY Register 552	0299 48A0h
48A4h	DDRSS_PHY_553	DDR PHY Register 553	0299 48A4h
48A8h	DDRSS_PHY_554	DDR PHY Register 554	0299 48A8h
48ACh	DDRSS_PHY_555	DDR PHY Register 555	0299 48ACh
48B0h	DDRSS_PHY_556	DDR PHY Register 556	0299 48B0h
48B4h	DDRSS_PHY_557	DDR PHY Register 557	0299 48B4h
48B8h	DDRSS_PHY_558	DDR PHY Register 558	0299 48B8h
48BCh	DDRSS_PHY_559	DDR PHY Register 559	0299 48BCh
48C0h	DDRSS_PHY_560	DDR PHY Register 560	0299 48C0h
48C4h	DDRSS_PHY_561	DDR PHY Register 561	0299 48C4h
48C8h	DDRSS_PHY_562	DDR PHY Register 562	0299 48C8h
48CCh	DDRSS_PHY_563	DDR PHY Register 563	0299 48CCh
48D0h	DDRSS_PHY_564	DDR PHY Register 564	0299 48D0h
48D4h	DDRSS_PHY_565	DDR PHY Register 565	0299 48D4h
48D8h	DDRSS_PHY_566	DDR PHY Register 566	0299 48D8h
48DCh	DDRSS_PHY_567	DDR PHY Register 567	0299 48DCh
48E0h	DDRSS_PHY_568	DDR PHY Register 568	0299 48E0h
48E4h	DDRSS_PHY_569	DDR PHY Register 569	0299 48E4h
48E8h	DDRSS_PHY_570	DDR PHY Register 570	0299 48E8h
48ECh	DDRSS_PHY_571	DDR PHY Register 571	0299 48ECh
48F0h	DDRSS_PHY_572	DDR PHY Register 572	0299 48F0h
48F4h	DDRSS_PHY_573	DDR PHY Register 573	0299 48F4h
48F8h	DDRSS_PHY_574	DDR PHY Register 574	0299 48F8h
48FCh	DDRSS_PHY_575	DDR PHY Register 575	0299 48FCh
4900h	DDRSS_PHY_576	DDR PHY Register 576	0299 4900h
4904h	DDRSS_PHY_577	DDR PHY Register 577	0299 4904h
4908h	DDRSS_PHY_578	DDR PHY Register 578	0299 4908h
490Ch	DDRSS_PHY_579	DDR PHY Register 579	0299 490Ch
4910h	DDRSS_PHY_580	DDR PHY Register 580	0299 4910h
4914h	DDRSS_PHY_581	DDR PHY Register 581	0299 4914h
4918h	DDRSS_PHY_582	DDR PHY Register 582	0299 4918h
491Ch	DDRSS_PHY_583	DDR PHY Register 583	0299 491Ch

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4920h	DDRSS_PHY_584	DDR PHY Register 584	0299 4920h
4924h	DDRSS_PHY_585	DDR PHY Register 585	0299 4924h
4928h	DDRSS_PHY_586	DDR PHY Register 586	0299 4928h
492Ch	DDRSS_PHY_587	DDR PHY Register 587	0299 492Ch
4930h	DDRSS_PHY_588	DDR PHY Register 588	0299 4930h
4934h	DDRSS_PHY_589	DDR PHY Register 589	0299 4934h
4938h	DDRSS_PHY_590	DDR PHY Register 590	0299 4938h
493Ch	DDRSS_PHY_591	DDR PHY Register 591	0299 493Ch
4940h	DDRSS_PHY_592	DDR PHY Register 592	0299 4940h
4944h	DDRSS_PHY_593	DDR PHY Register 593	0299 4944h
4948h	DDRSS_PHY_594	DDR PHY Register 594	0299 4948h
494Ch	DDRSS_PHY_595	DDR PHY Register 595	0299 494Ch
4950h	DDRSS_PHY_596	DDR PHY Register 596	0299 4950h
4954h	DDRSS_PHY_597	DDR PHY Register 597	0299 4954h
4958h	DDRSS_PHY_598	DDR PHY Register 598	0299 4958h
495Ch	DDRSS_PHY_599	DDR PHY Register 599	0299 495Ch
4960h	DDRSS_PHY_600	DDR PHY Register 600	0299 4960h
4964h	DDRSS_PHY_601	DDR PHY Register 601	0299 4964h
4968h	DDRSS_PHY_602	DDR PHY Register 602	0299 4968h
496Ch	DDRSS_PHY_603	DDR PHY Register 603	0299 496Ch
4970h	DDRSS_PHY_604	DDR PHY Register 604	0299 4970h
4974h	DDRSS_PHY_605	DDR PHY Register 605	0299 4974h
4978h	DDRSS_PHY_606	DDR PHY Register 606	0299 4978h
497Ch	DDRSS_PHY_607	DDR PHY Register 607	0299 497Ch
4980h	DDRSS_PHY_608	DDR PHY Register 608	0299 4980h
4984h	DDRSS_PHY_609	DDR PHY Register 609	0299 4984h
4988h	DDRSS_PHY_610	DDR PHY Register 610	0299 4988h
498Ch	DDRSS_PHY_611	DDR PHY Register 611	0299 498Ch
4990h	DDRSS_PHY_612	DDR PHY Register 612	0299 4990h
4994h	DDRSS_PHY_613	DDR PHY Register 613	0299 4994h
4998h	DDRSS_PHY_614	DDR PHY Register 614	0299 4998h
499Ch	DDRSS_PHY_615	DDR PHY Register 615	0299 499Ch
49A0h	DDRSS_PHY_616	DDR PHY Register 616	0299 49A0h
49A4h	DDRSS_PHY_617	DDR PHY Register 617	0299 49A4h
49A8h	DDRSS_PHY_618	DDR PHY Register 618	0299 49A8h
49ACh	DDRSS_PHY_619	DDR PHY Register 619	0299 49ACh
49B0h	DDRSS_PHY_620	DDR PHY Register 620	0299 49B0h
49B4h	DDRSS_PHY_621	DDR PHY Register 621	0299 49B4h
49B8h	DDRSS_PHY_622	DDR PHY Register 622	0299 49B8h
49BCh	DDRSS_PHY_623	DDR PHY Register 623	0299 49BCh
49C0h	DDRSS_PHY_624	DDR PHY Register 624	0299 49C0h
49C4h	DDRSS_PHY_625	DDR PHY Register 625	0299 49C4h
49C8h	DDRSS_PHY_626	DDR PHY Register 626	0299 49C8h
49CCh	DDRSS_PHY_627	DDR PHY Register 627	0299 49CCh
49D0h	DDRSS_PHY_628	DDR PHY Register 628	0299 49D0h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
49D4h	DDRSS_PHY_629	DDR PHY Register 629	0299 49D4h
49D8h	DDRSS_PHY_630	DDR PHY Register 630	0299 49D8h
49DCh	DDRSS_PHY_631	DDR PHY Register 631	0299 49DCh
49E0h	DDRSS_PHY_632	DDR PHY Register 632	0299 49E0h
49E4h	DDRSS_PHY_633	DDR PHY Register 633	0299 49E4h
49E8h	DDRSS_PHY_634	DDR PHY Register 634	0299 49E8h
49ECh	DDRSS_PHY_635	DDR PHY Register 635	0299 49ECh
49F0h	DDRSS_PHY_636	DDR PHY Register 636	0299 49F0h
49F4h	DDRSS_PHY_637	DDR PHY Register 637	0299 49F4h
49F8h	DDRSS_PHY_638	DDR PHY Register 638	0299 49F8h
49FCh	DDRSS_PHY_639	DDR PHY Register 639	0299 49FCh
4A00h	DDRSS_PHY_640	DDR PHY Register 640	0299 4A00h
4A04h	DDRSS_PHY_641	DDR PHY Register 641	0299 4A04h
4A08h	DDRSS_PHY_642	DDR PHY Register 642	0299 4A08h
4A0Ch	DDRSS_PHY_643	DDR PHY Register 643	0299 4A0Ch
4A10h	DDRSS_PHY_644	DDR PHY Register 644	0299 4A10h
4A14h	DDRSS_PHY_645	DDR PHY Register 645	0299 4A14h
4A18h	DDRSS_PHY_646	DDR PHY Register 646	0299 4A18h
4A1Ch	DDRSS_PHY_647	DDR PHY Register 647	0299 4A1Ch
4A20h	DDRSS_PHY_648	DDR PHY Register 648	0299 4A20h
4A24h	DDRSS_PHY_649	DDR PHY Register 649	0299 4A24h
4A28h	DDRSS_PHY_650	DDR PHY Register 650	0299 4A28h
4A2Ch	DDRSS_PHY_651	DDR PHY Register 651	0299 4A2Ch
4C00h	DDRSS_PHY_768	DDR PHY Register 768	0299 4C00h
4C04h	DDRSS_PHY_769	DDR PHY Register 769	0299 4C04h
4C08h	DDRSS_PHY_770	DDR PHY Register 770	0299 4C08h
4C0Ch	DDRSS_PHY_771	DDR PHY Register 771	0299 4C0Ch
4C10h	DDRSS_PHY_772	DDR PHY Register 772	0299 4C10h
4C14h	DDRSS_PHY_773	DDR PHY Register 773	0299 4C14h
4C18h	DDRSS_PHY_774	DDR PHY Register 774	0299 4C18h
4C1Ch	DDRSS_PHY_775	DDR PHY Register 775	0299 4C1Ch
4C20h	DDRSS_PHY_776	DDR PHY Register 776	0299 4C20h
4C24h	DDRSS_PHY_777	DDR PHY Register 777	0299 4C24h
4C28h	DDRSS_PHY_778	DDR PHY Register 778	0299 4C28h
4C2Ch	DDRSS_PHY_779	DDR PHY Register 779	0299 4C2Ch
4C30h	DDRSS_PHY_780	DDR PHY Register 780	0299 4C30h
4C34h	DDRSS_PHY_781	DDR PHY Register 781	0299 4C34h
4C38h	DDRSS_PHY_782	DDR PHY Register 782	0299 4C38h
4C3Ch	DDRSS_PHY_783	DDR PHY Register 783	0299 4C3Ch
4C40h	DDRSS_PHY_784	DDR PHY Register 784	0299 4C40h
4C44h	DDRSS_PHY_785	DDR PHY Register 785	0299 4C44h
4C48h	DDRSS_PHY_786	DDR PHY Register 786	0299 4C48h
4C4Ch	DDRSS_PHY_787	DDR PHY Register 787	0299 4C4Ch
4C50h	DDRSS_PHY_788	DDR PHY Register 788	0299 4C50h
4C54h	DDRSS_PHY_789	DDR PHY Register 789	0299 4C54h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4C58h	DDRSS_PHY_790	DDR PHY Register 790	0299 4C58h
4C5Ch	DDRSS_PHY_791	DDR PHY Register 791	0299 4C5Ch
4C60h	DDRSS_PHY_792	DDR PHY Register 792	0299 4C60h
4C64h	DDRSS_PHY_793	DDR PHY Register 793	0299 4C64h
4C68h	DDRSS_PHY_794	DDR PHY Register 794	0299 4C68h
4C6Ch	DDRSS_PHY_795	DDR PHY Register 795	0299 4C6Ch
4C70h	DDRSS_PHY_796	DDR PHY Register 796	0299 4C70h
4C74h	DDRSS_PHY_797	DDR PHY Register 797	0299 4C74h
4C78h	DDRSS_PHY_798	DDR PHY Register 798	0299 4C78h
4C7Ch	DDRSS_PHY_799	DDR PHY Register 799	0299 4C7Ch
4C80h	DDRSS_PHY_800	DDR PHY Register 800	0299 4C80h
4C84h	DDRSS_PHY_801	DDR PHY Register 801	0299 4C84h
4C88h	DDRSS_PHY_802	DDR PHY Register 802	0299 4C88h
4C8Ch	DDRSS_PHY_803	DDR PHY Register 803	0299 4C8Ch
4C90h	DDRSS_PHY_804	DDR PHY Register 804	0299 4C90h
4C94h	DDRSS_PHY_805	DDR PHY Register 805	0299 4C94h
4C98h	DDRSS_PHY_806	DDR PHY Register 806	0299 4C98h
4C9Ch	DDRSS_PHY_807	DDR PHY Register 807	0299 4C9Ch
4CA0h	DDRSS_PHY_808	DDR PHY Register 808	0299 4CA0h
4CA4h	DDRSS_PHY_809	DDR PHY Register 809	0299 4CA4h
4CA8h	DDRSS_PHY_810	DDR PHY Register 810	0299 4CA8h
4CACH	DDRSS_PHY_811	DDR PHY Register 811	0299 4CACH
4CB0h	DDRSS_PHY_812	DDR PHY Register 812	0299 4CB0h
4CB4h	DDRSS_PHY_813	DDR PHY Register 813	0299 4CB4h
4CB8h	DDRSS_PHY_814	DDR PHY Register 814	0299 4CB8h
4CBCh	DDRSS_PHY_815	DDR PHY Register 815	0299 4CBCh
4CC0h	DDRSS_PHY_816	DDR PHY Register 816	0299 4CC0h
4CC4h	DDRSS_PHY_817	DDR PHY Register 817	0299 4CC4h
4CC8h	DDRSS_PHY_818	DDR PHY Register 818	0299 4CC8h
4CCCh	DDRSS_PHY_819	DDR PHY Register 819	0299 4CCCh
4CD0h	DDRSS_PHY_820	DDR PHY Register 820	0299 4CD0h
4CD4h	DDRSS_PHY_821	DDR PHY Register 821	0299 4CD4h
4CD8h	DDRSS_PHY_822	DDR PHY Register 822	0299 4CD8h
4CDCh	DDRSS_PHY_823	DDR PHY Register 823	0299 4CDCh
4CE0h	DDRSS_PHY_824	DDR PHY Register 824	0299 4CE0h
4CE4h	DDRSS_PHY_825	DDR PHY Register 825	0299 4CE4h
4CE8h	DDRSS_PHY_826	DDR PHY Register 826	0299 4CE8h
4CECh	DDRSS_PHY_827	DDR PHY Register 827	0299 4CECh
4CF0h	DDRSS_PHY_828	DDR PHY Register 828	0299 4CF0h
4CF4h	DDRSS_PHY_829	DDR PHY Register 829	0299 4CF4h
4CF8h	DDRSS_PHY_830	DDR PHY Register 830	0299 4CF8h
4CFCh	DDRSS_PHY_831	DDR PHY Register 831	0299 4CFCh
4D00h	DDRSS_PHY_832	DDR PHY Register 832	0299 4D00h
4D04h	DDRSS_PHY_833	DDR PHY Register 833	0299 4D04h
4D08h	DDRSS_PHY_834	DDR PHY Register 834	0299 4D08h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4D0Ch	DDRSS_PHY_835	DDR PHY Register 835	0299 4D0Ch
4D10h	DDRSS_PHY_836	DDR PHY Register 836	0299 4D10h
4D14h	DDRSS_PHY_837	DDR PHY Register 837	0299 4D14h
4D18h	DDRSS_PHY_838	DDR PHY Register 838	0299 4D18h
4D1Ch	DDRSS_PHY_839	DDR PHY Register 839	0299 4D1Ch
4D20h	DDRSS_PHY_840	DDR PHY Register 840	0299 4D20h
4D24h	DDRSS_PHY_841	DDR PHY Register 841	0299 4D24h
4D28h	DDRSS_PHY_842	DDR PHY Register 842	0299 4D28h
4D2Ch	DDRSS_PHY_843	DDR PHY Register 843	0299 4D2Ch
4D30h	DDRSS_PHY_844	DDR PHY Register 844	0299 4D30h
4D34h	DDRSS_PHY_845	DDR PHY Register 845	0299 4D34h
4D38h	DDRSS_PHY_846	DDR PHY Register 846	0299 4D38h
4D3Ch	DDRSS_PHY_847	DDR PHY Register 847	0299 4D3Ch
4D40h	DDRSS_PHY_848	DDR PHY Register 848	0299 4D40h
4D44h	DDRSS_PHY_849	DDR PHY Register 849	0299 4D44h
4D48h	DDRSS_PHY_850	DDR PHY Register 850	0299 4D48h
4D4Ch	DDRSS_PHY_851	DDR PHY Register 851	0299 4D4Ch
4D50h	DDRSS_PHY_852	DDR PHY Register 852	0299 4D50h
4D54h	DDRSS_PHY_853	DDR PHY Register 853	0299 4D54h
4D58h	DDRSS_PHY_854	DDR PHY Register 854	0299 4D58h
4D5Ch	DDRSS_PHY_855	DDR PHY Register 855	0299 4D5Ch
4D60h	DDRSS_PHY_856	DDR PHY Register 856	0299 4D60h
4D64h	DDRSS_PHY_857	DDR PHY Register 857	0299 4D64h
4D68h	DDRSS_PHY_858	DDR PHY Register 858	0299 4D68h
4D6Ch	DDRSS_PHY_859	DDR PHY Register 859	0299 4D6Ch
4D70h	DDRSS_PHY_860	DDR PHY Register 860	0299 4D70h
4D74h	DDRSS_PHY_861	DDR PHY Register 861	0299 4D74h
4D78h	DDRSS_PHY_862	DDR PHY Register 862	0299 4D78h
4D7Ch	DDRSS_PHY_863	DDR PHY Register 863	0299 4D7Ch
4D80h	DDRSS_PHY_864	DDR PHY Register 864	0299 4D80h
4D84h	DDRSS_PHY_865	DDR PHY Register 865	0299 4D84h
4D88h	DDRSS_PHY_866	DDR PHY Register 866	0299 4D88h
4D8Ch	DDRSS_PHY_867	DDR PHY Register 867	0299 4D8Ch
4D90h	DDRSS_PHY_868	DDR PHY Register 868	0299 4D90h
4D94h	DDRSS_PHY_869	DDR PHY Register 869	0299 4D94h
4D98h	DDRSS_PHY_870	DDR PHY Register 870	0299 4D98h
4D9Ch	DDRSS_PHY_871	DDR PHY Register 871	0299 4D9Ch
4DA0h	DDRSS_PHY_872	DDR PHY Register 872	0299 4DA0h
4DA4h	DDRSS_PHY_873	DDR PHY Register 873	0299 4DA4h
4DA8h	DDRSS_PHY_874	DDR PHY Register 874	0299 4DA8h
4DACH	DDRSS_PHY_875	DDR PHY Register 875	0299 4DACH
4DB0h	DDRSS_PHY_876	DDR PHY Register 876	0299 4DB0h
4DB4h	DDRSS_PHY_877	DDR PHY Register 877	0299 4DB4h
4DB8h	DDRSS_PHY_878	DDR PHY Register 878	0299 4DB8h
4DBCh	DDRSS_PHY_879	DDR PHY Register 879	0299 4DBCh

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
4DC0h	DDRSS_PHY_880	DDR PHY Register 880	0299 4DC0h
4DC4h	DDRSS_PHY_881	DDR PHY Register 881	0299 4DC4h
4DC8h	DDRSS_PHY_882	DDR PHY Register 882	0299 4DC8h
4DCCh	DDRSS_PHY_883	DDR PHY Register 883	0299 4DCCh
4DD0h	DDRSS_PHY_884	DDR PHY Register 884	0299 4DD0h
4DD4h	DDRSS_PHY_885	DDR PHY Register 885	0299 4DD4h
4DD8h	DDRSS_PHY_886	DDR PHY Register 886	0299 4DD8h
4DDCh	DDRSS_PHY_887	DDR PHY Register 887	0299 4DDCh
4DE0h	DDRSS_PHY_888	DDR PHY Register 888	0299 4DE0h
4DE4h	DDRSS_PHY_889	DDR PHY Register 889	0299 4DE4h
4DE8h	DDRSS_PHY_890	DDR PHY Register 890	0299 4DE8h
4DECh	DDRSS_PHY_891	DDR PHY Register 891	0299 4DECh
4DF0h	DDRSS_PHY_892	DDR PHY Register 892	0299 4DF0h
4DF4h	DDRSS_PHY_893	DDR PHY Register 893	0299 4DF4h
4DF8h	DDRSS_PHY_894	DDR PHY Register 894	0299 4DF8h
4DFCh	DDRSS_PHY_895	DDR PHY Register 895	0299 4DFCh
4E00h	DDRSS_PHY_896	DDR PHY Register 896	0299 4E00h
4E04h	DDRSS_PHY_897	DDR PHY Register 897	0299 4E04h
4E08h	DDRSS_PHY_898	DDR PHY Register 898	0299 4E08h
4E0Ch	DDRSS_PHY_899	DDR PHY Register 899	0299 4E0Ch
4E10h	DDRSS_PHY_900	DDR PHY Register 900	0299 4E10h
4E14h	DDRSS_PHY_901	DDR PHY Register 901	0299 4E14h
4E18h	DDRSS_PHY_902	DDR PHY Register 902	0299 4E18h
4E1Ch	DDRSS_PHY_903	DDR PHY Register 903	0299 4E1Ch
4E20h	DDRSS_PHY_904	DDR PHY Register 904	0299 4E20h
4E24h	DDRSS_PHY_905	DDR PHY Register 905	0299 4E24h
4E28h	DDRSS_PHY_906	DDR PHY Register 906	0299 4E28h
4E2Ch	DDRSS_PHY_907	DDR PHY Register 907	0299 4E2Ch
5000h	DDRSS_PHY_1024	DDR PHY Register 1024	0299 5000h
5004h	DDRSS_PHY_1025	DDR PHY Register 1025	0299 5004h
5008h	DDRSS_PHY_1026	DDR PHY Register 1026	0299 5008h
500Ch	DDRSS_PHY_1027	DDR PHY Register 1027	0299 500Ch
5010h	DDRSS_PHY_1028	DDR PHY Register 1028	0299 5010h
5014h	DDRSS_PHY_1029	DDR PHY Register 1029	0299 5014h
5018h	DDRSS_PHY_1030	DDR PHY Register 1030	0299 5018h
501Ch	DDRSS_PHY_1031	DDR PHY Register 1031	0299 501Ch
5020h	DDRSS_PHY_1032	DDR PHY Register 1032	0299 5020h
5024h	DDRSS_PHY_1033	DDR PHY Register 1033	0299 5024h
5028h	DDRSS_PHY_1034	DDR PHY Register 1034	0299 5028h
502Ch	DDRSS_PHY_1035	DDR PHY Register 1035	0299 502Ch
5030h	DDRSS_PHY_1036	DDR PHY Register 1036	0299 5030h
5034h	DDRSS_PHY_1037	DDR PHY Register 1037	0299 5034h
5038h	DDRSS_PHY_1038	DDR PHY Register 1038	0299 5038h
503Ch	DDRSS_PHY_1039	DDR PHY Register 1039	0299 503Ch
5040h	DDRSS_PHY_1040	DDR PHY Register 1040	0299 5040h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
5044h	DDRSS_PHY_1041	DDR PHY Register 1041	0299 5044h
5048h	DDRSS_PHY_1042	DDR PHY Register 1042	0299 5048h
504Ch	DDRSS_PHY_1043	DDR PHY Register 1043	0299 504Ch
5050h	DDRSS_PHY_1044	DDR PHY Register 1044	0299 5050h
5054h	DDRSS_PHY_1045	DDR PHY Register 1045	0299 5054h
5058h	DDRSS_PHY_1046	DDR PHY Register 1046	0299 5058h
505Ch	DDRSS_PHY_1047	DDR PHY Register 1047	0299 505Ch
5060h	DDRSS_PHY_1048	DDR PHY Register 1048	0299 5060h
5064h	DDRSS_PHY_1049	DDR PHY Register 1049	0299 5064h
5068h	DDRSS_PHY_1050	DDR PHY Register 1050	0299 5068h
506Ch	DDRSS_PHY_1051	DDR PHY Register 1051	0299 506Ch
5070h	DDRSS_PHY_1052	DDR PHY Register 1052	0299 5070h
5074h	DDRSS_PHY_1053	DDR PHY Register 1053	0299 5074h
5078h	DDRSS_PHY_1054	DDR PHY Register 1054	0299 5078h
507Ch	DDRSS_PHY_1055	DDR PHY Register 1055	0299 507Ch
5080h	DDRSS_PHY_1056	DDR PHY Register 1056	0299 5080h
5084h	DDRSS_PHY_1057	DDR PHY Register 1057	0299 5084h
5088h	DDRSS_PHY_1058	DDR PHY Register 1058	0299 5088h
508Ch	DDRSS_PHY_1059	DDR PHY Register 1059	0299 508Ch
5090h	DDRSS_PHY_1060	DDR PHY Register 1060	0299 5090h
5094h	DDRSS_PHY_1061	DDR PHY Register 1061	0299 5094h
5098h	DDRSS_PHY_1062	DDR PHY Register 1062	0299 5098h
509Ch	DDRSS_PHY_1063	DDR PHY Register 1063	0299 509Ch
50A0h	DDRSS_PHY_1064	DDR PHY Register 1064	0299 50A0h
50A4h	DDRSS_PHY_1065	DDR PHY Register 1065	0299 50A4h
50A8h	DDRSS_PHY_1066	DDR PHY Register 1066	0299 50A8h
50ACh	DDRSS_PHY_1067	DDR PHY Register 1067	0299 50ACh
50B0h	DDRSS_PHY_1068	DDR PHY Register 1068	0299 50B0h
50B4h	DDRSS_PHY_1069	DDR PHY Register 1069	0299 50B4h
50B8h	DDRSS_PHY_1070	DDR PHY Register 1070	0299 50B8h
50BCh	DDRSS_PHY_1071	DDR PHY Register 1071	0299 50BCh
50C0h	DDRSS_PHY_1072	DDR PHY Register 1072	0299 50C0h
50C4h	DDRSS_PHY_1073	DDR PHY Register 1073	0299 50C4h
50C8h	DDRSS_PHY_1074	DDR PHY Register 1074	0299 50C8h
50CCh	DDRSS_PHY_1075	DDR PHY Register 1075	0299 50CCh
5400h	DDRSS_PHY_1280	DDR PHY Register 1280	0299 5400h
5404h	DDRSS_PHY_1281	DDR PHY Register 1281	0299 5404h
5408h	DDRSS_PHY_1282	DDR PHY Register 1282	0299 5408h
540Ch	DDRSS_PHY_1283	DDR PHY Register 1283	0299 540Ch
5410h	DDRSS_PHY_1284	DDR PHY Register 1284	0299 5410h
5414h	DDRSS_PHY_1285	DDR PHY Register 1285	0299 5414h
5418h	DDRSS_PHY_1286	DDR PHY Register 1286	0299 5418h
541Ch	DDRSS_PHY_1287	DDR PHY Register 1287	0299 541Ch
5420h	DDRSS_PHY_1288	DDR PHY Register 1288	0299 5420h
5424h	DDRSS_PHY_1289	DDR PHY Register 1289	0299 5424h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
5428h	DDRSS_PHY_1290	DDR PHY Register 1290	0299 5428h
542Ch	DDRSS_PHY_1291	DDR PHY Register 1291	0299 542Ch
5430h	DDRSS_PHY_1292	DDR PHY Register 1292	0299 5430h
5434h	DDRSS_PHY_1293	DDR PHY Register 1293	0299 5434h
5438h	DDRSS_PHY_1294	DDR PHY Register 1294	0299 5438h
543Ch	DDRSS_PHY_1295	DDR PHY Register 1295	0299 543Ch
5440h	DDRSS_PHY_1296	DDR PHY Register 1296	0299 5440h
5444h	DDRSS_PHY_1297	DDR PHY Register 1297	0299 5444h
5448h	DDRSS_PHY_1298	DDR PHY Register 1298	0299 5448h
544Ch	DDRSS_PHY_1299	DDR PHY Register 1299	0299 544Ch
5450h	DDRSS_PHY_1300	DDR PHY Register 1300	0299 5450h
5454h	DDRSS_PHY_1301	DDR PHY Register 1301	0299 5454h
5458h	DDRSS_PHY_1302	DDR PHY Register 1302	0299 5458h
545Ch	DDRSS_PHY_1303	DDR PHY Register 1303	0299 545Ch
5460h	DDRSS_PHY_1304	DDR PHY Register 1304	0299 5460h
5464h	DDRSS_PHY_1305	DDR PHY Register 1305	0299 5464h
5468h	DDRSS_PHY_1306	DDR PHY Register 1306	0299 5468h
546Ch	DDRSS_PHY_1307	DDR PHY Register 1307	0299 546Ch
5470h	DDRSS_PHY_1308	DDR PHY Register 1308	0299 5470h
5474h	DDRSS_PHY_1309	DDR PHY Register 1309	0299 5474h
5478h	DDRSS_PHY_1310	DDR PHY Register 1310	0299 5478h
547Ch	DDRSS_PHY_1311	DDR PHY Register 1311	0299 547Ch
5480h	DDRSS_PHY_1312	DDR PHY Register 1312	0299 5480h
5484h	DDRSS_PHY_1313	DDR PHY Register 1313	0299 5484h
5488h	DDRSS_PHY_1314	DDR PHY Register 1314	0299 5488h
548Ch	DDRSS_PHY_1315	DDR PHY Register 1315	0299 548Ch
5490h	DDRSS_PHY_1316	DDR PHY Register 1316	0299 5490h
5494h	DDRSS_PHY_1317	DDR PHY Register 1317	0299 5494h
5498h	DDRSS_PHY_1318	DDR PHY Register 1318	0299 5498h
549Ch	DDRSS_PHY_1319	DDR PHY Register 1319	0299 549Ch
54A0h	DDRSS_PHY_1320	DDR PHY Register 1320	0299 54A0h
54A4h	DDRSS_PHY_1321	DDR PHY Register 1321	0299 54A4h
54A8h	DDRSS_PHY_1322	DDR PHY Register 1322	0299 54A8h
54ACh	DDRSS_PHY_1323	DDR PHY Register 1323	0299 54ACh
54B0h	DDRSS_PHY_1324	DDR PHY Register 1324	0299 54B0h
54B4h	DDRSS_PHY_1325	DDR PHY Register 1325	0299 54B4h
54B8h	DDRSS_PHY_1326	DDR PHY Register 1326	0299 54B8h
54BCh	DDRSS_PHY_1327	DDR PHY Register 1327	0299 54BCh
54C0h	DDRSS_PHY_1328	DDR PHY Register 1328	0299 54C0h
54C4h	DDRSS_PHY_1329	DDR PHY Register 1329	0299 54C4h
54C8h	DDRSS_PHY_1330	DDR PHY Register 1330	0299 54C8h
54CCh	DDRSS_PHY_1331	DDR PHY Register 1331	0299 54CCh
54D0h	DDRSS_PHY_1332	DDR PHY Register 1332	0299 54D0h
54D4h	DDRSS_PHY_1333	DDR PHY Register 1333	0299 54D4h
54D8h	DDRSS_PHY_1334	DDR PHY Register 1334	0299 54D8h

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
54DCh	DDRSS_PHY_1335	DDR PHY Register 1335	0299 54DCh
54E0h	DDRSS_PHY_1336	DDR PHY Register 1336	0299 54E0h
54E4h	DDRSS_PHY_1337	DDR PHY Register 1337	0299 54E4h
54E8h	DDRSS_PHY_1338	DDR PHY Register 1338	0299 54E8h
54ECh	DDRSS_PHY_1339	DDR PHY Register 1339	0299 54ECh
54F0h	DDRSS_PHY_1340	DDR PHY Register 1340	0299 54F0h
54F4h	DDRSS_PHY_1341	DDR PHY Register 1341	0299 54F4h
54F8h	DDRSS_PHY_1342	DDR PHY Register 1342	0299 54F8h
54FCh	DDRSS_PHY_1343	DDR PHY Register 1343	0299 54FCh
5500h	DDRSS_PHY_1344	DDR PHY Register 1344	0299 5500h
5504h	DDRSS_PHY_1345	DDR PHY Register 1345	0299 5504h
5508h	DDRSS_PHY_1346	DDR PHY Register 1346	0299 5508h
550Ch	DDRSS_PHY_1347	DDR PHY Register 1347	0299 550Ch
5510h	DDRSS_PHY_1348	DDR PHY Register 1348	0299 5510h
5514h	DDRSS_PHY_1349	DDR PHY Register 1349	0299 5514h
5518h	DDRSS_PHY_1350	DDR PHY Register 1350	0299 5518h
551Ch	DDRSS_PHY_1351	DDR PHY Register 1351	0299 551Ch
5520h	DDRSS_PHY_1352	DDR PHY Register 1352	0299 5520h
5524h	DDRSS_PHY_1353	DDR PHY Register 1353	0299 5524h
5528h	DDRSS_PHY_1354	DDR PHY Register 1354	0299 5528h
552Ch	DDRSS_PHY_1355	DDR PHY Register 1355	0299 552Ch
5530h	DDRSS_PHY_1356	DDR PHY Register 1356	0299 5530h
5534h	DDRSS_PHY_1357	DDR PHY Register 1357	0299 5534h
5538h	DDRSS_PHY_1358	DDR PHY Register 1358	0299 5538h
553Ch	DDRSS_PHY_1359	DDR PHY Register 1359	0299 553Ch
5540h	DDRSS_PHY_1360	DDR PHY Register 1360	0299 5540h
5544h	DDRSS_PHY_1361	DDR PHY Register 1361	0299 5544h
5548h	DDRSS_PHY_1362	DDR PHY Register 1362	0299 5548h
554Ch	DDRSS_PHY_1363	DDR PHY Register 1363	0299 554Ch
5550h	DDRSS_PHY_1364	DDR PHY Register 1364	0299 5550h
5554h	DDRSS_PHY_1365	DDR PHY Register 1365	0299 5554h
5558h	DDRSS_PHY_1366	DDR PHY Register 1366	0299 5558h
555Ch	DDRSS_PHY_1367	DDR PHY Register 1367	0299 555Ch
5560h	DDRSS_PHY_1368	DDR PHY Register 1368	0299 5560h
5564h	DDRSS_PHY_1369	DDR PHY Register 1369	0299 5564h
5568h	DDRSS_PHY_1370	DDR PHY Register 1370	0299 5568h
556Ch	DDRSS_PHY_1371	DDR PHY Register 1371	0299 556Ch
5570h	DDRSS_PHY_1372	DDR PHY Register 1372	0299 5570h
5574h	DDRSS_PHY_1373	DDR PHY Register 1373	0299 5574h
5578h	DDRSS_PHY_1374	DDR PHY Register 1374	0299 5578h
557Ch	DDRSS_PHY_1375	DDR PHY Register 1375	0299 557Ch
5580h	DDRSS_PHY_1376	DDR PHY Register 1376	0299 5580h
5584h	DDRSS_PHY_1377	DDR PHY Register 1377	0299 5584h
5588h	DDRSS_PHY_1378	DDR PHY Register 1378	0299 5588h
558Ch	DDRSS_PHY_1379	DDR PHY Register 1379	0299 558Ch

Table 4-1596. DDR PHY Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_CT L_CFG_PHY Physical Address
5590h	DDRSS_PHY_1380	DDR PHY Register 1380	0299 5590h
5594h	DDRSS_PHY_1381	DDR PHY Register 1381	0299 5594h
5598h	DDRSS_PHY_1382	DDR PHY Register 1382	0299 5598h
559Ch	DDRSS_PHY_1383	DDR PHY Register 1383	0299 559Ch
55A0h	DDRSS_PHY_1384	DDR PHY Register 1384	0299 55A0h
55A4h	DDRSS_PHY_1385	DDR PHY Register 1385	0299 55A4h
55A8h	DDRSS_PHY_1386	DDR PHY Register 1386	0299 55A8h
55ACh	DDRSS_PHY_1387	DDR PHY Register 1387	0299 55ACh
55B0h	DDRSS_PHY_1388	DDR PHY Register 1388	0299 55B0h
55B4h	DDRSS_PHY_1389	DDR PHY Register 1389	0299 55B4h
55B8h	DDRSS_PHY_1390	DDR PHY Register 1390	0299 55B8h
55BCh	DDRSS_PHY_1391	DDR PHY Register 1391	0299 55BCh
55C0h	DDRSS_PHY_1392	DDR PHY Register 1392	0299 55C0h
55C4h	DDRSS_PHY_1393	DDR PHY Register 1393	0299 55C4h
55C8h	DDRSS_PHY_1394	DDR PHY Register 1394	0299 55C8h
55CCh	DDRSS_PHY_1395	DDR PHY Register 1395	0299 55CCh
55D0h	DDRSS_PHY_1396	DDR PHY Register 1396	0299 55D0h
55D4h	DDRSS_PHY_1397	DDR PHY Register 1397	0299 55D4h
55D8h	DDRSS_PHY_1398	DDR PHY Register 1398	0299 55D8h
55DCh	DDRSS_PHY_1399	DDR PHY Register 1399	0299 55DCh
55E0h	DDRSS_PHY_1400	DDR PHY Register 1400	0299 55E0h
55E4h	DDRSS_PHY_1401	DDR PHY Register 1401	0299 55E4h
55E8h	DDRSS_PHY_1402	DDR PHY Register 1402	0299 55E8h
55ECh	DDRSS_PHY_1403	DDR PHY Register 1403	0299 55ECh
55F0h	DDRSS_PHY_1404	DDR PHY Register 1404	0299 55F0h
55F4h	DDRSS_PHY_1405	DDR PHY Register 1405	0299 55F4h
55F8h	DDRSS_PHY_1406	DDR PHY Register 1406	0299 55F8h
55FCh	DDRSS_PHY_1407	DDR PHY Register 1407	0299 55FCh
5600h	DDRSS_PHY_1408	DDR PHY Register 1408	0299 5600h
5604h	DDRSS_PHY_1409	DDR PHY Register 1409	0299 5604h
5608h	DDRSS_PHY_1410	DDR PHY Register 1410	0299 5608h
560Ch	DDRSS_PHY_1411	DDR PHY Register 1411	0299 560Ch
5610h	DDRSS_PHY_1412	DDR PHY Register 1412	0299 5610h
5614h	DDRSS_PHY_1413	DDR PHY Register 1413	0299 5614h
5618h	DDRSS_PHY_1414	DDR PHY Register 1414	0299 5618h
561Ch	DDRSS_PHY_1415	DDR PHY Register 1415	0299 561Ch
5620h	DDRSS_PHY_1416	DDR PHY Register 1416	0299 5620h
5624h	DDRSS_PHY_1417	DDR PHY Register 1417	0299 5624h
5628h	DDRSS_PHY_1418	DDR PHY Register 1418	0299 5628h
562Ch	DDRSS_PHY_1419	DDR PHY Register 1419	0299 562Ch
5630h	DDRSS_PHY_1420	DDR PHY Register 1420	0299 5630h
5634h	DDRSS_PHY_1421	DDR PHY Register 1421	0299 5634h
5638h	DDRSS_PHY_1422	DDR PHY Register 1422	0299 5638h

4.4.1 DDRSS_PHY_0 Register (Offset = 4000h) [reset = X]

DDRSS_PHY_0 is shown in [Figure 4-795](#) and described in [Table 4-1598](#).

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Table 4-1597. DDRSS_PHY_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4000h

Figure 4-795. DDRSS_PHY_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CLK_WR_BYPASS_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1598. DDRSS_PHY_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_IO_PAD_DELAY_TIMING_BYPASS_0	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WR_BYPASS_SLAVE_DELAY_0	R/W	0h	Write data clock bypass mode slave delay setting for slice 0.} PADDING_BEFORE

4.4.2 DDRSS_PHY_1 Register (Offset = 4004h) [reset = X]

DDRSS_PHY_1 is shown in [Figure 4-796](#) and described in [Table 4-1600](#).

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Table 4-1599. DDRSS_PHY_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4004h

Figure 4-796. DDRSS_PHY_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_0		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1600. DDRSS_PHY_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_WRITE_PATH_LAT_ADD_BYPASS_0	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_0	R/W	0h	Write DQS bypass mode slave delay setting for slice 0.

4.4.3 DDRSS_PHY_2 Register (Offset = 4008h) [reset = X]

DDRSS_PHY_2 is shown in [Figure 4-797](#) and described in [Table 4-1602](#).

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Table 4-1601. DDRSS_PHY_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4008h

Figure 4-797. DDRSS_PHY_2 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_BYPASS_TWO_CYCLE_PREAMBLE_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1602. DDRSS_PHY_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CLK_BYPASS_OVERRIDE_0	R/W	0h	Bypass mode override setting for slice 0.
23-18	RESERVED	R/W	X	
17-16	PHY_BYPASS_TWO_CYCLE_PREAMBLE_0	R/W	0h	Two_cycle_preamble for bypass mode for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_0	R/W	0h	Read DQS bypass mode slave delay setting for slice 0.

4.4.4 DDRSS_PHY_3 Register (Offset = 400Ch) [reset = X]

DDRSS_PHY_3 is shown in Figure 4-798 and described in Table 4-1604.

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Table 4-1603. DDRSS_PHY_3 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 400Ch

Figure 4-798. DDRSS_PHY_3 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_0					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ2_SHIFT_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ1_SHIFT_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ0_SHIFT_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1604. DDRSS_PHY_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ3_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ2_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ1_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-1604. DDRSS_PHY_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ0_SHIF T_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.5 DDRSS_PHY_4 Register (Offset = 4010h) [reset = X]

DDRSS_PHY_4 is shown in Figure 4-799 and described in Table 4-1606.

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Table 4-1605. DDRSS_PHY_4 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4010h

Figure 4-799. DDRSS_PHY_4 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_0					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ6_SHIFT_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ5_SHIFT_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ4_SHIFT_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1606. DDRSS_PHY_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ7_SHIF T_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ6_SHIF T_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ5_SHIF T_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-1606. DDRSS_PHY_4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ4_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.6 DDRSS_PHY_5 Register (Offset = 4014h) [reset = X]

DDRSS_PHY_5 is shown in [Figure 4-800](#) and described in [Table 4-1608](#).

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Table 4-1607. DDRSS_PHY_5 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4014h

Figure 4-800. DDRSS_PHY_5 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_0
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
RESERVED						PHY_PER_RANK_CS_MAP_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_WRDQS_SHIFT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDM_SHIFT_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1608. DDRSS_PHY_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_PER_CS_TRAINING_MULTICAST_EN_0	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 0. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PHY_PER_RANK_CS_MAP_0	R/W	0h	Per-rank CS map for slice 0. Setting a bit uses that CS for the rank, bit (0) uses CS0, bit (1) uses CS1, etc.
15-12	RESERVED	R/W	X	
11-8	PHY_SW_WRDQS_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bit (3) is the cycle_shift value.
7-6	RESERVED	R/W	X	

Table 4-1608. DDRSS_PHY_5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PHY_SW_WRDM_SHIFT_0	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.7 DDRSS_PHY_6 Register (Offset = 4018h) [reset = X]

DDRSS_PHY_6 is shown in [Figure 4-801](#) and described in [Table 4-1610](#).

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Table 4-1609. DDRSS_PHY_6 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4018h

Figure 4-801. DDRSS_PHY_6 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_LP4_BOOT_RDDATA_EN_DLY_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_PER_CS_TRAINING_INDEX_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1610. DDRSS_PHY_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0.
23-21	RESERVED	R/W	X	
20-16	PHY_LP4_BOOT_RDDATA_EN_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 0.
15-10	RESERVED	R/W	X	
9-8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_INDEX_0	R/W	0h	For per-rank training, indicates which rank's parameters are read/written for slice 0.

4.4.8 DDRSS_PHY_7 Register (Offset = 401Ch) [reset = X]

DDRSS_PHY_7 is shown in Figure 4-802 and described in Table 4-1612.

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Table 4-1611. DDRSS_PHY_7 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 401Ch

Figure 4-802. DDRSS_PHY_7 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_OE_DLY_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1612. DDRSS_PHY_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 0.
23-18	RESERVED	R/W	X	
17-16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_0	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 0. Bit (0): disable pull in wrdata_en Bit (1): disable write path clock gating, clock always on
15-12	RESERVED	R/W	X	
11-8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_LP4_BOOT_RPTR_UPDATE_0	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 0.

4.4.9 DDRSS_PHY_8 Register (Offset = 4020h) [reset = X]

DDRSS_PHY_8 is shown in [Figure 4-803](#) and described in [Table 4-1614](#).

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Table 4-1613. DDRSS_PHY_8 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4020h

Figure 4-803. DDRSS_PHY_8 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_LPBK_CONTROL_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_LPBK_CONTROL_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_CTRL_LPBK_EN_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1614. DDRSS_PHY_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LPBK_DFX_TIMEOUT_EN_0	R/W	0h	Loopback read only test timeout mechanism enable for slice 0.
23-17	RESERVED	R/W	X	
16-8	PHY_LPBK_CONTROL_0	R/W	0h	Loopback control bits for slice 0.
7-2	RESERVED	R/W	X	
1-0	PHY_CTRL_LPBK_EN_0	R/W	0h	Loopback control en for slice 0.

4.4.10 DDRSS_PHY_9 Register (Offset = 4024h) [reset = 0h]

DDRSS_PHY_9 is shown in [Figure 4-804](#) and described in [Table 4-1616](#).

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Table 4-1615. DDRSS_PHY_9 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4024h

Figure 4-804. DDRSS_PHY_9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1616. DDRSS_PHY_9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_AUTO_TIMING_MARGIN_CONTROL_0	R/W	0h	Auto timing marging control bits for slice 0.

4.4.11 DDRSS_PHY_10 Register (Offset = 4028h) [reset = X]

DDRSS_PHY_10 is shown in [Figure 4-805](#) and described in [Table 4-1618](#).

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Table 4-1617. DDRSS_PHY_10 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4028h

Figure 4-805. DDRSS_PHY_10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_0																											
R-X				R-0h																											

LEGEND: R = Read Only; -n = value after reset

Table 4-1618. DDRSS_PHY_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-0	PHY_AUTO_TIMING_MARGIN_OBS_0	R	0h	Observation register for the auto_timing_margin for slice 0. READ-ONLY

4.4.12 DDRSS_PHY_11 Register (Offset = 402Ch) [reset = X]

DDRSS_PHY_11 is shown in [Figure 4-806](#) and described in [Table 4-1620](#).

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Table 4-1619. DDRSS_PHY_11 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 402Ch

Figure 4-806. DDRSS_PHY_11 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTIPATTERN_ENABLE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_PRBS_PATTERN_MASK_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_PRBS_PATTERN_MASK_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PHY_PRBS_PATTERN_START_0						
R/W-X	R/W-1h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1620. DDRSS_PHY_11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RDLVL_MULTIPATTERN_ENABLE_0	R/W	0h	Read Leveling Multi-pattern enable for slice 0.
23-17	RESERVED	R/W	X	
16-8	PHY_PRBS_PATTERN_MASK_0	R/W	0h	PRBS7 mask signal for slice 0.
7	RESERVED	R/W	X	
6-0	PHY_PRBS_PATTERN_START_0	R/W	1h	PRBS7 start pattern for slice 0.

4.4.13 DDRSS_PHY_12 Register (Offset = 4030h) [reset = X]

DDRSS_PHY_12 is shown in [Figure 4-807](#) and described in [Table 4-1622](#).

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Table 4-1621. DDRSS_PHY_12 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4030h

Figure 4-807. DDRSS_PHY_12 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PHY_VREF_TRAIN_OBS_0						
R/W-X	R-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_VREF_INITIAL_STEPSIZE_0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RDLVL_MULTIPATT_RST_DISABLE_0
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1622. DDRSS_PHY_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	PHY_VREF_TRAIN_OBS_0	R	0h	Observation register for best vref value for slice 0. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	PHY_VREF_INITIAL_STEPSIZE_0	R/W	0h	Data slice initial VREF training step size for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_RDLVL_MULTIPATT_RST_DISABLE_0	R/W	0h	Read Leveling read level windows disable reset for slice 0.

4.4.14 DDRSS_PHY_13 Register (Offset = 4034h) [reset = X]

DDRSS_PHY_13 is shown in [Figure 4-808](#) and described in [Table 4-1624](#).

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Table 4-1623. DDRSS_PHY_13 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4034h

Figure 4-808. DDRSS_PHY_13 Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_SNAP_OBS_REGS_0
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1624. DDRSS_PHY_13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SC_PHY_SNAP_OBS_REGS_0	W	0h	Initiates a snapshot of the internal observation registers for slice 0. Set to 1 to trigger. WRITE-ONLY
23-20	RESERVED	R/W	X	
19-16	PHY_GATE_ERROR_DELAY_SELECT_0	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	R/W	0h	Read DQS data clock bypass mode slave delay setting for slice 0.

4.4.15 DDRSS_PHY_14 Register (Offset = 4038h) [reset = X]

DDRSS_PHY_14 is shown in [Figure 4-809](#) and described in [Table 4-1626](#).

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Table 4-1625. DDRSS_PHY_14 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4038h

Figure 4-809. DDRSS_PHY_14 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MEM_CLASS_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							PHY_LPDDR_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1626. DDRSS_PHY_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_MEM_CLASS_0	R/W	0h	Indicates the type of DRAM for slice 0. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4
23-17	RESERVED	R/W	X	
16	PHY_LPDDR_0	R/W	0h	Adds a cycle of delay for the slice 0 to match the address slice. Set to 1 to add a cycle
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL1_SLAVE_DELAY_0	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 0.

4.4.16 DDRSS_PHY_15 Register (Offset = 403Ch) [reset = X]

DDRSS_PHY_15 is shown in [Figure 4-810](#) and described in [Table 4-1628](#).

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Table 4-1627. DDRSS_PHY_15 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 403Ch

Figure 4-810. DDRSS_PHY_15 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						ON_FLY_GATE_ADJUST_EN_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL2_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL2_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1628. DDRSS_PHY_15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	ON_FLY_GATE_ADJUST_EN_0	R/W	0h	Control the on-the-fly gate adjustment for slice 0.
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL2_SLAVE_DELAY_0	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 0.

4.4.17 DDRSS_PHY_16 Register (Offset = 4040h) [reset = 0h]

DDRSS_PHY_16 is shown in [Figure 4-811](#) and described in [Table 4-1630](#).

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Table 4-1629. DDRSS_PHY_16 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4040h

Figure 4-811. DDRSS_PHY_16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1630. DDRSS_PHY_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_GATE_TRACKING_OBS_0	R	0h	Report the on-the-fly gate measurement result for slice 0. READ-ONLY

4.4.18 DDRSS_PHY_17 Register (Offset = 4044h) [reset = X]

DDRSS_PHY_17 is shown in [Figure 4-812](#) and described in [Table 4-1632](#).

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Table 4-1631. DDRSS_PHY_17 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4044h

Figure 4-812. DDRSS_PHY_17 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1632. DDRSS_PHY_17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-8	PHY_LP4_PST_AMBLE_0	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_DFI40_POLARITY_0	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 0.

4.4.19 DDRSS_PHY_18 Register (Offset = 4048h) [reset = 0h]

DDRSS_PHY_18 is shown in [Figure 4-813](#) and described in [Table 4-1634](#).

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Table 4-1633. DDRSS_PHY_18 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4048h

Figure 4-813. DDRSS_PHY_18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1634. DDRSS_PHY_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT8_0	R/W	0h	Read leveling pattern 8 data for slice 0.

4.4.20 DDRSS_PHY_19 Register (Offset = 404Ch) [reset = 0h]

DDRSS_PHY_19 is shown in [Figure 4-814](#) and described in [Table 4-1636](#).

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Table 4-1635. DDRSS_PHY_19 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 404Ch

Figure 4-814. DDRSS_PHY_19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1636. DDRSS_PHY_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT9_0	R/W	0h	Read leveling pattern 9 data for slice 0.

4.4.21 DDRSS_PHY_20 Register (Offset = 4050h) [reset = 0h]

DDRSS_PHY_20 is shown in [Figure 4-815](#) and described in [Table 4-1638](#).

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Table 4-1637. DDRSS_PHY_20 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4050h

Figure 4-815. DDRSS_PHY_20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1638. DDRSS_PHY_20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT10_0	R/W	0h	Read leveling pattern 10 data for slice 0.

4.4.22 DDRSS_PHY_21 Register (Offset = 4054h) [reset = 0h]

DDRSS_PHY_21 is shown in [Figure 4-816](#) and described in [Table 4-1640](#).

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Table 4-1639. DDRSS_PHY_21 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4054h

Figure 4-816. DDRSS_PHY_21 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1640. DDRSS_PHY_21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT11_0	R/W	0h	Read leveling pattern 11 data for slice 0.

4.4.23 DDRSS_PHY_22 Register (Offset = 4058h) [reset = 0h]

DDRSS_PHY_22 is shown in [Figure 4-817](#) and described in [Table 4-1642](#).

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Table 4-1641. DDRSS_PHY_22 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4058h

Figure 4-817. DDRSS_PHY_22 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1642. DDRSS_PHY_22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT12_0	R/W	0h	Read leveling pattern 12 data for slice 0.

4.4.24 DDRSS_PHY_23 Register (Offset = 405Ch) [reset = 0h]

DDRSS_PHY_23 is shown in [Figure 4-818](#) and described in [Table 4-1644](#).

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Table 4-1643. DDRSS_PHY_23 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 405Ch

Figure 4-818. DDRSS_PHY_23 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1644. DDRSS_PHY_23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT13_0	R/W	0h	Read leveling pattern 13 data for slice 0.

4.4.25 DDRSS_PHY_24 Register (Offset = 4060h) [reset = 0h]

DDRSS_PHY_24 is shown in [Figure 4-819](#) and described in [Table 4-1646](#).

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Table 4-1645. DDRSS_PHY_24 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4060h

Figure 4-819. DDRSS_PHY_24 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1646. DDRSS_PHY_24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT14_0	R/W	0h	Read leveling pattern 14 data for slice 0.

4.4.26 DDRSS_PHY_25 Register (Offset = 4064h) [reset = 0h]

DDRSS_PHY_25 is shown in [Figure 4-820](#) and described in [Table 4-1648](#).

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Table 4-1647. DDRSS_PHY_25 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4064h

Figure 4-820. DDRSS_PHY_25 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1648. DDRSS_PHY_25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT15_0	R/W	0h	Read leveling pattern 15 data for slice 0.

4.4.27 DDRSS_PHY_26 Register (Offset = 4068h) [reset = X]

DDRSS_PHY_26 is shown in [Figure 4-821](#) and described in [Table 4-1650](#).

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Table 4-1649. DDRSS_PHY_26 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4068h

Figure 4-821. DDRSS_PHY_26 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_SELECT_0		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_0		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1650. DDRSS_PHY_26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_RDDQ_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ encoded slave delay observation register for slice 0.
23-20	RESERVED	R/W	X	
19-16	PHY_MASTER_DLY_LOCK_OBS_SELECT_0	R/W	0h	Select value to map the internal master delay observation registers to the accessible master delay observation register for slice 0.
15-9	RESERVED	R/W	X	
8	PHY_SW_FIFO_PTR_RST_DISABLE_0	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 0. Set to 1 to disable automatic resets.
7-3	RESERVED	R/W	X	
2-0	PHY_SLAVE_LOOP_CNT_UPDATE_0	R/W	0h	Reserved for future use for slice 0.

4.4.28 DDRSS_PHY_27 Register (Offset = 406Ch) [reset = X]

DDRSS_PHY_27 is shown in Figure 4-822 and described in Table 4-1652.

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Table 4-1651. DDRSS_PHY_27 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 406Ch

Figure 4-822. DDRSS_PHY_27 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1652. DDRSS_PHY_27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_FIFO_PTR_OBS_SELECT_0	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 0.
23-20	RESERVED	R/W	X	
19-16	PHY_WR_SHIFT_OBS_SELECT_0	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 0.
15-12	RESERVED	R/W	X	
11-8	PHY_WR_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ encoded slave delay observation register for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_DQ_ENC_OBS_SELECT_0	R/W	0h	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible read DQS DQ rise/fall encoded slave delay observation registers for slice 0.

4.4.29 DDRSS_PHY_28 Register (Offset = 4070h) [reset = X]

DDRSS_PHY_28 is shown in [Figure 4-823](#) and described in [Table 4-1654](#).

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Table 4-1653. DDRSS_PHY_28 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4070h

Figure 4-823. DDRSS_PHY_28 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_PER_START_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_ALGO_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_LVL_DEBUG_CONT_0
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LVL_DEBUG_MODE_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1654. DDRSS_PHY_28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_PER_START_0	R/W	0h	Observation register for write leveling status for slice 0. READ-ONLY
23-18	RESERVED	R/W	X	
17-16	PHY_WRLVL_ALGO_0	R/W	0h	Write leveling algorithm selection for slice 0.
15-9	RESERVED	R/W	X	
8	SC_PHY_LVL_DEBUG_CONT_0	W	0h	Allows the leveling state machine to advance (when in debug mode) for slice 0. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_LVL_DEBUG_MODE_0	R/W	0h	Enables leveling debug mode for slice 0. Set to 1 to enable.

4.4.30 DDRSS_PHY_29 Register (Offset = 4074h) [reset = X]

DDRSS_PHY_29 is shown in [Figure 4-824](#) and described in [Table 4-1656](#).

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Table 4-1655. DDRSS_PHY_29 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4074h

Figure 4-824. DDRSS_PHY_29 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_DQ_MASK_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_CAPTURE_CNT_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1656. DDRSS_PHY_29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_DQ_MASK_0	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 0.
15-12	RESERVED	R/W	X	
11-8	PHY_WRLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during write leveling for slice 0.
7-6	RESERVED	R/W	X	
5-0	PHY_WRLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS slave delay setting during write leveling for slice 0.

4.4.31 DDRSS_PHY_30 Register (Offset = 4078h) [reset = X]

DDRSS_PHY_30 is shown in [Figure 4-825](#) and described in [Table 4-1658](#).

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Table 4-1657. DDRSS_PHY_30 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4078h

Figure 4-825. DDRSS_PHY_30 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_CAPTURE_CNT_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_PER_START_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_PER_START_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1658. DDRSS_PHY_30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_GTLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles + 4 to wait after changing DQS slave delay setting during gate training for slice 0. The valid range is 0x0 to 0xB.
23-22	RESERVED	R/W	X	
21-16	PHY_GTLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS slave delay setting during gate training for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_PER_START_0	R/W	0h	Value to be added to the current gate delay position as the starting point for periodic gate training for slice 0.

4.4.32 DDRSS_PHY_31 Register (Offset = 407Ch) [reset = X]

DDRSS_PHY_31 is shown in Figure 4-826 and described in Table 4-1660.

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Table 4-1659. DDRSS_PHY_31 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 407Ch

Figure 4-826. DDRSS_PHY_31 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_RDLVL_OP_MODE_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_RDLVL_CAPTURE_CNT_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1660. DDRSS_PHY_31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 0.
23-18	RESERVED	R/W	X	
17-16	PHY_RDLVL_OP_MODE_0	R/W	0h	Read leveling algorithm select for slice 0. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right.
15-12	RESERVED	R/W	X	
11-8	PHY_RDLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during read leveling for slice 0.
7-6	RESERVED	R/W	X	
5-0	PHY_RDLVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each DQS slave delay setting during read leveling for slice 0.

4.4.33 DDRSS_PHY_32 Register (Offset = 4080h) [reset = X]

DDRSS_PHY_32 is shown in [Figure 4-827](#) and described in [Table 4-1662](#).

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Table 4-1661. DDRSS_PHY_32 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4080h

Figure 4-827. DDRSS_PHY_32 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_BURST_CNT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PHY_WDQLVL_CLK_JITTER_TOLERANCE_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_DATA_MASK_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_SELECT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1662. DDRSS_PHY_32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_WDQLVL_BURST_CNT_0	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 0.
23-16	PHY_WDQLVL_CLK_JITTER_TOLERANCE_0	R/W	0h	Defines the minimum gap requirement for the LE and TE window for slice 0.
15-8	PHY_RDLVL_DATA_MASK_0	R/W	0h	Per-bit mask for read leveling for slice 0. If all bits are not used, only 1 bit should be cleared to 0.
7-0	PHY_RDLVL_PERIODIC_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during periodic read leveling for slice 0.

4.4.34 DDRSS_PHY_33 Register (Offset = 4084h) [reset = X]

DDRSS_PHY_33 is shown in [Figure 4-828](#) and described in [Table 4-1664](#).

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Table 4-1663. DDRSS_PHY_33 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4084h

Figure 4-828. DDRSS_PHY_33 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_PATT_0		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1664. DDRSS_PHY_33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_WDQLVL_UPDT_WAIT_CNT_0	R/W	0h	Number of cycles to wait after changing the DQ slave delay setting during write data leveling for slice 0.
23-19	RESERVED	R/W	X	
18-8	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 0.
7-3	RESERVED	R/W	X	
2-0	PHY_WDQLVL_PATT_0	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 0. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen.

4.4.35 DDRSS_PHY_34 Register (Offset = 4088h) [reset = X]

DDRSS_PHY_34 is shown in [Figure 4-829](#) and described in [Table 4-1666](#).

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Table 4-1665. DDRSS_PHY_34 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4088h

Figure 4-829. DDRSS_PHY_34 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_WDQ LVL_CLR_PRE V_RESULTS_0
R/W-X							W-0h
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_SELECT_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1666. DDRSS_PHY_34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	SC_PHY_WDQLVL_CLR_PREV_RESULTS_0	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 0. Set to 1 to trigger. WRITE-ONLY
15-8	PHY_WDQLVL_PERIODIC_OBS_SELECT_0	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_WDQLVL_DQDM_OBS_SELECT_0	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 0.

4.4.36 DDRSS_PHY_35 Register (Offset = 408Ch) [reset = X]

DDRSS_PHY_35 is shown in [Figure 4-830](#) and described in [Table 4-1668](#).

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Table 4-1667. DDRSS_PHY_35 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 408Ch

Figure 4-830. DDRSS_PHY_35 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_WDQLVL_DATADM_MASK_0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1668. DDRSS_PHY_35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_WDQLVL_DATADM_MASK_0	R/W	0h	Per-bit mask for write data leveling for slice 0. Set to 1 to mask any bit from the leveling process.

4.4.37 DDRSS_PHY_36 Register (Offset = 4090h) [reset = 0h]

DDRSS_PHY_36 is shown in [Figure 4-831](#) and described in [Table 4-1670](#).

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Table 4-1669. DDRSS_PHY_36 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4090h

Figure 4-831. DDRSS_PHY_36 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT0_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1670. DDRSS_PHY_36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT0_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 3 to 0 written/read from device.

4.4.38 DDRSS_PHY_37 Register (Offset = 4094h) [reset = 0h]

DDRSS_PHY_37 is shown in [Figure 4-832](#) and described in [Table 4-1672](#).

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Table 4-1671. DDRSS_PHY_37 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4094h

Figure 4-832. DDRSS_PHY_37 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT1_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1672. DDRSS_PHY_37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT1_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 7 to 4 written/read from device.

4.4.39 DDRSS_PHY_38 Register (Offset = 4098h) [reset = 0h]

DDRSS_PHY_38 is shown in [Figure 4-833](#) and described in [Table 4-1674](#).

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Table 4-1673. DDRSS_PHY_38 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4098h

Figure 4-833. DDRSS_PHY_38 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT2_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1674. DDRSS_PHY_38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT2_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 11 to 8 written/read from device.

4.4.40 DDRSS_PHY_39 Register (Offset = 409Ch) [reset = 0h]

DDRSS_PHY_39 is shown in [Figure 4-834](#) and described in [Table 4-1676](#).

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Table 4-1675. DDRSS_PHY_39 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 409Ch

Figure 4-834. DDRSS_PHY_39 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT3_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1676. DDRSS_PHY_39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT3_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 15 to 12 written/read from device.

4.4.41 DDRSS_PHY_40 Register (Offset = 40A0h) [reset = X]

DDRSS_PHY_40 is shown in [Figure 4-835](#) and described in [Table 4-1678](#).

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Table 4-1677. DDRSS_PHY_40 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40A0h

Figure 4-835. DDRSS_PHY_40 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_MULT_TRAIN_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_USER_PATT4_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT4_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1678. DDRSS_PHY_40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_NTP_MULT_TRAIN_0	R/W	0h	Control for single pass only No-Topology training for slice 0.
15-0	PHY_USER_PATT4_0	R/W	0h	User-defined pattern to be used during write data leveling for slice 0. This register holds the DM bit for the 15 to 0 DQ written/read from device.

4.4.42 DDRSS_PHY_41 Register (Offset = 40A4h) [reset = X]

DDRSS_PHY_41 is shown in [Figure 4-836](#) and described in [Table 4-1680](#).

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Table 4-1679. DDRSS_PHY_41 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40A4h

Figure 4-836. DDRSS_PHY_41 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_EARLY_THRESHOLD_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1680. DDRSS_PHY_41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_0	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_EARLY_THRESHOLD_0	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 0.

4.4.43 DDRSS_PHY_42 Register (Offset = 40A8h) [reset = X]

DDRSS_PHY_42 is shown in [Figure 4-837](#) and described in [Table 4-1682](#).

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Table 4-1681. DDRSS_PHY_42 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40A8h

Figure 4-837. DDRSS_PHY_42 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1682. DDRSS_PHY_42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_MAX_0	R/W	0h	Maximum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_PERIOD_THRESHOLD_MIN_0	R/W	0h	Minimum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 0.

4.4.44 DDRSS_PHY_43 Register (Offset = 40ACh) [reset = X]

DDRSS_PHY_43 is shown in [Figure 4-838](#) and described in [Table 4-1684](#).

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Table 4-1683. DDRSS_PHY_43 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40ACh

Figure 4-838. DDRSS_PHY_43 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_0							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_0					
R/W-X		W-0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_0
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1684. DDRSS_PHY_43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_FIFO_PTR_OBS_0	R	0h	Observation register containing read entry FIFO pointers for slice 0. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	SC_PHY_MANUAL_CLEAR_0	W	0h	Manual reset/clear of internal logic for slice 0. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/max lock values. Bit (3) is manual reset of master delay unlock counter. Bit (4) is reset of leveling error bit in the leveling status registers. Bit (5) is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_CALVL_VREF_DRIVING_SLICE_0	R/W	0h	Indicates if slice 0 is used to drive the VREF value to the device during CA training.

4.4.45 DDRSS_PHY_44 Register (Offset = 40B0h) [reset = 00100000h]

DDRSS_PHY_44 is shown in [Figure 4-839](#) and described in [Table 4-1686](#).

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Table 4-1685. DDRSS_PHY_44 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40B0h

Figure 4-839. DDRSS_PHY_44 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_0																															
R-00100000h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1686. DDRSS_PHY_44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_LPBK_RESULT_OBS_0	R	00100000h	Observation register containing loopback status/results for slice 0. READ-ONLY

4.4.46 DDRSS_PHY_45 Register (Offset = 40B4h) [reset = X]

DDRSS_PHY_45 is shown in [Figure 4-840](#) and described in [Table 4-1688](#).

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Table 4-1687. DDRSS_PHY_45 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40B4h

Figure 4-840. DDRSS_PHY_45 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_0										
R-X					R-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_ERROR_COUNT_OBS_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1688. DDRSS_PHY_45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_MASTER_DLY_LOCK_OBS_0	R	0h	Observation register containing master delay results for slice 0. READ-ONLY
15-0	PHY_LPBK_ERROR_COUNT_OBS_0	R	0h	Observation register containing total number of loopback error data for slice 0. READ-ONLY

4.4.47 DDRSS_PHY_46 Register (Offset = 40B8h) [reset = X]

DDRSS_PHY_46 is shown in [Figure 4-841](#) and described in [Table 4-1690](#).

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Table 4-1689. DDRSS_PHY_46 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40B8h

Figure 4-841. DDRSS_PHY_46 Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0							
R-0h							
23	22	21	20	19	18	17	16
PHY_MEAS_DLY_STEP_VALUE_0							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0						
R-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_0						
R-X	R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 4-1690. DDRSS_PHY_46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS DQ rising edge adder slave delay encoded value for slice 0. READ-ONLY
23-16	PHY_MEAS_DLY_STEP_VALUE_0	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with denominator of 512, for slice 0. READ-ONLY
15	RESERVED	R	X	
14-8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS base slave delay encoded value for slice 0. READ-ONLY
7	RESERVED	R	X	
6-0	PHY_RDDQ_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQ slave delay encoded values for slice 0. READ-ONLY

4.4.48 DDRSS_PHY_47 Register (Offset = 40BCh) [reset = X]

DDRSS_PHY_47 is shown in [Figure 4-842](#) and described in [Table 4-1692](#).

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Table 4-1691. DDRSS_PHY_47 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40BCh

Figure 4-842. DDRSS_PHY_47 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0						
R-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0	
R-X						R-0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0							
R-0h							
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1692. DDRSS_PHY_47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	X	
30-24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write DQS base slave delay encoded value for slice 0. READ-ONLY
23-19	RESERVED	R	X	
18-8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS gate slave delay encoded value for slice 0. READ-ONLY
7-0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing read DQS DQ falling edge adder slave delay encoded value for slice 0. READ-ONLY

4.4.49 DDRSS_PHY_48 Register (Offset = 40C0h) [reset = X]

DDRSS_PHY_48 is shown in [Figure 4-843](#) and described in [Table 4-1694](#).

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Table 4-1693. DDRSS_PHY_48 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40C0h

Figure 4-843. DDRSS_PHY_48 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WR_SHIFT_OBS_0		
R-X					R-0h		
15	14	13	12	11	10	9	8
PHY_WR_ADDER_SLV_DLY_ENC_OBS_0							
R-0h							
7	6	5	4	3	2	1	0
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1694. DDRSS_PHY_48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18-16	PHY_WR_SHIFT_OBS_0	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 0. READ-ONLY
15-8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write adder slave delay encoded value for slice 0. READ-ONLY
7-0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing write DQ base slave delay encoded value for slice 0. READ-ONLY

4.4.50 DDRSS_PHY_49 Register (Offset = 40C4h) [reset = X]

DDRSS_PHY_49 is shown in [Figure 4-844](#) and described in [Table 4-1696](#).

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Table 4-1695. DDRSS_PHY_49 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40C4h

Figure 4-844. DDRSS_PHY_49 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_0									
R-X						R-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_0									
R-X						R-0h									

LEGEND: R = Read Only; -n = value after reset

Table 4-1696. DDRSS_PHY_49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_WRLVL_HARD1_DELAY_OBS_0	R	0h	Observation register containing write leveling first hard 1 DQS slave delay for slice 0. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_WRLVL_HARD0_DELAY_OBS_0	R	0h	Observation register containing write leveling last hard 0 DQS slave delay for slice 0. READ-ONLY

4.4.51 DDRSS_PHY_50 Register (Offset = 40C8h) [reset = X]

DDRSS_PHY_50 is shown in [Figure 4-845](#) and described in [Table 4-1698](#).

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Table 4-1697. DDRSS_PHY_50 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40C8h

Figure 4-845. DDRSS_PHY_50 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PHY_WRLVL_STATUS_OBS_0
R-X															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1698. DDRSS_PHY_50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-0	PHY_WRLVL_STATUS_OBS_0	R	0h	Observation register containing write leveling status for slice 0. READ-ONLY

4.4.52 DDRSS_PHY_51 Register (Offset = 40CCh) [reset = X]

DDRSS_PHY_51 is shown in [Figure 4-846](#) and described in [Table 4-1700](#).

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Table 4-1699. DDRSS_PHY_51 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40CCh

Figure 4-846. DDRSS_PHY_51 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1700. DDRSS_PHY_51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing gate sample2 slave delay encoded values for slice 0. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing gate sample1 slave delay encoded values for slice 0. READ-ONLY

4.4.53 DDRSS_PHY_52 Register (Offset = 40D0h) [reset = X]

DDRSS_PHY_52 is shown in [Figure 4-847](#) and described in [Table 4-1702](#).

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Table 4-1701. DDRSS_PHY_52 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40D0h

Figure 4-847. DDRSS_PHY_52 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_0													
R-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_ERROR_OBS_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1702. DDRSS_PHY_52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-16	PHY_GTLVL_HARD0_DELAY_OBS_0	R	0h	Observation register containing gate training first hard 0 DQS slave delay for slice 0. READ-ONLY
15-0	PHY_WRLVL_ERROR_OBS_0	R	0h	Observation register containing write leveling error status for slice 0. READ-ONLY

4.4.54 DDRSS_PHY_53 Register (Offset = 40D4h) [reset = X]

DDRSS_PHY_53 is shown in [Figure 4-848](#) and described in [Table 4-1704](#).

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Table 4-1703. DDRSS_PHY_53 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40D4h

Figure 4-848. DDRSS_PHY_53 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_0													
R-X		R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 4-1704. DDRSS_PHY_53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	X	
13-0	PHY_GTLVL_HARD1_DELAY_OBS_0	R	0h	Observation register containing gate training last hard 1 DQS slave delay for slice 0. READ-ONLY

4.4.55 DDRSS_PHY_54 Register (Offset = 40D8h) [reset = X]

DDRSS_PHY_54 is shown in [Figure 4-849](#) and described in [Table 4-1706](#).

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Table 4-1705. DDRSS_PHY_54 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40D8h

Figure 4-849. DDRSS_PHY_54 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													PHY_GTLVL_STATUS_OBS_0		
R-X													R-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1706. DDRSS_PHY_54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	PHY_GTLVL_STATUS_OBS_0	R	0h	Observation register containing gate training status for slice 0. READ-ONLY

4.4.56 DDRSS_PHY_55 Register (Offset = 40DCh) [reset = X]

DDRSS_PHY_55 is shown in [Figure 4-850](#) and described in [Table 4-1708](#).

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Table 4-1707. DDRSS_PHY_55 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40DCh

Figure 4-850. DDRSS_PHY_55 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1708. DDRSS_PHY_55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0	R	0h	Observation register containing read leveling data window trailing edge slave delay setting for slice 0. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0	R	0h	Observation register containing read leveling data window leading edge slave delay setting for slice 0. READ-ONLY

4.4.57 DDRSS_PHY_56 Register (Offset = 40E0h) [reset = X]

DDRSS_PHY_56 is shown in [Figure 4-851](#) and described in [Table 4-1710](#).

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Table 4-1709. DDRSS_PHY_56 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40E0h

Figure 4-851. DDRSS_PHY_56 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM _WINDOWS_OBS_0	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-1710. DDRSS_PHY_56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1-0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0	R	0h	Observation register containing read leveling number of windows found for slice 0. READ-ONLY

4.4.58 DDRSS_PHY_57 Register (Offset = 40E4h) [reset = 0h]

DDRSS_PHY_57 is shown in [Figure 4-852](#) and described in [Table 4-1712](#).

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Table 4-1711. DDRSS_PHY_57 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40E4h

Figure 4-852. DDRSS_PHY_57 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1712. DDRSS_PHY_57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_STATUS_OBS_0	R	0h	Observation register containing read leveling status for slice 0. READ-ONLY

4.4.59 DDRSS_PHY_58 Register (Offset = 40E8h) [reset = 0h]

DDRSS_PHY_58 is shown in [Figure 4-853](#) and described in [Table 4-1714](#).

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Table 4-1713. DDRSS_PHY_58 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40E8h

Figure 4-853. DDRSS_PHY_58 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1714. DDRSS_PHY_58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PERIODIC_OBS_0	R	0h	Observation register containing periodic read leveling status for slice 0. READ-ONLY

4.4.60 DDRSS_PHY_59 Register (Offset = 40ECh) [reset = X]

DDRSS_PHY_59 is shown in [Figure 4-854](#) and described in [Table 4-1716](#).

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Table 4-1715. DDRSS_PHY_59 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40ECh

Figure 4-854. DDRSS_PHY_59 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_0										
R-X					R-7FFh										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_0										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 4-1716. DDRSS_PHY_59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_WDQLVL_DQDM_TE_DLY_OBS_0	R	7FFh	Observation register containing write data leveling data window trailing edge slave delay setting for slice 0. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_WDQLVL_DQDM_LE_DLY_OBS_0	R	0h	Observation register containing write data leveling data window leading edge slave delay setting for slice 0. READ-ONLY

4.4.61 DDRSS_PHY_60 Register (Offset = 40F0h) [reset = 0h]

DDRSS_PHY_60 is shown in [Figure 4-855](#) and described in [Table 4-1718](#).

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Table 4-1717. DDRSS_PHY_60 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40F0h

Figure 4-855. DDRSS_PHY_60 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1718. DDRSS_PHY_60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_STATUS_OBS_0	R	0h	Observation register containing write data leveling status for slice 0. READ-ONLY

4.4.62 DDRSS_PHY_61 Register (Offset = 40F4h) [reset = 0h]

DDRSS_PHY_61 is shown in [Figure 4-856](#) and described in [Table 4-1720](#).

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Table 4-1719. DDRSS_PHY_61 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40F4h

Figure 4-856. DDRSS_PHY_61 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1720. DDRSS_PHY_61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_PERIODIC_OBS_0	R	0h	Observation register containing periodic write data leveling status for slice 0. READ-ONLY

4.4.63 DDRSS_PHY_62 Register (Offset = 40F8h) [reset = X]

DDRSS_PHY_62 is shown in [Figure 4-857](#) and described in [Table 4-1722](#).

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Table 4-1721. DDRSS_PHY_62 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40F8h

Figure 4-857. DDRSS_PHY_62 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE	PHY_DDL_MODE_0																														
SE																															
RV																															
ED																															
R/ W- X	R/W-0h																														

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1722. DDRSS_PHY_62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-0	PHY_DDL_MODE_0	R/W	0h	DDL mode for slice 0.

4.4.64 DDRSS_PHY_63 Register (Offset = 40FCh) [reset = X]

DDRSS_PHY_63 is shown in [Figure 4-858](#) and described in [Table 4-1724](#).

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Table 4-1723. DDRSS_PHY_63 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 40FCh

Figure 4-858. DDRSS_PHY_63 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PHY_DDL_MASK_0					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1724. DDRSS_PHY_63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	PHY_DDL_MASK_0	R/W	0h	DDL mask for slice 0.

4.4.65 DDRSS_PHY_64 Register (Offset = 4100h) [reset = 0h]

DDRSS_PHY_64 is shown in [Figure 4-859](#) and described in [Table 4-1726](#).

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Table 4-1725. DDRSS_PHY_64 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4100h

Figure 4-859. DDRSS_PHY_64 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1726. DDRSS_PHY_64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_OBS_0	R	0h	DDL test observation for slice 0. READ-ONLY

4.4.66 DDRSS_PHY_65 Register (Offset = 4104h) [reset = 0h]

DDRSS_PHY_65 is shown in [Figure 4-860](#) and described in [Table 4-1728](#).

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Table 4-1727. DDRSS_PHY_65 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4104h

Figure 4-860. DDRSS_PHY_65 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1728. DDRSS_PHY_65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_MSTR_DLY_OBS_0	R	0h	DDL test observation delays for slice 0 master DDL. READ-ONLY

4.4.67 DDRSS_PHY_66 Register (Offset = 4108h) [reset = X]

DDRSS_PHY_66 is shown in [Figure 4-861](#) and described in [Table 4-1730](#).

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Table 4-1729. DDRSS_PHY_66 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4108h

Figure 4-861. DDRSS_PHY_66 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_OVERRIDE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_RX_CAL_START_0
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1730. DDRSS_PHY_66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_OVERRIDE_0	R/W	0h	Manual setting of RX Calibration enable for slice 0.
23-17	RESERVED	R/W	X	
16	SC_PHY_RX_CAL_START_0	W	0h	Manual RX Calibration start for slice 0. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	PHY_LP4_WDQS_OE_EXTEND_0	R/W	0h	LPDDR4 write preamble extension enable for slice 0.
7-0	PHY_DDL_TRACK_UPD_THRESHOLD_0	R/W	0h	Specify threshold value for PHY init update tracking for slice 0.

4.4.68 DDRSS_PHY_67 Register (Offset = 410Ch) [reset = X]

DDRSS_PHY_67 is shown in [Figure 4-862](#) and described in [Table 4-1732](#).

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Table 4-1731. DDRSS_PHY_67 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 410Ch

Figure 4-862. DDRSS_PHY_67 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_SAMPLE_WAIT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1732. DDRSS_PHY_67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ0_0	R/W	0h	RX Calibration codes for DQ0 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8	PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_0	R/W	0h	Data slice power reduction disable for slice 0.
7-0	PHY_RX_CAL_SAMPLE_WAIT_0	R/W	0h	RX Calibration state machine wait count for slice 0.

4.4.69 DDRSS_PHY_68 Register (Offset = 4110h) [reset = X]

DDRSS_PHY_68 is shown in [Figure 4-863](#) and described in [Table 4-1734](#).

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Table 4-1733. DDRSS_PHY_68 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4110h

Figure 4-863. DDRSS_PHY_68 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ2_0							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ1_0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1734. DDRSS_PHY_68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ2_0	R/W	0h	RX Calibration codes for DQ2 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ1_0	R/W	0h	RX Calibration codes for DQ1 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.70 DDRSS_PHY_69 Register (Offset = 4114h) [reset = X]

DDRSS_PHY_69 is shown in [Figure 4-864](#) and described in [Table 4-1736](#).

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Table 4-1735. DDRSS_PHY_69 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4114h

Figure 4-864. DDRSS_PHY_69 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ4_0							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ3_0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1736. DDRSS_PHY_69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ4_0	R/W	0h	RX Calibration codes for DQ4 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ3_0	R/W	0h	RX Calibration codes for DQ3 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.71 DDRSS_PHY_70 Register (Offset = 4118h) [reset = X]

DDRSS_PHY_70 is shown in [Figure 4-865](#) and described in [Table 4-1738](#).

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Table 4-1737. DDRSS_PHY_70 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4118h

Figure 4-865. DDRSS_PHY_70 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ6_0							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ5_0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1738. DDRSS_PHY_70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ6_0	R/W	0h	RX Calibration codes for DQ6 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ5_0	R/W	0h	RX Calibration codes for DQ5 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.72 DDRSS_PHY_71 Register (Offset = 411Ch) [reset = X]

DDRSS_PHY_71 is shown in [Figure 4-866](#) and described in [Table 4-1740](#).

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Table 4-1739. DDRSS_PHY_71 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 411Ch

Figure 4-866. DDRSS_PHY_71 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ7_0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1740. DDRSS_PHY_71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ7_0	R/W	0h	RX Calibration codes for DQ7 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.73 DDRSS_PHY_72 Register (Offset = 4120h) [reset = X]

DDRSS_PHY_72 is shown in [Figure 4-867](#) and described in [Table 4-1742](#).

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Table 4-1741. DDRSS_PHY_72 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4120h

Figure 4-867. DDRSS_PHY_72 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_RX_CAL_DM_0																	
R/W-X														R/W-0h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1742. DDRSS_PHY_72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_RX_CAL_DM_0	R/W	0h	<p>RX Calibration codes for DM for slice 0.</p> <p>Bits (5:0) contain rx_cal_code_down.</p> <p>Bits (11:6) contain rx_cal_code_up.</p> <p>Bits (17:12) contain rx_cal_code2_down.</p> <p>Bits (23:18) contain rx_cal_code2_up.</p>

4.4.74 DDRSS_PHY_73 Register (Offset = 4124h) [reset = X]

DDRSS_PHY_73 is shown in [Figure 4-868](#) and described in [Table 4-1744](#).

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Table 4-1743. DDRSS_PHY_73 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4124h

Figure 4-868. DDRSS_PHY_73 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_FDBK_0							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQS_0							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1744. DDRSS_PHY_73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_FDBK_0	R/W	0h	RX Calibration codes for FDBK for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQS_0	R/W	0h	RX Calibration codes for DQS for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.75 DDRSS_PHY_74 Register (Offset = 4128h) [reset = X]

DDRSS_PHY_74 is shown in [Figure 4-869](#) and described in [Table 4-1746](#).

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Table 4-1745. DDRSS_PHY_74 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4128h

Figure 4-869. DDRSS_PHY_74 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_LOCK_OBS_0							
R-X								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_OBS_0							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1746. DDRSS_PHY_74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	X	
24-16	PHY_RX_CAL_LOCK_OBS_0	R	0h	RX Calibration lock results for slice 0. Bit (3:0) is the state machine rx_cal_sm. Bit (4) is the rx_cal_done signal. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_RX_CAL_OBS_0	R	0h	RX Calibration results for slice 0. Bits (7:0) contain calibration results from DQ 0-7. Bit (8) contains calibration result from DM. Bit (9) contains calibration result from DQS. Bit (10) contains calibration result from FDBK. READ-ONLY

4.4.76 DDRSS_PHY_75 Register (Offset = 412Ch) [reset = X]

DDRSS_PHY_75 is shown in [Figure 4-870](#) and described in [Table 4-1748](#).

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Table 4-1747. DDRSS_PHY_75 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 412Ch

Figure 4-870. DDRSS_PHY_75 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_COMP_VAL_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED	PHY_RX_CAL_DIFF_ADJUST_0						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_RX_CAL_SE_ADJUST_0						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RX_CAL_DISABLE_0
R/W-X							R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1748. DDRSS_PHY_75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_COMP_VAL_0	R/W	0h	Expected C value from RX pad for slice 0.
23	RESERVED	R/W	X	
22-16	PHY_RX_CAL_DIFF_ADJUST_0	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 0.
15	RESERVED	R/W	X	
14-8	PHY_RX_CAL_SE_ADJUST_0	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_RX_CAL_DISABLE_0	R/W	1h	RX CAL disable signal for slice 0, set 1 to bypass the rx calibration

4.4.77 DDRSS_PHY_76 Register (Offset = 4130h) [reset = X]

DDRSS_PHY_76 is shown in [Figure 4-871](#) and described in [Table 4-1750](#).

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Table 4-1749. DDRSS_PHY_76 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4130h

Figure 4-871. DDRSS_PHY_76 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_PAD_RX_BIAS_EN_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_RX_CAL_INDEX_MASK_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1750. DDRSS_PHY_76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PAD_RX_BIAS_EN_0	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 0.
15-12	RESERVED	R/W	X	
11-0	PHY_RX_CAL_INDEX_MASK_0	R/W	0h	RX offset calibration mask of all RX pad for slice 0.

4.4.78 DDRSS_PHY_77 Register (Offset = 4134h) [reset = X]

DDRSS_PHY_77 is shown in [Figure 4-872](#) and described in [Table 4-1752](#).

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Table 4-1751. DDRSS_PHY_77 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4134h

Figure 4-872. DDRSS_PHY_77 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_DATA_DC_WEIGHT_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DATA_DC_CAL_TIMEOUT_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_CAL_SAMPLE_WAIT_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_STATIC_TOG_DISABLE_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1752. DDRSS_PHY_77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_DATA_DC_WEIGHT_0	R/W	0h	Determines weight of average calculating for slice 0.
23-16	PHY_DATA_DC_CAL_TIMEOUT_0	R/W	0h	Determines timeout number of iteration for slice 0.
15-8	PHY_DATA_DC_CAL_SAMPLE_WAIT_0	R/W	0h	Determines number of cycles to wait for each sample for slice 0.
7-5	RESERVED	R/W	X	
4-0	PHY_STATIC_TOG_DISABLE_0	R/W	0h	Control to disable toggle during static activity for slice 0. bit 0: Write path delay line disable bit 1: Read path delay line disable bit 2: Read data path disable bit 3: clk_phy disable bit 4: master delay line disable.

4.4.79 DDRSS_PHY_78 Register (Offset = 4138h) [reset = X]

DDRSS_PHY_78 is shown in [Figure 4-873](#) and described in [Table 4-1754](#).

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Table 4-1753. DDRSS_PHY_78 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4138h

Figure 4-873. DDRSS_PHY_78 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_DATA_DC_ADJUST_THRSHLD_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_ADJUST_SAMPLE_CNT_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DATA_DC_ADJUST_START_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1754. DDRSS_PHY_78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_DATA_DC_ADJUST_DIRECT_0	R/W	0h	Adjust direction for slice 0.
23-16	PHY_DATA_DC_ADJUST_THRSHLD_0	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 0.
15-8	PHY_DATA_DC_ADJUST_SAMPLE_CNT_0	R/W	0h	Duty cycle adjust sample count for slice 0.
7-6	RESERVED	R/W	X	
5-0	PHY_DATA_DC_ADJUST_START_0	R/W	0h	Duty cycle adjust starting value for slice 0.

4.4.80 DDRSS_PHY_79 Register (Offset = 413Ch) [reset = X]

DDRSS_PHY_79 is shown in [Figure 4-874](#) and described in [Table 4-1756](#).

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Table 4-1755. DDRSS_PHY_79 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 413Ch

Figure 4-874. DDRSS_PHY_79 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_FDBK_PWR_CTRL_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_SW_RANK_0	
R/W-X						R/W-1h	
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_CAL_START_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_CAL_POLARITY_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1756. DDRSS_PHY_79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_FDBK_PWR_CTRL_0	R/W	0h	Shutoff gate feedback IO to reduce power for slice 0.
23-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_SW_RANK_0	R/W	1h	Rank selection for software based duty cycle correction for slice 0.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_CAL_START_0	R/W	0h	Manual trigger for DCC for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_CAL_POLARITY_0	R/W	0h	Calibration polarity for slice 0.

4.4.81 DDRSS_PHY_80 Register (Offset = 4140h) [reset = X]

DDRSS_PHY_80 is shown in [Figure 4-875](#) and described in [Table 4-1758](#).

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Table 4-1757. DDRSS_PHY_80 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4140h

Figure 4-875. DDRSS_PHY_80 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_RDPATH_GATE_DISABLE_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1758. DDRSS_PHY_80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SLICE_PWR_RDC_DISABLE_0	R/W	0h	Data slice power reduction disable for slice 0.
23-17	RESERVED	R/W	X	
16	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_0	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 0.
15-9	RESERVED	R/W	X	
8	PHY_RDPATH_GATE_DISABLE_0	R/W	0h	Data slice read path power reduction disable for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_SLV_DLY_CTRL_GATE_DISABLE_0	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 0.

4.4.82 DDRSS_PHY_81 Register (Offset = 4144h) [reset = X]

DDRSS_PHY_81 is shown in [Figure 4-876](#) and described in [Table 4-1760](#).

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Table 4-1759. DDRSS_PHY_81 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4144h

Figure 4-876. DDRSS_PHY_81 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_DS_FSM_ERROR_INFO_0													
R/W-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_PARITY_ERROR_REGIF_0										
R/W-X					R/W-0h										

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1760. DDRSS_PHY_81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_DS_FSM_ERROR_INFO_0	R	0h	Data slice level FSM Error Info for slice 0. READ-ONLY
15-11	RESERVED	R/W	X	
10-0	PHY_PARITY_ERROR_REGIF_0	R/W	0h	Inject parity error to register interface signals for slice 0.

4.4.83 DDRSS_PHY_82 Register (Offset = 4148h) [reset = X]

DDRSS_PHY_82 is shown in [Figure 4-877](#) and described in [Table 4-1762](#).

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Table 4-1761. DDRSS_PHY_82 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4148h

Figure 4-877. DDRSS_PHY_82 Register

31	30	29	28	27	26	25	24
RESERVED		SC_PHY_DS_FSM_ERROR_INFO_WOCLR_0					
R/W-X		W-0h					
23	22	21	20	19	18	17	16
SC_PHY_DS_FSM_ERROR_INFO_WOCLR_0							
W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_DS_FSM_ERROR_INFO_MASK_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
PHY_DS_FSM_ERROR_INFO_MASK_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1762. DDRSS_PHY_82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	SC_PHY_DS_FSM_ERROR_INFO_WOCLR_0	W	0h	Data slice level FSM Error Info for slice 0. WRITE-ONLY
15-14	RESERVED	R/W	X	
13-0	PHY_DS_FSM_ERROR_INFO_MASK_0	R/W	0h	Data slice level FSM Error Info Mask for slice 0.

4.4.84 DDRSS_PHY_83 Register (Offset = 414Ch) [reset = X]

DDRSS_PHY_83 is shown in [Figure 4-878](#) and described in [Table 4-1764](#).

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Table 4-1763. DDRSS_PHY_83 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 414Ch

Figure 4-878. DDRSS_PHY_83 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_0			
R/W-X				W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_0			
R/W-X				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1764. DDRSS_PHY_83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_0	W	0h	Data slice level training/calibration Error Info for slice 0. WRITE-ONLY
15-13	RESERVED	R/W	X	
12-8	PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_0	R/W	0h	Data slice level training/calibration Error Info Mask for slice 0.
7-5	RESERVED	R/W	X	
4-0	PHY_DS_TRAIN_CALIB_ERROR_INFO_0	R	0h	Data slice level training/calibration Error Info for slice 0. READ-ONLY

4.4.85 DDRSS_PHY_84 Register (Offset = 4150h) [reset = X]

DDRSS_PHY_84 is shown in [Figure 4-879](#) and described in [Table 4-1766](#).

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Table 4-1765. DDRSS_PHY_84 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4150h

Figure 4-879. DDRSS_PHY_84 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DQ_TSEL_SELECT_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_TSEL_SELECT_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_DQ_TSEL_ENABLE_0		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1766. DDRSS_PHY_84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_DQS_TSEL_ENABLE_0	R/W	0h	Operation type tsel enables for DQS signals for slice 0. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.
23-8	PHY_DQ_TSEL_SELECT_0	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 0.
7-3	RESERVED	R/W	X	
2-0	PHY_DQ_TSEL_ENABLE_0	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 0. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.

4.4.86 DDRSS_PHY_85 Register (Offset = 4154h) [reset = X]

DDRSS_PHY_85 is shown in [Figure 4-880](#) and described in [Table 4-1768](#).

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Table 4-1767. DDRSS_PHY_85 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4154h

Figure 4-880. DDRSS_PHY_85 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1768. DDRSS_PHY_85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PHY_VREF_INITIAL_START_POINT_0	R/W	0h	Data slice initial VREF training start value for slice 0.
23-18	RESERVED	R/W	X	
17-16	PHY_TWO_CYC_PREAMBLE_0	R/W	0h	2 cycle preamble support for slice 0. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2 cycle write preamble. Set each bit to 1 to enable.
15-0	PHY_DQS_TSEL_SELECT_0	R/W	0h	Operation type tsel select values for DQS signals for slice 0.

4.4.87 DDRSS_PHY_86 Register (Offset = 4158h) [reset = X]

DDRSS_PHY_86 is shown in [Figure 4-881](#) and described in [Table 4-1770](#).

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Table 4-1769. DDRSS_PHY_86 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4158h

Figure 4-881. DDRSS_PHY_86 Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1770. DDRSS_PHY_86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_NTP_WDQ_STEP_SIZE_0	R/W	0h	Step size of WR DQ slave delay during No-Topology training for slice 0.
23-17	RESERVED	R/W	X	
16	PHY_NTP_TRAIN_EN_0	R/W	0h	Enable for No-Topology training for slice 0.
15-10	RESERVED	R/W	X	
9-8	PHY_VREF_TRAINING_CTRL_0	R/W	0h	Data slice vref training enable control for slice 0.
7	RESERVED	R/W	X	
6-0	PHY_VREF_INITIAL_STOP_POINT_0	R/W	0h	Data slice initial VREF training stop value for slice 0.

4.4.88 DDRSS_PHY_87 Register (Offset = 415Ch) [reset = X]

DDRSS_PHY_87 is shown in [Figure 4-882](#) and described in [Table 4-1772](#).

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Table 4-1771. DDRSS_PHY_87 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 415Ch

Figure 4-882. DDRSS_PHY_87 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_NTP_WDQ_STOP_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_NTP_WDQ_START_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1772. DDRSS_PHY_87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_NTP_WDQ_STOP_0	R/W	0h	End of WR DQ slave delay in No-Topology training for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_NTP_WDQ_START_0	R/W	0h	Starting WR DQ slave delay in No-Topology training for slice 0.

4.4.89 DDRSS_PHY_88 Register (Offset = 4160h) [reset = X]

DDRSS_PHY_88 is shown in [Figure 4-883](#) and described in [Table 4-1774](#).

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Table 4-1773. DDRSS_PHY_88 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4160h

Figure 4-883. DDRSS_PHY_88 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_WDQLVL_DVW_MIN_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_WDQLVL_DVW_MIN_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_BIT_EN_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1774. DDRSS_PHY_88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SW_WDQLVL_DVW_MIN_EN_0	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 0.
23-18	RESERVED	R/W	X	
17-8	PHY_WDQLVL_DVW_MIN_0	R/W	0h	Minimum data valid window across DQs and ranks for slice 0.
7-0	PHY_NTP_WDQ_BIT_EN_0	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 0.

4.4.90 DDRSS_PHY_89 Register (Offset = 4164h) [reset = X]

DDRSS_PHY_89 is shown in [Figure 4-884](#) and described in [Table 4-1776](#).

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Table 4-1775. DDRSS_PHY_89 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4164h

Figure 4-884. DDRSS_PHY_89 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_0_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_TX_DCD_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1776. DDRSS_PHY_89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_0_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_TX_DCD_0	R/W	0h	Controls TX_DCD pin for each pad for slice 0.
15-12	RESERVED	R/W	X	
11-8	PHY_FAST_LVL_EN_0	R/W	0h	Enable for fast multi-pattern window search for slice 0.
7-6	RESERVED	R/W	X	
5-0	PHY_WDQLVL_PER_START_OFFSET_0	R/W	0h	Periodic training start point offset for slice 0.

4.4.91 DDRSS_PHY_90 Register (Offset = 4168h) [reset = X]

DDRSS_PHY_90 is shown in [Figure 4-885](#) and described in [Table 4-1778](#).

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Table 4-1777. DDRSS_PHY_90 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4168h

Figure 4-885. DDRSS_PHY_90 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_4_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_3_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_2_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_1_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1778. DDRSS_PHY_90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_4_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_3_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_2_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_1_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.

4.4.92 DDRSS_PHY_91 Register (Offset = 416Ch) [reset = X]

DDRSS_PHY_91 is shown in [Figure 4-886](#) and described in [Table 4-1780](#).

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Table 4-1779. DDRSS_PHY_91 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 416Ch

Figure 4-886. DDRSS_PHY_91 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_DM_RX_DCD_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_7_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_6_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_5_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1780. DDRSS_PHY_91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_DM_RX_DCD_0	R/W	0h	Controls RX_DCD pin for dm pad for slice 0.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_7_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_6_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_5_0	R/W	0h	Controls RX_DCD pin for each pad for slice 0.

4.4.93 DDRSS_PHY_92 Register (Offset = 4170h) [reset = X]

DDRSS_PHY_92 is shown in [Figure 4-887](#) and described in [Table 4-1782](#).

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Table 4-1781. DDRSS_PHY_92 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4170h

Figure 4-887. DDRSS_PHY_92 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PHY_PAD_DSLICE_IO_CFG_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_0				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_0				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1782. DDRSS_PHY_92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PHY_PAD_DSLICE_IO_CFG_0	R/W	0h	Controls PCLK/PARK pin for pad for slice 0.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_FDBK_RX_DCD_0	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 0.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_DQS_RX_DCD_0	R/W	0h	Controls RX_DCD pin for dqs pad for slice 0.

4.4.94 DDRSS_PHY_93 Register (Offset = 4174h) [reset = X]

DDRSS_PHY_93 is shown in [Figure 4-888](#) and described in [Table 4-1784](#).

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Table 4-1783. DDRSS_PHY_93 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4174h

Figure 4-888. DDRSS_PHY_93 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ1_SLAVE_DELAY_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ0_SLAVE_DELAY_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1784. DDRSS_PHY_93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ1_SLAVE_DELAY_0	R/W	0h	Read DQ1 slave delay setting for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ0_SLAVE_DELAY_0	R/W	0h	Read DQ0 slave delay setting for slice 0.

4.4.95 DDRSS_PHY_94 Register (Offset = 4178h) [reset = X]

DDRSS_PHY_94 is shown in [Figure 4-889](#) and described in [Table 4-1786](#).

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Table 4-1785. DDRSS_PHY_94 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4178h

Figure 4-889. DDRSS_PHY_94 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ3_SLAVE_DELAY_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ2_SLAVE_DELAY_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1786. DDRSS_PHY_94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ3_SLAVE_DELAY_0	R/W	0h	Read DQ3 slave delay setting for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ2_SLAVE_DELAY_0	R/W	0h	Read DQ2 slave delay setting for slice 0.

4.4.96 DDRSS_PHY_95 Register (Offset = 417Ch) [reset = X]

DDRSS_PHY_95 is shown in [Figure 4-890](#) and described in [Table 4-1788](#).

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Table 4-1787. DDRSS_PHY_95 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 417Ch

Figure 4-890. DDRSS_PHY_95 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ5_SLAVE_DELAY_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ4_SLAVE_DELAY_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1788. DDRSS_PHY_95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ5_SLAVE_DELAY_0	R/W	0h	Read DQ5 slave delay setting for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ4_SLAVE_DELAY_0	R/W	0h	Read DQ4 slave delay setting for slice 0.

4.4.97 DDRSS_PHY_96 Register (Offset = 4180h) [reset = X]

DDRSS_PHY_96 is shown in [Figure 4-891](#) and described in [Table 4-1790](#).

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Table 4-1789. DDRSS_PHY_96 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4180h

Figure 4-891. DDRSS_PHY_96 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ7_SLAVE_DELAY_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ6_SLAVE_DELAY_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1790. DDRSS_PHY_96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ7_SLAVE_DELAY_0	R/W	0h	Read DQ7 slave delay setting for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ6_SLAVE_DELAY_0	R/W	0h	Read DQ6 slave delay setting for slice 0.

4.4.98 DDRSS_PHY_97 Register (Offset = 4184h) [reset = X]

DDRSS_PHY_97 is shown in [Figure 4-892](#) and described in [Table 4-1792](#).

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Table 4-1791. DDRSS_PHY_97 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4184h

Figure 4-892. DDRSS_PHY_97 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_DATA_DC_CAL_CLK_SEL_0		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1792. DDRSS_PHY_97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_DATA_DC_CAL_CLK_SEL_0	R/W	0h	Determines DCC CAL clock for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDM_SLAVE_DELAY_0	R/W	0h	Read DM/DBI slave delay setting for slice 0. May be used for data swap.

4.4.99 DDRSS_PHY_98 Register (Offset = 4188h) [reset = 0h]

DDRSS_PHY_98 is shown in [Figure 4-893](#) and described in [Table 4-1794](#).

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Table 4-1793. DDRSS_PHY_98 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4188h

Figure 4-893. DDRSS_PHY_98 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_DQS_OE_TIMING_0								PHY_DQ_TSEL_WR_TIMING_0							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_TSEL_RD_TIMING_0								PHY_DQ_OE_TIMING_0							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1794. DDRSS_PHY_98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_OE_TIMING_0	R/W	0h	Start/end timing values for DQS output enable signals for slice 0.
23-16	PHY_DQ_TSEL_WR_TIMING_0	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 0.
15-8	PHY_DQ_TSEL_RD_TIMING_0	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 0.
7-0	PHY_DQ_OE_TIMING_0	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 0.

4.4.100 DDRSS_PHY_99 Register (Offset = 418Ch) [reset = X]

DDRSS_PHY_99 is shown in [Figure 4-894](#) and described in [Table 4-1796](#).

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Table 4-1795. DDRSS_PHY_99 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 418Ch

Figure 4-894. DDRSS_PHY_99 Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_0							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DQS_OE_RD_TIMING_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_RD_TIMING_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_IO_PAD_DELAY_TIMING_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1796. DDRSS_PHY_99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_TSEL_WR_TIMING_0	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 0.
23-16	PHY_DQS_OE_RD_TIMING_0	R/W	0h	Start/end timing values for DQS read based OE extension for slice 0.
15-8	PHY_DQS_TSEL_RD_TIMING_0	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_IO_PAD_DELAY_TIMING_0	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 0.

4.4.101 DDRSS_PHY_100 Register (Offset = 4190h) [reset = X]

DDRSS_PHY_100 is shown in [Figure 4-895](#) and described in [Table 4-1798](#).

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Table 4-1797. DDRSS_PHY_100 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4190h

Figure 4-895. DDRSS_PHY_100 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_VREF_CTRL_DQ_0											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_VREF_SETTING_TIME_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1798. DDRSS_PHY_100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PHY_PAD_VREF_CTRL_DQ_0	R/W	0h	Pad VREF control settings for DQ slice 0. <ul style="list-style-type: none"> Bits[27-24] = MODE Bits[23] = EN Bits[22-16] = VREFSEL
15-0	PHY_VREF_SETTING_TIME_0	R/W	0h	Number of cycles for vref settle after setting is changed for slice 0.

4.4.102 DDRSS_PHY_101 Register (Offset = 4194h) [reset = X]

DDRSS_PHY_101 is shown in [Figure 4-896](#) and described in [Table 4-1800](#).

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Table 4-1799. DDRSS_PHY_101 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4194h

Figure 4-896. DDRSS_PHY_101 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DQS_IE_TIMING_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_IE_TIMING_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_PER_CS_TRAINING_EN_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1800. DDRSS_PHY_101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_RDDATA_EN_IE_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 0.
23-16	PHY_DQS_IE_TIMING_0	R/W	0h	Start/end timing values for DQS input enable signals for slice 0.
15-8	PHY_DQ_IE_TIMING_0	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_EN_0	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 0. Must have same value in all slices.

4.4.103 DDRSS_PHY_102 Register (Offset = 4198h) [reset = X]

DDRSS_PHY_102 is shown in [Figure 4-897](#) and described in [Table 4-1802](#).

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Table 4-1801. DDRSS_PHY_102 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4198h

Figure 4-897. DDRSS_PHY_102 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDDATA_EN_OE_DLY_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_TSEL_DLY_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_DBI_MODE_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PHY_IE_MODE_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1802. DDRSS_PHY_102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDDATA_EN_OE_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 0.
23-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_TSEL_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 0.
15-9	RESERVED	R/W	X	
8	PHY_DBI_MODE_0	R/W	0h	DBI mode for slice 0. Bit (0) enables return of DBI read data.
7-2	RESERVED	R/W	X	
1-0	PHY_IE_MODE_0	R/W	0h	Input enable mode bits for slice 0. Bit (0) enables the mode where the input enables are always on set to 1 to enable. Bit (1) disables the input enable on the DM signal set to 1 to disable.

4.4.104 DDRSS_PHY_103 Register (Offset = 419Ch) [reset = X]

DDRSS_PHY_103 is shown in [Figure 4-898](#) and described in [Table 4-1804](#).

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Table 4-1803. DDRSS_PHY_103 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 419Ch

Figure 4-898. DDRSS_PHY_103 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_MASTER_DELAY_STEP_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DELAY_START_0		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_START_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_MASTER_MODE_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1804. DDRSS_PHY_103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_MASTER_DELAY_STEP_0	R/W	0h	Incremental step size for master delay line locking algorithm for slice 0.
23-19	RESERVED	R/W	X	
18-8	PHY_MASTER_DELAY_START_0	R/W	0h	Start value for master delay line locking algorithm for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_SW_MASTER_MODE_0	R/W	0h	Master delay line override settings for slice 0. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit (2) enables software bypass mode. Bit (3) is the software bypass mode value.

4.4.105 DDRSS_PHY_104 Register (Offset = 41A0h) [reset = X]

DDRSS_PHY_104 is shown in Figure 4-899 and described in Table 4-1806.

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Table 4-1805. DDRSS_PHY_104 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41A0h

Figure 4-899. DDRSS_PHY_104 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_DLY_STEP_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_RPTR_UPDATE_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_HALF_MEASURE_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_MASTER_DELAY_WAIT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1806. DDRSS_PHY_104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_DLY_STEP_0	R/W	0h	DQS slave delay step size during write leveling for slice 0.
23-20	RESERVED	R/W	X	
19-16	PHY_RPTR_UPDATE_0	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 0.
15-8	PHY_MASTER_DELAY_HALF_MEASURE_0	R/W	0h	Defines the number of delay line elements to be considered in determining whether to lock to a half clock cycle in the data slice master for slice 0.
7-0	PHY_MASTER_DELAY_WAIT_0	R/W	0h	Wait cycles for master delay line locking algorithm for slice 0. Bits (3:0) are the cycle wait count after a calibration clock setting change. Bits (7:4) are the cycle wait count after a master delay setting change.

4.4.106 DDRSS_PHY_105 Register (Offset = 41A4h) [reset = X]

DDRSS_PHY_105 is shown in Figure 4-900 and described in Table 4-1808.

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Table 4-1807. DDRSS_PHY_105 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41A4h

Figure 4-900. DDRSS_PHY_105 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_RESP_WAIT_CNT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_DLY_STEP_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_RESP_WAIT_CNT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_WRLVL_DLY_FINE_STEP_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1808. DDRSS_PHY_105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_GTLVL_RESP_WAIT_CNT_0	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 0. The valid range is 0x0 to 0xB.
23-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_DLY_STEP_0	R/W	0h	DQS slave delay step size during gate training for slice 0.
15-14	RESERVED	R/W	X	
13-8	PHY_WRLVL_RESP_WAIT_CNT_0	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_WRLVL_DLY_FINE_STEP_0	R/W	0h	DQS slave delay fine step size during write leveling for slice 0.

4.4.107 DDRSS_PHY_106 Register (Offset = 41A8h) [reset = X]

DDRSS_PHY_106 is shown in [Figure 4-901](#) and described in [Table 4-1810](#).

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Table 4-1809. DDRSS_PHY_106 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41A8h

Figure 4-901. DDRSS_PHY_106 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_FINAL_STEP_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_GTLVL_BACK_STEP_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1810. DDRSS_PHY_106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_GTLVL_FINAL_STEP_0	R/W	0h	Final backup step delay used in gate training algorithm for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_BACK_STEP_0	R/W	0h	Interim backup step delay used in gate training algorithm for slice 0.

4.4.108 DDRSS_PHY_107 Register (Offset = 41ACh) [reset = X]

DDRSS_PHY_107 is shown in Figure 4-902 and described in Table 4-1812.

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Table 4-1811. DDRSS_PHY_107 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41ACh

Figure 4-902. DDRSS_PHY_107 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_DLY_STEP_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PHY_TOGGLE_PRE_SUPP RT_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_WDQLVL_DLY_STEP_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1812. DDRSS_PHY_107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_RDLVL_DLY_STEP_0	R/W	0h	DQS slave delay step size during read leveling for slice 0.
23-17	RESERVED	R/W	X	
16	PHY_TOGGLE_PRE_SUPPORT_0	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 0.
15-12	RESERVED	R/W	X	
11-8	PHY_WDQLVL_QTR_DLY_STEP_0	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 0. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value.
7-0	PHY_WDQLVL_DLY_STEP_0	R/W	0h	DQ slave delay step size during write data leveling for slice 0.

4.4.109 DDRSS_PHY_108 Register (Offset = 41B0h) [reset = X]

DDRSS_PHY_108 is shown in [Figure 4-903](#) and described in [Table 4-1814](#).

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Table 4-1813. DDRSS_PHY_108 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41B0h

Figure 4-903. DDRSS_PHY_108 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_MAX_EDGE_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1814. DDRSS_PHY_108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_MAX_EDGE_0	R/W	0h	The maximum rdlvl slave delay search window for read eye training for slice 0.

4.4.110 DDRSS_PHY_109 Register (Offset = 41B4h) [reset = X]

DDRSS_PHY_109 is shown in Figure 4-904 and described in Table 4-1816.

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Table 4-1815. DDRSS_PHY_109 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41B4h

Figure 4-904. DDRSS_PHY_109 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_RDLVL_PER_START_OFFSET_0					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED							PHY_SW_RDLVL_DVW_MIN_EN_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_DVW_MIN_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_DVW_MIN_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1816. DDRSS_PHY_109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_RDLVL_PER_START_OFFSET_0	R/W	0h	Periodic training start point offset for slice 0.
23-17	RESERVED	R/W	X	
16	PHY_SW_RDLVL_DVW_MIN_EN_0	R/W	0h	SW override to enable use of PHY_RDLVL_DVW_MIN for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_DVW_MIN_0	R/W	0h	Minimum data valid window across DQs and ranks for slice 0.

4.4.111 DDRSS_PHY_110 Register (Offset = 41B8h) [reset = X]

DDRSS_PHY_110 is shown in [Figure 4-905](#) and described in [Table 4-1818](#).

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Table 4-1817. DDRSS_PHY_110 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41B8h

Figure 4-905. DDRSS_PHY_110 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_0	
R/W-X						R/W-3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1818. DDRSS_PHY_110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_INIT_DISABLE_0	R/W	3h	Disable duty cycle adjust at initialization for slice 0.
15-11	RESERVED	R/W	X	
10-8	PHY_WRPATH_GATE_TIMING_0	R/W	0h	Write path clock gating timing for slice 0. it means additional clock number to write path clock gate
7-2	RESERVED	R/W	X	
1-0	PHY_WRPATH_GATE_DISABLE_0	R/W	0h	Write path clock gating disable for slice 0. [0]: disable pull in wrdata_en [1]: disable write path clock gating, clock always on

4.4.112 DDRSS_PHY_111 Register (Offset = 41BCh) [reset = X]

DDRSS_PHY_111 is shown in [Figure 4-906](#) and described in [Table 4-1820](#).

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Table 4-1819. DDRSS_PHY_111 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41BCh

Figure 4-906. DDRSS_PHY_111 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ_INIT_SLV_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_INIT_SLV_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1820. DDRSS_PHY_111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_0	R/W	0h	Initial value of write DQ slave delay for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_0	R/W	0h	Initial value of write DQS slave delay for slice 0.

4.4.113 DDRSS_PHY_112 Register (Offset = 41C0h) [reset = X]

DDRSS_PHY_112 is shown in [Figure 4-907](#) and described in [Table 4-1822](#).

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Table 4-1821. DDRSS_PHY_112 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41C0h

Figure 4-907. DDRSS_PHY_112 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_0							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DM_CLK_SE_THRSHLD_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_0
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1822. DDRSS_PHY_112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_0	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 0.
23-16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_0	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 0.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_WDQLVL_ENABLE_0	R/W	0h	Enable duty cycle adjust during write DQ training for slice 0.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_WRLVL_ENABLE_0	R/W	0h	Enable duty cycle adjust during write leveling for slice 0.

4.4.114 DDRSS_PHY_113 Register (Offset = 41C4h) [reset = X]

DDRSS_PHY_113 is shown in [Figure 4-908](#) and described in [Table 4-1824](#).

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Table 4-1823. DDRSS_PHY_113 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41C4h

Figure 4-908. DDRSS_PHY_113 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_DLY_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED			PHY_MEAS_DLY_STEP_ENABLE_0				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQ_OSC_DELTA_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1824. DDRSS_PHY_113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_DLY_0	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 0.
15-14	RESERVED	R/W	X	
13-8	PHY_MEAS_DLY_STEP_ENABLE_0	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 0.
7	RESERVED	R/W	X	
6-0	PHY_WDQ_OSC_DELTA_0	R/W	0h	Slave delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 0.

4.4.115 DDRSS_PHY_114 Register (Offset = 41C8h) [reset = 0h]

DDRSS_PHY_114 is shown in [Figure 4-909](#) and described in [Table 4-1826](#).

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Table 4-1825. DDRSS_PHY_114 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41C8h

Figure 4-909. DDRSS_PHY_114 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1826. DDRSS_PHY_114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DQ_DM_SWIZZLE0_0	R/W	0h	DQ/DM bit swizzling 0 for slice 0. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0, Bits (7:4) inform the PHY which bit in {DM,DQ} map to DQ1, etc.

4.4.116 DDRSS_PHY_115 Register (Offset = 41CCh) [reset = X]

DDRSS_PHY_115 is shown in [Figure 4-910](#) and described in [Table 4-1828](#).

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Table 4-1827. DDRSS_PHY_115 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41CCh

Figure 4-910. DDRSS_PHY_115 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1828. DDRSS_PHY_115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PHY_DQ_DM_SWIZZLE1_0	R/W	0h	DQ/DM bit swizzling 1 for slice 0. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DM.

4.4.117 DDRSS_PHY_116 Register (Offset = 41D0h) [reset = X]

DDRSS_PHY_116 is shown in [Figure 4-911](#) and described in [Table 4-1830](#).

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Table 4-1829. DDRSS_PHY_116 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41D0h

Figure 4-911. DDRSS_PHY_116 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1830. DDRSS_PHY_116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ1_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ1 for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ0_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ0 for slice 0.

4.4.118 DDRSS_PHY_117 Register (Offset = 41D4h) [reset = X]

DDRSS_PHY_117 is shown in [Figure 4-912](#) and described in [Table 4-1832](#).

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Table 4-1831. DDRSS_PHY_117 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41D4h

Figure 4-912. DDRSS_PHY_117 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1832. DDRSS_PHY_117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ3_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ3 for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ2_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ2 for slice 0.

4.4.119 DDRSS_PHY_118 Register (Offset = 41D8h) [reset = X]

DDRSS_PHY_118 is shown in [Figure 4-913](#) and described in [Table 4-1834](#).

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Table 4-1833. DDRSS_PHY_118 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41D8h

Figure 4-913. DDRSS_PHY_118 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1834. DDRSS_PHY_118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ5_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ5 for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ4_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ4 for slice 0.

4.4.120 DDRSS_PHY_119 Register (Offset = 41DCh) [reset = X]

DDRSS_PHY_119 is shown in [Figure 4-914](#) and described in [Table 4-1836](#).

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Table 4-1835. DDRSS_PHY_119 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41DCh

Figure 4-914. DDRSS_PHY_119 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1836. DDRSS_PHY_119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ7_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ7 for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ6_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQ6 for slice 0.

4.4.121 DDRSS_PHY_120 Register (Offset = 41E0h) [reset = X]

DDRSS_PHY_120 is shown in [Figure 4-915](#) and described in [Table 4-1838](#).

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Table 4-1837. DDRSS_PHY_120 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41E0h

Figure 4-915. DDRSS_PHY_120 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_0									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_CLK_WRDM_SLAVE_DELAY_0									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1838. DDRSS_PHY_120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_CLK_WRDQS_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DQS for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDM_SLAVE_DELAY_0	R/W	0h	Write clock slave delay setting for DM for slice 0.

4.4.122 DDRSS_PHY_121 Register (Offset = 41E4h) [reset = X]

DDRSS_PHY_121 is shown in [Figure 4-916](#) and described in [Table 4-1840](#).

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Table 4-1839. DDRSS_PHY_121 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41E4h

Figure 4-916. DDRSS_PHY_121 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1840. DDRSS_PHY_121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ0 for slice 0.
7-2	RESERVED	R/W	X	
1-0	PHY_WRLVL_THRESHOLD_ADJUST_0	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 0.

4.4.123 DDRSS_PHY_122 Register (Offset = 41E8h) [reset = X]

DDRSS_PHY_122 is shown in [Figure 4-917](#) and described in [Table 4-1842](#).

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Table 4-1841. DDRSS_PHY_122 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41E8h

Figure 4-917. DDRSS_PHY_122 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1842. DDRSS_PHY_122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ1 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ0 for slice 0.

4.4.124 DDRSS_PHY_123 Register (Offset = 41ECh) [reset = X]

DDRSS_PHY_123 is shown in [Figure 4-918](#) and described in [Table 4-1844](#).

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Table 4-1843. DDRSS_PHY_123 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41ECh

Figure 4-918. DDRSS_PHY_123 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1844. DDRSS_PHY_123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ2 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ1 for slice 0.

4.4.125 DDRSS_PHY_124 Register (Offset = 41F0h) [reset = X]

DDRSS_PHY_124 is shown in [Figure 4-919](#) and described in [Table 4-1846](#).

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Table 4-1845. DDRSS_PHY_124 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41F0h

Figure 4-919. DDRSS_PHY_124 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1846. DDRSS_PHY_124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ3 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ2 for slice 0.

4.4.126 DDRSS_PHY_125 Register (Offset = 41F4h) [reset = X]

DDRSS_PHY_125 is shown in [Figure 4-920](#) and described in [Table 4-1848](#).

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Table 4-1847. DDRSS_PHY_125 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41F4h

Figure 4-920. DDRSS_PHY_125 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1848. DDRSS_PHY_125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ4 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ3 for slice 0.

4.4.127 DDRSS_PHY_126 Register (Offset = 41F8h) [reset = X]

DDRSS_PHY_126 is shown in [Figure 4-921](#) and described in [Table 4-1850](#).

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Table 4-1849. DDRSS_PHY_126 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41F8h

Figure 4-921. DDRSS_PHY_126 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1850. DDRSS_PHY_126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ5 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ4 for slice 0.

4.4.128 DDRSS_PHY_127 Register (Offset = 41FCh) [reset = X]

DDRSS_PHY_127 is shown in [Figure 4-922](#) and described in [Table 4-1852](#).

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Table 4-1851. DDRSS_PHY_127 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 41FCh

Figure 4-922. DDRSS_PHY_127 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1852. DDRSS_PHY_127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ6 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ5 for slice 0.

4.4.129 DDRSS_PHY_128 Register (Offset = 4200h) [reset = X]

DDRSS_PHY_128 is shown in [Figure 4-923](#) and described in [Table 4-1854](#).

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Table 4-1853. DDRSS_PHY_128 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4200h

Figure 4-923. DDRSS_PHY_128 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1854. DDRSS_PHY_128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DQ7 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ6 for slice 0.

4.4.130 DDRSS_PHY_129 Register (Offset = 4204h) [reset = X]

DDRSS_PHY_129 is shown in [Figure 4-924](#) and described in [Table 4-1856](#).

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Table 4-1855. DDRSS_PHY_129 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4204h

Figure 4-924. DDRSS_PHY_129 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DM_RISE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1856. DDRSS_PHY_129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	R/W	0h	Rising edge read DQS slave delay setting for DM for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DQ7 for slice 0.

4.4.131 DDRSS_PHY_130 Register (Offset = 4208h) [reset = X]

DDRSS_PHY_130 is shown in [Figure 4-925](#) and described in [Table 4-1858](#).

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Table 4-1857. DDRSS_PHY_130 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4208h

Figure 4-925. DDRSS_PHY_130 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1858. DDRSS_PHY_130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_GATE_SLAVE_DELAY_0	R/W	0h	Read DQS slave delay setting for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	R/W	0h	Falling edge read DQS slave delay setting for DM for slice 0.

4.4.132 DDRSS_PHY_131 Register (Offset = 420Ch) [reset = X]

DDRSS_PHY_131 is shown in [Figure 4-926](#) and described in [Table 4-1860](#).

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Table 4-1859. DDRSS_PHY_131 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 420Ch

Figure 4-926. DDRSS_PHY_131 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_DELAY_EARLY_THRESHOLD_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_WRITE_PATH_LAT_ADD_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_LATENCY_ADJUST_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1860. DDRSS_PHY_131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 0.
15-11	RESERVED	R/W	X	
10-8	PHY_WRITE_PATH_LAT_ADD_0	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_LATENCY_ADJUST_0	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 0.

4.4.133 DDRSS_PHY_132 Register (Offset = 4210h) [reset = X]

DDRSS_PHY_132 is shown in Figure 4-927 and described in Table 4-1862.

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Table 4-1861. DDRSS_PHY_132 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4210h

Figure 4-927. DDRSS_PHY_132 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_E ARLY_FORCE_ ZERO_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_ THRESHOLD_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1862. DDRSS_PHY_132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_WRLVL_EARLY_FORCE_ZERO_0	R/W	0h	Force the final write level delay value (that meets the early threshold) to 0 for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 0.

4.4.134 DDRSS_PHY_133 Register (Offset = 4214h) [reset = X]

DDRSS_PHY_133 is shown in Figure 4-928 and described in Table 4-1864.

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Table 4-1863. DDRSS_PHY_133 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4214h

Figure 4-928. DDRSS_PHY_133 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1864. DDRSS_PHY_133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_LAT_ADJ_START_0	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 0.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_RDDQS_SLV_DLY_START_0	R/W	0h	Initial read DQS gate slave delay setting during gate training for slice 0.

4.4.135 DDRSS_PHY_134 Register (Offset = 4218h) [reset = X]

DDRSS_PHY_134 is shown in Figure 4-929 and described in Table 4-1866.

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Table 4-1865. DDRSS_PHY_134 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4218h

Figure 4-929. DDRSS_PHY_134 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PAS S_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_NTP_WRLAT_START_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_START_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1866. DDRSS_PHY_134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_NTP_PASS_0	R/W	0h	Indicates if No-topology training found a passing result for slice 0.
23-20	RESERVED	R/W	X	
19-16	PHY_NTP_WRLAT_START_0	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_WDQLVL_DQDM_SLV_DLY_START_0	R/W	0h	Initial DQ/DM slave delay setting during write data leveling for slice 0.

4.4.136 DDRSS_PHY_135 Register (Offset = 421Ch) [reset = X]

DDRSS_PHY_135 is shown in [Figure 4-930](#) and described in [Table 4-1868](#).

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Table 4-1867. DDRSS_PHY_135 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 421Ch

Figure 4-930. DDRSS_PHY_135 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1868. DDRSS_PHY_135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	R/W	0h	Read leveling starting value for the DQS/DQ slave delay settings for slice 0.

4.4.137 DDRSS_PHY_136 Register (Offset = 4220h) [reset = 20202020h]

DDRSS_PHY_136 is shown in [Figure 4-931](#) and described in [Table 4-1870](#).

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Table 4-1869. DDRSS_PHY_136 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4220h

Figure 4-931. DDRSS_PHY_136 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_0							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ1_CLK_ADJUST_0							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ0_CLK_ADJUST_0							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_CLK_ADJUST_0							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1870. DDRSS_PHY_136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ2_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
23-16	PHY_DATA_DC_DQ1_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
15-8	PHY_DATA_DC_DQ0_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
7-0	PHY_DATA_DC_DQS_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.

4.4.138 DDRSS_PHY_137 Register (Offset = 4224h) [reset = 20202020h]

DDRSS_PHY_137 is shown in [Figure 4-932](#) and described in [Table 4-1872](#).

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Table 4-1871. DDRSS_PHY_137 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4224h

Figure 4-932. DDRSS_PHY_137 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ6_CLK_ADJUST_0							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ5_CLK_ADJUST_0							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ4_CLK_ADJUST_0							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ3_CLK_ADJUST_0							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1872. DDRSS_PHY_137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ6_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
23-16	PHY_DATA_DC_DQ5_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
15-8	PHY_DATA_DC_DQ4_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
7-0	PHY_DATA_DC_DQ3_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.

4.4.139 DDRSS_PHY_138 Register (Offset = 4228h) [reset = 2020h]

DDRSS_PHY_138 is shown in [Figure 4-933](#) and described in [Table 4-1874](#).

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Table 4-1873. DDRSS_PHY_138 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4228h

Figure 4-933. DDRSS_PHY_138 Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_0							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_0							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_0							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1874. DDRSS_PHY_138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_DSLICE_PAD_BOOSTPN_SETTING_0	R/W	0h	Setting for boost P/N of pad for slice 0.
15-8	PHY_DATA_DC_DM_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.
7-0	PHY_DATA_DC_DQ7_CLK_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 0.

4.4.140 DDRSS_PHY_139 Register (Offset = 422Ch) [reset = X]

DDRSS_PHY_139 is shown in [Figure 4-934](#) and described in [Table 4-1876](#).

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Table 4-1875. DDRSS_PHY_139 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 422Ch

Figure 4-934. DDRSS_PHY_139 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTL_SETTING_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1876. DDRSS_PHY_139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DQS_FFE_0	R/W	0h	TX_FFE setting for DQS pad for slice 0.
15-10	RESERVED	R/W	X	
9-8	PHY_DQ_FFE_0	R/W	0h	TX_FFE setting for DQ/DM pad for slice 0.
7-6	RESERVED	R/W	X	
5-0	PHY_DSLICE_PAD_RX_CTL_SETTING_0	R/W	0h	Setting for RX ctle P/N of pad for slice 0.

4.4.141 DDRSS_PHY_256 Register (Offset = 4400h) [reset = X]

DDRSS_PHY_256 is shown in [Figure 4-935](#) and described in [Table 4-1878](#).

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Table 4-1877. DDRSS_PHY_256 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4400h

Figure 4-935. DDRSS_PHY_256 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_1		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CLK_WR_BYPASS_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1878. DDRSS_PHY_256 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_IO_PAD_DELAY_TIMING_BYPASS_1	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WR_BYPASS_SLAVE_DELAY_1	R/W	0h	Write data clock bypass mode slave delay setting for slice 1.} PADDING_BEFORE

4.4.142 DDRSS_PHY_257 Register (Offset = 4404h) [reset = X]

DDRSS_PHY_257 is shown in [Figure 4-936](#) and described in [Table 4-1880](#).

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Table 4-1879. DDRSS_PHY_257 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4404h

Figure 4-936. DDRSS_PHY_257 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_1		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1880. DDRSS_PHY_257 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_WRITE_PATH_LAT_ADD_BYPASS_1	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_1	R/W	0h	Write DQS bypass mode slave delay setting for slice 1.

4.4.143 DDRSS_PHY_258 Register (Offset = 4408h) [reset = X]

DDRSS_PHY_258 is shown in Figure 4-937 and described in Table 4-1882.

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Table 4-1881. DDRSS_PHY_258 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4408h

Figure 4-937. DDRSS_PHY_258 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_BYPASS_TWO_CYCLE_PREAMBLE_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1882. DDRSS_PHY_258 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CLK_BYPASS_OVERRIDE_1	R/W	0h	Bypass mode override setting for slice 1.
23-18	RESERVED	R/W	X	
17-16	PHY_BYPASS_TWO_CYCLE_PREAMBLE_1	R/W	0h	Two_cycle_preamble for bypass mode for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1	R/W	0h	Read DQS bypass mode slave delay setting for slice 1.

4.4.144 DDRSS_PHY_259 Register (Offset = 440Ch) [reset = X]

DDRSS_PHY_259 is shown in Figure 4-938 and described in Table 4-1884.

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Table 4-1883. DDRSS_PHY_259 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 440Ch

Figure 4-938. DDRSS_PHY_259 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_1					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ2_SHIFT_1					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ1_SHIFT_1					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ0_SHIFT_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1884. DDRSS_PHY_259 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ3_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ2_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ1_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-1884. DDRSS_PHY_259 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ0_SHIF T_1	R/W	0h	<p>Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 1.</p> <p>Bit (0) enables override of half_cycle_shift.</p> <p>Bit (1) is the half_cycle_shift value.</p> <p>Bit (2) enables override of cycle shift.</p> <p>Bits (4:3) are the cycle_shift value.</p>

4.4.145 DDRSS_PHY_260 Register (Offset = 4410h) [reset = X]

DDRSS_PHY_260 is shown in [Figure 4-939](#) and described in [Table 4-1886](#).

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Table 4-1885. DDRSS_PHY_260 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4410h

Figure 4-939. DDRSS_PHY_260 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_1					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ6_SHIFT_1					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ5_SHIFT_1					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ4_SHIFT_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1886. DDRSS_PHY_260 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ7_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ6_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ5_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-1886. DDRSS_PHY_260 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ4_SHIF T_1	R/W	0h	<p>Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 1.</p> <p>Bit (0) enables override of half_cycle_shift.</p> <p>Bit (1) is the half_cycle_shift value.</p> <p>Bit (2) enables override of cycle shift.</p> <p>Bits (4:3) are the cycle_shift value.</p>

4.4.146 DDRSS_PHY_261 Register (Offset = 4414h) [reset = X]

DDRSS_PHY_261 is shown in Figure 4-940 and described in Table 4-1888.

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Table 4-1887. DDRSS_PHY_261 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4414h

Figure 4-940. DDRSS_PHY_261 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_1
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
RESERVED						PHY_PER_RANK_CS_MAP_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_WRDQS_SHIFT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDM_SHIFT_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1888. DDRSS_PHY_261 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_PER_CS_TRAINING_MULTICAST_EN_1	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 1. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PHY_PER_RANK_CS_MAP_1	R/W	0h	Per-rank CS map for slice 1. Setting a bit uses that CS for the rank, bit (0) uses CS0, bit (1) uses CS1, etc.
15-12	RESERVED	R/W	X	
11-8	PHY_SW_WRDQS_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bit (3) is the cycle_shift value.
7-6	RESERVED	R/W	X	

Table 4-1888. DDRSS_PHY_261 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PHY_SW_WRDM_SHIFT_1	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.147 DDRSS_PHY_262 Register (Offset = 4418h) [reset = X]

DDRSS_PHY_262 is shown in Figure 4-941 and described in Table 4-1890.

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Table 4-1889. DDRSS_PHY_262 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4418h

Figure 4-941. DDRSS_PHY_262 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_LP4_BOOT_RDDATA_EN_DLY_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_PER_CS_TRAINING_INDEX_1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1890. DDRSS_PHY_262 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1.
23-21	RESERVED	R/W	X	
20-16	PHY_LP4_BOOT_RDDATA_EN_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 1.
15-10	RESERVED	R/W	X	
9-8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_INDEX_1	R/W	0h	For per-rank training, indicates which rank's parameters are read/written for slice 1.

4.4.148 DDRSS_PHY_263 Register (Offset = 441Ch) [reset = X]

DDRSS_PHY_263 is shown in Figure 4-942 and described in Table 4-1892.

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Table 4-1891. DDRSS_PHY_263 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 441Ch

Figure 4-942. DDRSS_PHY_263 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_OE_DLY_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1892. DDRSS_PHY_263 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 1.
23-18	RESERVED	R/W	X	
17-16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_1	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 1. Bit (0): disable pull in wrdata_en Bit (1): disable write path clock gating, clock always on
15-12	RESERVED	R/W	X	
11-8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_1	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_LP4_BOOT_RPTR_UPDATE_1	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 1.

4.4.149 DDRSS_PHY_264 Register (Offset = 4420h) [reset = X]

DDRSS_PHY_264 is shown in [Figure 4-943](#) and described in [Table 4-1894](#).

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Table 4-1893. DDRSS_PHY_264 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4420h

Figure 4-943. DDRSS_PHY_264 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_LPBK_CONTROL_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_LPBK_CONTROL_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_CTRL_LPBK_EN_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1894. DDRSS_PHY_264 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LPBK_DFX_TIMEOUT_EN_1	R/W	0h	Loopback read only test timeout mechanism enable for slice 1.
23-17	RESERVED	R/W	X	
16-8	PHY_LPBK_CONTROL_1	R/W	0h	Loopback control bits for slice 1.
7-2	RESERVED	R/W	X	
1-0	PHY_CTRL_LPBK_EN_1	R/W	0h	Loopback control en for slice 1.

4.4.150 DDRSS_PHY_265 Register (Offset = 4424h) [reset = 0h]

DDRSS_PHY_265 is shown in [Figure 4-944](#) and described in [Table 4-1896](#).

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Table 4-1895. DDRSS_PHY_265 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4424h

Figure 4-944. DDRSS_PHY_265 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1896. DDRSS_PHY_265 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_AUTO_TIMING_MARGIN_CONTROL_1	R/W	0h	Auto timing marging control bits for slice 1.

4.4.151 DDRSS_PHY_266 Register (Offset = 4428h) [reset = X]

DDRSS_PHY_266 is shown in [Figure 4-945](#) and described in [Table 4-1898](#).

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Table 4-1897. DDRSS_PHY_266 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4428h

Figure 4-945. DDRSS_PHY_266 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_1																											
R-X				R-0h																											

LEGEND: R = Read Only; -n = value after reset

Table 4-1898. DDRSS_PHY_266 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-0	PHY_AUTO_TIMING_MARGIN_OBS_1	R	0h	Observation register for the auto_timing_margin for slice 1. READ-ONLY

4.4.152 DDRSS_PHY_267 Register (Offset = 442Ch) [reset = X]

DDRSS_PHY_267 is shown in Figure 4-946 and described in Table 4-1900.

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Table 4-1899. DDRSS_PHY_267 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 442Ch

Figure 4-946. DDRSS_PHY_267 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTIPATTERN_ENABLE_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_PRBS_PATTERN_MASK_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_PRBS_PATTERN_MASK_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PHY_PRBS_PATTERN_START_1						
R/W-X	R/W-1h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1900. DDRSS_PHY_267 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RDLVL_MULTIPATTERN_ENABLE_1	R/W	0h	Read Leveling Multi-pattern enable for slice 1.
23-17	RESERVED	R/W	X	
16-8	PHY_PRBS_PATTERN_MASK_1	R/W	0h	PRBS7 mask signal for slice 1.
7	RESERVED	R/W	X	
6-0	PHY_PRBS_PATTERN_START_1	R/W	1h	PRBS7 start pattern for slice 1.

4.4.153 DDRSS_PHY_268 Register (Offset = 4430h) [reset = X]

DDRSS_PHY_268 is shown in [Figure 4-947](#) and described in [Table 4-1902](#).

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Table 4-1901. DDRSS_PHY_268 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4430h

Figure 4-947. DDRSS_PHY_268 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PHY_VREF_TRAIN_OBS_1						
R/W-X	R-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_VREF_INITIAL_STEPSIZE_1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RDLVL_MULTIPATT_RST_DISABLE_1
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-1902. DDRSS_PHY_268 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	PHY_VREF_TRAIN_OBS_1	R	0h	Observation register for best vref value for slice 1. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	PHY_VREF_INITIAL_STEPSIZE_1	R/W	0h	Data slice initial VREF training step size for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_RDLVL_MULTIPATT_RST_DISABLE_1	R/W	0h	Read Leveling read level windows disable reset for slice 1.

4.4.154 DDRSS_PHY_269 Register (Offset = 4434h) [reset = X]

DDRSS_PHY_269 is shown in Figure 4-948 and described in Table 4-1904.

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Table 4-1903. DDRSS_PHY_269 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4434h

Figure 4-948. DDRSS_PHY_269 Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_SNAP_OBS_REGS_1
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1904. DDRSS_PHY_269 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SC_PHY_SNAP_OBS_REGS_1	W	0h	Initiates a snapshot of the internal observation registers for slice 1. Set to 1 to trigger. WRITE-ONLY
23-20	RESERVED	R/W	X	
19-16	PHY_GATE_ERROR_DELAY_SELECT_1	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	R/W	0h	Read DQS data clock bypass mode slave delay setting for slice 1.

4.4.155 DDRSS_PHY_270 Register (Offset = 4438h) [reset = X]

DDRSS_PHY_270 is shown in [Figure 4-949](#) and described in [Table 4-1906](#).

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Table 4-1905. DDRSS_PHY_270 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4438h

Figure 4-949. DDRSS_PHY_270 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MEM_CLASS_1		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							PHY_LPDDR_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1906. DDRSS_PHY_270 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_MEM_CLASS_1	R/W	0h	Indicates the type of DRAM for slice 1. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4
23-17	RESERVED	R/W	X	
16	PHY_LPDDR_1	R/W	0h	Adds a cycle of delay for the slice 1 to match the address slice. Set to 1 to add a cycle
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL1_SLAVE_DELAY_1	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 1.

4.4.156 DDRSS_PHY_271 Register (Offset = 443Ch) [reset = X]

DDRSS_PHY_271 is shown in Figure 4-950 and described in Table 4-1908.

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Table 4-1907. DDRSS_PHY_271 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 443Ch

Figure 4-950. DDRSS_PHY_271 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						ON_FLY_GATE_ADJUST_EN_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL2_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL2_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1908. DDRSS_PHY_271 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	ON_FLY_GATE_ADJUST_EN_1	R/W	0h	Control the on-the-fly gate adjustment for slice 1.
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL2_SLAVE_DELAY_1	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 1.

4.4.157 DDRSS_PHY_272 Register (Offset = 4440h) [reset = 0h]

DDRSS_PHY_272 is shown in [Figure 4-951](#) and described in [Table 4-1910](#).

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Table 4-1909. DDRSS_PHY_272 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4440h

Figure 4-951. DDRSS_PHY_272 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1910. DDRSS_PHY_272 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_GATE_TRACKING_OBS_1	R	0h	Report the on-the-fly gate measurement result for slice 1. READ-ONLY

4.4.158 DDRSS_PHY_273 Register (Offset = 4444h) [reset = X]

DDRSS_PHY_273 is shown in [Figure 4-952](#) and described in [Table 4-1912](#).

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Table 4-1911. DDRSS_PHY_273 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4444h

Figure 4-952. DDRSS_PHY_273 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1912. DDRSS_PHY_273 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-8	PHY_LP4_PST_AMBLE_1	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_DFI40_POLARITY_1	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 1.

4.4.159 DDRSS_PHY_274 Register (Offset = 4448h) [reset = 0h]

DDRSS_PHY_274 is shown in [Figure 4-953](#) and described in [Table 4-1914](#).

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Table 4-1913. DDRSS_PHY_274 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4448h

Figure 4-953. DDRSS_PHY_274 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1914. DDRSS_PHY_274 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT8_1	R/W	0h	Read leveling pattern 8 data for slice 1.

4.4.160 DDRSS_PHY_275 Register (Offset = 444Ch) [reset = 0h]

DDRSS_PHY_275 is shown in [Figure 4-954](#) and described in [Table 4-1916](#).

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Table 4-1915. DDRSS_PHY_275 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 444Ch

Figure 4-954. DDRSS_PHY_275 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1916. DDRSS_PHY_275 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT9_1	R/W	0h	Read leveling pattern 9 data for slice 1.

4.4.161 DDRSS_PHY_276 Register (Offset = 4450h) [reset = 0h]

DDRSS_PHY_276 is shown in [Figure 4-955](#) and described in [Table 4-1918](#).

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Table 4-1917. DDRSS_PHY_276 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4450h

Figure 4-955. DDRSS_PHY_276 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1918. DDRSS_PHY_276 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT10_1	R/W	0h	Read leveling pattern 10 data for slice 1.

4.4.162 DDRSS_PHY_277 Register (Offset = 4454h) [reset = 0h]

DDRSS_PHY_277 is shown in [Figure 4-956](#) and described in [Table 4-1920](#).

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Table 4-1919. DDRSS_PHY_277 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4454h

Figure 4-956. DDRSS_PHY_277 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1920. DDRSS_PHY_277 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT11_1	R/W	0h	Read leveling pattern 11 data for slice 1.

4.4.163 DDRSS_PHY_278 Register (Offset = 4458h) [reset = 0h]

DDRSS_PHY_278 is shown in [Figure 4-957](#) and described in [Table 4-1922](#).

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Table 4-1921. DDRSS_PHY_278 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4458h

Figure 4-957. DDRSS_PHY_278 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1922. DDRSS_PHY_278 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT12_1	R/W	0h	Read leveling pattern 12 data for slice 1.

4.4.164 DDRSS_PHY_279 Register (Offset = 445Ch) [reset = 0h]

DDRSS_PHY_279 is shown in [Figure 4-958](#) and described in [Table 4-1924](#).

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Table 4-1923. DDRSS_PHY_279 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 445Ch

Figure 4-958. DDRSS_PHY_279 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1924. DDRSS_PHY_279 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT13_1	R/W	0h	Read leveling pattern 13 data for slice 1.

4.4.165 DDRSS_PHY_280 Register (Offset = 4460h) [reset = 0h]

DDRSS_PHY_280 is shown in [Figure 4-959](#) and described in [Table 4-1926](#).

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Table 4-1925. DDRSS_PHY_280 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4460h

Figure 4-959. DDRSS_PHY_280 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1926. DDRSS_PHY_280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT14_1	R/W	0h	Read leveling pattern 14 data for slice 1.

4.4.166 DDRSS_PHY_281 Register (Offset = 4464h) [reset = 0h]

DDRSS_PHY_281 is shown in [Figure 4-960](#) and described in [Table 4-1928](#).

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Table 4-1927. DDRSS_PHY_281 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4464h

Figure 4-960. DDRSS_PHY_281 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1928. DDRSS_PHY_281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT15_1	R/W	0h	Read leveling pattern 15 data for slice 1.

4.4.167 DDRSS_PHY_282 Register (Offset = 4468h) [reset = X]

DDRSS_PHY_282 is shown in [Figure 4-961](#) and described in [Table 4-1930](#).

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Table 4-1929. DDRSS_PHY_282 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4468h

Figure 4-961. DDRSS_PHY_282 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_1		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_SELECT_1		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1930. DDRSS_PHY_282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_RDDQ_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ encoded slave delay observation register for slice 1.
23-20	RESERVED	R/W	X	
19-16	PHY_MASTER_DLY_LOCK_OBS_SELECT_1	R/W	0h	Select value to map the internal master delay observation registers to the accessible master delay observation register for slice 1.
15-9	RESERVED	R/W	X	
8	PHY_SW_FIFO_PTR_RST_DISABLE_1	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 1. Set to 1 to disable automatic resets.
7-3	RESERVED	R/W	X	
2-0	PHY_SLAVE_LOOP_CNT_UPDATE_1	R/W	0h	Reserved for future use for slice 1.

4.4.168 DDRSS_PHY_283 Register (Offset = 446Ch) [reset = X]

DDRSS_PHY_283 is shown in Figure 4-962 and described in Table 4-1932.

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Table 4-1931. DDRSS_PHY_283 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 446Ch

Figure 4-962. DDRSS_PHY_283 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1932. DDRSS_PHY_283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_FIFO_PTR_OBS_SELECT_1	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 1.
23-20	RESERVED	R/W	X	
19-16	PHY_WR_SHIFT_OBS_SELECT_1	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 1.
15-12	RESERVED	R/W	X	
11-8	PHY_WR_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ encoded slave delay observation register for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_DQ_ENC_OBS_SELECT_1	R/W	0h	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible read DQS DQ rise/fall encoded slave delay observation registers for slice 1.

4.4.169 DDRSS_PHY_284 Register (Offset = 4470h) [reset = X]

DDRSS_PHY_284 is shown in Figure 4-963 and described in Table 4-1934.

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Table 4-1933. DDRSS_PHY_284 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4470h

Figure 4-963. DDRSS_PHY_284 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_PER_START_1							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_ALGO_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_LVL_DEBUG_CONT_1
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LVL_DEBUG_MODE_1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1934. DDRSS_PHY_284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_PER_START_1	R/W	0h	Observation register for write leveling status for slice 1. READ-ONLY
23-18	RESERVED	R/W	X	
17-16	PHY_WRLVL_ALGO_1	R/W	0h	Write leveling algorithm selection for slice 1.
15-9	RESERVED	R/W	X	
8	SC_PHY_LVL_DEBUG_CONT_1	W	0h	Allows the leveling state machine to advance (when in debug mode) for slice 1. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_LVL_DEBUG_MODE_1	R/W	0h	Enables leveling debug mode for slice 1. Set to 1 to enable.

4.4.170 DDRSS_PHY_285 Register (Offset = 4474h) [reset = X]

DDRSS_PHY_285 is shown in [Figure 4-964](#) and described in [Table 4-1936](#).

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Table 4-1935. DDRSS_PHY_285 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4474h

Figure 4-964. DDRSS_PHY_285 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_DQ_MASK_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_CAPTURE_CNT_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1936. DDRSS_PHY_285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_DQ_MASK_1	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 1.
15-12	RESERVED	R/W	X	
11-8	PHY_WRLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during write leveling for slice 1.
7-6	RESERVED	R/W	X	
5-0	PHY_WRLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS slave delay setting during write leveling for slice 1.

4.4.171 DDRSS_PHY_286 Register (Offset = 4478h) [reset = X]

DDRSS_PHY_286 is shown in Figure 4-965 and described in Table 4-1938.

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Table 4-1937. DDRSS_PHY_286 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4478h

Figure 4-965. DDRSS_PHY_286 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_CAPTURE_CNT_1					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_PER_START_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_PER_START_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1938. DDRSS_PHY_286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_GTLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles + 4 to wait after changing DQS slave delay setting during gate training for slice 1. The valid range is 0x0 to 0xB.
23-22	RESERVED	R/W	X	
21-16	PHY_GTLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS slave delay setting during gate training for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_PER_START_1	R/W	0h	Value to be added to the current gate delay position as the starting point for periodic gate training for slice 1.

4.4.172 DDRSS_PHY_287 Register (Offset = 447Ch) [reset = X]

DDRSS_PHY_287 is shown in Figure 4-966 and described in Table 4-1940.

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Table 4-1939. DDRSS_PHY_287 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 447Ch

Figure 4-966. DDRSS_PHY_287 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_RDLVL_OP_MODE_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_RDLVL_CAPTURE_CNT_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1940. DDRSS_PHY_287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 1.
23-18	RESERVED	R/W	X	
17-16	PHY_RDLVL_OP_MODE_1	R/W	0h	Read leveling algorithm select for slice 1. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right.
15-12	RESERVED	R/W	X	
11-8	PHY_RDLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during read leveling for slice 1.
7-6	RESERVED	R/W	X	
5-0	PHY_RDLVL_CAPTURE_CNT_1	R/W	0h	Number of samples to take at each DQS slave delay setting during read leveling for slice 1.

4.4.173 DDRSS_PHY_288 Register (Offset = 4480h) [reset = X]

DDRSS_PHY_288 is shown in [Figure 4-967](#) and described in [Table 4-1942](#).

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Table 4-1941. DDRSS_PHY_288 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4480h

Figure 4-967. DDRSS_PHY_288 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_BURST_CNT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PHY_WDQLVL_CLK_JITTER_TOLERANCE_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_DATA_MASK_1							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_SELECT_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1942. DDRSS_PHY_288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_WDQLVL_BURST_CNT_1	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 1.
23-16	PHY_WDQLVL_CLK_JITTER_TOLERANCE_1	R/W	0h	Defines the minimum gap requirement for the LE and TE window for slice 1.
15-8	PHY_RDLVL_DATA_MASK_1	R/W	0h	Per-bit mask for read leveling for slice 1. If all bits are not used, only 1 bit should be cleared to 0.
7-0	PHY_RDLVL_PERIODIC_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during periodic read leveling for slice 1.

4.4.174 DDRSS_PHY_289 Register (Offset = 4484h) [reset = X]

DDRSS_PHY_289 is shown in [Figure 4-968](#) and described in [Table 4-1944](#).

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Table 4-1943. DDRSS_PHY_289 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4484h

Figure 4-968. DDRSS_PHY_289 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_PATT_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1944. DDRSS_PHY_289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_WDQLVL_UPDT_WAIT_CNT_1	R/W	0h	Number of cycles to wait after changing the DQ slave delay setting during write data leveling for slice 1.
23-19	RESERVED	R/W	X	
18-8	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 1.
7-3	RESERVED	R/W	X	
2-0	PHY_WDQLVL_PATT_1	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 1. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen.

4.4.175 DDRSS_PHY_290 Register (Offset = 4488h) [reset = X]

DDRSS_PHY_290 is shown in Figure 4-969 and described in Table 4-1946.

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Table 4-1945. DDRSS_PHY_290 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4488h

Figure 4-969. DDRSS_PHY_290 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_WDQ LVL_CLR_PRE V_RESULTS_1
R/W-X							W-0h
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_SELECT_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1946. DDRSS_PHY_290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	SC_PHY_WDQLVL_CLR_PREV_RESULTS_1	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 1. Set to 1 to trigger. WRITE-ONLY
15-8	PHY_WDQLVL_PERIODIC_OBS_SELECT_1	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_WDQLVL_DQDM_OBS_SELECT_1	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 1.

4.4.176 DDRSS_PHY_291 Register (Offset = 448Ch) [reset = X]

DDRSS_PHY_291 is shown in [Figure 4-970](#) and described in [Table 4-1948](#).

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Table 4-1947. DDRSS_PHY_291 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 448Ch

Figure 4-970. DDRSS_PHY_291 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_WDQLVL_DATADM_MASK_1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1948. DDRSS_PHY_291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_WDQLVL_DATADM_MASK_1	R/W	0h	Per-bit mask for write data leveling for slice 1. Set to 1 to mask any bit from the leveling process.

4.4.177 DDRSS_PHY_292 Register (Offset = 4490h) [reset = 0h]

DDRSS_PHY_292 is shown in [Figure 4-971](#) and described in [Table 4-1950](#).

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Table 4-1949. DDRSS_PHY_292 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4490h

Figure 4-971. DDRSS_PHY_292 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT0_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1950. DDRSS_PHY_292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT0_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 3 to 0 written/read from device.

4.4.178 DDRSS_PHY_293 Register (Offset = 4494h) [reset = 0h]

DDRSS_PHY_293 is shown in [Figure 4-972](#) and described in [Table 4-1952](#).

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Table 4-1951. DDRSS_PHY_293 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4494h

Figure 4-972. DDRSS_PHY_293 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT1_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1952. DDRSS_PHY_293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT1_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 7 to 4 written/read from device.

4.4.179 DDRSS_PHY_294 Register (Offset = 4498h) [reset = 0h]

DDRSS_PHY_294 is shown in [Figure 4-973](#) and described in [Table 4-1954](#).

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Table 4-1953. DDRSS_PHY_294 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4498h

Figure 4-973. DDRSS_PHY_294 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT2_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1954. DDRSS_PHY_294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT2_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 11 to 8 written/read from device.

4.4.180 DDRSS_PHY_295 Register (Offset = 449Ch) [reset = 0h]

DDRSS_PHY_295 is shown in [Figure 4-974](#) and described in [Table 4-1956](#).

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Table 4-1955. DDRSS_PHY_295 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 449Ch

Figure 4-974. DDRSS_PHY_295 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT3_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1956. DDRSS_PHY_295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT3_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 15 to 12 written/read from device.

4.4.181 DDRSS_PHY_296 Register (Offset = 44A0h) [reset = X]

DDRSS_PHY_296 is shown in [Figure 4-975](#) and described in [Table 4-1958](#).

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Table 4-1957. DDRSS_PHY_296 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44A0h

Figure 4-975. DDRSS_PHY_296 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_MULT_TRAIN_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_USER_PATT4_1							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT4_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1958. DDRSS_PHY_296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_NTP_MULT_TRAIN_1	R/W	0h	Control for single pass only No-Topology training for slice 1.
15-0	PHY_USER_PATT4_1	R/W	0h	User-defined pattern to be used during write data leveling for slice 1. This register holds the DM bit for the 15 to 0 DQ written/read from device.

4.4.182 DDRSS_PHY_297 Register (Offset = 44A4h) [reset = X]

DDRSS_PHY_297 is shown in Figure 4-976 and described in Table 4-1960.

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Table 4-1959. DDRSS_PHY_297 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44A4h

Figure 4-976. DDRSS_PHY_297 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_EARLY_THRESHOLD_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1960. DDRSS_PHY_297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_1	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_EARLY_THRESHOLD_1	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 1.

4.4.183 DDRSS_PHY_298 Register (Offset = 44A8h) [reset = X]

DDRSS_PHY_298 is shown in [Figure 4-977](#) and described in [Table 4-1962](#).

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Table 4-1961. DDRSS_PHY_298 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44A8h

Figure 4-977. DDRSS_PHY_298 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-1962. DDRSS_PHY_298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_MAX_1	R/W	0h	Maximum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_PERIOD_THRESHOLD_MIN_1	R/W	0h	Minimum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 1.

4.4.184 DDRSS_PHY_299 Register (Offset = 44ACh) [reset = X]

DDRSS_PHY_299 is shown in Figure 4-978 and described in Table 4-1964.

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Table 4-1963. DDRSS_PHY_299 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44ACh

Figure 4-978. DDRSS_PHY_299 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_1							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_1					
R/W-X		W-0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_1
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-1964. DDRSS_PHY_299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_FIFO_PTR_OBS_1	R	0h	Observation register containing read entry FIFO pointers for slice 1. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	SC_PHY_MANUAL_CLEAR_1	W	0h	Manual reset/clear of internal logic for slice 1. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/max lock values. Bit (3) is manual reset of master delay unlock counter. Bit (4) is reset of leveling error bit in the leveling status registers. Bit (5) is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_CALVL_VREF_DRIVING_SLICE_1	R/W	0h	Indicates if slice 1 is used to drive the VREF value to the device during CA training.

4.4.185 DDRSS_PHY_300 Register (Offset = 44B0h) [reset = 00100000h]

DDRSS_PHY_300 is shown in [Figure 4-979](#) and described in [Table 4-1966](#).

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Table 4-1965. DDRSS_PHY_300 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44B0h

Figure 4-979. DDRSS_PHY_300 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_1																															
R-00100000h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1966. DDRSS_PHY_300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_LPBK_RESULT_OBS_1	R	00100000h	Observation register containing loopback status/results for slice 1. READ-ONLY

4.4.186 DDRSS_PHY_301 Register (Offset = 44B4h) [reset = X]

DDRSS_PHY_301 is shown in [Figure 4-980](#) and described in [Table 4-1968](#).

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Table 4-1967. DDRSS_PHY_301 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44B4h

Figure 4-980. DDRSS_PHY_301 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_1										
R-X					R-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_ERROR_COUNT_OBS_1															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1968. DDRSS_PHY_301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_MASTER_DLY_LOCK_OBS_1	R	0h	Observation register containing master delay results for slice 1. READ-ONLY
15-0	PHY_LPBK_ERROR_COUNT_OBS_1	R	0h	Observation register containing total number of loopback error data for slice 1. READ-ONLY

4.4.187 DDRSS_PHY_302 Register (Offset = 44B8h) [reset = X]

DDRSS_PHY_302 is shown in Figure 4-981 and described in Table 4-1970.

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Table 4-1969. DDRSS_PHY_302 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44B8h

Figure 4-981. DDRSS_PHY_302 Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1							
R-0h							
23	22	21	20	19	18	17	16
PHY_MEAS_DLY_STEP_VALUE_1							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1						
R-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_1						
R-X	R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 4-1970. DDRSS_PHY_302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS DQ rising edge adder slave delay encoded value for slice 1. READ-ONLY
23-16	PHY_MEAS_DLY_STEP_VALUE_1	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with denominator of 512, for slice 1. READ-ONLY
15	RESERVED	R	X	
14-8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS base slave delay encoded value for slice 1. READ-ONLY
7	RESERVED	R	X	
6-0	PHY_RDDQ_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQ slave delay encoded values for slice 1. READ-ONLY

4.4.188 DDRSS_PHY_303 Register (Offset = 44BCh) [reset = X]

DDRSS_PHY_303 is shown in [Figure 4-982](#) and described in [Table 4-1972](#).

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Table 4-1971. DDRSS_PHY_303 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44BCh

Figure 4-982. DDRSS_PHY_303 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1						
R-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1		
R-X					R-0h		
15	14	13	12	11	10	9	8
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1							
R-0h							
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1972. DDRSS_PHY_303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	X	
30-24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write DQS base slave delay encoded value for slice 1. READ-ONLY
23-19	RESERVED	R	X	
18-8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS gate slave delay encoded value for slice 1. READ-ONLY
7-0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing read DQS DQ falling edge adder slave delay encoded value for slice 1. READ-ONLY

4.4.189 DDRSS_PHY_304 Register (Offset = 44C0h) [reset = X]

DDRSS_PHY_304 is shown in [Figure 4-983](#) and described in [Table 4-1974](#).

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Table 4-1973. DDRSS_PHY_304 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44C0h

Figure 4-983. DDRSS_PHY_304 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WR_SHIFT_OBS_1		
R-X					R-0h		
15	14	13	12	11	10	9	8
PHY_WR_ADDER_SLV_DLY_ENC_OBS_1							
R-0h							
7	6	5	4	3	2	1	0
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1974. DDRSS_PHY_304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18-16	PHY_WR_SHIFT_OBS_1	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 1. READ-ONLY
15-8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write adder slave delay encoded value for slice 1. READ-ONLY
7-0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing write DQ base slave delay encoded value for slice 1. READ-ONLY

4.4.190 DDRSS_PHY_305 Register (Offset = 44C4h) [reset = X]

DDRSS_PHY_305 is shown in [Figure 4-984](#) and described in [Table 4-1976](#).

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Table 4-1975. DDRSS_PHY_305 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44C4h

Figure 4-984. DDRSS_PHY_305 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_1									
R-X						R-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_1									
R-X						R-0h									

LEGEND: R = Read Only; -n = value after reset

Table 4-1976. DDRSS_PHY_305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_WRLVL_HARD1_DELAY_OBS_1	R	0h	Observation register containing write leveling first hard 1 DQS slave delay for slice 1. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_WRLVL_HARD0_DELAY_OBS_1	R	0h	Observation register containing write leveling last hard 0 DQS slave delay for slice 1. READ-ONLY

4.4.191 DDRSS_PHY_306 Register (Offset = 44C8h) [reset = X]

DDRSS_PHY_306 is shown in [Figure 4-985](#) and described in [Table 4-1978](#).

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Table 4-1977. DDRSS_PHY_306 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44C8h

Figure 4-985. DDRSS_PHY_306 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PHY_WRLVL_STATUS_OBS_1
R-X															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_1															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1978. DDRSS_PHY_306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-0	PHY_WRLVL_STATUS_OBS_1	R	0h	Observation register containing write leveling status for slice 1. READ-ONLY

4.4.192 DDRSS_PHY_307 Register (Offset = 44CCh) [reset = X]

DDRSS_PHY_307 is shown in [Figure 4-986](#) and described in [Table 4-1980](#).

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Table 4-1979. DDRSS_PHY_307 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44CCh

Figure 4-986. DDRSS_PHY_307 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1980. DDRSS_PHY_307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing gate sample2 slave delay encoded values for slice 1. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	R	0h	Observation register containing gate sample1 slave delay encoded values for slice 1. READ-ONLY

4.4.193 DDRSS_PHY_308 Register (Offset = 44D0h) [reset = X]

DDRSS_PHY_308 is shown in [Figure 4-987](#) and described in [Table 4-1982](#).

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Table 4-1981. DDRSS_PHY_308 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44D0h

Figure 4-987. DDRSS_PHY_308 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_1													
R-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_ERROR_OBS_1															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1982. DDRSS_PHY_308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-16	PHY_GTLVL_HARD0_DELAY_OBS_1	R	0h	Observation register containing gate training first hard 0 DQS slave delay for slice 1. READ-ONLY
15-0	PHY_WRLVL_ERROR_OBS_1	R	0h	Observation register containing write leveling error status for slice 1. READ-ONLY

4.4.194 DDRSS_PHY_309 Register (Offset = 44D4h) [reset = X]

DDRSS_PHY_309 is shown in [Figure 4-988](#) and described in [Table 4-1984](#).

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Table 4-1983. DDRSS_PHY_309 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44D4h

Figure 4-988. DDRSS_PHY_309 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_1													
R-X		R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 4-1984. DDRSS_PHY_309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	X	
13-0	PHY_GTLVL_HARD1_DELAY_OBS_1	R	0h	Observation register containing gate training last hard 1 DQS slave delay for slice 1. READ-ONLY

4.4.195 DDRSS_PHY_310 Register (Offset = 44D8h) [reset = X]

DDRSS_PHY_310 is shown in [Figure 4-989](#) and described in [Table 4-1986](#).

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Table 4-1985. DDRSS_PHY_310 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44D8h

Figure 4-989. DDRSS_PHY_310 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														PHY_GTLVL_STATUS_OBS_1	
R-X														R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_1															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-1986. DDRSS_PHY_310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	PHY_GTLVL_STATUS_OBS_1	R	0h	Observation register containing gate training status for slice 1. READ-ONLY

4.4.196 DDRSS_PHY_311 Register (Offset = 44DCh) [reset = X]

DDRSS_PHY_311 is shown in [Figure 4-990](#) and described in [Table 4-1988](#).

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Table 4-1987. DDRSS_PHY_311 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44DCh

Figure 4-990. DDRSS_PHY_311 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-1988. DDRSS_PHY_311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1	R	0h	Observation register containing read leveling data window trailing edge slave delay setting for slice 1. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	R	0h	Observation register containing read leveling data window leading edge slave delay setting for slice 1. READ-ONLY

4.4.197 DDRSS_PHY_312 Register (Offset = 44E0h) [reset = X]

DDRSS_PHY_312 is shown in [Figure 4-991](#) and described in [Table 4-1990](#).

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Table 4-1989. DDRSS_PHY_312 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44E0h

Figure 4-991. DDRSS_PHY_312 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-1990. DDRSS_PHY_312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1-0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	R	0h	Observation register containing read leveling number of windows found for slice 1. READ-ONLY

4.4.198 DDRSS_PHY_313 Register (Offset = 44E4h) [reset = 0h]

DDRSS_PHY_313 is shown in [Figure 4-992](#) and described in [Table 4-1992](#).

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Table 4-1991. DDRSS_PHY_313 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44E4h

Figure 4-992. DDRSS_PHY_313 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1992. DDRSS_PHY_313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_STATUS_OBS_1	R	0h	Observation register containing read leveling status for slice 1. READ-ONLY

4.4.199 DDRSS_PHY_314 Register (Offset = 44E8h) [reset = 0h]

DDRSS_PHY_314 is shown in [Figure 4-993](#) and described in [Table 4-1994](#).

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Table 4-1993. DDRSS_PHY_314 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44E8h

Figure 4-993. DDRSS_PHY_314 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1994. DDRSS_PHY_314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PERIODIC_OBS_1	R	0h	Observation register containing periodic read leveling status for slice 1. READ-ONLY

4.4.200 DDRSS_PHY_315 Register (Offset = 44ECh) [reset = X]

DDRSS_PHY_315 is shown in [Figure 4-994](#) and described in [Table 4-1996](#).

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Table 4-1995. DDRSS_PHY_315 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44ECh

Figure 4-994. DDRSS_PHY_315 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_1										
R-X					R-7FFh										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_1										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 4-1996. DDRSS_PHY_315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_WDQLVL_DQDM_TE_DLY_OBS_1	R	7FFh	Observation register containing write data leveling data window trailing edge slave delay setting for slice 1. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_WDQLVL_DQDM_LE_DLY_OBS_1	R	0h	Observation register containing write data leveling data window leading edge slave delay setting for slice 1. READ-ONLY

4.4.201 DDRSS_PHY_316 Register (Offset = 44F0h) [reset = 0h]

DDRSS_PHY_316 is shown in [Figure 4-995](#) and described in [Table 4-1998](#).

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Table 4-1997. DDRSS_PHY_316 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44F0h

Figure 4-995. DDRSS_PHY_316 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-1998. DDRSS_PHY_316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_STATUS_OBS_1	R	0h	Observation register containing write data leveling status for slice 1. READ-ONLY

4.4.202 DDRSS_PHY_317 Register (Offset = 44F4h) [reset = 0h]

DDRSS_PHY_317 is shown in [Figure 4-996](#) and described in [Table 4-2000](#).

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Table 4-1999. DDRSS_PHY_317 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44F4h

Figure 4-996. DDRSS_PHY_317 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2000. DDRSS_PHY_317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_PERIODIC_OBS_1	R	0h	Observation register containing periodic write data leveling status for slice 1. READ-ONLY

4.4.203 DDRSS_PHY_318 Register (Offset = 44F8h) [reset = X]

DDRSS_PHY_318 is shown in [Figure 4-997](#) and described in [Table 4-2002](#).

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Table 4-2001. DDRSS_PHY_318 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44F8h

Figure 4-997. DDRSS_PHY_318 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	PHY_DDL_MODE_1																														
R/W-X	R/W-0h																														

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2002. DDRSS_PHY_318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-0	PHY_DDL_MODE_1	R/W	0h	DDL mode for slice 1.

4.4.204 DDRSS_PHY_319 Register (Offset = 44FCh) [reset = X]

DDRSS_PHY_319 is shown in [Figure 4-998](#) and described in [Table 4-2004](#).

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Table 4-2003. DDRSS_PHY_319 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 44FCh

Figure 4-998. DDRSS_PHY_319 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PHY_DDL_MASK_1					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2004. DDRSS_PHY_319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	PHY_DDL_MASK_1	R/W	0h	DDL mask for slice 1.

4.4.205 DDRSS_PHY_320 Register (Offset = 4500h) [reset = 0h]

DDRSS_PHY_320 is shown in [Figure 4-999](#) and described in [Table 4-2006](#).

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Table 4-2005. DDRSS_PHY_320 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4500h

Figure 4-999. DDRSS_PHY_320 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2006. DDRSS_PHY_320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_OBS_1	R	0h	DDL test observation for slice 1. READ-ONLY

4.4.206 DDRSS_PHY_321 Register (Offset = 4504h) [reset = 0h]

DDRSS_PHY_321 is shown in [Figure 4-1000](#) and described in [Table 4-2008](#).

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Table 4-2007. DDRSS_PHY_321 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4504h

Figure 4-1000. DDRSS_PHY_321 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2008. DDRSS_PHY_321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_MSTR_DLY_OBS_1	R	0h	DDL test observation delays for slice 1 master DDL. READ-ONLY

4.4.207 DDRSS_PHY_322 Register (Offset = 4508h) [reset = X]

DDRSS_PHY_322 is shown in [Figure 4-1001](#) and described in [Table 4-2010](#).

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Table 4-2009. DDRSS_PHY_322 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4508h

Figure 4-1001. DDRSS_PHY_322 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_OVERRIDE_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_RX_CAL_START_1
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2010. DDRSS_PHY_322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_OVERRIDE_1	R/W	0h	Manual setting of RX Calibration enable for slice 1.
23-17	RESERVED	R/W	X	
16	SC_PHY_RX_CAL_START_1	W	0h	Manual RX Calibration start for slice 1. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	PHY_LP4_WDQS_OE_EXTEND_1	R/W	0h	LPDDR4 write preamble extension enable for slice 1.
7-0	PHY_DDL_TRACK_UPD_THRESHOLD_1	R/W	0h	Specify threshold value for PHY init update tracking for slice 1.

4.4.208 DDRSS_PHY_323 Register (Offset = 450Ch) [reset = X]

DDRSS_PHY_323 is shown in Figure 4-1002 and described in Table 4-2012.

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Table 4-2011. DDRSS_PHY_323 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 450Ch

Figure 4-1002. DDRSS_PHY_323 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_SAMPLE_WAIT_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2012. DDRSS_PHY_323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ0_1	R/W	0h	RX Calibration codes for DQ0 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8	PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_1	R/W	0h	Data slice power reduction disable for slice 1.
7-0	PHY_RX_CAL_SAMPLE_WAIT_1	R/W	0h	RX Calibration state machine wait count for slice 1.

4.4.209 DDRSS_PHY_324 Register (Offset = 4510h) [reset = X]

DDRSS_PHY_324 is shown in Figure 4-1003 and described in Table 4-2014.

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Table 4-2013. DDRSS_PHY_324 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4510h

Figure 4-1003. DDRSS_PHY_324 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ2_1							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ1_1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2014. DDRSS_PHY_324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ2_1	R/W	0h	RX Calibration codes for DQ2 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ1_1	R/W	0h	RX Calibration codes for DQ1 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.210 DDRSS_PHY_325 Register (Offset = 4514h) [reset = X]

DDRSS_PHY_325 is shown in Figure 4-1004 and described in Table 4-2016.

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Table 4-2015. DDRSS_PHY_325 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4514h

Figure 4-1004. DDRSS_PHY_325 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ4_1							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ3_1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2016. DDRSS_PHY_325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ4_1	R/W	0h	RX Calibration codes for DQ4 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ3_1	R/W	0h	RX Calibration codes for DQ3 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.211 DDRSS_PHY_326 Register (Offset = 4518h) [reset = X]

DDRSS_PHY_326 is shown in [Figure 4-1005](#) and described in [Table 4-2018](#).

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Table 4-2017. DDRSS_PHY_326 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4518h

Figure 4-1005. DDRSS_PHY_326 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ6_1							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ5_1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2018. DDRSS_PHY_326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ6_1	R/W	0h	RX Calibration codes for DQ6 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ5_1	R/W	0h	RX Calibration codes for DQ5 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.212 DDRSS_PHY_327 Register (Offset = 451Ch) [reset = X]

DDRSS_PHY_327 is shown in [Figure 4-1006](#) and described in [Table 4-2020](#).

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Table 4-2019. DDRSS_PHY_327 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 451Ch

Figure 4-1006. DDRSS_PHY_327 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ7_1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2020. DDRSS_PHY_327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ7_1	R/W	0h	RX Calibration codes for DQ7 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.213 DDRSS_PHY_328 Register (Offset = 4520h) [reset = X]

DDRSS_PHY_328 is shown in [Figure 4-1007](#) and described in [Table 4-2022](#).

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Table 4-2021. DDRSS_PHY_328 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4520h

Figure 4-1007. DDRSS_PHY_328 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_RX_CAL_DM_1																	
R/W-X														R/W-0h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2022. DDRSS_PHY_328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_RX_CAL_DM_1	R/W	0h	RX Calibration codes for DM for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.214 DDRSS_PHY_329 Register (Offset = 4524h) [reset = X]

DDRSS_PHY_329 is shown in [Figure 4-1008](#) and described in [Table 4-2024](#).

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Table 4-2023. DDRSS_PHY_329 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4524h

Figure 4-1008. DDRSS_PHY_329 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_FDBK_1							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQS_1							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2024. DDRSS_PHY_329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_FDBK_1	R/W	0h	RX Calibration codes for FDBK for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQS_1	R/W	0h	RX Calibration codes for DQS for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.215 DDRSS_PHY_330 Register (Offset = 4528h) [reset = X]

DDRSS_PHY_330 is shown in [Figure 4-1009](#) and described in [Table 4-2026](#).

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Table 4-2025. DDRSS_PHY_330 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4528h

Figure 4-1009. DDRSS_PHY_330 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_LOCK_OBS_1							
R-X								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_OBS_1							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2026. DDRSS_PHY_330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	X	
24-16	PHY_RX_CAL_LOCK_OBS_1	R	0h	RX Calibration lock results for slice 1. Bit (3:0) is the state machine rx_cal_sm. Bit (4) is the rx_cal_done signal. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_RX_CAL_OBS_1	R	0h	RX Calibration results for slice 1. Bits (7:0) contain calibration results from DQ 0-7. Bit (8) contains calibration result from DM. Bit (9) contains calibration result from DQS. Bit (10) contains calibration result from FDBK. READ-ONLY

4.4.216 DDRSS_PHY_331 Register (Offset = 452Ch) [reset = X]

DDRSS_PHY_331 is shown in Figure 4-1010 and described in Table 4-2028.

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Table 4-2027. DDRSS_PHY_331 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 452Ch

Figure 4-1010. DDRSS_PHY_331 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_COMP_VAL_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED	PHY_RX_CAL_DIFF_ADJUST_1						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_RX_CAL_SE_ADJUST_1						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RX_CAL_DISABLE_1
R/W-X							R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2028. DDRSS_PHY_331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_COMP_VAL_1	R/W	0h	Expected C value from RX pad for slice 1.
23	RESERVED	R/W	X	
22-16	PHY_RX_CAL_DIFF_ADJUST_1	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 1.
15	RESERVED	R/W	X	
14-8	PHY_RX_CAL_SE_ADJUST_1	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_RX_CAL_DISABLE_1	R/W	1h	RX CAL disable signal for slice 1, set 1 to bypass the rx calibration

4.4.217 DDRSS_PHY_332 Register (Offset = 4530h) [reset = X]

DDRSS_PHY_332 is shown in [Figure 4-1011](#) and described in [Table 4-2030](#).

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Table 4-2029. DDRSS_PHY_332 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4530h

Figure 4-1011. DDRSS_PHY_332 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_PAD_RX_BIAS_EN_1										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_RX_CAL_INDEX_MASK_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2030. DDRSS_PHY_332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PAD_RX_BIAS_EN_1	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 1.
15-12	RESERVED	R/W	X	
11-0	PHY_RX_CAL_INDEX_MASK_1	R/W	0h	RX offset calibration mask of all RX pad for slice 1.

4.4.218 DDRSS_PHY_333 Register (Offset = 4534h) [reset = X]

DDRSS_PHY_333 is shown in [Figure 4-1012](#) and described in [Table 4-2032](#).

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Table 4-2031. DDRSS_PHY_333 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4534h

Figure 4-1012. DDRSS_PHY_333 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_DATA_DC_WEIGHT_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DATA_DC_CAL_TIMEOUT_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_CAL_SAMPLE_WAIT_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_STATIC_TOG_DISABLE_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2032. DDRSS_PHY_333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_DATA_DC_WEIGHT_1	R/W	0h	Determines weight of average calculating for slice 1.
23-16	PHY_DATA_DC_CAL_TIMEOUT_1	R/W	0h	Determines timeout number of iteration for slice 1.
15-8	PHY_DATA_DC_CAL_SAMPLE_WAIT_1	R/W	0h	Determines number of cycles to wait for each sample for slice 1.
7-5	RESERVED	R/W	X	
4-0	PHY_STATIC_TOG_DISABLE_1	R/W	0h	Control to disable toggle during static activity for slice 1. bit 0: Write path delay line disable bit 1: Read path delay line disable bit 2: Read data path disable bit 3: clk_phy disable bit 4: master delay line disable.

4.4.219 DDRSS_PHY_334 Register (Offset = 4538h) [reset = X]

DDRSS_PHY_334 is shown in [Figure 4-1013](#) and described in [Table 4-2034](#).

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Table 4-2033. DDRSS_PHY_334 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4538h

Figure 4-1013. DDRSS_PHY_334 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_DATA_DC_ADJUST_THRSHLD_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_ADJUST_SAMPLE_CNT_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DATA_DC_ADJUST_START_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2034. DDRSS_PHY_334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_DATA_DC_ADJUST_DIRECT_1	R/W	0h	Adjust direction for slice 1.
23-16	PHY_DATA_DC_ADJUST_THRSHLD_1	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 1.
15-8	PHY_DATA_DC_ADJUST_SAMPLE_CNT_1	R/W	0h	Duty cycle adjust sample count for slice 1.
7-6	RESERVED	R/W	X	
5-0	PHY_DATA_DC_ADJUST_START_1	R/W	0h	Duty cycle adjust starting value for slice 1.

4.4.220 DDRSS_PHY_335 Register (Offset = 453Ch) [reset = X]

DDRSS_PHY_335 is shown in Figure 4-1014 and described in Table 4-2036.

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Table 4-2035. DDRSS_PHY_335 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 453Ch

Figure 4-1014. DDRSS_PHY_335 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_FDBK_PWR_CTRL_1		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_SW_RANK_1	
R/W-X						R/W-1h	
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_CAL_START_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_CAL_POLARITY_1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2036. DDRSS_PHY_335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_FDBK_PWR_CTRL_1	R/W	0h	Shutoff gate feedback IO to reduce power for slice 1.
23-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_SW_RANK_1	R/W	1h	Rank selection for software based duty cycle correction for slice 1.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_CAL_START_1	R/W	0h	Manual trigger for DCC for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_CAL_POLARITY_1	R/W	0h	Calibration polarity for slice 1.

4.4.221 DDRSS_PHY_336 Register (Offset = 4540h) [reset = X]

DDRSS_PHY_336 is shown in [Figure 4-1015](#) and described in [Table 4-2038](#).

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Table 4-2037. DDRSS_PHY_336 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4540h

Figure 4-1015. DDRSS_PHY_336 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_RDPATH_GATE_DISABLE_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2038. DDRSS_PHY_336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SLICE_PWR_RDC_DISABLE_1	R/W	0h	Data slice power reduction disable for slice 1.
23-17	RESERVED	R/W	X	
16	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_1	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 1.
15-9	RESERVED	R/W	X	
8	PHY_RDPATH_GATE_DISABLE_1	R/W	0h	Data slice read path power reduction disable for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_SLV_DLY_CTRL_GATE_DISABLE_1	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 1.

4.4.222 DDRSS_PHY_337 Register (Offset = 4544h) [reset = X]

DDRSS_PHY_337 is shown in [Figure 4-1016](#) and described in [Table 4-2040](#).

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Table 4-2039. DDRSS_PHY_337 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4544h

Figure 4-1016. DDRSS_PHY_337 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_DS_FSM_ERROR_INFO_1													
R/W-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_PARITY_ERROR_REGIF_1										
R/W-X					R/W-0h										

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2040. DDRSS_PHY_337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_DS_FSM_ERROR_INFO_1	R	0h	Data slice level FSM Error Info for slice 1. READ-ONLY
15-11	RESERVED	R/W	X	
10-0	PHY_PARITY_ERROR_REGIF_1	R/W	0h	Inject parity error to register interface signals for slice 1.

4.4.223 DDRSS_PHY_338 Register (Offset = 4548h) [reset = X]

DDRSS_PHY_338 is shown in [Figure 4-1017](#) and described in [Table 4-2042](#).

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Table 4-2041. DDRSS_PHY_338 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4548h

Figure 4-1017. DDRSS_PHY_338 Register

31	30	29	28	27	26	25	24
RESERVED		SC_PHY_DS_FSM_ERROR_INFO_WOCLR_1					
R/W-X		W-0h					
23	22	21	20	19	18	17	16
SC_PHY_DS_FSM_ERROR_INFO_WOCLR_1							
W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_DS_FSM_ERROR_INFO_MASK_1					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
PHY_DS_FSM_ERROR_INFO_MASK_1							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2042. DDRSS_PHY_338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	SC_PHY_DS_FSM_ERROR_INFO_WOCLR_1	W	0h	Data slice level FSM Error Info for slice 1. WRITE-ONLY
15-14	RESERVED	R/W	X	
13-0	PHY_DS_FSM_ERROR_INFO_MASK_1	R/W	0h	Data slice level FSM Error Info Mask for slice 1.

4.4.224 DDRSS_PHY_339 Register (Offset = 454Ch) [reset = X]

DDRSS_PHY_339 is shown in [Figure 4-1018](#) and described in [Table 4-2044](#).

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Table 4-2043. DDRSS_PHY_339 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 454Ch

Figure 4-1018. DDRSS_PHY_339 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_1			
R/W-X				W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_1			
R/W-X				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2044. DDRSS_PHY_339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_1	W	0h	Data slice level training/calibration Error Info for slice 1. WRITE-ONLY
15-13	RESERVED	R/W	X	
12-8	PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_1	R/W	0h	Data slice level training/calibration Error Info Mask for slice 1.
7-5	RESERVED	R/W	X	
4-0	PHY_DS_TRAIN_CALIB_ERROR_INFO_1	R	0h	Data slice level training/calibration Error Info for slice 1. READ-ONLY

4.4.225 DDRSS_PHY_340 Register (Offset = 4550h) [reset = X]

DDRSS_PHY_340 is shown in [Figure 4-1019](#) and described in [Table 4-2046](#).

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Table 4-2045. DDRSS_PHY_340 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4550h

Figure 4-1019. DDRSS_PHY_340 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_1		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DQ_TSEL_SELECT_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_TSEL_SELECT_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_DQ_TSEL_ENABLE_1		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2046. DDRSS_PHY_340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_DQS_TSEL_ENABLE_1	R/W	0h	Operation type tsel enables for DQS signals for slice 1. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.
23-8	PHY_DQ_TSEL_SELECT_1	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 1.
7-3	RESERVED	R/W	X	
2-0	PHY_DQ_TSEL_ENABLE_1	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 1. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.

4.4.226 DDRSS_PHY_341 Register (Offset = 4554h) [reset = X]

DDRSS_PHY_341 is shown in Figure 4-1020 and described in Table 4-2048.

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Table 4-2047. DDRSS_PHY_341 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4554h

Figure 4-1020. DDRSS_PHY_341 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_1						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_1							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2048. DDRSS_PHY_341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PHY_VREF_INITIAL_START_POINT_1	R/W	0h	Data slice initial VREF training start value for slice 1.
23-18	RESERVED	R/W	X	
17-16	PHY_TWO_CYC_PREAMBLE_1	R/W	0h	2 cycle preamble support for slice 1. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2 cycle write preamble. Set each bit to 1 to enable.
15-0	PHY_DQS_TSEL_SELECT_1	R/W	0h	Operation type tsel select values for DQS signals for slice 1.

4.4.227 DDRSS_PHY_342 Register (Offset = 4558h) [reset = X]

DDRSS_PHY_342 is shown in [Figure 4-1021](#) and described in [Table 4-2050](#).

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Table 4-2049. DDRSS_PHY_342 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4558h

Figure 4-1021. DDRSS_PHY_342 Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_1							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_1						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2050. DDRSS_PHY_342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_NTP_WDQ_STEP_SIZE_1	R/W	0h	Step size of WR DQ slave delay during No-Topology training for slice 1.
23-17	RESERVED	R/W	X	
16	PHY_NTP_TRAIN_EN_1	R/W	0h	Enable for No-Topology training for slice 1.
15-10	RESERVED	R/W	X	
9-8	PHY_VREF_TRAINING_CTRL_1	R/W	0h	Data slice vref training enable control for slice 1.
7	RESERVED	R/W	X	
6-0	PHY_VREF_INITIAL_STOP_POINT_1	R/W	0h	Data slice initial VREF training stop value for slice 1.

4.4.228 DDRSS_PHY_343 Register (Offset = 455Ch) [reset = X]

DDRSS_PHY_343 is shown in [Figure 4-1022](#) and described in [Table 4-2052](#).

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Table 4-2051. DDRSS_PHY_343 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 455Ch

Figure 4-1022. DDRSS_PHY_343 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_NTP_WDQ_STOP_1										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_NTP_WDQ_START_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2052. DDRSS_PHY_343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_NTP_WDQ_STOP_1	R/W	0h	End of WR DQ slave delay in No-Topology training for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_NTP_WDQ_START_1	R/W	0h	Starting WR DQ slave delay in No-Topology training for slice 1.

4.4.229 DDRSS_PHY_344 Register (Offset = 4560h) [reset = X]

DDRSS_PHY_344 is shown in [Figure 4-1023](#) and described in [Table 4-2054](#).

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Table 4-2053. DDRSS_PHY_344 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4560h

Figure 4-1023. DDRSS_PHY_344 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_WDQLVL_DVW_MIN_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_WDQLVL_DVW_MIN_1							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_BIT_EN_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2054. DDRSS_PHY_344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SW_WDQLVL_DVW_MIN_EN_1	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 1.
23-18	RESERVED	R/W	X	
17-8	PHY_WDQLVL_DVW_MIN_1	R/W	0h	Minimum data valid window across DQs and ranks for slice 1.
7-0	PHY_NTP_WDQ_BIT_EN_1	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 1.

4.4.230 DDRSS_PHY_345 Register (Offset = 4564h) [reset = X]

DDRSS_PHY_345 is shown in [Figure 4-1024](#) and described in [Table 4-2056](#).

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Table 4-2055. DDRSS_PHY_345 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4564h

Figure 4-1024. DDRSS_PHY_345 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_0_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_TX_DCD_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2056. DDRSS_PHY_345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_0_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_TX_DCD_1	R/W	0h	Controls TX_DCD pin for each pad for slice 1.
15-12	RESERVED	R/W	X	
11-8	PHY_FAST_LVL_EN_1	R/W	0h	Enable for fast multi-pattern window search for slice 1.
7-6	RESERVED	R/W	X	
5-0	PHY_WDQLVL_PER_START_OFFSET_1	R/W	0h	Periodic training start point offset for slice 1.

4.4.231 DDRSS_PHY_346 Register (Offset = 4568h) [reset = X]

DDRSS_PHY_346 is shown in [Figure 4-1025](#) and described in [Table 4-2058](#).

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Table 4-2057. DDRSS_PHY_346 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4568h

Figure 4-1025. DDRSS_PHY_346 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_4_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_3_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_2_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_1_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2058. DDRSS_PHY_346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_4_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_3_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_2_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_1_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.

4.4.232 DDRSS_PHY_347 Register (Offset = 456Ch) [reset = X]

DDRSS_PHY_347 is shown in [Figure 4-1026](#) and described in [Table 4-2060](#).

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Table 4-2059. DDRSS_PHY_347 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 456Ch

Figure 4-1026. DDRSS_PHY_347 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_DM_RX_DCD_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_7_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_6_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_5_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2060. DDRSS_PHY_347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_DM_RX_DCD_1	R/W	0h	Controls RX_DCD pin for dm pad for slice 1.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_7_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_6_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_5_1	R/W	0h	Controls RX_DCD pin for each pad for slice 1.

4.4.233 DDRSS_PHY_348 Register (Offset = 4570h) [reset = X]

DDRSS_PHY_348 is shown in [Figure 4-1027](#) and described in [Table 4-2062](#).

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Table 4-2061. DDRSS_PHY_348 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4570h

Figure 4-1027. DDRSS_PHY_348 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PHY_PAD_DSLICE_IO_CFG_1					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_1				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_1				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2062. DDRSS_PHY_348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PHY_PAD_DSLICE_IO_CFG_1	R/W	0h	Controls PCLK/PARK pin for pad for slice 1.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_FDBK_RX_DCD_1	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 1.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_DQS_RX_DCD_1	R/W	0h	Controls RX_DCD pin for dqs pad for slice 1.

4.4.234 DDRSS_PHY_349 Register (Offset = 4574h) [reset = X]

DDRSS_PHY_349 is shown in [Figure 4-1028](#) and described in [Table 4-2064](#).

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Table 4-2063. DDRSS_PHY_349 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4574h

Figure 4-1028. DDRSS_PHY_349 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ1_SLAVE_DELAY_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ0_SLAVE_DELAY_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2064. DDRSS_PHY_349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ1_SLAVE_DELAY_1	R/W	0h	Read DQ1 slave delay setting for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ0_SLAVE_DELAY_1	R/W	0h	Read DQ0 slave delay setting for slice 1.

4.4.235 DDRSS_PHY_350 Register (Offset = 4578h) [reset = X]

DDRSS_PHY_350 is shown in [Figure 4-1029](#) and described in [Table 4-2066](#).

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Table 4-2065. DDRSS_PHY_350 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4578h

Figure 4-1029. DDRSS_PHY_350 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ3_SLAVE_DELAY_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ2_SLAVE_DELAY_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2066. DDRSS_PHY_350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ3_SLAVE_DELAY_1	R/W	0h	Read DQ3 slave delay setting for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ2_SLAVE_DELAY_1	R/W	0h	Read DQ2 slave delay setting for slice 1.

4.4.236 DDRSS_PHY_351 Register (Offset = 457Ch) [reset = X]

DDRSS_PHY_351 is shown in [Figure 4-1030](#) and described in [Table 4-2068](#).

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Table 4-2067. DDRSS_PHY_351 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 457Ch

Figure 4-1030. DDRSS_PHY_351 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ5_SLAVE_DELAY_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ4_SLAVE_DELAY_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2068. DDRSS_PHY_351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ5_SLAVE_DELAY_1	R/W	0h	Read DQ5 slave delay setting for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ4_SLAVE_DELAY_1	R/W	0h	Read DQ4 slave delay setting for slice 1.

4.4.237 DDRSS_PHY_352 Register (Offset = 4580h) [reset = X]

DDRSS_PHY_352 is shown in [Figure 4-1031](#) and described in [Table 4-2070](#).

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Table 4-2069. DDRSS_PHY_352 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4580h

Figure 4-1031. DDRSS_PHY_352 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ7_SLAVE_DELAY_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ6_SLAVE_DELAY_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2070. DDRSS_PHY_352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ7_SLAVE_DELAY_1	R/W	0h	Read DQ7 slave delay setting for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ6_SLAVE_DELAY_1	R/W	0h	Read DQ6 slave delay setting for slice 1.

4.4.238 DDRSS_PHY_353 Register (Offset = 4584h) [reset = X]

DDRSS_PHY_353 is shown in [Figure 4-1032](#) and described in [Table 4-2072](#).

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Table 4-2071. DDRSS_PHY_353 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4584h

Figure 4-1032. DDRSS_PHY_353 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_DATA_DC_CAL_CLK_SEL_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2072. DDRSS_PHY_353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_DATA_DC_CAL_CLK_SEL_1	R/W	0h	Determines DCC CAL clock for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDM_SLAVE_DELAY_1	R/W	0h	Read DM/DBI slave delay setting for slice 1. May be used for data swap.

4.4.239 DDRSS_PHY_354 Register (Offset = 4588h) [reset = 0h]

DDRSS_PHY_354 is shown in Figure 4-1033 and described in Table 4-2074.

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Table 4-2073. DDRSS_PHY_354 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4588h

Figure 4-1033. DDRSS_PHY_354 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_DQS_OE_TIMING_1								PHY_DQ_TSEL_WR_TIMING_1							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_TSEL_RD_TIMING_1								PHY_DQ_OE_TIMING_1							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2074. DDRSS_PHY_354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_OE_TIMING_1	R/W	0h	Start/end timing values for DQS output enable signals for slice 1.
23-16	PHY_DQ_TSEL_WR_TIMING_1	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 1.
15-8	PHY_DQ_TSEL_RD_TIMING_1	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 1.
7-0	PHY_DQ_OE_TIMING_1	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 1.

4.4.240 DDRSS_PHY_355 Register (Offset = 458Ch) [reset = X]

DDRSS_PHY_355 is shown in [Figure 4-1034](#) and described in [Table 4-2076](#).

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Table 4-2075. DDRSS_PHY_355 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 458Ch

Figure 4-1034. DDRSS_PHY_355 Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_1							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DQS_OE_RD_TIMING_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_RD_TIMING_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_IO_PAD_DELAY_TIMING_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2076. DDRSS_PHY_355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_TSEL_WR_TIMING_1	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 1.
23-16	PHY_DQS_OE_RD_TIMING_1	R/W	0h	Start/end timing values for DQS read based OE extension for slice 1.
15-8	PHY_DQS_TSEL_RD_TIMING_1	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_IO_PAD_DELAY_TIMING_1	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 1.

4.4.241 DDRSS_PHY_356 Register (Offset = 4590h) [reset = X]

DDRSS_PHY_356 is shown in [Figure 4-1035](#) and described in [Table 4-2078](#).

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Table 4-2077. DDRSS_PHY_356 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4590h

Figure 4-1035. DDRSS_PHY_356 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_VREF_CTRL_DQ_1											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_VREF_SETTING_TIME_1															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2078. DDRSS_PHY_356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PHY_PAD_VREF_CTRL_DQ_1	R/W	0h	Pad VREF control settings for DQ slice 1. <ul style="list-style-type: none"> Bits[27-24] = MODE Bits[23] = EN Bits[22-16] = VREFSEL
15-0	PHY_VREF_SETTING_TIME_1	R/W	0h	Number of cycles for vref settle after setting is changed for slice 1.

4.4.242 DDRSS_PHY_357 Register (Offset = 4594h) [reset = X]

DDRSS_PHY_357 is shown in Figure 4-1036 and described in Table 4-2080.

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Table 4-2079. DDRSS_PHY_357 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4594h

Figure 4-1036. DDRSS_PHY_357 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DQS_IE_TIMING_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_IE_TIMING_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_PER_CS_TRAINING_EN_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2080. DDRSS_PHY_357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_RDDATA_EN_IE_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 1.
23-16	PHY_DQS_IE_TIMING_1	R/W	0h	Start/end timing values for DQS input enable signals for slice 1.
15-8	PHY_DQ_IE_TIMING_1	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_EN_1	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 1. Must have same value in all slices.

4.4.243 DDRSS_PHY_358 Register (Offset = 4598h) [reset = X]

DDRSS_PHY_358 is shown in [Figure 4-1037](#) and described in [Table 4-2082](#).

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Table 4-2081. DDRSS_PHY_358 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4598h

Figure 4-1037. DDRSS_PHY_358 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDDATA_EN_OE_DLY_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_TSEL_DLY_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_DBI_MODE_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PHY_IE_MODE_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2082. DDRSS_PHY_358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDDATA_EN_OE_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 1.
23-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_TSEL_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 1.
15-9	RESERVED	R/W	X	
8	PHY_DBI_MODE_1	R/W	0h	DBI mode for slice 1. Bit (0) enables return of DBI read data.
7-2	RESERVED	R/W	X	
1-0	PHY_IE_MODE_1	R/W	0h	Input enable mode bits for slice 1. Bit (0) enables the mode where the input enables are always on set to 1 to enable. Bit (1) disables the input enable on the DM signal set to 1 to disable.

4.4.244 DDRSS_PHY_359 Register (Offset = 459Ch) [reset = X]

DDRSS_PHY_359 is shown in Figure 4-1038 and described in Table 4-2084.

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Table 4-2083. DDRSS_PHY_359 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 459Ch

Figure 4-1038. DDRSS_PHY_359 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_MASTER_DELAY_STEP_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DELAY_START_1		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_START_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_MASTER_MODE_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2084. DDRSS_PHY_359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_MASTER_DELAY_STEP_1	R/W	0h	Incremental step size for master delay line locking algorithm for slice 1.
23-19	RESERVED	R/W	X	
18-8	PHY_MASTER_DELAY_START_1	R/W	0h	Start value for master delay line locking algorithm for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_SW_MASTER_MODE_1	R/W	0h	Master delay line override settings for slice 1. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit (2) enables software bypass mode. Bit (3) is the software bypass mode value.

4.4.245 DDRSS_PHY_360 Register (Offset = 45A0h) [reset = X]

DDRSS_PHY_360 is shown in Figure 4-1039 and described in Table 4-2086.

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Table 4-2085. DDRSS_PHY_360 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45A0h

Figure 4-1039. DDRSS_PHY_360 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_DLY_STEP_1							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_RPTR_UPDATE_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_HALF_MEASURE_1							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_MASTER_DELAY_WAIT_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2086. DDRSS_PHY_360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_DLY_STEP_1	R/W	0h	DQS slave delay step size during write leveling for slice 1.
23-20	RESERVED	R/W	X	
19-16	PHY_RPTR_UPDATE_1	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 1.
15-8	PHY_MASTER_DELAY_HALF_MEASURE_1	R/W	0h	Defines the number of delay line elements to be considered in determining whether to lock to a half clock cycle in the data slice master for slice 1.
7-0	PHY_MASTER_DELAY_WAIT_1	R/W	0h	Wait cycles for master delay line locking algorithm for slice 1. Bits (3:0) are the cycle wait count after a calibration clock setting change. Bits (7:4) are the cycle wait count after a master delay setting change.

4.4.246 DDRSS_PHY_361 Register (Offset = 45A4h) [reset = X]

DDRSS_PHY_361 is shown in Figure 4-1040 and described in Table 4-2088.

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Table 4-2087. DDRSS_PHY_361 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45A4h

Figure 4-1040. DDRSS_PHY_361 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_RESP_WAIT_CNT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_DLY_STEP_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_RESP_WAIT_CNT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_WRLVL_DLY_FINE_STEP_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2088. DDRSS_PHY_361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_GTLVL_RESP_WAIT_CNT_1	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 1. The valid range is 0x0 to 0xB.
23-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_DLY_STEP_1	R/W	0h	DQS slave delay step size during gate training for slice 1.
15-14	RESERVED	R/W	X	
13-8	PHY_WRLVL_RESP_WAIT_CNT_1	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_WRLVL_DLY_FINE_STEP_1	R/W	0h	DQS slave delay fine step size during write leveling for slice 1.

4.4.247 DDRSS_PHY_362 Register (Offset = 45A8h) [reset = X]

DDRSS_PHY_362 is shown in [Figure 4-1041](#) and described in [Table 4-2090](#).

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Table 4-2089. DDRSS_PHY_362 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45A8h

Figure 4-1041. DDRSS_PHY_362 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_FINAL_STEP_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_GTLVL_BACK_STEP_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2090. DDRSS_PHY_362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_GTLVL_FINAL_STEP_1	R/W	0h	Final backup step delay used in gate training algorithm for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_BACK_STEP_1	R/W	0h	Interim backup step delay used in gate training algorithm for slice 1.

4.4.248 DDRSS_PHY_363 Register (Offset = 45ACh) [reset = X]

DDRSS_PHY_363 is shown in Figure 4-1042 and described in Table 4-2092.

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Table 4-2091. DDRSS_PHY_363 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45ACh

Figure 4-1042. DDRSS_PHY_363 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_DLY_STEP_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PHY_TOGGLE_PRE_SUPP RT_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_WDQLVL_DLY_STEP_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2092. DDRSS_PHY_363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_RDLVL_DLY_STEP_1	R/W	0h	DQS slave delay step size during read leveling for slice 1.
23-17	RESERVED	R/W	X	
16	PHY_TOGGLE_PRE_SUPPORT_1	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 1.
15-12	RESERVED	R/W	X	
11-8	PHY_WDQLVL_QTR_DLY_STEP_1	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 1. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value.
7-0	PHY_WDQLVL_DLY_STEP_1	R/W	0h	DQ slave delay step size during write data leveling for slice 1.

4.4.249 DDRSS_PHY_364 Register (Offset = 45B0h) [reset = X]

DDRSS_PHY_364 is shown in [Figure 4-1043](#) and described in [Table 4-2094](#).

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Table 4-2093. DDRSS_PHY_364 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45B0h

Figure 4-1043. DDRSS_PHY_364 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_MAX_EDGE_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2094. DDRSS_PHY_364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_MAX_EDGE_1	R/W	0h	The maximum rdlvl slave delay search window for read eye training for slice 1.

4.4.250 DDRSS_PHY_365 Register (Offset = 45B4h) [reset = X]

DDRSS_PHY_365 is shown in [Figure 4-1044](#) and described in [Table 4-2096](#).

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Table 4-2095. DDRSS_PHY_365 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45B4h

Figure 4-1044. DDRSS_PHY_365 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_RDLVL_PER_START_OFFSET_1					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED							PHY_SW_RDLVL_DVW_MIN_EN_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_DVW_MIN_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_DVW_MIN_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2096. DDRSS_PHY_365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_RDLVL_PER_START_OFFSET_1	R/W	0h	Periodic training start point offset for slice 1.
23-17	RESERVED	R/W	X	
16	PHY_SW_RDLVL_DVW_MIN_EN_1	R/W	0h	SW override to enable use of PHY_RDLVL_DVW_MIN for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_DVW_MIN_1	R/W	0h	Minimum data valid window across DQs and ranks for slice 1.

4.4.251 DDRSS_PHY_366 Register (Offset = 45B8h) [reset = X]

DDRSS_PHY_366 is shown in [Figure 4-1045](#) and described in [Table 4-2098](#).

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Table 4-2097. DDRSS_PHY_366 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45B8h

Figure 4-1045. DDRSS_PHY_366 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_1	
R/W-X						R/W-3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_1		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2098. DDRSS_PHY_366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_INIT_DISABLE_1	R/W	3h	Disable duty cycle adjust at initialization for slice 1.
15-11	RESERVED	R/W	X	
10-8	PHY_WRPATH_GATE_TIMING_1	R/W	0h	Write path clock gating timing for slice 1. it means additional clock number to write path clock gate
7-2	RESERVED	R/W	X	
1-0	PHY_WRPATH_GATE_DISABLE_1	R/W	0h	Write path clock gating disable for slice 1. [0]: disable pull in wrdata_en [1]: disable write path clock gating, clock always on

4.4.252 DDRSS_PHY_367 Register (Offset = 45BCh) [reset = X]

DDRSS_PHY_367 is shown in [Figure 4-1046](#) and described in [Table 4-2100](#).

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Table 4-2099. DDRSS_PHY_367 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45BCh

Figure 4-1046. DDRSS_PHY_367 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_1		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ_INIT_SLV_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_INIT_SLV_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2100. DDRSS_PHY_367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_1	R/W	0h	Initial value of write DQ slave delay for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_1	R/W	0h	Initial value of write DQS slave delay for slice 1.

4.4.253 DDRSS_PHY_368 Register (Offset = 45C0h) [reset = X]

DDRSS_PHY_368 is shown in [Figure 4-1047](#) and described in [Table 4-2102](#).

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Table 4-2101. DDRSS_PHY_368 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45C0h

Figure 4-1047. DDRSS_PHY_368 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_1							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DM_CLK_SE_THRSHLD_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_1
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_1
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2102. DDRSS_PHY_368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_1	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 1.
23-16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_1	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 1.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_WDQLVL_ENABLE_1	R/W	0h	Enable duty cycle adjust during write DQ training for slice 1.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_WRLVL_ENABLE_1	R/W	0h	Enable duty cycle adjust during write leveling for slice 1.

4.4.254 DDRSS_PHY_369 Register (Offset = 45C4h) [reset = X]

DDRSS_PHY_369 is shown in Figure 4-1048 and described in Table 4-2104.

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Table 4-2103. DDRSS_PHY_369 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45C4h

Figure 4-1048. DDRSS_PHY_369 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_DLY_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED			PHY_MEAS_DLY_STEP_ENABLE_1				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQ_OSC_DELTA_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2104. DDRSS_PHY_369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_DLY_1	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 1.
15-14	RESERVED	R/W	X	
13-8	PHY_MEAS_DLY_STEP_ENABLE_1	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 1.
7	RESERVED	R/W	X	
6-0	PHY_WDQ_OSC_DELTA_1	R/W	0h	Slave delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 1.

4.4.255 DDRSS_PHY_370 Register (Offset = 45C8h) [reset = 0h]

DDRSS_PHY_370 is shown in [Figure 4-1049](#) and described in [Table 4-2106](#).

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Table 4-2105. DDRSS_PHY_370 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45C8h

Figure 4-1049. DDRSS_PHY_370 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2106. DDRSS_PHY_370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DQ_DM_SWIZZLE0_1	R/W	0h	DQ/DM bit swizzling 0 for slice 1. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0, Bits (7:4) inform the PHY which bit in {DM,DQ} map to DQ1, etc.

4.4.256 DDRSS_PHY_371 Register (Offset = 45CCh) [reset = X]

DDRSS_PHY_371 is shown in [Figure 4-1050](#) and described in [Table 4-2108](#).

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Table 4-2107. DDRSS_PHY_371 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45CCh

Figure 4-1050. DDRSS_PHY_371 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2108. DDRSS_PHY_371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PHY_DQ_DM_SWIZZLE1_1	R/W	0h	DQ/DM bit swizzling 1 for slice 1. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DM.

4.4.257 DDRSS_PHY_372 Register (Offset = 45D0h) [reset = X]

DDRSS_PHY_372 is shown in [Figure 4-1051](#) and described in [Table 4-2110](#).

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Table 4-2109. DDRSS_PHY_372 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45D0h

Figure 4-1051. DDRSS_PHY_372 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_1										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2110. DDRSS_PHY_372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ1_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ1 for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ0_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ0 for slice 1.

4.4.258 DDRSS_PHY_373 Register (Offset = 45D4h) [reset = X]

DDRSS_PHY_373 is shown in [Figure 4-1052](#) and described in [Table 4-2112](#).

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Table 4-2111. DDRSS_PHY_373 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45D4h

Figure 4-1052. DDRSS_PHY_373 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_1										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2112. DDRSS_PHY_373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ3_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ3 for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ2_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ2 for slice 1.

4.4.259 DDRSS_PHY_374 Register (Offset = 45D8h) [reset = X]

DDRSS_PHY_374 is shown in Figure 4-1053 and described in Table 4-2114.

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Table 4-2113. DDRSS_PHY_374 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45D8h

Figure 4-1053. DDRSS_PHY_374 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_1										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2114. DDRSS_PHY_374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ5_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ5 for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ4_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ4 for slice 1.

4.4.260 DDRSS_PHY_375 Register (Offset = 45DCh) [reset = X]

DDRSS_PHY_375 is shown in [Figure 4-1054](#) and described in [Table 4-2116](#).

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Table 4-2115. DDRSS_PHY_375 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45DCh

Figure 4-1054. DDRSS_PHY_375 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_1										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2116. DDRSS_PHY_375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ7_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ7 for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ6_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQ6 for slice 1.

4.4.261 DDRSS_PHY_376 Register (Offset = 45E0h) [reset = X]

DDRSS_PHY_376 is shown in [Figure 4-1055](#) and described in [Table 4-2118](#).

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Table 4-2117. DDRSS_PHY_376 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45E0h

Figure 4-1055. DDRSS_PHY_376 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_1									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_CLK_WRDM_SLAVE_DELAY_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2118. DDRSS_PHY_376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_CLK_WRDQS_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DQS for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDM_SLAVE_DELAY_1	R/W	0h	Write clock slave delay setting for DM for slice 1.

4.4.262 DDRSS_PHY_377 Register (Offset = 45E4h) [reset = X]

DDRSS_PHY_377 is shown in [Figure 4-1056](#) and described in [Table 4-2120](#).

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Table 4-2119. DDRSS_PHY_377 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45E4h

Figure 4-1056. DDRSS_PHY_377 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2120. DDRSS_PHY_377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ0 for slice 1.
7-2	RESERVED	R/W	X	
1-0	PHY_WRLVL_THRESHOLD_ADJUST_1	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 1.

4.4.263 DDRSS_PHY_378 Register (Offset = 45E8h) [reset = X]

DDRSS_PHY_378 is shown in [Figure 4-1057](#) and described in [Table 4-2122](#).

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Table 4-2121. DDRSS_PHY_378 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45E8h

Figure 4-1057. DDRSS_PHY_378 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2122. DDRSS_PHY_378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ1 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ0 for slice 1.

4.4.264 DDRSS_PHY_379 Register (Offset = 45ECh) [reset = X]

DDRSS_PHY_379 is shown in [Figure 4-1058](#) and described in [Table 4-2124](#).

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Table 4-2123. DDRSS_PHY_379 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45ECh

Figure 4-1058. DDRSS_PHY_379 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2124. DDRSS_PHY_379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ2 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ1 for slice 1.

4.4.265 DDRSS_PHY_380 Register (Offset = 45F0h) [reset = X]

DDRSS_PHY_380 is shown in [Figure 4-1059](#) and described in [Table 4-2126](#).

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Table 4-2125. DDRSS_PHY_380 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45F0h

Figure 4-1059. DDRSS_PHY_380 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2126. DDRSS_PHY_380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ3 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ2 for slice 1.

4.4.266 DDRSS_PHY_381 Register (Offset = 45F4h) [reset = X]

DDRSS_PHY_381 is shown in Figure 4-1060 and described in Table 4-2128.

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Table 4-2127. DDRSS_PHY_381 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45F4h

Figure 4-1060. DDRSS_PHY_381 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2128. DDRSS_PHY_381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ4 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ3 for slice 1.

4.4.267 DDRSS_PHY_382 Register (Offset = 45F8h) [reset = X]

DDRSS_PHY_382 is shown in [Figure 4-1061](#) and described in [Table 4-2130](#).

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Table 4-2129. DDRSS_PHY_382 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45F8h

Figure 4-1061. DDRSS_PHY_382 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2130. DDRSS_PHY_382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ5 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ4 for slice 1.

4.4.268 DDRSS_PHY_383 Register (Offset = 45FCh) [reset = X]

DDRSS_PHY_383 is shown in [Figure 4-1062](#) and described in [Table 4-2132](#).

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Table 4-2131. DDRSS_PHY_383 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 45FCh

Figure 4-1062. DDRSS_PHY_383 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2132. DDRSS_PHY_383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ6 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ5 for slice 1.

4.4.269 DDRSS_PHY_384 Register (Offset = 4600h) [reset = X]

DDRSS_PHY_384 is shown in [Figure 4-1063](#) and described in [Table 4-2134](#).

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Table 4-2133. DDRSS_PHY_384 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4600h

Figure 4-1063. DDRSS_PHY_384 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2134. DDRSS_PHY_384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DQ7 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ6 for slice 1.

4.4.270 DDRSS_PHY_385 Register (Offset = 4604h) [reset = X]

DDRSS_PHY_385 is shown in [Figure 4-1064](#) and described in [Table 4-2136](#).

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Table 4-2135. DDRSS_PHY_385 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4604h

Figure 4-1064. DDRSS_PHY_385 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DM_RISE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2136. DDRSS_PHY_385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	R/W	0h	Rising edge read DQS slave delay setting for DM for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DQ7 for slice 1.

4.4.271 DDRSS_PHY_386 Register (Offset = 4608h) [reset = X]

DDRSS_PHY_386 is shown in [Figure 4-1065](#) and described in [Table 4-2138](#).

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Table 4-2137. DDRSS_PHY_386 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4608h

Figure 4-1065. DDRSS_PHY_386 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2138. DDRSS_PHY_386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_GATE_SLAVE_DELAY_1	R/W	0h	Read DQS slave delay setting for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_1	R/W	0h	Falling edge read DQS slave delay setting for DM for slice 1.

4.4.272 DDRSS_PHY_387 Register (Offset = 460Ch) [reset = X]

DDRSS_PHY_387 is shown in [Figure 4-1066](#) and described in [Table 4-2140](#).

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Table 4-2139. DDRSS_PHY_387 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 460Ch

Figure 4-1066. DDRSS_PHY_387 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_1	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_DELAY_EARLY_THRESHOLD_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_WRITE_PATH_LAT_ADD_1		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_LATENCY_ADJUST_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2140. DDRSS_PHY_387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_1	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 1.
15-11	RESERVED	R/W	X	
10-8	PHY_WRITE_PATH_LAT_ADD_1	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 1.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_LATENCY_ADJUST_1	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 1.

4.4.273 DDRSS_PHY_388 Register (Offset = 4610h) [reset = X]

DDRSS_PHY_388 is shown in [Figure 4-1067](#) and described in [Table 4-2142](#).

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Table 4-2141. DDRSS_PHY_388 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4610h

Figure 4-1067. DDRSS_PHY_388 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_E ARLY_FORCE_ ZERO_1
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_ THRESHOLD_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2142. DDRSS_PHY_388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_WRLVL_EARLY_FORCE_ZERO_1	R/W	0h	Force the final write level delay value (that meets the early threshold) to 0 for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 1.

4.4.274 DDRSS_PHY_389 Register (Offset = 4614h) [reset = X]

DDRSS_PHY_389 is shown in [Figure 4-1068](#) and described in [Table 4-2144](#).

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Table 4-2143. DDRSS_PHY_389 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4614h

Figure 4-1068. DDRSS_PHY_389 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2144. DDRSS_PHY_389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_LAT_ADJ_START_1	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 1.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_RDDQS_SLV_DLY_START_1	R/W	0h	Initial read DQS gate slave delay setting during gate training for slice 1.

4.4.275 DDRSS_PHY_390 Register (Offset = 4618h) [reset = X]

DDRSS_PHY_390 is shown in Figure 4-1069 and described in Table 4-2146.

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Table 4-2145. DDRSS_PHY_390 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4618h

Figure 4-1069. DDRSS_PHY_390 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PAS S_1
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_NTP_WRLAT_START_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_1		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_START_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2146. DDRSS_PHY_390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_NTP_PASS_1	R/W	0h	Indicates if No-topology training found a passing result for slice 1.
23-20	RESERVED	R/W	X	
19-16	PHY_NTP_WRLAT_START_1	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_WDQLVL_DQDM_SLV_DLY_START_1	R/W	0h	Initial DQ/DM slave delay setting during write data leveling for slice 1.

4.4.276 DDRSS_PHY_391 Register (Offset = 461Ch) [reset = X]

DDRSS_PHY_391 is shown in [Figure 4-1070](#) and described in [Table 4-2148](#).

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Table 4-2147. DDRSS_PHY_391 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 461Ch

Figure 4-1070. DDRSS_PHY_391 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2148. DDRSS_PHY_391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	R/W	0h	Read leveling starting value for the DQS/DQ slave delay settings for slice 1.

4.4.277 DDRSS_PHY_392 Register (Offset = 4620h) [reset = 20202020h]

DDRSS_PHY_392 is shown in [Figure 4-1071](#) and described in [Table 4-2150](#).

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Table 4-2149. DDRSS_PHY_392 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4620h

Figure 4-1071. DDRSS_PHY_392 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_1							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ1_CLK_ADJUST_1							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ0_CLK_ADJUST_1							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_CLK_ADJUST_1							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2150. DDRSS_PHY_392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ2_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
23-16	PHY_DATA_DC_DQ1_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
15-8	PHY_DATA_DC_DQ0_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
7-0	PHY_DATA_DC_DQS_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.

4.4.278 DDRSS_PHY_393 Register (Offset = 4624h) [reset = 20202020h]

DDRSS_PHY_393 is shown in [Figure 4-1072](#) and described in [Table 4-2152](#).

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Table 4-2151. DDRSS_PHY_393 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4624h

Figure 4-1072. DDRSS_PHY_393 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ6_CLK_ADJUST_1							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ5_CLK_ADJUST_1							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ4_CLK_ADJUST_1							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ3_CLK_ADJUST_1							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2152. DDRSS_PHY_393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ6_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
23-16	PHY_DATA_DC_DQ5_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
15-8	PHY_DATA_DC_DQ4_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
7-0	PHY_DATA_DC_DQ3_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.

4.4.279 DDRSS_PHY_394 Register (Offset = 4628h) [reset = 2020h]

DDRSS_PHY_394 is shown in [Figure 4-1073](#) and described in [Table 4-2154](#).

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Table 4-2153. DDRSS_PHY_394 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4628h

Figure 4-1073. DDRSS_PHY_394 Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_1							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_1							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_1							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_1							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2154. DDRSS_PHY_394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_DSLICE_PAD_BOOSTPN_SETTING_1	R/W	0h	Setting for boost P/N of pad for slice 1.
15-8	PHY_DATA_DC_DM_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.
7-0	PHY_DATA_DC_DQ7_CLK_ADJUST_1	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 1.

4.4.280 DDRSS_PHY_395 Register (Offset = 462Ch) [reset = X]

DDRSS_PHY_395 is shown in [Figure 4-1074](#) and described in [Table 4-2156](#).

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Table 4-2155. DDRSS_PHY_395 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 462Ch

Figure 4-1074. DDRSS_PHY_395 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_1	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_1	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTL_SETTING_1					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2156. DDRSS_PHY_395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DQS_FFE_1	R/W	0h	TX_FFE setting for DQS pad for slice 1.
15-10	RESERVED	R/W	X	
9-8	PHY_DQ_FFE_1	R/W	0h	TX_FFE setting for DQ/DM pad for slice 1.
7-6	RESERVED	R/W	X	
5-0	PHY_DSLICE_PAD_RX_CTL_SETTING_1	R/W	0h	Setting for RX ctle P/N of pad for slice 1.

4.4.281 DDRSS_PHY_512 Register (Offset = 4800h) [reset = X]

DDRSS_PHY_512 is shown in [Figure 4-1075](#) and described in [Table 4-2158](#).

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Table 4-2157. DDRSS_PHY_512 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4800h

Figure 4-1075. DDRSS_PHY_512 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_2		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CLK_WR_BYPASS_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2158. DDRSS_PHY_512 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_IO_PAD_DELAY_TIMING_BYPASS_2	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WR_BYPASS_SLAVE_DELAY_2	R/W	0h	Write data clock bypass mode slave delay setting for slice 2.} PADDING_BEFORE

4.4.282 DDRSS_PHY_513 Register (Offset = 4804h) [reset = X]

DDRSS_PHY_513 is shown in [Figure 4-1076](#) and described in [Table 4-2160](#).

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Table 4-2159. DDRSS_PHY_513 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4804h

Figure 4-1076. DDRSS_PHY_513 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_2		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2160. DDRSS_PHY_513 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_WRITE_PATH_LAT_ADD_BYPASS_2	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrddata_en/dfi_wrddata signals for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_2	R/W	0h	Write DQS bypass mode slave delay setting for slice 2.

4.4.283 DDRSS_PHY_514 Register (Offset = 4808h) [reset = X]

DDRSS_PHY_514 is shown in [Figure 4-1077](#) and described in [Table 4-2162](#).

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Table 4-2161. DDRSS_PHY_514 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4808h

Figure 4-1077. DDRSS_PHY_514 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_BYPASS_TWO_CYCLE_PREAMBLE_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2162. DDRSS_PHY_514 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CLK_BYPASS_OVERRIDE_2	R/W	0h	Bypass mode override setting for slice 2.
23-18	RESERVED	R/W	X	
17-16	PHY_BYPASS_TWO_CYCLE_PREAMBLE_2	R/W	0h	Two_cycle_preamble for bypass mode for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_2	R/W	0h	Read DQS bypass mode slave delay setting for slice 2.

4.4.284 DDRSS_PHY_515 Register (Offset = 480Ch) [reset = X]

DDRSS_PHY_515 is shown in Figure 4-1078 and described in Table 4-2164.

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Table 4-2163. DDRSS_PHY_515 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 480Ch

Figure 4-1078. DDRSS_PHY_515 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_2					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ2_SHIFT_2					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ1_SHIFT_2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ0_SHIFT_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2164. DDRSS_PHY_515 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ3_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ2_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ1_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-2164. DDRSS_PHY_515 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ0_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.285 DDRSS_PHY_516 Register (Offset = 4810h) [reset = X]

DDRSS_PHY_516 is shown in [Figure 4-1079](#) and described in [Table 4-2166](#).

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Table 4-2165. DDRSS_PHY_516 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4810h

Figure 4-1079. DDRSS_PHY_516 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_2					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ6_SHIFT_2					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ5_SHIFT_2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ4_SHIFT_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2166. DDRSS_PHY_516 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ7_SHIF T_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ6_SHIF T_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ5_SHIF T_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-2166. DDRSS_PHY_516 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ4_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.286 DDRSS_PHY_517 Register (Offset = 4814h) [reset = X]

DDRSS_PHY_517 is shown in Figure 4-1080 and described in Table 4-2168.

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Table 4-2167. DDRSS_PHY_517 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4814h

Figure 4-1080. DDRSS_PHY_517 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_2
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
RESERVED						PHY_PER_RANK_CS_MAP_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_WRDQS_SHIFT_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDM_SHIFT_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2168. DDRSS_PHY_517 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_PER_CS_TRAINING_MULTICAST_EN_2	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 2. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PHY_PER_RANK_CS_MAP_2	R/W	0h	Per-rank CS map for slice 2. Setting a bit uses that CS for the rank, bit (0) uses CS0, bit (1) uses CS1, etc.
15-12	RESERVED	R/W	X	
11-8	PHY_SW_WRDQS_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bit (3) is the cycle_shift value.
7-6	RESERVED	R/W	X	

Table 4-2168. DDRSS_PHY_517 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PHY_SW_WRDM_SHIFT_2	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

4.4.287 DDRSS_PHY_518 Register (Offset = 4818h) [reset = X]

DDRSS_PHY_518 is shown in Figure 4-1081 and described in Table 4-2170.

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Table 4-2169. DDRSS_PHY_518 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4818h

Figure 4-1081. DDRSS_PHY_518 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_LP4_BOOT_RDDATA_EN_DLY_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_PER_CS_TRAINING_INDEX_2
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2170. DDRSS_PHY_518 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 2.
23-21	RESERVED	R/W	X	
20-16	PHY_LP4_BOOT_RDDATA_EN_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 2.
15-10	RESERVED	R/W	X	
9-8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_INDEX_2	R/W	0h	For per-rank training, indicates which rank's parameters are read/written for slice 2.

4.4.288 DDRSS_PHY_519 Register (Offset = 481Ch) [reset = X]

DDRSS_PHY_519 is shown in Figure 4-1082 and described in Table 4-2172.

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Table 4-2171. DDRSS_PHY_519 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 481Ch

Figure 4-1082. DDRSS_PHY_519 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_OE_DLY_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2172. DDRSS_PHY_519 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 2.
23-18	RESERVED	R/W	X	
17-16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_2	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 2. Bit (0): disable pull in wrdata_en Bit (1): disable write path clock gating, clock always on
15-12	RESERVED	R/W	X	
11-8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_2	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_LP4_BOOT_RPTR_UPDATE_2	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 2.

4.4.289 DDRSS_PHY_520 Register (Offset = 4820h) [reset = X]

DDRSS_PHY_520 is shown in [Figure 4-1083](#) and described in [Table 4-2174](#).

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Table 4-2173. DDRSS_PHY_520 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4820h

Figure 4-1083. DDRSS_PHY_520 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_LPBK_CONTROL_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_LPBK_CONTROL_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_CTRL_LPBK_EN_2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2174. DDRSS_PHY_520 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LPBK_DFX_TIMEOUT_EN_2	R/W	0h	Loopback read only test timeout mechanism enable for slice 2.
23-17	RESERVED	R/W	X	
16-8	PHY_LPBK_CONTROL_2	R/W	0h	Loopback control bits for slice 2.
7-2	RESERVED	R/W	X	
1-0	PHY_CTRL_LPBK_EN_2	R/W	0h	Loopback control en for slice 2.

4.4.290 DDRSS_PHY_521 Register (Offset = 4824h) [reset = 0h]

DDRSS_PHY_521 is shown in [Figure 4-1084](#) and described in [Table 4-2176](#).

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Table 4-2175. DDRSS_PHY_521 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4824h

Figure 4-1084. DDRSS_PHY_521 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2176. DDRSS_PHY_521 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_AUTO_TIMING_MARGIN_CONTROL_2	R/W	0h	Auto timing marging control bits for slice 2.

4.4.291 DDRSS_PHY_522 Register (Offset = 4828h) [reset = X]

DDRSS_PHY_522 is shown in [Figure 4-1085](#) and described in [Table 4-2178](#).

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Table 4-2177. DDRSS_PHY_522 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4828h

Figure 4-1085. DDRSS_PHY_522 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_2																											
R-X				R-0h																											

LEGEND: R = Read Only; -n = value after reset

Table 4-2178. DDRSS_PHY_522 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-0	PHY_AUTO_TIMING_MARGIN_OBS_2	R	0h	Observation register for the auto_timing_margin for slice 2. READ-ONLY

4.4.292 DDRSS_PHY_523 Register (Offset = 482Ch) [reset = X]

DDRSS_PHY_523 is shown in [Figure 4-1086](#) and described in [Table 4-2180](#).

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Table 4-2179. DDRSS_PHY_523 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 482Ch

Figure 4-1086. DDRSS_PHY_523 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTIPATTERN_ENABLE_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_PRBS_PATTERN_MASK_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_PRBS_PATTERN_MASK_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PHY_PRBS_PATTERN_START_2						
R/W-X	R/W-1h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2180. DDRSS_PHY_523 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RDLVL_MULTIPATTERN_ENABLE_2	R/W	0h	Read Leveling Multi-pattern enable for slice 2.
23-17	RESERVED	R/W	X	
16-8	PHY_PRBS_PATTERN_MASK_2	R/W	0h	PRBS7 mask signal for slice 2.
7	RESERVED	R/W	X	
6-0	PHY_PRBS_PATTERN_START_2	R/W	1h	PRBS7 start pattern for slice 2.

4.4.293 DDRSS_PHY_524 Register (Offset = 4830h) [reset = X]

DDRSS_PHY_524 is shown in [Figure 4-1087](#) and described in [Table 4-2182](#).

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Table 4-2181. DDRSS_PHY_524 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4830h

Figure 4-1087. DDRSS_PHY_524 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PHY_VREF_TRAIN_OBS_2						
R/W-X	R-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_VREF_INITIAL_STEPSIZE_2						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RDLVL_MULTIPATT_RST_DISABLE_2
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2182. DDRSS_PHY_524 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	PHY_VREF_TRAIN_OBS_2	R	0h	Observation register for best vref value for slice 2. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	PHY_VREF_INITIAL_STEPSIZE_2	R/W	0h	Data slice initial VREF training step size for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_RDLVL_MULTIPATT_RST_DISABLE_2	R/W	0h	Read Leveling read level windows disable reset for slice 2.

4.4.294 DDRSS_PHY_525 Register (Offset = 4834h) [reset = X]

DDRSS_PHY_525 is shown in [Figure 4-1088](#) and described in [Table 4-2184](#).

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Table 4-2183. DDRSS_PHY_525 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4834h

Figure 4-1088. DDRSS_PHY_525 Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_SNAP_OBS_REGS_2
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2184. DDRSS_PHY_525 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SC_PHY_SNAP_OBS_REGS_2	W	0h	Initiates a snapshot of the internal observation registers for slice 2. Set to 1 to trigger. WRITE-ONLY
23-20	RESERVED	R/W	X	
19-16	PHY_GATE_ERROR_DELAY_SELECT_2	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2	R/W	0h	Read DQS data clock bypass mode slave delay setting for slice 2.

4.4.295 DDRSS_PHY_526 Register (Offset = 4838h) [reset = X]

DDRSS_PHY_526 is shown in [Figure 4-1089](#) and described in [Table 4-2186](#).

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Table 4-2185. DDRSS_PHY_526 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4838h

Figure 4-1089. DDRSS_PHY_526 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MEM_CLASS_2		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							PHY_LPDDR_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2186. DDRSS_PHY_526 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_MEM_CLASS_2	R/W	0h	Indicates the type of DRAM for slice 2. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4
23-17	RESERVED	R/W	X	
16	PHY_LPDDR_2	R/W	0h	Adds a cycle of delay for the slice 2 to match the address slice. Set to 1 to add a cycle
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL1_SLAVE_DELAY_2	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 2.

4.4.296 DDRSS_PHY_527 Register (Offset = 483Ch) [reset = X]

DDRSS_PHY_527 is shown in [Figure 4-1090](#) and described in [Table 4-2188](#).

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Table 4-2187. DDRSS_PHY_527 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 483Ch

Figure 4-1090. DDRSS_PHY_527 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						ON_FLY_GATE_ADJUST_EN_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL2_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL2_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2188. DDRSS_PHY_527 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	ON_FLY_GATE_ADJUST_EN_2	R/W	0h	Control the on-the-fly gate adjustment for slice 2.
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL2_SLAVE_DELAY_2	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 2.

4.4.297 DDRSS_PHY_528 Register (Offset = 4840h) [reset = 0h]

DDRSS_PHY_528 is shown in [Figure 4-1091](#) and described in [Table 4-2190](#).

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Table 4-2189. DDRSS_PHY_528 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4840h

Figure 4-1091. DDRSS_PHY_528 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2190. DDRSS_PHY_528 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_GATE_TRACKING_OBS_2	R	0h	Report the on-the-fly gate measurement result for slice 2. READ-ONLY

4.4.298 DDRSS_PHY_529 Register (Offset = 4844h) [reset = X]

DDRSS_PHY_529 is shown in [Figure 4-1092](#) and described in [Table 4-2192](#).

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Table 4-2191. DDRSS_PHY_529 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4844h

Figure 4-1092. DDRSS_PHY_529 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_2
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2192. DDRSS_PHY_529 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-8	PHY_LP4_PST_AMBLE_2	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_DFI40_POLARITY_2	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 2.

4.4.299 DDRSS_PHY_530 Register (Offset = 4848h) [reset = 0h]

DDRSS_PHY_530 is shown in [Figure 4-1093](#) and described in [Table 4-2194](#).

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Table 4-2193. DDRSS_PHY_530 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4848h

Figure 4-1093. DDRSS_PHY_530 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2194. DDRSS_PHY_530 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT8_2	R/W	0h	Read leveling pattern 8 data for slice 2.

4.4.300 DDRSS_PHY_531 Register (Offset = 484Ch) [reset = 0h]

DDRSS_PHY_531 is shown in [Figure 4-1094](#) and described in [Table 4-2196](#).

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Table 4-2195. DDRSS_PHY_531 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 484Ch

Figure 4-1094. DDRSS_PHY_531 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2196. DDRSS_PHY_531 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT9_2	R/W	0h	Read leveling pattern 9 data for slice 2.

4.4.301 DDRSS_PHY_532 Register (Offset = 4850h) [reset = 0h]

DDRSS_PHY_532 is shown in [Figure 4-1095](#) and described in [Table 4-2198](#).

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Table 4-2197. DDRSS_PHY_532 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4850h

Figure 4-1095. DDRSS_PHY_532 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2198. DDRSS_PHY_532 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT10_2	R/W	0h	Read leveling pattern 10 data for slice 2.

4.4.302 DDRSS_PHY_533 Register (Offset = 4854h) [reset = 0h]

DDRSS_PHY_533 is shown in [Figure 4-1096](#) and described in [Table 4-2200](#).

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Table 4-2199. DDRSS_PHY_533 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4854h

Figure 4-1096. DDRSS_PHY_533 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2200. DDRSS_PHY_533 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT11_2	R/W	0h	Read leveling pattern 11 data for slice 2.

4.4.303 DDRSS_PHY_534 Register (Offset = 4858h) [reset = 0h]

DDRSS_PHY_534 is shown in [Figure 4-1097](#) and described in [Table 4-2202](#).

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Table 4-2201. DDRSS_PHY_534 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4858h

Figure 4-1097. DDRSS_PHY_534 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2202. DDRSS_PHY_534 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT12_2	R/W	0h	Read leveling pattern 12 data for slice 2.

4.4.304 DDRSS_PHY_535 Register (Offset = 485Ch) [reset = 0h]

DDRSS_PHY_535 is shown in [Figure 4-1098](#) and described in [Table 4-2204](#).

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Table 4-2203. DDRSS_PHY_535 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 485Ch

Figure 4-1098. DDRSS_PHY_535 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2204. DDRSS_PHY_535 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT13_2	R/W	0h	Read leveling pattern 13 data for slice 2.

4.4.305 DDRSS_PHY_536 Register (Offset = 4860h) [reset = 0h]

DDRSS_PHY_536 is shown in [Figure 4-1099](#) and described in [Table 4-2206](#).

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Table 4-2205. DDRSS_PHY_536 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4860h

Figure 4-1099. DDRSS_PHY_536 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2206. DDRSS_PHY_536 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT14_2	R/W	0h	Read leveling pattern 14 data for slice 2.

4.4.306 DDRSS_PHY_537 Register (Offset = 4864h) [reset = 0h]

DDRSS_PHY_537 is shown in [Figure 4-1100](#) and described in [Table 4-2208](#).

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Table 4-2207. DDRSS_PHY_537 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4864h

Figure 4-1100. DDRSS_PHY_537 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2208. DDRSS_PHY_537 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT15_2	R/W	0h	Read leveling pattern 15 data for slice 2.

4.4.307 DDRSS_PHY_538 Register (Offset = 4868h) [reset = X]

DDRSS_PHY_538 is shown in [Figure 4-1101](#) and described in [Table 4-2210](#).

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Table 4-2209. DDRSS_PHY_538 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4868h

Figure 4-1101. DDRSS_PHY_538 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_2		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_SELECT_2		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_2		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2210. DDRSS_PHY_538 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_RDDQ_ENC_OBS_SELECT_2	R/W	0h	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ encoded slave delay observation register for slice 2.
23-20	RESERVED	R/W	X	
19-16	PHY_MASTER_DLY_LOCK_OBS_SELECT_2	R/W	0h	Select value to map the internal master delay observation registers to the accessible master delay observation register for slice 2.
15-9	RESERVED	R/W	X	
8	PHY_SW_FIFO_PTR_RST_DISABLE_2	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 2. Set to 1 to disable automatic resets.
7-3	RESERVED	R/W	X	
2-0	PHY_SLAVE_LOOP_CNT_UPDATE_2	R/W	0h	Reserved for future use for slice 2.

4.4.308 DDRSS_PHY_539 Register (Offset = 486Ch) [reset = X]

DDRSS_PHY_539 is shown in Figure 4-1102 and described in Table 4-2212.

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Table 4-2211. DDRSS_PHY_539 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 486Ch

Figure 4-1102. DDRSS_PHY_539 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2212. DDRSS_PHY_539 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_FIFO_PTR_OBS_SELECT_2	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 2.
23-20	RESERVED	R/W	X	
19-16	PHY_WR_SHIFT_OBS_SELECT_2	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 2.
15-12	RESERVED	R/W	X	
11-8	PHY_WR_ENC_OBS_SELECT_2	R/W	0h	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ encoded slave delay observation register for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_DQ_ENC_OBS_SELECT_2	R/W	0h	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible read DQS DQ rise/fall encoded slave delay observation registers for slice 2.

4.4.309 DDRSS_PHY_540 Register (Offset = 4870h) [reset = X]

DDRSS_PHY_540 is shown in Figure 4-1103 and described in Table 4-2214.

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Table 4-2213. DDRSS_PHY_540 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4870h

Figure 4-1103. DDRSS_PHY_540 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_PER_START_2							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_ALGO_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_LVL_DEBUG_CONT_2
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LVL_DEBUG_MODE_2
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2214. DDRSS_PHY_540 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_PER_START_2	R/W	0h	Observation register for write leveling status for slice 2. READ-ONLY
23-18	RESERVED	R/W	X	
17-16	PHY_WRLVL_ALGO_2	R/W	0h	Write leveling algorithm selection for slice 2.
15-9	RESERVED	R/W	X	
8	SC_PHY_LVL_DEBUG_CONT_2	W	0h	Allows the leveling state machine to advance (when in debug mode) for slice 2. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_LVL_DEBUG_MODE_2	R/W	0h	Enables leveling debug mode for slice 2. Set to 1 to enable.

4.4.310 DDRSS_PHY_541 Register (Offset = 4874h) [reset = X]

DDRSS_PHY_541 is shown in [Figure 4-1104](#) and described in [Table 4-2216](#).

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Table 4-2215. DDRSS_PHY_541 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4874h

Figure 4-1104. DDRSS_PHY_541 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_DQ_MASK_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_CAPTURE_CNT_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2216. DDRSS_PHY_541 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_DQ_MASK_2	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 2.
15-12	RESERVED	R/W	X	
11-8	PHY_WRLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during write leveling for slice 2.
7-6	RESERVED	R/W	X	
5-0	PHY_WRLVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each DQS slave delay setting during write leveling for slice 2.

4.4.311 DDRSS_PHY_542 Register (Offset = 4878h) [reset = X]

DDRSS_PHY_542 is shown in Figure 4-1105 and described in Table 4-2218.

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Table 4-2217. DDRSS_PHY_542 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4878h

Figure 4-1105. DDRSS_PHY_542 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_CAPTURE_CNT_2					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_PER_START_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_PER_START_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2218. DDRSS_PHY_542 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_GTLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles + 4 to wait after changing DQS slave delay setting during gate training for slice 2. The valid range is 0x0 to 0xB.
23-22	RESERVED	R/W	X	
21-16	PHY_GTLVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each DQS slave delay setting during gate training for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_PER_START_2	R/W	0h	Value to be added to the current gate delay position as the starting point for periodic gate training for slice 2.

4.4.312 DDRSS_PHY_543 Register (Offset = 487Ch) [reset = X]

DDRSS_PHY_543 is shown in Figure 4-1106 and described in Table 4-2220.

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Table 4-2219. DDRSS_PHY_543 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 487Ch

Figure 4-1106. DDRSS_PHY_543 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_RDDQS_DQ_OBS_SELECT_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_RDLVL_OP_MODE_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_RDLVL_CAPTURE_CNT_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2220. DDRSS_PHY_543 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_2	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 2.
23-18	RESERVED	R/W	X	
17-16	PHY_RDLVL_OP_MODE_2	R/W	0h	Read leveling algorithm select for slice 2. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right.
15-12	RESERVED	R/W	X	
11-8	PHY_RDLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during read leveling for slice 2.
7-6	RESERVED	R/W	X	
5-0	PHY_RDLVL_CAPTURE_CNT_2	R/W	0h	Number of samples to take at each DQS slave delay setting during read leveling for slice 2.

4.4.313 DDRSS_PHY_544 Register (Offset = 4880h) [reset = X]

DDRSS_PHY_544 is shown in Figure 4-1107 and described in Table 4-2222.

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Table 4-2221. DDRSS_PHY_544 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4880h

Figure 4-1107. DDRSS_PHY_544 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_WDQLVL_BURST_CNT_2					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
PHY_WDQLVL_CLK_JITTER_TOLERANCE_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_DATA_MASK_2							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_SELECT_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2222. DDRSS_PHY_544 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_WDQLVL_BURST_CNT_2	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 2.
23-16	PHY_WDQLVL_CLK_JITTER_TOLERANCE_2	R/W	0h	Defines the minimum gap requirement for the LE and TE window for slice 2.
15-8	PHY_RDLVL_DATA_MASK_2	R/W	0h	Per-bit mask for read leveling for slice 2. If all bits are not used, only 1 bit should be cleared to 0.
7-0	PHY_RDLVL_PERIODIC_OBS_SELECT_2	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during periodic read leveling for slice 2.

4.4.314 DDRSS_PHY_545 Register (Offset = 4884h) [reset = X]

DDRSS_PHY_545 is shown in [Figure 4-1108](#) and described in [Table 4-2224](#).

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Table 4-2223. DDRSS_PHY_545 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4884h

Figure 4-1108. DDRSS_PHY_545 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_PATT_2		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2224. DDRSS_PHY_545 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_WDQLVL_UPDT_WAIT_CNT_2	R/W	0h	Number of cycles to wait after changing the DQ slave delay setting during write data leveling for slice 2.
23-19	RESERVED	R/W	X	
18-8	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 2.
7-3	RESERVED	R/W	X	
2-0	PHY_WDQLVL_PATT_2	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 2. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen.

4.4.315 DDRSS_PHY_546 Register (Offset = 4888h) [reset = X]

DDRSS_PHY_546 is shown in Figure 4-1109 and described in Table 4-2226.

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Table 4-2225. DDRSS_PHY_546 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4888h

Figure 4-1109. DDRSS_PHY_546 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_WDQ LVL_CLR_PRE V_RESULTS_2
R/W-X							W-0h
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_SELECT_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2226. DDRSS_PHY_546 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	SC_PHY_WDQLVL_CLR_PREV_RESULTS_2	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 2. Set to 1 to trigger. WRITE-ONLY
15-8	PHY_WDQLVL_PERIODIC_OBS_SELECT_2	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_WDQLVL_DQDM_OBS_SELECT_2	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 2.

4.4.316 DDRSS_PHY_547 Register (Offset = 488Ch) [reset = X]

DDRSS_PHY_547 is shown in [Figure 4-1110](#) and described in [Table 4-2228](#).

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Table 4-2227. DDRSS_PHY_547 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 488Ch

Figure 4-1110. DDRSS_PHY_547 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_WDQLVL_DATADM_MASK_2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2228. DDRSS_PHY_547 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_WDQLVL_DATADM_MASK_2	R/W	0h	Per-bit mask for write data leveling for slice 2. Set to 1 to mask any bit from the leveling process.

4.4.317 DDRSS_PHY_548 Register (Offset = 4890h) [reset = 0h]

DDRSS_PHY_548 is shown in [Figure 4-1111](#) and described in [Table 4-2230](#).

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Table 4-2229. DDRSS_PHY_548 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4890h

Figure 4-1111. DDRSS_PHY_548 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT0_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2230. DDRSS_PHY_548 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT0_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 3 to 0 written/read from device.

4.4.318 DDRSS_PHY_549 Register (Offset = 4894h) [reset = 0h]

DDRSS_PHY_549 is shown in [Figure 4-1112](#) and described in [Table 4-2232](#).

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Table 4-2231. DDRSS_PHY_549 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4894h

Figure 4-1112. DDRSS_PHY_549 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT1_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2232. DDRSS_PHY_549 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT1_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 7 to 4 written/read from device.

4.4.319 DDRSS_PHY_550 Register (Offset = 4898h) [reset = 0h]

DDRSS_PHY_550 is shown in [Figure 4-1113](#) and described in [Table 4-2234](#).

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Table 4-2233. DDRSS_PHY_550 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4898h

Figure 4-1113. DDRSS_PHY_550 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT2_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2234. DDRSS_PHY_550 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT2_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 11 to 8 written/read from device.

4.4.320 DDRSS_PHY_551 Register (Offset = 489Ch) [reset = 0h]

DDRSS_PHY_551 is shown in [Figure 4-1114](#) and described in [Table 4-2236](#).

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Table 4-2235. DDRSS_PHY_551 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 489Ch

Figure 4-1114. DDRSS_PHY_551 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT3_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2236. DDRSS_PHY_551 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT3_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 15 to 12 written/read from device.

4.4.321 DDRSS_PHY_552 Register (Offset = 48A0h) [reset = X]

DDRSS_PHY_552 is shown in [Figure 4-1115](#) and described in [Table 4-2238](#).

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Table 4-2237. DDRSS_PHY_552 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48A0h

Figure 4-1115. DDRSS_PHY_552 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_MULT_TRAIN_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_USER_PATT4_2							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT4_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2238. DDRSS_PHY_552 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_NTP_MULT_TRAIN_2	R/W	0h	Control for single pass only No-Topology training for slice 2.
15-0	PHY_USER_PATT4_2	R/W	0h	User-defined pattern to be used during write data leveling for slice 2. This register holds the DM bit for the 15 to 0 DQ written/read from device.

4.4.322 DDRSS_PHY_553 Register (Offset = 48A4h) [reset = X]

DDRSS_PHY_553 is shown in [Figure 4-1116](#) and described in [Table 4-2240](#).

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Table 4-2239. DDRSS_PHY_553 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48A4h

Figure 4-1116. DDRSS_PHY_553 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_EARLY_THRESHOLD_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2240. DDRSS_PHY_553 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_2	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_EARLY_THRESHOLD_2	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 2.

4.4.323 DDRSS_PHY_554 Register (Offset = 48A8h) [reset = X]

DDRSS_PHY_554 is shown in [Figure 4-1117](#) and described in [Table 4-2242](#).

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Table 4-2241. DDRSS_PHY_554 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48A8h

Figure 4-1117. DDRSS_PHY_554 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2242. DDRSS_PHY_554 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_MAX_2	R/W	0h	Maximum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_PERIOD_THRESHOLD_MIN_2	R/W	0h	Minimum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 2.

4.4.324 DDRSS_PHY_555 Register (Offset = 48ACh) [reset = X]

DDRSS_PHY_555 is shown in Figure 4-1118 and described in Table 4-2244.

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Table 4-2243. DDRSS_PHY_555 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48ACh

Figure 4-1118. DDRSS_PHY_555 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_2							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_2					
R/W-X		W-0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_2
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2244. DDRSS_PHY_555 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_FIFO_PTR_OBS_2	R	0h	Observation register containing read entry FIFO pointers for slice 2. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	SC_PHY_MANUAL_CLEAR_2	W	0h	Manual reset/clear of internal logic for slice 2. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/max lock values. Bit (3) is manual reset of master delay unlock counter. Bit (4) is reset of leveling error bit in the leveling status registers. Bit (5) is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_CALVL_VREF_DRIVING_SLICE_2	R/W	0h	Indicates if slice 2 is used to drive the VREF value to the device during CA training.

4.4.325 DDRSS_PHY_556 Register (Offset = 48B0h) [reset = 00100000h]

DDRSS_PHY_556 is shown in [Figure 4-1119](#) and described in [Table 4-2246](#).

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Table 4-2245. DDRSS_PHY_556 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48B0h

Figure 4-1119. DDRSS_PHY_556 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_2																															
R-00100000h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2246. DDRSS_PHY_556 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_LPBK_RESULT_OBS_2	R	00100000h	Observation register containing loopback status/results for slice 2. READ-ONLY

4.4.326 DDRSS_PHY_557 Register (Offset = 48B4h) [reset = X]

DDRSS_PHY_557 is shown in [Figure 4-1120](#) and described in [Table 4-2248](#).

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Table 4-2247. DDRSS_PHY_557 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48B4h

Figure 4-1120. DDRSS_PHY_557 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_2										
R-X					R-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_ERROR_COUNT_OBS_2															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2248. DDRSS_PHY_557 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_MASTER_DLY_LOCK_OBS_2	R	0h	Observation register containing master delay results for slice 2. READ-ONLY
15-0	PHY_LPBK_ERROR_COUNT_OBS_2	R	0h	Observation register containing total number of loopback error data for slice 2. READ-ONLY

4.4.327 DDRSS_PHY_558 Register (Offset = 48B8h) [reset = X]

DDRSS_PHY_558 is shown in Figure 4-1121 and described in Table 4-2250.

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Table 4-2249. DDRSS_PHY_558 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48B8h

Figure 4-1121. DDRSS_PHY_558 Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_2							
R-0h							
23	22	21	20	19	18	17	16
PHY_MEAS_DLY_STEP_VALUE_2							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_2						
R-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_2						
R-X	R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 4-2250. DDRSS_PHY_558 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS DQ rising edge adder slave delay encoded value for slice 2. READ-ONLY
23-16	PHY_MEAS_DLY_STEP_VALUE_2	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with denominator of 512, for slice 2. READ-ONLY
15	RESERVED	R	X	
14-8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS base slave delay encoded value for slice 2. READ-ONLY
7	RESERVED	R	X	
6-0	PHY_RDDQ_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQ slave delay encoded values for slice 2. READ-ONLY

4.4.328 DDRSS_PHY_559 Register (Offset = 48BCh) [reset = X]

DDRSS_PHY_559 is shown in Figure 4-1122 and described in Table 4-2252.

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Table 4-2251. DDRSS_PHY_559 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48BCh

Figure 4-1122. DDRSS_PHY_559 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_2						
R-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2	
R-X						R-0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2							
R-0h							
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_2							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2252. DDRSS_PHY_559 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	X	
30-24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing write DQS base slave delay encoded value for slice 2. READ-ONLY
23-19	RESERVED	R	X	
18-8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS gate slave delay encoded value for slice 2. READ-ONLY
7-0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing read DQS DQ falling edge adder slave delay encoded value for slice 2. READ-ONLY

4.4.329 DDRSS_PHY_560 Register (Offset = 48C0h) [reset = X]

DDRSS_PHY_560 is shown in Figure 4-1123 and described in Table 4-2254.

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Table 4-2253. DDRSS_PHY_560 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48C0h

Figure 4-1123. DDRSS_PHY_560 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WR_SHIFT_OBS_2		
R-X					R-0h		
15	14	13	12	11	10	9	8
PHY_WR_ADDER_SLV_DLY_ENC_OBS_2							
R-0h							
7	6	5	4	3	2	1	0
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_2							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2254. DDRSS_PHY_560 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18-16	PHY_WR_SHIFT_OBS_2	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 2. READ-ONLY
15-8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing write adder slave delay encoded value for slice 2. READ-ONLY
7-0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing write DQ base slave delay encoded value for slice 2. READ-ONLY

4.4.330 DDRSS_PHY_561 Register (Offset = 48C4h) [reset = X]

DDRSS_PHY_561 is shown in [Figure 4-1124](#) and described in [Table 4-2256](#).

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Table 4-2255. DDRSS_PHY_561 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48C4h

Figure 4-1124. DDRSS_PHY_561 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_2									
R-X						R-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_2									
R-X						R-0h									

LEGEND: R = Read Only; -n = value after reset

Table 4-2256. DDRSS_PHY_561 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_WRLVL_HARD1_DELAY_OBS_2	R	0h	Observation register containing write leveling first hard 1 DQS slave delay for slice 2. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_WRLVL_HARD0_DELAY_OBS_2	R	0h	Observation register containing write leveling last hard 0 DQS slave delay for slice 2. READ-ONLY

4.4.331 DDRSS_PHY_562 Register (Offset = 48C8h) [reset = X]

DDRSS_PHY_562 is shown in [Figure 4-1125](#) and described in [Table 4-2258](#).

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Table 4-2257. DDRSS_PHY_562 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48C8h

Figure 4-1125. DDRSS_PHY_562 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PHY_WRLVL_STATUS_OBS_2
R-X															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_2															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2258. DDRSS_PHY_562 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-0	PHY_WRLVL_STATUS_OBS_2	R	0h	Observation register containing write leveling status for slice 2. READ-ONLY

4.4.332 DDRSS_PHY_563 Register (Offset = 48CCh) [reset = X]

DDRSS_PHY_563 is shown in [Figure 4-1126](#) and described in [Table 4-2260](#).

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Table 4-2259. DDRSS_PHY_563 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48CCh

Figure 4-1126. DDRSS_PHY_563 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2260. DDRSS_PHY_563 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing gate sample2 slave delay encoded values for slice 2. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2	R	0h	Observation register containing gate sample1 slave delay encoded values for slice 2. READ-ONLY

4.4.333 DDRSS_PHY_564 Register (Offset = 48D0h) [reset = X]

DDRSS_PHY_564 is shown in Figure 4-1127 and described in Table 4-2262.

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Table 4-2261. DDRSS_PHY_564 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48D0h

Figure 4-1127. DDRSS_PHY_564 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_2													
R-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_ERROR_OBS_2															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2262. DDRSS_PHY_564 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-16	PHY_GTLVL_HARD0_DELAY_OBS_2	R	0h	Observation register containing gate training first hard 0 DQS slave delay for slice 2. READ-ONLY
15-0	PHY_WRLVL_ERROR_OBS_2	R	0h	Observation register containing write leveling error status for slice 2. READ-ONLY

4.4.334 DDRSS_PHY_565 Register (Offset = 48D4h) [reset = X]

DDRSS_PHY_565 is shown in [Figure 4-1128](#) and described in [Table 4-2264](#).

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Table 4-2263. DDRSS_PHY_565 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48D4h

Figure 4-1128. DDRSS_PHY_565 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_2													
R-X		R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 4-2264. DDRSS_PHY_565 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	X	
13-0	PHY_GTLVL_HARD1_DELAY_OBS_2	R	0h	Observation register containing gate training last hard 1 DQS slave delay for slice 2. READ-ONLY

4.4.335 DDRSS_PHY_566 Register (Offset = 48D8h) [reset = X]

DDRSS_PHY_566 is shown in [Figure 4-1129](#) and described in [Table 4-2266](#).

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Table 4-2265. DDRSS_PHY_566 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48D8h

Figure 4-1129. DDRSS_PHY_566 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													PHY_GTLVL_STATUS_OBS_2		
R-X													R-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_2															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2266. DDRSS_PHY_566 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	PHY_GTLVL_STATUS_OBS_2	R	0h	Observation register containing gate training status for slice 2. READ-ONLY

4.4.336 DDRSS_PHY_567 Register (Offset = 48DCh) [reset = X]

DDRSS_PHY_567 is shown in Figure 4-1130 and described in Table 4-2268.

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Table 4-2267. DDRSS_PHY_567 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48DCh

Figure 4-1130. DDRSS_PHY_567 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2268. DDRSS_PHY_567 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2	R	0h	Observation register containing read leveling data window trailing edge slave delay setting for slice 2. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2	R	0h	Observation register containing read leveling data window leading edge slave delay setting for slice 2. READ-ONLY

4.4.337 DDRSS_PHY_568 Register (Offset = 48E0h) [reset = X]

DDRSS_PHY_568 is shown in [Figure 4-1131](#) and described in [Table 4-2270](#).

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Table 4-2269. DDRSS_PHY_568 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48E0h

Figure 4-1131. DDRSS_PHY_568 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM _WINDOWS_OBS_2	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-2270. DDRSS_PHY_568 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1-0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_2	R	0h	Observation register containing read leveling number of windows found for slice 2. READ-ONLY

4.4.338 DDRSS_PHY_569 Register (Offset = 48E4h) [reset = 0h]

DDRSS_PHY_569 is shown in [Figure 4-1132](#) and described in [Table 4-2272](#).

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Table 4-2271. DDRSS_PHY_569 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48E4h

Figure 4-1132. DDRSS_PHY_569 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2272. DDRSS_PHY_569 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_STATUS_OBS_2	R	0h	Observation register containing read leveling status for slice 2. READ-ONLY

4.4.339 DDRSS_PHY_570 Register (Offset = 48E8h) [reset = 0h]

DDRSS_PHY_570 is shown in [Figure 4-1133](#) and described in [Table 4-2274](#).

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Table 4-2273. DDRSS_PHY_570 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48E8h

Figure 4-1133. DDRSS_PHY_570 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2274. DDRSS_PHY_570 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PERIODIC_OBS_2	R	0h	Observation register containing periodic read leveling status for slice 2. READ-ONLY

4.4.340 DDRSS_PHY_571 Register (Offset = 48ECh) [reset = X]

DDRSS_PHY_571 is shown in [Figure 4-1134](#) and described in [Table 4-2276](#).

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Table 4-2275. DDRSS_PHY_571 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48ECh

Figure 4-1134. DDRSS_PHY_571 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_2										
R-X					R-7FFh										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_2										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 4-2276. DDRSS_PHY_571 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_WDQLVL_DQDM_TE_DLY_OBS_2	R	7FFh	Observation register containing write data leveling data window trailing edge slave delay setting for slice 2. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_WDQLVL_DQDM_LE_DLY_OBS_2	R	0h	Observation register containing write data leveling data window leading edge slave delay setting for slice 2. READ-ONLY

4.4.341 DDRSS_PHY_572 Register (Offset = 48F0h) [reset = 0h]

DDRSS_PHY_572 is shown in [Figure 4-1135](#) and described in [Table 4-2278](#).

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Table 4-2277. DDRSS_PHY_572 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48F0h

Figure 4-1135. DDRSS_PHY_572 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2278. DDRSS_PHY_572 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_STATUS_OBS_2	R	0h	Observation register containing write data leveling status for slice 2. READ-ONLY

4.4.342 DDRSS_PHY_573 Register (Offset = 48F4h) [reset = 0h]

DDRSS_PHY_573 is shown in [Figure 4-1136](#) and described in [Table 4-2280](#).

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Table 4-2279. DDRSS_PHY_573 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48F4h

Figure 4-1136. DDRSS_PHY_573 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2280. DDRSS_PHY_573 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_PERIODIC_OBS_2	R	0h	Observation register containing periodic write data leveling status for slice 2. READ-ONLY

4.4.343 DDRSS_PHY_574 Register (Offset = 48F8h) [reset = X]

DDRSS_PHY_574 is shown in [Figure 4-1137](#) and described in [Table 4-2282](#).

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Table 4-2281. DDRSS_PHY_574 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48F8h

Figure 4-1137. DDRSS_PHY_574 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE SE RV ED	PHY_DDL_MODE_2																														
R/ W- X	R/W-0h																														

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2282. DDRSS_PHY_574 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-0	PHY_DDL_MODE_2	R/W	0h	DDL mode for slice 2.

4.4.344 DDRSS_PHY_575 Register (Offset = 48FCh) [reset = X]

DDRSS_PHY_575 is shown in [Figure 4-1138](#) and described in [Table 4-2284](#).

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Table 4-2283. DDRSS_PHY_575 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 48FCh

Figure 4-1138. DDRSS_PHY_575 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PHY_DDL_MASK_2					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2284. DDRSS_PHY_575 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	PHY_DDL_MASK_2	R/W	0h	DDL mask for slice 2.

4.4.345 DDRSS_PHY_576 Register (Offset = 4900h) [reset = 0h]

DDRSS_PHY_576 is shown in [Figure 4-1139](#) and described in [Table 4-2286](#).

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Table 4-2285. DDRSS_PHY_576 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4900h

Figure 4-1139. DDRSS_PHY_576 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2286. DDRSS_PHY_576 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_OBS_2	R	0h	DDL test observation for slice 2. READ-ONLY

4.4.346 DDRSS_PHY_577 Register (Offset = 4904h) [reset = 0h]

DDRSS_PHY_577 is shown in [Figure 4-1140](#) and described in [Table 4-2288](#).

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Table 4-2287. DDRSS_PHY_577 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4904h

Figure 4-1140. DDRSS_PHY_577 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2288. DDRSS_PHY_577 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_MSTR_DLY_OBS_2	R	0h	DDL test observation delays for slice 2 master DDL. READ-ONLY

4.4.347 DDRSS_PHY_578 Register (Offset = 4908h) [reset = X]

DDRSS_PHY_578 is shown in [Figure 4-1141](#) and described in [Table 4-2290](#).

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Table 4-2289. DDRSS_PHY_578 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4908h

Figure 4-1141. DDRSS_PHY_578 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_OVERRIDE_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_RX_CAL_START_2
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2290. DDRSS_PHY_578 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_OVERRIDE_2	R/W	0h	Manual setting of RX Calibration enable for slice 2.
23-17	RESERVED	R/W	X	
16	SC_PHY_RX_CAL_START_2	W	0h	Manual RX Calibration start for slice 2. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	PHY_LP4_WDQS_OE_EXTEND_2	R/W	0h	LPDDR4 write preamble extension enable for slice 2.
7-0	PHY_DDL_TRACK_UPD_THRESHOLD_2	R/W	0h	Specify threshold value for PHY init update tracking for slice 2.

4.4.348 DDRSS_PHY_579 Register (Offset = 490Ch) [reset = X]

DDRSS_PHY_579 is shown in Figure 4-1142 and described in Table 4-2292.

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Table 4-2291. DDRSS_PHY_579 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 490Ch

Figure 4-1142. DDRSS_PHY_579 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_SAMPLE_WAIT_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2292. DDRSS_PHY_579 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ0_2	R/W	0h	RX Calibration codes for DQ0 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8	PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_2	R/W	0h	Data slice power reduction disable for slice 2.
7-0	PHY_RX_CAL_SAMPLE_WAIT_2	R/W	0h	RX Calibration state machine wait count for slice 2.

4.4.349 DDRSS_PHY_580 Register (Offset = 4910h) [reset = X]

DDRSS_PHY_580 is shown in [Figure 4-1143](#) and described in [Table 4-2294](#).

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Table 4-2293. DDRSS_PHY_580 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4910h

Figure 4-1143. DDRSS_PHY_580 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ2_2							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ1_2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2294. DDRSS_PHY_580 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ2_2	R/W	0h	RX Calibration codes for DQ2 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ1_2	R/W	0h	RX Calibration codes for DQ1 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.350 DDRSS_PHY_581 Register (Offset = 4914h) [reset = X]

DDRSS_PHY_581 is shown in Figure 4-1144 and described in Table 4-2296.

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Table 4-2295. DDRSS_PHY_581 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4914h

Figure 4-1144. DDRSS_PHY_581 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ4_2							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ3_2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2296. DDRSS_PHY_581 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ4_2	R/W	0h	RX Calibration codes for DQ4 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ3_2	R/W	0h	RX Calibration codes for DQ3 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.351 DDRSS_PHY_582 Register (Offset = 4918h) [reset = X]

DDRSS_PHY_582 is shown in [Figure 4-1145](#) and described in [Table 4-2298](#).

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Table 4-2297. DDRSS_PHY_582 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4918h

Figure 4-1145. DDRSS_PHY_582 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ6_2							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ5_2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2298. DDRSS_PHY_582 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ6_2	R/W	0h	RX Calibration codes for DQ6 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ5_2	R/W	0h	RX Calibration codes for DQ5 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.352 DDRSS_PHY_583 Register (Offset = 491Ch) [reset = X]

DDRSS_PHY_583 is shown in [Figure 4-1146](#) and described in [Table 4-2300](#).

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Table 4-2299. DDRSS_PHY_583 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 491Ch

Figure 4-1146. DDRSS_PHY_583 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ7_2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2300. DDRSS_PHY_583 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ7_2	R/W	0h	RX Calibration codes for DQ7 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.353 DDRSS_PHY_584 Register (Offset = 4920h) [reset = X]

DDRSS_PHY_584 is shown in [Figure 4-1147](#) and described in [Table 4-2302](#).

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Table 4-2301. DDRSS_PHY_584 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4920h

Figure 4-1147. DDRSS_PHY_584 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_RX_CAL_DM_2																	
R/W-X														R/W-0h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2302. DDRSS_PHY_584 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_RX_CAL_DM_2	R/W	0h	<p>RX Calibration codes for DM for slice 2.</p> <p>Bits (5:0) contain rx_cal_code_down.</p> <p>Bits (11:6) contain rx_cal_code_up.</p> <p>Bits (17:12) contain rx_cal_code2_down.</p> <p>Bits (23:18) contain rx_cal_code2_up.</p>

4.4.354 DDRSS_PHY_585 Register (Offset = 4924h) [reset = X]

DDRSS_PHY_585 is shown in Figure 4-1148 and described in Table 4-2304.

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Table 4-2303. DDRSS_PHY_585 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4924h

Figure 4-1148. DDRSS_PHY_585 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_FDBK_2							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQS_2							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2304. DDRSS_PHY_585 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_FDBK_2	R/W	0h	RX Calibration codes for FDBK for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQS_2	R/W	0h	RX Calibration codes for DQS for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.355 DDRSS_PHY_586 Register (Offset = 4928h) [reset = X]

DDRSS_PHY_586 is shown in [Figure 4-1149](#) and described in [Table 4-2306](#).

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Table 4-2305. DDRSS_PHY_586 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4928h

Figure 4-1149. DDRSS_PHY_586 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_LOCK_OBS_2							
R-X								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_OBS_2							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2306. DDRSS_PHY_586 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	X	
24-16	PHY_RX_CAL_LOCK_OBS_2	R	0h	RX Calibration lock results for slice 2. Bit (3:0) is the state machine rx_cal_sm. Bit (4) is the rx_cal_done signal. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_RX_CAL_OBS_2	R	0h	RX Calibration results for slice 2. Bits (7:0) contain calibration results from DQ 0-7. Bit (8) contains calibration result from DM. Bit (9) contains calibration result from DQS. Bit (10) contains calibration result from FDBK. READ-ONLY

4.4.356 DDRSS_PHY_587 Register (Offset = 492Ch) [reset = X]

DDRSS_PHY_587 is shown in Figure 4-1150 and described in Table 4-2308.

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Table 4-2307. DDRSS_PHY_587 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 492Ch

Figure 4-1150. DDRSS_PHY_587 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_COMP_VAL_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED	PHY_RX_CAL_DIFF_ADJUST_2						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_RX_CAL_SE_ADJUST_2						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RX_CAL_DISABLE_2
R/W-X							R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2308. DDRSS_PHY_587 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_COMP_VAL_2	R/W	0h	Expected C value from RX pad for slice 2.
23	RESERVED	R/W	X	
22-16	PHY_RX_CAL_DIFF_ADJUST_2	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 2.
15	RESERVED	R/W	X	
14-8	PHY_RX_CAL_SE_ADJUST_2	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_RX_CAL_DISABLE_2	R/W	1h	RX CAL disable signal for slice 2, set 1 to bypass the rx calibration

4.4.357 DDRSS_PHY_588 Register (Offset = 4930h) [reset = X]

DDRSS_PHY_588 is shown in [Figure 4-1151](#) and described in [Table 4-2310](#).

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Table 4-2309. DDRSS_PHY_588 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4930h

Figure 4-1151. DDRSS_PHY_588 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_PAD_RX_BIAS_EN_2										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_RX_CAL_INDEX_MASK_2										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2310. DDRSS_PHY_588 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PAD_RX_BIAS_EN_2	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 2.
15-12	RESERVED	R/W	X	
11-0	PHY_RX_CAL_INDEX_MASK_2	R/W	0h	RX offset calibration mask of all RX pad for slice 2.

4.4.358 DDRSS_PHY_589 Register (Offset = 4934h) [reset = X]

DDRSS_PHY_589 is shown in Figure 4-1152 and described in Table 4-2312.

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Table 4-2311. DDRSS_PHY_589 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4934h

Figure 4-1152. DDRSS_PHY_589 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_DATA_DC_WEIGHT_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DATA_DC_CAL_TIMEOUT_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_CAL_SAMPLE_WAIT_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_STATIC_TOG_DISABLE_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2312. DDRSS_PHY_589 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_DATA_DC_WEIGHT_2	R/W	0h	Determines weight of average calculating for slice 2.
23-16	PHY_DATA_DC_CAL_TIMEOUT_2	R/W	0h	Determines timeout number of iteration for slice 2.
15-8	PHY_DATA_DC_CAL_SAMPLE_WAIT_2	R/W	0h	Determines number of cycles to wait for each sample for slice 2.
7-5	RESERVED	R/W	X	
4-0	PHY_STATIC_TOG_DISABLE_2	R/W	0h	Control to disable toggle during static activity for slice 2. bit 0: Write path delay line disable bit 1: Read path delay line disable bit 2: Read data path disable bit 3: clk_phy disable bit 4: master delay line disable.

4.4.359 DDRSS_PHY_590 Register (Offset = 4938h) [reset = X]

DDRSS_PHY_590 is shown in Figure 4-1153 and described in Table 4-2314.

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Table 4-2313. DDRSS_PHY_590 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4938h

Figure 4-1153. DDRSS_PHY_590 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_DATA_DC_ADJUST_THRSHLD_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_ADJUST_SAMPLE_CNT_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DATA_DC_ADJUST_START_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2314. DDRSS_PHY_590 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_DATA_DC_ADJUST_DIRECT_2	R/W	0h	Adjust direction for slice 2.
23-16	PHY_DATA_DC_ADJUST_THRSHLD_2	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 2.
15-8	PHY_DATA_DC_ADJUST_SAMPLE_CNT_2	R/W	0h	Duty cycle adjust sample count for slice 2.
7-6	RESERVED	R/W	X	
5-0	PHY_DATA_DC_ADJUST_START_2	R/W	0h	Duty cycle adjust starting value for slice 2.

4.4.360 DDRSS_PHY_591 Register (Offset = 493Ch) [reset = X]

DDRSS_PHY_591 is shown in Figure 4-1154 and described in Table 4-2316.

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Table 4-2315. DDRSS_PHY_591 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 493Ch

Figure 4-1154. DDRSS_PHY_591 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_FDBK_PWR_CTRL_2		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_SW_RANK_2	
R/W-X						R/W-1h	
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_CAL_START_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_CAL_POLARITY_2
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2316. DDRSS_PHY_591 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_FDBK_PWR_CTRL_2	R/W	0h	Shutoff gate feedback IO to reduce power for slice 2.
23-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_SW_RANK_2	R/W	1h	Rank selection for software based duty cycle correction for slice 2.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_CAL_START_2	R/W	0h	Manual trigger for DCC for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_CAL_POLARITY_2	R/W	0h	Calibration polarity for slice 2.

4.4.361 DDRSS_PHY_592 Register (Offset = 4940h) [reset = X]

DDRSS_PHY_592 is shown in Figure 4-1155 and described in Table 4-2318.

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Table 4-2317. DDRSS_PHY_592 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4940h

Figure 4-1155. DDRSS_PHY_592 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_RDPATH_GATE_DISABLE_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_2
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2318. DDRSS_PHY_592 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SLICE_PWR_RDC_DISABLE_2	R/W	0h	Data slice power reduction disable for slice 2.
23-17	RESERVED	R/W	X	
16	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_2	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 2.
15-9	RESERVED	R/W	X	
8	PHY_RDPATH_GATE_DISABLE_2	R/W	0h	Data slice read path power reduction disable for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_SLV_DLY_CTRL_GATE_DISABLE_2	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 2.

4.4.362 DDRSS_PHY_593 Register (Offset = 4944h) [reset = X]

DDRSS_PHY_593 is shown in [Figure 4-1156](#) and described in [Table 4-2320](#).

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Table 4-2319. DDRSS_PHY_593 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4944h

Figure 4-1156. DDRSS_PHY_593 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_DS_FSM_ERROR_INFO_2													
R/W-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_PARITY_ERROR_REGIF_2										
R/W-X					R/W-0h										

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2320. DDRSS_PHY_593 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_DS_FSM_ERROR_INFO_2	R	0h	Data slice level FSM Error Info for slice 2. READ-ONLY
15-11	RESERVED	R/W	X	
10-0	PHY_PARITY_ERROR_REGIF_2	R/W	0h	Inject parity error to register interface signals for slice 2.

4.4.363 DDRSS_PHY_594 Register (Offset = 4948h) [reset = X]

DDRSS_PHY_594 is shown in Figure 4-1157 and described in Table 4-2322.

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Table 4-2321. DDRSS_PHY_594 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4948h

Figure 4-1157. DDRSS_PHY_594 Register

31	30	29	28	27	26	25	24
RESERVED		SC_PHY_DS_FSM_ERROR_INFO_WOCLR_2					
R/W-X		W-0h					
23	22	21	20	19	18	17	16
SC_PHY_DS_FSM_ERROR_INFO_WOCLR_2							
W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_DS_FSM_ERROR_INFO_MASK_2					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
PHY_DS_FSM_ERROR_INFO_MASK_2							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2322. DDRSS_PHY_594 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	SC_PHY_DS_FSM_ERROR_INFO_WOCLR_2	W	0h	Data slice level FSM Error Info for slice 2. WRITE-ONLY
15-14	RESERVED	R/W	X	
13-0	PHY_DS_FSM_ERROR_INFO_MASK_2	R/W	0h	Data slice level FSM Error Info Mask for slice 2.

4.4.364 DDRSS_PHY_595 Register (Offset = 494Ch) [reset = X]

DDRSS_PHY_595 is shown in [Figure 4-1158](#) and described in [Table 4-2324](#).

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Table 4-2323. DDRSS_PHY_595 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 494Ch

Figure 4-1158. DDRSS_PHY_595 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_2			
R/W-X				W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_2			
R/W-X				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2324. DDRSS_PHY_595 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_2	W	0h	Data slice level training/calibration Error Info for slice 2. WRITE-ONLY
15-13	RESERVED	R/W	X	
12-8	PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_2	R/W	0h	Data slice level training/calibration Error Info Mask for slice 2.
7-5	RESERVED	R/W	X	
4-0	PHY_DS_TRAIN_CALIB_ERROR_INFO_2	R	0h	Data slice level training/calibration Error Info for slice 2. READ-ONLY

4.4.365 DDRSS_PHY_596 Register (Offset = 4950h) [reset = X]

DDRSS_PHY_596 is shown in [Figure 4-1159](#) and described in [Table 4-2326](#).

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Table 4-2325. DDRSS_PHY_596 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4950h

Figure 4-1159. DDRSS_PHY_596 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_2		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DQ_TSEL_SELECT_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_TSEL_SELECT_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_DQ_TSEL_ENABLE_2		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2326. DDRSS_PHY_596 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_DQS_TSEL_ENABLE_2	R/W	0h	Operation type tsel enables for DQS signals for slice 2. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.
23-8	PHY_DQ_TSEL_SELECT_2	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 2.
7-3	RESERVED	R/W	X	
2-0	PHY_DQ_TSEL_ENABLE_2	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 2. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.

4.4.366 DDRSS_PHY_597 Register (Offset = 4954h) [reset = X]

DDRSS_PHY_597 is shown in Figure 4-1160 and described in Table 4-2328.

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Table 4-2327. DDRSS_PHY_597 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4954h

Figure 4-1160. DDRSS_PHY_597 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_2						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_2							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2328. DDRSS_PHY_597 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PHY_VREF_INITIAL_START_POINT_2	R/W	0h	Data slice initial VREF training start value for slice 2.
23-18	RESERVED	R/W	X	
17-16	PHY_TWO_CYC_PREAMBLE_2	R/W	0h	2 cycle preamble support for slice 2. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2 cycle write preamble. Set each bit to 1 to enable.
15-0	PHY_DQS_TSEL_SELECT_2	R/W	0h	Operation type tsel select values for DQS signals for slice 2.

4.4.367 DDRSS_PHY_598 Register (Offset = 4958h) [reset = X]

DDRSS_PHY_598 is shown in [Figure 4-1161](#) and described in [Table 4-2330](#).

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Table 4-2329. DDRSS_PHY_598 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4958h

Figure 4-1161. DDRSS_PHY_598 Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_2							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_2						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2330. DDRSS_PHY_598 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_NTP_WDQ_STEP_SIZE_2	R/W	0h	Step size of WR DQ slave delay during No-Topology training for slice 2.
23-17	RESERVED	R/W	X	
16	PHY_NTP_TRAIN_EN_2	R/W	0h	Enable for No-Topology training for slice 2.
15-10	RESERVED	R/W	X	
9-8	PHY_VREF_TRAINING_CTRL_2	R/W	0h	Data slice vref training enable control for slice 2.
7	RESERVED	R/W	X	
6-0	PHY_VREF_INITIAL_STOP_POINT_2	R/W	0h	Data slice initial VREF training stop value for slice 2.

4.4.368 DDRSS_PHY_599 Register (Offset = 495Ch) [reset = X]

DDRSS_PHY_599 is shown in [Figure 4-1162](#) and described in [Table 4-2332](#).

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Table 4-2331. DDRSS_PHY_599 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 495Ch

Figure 4-1162. DDRSS_PHY_599 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_NTP_WDQ_STOP_2										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_NTP_WDQ_START_2										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2332. DDRSS_PHY_599 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_NTP_WDQ_STOP_2	R/W	0h	End of WR DQ slave delay in No-Topology training for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_NTP_WDQ_START_2	R/W	0h	Starting WR DQ slave delay in No-Topology training for slice 2.

4.4.369 DDRSS_PHY_600 Register (Offset = 4960h) [reset = X]

DDRSS_PHY_600 is shown in Figure 4-1163 and described in Table 4-2334.

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Table 4-2333. DDRSS_PHY_600 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4960h

Figure 4-1163. DDRSS_PHY_600 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQ_LVL_DVW_MIN_EN_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_WDQLVL_DVW_MIN_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_WDQLVL_DVW_MIN_2							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_BIT_EN_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2334. DDRSS_PHY_600 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SW_WDQLVL_DVW_MIN_EN_2	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 2.
23-18	RESERVED	R/W	X	
17-8	PHY_WDQLVL_DVW_MIN_2	R/W	0h	Minimum data valid window across DQs and ranks for slice 2.
7-0	PHY_NTP_WDQ_BIT_EN_2	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 2.

4.4.370 DDRSS_PHY_601 Register (Offset = 4964h) [reset = X]

DDRSS_PHY_601 is shown in [Figure 4-1164](#) and described in [Table 4-2336](#).

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Table 4-2335. DDRSS_PHY_601 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4964h

Figure 4-1164. DDRSS_PHY_601 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_0_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_TX_DCD_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2336. DDRSS_PHY_601 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_0_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_TX_DCD_2	R/W	0h	Controls TX_DCD pin for each pad for slice 2.
15-12	RESERVED	R/W	X	
11-8	PHY_FAST_LVL_EN_2	R/W	0h	Enable for fast multi-pattern window search for slice 2.
7-6	RESERVED	R/W	X	
5-0	PHY_WDQLVL_PER_START_OFFSET_2	R/W	0h	Periodic training start point offset for slice 2.

4.4.371 DDRSS_PHY_602 Register (Offset = 4968h) [reset = X]

DDRSS_PHY_602 is shown in Figure 4-1165 and described in Table 4-2338.

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Table 4-2337. DDRSS_PHY_602 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4968h

Figure 4-1165. DDRSS_PHY_602 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_4_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_3_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_2_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_1_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2338. DDRSS_PHY_602 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_4_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_3_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_2_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_1_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.

4.4.372 DDRSS_PHY_603 Register (Offset = 496Ch) [reset = X]

DDRSS_PHY_603 is shown in Figure 4-1166 and described in Table 4-2340.

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Table 4-2339. DDRSS_PHY_603 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 496Ch

Figure 4-1166. DDRSS_PHY_603 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_DM_RX_DCD_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_7_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_6_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_5_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2340. DDRSS_PHY_603 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_DM_RX_DCD_2	R/W	0h	Controls RX_DCD pin for dm pad for slice 2.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_7_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_6_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_5_2	R/W	0h	Controls RX_DCD pin for each pad for slice 2.

4.4.373 DDRSS_PHY_604 Register (Offset = 4970h) [reset = X]

DDRSS_PHY_604 is shown in Figure 4-1167 and described in Table 4-2342.

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Table 4-2341. DDRSS_PHY_604 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4970h

Figure 4-1167. DDRSS_PHY_604 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PHY_PAD_DSLICE_IO_CFG_2					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_2				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_2				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2342. DDRSS_PHY_604 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PHY_PAD_DSLICE_IO_CFG_2	R/W	0h	Controls PCLK/PARK pin for pad for slice 2.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_FDBK_RX_DCD_2	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 2.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_DQS_RX_DCD_2	R/W	0h	Controls RX_DCD pin for dqs pad for slice 2.

4.4.374 DDRSS_PHY_605 Register (Offset = 4974h) [reset = X]

DDRSS_PHY_605 is shown in [Figure 4-1168](#) and described in [Table 4-2344](#).

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Table 4-2343. DDRSS_PHY_605 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4974h

Figure 4-1168. DDRSS_PHY_605 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ1_SLAVE_DELAY_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ0_SLAVE_DELAY_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2344. DDRSS_PHY_605 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ1_SLAVE_DELAY_2	R/W	0h	Read DQ1 slave delay setting for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ0_SLAVE_DELAY_2	R/W	0h	Read DQ0 slave delay setting for slice 2.

4.4.375 DDRSS_PHY_606 Register (Offset = 4978h) [reset = X]

DDRSS_PHY_606 is shown in [Figure 4-1169](#) and described in [Table 4-2346](#).

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Table 4-2345. DDRSS_PHY_606 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4978h

Figure 4-1169. DDRSS_PHY_606 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ3_SLAVE_DELAY_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ2_SLAVE_DELAY_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2346. DDRSS_PHY_606 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ3_SLAVE_DELAY_2	R/W	0h	Read DQ3 slave delay setting for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ2_SLAVE_DELAY_2	R/W	0h	Read DQ2 slave delay setting for slice 2.

4.4.376 DDRSS_PHY_607 Register (Offset = 497Ch) [reset = X]

DDRSS_PHY_607 is shown in [Figure 4-1170](#) and described in [Table 4-2348](#).

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Table 4-2347. DDRSS_PHY_607 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 497Ch

Figure 4-1170. DDRSS_PHY_607 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ5_SLAVE_DELAY_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ4_SLAVE_DELAY_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2348. DDRSS_PHY_607 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ5_SLAVE_DELAY_2	R/W	0h	Read DQ5 slave delay setting for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ4_SLAVE_DELAY_2	R/W	0h	Read DQ4 slave delay setting for slice 2.

4.4.377 DDRSS_PHY_608 Register (Offset = 4980h) [reset = X]

DDRSS_PHY_608 is shown in Figure 4-1171 and described in Table 4-2350.

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Table 4-2349. DDRSS_PHY_608 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4980h

Figure 4-1171. DDRSS_PHY_608 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ7_SLAVE_DELAY_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ6_SLAVE_DELAY_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2350. DDRSS_PHY_608 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ7_SLAVE_DELAY_2	R/W	0h	Read DQ7 slave delay setting for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ6_SLAVE_DELAY_2	R/W	0h	Read DQ6 slave delay setting for slice 2.

4.4.378 DDRSS_PHY_609 Register (Offset = 4984h) [reset = X]

DDRSS_PHY_609 is shown in [Figure 4-1172](#) and described in [Table 4-2352](#).

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Table 4-2351. DDRSS_PHY_609 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4984h

Figure 4-1172. DDRSS_PHY_609 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_DATA_DC_CAL_CLK_SEL_2		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2352. DDRSS_PHY_609 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_DATA_DC_CAL_CLK_SEL_2	R/W	0h	Determines DCC CAL clock for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDM_SLAVE_DELAY_2	R/W	0h	Read DM/DBI slave delay setting for slice 2. May be used for data swap.

4.4.379 DDRSS_PHY_610 Register (Offset = 4988h) [reset = 0h]

DDRSS_PHY_610 is shown in [Figure 4-1173](#) and described in [Table 4-2354](#).

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Table 4-2353. DDRSS_PHY_610 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4988h

Figure 4-1173. DDRSS_PHY_610 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_DQS_OE_TIMING_2								PHY_DQ_TSEL_WR_TIMING_2							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_TSEL_RD_TIMING_2								PHY_DQ_OE_TIMING_2							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2354. DDRSS_PHY_610 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_OE_TIMING_2	R/W	0h	Start/end timing values for DQS output enable signals for slice 2.
23-16	PHY_DQ_TSEL_WR_TIMING_2	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 2.
15-8	PHY_DQ_TSEL_RD_TIMING_2	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 2.
7-0	PHY_DQ_OE_TIMING_2	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 2.

4.4.380 DDRSS_PHY_611 Register (Offset = 498Ch) [reset = X]

DDRSS_PHY_611 is shown in [Figure 4-1174](#) and described in [Table 4-2356](#).

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Table 4-2355. DDRSS_PHY_611 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 498Ch

Figure 4-1174. DDRSS_PHY_611 Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_2							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DQS_OE_RD_TIMING_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_RD_TIMING_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_IO_PAD_DELAY_TIMING_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2356. DDRSS_PHY_611 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_TSEL_WR_TIMING_2	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 2.
23-16	PHY_DQS_OE_RD_TIMING_2	R/W	0h	Start/end timing values for DQS read based OE extension for slice 2.
15-8	PHY_DQS_TSEL_RD_TIMING_2	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_IO_PAD_DELAY_TIMING_2	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 2.

4.4.381 DDRSS_PHY_612 Register (Offset = 4990h) [reset = X]

DDRSS_PHY_612 is shown in [Figure 4-1175](#) and described in [Table 4-2358](#).

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Table 4-2357. DDRSS_PHY_612 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4990h

Figure 4-1175. DDRSS_PHY_612 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_VREF_CTRL_DQ_2											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_VREF_SETTING_TIME_2															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2358. DDRSS_PHY_612 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PHY_PAD_VREF_CTRL_DQ_2	R/W	0h	Pad VREF control settings for DQ slice 2. <ul style="list-style-type: none"> Bits[27-24] = MODE Bits[23] = EN Bits[22-16] = VREFSEL
15-0	PHY_VREF_SETTING_TIME_2	R/W	0h	Number of cycles for vref settle after setting is changed for slice 2.

4.4.382 DDRSS_PHY_613 Register (Offset = 4994h) [reset = X]

DDRSS_PHY_613 is shown in [Figure 4-1176](#) and described in [Table 4-2360](#).

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Table 4-2359. DDRSS_PHY_613 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4994h

Figure 4-1176. DDRSS_PHY_613 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DQS_IE_TIMING_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_IE_TIMING_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_PER_CS_TRAINING_EN_2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2360. DDRSS_PHY_613 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_RDDATA_EN_IE_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 2.
23-16	PHY_DQS_IE_TIMING_2	R/W	0h	Start/end timing values for DQS input enable signals for slice 2.
15-8	PHY_DQ_IE_TIMING_2	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_EN_2	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 2. Must have same value in all slices.

4.4.383 DDRSS_PHY_614 Register (Offset = 4998h) [reset = X]

DDRSS_PHY_614 is shown in Figure 4-1177 and described in Table 4-2362.

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Table 4-2361. DDRSS_PHY_614 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4998h

Figure 4-1177. DDRSS_PHY_614 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDDATA_EN_OE_DLY_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_TSEL_DLY_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_DBI_MODE_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PHY_IE_MODE_2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2362. DDRSS_PHY_614 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDDATA_EN_OE_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 2.
23-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_TSEL_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 2.
15-9	RESERVED	R/W	X	
8	PHY_DBI_MODE_2	R/W	0h	DBI mode for slice 2. Bit (0) enables return of DBI read data.
7-2	RESERVED	R/W	X	
1-0	PHY_IE_MODE_2	R/W	0h	Input enable mode bits for slice 2. Bit (0) enables the mode where the input enables are always on set to 1 to enable. Bit (1) disables the input enable on the DM signal set to 1 to disable.

4.4.384 DDRSS_PHY_615 Register (Offset = 499Ch) [reset = X]

DDRSS_PHY_615 is shown in Figure 4-1178 and described in Table 4-2364.

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Table 4-2363. DDRSS_PHY_615 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 499Ch

Figure 4-1178. DDRSS_PHY_615 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_MASTER_DELAY_STEP_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DELAY_START_2		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_START_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_MASTER_MODE_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2364. DDRSS_PHY_615 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_MASTER_DELAY_STEP_2	R/W	0h	Incremental step size for master delay line locking algorithm for slice 2.
23-19	RESERVED	R/W	X	
18-8	PHY_MASTER_DELAY_START_2	R/W	0h	Start value for master delay line locking algorithm for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_SW_MASTER_MODE_2	R/W	0h	Master delay line override settings for slice 2. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit (2) enables software bypass mode. Bit (3) is the software bypass mode value.

4.4.385 DDRSS_PHY_616 Register (Offset = 49A0h) [reset = X]

DDRSS_PHY_616 is shown in Figure 4-1179 and described in Table 4-2366.

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Table 4-2365. DDRSS_PHY_616 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49A0h

Figure 4-1179. DDRSS_PHY_616 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_DLY_STEP_2							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_RPTR_UPDATE_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_HALF_MEASURE_2							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_MASTER_DELAY_WAIT_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2366. DDRSS_PHY_616 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_DLY_STEP_2	R/W	0h	DQS slave delay step size during write leveling for slice 2.
23-20	RESERVED	R/W	X	
19-16	PHY_RPTR_UPDATE_2	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 2.
15-8	PHY_MASTER_DELAY_HALF_MEASURE_2	R/W	0h	Defines the number of delay line elements to be considered in determining whether to lock to a half clock cycle in the data slice master for slice 2.
7-0	PHY_MASTER_DELAY_WAIT_2	R/W	0h	Wait cycles for master delay line locking algorithm for slice 2. Bits (3:0) are the cycle wait count after a calibration clock setting change. Bits (7:4) are the cycle wait count after a master delay setting change.

4.4.386 DDRSS_PHY_617 Register (Offset = 49A4h) [reset = X]

DDRSS_PHY_617 is shown in Figure 4-1180 and described in Table 4-2368.

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Table 4-2367. DDRSS_PHY_617 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49A4h

Figure 4-1180. DDRSS_PHY_617 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_RESP_WAIT_CNT_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_DLY_STEP_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_RESP_WAIT_CNT_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_WRLVL_DLY_FINE_STEP_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2368. DDRSS_PHY_617 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_GTLVL_RESP_WAIT_CNT_2	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 2. The valid range is 0x0 to 0xB.
23-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_DLY_STEP_2	R/W	0h	DQS slave delay step size during gate training for slice 2.
15-14	RESERVED	R/W	X	
13-8	PHY_WRLVL_RESP_WAIT_CNT_2	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_WRLVL_DLY_FINE_STEP_2	R/W	0h	DQS slave delay fine step size during write leveling for slice 2.

4.4.387 DDRSS_PHY_618 Register (Offset = 49A8h) [reset = X]

DDRSS_PHY_618 is shown in Figure 4-1181 and described in Table 4-2370.

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Table 4-2369. DDRSS_PHY_618 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49A8h

Figure 4-1181. DDRSS_PHY_618 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_FINAL_STEP_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_GTLVL_BACK_STEP_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2370. DDRSS_PHY_618 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_GTLVL_FINAL_STEP_2	R/W	0h	Final backup step delay used in gate training algorithm for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_BACK_STEP_2	R/W	0h	Interim backup step delay used in gate training algorithm for slice 2.

4.4.388 DDRSS_PHY_619 Register (Offset = 49ACh) [reset = X]

DDRSS_PHY_619 is shown in Figure 4-1182 and described in Table 4-2372.

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Table 4-2371. DDRSS_PHY_619 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49ACh

Figure 4-1182. DDRSS_PHY_619 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_DLY_STEP_2			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PHY_TOGGLE_PRE_SUPP RT_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_2			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_WDQLVL_DLY_STEP_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2372. DDRSS_PHY_619 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_RDLVL_DLY_STEP_2	R/W	0h	DQS slave delay step size during read leveling for slice 2.
23-17	RESERVED	R/W	X	
16	PHY_TOGGLE_PRE_SUPPORT_2	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 2.
15-12	RESERVED	R/W	X	
11-8	PHY_WDQLVL_QTR_DLY_STEP_2	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 2. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value.
7-0	PHY_WDQLVL_DLY_STEP_2	R/W	0h	DQ slave delay step size during write data leveling for slice 2.

4.4.389 DDRSS_PHY_620 Register (Offset = 49B0h) [reset = X]

DDRSS_PHY_620 is shown in [Figure 4-1183](#) and described in [Table 4-2374](#).

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Table 4-2373. DDRSS_PHY_620 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49B0h

Figure 4-1183. DDRSS_PHY_620 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_MAX_EDGE_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2374. DDRSS_PHY_620 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_MAX_EDGE_2	R/W	0h	The maximum rdlvl slave delay search window for read eye training for slice 2.

4.4.390 DDRSS_PHY_621 Register (Offset = 49B4h) [reset = X]

DDRSS_PHY_621 is shown in [Figure 4-1184](#) and described in [Table 4-2376](#).

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Table 4-2375. DDRSS_PHY_621 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49B4h

Figure 4-1184. DDRSS_PHY_621 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_RDLVL_PER_START_OFFSET_2					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED							PHY_SW_RDLVL_DVW_MIN_EN_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_DVW_MIN_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_DVW_MIN_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2376. DDRSS_PHY_621 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_RDLVL_PER_START_OFFSET_2	R/W	0h	Periodic training start point offset for slice 2.
23-17	RESERVED	R/W	X	
16	PHY_SW_RDLVL_DVW_MIN_EN_2	R/W	0h	SW override to enable use of PHY_RDLVL_DVW_MIN for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_DVW_MIN_2	R/W	0h	Minimum data valid window across DQs and ranks for slice 2.

4.4.391 DDRSS_PHY_622 Register (Offset = 49B8h) [reset = X]

DDRSS_PHY_622 is shown in Figure 4-1185 and described in Table 4-2378.

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Table 4-2377. DDRSS_PHY_622 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49B8h

Figure 4-1185. DDRSS_PHY_622 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_2	
R/W-X						R/W-3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_2		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2378. DDRSS_PHY_622 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_INIT_DISABLE_2	R/W	3h	Disable duty cycle adjust at initialization for slice 2.
15-11	RESERVED	R/W	X	
10-8	PHY_WRPATH_GATE_TIMING_2	R/W	0h	Write path clock gating timing for slice 2. it means additional clock number to write path clock gate
7-2	RESERVED	R/W	X	
1-0	PHY_WRPATH_GATE_DISABLE_2	R/W	0h	Write path clock gating disable for slice 2. [0]: disable pull in wrdata_en [1]: disable write path clock gating, clock always on

4.4.392 DDRSS_PHY_623 Register (Offset = 49BCh) [reset = X]

DDRSS_PHY_623 is shown in [Figure 4-1186](#) and described in [Table 4-2380](#).

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Table 4-2379. DDRSS_PHY_623 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49BCh

Figure 4-1186. DDRSS_PHY_623 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_2		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ_INIT_SLV_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_INIT_SLV_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2380. DDRSS_PHY_623 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_2	R/W	0h	Initial value of write DQ slave delay for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_2	R/W	0h	Initial value of write DQS slave delay for slice 2.

4.4.393 DDRSS_PHY_624 Register (Offset = 49C0h) [reset = X]

DDRSS_PHY_624 is shown in Figure 4-1187 and described in Table 4-2382.

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Table 4-2381. DDRSS_PHY_624 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49C0h

Figure 4-1187. DDRSS_PHY_624 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_2							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DM_CLK_SE_THRSHLD_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_2
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_2
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2382. DDRSS_PHY_624 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_2	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 2.
23-16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_2	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 2.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_WDQLVL_ENABLE_2	R/W	0h	Enable duty cycle adjust during write DQ training for slice 2.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_WRLVL_ENABLE_2	R/W	0h	Enable duty cycle adjust during write leveling for slice 2.

4.4.394 DDRSS_PHY_625 Register (Offset = 49C4h) [reset = X]

DDRSS_PHY_625 is shown in [Figure 4-1188](#) and described in [Table 4-2384](#).

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Table 4-2383. DDRSS_PHY_625 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49C4h

Figure 4-1188. DDRSS_PHY_625 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_DLY_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED			PHY_MEAS_DLY_STEP_ENABLE_2				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQ_OSC_DELTA_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2384. DDRSS_PHY_625 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_DLY_2	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 2.
15-14	RESERVED	R/W	X	
13-8	PHY_MEAS_DLY_STEP_ENABLE_2	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 2.
7	RESERVED	R/W	X	
6-0	PHY_WDQ_OSC_DELTA_2	R/W	0h	Slave delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 2.

4.4.395 DDRSS_PHY_626 Register (Offset = 49C8h) [reset = 0h]

DDRSS_PHY_626 is shown in [Figure 4-1189](#) and described in [Table 4-2386](#).

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Table 4-2385. DDRSS_PHY_626 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49C8h

Figure 4-1189. DDRSS_PHY_626 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2386. DDRSS_PHY_626 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DQ_DM_SWIZZLE0_2	R/W	0h	DQ/DM bit swizzling 0 for slice 2. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0, Bits (7:4) inform the PHY which bit in {DM,DQ} map to DQ1, etc.

4.4.396 DDRSS_PHY_627 Register (Offset = 49CCh) [reset = X]

DDRSS_PHY_627 is shown in [Figure 4-1190](#) and described in [Table 4-2388](#).

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Table 4-2387. DDRSS_PHY_627 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49CCh

Figure 4-1190. DDRSS_PHY_627 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2388. DDRSS_PHY_627 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PHY_DQ_DM_SWIZZLE1_2	R/W	0h	DQ/DM bit swizzling 1 for slice 2. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DM.

4.4.397 DDRSS_PHY_628 Register (Offset = 49D0h) [reset = X]

DDRSS_PHY_628 is shown in [Figure 4-1191](#) and described in [Table 4-2390](#).

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Table 4-2389. DDRSS_PHY_628 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49D0h

Figure 4-1191. DDRSS_PHY_628 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_2										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_2										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2390. DDRSS_PHY_628 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ1_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ1 for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ0_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ0 for slice 2.

4.4.398 DDRSS_PHY_629 Register (Offset = 49D4h) [reset = X]

DDRSS_PHY_629 is shown in [Figure 4-1192](#) and described in [Table 4-2392](#).

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Table 4-2391. DDRSS_PHY_629 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49D4h

Figure 4-1192. DDRSS_PHY_629 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_2										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_2										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2392. DDRSS_PHY_629 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ3_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ3 for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ2_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ2 for slice 2.

4.4.399 DDRSS_PHY_630 Register (Offset = 49D8h) [reset = X]

DDRSS_PHY_630 is shown in Figure 4-1193 and described in Table 4-2394.

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Table 4-2393. DDRSS_PHY_630 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49D8h

Figure 4-1193. DDRSS_PHY_630 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_2										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_2										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2394. DDRSS_PHY_630 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ5_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ5 for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ4_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ4 for slice 2.

4.4.400 DDRSS_PHY_631 Register (Offset = 49DCh) [reset = X]

DDRSS_PHY_631 is shown in [Figure 4-1194](#) and described in [Table 4-2396](#).

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Table 4-2395. DDRSS_PHY_631 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49DCh

Figure 4-1194. DDRSS_PHY_631 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_2										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_2										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2396. DDRSS_PHY_631 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ7_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ7 for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ6_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQ6 for slice 2.

4.4.401 DDRSS_PHY_632 Register (Offset = 49E0h) [reset = X]

DDRSS_PHY_632 is shown in Figure 4-1195 and described in Table 4-2398.

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Table 4-2397. DDRSS_PHY_632 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49E0h

Figure 4-1195. DDRSS_PHY_632 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_2									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_CLK_WRDM_SLAVE_DELAY_2									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2398. DDRSS_PHY_632 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_CLK_WRDQS_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DQS for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDM_SLAVE_DELAY_2	R/W	0h	Write clock slave delay setting for DM for slice 2.

4.4.402 DDRSS_PHY_633 Register (Offset = 49E4h) [reset = X]

DDRSS_PHY_633 is shown in [Figure 4-1196](#) and described in [Table 4-2400](#).

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Table 4-2399. DDRSS_PHY_633 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49E4h

Figure 4-1196. DDRSS_PHY_633 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_ADJUST_2	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2400. DDRSS_PHY_633 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ0 for slice 2.
7-2	RESERVED	R/W	X	
1-0	PHY_WRLVL_THRESHOLD_ADJUST_2	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 2.

4.4.403 DDRSS_PHY_634 Register (Offset = 49E8h) [reset = X]

DDRSS_PHY_634 is shown in [Figure 4-1197](#) and described in [Table 4-2402](#).

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Table 4-2401. DDRSS_PHY_634 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49E8h

Figure 4-1197. DDRSS_PHY_634 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2402. DDRSS_PHY_634 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ1 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ0 for slice 2.

4.4.404 DDRSS_PHY_635 Register (Offset = 49ECh) [reset = X]

DDRSS_PHY_635 is shown in [Figure 4-1198](#) and described in [Table 4-2404](#).

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Table 4-2403. DDRSS_PHY_635 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49ECh

Figure 4-1198. DDRSS_PHY_635 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2404. DDRSS_PHY_635 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ2 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ1 for slice 2.

4.4.405 DDRSS_PHY_636 Register (Offset = 49F0h) [reset = X]

DDRSS_PHY_636 is shown in Figure 4-1199 and described in Table 4-2406.

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Table 4-2405. DDRSS_PHY_636 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49F0h

Figure 4-1199. DDRSS_PHY_636 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2406. DDRSS_PHY_636 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ3 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ2 for slice 2.

4.4.406 DDRSS_PHY_637 Register (Offset = 49F4h) [reset = X]

DDRSS_PHY_637 is shown in [Figure 4-1200](#) and described in [Table 4-2408](#).

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Table 4-2407. DDRSS_PHY_637 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49F4h

Figure 4-1200. DDRSS_PHY_637 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2408. DDRSS_PHY_637 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ4 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ3 for slice 2.

4.4.407 DDRSS_PHY_638 Register (Offset = 49F8h) [reset = X]

DDRSS_PHY_638 is shown in [Figure 4-1201](#) and described in [Table 4-2410](#).

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Table 4-2409. DDRSS_PHY_638 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49F8h

Figure 4-1201. DDRSS_PHY_638 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2410. DDRSS_PHY_638 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ5 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ4 for slice 2.

4.4.408 DDRSS_PHY_639 Register (Offset = 49FCh) [reset = X]

DDRSS_PHY_639 is shown in [Figure 4-1202](#) and described in [Table 4-2412](#).

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Table 4-2411. DDRSS_PHY_639 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 49FCh

Figure 4-1202. DDRSS_PHY_639 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2412. DDRSS_PHY_639 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ6 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ5 for slice 2.

4.4.409 DDRSS_PHY_640 Register (Offset = 4A00h) [reset = X]

DDRSS_PHY_640 is shown in [Figure 4-1203](#) and described in [Table 4-2414](#).

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Table 4-2413. DDRSS_PHY_640 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A00h

Figure 4-1203. DDRSS_PHY_640 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2414. DDRSS_PHY_640 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DQ7 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ6 for slice 2.

4.4.410 DDRSS_PHY_641 Register (Offset = 4A04h) [reset = X]

DDRSS_PHY_641 is shown in [Figure 4-1204](#) and described in [Table 4-2416](#).

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Table 4-2415. DDRSS_PHY_641 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A04h

Figure 4-1204. DDRSS_PHY_641 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DM_RISE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2416. DDRSS_PHY_641 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_2	R/W	0h	Rising edge read DQS slave delay setting for DM for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DQ7 for slice 2.

4.4.411 DDRSS_PHY_642 Register (Offset = 4A08h) [reset = X]

DDRSS_PHY_642 is shown in [Figure 4-1205](#) and described in [Table 4-2418](#).

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Table 4-2417. DDRSS_PHY_642 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A08h

Figure 4-1205. DDRSS_PHY_642 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2418. DDRSS_PHY_642 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_GATE_SLAVE_DELAY_2	R/W	0h	Read DQS slave delay setting for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_2	R/W	0h	Falling edge read DQS slave delay setting for DM for slice 2.

4.4.412 DDRSS_PHY_643 Register (Offset = 4A0Ch) [reset = X]

DDRSS_PHY_643 is shown in [Figure 4-1206](#) and described in [Table 4-2420](#).

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Table 4-2419. DDRSS_PHY_643 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A0Ch

Figure 4-1206. DDRSS_PHY_643 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_2	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_DELAY_EARLY_THRESHOLD_2							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_WRITE_PATH_LAT_ADD_2		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_LATENCY_ADJUST_2			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2420. DDRSS_PHY_643 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_2	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 2.
15-11	RESERVED	R/W	X	
10-8	PHY_WRITE_PATH_LAT_ADD_2	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 2.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_LATENCY_ADJUST_2	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 2.

4.4.413 DDRSS_PHY_644 Register (Offset = 4A10h) [reset = X]

DDRSS_PHY_644 is shown in [Figure 4-1207](#) and described in [Table 4-2422](#).

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Table 4-2421. DDRSS_PHY_644 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A10h

Figure 4-1207. DDRSS_PHY_644 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_E ARLY_FORCE_ ZERO_2
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_ THRESHOLD_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2422. DDRSS_PHY_644 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_WRLVL_EARLY_FORCE_ZERO_2	R/W	0h	Force the final write level delay value (that meets the early threshold) to 0 for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 2.

4.4.414 DDRSS_PHY_645 Register (Offset = 4A14h) [reset = X]

DDRSS_PHY_645 is shown in [Figure 4-1208](#) and described in [Table 4-2424](#).

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Table 4-2423. DDRSS_PHY_645 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A14h

Figure 4-1208. DDRSS_PHY_645 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2424. DDRSS_PHY_645 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_LAT_ADJ_START_2	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 2.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_RDDQS_SLV_DLY_START_2	R/W	0h	Initial read DQS gate slave delay setting during gate training for slice 2.

4.4.415 DDRSS_PHY_646 Register (Offset = 4A18h) [reset = X]

DDRSS_PHY_646 is shown in Figure 4-1209 and described in Table 4-2426.

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Table 4-2425. DDRSS_PHY_646 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A18h

Figure 4-1209. DDRSS_PHY_646 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PAS S_2
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_NTP_WRLAT_START_2			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_2		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_START_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2426. DDRSS_PHY_646 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_NTP_PASS_2	R/W	0h	Indicates if No-topology training found a passing result for slice 2.
23-20	RESERVED	R/W	X	
19-16	PHY_NTP_WRLAT_START_2	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 2.
15-11	RESERVED	R/W	X	
10-0	PHY_WDQLVL_DQDM_SLV_DLY_START_2	R/W	0h	Initial DQ/DM slave delay setting during write data leveling for slice 2.

4.4.416 DDRSS_PHY_647 Register (Offset = 4A1Ch) [reset = X]

DDRSS_PHY_647 is shown in [Figure 4-1210](#) and described in [Table 4-2428](#).

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Table 4-2427. DDRSS_PHY_647 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A1Ch

Figure 4-1210. DDRSS_PHY_647 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2428. DDRSS_PHY_647 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2	R/W	0h	Read leveling starting value for the DQS/DQ slave delay settings for slice 2.

4.4.417 DDRSS_PHY_648 Register (Offset = 4A20h) [reset = 20202020h]

DDRSS_PHY_648 is shown in [Figure 4-1211](#) and described in [Table 4-2430](#).

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Table 4-2429. DDRSS_PHY_648 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A20h

Figure 4-1211. DDRSS_PHY_648 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_2							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ1_CLK_ADJUST_2							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ0_CLK_ADJUST_2							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_CLK_ADJUST_2							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2430. DDRSS_PHY_648 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ2_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
23-16	PHY_DATA_DC_DQ1_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
15-8	PHY_DATA_DC_DQ0_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
7-0	PHY_DATA_DC_DQS_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.

4.4.418 DDRSS_PHY_649 Register (Offset = 4A24h) [reset = 20202020h]

DDRSS_PHY_649 is shown in [Figure 4-1212](#) and described in [Table 4-2432](#).

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Table 4-2431. DDRSS_PHY_649 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A24h

Figure 4-1212. DDRSS_PHY_649 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ6_CLK_ADJUST_2							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ5_CLK_ADJUST_2							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ4_CLK_ADJUST_2							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ3_CLK_ADJUST_2							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2432. DDRSS_PHY_649 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ6_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
23-16	PHY_DATA_DC_DQ5_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
15-8	PHY_DATA_DC_DQ4_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
7-0	PHY_DATA_DC_DQ3_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.

4.4.419 DDRSS_PHY_650 Register (Offset = 4A28h) [reset = 2020h]

DDRSS_PHY_650 is shown in [Figure 4-1213](#) and described in [Table 4-2434](#).

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Table 4-2433. DDRSS_PHY_650 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A28h

Figure 4-1213. DDRSS_PHY_650 Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_2							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_2							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_2							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_2							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2434. DDRSS_PHY_650 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_DSLICE_PAD_BOOSTPN_SETTING_2	R/W	0h	Setting for boost P/N of pad for slice 2.
15-8	PHY_DATA_DC_DM_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.
7-0	PHY_DATA_DC_DQ7_CLK_ADJUST_2	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 2.

4.4.420 DDRSS_PHY_651 Register (Offset = 4A2Ch) [reset = X]

DDRSS_PHY_651 is shown in [Figure 4-1214](#) and described in [Table 4-2436](#).

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Table 4-2435. DDRSS_PHY_651 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4A2Ch

Figure 4-1214. DDRSS_PHY_651 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_2	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_2	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTL_SETTING_2					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2436. DDRSS_PHY_651 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DQS_FFE_2	R/W	0h	TX_FFE setting for DQS pad for slice 2.
15-10	RESERVED	R/W	X	
9-8	PHY_DQ_FFE_2	R/W	0h	TX_FFE setting for DQ/DM pad for slice 2.
7-6	RESERVED	R/W	X	
5-0	PHY_DSLICE_PAD_RX_CTL_SETTING_2	R/W	0h	Setting for RX ctl P/N of pad for slice 2.

4.4.421 DDRSS_PHY_768 Register (Offset = 4C00h) [reset = X]

DDRSS_PHY_768 is shown in [Figure 4-1215](#) and described in [Table 4-2438](#).

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Table 4-2437. DDRSS_PHY_768 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C00h

Figure 4-1215. DDRSS_PHY_768 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_IO_PAD_DELAY_TIMING_BYPASS_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_CLK_WR_BYPASS_SLAVE_DELAY_3		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CLK_WR_BYPASS_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2438. DDRSS_PHY_768 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_IO_PAD_DELAY_TIMING_BYPASS_3	R/W	0h	Feedback pad's OPAD and IPAD delay timing on bypass mode for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WR_BYPASS_SLAVE_DELAY_3	R/W	0h	Write data clock bypass mode slave delay setting for slice 3.} PADDING_BEFORE

4.4.422 DDRSS_PHY_769 Register (Offset = 4C04h) [reset = X]

DDRSS_PHY_769 is shown in [Figure 4-1216](#) and described in [Table 4-2440](#).

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Table 4-2439. DDRSS_PHY_769 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C04h

Figure 4-1216. DDRSS_PHY_769 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WRITE_PATH_LAT_ADD_BYPASS_3		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2440. DDRSS_PHY_769 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_WRITE_PATH_LAT_ADD_BYPASS_3	R/W	0h	Number of cycles on bypass mode to delay the incoming dfi_wrddata_en/dfi_wrddata signals for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_CLK_WRDQS_SLAVE_DELAY_BYPASS_3	R/W	0h	Write DQS bypass mode slave delay setting for slice 3.

4.4.423 DDRSS_PHY_770 Register (Offset = 4C08h) [reset = X]

DDRSS_PHY_770 is shown in Figure 4-1217 and described in Table 4-2442.

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Table 4-2441. DDRSS_PHY_770 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C08h

Figure 4-1217. DDRSS_PHY_770 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_BYPASS_OVERRIDE_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_BYPASS_TWO_CYCLE_PREAMBLE_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2442. DDRSS_PHY_770 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CLK_BYPASS_OVERRIDE_3	R/W	0h	Bypass mode override setting for slice 3.
23-18	RESERVED	R/W	X	
17-16	PHY_BYPASS_TWO_CYCLE_PREAMBLE_3	R/W	0h	Two_cycle_preamble for bypass mode for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3	R/W	0h	Read DQS bypass mode slave delay setting for slice 3.

4.4.424 DDRSS_PHY_771 Register (Offset = 4C0Ch) [reset = X]

DDRSS_PHY_771 is shown in Figure 4-1218 and described in Table 4-2444.

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Table 4-2443. DDRSS_PHY_771 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C0Ch

Figure 4-1218. DDRSS_PHY_771 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ3_SHIFT_3					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ2_SHIFT_3					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ1_SHIFT_3					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ0_SHIFT_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2444. DDRSS_PHY_771 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ3_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ2_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ1_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-2444. DDRSS_PHY_771 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ0_SHIF T_3	R/W	0h	<p>Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 3.</p> <p>Bit (0) enables override of half_cycle_shift.</p> <p>Bit (1) is the half_cycle_shift value.</p> <p>Bit (2) enables override of cycle shift.</p> <p>Bits (4:3) are the cycle_shift value.</p>

4.4.425 DDRSS_PHY_772 Register (Offset = 4C10h) [reset = X]

DDRSS_PHY_772 is shown in Figure 4-1219 and described in Table 4-2446.

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Table 4-2445. DDRSS_PHY_772 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C10h

Figure 4-1219. DDRSS_PHY_772 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_SW_WRDQ7_SHIFT_3					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_SW_WRDQ6_SHIFT_3					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED		PHY_SW_WRDQ5_SHIFT_3					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDQ4_SHIFT_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2446. DDRSS_PHY_772 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_SW_WRDQ7_SHIF T_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
23-22	RESERVED	R/W	X	
21-16	PHY_SW_WRDQ6_SHIF T_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.
15-14	RESERVED	R/W	X	
13-8	PHY_SW_WRDQ5_SHIF T_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) are the cycle_shift value.

Table 4-2446. DDRSS_PHY_772 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	X	
5-0	PHY_SW_WRDQ4_SHIF T_3	R/W	0h	<p>Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 3.</p> <p>Bit (0) enables override of half_cycle_shift.</p> <p>Bit (1) is the half_cycle_shift value.</p> <p>Bit (2) enables override of cycle shift.</p> <p>Bits (4:3) are the cycle_shift value.</p>

4.4.426 DDRSS_PHY_773 Register (Offset = 4C14h) [reset = X]

DDRSS_PHY_773 is shown in Figure 4-1220 and described in Table 4-2448.

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Table 4-2447. DDRSS_PHY_773 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C14h

Figure 4-1220. DDRSS_PHY_773 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_PER_CS_TRAINING_MULTICAST_EN_3
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
RESERVED						PHY_PER_RANK_CS_MAP_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_WRDQS_SHIFT_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_SW_WRDM_SHIFT_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2448. DDRSS_PHY_773 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_PER_CS_TRAINING_MULTICAST_EN_3	R/W	1h	When set, a register write will update parameters for all ranks at the same time in slice 3. Set to 1 to enable.
23-18	RESERVED	R/W	X	
17-16	PHY_PER_RANK_CS_MAP_3	R/W	0h	Per-rank CS map for slice 3. Setting a bit uses that CS for the rank, bit (0) uses CS0, bit (1) uses CS1, etc.
15-12	RESERVED	R/W	X	
11-8	PHY_SW_WRDQS_SHIFT_3	R/W	0h	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bit (3) is the cycle_shift value.
7-6	RESERVED	R/W	X	

Table 4-2448. DDRSS_PHY_773 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	PHY_SW_WRDM_SHIFT_3	R/W	0h	<p>Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 3.</p> <p>Bit (0) enables override of half_cycle_shift.</p> <p>Bit (1) is the half_cycle_shift value.</p> <p>Bit (2) enables override of cycle shift.</p> <p>Bits (4:3) are the cycle_shift value.</p>

4.4.427 DDRSS_PHY_774 Register (Offset = 4C18h) [reset = X]

DDRSS_PHY_774 is shown in Figure 4-1221 and described in Table 4-2450.

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Table 4-2449. DDRSS_PHY_774 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C18h

Figure 4-1221. DDRSS_PHY_774 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_LP4_BOOT_RDDATA_EN_DLY_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_BOOT_RDDATA_EN_IE_DLY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_PER_CS_TRAINING_INDEX_3
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2450. DDRSS_PHY_774 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 3.
23-21	RESERVED	R/W	X	
20-16	PHY_LP4_BOOT_RDDATA_EN_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is early for slice 3.
15-10	RESERVED	R/W	X	
9-8	PHY_LP4_BOOT_RDDATA_EN_IE_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_INDEX_3	R/W	0h	For per-rank training, indicates which rank's parameters are read/written for slice 3.

4.4.428 DDRSS_PHY_775 Register (Offset = 4C1Ch) [reset = X]

DDRSS_PHY_775 is shown in Figure 4-1222 and described in Table 4-2452.

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Table 4-2451. DDRSS_PHY_775 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C1Ch

Figure 4-1222. DDRSS_PHY_775 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_LP4_BOOT_RDDATA_EN_OE_DLY_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_LP4_BOOT_WRPATH_GATE_DISABLE_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_LP4_BOOT_RPTR_UPDATE_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2452. DDRSS_PHY_775 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_LP4_BOOT_RDDATA_EN_OE_DLY_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than necessary for extended OE generation for slice 3.
23-18	RESERVED	R/W	X	
17-16	PHY_LP4_BOOT_WRPATH_GATE_DISABLE_3	R/W	0h	For LPDDR4 boot frequency, write path clock gating disable for slice 3. Bit (0): disable pull in wrdata_en Bit (1): disable write path clock gating, clock always on
15-12	RESERVED	R/W	X	
11-8	PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_3	R/W	0h	For LPDDR4 boot frequency, the number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_LP4_BOOT_RPTR_UPDATE_3	R/W	0h	For LPDDR4 boot frequency, the offset in cycles from the dfi_rddata_en signal to releasing data from the entry FIFO for slice 3.

4.4.429 DDRSS_PHY_776 Register (Offset = 4C20h) [reset = X]

DDRSS_PHY_776 is shown in [Figure 4-1223](#) and described in [Table 4-2454](#).

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Table 4-2453. DDRSS_PHY_776 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C20h

Figure 4-1223. DDRSS_PHY_776 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LPBK_DFX_TIMEOUT_EN_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_LPBK_CONTROL_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_LPBK_CONTROL_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_CTRL_LPBK_EN_3	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2454. DDRSS_PHY_776 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LPBK_DFX_TIMEOUT_EN_3	R/W	0h	Loopback read only test timeout mechanism enable for slice 3.
23-17	RESERVED	R/W	X	
16-8	PHY_LPBK_CONTROL_3	R/W	0h	Loopback control bits for slice 3.
7-2	RESERVED	R/W	X	
1-0	PHY_CTRL_LPBK_EN_3	R/W	0h	Loopback control en for slice 3.

4.4.430 DDRSS_PHY_777 Register (Offset = 4C24h) [reset = 0h]

DDRSS_PHY_777 is shown in [Figure 4-1224](#) and described in [Table 4-2456](#).

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Table 4-2455. DDRSS_PHY_777 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C24h

Figure 4-1224. DDRSS_PHY_777 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_AUTO_TIMING_MARGIN_CONTROL_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2456. DDRSS_PHY_777 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_AUTO_TIMING_MARGIN_CONTROL_3	R/W	0h	Auto timing marging control bits for slice 3.

4.4.431 DDRSS_PHY_778 Register (Offset = 4C28h) [reset = X]

DDRSS_PHY_778 is shown in [Figure 4-1225](#) and described in [Table 4-2458](#).

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Table 4-2457. DDRSS_PHY_778 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C28h

Figure 4-1225. DDRSS_PHY_778 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				PHY_AUTO_TIMING_MARGIN_OBS_3																											
R-X				R-0h																											

LEGEND: R = Read Only; -n = value after reset

Table 4-2458. DDRSS_PHY_778 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-0	PHY_AUTO_TIMING_MARGIN_OBS_3	R	0h	Observation register for the auto_timing_margin for slice 3. READ-ONLY

4.4.432 DDRSS_PHY_779 Register (Offset = 4C2Ch) [reset = X]

DDRSS_PHY_779 is shown in [Figure 4-1226](#) and described in [Table 4-2460](#).

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Table 4-2459. DDRSS_PHY_779 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C2Ch

Figure 4-1226. DDRSS_PHY_779 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RDLVL_MULTIPATTERN_ENABLE_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_PRBS_PATTERN_MASK_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_PRBS_PATTERN_MASK_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED	PHY_PRBS_PATTERN_START_3						
R/W-X	R/W-1h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2460. DDRSS_PHY_779 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RDLVL_MULTIPATTERN_ENABLE_3	R/W	0h	Read Leveling Multi-pattern enable for slice 3.
23-17	RESERVED	R/W	X	
16-8	PHY_PRBS_PATTERN_MASK_3	R/W	0h	PRBS7 mask signal for slice 3.
7	RESERVED	R/W	X	
6-0	PHY_PRBS_PATTERN_START_3	R/W	1h	PRBS7 start pattern for slice 3.

4.4.433 DDRSS_PHY_780 Register (Offset = 4C30h) [reset = X]

DDRSS_PHY_780 is shown in [Figure 4-1227](#) and described in [Table 4-2462](#).

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Table 4-2461. DDRSS_PHY_780 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C30h

Figure 4-1227. DDRSS_PHY_780 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	PHY_VREF_TRAIN_OBS_3						
R/W-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED		PHY_VREF_INITIAL_STEPSIZE_3					
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PHY_RDLVL_MULTIPATT_RST_DISABLE_3
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2462. DDRSS_PHY_780 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	PHY_VREF_TRAIN_OBS_3	R	0h	Observation register for best vref value for slice 3. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	PHY_VREF_INITIAL_STEPSIZE_3	R/W	0h	Data slice initial VREF training step size for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_RDLVL_MULTIPATT_RST_DISABLE_3	R/W	0h	Read Leveling read level windows disable reset for slice 3.

4.4.434 DDRSS_PHY_781 Register (Offset = 4C34h) [reset = X]

DDRSS_PHY_781 is shown in Figure 4-1228 and described in Table 4-2464.

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Table 4-2463. DDRSS_PHY_781 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C34h

Figure 4-1228. DDRSS_PHY_781 Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_SNAP_OBS_REGS_3
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_GATE_ERROR_DELAY_SELECT_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2464. DDRSS_PHY_781 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SC_PHY_SNAP_OBS_REGS_3	W	0h	Initiates a snapshot of the internal observation registers for slice 3. Set to 1 to trigger. WRITE-ONLY
23-20	RESERVED	R/W	X	
19-16	PHY_GATE_ERROR_DELAY_SELECT_3	R/W	0h	Number of cycles to wait for the DQS gate to close before flagging an error for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3	R/W	0h	Read DQS data clock bypass mode slave delay setting for slice 3.

4.4.435 DDRSS_PHY_782 Register (Offset = 4C38h) [reset = X]

DDRSS_PHY_782 is shown in [Figure 4-1229](#) and described in [Table 4-2466](#).

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Table 4-2465. DDRSS_PHY_782 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C38h

Figure 4-1229. DDRSS_PHY_782 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_MEM_CLASS_3		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							PHY_LPDDR_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_GATE_SMPL1_SLAVE_DELAY_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2466. DDRSS_PHY_782 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_MEM_CLASS_3	R/W	0h	Indicates the type of DRAM for slice 3. 0 for DDR3, 1 for DDR4, 2 for DDR5, 4 for LPDDR2, 5 for LPDDR3. 6 for LPDDR4
23-17	RESERVED	R/W	X	
16	PHY_LPDDR_3	R/W	0h	Adds a cycle of delay for the slice 3 to match the address slice. Set to 1 to add a cycle
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL1_SLAVE_DELAY_3	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate1 signal for on-the-fly read DQS training for slice 3.

4.4.436 DDRSS_PHY_783 Register (Offset = 4C3Ch) [reset = X]

DDRSS_PHY_783 is shown in [Figure 4-1230](#) and described in [Table 4-2468](#).

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Table 4-2467. DDRSS_PHY_783 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C3Ch

Figure 4-1230. DDRSS_PHY_783 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						ON_FLY_GATE_ADJUST_EN_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL2_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL2_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2468. DDRSS_PHY_783 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	ON_FLY_GATE_ADJUST_EN_3	R/W	0h	Control the on-the-fly gate adjustment for slice 3.
15-9	RESERVED	R/W	X	
8-0	PHY_GATE_SMPL2_SLAVE_DELAY_3	R/W	0h	Number of cycles to delay the read DQS gate signal to generate gate2 signal for on-the-fly read DQS training for slice 3.

4.4.437 DDRSS_PHY_784 Register (Offset = 4C40h) [reset = 0h]

DDRSS_PHY_784 is shown in [Figure 4-1231](#) and described in [Table 4-2470](#).

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Table 4-2469. DDRSS_PHY_784 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C40h

Figure 4-1231. DDRSS_PHY_784 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GATE_TRACKING_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2470. DDRSS_PHY_784 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_GATE_TRACKING_OBS_3	R	0h	Report the on-the-fly gate measurement result for slice 3. READ-ONLY

4.4.438 DDRSS_PHY_785 Register (Offset = 4C44h) [reset = X]

DDRSS_PHY_785 is shown in [Figure 4-1232](#) and described in [Table 4-2472](#).

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Table 4-2471. DDRSS_PHY_785 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C44h

Figure 4-1232. DDRSS_PHY_785 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_LP4_PST_AMBLE_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_DFI40_POLARITY_3
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2472. DDRSS_PHY_785 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-8	PHY_LP4_PST_AMBLE_3	R/W	0h	Controls the read postamble extension for LPDDR4 for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_DFI40_POLARITY_3	R/W	0h	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or high active for slice 3.

4.4.439 DDRSS_PHY_786 Register (Offset = 4C48h) [reset = 0h]

DDRSS_PHY_786 is shown in [Figure 4-1233](#) and described in [Table 4-2474](#).

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Table 4-2473. DDRSS_PHY_786 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C48h

Figure 4-1233. DDRSS_PHY_786 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT8_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2474. DDRSS_PHY_786 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT8_3	R/W	0h	Read leveling pattern 8 data for slice 3.

4.4.440 DDRSS_PHY_787 Register (Offset = 4C4Ch) [reset = 0h]

DDRSS_PHY_787 is shown in [Figure 4-1234](#) and described in [Table 4-2476](#).

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Table 4-2475. DDRSS_PHY_787 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C4Ch

Figure 4-1234. DDRSS_PHY_787 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT9_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2476. DDRSS_PHY_787 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT9_3	R/W	0h	Read leveling pattern 9 data for slice 3.

4.4.441 DDRSS_PHY_788 Register (Offset = 4C50h) [reset = 0h]

DDRSS_PHY_788 is shown in [Figure 4-1235](#) and described in [Table 4-2478](#).

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Table 4-2477. DDRSS_PHY_788 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C50h

Figure 4-1235. DDRSS_PHY_788 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT10_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2478. DDRSS_PHY_788 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT10_3	R/W	0h	Read leveling pattern 10 data for slice 3.

4.4.442 DDRSS_PHY_789 Register (Offset = 4C54h) [reset = 0h]

DDRSS_PHY_789 is shown in [Figure 4-1236](#) and described in [Table 4-2480](#).

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Table 4-2479. DDRSS_PHY_789 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C54h

Figure 4-1236. DDRSS_PHY_789 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT11_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2480. DDRSS_PHY_789 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT11_3	R/W	0h	Read leveling pattern 11 data for slice 3.

4.4.443 DDRSS_PHY_790 Register (Offset = 4C58h) [reset = 0h]

DDRSS_PHY_790 is shown in [Figure 4-1237](#) and described in [Table 4-2482](#).

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Table 4-2481. DDRSS_PHY_790 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C58h

Figure 4-1237. DDRSS_PHY_790 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT12_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2482. DDRSS_PHY_790 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT12_3	R/W	0h	Read leveling pattern 12 data for slice 3.

4.4.444 DDRSS_PHY_791 Register (Offset = 4C5Ch) [reset = 0h]

DDRSS_PHY_791 is shown in [Figure 4-1238](#) and described in [Table 4-2484](#).

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Table 4-2483. DDRSS_PHY_791 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C5Ch

Figure 4-1238. DDRSS_PHY_791 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT13_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2484. DDRSS_PHY_791 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT13_3	R/W	0h	Read leveling pattern 13 data for slice 3.

4.4.445 DDRSS_PHY_792 Register (Offset = 4C60h) [reset = 0h]

DDRSS_PHY_792 is shown in [Figure 4-1239](#) and described in [Table 4-2486](#).

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Table 4-2485. DDRSS_PHY_792 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C60h

Figure 4-1239. DDRSS_PHY_792 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT14_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2486. DDRSS_PHY_792 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT14_3	R/W	0h	Read leveling pattern 14 data for slice 3.

4.4.446 DDRSS_PHY_793 Register (Offset = 4C64h) [reset = 0h]

DDRSS_PHY_793 is shown in [Figure 4-1240](#) and described in [Table 4-2488](#).

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Table 4-2487. DDRSS_PHY_793 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C64h

Figure 4-1240. DDRSS_PHY_793 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PATT15_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2488. DDRSS_PHY_793 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PATT15_3	R/W	0h	Read leveling pattern 15 data for slice 3.

4.4.447 DDRSS_PHY_794 Register (Offset = 4C68h) [reset = X]

DDRSS_PHY_794 is shown in Figure 4-1241 and described in Table 4-2490.

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Table 4-2489. DDRSS_PHY_794 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C68h

Figure 4-1241. DDRSS_PHY_794 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_RDDQ_ENC_OBS_SELECT_3		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_SELECT_3		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_FIFO_PTR_RST_DISABLE_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					PHY_SLAVE_LOOP_CNT_UPDATE_3		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2490. DDRSS_PHY_794 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_RDDQ_ENC_OBS_SELECT_3	R/W	0h	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ encoded slave delay observation register for slice 3.
23-20	RESERVED	R/W	X	
19-16	PHY_MASTER_DLY_LOCK_OBS_SELECT_3	R/W	0h	Select value to map the internal master delay observation registers to the accessible master delay observation register for slice 3.
15-9	RESERVED	R/W	X	
8	PHY_SW_FIFO_PTR_RST_DISABLE_3	R/W	0h	Disables automatic reset of the read entry FIFO pointers for slice 3. Set to 1 to disable automatic resets.
7-3	RESERVED	R/W	X	
2-0	PHY_SLAVE_LOOP_CNT_UPDATE_3	R/W	0h	Reserved for future use for slice 3.

4.4.448 DDRSS_PHY_795 Register (Offset = 4C6Ch) [reset = X]

DDRSS_PHY_795 is shown in [Figure 4-1242](#) and described in [Table 4-2492](#).

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Table 4-2491. DDRSS_PHY_795 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C6Ch

Figure 4-1242. DDRSS_PHY_795 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_FIFO_PTR_OBS_SELECT_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_WR_SHIFT_OBS_SELECT_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WR_ENC_OBS_SELECT_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_DQ_ENC_OBS_SELECT_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2492. DDRSS_PHY_795 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_FIFO_PTR_OBS_SELECT_3	R/W	0h	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO pointer observation register for slice 3.
23-20	RESERVED	R/W	X	
19-16	PHY_WR_SHIFT_OBS_SELECT_3	R/W	0h	Select value to map the internal write DQ/DQS automatic cycle/half_cycle shift settings to the accessible write DQ/DQS shift observation register for slice 3.
15-12	RESERVED	R/W	X	
11-8	PHY_WR_ENC_OBS_SELECT_3	R/W	0h	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ encoded slave delay observation register for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_DQ_ENC_OBS_SELECT_3	R/W	0h	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible read DQS DQ rise/fall encoded slave delay observation registers for slice 3.

4.4.449 DDRSS_PHY_796 Register (Offset = 4C70h) [reset = X]

DDRSS_PHY_796 is shown in Figure 4-1243 and described in Table 4-2494.

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Table 4-2493. DDRSS_PHY_796 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C70h

Figure 4-1243. DDRSS_PHY_796 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_PER_START_3							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_ALGO_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_LVL_DEBUG_CONT_3
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_LVL_DEBUG_MODE_3
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2494. DDRSS_PHY_796 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_PER_START_3	R/W	0h	Observation register for write leveling status for slice 3. READ-ONLY
23-18	RESERVED	R/W	X	
17-16	PHY_WRLVL_ALGO_3	R/W	0h	Write leveling algorithm selection for slice 3.
15-9	RESERVED	R/W	X	
8	SC_PHY_LVL_DEBUG_CONT_3	W	0h	Allows the leveling state machine to advance (when in debug mode) for slice 3. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_LVL_DEBUG_MODE_3	R/W	0h	Enables leveling debug mode for slice 3. Set to 1 to enable.

4.4.450 DDRSS_PHY_797 Register (Offset = 4C74h) [reset = X]

DDRSS_PHY_797 is shown in Figure 4-1244 and described in Table 4-2496.

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Table 4-2495. DDRSS_PHY_797 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C74h

Figure 4-1244. DDRSS_PHY_797 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_DQ_MASK_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_UPDT_WAIT_CNT_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WRLVL_CAPTURE_CNT_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2496. DDRSS_PHY_797 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_DQ_MASK_3	R/W	0h	For ECC slice, should set this register to do DQ bit mask for slice 3.
15-12	RESERVED	R/W	X	
11-8	PHY_WRLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during write leveling for slice 3.
7-6	RESERVED	R/W	X	
5-0	PHY_WRLVL_CAPTURE_CNT_3	R/W	0h	Number of samples to take at each DQS slave delay setting during write leveling for slice 3.

4.4.451 DDRSS_PHY_798 Register (Offset = 4C78h) [reset = X]

DDRSS_PHY_798 is shown in Figure 4-1245 and described in Table 4-2498.

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Table 4-2497. DDRSS_PHY_798 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C78h

Figure 4-1245. DDRSS_PHY_798 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_UPDT_WAIT_CNT_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_CAPTURE_CNT_3					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_PER_START_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_PER_START_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2498. DDRSS_PHY_798 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_GTLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles + 4 to wait after changing DQS slave delay setting during gate training for slice 3. The valid range is 0x0 to 0xB.
23-22	RESERVED	R/W	X	
21-16	PHY_GTLVL_CAPTURE_CNT_3	R/W	0h	Number of samples to take at each DQS slave delay setting during gate training for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_PER_START_3	R/W	0h	Value to be added to the current gate delay position as the starting point for periodic gate training for slice 3.

4.4.452 DDRSS_PHY_799 Register (Offset = 4C7Ch) [reset = X]

DDRSS_PHY_799 is shown in Figure 4-1246 and described in Table 4-2500.

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Table 4-2499. DDRSS_PHY_799 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C7Ch

Figure 4-1246. DDRSS_PHY_799 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_RDDQS_DQ_OBS_SELECT_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_RDLVL_OP_MODE_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_RDLVL_UPDT_WAIT_CNT_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_RDLVL_CAPTURE_CNT_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2500. DDRSS_PHY_799 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDLVL_RDDQS_DQ_OBS_SELECT_3	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during read leveling for slice 3.
23-18	RESERVED	R/W	X	
17-16	PHY_RDLVL_OP_MODE_3	R/W	0h	Read leveling algorithm select for slice 3. Clear to 0 to move linearly from left to right. Set to 1 to start inside the window, move left and then move right.
15-12	RESERVED	R/W	X	
11-8	PHY_RDLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles to wait after changing DQS slave delay setting during read leveling for slice 3.
7-6	RESERVED	R/W	X	
5-0	PHY_RDLVL_CAPTURE_CNT_3	R/W	0h	Number of samples to take at each DQS slave delay setting during read leveling for slice 3.

4.4.453 DDRSS_PHY_800 Register (Offset = 4C80h) [reset = X]

DDRSS_PHY_800 is shown in Figure 4-1247 and described in Table 4-2502.

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Table 4-2501. DDRSS_PHY_800 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C80h

Figure 4-1247. DDRSS_PHY_800 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_BURST_CNT_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PHY_WDQLVL_CLK_JITTER_TOLERANCE_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_RDLVL_DATA_MASK_3							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_SELECT_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2502. DDRSS_PHY_800 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_WDQLVL_BURST_CNT_3	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 3.
23-16	PHY_WDQLVL_CLK_JITTER_TOLERANCE_3	R/W	0h	Defines the minimum gap requirement for the LE and TE window for slice 3.
15-8	PHY_RDLVL_DATA_MASK_3	R/W	0h	Per-bit mask for read leveling for slice 3. If all bits are not used, only 1 bit should be cleared to 0.
7-0	PHY_RDLVL_PERIODIC_OBS_SELECT_3	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during periodic read leveling for slice 3.

4.4.454 DDRSS_PHY_801 Register (Offset = 4C84h) [reset = X]

DDRSS_PHY_801 is shown in [Figure 4-1248](#) and described in [Table 4-2504](#).

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Table 4-2503. DDRSS_PHY_801 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C84h

Figure 4-1248. DDRSS_PHY_801 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_WDQLVL_UPDT_WAIT_CNT_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_PATT_3		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2504. DDRSS_PHY_801 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_WDQLVL_UPDT_WAIT_CNT_3	R/W	0h	Number of cycles to wait after changing the DQ slave delay setting during write data leveling for slice 3.
23-19	RESERVED	R/W	X	
18-8	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3	R/W	0h	Defines the write/read burst length in bytes during the write data leveling sequence for slice 3.
7-3	RESERVED	R/W	X	
2-0	PHY_WDQLVL_PATT_3	R/W	0h	Defines the training patterns to be used during the write data leveling sequence for slice 3. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined data pattern training. If multiple bits are set, the training for each of the chosen patterns will be executed and the settings that give the smallest data valid window eye will be chosen.

4.4.455 DDRSS_PHY_802 Register (Offset = 4C88h) [reset = X]

DDRSS_PHY_802 is shown in Figure 4-1249 and described in Table 4-2506.

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Table 4-2505. DDRSS_PHY_802 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C88h

Figure 4-1249. DDRSS_PHY_802 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_WDQ LVL_CLR_PRE V_RESULTS_3
R/W-X							W-0h
15	14	13	12	11	10	9	8
PHY_WDQLVL_PERIODIC_OBS_SELECT_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_WDQLVL_DQDM_OBS_SELECT_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2506. DDRSS_PHY_802 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	SC_PHY_WDQLVL_CLR_PREV_RESULTS_3	W	0h	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for slice 3. Set to 1 to trigger. WRITE-ONLY
15-8	PHY_WDQLVL_PERIODIC_OBS_SELECT_3	R/W	0h	Select value to map specific information during or post periodic write data leveling for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_WDQLVL_DQDM_OBS_SELECT_3	R/W	0h	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge observation registers during write data leveling for slice 3.

4.4.456 DDRSS_PHY_803 Register (Offset = 4C8Ch) [reset = X]

DDRSS_PHY_803 is shown in [Figure 4-1250](#) and described in [Table 4-2508](#).

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Table 4-2507. DDRSS_PHY_803 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C8Ch

Figure 4-1250. DDRSS_PHY_803 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_WDQLVL_DATADM_MASK_3							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2508. DDRSS_PHY_803 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_WDQLVL_DATADM_MASK_3	R/W	0h	Per-bit mask for write data leveling for slice 3. Set to 1 to mask any bit from the leveling process.

4.4.457 DDRSS_PHY_804 Register (Offset = 4C90h) [reset = 0h]

DDRSS_PHY_804 is shown in [Figure 4-1251](#) and described in [Table 4-2510](#).

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Table 4-2509. DDRSS_PHY_804 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C90h

Figure 4-1251. DDRSS_PHY_804 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT0_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2510. DDRSS_PHY_804 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT0_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 3 to 0 written/read from device.

4.4.458 DDRSS_PHY_805 Register (Offset = 4C94h) [reset = 0h]

DDRSS_PHY_805 is shown in [Figure 4-1252](#) and described in [Table 4-2512](#).

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Table 4-2511. DDRSS_PHY_805 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C94h

Figure 4-1252. DDRSS_PHY_805 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT1_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2512. DDRSS_PHY_805 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT1_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 7 to 4 written/read from device.

4.4.459 DDRSS_PHY_806 Register (Offset = 4C98h) [reset = 0h]

DDRSS_PHY_806 is shown in [Figure 4-1253](#) and described in [Table 4-2514](#).

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Table 4-2513. DDRSS_PHY_806 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C98h

Figure 4-1253. DDRSS_PHY_806 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT2_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2514. DDRSS_PHY_806 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT2_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 11 to 8 written/read from device.

4.4.460 DDRSS_PHY_807 Register (Offset = 4C9Ch) [reset = 0h]

DDRSS_PHY_807 is shown in [Figure 4-1254](#) and described in [Table 4-2516](#).

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Table 4-2515. DDRSS_PHY_807 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4C9Ch

Figure 4-1254. DDRSS_PHY_807 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_USER_PATT3_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2516. DDRSS_PHY_807 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_USER_PATT3_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 15 to 12 written/read from device.

4.4.461 DDRSS_PHY_808 Register (Offset = 4CA0h) [reset = X]

DDRSS_PHY_808 is shown in [Figure 4-1255](#) and described in [Table 4-2518](#).

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Table 4-2517. DDRSS_PHY_808 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CA0h

Figure 4-1255. DDRSS_PHY_808 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_MULT_TRAIN_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_USER_PATT4_3							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_USER_PATT4_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2518. DDRSS_PHY_808 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_NTP_MULT_TRAIN_3	R/W	0h	Control for single pass only No-Topology training for slice 3.
15-0	PHY_USER_PATT4_3	R/W	0h	User-defined pattern to be used during write data leveling for slice 3. This register holds the DM bit for the 15 to 0 DQ written/read from device.

4.4.462 DDRSS_PHY_809 Register (Offset = 4CA4h) [reset = X]

DDRSS_PHY_809 is shown in [Figure 4-1256](#) and described in [Table 4-2520](#).

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Table 4-2519. DDRSS_PHY_809 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CA4h

Figure 4-1256. DDRSS_PHY_809 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_EARLY_THRESHOLD_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2520. DDRSS_PHY_809 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_3	R/W	0h	Threshold Criteria of period threshold after No-Topology training is completed for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_EARLY_THRESHOLD_3	R/W	0h	Threshold Criteria of early threshold after No-Topology training is completed for slice 3.

4.4.463 DDRSS_PHY_810 Register (Offset = 4CA8h) [reset = X]

DDRSS_PHY_810 is shown in [Figure 4-1257](#) and described in [Table 4-2522](#).

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Table 4-2521. DDRSS_PHY_810 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CA8h

Figure 4-1257. DDRSS_PHY_810 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MAX_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_NTP_PERIOD_THRESHOLD_MIN_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2522. DDRSS_PHY_810 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_NTP_PERIOD_THRESHOLD_MAX_3	R/W	0h	Maximum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_NTP_PERIOD_THRESHOLD_MIN_3	R/W	0h	Minimum Threshold that phy_clk_wrdqs_slave_delay could cross boundary, to set period threshold/early threshold after No-Topology training is completed for slice 3.

4.4.464 DDRSS_PHY_811 Register (Offset = 4CACH) [reset = X]

DDRSS_PHY_811 is shown in [Figure 4-1258](#) and described in [Table 4-2524](#).

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Table 4-2523. DDRSS_PHY_811 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CACH

Figure 4-1258. DDRSS_PHY_811 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PHY_FIFO_PTR_OBS_3							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_MANUAL_CLEAR_3					
R/W-X		W-0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_CALVL_VREF_DRIVING_SLICE_3
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2524. DDRSS_PHY_811 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PHY_FIFO_PTR_OBS_3	R	0h	Observation register containing read entry FIFO pointers for slice 3. READ-ONLY
15-14	RESERVED	R/W	X	
13-8	SC_PHY_MANUAL_CLEAR_3	W	0h	Manual reset/clear of internal logic for slice 3. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/max lock values. Bit (3) is manual reset of master delay unlock counter. Bit (4) is reset of leveling error bit in the leveling status registers. Bit (5) is clearing of the gate tracking observation register. Set each bit to 1 to initiate/reset. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_CALVL_VREF_DRIVING_SLICE_3	R/W	0h	Indicates if slice 3 is used to drive the VREF value to the device during CA training.

4.4.465 DDRSS_PHY_812 Register (Offset = 4CB0h) [reset = 00100000h]

DDRSS_PHY_812 is shown in [Figure 4-1259](#) and described in [Table 4-2526](#).

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Table 4-2525. DDRSS_PHY_812 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CB0h

Figure 4-1259. DDRSS_PHY_812 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_RESULT_OBS_3																															
R-00100000h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2526. DDRSS_PHY_812 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_LPBK_RESULT_OBS_3	R	00100000h	Observation register containing loopback status/results for slice 3. READ-ONLY

4.4.466 DDRSS_PHY_813 Register (Offset = 4CB4h) [reset = X]

DDRSS_PHY_813 is shown in [Figure 4-1260](#) and described in [Table 4-2528](#).

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Table 4-2527. DDRSS_PHY_813 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CB4h

Figure 4-1260. DDRSS_PHY_813 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_MASTER_DLY_LOCK_OBS_3										
R-X					R-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LPBK_ERROR_COUNT_OBS_3															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2528. DDRSS_PHY_813 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_MASTER_DLY_LOCK_OBS_3	R	0h	Observation register containing master delay results for slice 3. READ-ONLY
15-0	PHY_LPBK_ERROR_COUNT_OBS_3	R	0h	Observation register containing total number of loopback error data for slice 3. READ-ONLY

4.4.467 DDRSS_PHY_814 Register (Offset = 4CB8h) [reset = X]

DDRSS_PHY_814 is shown in [Figure 4-1261](#) and described in [Table 4-2530](#).

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Table 4-2529. DDRSS_PHY_814 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CB8h

Figure 4-1261. DDRSS_PHY_814 Register

31	30	29	28	27	26	25	24
PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_3							
R-0h							
23	22	21	20	19	18	17	16
PHY_MEAS_DLY_STEP_VALUE_3							
R-0h							
15	14	13	12	11	10	9	8
RESERVED	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_3						
R-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_RDDQ_SLV_DLY_ENC_OBS_3						
R-X	R-0h						

LEGEND: R = Read Only; -n = value after reset

Table 4-2530. DDRSS_PHY_814 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS DQ rising edge adder slave delay encoded value for slice 3. READ-ONLY
23-16	PHY_MEAS_DLY_STEP_VALUE_3	R	0h	Observation register containing fraction of the cycle in 1 delay element, numerator with denominator of 512, for slice 3. READ-ONLY
15	RESERVED	R	X	
14-8	PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS base slave delay encoded value for slice 3. READ-ONLY
7	RESERVED	R	X	
6-0	PHY_RDDQ_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQ slave delay encoded values for slice 3. READ-ONLY

4.4.468 DDRSS_PHY_815 Register (Offset = 4CBCh) [reset = X]

DDRSS_PHY_815 is shown in Figure 4-1262 and described in Table 4-2532.

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Table 4-2531. DDRSS_PHY_815 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CBCh

Figure 4-1262. DDRSS_PHY_815 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_3						
R-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED					PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3		
R-X					R-0h		
15	14	13	12	11	10	9	8
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3							
R-0h							
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_3							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2532. DDRSS_PHY_815 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	X	
30-24	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing write DQS base slave delay encoded value for slice 3. READ-ONLY
23-19	RESERVED	R	X	
18-8	PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS gate slave delay encoded value for slice 3. READ-ONLY
7-0	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing read DQS DQ falling edge adder slave delay encoded value for slice 3. READ-ONLY

4.4.469 DDRSS_PHY_816 Register (Offset = 4CC0h) [reset = X]

DDRSS_PHY_816 is shown in Figure 4-1263 and described in Table 4-2534.

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Table 4-2533. DDRSS_PHY_816 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CC0h

Figure 4-1263. DDRSS_PHY_816 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_WR_SHIFT_OBS_3		
R-X					R-0h		
15	14	13	12	11	10	9	8
PHY_WR_ADDER_SLV_DLY_ENC_OBS_3							
R-0h							
7	6	5	4	3	2	1	0
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_3							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2534. DDRSS_PHY_816 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18-16	PHY_WR_SHIFT_OBS_3	R	0h	Observation register containing automatic half cycle and cycle shift values for slice 3. READ-ONLY
15-8	PHY_WR_ADDER_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing write adder slave delay encoded value for slice 3. READ-ONLY
7-0	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing write DQ base slave delay encoded value for slice 3. READ-ONLY

4.4.470 DDRSS_PHY_817 Register (Offset = 4CC4h) [reset = X]

DDRSS_PHY_817 is shown in [Figure 4-1264](#) and described in [Table 4-2536](#).

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Table 4-2535. DDRSS_PHY_817 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CC4h

Figure 4-1264. DDRSS_PHY_817 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_WRLVL_HARD1_DELAY_OBS_3									
R-X						R-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_HARD0_DELAY_OBS_3									
R-X						R-0h									

LEGEND: R = Read Only; -n = value after reset

Table 4-2536. DDRSS_PHY_817 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_WRLVL_HARD1_DELAY_OBS_3	R	0h	Observation register containing write leveling first hard 1 DQS slave delay for slice 3. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_WRLVL_HARD0_DELAY_OBS_3	R	0h	Observation register containing write leveling last hard 0 DQS slave delay for slice 3. READ-ONLY

4.4.471 DDRSS_PHY_818 Register (Offset = 4CC8h) [reset = X]

DDRSS_PHY_818 is shown in [Figure 4-1265](#) and described in [Table 4-2538](#).

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Table 4-2537. DDRSS_PHY_818 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CC8h

Figure 4-1265. DDRSS_PHY_818 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PHY_WRLVL_STATUS_OBS_3
R-X															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_STATUS_OBS_3															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2538. DDRSS_PHY_818 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-0	PHY_WRLVL_STATUS_OBS_3	R	0h	Observation register containing write leveling status for slice 3. READ-ONLY

4.4.472 DDRSS_PHY_819 Register (Offset = 4CCCh) [reset = X]

DDRSS_PHY_819 is shown in [Figure 4-1266](#) and described in [Table 4-2540](#).

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Table 4-2539. DDRSS_PHY_819 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CCCh

Figure 4-1266. DDRSS_PHY_819 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2540. DDRSS_PHY_819 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing gate sample2 slave delay encoded values for slice 3. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3	R	0h	Observation register containing gate sample1 slave delay encoded values for slice 3. READ-ONLY

4.4.473 DDRSS_PHY_820 Register (Offset = 4CD0h) [reset = X]

DDRSS_PHY_820 is shown in [Figure 4-1267](#) and described in [Table 4-2542](#).

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Table 4-2541. DDRSS_PHY_820 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CD0h

Figure 4-1267. DDRSS_PHY_820 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_GTLVL_HARD0_DELAY_OBS_3													
R-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WRLVL_ERROR_OBS_3															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2542. DDRSS_PHY_820 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29-16	PHY_GTLVL_HARD0_DELAY_OBS_3	R	0h	Observation register containing gate training first hard 0 DQS slave delay for slice 3. READ-ONLY
15-0	PHY_WRLVL_ERROR_OBS_3	R	0h	Observation register containing write leveling error status for slice 3. READ-ONLY

4.4.474 DDRSS_PHY_821 Register (Offset = 4CD4h) [reset = X]

DDRSS_PHY_821 is shown in [Figure 4-1268](#) and described in [Table 4-2544](#).

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Table 4-2543. DDRSS_PHY_821 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CD4h

Figure 4-1268. DDRSS_PHY_821 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PHY_GTLVL_HARD1_DELAY_OBS_3													
R-X		R-0h													

LEGEND: R = Read Only; -n = value after reset

Table 4-2544. DDRSS_PHY_821 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	X	
13-0	PHY_GTLVL_HARD1_DELAY_OBS_3	R	0h	Observation register containing gate training last hard 1 DQS slave delay for slice 3. READ-ONLY

4.4.475 DDRSS_PHY_822 Register (Offset = 4CD8h) [reset = X]

DDRSS_PHY_822 is shown in [Figure 4-1269](#) and described in [Table 4-2546](#).

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Table 4-2545. DDRSS_PHY_822 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CD8h

Figure 4-1269. DDRSS_PHY_822 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														PHY_GTLVL_STATUS_OBS_3	
R-X														R-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_GTLVL_STATUS_OBS_3															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2546. DDRSS_PHY_822 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	PHY_GTLVL_STATUS_OBS_3	R	0h	Observation register containing gate training status for slice 3. READ-ONLY

4.4.476 DDRSS_PHY_823 Register (Offset = 4CDCh) [reset = X]

DDRSS_PHY_823 is shown in Figure 4-1270 and described in Table 4-2548.

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Table 4-2547. DDRSS_PHY_823 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CDCh

Figure 4-1270. DDRSS_PHY_823 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3	
R-X						R-0h	
23	22	21	20	19	18	17	16
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3	
R-X						R-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2548. DDRSS_PHY_823 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	X	
25-16	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3	R	0h	Observation register containing read leveling data window trailing edge slave delay setting for slice 3. READ-ONLY
15-10	RESERVED	R	X	
9-0	PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3	R	0h	Observation register containing read leveling data window leading edge slave delay setting for slice 3. READ-ONLY

4.4.477 DDRSS_PHY_824 Register (Offset = 4CE0h) [reset = X]

DDRSS_PHY_824 is shown in [Figure 4-1271](#) and described in [Table 4-2550](#).

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Table 4-2549. DDRSS_PHY_824 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CE0h

Figure 4-1271. DDRSS_PHY_824 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_3	
R-X						R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 4-2550. DDRSS_PHY_824 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	X	
1-0	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_3	R	0h	Observation register containing read leveling number of windows found for slice 3. READ-ONLY

4.4.478 DDRSS_PHY_825 Register (Offset = 4CE4h) [reset = 0h]

DDRSS_PHY_825 is shown in [Figure 4-1272](#) and described in [Table 4-2552](#).

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Table 4-2551. DDRSS_PHY_825 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CE4h

Figure 4-1272. DDRSS_PHY_825 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_STATUS_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2552. DDRSS_PHY_825 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_STATUS_OBS_3	R	0h	Observation register containing read leveling status for slice 3. READ-ONLY

4.4.479 DDRSS_PHY_826 Register (Offset = 4CE8h) [reset = 0h]

DDRSS_PHY_826 is shown in [Figure 4-1273](#) and described in [Table 4-2554](#).

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Table 4-2553. DDRSS_PHY_826 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CE8h

Figure 4-1273. DDRSS_PHY_826 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_RDLVL_PERIODIC_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2554. DDRSS_PHY_826 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_RDLVL_PERIODIC_OBS_3	R	0h	Observation register containing periodic read leveling status for slice 3. READ-ONLY

4.4.480 DDRSS_PHY_827 Register (Offset = 4CECh) [reset = X]

DDRSS_PHY_827 is shown in [Figure 4-1274](#) and described in [Table 4-2556](#).

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Table 4-2555. DDRSS_PHY_827 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CECh

Figure 4-1274. DDRSS_PHY_827 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_WDQLVL_DQDM_TE_DLY_OBS_3										
R-X					R-7FFh										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_WDQLVL_DQDM_LE_DLY_OBS_3										
R-X					R-0h										

LEGEND: R = Read Only; -n = value after reset

Table 4-2556. DDRSS_PHY_827 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-16	PHY_WDQLVL_DQDM_TE_DLY_OBS_3	R	7FFh	Observation register containing write data leveling data window trailing edge slave delay setting for slice 3. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_WDQLVL_DQDM_LE_DLY_OBS_3	R	0h	Observation register containing write data leveling data window leading edge slave delay setting for slice 3. READ-ONLY

4.4.481 DDRSS_PHY_828 Register (Offset = 4CF0h) [reset = 0h]

DDRSS_PHY_828 is shown in [Figure 4-1275](#) and described in [Table 4-2558](#).

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Table 4-2557. DDRSS_PHY_828 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CF0h

Figure 4-1275. DDRSS_PHY_828 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_STATUS_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2558. DDRSS_PHY_828 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_STATUS_OBS_3	R	0h	Observation register containing write data leveling status for slice 3. READ-ONLY

4.4.482 DDRSS_PHY_829 Register (Offset = 4CF4h) [reset = 0h]

DDRSS_PHY_829 is shown in [Figure 4-1276](#) and described in [Table 4-2560](#).

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Table 4-2559. DDRSS_PHY_829 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CF4h

Figure 4-1276. DDRSS_PHY_829 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_WDQLVL_PERIODIC_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2560. DDRSS_PHY_829 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_WDQLVL_PERIODIC_OBS_3	R	0h	Observation register containing periodic write data leveling status for slice 3. READ-ONLY

4.4.483 DDRSS_PHY_830 Register (Offset = 4CF8h) [reset = X]

DDRSS_PHY_830 is shown in [Figure 4-1277](#) and described in [Table 4-2562](#).

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Table 4-2561. DDRSS_PHY_830 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CF8h

Figure 4-1277. DDRSS_PHY_830 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE SE RV ED	PHY_DDL_MODE_3																														
R/ W- X	R/W-0h																														

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2562. DDRSS_PHY_830 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-0	PHY_DDL_MODE_3	R/W	0h	DDL mode for slice 3.

4.4.484 DDRSS_PHY_831 Register (Offset = 4CFCh) [reset = X]

DDRSS_PHY_831 is shown in [Figure 4-1278](#) and described in [Table 4-2564](#).

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Table 4-2563. DDRSS_PHY_831 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4CFCh

Figure 4-1278. DDRSS_PHY_831 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PHY_DDL_MASK_3					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2564. DDRSS_PHY_831 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	PHY_DDL_MASK_3	R/W	0h	DDL mask for slice 3.

4.4.485 DDRSS_PHY_832 Register (Offset = 4D00h) [reset = 0h]

DDRSS_PHY_832 is shown in [Figure 4-1279](#) and described in [Table 4-2566](#).

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Table 4-2565. DDRSS_PHY_832 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D00h

Figure 4-1279. DDRSS_PHY_832 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2566. DDRSS_PHY_832 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_OBS_3	R	0h	DDL test observation for slice 3. READ-ONLY

4.4.486 DDRSS_PHY_833 Register (Offset = 4D04h) [reset = 0h]

DDRSS_PHY_833 is shown in [Figure 4-1280](#) and described in [Table 4-2568](#).

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Table 4-2567. DDRSS_PHY_833 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D04h

Figure 4-1280. DDRSS_PHY_833 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_TEST_MSTR_DLY_OBS_3																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2568. DDRSS_PHY_833 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_TEST_MSTR_DLY_OBS_3	R	0h	DDL test observation delays for slice 3 master DDL. READ-ONLY

4.4.487 DDRSS_PHY_834 Register (Offset = 4D08h) [reset = X]

DDRSS_PHY_834 is shown in Figure 4-1281 and described in Table 4-2570.

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Table 4-2569. DDRSS_PHY_834 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D08h

Figure 4-1281. DDRSS_PHY_834 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_OVERRIDE_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_RX_CAL_START_3
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_LP4_WDQS_OE_EXTEND_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_DDL_TRACK_UPD_THRESHOLD_3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2570. DDRSS_PHY_834 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_OVERRIDE_3	R/W	0h	Manual setting of RX Calibration enable for slice 3.
23-17	RESERVED	R/W	X	
16	SC_PHY_RX_CAL_START_3	W	0h	Manual RX Calibration start for slice 3. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	PHY_LP4_WDQS_OE_EXTEND_3	R/W	0h	LPDDR4 write preamble extension enable for slice 3.
7-0	PHY_DDL_TRACK_UPD_THRESHOLD_3	R/W	0h	Specify threshold value for PHY init update tracking for slice 3.

4.4.488 DDRSS_PHY_835 Register (Offset = 4D0Ch) [reset = X]

DDRSS_PHY_835 is shown in [Figure 4-1282](#) and described in [Table 4-2572](#).

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Table 4-2571. DDRSS_PHY_835 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D0Ch

Figure 4-1282. DDRSS_PHY_835 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_DQ0_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_RX_CAL_DQ0_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_RX_CAL_SAMPLE_WAIT_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2572. DDRSS_PHY_835 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ0_3	R/W	0h	RX Calibration codes for DQ0 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8	PHY_SLICE_RXCAL_SHUTOFF_FDBK_OE_3	R/W	0h	Data slice power reduction disable for slice 3.
7-0	PHY_RX_CAL_SAMPLE_WAIT_3	R/W	0h	RX Calibration state machine wait count for slice 3.

4.4.489 DDRSS_PHY_836 Register (Offset = 4D10h) [reset = X]

DDRSS_PHY_836 is shown in [Figure 4-1283](#) and described in [Table 4-2574](#).

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Table 4-2573. DDRSS_PHY_836 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D10h

Figure 4-1283. DDRSS_PHY_836 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ2_3							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ1_3							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2574. DDRSS_PHY_836 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ2_3	R/W	0h	RX Calibration codes for DQ2 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ1_3	R/W	0h	RX Calibration codes for DQ1 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.490 DDRSS_PHY_837 Register (Offset = 4D14h) [reset = X]

DDRSS_PHY_837 is shown in Figure 4-1284 and described in Table 4-2576.

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Table 4-2575. DDRSS_PHY_837 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D14h

Figure 4-1284. DDRSS_PHY_837 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ4_3							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ3_3							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2576. DDRSS_PHY_837 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ4_3	R/W	0h	RX Calibration codes for DQ4 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ3_3	R/W	0h	RX Calibration codes for DQ3 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.491 DDRSS_PHY_838 Register (Offset = 4D18h) [reset = X]

DDRSS_PHY_838 is shown in [Figure 4-1285](#) and described in [Table 4-2578](#).

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Table 4-2577. DDRSS_PHY_838 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D18h

Figure 4-1285. DDRSS_PHY_838 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_DQ6_3							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ5_3							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2578. DDRSS_PHY_838 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_DQ6_3	R/W	0h	RX Calibration codes for DQ6 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ5_3	R/W	0h	RX Calibration codes for DQ5 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.492 DDRSS_PHY_839 Register (Offset = 4D1Ch) [reset = X]

DDRSS_PHY_839 is shown in [Figure 4-1286](#) and described in [Table 4-2580](#).

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Table 4-2579. DDRSS_PHY_839 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D1Ch

Figure 4-1286. DDRSS_PHY_839 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQ7_3							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2580. DDRSS_PHY_839 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQ7_3	R/W	0h	RX Calibration codes for DQ7 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.493 DDRSS_PHY_840 Register (Offset = 4D20h) [reset = X]

DDRSS_PHY_840 is shown in [Figure 4-1287](#) and described in [Table 4-2582](#).

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Table 4-2581. DDRSS_PHY_840 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D20h

Figure 4-1287. DDRSS_PHY_840 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_RX_CAL_DM_3																	
R/W-X														R/W-0h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2582. DDRSS_PHY_840 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_RX_CAL_DM_3	R/W	0h	RX Calibration codes for DM for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.494 DDRSS_PHY_841 Register (Offset = 4D24h) [reset = X]

DDRSS_PHY_841 is shown in Figure 4-1288 and described in Table 4-2584.

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Table 4-2583. DDRSS_PHY_841 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D24h

Figure 4-1288. DDRSS_PHY_841 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_FDBK_3							
R/W-X								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_DQS_3							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2584. DDRSS_PHY_841 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_RX_CAL_FDBK_3	R/W	0h	RX Calibration codes for FDBK for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.
15-9	RESERVED	R/W	X	
8-0	PHY_RX_CAL_DQS_3	R/W	0h	RX Calibration codes for DQS for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits (17:12) contain rx_cal_code2_down. Bits (23:18) contain rx_cal_code2_up.

4.4.495 DDRSS_PHY_842 Register (Offset = 4D28h) [reset = X]

DDRSS_PHY_842 is shown in [Figure 4-1289](#) and described in [Table 4-2586](#).

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Table 4-2585. DDRSS_PHY_842 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D28h

Figure 4-1289. DDRSS_PHY_842 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								PHY_RX_CAL_LOCK_OBS_3							
R-X								R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_RX_CAL_OBS_3							
R-X								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2586. DDRSS_PHY_842 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	X	
24-16	PHY_RX_CAL_LOCK_OBS_3	R	0h	RX Calibration lock results for slice 3. Bit (3:0) is the state machine rx_cal_sm. Bit (4) is the rx_cal_done signal. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_RX_CAL_OBS_3	R	0h	RX Calibration results for slice 3. Bits (7:0) contain calibration results from DQ 0-7. Bit (8) contains calibration result from DM. Bit (9) contains calibration result from DQS. Bit (10) contains calibration result from FDBK. READ-ONLY

4.4.496 DDRSS_PHY_843 Register (Offset = 4D2Ch) [reset = X]

DDRSS_PHY_843 is shown in Figure 4-1290 and described in Table 4-2588.

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Table 4-2587. DDRSS_PHY_843 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D2Ch

Figure 4-1290. DDRSS_PHY_843 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_RX_CAL_COMP_VAL_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED	PHY_RX_CAL_DIFF_ADJUST_3						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_RX_CAL_SE_ADJUST_3						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED							PHY_RX_CAL_DISABLE_3
R/W-X							R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2588. DDRSS_PHY_843 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_RX_CAL_COMP_VAL_3	R/W	0h	Expected C value from RX pad for slice 3.
23	RESERVED	R/W	X	
22-16	PHY_RX_CAL_DIFF_ADJUST_3	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 3.
15	RESERVED	R/W	X	
14-8	PHY_RX_CAL_SE_ADJUST_3	R/W	0h	Fine adjustment for Single-Ended RX pad of RX CAL V2 for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_RX_CAL_DISABLE_3	R/W	1h	RX CAL disable signal for slice 3, set 1 to bypass the rx calibration

4.4.497 DDRSS_PHY_844 Register (Offset = 4D30h) [reset = X]

DDRSS_PHY_844 is shown in [Figure 4-1291](#) and described in [Table 4-2590](#).

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Table 4-2589. DDRSS_PHY_844 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D30h

Figure 4-1291. DDRSS_PHY_844 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_PAD_RX_BIAS_EN_3										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_RX_CAL_INDEX_MASK_3										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2590. DDRSS_PHY_844 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PAD_RX_BIAS_EN_3	R/W	0h	Controls RX_BIAS_EN pin for each pad for slice 3.
15-12	RESERVED	R/W	X	
11-0	PHY_RX_CAL_INDEX_MASK_3	R/W	0h	RX offset calibration mask of all RX pad for slice 3.

4.4.498 DDRSS_PHY_845 Register (Offset = 4D34h) [reset = X]

DDRSS_PHY_845 is shown in Figure 4-1292 and described in Table 4-2592.

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Table 4-2591. DDRSS_PHY_845 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D34h

Figure 4-1292. DDRSS_PHY_845 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_DATA_DC_WEIGHT_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DATA_DC_CAL_TIMEOUT_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_CAL_SAMPLE_WAIT_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_STATIC_TOG_DISABLE_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2592. DDRSS_PHY_845 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_DATA_DC_WEIGHT_3	R/W	0h	Determines weight of average calculating for slice 3.
23-16	PHY_DATA_DC_CAL_TIMEOUT_3	R/W	0h	Determines timeout number of iteration for slice 3.
15-8	PHY_DATA_DC_CAL_SAMPLE_WAIT_3	R/W	0h	Determines number of cycles to wait for each sample for slice 3.
7-5	RESERVED	R/W	X	
4-0	PHY_STATIC_TOG_DISABLE_3	R/W	0h	Control to disable toggle during static activity for slice 3. bit 0: Write path delay line disable bit 1: Read path delay line disable bit 2: Read data path disable bit 3: clk_phy disable bit 4: master delay line disable.

4.4.499 DDRSS_PHY_846 Register (Offset = 4D38h) [reset = X]

DDRSS_PHY_846 is shown in [Figure 4-1293](#) and described in [Table 4-2594](#).

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Table 4-2593. DDRSS_PHY_846 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D38h

Figure 4-1293. DDRSS_PHY_846 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_DATA_DC_ADJUST_DIRECT_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_DATA_DC_ADJUST_THRSHLD_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_ADJUST_SAMPLE_CNT_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		PHY_DATA_DC_ADJUST_START_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2594. DDRSS_PHY_846 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_DATA_DC_ADJUST_DIRECT_3	R/W	0h	Adjust direction for slice 3.
23-16	PHY_DATA_DC_ADJUST_THRSHLD_3	R/W	0h	Duty cycle adjust threshold around the mid-point for slice 3.
15-8	PHY_DATA_DC_ADJUST_SAMPLE_CNT_3	R/W	0h	Duty cycle adjust sample count for slice 3.
7-6	RESERVED	R/W	X	
5-0	PHY_DATA_DC_ADJUST_START_3	R/W	0h	Duty cycle adjust starting value for slice 3.

4.4.500 DDRSS_PHY_847 Register (Offset = 4D3Ch) [reset = X]

DDRSS_PHY_847 is shown in Figure 4-1294 and described in Table 4-2596.

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Table 4-2595. DDRSS_PHY_847 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D3Ch

Figure 4-1294. DDRSS_PHY_847 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_FDBK_PWR_CTRL_3		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_SW_RANK_3	
R/W-X						R/W-1h	
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_CAL_START_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_CAL_POLARITY_3
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2596. DDRSS_PHY_847 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_FDBK_PWR_CTRL_3	R/W	0h	Shutoff gate feedback IO to reduce power for slice 3.
23-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_SW_RANK_3	R/W	1h	Rank selection for software based duty cycle correction for slice 3.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_CAL_START_3	R/W	0h	Manual trigger for DCC for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_CAL_POLARITY_3	R/W	0h	Calibration polarity for slice 3.

4.4.501 DDRSS_PHY_848 Register (Offset = 4D40h) [reset = X]

DDRSS_PHY_848 is shown in [Figure 4-1295](#) and described in [Table 4-2598](#).

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Table 4-2597. DDRSS_PHY_848 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D40h

Figure 4-1295. DDRSS_PHY_848 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SLICE_PWR_RDC_DISABLE_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_DCC_RXCAL_CTRL_GATE_DISABLE_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_RDPATH_GATE_DISABLE_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_SLV_DLY_CTRL_GATE_DISABLE_3
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2598. DDRSS_PHY_848 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SLICE_PWR_RDC_DISABLE_3	R/W	0h	Data slice power reduction disable for slice 3.
23-17	RESERVED	R/W	X	
16	PHY_DCC_RXCAL_CTRL_GATE_DISABLE_3	R/W	0h	Data slice DCC and RX_CAL block power reduction disable for slice 3.
15-9	RESERVED	R/W	X	
8	PHY_RDPATH_GATE_DISABLE_3	R/W	0h	Data slice read path power reduction disable for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_SLV_DLY_CTRL_GATE_DISABLE_3	R/W	0h	Data slice slv_dly_control block power reduction disable for slice 3.

4.4.502 DDRSS_PHY_849 Register (Offset = 4D44h) [reset = X]

DDRSS_PHY_849 is shown in [Figure 4-1296](#) and described in [Table 4-2600](#).

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Table 4-2599. DDRSS_PHY_849 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D44h

Figure 4-1296. DDRSS_PHY_849 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		PHY_DS_FSM_ERROR_INFO_3													
R/W-X		R-0h													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_PARITY_ERROR_REGIF_3										
R/W-X					R/W-0h										

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2600. DDRSS_PHY_849 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_DS_FSM_ERROR_INFO_3	R	0h	Data slice level FSM Error Info for slice 3. READ-ONLY
15-11	RESERVED	R/W	X	
10-0	PHY_PARITY_ERROR_REGIF_3	R/W	0h	Inject parity error to register interface signals for slice 3.

4.4.503 DDRSS_PHY_850 Register (Offset = 4D48h) [reset = X]

DDRSS_PHY_850 is shown in [Figure 4-1297](#) and described in [Table 4-2602](#).

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Table 4-2601. DDRSS_PHY_850 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D48h

Figure 4-1297. DDRSS_PHY_850 Register

31	30	29	28	27	26	25	24
RESERVED		SC_PHY_DS_FSM_ERROR_INFO_WOCLR_3					
R/W-X		W-0h					
23	22	21	20	19	18	17	16
SC_PHY_DS_FSM_ERROR_INFO_WOCLR_3							
W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_DS_FSM_ERROR_INFO_MASK_3					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
PHY_DS_FSM_ERROR_INFO_MASK_3							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2602. DDRSS_PHY_850 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	SC_PHY_DS_FSM_ERROR_INFO_WOCLR_3	W	0h	Data slice level FSM Error Info for slice 3. WRITE-ONLY
15-14	RESERVED	R/W	X	
13-0	PHY_DS_FSM_ERROR_INFO_MASK_3	R/W	0h	Data slice level FSM Error Info Mask for slice 3.

4.4.504 DDRSS_PHY_851 Register (Offset = 4D4Ch) [reset = X]

DDRSS_PHY_851 is shown in [Figure 4-1298](#) and described in [Table 4-2604](#).

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Table 4-2603. DDRSS_PHY_851 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D4Ch

Figure 4-1298. DDRSS_PHY_851 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_3			
R/W-X				W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_DS_TRAIN_CALIB_ERROR_INFO_3			
R/W-X				R-0h			

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2604. DDRSS_PHY_851 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	SC_PHY_DS_TRAIN_CALIB_ERROR_INFO_WOCLR_3	W	0h	Data slice level training/calibration Error Info for slice 3. WRITE-ONLY
15-13	RESERVED	R/W	X	
12-8	PHY_DS_TRAIN_CALIB_ERROR_INFO_MASK_3	R/W	0h	Data slice level training/calibration Error Info Mask for slice 3.
7-5	RESERVED	R/W	X	
4-0	PHY_DS_TRAIN_CALIB_ERROR_INFO_3	R	0h	Data slice level training/calibration Error Info for slice 3. READ-ONLY

4.4.505 DDRSS_PHY_852 Register (Offset = 4D50h) [reset = X]

DDRSS_PHY_852 is shown in [Figure 4-1299](#) and described in [Table 4-2606](#).

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Table 4-2605. DDRSS_PHY_852 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D50h

Figure 4-1299. DDRSS_PHY_852 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DQS_TSEL_ENABLE_3		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DQ_TSEL_SELECT_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_TSEL_SELECT_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_DQ_TSEL_ENABLE_3		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2606. DDRSS_PHY_852 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_DQS_TSEL_ENABLE_3	R/W	0h	Operation type tsel enables for DQS signals for slice 3. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.
23-8	PHY_DQ_TSEL_SELECT_3	R/W	0h	Operation type tsel select values for DQ/DM signals for slice 3.
7-3	RESERVED	R/W	X	
2-0	PHY_DQ_TSEL_ENABLE_3	R/W	0h	Operation type tsel enables for DQ/DM signals for slice 3. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write cycles. Bit (2) enables tsel_en during idle cycles. Set each bit to 1 to enable.

4.4.506 DDRSS_PHY_853 Register (Offset = 4D54h) [reset = X]

DDRSS_PHY_853 is shown in [Figure 4-1300](#) and described in [Table 4-2608](#).

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Table 4-2607. DDRSS_PHY_853 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D54h

Figure 4-1300. DDRSS_PHY_853 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_VREF_INITIAL_START_POINT_3						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
RESERVED						PHY_TWO_CYC_PREAMBLE_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_SELECT_3							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_DQS_TSEL_SELECT_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2608. DDRSS_PHY_853 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PHY_VREF_INITIAL_START_POINT_3	R/W	0h	Data slice initial VREF training start value for slice 3.
23-18	RESERVED	R/W	X	
17-16	PHY_TWO_CYC_PREAMBLE_3	R/W	0h	2 cycle preamble support for slice 3. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2 cycle write preamble. Set each bit to 1 to enable.
15-0	PHY_DQS_TSEL_SELECT_3	R/W	0h	Operation type tsel select values for DQS signals for slice 3.

4.4.507 DDRSS_PHY_854 Register (Offset = 4D58h) [reset = X]

DDRSS_PHY_854 is shown in Figure 4-1301 and described in Table 4-2610.

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Table 4-2609. DDRSS_PHY_854 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D58h

Figure 4-1301. DDRSS_PHY_854 Register

31	30	29	28	27	26	25	24
PHY_NTP_WDQ_STEP_SIZE_3							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED							PHY_NTP_TRAIN_EN_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_VREF_TRAINING_CTRL_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	PHY_VREF_INITIAL_STOP_POINT_3						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2610. DDRSS_PHY_854 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_NTP_WDQ_STEP_SIZE_3	R/W	0h	Step size of WR DQ slave delay during No-Topology training for slice 3.
23-17	RESERVED	R/W	X	
16	PHY_NTP_TRAIN_EN_3	R/W	0h	Enable for No-Topology training for slice 3.
15-10	RESERVED	R/W	X	
9-8	PHY_VREF_TRAINING_CTRL_3	R/W	0h	Data slice vref training enable control for slice 3.
7	RESERVED	R/W	X	
6-0	PHY_VREF_INITIAL_STOP_POINT_3	R/W	0h	Data slice initial VREF training stop value for slice 3.

4.4.508 DDRSS_PHY_855 Register (Offset = 4D5Ch) [reset = X]

DDRSS_PHY_855 is shown in [Figure 4-1302](#) and described in [Table 4-2612](#).

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Table 4-2611. DDRSS_PHY_855 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D5Ch

Figure 4-1302. DDRSS_PHY_855 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_NTP_WDQ_STOP_3										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_NTP_WDQ_START_3										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2612. DDRSS_PHY_855 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_NTP_WDQ_STOP_3	R/W	0h	End of WR DQ slave delay in No-Topology training for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_NTP_WDQ_START_3	R/W	0h	Starting WR DQ slave delay in No-Topology training for slice 3.

4.4.509 DDRSS_PHY_856 Register (Offset = 4D60h) [reset = X]

DDRSS_PHY_856 is shown in [Figure 4-1303](#) and described in [Table 4-2614](#).

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Table 4-2613. DDRSS_PHY_856 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D60h

Figure 4-1303. DDRSS_PHY_856 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_SW_WDQLVL_DVW_MIN_EN_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_WDQLVL_DVW_MIN_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_WDQLVL_DVW_MIN_3							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_NTP_WDQ_BIT_EN_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2614. DDRSS_PHY_856 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_SW_WDQLVL_DVW_MIN_EN_3	R/W	0h	SW override to enable use of PHY_WDQLVL_DVW_MIN for slice 3.
23-18	RESERVED	R/W	X	
17-8	PHY_WDQLVL_DVW_MIN_3	R/W	0h	Minimum data valid window across DQs and ranks for slice 3.
7-0	PHY_NTP_WDQ_BIT_EN_3	R/W	0h	Enable Bit for WR DQ during No-Topology training for slice 3.

4.4.510 DDRSS_PHY_857 Register (Offset = 4D64h) [reset = X]

DDRSS_PHY_857 is shown in [Figure 4-1304](#) and described in [Table 4-2616](#).

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Table 4-2615. DDRSS_PHY_857 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D64h

Figure 4-1304. DDRSS_PHY_857 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_0_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_TX_DCD_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_FAST_LVL_EN_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQLVL_PER_START_OFFSET_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2616. DDRSS_PHY_857 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_0_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_TX_DCD_3	R/W	0h	Controls TX_DCD pin for each pad for slice 3.
15-12	RESERVED	R/W	X	
11-8	PHY_FAST_LVL_EN_3	R/W	0h	Enable for fast multi-pattern window search for slice 3.
7-6	RESERVED	R/W	X	
5-0	PHY_WDQLVL_PER_START_OFFSET_3	R/W	0h	Periodic training start point offset for slice 3.

4.4.511 DDRSS_PHY_858 Register (Offset = 4D68h) [reset = X]

DDRSS_PHY_858 is shown in [Figure 4-1305](#) and described in [Table 4-2618](#).

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Table 4-2617. DDRSS_PHY_858 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D68h

Figure 4-1305. DDRSS_PHY_858 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_RX_DCD_4_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_3_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_2_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_1_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2618. DDRSS_PHY_858 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_RX_DCD_4_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_3_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_2_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_1_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.

4.4.512 DDRSS_PHY_859 Register (Offset = 4D6Ch) [reset = X]

DDRSS_PHY_859 is shown in [Figure 4-1306](#) and described in [Table 4-2620](#).

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Table 4-2619. DDRSS_PHY_859 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D6Ch

Figure 4-1306. DDRSS_PHY_859 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PAD_DM_RX_DCD_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_RX_DCD_7_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_RX_DCD_6_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_PAD_RX_DCD_5_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2620. DDRSS_PHY_859 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PAD_DM_RX_DCD_3	R/W	0h	Controls RX_DCD pin for dm pad for slice 3.
23-21	RESERVED	R/W	X	
20-16	PHY_PAD_RX_DCD_7_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_RX_DCD_6_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_RX_DCD_5_3	R/W	0h	Controls RX_DCD pin for each pad for slice 3.

4.4.513 DDRSS_PHY_860 Register (Offset = 4D70h) [reset = X]

DDRSS_PHY_860 is shown in [Figure 4-1307](#) and described in [Table 4-2622](#).

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Table 4-2621. DDRSS_PHY_860 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D70h

Figure 4-1307. DDRSS_PHY_860 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PHY_PAD_DSLICE_IO_CFG_3					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED			PHY_PAD_FDBK_RX_DCD_3				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED			PHY_PAD_DQS_RX_DCD_3				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2622. DDRSS_PHY_860 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PHY_PAD_DSLICE_IO_CFG_3	R/W	0h	Controls PCLK/PARK pin for pad for slice 3.
15-13	RESERVED	R/W	X	
12-8	PHY_PAD_FDBK_RX_DCD_3	R/W	0h	Controls RX_DCD pin for fdbk pad for slice 3.
7-5	RESERVED	R/W	X	
4-0	PHY_PAD_DQS_RX_DCD_3	R/W	0h	Controls RX_DCD pin for dqs pad for slice 3.

4.4.514 DDRSS_PHY_861 Register (Offset = 4D74h) [reset = X]

DDRSS_PHY_861 is shown in [Figure 4-1308](#) and described in [Table 4-2624](#).

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Table 4-2623. DDRSS_PHY_861 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D74h

Figure 4-1308. DDRSS_PHY_861 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ1_SLAVE_DELAY_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ0_SLAVE_DELAY_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2624. DDRSS_PHY_861 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ1_SLAVE_DELAY_3	R/W	0h	Read DQ1 slave delay setting for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ0_SLAVE_DELAY_3	R/W	0h	Read DQ0 slave delay setting for slice 3.

4.4.515 DDRSS_PHY_862 Register (Offset = 4D78h) [reset = X]

DDRSS_PHY_862 is shown in [Figure 4-1309](#) and described in [Table 4-2626](#).

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Table 4-2625. DDRSS_PHY_862 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D78h

Figure 4-1309. DDRSS_PHY_862 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ3_SLAVE_DELAY_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ2_SLAVE_DELAY_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2626. DDRSS_PHY_862 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ3_SLAVE_DELAY_3	R/W	0h	Read DQ3 slave delay setting for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ2_SLAVE_DELAY_3	R/W	0h	Read DQ2 slave delay setting for slice 3.

4.4.516 DDRSS_PHY_863 Register (Offset = 4D7Ch) [reset = X]

DDRSS_PHY_863 is shown in [Figure 4-1310](#) and described in [Table 4-2628](#).

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Table 4-2627. DDRSS_PHY_863 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D7Ch

Figure 4-1310. DDRSS_PHY_863 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ5_SLAVE_DELAY_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ4_SLAVE_DELAY_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2628. DDRSS_PHY_863 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ5_SLAVE_DELAY_3	R/W	0h	Read DQ5 slave delay setting for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ4_SLAVE_DELAY_3	R/W	0h	Read DQ4 slave delay setting for slice 3.

4.4.517 DDRSS_PHY_864 Register (Offset = 4D80h) [reset = X]

DDRSS_PHY_864 is shown in [Figure 4-1311](#) and described in [Table 4-2630](#).

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Table 4-2629. DDRSS_PHY_864 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D80h

Figure 4-1311. DDRSS_PHY_864 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQ7_SLAVE_DELAY_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDDQ6_SLAVE_DELAY_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2630. DDRSS_PHY_864 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQ7_SLAVE_DELAY_3	R/W	0h	Read DQ7 slave delay setting for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQ6_SLAVE_DELAY_3	R/W	0h	Read DQ6 slave delay setting for slice 3.

4.4.518 DDRSS_PHY_865 Register (Offset = 4D84h) [reset = X]

DDRSS_PHY_865 is shown in [Figure 4-1312](#) and described in [Table 4-2632](#).

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Table 4-2631. DDRSS_PHY_865 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D84h

Figure 4-1312. DDRSS_PHY_865 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_DATA_DC_CAL_CLK_SEL_3		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDM_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDM_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2632. DDRSS_PHY_865 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-16	PHY_DATA_DC_CAL_CLK_SEL_3	R/W	0h	Determines DCC CAL clock for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDM_SLAVE_DELAY_3	R/W	0h	Read DM/DBI slave delay setting for slice 3. May be used for data swap.

4.4.519 DDRSS_PHY_866 Register (Offset = 4D88h) [reset = 0h]

DDRSS_PHY_866 is shown in [Figure 4-1313](#) and described in [Table 4-2634](#).

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Table 4-2633. DDRSS_PHY_866 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D88h

Figure 4-1313. DDRSS_PHY_866 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PHY_DQS_OE_TIMING_3								PHY_DQ_TSEL_WR_TIMING_3							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_TSEL_RD_TIMING_3								PHY_DQ_OE_TIMING_3							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2634. DDRSS_PHY_866 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_OE_TIMING_3	R/W	0h	Start/end timing values for DQS output enable signals for slice 3.
23-16	PHY_DQ_TSEL_WR_TIMING_3	R/W	0h	Start/end timing values for DQ/DM write based termination enable and select signals for slice 3.
15-8	PHY_DQ_TSEL_RD_TIMING_3	R/W	0h	Start/end timing values for DQ/DM read based termination enable and select signals for slice 3.
7-0	PHY_DQ_OE_TIMING_3	R/W	0h	Start/end timing values for DQ/DM output enable signals for slice 3.

4.4.520 DDRSS_PHY_867 Register (Offset = 4D8Ch) [reset = X]

DDRSS_PHY_867 is shown in [Figure 4-1314](#) and described in [Table 4-2636](#).

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Table 4-2635. DDRSS_PHY_867 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D8Ch

Figure 4-1314. DDRSS_PHY_867 Register

31	30	29	28	27	26	25	24
PHY_DQS_TSEL_WR_TIMING_3							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DQS_OE_RD_TIMING_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQS_TSEL_RD_TIMING_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_IO_PAD_DELAY_TIMING_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2636. DDRSS_PHY_867 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DQS_TSEL_WR_TIMING_3	R/W	0h	Start/end timing values for DQS write based termination enable and select signals for slice 3.
23-16	PHY_DQS_OE_RD_TIMING_3	R/W	0h	Start/end timing values for DQS read based OE extension for slice 3.
15-8	PHY_DQS_TSEL_RD_TIMING_3	R/W	0h	Start/end timing values for DQS read based termination enable and select signals for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_IO_PAD_DELAY_TIMING_3	R/W	0h	Feedback pad's OPAD and IPAD delay timing for slice 3.

4.4.521 DDRSS_PHY_868 Register (Offset = 4D90h) [reset = X]

DDRSS_PHY_868 is shown in [Figure 4-1315](#) and described in [Table 4-2638](#).

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Table 4-2637. DDRSS_PHY_868 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D90h

Figure 4-1315. DDRSS_PHY_868 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PHY_PAD_VREF_CTRL_DQ_3											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_VREF_SETTING_TIME_3															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2638. DDRSS_PHY_868 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-16	PHY_PAD_VREF_CTRL_DQ_3	R/W	0h	Pad VREF control settings for DQ slice 3. <ul style="list-style-type: none"> Bits[27-24] = MODE Bits[23] = EN Bits[22-16] = VREFSEL
15-0	PHY_VREF_SETTING_TIME_3	R/W	0h	Number of cycles for vref settle after setting is changed for slice 3.

4.4.522 DDRSS_PHY_869 Register (Offset = 4D94h) [reset = X]

DDRSS_PHY_869 is shown in Figure 4-1316 and described in Table 4-2640.

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Table 4-2639. DDRSS_PHY_869 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D94h

Figure 4-1316. DDRSS_PHY_869 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDATA_EN_IE_DLY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_DQS_IE_TIMING_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DQ_IE_TIMING_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_PER_CS_TRAINING_EN_3	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2640. DDRSS_PHY_869 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_RDDATA_EN_IE_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for input enable generation for slice 3.
23-16	PHY_DQS_IE_TIMING_3	R/W	0h	Start/end timing values for DQS input enable signals for slice 3.
15-8	PHY_DQ_IE_TIMING_3	R/W	0h	Start/end timing values for DQ/DM input enable signals for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_PER_CS_TRAINING_EN_3	R/W	0h	Enables the per-rank training and read/write timing capabilities for slice 3. Must have same value in all slices.

4.4.523 DDRSS_PHY_870 Register (Offset = 4D98h) [reset = X]

DDRSS_PHY_870 is shown in Figure 4-1317 and described in Table 4-2642.

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Table 4-2641. DDRSS_PHY_870 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D98h

Figure 4-1317. DDRSS_PHY_870 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDDATA_EN_OE_DLY_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_TSEL_DLY_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_DBI_MODE_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PHY_IE_MODE_3	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2642. DDRSS_PHY_870 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_RDDATA_EN_OE_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for LP4 OE extension generation for slice 3.
23-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_TSEL_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is earlier than necessary for TSEL enable generation for slice 3.
15-9	RESERVED	R/W	X	
8	PHY_DBI_MODE_3	R/W	0h	DBI mode for slice 3. Bit (0) enables return of DBI read data.
7-2	RESERVED	R/W	X	
1-0	PHY_IE_MODE_3	R/W	0h	Input enable mode bits for slice 3. Bit (0) enables the mode where the input enables are always on set to 1 to enable. Bit (1) disables the input enable on the DM signal set to 1 to disable.

4.4.524 DDRSS_PHY_871 Register (Offset = 4D9Ch) [reset = X]

DDRSS_PHY_871 is shown in [Figure 4-1318](#) and described in [Table 4-2644](#).

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Table 4-2643. DDRSS_PHY_871 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4D9Ch

Figure 4-1318. DDRSS_PHY_871 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_MASTER_DELAY_STEP_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_MASTER_DELAY_START_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_START_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_MASTER_MODE_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2644. DDRSS_PHY_871 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_MASTER_DELAY_STEP_3	R/W	0h	Incremental step size for master delay line locking algorithm for slice 3.
23-19	RESERVED	R/W	X	
18-8	PHY_MASTER_DELAY_START_3	R/W	0h	Start value for master delay line locking algorithm for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_SW_MASTER_MODE_3	R/W	0h	Master delay line override settings for slice 3. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit (2) enables software bypass mode. Bit (3) is the software bypass mode value.

4.4.525 DDRSS_PHY_872 Register (Offset = 4DA0h) [reset = X]

DDRSS_PHY_872 is shown in Figure 4-1319 and described in Table 4-2646.

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Table 4-2645. DDRSS_PHY_872 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DA0h

Figure 4-1319. DDRSS_PHY_872 Register

31	30	29	28	27	26	25	24
PHY_WRLVL_DLY_STEP_3							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_RPTR_UPDATE_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PHY_MASTER_DELAY_HALF_MEASURE_3							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_MASTER_DELAY_WAIT_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2646. DDRSS_PHY_872 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_WRLVL_DLY_STEP_3	R/W	0h	DQS slave delay step size during write leveling for slice 3.
23-20	RESERVED	R/W	X	
19-16	PHY_RPTR_UPDATE_3	R/W	0h	Offset in cycles from the dfi_rddata_en signal to release data from the entry FIFO for slice 3.
15-8	PHY_MASTER_DELAY_HALF_MEASURE_3	R/W	0h	Defines the number of delay line elements to be considered in determining whether to lock to a half clock cycle in the data slice master for slice 3.
7-0	PHY_MASTER_DELAY_WAIT_3	R/W	0h	Wait cycles for master delay line locking algorithm for slice 3. Bits (3:0) are the cycle wait count after a calibration clock setting change. Bits (7:4) are the cycle wait count after a master delay setting change.

4.4.526 DDRSS_PHY_873 Register (Offset = 4DA4h) [reset = X]

DDRSS_PHY_873 is shown in Figure 4-1320 and described in Table 4-2648.

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Table 4-2647. DDRSS_PHY_873 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DA4h

Figure 4-1320. DDRSS_PHY_873 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_GTLVL_RESP_WAIT_CNT_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_DLY_STEP_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_WRLVL_RESP_WAIT_CNT_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_WRLVL_DLY_FINE_STEP_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2648. DDRSS_PHY_873 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_GTLVL_RESP_WAIT_CNT_3	R/W	0h	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate training for slice 3. The valid range is 0x0 to 0xB.
23-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_DLY_STEP_3	R/W	0h	DQS slave delay step size during gate training for slice 3.
15-14	RESERVED	R/W	X	
13-8	PHY_WRLVL_RESP_WAIT_CNT_3	R/W	0h	Number of cycles to wait between dfi_wrlvl_strobe and the sampling of the DQs during write leveling for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_WRLVL_DLY_FINE_STEP_3	R/W	0h	DQS slave delay fine step size during write leveling for slice 3.

4.4.527 DDRSS_PHY_874 Register (Offset = 4DA8h) [reset = X]

DDRSS_PHY_874 is shown in [Figure 4-1321](#) and described in [Table 4-2650](#).

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Table 4-2649. DDRSS_PHY_874 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DA8h

Figure 4-1321. DDRSS_PHY_874 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_GTLVL_FINAL_STEP_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_GTLVL_BACK_STEP_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2650. DDRSS_PHY_874 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_GTLVL_FINAL_STEP_3	R/W	0h	Final backup step delay used in gate training algorithm for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_BACK_STEP_3	R/W	0h	Interim backup step delay used in gate training algorithm for slice 3.

4.4.528 DDRSS_PHY_875 Register (Offset = 4DACH) [reset = X]

DDRSS_PHY_875 is shown in Figure 4-1322 and described in Table 4-2652.

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Table 4-2651. DDRSS_PHY_875 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DACH

Figure 4-1322. DDRSS_PHY_875 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_RDLVL_DLY_STEP_3			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							PHY_TOGGLE_PRE_SUPP RT_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PHY_WDQLVL_QTR_DLY_STEP_3			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_WDQLVL_DLY_STEP_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2652. DDRSS_PHY_875 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_RDLVL_DLY_STEP_3	R/W	0h	DQS slave delay step size during read leveling for slice 3.
23-17	RESERVED	R/W	X	
16	PHY_TOGGLE_PRE_SUPPORT_3	R/W	0h	Support the toggle read preamble for LPDDR4 for slice 3.
15-12	RESERVED	R/W	X	
11-8	PHY_WDQLVL_QTR_DLY_STEP_3	R/W	0h	Defines the step granularity for the logic to use once an edge is found for slice 3. When this occurs, the logic jumps back to the previous invalid value and uses this step size to determine a more accurate delay value.
7-0	PHY_WDQLVL_DLY_STEP_3	R/W	0h	DQ slave delay step size during write data leveling for slice 3.

4.4.529 DDRSS_PHY_876 Register (Offset = 4DB0h) [reset = X]

DDRSS_PHY_876 is shown in [Figure 4-1323](#) and described in [Table 4-2654](#).

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Table 4-2653. DDRSS_PHY_876 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DB0h

Figure 4-1323. DDRSS_PHY_876 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_RDLVL_MAX_EDGE_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2654. DDRSS_PHY_876 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_MAX_EDGE_3	R/W	0h	The maximum rdlvl slave delay search window for read eye training for slice 3.

4.4.530 DDRSS_PHY_877 Register (Offset = 4DB4h) [reset = X]

DDRSS_PHY_877 is shown in [Figure 4-1324](#) and described in [Table 4-2656](#).

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Table 4-2655. DDRSS_PHY_877 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DB4h

Figure 4-1324. DDRSS_PHY_877 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_RDLVL_PER_START_OFFSET_3					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED							PHY_SW_RDLVL_DVW_MIN_EN_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_DVW_MIN_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_DVW_MIN_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2656. DDRSS_PHY_877 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_RDLVL_PER_START_OFFSET_3	R/W	0h	Periodic training start point offset for slice 3.
23-17	RESERVED	R/W	X	
16	PHY_SW_RDLVL_DVW_MIN_EN_3	R/W	0h	SW override to enable use of PHY_RDLVL_DVW_MIN for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_DVW_MIN_3	R/W	0h	Minimum data valid window across DQs and ranks for slice 3.

4.4.531 DDRSS_PHY_878 Register (Offset = 4DB8h) [reset = X]

DDRSS_PHY_878 is shown in [Figure 4-1325](#) and described in [Table 4-2658](#).

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Table 4-2657. DDRSS_PHY_878 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DB8h

Figure 4-1325. DDRSS_PHY_878 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DATA_DC_INIT_DISABLE_3	
R/W-X						R/W-3h	
15	14	13	12	11	10	9	8
RESERVED					PHY_WRPATH_GATE_TIMING_3		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED						PHY_WRPATH_GATE_DISABLE_3	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2658. DDRSS_PHY_878 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DATA_DC_INIT_DISABLE_3	R/W	3h	Disable duty cycle adjust at initialization for slice 3.
15-11	RESERVED	R/W	X	
10-8	PHY_WRPATH_GATE_TIMING_3	R/W	0h	Write path clock gating timing for slice 3. it means additional clock number to write path clock gate
7-2	RESERVED	R/W	X	
1-0	PHY_WRPATH_GATE_DISABLE_3	R/W	0h	Write path clock gating disable for slice 3. [0]: disable pull in wrdata_en [1]: disable write path clock gating, clock always on

4.4.532 DDRSS_PHY_879 Register (Offset = 4DBCh) [reset = X]

DDRSS_PHY_879 is shown in [Figure 4-1326](#) and described in [Table 4-2660](#).

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Table 4-2659. DDRSS_PHY_879 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DBCh

Figure 4-1326. DDRSS_PHY_879 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_DATA_DC_DQ_INIT_SLV_DELAY_3		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ_INIT_SLV_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_DATA_DC_DQS_INIT_SLV_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_INIT_SLV_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2660. DDRSS_PHY_879 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_DATA_DC_DQ_INIT_SLV_DELAY_3	R/W	0h	Initial value of write DQ slave delay for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_DATA_DC_DQS_INIT_SLV_DELAY_3	R/W	0h	Initial value of write DQS slave delay for slice 3.

4.4.533 DDRSS_PHY_880 Register (Offset = 4DC0h) [reset = X]

DDRSS_PHY_880 is shown in [Figure 4-1327](#) and described in [Table 4-2662](#).

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Table 4-2661. DDRSS_PHY_880 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DC0h

Figure 4-1327. DDRSS_PHY_880 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_3							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DM_CLK_SE_THRSHLD_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_DATA_DC_WDQLVL_ENABLE_3
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_DATA_DC_WRLVL_ENABLE_3
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2662. DDRSS_PHY_880 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DM_CLK_DIFF_THRSHLD_3	R/W	0h	Clock measurement cell threshold offset for differential signals for slice 3.
23-16	PHY_DATA_DC_DM_CLK_SE_THRSHLD_3	R/W	0h	Clock measurement cell threshold offset for single ended signals for slice 3.
15-9	RESERVED	R/W	X	
8	PHY_DATA_DC_WDQLVL_ENABLE_3	R/W	0h	Enable duty cycle adjust during write DQ training for slice 3.
7-1	RESERVED	R/W	X	
0	PHY_DATA_DC_WRLVL_ENABLE_3	R/W	0h	Enable duty cycle adjust during write leveling for slice 3.

4.4.534 DDRSS_PHY_881 Register (Offset = 4DC4h) [reset = X]

DDRSS_PHY_881 is shown in [Figure 4-1328](#) and described in [Table 4-2664](#).

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Table 4-2663. DDRSS_PHY_881 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DC4h

Figure 4-1328. DDRSS_PHY_881 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_RDDATA_EN_DLY_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED			PHY_MEAS_DLY_STEP_ENABLE_3				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
RESERVED		PHY_WDQ_OSC_DELTA_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2664. DDRSS_PHY_881 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_RDDATA_EN_DLY_3	R/W	0h	Number of cycles that the dfi_rddata_en signal is early for slice 3.
15-14	RESERVED	R/W	X	
13-8	PHY_MEAS_DLY_STEP_ENABLE_3	R/W	0h	Data slice training step definition using phy_meas_dly_step_value for slice 3.
7	RESERVED	R/W	X	
6-0	PHY_WDQ_OSC_DELTA_3	R/W	0h	Slave delay offset that applies to a 1 bit change of dfi_wdq_osc_code for slice 3.

4.4.535 DDRSS_PHY_882 Register (Offset = 4DC8h) [reset = 0h]

DDRSS_PHY_882 is shown in [Figure 4-1329](#) and described in [Table 4-2666](#).

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Table 4-2665. DDRSS_PHY_882 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DC8h

Figure 4-1329. DDRSS_PHY_882 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DQ_DM_SWIZZLE0_3																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2666. DDRSS_PHY_882 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DQ_DM_SWIZZLE0_3	R/W	0h	DQ/DM bit swizzling 0 for slice 3. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0, Bits (7:4) inform the PHY which bit in {DM,DQ} map to DQ1, etc.

4.4.536 DDRSS_PHY_883 Register (Offset = 4DCCh) [reset = X]

DDRSS_PHY_883 is shown in [Figure 4-1330](#) and described in [Table 4-2668](#).

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Table 4-2667. DDRSS_PHY_883 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DCCh

Figure 4-1330. DDRSS_PHY_883 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PHY_DQ_DM_SWIZZLE1_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2668. DDRSS_PHY_883 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PHY_DQ_DM_SWIZZLE1_3	R/W	0h	DQ/DM bit swizzling 1 for slice 3. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DM.

4.4.537 DDRSS_PHY_884 Register (Offset = 4DD0h) [reset = X]

DDRSS_PHY_884 is shown in [Figure 4-1331](#) and described in [Table 4-2670](#).

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Table 4-2669. DDRSS_PHY_884 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DD0h

Figure 4-1331. DDRSS_PHY_884 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ1_SLAVE_DELAY_3										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ0_SLAVE_DELAY_3										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2670. DDRSS_PHY_884 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ1_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ1 for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ0_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ0 for slice 3.

4.4.538 DDRSS_PHY_885 Register (Offset = 4DD4h) [reset = X]

DDRSS_PHY_885 is shown in [Figure 4-1332](#) and described in [Table 4-2672](#).

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Table 4-2671. DDRSS_PHY_885 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DD4h

Figure 4-1332. DDRSS_PHY_885 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ3_SLAVE_DELAY_3										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ2_SLAVE_DELAY_3										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2672. DDRSS_PHY_885 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ3_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ3 for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ2_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ2 for slice 3.

4.4.539 DDRSS_PHY_886 Register (Offset = 4DD8h) [reset = X]

DDRSS_PHY_886 is shown in [Figure 4-1333](#) and described in [Table 4-2674](#).

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Table 4-2673. DDRSS_PHY_886 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DD8h

Figure 4-1333. DDRSS_PHY_886 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ5_SLAVE_DELAY_3										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ4_SLAVE_DELAY_3										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2674. DDRSS_PHY_886 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ5_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ5 for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ4_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ4 for slice 3.

4.4.540 DDRSS_PHY_887 Register (Offset = 4DDCh) [reset = X]

DDRSS_PHY_887 is shown in [Figure 4-1334](#) and described in [Table 4-2676](#).

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Table 4-2675. DDRSS_PHY_887 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DDCh

Figure 4-1334. DDRSS_PHY_887 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_CLK_WRDQ7_SLAVE_DELAY_3										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_WRDQ6_SLAVE_DELAY_3										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2676. DDRSS_PHY_887 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CLK_WRDQ7_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ7 for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDQ6_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQ6 for slice 3.

4.4.541 DDRSS_PHY_888 Register (Offset = 4DE0h) [reset = X]

DDRSS_PHY_888 is shown in [Figure 4-1335](#) and described in [Table 4-2678](#).

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Table 4-2677. DDRSS_PHY_888 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DE0h

Figure 4-1335. DDRSS_PHY_888 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						PHY_CLK_WRDQS_SLAVE_DELAY_3									
R/W-X						R/W-0h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_CLK_WRDM_SLAVE_DELAY_3									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2678. DDRSS_PHY_888 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_CLK_WRDQS_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DQS for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_CLK_WRDM_SLAVE_DELAY_3	R/W	0h	Write clock slave delay setting for DM for slice 3.

4.4.542 DDRSS_PHY_889 Register (Offset = 4DE4h) [reset = X]

DDRSS_PHY_889 is shown in [Figure 4-1336](#) and described in [Table 4-2680](#).

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Table 4-2679. DDRSS_PHY_889 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DE4h

Figure 4-1336. DDRSS_PHY_889 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_RDDQS_DQ0_RISE_SLAV E_DELAY_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_3							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_WRLVL_THRESHOLD_AD JUST_3	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2680. DDRSS_PHY_889 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-8	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ0 for slice 3.
7-2	RESERVED	R/W	X	
1-0	PHY_WRLVL_THRESHOLD_ADJUST_3	R/W	0h	Write level threshold adjust value based on those thresholds for DQS for slice 3.

4.4.543 DDRSS_PHY_890 Register (Offset = 4DE8h) [reset = X]

DDRSS_PHY_890 is shown in [Figure 4-1337](#) and described in [Table 4-2682](#).

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Table 4-2681. DDRSS_PHY_890 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DE8h

Figure 4-1337. DDRSS_PHY_890 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2682. DDRSS_PHY_890 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ1 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ0 for slice 3.

4.4.544 DDRSS_PHY_891 Register (Offset = 4DECh) [reset = X]

DDRSS_PHY_891 is shown in [Figure 4-1338](#) and described in [Table 4-2684](#).

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Table 4-2683. DDRSS_PHY_891 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DECh

Figure 4-1338. DDRSS_PHY_891 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2684. DDRSS_PHY_891 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ2 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ1 for slice 3.

4.4.545 DDRSS_PHY_892 Register (Offset = 4DF0h) [reset = X]

DDRSS_PHY_892 is shown in [Figure 4-1339](#) and described in [Table 4-2686](#).

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Table 4-2685. DDRSS_PHY_892 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DF0h

Figure 4-1339. DDRSS_PHY_892 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2686. DDRSS_PHY_892 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ3 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ2 for slice 3.

4.4.546 DDRSS_PHY_893 Register (Offset = 4DF4h) [reset = X]

DDRSS_PHY_893 is shown in [Figure 4-1340](#) and described in [Table 4-2688](#).

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Table 4-2687. DDRSS_PHY_893 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DF4h

Figure 4-1340. DDRSS_PHY_893 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2688. DDRSS_PHY_893 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ4 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ3 for slice 3.

4.4.547 DDRSS_PHY_894 Register (Offset = 4DF8h) [reset = X]

DDRSS_PHY_894 is shown in [Figure 4-1341](#) and described in [Table 4-2690](#).

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Table 4-2689. DDRSS_PHY_894 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DF8h

Figure 4-1341. DDRSS_PHY_894 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2690. DDRSS_PHY_894 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ5 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ4 for slice 3.

4.4.548 DDRSS_PHY_895 Register (Offset = 4DFCh) [reset = X]

DDRSS_PHY_895 is shown in [Figure 4-1342](#) and described in [Table 4-2692](#).

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Table 4-2691. DDRSS_PHY_895 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4DFCh

Figure 4-1342. DDRSS_PHY_895 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2692. DDRSS_PHY_895 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ6 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ5 for slice 3.

4.4.549 DDRSS_PHY_896 Register (Offset = 4E00h) [reset = X]

DDRSS_PHY_896 is shown in [Figure 4-1343](#) and described in [Table 4-2694](#).

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Table 4-2693. DDRSS_PHY_896 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E00h

Figure 4-1343. DDRSS_PHY_896 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2694. DDRSS_PHY_896 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DQ7 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ6 for slice 3.

4.4.550 DDRSS_PHY_897 Register (Offset = 4E04h) [reset = X]

DDRSS_PHY_897 is shown in Figure 4-1344 and described in Table 4-2696.

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Table 4-2695. DDRSS_PHY_897 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E04h

Figure 4-1344. DDRSS_PHY_897 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_DM_RISE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_DM_RISE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2696. DDRSS_PHY_897 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_DM_RISE_SLAVE_DELAY_3	R/W	0h	Rising edge read DQS slave delay setting for DM for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DQ7 for slice 3.

4.4.551 DDRSS_PHY_898 Register (Offset = 4E08h) [reset = X]

DDRSS_PHY_898 is shown in [Figure 4-1345](#) and described in [Table 4-2698](#).

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Table 4-2697. DDRSS_PHY_898 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E08h

Figure 4-1345. DDRSS_PHY_898 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_RDDQS_GATE_SLAVE_DELAY_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_RDDQS_GATE_SLAVE_DELAY_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDDQS_DM_FALL_SLAVE_DELAY_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDDQS_DM_FALL_SLAVE_DELAY_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2698. DDRSS_PHY_898 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_RDDQS_GATE_SLAVE_DELAY_3	R/W	0h	Read DQS slave delay setting for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_RDDQS_DM_FALL_SLAVE_DELAY_3	R/W	0h	Falling edge read DQS slave delay setting for DM for slice 3.

4.4.552 DDRSS_PHY_899 Register (Offset = 4E0Ch) [reset = X]

DDRSS_PHY_899 is shown in [Figure 4-1346](#) and described in [Table 4-2700](#).

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Table 4-2699. DDRSS_PHY_899 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E0Ch

Figure 4-1346. DDRSS_PHY_899 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_WRLVL_DELAY_EARLY_THRESHOLD_3	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_WRLVL_DELAY_EARLY_THRESHOLD_3							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_WRITE_PATH_LAT_ADD_3		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED				PHY_RDDQS_LATENCY_ADJUST_3			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2700. DDRSS_PHY_899 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_WRLVL_DELAY_EARLY_THRESHOLD_3	R/W	0h	Write level delay threshold above which will be considered in previous cycle for slice 3.
15-11	RESERVED	R/W	X	
10-8	PHY_WRITE_PATH_LAT_ADD_3	R/W	0h	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata signals for slice 3.
7-4	RESERVED	R/W	X	
3-0	PHY_RDDQS_LATENCY_ADJUST_3	R/W	0h	Number of cycles to delay the incoming dfi_rddata_en for read DQS gate generation for slice 3.

4.4.553 DDRSS_PHY_900 Register (Offset = 4E10h) [reset = X]

DDRSS_PHY_900 is shown in [Figure 4-1347](#) and described in [Table 4-2702](#).

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Table 4-2701. DDRSS_PHY_900 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E10h

Figure 4-1347. DDRSS_PHY_900 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_WRLVL_E ARLY_FORCE_ ZERO_3
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_WRLVL_DELAY_PERIOD_ THRESHOLD_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2702. DDRSS_PHY_900 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_WRLVL_EARLY_FORCE_ZERO_3	R/W	0h	Force the final write level delay value (that meets the early threshold) to 0 for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3	R/W	0h	Write level delay threshold below which will add a cycle of write path latency for slice 3.

4.4.554 DDRSS_PHY_901 Register (Offset = 4E14h) [reset = X]

DDRSS_PHY_901 is shown in [Figure 4-1348](#) and described in [Table 4-2704](#).

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Table 4-2703. DDRSS_PHY_901 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E14h

Figure 4-1348. DDRSS_PHY_901 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_GTLVL_LAT_ADJ_START_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_GTLVL_RDDQS_SLV_DLY_START_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_GTLVL_RDDQS_SLV_DLY_START_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2704. DDRSS_PHY_901 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_GTLVL_LAT_ADJ_START_3	R/W	0h	Initial read DQS gate cycle delay from dfi_rddata_en during gate training for slice 3.
15-10	RESERVED	R/W	X	
9-0	PHY_GTLVL_RDDQS_SLV_DLY_START_3	R/W	0h	Initial read DQS gate slave delay setting during gate training for slice 3.

4.4.555 DDRSS_PHY_902 Register (Offset = 4E18h) [reset = X]

DDRSS_PHY_902 is shown in Figure 4-1349 and described in Table 4-2706.

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Table 4-2705. DDRSS_PHY_902 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E18h

Figure 4-1349. DDRSS_PHY_902 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_NTP_PAS S_3
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_NTP_WRLAT_START_3			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_WDQLVL_DQDM_SLV_DLY_START_3		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_WDQLVL_DQDM_SLV_DLY_START_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2706. DDRSS_PHY_902 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_NTP_PASS_3	R/W	0h	Indicates if No-topology training found a passing result for slice 3.
23-20	RESERVED	R/W	X	
19-16	PHY_NTP_WRLAT_START_3	R/W	0h	Initial value for phy_write_path_lat_add for No-topology training and early threshold for slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_WDQLVL_DQDM_SLV_DLY_START_3	R/W	0h	Initial DQ/DM slave delay setting during write data leveling for slice 3.

4.4.556 DDRSS_PHY_903 Register (Offset = 4E1Ch) [reset = X]

DDRSS_PHY_903 is shown in [Figure 4-1350](#) and described in [Table 4-2708](#).

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Table 4-2707. DDRSS_PHY_903 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E1Ch

Figure 4-1350. DDRSS_PHY_903 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2708. DDRSS_PHY_903 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3	R/W	0h	Read leveling starting value for the DQS/DQ slave delay settings for slice 3.

4.4.557 DDRSS_PHY_904 Register (Offset = 4E20h) [reset = 20202020h]

DDRSS_PHY_904 is shown in [Figure 4-1351](#) and described in [Table 4-2710](#).

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Table 4-2709. DDRSS_PHY_904 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E20h

Figure 4-1351. DDRSS_PHY_904 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ2_CLK_ADJUST_3							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ1_CLK_ADJUST_3							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ0_CLK_ADJUST_3							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQS_CLK_ADJUST_3							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2710. DDRSS_PHY_904 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ2_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
23-16	PHY_DATA_DC_DQ1_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
15-8	PHY_DATA_DC_DQ0_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
7-0	PHY_DATA_DC_DQS_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.

4.4.558 DDRSS_PHY_905 Register (Offset = 4E24h) [reset = 20202020h]

DDRSS_PHY_905 is shown in [Figure 4-1352](#) and described in [Table 4-2712](#).

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Table 4-2711. DDRSS_PHY_905 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E24h

Figure 4-1352. DDRSS_PHY_905 Register

31	30	29	28	27	26	25	24
PHY_DATA_DC_DQ6_CLK_ADJUST_3							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_DATA_DC_DQ5_CLK_ADJUST_3							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DQ4_CLK_ADJUST_3							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ3_CLK_ADJUST_3							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2712. DDRSS_PHY_905 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_DATA_DC_DQ6_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
23-16	PHY_DATA_DC_DQ5_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
15-8	PHY_DATA_DC_DQ4_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
7-0	PHY_DATA_DC_DQ3_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.

4.4.559 DDRSS_PHY_906 Register (Offset = 4E28h) [reset = 2020h]

DDRSS_PHY_906 is shown in [Figure 4-1353](#) and described in [Table 4-2714](#).

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Table 4-2713. DDRSS_PHY_906 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E28h

Figure 4-1353. DDRSS_PHY_906 Register

31	30	29	28	27	26	25	24
PHY_DSLICE_PAD_BOOSTPN_SETTING_3							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_DSLICE_PAD_BOOSTPN_SETTING_3							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_DATA_DC_DM_CLK_ADJUST_3							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_DATA_DC_DQ7_CLK_ADJUST_3							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2714. DDRSS_PHY_906 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_DSLICE_PAD_BOOSTPN_SETTING_3	R/W	0h	Setting for boost P/N of pad for slice 3.
15-8	PHY_DATA_DC_DM_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.
7-0	PHY_DATA_DC_DQ7_CLK_ADJUST_3	R/W	20h	Adjust value of Duty Cycle Adjuster for slice 3.

4.4.560 DDRSS_PHY_907 Register (Offset = 4E2Ch) [reset = X]

DDRSS_PHY_907 is shown in Figure 4-1354 and described in Table 4-2716.

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Table 4-2715. DDRSS_PHY_907 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 4E2Ch

Figure 4-1354. DDRSS_PHY_907 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						PHY_DQS_FFE_3	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_DQ_FFE_3	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		PHY_DSLICE_PAD_RX_CTL_SETTING_3					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2716. DDRSS_PHY_907 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	PHY_DQS_FFE_3	R/W	0h	TX_FFE setting for DQS pad for slice 3.
15-10	RESERVED	R/W	X	
9-8	PHY_DQ_FFE_3	R/W	0h	TX_FFE setting for DQ/DM pad for slice 3.
7-6	RESERVED	R/W	X	
5-0	PHY_DSLICE_PAD_RX_CTL_SETTING_3	R/W	0h	Setting for RX ctle P/N of pad for slice 3.

4.4.561 DDRSS_PHY_1024 Register (Offset = 5000h) [reset = X]

DDRSS_PHY_1024 is shown in Figure 4-1355 and described in Table 4-2718.

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Table 4-2717. DDRSS_PHY_1024 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5000h

Figure 4-1355. DDRSS_PHY_1024 Register

31	30	29	28	27	26	25	24
RESERVED					SC_PHY_ADR_MANUAL_CLEAR_0		
R/W-X					W-0h		
23	22	21	20	19	18	17	16
RESERVED							PHY_ADR_CLK_BYPASS_OVERRIDE_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2718. DDRSS_PHY_1024 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	SC_PHY_ADR_MANUAL_CLEAR_0	W	0h	Manual reset/clear of internal logic for address slice 0. Bit (0) is reset of master delay min/max lock values. Bit (1) is manual reset of master delay unlock counter. Bit (2) clears the loopback error/results registers. Set each bit to 1 to reset. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PHY_ADR_CLK_BYPASS_OVERRIDE_0	R/W	0h	Bypass mode override setting for address slice 0. Set to 1 to enable.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0	R/W	0h	Command/Address clock bypass mode slave delay setting for address slice 0.

4.4.562 DDRSS_PHY_1025 Register (Offset = 5004h) [reset = 1000h]

DDRSS_PHY_1025 is shown in [Figure 4-1356](#) and described in [Table 4-2720](#).

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Table 4-2719. DDRSS_PHY_1025 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5004h

Figure 4-1356. DDRSS_PHY_1025 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_LPBK_RESULT_OBS_0																															
R-1000h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2720. DDRSS_PHY_1025 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_LPBK_RESULT_OBS_0	R	1000h	Observation register containing loopback status/results for address slice 0. READ-ONLY

4.4.563 DDRSS_PHY_1026 Register (Offset = 5008h) [reset = X]

DDRSS_PHY_1026 is shown in [Figure 4-1357](#) and described in [Table 4-2722](#).

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Table 4-2721. DDRSS_PHY_1026 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5008h

Figure 4-1357. DDRSS_PHY_1026 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PHY_ADR_MEAS_DLY_STEP_VALUE_0							
R-0h							
15	14	13	12	11	10	9	8
PHY_ADR_LPBK_ERROR_COUNT_OBS_0							
R-0h							
7	6	5	4	3	2	1	0
PHY_ADR_LPBK_ERROR_COUNT_OBS_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2722. DDRSS_PHY_1026 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0	R/W	0h	Select value to map the internal master delay observation registers to the accessible master delay observation register for address slice 0.
23-16	PHY_ADR_MEAS_DLY_STEP_VALUE_0	R	0h	Contains the fraction of a cycle in 1 delay element numerator with demominator of 512, for address slice 0. READ-ONLY
15-0	PHY_ADR_LPBK_ERROR_COUNT_OBS_0	R	0h	Observation register containing total number of loopback error data for address slice 0. READ-ONLY

4.4.564 DDRSS_PHY_1027 Register (Offset = 500Ch) [reset = X]

DDRSS_PHY_1027 is shown in Figure 4-1358 and described in Table 4-2724.

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Table 4-2723. DDRSS_PHY_1027 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 500Ch

Figure 4-1358. DDRSS_PHY_1027 Register

31	30	29	28	27	26	25	24
PHY_ADR_ADDER_SLV_DLY_ENC_OBS_0							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	PHY_ADR_BASE_SLV_DLY_ENC_OBS_0						
R-X	R-0h						
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DLY_LOCK_OBS_0		
R-X					R-0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DLY_LOCK_OBS_0							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-2724. DDRSS_PHY_1027 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_ADR_ADDER_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing addr slave delay for address slice 0. READ-ONLY
23	RESERVED	R	X	
22-16	PHY_ADR_BASE_SLV_DLY_ENC_OBS_0	R	0h	Observation register containing base slave delay for address slice 0. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_ADR_MASTER_DLY_LOCK_OBS_0	R	0h	Observation register containing master delay results for address slice 0. READ-ONLY

4.4.565 DDRSS_PHY_1028 Register (Offset = 5010h) [reset = X]

DDRSS_PHY_1028 is shown in [Figure 4-1359](#) and described in [Table 4-2726](#).

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Table 4-2725. DDRSS_PHY_1028 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5010h

Figure 4-1359. DDRSS_PHY_1028 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_TSEL_ENABLE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_SNAP_OBS_REGS_0
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED					PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2726. DDRSS_PHY_1028 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADR_TSEL_ENABLER_0	R/W	0h	Enables tsel_en for address slice 0.
23-17	RESERVED	R/W	X	
16	SC_PHY_ADR_SNAP_OBS_REGS_0	W	0h	Initiates a snapshot of the internal observation registers for address slice 0. Set to 1 to trigger. WRITE-ONLY
15-11	RESERVED	R/W	X	
10-8	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0	R/W	0h	Select value to map the addr bits delay observation registers to the accessible delay observation register for address slice 0.
7-3	RESERVED	R/W	X	
2-0	PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0	R/W	0h	Reserved for address slice 0.

4.4.566 DDRSS_PHY_1029 Register (Offset = 5014h) [reset = X]

DDRSS_PHY_1029 is shown in Figure 4-1360 and described in Table 4-2728.

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Table 4-2727. DDRSS_PHY_1029 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5014h

Figure 4-1360. DDRSS_PHY_1029 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_PW R_RDC_DISAB LE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED			PHY_ADR_PRBS_PATTERN_MASK_0				
R/W-X			R/W-0h				
15	14	13	12	11	10	9	8
RESERVED	PHY_ADR_PRBS_PATTERN_START_0						
R/W-X	R/W-1h						
7	6	5	4	3	2	1	0
RESERVED	PHY_ADR_LPBK_CONTROL_0						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2728. DDRSS_PHY_1029 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADR_PWR_RDC_DISABLE_0	R/W	0h	Power reduction disable for address slice 0.
23-21	RESERVED	R/W	X	
20-16	PHY_ADR_PRBS_PATTERN_MASK_0	R/W	0h	PRBS7 mask signal for address slice 0.
15	RESERVED	R/W	X	
14-8	PHY_ADR_PRBS_PATTERN_START_0	R/W	1h	PRBS7 start pattern for address slice 0.
7	RESERVED	R/W	X	
6-0	PHY_ADR_LPBK_CONTROL_0	R/W	0h	Loopback control bits for address slice 0.

4.4.567 DDRSS_PHY_1030 Register (Offset = 5018h) [reset = X]

DDRSS_PHY_1030 is shown in [Figure 4-1361](#) and described in [Table 4-2730](#).

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Table 4-2729. DDRSS_PHY_1030 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5018h

Figure 4-1361. DDRSS_PHY_1030 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_IE_MODE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED					PHY_ADR_WRADDR_SHIFT_OBS_0		
R/W-X					R-0h		
15	14	13	12	11	10	9	8
RESERVED						PHY_ADR_TYPE_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_0
R/W-X							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2730. DDRSS_PHY_1030 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADR_IE_MODE_0	R/W	0h	Input enable control for address slice 0.
23-19	RESERVED	R/W	X	
18-16	PHY_ADR_WRADDR_SHIFT_OBS_0	R	0h	Observation register containing automatic half cycle and cycle shift values for address slice 0. READ-ONLY
15-10	RESERVED	R/W	X	
9-8	PHY_ADR_TYPE_0	R/W	0h	DRAM type for address slice 0.
7-1	RESERVED	R/W	X	
0	PHY_ADR_SLV_DLY_CTRL_GATE_DISABLE_0	R/W	0h	Power reduction slv_dly_control block gate disable for address slice 0.

4.4.568 DDRSS_PHY_1031 Register (Offset = 501Ch) [reset = X]

DDRSS_PHY_1031 is shown in [Figure 4-1362](#) and described in [Table 4-2732](#).

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Table 4-2731. DDRSS_PHY_1031 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 501Ch

Figure 4-1362. DDRSS_PHY_1031 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_ADR_DDL_MODE_0																									
R/W-X						R/W-0h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2732. DDRSS_PHY_1031 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	PHY_ADR_DDL_MODE_0	R/W	0h	DDL mode for address slice 0.

4.4.569 DDRSS_PHY_1032 Register (Offset = 5020h) [reset = X]

DDRSS_PHY_1032 is shown in [Figure 4-1363](#) and described in [Table 4-2734](#).

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Table 4-2733. DDRSS_PHY_1032 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5020h

Figure 4-1363. DDRSS_PHY_1032 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										PHY_ADR_DDL_MASK_0					
R/W-X										R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2734. DDRSS_PHY_1032 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5-0	PHY_ADR_DDL_MASK_0	R/W	0h	DDL mask for address slice 0.

4.4.570 DDRSS_PHY_1033 Register (Offset = 5024h) [reset = 0h]

DDRSS_PHY_1033 is shown in [Figure 4-1364](#) and described in [Table 4-2736](#).

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Table 4-2735. DDRSS_PHY_1033 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5024h

Figure 4-1364. DDRSS_PHY_1033 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2736. DDRSS_PHY_1033 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_DDL_TEST_OBS_0	R	0h	Observation register containing DDL test bits for address slice 0. READ-ONLY

4.4.571 DDRSS_PHY_1034 Register (Offset = 5028h) [reset = 0h]

DDRSS_PHY_1034 is shown in [Figure 4-1365](#) and described in [Table 4-2738](#).

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Table 4-2737. DDRSS_PHY_1034 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5028h

Figure 4-1365. DDRSS_PHY_1034 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2738. DDRSS_PHY_1034 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0	R	0h	Observation register containing master DDL bits for address slice 0. READ-ONLY

4.4.572 DDRSS_PHY_1035 Register (Offset = 502Ch) [reset = X]

DDRSS_PHY_1035 is shown in [Figure 4-1366](#) and described in [Table 4-2740](#).

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Table 4-2739. DDRSS_PHY_1035 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 502Ch

Figure 4-1366. DDRSS_PHY_1035 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_ADR_CALVL_COARSE_DLY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_ADR_CALVL_START_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2740. DDRSS_PHY_1035 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_ADR_CALVL_COARSE_DLY_0	R/W	0h	Coarse CA training DDL increment value for address slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR_CALVL_START_0	R/W	0h	CA training DDL start value for address slice 0.

4.4.573 DDRSS_PHY_1036 Register (Offset = 5030h) [reset = X]

DDRSS_PHY_1036 is shown in [Figure 4-1367](#) and described in [Table 4-2742](#).

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Table 4-2741. DDRSS_PHY_1036 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5030h

Figure 4-1367. DDRSS_PHY_1036 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_ADR_CALVL_QTR_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2742. DDRSS_PHY_1036 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	PHY_ADR_CALVL_QTR_0	R/W	0h	CA training DDL quarter cycle delay value for address slice 0.

4.4.574 DDRSS_PHY_1037 Register (Offset = 5034h) [reset = X]

DDRSS_PHY_1037 is shown in [Figure 4-1368](#) and described in [Table 4-2744](#).

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Table 4-2743. DDRSS_PHY_1037 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5034h

Figure 4-1368. DDRSS_PHY_1037 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_ADR_CALVL_SWIZZLE0_0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2744. DDRSS_PHY_1037 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PHY_ADR_CALVL_SWIZZLE0_0	R/W	0h	CA training RD DQ bit swizzle map 0 for address slice 0.

4.4.575 DDRSS_PHY_1038 Register (Offset = 5038h) [reset = X]

DDRSS_PHY_1038 is shown in [Figure 4-1369](#) and described in [Table 4-2746](#).

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Table 4-2745. DDRSS_PHY_1038 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5038h

Figure 4-1369. DDRSS_PHY_1038 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_CALVL_RANK_CTRL_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_SWIZZLE1_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_ADR_CALVL_SWIZZLE1_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_ADR_CALVL_SWIZZLE1_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2746. DDRSS_PHY_1038 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_ADR_CALVL_RANK_CTRL_0	R/W	0h	CA training rank aggregation control bits for address slice 0.
23-0	PHY_ADR_CALVL_SWIZZLE1_0	R/W	0h	CA training RD DQ bit swizzle map 1 for address slice 0.

4.4.576 DDRSS_PHY_1039 Register (Offset = 503Ch) [reset = X]

DDRSS_PHY_1039 is shown in [Figure 4-1370](#) and described in [Table 4-2748](#).

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Table 4-2747. DDRSS_PHY_1039 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 503Ch

Figure 4-1370. DDRSS_PHY_1039 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_CALVL_PERIODIC_START_OFFSET_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_ADR_CALVL_PERIODIC_START_OFFSET_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				PHY_ADR_CALVL_RESP_WAIT_CNT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED						PHY_ADR_CALVL_NUM_PATTERNS_0	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2748. DDRSS_PHY_1039 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_ADR_CALVL_PERIODIC_START_OFFSET_0	R/W	0h	Relative offset to start periodic CALVL from previous result
15-12	RESERVED	R/W	X	
11-8	PHY_ADR_CALVL_RESP_WAIT_CNT_0	R/W	0h	Number of samples to wait before sampling response during CA training for address slice 0.
7-2	RESERVED	R/W	X	
1-0	PHY_ADR_CALVL_NUM_PATTERNS_0	R/W	0h	Number of patterns to use during CA training for address slice 0.

4.4.577 DDRSS_PHY_1040 Register (Offset = 5040h) [reset = X]

DDRSS_PHY_1040 is shown in Figure 4-1371 and described in Table 4-2750.

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Table 4-2749. DDRSS_PHY_1040 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5040h

Figure 4-1371. DDRSS_PHY_1040 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ADR_CALVL_OBS_SELECT_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							SC_PHY_ADR_CALVL_ERROR_CLR_0
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_ADR_CALVL_DEBUG_CONT_0
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_CALVL_DEBUG_MODE_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2750. DDRSS_PHY_1040 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_ADR_CALVL_OBS_SELECT_0	R/W	0h	CA bit lane to observe result from OBS0 during CA training for address slice 0.
23-17	RESERVED	R/W	X	
16	SC_PHY_ADR_CALVL_ERROR_CLR_0	W	0h	Clears the CA training state machine error status for address slice 0. Set to 1 to trigger. WRITE-ONLY
15-9	RESERVED	R/W	X	
8	SC_PHY_ADR_CALVL_DEBUG_CONT_0	W	0h	Allows the CA training state machine to advance (when in debug mode) for address slice 0. Set to 1 to trigger. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_ADR_CALVL_DEBUG_MODE_0	R/W	0h	Enables CA training debug mode for address slice 0. Set to 1 to enable.

4.4.578 DDRSS_PHY_1041 Register (Offset = 5044h) [reset = 0h]

DDRSS_PHY_1041 is shown in [Figure 4-1372](#) and described in [Table 4-2752](#).

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Table 4-2751. DDRSS_PHY_1041 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5044h

Figure 4-1372. DDRSS_PHY_1041 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_CALVL_CH0_OBS0_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2752. DDRSS_PHY_1041 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_CALVL_CH0_OBS0_0	R	0h	Observation register for CA training for channel 0 slice 0. READ-ONLY

4.4.579 DDRSS_PHY_1042 Register (Offset = 5048h) [reset = 0h]

DDRSS_PHY_1042 is shown in [Figure 4-1373](#) and described in [Table 4-2754](#).

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Table 4-2753. DDRSS_PHY_1042 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5048h

Figure 4-1373. DDRSS_PHY_1042 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_CALVL_CH1_OBS0_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2754. DDRSS_PHY_1042 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_CALVL_CH1_OBS0_0	R	0h	Observation register for CA training for channel 1 slice 0. READ-ONLY

4.4.580 DDRSS_PHY_1043 Register (Offset = 504Ch) [reset = 0h]

DDRSS_PHY_1043 is shown in [Figure 4-1374](#) and described in [Table 4-2756](#).

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Table 4-2755. DDRSS_PHY_1043 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 504Ch

Figure 4-1374. DDRSS_PHY_1043 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS1_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2756. DDRSS_PHY_1043 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_CALVL_OBS1_0	R	0h	Observation register contains general CA training bits for slice 0. READ-ONLY

4.4.581 DDRSS_PHY_1044 Register (Offset = 5050h) [reset = 0h]

DDRSS_PHY_1044 is shown in [Figure 4-1375](#) and described in [Table 4-2758](#).

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Table 4-2757. DDRSS_PHY_1044 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5050h

Figure 4-1375. DDRSS_PHY_1044 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ADR_CALVL_OBS2_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2758. DDRSS_PHY_1044 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_ADR_CALVL_OBS2_0	R	0h	Observation register contains periodic CA training bits for slice 0. READ-ONLY

4.4.582 DDRSS_PHY_1045 Register (Offset = 5054h) [reset = X]

DDRSS_PHY_1045 is shown in [Figure 4-1376](#) and described in [Table 4-2760](#).

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Table 4-2759. DDRSS_PHY_1045 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5054h

Figure 4-1376. DDRSS_PHY_1045 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_FG_0_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2760. DDRSS_PHY_1045 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_FG_0_0	R/W	0h	CA training foreground pattern 0 for address slice 0.

4.4.583 DDRSS_PHY_1046 Register (Offset = 5058h) [reset = X]

DDRSS_PHY_1046 is shown in [Figure 4-1377](#) and described in [Table 4-2762](#).

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Table 4-2761. DDRSS_PHY_1046 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5058h

Figure 4-1377. DDRSS_PHY_1046 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_BG_0_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2762. DDRSS_PHY_1046 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_BG_0_0	R/W	0h	CA training background pattern 0 for address slice 0.

4.4.584 DDRSS_PHY_1047 Register (Offset = 505Ch) [reset = X]

DDRSS_PHY_1047 is shown in [Figure 4-1378](#) and described in [Table 4-2764](#).

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Table 4-2763. DDRSS_PHY_1047 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 505Ch

Figure 4-1378. DDRSS_PHY_1047 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_FG_1_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2764. DDRSS_PHY_1047 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_FG_1_0	R/W	0h	CA training foreground pattern 1 for address slice 0.

4.4.585 DDRSS_PHY_1048 Register (Offset = 5060h) [reset = X]

DDRSS_PHY_1048 is shown in [Figure 4-1379](#) and described in [Table 4-2766](#).

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Table 4-2765. DDRSS_PHY_1048 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5060h

Figure 4-1379. DDRSS_PHY_1048 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_BG_1_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2766. DDRSS_PHY_1048 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_BG_1_0	R/W	0h	CA training background pattern 1 for address slice 0.

4.4.586 DDRSS_PHY_1049 Register (Offset = 5064h) [reset = X]

DDRSS_PHY_1049 is shown in [Figure 4-1380](#) and described in [Table 4-2768](#).

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Table 4-2767. DDRSS_PHY_1049 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5064h

Figure 4-1380. DDRSS_PHY_1049 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_FG_2_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2768. DDRSS_PHY_1049 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_FG_2_0	R/W	0h	CA training foreground pattern 2 for address slice 0.

4.4.587 DDRSS_PHY_1050 Register (Offset = 5068h) [reset = X]

DDRSS_PHY_1050 is shown in [Figure 4-1381](#) and described in [Table 4-2770](#).

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Table 4-2769. DDRSS_PHY_1050 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5068h

Figure 4-1381. DDRSS_PHY_1050 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_BG_2_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2770. DDRSS_PHY_1050 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_BG_2_0	R/W	0h	CA training background pattern 2 for address slice 0.

4.4.588 DDRSS_PHY_1051 Register (Offset = 506Ch) [reset = X]

DDRSS_PHY_1051 is shown in [Figure 4-1382](#) and described in [Table 4-2772](#).

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Table 4-2771. DDRSS_PHY_1051 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 506Ch

Figure 4-1382. DDRSS_PHY_1051 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_FG_3_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2772. DDRSS_PHY_1051 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_FG_3_0	R/W	0h	CA training foreground pattern 3 for address slice 0.

4.4.589 DDRSS_PHY_1052 Register (Offset = 5070h) [reset = X]

DDRSS_PHY_1052 is shown in [Figure 4-1383](#) and described in [Table 4-2774](#).

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Table 4-2773. DDRSS_PHY_1052 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5070h

Figure 4-1383. DDRSS_PHY_1052 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												PHY_ADR_CALVL_BG_3_0																			
R/W-X												R/W-0h																			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2774. DDRSS_PHY_1052 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_ADR_CALVL_BG_3_0	R/W	0h	CA training background pattern 3 for address slice 0.

4.4.590 DDRSS_PHY_1053 Register (Offset = 5074h) [reset = X]

DDRSS_PHY_1053 is shown in [Figure 4-1384](#) and described in [Table 4-2776](#).

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Table 4-2775. DDRSS_PHY_1053 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5074h

Figure 4-1384. DDRSS_PHY_1053 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_ADR_ADDR_SEL_0																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2776. DDRSS_PHY_1053 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	PHY_ADR_ADDR_SEL_0	R/W	0h	Selects which DFI address pins connect to which CA pins for LPDDR3/4 for address slice 0.

4.4.591 DDRSS_PHY_1054 Register (Offset = 5078h) [reset = X]

DDRSS_PHY_1054 is shown in Figure 4-1385 and described in Table 4-2778.

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Table 4-2777. DDRSS_PHY_1054 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5078h

Figure 4-1385. DDRSS_PHY_1054 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADR_SEG_MASK_0					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_BIT_MASK_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED						PHY_ADR_LP4_BOOT_SLV_DELAY_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_ADR_LP4_BOOT_SLV_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2778. DDRSS_PHY_1054 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_ADR_SEG_MASK_0	R/W	0h	Segment mask bit for address slice 0. Set to 1 to indicate that the bit is either CA 4 or CA 9.
23-22	RESERVED	R/W	X	
21-16	PHY_ADR_BIT_MASK_0	R/W	0h	Mask bit for address slice 0. Set to 1 to indicate that the bit is used.
15-10	RESERVED	R/W	X	
9-0	PHY_ADR_LP4_BOOT_SLV_DELAY_0	R/W	0h	Address slave delay setting during the LPDDR4 boot frequency operation for address slice 0.

4.4.592 DDRSS_PHY_1055 Register (Offset = 507Ch) [reset = X]

DDRSS_PHY_1055 is shown in [Figure 4-1386](#) and described in [Table 4-2780](#).

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Table 4-2779. DDRSS_PHY_1055 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 507Ch

Figure 4-1386. DDRSS_PHY_1055 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_SW_TXIO_CTRL_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_STATIC_TOG_DISABLE_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_ADR_CSLVL_TRAIN_MASK_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_TRAIN_MASK_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2780. DDRSS_PHY_1055 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_ADR_SW_TXIO_CTRL_0	R/W	0h	Controls address pad output enable for address slice 0. Set to 1 to disable output enable.
23-20	RESERVED	R/W	X	
19-16	PHY_ADR_STATIC_TOG_DISABLE_0	R/W	0h	Toggle control during static activity for address slice 0. Set bit to disable toggling, bit 0: Write path delay line, bit 1: Read path delay line, bit 2: Read data path, bit 3: clk_phy, bit 4: master delay line.
15-14	RESERVED	R/W	X	
13-8	PHY_ADR_CSLVL_TRAIN_MASK_0	R/W	0h	Mask bit for CS training participation for address slice 0. Set to 1 to indicate that the bit is participating in CS training.
7-6	RESERVED	R/W	X	
5-0	PHY_ADR_CALVL_TRAIN_MASK_0	R/W	0h	Mask bit for CA training participation for address slice 0. Set to 1 to indicate that the bit is participating in CA training.

4.4.593 DDRSS_PHY_1056 Register (Offset = 5080h) [reset = X]

DDRSS_PHY_1056 is shown in [Figure 4-1387](#) and described in [Table 4-2782](#).

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Table 4-2781. DDRSS_PHY_1056 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5080h

Figure 4-1387. DDRSS_PHY_1056 Register

31	30	29	28	27	26	25	24
PHY_ADR_DC_ADR2_CLK_ADJUST_0							
R/W-20h							
23	22	21	20	19	18	17	16
PHY_ADR_DC_ADR1_CLK_ADJUST_0							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_ADR_DC_ADR0_CLK_ADJUST_0							
R/W-20h							
7	6	5	4	3	2	1	0
RESERVED						PHY_ADR_DC_INIT_DISABLE_0	
R/W-X						R/W-3h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2782. DDRSS_PHY_1056 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_ADR_DC_ADR2_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 2 for address slice 0.
23-16	PHY_ADR_DC_ADR1_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 1 for address slice 0.
15-8	PHY_ADR_DC_ADR0_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 0 for address slice 0.
7-2	RESERVED	R/W	X	
1-0	PHY_ADR_DC_INIT_DISABLE_0	R/W	3h	Duty Cycle Corrector disable at initialization for address slice 0. Set to 1 to disable, bit (1) controls data path, bit (0) controls clock path.

4.4.594 DDRSS_PHY_1057 Register (Offset = 5084h) [reset = X]

DDRSS_PHY_1057 is shown in [Figure 4-1388](#) and described in [Table 4-2784](#).

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Table 4-2783. DDRSS_PHY_1057 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5084h

Figure 4-1388. DDRSS_PHY_1057 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DC C_RXCAL_CTRL_GATE_DISABLE_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_ADR_DC_ADR5_CLK_ADJUST_0							
R/W-20h							
15	14	13	12	11	10	9	8
PHY_ADR_DC_ADR4_CLK_ADJUST_0							
R/W-20h							
7	6	5	4	3	2	1	0
PHY_ADR_DC_ADR3_CLK_ADJUST_0							
R/W-20h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2784. DDRSS_PHY_1057 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADR_DCC_RXCAL_CTRL_GATE_DISABLE_0	R/W	0h	DCC and RX_CAL clk gate disable for address slice 0. 1 = disable clk gate.
23-16	PHY_ADR_DC_ADR5_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 5 for address slice 0.
15-8	PHY_ADR_DC_ADR4_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 4 for address slice 0.
7-0	PHY_ADR_DC_ADR3_CLK_ADJUST_0	R/W	20h	Adjust value of Clock Duty Cycle Adjuster lane 3 for address slice 0.

4.4.595 DDRSS_PHY_1058 Register (Offset = 5088h) [reset = X]

DDRSS_PHY_1058 is shown in Figure 4-1389 and described in Table 4-2786.

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Table 4-2785. DDRSS_PHY_1058 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5088h

Figure 4-1389. DDRSS_PHY_1058 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR_DC_ADJUST_START_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_ADR_DC_WEIGHT_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_ADR_DC_CAL_TIMEOUT_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_ADR_DC_CAL_SAMPLE_WAIT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2786. DDRSS_PHY_1058 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_ADR_DC_ADJUST_START_0	R/W	0h	DCC calibration starting value for address slice 0.
23-18	RESERVED	R/W	X	
17-16	PHY_ADR_DC_WEIGHT_0	R/W	0h	DCC weighting factor base value for address slice 0.
15-8	PHY_ADR_DC_CAL_TIMEOUT_0	R/W	0h	DCC number of iterations to wait before timeout for address slice 0.
7-0	PHY_ADR_DC_CAL_SAMPLE_WAIT_0	R/W	0h	DCC cycles to wait after calibration change before sampling results for address slice 0.

4.4.596 DDRSS_PHY_1059 Register (Offset = 508Ch) [reset = X]

DDRSS_PHY_1059 is shown in [Figure 4-1390](#) and described in [Table 4-2788](#).

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Table 4-2787. DDRSS_PHY_1059 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 508Ch

Figure 4-1390. DDRSS_PHY_1059 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_DC_CAL_POLARITY_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_ADR_DC_ADJUST_DIRECT_0
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_ADR_DC_ADJUST_THRSHLD_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_ADR_DC_ADJUST_SAMPLE_CNT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2788. DDRSS_PHY_1059 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADR_DC_CAL_POLARITY_0	R/W	0h	DCC calibration polarity for address slice 0.
23-17	RESERVED	R/W	X	
16	PHY_ADR_DC_ADJUST_DIRECT_0	R/W	0h	DCC adjust direction for address slice 0.
15-8	PHY_ADR_DC_ADJUST_THRSHLD_0	R/W	0h	DCC adjust threshold around the mid-point for address slice 0.
7-0	PHY_ADR_DC_ADJUST_SAMPLE_CNT_0	R/W	0h	DCC number of samples to take for address slice 0.

4.4.597 DDRSS_PHY_1060 Register (Offset = 5090h) [reset = X]

DDRSS_PHY_1060 is shown in [Figure 4-1391](#) and described in [Table 4-2790](#).

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Table 4-2789. DDRSS_PHY_1060 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5090h

Figure 4-1391. DDRSS_PHY_1060 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PARITY_ERROR_REGIF_ADR_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_PARITY_ERROR_REGIF_ADR_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_ADR_SW_TXPWR_CTRL_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CAL_START_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2790. DDRSS_PHY_1060 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PARITY_ERROR_REGIF_ADR_0	R/W	0h	Inject parity error to register interface signals for address slice 0.
15-14	RESERVED	R/W	X	
13-8	PHY_ADR_SW_TXPWR_CTRL_0	R/W	0h	Disable address output enables in deep sleep mode for address slice 0.
7-1	RESERVED	R/W	X	
0	PHY_ADR_DC_CAL_START_0	R/W	0h	DCC Manual trigger for address slice 0.

4.4.598 DDRSS_PHY_1061 Register (Offset = 5094h) [reset = X]

DDRSS_PHY_1061 is shown in [Figure 4-1392](#) and described in [Table 4-2792](#).

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Table 4-2791. DDRSS_PHY_1061 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5094h

Figure 4-1392. DDRSS_PHY_1061 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_AS_FSM_ERROR_INFO_MASK_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_AS_FSM_ERROR_INFO_MASK_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_AS_FSM_ERROR_INFO_0
R/W-X							R-0h
7	6	5	4	3	2	1	0
PHY_AS_FSM_ERROR_INFO_0							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2792. DDRSS_PHY_1061 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	PHY_AS_FSM_ERROR_INFO_MASK_0	R/W	0h	FSM Error Info Mask for address slice 0.
15-9	RESERVED	R/W	X	
8-0	PHY_AS_FSM_ERROR_INFO_0	R	0h	FSM Error Info for address slice 0. READ-ONLY

4.4.599 DDRSS_PHY_1062 Register (Offset = 5098h) [reset = X]

DDRSS_PHY_1062 is shown in [Figure 4-1393](#) and described in [Table 4-2794](#).

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Table 4-2793. DDRSS_PHY_1062 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5098h

Figure 4-1393. DDRSS_PHY_1062 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_AS_TRAIN_CALIB_ERROR_INFO_MASK_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_AS_TRAIN_CALIB_ERROR_INFO_0
R/W-X							R-0h
15	14	13	12	11	10	9	8
RESERVED							SC_PHY_AS_FSM_ERROR_INFO_WOCLR_0
R/W-X							W-0h
7	6	5	4	3	2	1	0
SC_PHY_AS_FSM_ERROR_INFO_WOCLR_0							
W-0h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2794. DDRSS_PHY_1062 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_AS_TRAIN_CALIB_ERROR_INFO_MASK_0	R/W	0h	Training/Calibration Error Info Mask for address slice 0.
23-17	RESERVED	R/W	X	
16	PHY_AS_TRAIN_CALIB_ERROR_INFO_0	R	0h	Training/Calibration Error Info for address slice 0. READ-ONLY
15-9	RESERVED	R/W	X	
8-0	SC_PHY_AS_FSM_ERROR_INFO_WOCLR_0	W	0h	FSM Error Info clear for address slice 0. WRITE-ONLY

4.4.600 DDRSS_PHY_1063 Register (Offset = 509Ch) [reset = X]

DDRSS_PHY_1063 is shown in [Figure 4-1394](#) and described in [Table 4-2796](#).

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Table 4-2795. DDRSS_PHY_1063 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 509Ch

Figure 4-1394. DDRSS_PHY_1063 Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_AS_T RAIN_CALIB_E RROR_INFO_ WOCLR_0
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-2796. DDRSS_PHY_1063 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	SC_PHY_AS_TRAIN_CALIB_ERROR_INFO_WOCLR_0	W	0h	Training/Calibration Error Info clear for address slice 0. WRITE-ONLY

4.4.601 DDRSS_PHY_1064 Register (Offset = 50A0h) [reset = X]

DDRSS_PHY_1064 is shown in Figure 4-1395 and described in Table 4-2798.

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Table 4-2797. DDRSS_PHY_1064 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50A0h

Figure 4-1395. DDRSS_PHY_1064 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PAD_ADR_IO_CFG_0		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_PAD_ADR_IO_CFG_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_DC_CAL_CLK_SEL_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR_TSEL_SELECT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2798. DDRSS_PHY_1064 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PAD_ADR_IO_CFG_0	R/W	0h	Controls I/O pads for address pad for address slice 0. Bits (10:5) = Park value, bits (4) park override, bits (2:0) clk divider.
15-11	RESERVED	R/W	X	
10-8	PHY_ADR_DC_CAL_CLK_SEL_0	R/W	0h	DCC CAL clock for address slice 0.
7-0	PHY_ADR_TSEL_SELECT_0	R/W	0h	Tsel select values for address slice 0.

4.4.602 DDRSS_PHY_1065 Register (Offset = 50A4h) [reset = X]

DDRSS_PHY_1065 is shown in Figure 4-1396 and described in Table 4-2800.

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Table 4-2799. DDRSS_PHY_1065 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50A4h

Figure 4-1396. DDRSS_PHY_1065 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_ADR1_SW_WRADDR_SHIFT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED					PHY_ADR0_CLK_WR_SLAVE_DELAY_0		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_ADR0_CLK_WR_SLAVE_DELAY_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR0_SW_WRADDR_SHIFT_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2800. DDRSS_PHY_1065 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_ADR1_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 1 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) is the cycle_shift value. For bits (4:3), clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles.
23-19	RESERVED	R/W	X	
18-8	PHY_ADR0_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 0 slave delay setting for address slice 0.
7-5	RESERVED	R/W	X	

Table 4-2800. DDRSS_PHY_1065 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	PHY_ADR0_SW_WRADDR_SHIFT_0	R/W	0h	<p>Manual override of CA bit 0 of automatic half_cycle_shift/cycle_shift for address slice 0.</p> <p>Bit (0) enables override of half_cycle_shift.</p> <p>Bit (1) is the half_cycle_shift value.</p> <p>Bit (2) enables override of cycle shift.</p> <p>Bits (4:3) is the cycle_shift value.</p> <p>For bits (4:3), clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles.</p>

4.4.603 DDRSS_PHY_1066 Register (Offset = 50A8h) [reset = X]

DDRSS_PHY_1066 is shown in [Figure 4-1397](#) and described in [Table 4-2802](#).

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Table 4-2801. DDRSS_PHY_1066 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50A8h

Figure 4-1397. DDRSS_PHY_1066 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR2_SW_WRADDR_SHIFT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR1_CLK_WR_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR1_CLK_WR_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2802. DDRSS_PHY_1066 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_ADR2_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 2 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) is the cycle_shift value. For bits (4:3), clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR1_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 1 slave delay setting for address slice 0.

4.4.604 DDRSS_PHY_1067 Register (Offset = 50ACh) [reset = X]

DDRSS_PHY_1067 is shown in Figure 4-1398 and described in Table 4-2804.

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Table 4-2803. DDRSS_PHY_1067 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50ACh

Figure 4-1398. DDRSS_PHY_1067 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR3_SW_WRADDR_SHIFT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR2_CLK_WR_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR2_CLK_WR_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2804. DDRSS_PHY_1067 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_ADR3_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 3 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) is the cycle_shift value. For bits (4:3), clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR2_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 2 slave delay setting for address slice 0.

4.4.605 DDRSS_PHY_1068 Register (Offset = 50B0h) [reset = X]

DDRSS_PHY_1068 is shown in [Figure 4-1399](#) and described in [Table 4-2806](#).

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Table 4-2805. DDRSS_PHY_1068 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50B0h

Figure 4-1399. DDRSS_PHY_1068 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR4_SW_WRADDR_SHIFT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR3_CLK_WR_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR3_CLK_WR_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2806. DDRSS_PHY_1068 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_ADR4_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 4 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) is the cycle_shift value. For bits (4:3), clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR3_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 3 slave delay setting for address slice 0.

4.4.606 DDRSS_PHY_1069 Register (Offset = 50B4h) [reset = X]

DDRSS_PHY_1069 is shown in Figure 4-1400 and described in Table 4-2808.

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Table 4-2807. DDRSS_PHY_1069 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50B4h

Figure 4-1400. DDRSS_PHY_1069 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR5_SW_WRADDR_SHIFT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR4_CLK_WR_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR4_CLK_WR_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2808. DDRSS_PHY_1069 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_ADR5_SW_WRADDR_SHIFT_0	R/W	0h	Manual override of CA bit 5 of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits (4:3) is the cycle_shift value. For bits (4:3), clear to 0x0 for no offset, program to 0x1 for -1 cycle, program to 0x2 for +1 cycle, or program to 0x3 for -2 cycles.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR4_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 4 slave delay setting for address slice 0.

4.4.607 DDRSS_PHY_1070 Register (Offset = 50B8h) [reset = X]

DDRSS_PHY_1070 is shown in [Figure 4-1401](#) and described in [Table 4-2810](#).

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Table 4-2809. DDRSS_PHY_1070 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50B8h

Figure 4-1401. DDRSS_PHY_1070 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_ADR_SW_MASTER_MODE_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR5_CLK_WR_SLAVE_DELAY_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR5_CLK_WR_SLAVE_DELAY_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2810. DDRSS_PHY_1070 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	PHY_ADR_SW_MASTER_MODE_0	R/W	0h	Master delay line override settings for address slice 0. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit (2) enables software bypass mode. Bit (3) is the software bypass mode value.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR5_CLK_WR_SLAVE_DELAY_0	R/W	0h	CA bit 5 slave delay setting for address slice 0.

4.4.608 DDRSS_PHY_1071 Register (Offset = 50BCh) [reset = X]

DDRSS_PHY_1071 is shown in [Figure 4-1402](#) and described in [Table 4-2812](#).

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Table 4-2811. DDRSS_PHY_1071 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50BCh

Figure 4-1402. DDRSS_PHY_1071 Register

31	30	29	28	27	26	25	24
PHY_ADR_MASTER_DELAY_WAIT_0							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_ADR_MASTER_DELAY_STEP_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED					PHY_ADR_MASTER_DELAY_START_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DELAY_START_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2812. DDRSS_PHY_1071 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_ADR_MASTER_DELAY_WAIT_0	R/W	0h	Wait cycles for master delay line locking algorithm for address slice 0. Bits (3:0) is the cycle wait count after a calibration clock setting change. Bits (7:4) is the cycle wait count after a master delay setting change.
23-22	RESERVED	R/W	X	
21-16	PHY_ADR_MASTER_DELAY_STEP_0	R/W	0h	Incremental step size for master delay line locking algorithm for address slice 0.
15-11	RESERVED	R/W	X	
10-0	PHY_ADR_MASTER_DELAY_START_0	R/W	0h	Start value for master delay line locking algorithm for address slice 0.

4.4.609 DDRSS_PHY_1072 Register (Offset = 50C0h) [reset = X]

DDRSS_PHY_1072 is shown in [Figure 4-1403](#) and described in [Table 4-2814](#).

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Table 4-2813. DDRSS_PHY_1072 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50C0h

Figure 4-1403. DDRSS_PHY_1072 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADR_SW_CALVL_DVW_MIN_EN_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_ADR_SW_CALVL_DVW_MIN_0	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
PHY_ADR_SW_CALVL_DVW_MIN_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_ADR_MASTER_DELAY_HALF_MEASURE_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2814. DDRSS_PHY_1072 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADR_SW_CALVL_DVW_MIN_EN_0	R/W	0h	Enables the software override data valid window size during CA training for address slice 0.
23-18	RESERVED	R/W	X	
17-8	PHY_ADR_SW_CALVL_DVW_MIN_0	R/W	0h	Sets the software override data valid window size during CA training for address slice 0.
7-0	PHY_ADR_MASTER_DELAY_HALF_MEASURE_0	R/W	0h	Defines the number of delay line elements to be considered in determining whether to lock to a half clock cycle for the master in address slice 0

4.4.610 DDRSS_PHY_1073 Register (Offset = 50C4h) [reset = X]

DDRSS_PHY_1073 is shown in [Figure 4-1404](#) and described in [Table 4-2816](#).

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Table 4-2815. DDRSS_PHY_1073 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50C4h

Figure 4-1404. DDRSS_PHY_1073 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_DLY_STEP_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2816. DDRSS_PHY_1073 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-0	PHY_ADR_CALVL_DLY_STEP_0	R/W	0h	Sets the delay step size plus 1 during CA training for address slice 0.

4.4.611 DDRSS_PHY_1074 Register (Offset = 50C8h) [reset = X]

DDRSS_PHY_1074 is shown in Figure 4-1405 and described in Table 4-2818.

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Table 4-2817. DDRSS_PHY_1074 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50C8h

Figure 4-1405. DDRSS_PHY_1074 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADR_DC_INIT_SLV_DELAY_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_ADR_DC_INIT_SLV_DELAY_0							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_ADR_MEAS_DLY_STEP_ENABLE_0	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED				PHY_ADR_CALVL_CAPTURE_CNT_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2818. DDRSS_PHY_1074 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_ADR_DC_INIT_SLV_DELAY_0	R/W	0h	DCC initialization value of write ADDR slave delay for address slice 0.
15-9	RESERVED	R/W	X	
8	PHY_ADR_MEAS_DLY_STEP_ENABLE_0	R/W	0h	Enables delay parameter setting using phy_adr_meas_dly_step_value for address slice 0.
7-4	RESERVED	R/W	X	
3-0	PHY_ADR_CALVL_CAPTURE_CNT_0	R/W	0h	Number of samples to take at each ADDR slave delay setting during CA training for address slice 0.

4.4.612 DDRSS_PHY_1075 Register (Offset = 50CCh) [reset = X]

DDRSS_PHY_1075 is shown in [Figure 4-1406](#) and described in [Table 4-2820](#).

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Table 4-2819. DDRSS_PHY_1075 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 50CCh

Figure 4-1406. DDRSS_PHY_1075 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
PHY_ADR_DC_DM_CLK_THRSHLD_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_ADR_DC_CALVL_ENABLE_0
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2820. DDRSS_PHY_1075 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	PHY_ADR_DC_DM_CLK_THRSHLD_0	R/W	0h	DCC clock measurement cell threshold offset for address slice 0.
7-1	RESERVED	R/W	X	
0	PHY_ADR_DC_CALVL_ENABLE_0	R/W	0h	DCC enable duty cycle adjust during CA leveling for address slice 0.

4.4.613 DDRSS_PHY_1280 Register (Offset = 5400h) [reset = X]

DDRSS_PHY_1280 is shown in [Figure 4-1407](#) and described in [Table 4-2822](#).

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Table 4-2821. DDRSS_PHY_1280 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5400h

Figure 4-1407. DDRSS_PHY_1280 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PHY_FREQ_SEL	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2822. DDRSS_PHY_1280 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	PHY_FREQ_SEL	R/W	0h	Specifies which copy of the frequency-dependent timing parameters will be used by the PHY.

4.4.614 DDRSS_PHY_1281 Register (Offset = 5404h) [reset = X]

DDRSS_PHY_1281 is shown in Figure 4-1408 and described in Table 4-2824.

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Table 4-2823. DDRSS_PHY_1281 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5404h

Figure 4-1408. DDRSS_PHY_1281 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_GRP0_SHIFT_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_FREQ_SEL_INDEX	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							PHY_FREQ_SEL_MULTICAST_EN
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
RESERVED							PHY_FREQ_SEL_FROM_REGIF
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2824. DDRSS_PHY_1281 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_SW_GRP0_SHIFT_0	R/W	0h	Address slice slave delay setting for address slice 4.
23-18	RESERVED	R/W	X	
17-16	PHY_FREQ_SEL_INDEX	R/W	0h	Selects which frequency set to update when PHY_FREQ_SEL_MULTICAST_EN is not set.
15-9	RESERVED	R/W	X	
8	PHY_FREQ_SEL_MULTICAST_EN	R/W	1h	When set, a register write will update parameters for all frequency sets simultaneously. Set to 1 to enable.
7-1	RESERVED	R/W	X	
0	PHY_FREQ_SEL_FROM_REGIF	R/W	0h	Indicates which source is used to select the frequency copy. When set to 1, the frequency select source is given by parameter PHY_FREQ_SEL from register I/F. When cleared to 0, the frequency select source is the PHY input signal dfi_frequency

4.4.615 DDRSS_PHY_1282 Register (Offset = 5408h) [reset = X]

DDRSS_PHY_1282 is shown in [Figure 4-1409](#) and described in [Table 4-2826](#).

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Table 4-2825. DDRSS_PHY_1282 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5408h

Figure 4-1409. DDRSS_PHY_1282 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_GRP0_SHIFT_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_SW_GRP3_SHIFT_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_GRP2_SHIFT_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_GRP1_SHIFT_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2826. DDRSS_PHY_1282 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_SW_GRP0_SHIFT_1	R/W	0h	Address slice slave delay setting for address slice 4.
23-21	RESERVED	R/W	X	
20-16	PHY_SW_GRP3_SHIFT_0	R/W	0h	Address slice slave delay setting for address slice 4.
15-13	RESERVED	R/W	X	
12-8	PHY_SW_GRP2_SHIFT_0	R/W	0h	Address slice slave delay setting for address slice 4.
7-5	RESERVED	R/W	X	
4-0	PHY_SW_GRP1_SHIFT_0	R/W	0h	Address slice slave delay setting for address slice 4.

4.4.616 DDRSS_PHY_1283 Register (Offset = 540Ch) [reset = X]

DDRSS_PHY_1283 is shown in Figure 4-1410 and described in Table 4-2828.

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Table 4-2827. DDRSS_PHY_1283 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 540Ch

Figure 4-1410. DDRSS_PHY_1283 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_SW_GRP3_SHIFT_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_SW_GRP2_SHIFT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_SW_GRP1_SHIFT_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2828. DDRSS_PHY_1283 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_SW_GRP3_SHIFT_1	R/W	0h	Address slice slave delay setting for address slice 4.
15-13	RESERVED	R/W	X	
12-8	PHY_SW_GRP2_SHIFT_1	R/W	0h	Address slice slave delay setting for address slice 4.
7-5	RESERVED	R/W	X	
4-0	PHY_SW_GRP1_SHIFT_1	R/W	0h	Address slice slave delay setting for address slice 4.

4.4.617 DDRSS_PHY_1284 Register (Offset = 5410h) [reset = X]

DDRSS_PHY_1284 is shown in [Figure 4-1411](#) and described in [Table 4-2830](#).

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Table 4-2829. DDRSS_PHY_1284 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5410h

Figure 4-1411. DDRSS_PHY_1284 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_GRP_BY PASS_OVERRI DE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED			PHY_SW_GRP_BYPASS_SHIFT				
R/W-X			R/W-0h				
15	14	13	12	11	10	9	8
RESERVED					PHY_GRP_BYPASS_SLAVE_DELAY		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_GRP_BYPASS_SLAVE_DELAY							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2830. DDRSS_PHY_1284 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_GRP_BYPASS_OV ERRIDE	R/W	0h	Address/control group slice bypass mode override setting.
23-21	RESERVED	R/W	X	
20-16	PHY_SW_GRP_BYPASS _SHIFT	R/W	0h	Address/control group slice bypass mode shift settings.
15-11	RESERVED	R/W	X	
10-0	PHY_GRP_BYPASS_SLA VE_DELAY	R/W	0h	Address/control group slice bypass mode slave delay setting.

4.4.618 DDRSS_PHY_1285 Register (Offset = 5414h) [reset = X]

DDRSS_PHY_1285 is shown in [Figure 4-1412](#) and described in [Table 4-2832](#).

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Table 4-2831. DDRSS_PHY_1285 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5414h

Figure 4-1412. DDRSS_PHY_1285 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_CSLVL_START		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_CSLVL_START							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_MANUAL_UPDATE_PHY_UPD_ENABLE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_MANUAL_UPDATE
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2832. DDRSS_PHY_1285 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_CSLVL_START	R/W	0h	Defines the CS training DDL start value.
15-9	RESERVED	R/W	X	
8	PHY_MANUAL_UPDATE_PHYUPD_ENABLE	R/W	0h	Manual update selection of all slave delay line settings. Set 1 to assert phyupd_req and wait phyupd_ack to update delay line, set 0 to update delay line directly.
7-1	RESERVED	R/W	X	
0	SC_PHY_MANUAL_UPDATE	W	0h	Manual update of all slave delay line settings. Set to 1 to trigger. WRITE-ONLY

4.4.619 DDRSS_PHY_1286 Register (Offset = 5418h) [reset = X]

DDRSS_PHY_1286 is shown in [Figure 4-1413](#) and described in [Table 4-2834](#).

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Table 4-2833. DDRSS_PHY_1286 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5418h

Figure 4-1413. DDRSS_PHY_1286 Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_CSLVL_DEBUG_COUNT
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_CSLVL_DEBUG_MODE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED					PHY_CSLVL_COARSE_DLY		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CSLVL_COARSE_DLY							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2834. DDRSS_PHY_1286 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	SC_PHY_CSLVL_DEBUG_COUNT	W	0h	Allows the CS training state machine to advance (when in debug mode). Set to 1 to trigger. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PHY_CSLVL_DEBUG_MODE	R/W	0h	Enables CS training debug mode. Set to 1 to enable.
15-11	RESERVED	R/W	X	
10-0	PHY_CSLVL_COARSE_DLY	R/W	0h	Defines the CS training DDL coarse cycle delay value.

4.4.620 DDRSS_PHY_1287 Register (Offset = 541Ch) [reset = X]

DDRSS_PHY_1287 is shown in [Figure 4-1414](#) and described in [Table 4-2836](#).

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Table 4-2835. DDRSS_PHY_1287 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 541Ch

Figure 4-1414. DDRSS_PHY_1287 Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_CSLV L_ERROR_CL R
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-2836. DDRSS_PHY_1287 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	SC_PHY_CSLVL_ERROR_CLR	W	0h	Clears the CS training state machine error status. Set to 1 to trigger. WRITE-ONLY

4.4.621 DDRSS_PHY_1288 Register (Offset = 5420h) [reset = 06800000h]

DDRSS_PHY_1288 is shown in [Figure 4-1415](#) and described in [Table 4-2838](#).

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Table 4-2837. DDRSS_PHY_1288 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5420h

Figure 4-1415. DDRSS_PHY_1288 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CSLVL_OBS0																															
R-06800000h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2838. DDRSS_PHY_1288 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_CSLVL_OBS0	R	06800000h	Observation register for CS training delay values. READ-ONLY

4.4.622 DDRSS_PHY_1289 Register (Offset = 5424h) [reset = 0h]

DDRSS_PHY_1289 is shown in [Figure 4-1416](#) and described in [Table 4-2840](#).

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Table 4-2839. DDRSS_PHY_1289 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5424h

Figure 4-1416. DDRSS_PHY_1289 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CSLVL_OBS1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2840. DDRSS_PHY_1289 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_CSLVL_OBS1	R	0h	Observation register for CS training algorithm status. READ-ONLY

4.4.623 DDRSS_PHY_1290 Register (Offset = 5428h) [reset = 0h]

DDRSS_PHY_1290 is shown in [Figure 4-1417](#) and described in [Table 4-2842](#).

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Table 4-2841. DDRSS_PHY_1290 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5428h

Figure 4-1417. DDRSS_PHY_1290 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CSLVL_OBS2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2842. DDRSS_PHY_1290 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_CSLVL_OBS2	R	0h	Observation register for periodic CS training delay values. READ-ONLY

4.4.624 DDRSS_PHY_1291 Register (Offset = 542Ch) [reset = X]

DDRSS_PHY_1291 is shown in [Figure 4-1418](#) and described in [Table 4-2844](#).

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Table 4-2843. DDRSS_PHY_1291 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 542Ch

Figure 4-1418. DDRSS_PHY_1291 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LP4_BOOT_DISABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_CSLVL_PERIODIC_START_OFFSET
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_CSLVL_PERIODIC_START_OFFSET							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_CSLVL_ENABLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2844. DDRSS_PHY_1291 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LP4_BOOT_DISABLE	R/W	0h	Controls the handling of the DFI frequency. When set to 1, DFI frequency 0 is considered the first operational frequency. When cleared to 0, DFI frequency 0 is the boot frequency and other DFI frequency values are operational frequencies. Must be cleared to 0 for LPDDR3 devices operating in an LPDDR4 capable configuration.
23-17	RESERVED	R/W	X	
16-8	PHY_CSLVL_PERIODIC_START_OFFSET	R/W	0h	Defines the relative offset from previous LE and TE to start periodic CSLVL with.
7-1	RESERVED	R/W	X	
0	PHY_CSLVL_ENABLE	R/W	0h	CS training enable. Set to 1 to enable CS training during CA training.

4.4.625 DDRSS_PHY_1292 Register (Offset = 5430h) [reset = X]

DDRSS_PHY_1292 is shown in [Figure 4-1419](#) and described in [Table 4-2846](#).

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Table 4-2845. DDRSS_PHY_1292 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5430h

Figure 4-1419. DDRSS_PHY_1292 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED					PHY_CSLVL_QTR		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_CSLVL_QTR							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_CSLVL_CS_MAP			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2846. DDRSS_PHY_1292 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R/W	X	
18-8	PHY_CSLVL_QTR	R/W	0h	Defines the CS training DDL 1/4 cycle delay value.
7-4	RESERVED	R/W	X	
3-0	PHY_CSLVL_CS_MAP	R/W	0h	CS training map. Set each CS bit to 1 to allow that CS to participate in CS training results. NOT CURRENTLY USED.

4.4.626 DDRSS_PHY_1293 Register (Offset = 5434h) [reset = X]

DDRSS_PHY_1293 is shown in Figure 4-1420 and described in Table 4-2848.

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Table 4-2847. DDRSS_PHY_1293 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5434h

Figure 4-1420. DDRSS_PHY_1293 Register

31	30	29	28	27	26	25	24
PHY_CALVL_CS_MAP							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED				PHY_CSLVL_COARSE_CAPTURE_CNT			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED					PHY_CSLVL_COARSE_CHK		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CSLVL_COARSE_CHK							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2848. DDRSS_PHY_1293 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_CALVL_CS_MAP	R/W	0h	Defines the slice numbers associated with each CS during CA training.
23-20	RESERVED	R/W	X	
19-16	PHY_CSLVL_COARSE_CAPTURE_CNT	R/W	0h	Defines the number of samples to take at each GRP slave delay setting during CS training coarse CA training.
15-11	RESERVED	R/W	X	
10-0	PHY_CSLVL_COARSE_CHK	R/W	0h	Defines the CS training coarse CA training DDL 1/16th cycle delay value.

4.4.627 DDRSS_PHY_1294 Register (Offset = 5438h) [reset = X]

DDRSS_PHY_1294 is shown in Figure 4-1421 and described in Table 4-2850.

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Table 4-2849. DDRSS_PHY_1294 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5438h

Figure 4-1421. DDRSS_PHY_1294 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_ADRCTL_LPDDR
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED						PHY_DFI_PHYUPD_TYPE	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED							PHY_ADRCTL_SNAP_OBS_REGS
R/W-X							W-0h
7	6	5	4	3	2	1	0
RESERVED					PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2850. DDRSS_PHY_1294 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_ADRCTL_LPDDR	R/W	0h	Adds a cycle of delay for the address/control slices to match the address slice.
23-18	RESERVED	R/W	X	
17-16	PHY_DFI_PHYUPD_TYPE	R/W	0h	Defines the value of the dfi_phyupd_type output signal to MC.
15-9	RESERVED	R/W	X	
8	PHY_ADRCTL_SNAP_OBS_REGS	W	0h	Initiates a snapshot of the internal observation registers for the address/control block. Set to 1 to trigger. WRITE-ONLY
7-3	RESERVED	R/W	X	
2-0	PHY_ADRCTL_SLAVE_LOOP_CNT_UPDATE	R/W	0h	Reserved for the address/control master.

4.4.628 DDRSS_PHY_1295 Register (Offset = 543Ch) [reset = X]

DDRSS_PHY_1295 is shown in [Figure 4-1422](#) and described in [Table 4-2852](#).

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Table 4-2851. DDRSS_PHY_1295 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 543Ch

Figure 4-1422. DDRSS_PHY_1295 Register

31	30	29	28	27	26	25	24
PHY_CLK_DC_CAL_TIMEOUT							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_CLK_DC_CAL_SAMPLE_WAIT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_LPDDR3_CS
R/W-X							R/W-1h
7	6	5	4	3	2	1	0
RESERVED							PHY_LP4_ACTIVE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2852. DDRSS_PHY_1295 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_CLK_DC_CAL_TIMEOUT	R/W	0h	Duty cycle correction maximum iteration count.
23-16	PHY_CLK_DC_CAL_SAMPLE_WAIT	R/W	0h	Number of cal clock cycles to wait for a sample to be taken.
15-9	RESERVED	R/W	X	
8	PHY_LPDDR3_CS	R/W	1h	Alters reset state polarity for LPDDR chip selects.
7-1	RESERVED	R/W	X	
0	PHY_LP4_ACTIVE	R/W	0h	Indicates an LPDDR4 device is connected to the PHY.

4.4.629 DDRSS_PHY_1296 Register (Offset = 5440h) [reset = X]

DDRSS_PHY_1296 is shown in [Figure 4-1423](#) and described in [Table 4-2854](#).

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Table 4-2853. DDRSS_PHY_1296 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5440h

Figure 4-1423. DDRSS_PHY_1296 Register

31	30	29	28	27	26	25	24
PHY_CLK_DC_ADJUST_SAMPLE_CNT							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED		PHY_CLK_DC_ADJUST_START					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							PHY_CLK_DC_FREQ_CHG_ADJ
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PHY_CLK_DC_WEIGHT	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2854. DDRSS_PHY_1296 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	PHY_CLK_DC_ADJUST_SAMPLE_CNT	R/W	0h	Duty cycle correction algorithm sample count per adjustment setting.
23-22	RESERVED	R/W	X	
21-16	PHY_CLK_DC_ADJUST_START	R/W	0h	Duty cycle correction algorithm adjustment starting value.
15-9	RESERVED	R/W	X	
8	PHY_CLK_DC_FREQ_CHG_ADJ	R/W	0h	Duty cycle correction during frequency change control.
7-2	RESERVED	R/W	X	
1-0	PHY_CLK_DC_WEIGHT	R/W	0h	Duty cycle correction weighting factor base value.

4.4.630 DDRSS_PHY_1297 Register (Offset = 5444h) [reset = X]

DDRSS_PHY_1297 is shown in Figure 4-1424 and described in Table 4-2856.

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Table 4-2855. DDRSS_PHY_1297 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5444h

Figure 4-1424. DDRSS_PHY_1297 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_DC_CAL_START
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_CLK_DC_CAL_POLARITY
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_CLK_DC_ADJUST_DIRECT
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_CLK_DC_ADJUST_THRSHLD							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2856. DDRSS_PHY_1297 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CLK_DC_CAL_START	R/W	0h	Duty cycle correction calibration manual start.
23-17	RESERVED	R/W	X	
16	PHY_CLK_DC_CAL_POLARITY	R/W	0h	Duty cycle correction algorithm measurement polarity.
15-9	RESERVED	R/W	X	
8	PHY_CLK_DC_ADJUST_DIRECT	R/W	0h	Duty cycle correction algorithm adjustment direction.
7-0	PHY_CLK_DC_ADJUST_THRSHLD	R/W	0h	Duty cycle correction algorithm threshold delta comparison.

4.4.631 DDRSS_PHY_1298 Register (Offset = 5448h) [reset = X]

DDRSS_PHY_1298 is shown in [Figure 4-1425](#) and described in [Table 4-2858](#).

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Table 4-2857. DDRSS_PHY_1298 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5448h

Figure 4-1425. DDRSS_PHY_1298 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_SW_TXIO_CTRL_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_SW_TXIO_CTRL_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							PHY_CONTINUOUS_CLK_CAL_UPDATE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_UPDATE_CLK_CAL_VALUES
R/W-X							W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2858. DDRSS_PHY_1298 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_SW_TXIO_CTRL_1	R/W	0h	This register is used to control if command pad (CS/RAS...) should be shutoff for TX mode.
23-20	RESERVED	R/W	X	
19-16	PHY_SW_TXIO_CTRL_0	R/W	0h	This register is used to control if command pad (CS/RAS...) should be shutoff for TX mode.
15-9	RESERVED	R/W	X	
8	PHY_CONTINUOUS_CLK_CAL_UPDATE	R/W	0h	Continuous update of all latest PVTP,PVTN and PVTR values to the CLK IO pads. Set to 1 to keep this enabled.
7-1	RESERVED	R/W	X	
0	SC_PHY_UPDATE_CLK_CAL_VALUES	W	0h	Manual update of all latest PVTP,PVTN and PVTR values to the CLK IO pads. Set to 1 to trigger. WRITE-ONLY

4.4.632 DDRSS_PHY_1299 Register (Offset = 544Ch) [reset = X]

DDRSS_PHY_1299 is shown in [Figure 4-1426](#) and described in [Table 4-2860](#).

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Table 4-2859. DDRSS_PHY_1299 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 544Ch

Figure 4-1426. DDRSS_PHY_1299 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_MEMCLK_SW_TXPWR_CTRL
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_ADRCTL_SW_TXPWR_CTRL_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED							PHY_MEMCLK_SW_TXIO_CTRL
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2860. DDRSS_PHY_1299 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_MEMCLK_SW_TXPWR_CTRL	R/W	0h	This register is used to control if clk pads should be shutoff for TX mode in deep sleep mode.
23-20	RESERVED	R/W	X	
19-16	PHY_ADRCTL_SW_TXPWR_CTRL_1	R/W	0h	This register is used to control if address/command pad (address/CS/RAS...) should be shutoff for TX mode in deep sleep mode.
15-12	RESERVED	R/W	X	
11-8	PHY_ADRCTL_SW_TXPWR_CTRL_0	R/W	0h	This register is used to control if address/command pad (address/CS/RAS...) should be shutoff for TX mode in deep sleep mode.
7-1	RESERVED	R/W	X	
0	PHY_MEMCLK_SW_TXIO_CTRL	R/W	0h	This register is used to control if clk pads should be shutoff for TX mode.

4.4.633 DDRSS_PHY_1300 Register (Offset = 5450h) [reset = X]

DDRSS_PHY_1300 is shown in [Figure 4-1427](#) and described in [Table 4-2862](#).

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Table 4-2861. DDRSS_PHY_1300 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5450h

Figure 4-1427. DDRSS_PHY_1300 Register

31	30	29	28	27	26	25	24
PHY_STATIC_TOG_CONTROL							
R/W-0h							
23	22	21	20	19	18	17	16
PHY_STATIC_TOG_CONTROL							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_BYTE_DISABLE_STATIC_TOG_DISABLE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_TOP_STATIC_TOG_DISABLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2862. DDRSS_PHY_1300 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	PHY_STATIC_TOG_CONTROL	R/W	0h	Clock divider to create toggle signal. Use long counter as the base.
15-9	RESERVED	R/W	X	
8	PHY_BYTE_DISABLE_STATIC_TOG_DISABLE	R/W	0h	Control to disable the toggle signal for data slice during static activity when dfi_data_byte_disable is asserted.
7-1	RESERVED	R/W	X	
0	PHY_TOP_STATIC_TOG_DISABLE	R/W	0h	Disables the generation of the toggle for static clock based paths in the PHY to prevent assymmetric aging.

4.4.634 DDRSS_PHY_1301 Register (Offset = 5454h) [reset = X]

DDRSS_PHY_1301 is shown in Figure 4-1428 and described in Table 4-2864.

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Table 4-2863. DDRSS_PHY_1301 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5454h

Figure 4-1428. DDRSS_PHY_1301 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_LP4_BOOT_PLL_BYPASS
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_MEMCLK_STATIC_TOG_DISABLE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				PHY_ADRCTL_STATIC_TOG_DISABLE			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2864. DDRSS_PHY_1301 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_LP4_BOOT_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select.
15-9	RESERVED	R/W	X	
8	PHY_MEMCLK_STATIC_TOG_DISABLE	R/W	0h	Control to disable toggle during static activity. bit 0: clock disable.
7-4	RESERVED	R/W	X	
3-0	PHY_ADRCTL_STATIC_TOG_DISABLE	R/W	0h	Control to disable toggle during static activity. bit 0: Write path delay line disable bit 1: clock disable bit 2: adrctl master delay line disable (if exists) bit 3: adrctl misc core clk disable.(if exists)

4.4.635 DDRSS_PHY_1302 Register (Offset = 5458h) [reset = 10082650h]

DDRSS_PHY_1302 is shown in [Figure 4-1429](#) and described in [Table 4-2866](#).

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Table 4-2865. DDRSS_PHY_1302 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5458h

Figure 4-1429. DDRSS_PHY_1302 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CLK_SWITCH_OBS																															
R-10082650h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2866. DDRSS_PHY_1302 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_CLK_SWITCH_OBS	R	10082650h	Observation register for Clock switch state machine READ-ONLY

4.4.636 DDRSS_PHY_1303 Register (Offset = 545Ch) [reset = X]

DDRSS_PHY_1303 is shown in [Figure 4-1430](#) and described in [Table 4-2868](#).

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Table 4-2867. DDRSS_PHY_1303 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 545Ch

Figure 4-1430. DDRSS_PHY_1303 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHY_PLL_WAIT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2868. DDRSS_PHY_1303 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHY_PLL_WAIT	R/W	0h	PHY clock PLL wait time after locking.

4.4.637 DDRSS_PHY_1304 Register (Offset = 5460h) [reset = X]

DDRSS_PHY_1304 is shown in [Figure 4-1431](#) and described in [Table 4-2870](#).

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Table 4-2869. DDRSS_PHY_1304 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5460h

Figure 4-1431. DDRSS_PHY_1304 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PHY_SW_PLL_BYPASS
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2870. DDRSS_PHY_1304 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PHY_SW_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select.

4.4.638 DDRSS_PHY_1305 Register (Offset = 5464h) [reset = X]

DDRSS_PHY_1305 is shown in [Figure 4-1432](#) and described in [Table 4-2872](#).

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Table 4-2871. DDRSS_PHY_1305 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5464h

Figure 4-1432. DDRSS_PHY_1305 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CS_ACS_ALLOCATION_BIT1_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CS_ACS_ALLOCATION_BIT0_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_SET_DFI_INPUT_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_SET_DFI_INPUT_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2872. DDRSS_PHY_1305 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_CS_ACS_ALLOCATION_BIT1_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_0 bit1, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s.
23-20	RESERVED	R/W	X	
19-16	PHY_CS_ACS_ALLOCATION_BIT0_0	R/W	0h	The map for which chip select is associated with each bit in the adrctl slice 0. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_0 bit0, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s.
15-12	RESERVED	R/W	X	
11-8	PHY_SET_DFI_INPUT_1	R/W	0h	Used to indicate the default value of the adrctl slice bits.
7-4	RESERVED	R/W	X	
3-0	PHY_SET_DFI_INPUT_0	R/W	0h	Used to indicate the default value of the adrctl slice bits.

4.4.639 DDRSS_PHY_1306 Register (Offset = 5468h) [reset = X]

DDRSS_PHY_1306 is shown in [Figure 4-1433](#) and described in [Table 4-2874](#).

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Table 4-2873. DDRSS_PHY_1306 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5468h

Figure 4-1433. DDRSS_PHY_1306 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CS_ACS_ALLOCATION_BIT1_1			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CS_ACS_ALLOCATION_BIT0_1			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_CS_ACS_ALLOCATION_BIT3_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CS_ACS_ALLOCATION_BIT2_0			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2874. DDRSS_PHY_1306 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_CS_ACS_ALLOCATION_BIT1_1	R/W	0h	The map for which chip select is associated with each bit in the adrcctl slice 1. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_1 bit1, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s.
23-20	RESERVED	R/W	X	
19-16	PHY_CS_ACS_ALLOCATION_BIT0_1	R/W	0h	The map for which chip select is associated with each bit in the adrcctl slice 1. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_1 bit0, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_1, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s.
15-12	RESERVED	R/W	X	
11-8	PHY_CS_ACS_ALLOCATION_BIT3_0	R/W	0h	The map for which chip select is associated with each bit in the adrcctl slice 0. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_0 bit3, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s.
7-4	RESERVED	R/W	X	

Table 4-2874. DDRSS_PHY_1306 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	PHY_CS_ACS_ALLOCAT ION_BIT2_0	R/W	0h	<p>The map for which chip select is associated with each bit in the adrctl slice 0.</p> <p>Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_0 bit2 , 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not tranfser on ACS_0, if the accroding cs[n]'s training is not enabled, need to set the value to all 1s.</p>

4.4.640 DDRSS_PHY_1307 Register (Offset = 546Ch) [reset = X]

DDRSS_PHY_1307 is shown in [Figure 4-1434](#) and described in [Table 4-2876](#).

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Table 4-2875. DDRSS_PHY_1307 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 546Ch

Figure 4-1434. DDRSS_PHY_1307 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CLK_DC_INIT_DISABLE
R/W-X							R/W-1h
23	22	21	20	19	18	17	16
PHY_CLK_DC_ADJUST_0							
R/W-20h							
15	14	13	12	11	10	9	8
RESERVED				PHY_CS_ACS_ALLOCATION_BIT3_1			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CS_ACS_ALLOCATION_BIT2_1			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2876. DDRSS_PHY_1307 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CLK_DC_INIT_DISABLE	R/W	1h	Disable duty cycle adjust at initialization.
23-16	PHY_CLK_DC_ADJUST_0	R/W	20h	Adjust value of Duty Cycle Adjuster for clock slice 0.
15-12	RESERVED	R/W	X	
11-8	PHY_CS_ACS_ALLOCATION_BIT3_1	R/W	0h	The map for which chip select is associated with each bit in the address slice 1. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_1 bit3, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_1, if the according cs[n]'s training is not enabled, need to set the value to all 1s.
7-4	RESERVED	R/W	X	
3-0	PHY_CS_ACS_ALLOCATION_BIT2_1	R/W	0h	The map for which chip select is associated with each bit in the address slice 1. Bit (n), 1 means cs[n]'s signal(CS/CKE/ODT/RST) is allocated on ACS_1 bit2, 0 means cs[n]'s signal(CS/CKE/ODT/RST) is not transfer on ACS_1, if the according cs[n]'s training is not enabled, need to set the value to all 1s.

4.4.641 DDRSS_PHY_1308 Register (Offset = 5470h) [reset = X]

DDRSS_PHY_1308 is shown in [Figure 4-1435](#) and described in [Table 4-2878](#).

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Table 4-2877. DDRSS_PHY_1308 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5470h

Figure 4-1435. DDRSS_PHY_1308 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED											PHY_LP4_BOOT_PLL_CTRL				
R/W-X											R/W-0h				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LP4_BOOT_PLL_CTRL								PHY_CLK_DC_DM_THRSHLD							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2878. DDRSS_PHY_1308 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-8	PHY_LP4_BOOT_PLL_CTRL	R/W	0h	PHY deskew PLL controls for LPDDR4 boot frequency.
7-0	PHY_CLK_DC_DM_THRSHLD	R/W	0h	Data measurement cell threshold offset.

4.4.642 DDRSS_PHY_1309 Register (Offset = 5474h) [reset = X]

DDRSS_PHY_1309 is shown in [Figure 4-1436](#) and described in [Table 4-2880](#).

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Table 4-2879. DDRSS_PHY_1309 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5474h

Figure 4-1436. DDRSS_PHY_1309 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_USE_PLL_DSKEWCALLOCK
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_PLL_CTRL_OVERRIDE							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_PLL_CTRL_OVERRIDE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2880. DDRSS_PHY_1309 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_USE_PLL_DSKEWCALLOCK	R/W	0h	Use DSKEWCALLOCK or not.
15-0	PHY_PLL_CTRL_OVERRIDE	R/W	0h	Individual PHY clock PLL control overrides.

4.4.643 DDRSS_PHY_1310 Register (Offset = 5478h) [reset = X]

DDRSS_PHY_1310 is shown in [Figure 4-1437](#) and described in [Table 4-2882](#).

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Table 4-2881. DDRSS_PHY_1310 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5478h

Figure 4-1437. DDRSS_PHY_1310 Register

31	30	29	28	27	26	25	24
RESERVED						SC_PHY_PLL_SPO_CAL_SNAP_OBS	
R/W-X						W-0h	
23	22	21	20	19	18	17	16
RESERVED					PHY_PLL_SPO_CAL_CTRL		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_PLL_SPO_CAL_CTRL							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_PLL_SPO_CAL_CTRL							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2882. DDRSS_PHY_1310 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	SC_PHY_PLL_SPO_CAL_SNAP_OBS	W	0h	Register command to take a snapshot of PLL output. WRITE-ONLY
23-19	RESERVED	R/W	X	
18-0	PHY_PLL_SPO_CAL_CTRL	R/W	0h	PLL SPO Cal controls.

4.4.644 DDRSS_PHY_1311 Register (Offset = 547Ch) [reset = X]

DDRSS_PHY_1311 is shown in [Figure 4-1438](#) and described in [Table 4-2884](#).

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Table 4-2883. DDRSS_PHY_1311 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 547Ch

Figure 4-1438. DDRSS_PHY_1311 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED						SC_PHY_PLL_CAL_CLK_MEAS	
R/W-X						W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_PLL_CAL_CLK_MEAS_CYCLES	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_PLL_CAL_CLK_MEAS_CYCLES							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2884. DDRSS_PHY_1311 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-16	SC_PHY_PLL_CAL_CLK_MEAS	W	0h	Register command to initiate cal_clkout clock frequency measurement. WRITE-ONLY
15-10	RESERVED	R/W	X	
9-0	PHY_PLL_CAL_CLK_MEAS_CYCLES	R/W	0h	Measurement cycles of cal_clkout clock.

4.4.645 DDRSS_PHY_1312 Register (Offset = 5480h) [reset = X]

DDRSS_PHY_1312 is shown in [Figure 4-1439](#) and described in [Table 4-2886](#).

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Table 4-2885. DDRSS_PHY_1312 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5480h

Figure 4-1439. DDRSS_PHY_1312 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHY_PLL_OBS_0															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2886. DDRSS_PHY_1312 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	PHY_PLL_OBS_0	R	0h	PHY TOP level clock PLL_0 observe values. READ-ONLY

4.4.646 DDRSS_PHY_1313 Register (Offset = 5484h) [reset = X]

DDRSS_PHY_1313 is shown in [Figure 4-1440](#) and described in [Table 4-2888](#).

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Table 4-2887. DDRSS_PHY_1313 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5484h

Figure 4-1440. DDRSS_PHY_1313 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PHY_P LL_SP O_CAL _OBS_ _0
R-X															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PLL_SPO_CAL_OBS_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2888. DDRSS_PHY_1313 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-0	PHY_PLL_SPO_CAL_OBS_0	R	0h	PHY TOP level PLL_0 SPO Cal observe values. READ-ONLY

4.4.647 DDRSS_PHY_1314 Register (Offset = 5488h) [reset = X]

DDRSS_PHY_1314 is shown in [Figure 4-1441](#) and described in [Table 4-2890](#).

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Table 4-2889. DDRSS_PHY_1314 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5488h

Figure 4-1441. DDRSS_PHY_1314 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													PHY_PLL_CAL_CLK_MEAS_OBS_0		
R-X													R-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PLL_CAL_CLK_MEAS_OBS_0															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2890. DDRSS_PHY_1314 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17-0	PHY_PLL_CAL_CLK_MEAS_OBS_0	R	0h	PHY TOP level PLL_0 cal_clkout measurement observe values. READ-ONLY

4.4.648 DDRSS_PHY_1315 Register (Offset = 548Ch) [reset = X]

DDRSS_PHY_1315 is shown in [Figure 4-1442](#) and described in [Table 4-2892](#).

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Table 4-2891. DDRSS_PHY_1315 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 548Ch

Figure 4-1442. DDRSS_PHY_1315 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHY_PLL_OBS_1															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2892. DDRSS_PHY_1315 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	PHY_PLL_OBS_1	R	0h	PHY TOP level clock PLL_1 observe values. READ-ONLY

4.4.649 DDRSS_PHY_1316 Register (Offset = 5490h) [reset = X]

DDRSS_PHY_1316 is shown in [Figure 4-1443](#) and described in [Table 4-2894](#).

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Table 4-2893. DDRSS_PHY_1316 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5490h

Figure 4-1443. DDRSS_PHY_1316 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															PHY_P LL_SP O_CAL _OBS_ _1
R-X															R-0h
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PLL_SPO_CAL_OBS_1															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 4-2894. DDRSS_PHY_1316 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	X	
16-0	PHY_PLL_SPO_CAL_OBS_1	R	0h	PHY TOP level PLL_1 SPO Cal observe values. READ-ONLY

4.4.650 DDRSS_PHY_1317 Register (Offset = 5494h) [reset = X]

DDRSS_PHY_1317 is shown in Figure 4-1444 and described in Table 4-2896.

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Table 4-2895. DDRSS_PHY_1317 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5494h

Figure 4-1444. DDRSS_PHY_1317 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LP4_BOOT_LOW_FREQ_SEL
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_PLL_CAL_CLK_MEAS_OBS_1
R/W-X							R-0h
15	14	13	12	11	10	9	8
PHY_PLL_CAL_CLK_MEAS_OBS_1							
R-0h							
7	6	5	4	3	2	1	0
PHY_PLL_CAL_CLK_MEAS_OBS_1							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2896. DDRSS_PHY_1317 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LP4_BOOT_LOW_FREQ_SEL	R/W	0h	Control the PLL domain enter/exit from the negative clock edge for LPDDR4 boot frequency.
23-18	RESERVED	R/W	X	
17-0	PHY_PLL_CAL_CLK_MEAS_OBS_1	R	0h	PHY TOP level PLL_1 cal_clkout measurement observe values. READ-ONLY

4.4.651 DDRSS_PHY_1318 Register (Offset = 5498h) [reset = X]

DDRSS_PHY_1318 is shown in Figure 4-1445 and described in Table 4-2898.

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Table 4-2897. DDRSS_PHY_1318 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5498h

Figure 4-1445. DDRSS_PHY_1318 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_LS_IDLE_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_LP_WAKEUP							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				PHY_TCKSRE_WAIT			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2898. DDRSS_PHY_1318 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_LS_IDLE_EN	R/W	0h	Indicates the Reduced Idle Power State is enabled in low power mode.
15-8	PHY_LP_WAKEUP	R/W	0h	Specifies the number of cycles the PHY takes to wakeup in low power mode.
7-4	RESERVED	R/W	X	
3-0	PHY_TCKSRE_WAIT	R/W	0h	Specifies the number of cycles the PHY should wait before turning off the PLL for a deep sleep or DFS event.

4.4.652 DDRSS_PHY_1319 Register (Offset = 549Ch) [reset = X]

DDRSS_PHY_1319 is shown in [Figure 4-1446](#) and described in [Table 4-2900](#).

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Table 4-2899. DDRSS_PHY_1319 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 549Ch

Figure 4-1446. DDRSS_PHY_1319 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_TDFI_PHY_WRDELAY
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED						PHY_LP_CTRLUPD_CNTR_CFG	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_LP_CTRLUPD_CNTR_CFG							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2900. DDRSS_PHY_1319 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_TDFI_PHY_WRDELAY	R/W	0h	DFI timing parameter TDFI_PHY_WRDELAY.
15-10	RESERVED	R/W	X	
9-0	PHY_LP_CTRLUPD_CNTR_CFG	R/W	0h	Specifies the number of cycles the PHY takes from light sleep req deassert to ack deassert in low power mode.

4.4.653 DDRSS_PHY_1320 Register (Offset = 54A0h) [reset = X]

DDRSS_PHY_1320 is shown in [Figure 4-1447](#) and described in [Table 4-2902](#).

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Table 4-2901. DDRSS_PHY_1320 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54A0h

Figure 4-1447. DDRSS_PHY_1320 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_FDBK_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2902. DDRSS_PHY_1320 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_FDBK_TERM	R/W	4410h	Controls term settings for gate feedback pads.

4.4.654 DDRSS_PHY_1321 Register (Offset = 54A4h) [reset = X]

DDRSS_PHY_1321 is shown in [Figure 4-1448](#) and described in [Table 4-2904](#).

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Table 4-2903. DDRSS_PHY_1321 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54A4h

Figure 4-1448. DDRSS_PHY_1321 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHY_PAD_DATA_TERM															
R/W-X																R/W-4410h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2904. DDRSS_PHY_1321 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16-0	PHY_PAD_DATA_TERM	R/W	4410h	Controls term settings for data pads.

4.4.655 DDRSS_PHY_1322 Register (Offset = 54A8h) [reset = X]

DDRSS_PHY_1322 is shown in [Figure 4-1449](#) and described in [Table 4-2906](#).

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Table 4-2905. DDRSS_PHY_1322 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54A8h

Figure 4-1449. DDRSS_PHY_1322 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PHY_PAD_DQS_TERM															
R/W-X																R/W-4410h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2906. DDRSS_PHY_1322 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16-0	PHY_PAD_DQS_TERM	R/W	4410h	Controls term settings for dqs pads.

4.4.656 DDRSS_PHY_1323 Register (Offset = 54ACh) [reset = X]

DDRSS_PHY_1323 is shown in [Figure 4-1450](#) and described in [Table 4-2908](#).

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Table 4-2907. DDRSS_PHY_1323 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54ACh

Figure 4-1450. DDRSS_PHY_1323 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_ADDR_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2908. DDRSS_PHY_1323 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_ADDR_TERM	R/W	4410h	Controls term settings for the address/control pads.

4.4.657 DDRSS_PHY_1324 Register (Offset = 54B0h) [reset = X]

DDRSS_PHY_1324 is shown in [Figure 4-1451](#) and described in [Table 4-2910](#).

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Table 4-2909. DDRSS_PHY_1324 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54B0h

Figure 4-1451. DDRSS_PHY_1324 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_CLK_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2910. DDRSS_PHY_1324 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_CLK_TERM	R/W	4410h	Controls term settings for clock pads.

4.4.658 DDRSS_PHY_1325 Register (Offset = 54B4h) [reset = X]

DDRSS_PHY_1325 is shown in [Figure 4-1452](#) and described in [Table 4-2912](#).

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Table 4-2911. DDRSS_PHY_1325 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54B4h

Figure 4-1452. DDRSS_PHY_1325 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_CKE_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2912. DDRSS_PHY_1325 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_CKE_TERM	R/W	4410h	Controls term settings for cke pads.

4.4.659 DDRSS_PHY_1326 Register (Offset = 54B8h) [reset = X]

DDRSS_PHY_1326 is shown in [Figure 4-1453](#) and described in [Table 4-2914](#).

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Table 4-2913. DDRSS_PHY_1326 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54B8h

Figure 4-1453. DDRSS_PHY_1326 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_RST_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2914. DDRSS_PHY_1326 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_RST_TERM	R/W	4410h	Controls term settings for reset_n pads.

4.4.660 DDRSS_PHY_1327 Register (Offset = 54BCh) [reset = X]

DDRSS_PHY_1327 is shown in [Figure 4-1454](#) and described in [Table 4-2916](#).

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Table 4-2915. DDRSS_PHY_1327 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54BCh

Figure 4-1454. DDRSS_PHY_1327 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_CS_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2916. DDRSS_PHY_1327 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_CS_TERM	R/W	4410h	Controls term settings for cs pads.

4.4.661 DDRSS_PHY_1328 Register (Offset = 54C0h) [reset = X]

DDRSS_PHY_1328 is shown in [Figure 4-1455](#) and described in [Table 4-2918](#).

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Table 4-2917. DDRSS_PHY_1328 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54C0h

Figure 4-1455. DDRSS_PHY_1328 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_ODT_TERM																	
R/W-X														R/W-4410h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2918. DDRSS_PHY_1328 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_ODT_TERM	R/W	4410h	Controls term settings for odt pads.

4.4.662 DDRSS_PHY_1329 Register (Offset = 54C4h) [reset = X]

DDRSS_PHY_1329 is shown in Figure 4-1456 and described in Table 4-2920.

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Table 4-2919. DDRSS_PHY_1329 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54C4h

Figure 4-1456. DDRSS_PHY_1329 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				PHY_ADRCTL_LP3_RX_CAL											
R/W-X				R/W-0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_ADRCTL_RX_CAL									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2920. DDRSS_PHY_1329 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-16	PHY_ADRCTL_LP3_RX_CAL	R/W	0h	PHY CKE/RESET_N RX calibration controls.
15-10	RESERVED	R/W	X	
9-0	PHY_ADRCTL_RX_CAL	R/W	0h	PHY address/control RX calibration controls.

4.4.663 DDRSS_PHY_1330 Register (Offset = 54C8h) [reset = X]

DDRSS_PHY_1330 is shown in [Figure 4-1457](#) and described in [Table 4-2922](#).

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Table 4-2921. DDRSS_PHY_1330 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54C8h

Figure 4-1457. DDRSS_PHY_1330 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CAL_START_0
R/W-X							W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_CAL_CLEAR_0
R/W-X							W-0h
15	14	13	12	11	10	9	8
RESERVED			PHY_CAL_MODE_0				
R/W-X			R/W-0h				
7	6	5	4	3	2	1	0
PHY_CAL_MODE_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2922. DDRSS_PHY_1330 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CAL_START_0	W	0h	Manual start for the pad calibration state machine for block 0. Set to 1 to trigger. WRITE-ONLY
23-17	RESERVED	R/W	X	
16	PHY_CAL_CLEAR_0	W	0h	Clear the pad calibration state machine and results for block 0. Set to 1 to trigger. WRITE-ONLY
15-13	RESERVED	R/W	X	
12-0	PHY_CAL_MODE_0	R/W	0h	Pad calibration mode bits for block 0. Bit (0) disables pad calibration upon initialization. Bit (1) enables automatic interval based calibration. Bits (3:2) set the base interval for the interval counter. Bits (7:4) are direct connections to pad control signals.

4.4.664 DDRSS_PHY_1331 Register (Offset = 54CCh) [reset = 0h]

DDRSS_PHY_1331 is shown in [Figure 4-1458](#) and described in [Table 4-2924](#).

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Table 4-2923. DDRSS_PHY_1331 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54CCh

Figure 4-1458. DDRSS_PHY_1331 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CAL_INTERVAL_COUNT_0																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2924. DDRSS_PHY_1331 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_CAL_INTERVAL_COUNT_0	R/W	0h	Pad calibration interval counter compare value for block 0.

4.4.665 DDRSS_PHY_1332 Register (Offset = 54D0h) [reset = X]

DDRSS_PHY_1332 is shown in [Figure 4-1459](#) and described in [Table 4-2926](#).

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Table 4-2925. DDRSS_PHY_1332 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54D0h

Figure 4-1459. DDRSS_PHY_1332 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED					PHY_LP4_BOOT_CAL_CLK_SELECT_0		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
PHY_CAL_SAMPLE_WAIT_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2926. DDRSS_PHY_1332 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-8	PHY_LP4_BOOT_CAL_CLK_SELECT_0	R/W	0h	Pad calibration pad clock frequency select setting for LPDDR4 boot frequency for block 0.
7-0	PHY_CAL_SAMPLE_WAIT_0	R/W	0h	Pad calibration state machine wait count in pad clock cycles for block 0.

4.4.666 DDRSS_PHY_1333 Register (Offset = 54D4h) [reset = X]

DDRSS_PHY_1333 is shown in [Figure 4-1460](#) and described in [Table 4-2928](#).

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Table 4-2927. DDRSS_PHY_1333 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54D4h

Figure 4-1460. DDRSS_PHY_1333 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CAL_RESULT_OBS_0																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 4-2928. DDRSS_PHY_1333 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	PHY_CAL_RESULT_OBS_0	R	0h	Pad calibration results observation values for block 0. READ-ONLY

4.4.667 DDRSS_PHY_1334 Register (Offset = 54D8h) [reset = X]

DDRSS_PHY_1334 is shown in [Figure 4-1461](#) and described in [Table 4-2930](#).

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Table 4-2929. DDRSS_PHY_1334 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54D8h

Figure 4-1461. DDRSS_PHY_1334 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CAL_RESULT2_OBS_0																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 4-2930. DDRSS_PHY_1334 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	PHY_CAL_RESULT2_OBS_0	R	0h	Pad calibration results (CKE/RESET_N) observation values for block 0. READ-ONLY

4.4.668 DDRSS_PHY_1335 Register (Offset = 54DCh) [reset = X]

DDRSS_PHY_1335 is shown in [Figure 4-1462](#) and described in [Table 4-2932](#).

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Table 4-2931. DDRSS_PHY_1335 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54DCh

Figure 4-1462. DDRSS_PHY_1335 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CAL_RESULT4_OBS_0																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 4-2932. DDRSS_PHY_1335 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	PHY_CAL_RESULT4_OBS_0	R	0h	Pad calibration pass1 shadow results observation values for block 0. READ-ONLY

4.4.669 DDRSS_PHY_1336 Register (Offset = 54E0h) [reset = X]

DDRSS_PHY_1336 is shown in [Figure 4-1463](#) and described in [Table 4-2934](#).

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Table 4-2933. DDRSS_PHY_1336 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54E0h

Figure 4-1463. DDRSS_PHY_1336 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CAL_RESULT5_OBS_0																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 4-2934. DDRSS_PHY_1336 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	PHY_CAL_RESULT5_OBS_0	R	0h	Pad calibration pass2 shadow results observation values for block 0. READ-ONLY

4.4.670 DDRSS_PHY_1337 Register (Offset = 54E4h) [reset = X]

DDRSS_PHY_1337 is shown in [Figure 4-1464](#) and described in [Table 4-2936](#).

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Table 4-2935. DDRSS_PHY_1337 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54E4h

Figure 4-1464. DDRSS_PHY_1337 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CAL_RESULT6_OBS_0																							
R-X								R-0h																							

LEGEND: R = Read Only; -n = value after reset

Table 4-2936. DDRSS_PHY_1337 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-0	PHY_CAL_RESULT6_OBS_0	R	0h	Pad calibration internal results observation delta values for block 0. READ-ONLY

4.4.671 DDRSS_PHY_1338 Register (Offset = 54E8h) [reset = X]

DDRSS_PHY_1338 is shown in [Figure 4-1465](#) and described in [Table 4-2938](#).

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Table 4-2937. DDRSS_PHY_1338 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54E8h

Figure 4-1465. DDRSS_PHY_1338 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESE RVED	PHY_CAL_CPTR_CNT_0							PHY_CAL_RESULT7_OBS_0							
R/W-X	R/W-0h							R-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CAL_RESULT7_OBS_0															
R-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2938. DDRSS_PHY_1338 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PHY_CAL_CPTR_CNT_0	R/W	0h	defines sample capture number in pad calibration process
23-0	PHY_CAL_RESULT7_OBS_0	R	0h	Pad calibration internal results observation delta values for block 0. READ-ONLY

4.4.672 DDRSS_PHY_1339 Register (Offset = 54ECh) [reset = X]

DDRSS_PHY_1339 is shown in [Figure 4-1466](#) and described in [Table 4-2940](#).

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Table 4-2939. DDRSS_PHY_1339 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54ECh

Figure 4-1466. DDRSS_PHY_1339 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_CAL_DBG_CFG_0
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
PHY_CAL_RCV_FINE_ADJ_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_CAL_PD_FINE_ADJ_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_CAL_PU_FINE_ADJ_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2940. DDRSS_PHY_1339 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_CAL_DBG_CFG_0	R/W	0h	defines debug configuration in pad calibration process
23-16	PHY_CAL_RCV_FINE_ADJ_0	R/W	0h	defines adjustment for RCV code in pad calibration process
15-8	PHY_CAL_PD_FINE_ADJ_0	R/W	0h	defines adjustment for PD code in pad calibration process
7-0	PHY_CAL_PU_FINE_ADJ_0	R/W	0h	defines adjustment for PU code in pad calibration process

4.4.673 DDRSS_PHY_1340 Register (Offset = 54F0h) [reset = X]

DDRSS_PHY_1340 is shown in [Figure 4-1467](#) and described in [Table 4-2942](#).

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Table 4-2941. DDRSS_PHY_1340 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54F0h

Figure 4-1467. DDRSS_PHY_1340 Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							SC_PHY_PAD_DBG_CONT_0
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 4-2942. DDRSS_PHY_1340 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	SC_PHY_PAD_DBG_CNT_0	W	0h	Allows the pad calibration state machine to advance (when in debug mode) for slice 0. Set to 1 to trigger. WRITE-ONLY

4.4.674 DDRSS_PHY_1341 Register (Offset = 54F4h) [reset = 0h]

DDRSS_PHY_1341 is shown in [Figure 4-1468](#) and described in [Table 4-2944](#).

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Table 4-2943. DDRSS_PHY_1341 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54F4h

Figure 4-1468. DDRSS_PHY_1341 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CAL_RESULT3_OBS_0																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2944. DDRSS_PHY_1341 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_CAL_RESULT3_OBS_0	R	0h	Pad calibration results first/last0/1 observation values for block 0. READ-ONLY

4.4.675 DDRSS_PHY_1342 Register (Offset = 54F8h) [reset = X]

DDRSS_PHY_1342 is shown in [Figure 4-1469](#) and described in [Table 4-2946](#).

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Table 4-2945. DDRSS_PHY_1342 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54F8h

Figure 4-1469. DDRSS_PHY_1342 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CAL_SLOPE_ADJ_0			
R/W-X				R/W-00041020h			
23	22	21	20	19	18	17	16
PHY_CAL_SLOPE_ADJ_0							
R/W-00041020h							
15	14	13	12	11	10	9	8
PHY_CAL_SLOPE_ADJ_0							
R/W-00041020h							
7	6	5	4	3	2	1	0
RESERVED		PHY_ADRCTL_PVT_MAP_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2946. DDRSS_PHY_1342 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-8	PHY_CAL_SLOPE_ADJ_0	R/W	00041020h	defines slope configure in pad calibration process
7	RESERVED	R/W	X	
6-0	PHY_ADRCTL_PVT_MAP_0	R/W	0h	defines slope configure in pad calibration process

4.4.676 DDRSS_PHY_1343 Register (Offset = 54FCh) [reset = X]

DDRSS_PHY_1343 is shown in [Figure 4-1470](#) and described in [Table 4-2948](#).

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Table 4-2947. DDRSS_PHY_1343 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 54FCh

Figure 4-1470. DDRSS_PHY_1343 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PHY_CAL_SLOPE_ADJ_PASS2_0			
R/W-X												R/W-00041020h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_CAL_SLOPE_ADJ_PASS2_0															
R/W-00041020h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2948. DDRSS_PHY_1343 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_CAL_SLOPE_ADJ_PASS2_0	R/W	00041020h	defines slope configure for pass2 in pad calibration process

4.4.677 DDRSS_PHY_1344 Register (Offset = 5500h) [reset = X]

DDRSS_PHY_1344 is shown in [Figure 4-1471](#) and described in [Table 4-2950](#).

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Table 4-2949. DDRSS_PHY_1344 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5500h

Figure 4-1471. DDRSS_PHY_1344 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PHY_CAL_TWO_PASS_CFG_0																							
R/W-X								R/W-00C98C98h																							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2950. DDRSS_PHY_1344 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-0	PHY_CAL_TWO_PASS_CFG_0	R/W	00C98C98h	defines cal_en configure in pad calibration process

4.4.678 DDRSS_PHY_1345 Register (Offset = 5504h) [reset = X]

DDRSS_PHY_1345 is shown in [Figure 4-1472](#) and described in [Table 4-2952](#).

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Table 4-2951. DDRSS_PHY_1345 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5504h

Figure 4-1472. DDRSS_PHY_1345 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0					
R/W-X		R/W-3Fh					
23	22	21	20	19	18	17	16
RESERVED		PHY_CAL_SW_CAL_CFG_0					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
PHY_CAL_SW_CAL_CFG_0							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_CAL_SW_CAL_CFG_0							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2952. DDRSS_PHY_1345 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_CAL_RANGE_PASS1_PU_MAX_DELTA_0	R/W	3Fh	Pad calibration pass1 pu results won't update if out of max delta range .
23	RESERVED	R/W	X	
22-0	PHY_CAL_SW_CAL_CFG_0	R/W	0h	defines firmware based pad calibration process

4.4.679 DDRSS_PHY_1346 Register (Offset = 5508h) [reset = X]

DDRSS_PHY_1346 is shown in [Figure 4-1473](#) and described in [Table 4-2954](#).

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Table 4-2953. DDRSS_PHY_1346 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5508h

Figure 4-1473. DDRSS_PHY_1346 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0					
R/W-X		R/W-3Fh					
23	22	21	20	19	18	17	16
RESERVED		PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0					
R/W-X		R/W-3Fh					
15	14	13	12	11	10	9	8
RESERVED		PHY_CAL_RANGE_PASS1_RX_MAX_DELTA_0					
R/W-X		R/W-1Fh					
7	6	5	4	3	2	1	0
RESERVED		PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0					
R/W-X		R/W-3Fh					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2954. DDRSS_PHY_1346 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_CAL_RANGE_PASS2_PD_MAX_DELTA_0	R/W	3Fh	Pad calibration pass2 pd results won't update if out of max delta range .
23-22	RESERVED	R/W	X	
21-16	PHY_CAL_RANGE_PASS2_PU_MAX_DELTA_0	R/W	3Fh	Pad calibration pass2 pu results won't update if out of max delta range .
15-13	RESERVED	R/W	X	
12-8	PHY_CAL_RANGE_PASS1_RX_MAX_DELTA_0	R/W	1Fh	Pad calibration pass1 rx results won't update if out of max delta range .
7-6	RESERVED	R/W	X	
5-0	PHY_CAL_RANGE_PASS1_PD_MAX_DELTA_0	R/W	3Fh	Pad calibration pass1 pd results won't update if out of max delta range .

4.4.680 DDRSS_PHY_1347 Register (Offset = 550Ch) [reset = X]

DDRSS_PHY_1347 is shown in Figure 4-1474 and described in Table 4-2956.

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Table 4-2955. DDRSS_PHY_1347 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 550Ch

Figure 4-1474. DDRSS_PHY_1347 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CAL_RANGE_PASS1_RX_MIN_DELTA_0			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				PHY_CAL_RANGE_PASS2_RX_MAX_DELTA_0			
R/W-X				R/W-1Fh			

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2956. DDRSS_PHY_1347 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_CAL_RANGE_PASS1_RX_MIN_DELTA_0	R/W	0h	Pad calibration pass1 rx results won't update if out of min delta range .
23-22	RESERVED	R/W	X	
21-16	PHY_CAL_RANGE_PASS1_PD_MIN_DELTA_0	R/W	0h	Pad calibration pass1 pd results won't update if out of min delta range .
15-14	RESERVED	R/W	X	
13-8	PHY_CAL_RANGE_PASS1_PU_MIN_DELTA_0	R/W	0h	Pad calibration pass1 pu results won't update if out of min delta range .
7-5	RESERVED	R/W	X	
4-0	PHY_CAL_RANGE_PASS2_RX_MAX_DELTA_0	R/W	1Fh	Pad calibration pass2 rx results won't update if out of max delta range .

4.4.681 DDRSS_PHY_1348 Register (Offset = 5510h) [reset = X]

DDRSS_PHY_1348 is shown in [Figure 4-1475](#) and described in [Table 4-2958](#).

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Table 4-2957. DDRSS_PHY_1348 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5510h

Figure 4-1475. DDRSS_PHY_1348 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_CAL_RANGE_PASS2_RX_MIN_DELTA_0			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED		PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2958. DDRSS_PHY_1348 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R/W	X	
20-16	PHY_CAL_RANGE_PASS2_RX_MIN_DELTA_0	R/W	0h	Pad calibration pass2 rx results won't update if out of min delta range .
15-14	RESERVED	R/W	X	
13-8	PHY_CAL_RANGE_PASS2_PD_MIN_DELTA_0	R/W	0h	Pad calibration pass2 pd results won't update if out of min delta range .
7-6	RESERVED	R/W	X	
5-0	PHY_CAL_RANGE_PASS2_PU_MIN_DELTA_0	R/W	0h	Pad calibration pass2 pu results won't update if out of min delta range .

4.4.682 DDRSS_PHY_1349 Register (Offset = 5514h) [reset = X]

DDRSS_PHY_1349 is shown in [Figure 4-1476](#) and described in [Table 4-2960](#).

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Table 4-2959. DDRSS_PHY_1349 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5514h

Figure 4-1476. DDRSS_PHY_1349 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_PARITY_ERROR_REGIF_AC										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PAD_ATB_CTRL															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2960. DDRSS_PHY_1349 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_PARITY_ERROR_REGIF_AC	R/W	0h	Inject parity error to register interface signals for ac slice.
15-0	PHY_PAD_ATB_CTRL	R/W	0h	Pad ATB control settings. Bit (0) is the enable signal. Bits (5:1) are the ATB data signals. Bits (15:8) are the 1 hot select for which pad is selected.

4.4.683 DDRSS_PHY_1350 Register (Offset = 5518h) [reset = X]

DDRSS_PHY_1350 is shown in [Figure 4-1477](#) and described in [Table 4-2962](#).

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Table 4-2961. DDRSS_PHY_1350 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5518h

Figure 4-1477. DDRSS_PHY_1350 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_AC_LPBK_ENABLE	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PHY_AC_LPBK_OBS_SELECT	
R/W-X						R/W-0h	
15	14	13	12	11	10	9	8
RESERVED						PHY_AC_LPBK_ERR_CLEAR	
R/W-X						W-0h	
7	6	5	4	3	2	1	0
RESERVED						PHY_ADRCTL_MANUAL_UPDATE	
R/W-X						W-0h	

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-2962. DDRSS_PHY_1350 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_AC_LPBK_ENABLE	R/W	0h	Loopback enable for the address/control slices.
23-17	RESERVED	R/W	X	
16	PHY_AC_LPBK_OBS_SELECT	R/W	0h	Select value to map an individual loopback address/control slice observation register to the global observation register.
15-9	RESERVED	R/W	X	
8	PHY_AC_LPBK_ERR_CLEAR	W	0h	Address/control loopback error clear. Set to 1 to clear error. WRITE-ONLY
7-1	RESERVED	R/W	X	
0	PHY_ADRCTL_MANUAL_UPDATE	W	0h	Address/control manual update of slave delay lines. Set to 1 to update. WRITE-ONLY

4.4.684 DDRSS_PHY_1351 Register (Offset = 551Ch) [reset = X]

DDRSS_PHY_1351 is shown in Figure 4-1478 and described in Table 4-2964.

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Table 4-2963. DDRSS_PHY_1351 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 551Ch

Figure 4-1478. DDRSS_PHY_1351 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_AC_PRBS_PATTERN_MASK			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED	PHY_AC_PRBS_PATTERN_START						
R/W-X				R/W-1h			
15	14	13	12	11	10	9	8
RESERVED							PHY_AC_LPBK_CONTROL
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_AC_LPBK_CONTROL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2964. DDRSS_PHY_1351 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_AC_PRBS_PATTER N_MASK	R/W	0h	PRBS7 mask signal for address/control slice.
23	RESERVED	R/W	X	
22-16	PHY_AC_PRBS_PATTER N_START	R/W	1h	PRBS7 start pattern for address/control slice.
15-9	RESERVED	R/W	X	
8-0	PHY_AC_LPBK_CONTR OL	R/W	0h	Address/control slice loopback control setting.

4.4.685 DDRSS_PHY_1352 Register (Offset = 5520h) [reset = 0h]

DDRSS_PHY_1352 is shown in [Figure 4-1479](#) and described in [Table 4-2966](#).

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Table 4-2965. DDRSS_PHY_1352 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5520h

Figure 4-1479. DDRSS_PHY_1352 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_AC_LPBK_RESULT_OBS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2966. DDRSS_PHY_1352 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_AC_LPBK_RESULT_OBS	R	0h	Observation register for the loopback address/control slices. READ-ONLY

4.4.686 DDRSS_PHY_1353 Register (Offset = 5524h) [reset = X]

DDRSS_PHY_1353 is shown in Figure 4-1480 and described in Table 4-2968.

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Table 4-2967. DDRSS_PHY_1353 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5524h

Figure 4-1480. DDRSS_PHY_1353 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED		PHY_AC_CLK_LPBK_CONTROL					
R/W-X		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							PHY_AC_CLK_LPBK_ENABLE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_AC_CLK_LPBK_OBS_SELECT
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2968. DDRSS_PHY_1353 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R/W	X	
21-16	PHY_AC_CLK_LPBK_CONTROL	R/W	0h	Mem clk block loopback control setting.
15-9	RESERVED	R/W	X	
8	PHY_AC_CLK_LPBK_ENABLE	R/W	0h	Loopback enable for mem clk blocks.
7-1	RESERVED	R/W	X	
0	PHY_AC_CLK_LPBK_OBS_SELECT	R/W	0h	Select value to map an individual loopback mem clk block observation register to the global observation register.

4.4.687 DDRSS_PHY_1354 Register (Offset = 5528h) [reset = X]

DDRSS_PHY_1354 is shown in [Figure 4-1481](#) and described in [Table 4-2970](#).

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Table 4-2969. DDRSS_PHY_1354 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5528h

Figure 4-1481. DDRSS_PHY_1354 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_TOP_PWR_RDC_DISABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_AC_PWR_RDC_DISABLE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
PHY_AC_CLK_LPBK_RESULT_OBS							
R-0h							
7	6	5	4	3	2	1	0
PHY_AC_CLK_LPBK_RESULT_OBS							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2970. DDRSS_PHY_1354 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_TOP_PWR_RDC_DISABLE	R/W	0h	top param power reduction disable.
23-17	RESERVED	R/W	X	
16	PHY_AC_PWR_RDC_DISABLE	R/W	0h	ac slice power reduction disable.
15-0	PHY_AC_CLK_LPBK_RESULT_OBS	R	0h	Observation register for loopback mem clk blocks. READ-ONLY

4.4.688 DDRSS_PHY_1355 Register (Offset = 552Ch) [reset = X]

DDRSS_PHY_1355 is shown in [Figure 4-1482](#) and described in [Table 4-2972](#).

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Table 4-2971. DDRSS_PHY_1355 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 552Ch

Figure 4-1482. DDRSS_PHY_1355 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PHY_AC_SLV_DLY_CTRL_GATE_DISABLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2972. DDRSS_PHY_1355 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PHY_AC_SLV_DLY_CTRL_GATE_DISABLE	R/W	0h	ac slice slv_dly_control block power reduction disable.

4.4.689 DDRSS_PHY_1356 Register (Offset = 5530h) [reset = 0h]

DDRSS_PHY_1356 is shown in [Figure 4-1483](#) and described in [Table 4-2974](#).

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Table 4-2973. DDRSS_PHY_1356 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5530h

Figure 4-1483. DDRSS_PHY_1356 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DATA_BYTE_ORDER_SEL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2974. DDRSS_PHY_1356 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DATA_BYTE_ORDER_SEL	R/W	0h	Used to define the data slice's byte swap for CA bits 7:0.

4.4.690 DDRSS_PHY_1357 Register (Offset = 5534h) [reset = X]

DDRSS_PHY_1357 is shown in [Figure 4-1484](#) and described in [Table 4-2976](#).

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Table 4-2975. DDRSS_PHY_1357 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5534h

Figure 4-1484. DDRSS_PHY_1357 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_0	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED				PHY_CALVL_DEVICE_MAP			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED						PHY_LPDDR4_CONNECT	
R/W-X						R/W-0h	
7	6	5	4	3	2	1	0
PHY_DATA_BYTE_ORDER_SEL_HIGH							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2976. DDRSS_PHY_1357 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_ADRCTL_MSTR_DLY_ENC_SEL_0	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 0 .
23-21	RESERVED	R/W	X	
20-16	PHY_CALVL_DEVICE_MAP	R/W	0h	Define which device's DQ feedback data bits should be used during CA training
15-9	RESERVED	R/W	X	
8	PHY_LPDDR4_CONNECT	R/W	0h	PHY is connected to LPDDR4 devices
7-0	PHY_DATA_BYTE_ORDER_SEL_HIGH	R/W	0h	Used to define the data slice's byte swap for CA bits 9:8.

4.4.691 DDRSS_PHY_1358 Register (Offset = 5538h) [reset = X]

DDRSS_PHY_1358 is shown in [Figure 4-1485](#) and described in [Table 4-2978](#).

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Table 4-2977. DDRSS_PHY_1358 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5538h

Figure 4-1485. DDRSS_PHY_1358 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PHY_ADRCTL_MSTR_DLY_ENC_SEL_1	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2978. DDRSS_PHY_1358 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	PHY_ADRCTL_MSTR_DLY_ENC_SEL_1	R/W	0h	Select adrctl_mstr_dly_enc for the address/control slice 1 .

4.4.692 DDRSS_PHY_1359 Register (Offset = 553Ch) [reset = 0h]

DDRSS_PHY_1359 is shown in [Figure 4-1486](#) and described in [Table 4-2980](#).

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Table 4-2979. DDRSS_PHY_1359 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 553Ch

Figure 4-1486. DDRSS_PHY_1359 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DDL_AC_ENABLE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2980. DDRSS_PHY_1359 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DDL_AC_ENABLE	R/W	0h	PHY Address/Control DDL BIST mode enable.

4.4.693 DDRSS_PHY_1360 Register (Offset = 5540h) [reset = X]

DDRSS_PHY_1360 is shown in [Figure 4-1487](#) and described in [Table 4-2982](#).

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Table 4-2981. DDRSS_PHY_1360 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5540h

Figure 4-1487. DDRSS_PHY_1360 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_DDL_AC_MODE																									
R/W-X						R/W-0h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2982. DDRSS_PHY_1360 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-0	PHY_DDL_AC_MODE	R/W	0h	PHY Address/Control DDL BIST mode.

4.4.694 DDRSS_PHY_1361 Register (Offset = 5544h) [reset = X]

DDRSS_PHY_1361 is shown in [Figure 4-1488](#) and described in [Table 4-2984](#).

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Table 4-2983. DDRSS_PHY_1361 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5544h

Figure 4-1488. DDRSS_PHY_1361 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_ERR_MASK_EN		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
PHY_DDL_TRACK_UPD_THRESHOLD_AC							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					PHY_INIT_UPDATE_CONFIG		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED		PHY_DDL_AC_MASK					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2984. DDRSS_PHY_1361 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_ERR_MASK_EN	R/W	0h	PHY ERROR information report mask enable.
23-16	PHY_DDL_TRACK_UPD_THRESHOLD_AC	R/W	0h	Specify threshold value for PHY init update tracking for AC slice.
15-11	RESERVED	R/W	X	
10-8	PHY_INIT_UPDATE_CONFIG	R/W	0h	PHY init update function configuration.
7-6	RESERVED	R/W	X	
5-0	PHY_DDL_AC_MASK	R/W	0h	PHY Address/Control DDL BIST mask.

4.4.695 DDRSS_PHY_1362 Register (Offset = 5548h) [reset = X]

DDRSS_PHY_1362 is shown in [Figure 4-1489](#) and described in [Table 4-2986](#).

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Table 4-2985. DDRSS_PHY_1362 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5548h

Figure 4-1489. DDRSS_PHY_1362 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					PHY_ERR_STATUS		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2986. DDRSS_PHY_1362 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	PHY_ERR_STATUS	R/W	0h	PHY ERROR information.

4.4.696 DDRSS_PHY_1363 Register (Offset = 554Ch) [reset = 0h]

DDRSS_PHY_1363 is shown in [Figure 4-1490](#) and described in [Table 4-2988](#).

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Table 4-2987. DDRSS_PHY_1363 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 554Ch

Figure 4-1490. DDRSS_PHY_1363 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DS0_DQS_ERR_COUNTER																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2988. DDRSS_PHY_1363 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DS0_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 0 DQS ERROR counter.

4.4.697 DDRSS_PHY_1364 Register (Offset = 5550h) [reset = 0h]

DDRSS_PHY_1364 is shown in [Figure 4-1491](#) and described in [Table 4-2990](#).

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Table 4-2989. DDRSS_PHY_1364 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5550h

Figure 4-1491. DDRSS_PHY_1364 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DS1_DQS_ERR_COUNTER																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2990. DDRSS_PHY_1364 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DS1_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 1 DQS ERROR counter.

4.4.698 DDRSS_PHY_1365 Register (Offset = 5554h) [reset = 0h]

DDRSS_PHY_1365 is shown in [Figure 4-1492](#) and described in [Table 4-2992](#).

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Table 4-2991. DDRSS_PHY_1365 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5554h

Figure 4-1492. DDRSS_PHY_1365 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DS2_DQS_ERR_COUNTER																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2992. DDRSS_PHY_1365 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DS2_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 2 DQS ERROR counter.

4.4.699 DDRSS_PHY_1366 Register (Offset = 5558h) [reset = 0h]

DDRSS_PHY_1366 is shown in [Figure 4-1493](#) and described in [Table 4-2994](#).

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Table 4-2993. DDRSS_PHY_1366 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5558h

Figure 4-1493. DDRSS_PHY_1366 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_DS3_DQS_ERR_COUNTER																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 4-2994. DDRSS_PHY_1366 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_DS3_DQS_ERR_COUNTER	R	0h	PHY DATA SLICE 3 DQS ERROR counter.

4.4.700 DDRSS_PHY_1367 Register (Offset = 555Ch) [reset = X]

DDRSS_PHY_1367 is shown in Figure 4-1494 and described in Table 4-2996.

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Table 4-2995. DDRSS_PHY_1367 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 555Ch

Figure 4-1494. DDRSS_PHY_1367 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_DS_INIT_COMPLETE_OBS			
R/W-X				R-0h			
23	22	21	20	19	18	17	16
RESERVED						PHY_AC_INIT_COMPLETE_OBS	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
PHY_AC_INIT_COMPLETE_OBS							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						PHY_DLL_RST_EN	
R/W-X						R/W-2h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-2996. DDRSS_PHY_1367 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_DS_INIT_COMPLETE_OBS	R	0h	Observation register for dfi_init_complete for data slice. Bit0 is for data_slice0 bit1 is for data_slice 1,... READ-ONLY.
23-18	RESERVED	R/W	X	
17-8	PHY_AC_INIT_COMPLETE_OBS	R	0h	Observation register for dfi_init_complete for adr and ac slice. Bit 0 is for dfi_init_complete for all slices. Bit(7:4) is for adr slice, bit4 is adr_slice0..., if the adr slice number is 3, bit7 is 0. Bit8 is for ac_slice0 bit9 is for ac_slice 1,... READ-ONLY.
7-2	RESERVED	R/W	X	
1-0	PHY_DLL_RST_EN	R/W	2h	PHY DDL reset software interface enable.

4.4.701 DDRSS_PHY_1368 Register (Offset = 5560h) [reset = X]

DDRSS_PHY_1368 is shown in Figure 4-1495 and described in Table 4-2998.

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Table 4-2997. DDRSS_PHY_1368 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5560h

Figure 4-1495. DDRSS_PHY_1368 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_GRP_SHIFT_OBS_SELECT		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_GRP_SLV_DLY_ENC_OBS_SELECT		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							PHY_AC_DCC_RXCAL_CTRL_GATE_DISABLE
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							PHY_UPDATE_MASK
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-2998. DDRSS_PHY_1368 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_GRP_SHIFT_OBS_SELECT	R/W	0h	Select value to map an individual address/control group slice automatic cycle/half_cycle shift settings to the observation register.
23-20	RESERVED	R/W	X	
19-16	PHY_GRP_SLV_DLY_ENC_OBS_SELECT	R/W	0h	Select value to map an individual address/control group slice slave delay to the encoded value observation register.
15-9	RESERVED	R/W	X	
8	PHY_AC_DCC_RXCAL_CTRL_GATE_DISABLE	R/W	0h	Memory clock bit slice DCC block power reduction disable.
7-1	RESERVED	R/W	X	
0	PHY_UPDATE_MASK	R/W	0h	Control to disable the generation of dfi_phyupd_req and use of dfi_ctrlupd_req. If this is 0 the PHY is normal mode if this is 1, the PHY will not respond to dfi_ctrlupd_req or not to send dfi_phyupd_req

4.4.702 DDRSS_PHY_1369 Register (Offset = 5564h) [reset = X]

DDRSS_PHY_1369 is shown in [Figure 4-1496](#) and described in [Table 4-3000](#).

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Table 4-2999. DDRSS_PHY_1369 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5564h

Figure 4-1496. DDRSS_PHY_1369 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_GRP_SHIFT_OBS			
R-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_GRP_SLV_DLY_ENC_OBS			
R-X				R-0h			
7	6	5	4	3	2	1	0
PHY_GRP_SLV_DLY_ENC_OBS							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 4-3000. DDRSS_PHY_1369 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	X	
18-16	PHY_GRP_SHIFT_OBS	R	0h	Observation register for the address/control group automatic half cycle and cycle shift values. READ-ONLY
15-11	RESERVED	R	X	
10-0	PHY_GRP_SLV_DLY_ENC_OBS	R	0h	Observation register for all address/control group slice slave delay encoded values. READ-ONLY

4.4.703 DDRSS_PHY_1370 Register (Offset = 5568h) [reset = X]

DDRSS_PHY_1370 is shown in [Figure 4-1497](#) and described in [Table 4-3002](#).

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Table 4-3001. DDRSS_PHY_1370 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5568h

Figure 4-1497. DDRSS_PHY_1370 Register

31	30	29	28	27	26	25	24
RESERVED					PHY_PLL_LOCK_DEASSERT_MASK		
R/W-X					R/W-0h		
23	22	21	20	19	18	17	16
RESERVED					PHY_PARITY_ERROR_REGIF_PS		
R/W-X					R/W-0h		
15	14	13	12	11	10	9	8
PHY_PARITY_ERROR_REGIF_PS							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED							PHY_PARITY_ERROR_INJECTION_ENABLE
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3002. DDRSS_PHY_1370 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	PHY_PLL_LOCK_DEASSERT_MASK	R/W	0h	PLL Lock de-assert Mask.
23-19	RESERVED	R/W	X	
18-8	PHY_PARITY_ERROR_REGIF_PS	R/W	0h	Injects parity error to register interface signals in param_split.
7-1	RESERVED	R/W	X	
0	PHY_PARITY_ERROR_INJECTION_ENABLE	R/W	0h	Enable parity error injection. When enabled, a register write will never update any registers but instead inject a parity error to the register.

4.4.704 DDRSS_PHY_1371 Register (Offset = 556Ch) [reset = X]

DDRSS_PHY_1371 is shown in Figure 4-1498 and described in Table 4-3004.

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Table 4-3003. DDRSS_PHY_1371 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 556Ch

Figure 4-1498. DDRSS_PHY_1371 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	SC_PHY_PARITY_ERROR_INFO_WOCLR						
R/W-X	W-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_PARITY_ERROR_INFO_MASK						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	PHY_PARITY_ERROR_INFO						
R/W-X	R-0h						

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3004. DDRSS_PHY_1371 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R/W	X	
22-16	SC_PHY_PARITY_ERROR_INFO_WOCLR	W	0h	Parity Error Info. WRITE-ONLY
15	RESERVED	R/W	X	
14-8	PHY_PARITY_ERROR_INFO_MASK	R/W	0h	Parity Error Info Mask.
7	RESERVED	R/W	X	
6-0	PHY_PARITY_ERROR_INFO	R	0h	Parity Error Info. READ-ONLY

4.4.705 DDRSS_PHY_1372 Register (Offset = 5570h) [reset = X]

DDRSS_PHY_1372 is shown in [Figure 4-1499](#) and described in [Table 4-3006](#).

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Table 4-3005. DDRSS_PHY_1372 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5570h

Figure 4-1499. DDRSS_PHY_1372 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_TIMEOUT_ERROR_INFO_MASK					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
PHY_TIMEOUT_ERROR_INFO_MASK							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_TIMEOUT_ERROR_INFO					
R/W-X		R-0h					
7	6	5	4	3	2	1	0
PHY_TIMEOUT_ERROR_INFO							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-3006. DDRSS_PHY_1372 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_TIMEOUT_ERROR_INFO_MASK	R/W	0h	Timeout Error Info Mask.
15-14	RESERVED	R/W	X	
13-0	PHY_TIMEOUT_ERROR_INFO	R	0h	Timeout Error Info. READ-ONLY

4.4.706 DDRSS_PHY_1373 Register (Offset = 5574h) [reset = X]

DDRSS_PHY_1373 is shown in [Figure 4-1500](#) and described in [Table 4-3008](#).

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Table 4-3007. DDRSS_PHY_1373 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5574h

Figure 4-1500. DDRSS_PHY_1373 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_PLL_FREQUENCY_ERROR_MASK					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
RESERVED				PHY_PLL_FREQUENCY_ERROR			
R/W-X				R-0h			
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_TIMEOUT_ERROR_INFO_WOCLR					
R/W-X		W-0h					
7	6	5	4	3	2	1	0
SC_PHY_TIMEOUT_ERROR_INFO_WOCLR							
W-0h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3008. DDRSS_PHY_1373 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-24	PHY_PLL_FREQUENCY_ERROR_MASK	R/W	0h	PLL Frequency Error Info Mask.
23-20	RESERVED	R/W	X	
19-16	PHY_PLL_FREQUENCY_ERROR	R	0h	PLL Frequency Error Info. READ-ONLY
15-14	RESERVED	R/W	X	
13-0	SC_PHY_TIMEOUT_ERROR_INFO_WOCLR	W	0h	Timeout Error Info. WRITE-ONLY

4.4.707 DDRSS_PHY_1374 Register (Offset = 5578h) [reset = X]

DDRSS_PHY_1374 is shown in [Figure 4-1501](#) and described in [Table 4-3010](#).

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Table 4-3009. DDRSS_PHY_1374 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5578h

Figure 4-1501. DDRSS_PHY_1374 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED				PHY_PLL_DSKEWCALOUT_MIN			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PHY_PLL_DSKEWCALOUT_MIN							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		SC_PHY_PLL_FREQUENCY_ERROR_WOCLR					
R/W-X		W-0h					

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3010. DDRSS_PHY_1374 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-8	PHY_PLL_DSKEWCALOUT_MIN	R/W	0h	PLL DSKEWCALOUT threshold min value.
7-6	RESERVED	R/W	X	
5-0	SC_PHY_PLL_FREQUENCY_ERROR_WOCLR	W	0h	PLL_Frequency Error Info. WRITE-ONLY

4.4.708 DDRSS_PHY_1375 Register (Offset = 557Ch) [reset = X]

DDRSS_PHY_1375 is shown in [Figure 4-1502](#) and described in [Table 4-3012](#).

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Table 4-3011. DDRSS_PHY_1375 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 557Ch

Figure 4-1502. DDRSS_PHY_1375 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_PLL_DSKEWCALOUT_ERROR_INFO_MASK	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PHY_PLL_DSKEWCALOUT_ERROR_INFO	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED				PHY_PLL_DSKEWCALOUT_MAX			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_PLL_DSKEWCALOUT_MAX							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-3012. DDRSS_PHY_1375 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_PLL_DSKEWCALOUT_ERROR_INFO_MASK	R/W	0h	PLL DSKEWCALOUT threshold Error Info Mask.
23-18	RESERVED	R/W	X	
17-16	PHY_PLL_DSKEWCALOUT_ERROR_INFO	R	0h	PLL DSKEWCALOUT threshold Error Info. READ-ONLY
15-12	RESERVED	R/W	X	
11-0	PHY_PLL_DSKEWCALOUT_MAX	R/W	0h	PLL DSKEWCALOUT threshold max value.

4.4.709 DDRSS_PHY_1376 Register (Offset = 5580h) [reset = X]

DDRSS_PHY_1376 is shown in Figure 4-1503 and described in Table 4-3014.

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Table 4-3013. DDRSS_PHY_1376 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5580h

Figure 4-1503. DDRSS_PHY_1376 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_TOP_FSM_ERROR_INFO
R/W-X							R-0h
15	14	13	12	11	10	9	8
PHY_TOP_FSM_ERROR_INFO							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SC_PHY_PLL_DSKEWCALOUT_ERROR_INFO_WOCLR	
R/W-X						W-0h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3014. DDRSS_PHY_1376 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16-8	PHY_TOP_FSM_ERROR_INFO	R	0h	Top level FSM Error Info. READ-ONLY
7-2	RESERVED	R/W	X	
1-0	SC_PHY_PLL_DSKEWCALOUT_ERROR_INFO_WOCLR	W	0h	PLL DSKEWCALOUT threshold Error Info. WRITE-ONLY

4.4.710 DDRSS_PHY_1377 Register (Offset = 5584h) [reset = X]

DDRSS_PHY_1377 is shown in [Figure 4-1504](#) and described in [Table 4-3016](#).

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Table 4-3015. DDRSS_PHY_1377 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5584h

Figure 4-1504. DDRSS_PHY_1377 Register

31	30	29	28	27	26	25	24
RESERVED							SC_PHY_TOP_FSM_ERROR_INFO_WOCLR
R/W-X							W-0h
23	22	21	20	19	18	17	16
SC_PHY_TOP_FSM_ERROR_INFO_WOCLR							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							PHY_TOP_FSM_ERROR_INFO_MASK
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_TOP_FSM_ERROR_INFO_MASK							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3016. DDRSS_PHY_1377 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24-16	SC_PHY_TOP_FSM_ERROR_INFO_WOCLR	W	0h	Top level FSM Error Info. WRITE-ONLY
15-9	RESERVED	R/W	X	
8-0	PHY_TOP_FSM_ERROR_INFO_MASK	R/W	0h	Top level FSM Error Info Mask.

4.4.711 DDRSS_PHY_1378 Register (Offset = 5588h) [reset = X]

DDRSS_PHY_1378 is shown in [Figure 4-1505](#) and described in [Table 4-3018](#).

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Table 4-3017. DDRSS_PHY_1378 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5588h

Figure 4-1505. DDRSS_PHY_1378 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_FSM_TRANSIENT_ERROR_INFO_MASK	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
PHY_FSM_TRANSIENT_ERROR_INFO_MASK							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED						PHY_FSM_TRANSIENT_ERROR_INFO	
R/W-X						R-0h	
7	6	5	4	3	2	1	0
PHY_FSM_TRANSIENT_ERROR_INFO							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-3018. DDRSS_PHY_1378 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	PHY_FSM_TRANSIENT_ERROR_INFO_MASK	R/W	0h	Accumulated Top level FSM Error Info Mask.
15-10	RESERVED	R/W	X	
9-0	PHY_FSM_TRANSIENT_ERROR_INFO	R	0h	Accumulated Top level FSM Error Info. READ-ONLY

4.4.712 DDRSS_PHY_1379 Register (Offset = 558Ch) [reset = X]

DDRSS_PHY_1379 is shown in Figure 4-1506 and described in Table 4-3020.

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Table 4-3019. DDRSS_PHY_1379 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 558Ch

Figure 4-1506. DDRSS_PHY_1379 Register

31	30	29	28	27	26	25	24
RESERVED						PHY_TOP_TRAIN_CALIB_ERROR_INFO_MASK	
R/W-X						R/W-0h	
23	22	21	20	19	18	17	16
RESERVED						PHY_TOP_TRAIN_CALIB_ERROR_INFO	
R/W-X						R-0h	
15	14	13	12	11	10	9	8
RESERVED						SC_PHY_FSM_TRANSIENT_ERROR_INFO_WOCLR	
R/W-X						W-0h	
7	6	5	4	3	2	1	0
SC_PHY_FSM_TRANSIENT_ERROR_INFO_WOCLR							
W-0h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3020. DDRSS_PHY_1379 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-24	PHY_TOP_TRAIN_CALIB_ERROR_INFO_MASK	R/W	0h	Training/Calibration Error Info Mask for TOP.
23-18	RESERVED	R/W	X	
17-16	PHY_TOP_TRAIN_CALIB_ERROR_INFO	R	0h	Training/Calibration Error Info for TOP. READ-ONLY
15-10	RESERVED	R/W	X	
9-0	SC_PHY_FSM_TRANSIENT_ERROR_INFO_WOCLR	W	0h	Accumulated Top level FSM Error Info. WRITE-ONLY

4.4.713 DDRSS_PHY_1380 Register (Offset = 5590h) [reset = X]

DDRSS_PHY_1380 is shown in [Figure 4-1507](#) and described in [Table 4-3022](#).

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Table 4-3021. DDRSS_PHY_1380 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5590h

Figure 4-1507. DDRSS_PHY_1380 Register

31	30	29	28	27	26	25	24
RESERVED	SC_PHY_TRAIN_CALIB_ERROR_INFO_WOCLR						
R/W-X	W-0h						
23	22	21	20	19	18	17	16
RESERVED	PHY_TRAIN_CALIB_ERROR_INFO_MASK						
R/W-X	R/W-0h						
15	14	13	12	11	10	9	8
RESERVED	PHY_TRAIN_CALIB_ERROR_INFO						
R/W-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED						SC_PHY_TOP_TRAIN_CALIB_ERROR_INFO_WOCLR	
R/W-X						W-0h	

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3022. DDRSS_PHY_1380 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	SC_PHY_TRAIN_CALIB_ERROR_INFO_WOCLR	W	0h	Training/Calibration Error Info. WRITE-ONLY
23	RESERVED	R/W	X	
22-16	PHY_TRAIN_CALIB_ERROR_INFO_MASK	R/W	0h	Training/Calibration Error Info Mask.
15	RESERVED	R/W	X	
14-8	PHY_TRAIN_CALIB_ERROR_INFO	R	0h	Training/Calibration Error Info. READ-ONLY
7-2	RESERVED	R/W	X	
1-0	SC_PHY_TOP_TRAIN_CALIB_ERROR_INFO_WOCLR	W	0h	Training/Calibration Error Info for TOP. WRITE-ONLY

4.4.714 DDRSS_PHY_1381 Register (Offset = 5594h) [reset = X]

DDRSS_PHY_1381 is shown in [Figure 4-1508](#) and described in [Table 4-3024](#).

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Table 4-3023. DDRSS_PHY_1381 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5594h

Figure 4-1508. DDRSS_PHY_1381 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		PHY_GLOBAL_ERROR_INFO_MASK					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
RESERVED		PHY_GLOBAL_ERROR_INFO					
R/W-X		R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-3024. DDRSS_PHY_1381 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	PHY_GLOBAL_ERROR_INFO_MASK	R/W	0h	Global Error Info Mask.
7-6	RESERVED	R/W	X	
5-0	PHY_GLOBAL_ERROR_INFO	R	0h	Global Error Info. READ-ONLY

4.4.715 DDRSS_PHY_1382 Register (Offset = 5598h) [reset = X]

DDRSS_PHY_1382 is shown in [Figure 4-1509](#) and described in [Table 4-3026](#).

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Table 4-3025. DDRSS_PHY_1382 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5598h

Figure 4-1509. DDRSS_PHY_1382 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PHY_TRAINING_TIMEOUT_VALUE			
R/W-X												R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_TRAINING_TIMEOUT_VALUE															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3026. DDRSS_PHY_1382 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_TRAINING_TIMEOUT_VALUE	R/W	0h	Training timeout value.

4.4.716 DDRSS_PHY_1383 Register (Offset = 559Ch) [reset = X]

DDRSS_PHY_1383 is shown in [Figure 4-1510](#) and described in [Table 4-3028](#).

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Table 4-3027. DDRSS_PHY_1383 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 559Ch

Figure 4-1510. DDRSS_PHY_1383 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												PHY_INIT_TIMEOUT_VALUE			
R/W-X												R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_INIT_TIMEOUT_VALUE															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3028. DDRSS_PHY_1383 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-0	PHY_INIT_TIMEOUT_VALUE	R/W	0h	Init or DFS timeout value.

4.4.717 DDRSS_PHY_1384 Register (Offset = 55A0h) [reset = X]

DDRSS_PHY_1384 is shown in [Figure 4-1511](#) and described in [Table 4-3030](#).

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Table 4-3029. DDRSS_PHY_1384 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55A0h

Figure 4-1511. DDRSS_PHY_1384 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_LP_TIMEOUT_VALUE															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3030. DDRSS_PHY_1384 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PHY_LP_TIMEOUT_VALUE	R/W	0h	DFI LP timeout value.

4.4.718 DDRSS_PHY_1385 Register (Offset = 55A4h) [reset = 0h]

DDRSS_PHY_1385 is shown in [Figure 4-1512](#) and described in [Table 4-3032](#).

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Table 4-3031. DDRSS_PHY_1385 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55A4h

Figure 4-1512. DDRSS_PHY_1385 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PHYUPD_TIMEOUT_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3032. DDRSS_PHY_1385 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_PHYUPD_TIMEOUT_VALUE	R/W	0h	DFI PHYUPD timeout value.

4.4.719 DDRSS_PHY_1386 Register (Offset = 55A8h) [reset = X]

DDRSS_PHY_1386 is shown in [Figure 4-1513](#) and described in [Table 4-3034](#).

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Table 4-3033. DDRSS_PHY_1386 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55A8h

Figure 4-1513. DDRSS_PHY_1386 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PLL_LOCK_0_MIN_VALUE			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_PHYMSTR_TIMEOUT_VALUE			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
PHY_PHYMSTR_TIMEOUT_VALUE							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_PHYMSTR_TIMEOUT_VALUE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3034. DDRSS_PHY_1386 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R/W	X	
28-24	PHY_PLL_LOCK_0_MIN_VALUE	R/W	0h	PLL min timeout value.
23-20	RESERVED	R/W	X	
19-0	PHY_PHYMSTR_TIMEOUT_VALUE	R/W	0h	DFI PHYMSTR timeout value.

4.4.720 DDRSS_PHY_1387 Register (Offset = 55ACh) [reset = X]

DDRSS_PHY_1387 is shown in [Figure 4-1514](#) and described in [Table 4-3036](#).

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Table 4-3035. DDRSS_PHY_1387 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55ACh

Figure 4-1514. DDRSS_PHY_1387 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_PLL_FREQUENCY_DELTA			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
PHY_RDDATA_VALID_TIMEOUT_VALUE							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_PLL_LOCK_TIMEOUT_VALUE							
R/W-0h							
7	6	5	4	3	2	1	0
PHY_PLL_LOCK_TIMEOUT_VALUE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3036. DDRSS_PHY_1387 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_PLL_FREQUENCY_DELTA	R/W	0h	Acceptable PLL frequency delta.
23-16	PHY_RDDATA_VALID_TIMEOUT_VALUE	R/W	0h	RDDATA VALID timeout value.
15-0	PHY_PLL_LOCK_TIMEOUT_VALUE	R/W	0h	PLL max timeout value.

4.4.721 DDRSS_PHY_1388 Register (Offset = 55B0h) [reset = X]

DDRSS_PHY_1388 is shown in [Figure 4-1515](#) and described in [Table 4-3038](#).

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Table 4-3037. DDRSS_PHY_1388 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55B0h

Figure 4-1515. DDRSS_PHY_1388 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			PHY_ADRCTL_FSM_ERROR_INFO_0												
R/W-X			R-0h												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PLL_FREQUENCY_COMPARE_INTERVAL															
R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-3038. DDRSS_PHY_1388 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_ADRCTL_FSM_ERROR_INFO_0	R	0h	ADRCTL slice level FSM Error Info. READ-ONLY
15-0	PHY_PLL_FREQUENCY_COMPARE_INTERVAL	R/W	0h	PLL Frequency compare interval.

4.4.722 DDRSS_PHY_1389 Register (Offset = 55B4h) [reset = X]

DDRSS_PHY_1389 is shown in [Figure 4-1516](#) and described in [Table 4-3040](#).

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Table 4-3039. DDRSS_PHY_1389 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55B4h

Figure 4-1516. DDRSS_PHY_1389 Register

31	30	29	28	27	26	25	24
RESERVED		SC_PHY_ADRCTL_FSM_ERROR_INFO_WOCLR_0					
R/W-X		W-0h					
23	22	21	20	19	18	17	16
SC_PHY_ADRCTL_FSM_ERROR_INFO_WOCLR_0							
W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_ADRCTL_FSM_ERROR_INFO_MASK_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
PHY_ADRCTL_FSM_ERROR_INFO_MASK_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3040. DDRSS_PHY_1389 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	SC_PHY_ADRCTL_FSM_ERROR_INFO_WOCLR_0	W	0h	ADRCTL Slice level FSM Error Info. WRITE-ONLY
15-14	RESERVED	R/W	X	
13-0	PHY_ADRCTL_FSM_ERROR_INFO_MASK_0	R/W	0h	ADRCTL Slice level FSM Error Info Mask.

4.4.723 DDRSS_PHY_1390 Register (Offset = 55B8h) [reset = X]

DDRSS_PHY_1390 is shown in [Figure 4-1517](#) and described in [Table 4-3042](#).

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Table 4-3041. DDRSS_PHY_1390 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55B8h

Figure 4-1517. DDRSS_PHY_1390 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_ADRCTL_FSM_ERROR_INFO_MASK_1					
R/W-X		R/W-0h					
23	22	21	20	19	18	17	16
PHY_ADRCTL_FSM_ERROR_INFO_MASK_1							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_ADRCTL_FSM_ERROR_INFO_1					
R/W-X		R-0h					
7	6	5	4	3	2	1	0
PHY_ADRCTL_FSM_ERROR_INFO_1							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-3042. DDRSS_PHY_1390 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_ADRCTL_FSM_ERROR_INFO_MASK_1	R/W	0h	ADRCTL Slice level FSM Error Info Mask.
15-14	RESERVED	R/W	X	
13-0	PHY_ADRCTL_FSM_ERROR_INFO_1	R	0h	ADRCTL slice level FSM Error Info. READ-ONLY

4.4.724 DDRSS_PHY_1391 Register (Offset = 55BCh) [reset = X]

DDRSS_PHY_1391 is shown in [Figure 4-1518](#) and described in [Table 4-3044](#).

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Table 4-3043. DDRSS_PHY_1391 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55BCh

Figure 4-1518. DDRSS_PHY_1391 Register

31	30	29	28	27	26	25	24
RESERVED		PHY_MEMCLK_FSM_ERROR_INFO_0					
R/W-X		R-0h					
23	22	21	20	19	18	17	16
PHY_MEMCLK_FSM_ERROR_INFO_0							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		SC_PHY_ADRCTL_FSM_ERROR_INFO_WOCLR_1					
R/W-X		W-0h					
7	6	5	4	3	2	1	0
SC_PHY_ADRCTL_FSM_ERROR_INFO_WOCLR_1							
W-0h							

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3044. DDRSS_PHY_1391 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	PHY_MEMCLK_FSM_ERROR_INFO_0	R	0h	MEMCLK slice level FSM Error Info. READ-ONLY
15-14	RESERVED	R/W	X	
13-0	SC_PHY_ADRCTL_FSM_ERROR_INFO_WOCLR_1	W	0h	ADRCTL Slice level FSM Error Info. WRITE-ONLY

4.4.725 DDRSS_PHY_1392 Register (Offset = 55C0h) [reset = X]

DDRSS_PHY_1392 is shown in [Figure 4-1519](#) and described in [Table 4-3046](#).

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Table 4-3045. DDRSS_PHY_1392 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55C0h

Figure 4-1519. DDRSS_PHY_1392 Register

31	30	29	28	27	26	25	24
RESERVED		SC_PHY_MEMCLK_FSM_ERROR_INFO_WOCLR_0					
R/W-X		W-0h					
23	22	21	20	19	18	17	16
SC_PHY_MEMCLK_FSM_ERROR_INFO_WOCLR_0							
W-0h							
15	14	13	12	11	10	9	8
RESERVED		PHY_MEMCLK_FSM_ERROR_INFO_MASK_0					
R/W-X		R/W-0h					
7	6	5	4	3	2	1	0
PHY_MEMCLK_FSM_ERROR_INFO_MASK_0							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 4-3046. DDRSS_PHY_1392 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-16	SC_PHY_MEMCLK_FSM_ERROR_INFO_WOCLR_0	W	0h	MEMCLK Slice level FSM Error Info. WRITE-ONLY
15-14	RESERVED	R/W	X	
13-0	PHY_MEMCLK_FSM_ERROR_INFO_MASK_0	R/W	0h	MEMCLK Slice level FSM Error Info Mask.

4.4.726 DDRSS_PHY_1393 Register (Offset = 55C4h) [reset = X]

DDRSS_PHY_1393 is shown in [Figure 4-1520](#) and described in [Table 4-3048](#).

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Table 4-3047. DDRSS_PHY_1393 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55C4h

Figure 4-1520. DDRSS_PHY_1393 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													PHY_PAD_CAL_IO_CFG_0		
R/W-X													R/W-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PAD_CAL_IO_CFG_0															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3048. DDRSS_PHY_1393 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_CAL_IO_CFG_0	R/W	0h	Pad calibration Controls PCLK/PARK pin and vref switch.

4.4.727 DDRSS_PHY_1394 Register (Offset = 55C8h) [reset = X]

DDRSS_PHY_1394 is shown in [Figure 4-1521](#) and described in [Table 4-3050](#).

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Table 4-3049. DDRSS_PHY_1394 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55C8h

Figure 4-1521. DDRSS_PHY_1394 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PHY_PAD_ACS_IO_CFG													
R/W-X		R/W-0h													

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3050. DDRSS_PHY_1394 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-0	PHY_PAD_ACS_IO_CFG	R/W	0h	Controls PCLK/PARK pin for acs pad.

4.4.728 DDRSS_PHY_1395 Register (Offset = 55CCh) [reset = X]

DDRSS_PHY_1395 is shown in [Figure 4-1522](#) and described in [Table 4-3052](#).

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Table 4-3051. DDRSS_PHY_1395 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55CCh

Figure 4-1522. DDRSS_PHY_1395 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PHY_PLL_BYPASS
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3052. DDRSS_PHY_1395 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PHY_PLL_BYPASS	R/W	0h	PHY clock PLL bypass select.

4.4.729 DDRSS_PHY_1396 Register (Offset = 55D0h) [reset = X]

DDRSS_PHY_1396 is shown in Figure 4-1523 and described in Table 4-3054.

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Table 4-3053. DDRSS_PHY_1396 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55D0h

Figure 4-1523. DDRSS_PHY_1396 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							PHY_LOW_FREQ_SEL
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				PHY_PLL_CTRL			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_PLL_CTRL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3054. DDRSS_PHY_1396 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	PHY_LOW_FREQ_SEL	R/W	0h	Enables the PHY to enter/exit the PLL domain from the negative clock edge. Set to 1 at low frequencies to enable.
15-13	RESERVED	R/W	X	
12-0	PHY_PLL_CTRL	R/W	0h	PHY clock PLL controls.

4.4.730 DDRSS_PHY_1397 Register (Offset = 55D4h) [reset = X]

DDRSS_PHY_1397 is shown in Figure 4-1524 and described in Table 4-3056.

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Table 4-3055. DDRSS_PHY_1397 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55D4h

Figure 4-1524. DDRSS_PHY_1397 Register

31	30	29	28	27	26	25	24
RESERVED				PHY_CSLVL_DLY_STEP			
R/W-X				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				PHY_CSLVL_CAPTURE_CNT			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				PHY_PAD_VREF_CTRL_AC			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
PHY_PAD_VREF_CTRL_AC							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3056. DDRSS_PHY_1397 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-24	PHY_CSLVL_DLY_STEP	R/W	0h	Sets the delay step size plus 1 during CS training.
23-20	RESERVED	R/W	X	
19-16	PHY_CSLVL_CAPTURE_CNT	R/W	0h	Defines the number of samples to take at each GRP slave delay setting during CS training.
15-12	RESERVED	R/W	X	
11-0	PHY_PAD_VREF_CTRL_AC	R/W	0h	Pad VREF control settings for the address/control.

4.4.731 DDRSS_PHY_1398 Register (Offset = 55D8h) [reset = X]

DDRSS_PHY_1398 is shown in Figure 4-1525 and described in Table 4-3058.

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Table 4-3057. DDRSS_PHY_1398 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55D8h

Figure 4-1525. DDRSS_PHY_1398 Register

31	30	29	28	27	26	25	24
RESERVED							PHY_LVL_MEAS_DLY_STEP_ENABLE
R/W-X							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							PHY_SW_CSLVL_DVW_MIN_EN
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							PHY_SW_CSLVL_DVW_MIN
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
PHY_SW_CSLVL_DVW_MIN							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3058. DDRSS_PHY_1398 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	PHY_LVL_MEAS_DLY_STEP_ENABLE	R/W	0h	Enables the phy_adr_meas_dly_step_value to be used instead of the phy_cslvl_dly_step parameter.
23-17	RESERVED	R/W	X	
16	PHY_SW_CSLVL_DVW_MIN_EN	R/W	0h	Enables the software override data valid window size during CS training.
15-9	RESERVED	R/W	X	
8-0	PHY_SW_CSLVL_DVW_MIN	R/W	0h	Sets the software override data valid window size during CS training.

4.4.732 DDRSS_PHY_1399 Register (Offset = 55DCh) [reset = X]

DDRSS_PHY_1399 is shown in [Figure 4-1526](#) and described in [Table 4-3060](#).

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Table 4-3059. DDRSS_PHY_1399 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55DCh

Figure 4-1526. DDRSS_PHY_1399 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_GRP1_SLAVE_DELAY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_GRP0_SLAVE_DELAY_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3060. DDRSS_PHY_1399 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_GRP1_SLAVE_DELAY_0	R/W	0h	Address slice slave delay setting for address slice 1.
15-11	RESERVED	R/W	X	
10-0	PHY_GRP0_SLAVE_DELAY_0	R/W	0h	Address slice slave delay setting for address slice 0.

4.4.733 DDRSS_PHY_1400 Register (Offset = 55E0h) [reset = X]

DDRSS_PHY_1400 is shown in [Figure 4-1527](#) and described in [Table 4-3062](#).

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Table 4-3061. DDRSS_PHY_1400 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55E0h

Figure 4-1527. DDRSS_PHY_1400 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					PHY_GRP3_SLAVE_DELAY_0										
R/W-X					R/W-0h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_GRP2_SLAVE_DELAY_0										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3062. DDRSS_PHY_1400 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-16	PHY_GRP3_SLAVE_DELAY_0	R/W	0h	Address slice slave delay setting for address slice 3.
15-11	RESERVED	R/W	X	
10-0	PHY_GRP2_SLAVE_DELAY_0	R/W	0h	Address slice slave delay setting for address slice 2.

4.4.734 DDRSS_PHY_1401 Register (Offset = 55E4h) [reset = X]

DDRSS_PHY_1401 is shown in [Figure 4-1528](#) and described in [Table 4-3064](#).

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Table 4-3063. DDRSS_PHY_1401 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55E4h

Figure 4-1528. DDRSS_PHY_1401 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_GRP0_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3064. DDRSS_PHY_1401 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	PHY_GRP0_SLAVE_DELAY_1	R/W	0h	Address slice slave delay setting for address slice 0.

4.4.735 DDRSS_PHY_1402 Register (Offset = 55E8h) [reset = X]

DDRSS_PHY_1402 is shown in [Figure 4-1529](#) and described in [Table 4-3066](#).

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Table 4-3065. DDRSS_PHY_1402 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55E8h

Figure 4-1529. DDRSS_PHY_1402 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_GRP1_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3066. DDRSS_PHY_1402 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	PHY_GRP1_SLAVE_DELAY_1	R/W	0h	Address slice slave delay setting for address slice 1.

4.4.736 DDRSS_PHY_1403 Register (Offset = 55ECh) [reset = X]

DDRSS_PHY_1403 is shown in [Figure 4-1530](#) and described in [Table 4-3068](#).

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Table 4-3067. DDRSS_PHY_1403 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55ECh

Figure 4-1530. DDRSS_PHY_1403 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_GRP2_SLAVE_DELAY_1										
R/W-X					R/W-0h										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3068. DDRSS_PHY_1403 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	PHY_GRP2_SLAVE_DELAY_1	R/W	0h	Address slice slave delay setting for address slice 2.

4.4.737 DDRSS_PHY_1404 Register (Offset = 55F0h) [reset = X]

DDRSS_PHY_1404 is shown in [Figure 4-1531](#) and described in [Table 4-3070](#).

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Table 4-3069. DDRSS_PHY_1404 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55F0h

Figure 4-1531. DDRSS_PHY_1404 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_GRP3_SLAVE_DELAY_1									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3070. DDRSS_PHY_1404 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10-0	PHY_GRP3_SLAVE_DELAY_1	R/W	0h	Address slice slave delay setting for address slice 3.

4.4.738 DDRSS_PHY_1405 Register (Offset = 55F4h) [reset = X]

DDRSS_PHY_1405 is shown in [Figure 4-1532](#) and described in [Table 4-3072](#).

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Table 4-3071. DDRSS_PHY_1405 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55F4h

Figure 4-1532. DDRSS_PHY_1405 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					PHY_CLK_DC_CAL_CLK_SEL		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3072. DDRSS_PHY_1405 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	PHY_CLK_DC_CAL_CLK_SEL	R/W	0h	Determines DCC CAL clock.

4.4.739 DDRSS_PHY_1406 Register (Offset = 55F8h) [reset = X]

DDRSS_PHY_1406 is shown in [Figure 4-1533](#) and described in [Table 4-3074](#).

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Table 4-3073. DDRSS_PHY_1406 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55F8h

Figure 4-1533. DDRSS_PHY_1406 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE																															
RVED																															
R/W-X																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3074. DDRSS_PHY_1406 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PHY_PAD_FDBK_DRIVE	R/W	FFh	Controls drive settings for gate feedback pads.

4.4.740 DDRSS_PHY_1407 Register (Offset = 55FCh) [reset = X]

DDRSS_PHY_1407 is shown in [Figure 4-1534](#) and described in [Table 4-3076](#).

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Table 4-3075. DDRSS_PHY_1407 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 55FCh

Figure 4-1534. DDRSS_PHY_1407 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														PHY_PAD_FDBK_DRIVE2	
R/W-X														R/W-FFh	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PAD_FDBK_DRIVE2															
R/W-FFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3076. DDRSS_PHY_1407 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_FDBK_DRIVE2	R/W	FFh	Controls drive settings (enslice/boost) for gate feedback pads.

4.4.741 DDRSS_PHY_1408 Register (Offset = 5600h) [reset = X]

DDRSS_PHY_1408 is shown in [Figure 4-1535](#) and described in [Table 4-3078](#).

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Table 4-3077. DDRSS_PHY_1408 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5600h

Figure 4-1535. DDRSS_PHY_1408 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RE	PHY_PAD_DATA_DRIVE																														
SE																															
RV																															
ED																															
R/ W- X	R/W-0h																														

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3078. DDRSS_PHY_1408 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-0	PHY_PAD_DATA_DRIVE	R/W	0h	Controls drive settings for data pads.

4.4.742 DDRSS_PHY_1409 Register (Offset = 5604h) [reset = 0h]

DDRSS_PHY_1409 is shown in [Figure 4-1536](#) and described in [Table 4-3080](#).

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Table 4-3079. DDRSS_PHY_1409 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5604h

Figure 4-1536. DDRSS_PHY_1409 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PAD_DQS_DRIVE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3080. DDRSS_PHY_1409 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_PAD_DQS_DRIVE	R/W	0h	Controls drive settings for dqs pads.

4.4.743 DDRSS_PHY_1410 Register (Offset = 5608h) [reset = X]

DDRSS_PHY_1410 is shown in [Figure 4-1537](#) and described in [Table 4-3082](#).

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Table 4-3081. DDRSS_PHY_1410 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5608h

Figure 4-1537. DDRSS_PHY_1410 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE																															
RVED																															
R/W-X																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3082. DDRSS_PHY_1410 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PHY_PAD_ADDR_DRIVE	R/W	FFh	Controls drive settings for the address/control pads.

4.4.744 DDRSS_PHY_1411 Register (Offset = 560Ch) [reset = X]

DDRSS_PHY_1411 is shown in [Figure 4-1538](#) and described in [Table 4-3084](#).

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Table 4-3083. DDRSS_PHY_1411 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 560Ch

Figure 4-1538. DDRSS_PHY_1411 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_PAD_ADDR_DRIVE2																									
R/W-X						R/W-00FFFF00h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3084. DDRSS_PHY_1411 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	PHY_PAD_ADDR_DRIVE2	R/W	00FFFF00h	Controls drive settings for the address/control pads.

4.4.745 DDRSS_PHY_1412 Register (Offset = 5610h) [reset = FFh]

DDRSS_PHY_1412 is shown in [Figure 4-1539](#) and described in [Table 4-3086](#).

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Table 4-3085. DDRSS_PHY_1412 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5610h

Figure 4-1539. DDRSS_PHY_1412 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_PAD_CLK_DRIVE																															
R/W-FFh																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3086. DDRSS_PHY_1412 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHY_PAD_CLK_DRIVE	R/W	FFh	Controls drive settings for clock pads.

4.4.746 DDRSS_PHY_1413 Register (Offset = 5614h) [reset = X]

DDRSS_PHY_1413 is shown in [Figure 4-1540](#) and described in [Table 4-3088](#).

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Table 4-3087. DDRSS_PHY_1413 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5614h

Figure 4-1540. DDRSS_PHY_1413 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														PHY_PAD_CLK_DRIVE2																	
R/W-X														R/W-FFh																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3088. DDRSS_PHY_1413 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R/W	X	
17-0	PHY_PAD_CLK_DRIVE2	R/W	FFh	Controls drive settings for clock pads.

4.4.747 DDRSS_PHY_1414 Register (Offset = 5618h) [reset = X]

DDRSS_PHY_1414 is shown in [Figure 4-1541](#) and described in [Table 4-3090](#).

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Table 4-3089. DDRSS_PHY_1414 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5618h

Figure 4-1541. DDRSS_PHY_1414 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE																															
RVED																															
R/W-X																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3090. DDRSS_PHY_1414 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PHY_PAD_CKE_DRIVE	R/W	FFh	Controls drive settings for cke pads.

4.4.748 DDRSS_PHY_1415 Register (Offset = 561Ch) [reset = X]

DDRSS_PHY_1415 is shown in [Figure 4-1542](#) and described in [Table 4-3092](#).

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Table 4-3091. DDRSS_PHY_1415 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 561Ch

Figure 4-1542. DDRSS_PHY_1415 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_PAD_CKE_DRIVE2																									
R/W-X						R/W-01FFFF00h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3092. DDRSS_PHY_1415 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	PHY_PAD_CKE_DRIVE2	R/W	01FFFF00h	Controls drive settings for cke pads.

4.4.749 DDRSS_PHY_1416 Register (Offset = 5620h) [reset = X]

DDRSS_PHY_1416 is shown in [Figure 4-1543](#) and described in [Table 4-3094](#).

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Table 4-3093. DDRSS_PHY_1416 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5620h

Figure 4-1543. DDRSS_PHY_1416 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE																															
RVED																															
R/W-X																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3094. DDRSS_PHY_1416 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PHY_PAD_RST_DRIVE	R/W	FFh	Controls drive settings for reset_n pads.

4.4.750 DDRSS_PHY_1417 Register (Offset = 5624h) [reset = X]

DDRSS_PHY_1417 is shown in [Figure 4-1544](#) and described in [Table 4-3096](#).

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Table 4-3095. DDRSS_PHY_1417 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5624h

Figure 4-1544. DDRSS_PHY_1417 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					PHY_PAD_RST_DRIVE2																										
R/W-X					R/W-01FFFF00h																										

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3096. DDRSS_PHY_1417 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	PHY_PAD_RST_DRIVE2	R/W	01FFFF00h	Controls drive settings for reset_n pads.

4.4.751 DDRSS_PHY_1418 Register (Offset = 5628h) [reset = X]

DDRSS_PHY_1418 is shown in [Figure 4-1545](#) and described in [Table 4-3098](#).

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Table 4-3097. DDRSS_PHY_1418 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5628h

Figure 4-1545. DDRSS_PHY_1418 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE																															
RVED																															
R/W-X																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3098. DDRSS_PHY_1418 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PHY_PAD_CS_DRIVE	R/W	FFh	Controls drive settings for cs pads.

4.4.752 DDRSS_PHY_1419 Register (Offset = 562Ch) [reset = X]

DDRSS_PHY_1419 is shown in [Figure 4-1546](#) and described in [Table 4-3100](#).

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Table 4-3099. DDRSS_PHY_1419 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 562Ch

Figure 4-1546. DDRSS_PHY_1419 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_PAD_CS_DRIVE2																									
R/W-X						R/W-01FFFF00h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3100. DDRSS_PHY_1419 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	PHY_PAD_CS_DRIVE2	R/W	01FFFF00h	Controls drive settings for cs pads.

4.4.753 DDRSS_PHY_1420 Register (Offset = 5630h) [reset = X]

DDRSS_PHY_1420 is shown in [Figure 4-1547](#) and described in [Table 4-3102](#).

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Table 4-3101. DDRSS_PHY_1420 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5630h

Figure 4-1547. DDRSS_PHY_1420 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESE																															
RVED																															
R/W-X																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3102. DDRSS_PHY_1420 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-0	PHY_PAD_ODT_DRIVE	R/W	FFh	Controls drive settings for odt pads.

4.4.754 DDRSS_PHY_1421 Register (Offset = 5634h) [reset = X]

DDRSS_PHY_1421 is shown in [Figure 4-1548](#) and described in [Table 4-3104](#).

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Table 4-3103. DDRSS_PHY_1421 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5634h

Figure 4-1548. DDRSS_PHY_1421 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						PHY_PAD_ODT_DRIVE2																									
R/W-X						R/W-01FFFF00h																									

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3104. DDRSS_PHY_1421 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-0	PHY_PAD_ODT_DRIVE2	R/W	01FFFF00h	Controls drive settings for odt pads.

4.4.755 DDRSS_PHY_1422 Register (Offset = 5638h) [reset = X]

DDRSS_PHY_1422 is shown in [Figure 4-1549](#) and described in [Table 4-3106](#).

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Table 4-3105. DDRSS_PHY_1422 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CTL_CFG_PHY	0299 5638h

Figure 4-1549. DDRSS_PHY_1422 Register

31	30	29	28	27	26	25	24
RESERVED	PHY_CAL_SETTLING_PRD_0						
R/W-X	R/W-0h						
23	22	21	20	19	18	17	16
PHY_CAL_VREF_SWITCH_TIMER_0							
R/W-0h							
15	14	13	12	11	10	9	8
PHY_CAL_VREF_SWITCH_TIMER_0							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED					PHY_CAL_CLK_SELECT_0		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3106. DDRSS_PHY_1422 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-24	PHY_CAL_SETTLING_PRD_0	R/W	0h	Number of clock cycles to extend dfi_phyupd_req after the ack is received for settling of final values
23-8	PHY_CAL_VREF_SWITCH_TIMER_0	R/W	0h	The settling time for a switch in VREF during IO pad calibration.
7-3	RESERVED	R/W	X	
2-0	PHY_CAL_CLK_SELECT_0	R/W	0h	Pad calibration pad clock frequency select setting for block 0.

4.5 DDRSS0_ECC_AGGR_CFG Registers

Table 4-3108 lists the memory-mapped registers for the DDRSS0_ECC_AGGR_CFG. All register offset addresses not listed in Table 4-3108 should be considered as reserved locations and the register contents should not be modified.

Table 4-3107. DDRSS0_ECC_AGGR_CFG Instances

Instance	Base Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0800h

Table 4-3108. DDRSS0_ECC_AGGR_CFG Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_EC C_AGGR_CFG Physical Address
0h	DDRSS_REV	Aggregator Revision Register	4D200B 0800h
8h	DDRSS_VECTOR	ECC Vector Register	4D200B 0808h
Ch	DDRSS_STAT	Misc Status	4D200B 080Ch
10h + formula	DDRSS_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4D200B 0810h + formula
3Ch	DDRSS_SEC_EOI_REG	EOI Register	4D200B 083Ch
40h	DDRSS_SEC_STATUS_REG0	Interrupt Status Register 0	4D200B 0840h
80h	DDRSS_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4D200B 0880h
C0h	DDRSS_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4D200B 08C0h
13Ch	DDRSS_DED_EOI_REG	EOI Register	4D200B 093Ch
140h	DDRSS_DED_STATUS_REG0	Interrupt Status Register 0	4D200B 0940h
180h	DDRSS_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4D200B 0980h
1C0h	DDRSS_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4D200B 09C0h
200h	DDRSS_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4D200B 0A00h
204h	DDRSS_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4D200B 0A04h
208h	DDRSS_AGGR_STATUS_SET	AGGR interrupt status set Register	4D200B 0A08h
20Ch	DDRSS_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4D200B 0A0Ch

4.5.1 DDRSS_REV Register (Offset = 0h) [reset = 66A0EA00h]

DDRSS_REV is shown in [Figure 4-1550](#) and described in [Table 4-3110](#).

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Table 4-3109. DDRSS_REV Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0800h

Figure 4-1550. DDRSS_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-3110. DDRSS_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

4.5.2 DDRSS_VECTOR Register (Offset = 8h) [reset = X]

DDRSS_VECTOR is shown in [Figure 4-1551](#) and described in [Table 4-3112](#).

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ECC Vector Register

Table 4-3111. DDRSS_VECTOR Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0808h

Figure 4-1551. DDRSS_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3112. DDRSS_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

4.5.3 DDRSS_STAT Register (Offset = Ch) [reset = X]

DDRSS_STAT is shown in [Figure 4-1552](#) and described in [Table 4-3114](#).

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Misc Status

Table 4-3113. DDRSS_STAT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGREGATOR_CFG	4D200B 080Ch

Figure 4-1552. DDRSS_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
RESERVED																					NUM_RAM															
R-X																					R-7h															

LEGEND: R = Read Only; -n = value after reset

Table 4-3114. DDRSS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAM	R	7h	Indicates the number of RAMS serviced by the ECC aggregator

4.5.4 DDRSS_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

DDRSS_RESERVED_SVBUS_y is shown in [Figure 4-1553](#) and described in [Table 4-3116](#).

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 4-3115. DDRSS_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0810h + formula

Figure 4-1553. DDRSS_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3116. DDRSS_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

4.5.5 DDRSS_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

DDRSS_SEC_EOI_REG is shown in [Figure 4-1554](#) and described in [Table 4-3118](#).

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-3117. DDRSS_SEC_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 083Ch

Figure 4-1554. DDRSS_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3118. DDRSS_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.5.6 DDRSS_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

DDRSS_SEC_STATUS_REG0 is shown in Figure 4-1555 and described in Table 4-3120.

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Interrupt Status Register 0

**Table 4-3119. DDRSS_SEC_STATUS_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0840h

Figure 4-1555. DDRSS_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_PEND	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_PEND	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_INT_CBASS_INT_CFG_GBUSECC_PEND	DST_M2P_DST_BUSECC_PEND	DST_M2P_SRC_BUSECC_PEND	M2M_M2M_VB_USS_PEND	M2M_DST_VB_USS_PEND
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3120. DDRSS_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_src_busecc_pend
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_edc_ctrl_busecc_pend

Table 4-3120. DDRSS_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDR32SS_16FFC_EW_D V_WRAP_DDRSS_BRCT L_SC_CBASS_CFG_GCL K_EDC_CTRL_CBASS_I NT_CFG_GBUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_cfg_gclk_edc_ct rl_cbass_int_cfg_gbusecc_pend
3	DST_M2P_DST_BUSECC _PEND	R/W1S	0h	Interrupt Pending Status for dst_m2p_dst_busecc_pend
2	DST_M2P_SRC_BUSECC _PEND	R/W1S	0h	Interrupt Pending Status for dst_m2p_src_busecc_pend
1	M2M_M2M_VBUSS_PEN D	R/W1S	0h	Interrupt Pending Status for m2m_m2m_vbuss_pend
0	M2M_DST_VBUSS_PEN D	R/W1S	0h	Interrupt Pending Status for m2m_dst_vbuss_pend

4.5.7 DDRSS_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

DDRSS_SEC_ENABLE_SET_REG0 is shown in [Figure 4-1556](#) and described in [Table 4-3122](#).

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Interrupt Enable Set Register 0

**Table 4-3121. DDRSS_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0880h

Figure 4-1556. DDRSS_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_INT_CFG_GBUSECC_ENABLE_SET	DST_M2P_DST_BUSECC_ENABLE_SET	DST_M2P_SRC_BUSECC_ENABLE_SET	M2M_M2M_VB_USS_ENABLE_SET	M2M_DST_VB_USS_ENABLE_SET
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3122. DDRSS_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_src_busecc_pend
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_edc_ctrl_busecc_pend

Table 4-3122. DDRSS_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CFG_GCLK_EDC_CTRL_CBASS_INTERRUPT_CFG_GBUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_cfg_gclk_edc_ctrl_cbass_int_cfg_gbusecc_pend
3	DST_M2P_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dst_m2p_dst_busecc_pend
2	DST_M2P_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dst_m2p_src_busecc_pend
1	M2M_M2M_VBUSS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for m2m_m2m_vbuss_pend
0	M2M_DST_VBUSS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for m2m_dst_vbuss_pend

4.5.8 DDRSS_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

DDRSS_SEC_ENABLE_CLR_REG0 is shown in [Figure 4-1557](#) and described in [Table 4-3124](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

**Table 4-3123. DDRSS_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 08C0h

Figure 4-1557. DDRSS_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_INT_CBASS_INT_CFG_GBUSECC_ENABLE_CLR	DST_M2P_DST_BUSECC_ENABLE_CLR	DST_M2P_SRC_BUSECC_ENABLE_CLR	M2M_M2M_VB_USS_ENABLE_CLR	M2M_DST_VB_USS_ENABLE_CLR
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3124. DDRSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_src_busecc_pend
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_edc_ctrl_busecc_pend

Table 4-3124. DDRSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CFG_GCLK_EDC_CTRL_CBASS_INTERRUPT_CFG_GBUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_cfg_gclk_edc_ctrl_cbass_int_cfg_gbusecc_pend
3	DST_M2P_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dst_m2p_dst_busecc_pend
2	DST_M2P_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dst_m2p_src_busecc_pend
1	M2M_M2M_VBUSS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for m2m_m2m_vbuss_pend
0	M2M_DST_VBUSS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for m2m_dst_vbuss_pend

4.5.9 DDRSS_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

DDRSS_DED_EOI_REG is shown in [Figure 4-1558](#) and described in [Table 4-3126](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-3125. DDRSS_DED_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 093Ch

Figure 4-1558. DDRSS_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3126. DDRSS_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.5.10 DDRSS_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

DDRSS_DED_STATUS_REG0 is shown in [Figure 4-1559](#) and described in [Table 4-3128](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 4-3127. DDRSS_DED_STATUS_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0940h

Figure 4-1559. DDRSS_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_PEND	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_PEND	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_INT_CFG_GBUSECC_PEND	DST_M2P_DST_BUSECC_PEND	DST_M2P_SRC_BUSECC_PEND	M2M_M2M_VB_USS_PEND	M2M_DST_VB_USS_PEND
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3128. DDRSS_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_src_busecc_pend
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_edc_ctrl_busecc_pend

Table 4-3128. DDRSS_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDR32SS_16FFC_EW_D V_WRAP_DDRSS_BRCT L_SC_CBASS_CFG_GCL K_EDC_CTRL_CBASS_I NT_CFG_GBUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_cfg_gclk_edc_ct rl_cbass_int_cfg_gbusecc_pend
3	DST_M2P_DST_BUSECC _PEND	R/W1S	0h	Interrupt Pending Status for dst_m2p_dst_busecc_pend
2	DST_M2P_SRC_BUSECC _PEND	R/W1S	0h	Interrupt Pending Status for dst_m2p_src_busecc_pend
1	M2M_M2M_VBUSS_PEN D	R/W1S	0h	Interrupt Pending Status for m2m_m2m_vbuss_pend
0	M2M_DST_VBUSS_PEN D	R/W1S	0h	Interrupt Pending Status for m2m_dst_vbuss_pend

4.5.11 DDRSS_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

DDRSS_DED_ENABLE_SET_REG0 is shown in Figure 4-1560 and described in Table 4-3130.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 4-3129. DDRSS_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0980h

Figure 4-1560. DDRSS_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_INT_CFG_GBUSECC_ENABLE_SET	DST_M2P_DST_BUSECC_ENABLE_SET	DST_M2P_SRC_BUSECC_ENABLE_SET	M2M_M2M_VB_USS_ENABLE_SET	M2M_DST_VB_USS_ENABLE_SET
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3130. DDRSS_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_src_busecc_pend
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_edc_ctrl_busecc_pend

Table 4-3130. DDRSS_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CFG_GCLK_EDC_CTRL_CBASS_INTERRUPT_CFG_GBUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_cfg_gclk_edc_ctrl_cbass_int_cfg_gbusecc_pend
3	DST_M2P_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dst_m2p_dst_busecc_pend
2	DST_M2P_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dst_m2p_src_busecc_pend
1	M2M_M2M_VBUSS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for m2m_m2m_vbuss_pend
0	M2M_DST_VBUSS_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for m2m_dst_vbuss_pend

4.5.12 DDRSS_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

DDRSS_DED_ENABLE_CLR_REG0 is shown in Figure 4-1561 and described in Table 4-3132.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 4-3131. DDRSS_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 09C0h

Figure 4-1561. DDRSS_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_INT_CFG_GBUSECC_ENABLE_CLR	DST_M2P_DST_BUSECC_ENABLE_CLR	DST_M2P_SRC_BUSECC_ENABLE_CLR	M2M_M2M_VB_USS_ENABLE_CLR	M2M_DST_VB_USS_ENABLE_CLR
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3132. DDRSS_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_src_busecc_pend
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_scr_scr_edc_ctrl_busecc_pend

Table 4-3132. DDRSS_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CFG_GCLK_EDC_CTRL_CBASS_INTERRUPT_CFG_GBUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_cfg_gclk_edc_ctrl_cbass_int_cfg_gbusecc_pend
3	DST_M2P_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dst_m2p_dst_busecc_pend
2	DST_M2P_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dst_m2p_src_busecc_pend
1	M2M_M2M_VBUSS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for m2m_m2m_vbuss_pend
0	M2M_DST_VBUSS_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for m2m_dst_vbuss_pend

4.5.13 DDRSS_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

DDRSS_AGGR_ENABLE_SET is shown in [Figure 4-1562](#) and described in [Table 4-3134](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 4-3133. DDRSS_AGGR_ENABLE_SET Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0A00h

Figure 4-1562. DDRSS_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3134. DDRSS_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

4.5.14 DDRSS_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

DDRSS_AGGR_ENABLE_CLR is shown in [Figure 4-1563](#) and described in [Table 4-3136](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

**Table 4-3135. DDRSS_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0A04h

Figure 4-1563. DDRSS_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3136. DDRSS_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

4.5.15 DDRSS_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

DDRSS_AGGR_STATUS_SET is shown in [Figure 4-1564](#) and described in [Table 4-3138](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

**Table 4-3137. DDRSS_AGGR_STATUS_SET
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0A08h

Figure 4-1564. DDRSS_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 4-3138. DDRSS_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

4.5.16 DDRSS_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

DDRSS_AGGR_STATUS_CLR is shown in [Figure 4-1565](#) and described in [Table 4-3140](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

**Table 4-3139. DDRSS_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CFG	4D200B 0A0Ch

Figure 4-1565. DDRSS_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 4-3140. DDRSS_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

4.6 DDRSS0_ECC_AGGR_CTL Registers

Table 4-3142 lists the memory-mapped registers for the DDRSS0_ECC_AGGR_CTL. All register offset addresses not listed in Table 4-3142 should be considered as reserved locations and the register contents should not be modified.

Table 4-3141. DDRSS0_ECC_AGGR_CTL Instances

Instance	Base Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0000h

Table 4-3142. DDRSS0_ECC_AGGR_CTL Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_EC C_AGGR_CTL Physical Address
0h	DDRSS_REV	Aggregator Revision Register	4D200B 0000h
8h	DDRSS_VECTOR	ECC Vector Register	4D200B 0008h
Ch	DDRSS_STAT	Misc Status	4D200B 000Ch
10h + formula	DDRSS_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4D200B 0010h + formula
3Ch	DDRSS_SEC_EOI_REG	EOI Register	4D200B 003Ch
40h	DDRSS_SEC_STATUS_REG0	Interrupt Status Register 0	4D200B 0040h
80h	DDRSS_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4D200B 0080h
C0h	DDRSS_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4D200B 00C0h
13Ch	DDRSS_DED_EOI_REG	EOI Register	4D200B 013Ch
140h	DDRSS_DED_STATUS_REG0	Interrupt Status Register 0	4D200B 0140h
180h	DDRSS_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4D200B 0180h
1C0h	DDRSS_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4D200B 01C0h
200h	DDRSS_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4D200B 0200h
204h	DDRSS_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4D200B 0204h
208h	DDRSS_AGGR_STATUS_SET	AGGR interrupt status set Register	4D200B 0208h
20Ch	DDRSS_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4D200B 020Ch

4.6.1 DDRSS_REV Register (Offset = 0h) [reset = 66A0EA00h]

DDRSS_REV is shown in [Figure 4-1566](#) and described in [Table 4-3144](#).

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Revision parameters

Table 4-3143. DDRSS_REV Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0000h

Figure 4-1566. DDRSS_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-3144. DDRSS_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

4.6.2 DDRSS_VECTOR Register (Offset = 8h) [reset = X]

DDRSS_VECTOR is shown in [Figure 4-1567](#) and described in [Table 4-3146](#).

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ECC Vector Register

Table 4-3145. DDRSS_VECTOR Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0008h

Figure 4-1567. DDRSS_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3146. DDRSS_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

4.6.3 DDRSS_STAT Register (Offset = Ch) [reset = X]

DDRSS_STAT is shown in [Figure 4-1568](#) and described in [Table 4-3148](#).

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Misc Status

Table 4-3147. DDRSS_STAT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGREGATOR_CTL	4D200B 000Ch

Figure 4-1568. DDRSS_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					NUM_RAMs																
R-X																					R-6h																

LEGEND: R = Read Only; -n = value after reset

Table 4-3148. DDRSS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAM	R	6h	Indicates the number of RAMS serviced by the ECC aggregator

4.6.4 DDRSS_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

DDRSS_RESERVED_SVBUS_y is shown in [Figure 4-1569](#) and described in [Table 4-3150](#).

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 4-3149. DDRSS_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0010h + formula

Figure 4-1569. DDRSS_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3150. DDRSS_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

4.6.5 DDRSS_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

DDRSS_SEC_EOI_REG is shown in [Figure 4-1570](#) and described in [Table 4-3152](#).

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-3151. DDRSS_SEC_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 003Ch

Figure 4-1570. DDRSS_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3152. DDRSS_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.6.6 DDRSS_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

DDRSS_SEC_STATUS_REG0 is shown in Figure 4-1571 and described in Table 4-3154.

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Interrupt Status Register 0

**Table 4-3153. DDRSS_SEC_STATUS_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0040h

Figure 4-1571. DDRSS_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_PEND	V2A_EDC_CTRL_PEND	ASAFE_3_SI_PEND	ASAFE_2_SI_PEND	ASAFE_1_SI_PEND	ASAFE_0_SI_PEND
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3154. DDRSS_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_dst_busecc_pend
4	V2A_EDC_CTRL_PEND	R/W1S	0h	Interrupt Pending Status for v2a_edc_ctrl_pend
3	ASAFE_3_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_3_si_pend
2	ASAFE_2_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_2_si_pend
1	ASAFE_1_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_1_si_pend
0	ASAFE_0_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_0_si_pend

4.6.7 DDRSS_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

DDRSS_SEC_ENABLE_SET_REG0 is shown in [Figure 4-1572](#) and described in [Table 4-3156](#).

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Interrupt Enable Set Register 0

**Table 4-3155. DDRSS_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0080h

Figure 4-1572. DDRSS_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	V2A_EDC_CTRL_ENABLE_SET	ASAFE_3_SI_ENABLE_SET	ASAFE_2_SI_ENABLE_SET	ASAFE_1_SI_ENABLE_SET	ASAFE_0_SI_ENABLE_SET	
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3156. DDRSS_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_dst_busecc_pend
4	V2A_EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for v2a_edc_ctrl_pend
3	ASAFE_3_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_3_si_pend
2	ASAFE_2_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_2_si_pend
1	ASAFE_1_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_1_si_pend

Table 4-3156. DDRSS_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASAFE_0_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_0_si_pend

4.6.8 DDRSS_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

DDRSS_SEC_ENABLE_CLR_REG0 is shown in [Figure 4-1573](#) and described in [Table 4-3158](#).

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Interrupt Enable Clear Register 0

**Table 4-3157. DDRSS_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 00C0h

Figure 4-1573. DDRSS_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	V2A_EDC_CTRL_ENABLE_CLR	ASAFE_3_SI_ENABLE_CLR	ASAFE_2_SI_ENABLE_CLR	ASAFE_1_SI_ENABLE_CLR	ASAFE_0_SI_ENABLE_CLR	
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3158. DDRSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_dst_busecc_pend
4	V2A_EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for v2a_edc_ctrl_pend
3	ASAFE_3_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_3_si_pend
2	ASAFE_2_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_2_si_pend
1	ASAFE_1_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_1_si_pend

Table 4-3158. DDRSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASAFE_0_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_0_si_pend

4.6.9 DDRSS_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

DDRSS_DED_EOI_REG is shown in [Figure 4-1574](#) and described in [Table 4-3160](#).

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-3159. DDRSS_DED_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 013Ch

Figure 4-1574. DDRSS_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3160. DDRSS_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.6.10 DDRSS_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

DDRSS_DED_STATUS_REG0 is shown in [Figure 4-1575](#) and described in [Table 4-3162](#).

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Interrupt Status Register 0

**Table 4-3161. DDRSS_DED_STATUS_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0140h

Figure 4-1575. DDRSS_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED		DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_PEND	V2A_EDC_CTRL_PEND	ASAFE_3_SI_PEND	ASAFE_2_SI_PEND	ASAFE_1_SI_PEND	ASAFE_0_SI_PEND
R/W-X		R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3162. DDRSS_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_dst_busecc_pend
4	V2A_EDC_CTRL_PEND	R/W1S	0h	Interrupt Pending Status for v2a_edc_ctrl_pend
3	ASAFE_3_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_3_si_pend
2	ASAFE_2_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_2_si_pend
1	ASAFE_1_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_1_si_pend
0	ASAFE_0_SI_PEND	R/W1S	0h	Interrupt Pending Status for asafe_0_si_pend

4.6.11 DDRSS_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

DDRSS_DED_ENABLE_SET_REG0 is shown in Figure 4-1576 and described in Table 4-3164.

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Interrupt Enable Set Register 0

**Table 4-3163. DDRSS_DED_ENABLE_SET_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0180h

Figure 4-1576. DDRSS_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	V2A_EDC_CTRL_ENABLE_SET	ASAFE_3_SI_ENABLE_SET	ASAFE_2_SI_ENABLE_SET	ASAFE_1_SI_ENABLE_SET	ASAFE_0_SI_ENABLE_SET	
R/W-X	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3164. DDRSS_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_dst_busecc_pend
4	V2A_EDC_CTRL_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for v2a_edc_ctrl_pend
3	ASAFE_3_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_3_si_pend
2	ASAFE_2_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_2_si_pend
1	ASAFE_1_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_1_si_pend

Table 4-3164. DDRSS_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASAFE_0_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for asafe_0_si_pend

4.6.12 DDRSS_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

DDRSS_DED_ENABLE_CLR_REG0 is shown in Figure 4-1577 and described in Table 4-3166.

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Interrupt Enable Clear Register 0

**Table 4-3165. DDRSS_DED_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 01C0h

Figure 4-1577. DDRSS_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	DDR32SS_16FC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	V2A_EDC_CTRL_ENABLE_CLR	ASAFE_3_SI_ENABLE_CLR	ASAFE_2_SI_ENABLE_CLR	ASAFE_1_SI_ENABLE_CLR	ASAFE_0_SI_ENABLE_CLR	
R/W-X	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3166. DDRSS_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R/W	X	
5	DDR32SS_16FFC_EW_DV_WRAP_DDRSS_BRCTL_SC_CBASS_CTL_CFG_P2P_BRIDGE_CTL_CFG_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ddr32ss_16ffc_ew_dv_wrap_ddrss_brctl_sc_cbass_ctl_cfg_p2p_bridge_ctl_cfg_bridge_dst_busecc_pend
4	V2A_EDC_CTRL_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for v2a_edc_ctrl_pend
3	ASAFE_3_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_3_si_pend
2	ASAFE_2_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_2_si_pend
1	ASAFE_1_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_1_si_pend

Table 4-3166. DDRSS_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ASAFE_0_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for asafe_0_si_pend

4.6.13 DDRSS_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

DDRSS_AGGR_ENABLE_SET is shown in [Figure 4-1578](#) and described in [Table 4-3168](#).

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AGGR interrupt enable set Register

**Table 4-3167. DDRSS_AGGR_ENABLE_SET
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0200h

Figure 4-1578. DDRSS_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3168. DDRSS_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

4.6.14 DDRSS_AGGR_ENABLE_CLR Register (Offset = 0204h) [reset = X]

DDRSS_AGGR_ENABLE_CLR is shown in [Figure 4-1579](#) and described in [Table 4-3170](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

**Table 4-3169. DDRSS_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0204h

Figure 4-1579. DDRSS_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3170. DDRSS_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

4.6.15 DDRSS_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

DDRSS_AGGR_STATUS_SET is shown in [Figure 4-1580](#) and described in [Table 4-3172](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

**Table 4-3171. DDRSS_AGGR_STATUS_SET
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 0208h

Figure 4-1580. DDRSS_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 4-3172. DDRSS_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

4.6.16 DDRSS_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

DDRSS_AGGR_STATUS_CLR is shown in [Figure 4-1581](#) and described in [Table 4-3174](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

**Table 4-3173. DDRSS_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_CTL	4D200B 020Ch

Figure 4-1581. DDRSS_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 4-3174. DDRSS_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

4.7 DDRSS0_ECC_AGGR_VBUS Registers

Table 4-3176 lists the memory-mapped registers for the DDRSS0_ECC_AGGR_VBUS. All register offset addresses not listed in Table 4-3176 should be considered as reserved locations and the register contents should not be modified.

**Table 4-3175. DDRSS0_ECC_AGGR_VBUS
Instances**

Instance	Base Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0400h

Table 4-3176. DDRSS0_ECC_AGGR_VBUS Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_EC C_AGGR_VBUS Physical Address
0h	DDRSS_REV	Aggregator Revision Register	4D200B 0400h
8h	DDRSS_VECTOR	ECC Vector Register	4D200B 0408h
Ch	DDRSS_STAT	Misc Status	4D200B 040Ch
10h + formula	DDRSS_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4D200B 0410h + formula
3Ch	DDRSS_SEC_EOI_REG	EOI Register	4D200B 043Ch
40h	DDRSS_SEC_STATUS_REG0	Interrupt Status Register 0	4D200B 0440h
80h	DDRSS_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4D200B 0480h
C0h	DDRSS_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4D200B 04C0h
13Ch	DDRSS_DED_EOI_REG	EOI Register	4D200B 053Ch
140h	DDRSS_DED_STATUS_REG0	Interrupt Status Register 0	4D200B 0540h
180h	DDRSS_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4D200B 0580h
1C0h	DDRSS_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4D200B 05C0h
200h	DDRSS_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4D200B 0600h
204h	DDRSS_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4D200B 0604h
208h	DDRSS_AGGR_STATUS_SET	AGGR interrupt status set Register	4D200B 0608h
20Ch	DDRSS_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4D200B 060Ch

4.7.1 DDRSS_REV Register (Offset = 0h) [reset = 66A0EA00h]

DDRSS_REV is shown in [Figure 4-1582](#) and described in [Table 4-3178](#).

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Table 4-3177. DDRSS_REV Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0400h

Figure 4-1582. DDRSS_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 4-3178. DDRSS_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

4.7.2 DDRSS_VECTOR Register (Offset = 8h) [reset = X]

DDRSS_VECTOR is shown in [Figure 4-1583](#) and described in [Table 4-3180](#).

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ECC Vector Register

Table 4-3179. DDRSS_VECTOR Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0408h

Figure 4-1583. DDRSS_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3180. DDRSS_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

4.7.3 DDRSS_STAT Register (Offset = Ch) [reset = X]

DDRSS_STAT is shown in [Figure 4-1584](#) and described in [Table 4-3182](#).

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Table 4-3181. DDRSS_STAT Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 040Ch

Figure 4-1584. DDRSS_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					NUM_RAMs																
R-X																					R-1h																

LEGEND: R = Read Only; -n = value after reset

Table 4-3182. DDRSS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	1h	Indicates the number of RAMs serviced by the ECC aggregator

4.7.4 DDRSS_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

DDRSS_RESERVED_SVBUS_y is shown in [Figure 4-1585](#) and described in [Table 4-3184](#).

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Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 4-3183. DDRSS_RESERVED_SVBUS_y
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0410h + formula

Figure 4-1585. DDRSS_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-3184. DDRSS_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

4.7.5 DDRSS_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

DDRSS_SEC_EOI_REG is shown in [Figure 4-1586](#) and described in [Table 4-3186](#).

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-3185. DDRSS_SEC_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 043Ch

Figure 4-1586. DDRSS_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3186. DDRSS_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.7.6 DDRSS_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

DDRSS_SEC_STATUS_REG0 is shown in Figure 4-1587 and described in Table 4-3188.

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Interrupt Status Register 0

**Table 4-3187. DDRSS_SEC_STATUS_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0440h

Figure 4-1587. DDRSS_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							VSAFE_SI_PEND
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3188. DDRSS_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	VSAFE_SI_PEND	R/W1S	0h	Interrupt Pending Status for vsafe_si_pend

4.7.7 DDRSS_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

DDRSS_SEC_ENABLE_SET_REG0 is shown in [Figure 4-1588](#) and described in [Table 4-3190](#).

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Interrupt Enable Set Register 0

**Table 4-3189. DDRSS_SEC_ENABLE_SET_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0480h

Figure 4-1588. DDRSS_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							VSAFE_SI_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3190. DDRSS_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	VSAFE_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for vsafe_si_pend

4.7.8 DDRSS_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

DDRSS_SEC_ENABLE_CLR_REG0 is shown in [Figure 4-1589](#) and described in [Table 4-3192](#).

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Interrupt Enable Clear Register 0

**Table 4-3191. DDRSS_SEC_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 04C0h

Figure 4-1589. DDRSS_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							VSAFE_SI_ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3192. DDRSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	VSAFE_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for vsafe_si_pend

4.7.9 DDRSS_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

DDRSS_DED_EOI_REG is shown in [Figure 4-1590](#) and described in [Table 4-3194](#).

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EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-3193. DDRSS_DED_EOI_REG Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 053Ch

Figure 4-1590. DDRSS_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3194. DDRSS_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

4.7.10 DDRSS_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

DDRSS_DED_STATUS_REG0 is shown in [Figure 4-1591](#) and described in [Table 4-3196](#).

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Interrupt Status Register 0

**Table 4-3195. DDRSS_DED_STATUS_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0540h

Figure 4-1591. DDRSS_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							VSAFE_SI_PEND
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3196. DDRSS_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	VSAFE_SI_PEND	R/W1S	0h	Interrupt Pending Status for vsafe_si_pend

4.7.11 DDRSS_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

DDRSS_DED_ENABLE_SET_REG0 is shown in [Figure 4-1592](#) and described in [Table 4-3198](#).

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Interrupt Enable Set Register 0

**Table 4-3197. DDRSS_DED_ENABLE_SET_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0580h

Figure 4-1592. DDRSS_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							VSAFE_SI_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3198. DDRSS_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	VSAFE_SI_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for vsafe_si_pend

4.7.12 DDRSS_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

DDRSS_DED_ENABLE_CLR_REG0 is shown in [Figure 4-1593](#) and described in [Table 4-3200](#).

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Interrupt Enable Clear Register 0

**Table 4-3199. DDRSS_DED_ENABLE_CLR_REG0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 05C0h

Figure 4-1593. DDRSS_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							VSAFE_SI_ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3200. DDRSS_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	VSAFE_SI_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for vsafe_si_pend

4.7.13 DDRSS_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

DDRSS_AGGR_ENABLE_SET is shown in [Figure 4-1594](#) and described in [Table 4-3202](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 4-3201. DDRSS_AGGR_ENABLE_SET Instances

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0600h

Figure 4-1594. DDRSS_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-3202. DDRSS_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

4.7.14 DDRSS_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

DDRSS_AGGR_ENABLE_CLR is shown in [Figure 4-1595](#) and described in [Table 4-3204](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

**Table 4-3203. DDRSS_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0604h

Figure 4-1595. DDRSS_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-3204. DDRSS_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

4.7.15 DDRSS_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

DDRSS_AGGR_STATUS_SET is shown in [Figure 4-1596](#) and described in [Table 4-3206](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

**Table 4-3205. DDRSS_AGGR_STATUS_SET
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 0608h

Figure 4-1596. DDRSS_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 4-3206. DDRSS_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

4.7.16 DDRSS_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

DDRSS_AGGR_STATUS_CLR is shown in [Figure 4-1597](#) and described in [Table 4-3208](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

**Table 4-3207. DDRSS_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_ECC_AGGR_VBUS	4D200B 060Ch

Figure 4-1597. DDRSS_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 4-3208. DDRSS_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

5 VirtSS Registers

5.1 TCU_CFG Registers

Table 5-2 lists the memory-mapped registers for the NAVSS0_TCU_CFG registers. All register offset addresses not listed in Table 5-2 should be considered as reserved locations and the register contents should not be modified.

TCU Registers

Table 5-1. TCU_CFG Instances

Instance	Base Address
TCU_CFG	36600000h

Table 5-2. TCU_CFG Registers

Offset	Acronym	Register Name	TCU_CFG Physical Address
00000h	SMMU_IDR0		36600000h
00004h	SMMU_IDR1		36600004h
00008h	SMMU_IDR2		36600008h
0000Ch	SMMU_IDR3		3660000Ch
00014h	SMMU_IDR5		36600014h
00018h	SMMU_IIDR		36600018h
0001Ch	SMMU_AIDR		3660001Ch
00020h	SMMU_CR0		36600020h
00024h	SMMU_CR0ACK		36600024h
00028h	SMMU_CR1		36600028h
0002Ch	SMMU_CR2		3660002Ch
00044h	SMMU_GBPA		36600044h
00050h	SMMU_IRQ_CTRL		36600050h
00054h	SMMU_IRQ_CTRLACK		36600054h
00060h	SMMU_GERROR		36600060h
00064h	SMMU_GERRORN		36600064h
00068h	SMMU_GERROR_IRQ_CFG0_LO		36600068h
0006Ch	SMMU_GERROR_IRQ_CFG0_HI		3660006Ch
00070h	SMMU_GERROR_IRQ_CFG1		36600070h
00074h	SMMU_GERROR_IRQ_CFG2		36600074h
00080h	SMMU_STRTAB_BASE_LO		36600080h
00084h	SMMU_STRTAB_BASE_HI		36600084h
00088h	SMMU_STRTAB_BASE_CFG		36600088h
00090h	SMMU_CMDQ_BASE_LO		36600090h
00094h	SMMU_CMDQ_BASE_HI		36600094h
00098h	SMMU_CMDQ_PROD		36600098h
0009Ch	SMMU_CMDQ_CONS		3660009Ch
000A0h	SMMU_EVENTQ_BASE_LO		366000A0h
000A4h	SMMU_EVENTQ_BASE_HI		366000A4h
000B0h	SMMU_EVENTQ_IRQ_CFG0_LO		366000B0h
000B4h	SMMU_EVENTQ_IRQ_CFG0_HI		366000B4h
000B8h	SMMU_EVENTQ_IRQ_CFG1		366000B8h
000BCh	SMMU_EVENTQ_IRQ_CFG2		366000BCh
00FD0h	SMMU_PIDR4		36600FD0h
00FD4h	SMMU_PIDR5		36600FD4h
00FD8h	SMMU_PIDR6		36600FD8h
00FDCh	SMMU_PIDR7		36600FDCh

Table 5-2. TCU_CFG Registers (continued)

Offset	Acronym	Register Name	TCU_CFG Physical Address
00FE0h	SMMU_PIDR0		36600FE0h
00FE4h	SMMU_PIDR1		36600FE4h
00FE8h	SMMU_PIDR2		36600FE8h
00FECh	SMMU_PIDR3		36600FECh
00FF0h	SMMU_CIDR0		36600FF0h
00FF4h	SMMU_CIDR1		36600FF4h
00FF8h	SMMU_CIDR2		36600FF8h
00FFCh	SMMU_CIDR3		36600FFCh
02400h	SMMU_PMCG_EVTYPER0		36602400h
02404h	SMMU_PMCG_EVTYPER1		36602404h
02408h	SMMU_PMCG_EVTYPER2		36602408h
0240Ch	SMMU_PMCG_EVTYPER3		3660240Ch
02A00h	SMMU_PMCG_SMR0		36602A00h
02C00h	SMMU_PMCG_CNTENSET0		36602C00h
02C20h	SMMU_PMCG_CNTENCLR0		36602C20h
02C40h	SMMU_PMCG_INTENSET0		36602C40h
02C60h	SMMU_PMCG_INTENCLR0		36602C60h
02DF8h	SMMU_PMCG_SCR		36602DF8h
02E00h	SMMU_PMCG_CFGR		36602E00h
02E04h	SMMU_PMCG_CR		36602E04h
02E20h	SMMU_PMCG_CEID0_LO		36602E20h
02E24h	SMMU_PMCG_CEID0_HI		36602E24h
02E28h	SMMU_PMCG_CEID1_LO		36602E28h
02E2Ch	SMMU_PMCG_CEID1_HI		36602E2Ch
02E50h	SMMU_PMCG_IRQ_CTRL		36602E50h
02E54h	SMMU_PMCG_IRQ_CTRLACK		36602E54h
02E70h	SMMU_PMCG_AIDR		36602E70h
02FB8h	SMMU_PMCG_PMAUTHSTATUS		36602FB8h
02FBCh	SMMU_PMCG_PMDEVARCH		36602FBCh
02FCCh	SMMU_PMCG_PMDEVTYPE		36602FCCh
02FD0h	SMMU_PMCG_PIDR4		36602FD0h
02FD4h	SMMU_PMCG_PIDR5		36602FD4h
02FD8h	SMMU_PMCG_PIDR6		36602FD8h
02FDCh	SMMU_PMCG_PIDR7		36602FDCh
02FE0h	SMMU_PMCG_PIDR0		36602FE0h
02FE4h	SMMU_PMCG_PIDR1		36602FE4h
02FE8h	SMMU_PMCG_PIDR2		36602FE8h
02FECh	SMMU_PMCG_PIDR3		36602FECh
02FF0h	SMMU_PMCG_CIDR0		36602FF0h
02FF4h	SMMU_PMCG_CIDR1		36602FF4h
02FF8h	SMMU_PMCG_CIDR2		36602FF8h
02FFCh	SMMU_PMCG_CIDR3		36602FFCh
08000h	SMMU_S_IDR0		36608000h
08004h	SMMU_S_IDR1		36608004h
0800Ch	SMMU_S_IDR3		3660800Ch
08020h	SMMU_S_CR0		36608020h

Table 5-2. TCU_CFG Registers (continued)

Offset	Acronym	Register Name	TCU_CFG Physical Address
08024h	SMMU_S_CR0ACK		36608024h
08028h	SMMU_S_CR1		36608028h
0802Ch	SMMU_S_CR2		3660802Ch
0803Ch	SMMU_S_INIT		3660803Ch
08044h	SMMU_S_GBPA		36608044h
08050h	SMMU_S_IRQ_CTRL		36608050h
08054h	SMMU_S_IRQ_CTRLACK		36608054h
08060h	SMMU_S_GERROR		36608060h
08064h	SMMU_S_GERRORN		36608064h
08068h	SMMU_S_GERROR_IRQ_CFG0_LO		36608068h
0806Ch	SMMU_S_GERROR_IRQ_CFG0_HI		3660806Ch
08070h	SMMU_S_GERROR_IRQ_CFG1		36608070h
08074h	SMMU_S_GERROR_IRQ_CFG2		36608074h
08080h	SMMU_S_STRTAB_BASE_LO		36608080h
08084h	SMMU_S_STRTAB_BASE_HI		36608084h
08088h	SMMU_S_STRTAB_BASE_CFG		36608088h
08090h	SMMU_S_CMDQ_BASE_LO		36608090h
08094h	SMMU_S_CMDQ_BASE_HI		36608094h
08098h	SMMU_S_CMDQ_PROD		36608098h
0809Ch	SMMU_S_CMDQ_CONS		3660809Ch
080A0h	SMMU_S_EVENTQ_BASE_LO		366080A0h
080A4h	SMMU_S_EVENTQ_BASE_HI		366080A4h
080A8h	SMMU_S_EVENTQ_PROD		366080A8h
080ACh	SMMU_S_EVENTQ_CONS		366080ACh
080B0h	SMMU_S_EVENTQ_IRQ_CFG0_LO		366080B0h
080B4h	SMMU_S_EVENTQ_IRQ_CFG0_HI		366080B4h
080B8h	SMMU_S_EVENTQ_IRQ_CFG1		366080B8h
080BCh	SMMU_S_EVENTQ_IRQ_CFG2		366080BCh
08E00h	TCU_CTRL		36608E00h
08E04h	TCU_QOS		36608E04h
08E08h	TCU_CFG		36608E08h
08E10h	TCU_STATUS		36608E10h
08E18h	TCU_SCR		36608E18h
08E80h	TCU_ERRFR_LO		36608E80h
08E84h	TCU_ERRFR_HI		36608E84h
08E88h	TCU_ERRCTLR_LO		36608E88h
08E8Ch	TCU_ERRCTLR_HI		36608E8Ch
08E90h	TCU_ERRSTATUS_LO		36608E90h
08E94h	TCU_ERRSTATUS_HI		36608E94h
08EC0h	TCU_ERRGEN_LO		36608EC0h
08EC4h	TCU_ERRGEN_HI		36608EC4h
09000h + formula	TCU_NODE_CTRLn		36609000h + formula
09400h + formula	TCU_NODE_STATUSn		36609400h + formula
100A8h	SMMU_EVENTQ_PROD		366100A8h
100ACh	SMMU_EVENTQ_CONS		366100ACh

Table 5-2. TCU_CFG Registers (continued)

Offset	Acronym	Register Name	TCU_CFG Physical Address
22000h	SMMU_PMCG_EVCNTR0		36622000h
22004h	SMMU_PMCG_EVCNTR1		36622004h
22008h	SMMU_PMCG_EVCNTR2		36622008h
2200Ch	SMMU_PMCG_EVCNTR3		3662200Ch
22600h	SMMU_PMCG_SVR0		36622600h
22604h	SMMU_PMCG_SVR1		36622604h
22608h	SMMU_PMCG_SVR2		36622608h
2260Ch	SMMU_PMCG_SVR3		3662260Ch
22C80h	SMMU_PMCG_OVSCLR0		36622C80h
22CC0h	SMMU_PMCG_OVSSET0		36622CC0h
22D88h	SMMU_PMCG_CAPR		36622D88h

5.1.1 SMMU_IDR0 Register (Offset = 00000h) [reset = 080E3E0Fh]

SMMU_IDR0 is shown in Figure 5-1 and described in Table 5-3.

Return to [Summary Table](#).

SMMU_IDR0

Figure 5-1. SMMU_IDR0 Register

31	30	29	28	27	26	25	24
RESERVED			ST_LEVEL		TERM_MODEL	STALL_MODEL	
R-0h			R-1h		R-0h	R-0h	
23	22	21	20	19	18	17	16
RESERVED	TTENDIAN		VATOS	CD2L	VMID16	VMW	PRI
R-0h	R-0h		R-0h	R-1h	R-1h	R-1h	R-0h
15	14	13	12	11	10	9	8
ATOS	SEV	MSI	ASID16	NS1ATS	ATS	HYP	DORMHINT
R-0h	R-0h	R-1h	R-1h	R-1h	R-1h	R-1h	R-0h
7	6	5	4	3	2	1	0
HTTU		BTM	COHACC	TTF		S1P	S2P
R-0h		R-0h	R-0h	R-3h		R-1h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 5-3. SMMU_IDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved_31_29
28-27	ST_LEVEL	R	1h	ST_LEVEL
26	TERM_MODEL	R	0h	TERM_MODEL
25-24	STALL_MODEL	R	0h	STALL_MODEL
23	RESERVED	R	0h	Reserved_23_23
22-21	TTENDIAN	R	0h	TTENDIAN
20	VATOS	R	0h	VATOS
19	CD2L	R	1h	CD2L
18	VMID16	R	1h	VMID16
17	VMW	R	1h	VMW
16	PRI	R	0h	PRI
15	ATOS	R	0h	ATOS
14	SEV	R	0h	SEV
13	MSI	R	1h	MSI
12	ASID16	R	1h	ASID16
11	NS1ATS	R	1h	NS1ATS
10	ATS	R	1h	ATS
9	HYP	R	1h	HYP
8	DORMHINT	R	0h	DORMHINT
7-6	HTTU	R	0h	HTTU
5	BTM	R	0h	BTM

Table 5-3. SMMU_IDR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	COHACC	R	0h	COHACC
3-2	TTF	R	3h	TTF
1	S1P	R	1h	S1P
0	S2P	R	1h	S2P

Table 5-4. Register Call Summary for SMMU_IDR0

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_IDR0 Register \(Offset = 00000h\) \[reset = 080E3E0Fh\]: \[0\] \[1\]](#)

5.1.2 SMMU_IDR1 Register (Offset = 00004h) [reset = 0E730518h]

SMMU_IDR1 is shown in Figure 5-2 and described in Table 5-5.

Return to [Summary Table](#).

SMMU_IDR1

Figure 5-2. SMMU_IDR1 Register

31	30	29	28	27	26	25	24
RESERVED	TABLES_PRESET	QUEUES_PRESET	REL	ATTR_TYPES_OVR	ATTR_PERMS_OVR	CMDQS	
R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-13h	
23	22	21	20	19	18	17	16
CMDQS			EVENTQS				
R-13h			R-13h				
15	14	13	12	11	10	9	8
PRIQS					SSIDSIZE		
R-0h					R-14h		
7	6	5	4	3	2	1	0
SSIDSIZE		SIDSIZE					
R-14h				R-18h			

LEGEND: R = Read Only; -n = value after reset

Table 5-5. SMMU_IDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	TABLES_PRESET	R	0h	TABLES_PRESET
29	QUEUES_PRESET	R	0h	QUEUES_PRESET
28	REL	R	0h	REL
27	ATTR_TYPES_OVR	R	1h	ATTR_TYPES_OVR
26	ATTR_PERMS_OVR	R	1h	ATTR_PERMS_OVR
25-21	CMDQS	R	13h	CMDQS
20-16	EVENTQS	R	13h	EVENTQS
15-11	PRIQS	R	0h	PRIQS
10-6	SSIDSIZE	R	14h	SSIDSIZE
5-0	SIDSIZE	R	18h	SIDSIZE

Table 5-6. Register Call Summary for SMMU_IDR1

TCU_CFG Registers

- [SMMU_IDR1 Register \(Offset = 00004h\) \[reset = 0E730518h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.3 SMMU_IDR2 Register (Offset = 00008h) [reset = 0h]

SMMU_IDR2 is shown in [Figure 5-3](#) and described in [Table 5-7](#).

Return to [Summary Table](#).

SMMU_IDR2

Figure 5-3. SMMU_IDR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						BA_VATOS															
R-0h																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-7. SMMU_IDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved_31_10
9-0	BA_VATOS	R	0h	BA_VATOS

Table 5-8. Register Call Summary for SMMU_IDR2

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_IDR2 Register \(Offset = 00008h\) \[reset = 0h\]](#): [0] [1]

5.1.4 SMMU_IDR3 Register (Offset = 0000Ch) [reset = 1Ch]

SMMU_IDR3 is shown in Figure 5-4 and described in Table 5-9.

Return to [Summary Table](#).

SMMU_IDR3

Figure 5-4. SMMU_IDR3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			XNX	PBHA	HAD	RESERVED	
R-0h			R-1h	R-1h	R-1h	R-0h	

LEGEND: R = Read Only; -n = value after reset

Table 5-9. SMMU_IDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved_31_5
4	XNX	R	1h	XNX
3	PBHA	R	1h	PBHA
2	HAD	R	1h	HAD
1-0	RESERVED	R	0h	Reserved_1_0

Table 5-10. Register Call Summary for SMMU_IDR3

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_IDR3 Register \(Offset = 0000Ch\) \[reset = 1Ch\]](#): [0] [1]

5.1.5 SMMU_IDR5 Register (Offset = 00014h) [reset = 00040070h]

SMMU_IDR5 is shown in Figure 5-5 and described in Table 5-11.

Return to [Summary Table](#).

SMMU_IDR5

Figure 5-5. SMMU_IDR5 Register

31	30	29	28	27	26	25	24
STALL_MAX							
R-4h							
23	22	21	20	19	18	17	16
STALL_MAX							
R-4h							
15	14	13	12	11	10	9	8
RESERVED				VAX		RESERVED	
R-0h				R-0h		R-0h	
7	6	5	4	3	2	1	0
RESERVED	GRAN64K	GRAN16K	GRAN4K	RESERVED	OAS		
R-0h	R-1h	R-1h	R-1h	R-0h	R-0h		

LEGEND: R = Read Only; -n = value after reset

Table 5-11. SMMU_IDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	STALL_MAX	R	4h	STALL_MAX
15-12	RESERVED	R	0h	Reserved_15_12
11-10	VAX	R	0h	VAX
9-7	RESERVED	R	0h	Reserved_9_7
6	GRAN64K	R	1h	GRAN64K
5	GRAN16K	R	1h	GRAN16K
4	GRAN4K	R	1h	GRAN4K
3	RESERVED	R	0h	Reserved_3_3
2-0	OAS	R	0h	OAS

Table 5-12. Register Call Summary for SMMU_IDR5

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_IDR5 Register (Offset = 00014h) [reset = 00040070h]: [0] [1] TCU_CFG Registers: [0]

5.1.6 SMMU_IIDR Register (Offset = 00018h) [reset = 4830243Bh]

SMMU_IIDR is shown in [Figure 5-6](#) and described in [Table 5-13](#).

Return to [Summary Table](#).

SMMU_IIDR

Figure 5-6. SMMU_IIDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRODUCTID												VARIANT			
R-483h												R-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION				IMPLEMENTER											
R-2h				R-43Bh											

LEGEND: R = Read Only; -n = value after reset

Table 5-13. SMMU_IIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	PRODUCTID	R	483h	ProductID
19-16	VARIANT	R	0h	Variant
15-12	REVISION	R	2h	Revision
11-0	IMPLEMENTER	R	43Bh	Implementer

Table 5-14. Register Call Summary for SMMU_IIDR

TCU_CFG Registers

- [SMMU_IIDR Register \(Offset = 00018h\) \[reset = 4830243Bh\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.7 SMMU_AIDR Register (Offset = 0001Ch) [reset = 1h]

SMMU_AIDR is shown in [Figure 5-7](#) and described in [Table 5-15](#).

Return to [Summary Table](#).

SMMU_AIDR

Figure 5-7. SMMU_AIDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ARCHMAJORREV				ARCHMINORREV			
R-0h								R-0h				R-1h			

LEGEND: R = Read Only; -n = value after reset

Table 5-15. SMMU_AIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	ARCHMAJORREV	R	0h	ArchMajorRev
3-0	ARCHMINORREV	R	1h	ArchMinorRev

Table 5-16. Register Call Summary for SMMU_AIDR

TCU_CFG Registers

- [SMMU_AIDR Register \(Offset = 0001Ch\) \[reset = 1h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.8 SMMU_CR0 Register (Offset = 00020h) [reset = 0h]

SMMU_CR0 is shown in [Figure 5-8](#) and described in [Table 5-17](#).

Return to [Summary Table](#).

SMMU_CR0

Figure 5-8. SMMU_CR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							VMW
R-0h							R/W-0h
7	6	5	4	3	2	1	0
VMW		RESERVED	ATSCHK	CMDQEN	EVENTQEN	RESERVED	SMMUEN
R/W-0h		R-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-17. SMMU_CR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved_31_9
8-6	VMW	R/W	0h	VMW
5	RESERVED	R	0h	Reserved_5_5
4	ATSCHK	R/W	0h	ATSCHK
3	CMDQEN	R/W	0h	CMDQEN
2	EVENTQEN	R/W	0h	EVENTQEN
1	RESERVED	R	0h	Reserved_1_1
0	SMMUEN	R/W	0h	SMMUEN

Table 5-18. Register Call Summary for SMMU_CR0

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_CR0 Register \(Offset = 00020h\) \[reset = 0h\]](#): [0] [1]

5.1.9 SMMU_CR0ACK Register (Offset = 00024h) [reset = 0h]

SMMU_CR0ACK is shown in [Figure 5-9](#) and described in [Table 5-19](#).

Return to [Summary Table](#).

SMMU_CR0ACK

Figure 5-9. SMMU_CR0ACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							VMW
R-0h							R-0h
7	6	5	4	3	2	1	0
VMW		RESERVED	ATSCHK	CMDQEN	EVENTQEN	RESERVED	SMMUEN
R-0h		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-19. SMMU_CR0ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved_31_9
8-6	VMW	R	0h	VMW
5	RESERVED	R	0h	Reserved_5_5
4	ATSCHK	R	0h	ATSCHK
3	CMDQEN	R	0h	CMDQEN
2	EVENTQEN	R	0h	EVENTQEN
1	RESERVED	R	0h	Reserved_1_1
0	SMMUEN	R	0h	SMMUEN

Table 5-20. Register Call Summary for SMMU_CR0ACK

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_CR0ACK Register \(Offset = 00024h\) \[reset = 0h\]](#): [0] [1]

5.1.10 SMMU_CR1 Register (Offset = 00028h) [reset = 0h]

SMMU_CR1 is shown in [Figure 5-10](#) and described in [Table 5-21](#).

Return to [Summary Table](#).

SMMU_CR1

Figure 5-10. SMMU_CR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				TABLE_SH		TABLE_OC	
R-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
TABLE_IC		QUEUE_SH		QUEUE_OC		QUEUE_IC	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-21. SMMU_CR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved_31_12
11-10	TABLE_SH	R/W	0h	TABLE_SH
9-8	TABLE_OC	R/W	0h	TABLE_OC
7-6	TABLE_IC	R/W	0h	TABLE_IC
5-4	QUEUE_SH	R/W	0h	QUEUE_SH
3-2	QUEUE_OC	R/W	0h	QUEUE_OC
1-0	QUEUE_IC	R/W	0h	QUEUE_IC

Table 5-22. Register Call Summary for SMMU_CR1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_CR1 Register \(Offset = 00028h\) \[reset = 0h\]](#): [0] [1]

5.1.11 SMMU_CR2 Register (Offset = 0002Ch) [reset = 0h]

SMMU_CR2 is shown in [Figure 5-11](#) and described in [Table 5-23](#).

Return to [Summary Table](#).

SMMU_CR2

Figure 5-11. SMMU_CR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					PTM	RECINVSID	E2H
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-23. SMMU_CR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved_31_3
2	PTM	R/W	0h	PTM
1	RECINVSID	R/W	0h	RECINVSID
0	E2H	R/W	0h	E2H

Table 5-24. Register Call Summary for SMMU_CR2

TCU_CFG Registers

- [SMMU_CR2 Register \(Offset = 0002Ch\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.12 SMMU_GBPA Register (Offset = 00044h) [reset = 0h]

SMMU_GBPA is shown in [Figure 5-12](#) and described in [Table 5-25](#).

Return to [Summary Table](#).

SMMU_GBPA

Figure 5-12. SMMU_GBPA Register

31	30	29	28	27	26	25	24
UPDATE	RESERVED						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED			ABORT	INSTCFG		PRIVCFG	
R-0h			R/W-0h	R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED		SHCFG		ALLOCCFG			
R-0h		R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
RESERVED			MTCFG	MEMATTR			
R-0h			R/W-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-25. SMMU_GBPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UPDATE	R/W	0h	Update
30-21	RESERVED	R	0h	Reserved_30_21
20	ABORT	R/W	0h	ABORT
19-18	INSTCFG	R/W	0h	INSTCFG
17-16	PRIVCFG	R/W	0h	PRIVCFG
15-14	RESERVED	R	0h	Reserved_15_14
13-12	SHCFG	R/W	0h	SHCFG
11-8	ALLOCCFG	R/W	0h	ALLOCCFG
7-5	RESERVED	R	0h	Reserved_7_5
4	MTCFG	R/W	0h	MTCFG
3-0	MEMATTR	R/W	0h	MemAttr

Table 5-26. Register Call Summary for SMMU_GBPA

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_GBPA Register \(Offset = 00044h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.13 SMMU_IRQ_CTRL Register (Offset = 00050h) [reset = 0h]

SMMU_IRQ_CTRL is shown in [Figure 5-13](#) and described in [Table 5-27](#).

Return to [Summary Table](#).

SMMU_IRQ_CTRL

Figure 5-13. SMMU_IRQ_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					EVENTQ_IRQE N	RESERVED	GERROR_IRQ EN
R-0h					R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-27. SMMU_IRQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved_31_3
2	EVENTQ_IRQEN	R/W	0h	EVENTQ_IRQEN
1	RESERVED	R	0h	Reserved_1_1
0	GERROR_IRQEN	R/W	0h	GERROR_IRQEN

Table 5-28. Register Call Summary for SMMU_IRQ_CTRL

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_IRQ_CTRL Register \(Offset = 00050h\) \[reset = 0h\]](#): [0] [1]

5.1.14 SMMU_IRQ_CTRLACK Register (Offset = 00054h) [reset = 0h]

SMMU_IRQ_CTRLACK is shown in [Figure 5-14](#) and described in [Table 5-29](#).

Return to [Summary Table](#).

SMMU_IRQ_CTRLACK

Figure 5-14. SMMU_IRQ_CTRLACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					EVENTQ_IRQE N	RESERVED	GERROR_IRQ EN
R-0h					R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-29. SMMU_IRQ_CTRLACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved_31_3
2	EVENTQ_IRQEN	R	0h	EVENTQ_IRQEN
1	RESERVED	R	0h	Reserved_1_1
0	GERROR_IRQEN	R	0h	GERROR_IRQEN

Table 5-30. Register Call Summary for SMMU_IRQ_CTRLACK

TCU_CFG Registers

- [SMMU_IRQ_CTRLACK Register \(Offset = 00054h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.15 SMMU_GERROR Register (Offset = 00060h) [reset = 0h]

SMMU_GERROR is shown in [Figure 5-15](#) and described in [Table 5-31](#).

Return to [Summary Table](#).

SMMU_GERROR

Figure 5-15. SMMU_GERROR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
MSI_GERROR_AB_T_ERR	RESERVED	MSI_EVENTQ_AB_T_ERR	MSI_CMDQ_ABT_ERR	RESERVED	EVENTQ_AB_T_ERR	RESERVED	CMDQ_ERR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-31. SMMU_GERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7	MSI_GERROR_AB_T_ERR	R	0h	MSI_GERROR_AB_T_ERR
6	RESERVED	R	0h	Reserved_6_6
5	MSI_EVENTQ_AB_T_ERR	R	0h	MSI_EVENTQ_AB_T_ERR
4	MSI_CMDQ_AB_T_ERR	R	0h	MSI_CMDQ_AB_T_ERR
3	RESERVED	R	0h	Reserved_3_3
2	EVENTQ_AB_T_ERR	R	0h	EVENTQ_AB_T_ERR
1	RESERVED	R	0h	Reserved_1_1
0	CMDQ_ERR	R	0h	CMDQ_ERR

Table 5-32. Register Call Summary for SMMU_GERROR

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_GERROR Register \(Offset = 00060h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.16 SMMU_GERRORN Register (Offset = 00064h) [reset = 0h]

SMMU_GERRORN is shown in Figure 5-16 and described in Table 5-33.

Return to [Summary Table](#).

SMMU_GERRORN

Figure 5-16. SMMU_GERRORN Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
MSI_GERROR_ABT_ERR	RESERVED	MSI_EVENTQ_ABT_ERR	MSI_CMDQ_ABT_ERR	RESERVED	EVENTQ_ABT_ERR	RESERVED	CMDQ_ERR
R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-33. SMMU_GERRORN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7	MSI_GERROR_ABT_ERR	R/W	0h	MSI_GERROR_ABT_ERR
6	RESERVED	R	0h	Reserved_6_6
5	MSI_EVENTQ_ABT_ERR	R/W	0h	MSI_EVENTQ_ABT_ERR
4	MSI_CMDQ_ABT_ERR	R/W	0h	MSI_CMDQ_ABT_ERR
3	RESERVED	R	0h	Reserved_3_3
2	EVENTQ_ABT_ERR	R/W	0h	EVENTQ_ABT_ERR
1	RESERVED	R	0h	Reserved_1_1
0	CMDQ_ERR	R/W	0h	CMDQ_ERR

Table 5-34. Register Call Summary for SMMU_GERRORN

TCU_CFG Registers

- [SMMU_GERRORN Register \(Offset = 00064h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.17 SMMU_GERROR_IRQ_CFG0_LO Register (Offset = 00068h) [reset = 0h]

SMMU_GERROR_IRQ_CFG0_LO is shown in [Figure 5-17](#) and described in [Table 5-35](#).

Return to [Summary Table](#).

SMMU_GERROR_IRQ_CFG0_LO

Figure 5-17. SMMU_GERROR_IRQ_CFG0_LO Register

31	30	29	28	27	26	25	24
ADDR							
R/W-0h							
23	22	21	20	19	18	17	16
ADDR							
R/W-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR						RESERVED	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-35. SMMU_GERROR_IRQ_CFG0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R/W	0h	ADDR
1-0	RESERVED	R	0h	Reserved_1_0

Table 5-36. Register Call Summary for SMMU_GERROR_IRQ_CFG0_LO

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_GERROR_IRQ_CFG0_LO Register \(Offset = 00068h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.18 SMMU_GERROR_IRQ_CFG0_HI Register (Offset = 0006Ch) [reset = 0h]

SMMU_GERROR_IRQ_CFG0_HI is shown in [Figure 5-18](#) and described in [Table 5-37](#).

Return to [Summary Table](#).

SMMU_GERROR_IRQ_CFG0_HI

Figure 5-18. SMMU_GERROR_IRQ_CFG0_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-37. SMMU_GERROR_IRQ_CFG0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved_31_16
15-0	ADDR	R/W	0h	ADDR

Table 5-38. Register Call Summary for SMMU_GERROR_IRQ_CFG0_HI

TCU_CFG Registers
<ul style="list-style-type: none"> TCU_CFG Registers: [0] SMMU_GERROR_IRQ_CFG0_HI Register (Offset = 0006Ch) [reset = 0h]: [0] [1]

5.1.19 SMMU_GERROR_IRQ_CFG1 Register (Offset = 00070h) [reset = 0h]

SMMU_GERROR_IRQ_CFG1 is shown in [Figure 5-19](#) and described in [Table 5-39](#).

Return to [Summary Table](#).

SMMU_GERROR_IRQ_CFG1

Figure 5-19. SMMU_GERROR_IRQ_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-39. SMMU_GERROR_IRQ_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	DATA

Table 5-40. Register Call Summary for SMMU_GERROR_IRQ_CFG1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_GERROR_IRQ_CFG1 Register \(Offset = 00070h\) \[reset = 0h\]](#): [0] [1]

5.1.20 SMMU_GERROR_IRQ_CFG2 Register (Offset = 00074h) [reset = 0h]

SMMU_GERROR_IRQ_CFG2 is shown in [Figure 5-20](#) and described in [Table 5-41](#).

Return to [Summary Table](#).

SMMU_GERROR_IRQ_CFG2

Figure 5-20. SMMU_GERROR_IRQ_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SH		MEMATTR			
R-0h										R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-41. SMMU_GERROR_IRQ_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved_31_6
5-4	SH	R/W	0h	SH
3-0	MEMATTR	R/W	0h	MemAttr

Table 5-42. Register Call Summary for SMMU_GERROR_IRQ_CFG2

TCU_CFG Registers

- [SMMU_GERROR_IRQ_CFG2 Register \(Offset = 00074h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.21 SMMU_STRTAB_BASE_LO Register (Offset = 00080h) [reset = 0h]

SMMU_STRTAB_BASE_LO is shown in [Figure 5-21](#) and described in [Table 5-43](#).

Return to [Summary Table](#).

SMMU_STRTAB_BASE_LO

Figure 5-21. SMMU_STRTAB_BASE_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR										RESERVED					
R/W-0h										R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-43. SMMU_STRTAB_BASE_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	ADDR	R/W	0h	ADDR
5-0	RESERVED	R	0h	Reserved_5_0

Table 5-44. Register Call Summary for SMMU_STRTAB_BASE_LO

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_STRTAB_BASE_LO Register (Offset = 00080h) [reset = 0h]: [0] [1] TCU_CFG Registers: [0]

5.1.22 SMMU_STRTAB_BASE_HI Register (Offset = 00084h) [reset = 0h]

SMMU_STRTAB_BASE_HI is shown in [Figure 5-22](#) and described in [Table 5-45](#).

Return to [Summary Table](#).

SMMU_STRTAB_BASE_HI

Figure 5-22. SMMU_STRTAB_BASE_HI Register

31	30	29	28	27	26	25	24
RESERVED	RA	RESERVED					
R-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-45. SMMU_STRTAB_BASE_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	RA	R/W	0h	RA
29-16	RESERVED	R	0h	Reserved_29_16
15-0	ADDR	R/W	0h	ADDR

Table 5-46. Register Call Summary for SMMU_STRTAB_BASE_HI

TCU_CFG Registers

- [SMMU_STRTAB_BASE_HI Register \(Offset = 00084h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.23 SMMU_STRTAB_BASE_CFG Register (Offset = 00088h) [reset = 0h]

SMMU_STRTAB_BASE_CFG is shown in [Figure 5-23](#) and described in [Table 5-47](#).

Return to [Summary Table](#).

SMMU_STRTAB_BASE_CFG

Figure 5-23. SMMU_STRTAB_BASE_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														FMT	
R-0h														R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						SPLIT					LOG2SIZE				
R-0h						R/W-0h					R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-47. SMMU_STRTAB_BASE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved_31_18
17-16	FMT	R/W	0h	FMT
15-11	RESERVED	R	0h	Reserved_15_11
10-6	SPLIT	R/W	0h	SPLIT
5-0	LOG2SIZE	R/W	0h	LOG2SIZE

Table 5-48. Register Call Summary for SMMU_STRTAB_BASE_CFG

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_STRTAB_BASE_CFG Register \(Offset = 00088h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.24 SMMU_CMDQ_BASE_LO Register (Offset = 00090h) [reset = 0h]

SMMU_CMDQ_BASE_LO is shown in [Figure 5-24](#) and described in [Table 5-49](#).

Return to [Summary Table](#).

SMMU_CMDQ_BASE_LO

Figure 5-24. SMMU_CMDQ_BASE_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR											LOG2SIZE				
R/W-0h											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-49. SMMU_CMDQ_BASE_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	ADDR	R/W	0h	ADDR
4-0	LOG2SIZE	R/W	0h	LOG2SIZE

Table 5-50. Register Call Summary for SMMU_CMDQ_BASE_LO

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_CMDQ_BASE_LO Register \(Offset = 00090h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.25 SMMU_CMDQ_BASE_HI Register (Offset = 00094h) [reset = 0h]

SMMU_CMDQ_BASE_HI is shown in [Figure 5-25](#) and described in [Table 5-51](#).

Return to [Summary Table](#).

SMMU_CMDQ_BASE_HI

Figure 5-25. SMMU_CMDQ_BASE_HI Register

31	30	29	28	27	26	25	24
RESERVED	RA	RESERVED					
R-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-51. SMMU_CMDQ_BASE_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	RA	R/W	0h	RA
29-16	RESERVED	R	0h	Reserved_29_16
15-0	ADDR	R/W	0h	ADDR

Table 5-52. Register Call Summary for SMMU_CMDQ_BASE_HI

TCU_CFG Registers
<ul style="list-style-type: none"> TCU_CFG Registers: [0] SMMU_CMDQ_BASE_HI Register (Offset = 00094h) [reset = 0h]: [0] [1]

5.1.26 SMMU_CMDQ_PROD Register (Offset = 00098h) [reset = 0h]

SMMU_CMDQ_PROD is shown in [Figure 5-26](#) and described in [Table 5-53](#).

Return to [Summary Table](#).

SMMU_CMDQ_PROD

Figure 5-26. SMMU_CMDQ_PROD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												WR																			
R-0h												R/W-0h																			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-53. SMMU_CMDQ_PROD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved_31_20
19-0	WR	R/W	0h	WR

Table 5-54. Register Call Summary for SMMU_CMDQ_PROD

TCU_CFG Registers

- [SMMU_CMDQ_PROD Register \(Offset = 00098h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.27 SMMU_CMDQ_CONS Register (Offset = 0009Ch) [reset = 0h]

SMMU_CMDQ_CONS is shown in Figure 5-27 and described in Table 5-55.

Return to [Summary Table](#).

SMMU_CMDQ_CONS

Figure 5-27. SMMU_CMDQ_CONS Register

31	30	29	28	27	26	25	24
RESERVED				ERR			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				RD			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
				RD			
				R/W-0h			
7	6	5	4	3	2	1	0
				RD			
				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-55. SMMU_CMDQ_CONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30-24	ERR	R/W	0h	ERR
23-20	RESERVED	R	0h	Reserved_23_20
19-0	RD	R/W	0h	RD

Table 5-56. Register Call Summary for SMMU_CMDQ_CONS

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_CMDQ_CONS Register \(Offset = 0009Ch\) \[reset = 0h\]](#): [0] [1]

5.1.28 SMMU_EVENTQ_BASE_LO Register (Offset = 000A0h) [reset = 0h]

SMMU_EVENTQ_BASE_LO is shown in [Figure 5-28](#) and described in [Table 5-57](#).

Return to [Summary Table](#).

SMMU_EVENTQ_BASE_LO

Figure 5-28. SMMU_EVENTQ_BASE_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR											LOG2SIZE				
R/W-0h											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-57. SMMU_EVENTQ_BASE_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	ADDR	R/W	0h	ADDR
4-0	LOG2SIZE	R/W	0h	LOG2SIZE

Table 5-58. Register Call Summary for SMMU_EVENTQ_BASE_LO

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_EVENTQ_BASE_LO Register \(Offset = 000A0h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.29 SMMU_EVENTQ_BASE_HI Register (Offset = 000A4h) [reset = 0h]

SMMU_EVENTQ_BASE_HI is shown in [Figure 5-29](#) and described in [Table 5-59](#).

Return to [Summary Table](#).

SMMU_EVENTQ_BASE_HI

Figure 5-29. SMMU_EVENTQ_BASE_HI Register

31	30	29	28	27	26	25	24
RESERVED	WA	RESERVED					
R-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-59. SMMU_EVENTQ_BASE_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	WA	R/W	0h	WA
29-16	RESERVED	R	0h	Reserved_29_16
15-0	ADDR	R/W	0h	ADDR

Table 5-60. Register Call Summary for SMMU_EVENTQ_BASE_HI

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_EVENTQ_BASE_HI Register \(Offset = 000A4h\) \[reset = 0h\]](#): [0] [1]

5.1.30 SMMU_EVENTQ_IRQ_CFG0_LO Register (Offset = 000B0h) [reset = 0h]

SMMU_EVENTQ_IRQ_CFG0_LO is shown in [Figure 5-30](#) and described in [Table 5-61](#).

Return to [Summary Table](#).

SMMU_EVENTQ_IRQ_CFG0_LO

Figure 5-30. SMMU_EVENTQ_IRQ_CFG0_LO Register

31	30	29	28	27	26	25	24
ADDR							
R/W-0h							
23	22	21	20	19	18	17	16
ADDR							
R/W-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR						RESERVED	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-61. SMMU_EVENTQ_IRQ_CFG0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R/W	0h	ADDR
1-0	RESERVED	R	0h	Reserved_1_0

Table 5-62. Register Call Summary for SMMU_EVENTQ_IRQ_CFG0_LO

TCU_CFG Registers

- [SMMU_EVENTQ_IRQ_CFG0_LO Register \(Offset = 000B0h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.31 SMMU_EVENTQ_IRQ_CFG0_HI Register (Offset = 000B4h) [reset = 0h]

SMMU_EVENTQ_IRQ_CFG0_HI is shown in [Figure 5-31](#) and described in [Table 5-63](#).

Return to [Summary Table](#).

SMMU_EVENTQ_IRQ_CFG0_HI

Figure 5-31. SMMU_EVENTQ_IRQ_CFG0_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-63. SMMU_EVENTQ_IRQ_CFG0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved_31_16
15-0	ADDR	R/W	0h	ADDR

Table 5-64. Register Call Summary for SMMU_EVENTQ_IRQ_CFG0_HI

TCU_CFG Registers

- [SMMU_EVENTQ_IRQ_CFG0_HI Register \(Offset = 000B4h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.32 SMMU_EVENTQ_IRQ_CFG1 Register (Offset = 000B8h) [reset = 0h]

SMMU_EVENTQ_IRQ_CFG1 is shown in [Figure 5-32](#) and described in [Table 5-65](#).

[Return to Summary Table.](#)

SMMU_EVENTQ_IRQ_CFG1

Figure 5-32. SMMU_EVENTQ_IRQ_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-65. SMMU_EVENTQ_IRQ_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	DATA

Table 5-66. Register Call Summary for SMMU_EVENTQ_IRQ_CFG1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_EVENTQ_IRQ_CFG1 Register \(Offset = 000B8h\) \[reset = 0h\]](#): [0] [1]

5.1.33 SMMU_EVENTQ_IRQ_CFG2 Register (Offset = 000BCh) [reset = 0h]

SMMU_EVENTQ_IRQ_CFG2 is shown in [Figure 5-33](#) and described in [Table 5-67](#).

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SMMU_EVENTQ_IRQ_CFG2

Figure 5-33. SMMU_EVENTQ_IRQ_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SH		MEMATTR			
R-0h										R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-67. SMMU_EVENTQ_IRQ_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved_31_6
5-4	SH	R/W	0h	SH
3-0	MEMATTR	R/W	0h	MemAttr

Table 5-68. Register Call Summary for SMMU_EVENTQ_IRQ_CFG2

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_EVENTQ_IRQ_CFG2 Register \(Offset = 000BCh\) \[reset = 0h\]](#): [0] [1]

5.1.34 SMMU_PIDR4 Register (Offset = 00FD0h) [reset = 4h]

SMMU_PIDR4 is shown in [Figure 5-34](#) and described in [Table 5-69](#).

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This is the TCU Peripheral ID register 4. This is a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-34. SMMU_PIDR4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZE				DES_2			
R-0h								R-0h				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 5-69. SMMU_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	SIZE	R	0h	4KB region count.
3-0	DES_2	R	4h	JEP106 continuation code for ARM.

Table 5-70. Register Call Summary for SMMU_PIDR4

TCU_CFG Registers

- [SMMU_PIDR4 Register \(Offset = 00FD0h\) \[reset = 4h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.35 SMMU_PIDR5 Register (Offset = 00FD4h) [reset = 0h]

SMMU_PIDR5 is shown in [Figure 5-35](#) and described in [Table 5-71](#).

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This is the TCU Peripheral ID register 5. This is a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-35. SMMU_PIDR5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-71. SMMU_PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	RESERVED	R	0h	Reserved.

Table 5-72. Register Call Summary for SMMU_PIDR5

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PIDR5 Register \(Offset = 00FD4h\) \[reset = 0h\]](#): [0]

5.1.36 SMMU_PIDR6 Register (Offset = 00FD8h) [reset = 0h]

SMMU_PIDR6 is shown in [Figure 5-36](#) and described in [Table 5-73](#).

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This is the TCU Peripheral ID register 6. This is a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-36. SMMU_PIDR6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-73. SMMU_PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	RESERVED	R	0h	Reserved.

Table 5-74. Register Call Summary for SMMU_PIDR6

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PIDR6 Register \(Offset = 00FD8h\) \[reset = 0h\]](#): [0]

5.1.37 SMMU_PIDR7 Register (Offset = 00FDCh) [reset = 0h]

SMMU_PIDR7 is shown in [Figure 5-37](#) and described in [Table 5-75](#).

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This is the TCU Peripheral ID register 7, a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-37. SMMU_PIDR7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-75. SMMU_PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	RESERVED	R	0h	Reserved.

Table 5-76. Register Call Summary for SMMU_PIDR7

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PIDR7 Register \(Offset = 00FDCh\) \[reset = 0h\]](#): [0]

5.1.38 SMMU_PIDR0 Register (Offset = 00FE0h) [reset = 83h]

SMMU_PIDR0 is shown in [Figure 5-38](#) and described in [Table 5-77](#).

Return to [Summary Table](#).

This is the TCU Peripheral ID register 0, a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-38. SMMU_PIDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PART_0							
R-0h																								R-83h							

LEGEND: R = Read Only; -n = value after reset

Table 5-77. SMMU_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PART_0	R	83h	Part number [7:0].

Table 5-78. Register Call Summary for SMMU_PIDR0

TCU_CFG Registers

- [SMMU_PIDR0 Register \(Offset = 00FE0h\) \[reset = 83h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.39 SMMU_PIDR1 Register (Offset = 00FE4h) [reset = B4h]

SMMU_PIDR1 is shown in Figure 5-39 and described in Table 5-79.

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This is the TCU Peripheral ID register 1, a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-39. SMMU_PIDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DES_0				PART_1			
R-0h								R-Bh				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 5-79. SMMU_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	DES_0	R	Bh	JEP106 ID code [3:0] for ARM.
3-0	PART_1	R	4h	Part number [11:8].

Table 5-80. Register Call Summary for SMMU_PIDR1

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_PIDR1 Register (Offset = 00FE4h) [reset = B4h]: [0] TCU_CFG Registers: [0]

5.1.40 SMMU_PIDR2 Register (Offset = 00FE8h) [reset = Bh]

SMMU_PIDR2 is shown in [Figure 5-40](#) and described in [Table 5-81](#).

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This is the TCU Peripheral ID register 2, a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-40. SMMU_PIDR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC		DES_1	
R-0h				R-1h		R-3h	

LEGEND: R = Read Only; -n = value after reset

Table 5-81. SMMU_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	REVISION	R	0h	MMU-600 major revision. The value indicates major product revision rX.
3	JEDEC	R	1h	IC uses a manufacturer identity code that is allocated by JEDEC, according to the JEP106 specification.
2-0	DES_1	R	3h	JEP106 ID code [6:4] for ARM.

Table 5-82. Register Call Summary for SMMU_PIDR2

TCU_CFG Registers

- [SMMU_PIDR2 Register \(Offset = 00FE8h\) \[reset = Bh\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.41 SMMU_PIDR3 Register (Offset = 00FECh) [reset = 20h]

SMMU_PIDR3 is shown in [Figure 5-41](#) and described in [Table 5-83](#).

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This is the TCU Peripheral ID register 3, a standard JEP106 register that provides key information about the MMU-600 hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-41. SMMU_PIDR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REVAND				CMOD			
R-0h								R-2h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 5-83. SMMU_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	REVAND	R	2h	MMU-600 minor revision. The value indicates minor product revision pY.
3-0	CMOD	R	0h	Customer modification number. Do not modify this number unless you have permission from ARM.

Table 5-84. Register Call Summary for SMMU_PIDR3

TCU_CFG Registers

- [SMMU_PIDR3 Register \(Offset = 00FECh\) \[reset = 20h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.42 SMMU_CIDR0 Register (Offset = 00FF0h) [reset = Dh]

SMMU_CIDR0 is shown in [Figure 5-42](#) and described in [Table 5-85](#).

Return to [Summary Table](#).

This is the TCU Component Identification register 0. This register provides information that identifies the MMU-600 as an ARM component.

Figure 5-42. SMMU_CIDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PREAMBLE							
R-0h																								R-Dh							

LEGEND: R = Read Only; -n = value after reset

Table 5-85. SMMU_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PREAMBLE	R	Dh	The value 0x0D identifies the MMU-600 as an ARM component.

Table 5-86. Register Call Summary for SMMU_CIDR0

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_CIDR0 Register \(Offset = 00FF0h\) \[reset = Dh\]](#): [0]

5.1.43 SMMU_CIDR1 Register (Offset = 00FF4h) [reset = F0h]

SMMU_CIDR1 is shown in [Figure 5-43](#) and described in [Table 5-87](#).

Return to [Summary Table](#).

This is the TCU Component Identification register 1. This register provides information that identifies the MMU-600 as an ARM component.

Figure 5-43. SMMU_CIDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLASS				PREAMBLE			
R-0h								R-Fh				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 5-87. SMMU_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	CLASS	R	Fh	The value 0xF identifies the MMU-600 as an ARM CoreLink component.
3-0	PREAMBLE	R	0h	The value 0x0 identifies the MMU-600 as an ARM component.

Table 5-88. Register Call Summary for SMMU_CIDR1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_CIDR1 Register \(Offset = 00FF4h\) \[reset = F0h\]](#): [0]

5.1.44 SMMU_CIDR2 Register (Offset = 00FF8h) [reset = 5h]

SMMU_CIDR2 is shown in [Figure 5-44](#) and described in [Table 5-89](#).

Return to [Summary Table](#).

This is the TCU Component Identification register 2. This register provides information that identifies the MMU-600 as an ARM component.

Figure 5-44. SMMU_CIDR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PREAMBLE							
R-0h																								R-5h							

LEGEND: R = Read Only; -n = value after reset

Table 5-89. SMMU_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PREAMBLE	R	5h	The value 0x05 identifies the MMU-600 as an ARM component.

Table 5-90. Register Call Summary for SMMU_CIDR2

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_CIDR2 Register \(Offset = 00FF8h\) \[reset = 5h\]: \[0\]](#)

5.1.45 SMMU_CIDR3 Register (Offset = 00FFCh) [reset = B1h]

SMMU_CIDR3 is shown in [Figure 5-45](#) and described in [Table 5-91](#).

Return to [Summary Table](#).

This is the TCU Component Identification register 3. This register provides information that identifies the MMU-600 as an ARM component.

Figure 5-45. SMMU_CIDR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PREAMBLE							
R-0h																								R-B1h							

LEGEND: R = Read Only; -n = value after reset

Table 5-91. SMMU_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PREAMBLE	R	B1h	The value 0xB1 identifies the MMU-600 as an ARM component.

Table 5-92. Register Call Summary for SMMU_CIDR3

TCU_CFG Registers

- [SMMU_CIDR3 Register \(Offset = 00FFCh\) \[reset = B1h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.46 SMMU_PMC_G_EVTYPER0 Register (Offset = 02400h) [reset = 0h]

SMMU_PMC_G_EVTYPER0 is shown in [Figure 5-46](#) and described in [Table 5-93](#).

Return to [Summary Table](#).

SMMU_PMC_G_EVTYPER0

Figure 5-46. SMMU_PMC_G_EVTYPER0 Register

31	30	29	28	27	26	25	24
OVFCAP	FILTER_SEC_S ID	FILTER_SID_S PAN	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R-0h				
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EVNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-93. SMMU_PMC_G_EVTYPER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVFCAP	R/W	0h	OVFCAP
30	FILTER_SEC_SID	R/W	0h	FILTER_SEC_SID
29	FILTER_SID_SPAN	R/W	0h	FILTER_SID_SPAN
28-8	RESERVED	R	0h	Reserved_28_8
7-0	EVNT	R/W	0h	EVNT

Table 5-94. Register Call Summary for SMMU_PMC_G_EVTYPER0

TCU_CFG Registers

- [SMMU_PMC_G_EVTYPER0 Register \(Offset = 02400h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.47 SMMU_PMC_G_EVTYPER1 Register (Offset = 02404h) [reset = 0h]

SMMU_PMC_G_EVTYPER1 is shown in Figure 5-47 and described in Table 5-95.

Return to [Summary Table](#).

SMMU_PMC_G_EVTYPER1

Figure 5-47. SMMU_PMC_G_EVTYPER1 Register

31	30	29	28	27	26	25	24
OVFCAP	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EVNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-95. SMMU_PMC_G_EVTYPER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVFCAP	R/W	0h	OVFCAP
30-8	RESERVED	R	0h	Reserved_30_8
7-0	EVNT	R/W	0h	EVNT

Table 5-96. Register Call Summary for SMMU_PMC_G_EVTYPER1

TCU_CFG Registers

- [SMMU_PMC_G_EVTYPER1 Register \(Offset = 02404h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.48 SMMU_PMC_G_EVTYPER2 Register (Offset = 02408h) [reset = 0h]

SMMU_PMC_G_EVTYPER2 is shown in [Figure 5-48](#) and described in [Table 5-97](#).

[Return to Summary Table.](#)

SMMU_PMC_G_EVTYPER2

Figure 5-48. SMMU_PMC_G_EVTYPER2 Register

31	30	29	28	27	26	25	24
OVFCAP	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EVNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-97. SMMU_PMC_G_EVTYPER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVFCAP	R/W	0h	OVFCAP
30-8	RESERVED	R	0h	Reserved_30_8
7-0	EVNT	R/W	0h	EVNT

Table 5-98. Register Call Summary for SMMU_PMC_G_EVTYPER2

TCU_CFG Registers

- [SMMU_PMC_G_EVTYPER2 Register \(Offset = 02408h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.49 SMMU_PMC_G_EVTYPER3 Register (Offset = 0240Ch) [reset = 0h]

SMMU_PMC_G_EVTYPER3 is shown in [Figure 5-49](#) and described in [Table 5-99](#).

[Return to Summary Table.](#)

SMMU_PMC_G_EVTYPER3

Figure 5-49. SMMU_PMC_G_EVTYPER3 Register

31	30	29	28	27	26	25	24
OVFCAP	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
EVNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-99. SMMU_PMC_G_EVTYPER3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVFCAP	R/W	0h	OVFCAP
30-8	RESERVED	R	0h	Reserved_30_8
7-0	EVNT	R/W	0h	EVNT

Table 5-100. Register Call Summary for SMMU_PMC_G_EVTYPER3

TCU_CFG Registers

- [SMMU_PMC_G_EVTYPER3 Register \(Offset = 0240Ch\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.50 SMMU_PMCG_SMR0 Register (Offset = 02A00h) [reset = 0h]

SMMU_PMCG_SMR0 is shown in [Figure 5-50](#) and described in [Table 5-101](#).

Return to [Summary Table](#).

SMMU_PMCG_SMR0

Figure 5-50. SMMU_PMCG_SMR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								STREAMID																							
R-0h								R/W-0h																							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-101. SMMU_PMCG_SMR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved_31_24
23-0	STREAMID	R/W	0h	STREAMID

Table 5-102. Register Call Summary for SMMU_PMCG_SMR0

TCU_CFG Registers

- [SMMU_PMCG_SMR0 Register \(Offset = 02A00h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.51 SMMU_PMC_G_CNTENSET0 Register (Offset = 02C00h) [reset = 0h]

SMMU_PMC_G_CNTENSET0 is shown in [Figure 5-51](#) and described in [Table 5-103](#).

Return to [Summary Table](#).

SMMU_PMC_G_CNTENSET0

Figure 5-51. SMMU_PMC_G_CNTENSET0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CNTEN			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-103. SMMU_PMC_G_CNTENSET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3-0	CNTEN	R/W	0h	CNTEN

Table 5-104. Register Call Summary for SMMU_PMC_G_CNTENSET0

TCU_CFG Registers

- [SMMU_PMC_G_CNTENSET0 Register \(Offset = 02C00h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.52 SMMU_PMC_G_CNTENCLR0 Register (Offset = 02C20h) [reset = 0h]

SMMU_PMC_G_CNTENCLR0 is shown in [Figure 5-52](#) and described in [Table 5-105](#).

Return to [Summary Table](#).

SMMU_PMC_G_CNTENCLR0

Figure 5-52. SMMU_PMC_G_CNTENCLR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CNTEN			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-105. SMMU_PMC_G_CNTENCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3-0	CNTEN	R/W	0h	CNTEN

Table 5-106. Register Call Summary for SMMU_PMC_G_CNTENCLR0

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_PMC_G_CNTENCLR0 Register \(Offset = 02C20h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.53 SMMU_PMC_G_INTENSET0 Register (Offset = 02C40h) [reset = 0h]

SMMU_PMC_G_INTENSET0 is shown in [Figure 5-53](#) and described in [Table 5-107](#).

Return to [Summary Table](#).

SMMU_PMC_G_INTENSET0

Figure 5-53. SMMU_PMC_G_INTENSET0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												INTEN			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-107. SMMU_PMC_G_INTENSET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3-0	INTEN	R/W	0h	INTEN

Table 5-108. Register Call Summary for SMMU_PMC_G_INTENSET0

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_PMC_G_INTENSET0 Register \(Offset = 02C40h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.54 SMMU_PMCg_INTENCLR0 Register (Offset = 02C60h) [reset = 0h]

SMMU_PMCg_INTENCLR0 is shown in [Figure 5-54](#) and described in [Table 5-109](#).

Return to [Summary Table](#).

SMMU_PMCg_INTENCLR0

Figure 5-54. SMMU_PMCg_INTENCLR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												INTEN			
R-0h												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-109. SMMU_PMCg_INTENCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3-0	INTEN	R/W	0h	INTEN

Table 5-110. Register Call Summary for SMMU_PMCg_INTENCLR0

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_PMCg_INTENCLR0 Register \(Offset = 02C60h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.55 SMMU_PMC_G_SCR Register (Offset = 02DF8h) [reset = 80000002h]

SMMU_PMC_G_SCR is shown in [Figure 5-55](#) and described in [Table 5-111](#).

Return to [Summary Table](#).

SMMU_PMC_G_SCR

Figure 5-55. SMMU_PMC_G_SCR Register

31	30	29	28	27	26	25	24
READS_AS_ONE	RESERVED						
R/W-1h				R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					NSMSI	NSRA	SO
R-0h					R/W-0h	R/W-1h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-111. SMMU_PMC_G_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	READS_AS_ONE	R/W	1h	READS_AS_ONE
30-3	RESERVED	R	0h	Reserved_30_3
2	NSMSI	R/W	0h	NSMSI
1	NSRA	R/W	1h	NSRA
0	SO	R/W	0h	SO

Table 5-112. Register Call Summary for SMMU_PMC_G_SCR

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_PMC_G_SCR Register \(Offset = 02DF8h\) \[reset = 80000002h\]: \[0\] \[1\]](#)

5.1.56 SMMU_PMCGR_CFGR Register (Offset = 02E00h) [reset = 00D01F03h]

SMMU_PMCGR_CFGR is shown in Figure 5-56 and described in Table 5-113.

Return to [Summary Table](#).

SMMU_PMCGR_CFGR

Figure 5-56. SMMU_PMCGR_CFGR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
SID_FILTER_T YPE	CAPTURE	MSI	RELOC_CTRS	RESERVED			
R-1h	R-1h	R-0h	R-1h	R-0h			
15	14	13	12	11	10	9	8
RESERVED		SIZE					
R-0h		R-1Fh					
7	6	5	4	3	2	1	0
RESERVED		NCTR					
R-0h		R-3h					

LEGEND: R = Read Only; -n = value after reset

Table 5-113. SMMU_PMCGR_CFGR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved_31_24
23	SID_FILTER_TYPE	R	1h	SID_FILTER_TYPE
22	CAPTURE	R	1h	CAPTURE
21	MSI	R	0h	MSI
20	RELOC_CTRS	R	1h	RELOC_CTRS
19-14	RESERVED	R	0h	Reserved_19_14
13-8	SIZE	R	1Fh	SIZE
7-6	RESERVED	R	0h	Reserved_7_6
5-0	NCTR	R	3h	NCTR

Table 5-114. Register Call Summary for SMMU_PMCGR_CFGR

TCU_CFG Registers

- [SMMU_PMCGR_CFGR Register \(Offset = 02E00h\) \[reset = 00D01F03h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.57 SMMU_PMCG_CR Register (Offset = 02E04h) [reset = 0h]

SMMU_PMCG_CR is shown in [Figure 5-57](#) and described in [Table 5-115](#).

Return to [Summary Table](#).

SMMU_PMCG_CR

Figure 5-57. SMMU_PMCG_CR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															E
R-0h																															R/ W- 0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-115. SMMU_PMCG_CR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved_31_1
0	E	R/W	0h	E

Table 5-116. Register Call Summary for SMMU_PMCG_CR

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_CR Register \(Offset = 02E04h\) \[reset = 0h\]](#): [0] [1]

5.1.58 SMMU_PMC_G_CEID0_LO Register (Offset = 02E20h) [reset = 7Fh]

SMMU_PMC_G_CEID0_LO is shown in [Figure 5-58](#) and described in [Table 5-117](#).

Return to [Summary Table](#).

SMMU_PMC_G_CEID0_LO

Figure 5-58. SMMU_PMC_G_CEID0_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N																															
R-7Fh																															

LEGEND: R = Read Only; -n = value after reset

Table 5-117. SMMU_PMC_G_CEID0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	N	R	7Fh	N

Table 5-118. Register Call Summary for SMMU_PMC_G_CEID0_LO

TCU_CFG Registers

- [SMMU_PMC_G_CEID0_LO Register \(Offset = 02E20h\) \[reset = 7Fh\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.59 SMMU_PMCG_CEID0_HI Register (Offset = 02E24h) [reset = 0h]

SMMU_PMCG_CEID0_HI is shown in [Figure 5-59](#) and described in [Table 5-119](#).

Return to [Summary Table](#).

SMMU_PMCG_CEID0_HI

Figure 5-59. SMMU_PMCG_CEID0_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-119. SMMU_PMCG_CEID0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	N	R	0h	N

Table 5-120. Register Call Summary for SMMU_PMCG_CEID0_HI

TCU_CFG Registers

- [SMMU_PMCG_CEID0_HI Register \(Offset = 02E24h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.60 SMMU_PMC_G_CEID1_LO Register (Offset = 02E28h) [reset = 0h]

SMMU_PMC_G_CEID1_LO is shown in [Figure 5-60](#) and described in [Table 5-121](#).

Return to [Summary Table](#).

SMMU_PMC_G_CEID1_LO

Figure 5-60. SMMU_PMC_G_CEID1_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-121. SMMU_PMC_G_CEID1_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	N	R	0h	N

Table 5-122. Register Call Summary for SMMU_PMC_G_CEID1_LO

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMC_G_CEID1_LO Register \(Offset = 02E28h\) \[reset = 0h\]](#): [0] [1]

5.1.61 SMMU_PMCG_CEID1_HI Register (Offset = 02E2Ch) [reset = 0h]

SMMU_PMCG_CEID1_HI is shown in [Figure 5-61](#) and described in [Table 5-123](#).

Return to [Summary Table](#).

SMMU_PMCG_CEID1_HI

Figure 5-61. SMMU_PMCG_CEID1_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-123. SMMU_PMCG_CEID1_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	N	R	0h	N

Table 5-124. Register Call Summary for SMMU_PMCG_CEID1_HI

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_CEID1_HI Register \(Offset = 02E2Ch\) \[reset = 0h\]](#): [0] [1]

5.1.62 SMMU_PMCGR_IRQ_CTRL Register (Offset = 02E50h) [reset = 0h]

SMMU_PMCGR_IRQ_CTRL is shown in [Figure 5-62](#) and described in [Table 5-125](#).

[Return to Summary Table.](#)

[SMMU_PMCGR_IRQ_CTRL](#)

Figure 5-62. SMMU_PMCGR_IRQ_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							IRQEN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-125. SMMU_PMCGR_IRQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved_31_1
0	IRQEN	R/W	0h	IRQEN

Table 5-126. Register Call Summary for SMMU_PMCGR_IRQ_CTRL

TCU_CFG Registers

- [SMMU_PMCGR_IRQ_CTRL Register \(Offset = 02E50h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.63 SMMU_PMCGR_IRQ_CTRLACK Register (Offset = 02E54h) [reset = 0h]

SMMU_PMCGR_IRQ_CTRLACK is shown in [Figure 5-63](#) and described in [Table 5-127](#).

Return to [Summary Table](#).

SMMU_PMCGR_IRQ_CTRLACK

Figure 5-63. SMMU_PMCGR_IRQ_CTRLACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							IRQEN
R-0h							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-127. SMMU_PMCGR_IRQ_CTRLACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved_31_1
0	IRQEN	R	0h	IRQEN

Table 5-128. Register Call Summary for SMMU_PMCGR_IRQ_CTRLACK

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCGR_IRQ_CTRLACK Register \(Offset = 02E54h\) \[reset = 0h\]](#): [0] [1]

5.1.64 SMMU_PMCG_AIDR Register (Offset = 02E70h) [reset = 1h]

SMMU_PMCG_AIDR is shown in [Figure 5-64](#) and described in [Table 5-129](#).

Return to [Summary Table](#).

[SMMU_PMCG_AIDR](#)

Figure 5-64. SMMU_PMCG_AIDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								ARCHMAJORREV				ARCHMINORREV			
R-0h								R-0h				R-1h			

LEGEND: R = Read Only; -n = value after reset

Table 5-129. SMMU_PMCG_AIDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	ARCHMAJORREV	R	0h	ARCHMAJORREV
3-0	ARCHMINORREV	R	1h	ARCHMINORREV

Table 5-130. Register Call Summary for SMMU_PMCG_AIDR

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_AIDR Register \(Offset = 02E70h\) \[reset = 1h\]](#): [0] [1]

5.1.65 SMMU_PMC_G_PMAUTHSTATUS Register (Offset = 02FB8h) [reset = 0h]

SMMU_PMC_G_PMAUTHSTATUS is shown in [Figure 5-65](#) and described in [Table 5-131](#).

Return to [Summary Table](#).

SMMU_PMC_G_PMAUTHSTATUS

Figure 5-65. SMMU_PMC_G_PMAUTHSTATUS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
SNI	SNE	SI	SE	NSNI	NSNE	NSI	NSE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-131. SMMU_PMC_G_PMAUTHSTATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7	SNI	R	0h	SNI
6	SNE	R	0h	SNE
5	SI	R	0h	SI
4	SE	R	0h	SE
3	NSNI	R	0h	NSNI
2	NSNE	R	0h	NSNE
1	NSI	R	0h	NSI
0	NSE	R	0h	NSE

Table 5-132. Register Call Summary for SMMU_PMC_G_PMAUTHSTATUS

TCU_CFG Registers

- [SMMU_PMC_G_PMAUTHSTATUS Register \(Offset = 02FB8h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.66 SMMU_PMC_G_PMDEVARCH Register (Offset = 02FBCh) [reset = 47702A56h]

SMMU_PMC_G_PMDEVARCH is shown in [Figure 5-66](#) and described in [Table 5-133](#).

Return to [Summary Table](#).

SMMU_PMC_G_PMDEVARCH

Figure 5-66. SMMU_PMC_G_PMDEVARCH Register

31	30	29	28	27	26	25	24
ARCHITECT							
R-23Bh							
23	22	21	20	19	18	17	16
ARCHITECT			PRESENT	REVISION			
R-23Bh			R-1h	R-0h			
15	14	13	12	11	10	9	8
ARCHID							
R-2A56h							
7	6	5	4	3	2	1	0
ARCHID							
R-2A56h							

LEGEND: R = Read Only; -n = value after reset

Table 5-133. SMMU_PMC_G_PMDEVARCH Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	ARCHITECT	R	23Bh	ARCHITECT
20	PRESENT	R	1h	PRESENT
19-16	REVISION	R	0h	REVISION
15-0	ARCHID	R	2A56h	ARCHID

Table 5-134. Register Call Summary for SMMU_PMC_G_PMDEVARCH

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMC_G_PMDEVARCH Register \(Offset = 02FBCh\) \[reset = 47702A56h\]](#): [0] [1]

5.1.67 SMMU_PMC_G_PMDEVTYPE Register (Offset = 02FCCh) [reset = 56h]

SMMU_PMC_G_PMDEVTYPE is shown in [Figure 5-67](#) and described in [Table 5-135](#).

Return to [Summary Table](#).

SMMU_PMC_G_PMDEVTYPE

Figure 5-67. SMMU_PMC_G_PMDEVTYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SUB_TYPE				CLS			
R-0h								R-5h				R-6h			

LEGEND: R = Read Only; -n = value after reset

Table 5-135. SMMU_PMC_G_PMDEVTYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	SUB_TYPE	R	5h	SUB_TYPE
3-0	CLS	R	6h	CLS

Table 5-136. Register Call Summary for SMMU_PMC_G_PMDEVTYPE

TCU_CFG Registers

- [SMMU_PMC_G_PMDEVTYPE Register \(Offset = 02FCCh\) \[reset = 56h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.68 SMMU_PMC_G_PIDR4 Register (Offset = 02FD0h) [reset = 4h]

SMMU_PMC_G_PIDR4 is shown in Figure 5-68 and described in Table 5-137.

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This is the PMU Peripheral ID register 4. This is a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-68. SMMU_PMC_G_PIDR4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								SIZE				DES_2			
R-0h								R-0h				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 5-137. SMMU_PMC_G_PIDR4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	SIZE	R	0h	4KB region count.
3-0	DES_2	R	4h	JEP106 continuation code for ARM.

Table 5-138. Register Call Summary for SMMU_PMC_G_PIDR4

TCU_CFG Registers

- [SMMU_PMC_G_PIDR4 Register \(Offset = 02FD0h\) \[reset = 4h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.69 SMMU_PMCG_PIDR5 Register (Offset = 02FD4h) [reset = 0h]

SMMU_PMCG_PIDR5 is shown in [Figure 5-69](#) and described in [Table 5-139](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 5. This is a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-69. SMMU_PMCG_PIDR5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-139. SMMU_PMCG_PIDR5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	RESERVED	R	0h	Reserved.

Table 5-140. Register Call Summary for SMMU_PMCG_PIDR5

TCU_CFG Registers

- [SMMU_PMCG_PIDR5 Register \(Offset = 02FD4h\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.70 SMMU_PMCg_PIDR6 Register (Offset = 02FD8h) [reset = 0h]

SMMU_PMCg_PIDR6 is shown in [Figure 5-70](#) and described in [Table 5-141](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 6. This is a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-70. SMMU_PMCg_PIDR6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-141. SMMU_PMCg_PIDR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	RESERVED	R	0h	Reserved.

Table 5-142. Register Call Summary for SMMU_PMCg_PIDR6

TCU_CFG Registers

- [SMMU_PMCg_PIDR6 Register \(Offset = 02FD8h\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.71 SMMU_PMCG_PIDR7 Register (Offset = 02FDCh) [reset = 0h]

SMMU_PMCG_PIDR7 is shown in [Figure 5-71](#) and described in [Table 5-143](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 7, a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-71. SMMU_PMCG_PIDR7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RESERVED															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 5-143. SMMU_PMCG_PIDR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	RESERVED	R	0h	Reserved.

Table 5-144. Register Call Summary for SMMU_PMCG_PIDR7

TCU_CFG Registers

- [SMMU_PMCG_PIDR7 Register \(Offset = 02FDCh\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.72 SMMU_PMC_G_PIDR0 Register (Offset = 02FE0h) [reset = 83h]

SMMU_PMC_G_PIDR0 is shown in [Figure 5-72](#) and described in [Table 5-145](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 0, a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-72. SMMU_PMC_G_PIDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PART_0							
R-0h																								R-83h							

LEGEND: R = Read Only; -n = value after reset

Table 5-145. SMMU_PMC_G_PIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PART_0	R	83h	Part number [7:0].

Table 5-146. Register Call Summary for SMMU_PMC_G_PIDR0

TCU_CFG Registers
<ul style="list-style-type: none"> • TCU_CFG Registers: [0] • SMMU_PMC_G_PIDR0 Register (Offset = 02FE0h) [reset = 83h]: [0]

5.1.73 SMMU_PMCG_PIDR1 Register (Offset = 02FE4h) [reset = B4h]

SMMU_PMCG_PIDR1 is shown in [Figure 5-73](#) and described in [Table 5-147](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 1, a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-73. SMMU_PMCG_PIDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DES_0				PART_1			
R-0h								R-Bh				R-4h			

LEGEND: R = Read Only; -n = value after reset

Table 5-147. SMMU_PMCG_PIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	DES_0	R	Bh	JEP106 ID code [3:0] for ARM.
3-0	PART_1	R	4h	Part number [11:8].

Table 5-148. Register Call Summary for SMMU_PMCG_PIDR1

TCU_CFG Registers

- [SMMU_PMCG_PIDR1 Register \(Offset = 02FE4h\) \[reset = B4h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.74 SMMU_PMCG_PIDR2 Register (Offset = 02FE8h) [reset = Bh]

SMMU_PMCG_PIDR2 is shown in [Figure 5-74](#) and described in [Table 5-149](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 2, a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-74. SMMU_PMCG_PIDR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
REVISION				JEDEC		DES_1	
R-0h				R-1h		R-3h	

LEGEND: R = Read Only; -n = value after reset

Table 5-149. SMMU_PMCG_PIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	REVISION	R	0h	MMU-600 major revision. The value indicates major product revision rX.
3	JEDEC	R	1h	IC uses a manufacturer identity code that is allocated by JEDEC, according to the JEP106 specification.
2-0	DES_1	R	3h	JEP106 ID code [6:4] for ARM.

Table 5-150. Register Call Summary for SMMU_PMCG_PIDR2

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_PIDR2 Register \(Offset = 02FE8h\) \[reset = Bh\]](#): [0]

5.1.75 SMMU_PMCg_PIDR3 Register (Offset = 02FECh) [reset = 20h]

SMMU_PMCg_PIDR3 is shown in [Figure 5-75](#) and described in [Table 5-151](#).

Return to [Summary Table](#).

This is the PMU Peripheral ID register 3, a standard JEP106 register that provides key information about the MMU-600 PMU hardware. The least significant 8 bits of the eight Peripheral ID registers form a single 64-bit conceptual ID register.

Figure 5-75. SMMU_PMCg_PIDR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								REVAND				CMOD			
R-0h								R-2h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 5-151. SMMU_PMCg_PIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	REVAND	R	2h	MMU-600 minor revision. The value indicates minor product revision pY.
3-0	CMOD	R	0h	Customer modification number. Do not modify this number unless you have permission from ARM.

Table 5-152. Register Call Summary for SMMU_PMCg_PIDR3

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_PMCg_PIDR3 Register \(Offset = 02FECh\) \[reset = 20h\]: \[0\]](#)

5.1.76 SMMU_PMCG_CIDR0 Register (Offset = 02FF0h) [reset = Dh]

SMMU_PMCG_CIDR0 is shown in [Figure 5-76](#) and described in [Table 5-153](#).

Return to [Summary Table](#).

This is the PMU Component Identification register 0. This register provides information that identifies the MMU-600 PMU as an ARM component.

Figure 5-76. SMMU_PMCG_CIDR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PREAMBLE							
R-0h																								R-Dh							

LEGEND: R = Read Only; -n = value after reset

Table 5-153. SMMU_PMCG_CIDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PREAMBLE	R	Dh	The value 0x0D identifies the MMU-600 PMU as an ARM component.

Table 5-154. Register Call Summary for SMMU_PMCG_CIDR0

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_PMCG_CIDR0 Register (Offset = 02FF0h) [reset = Dh]: [0] TCU_CFG Registers: [0]

5.1.77 SMMU_PMCG_CIDR1 Register (Offset = 02FF4h) [reset = 90h]

SMMU_PMCG_CIDR1 is shown in [Figure 5-77](#) and described in [Table 5-155](#).

Return to [Summary Table](#).

This is the PMU Component Identification register 1. This register provides information that identifies the MMU-600 PMU as an ARM component.

Figure 5-77. SMMU_PMCG_CIDR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLASS				PREAMBLE			
R-0h								R-9h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 5-155. SMMU_PMCG_CIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-4	CLASS	R	9h	The value 0x9 identifies the MMU-600 as an ARM CoreSight component.
3-0	PREAMBLE	R	0h	The value 0x0 identifies the MMU-600 as an ARM component.

Table 5-156. Register Call Summary for SMMU_PMCG_CIDR1

TCU_CFG Registers

- [SMMU_PMCG_CIDR1 Register \(Offset = 02FF4h\) \[reset = 90h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.78 SMMU_PMCG_CIDR2 Register (Offset = 02FF8h) [reset = 5h]

SMMU_PMCG_CIDR2 is shown in [Figure 5-78](#) and described in [Table 5-157](#).

Return to [Summary Table](#).

This is the PMU Component Identification register 2. This register provides information that identifies the MMU-600 PMU as an ARM component.

Figure 5-78. SMMU_PMCG_CIDR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PREAMBLE							
R-0h																								R-5h							

LEGEND: R = Read Only; -n = value after reset

Table 5-157. SMMU_PMCG_CIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PREAMBLE	R	5h	The value 0x05 identifies the MMU-600 PMU as an ARM component.

Table 5-158. Register Call Summary for SMMU_PMCG_CIDR2

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_PMCG_CIDR2 Register (Offset = 02FF8h) [reset = 5h]: [0] TCU_CFG Registers: [0]

5.1.79 SMMU_PMCG_CIDR3 Register (Offset = 02FFCh) [reset = B1h]

SMMU_PMCG_CIDR3 is shown in [Figure 5-79](#) and described in [Table 5-159](#).

Return to [Summary Table](#).

This is the PMU Component Identification register 3. This register provides information that identifies the MMU-600 PMU as an ARM component.

Figure 5-79. SMMU_PMCG_CIDR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								PREAMBLE							
R-0h																								R-B1h							

LEGEND: R = Read Only; -n = value after reset

Table 5-159. SMMU_PMCG_CIDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-0	PREAMBLE	R	B1h	The value 0xB1 identifies the MMU-600 PMU as an ARM component.

Table 5-160. Register Call Summary for SMMU_PMCG_CIDR3

TCU_CFG Registers

- [SMMU_PMCG_CIDR3 Register \(Offset = 02FFCh\) \[reset = B1h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.80 SMMU_S_IDR0 Register (Offset = 08000h) [reset = 2000h]

SMMU_S_IDR0 is shown in [Figure 5-80](#) and described in [Table 5-161](#).

Return to [Summary Table](#).

SMMU_S_IDR0

Figure 5-80. SMMU_S_IDR0 Register

31	30	29	28	27	26	25	24
RESERVED						STALL_MODEL	
R-0h						R-0h	
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		MSI	RESERVED				
R-0h		R-1h	R-0h				
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 5-161. SMMU_S_IDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved_31_26
25-24	STALL_MODEL	R	0h	STALL_MODEL
23-14	RESERVED	R	0h	Reserved_23_14
13	MSI	R	1h	MSI
12-0	RESERVED	R	0h	Reserved_12_0

Table 5-162. Register Call Summary for SMMU_S_IDR0

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_IDR0 Register \(Offset = 08000h\) \[reset = 2000h\]: \[0\] \[1\]](#)

5.1.81 SMMU_S_IDR1 Register (Offset = 08004h) [reset = 80000018h]

SMMU_S_IDR1 is shown in [Figure 5-81](#) and described in [Table 5-163](#).

Return to [Summary Table](#).

SMMU_S_IDR1

Figure 5-81. SMMU_S_IDR1 Register

31	30	29	28	27	26	25	24
SECURE_IMPL	RESERVED						
R-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		S_SIDSIZE					
R-0h		R-18h					

LEGEND: R = Read Only; -n = value after reset

Table 5-163. SMMU_S_IDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SECURE_IMPL	R	1h	SECURE_IMPL
30-6	RESERVED	R	0h	Reserved_30_6
5-0	S_SIDSIZE	R	18h	S_SIDSIZE

Table 5-164. Register Call Summary for SMMU_S_IDR1

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_S_IDR1 Register (Offset = 08004h) [reset = 80000018h]: [0] [1] TCU_CFG Registers: [0]

5.1.82 SMMU_S_IDR3 Register (Offset = 0800Ch) [reset = 40h]

SMMU_S_IDR3 is shown in [Figure 5-82](#) and described in [Table 5-165](#).

Return to [Summary Table](#).

SMMU_S_IDR3

Figure 5-82. SMMU_S_IDR3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	SAMS	RESERVED					
R-0h	R-1h	R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 5-165. SMMU_S_IDR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R	0h	Reserved_31_7
6	SAMS	R	1h	SAMS
5-0	RESERVED	R	0h	Reserved_5_0

Table 5-166. Register Call Summary for SMMU_S_IDR3

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_IDR3 Register \(Offset = 0800Ch\) \[reset = 40h\]: \[0\] \[1\]](#)

5.1.83 SMMU_S_CR0 Register (Offset = 08020h) [reset = 0h]

SMMU_S_CR0 is shown in [Figure 5-83](#) and described in [Table 5-167](#).

Return to [Summary Table](#).

SMMU_S_CR0

Figure 5-83. SMMU_S_CR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						NSSTALLD	RESERVED
R-0h						R/W-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED		SIF	RESERVED	CMDQEN	EVENTQEN	RESERVED	SMMUEN
R-0h		R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-167. SMMU_S_CR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved_31_10
9	NSSTALLD	R/W	0h	NSSTALLD
8-6	RESERVED	R	0h	Reserved_8_6
5	SIF	R/W	0h	SIF
4	RESERVED	R	0h	Reserved_4_4
3	CMDQEN	R/W	0h	CMDQEN
2	EVENTQEN	R/W	0h	EVENTQEN
1	RESERVED	R	0h	Reserved_1_1
0	SMMUEN	R/W	0h	SMMUEN

Table 5-168. Register Call Summary for SMMU_S_CR0

TCU_CFG Registers

- [SMMU_S_CR0 Register \(Offset = 08020h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.84 SMMU_S_CR0ACK Register (Offset = 08024h) [reset = 0h]

SMMU_S_CR0ACK is shown in [Figure 5-84](#) and described in [Table 5-169](#).

Return to [Summary Table](#).

SMMU_S_CR0ACK

Figure 5-84. SMMU_S_CR0ACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED						NSSTALLD	RESERVED
R-0h						R/W-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED		SIF	RESERVED	CMDQEN	EVENTQEN	RESERVED	SMMUEN
R-0h		R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-169. SMMU_S_CR0ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved_31_10
9	NSSTALLD	R/W	0h	NSSTALLD
8-6	RESERVED	R	0h	Reserved_8_6
5	SIF	R/W	0h	SIF
4	RESERVED	R	0h	Reserved_4_4
3	CMDQEN	R/W	0h	CMDQEN
2	EVENTQEN	R/W	0h	EVENTQEN
1	RESERVED	R	0h	Reserved_1_1
0	SMMUEN	R/W	0h	SMMUEN

Table 5-170. Register Call Summary for SMMU_S_CR0ACK

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_CR0ACK Register \(Offset = 08024h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.85 SMMU_S_CR1 Register (Offset = 08028h) [reset = 0h]

SMMU_S_CR1 is shown in [Figure 5-85](#) and described in [Table 5-171](#).

Return to [Summary Table](#).

SMMU_S_CR1

Figure 5-85. SMMU_S_CR1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				TABLE_SH		TABLE_OC	
R-0h				R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
TABLE_IC		QUEUE_SH		QUEUE_OC		QUEUE_IC	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-171. SMMU_S_CR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved_31_12
11-10	TABLE_SH	R/W	0h	TABLE_SH
9-8	TABLE_OC	R/W	0h	TABLE_OC
7-6	TABLE_IC	R/W	0h	TABLE_IC
5-4	QUEUE_SH	R/W	0h	QUEUE_SH
3-2	QUEUE_OC	R/W	0h	QUEUE_OC
1-0	QUEUE_IC	R/W	0h	QUEUE_IC

Table 5-172. Register Call Summary for SMMU_S_CR1

TCU_CFG Registers

- [SMMU_S_CR1 Register \(Offset = 08028h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.86 SMMU_S_CR2 Register (Offset = 0802Ch) [reset = 0h]

SMMU_S_CR2 is shown in [Figure 5-86](#) and described in [Table 5-173](#).

Return to [Summary Table](#).

SMMU_S_CR2

Figure 5-86. SMMU_S_CR2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					PTM	RECINVSID	RESERVED
R-0h					R/W-0h	R/W-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-173. SMMU_S_CR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved_31_3
2	PTM	R/W	0h	PTM
1	RECINVSID	R/W	0h	RECINVSID
0	RESERVED	R	0h	Reserved_0_0

Table 5-174. Register Call Summary for SMMU_S_CR2

TCU_CFG Registers

- [SMMU_S_CR2 Register \(Offset = 0802Ch\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.87 SMMU_S_INIT Register (Offset = 0803Ch) [reset = 0h]

SMMU_S_INIT is shown in [Figure 5-87](#) and described in [Table 5-175](#).

Return to [Summary Table](#).

SMMU_S_INIT

Figure 5-87. SMMU_S_INIT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							INV_ALL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-175. SMMU_S_INIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved_31_1
0	INV_ALL	R/W	0h	INV_ALL

Table 5-176. Register Call Summary for SMMU_S_INIT

TCU_CFG Registers

- [SMMU_S_INIT Register \(Offset = 0803Ch\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)
- [TCU_SCR Register \(Offset = 08E18h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.88 SMMU_S_GBPA Register (Offset = 08044h) [reset = 0h]

SMMU_S_GBPA is shown in [Figure 5-88](#) and described in [Table 5-177](#).

Return to [Summary Table](#).

SMMU_S_GBPA

Figure 5-88. SMMU_S_GBPA Register

31	30	29	28	27	26	25	24
UPDATE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED			ABORT	INSTCFG		PRIVCFG	
R-0h			R/W-0h	R/W-0h		R/W-0h	
15	14	13	12	11	10	9	8
NSCFG		SHCFG		ALLOCCFG			
R/W-0h		R/W-0h		R/W-0h			
7	6	5	4	3	2	1	0
RESERVED			MTCFG	MEMATTR			
R-0h			R/W-0h	R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-177. SMMU_S_GBPA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UPDATE	R/W	0h	Update
30-21	RESERVED	R	0h	Reserved_30_21
20	ABORT	R/W	0h	ABORT
19-18	INSTCFG	R/W	0h	INSTCFG
17-16	PRIVCFG	R/W	0h	PRIVCFG
15-14	NSCFG	R/W	0h	NSCFG
13-12	SHCFG	R/W	0h	SHCFG
11-8	ALLOCCFG	R/W	0h	ALLOCCFG
7-5	RESERVED	R	0h	Reserved_7_5
4	MTCFG	R/W	0h	MTCFG
3-0	MEMATTR	R/W	0h	MemAttr

Table 5-178. Register Call Summary for SMMU_S_GBPA

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_GBPA Register \(Offset = 08044h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.89 SMMU_S_IRQ_CTRL Register (Offset = 08050h) [reset = 0h]

SMMU_S_IRQ_CTRL is shown in [Figure 5-89](#) and described in [Table 5-179](#).

Return to [Summary Table](#).

SMMU_S_IRQ_CTRL

Figure 5-89. SMMU_S_IRQ_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					EVENTQ_IRQE N	RESERVED	GERROR_IRQ EN
R-0h					R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-179. SMMU_S_IRQ_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved_31_3
2	EVENTQ_IRQEN	R/W	0h	EVENTQ_IRQEN
1	RESERVED	R	0h	Reserved_1_1
0	GERROR_IRQEN	R/W	0h	GERROR_IRQEN

Table 5-180. Register Call Summary for SMMU_S_IRQ_CTRL

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_IRQ_CTRL Register \(Offset = 08050h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.90 SMMU_S_IRQ_CTRLACK Register (Offset = 08054h) [reset = 0h]

SMMU_S_IRQ_CTRLACK is shown in [Figure 5-90](#) and described in [Table 5-181](#).

Return to [Summary Table](#).

SMMU_S_IRQ_CTRLACK

Figure 5-90. SMMU_S_IRQ_CTRLACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					EVENTQ_IRQE N	RESERVED	GERROR_IRQ EN
R-0h					R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-181. SMMU_S_IRQ_CTRLACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved_31_3
2	EVENTQ_IRQEN	R	0h	EVENTQ_IRQEN
1	RESERVED	R	0h	Reserved_1_1
0	GERROR_IRQEN	R	0h	GERROR_IRQEN

Table 5-182. Register Call Summary for SMMU_S_IRQ_CTRLACK

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_IRQ_CTRLACK Register \(Offset = 08054h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.91 SMMU_S_GERROR Register (Offset = 08060h) [reset = 0h]

SMMU_S_GERROR is shown in [Figure 5-91](#) and described in [Table 5-183](#).

Return to [Summary Table](#).

SMMU_S_GERROR

Figure 5-91. SMMU_S_GERROR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
MSI_GERROR_ABT_ERR	RESERVED	MSI_EVENTQ_ABT_ERR	MSI_CMDQ_ABT_ERR	RESERVED	EVENTQ_ABT_ERR	RESERVED	CMDQ_ERR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-183. SMMU_S_GERROR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7	MSI_GERROR_ABT_ERR	R	0h	MSI_GERROR_ABT_ERR
6	RESERVED	R	0h	Reserved_6_6
5	MSI_EVENTQ_ABT_ERR	R	0h	MSI_EVENTQ_ABT_ERR
4	MSI_CMDQ_ABT_ERR	R	0h	MSI_CMDQ_ABT_ERR
3	RESERVED	R	0h	Reserved_3_3
2	EVENTQ_ABT_ERR	R	0h	EVENTQ_ABT_ERR
1	RESERVED	R	0h	Reserved_1_1
0	CMDQ_ERR	R	0h	CMDQ_ERR

Table 5-184. Register Call Summary for SMMU_S_GERROR

TCU_CFG Registers
<ul style="list-style-type: none"> • TCU_CFG Registers: [0] • SMMU_S_GERROR Register (Offset = 08060h) [reset = 0h]: [0] [1]

5.1.92 SMMU_S_GERRORN Register (Offset = 08064h) [reset = 0h]

SMMU_S_GERRORN is shown in Figure 5-92 and described in Table 5-185.

Return to [Summary Table](#).

SMMU_S_GERRORN

Figure 5-92. SMMU_S_GERRORN Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
MSI_GERROR_ABT_ERR	RESERVED	MSI_EVENTQ_ABT_ERR	MSI_CMDQ_ABT_ERR	RESERVED	EVENTQ_ABT_ERR	RESERVED	CMDQ_ERR
R/W-0h	R-0h	R/W-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-185. SMMU_S_GERRORN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7	MSI_GERROR_ABT_ERR	R/W	0h	MSI_GERROR_ABT_ERR
6	RESERVED	R	0h	Reserved_6_6
5	MSI_EVENTQ_ABT_ERR	R/W	0h	MSI_EVENTQ_ABT_ERR
4	MSI_CMDQ_ABT_ERR	R/W	0h	MSI_CMDQ_ABT_ERR
3	RESERVED	R	0h	Reserved_3_3
2	EVENTQ_ABT_ERR	R/W	0h	EVENTQ_ABT_ERR
1	RESERVED	R	0h	Reserved_1_1
0	CMDQ_ERR	R/W	0h	CMDQ_ERR

Table 5-186. Register Call Summary for SMMU_S_GERRORN

TCU_CFG Registers

- [SMMU_S_GERRORN Register \(Offset = 08064h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.93 SMMU_S_GERROR_IRQ_CFG0_LO Register (Offset = 08068h) [reset = 0h]

SMMU_S_GERROR_IRQ_CFG0_LO is shown in [Figure 5-93](#) and described in [Table 5-187](#).

Return to [Summary Table](#).

SMMU_S_GERROR_IRQ_CFG0_LO

Figure 5-93. SMMU_S_GERROR_IRQ_CFG0_LO Register

31	30	29	28	27	26	25	24
ADDR							
R/W-0h							
23	22	21	20	19	18	17	16
ADDR							
R/W-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR						RESERVED	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-187. SMMU_S_GERROR_IRQ_CFG0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R/W	0h	ADDR
1-0	RESERVED	R	0h	Reserved_1_0

Table 5-188. Register Call Summary for SMMU_S_GERROR_IRQ_CFG0_LO

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_GERROR_IRQ_CFG0_LO Register \(Offset = 08068h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.94 SMMU_S_GERROR_IRQ_CFG0_HI Register (Offset = 0806Ch) [reset = 0h]

SMMU_S_GERROR_IRQ_CFG0_HI is shown in [Figure 5-94](#) and described in [Table 5-189](#).

Return to [Summary Table](#).

SMMU_S_GERROR_IRQ_CFG0_HI

Figure 5-94. SMMU_S_GERROR_IRQ_CFG0_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-189. SMMU_S_GERROR_IRQ_CFG0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved_31_16
15-0	ADDR	R/W	0h	ADDR

Table 5-190. Register Call Summary for SMMU_S_GERROR_IRQ_CFG0_HI

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_S_GERROR_IRQ_CFG0_HI Register \(Offset = 0806Ch\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.95 SMMU_S_GERROR_IRQ_CFG1 Register (Offset = 08070h) [reset = 0h]

SMMU_S_GERROR_IRQ_CFG1 is shown in [Figure 5-95](#) and described in [Table 5-191](#).

Return to [Summary Table](#).

SMMU_S_GERROR_IRQ_CFG1

Figure 5-95. SMMU_S_GERROR_IRQ_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-191. SMMU_S_GERROR_IRQ_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	DATA

Table 5-192. Register Call Summary for SMMU_S_GERROR_IRQ_CFG1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_S_GERROR_IRQ_CFG1 Register \(Offset = 08070h\) \[reset = 0h\]](#): [0] [1]

5.1.96 SMMU_S_GERROR_IRQ_CFG2 Register (Offset = 08074h) [reset = 0h]

SMMU_S_GERROR_IRQ_CFG2 is shown in [Figure 5-96](#) and described in [Table 5-193](#).

Return to [Summary Table](#).

SMMU_S_GERROR_IRQ_CFG2

Figure 5-96. SMMU_S_GERROR_IRQ_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SH		MEMATTR			
R-0h										R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-193. SMMU_S_GERROR_IRQ_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved_31_6
5-4	SH	R/W	0h	SH
3-0	MEMATTR	R/W	0h	MemAttr

Table 5-194. Register Call Summary for SMMU_S_GERROR_IRQ_CFG2

TCU_CFG Registers

- [SMMU_S_GERROR_IRQ_CFG2 Register \(Offset = 08074h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.97 SMMU_S_STRTAB_BASE_LO Register (Offset = 08080h) [reset = 0h]

SMMU_S_STRTAB_BASE_LO is shown in [Figure 5-97](#) and described in [Table 5-195](#).

Return to [Summary Table](#).

SMMU_S_STRTAB_BASE_LO

Figure 5-97. SMMU_S_STRTAB_BASE_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR										RESERVED					
R/W-0h										R-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-195. SMMU_S_STRTAB_BASE_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	ADDR	R/W	0h	ADDR
5-0	RESERVED	R	0h	Reserved_5_0

Table 5-196. Register Call Summary for SMMU_S_STRTAB_BASE_LO

TCU_CFG Registers

- [SMMU_S_STRTAB_BASE_LO Register \(Offset = 08080h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.98 SMMU_S_STRTAB_BASE_HI Register (Offset = 08084h) [reset = 0h]

SMMU_S_STRTAB_BASE_HI is shown in [Figure 5-98](#) and described in [Table 5-197](#).

Return to [Summary Table](#).

SMMU_S_STRTAB_BASE_HI

Figure 5-98. SMMU_S_STRTAB_BASE_HI Register

31	30	29	28	27	26	25	24
RESERVED	RA	RESERVED					
R-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-197. SMMU_S_STRTAB_BASE_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	RA	R/W	0h	RA
29-16	RESERVED	R	0h	Reserved_29_16
15-0	ADDR	R/W	0h	ADDR

Table 5-198. Register Call Summary for SMMU_S_STRTAB_BASE_HI

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_S_STRTAB_BASE_HI Register \(Offset = 08084h\) \[reset = 0h\]](#): [0] [1]

5.1.99 SMMU_S_STRTAB_BASE_CFG Register (Offset = 08088h) [reset = 0h]

SMMU_S_STRTAB_BASE_CFG is shown in [Figure 5-99](#) and described in [Table 5-199](#).

Return to [Summary Table](#).

SMMU_S_STRTAB_BASE_CFG

Figure 5-99. SMMU_S_STRTAB_BASE_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED													FMT		
R-0h													R/W-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					SPLIT					LOG2SIZE					
R-0h					R/W-0h					R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-199. SMMU_S_STRTAB_BASE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved_31_18
17-16	FMT	R/W	0h	FMT
15-11	RESERVED	R	0h	Reserved_15_11
10-6	SPLIT	R/W	0h	SPLIT
5-0	LOG2SIZE	R/W	0h	LOG2SIZE

Table 5-200. Register Call Summary for SMMU_S_STRTAB_BASE_CFG

TCU_CFG Registers

- [SMMU_S_STRTAB_BASE_CFG Register \(Offset = 08088h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.100 SMMU_S_CMDQ_BASE_LO Register (Offset = 08090h) [reset = 0h]

SMMU_S_CMDQ_BASE_LO is shown in [Figure 5-100](#) and described in [Table 5-201](#).

Return to [Summary Table](#).

SMMU_S_CMDQ_BASE_LO

Figure 5-100. SMMU_S_CMDQ_BASE_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR											LOG2SIZE				
R/W-0h											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-201. SMMU_S_CMDQ_BASE_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	ADDR	R/W	0h	ADDR
4-0	LOG2SIZE	R/W	0h	LOG2SIZE

Table 5-202. Register Call Summary for SMMU_S_CMDQ_BASE_LO

TCU_CFG Registers

- [SMMU_S_CMDQ_BASE_LO Register \(Offset = 08090h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.101 SMMU_S_CMDQ_BASE_HI Register (Offset = 08094h) [reset = 0h]

SMMU_S_CMDQ_BASE_HI is shown in [Figure 5-101](#) and described in [Table 5-203](#).

Return to [Summary Table](#).

SMMU_S_CMDQ_BASE_HI

Figure 5-101. SMMU_S_CMDQ_BASE_HI Register

31	30	29	28	27	26	25	24
RESERVED	RA	RESERVED					
R-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-203. SMMU_S_CMDQ_BASE_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	RA	R/W	0h	RA
29-16	RESERVED	R	0h	Reserved_29_16
15-0	ADDR	R/W	0h	ADDR

Table 5-204. Register Call Summary for SMMU_S_CMDQ_BASE_HI

TCU_CFG Registers

- [SMMU_S_CMDQ_BASE_HI Register \(Offset = 08094h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.102 SMMU_S_CMDQ_PROD Register (Offset = 08098h) [reset = 0h]

SMMU_S_CMDQ_PROD is shown in [Figure 5-102](#) and described in [Table 5-205](#).

Return to [Summary Table](#).

SMMU_S_CMDQ_PROD

Figure 5-102. SMMU_S_CMDQ_PROD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												WR																			
R-0h												R/W-0h																			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-205. SMMU_S_CMDQ_PROD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved_31_20
19-0	WR	R/W	0h	WR

Table 5-206. Register Call Summary for SMMU_S_CMDQ_PROD

TCU_CFG Registers
<ul style="list-style-type: none"> TCU_CFG Registers: [0] SMMU_S_CMDQ_PROD Register (Offset = 08098h) [reset = 0h]: [0] [1]

5.1.103 SMMU_S_CMDQ_CONS Register (Offset = 0809Ch) [reset = 0h]

SMMU_S_CMDQ_CONS is shown in Figure 5-103 and described in Table 5-207.

Return to [Summary Table](#).

SMMU_S_CMDQ_CONS

Figure 5-103. SMMU_S_CMDQ_CONS Register

31	30	29	28	27	26	25	24
RESERVED				ERR			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED				RD			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RD							
R/W-0h							
7	6	5	4	3	2	1	0
RD							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-207. SMMU_S_CMDQ_CONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30-24	ERR	R/W	0h	ERR
23-20	RESERVED	R	0h	Reserved_23_20
19-0	RD	R/W	0h	RD

Table 5-208. Register Call Summary for SMMU_S_CMDQ_CONS

TCU_CFG Registers

- [SMMU_S_CMDQ_CONS Register \(Offset = 0809Ch\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.104 SMMU_S_EVENTQ_BASE_LO Register (Offset = 080A0h) [reset = 0h]

SMMU_S_EVENTQ_BASE_LO is shown in [Figure 5-104](#) and described in [Table 5-209](#).

Return to [Summary Table](#).

SMMU_S_EVENTQ_BASE_LO

Figure 5-104. SMMU_S_EVENTQ_BASE_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADDR															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR											LOG2SIZE				
R/W-0h											R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-209. SMMU_S_EVENTQ_BASE_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	ADDR	R/W	0h	ADDR
4-0	LOG2SIZE	R/W	0h	LOG2SIZE

Table 5-210. Register Call Summary for SMMU_S_EVENTQ_BASE_LO

TCU_CFG Registers

- [SMMU_S_EVENTQ_BASE_LO Register \(Offset = 080A0h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.105 SMMU_S_EVENTQ_BASE_HI Register (Offset = 080A4h) [reset = 0h]

SMMU_S_EVENTQ_BASE_HI is shown in [Figure 5-105](#) and described in [Table 5-211](#).

Return to [Summary Table](#).

SMMU_S_EVENTQ_BASE_HI

Figure 5-105. SMMU_S_EVENTQ_BASE_HI Register

31	30	29	28	27	26	25	24
RESERVED	WA	RESERVED					
R-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-211. SMMU_S_EVENTQ_BASE_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	WA	R/W	0h	WA
29-16	RESERVED	R	0h	Reserved_29_16
15-0	ADDR	R/W	0h	ADDR

Table 5-212. Register Call Summary for SMMU_S_EVENTQ_BASE_HI

TCU_CFG Registers

- [SMMU_S_EVENTQ_BASE_HI Register \(Offset = 080A4h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.106 SMMU_S_EVENTQ_PROD Register (Offset = 080A8h) [reset = 0h]

SMMU_S_EVENTQ_PROD is shown in Figure 5-106 and described in Table 5-213.

Return to [Summary Table](#).

SMMU_S_EVENTQ_PROD

Figure 5-106. SMMU_S_EVENTQ_PROD Register

31	30	29	28	27	26	25	24
OVFLG	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED				WR			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
WR							
R/W-0h							
7	6	5	4	3	2	1	0
WR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-213. SMMU_S_EVENTQ_PROD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVFLG	R/W	0h	OVFLG
30-20	RESERVED	R	0h	Reserved_30_20
19-0	WR	R/W	0h	WR

Table 5-214. Register Call Summary for SMMU_S_EVENTQ_PROD

TCU_CFG Registers

- [SMMU_S_EVENTQ_PROD Register \(Offset = 080A8h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.107 SMMU_S_EVENTQ_CONS Register (Offset = 080ACh) [reset = 0h]

SMMU_S_EVENTQ_CONS is shown in [Figure 5-107](#) and described in [Table 5-215](#).

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SMMU_S_EVENTQ_CONS

Figure 5-107. SMMU_S_EVENTQ_CONS Register

31	30	29	28	27	26	25	24
OVACKFLG	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED				RD			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RD							
R/W-0h							
7	6	5	4	3	2	1	0
RD							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-215. SMMU_S_EVENTQ_CONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVACKFLG	R/W	0h	OVACKFLG
30-20	RESERVED	R	0h	Reserved_30_20
19-0	RD	R/W	0h	RD

Table 5-216. Register Call Summary for SMMU_S_EVENTQ_CONS

TCU_CFG Registers

- [SMMU_S_EVENTQ_CONS Register \(Offset = 080ACh\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.108 SMMU_S_EVENTQ_IRQ_CFG0_LO Register (Offset = 080B0h) [reset = 0h]

SMMU_S_EVENTQ_IRQ_CFG0_LO is shown in [Figure 5-108](#) and described in [Table 5-217](#).

Return to [Summary Table](#).

SMMU_S_EVENTQ_IRQ_CFG0_LO

Figure 5-108. SMMU_S_EVENTQ_IRQ_CFG0_LO Register

31	30	29	28	27	26	25	24
ADDR							
R/W-0h							
23	22	21	20	19	18	17	16
ADDR							
R/W-0h							
15	14	13	12	11	10	9	8
ADDR							
R/W-0h							
7	6	5	4	3	2	1	0
ADDR						RESERVED	
R/W-0h						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-217. SMMU_S_EVENTQ_IRQ_CFG0_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	ADDR	R/W	0h	ADDR
1-0	RESERVED	R	0h	Reserved_1_0

Table 5-218. Register Call Summary for SMMU_S_EVENTQ_IRQ_CFG0_LO

TCU_CFG Registers

- [SMMU_S_EVENTQ_IRQ_CFG0_LO Register \(Offset = 080B0h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.109 SMMU_S_EVENTQ_IRQ_CFG0_HI Register (Offset = 080B4h) [reset = 0h]

SMMU_S_EVENTQ_IRQ_CFG0_HI is shown in Figure 5-109 and described in Table 5-219.

Return to [Summary Table](#).

SMMU_S_EVENTQ_IRQ_CFG0_HI

Figure 5-109. SMMU_S_EVENTQ_IRQ_CFG0_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-219. SMMU_S_EVENTQ_IRQ_CFG0_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved_31_16
15-0	ADDR	R/W	0h	ADDR

Table 5-220. Register Call Summary for SMMU_S_EVENTQ_IRQ_CFG0_HI

TCU_CFG Registers

- [SMMU_S_EVENTQ_IRQ_CFG0_HI Register \(Offset = 080B4h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.110 SMMU_S_EVENTQ_IRQ_CFG1 Register (Offset = 080B8h) [reset = 0h]

SMMU_S_EVENTQ_IRQ_CFG1 is shown in [Figure 5-110](#) and described in [Table 5-221](#).

Return to [Summary Table](#).

SMMU_S_EVENTQ_IRQ_CFG1

Figure 5-110. SMMU_S_EVENTQ_IRQ_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-221. SMMU_S_EVENTQ_IRQ_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	DATA

Table 5-222. Register Call Summary for SMMU_S_EVENTQ_IRQ_CFG1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_S_EVENTQ_IRQ_CFG1 Register \(Offset = 080B8h\) \[reset = 0h\]](#): [0] [1]

5.1.111 SMMU_S_EVENTQ_IRQ_CFG2 Register (Offset = 080BCh) [reset = 0h]

SMMU_S_EVENTQ_IRQ_CFG2 is shown in [Figure 5-111](#) and described in [Table 5-223](#).

Return to [Summary Table](#).

SMMU_S_EVENTQ_IRQ_CFG2

Figure 5-111. SMMU_S_EVENTQ_IRQ_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SH		MEMATTR			
R-0h										R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-223. SMMU_S_EVENTQ_IRQ_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved_31_6
5-4	SH	R/W	0h	SH
3-0	MEMATTR	R/W	0h	MemAttr

Table 5-224. Register Call Summary for SMMU_S_EVENTQ_IRQ_CFG2

TCU_CFG Registers
<ul style="list-style-type: none"> TCU_CFG Registers: [0] SMMU_S_EVENTQ_IRQ_CFG2 Register (Offset = 080BCh) [reset = 0h]: [0] [1]

5.1.112 TCU_CTRL Register (Offset = 08E00h) [reset = 0h]

TCU_CTRL is shown in Figure 5-112 and described in Table 5-225.

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The TCU Control register disables TCU features. You can disable individual walk caches, which can improve performance in some systems if the hit rate of the individual walk cache is very low. Do not modify the other bits unless directed to by ARM.

Figure 5-112. TCU_CTRL Register

31	30	29	28	27	26	25	24
AUX31	AUX30	AUX29	AUX28	AUX27	AUX26	AUX25	AUX24
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
AUX23	AUX22	AUX21	AUX20	AUX19	AUX18	AUX17	AUX16
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
WCS2L3_DIS	WCS2L2_DIS	WCS2L1_DIS	WCS2L0_DIS	WCS1L3_DIS	WCS1L2_DIS	WCS1L1_DIS	WCS1L0_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
AUX7	AUX6	AUX5	AUX4	AUX3	AUX2	AUX1	AUX0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-225. TCU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	AUX31	R/W	0h	Leave this bit as zero.
30	AUX30	R/W	0h	Leave this bit as zero.
29	AUX29	R/W	0h	Leave this bit as zero.
28	AUX28	R/W	0h	Leave this bit as zero.
27	AUX27	R/W	0h	Leave this bit as zero.
26	AUX26	R/W	0h	Leave this bit as zero.
25	AUX25	R/W	0h	Leave this bit as zero.
24	AUX24	R/W	0h	Leave this bit as zero.
23	AUX23	R/W	0h	Leave this bit as zero.
22	AUX22	R/W	0h	Leave this bit as zero.
21	AUX21	R/W	0h	Leave this bit as zero.
20	AUX20	R/W	0h	Leave this bit as zero.
19	AUX19	R/W	0h	Leave this bit as zero.
18	AUX18	R/W	0h	Leave this bit as zero.
17	AUX17	R/W	0h	Leave this bit as zero.
16	AUX16	R/W	0h	Leave this bit as zero.
15	WCS2L3_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 2 level 3 walk cache is disabled.
14	WCS2L2_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 2 level 2 walk cache is disabled.

Table 5-225. TCU_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	WCS2L1_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 2 level 1 walk cache is disabled.
12	WCS2L0_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 2 level 0 walk cache is disabled.
11	WCS1L3_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 1 level 3 walk cache is disabled.
10	WCS1L2_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 1 level 2 walk cache is disabled.
9	WCS1L1_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 1 level 1 walk cache is disabled.
8	WCS1L0_DIS	R/W	0h	Walk cache disable. When this bit is set to 1, the stage 2 level 0 walk cache is disabled.
7	AUX7	R/W	0h	Leave this bit as zero.
6	AUX6	R/W	0h	Leave this bit as zero.
5	AUX5	R/W	0h	Leave this bit as zero.
4	AUX4	R/W	0h	Leave this bit as zero.
3	AUX3	R/W	0h	Leave this bit as zero.
2	AUX2	R/W	0h	Leave this bit as zero.
1	AUX1	R/W	0h	Leave this bit as zero.
0	AUX0	R/W	0h	Leave this bit as zero.

Table 5-226. Register Call Summary for TCU_CTRL

TCU_CFG Registers

- [TCU_CTRL Register \(Offset = 08E00h\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.113 TCU_QOS Register (Offset = 08E04h) [reset = 0h]

TCU_QOS is shown in [Figure 5-113](#) and described in [Table 5-227](#).

Return to [Summary Table](#).

This is the TCU Quality of Service register. Use this register to specify QoS values for each transaction type. The MMU-600 uses the QoS value as a priority indicator for arbitration of requests.

Figure 5-113. TCU_QOS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				QOS_DVMSYNC				QOS_MSI				QOS_QUEUE			
R-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QOS_PTW3				QOS_PTW2				QOS_PTW1				QOS_PTW0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-227. TCU_QOS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved_31_28
27-24	QOS_DVMSYNC	R/W	0h	The QoS priority level that is used for DVM Sync Completion messages.
23-20	QOS_MSI	R/W	0h	The QoS priority level that is used for MSIs.
19-16	QOS_QUEUE	R/W	0h	The QoS priority level that is used for queue accesses.
15-12	QOS_PTW3	R/W	0h	The QoS priority level that is used for translation table walks. This level is used for translations where TCU_NODE_CTRLn.PRIORITY=3 for the requesting node.
11-8	QOS_PTW2	R/W	0h	The QoS priority level that is used for translation table walks for translations where TCU_NODE_CTRLn.PRIORITY=2 for the requesting node.
7-4	QOS_PTW1	R/W	0h	The QoS priority level that is used for translation table walks for translations where TCU_NODE_CTRLn.PRIORITY=1 for the requesting node.
3-0	QOS_PTW0	R/W	0h	The QoS priority level that is used for translation table walks for ATOS translations and for translations where TCU_NODE_CTRLn.PRIORITY=0 for the requesting node.

Table 5-228. Register Call Summary for TCU_QOS

TCU_CFG Registers

- [TCU_QOS Register \(Offset = 08E04h\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.114 TCU_CFG Register (Offset = 08E08h) [reset = 40h]

TCU_CFG is shown in [Figure 5-114](#) and described in [Table 5-229](#).

Return to [Summary Table](#).

This is the TCU Configuration Information register.

Figure 5-114. TCU_CFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XLATE_SLOTS												RESERVED			
R-4h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 5-229. TCU_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved_31_16
15-4	XLATE_SLOTS	R	4h	This is the number of translation slots that are available for sharing between all nodes.
3-0	RESERVED	R	0h	Reserved_3_0

Table 5-230. Register Call Summary for TCU_CFG

TCU_CFG Registers

- [TCU_CFG Register \(Offset = 08E08h\) \[reset = 40h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.115 TCU_STATUS Register (Offset = 08E10h) [reset = 0h]

TCU_STATUS is shown in [Figure 5-115](#) and described in [Table 5-231](#).

Return to [Summary Table](#).

This is the TCU Status Information register.

Figure 5-115. TCU_STATUS Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GNT_XLATE_SLOTS												RESERVED			
R-0h												R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 5-231. TCU_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved_31_16
15-4	GNT_XLATE_SLOTS	R	0h	This is the number of translation slots that are currently allocated to connected nodes. You can use this value for debugging purposes.
3-0	RESERVED	R	0h	Reserved_3_0

Table 5-232. Register Call Summary for TCU_STATUS

TCU_CFG Registers

- [TCU_STATUS Register \(Offset = 08E10h\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.116 TCU_SCR Register (Offset = 08E18h) [reset = 0h]

TCU_SCR is shown in Figure 5-116 and described in Table 5-233.

Return to [Summary Table](#).

This is the TCU Secure Control register.

Figure 5-116. TCU_SCR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				NS_INIT	RESERVED	NS_RAS	NS_UARCH
R-0h				R/W-0h	R-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-233. TCU_SCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3	NS_INIT	R/W	0h	Non-secure register access to SMMU_S_INIT . When this bit is set to 0, Non-secure accesses to the SMMU_S_INIT register are RAZ/WI.
2	RESERVED	R	0h	Reserved_2_2
1	NS_RAS	R/W	0h	Non-secure register access permitted for RAS registers. When this bit is set to 0, Non-secure accesses to register addresses 0x08E80-0x08EBC are RAZ/WI. The sec_override input signal defines the reset value of this bit.
0	NS_UARCH	R/W	0h	Non-secure register access permitted for MMU-600 registers. When this bit is set to 0, Non-secure accesses to register addresses 0x08E00-0x08E7C and 0x09000-0x093FC are RAZ/WI. The sec_override input signal defines the reset value of this bit. ARM recommends setting this bit to 0 if your implementation might use Secure translation.

Table 5-234. Register Call Summary for TCU_SCR

TCU_CFG Registers

- [TCU_SCR Register \(Offset = 08E18h\) \[reset = 0h\]: \[0\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.117 TCU_ERRFR_LO Register (Offset = 08E80h) [reset = 81h]

TCU_ERRFR_LO is shown in [Figure 5-117](#) and described in [Table 5-235](#).

Return to [Summary Table](#).

TCU_ERRFR_LO

Figure 5-117. TCU_ERRFR_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FI		RESERVED				ED	
R-0h								R-2h		R-0h				R-1h	

LEGEND: R = Read Only; -n = value after reset

Table 5-235. TCU_ERRFR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved_31_8
7-6	FI	R	2h	The value 0x2 indicates that the fault handling interrupt is controllable.
5-2	RESERVED	R	0h	Reserved_5_2
1-0	ED	R	1h	The value 0x1 indicates that TCU error detection is always enabled.

Table 5-236. Register Call Summary for TCU_ERRFR_LO

TCU_CFG Registers

- [TCU_ERRFR_LO Register \(Offset = 08E80h\) \[reset = 81h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.118 TCU_ERRFR_HI Register (Offset = 08E84h) [reset = 0h]

TCU_ERRFR_HI is shown in [Figure 5-118](#) and described in [Table 5-237](#).

Return to [Summary Table](#).

TCU_ERRFR_HI

Figure 5-118. TCU_ERRFR_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-237. TCU_ERRFR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved_31_0

Table 5-238. Register Call Summary for TCU_ERRFR_HI

TCU_CFG Registers
<ul style="list-style-type: none"> TCU_ERRFR_HI Register (Offset = 08E84h) [reset = 0h]: [0] [1] TCU_CFG Registers: [0]

5.1.119 TCU_ERRCTLR_LO Register (Offset = 08E88h) [reset = 8h]

TCU_ERRCTLR_LO is shown in [Figure 5-119](#) and described in [Table 5-239](#).

Return to [Summary Table](#).

TCU_ERRCTLR_LO

Figure 5-119. TCU_ERRCTLR_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												FI	RESERVED		
R-0h												R/W-1h		R-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-239. TCU_ERRCTLR_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3	FI	R/W	1h	Set this bit to 1 to enable fault handling interrupts for the TCU.
2-0	RESERVED	R	0h	Reserved_2_0

Table 5-240. Register Call Summary for TCU_ERRCTLR_LO

TCU_CFG Registers

- [TCU_ERRCTLR_LO Register \(Offset = 08E88h\) \[reset = 8h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.120 TCU_ERRCTLR_HI Register (Offset = 08E8Ch) [reset = 0h]

TCU_ERRCTLR_HI is shown in [Figure 5-120](#) and described in [Table 5-241](#).

Return to [Summary Table](#).

TCU_ERRCTLR_HI

Figure 5-120. TCU_ERRCTLR_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-241. TCU_ERRCTLR_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved_31_0

Table 5-242. Register Call Summary for TCU_ERRCTLR_HI

TCU_CFG Registers

- [TCU_ERRCTLR_HI Register \(Offset = 08E8Ch\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.121 TCU_ERRSTATUS_LO Register (Offset = 08E90h) [reset = 0h]

TCU_ERRSTATUS_LO is shown in [Figure 5-121](#) and described in [Table 5-243](#).

Return to [Summary Table](#).

TCU_ERRSTATUS_LO

Figure 5-121. TCU_ERRSTATUS_LO Register

31	30	29	28	27	26	25	24
RESERVED	V	RESERVED	OF	RESERVED	CE		
R-0h	R/W-0h	R-0h	R/W-0h	R-0h	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
IERR							
R/W-0h							
7	6	5	4	3	2	1	0
SERR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-243. TCU_ERRSTATUS_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved_31_31
30	V	R/W	0h	Register valid. This bit is set to 1 to indicate that at least one RAS error was recorded. Clear this bit by writing a 1 to it. If CE is not 00 and is not being cleared, the write is ignored. A write of 0 is ignored.
29-28	RESERVED	R	0h	Reserved_29_28
27	OF	R/W	0h	Overflow. This bit is set to 1 to indicate that multiple errors were recorded. Clear this bit by writing a 1 to it. A write of 0 is ignored.
26	RESERVED	R	0h	Reserved_26_26
25-24	CE	R/W	0h	Correctable Error. This field is set to 1 to indicate that a corrected error occurred. Clear this bit by writing a 11 to it. If OF is set to 1 and is not being cleared, the write is ignored. A write of any value other than 11 is ignored.
23-16	RESERVED	R	0h	Reserved_23_16

Table 5-243. TCU_ERRSTATUS_LO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-8	IERR	R/W	0h	Implementation defined error code. When SERR is not set to 0, this field indicates the source of the error, as follows: 0x00 Stage 1, level 0 walk cache. 0x01 Stage 1, level 1 walk cache. 0x02 Stage 1, level 2 walk cache. 0x03 Stage 1, level 3 walk cache. 0x04 Stage 2, level 0 walk cache. 0x05 Stage 2, level 1 walk cache. 0x06 Stage 2, level 2 walk cache. 0x07 Stage 2, level 3 walk cache. Writes to this field are ignored.
7-0	SERR	R/W	0h	Error code. This read-only field provides information about the earliest unacknowledged correctable error, as follows: 0x00 No error. This occurs when CE = 00. 0x07 Tag corrupted. This can occur when CE != 00. 0x08 Data corrupted. This can occur when CE != 00.

Table 5-244. Register Call Summary for TCU_ERRSTATUS_LO

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [TCU_ERRSTATUS_LO Register \(Offset = 08E90h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.1.122 TCU_ERRSTATUS_HI Register (Offset = 08E94h) [reset = 0h]

TCU_ERRSTATUS_HI is shown in [Figure 5-122](#) and described in [Table 5-245](#).

Return to [Summary Table](#).

TCU_ERRSTATUS_HI

Figure 5-122. TCU_ERRSTATUS_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-245. TCU_ERRSTATUS_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved_31_0

Table 5-246. Register Call Summary for TCU_ERRSTATUS_HI

TCU_CFG Registers

- [TCU_ERRSTATUS_HI Register \(Offset = 08E94h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.123 TCU_ERRGEN_LO Register (Offset = 08EC0h) [reset = 0h]

TCU_ERRGEN_LO is shown in Figure 5-123 and described in Table 5-247.

Return to [Summary Table](#).

TCU_ERRGEN_LO

Figure 5-123. TCU_ERRGEN_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												TCC	DCC	TWC	DWC
R-0h												R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-247. TCU_ERRGEN_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3	TCC	R/W	0h	When 1, entries allocated into the configuration cache are written with a tag parity error.
2	DCC	R/W	0h	When 1, entries allocated into the configuration cache are written with a data parity error.
1	TWC	R/W	0h	When 1, entries allocated into any walk cache are written with a tag parity error.
0	DWC	R/W	0h	When 1, entries allocated into any walk cache are written with a data parity error.

Table 5-248. Register Call Summary for TCU_ERRGEN_LO

TCU_CFG Registers

- [TCU_ERRGEN_LO Register \(Offset = 08EC0h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.124 TCU_ERRGEN_HI Register (Offset = 08EC4h) [reset = 0h]

TCU_ERRGEN_HI is shown in [Figure 5-124](#) and described in [Table 5-249](#).

Return to [Summary Table](#).

TCU_ERRGEN_HI

Figure 5-124. TCU_ERRGEN_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-249. TCU_ERRGEN_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved_31_0

Table 5-250. Register Call Summary for TCU_ERRGEN_HI

TCU_CFG Registers

- [TCU_ERRGEN_HI Register \(Offset = 08EC4h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.125 TCU_NODE_CTRLn Register (Offset = 09000h + formula) [reset = 0h]

TCU_NODE_CTRLn is shown in [Figure 5-125](#) and described in [Table 5-251](#).

Return to [Summary Table](#).

TCU_NODE_CTRLn

Offset = 09000h + (n * 4h); where n = 0h to 3Dh

Figure 5-125. TCU_NODE_CTRLn Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			DIS_DVM	RESERVED		PRI_LEVEL	
R-0h			R/W-0h	R-0h		R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-251. TCU_NODE_CTRLn Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved_31_5
4	DIS_DVM	R/W	0h	Disable DVM. When this bit is set to 1, the corresponding node does not participate in DVM invalidation. Set this bit to 1 to improve performance if the node is slow to respond to invalidations issued over DTI.
3-2	RESERVED	R	0h	Reserved_3_2
1-0	PRI_LEVEL	R/W	0h	Priority level. This field indicates the priority level of the corresponding node. Translation requests from a node with a higher priority level are normally progressed before those from a node with a lower priority level.

Table 5-252. Register Call Summary for TCU_NODE_CTRLn

TCU_CFG Registers

- [TCU_QOS Register](#) (Offset = 08E04h) [reset = 0h]: [0] [1] [2] [3]
- [TCU_NODE_CTRLn Register](#) (Offset = 09000h + formula) [reset = 0h]: [0] [1]
- [TCU_CFG Registers](#): [0]

5.1.126 TCU_NODE_STATUSn Register (Offset = 09400h + formula) [reset = 0h]

TCU_NODE_STATUSn is shown in [Figure 5-126](#) and described in [Table 5-253](#).

Return to [Summary Table](#).

TCU_NODE_STATUSn

Offset = 09000h + (n * 4h); where n = 0h to 3Dh

Figure 5-126. TCU_NODE_STATUSn Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ATS	CONNECTED
R-0h						R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 5-253. TCU_NODE_STATUSn Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved_31_2
1	ATS	R	0h	ATS implemented. When this bit is set to 0, the corresponding node is a TBU that is connected to the TCU using the DTI-TBU protocol. When this bit is set to 1, the corresponding node is a PCIe Root Complex that supports ATS, and is connected to the TCU using the DTI-ATS protocol.
0	CONNECTED	R	0h	DTI link connected. When this bit is set to 0, the DTI link for the corresponding node is not connected. When this bit is set to 1, the DTI link for the corresponding node is connected. If a DTI link is not connected, accesses to TBU registers are RAZ/WI. However, the state might change between reading this register and attempting to access the TBU.

Table 5-254. Register Call Summary for TCU_NODE_STATUSn

TCU_CFG Registers

- TCU_NODE_STATUSn Register (Offset = 09400h + formula) [reset = 0h]: [0] [1]
- TCU_CFG Registers: [0]

5.1.127 SMMU_EVENTQ_PROD Register (Offset = 100A8h) [reset = 0h]

SMMU_EVENTQ_PROD is shown in [Figure 5-127](#) and described in [Table 5-255](#).

[Return to Summary Table.](#)

SMMU_EVENTQ_PROD

Figure 5-127. SMMU_EVENTQ_PROD Register

31	30	29	28	27	26	25	24
OVFLG	RESERVED						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED				WR			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
WR							
R/W-0h							
7	6	5	4	3	2	1	0
WR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-255. SMMU_EVENTQ_PROD Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVFLG	R/W	0h	OVFLG
30-20	RESERVED	R	0h	Reserved_30_20
19-0	WR	R/W	0h	WR

Table 5-256. Register Call Summary for SMMU_EVENTQ_PROD

TCU_CFG Registers

- [SMMU_EVENTQ_PROD Register \(Offset = 100A8h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.128 SMMU_EVENTQ_CONS Register (Offset = 100ACh) [reset = 0h]

SMMU_EVENTQ_CONS is shown in Figure 5-128 and described in Table 5-257.

Return to [Summary Table](#).

SMMU_EVENTQ_CONS

Figure 5-128. SMMU_EVENTQ_CONS Register

31	30	29	28	27	26	25	24
OVACKFLG	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED				RD			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
RD							
R/W-0h							
7	6	5	4	3	2	1	0
RD							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-257. SMMU_EVENTQ_CONS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	OVACKFLG	R/W	0h	OVACKFLG
30-20	RESERVED	R	0h	Reserved_30_20
19-0	RD	R/W	0h	RD

Table 5-258. Register Call Summary for SMMU_EVENTQ_CONS

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_EVENTQ_CONS Register (Offset = 100ACh) [reset = 0h]: [0] [1] TCU_CFG Registers: [0]

5.1.129 SMMU_PMCG_EVCNTR0 Register (Offset = 22000h) [reset = 0h]

SMMU_PMCG_EVCNTR0 is shown in [Figure 5-129](#) and described in [Table 5-259](#).

Return to [Summary Table](#).

SMMU_PMCG_EVCNTR0

Figure 5-129. SMMU_PMCG_EVCNTR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-259. SMMU_PMCG_EVCNTR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNTER_VALUE	R/W	0h	COUNTER_VALUE

Table 5-260. Register Call Summary for SMMU_PMCG_EVCNTR0

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_EVCNTR0 Register \(Offset = 22000h\) \[reset = 0h\]](#): [0] [1]

5.1.130 SMMU_PMCG_EVCNTR1 Register (Offset = 22004h) [reset = 0h]

SMMU_PMCG_EVCNTR1 is shown in [Figure 5-130](#) and described in [Table 5-261](#).

Return to [Summary Table](#).

SMMU_PMCG_EVCNTR1

Figure 5-130. SMMU_PMCG_EVCNTR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-261. SMMU_PMCG_EVCNTR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNTER_VALUE	R/W	0h	COUNTER_VALUE

Table 5-262. Register Call Summary for SMMU_PMCG_EVCNTR1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_EVCNTR1 Register \(Offset = 22004h\) \[reset = 0h\]](#): [0] [1]

5.1.131 SMMU_PMCG_EVCNTR2 Register (Offset = 22008h) [reset = 0h]

SMMU_PMCG_EVCNTR2 is shown in [Figure 5-131](#) and described in [Table 5-263](#).

Return to [Summary Table](#).

SMMU_PMCG_EVCNTR2

Figure 5-131. SMMU_PMCG_EVCNTR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-263. SMMU_PMCG_EVCNTR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNTER_VALUE	R/W	0h	COUNTER_VALUE

Table 5-264. Register Call Summary for SMMU_PMCG_EVCNTR2

TCU_CFG Registers

- [SMMU_PMCG_EVCNTR2 Register \(Offset = 22008h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.132 SMMU_PMCg_EVCNTR3 Register (Offset = 2200Ch) [reset = 0h]

SMMU_PMCg_EVCNTR3 is shown in [Figure 5-132](#) and described in [Table 5-265](#).

Return to [Summary Table](#).

[SMMU_PMCg_EVCNTR3](#)

Figure 5-132. SMMU_PMCg_EVCNTR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNTER_VALUE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-265. SMMU_PMCg_EVCNTR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNTER_VALUE	R/W	0h	COUNTER_VALUE

Table 5-266. Register Call Summary for SMMU_PMCg_EVCNTR3

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCg_EVCNTR3 Register \(Offset = 2200Ch\) \[reset = 0h\]](#): [0] [1]

5.1.133 SMMU_PMCG_SVR0 Register (Offset = 22600h) [reset = 0h]

SMMU_PMCG_SVR0 is shown in [Figure 5-133](#) and described in [Table 5-267](#).

Return to [Summary Table](#).

SMMU_PMCG_SVR0

Figure 5-133. SMMU_PMCG_SVR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOW_COUNTER_VALUE																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-267. SMMU_PMCG_SVR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHADOW_COUNTER_VALUE	R	0h	SHADOW_COUNTER_VALUE

Table 5-268. Register Call Summary for SMMU_PMCG_SVR0

TCU_CFG Registers
<ul style="list-style-type: none"> TCU_CFG Registers: [0] SMMU_PMCG_SVR0 Register (Offset = 22600h) [reset = 0h]: [0] [1]

5.1.134 SMMU_PMCG_SVR1 Register (Offset = 22604h) [reset = 0h]

SMMU_PMCG_SVR1 is shown in [Figure 5-134](#) and described in [Table 5-269](#).

Return to [Summary Table](#).

SMMU_PMCG_SVR1

Figure 5-134. SMMU_PMCG_SVR1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOW_COUNTER_VALUE																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-269. SMMU_PMCG_SVR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHADOW_COUNTER_VALUE	R	0h	SHADOW_COUNTER_VALUE

Table 5-270. Register Call Summary for SMMU_PMCG_SVR1

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_SVR1 Register \(Offset = 22604h\) \[reset = 0h\]](#): [0] [1]

5.1.135 SMMU_PMCG_SVR2 Register (Offset = 22608h) [reset = 0h]

SMMU_PMCG_SVR2 is shown in [Figure 5-135](#) and described in [Table 5-271](#).

Return to [Summary Table](#).

SMMU_PMCG_SVR2

Figure 5-135. SMMU_PMCG_SVR2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOW_COUNTER_VALUE																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-271. SMMU_PMCG_SVR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHADOW_COUNTER_VALUE	R	0h	SHADOW_COUNTER_VALUE

Table 5-272. Register Call Summary for SMMU_PMCG_SVR2

TCU_CFG Registers
<ul style="list-style-type: none"> SMMU_PMCG_SVR2 Register (Offset = 22608h) [reset = 0h]: [0] [1] TCU_CFG Registers: [0]

5.1.136 SMMU_PMCG_SVR3 Register (Offset = 2260Ch) [reset = 0h]

SMMU_PMCG_SVR3 is shown in [Figure 5-136](#) and described in [Table 5-273](#).

Return to [Summary Table](#).

SMMU_PMCG_SVR3

Figure 5-136. SMMU_PMCG_SVR3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHADOW_COUNTER_VALUE																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 5-273. SMMU_PMCG_SVR3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SHADOW_COUNTER_VALUE	R	0h	SHADOW_COUNTER_VALUE

Table 5-274. Register Call Summary for SMMU_PMCG_SVR3

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_SVR3 Register \(Offset = 2260Ch\) \[reset = 0h\]](#): [0] [1]

5.1.137 SMMU_PMCG_OVSCLR0 Register (Offset = 22C80h) [reset = 0h]

SMMU_PMCG_OVSCLR0 is shown in [Figure 5-137](#) and described in [Table 5-275](#).

Return to [Summary Table](#).

SMMU_PMCG_OVSCLR0

Figure 5-137. SMMU_PMCG_OVSCLR0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OVS			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-275. SMMU_PMCG_OVSCLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3-0	OVS	R/W	0h	OVS

Table 5-276. Register Call Summary for SMMU_PMCG_OVSCLR0

TCU_CFG Registers

- [TCU_CFG Registers](#): [0]
- [SMMU_PMCG_OVSCLR0 Register \(Offset = 22C80h\) \[reset = 0h\]](#): [0] [1]

5.1.138 SMMU_PMCG_OVSSET0 Register (Offset = 22CC0h) [reset = 0h]

SMMU_PMCG_OVSSET0 is shown in [Figure 5-138](#) and described in [Table 5-277](#).

Return to [Summary Table](#).

[SMMU_PMCG_OVSSET0](#)

Figure 5-138. SMMU_PMCG_OVSSET0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OVS			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 5-277. SMMU_PMCG_OVSSET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved_31_4
3-0	OVS	R/W	0h	OVS

Table 5-278. Register Call Summary for SMMU_PMCG_OVSSET0

TCU_CFG Registers

- [SMMU_PMCG_OVSSET0 Register \(Offset = 22CC0h\) \[reset = 0h\]: \[0\] \[1\]](#)
- [TCU_CFG Registers: \[0\]](#)

5.1.139 SMMU_PMCG_CAPR Register (Offset = 22D88h) [reset = 0h]

SMMU_PMCG_CAPR is shown in [Figure 5-139](#) and described in [Table 5-279](#).

Return to [Summary Table](#).

SMMU_PMCG_CAPR

Figure 5-139. SMMU_PMCG_CAPR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CAPTURE
R-0h							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 5-279. SMMU_PMCG_CAPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved_31_1
0	CAPTURE	W	0h	CAPTURE

Table 5-280. Register Call Summary for SMMU_PMCG_CAPR

TCU_CFG Registers

- [TCU_CFG Registers: \[0\]](#)
- [SMMU_PMCG_CAPR Register \(Offset = 22D88h\) \[reset = 0h\]: \[0\] \[1\]](#)

5.2 VIRTSS_ECCAGGR_CFG Registers

Table 5-282 lists the memory-mapped registers for the VIRTSS_ECCAGGR_CFG registers. All register offset addresses not listed in Table 5-282 should be considered as reserved locations and the register contents should not be modified.

Table 5-281. VIRTSS_ECCAGGR_CFG Instances

Instance	Base Address
VIRTSS_ECCAGGR_CFG	3100 2000h

Table 5-282. VIRTSS_ECCAGGR_CFG Registers

Offset	Acronym	Register Name	VIRTSS_ECCAGGR_CFG Physical Address
000h	ECC_REV	Aggregator Revision Register	31002000h
008h	ECC_VECTOR	ECC Vector Register	31002008h
00Ch	ECC_STAT	Misc Status	3100200Ch
010h + formula	ECC_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	31002010h + formula
03Ch	ECC_SEC_EOI_REG	EOI Register	3100203Ch
040h	ECC_SEC_STATUS_REG0	Interrupt Status Register 0	31002040h
044h	ECC_SEC_STATUS_REG1	Interrupt Status Register 1	31002044h
048h	ECC_SEC_STATUS_REG2	Interrupt Status Register 2	31002048h
04Ch	ECC_SEC_STATUS_REG3	Interrupt Status Register 3	3100204Ch
080h	ECC_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	31002080h
084h	ECC_SEC_ENABLE_SET_REG1	Interrupt Enable Set Register 1	31002084h
088h	ECC_SEC_ENABLE_SET_REG2	Interrupt Enable Set Register 2	31002088h
08Ch	ECC_SEC_ENABLE_SET_REG3	Interrupt Enable Set Register 3	3100208Ch
0C0h	ECC_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	310020C0h
0C4h	ECC_SEC_ENABLE_CLR_REG1	Interrupt Enable Clear Register 1	310020C4h
0C8h	ECC_SEC_ENABLE_CLR_REG2	Interrupt Enable Clear Register 2	310020C8h
0CCh	ECC_SEC_ENABLE_CLR_REG3	Interrupt Enable Clear Register 3	310020CCh
13Ch	ECC_DED_EOI_REG	EOI Register	3100213Ch
140h	ECC_DED_STATUS_REG0	Interrupt Status Register 0	31002140h
144h	ECC_DED_STATUS_REG1	Interrupt Status Register 1	31002144h
148h	ECC_DED_STATUS_REG2	Interrupt Status Register 2	31002148h
14Ch	ECC_DED_STATUS_REG3	Interrupt Status Register 3	3100214Ch
180h	ECC_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	31002180h
184h	ECC_DED_ENABLE_SET_REG1	Interrupt Enable Set Register 1	31002184h
188h	ECC_DED_ENABLE_SET_REG2	Interrupt Enable Set Register 2	31002188h
18Ch	ECC_DED_ENABLE_SET_REG3	Interrupt Enable Set Register 3	3100218Ch
1C0h	ECC_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	310021C0h
1C4h	ECC_DED_ENABLE_CLR_REG1	Interrupt Enable Clear Register 1	310021C4h
1C8h	ECC_DED_ENABLE_CLR_REG2	Interrupt Enable Clear Register 2	310021C8h
1CCh	ECC_DED_ENABLE_CLR_REG3	Interrupt Enable Clear Register 3	310021CCh
200h	ECC_AGGR_ENABLE_SET	AGGR interrupt enable set Register	31002200h
204h	ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	31002204h
208h	ECC_AGGR_STATUS_SET	AGGR interrupt status set Register	31002208h
20Ch	ECC_AGGR_STATUS_CLR	AGGR interrupt status clear Register	3100220Ch

5.2.1 ECC_REV Register (Offset = 000h) [reset = 66A0EA00h]

ECC_REV is shown in Figure 5-140 and described in Table 5-283.

Return to [Summary Table](#).

Revision parameters

Figure 5-140. ECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 5-283. ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

Table 5-284. Register Call Summary for ECC_REV

VIRTSS_ECCAGGR_CFG Registers

- [ECC_REV Register \(Offset = 31002000h\) \[reset = 66A0EA00h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.2 ECC_VECTOR Register (Offset = 008h) [reset = X]

ECC_VECTOR is shown in [Figure 5-141](#) and described in [Table 5-285](#).

Return to [Summary Table](#).

ECC Vector Register

Figure 5-141. ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_D ONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-285. ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

Table 5-286. Register Call Summary for ECC_VECTOR

VIRTSS_ECCAGGR_CFG Registers	
•	ECC_VECTOR Register (Offset = 31002008h) [reset = X]: [0] [1] [2] [3]
•	virtss_eccaggr_cfg_regs Registers: [0]

5.2.3 ECC_STAT Register (Offset = 00Ch) [reset = X]

ECC_STAT is shown in [Figure 5-142](#) and described in [Table 5-287](#).

Return to [Summary Table](#).

Misc Status

Figure 5-142. ECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											NUM_RAMs																				
R-X											R-70h																				

LEGEND: R = Read Only; -n = value after reset

Table 5-287. ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	70h	Indicates the number of RAMs serviced by the ECC aggregator

Table 5-288. Register Call Summary for ECC_STAT

VIRTSS_ECCAGGR_CFG Registers

- [ECC_STAT Register \(Offset = 3100200Ch\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.4 ECC_RESERVED_SVBUS_y Register (Offset = 010h + formula) [reset = 0h]

ECC_RESERVED_SVBUS_y is shown in [Figure 5-143](#) and described in [Table 5-289](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 010h + (y * 4h); where y = 0h to 7h

Figure 5-143. ECC_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-289. ECC_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

Table 5-290. Register Call Summary for ECC_RESERVED_SVBUS_y

VIRTSS_ECCAGGR_CFG Registers

- [ECC_RESERVED_SVBUS_y Register \(Offset = 31002010h + formula\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.5 ECC_SEC_EOI_REG Register (Offset = 03Ch) [reset = X]

ECC_SEC_EOI_REG is shown in [Figure 5-144](#) and described in [Table 5-291](#).

Return to [Summary Table](#).

EOI Register

Figure 5-144. ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-291. ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 5-292. Register Call Summary for ECC_SEC_EOI_REG

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_EOI_REG Register \(Offset = 3100203Ch\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.6 ECC_SEC_STATUS_REG0 Register (Offset = 040h) [reset = 0h]

ECC_SEC_STATUS_REG0 is shown in Figure 5-145 and described in Table 5-293.

Return to [Summary Table](#).

Interrupt Status Register 0

Figure 5-145. ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
TCU_DTIB_RA MECC_PEND	NAVSS512L_VI RTSS_IO_TBU 0_EDC_CTRL_ BUSECC_PEN D	NAVSS512L_VI RTSS_IO_TBU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_I O_TBU0_SRC_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_IO_TBU 0_AXI2M_W_B USECC_PEND	NAVSS512L_VI RTSS_IO_TBU 0_AXI2M_R_B USECC_PEND	NAVSS512L_VI RTSS_IO_TBU 0_M2AXI_BUS ECC_PEND	IO_TBU0_ENT B_TAG3_RAME CC_PEND	IO_TBU0_ENT B_TAG2_RAME CC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
IO_TBU0_ENT B_TAG1_RAME CC_PEND	IO_TBU0_ENT B_TAG0_RAME CC_PEND	IO_TBU0_MTL B_TAG3_RAME CC_PEND	IO_TBU0_MTL B_TAG2_RAME CC_PEND	IO_TBU0_MTL B_TAG1_RAME CC_PEND	IO_TBU0_MTL B_TAG0_RAME CC_PEND	IO_TBU0_WBB _RAMECC_PE ND	NAVSS512L_VI RTSS_DMA_P VU1_EDC_CTR L_BUSECC_PE ND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
DMA_PVU1_TL B_BANK_RAM CC_PEND	NAVSS512L_VI RTSS_IO_PVU 1_EDC_CTRL_ BUSECC_PEN D	IO_PVU1_TLB BANK_RAMCC _PEND	NAVSS512L_VI RTSS_IO_PVU 0_EDC_CTRL_ BUSECC_PEN D	IO_PVU0_TLB BANK_RAMCC _PEND	NAVSS512L_VI RTSS_PAT4_E DC_CTRL_BUS ECC_PEND	PAT4_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT3_E DC_CTRL_BUS ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
PAT3_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT2_E DC_CTRL_BUS ECC_PEND	PAT2_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT1_E DC_CTRL_BUS ECC_PEND	PAT1_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT0_E DC_CTRL_BUS ECC_PEND	PAT0_TABLE_ RAMECC_PEN D	ECCAGG_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-293. ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCU_DTIB_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_dtib_amecc_pending
30	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_src_m2m_bridge_navss512l_virtss_io_tbu0_src_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_axi2m_w_busecc_pending

Table 5-293. ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_axi2m_r_busecc_pend
26	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_m2axi_busecc_pend
25	IO_TBU0_ENTB_TAG3_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag3_amecc_pend
24	IO_TBU0_ENTB_TAG2_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag2_amecc_pend
23	IO_TBU0_ENTB_TAG1_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag1_amecc_pend
22	IO_TBU0_ENTB_TAG0_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag0_amecc_pend
21	IO_TBU0_MTLB_TAG3_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag3_amecc_pend
20	IO_TBU0_MTLB_TAG2_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag2_amecc_pend
19	IO_TBU0_MTLB_TAG1_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag1_amecc_pend
18	IO_TBU0_MTLB_TAG0_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag0_amecc_pend
17	IO_TBU0_WBB_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_wbb_amecc_pend
16	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_dma_pvu1_edc_ctrl_busecc_pend
15	DMA_PVU1_TLB_BANK_RAMCC_PEND	R/W1S	0h	Interrupt Pending Status for dma_pvu1_tlb_bank_ramcc_pend
14	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_pvu1_edc_ctrl_busecc_pend
13	IO_PVU1_TLB_BANK_RAMCC_PEND	R/W1S	0h	Interrupt Pending Status for io_pvu1_tlb_bank_ramcc_pend
12	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_pvu0_edc_ctrl_busecc_pend
11	IO_PVU0_TLB_BANK_RAMCC_PEND	R/W1S	0h	Interrupt Pending Status for io_pvu0_tlb_bank_ramcc_pend
10	NAVSS512L_VIRTSS_PA_T4_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat4_edc_ctrl_busecc_pend
9	PAT4_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat4_table_amecc_pend
8	NAVSS512L_VIRTSS_PA_T3_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat3_edc_ctrl_busecc_pend
7	PAT3_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat3_table_amecc_pend
6	NAVSS512L_VIRTSS_PA_T2_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat2_edc_ctrl_busecc_pend
5	PAT2_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat2_table_amecc_pend
4	NAVSS512L_VIRTSS_PA_T1_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat1_edc_ctrl_busecc_pend

Table 5-293. ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAT1_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat1_table_ramecc_pend
2	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat0_edc_ctrl_busecc_pend
1	PAT0_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat0_table_ramecc_pend
0	ECCAGG_PEND	R/W1S	0h	Interrupt Pending Status for eccagg_pend

Table 5-294. Register Call Summary for ECC_SEC_STATUS_REG0

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_STATUS_REG0 Register \(Offset = 31002040h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.7 ECC_SEC_STATUS_REG1 Register (Offset = 044h) [reset = 0h]

ECC_SEC_STATUS_REG1 is shown in Figure 5-146 and described in Table 5-295.

Return to [Summary Table](#).

Interrupt Status Register 1

Figure 5-146. ECC_SEC_STATUS_REG1 Register

31	30	29	28	27	26	25	24
NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VIRTSS_DATA_C BASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_PENDING	SMMU_BUFFER2_WFIFO_RA_MECC_PENDING	SMMU_BUFFER2_CFIFO_RA_MECC_PENDING	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_PENDING	SMMU_BUFFER1_WFIFO_RA_MECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
SMMU_BUFFER1_CFIFO_RA_MECC_PENDING	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_PENDING	SMMU_BUFFER0_WFIFO_RA_MECC_PENDING	SMMU_BUFFER0_CFIFO_RA_MECC_PENDING	TCU_AXI2M_WBUSECC_PENDING	TCU_AXI2M_RBUSECC_PENDING	TCU_WCB_TAG3_RAMECC_PENDING	TCU_WCB_TAG2_RAMECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
TCU_WCB_TAG1_RAMECC_PENDING	TCU_WCB_TAG0_RAMECC_PENDING	TCU_CCB_TAG3_RAMECC_PENDING	TCU_CCB_TAG2_RAMECC_PENDING	TCU_CCB_TAG1_RAMECC_PENDING	TCU_CCB_TAG0_RAMECC_PENDING	TCU_WCB_ENT_RAMECC_PENDING	TCU_CCB_ENT_RAMECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-295. ECC_SEC_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-295. ECC_SEC_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
27	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
26	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
25	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
24	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
23	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
22	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-295. ECC_SEC_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_smmu_buffer2_src_edc_ctrl_busecc_pend
19	SMMU_BUFFER2_WFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer2_wfifo_ramecc_pend
18	SMMU_BUFFER2_CFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer2_cfifo_ramecc_pend
17	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_smmu_buffer1_src_edc_ctrl_busecc_pend
16	SMMU_BUFFER1_WFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer1_wfifo_ramecc_pend
15	SMMU_BUFFER1_CFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer1_cfifo_ramecc_pend
14	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_smmu_buffer0_src_edc_ctrl_busecc_pend
13	SMMU_BUFFER0_WFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer0_wfifo_ramecc_pend
12	SMMU_BUFFER0_CFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer0_cfifo_ramecc_pend
11	TCU_AXI2M_W_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_axi2m_w_busecc_pend
10	TCU_AXI2M_R_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_axi2m_r_busecc_pend
9	TCU_WCB_TAG3_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag3_ramecc_pend
8	TCU_WCB_TAG2_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag2_ramecc_pend
7	TCU_WCB_TAG1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag1_ramecc_pend
6	TCU_WCB_TAG0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag0_ramecc_pend
5	TCU_CCB_TAG3_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag3_ramecc_pend
4	TCU_CCB_TAG2_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag2_ramecc_pend
3	TCU_CCB_TAG1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag1_ramecc_pend
2	TCU_CCB_TAG0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag0_ramecc_pend
1	TCU_WCB_ENT_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_ent_ramecc_pend
0	TCU_CCB_ENT_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_ent_ramecc_pend

Table 5-296. Register Call Summary for ECC_SEC_STATUS_REG1

VIRTSS_ECCAGGR_CFG Registers	
•	ECC_SEC_STATUS_REG1 Register (Offset = 31002044h) [reset = 0h]: [0]
•	virtss_eccaggr_cfg_regs Registers: [0]

5.2.8 ECC_SEC_STATUS_REG2 Register (Offset = 048h) [reset = 0h]

ECC_SEC_STATUS_REG2 is shown in Figure 5-147 and described in Table 5-297.

Return to [Summary Table](#).

Interrupt Status Register 2

Figure 5-147. ECC_SEC_STATUS_REG2 Register

31	30	29	28	27	26	25	24
NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_1_PEND	NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_0_PEND	NAVSS512L_VI RTSS_DATA_C BASS_ECCAG GR_CFG_P2P BRIDGE_ECCA GGR_CFG_BRI DGE_BUSECC _PEND	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_SRC_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 3_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV3_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 2_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV2_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 1_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV1_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_DMA_SL V0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_DM A_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_BU SECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_MOD_S LV0_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_M OD_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_B USECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_AC_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_AC_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_VIRTSS _CFG_P2P_BR IDGE_VIRTSS_ CFG_BRIDGE_ BUSECC_PEN D	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_DST_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_MS T0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_NB_ MST0_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_DMA_M ST3_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_D MA_MST3_M2 M_BRIDGE_SR C_EDC_CTRL_ BUSECC_PEN D

Figure 5-147. ECC_SEC_STATUS_REG2 Register (continued)

R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
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LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-297. ECC_SEC_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_1_pend
30	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_0_pend
29	NAVSS512L_VIRTSS_DATA_CBASS_ECCAGGR_CFG_P2P_BRIDGE_ECC AGGR_CFG_BRIDGE_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_eccaggr_cfg_p2p_bridge_eccaggr_cf g_bridge_busecc_pend
28	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_NAVSS 512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_SRC_EDC_CTR L_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_navss 512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_src_edc_ctr l_busecc_pend
27	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_NAVSS 512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_SRC_EDC_CTR L_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_navss 512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_src_edc_ctr l_busecc_pend
26	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_NAVSS 512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_SRC_EDC_CTR L_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_navss 512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_src_edc_ctr l_busecc_pend
25	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_NAVSS 512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTR L_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_navss51 2l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_src_edc_ctrl_bu secc_pend
24	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_NAVSS 512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTR L_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_navss512l _virtss_data_cbass_io_pvu1_src_m2m_bridge_src_edc_ctrl_busecc _pend

Table 5-297. ECC_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
22	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat4_src_m2m_bridge_navss512l_virtss_data_cbass_pat4_src_m2m_bridge_src_edc_ctrl_busecc_pend
21	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat3_src_m2m_bridge_navss512l_virtss_data_cbass_pat3_src_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat2_src_m2m_bridge_navss512l_virtss_data_cbass_pat2_src_m2m_bridge_src_edc_ctrl_busecc_pend
19	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat1_src_m2m_bridge_navss512l_virtss_data_cbass_pat1_src_m2m_bridge_src_edc_ctrl_busecc_pend
18	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat0_src_m2m_bridge_navss512l_virtss_data_cbass_pat0_src_m2m_bridge_src_edc_ctrl_busecc_pend
17	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_src_edc_ctrl_busecc_pend
16	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_src_edc_ctrl_busecc_pend
15	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-297. ECC_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
12	NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_VIRTSS_CFG_P2P_BRIDGE_VIRTSS_CFG_BRIDGE_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_virtss_cfg_p2p_bridge_virtss_cfg_bridge_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-297. ECC_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_src_edc_ctrl_busecc_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_src_edc_ctrl_busecc_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
2	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-298. Register Call Summary for ECC_SEC_STATUS_REG2

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_STATUS_REG2 Register \(Offset = 31002048h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.9 ECC_SEC_STATUS_REG3 Register (Offset = 04Ch) [reset = X]

ECC_SEC_STATUS_REG3 is shown in Figure 5-148 and described in Table 5-299.

Return to [Summary Table](#).

Interrupt Status Register 3

Figure 5-148. ECC_SEC_STATUS_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUS ECC_1_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUS ECC_0_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DS_T_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SR_C_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CFG_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_EDC_CTRL_BUSECC_1_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_EDC_CTRL_BUSECC_0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_4_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_3_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_2_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-299. ECC_SEC_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_1_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_0_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cbass_int_dmesc_scr_navss512l_virtss_data_cbass_cbass_int_dmesc_scr_edc_ctrl_busecc_pend

Table 5-299. ECC_SEC_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DST_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_dst_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SRC_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_src_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cbass_default_mmrs_navss512l_virtss_data_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_1_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_1_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_0_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_0_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_9_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_8_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_7_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_6_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_5_pend

Table 5-299. ECC_SEC_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_4_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_4_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_3_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_3_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_2_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_2_pend

Table 5-300. Register Call Summary for ECC_SEC_STATUS_REG3

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_STATUS_REG3 Register \(Offset = 3100204Ch\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.10 ECC_SEC_ENABLE_SET_REG0 Register (Offset = 080h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG0 is shown in Figure 5-149 and described in Table 5-301.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Figure 5-149. ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
TCU_DTIB_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUS_ECC_ENABLE_SET	IO_TBU0_ENT_B_TAG3_RAMECC_ENABLE_SET	IO_TBU0_ENT_B_TAG2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
IO_TBU0_ENT_B_TAG1_RAMECC_ENABLE_SET	IO_TBU0_ENT_B_TAG0_RAMECC_ENABLE_SET	IO_TBU0_MTL_B_TAG3_RAMECC_ENABLE_SET	IO_TBU0_MTL_B_TAG2_RAMECC_ENABLE_SET	IO_TBU0_MTL_B_TAG1_RAMECC_ENABLE_SET	IO_TBU0_MTL_B_TAG0_RAMECC_ENABLE_SET	IO_TBU0_WBB_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
DMA_PVU1_TLB_BANK_RAMCC_ENABLE_SET	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_SET	IO_PVU1_TLB_BANK_RAMCC_ENABLE_SET	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_SET	IO_PVU0_TLB_BANK_RAMCC_ENABLE_SET	NAVSS512L_VIRTSS_PAT4_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT4_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT3_EDC_CTRL_BUS_ECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
PAT3_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT2_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT2_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT1_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT1_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT0_TABLE_RAMECC_ENABLE_SET	ECCAGG_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-301. ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCU_DTIB_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_dtib_ramecc_pending
30	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_src_m2m_bridge_navss512l_virtss_io_tbu0_src_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_axi2m_w_busecc_pending

Table 5-301. ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_axi2m_r_busecc_pend
26	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_m2axi_busecc_pend
25	IO_TBU0_ENTB_TAG3_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag3_amecc_pend
24	IO_TBU0_ENTB_TAG2_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag2_amecc_pend
23	IO_TBU0_ENTB_TAG1_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag1_amecc_pend
22	IO_TBU0_ENTB_TAG0_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag0_amecc_pend
21	IO_TBU0_MTLB_TAG3_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag3_amecc_pend
20	IO_TBU0_MTLB_TAG2_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag2_amecc_pend
19	IO_TBU0_MTLB_TAG1_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag1_amecc_pend
18	IO_TBU0_MTLB_TAG0_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag0_amecc_pend
17	IO_TBU0_WBB_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_wbb_amecc_pend
16	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_dma_pvu1_edc_ctrl_busecc_pend
15	DMA_PVU1_TLB_BANK_RAMCC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dma_pvu1_tlb_bank_ramcc_pend
14	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_pvu1_edc_ctrl_busecc_pend
13	IO_PVU1_TLB_BANK_RAMCC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_pvu1_tlb_bank_ramcc_pend
12	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_pvu0_edc_ctrl_busecc_pend
11	IO_PVU0_TLB_BANK_RAMCC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_pvu0_tlb_bank_ramcc_pend
10	NAVSS512L_VIRTSS_PA_T4_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat4_edc_ctrl_busecc_pend
9	PAT4_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat4_table_amecc_pend
8	NAVSS512L_VIRTSS_PA_T3_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat3_edc_ctrl_busecc_pend
7	PAT3_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat3_table_amecc_pend
6	NAVSS512L_VIRTSS_PA_T2_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat2_edc_ctrl_busecc_pend
5	PAT2_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat2_table_amecc_pend
4	NAVSS512L_VIRTSS_PA_T1_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat1_edc_ctrl_busecc_pend

Table 5-301. ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAT1_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat1_table_ramecc_pend
2	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat0_edc_ctrl_busecc_pend
1	PAT0_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat0_table_ramecc_pend
0	ECCAGG_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for eccagg_pend

Table 5-302. Register Call Summary for ECC_SEC_ENABLE_SET_REG0

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_SET_REG0 Register \(Offset = 31002080h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.11 ECC_SEC_ENABLE_SET_REG1 Register (Offset = 084h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG1 is shown in Figure 5-150 and described in Table 5-303.

Return to [Summary Table](#).

Interrupt Enable Set Register 1

Figure 5-150. ECC_SEC_ENABLE_SET_REG1 Register

31	30	29	28	27	26	25	24
NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VIRTSS_DATA_C BASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_SET	SMMU_BUFFER2_WFIFO_RA_MECC_ENABLE_SET	SMMU_BUFFER2_CFIFO_RA_MECC_ENABLE_SET	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_SET	SMMU_BUFFER1_WFIFO_RA_MECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
SMMU_BUFFER1_CFIFO_RA_MECC_ENABLE_SET	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_SET	SMMU_BUFFER0_WFIFO_RA_MECC_ENABLE_SET	SMMU_BUFFER0_CFIFO_RA_MECC_ENABLE_SET	TCU_AXI2M_WBUSECC_ENABLE_SET	TCU_AXI2M_RBUSECC_ENABLE_SET	TCU_WCB_TA_G3_RAMECC_ENABLE_SET	TCU_WCB_TA_G2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
TCU_WCB_TA_G1_RAMECC_ENABLE_SET	TCU_WCB_TA_G0_RAMECC_ENABLE_SET	TCU_CCB_TA_G3_RAMECC_ENABLE_SET	TCU_CCB_TA_G2_RAMECC_ENABLE_SET	TCU_CCB_TA_G1_RAMECC_ENABLE_SET	TCU_CCB_TA_G0_RAMECC_ENABLE_SET	TCU_WCB_ENT_RAMECC_ENABLE_SET	TCU_CCB_ENT_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-303. ECC_SEC_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-303. ECC_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
27	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
26	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
25	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
24	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
23	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
22	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-303. ECC_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_smmu_buffer2_src_edc_ctrl_busecc_pend
19	SMMU_BUFFER2_WFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer2_wfifo_ramecc_pend
18	SMMU_BUFFER2_CFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer2_cfifo_ramecc_pend
17	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_smmu_buffer1_src_edc_ctrl_busecc_pend
16	SMMU_BUFFER1_WFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer1_wfifo_ramecc_pend
15	SMMU_BUFFER1_CFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer1_cfifo_ramecc_pend
14	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_smmu_buffer0_src_edc_ctrl_busecc_pend
13	SMMU_BUFFER0_WFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer0_wfifo_ramecc_pend
12	SMMU_BUFFER0_CFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer0_cfifo_ramecc_pend
11	TCU_AXI2M_W_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_axi2m_w_busecc_pend
10	TCU_AXI2M_R_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_axi2m_r_busecc_pend
9	TCU_WCB_TAG3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag3_ramecc_pend
8	TCU_WCB_TAG2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag2_ramecc_pend
7	TCU_WCB_TAG1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag1_ramecc_pend
6	TCU_WCB_TAG0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag0_ramecc_pend
5	TCU_CCB_TAG3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag3_ramecc_pend
4	TCU_CCB_TAG2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag2_ramecc_pend
3	TCU_CCB_TAG1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag1_ramecc_pend
2	TCU_CCB_TAG0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag0_ramecc_pend
1	TCU_WCB_ENT_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_ent_ramecc_pend

Table 5-303. ECC_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TCU_CCB_ENT_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_ent_ramecc_pend

Table 5-304. Register Call Summary for ECC_SEC_ENABLE_SET_REG1

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_SET_REG1 Register \(Offset = 31002084h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.12 ECC_SEC_ENABLE_SET_REG2 Register (Offset = 088h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG2 is shown in Figure 5-151 and described in Table 5-305.

Return to [Summary Table](#).

Interrupt Enable Set Register 2

Figure 5-151. ECC_SEC_ENABLE_SET_REG2 Register

31	30	29	28	27	26	25	24
NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_1_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_0_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_ECCAG GR_CFG_P2P BRIDGE_ECCA GGR_CFG_BRI DGE_BUSECC _ENABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_SRC_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 3_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV3_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 2_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV2_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 1_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV1_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_DMA_SL V0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_DM A_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_BU SECC_ENABL E_SET	NAVSS512L_VI RTSS_DATA_C BASS_MOD_S LV0_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_M OD_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_B USECC_ENAB LE_SET	NAVSS512L_VI RTSS_DATA_C BASS_AC_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_AC_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_VIRTSS _CFG_P2P_BR IDGE_VIRTSS_ CFG_BRIDGE_ BUSECC_ENA BLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_DST_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 5-151. ECC_SEC_ENABLE_SET_REG2 Register (continued)

NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-305. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_1_pend
30	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_0_pend
29	NAVSS512L_VIRTSS_DATA_CBASS_ECCAGGR_CFG_P2P_BRIDGE_ECCAGGR_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_eccaggr_cfg_p2p_bridge_eccaggr_cfg_bridge_busecc_pend
28	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_src_edc_ctrl_busecc_pend
27	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_src_edc_ctrl_busecc_pend
26	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-305. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
24	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
23	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
22	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat4_src_m2m_bridge_navss512l_virtss_data_cbass_pat4_src_m2m_bridge_src_edc_ctrl_busecc_pend
21	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat3_src_m2m_bridge_navss512l_virtss_data_cbass_pat3_src_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat2_src_m2m_bridge_navss512l_virtss_data_cbass_pat2_src_m2m_bridge_src_edc_ctrl_busecc_pend
19	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat1_src_m2m_bridge_navss512l_virtss_data_cbass_pat1_src_m2m_bridge_src_edc_ctrl_busecc_pend
18	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat0_src_m2m_bridge_navss512l_virtss_data_cbass_pat0_src_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-305. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_src_edc_ctrl_busecc_pend
16	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_src_edc_ctrl_busecc_pend
15	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_src_edc_ctrl_busecc_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
12	NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_VIRTSS_CFG_P2P_BRIDGE_VIRTSS_CFG_P2P_BRIDGE_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_virtss_cfg_p2p_bridge_virtss_cfg_p2p_bridge_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-305. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_src_edc_ctrl_busecc_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_src_edc_ctrl_busecc_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_src_edc_ctrl_busecc_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
2	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-305. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-306. Register Call Summary for ECC_SEC_ENABLE_SET_REG2

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_SET_REG2 Register \(Offset = 31002088h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.13 ECC_SEC_ENABLE_SET_REG3 Register (Offset = 08Ch) [reset = X]

ECC_SEC_ENABLE_SET_REG3 is shown in Figure 5-152 and described in Table 5-307.

Return to [Summary Table](#).

Interrupt Enable Set Register 3

Figure 5-152. ECC_SEC_ENABLE_SET_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
NAVSS512L_VIRTSS_DATA_C BASS_GCLK_EDC_CTRL_CBA SS_INT_GBUSECC_1_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_GCLK_EDC_CTRL_CBA SS_INT_GBUSECC_0_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SR_C_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_S_CR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_CR_EDC_CTRL_BUSECC_1_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_S_CR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_CR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_9_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_8_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_7_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_6_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_5_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_4_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_3_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_2_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-307. ECC_SEC_ENABLE_SET_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_1_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_0_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cbass_int_dmesc_scr_navss512l_virtss_data_cbass_cbass_int_dmesc_scr_edc_ctrl_busecc_pend

Table 5-307. ECC_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_dst_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_src_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cbass_default_mmrs_navss512l_virtss_data_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_1_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_0_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_9_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_8_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_7_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_6_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_5_pend

Table 5-307. ECC_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_4_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_3_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_2_pend

Table 5-308. Register Call Summary for ECC_SEC_ENABLE_SET_REG3

VIRTSS_ECCAGGR_CFG Registers

- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)
- [ECC_SEC_ENABLE_SET_REG3 Register \(Offset = 3100208Ch\) \[reset = X\]: \[0\]](#)

5.2.14 ECC_SEC_ENABLE_CLR_REG0 Register (Offset = 0C0h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG0 is shown in Figure 5-153 and described in Table 5-309.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Figure 5-153. ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
TCU_DTIB_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUS_ECC_ENABLE_CLR	IO_TBU0_ENT_B_TAG3_RAMECC_ENABLE_CLR	IO_TBU0_ENT_B_TAG2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
IO_TBU0_ENT_B_TAG1_RAMECC_ENABLE_CLR	IO_TBU0_ENT_B_TAG0_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG3_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG2_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG1_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG0_RAMECC_ENABLE_CLR	IO_TBU0_WBB_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
DMA_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR	IO_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_CLR	IO_PVU0_TLB_BANK_RAMCC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT4_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT4_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT3_EDC_CTRL_BUS_ECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
PAT3_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT2_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT2_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT1_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT1_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT0_TABLE_RAMECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-309. ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCU_DTIB_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_dtib_ramecc_pend
30	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_edc_ctrl_busecc_pend
29	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_src_m2m_bridge_navss512l_virtss_io_tbu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
28	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_axi2m_w_busecc_pend

Table 5-309. ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_axi2m_r_busecc_pend
26	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_m2axi_busecc_pend
25	IO_TBU0_ENTB_TAG3_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag3_amecc_pend
24	IO_TBU0_ENTB_TAG2_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag2_amecc_pend
23	IO_TBU0_ENTB_TAG1_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag1_amecc_pend
22	IO_TBU0_ENTB_TAG0_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag0_amecc_pend
21	IO_TBU0_MTLB_TAG3_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag3_amecc_pend
20	IO_TBU0_MTLB_TAG2_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag2_amecc_pend
19	IO_TBU0_MTLB_TAG1_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag1_amecc_pend
18	IO_TBU0_MTLB_TAG0_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag0_amecc_pend
17	IO_TBU0_WBB_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_wbb_amecc_pend
16	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_dma_pvu1_edc_ctrl_busecc_pend
15	DMA_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dma_pvu1_tlb_bank_ramcc_pend
14	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_pvu1_edc_ctrl_busecc_pend
13	IO_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_pvu1_tlb_bank_ramcc_pend
12	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_pvu0_edc_ctrl_busecc_pend
11	IO_PVU0_TLB_BANK_RAMCC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_pvu0_tlb_bank_ramcc_pend
10	NAVSS512L_VIRTSS_PA_T4_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat4_edc_ctrl_busecc_pend
9	PAT4_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat4_table_amecc_pend
8	NAVSS512L_VIRTSS_PA_T3_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat3_edc_ctrl_busecc_pend
7	PAT3_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat3_table_amecc_pend
6	NAVSS512L_VIRTSS_PA_T2_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat2_edc_ctrl_busecc_pend
5	PAT2_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat2_table_amecc_pend
4	NAVSS512L_VIRTSS_PA_T1_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat1_edc_ctrl_busecc_pend

Table 5-309. ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAT1_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat1_table_ramecc_pend
2	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat0_edc_ctrl_busecc_pend
1	PAT0_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat0_table_ramecc_pend
0	ECCAGG_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for eccagg_pend

Table 5-310. Register Call Summary for ECC_SEC_ENABLE_CLR_REG0

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_CLR_REG0 Register \(Offset = 310020C0h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.15 ECC_SEC_ENABLE_CLR_REG1 Register (Offset = 0C4h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG1 is shown in Figure 5-154 and described in Table 5-311.

Return to [Summary Table](#).

Interrupt Enable Clear Register 1

Figure 5-154. ECC_SEC_ENABLE_CLR_REG1 Register

31	30	29	28	27	26	25	24
NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS512L_VIRTSS_DATA_C BASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	SMMU_BUFFER2_WFIFO_RA_MECC_ENABLE_CLR	SMMU_BUFFER2_CFIFO_RA_MECC_ENABLE_CLR	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	SMMU_BUFFER1_WFIFO_RA_MECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
SMMU_BUFFER1_CFIFO_RA_MECC_ENABLE_CLR	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	SMMU_BUFFER0_WFIFO_RA_MECC_ENABLE_CLR	SMMU_BUFFER0_CFIFO_RA_MECC_ENABLE_CLR	TCU_AXI2M_WBUSECC_ENABLE_CLR	TCU_AXI2M_RBUSECC_ENABLE_CLR	TCU_WCB_TAG3_RAMECC_ENABLE_CLR	TCU_WCB_TAG2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
TCU_WCB_TAG1_RAMECC_ENABLE_CLR	TCU_WCB_TAG0_RAMECC_ENABLE_CLR	TCU_CCB_TAG3_RAMECC_ENABLE_CLR	TCU_CCB_TAG2_RAMECC_ENABLE_CLR	TCU_CCB_TAG1_RAMECC_ENABLE_CLR	TCU_CCB_TAG0_RAMECC_ENABLE_CLR	TCU_WCB_ENT_RAMECC_ENABLE_CLR	TCU_CCB_ENT_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-311. ECC_SEC_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-311. ECC_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
27	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
26	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
25	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
24	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
23	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
22	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-311. ECC_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_smmu_buffer2_src_edc_ctrl_busecc_pend
19	SMMU_BUFFER2_WFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer2_wfifo_ramecc_pend
18	SMMU_BUFFER2_CFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer2_cfifo_ramecc_pend
17	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_smmu_buffer1_src_edc_ctrl_busecc_pend
16	SMMU_BUFFER1_WFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer1_wfifo_ramecc_pend
15	SMMU_BUFFER1_CFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer1_cfifo_ramecc_pend
14	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_smmu_buffer0_src_edc_ctrl_busecc_pend
13	SMMU_BUFFER0_WFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer0_wfifo_ramecc_pend
12	SMMU_BUFFER0_CFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer0_cfifo_ramecc_pend
11	TCU_AXI2M_W_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_axi2m_w_busecc_pend
10	TCU_AXI2M_R_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_axi2m_r_busecc_pend
9	TCU_WCB_TAG3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag3_ramecc_pend
8	TCU_WCB_TAG2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag2_ramecc_pend
7	TCU_WCB_TAG1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag1_ramecc_pend
6	TCU_WCB_TAG0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag0_ramecc_pend
5	TCU_CCB_TAG3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag3_ramecc_pend
4	TCU_CCB_TAG2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag2_ramecc_pend
3	TCU_CCB_TAG1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag1_ramecc_pend
2	TCU_CCB_TAG0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag0_ramecc_pend

Table 5-311. ECC_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TCU_WCB_ENT_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_ent_ramecc_pend
0	TCU_CCB_ENT_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_ent_ramecc_pend

Table 5-312. Register Call Summary for ECC_SEC_ENABLE_CLR_REG1

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_CLR_REG1 Register \(Offset = 310020C4h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.16 ECC_SEC_ENABLE_CLR_REG2 Register (Offset = 0C8h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG2 is shown in Figure 5-155 and described in Table 5-313.

Return to [Summary Table](#).

Interrupt Enable Clear Register 2

Figure 5-155. ECC_SEC_ENABLE_CLR_REG2 Register

31	30	29	28	27	26	25	24
NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_1_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_0_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_ECCAG GR_CFG_P2P BRIDGE_ECCA GGR_CFG_BRI DGE_BUSECC _ENABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_SRC_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 3_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV3_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 2_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV2_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 1_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV1_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_DMA_SL V0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_DM A_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_BU SECC_ENABL E_CLR	NAVSS512L_VI RTSS_DATA_C BASS_MOD_S LV0_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_M OD_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_B USECC_ENAB LE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_AC_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_AC_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_VIRTSS _CFG_P2P_BR IDGE_VIRTSS_ CFG_BRIDGE_ BUSECC_ENA BLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_DST_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0

Figure 5-155. ECC_SEC_ENABLE_CLR_REG2 Register (continued)

NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-313. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_1_pend
30	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_0_pend
29	NAVSS512L_VIRTSS_DATA_CBASS_ECCAGGR_CFG_P2P_BRIDGE_ECCAGGR_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_eccaggr_cfg_p2p_bridge_eccaggr_cfg_bridge_busecc_pend
28	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_src_edc_ctrl_busecc_pend
27	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_src_edc_ctrl_busecc_pend
26	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-313. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
24	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
23	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
22	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat4_src_m2m_bridge_navss512l_virtss_data_cbass_pat4_src_m2m_bridge_src_edc_ctrl_busecc_pend
21	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat3_src_m2m_bridge_navss512l_virtss_data_cbass_pat3_src_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat2_src_m2m_bridge_navss512l_virtss_data_cbass_pat2_src_m2m_bridge_src_edc_ctrl_busecc_pend
19	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat1_src_m2m_bridge_navss512l_virtss_data_cbass_pat1_src_m2m_bridge_src_edc_ctrl_busecc_pend
18	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat0_src_m2m_bridge_navss512l_virtss_data_cbass_pat0_src_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-313. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_src_edc_ctrl_busecc_pend
16	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_src_edc_ctrl_busecc_pend
15	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_src_edc_ctrl_busecc_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
12	NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_VIRTSS_CFG_P2P_BRIDGE_VIRTSS_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_virtss_cfg_p2p_bridge_virtss_cfg_bridge_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-313. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_src_edc_ctrl_busecc_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_src_edc_ctrl_busecc_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_src_edc_ctrl_busecc_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
2	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-313. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-314. Register Call Summary for ECC_SEC_ENABLE_CLR_REG2

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_CLR_REG2 Register \(Offset = 310020C8h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.17 ECC_SEC_ENABLE_CLR_REG3 Register (Offset = 0CCh) [reset = X]

ECC_SEC_ENABLE_CLR_REG3 is shown in Figure 5-156 and described in Table 5-315.

Return to [Summary Table](#).

Interrupt Enable Clear Register 3

Figure 5-156. ECC_SEC_ENABLE_CLR_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
NAVSS512L_VIRTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUS ECC_1_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUS ECC_0_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DS_T_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SR_C_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_EDC_CTRL_BUSECC_1_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_9_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_8_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_7_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_6_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_5_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_4_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_3_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_2_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-315. ECC_SEC_ENABLE_CLR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_1_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_0_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cbass_int_dmesc_scr_navss512l_virtss_data_cbass_cbass_int_dmesc_scr_edc_ctrl_busecc_pend

Table 5-315. ECC_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_dst_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_src_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cbass_default_mmrs_navss512l_virtss_data_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_1_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_0_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_9_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_8_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_7_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_6_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_5_pend

Table 5-315. ECC_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_4_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_4_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_3_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_2_pend

Table 5-316. Register Call Summary for ECC_SEC_ENABLE_CLR_REG3

VIRTSS_ECCAGGR_CFG Registers

- [ECC_SEC_ENABLE_CLR_REG3 Register \(Offset = 310020CCh\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.18 ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

ECC_DED_EOI_REG is shown in [Figure 5-157](#) and described in [Table 5-317](#).

Return to [Summary Table](#).

EOI Register

Figure 5-157. ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-317. ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

Table 5-318. Register Call Summary for ECC_DED_EOI_REG

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_EOI_REG Register \(Offset = 3100213Ch\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.19 ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

ECC_DED_STATUS_REG0 is shown in Figure 5-158 and described in Table 5-319.

Return to [Summary Table](#).

Interrupt Status Register 0

Figure 5-158. ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
TCU_DTIB_RA MECC_PEND	NAVSS512L_VI RTSS_IO_TBU 0_EDC_CTRL_ BUSECC_PEN D	NAVSS512L_VI RTSS_IO_TBU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_I O_TBU0_SRC_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_IO_TBU 0_AXI2M_W_B USECC_PEND	NAVSS512L_VI RTSS_IO_TBU 0_AXI2M_R_B USECC_PEND	NAVSS512L_VI RTSS_IO_TBU 0_M2AXI_BUS ECC_PEND	IO_TBU0_ENT B_TAG3_RAME CC_PEND	IO_TBU0_ENT B_TAG2_RAME CC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
IO_TBU0_ENT B_TAG1_RAME CC_PEND	IO_TBU0_ENT B_TAG0_RAME CC_PEND	IO_TBU0_MTL B_TAG3_RAME CC_PEND	IO_TBU0_MTL B_TAG2_RAME CC_PEND	IO_TBU0_MTL B_TAG1_RAME CC_PEND	IO_TBU0_MTL B_TAG0_RAME CC_PEND	IO_TBU0_WBB _RAMECC_PE ND	NAVSS512L_VI RTSS_DMA_P VU1_EDC_CTR L_BUSECC_PE ND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
DMA_PVU1_TL B_BANK_RAM CC_PEND	NAVSS512L_VI RTSS_IO_PVU 1_EDC_CTRL_ BUSECC_PEN D	IO_PVU1_TLB BANK_RAMCC _PEND	NAVSS512L_VI RTSS_IO_PVU 0_EDC_CTRL_ BUSECC_PEN D	IO_PVU0_TLB BANK_RAMCC _PEND	NAVSS512L_VI RTSS_PAT4_E DC_CTRL_BUS ECC_PEND	PAT4_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT3_E DC_CTRL_BUS ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
PAT3_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT2_E DC_CTRL_BUS ECC_PEND	PAT2_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT1_E DC_CTRL_BUS ECC_PEND	PAT1_TABLE_ RAMECC_PEN D	NAVSS512L_VI RTSS_PAT0_E DC_CTRL_BUS ECC_PEND	PAT0_TABLE_ RAMECC_PEN D	ECCAGG_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-319. ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCU_DTIB_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_dtib_amecc_pending
30	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_src_m2m_bridge_navss512l_virtss_io_tbu0_src_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_axi2m_w_busecc_pending

Table 5-319. ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_axi2m_r_busecc_pend
26	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_tbu0_m2axi_busecc_pend
25	IO_TBU0_ENTB_TAG3_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag3_amecc_pend
24	IO_TBU0_ENTB_TAG2_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag2_amecc_pend
23	IO_TBU0_ENTB_TAG1_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag1_amecc_pend
22	IO_TBU0_ENTB_TAG0_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_entb_tag0_amecc_pend
21	IO_TBU0_MTLB_TAG3_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag3_amecc_pend
20	IO_TBU0_MTLB_TAG2_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag2_amecc_pend
19	IO_TBU0_MTLB_TAG1_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag1_amecc_pend
18	IO_TBU0_MTLB_TAG0_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_mtlb_tag0_amecc_pend
17	IO_TBU0_WBB_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for io_tbu0_wbb_amecc_pend
16	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_dma_pvu1_edc_ctrl_busecc_pend
15	DMA_PVU1_TLB_BANK_RAMCC_PEND	R/W1S	0h	Interrupt Pending Status for dma_pvu1_tlb_bank_ramcc_pend
14	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_pvu1_edc_ctrl_busecc_pend
13	IO_PVU1_TLB_BANK_RAMCC_PEND	R/W1S	0h	Interrupt Pending Status for io_pvu1_tlb_bank_ramcc_pend
12	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_io_pvu0_edc_ctrl_busecc_pend
11	IO_PVU0_TLB_BANK_RAMCC_PEND	R/W1S	0h	Interrupt Pending Status for io_pvu0_tlb_bank_ramcc_pend
10	NAVSS512L_VIRTSS_PA_T4_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat4_edc_ctrl_busecc_pend
9	PAT4_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat4_table_amecc_pend
8	NAVSS512L_VIRTSS_PA_T3_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat3_edc_ctrl_busecc_pend
7	PAT3_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat3_table_amecc_pend
6	NAVSS512L_VIRTSS_PA_T2_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat2_edc_ctrl_busecc_pend
5	PAT2_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat2_table_amecc_pend
4	NAVSS512L_VIRTSS_PA_T1_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat1_edc_ctrl_busecc_pend

Table 5-319. ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAT1_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat1_table_ramecc_pend
2	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_pat0_edc_ctrl_busecc_pend
1	PAT0_TABLE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for pat0_table_ramecc_pend
0	ECCAGG_PEND	R/W1S	0h	Interrupt Pending Status for eccagg_pend

Table 5-320. Register Call Summary for ECC_DED_STATUS_REG0

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_STATUS_REG0 Register \(Offset = 31002140h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.20 ECC_DED_STATUS_REG1 Register (Offset = 144h) [reset = 0h]

ECC_DED_STATUS_REG1 is shown in Figure 5-159 and described in Table 5-321.

Return to [Summary Table](#).

Interrupt Status Register 1

Figure 5-159. ECC_DED_STATUS_REG1 Register

31	30	29	28	27	26	25	24
NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VIRTSS_DATA_C BASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	NAVSS512L_VIRTSS_DATA_C SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_PENDING	SMMU_BUFFER2_WFIFO_RA_MECC_PENDING	SMMU_BUFFER2_CFIFO_RA_MECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	SMMU_BUFFER1_WFIFO_RA_MECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
SMMU_BUFFER1_CFIFO_RA_MECC_PENDING	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	SMMU_BUFFER0_WFIFO_RA_MECC_PENDING	SMMU_BUFFER0_CFIFO_RA_MECC_PENDING	TCU_AXI2M_WBUSECC_PENDING	TCU_AXI2M_RBUSECC_PENDING	TCU_WCB_TAG3_RAMECC_PENDING	TCU_WCB_TAG2_RAMECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
TCU_WCB_TAG1_RAMECC_PENDING	TCU_WCB_TAG0_RAMECC_PENDING	TCU_CCB_TAG3_RAMECC_PENDING	TCU_CCB_TAG2_RAMECC_PENDING	TCU_CCB_TAG1_RAMECC_PENDING	TCU_CCB_TAG0_RAMECC_PENDING	TCU_WCB_ENT_RAMECC_PENDING	TCU_CCB_ENT_RAMECC_PENDING
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-321. ECC_DED_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-321. ECC_DED_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
27	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
26	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
25	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
24	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
23	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
22	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-321. ECC_DED_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_smmu_buffer2_src_edc_ctrl_busecc_pend
19	SMMU_BUFFER2_WFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer2_wfifo_ramecc_pend
18	SMMU_BUFFER2_CFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer2_cfifo_ramecc_pend
17	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_smmu_buffer1_src_edc_ctrl_busecc_pend
16	SMMU_BUFFER1_WFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer1_wfifo_ramecc_pend
15	SMMU_BUFFER1_CFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer1_cfifo_ramecc_pend
14	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_smmu_buffer0_src_edc_ctrl_busecc_pend
13	SMMU_BUFFER0_WFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer0_wfifo_ramecc_pend
12	SMMU_BUFFER0_CFIFO_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for smmu_buffer0_cfifo_ramecc_pend
11	TCU_AXI2M_W_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_axi2m_w_busecc_pend
10	TCU_AXI2M_R_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_axi2m_r_busecc_pend
9	TCU_WCB_TAG3_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag3_ramecc_pend
8	TCU_WCB_TAG2_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag2_ramecc_pend
7	TCU_WCB_TAG1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag1_ramecc_pend
6	TCU_WCB_TAG0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_tag0_ramecc_pend
5	TCU_CCB_TAG3_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag3_ramecc_pend
4	TCU_CCB_TAG2_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag2_ramecc_pend
3	TCU_CCB_TAG1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag1_ramecc_pend
2	TCU_CCB_TAG0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_tag0_ramecc_pend
1	TCU_WCB_ENT_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_wcb_ent_ramecc_pend
0	TCU_CCB_ENT_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for tcu_ccb_ent_ramecc_pend

Table 5-322. Register Call Summary for ECC_DED_STATUS_REG1

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_STATUS_REG1 Register \(Offset = 31002144h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.21 ECC_DED_STATUS_REG2 Register (Offset = 148h) [reset = 0h]

ECC_DED_STATUS_REG2 is shown in Figure 5-160 and described in Table 5-323.

Return to [Summary Table](#).

Interrupt Status Register 2

Figure 5-160. ECC_DED_STATUS_REG2 Register

31	30	29	28	27	26	25	24
NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_1_PEND	NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_0_PEND	NAVSS512L_VI RTSS_DATA_C BASS_ECCAG GR_CFG_P2P BRIDGE_ECCA GGR_CFG_BRI DGE_BUSECC _PEND	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_SRC_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 3_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV3_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 2_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV2_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 1_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV1_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_DMA_SL V0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_DM A_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_BU SECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_MOD_S LV0_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_M OD_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_B USECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_AC_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_AC_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_VIRTSS _CFG_P2P_BR IDGE_VIRTSS_ CFG_BRIDGE_ BUSECC_PEN D	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_DST_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_P END	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_D ST_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_NB_MS T0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_NB_ MST0_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_PEND	NAVSS512L_VI RTSS_DATA_C BASS_DMA_M ST3_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_D MA_MST3_M2 M_BRIDGE_SR C_EDC_CTRL_ BUSECC_PEN D

Figure 5-160. ECC_DED_STATUS_REG2 Register (continued)

R/W1S-0h R/W1S-0h R/W1S-0h R/W1S-0h R/W1S-0h R/W1S-0h R/W1S-0h R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-323. ECC_DED_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_1_pend
30	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_0_pend
29	NAVSS512L_VIRTSS_DATA_CBASS_ECCAGGR_CFG_P2P_BRIDGE_ECC AGGR_CFG_BRIDGE_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_eccaggr_cfg_p2p_bridge_eccaggr_cf g_bridge_busecc_pend
28	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_ NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_ SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_navss 512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_src_edc_ctr l_busecc_pend
27	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_ NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_ SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_navss 512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_src_edc_ctr l_busecc_pend
26	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_ NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_ SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_navss 512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_src_edc_ctr l_busecc_pend
25	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_NAV SS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_SRC_EDC CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_navss51 2l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_src_edc_ctrl_bu secc_pend
24	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_NAVSS 512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_SRC_EDC_C TRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_navss512l _virtss_data_cbass_io_pvu1_src_m2m_bridge_src_edc_ctrl_busecc _pend

Table 5-323. ECC_DED_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
22	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat4_src_m2m_bridge_navss512l_virtss_data_cbass_pat4_src_m2m_bridge_src_edc_ctrl_busecc_pend
21	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat3_src_m2m_bridge_navss512l_virtss_data_cbass_pat3_src_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat2_src_m2m_bridge_navss512l_virtss_data_cbass_pat2_src_m2m_bridge_src_edc_ctrl_busecc_pend
19	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat1_src_m2m_bridge_navss512l_virtss_data_cbass_pat1_src_m2m_bridge_src_edc_ctrl_busecc_pend
18	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat0_src_m2m_bridge_navss512l_virtss_data_cbass_pat0_src_m2m_bridge_src_edc_ctrl_busecc_pend
17	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_src_edc_ctrl_busecc_pend
16	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_src_edc_ctrl_busecc_pend
15	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-323. ECC_DED_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
12	NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_VIRTSS_CFG_P2P_BRIDGE_VIRTSS_CFG_BRIDGE_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_virtss_cfg_p2p_bridge_virtss_cfg_bridge_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-323. ECC_DED_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_src_edc_ctrl_busecc_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_src_edc_ctrl_busecc_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
2	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-324. Register Call Summary for ECC_DED_STATUS_REG2

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_STATUS_REG2 Register \(Offset = 31002148h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.22 ECC_DED_STATUS_REG3 Register (Offset = 14Ch) [reset = X]

ECC_DED_STATUS_REG3 is shown in Figure 5-161 and described in Table 5-325.

Return to [Summary Table](#).

Interrupt Status Register 3

Figure 5-161. ECC_DED_STATUS_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUSECC_1_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUSECC_0_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DS_T_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SR_C_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CFG_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_EDC_CTRL_BUSECC_1_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_CFG_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_EDC_CTRL_BUSECC_0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_4_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_3_PEND	NAVSS512L_VIRTSS_DATA_C RTSS_DATA_C BASS_SCR_S CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_2_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-325. ECC_DED_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_1_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_0_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cbass_int_dmsc_scr_navss512l_virtss_data_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend

Table 5-325. ECC_DED_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DST_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_dst_busecc_pending
11	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SRC_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_src_busecc_pending
10	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cbass_default_mmrs_navss512l_virtss_data_cbass_cbass_default_mmrs_edc_ctrl_busecc_pending
9	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_1_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_1_pending
8	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_0_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_0_pending
7	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_9_pending
6	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_8_pending
5	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_7_pending
4	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_6_pending
3	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_PENDING	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_5_pending

Table 5-325. ECC_DED_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_4_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_4_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_3_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_3_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_2_PEND	R/W1S	0h	Interrupt Pending Status for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_2_pend

Table 5-326. Register Call Summary for ECC_DED_STATUS_REG3

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_STATUS_REG3 Register \(Offset = 3100214Ch\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.23 ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

ECC_DED_ENABLE_SET_REG0 is shown in Figure 5-162 and described in Table 5-327.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Figure 5-162. ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
TCU_DTIB_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUS_ECC_ENABLE_SET	IO_TBU0_ENTB_TAG3_RAMECC_ENABLE_SET	IO_TBU0_ENTB_TAG2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
IO_TBU0_ENTB_TAG1_RAMECC_ENABLE_SET	IO_TBU0_ENTB_TAG0_RAMECC_ENABLE_SET	IO_TBU0_MTLB_TAG3_RAMECC_ENABLE_SET	IO_TBU0_MTLB_TAG2_RAMECC_ENABLE_SET	IO_TBU0_MTLB_TAG1_RAMECC_ENABLE_SET	IO_TBU0_MTLB_TAG0_RAMECC_ENABLE_SET	IO_TBU0_WBB_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
DMA_PVU1_TLB_BANK_RAMCC_ENABLE_SET	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_SET	IO_PVU1_TLB_BANK_RAMCC_ENABLE_SET	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_SET	IO_PVU0_TLB_BANK_RAMCC_ENABLE_SET	NAVSS512L_VIRTSS_PAT4_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT4_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT3_EDC_CTRL_BUS_ECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
PAT3_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT2_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT2_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT1_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT1_TABLE_RAMECC_ENABLE_SET	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUS_ECC_ENABLE_SET	PAT0_TABLE_RAMECC_ENABLE_SET	ECCAGG_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-327. ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCU_DTIB_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_dtib_ramecc_pending
30	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_src_m2m_bridge_navss512l_virtss_io_tbu0_src_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_axi2m_w_busecc_pending

Table 5-327. ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_axi2m_r_busecc_pend
26	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_tbu0_m2axi_busecc_pend
25	IO_TBU0_ENTB_TAG3_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag3_amecc_pend
24	IO_TBU0_ENTB_TAG2_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag2_amecc_pend
23	IO_TBU0_ENTB_TAG1_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag1_amecc_pend
22	IO_TBU0_ENTB_TAG0_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_entb_tag0_amecc_pend
21	IO_TBU0_MTLB_TAG3_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag3_amecc_pend
20	IO_TBU0_MTLB_TAG2_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag2_amecc_pend
19	IO_TBU0_MTLB_TAG1_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag1_amecc_pend
18	IO_TBU0_MTLB_TAG0_R_AMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_mtlb_tag0_amecc_pend
17	IO_TBU0_WBB_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_tbu0_wbb_amecc_pend
16	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_dma_pvu1_edc_ctrl_busecc_pend
15	DMA_PVU1_TLB_BANK_RAMCC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for dma_pvu1_tlb_bank_ramcc_pend
14	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_pvu1_edc_ctrl_busecc_pend
13	IO_PVU1_TLB_BANK_RAMCC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_pvu1_tlb_bank_ramcc_pend
12	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_io_pvu0_edc_ctrl_busecc_pend
11	IO_PVU0_TLB_BANK_RAMCC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for io_pvu0_tlb_bank_ramcc_pend
10	NAVSS512L_VIRTSS_PA_T4_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat4_edc_ctrl_busecc_pend
9	PAT4_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat4_table_amecc_pend
8	NAVSS512L_VIRTSS_PA_T3_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat3_edc_ctrl_busecc_pend
7	PAT3_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat3_table_amecc_pend
6	NAVSS512L_VIRTSS_PA_T2_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat2_edc_ctrl_busecc_pend
5	PAT2_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat2_table_amecc_pend
4	NAVSS512L_VIRTSS_PA_T1_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat1_edc_ctrl_busecc_pend

Table 5-327. ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAT1_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat1_table_ramecc_pend
2	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_pat0_edc_ctrl_busecc_pend
1	PAT0_TABLE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for pat0_table_ramecc_pend
0	ECCAGG_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for eccagg_pend

Table 5-328. Register Call Summary for ECC_DED_ENABLE_SET_REG0

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_SET_REG0 Register \(Offset = 31002180h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.24 ECC_DED_ENABLE_SET_REG1 Register (Offset = 184h) [reset = 0h]

ECC_DED_ENABLE_SET_REG1 is shown in Figure 5-163 and described in Table 5-329.

Return to [Summary Table](#).

Interrupt Enable Set Register 1

Figure 5-163. ECC_DED_ENABLE_SET_REG1 Register

31	30	29	28	27	26	25	24
NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VIRTSS_DATA_C BASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_SET	SMMU_BUFFER2_WFIFO_RA_MECC_ENABLE_SET	SMMU_BUFFER2_CFIFO_RA_MECC_ENABLE_SET	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_SET	SMMU_BUFFER1_WFIFO_RA_MECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
SMMU_BUFFER1_CFIFO_RA_MECC_ENABLE_SET	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_SET	SMMU_BUFFER0_WFIFO_RA_MECC_ENABLE_SET	SMMU_BUFFER0_CFIFO_RA_MECC_ENABLE_SET	TCU_AXI2M_WBUSECC_ENABLE_SET	TCU_AXI2M_RBUSECC_ENABLE_SET	TCU_WCB_TAG3_RAMECC_ENABLE_SET	TCU_WCB_TAG2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
TCU_WCB_TAG1_RAMECC_ENABLE_SET	TCU_WCB_TAG0_RAMECC_ENABLE_SET	TCU_CCB_TAG3_RAMECC_ENABLE_SET	TCU_CCB_TAG2_RAMECC_ENABLE_SET	TCU_CCB_TAG1_RAMECC_ENABLE_SET	TCU_CCB_TAG0_RAMECC_ENABLE_SET	TCU_WCB_ENT_RAMECC_ENABLE_SET	TCU_CCB_ENT_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-329. ECC_DED_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-329. ECC_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
27	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
26	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
25	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
24	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
23	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
22	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-329. ECC_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_smmu_buffer2_src_edc_ctrl_busecc_pend
19	SMMU_BUFFER2_WFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer2_wfifo_ramecc_pend
18	SMMU_BUFFER2_CFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer2_cfifo_ramecc_pend
17	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_smmu_buffer1_src_edc_ctrl_busecc_pend
16	SMMU_BUFFER1_WFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer1_wfifo_ramecc_pend
15	SMMU_BUFFER1_CFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer1_cfifo_ramecc_pend
14	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_smmu_buffer0_src_edc_ctrl_busecc_pend
13	SMMU_BUFFER0_WFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer0_wfifo_ramecc_pend
12	SMMU_BUFFER0_CFIFO_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for smmu_buffer0_cfifo_ramecc_pend
11	TCU_AXI2M_W_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_axi2m_w_busecc_pend
10	TCU_AXI2M_R_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_axi2m_r_busecc_pend
9	TCU_WCB_TAG3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag3_ramecc_pend
8	TCU_WCB_TAG2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag2_ramecc_pend
7	TCU_WCB_TAG1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag1_ramecc_pend
6	TCU_WCB_TAG0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_tag0_ramecc_pend
5	TCU_CCB_TAG3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag3_ramecc_pend
4	TCU_CCB_TAG2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag2_ramecc_pend
3	TCU_CCB_TAG1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag1_ramecc_pend
2	TCU_CCB_TAG0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_tag0_ramecc_pend
1	TCU_WCB_ENT_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_wcb_ent_ramecc_pend

Table 5-329. ECC_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TCU_CCB_ENT_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for tcu_ccb_ent_ramecc_pend

Table 5-330. Register Call Summary for ECC_DED_ENABLE_SET_REG1

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_SET_REG1 Register \(Offset = 31002184h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.25 ECC_DED_ENABLE_SET_REG2 Register (Offset = 188h) [reset = 0h]

ECC_DED_ENABLE_SET_REG2 is shown in Figure 5-164 and described in Table 5-331.

Return to [Summary Table](#).

Interrupt Enable Set Register 2

Figure 5-164. ECC_DED_ENABLE_SET_REG2 Register

31	30	29	28	27	26	25	24
NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_1_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_0_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_ECCAG GR_CFG_P2P BRIDGE_ECCA GGR_CFG_BRI DGE_BUSECC _ENABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_SRC_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 3_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV3_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 2_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV2_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 1_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV1_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_DMA_SL V0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_DM A_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_BU SECC_ENABL E_SET	NAVSS512L_VI RTSS_DATA_C BASS_MOD_S LV0_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_M OD_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_B USECC_ENAB LE_SET	NAVSS512L_VI RTSS_DATA_C BASS_AC_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_AC_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS512L_VI RTSS_DATA_C BASS_VIRTSS _CFG_P2P_BR IDGE_VIRTSS_ CFG_BRIDGE_ BUSECC_ENA BLE_SET	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_DST_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ SET	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 5-164. ECC_DED_ENABLE_SET_REG2 Register (continued)

NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-331. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_1_pend
30	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_0_pend
29	NAVSS512L_VIRTSS_DATA_CBASS_ECCAGGR_CFG_P2P_BRIDGE_ECCAGGR_CFG_BRIDGE_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_eccaggr_cfg_p2p_bridge_eccaggr_cfg_bridge_busecc_pend
28	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_src_edc_ctrl_busecc_pend
27	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_src_edc_ctrl_busecc_pend
26	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-331. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
24	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
23	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
22	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat4_src_m2m_bridge_navss512l_virtss_data_cbass_pat4_src_m2m_bridge_src_edc_ctrl_busecc_pend
21	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat3_src_m2m_bridge_navss512l_virtss_data_cbass_pat3_src_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat2_src_m2m_bridge_navss512l_virtss_data_cbass_pat2_src_m2m_bridge_src_edc_ctrl_busecc_pend
19	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat1_src_m2m_bridge_navss512l_virtss_data_cbass_pat1_src_m2m_bridge_src_edc_ctrl_busecc_pend
18	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat0_src_m2m_bridge_navss512l_virtss_data_cbass_pat0_src_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-331. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_src_edc_ctrl_busecc_pend
16	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_src_edc_ctrl_busecc_pend
15	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_src_edc_ctrl_busecc_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
12	NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_VIRTSS_CFG_P2P_BRIDGE_VIRTSS_CFG_P2P_BRIDGE_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_virtss_cfg_p2p_bridge_virtss_cfg_p2p_bridge_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-331. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_src_edc_ctrl_busecc_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_src_edc_ctrl_busecc_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_src_edc_ctrl_busecc_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
2	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-331. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-332. Register Call Summary for ECC_DED_ENABLE_SET_REG2

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_SET_REG2 Register \(Offset = 31002188h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.26 ECC_DED_ENABLE_SET_REG3 Register (Offset = 18Ch) [reset = X]

ECC_DED_ENABLE_SET_REG3 is shown in Figure 5-165 and described in Table 5-333.

Return to [Summary Table](#).

Interrupt Enable Set Register 3

Figure 5-165. ECC_DED_ENABLE_SET_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
NAVSS512L_VIRTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUS ECC_1_ENABLE E_SET	NAVSS512L_VIRTSS_DATA_C BASS_GCLK_E DC_CTRL_CBA SS_INT_GBUS ECC_0_ENABLE E_SET	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SR_C_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_S_CR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_CR_EDC_CTRL_BUSECC_1_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_S_CR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_S_CR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_9_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_8_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_7_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_6_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_5_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_4_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_3_ENABLE_SET	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_EDC_CTRL_BUSECC_2_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-333. ECC_DED_ENABLE_SET_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_1_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_0_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cbass_int_dmesc_scr_navss512l_virtss_data_cbass_cbass_int_dmesc_scr_edc_ctrl_busecc_pend

Table 5-333. ECC_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_dst_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_src_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cbass_default_mmrs_navss512l_virtss_data_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_1_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_0_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_9_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_8_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_7_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_6_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_5_pend

Table 5-333. ECC_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_4_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_3_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_2_pend

Table 5-334. Register Call Summary for ECC_DED_ENABLE_SET_REG3

VIRTSS_ECCAGGR_CFG Registers

- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)
- [ECC_DED_ENABLE_SET_REG3 Register \(Offset = 3100218Ch\) \[reset = X\]: \[0\]](#)

5.2.27 ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG0 is shown in Figure 5-166 and described in Table 5-335.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Figure 5-166. ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
TCU_DTIB_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUS_ECC_ENABLE_CLR	IO_TBU0_ENT_B_TAG3_RAMECC_ENABLE_CLR	IO_TBU0_ENT_B_TAG2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
IO_TBU0_ENT_B_TAG1_RAMECC_ENABLE_CLR	IO_TBU0_ENT_B_TAG0_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG3_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG2_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG1_RAMECC_ENABLE_CLR	IO_TBU0_MTL_B_TAG0_RAMECC_ENABLE_CLR	IO_TBU0_WBB_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
DMA_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR	IO_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_CLR	IO_PVU0_TLB_BANK_RAMCC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT4_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT4_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT3_EDC_CTRL_BUS_ECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
PAT3_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT2_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT2_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT1_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT1_TABLE_RAMECC_ENABLE_CLR	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUS_ECC_ENABLE_CLR	PAT0_TABLE_RAMECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-335. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TCU_DTIB_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_dtib_ramecc_pending
30	NAVSS512L_VIRTSS_IO_TBU0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_IO_TBU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_src_m2m_bridge_navss512l_virtss_io_tbu0_src_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_W_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_axi2m_w_busecc_pending

Table 5-335. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS512L_VIRTSS_IO_TBU0_AXI2M_R_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_axi2m_r_busecc_pend
26	NAVSS512L_VIRTSS_IO_TBU0_M2AXI_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_tbu0_m2axi_busecc_pend
25	IO_TBU0_ENTB_TAG3_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag3_amecc_pend
24	IO_TBU0_ENTB_TAG2_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag2_amecc_pend
23	IO_TBU0_ENTB_TAG1_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag1_amecc_pend
22	IO_TBU0_ENTB_TAG0_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_entb_tag0_amecc_pend
21	IO_TBU0_MTLB_TAG3_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag3_amecc_pend
20	IO_TBU0_MTLB_TAG2_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag2_amecc_pend
19	IO_TBU0_MTLB_TAG1_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag1_amecc_pend
18	IO_TBU0_MTLB_TAG0_R_AMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_mtlb_tag0_amecc_pend
17	IO_TBU0_WBB_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_tbu0_wbb_amecc_pend
16	NAVSS512L_VIRTSS_DMA_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_dma_pvu1_edc_ctrl_busecc_pend
15	DMA_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for dma_pvu1_tlb_bank_ramcc_pend
14	NAVSS512L_VIRTSS_IO_PVU1_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_pvu1_edc_ctrl_busecc_pend
13	IO_PVU1_TLB_BANK_RAMCC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_pvu1_tlb_bank_ramcc_pend
12	NAVSS512L_VIRTSS_IO_PVU0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_io_pvu0_edc_ctrl_busecc_pend
11	IO_PVU0_TLB_BANK_RAMCC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for io_pvu0_tlb_bank_ramcc_pend
10	NAVSS512L_VIRTSS_PA_T4_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat4_edc_ctrl_busecc_pend
9	PAT4_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat4_table_amecc_pend
8	NAVSS512L_VIRTSS_PA_T3_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat3_edc_ctrl_busecc_pend
7	PAT3_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat3_table_amecc_pend
6	NAVSS512L_VIRTSS_PA_T2_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat2_edc_ctrl_busecc_pend
5	PAT2_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat2_table_amecc_pend
4	NAVSS512L_VIRTSS_PA_T1_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat1_edc_ctrl_busecc_pend

Table 5-335. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PAT1_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat1_table_ramecc_pend
2	NAVSS512L_VIRTSS_PAT0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_pat0_edc_ctrl_busecc_pend
1	PAT0_TABLE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for pat0_table_ramecc_pend
0	ECCAGG_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for eccagg_pend

Table 5-336. Register Call Summary for ECC_DED_ENABLE_CLR_REG0

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_CLR_REG0 Register \(Offset = 310021C0h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.28 ECC_DED_ENABLE_CLR_REG1 Register (Offset = 1C4h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG1 is shown in Figure 5-167 and described in Table 5-337.

Return to [Summary Table](#).

Interrupt Enable Clear Register 1

Figure 5-167. ECC_DED_ENABLE_CLR_REG1 Register

31	30	29	28	27	26	25	24
NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS512L_VIRTSS_DATA_C BASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	SMMU_BUFFER2_WFIFO_RA_MECC_ENABLE_CLR	SMMU_BUFFER2_CFIFO_RA_MECC_ENABLE_CLR	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	SMMU_BUFFER1_WFIFO_RA_MECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
SMMU_BUFFER1_CFIFO_RA_MECC_ENABLE_CLR	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	SMMU_BUFFER0_WFIFO_RA_MECC_ENABLE_CLR	SMMU_BUFFER0_CFIFO_RA_MECC_ENABLE_CLR	TCU_AXI2M_WBUSECC_ENABLE_CLR	TCU_AXI2M_RBUSECC_ENABLE_CLR	TCU_WCB_TA_G3_RAMECC_ENABLE_CLR	TCU_WCB_TA_G2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
TCU_WCB_TA_G1_RAMECC_ENABLE_CLR	TCU_WCB_TA_G0_RAMECC_ENABLE_CLR	TCU_CCB_TA_G3_RAMECC_ENABLE_CLR	TCU_CCB_TA_G2_RAMECC_ENABLE_CLR	TCU_CCB_TA_G1_RAMECC_ENABLE_CLR	TCU_CCB_TA_G0_RAMECC_ENABLE_CLR	TCU_WCB_ENT_RAMECC_ENABLE_CLR	TCU_CCB_ENT_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-337. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_C BASS_DMA_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_navss512l_virtss_data_cbass_dma_mst2_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-337. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_navss512l_virtss_data_cbass_dma_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
29	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_navss512l_virtss_data_cbass_dma_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
28	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_navss512l_virtss_data_cbass_mod_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
27	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_navss512l_virtss_data_cbass_mod_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
26	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_navss512l_virtss_data_cbass_mod_mst1_m2m_bridge_src_edc_ctrl_busecc_pending
25	NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_navss512l_virtss_data_cbass_mod_mst0_m2m_bridge_src_edc_ctrl_busecc_pending
24	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_navss512l_virtss_data_cbass_ac_mst3_m2m_bridge_src_edc_ctrl_busecc_pending
23	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_navss512l_virtss_data_cbass_ac_mst2_m2m_bridge_src_edc_ctrl_busecc_pending
22	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_navss512l_virtss_data_cbass_ac_mst1_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-337. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_navss512l_virtss_data_cbass_ac_mst0_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_SMMU_BUFFER2_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_smmu_buffer2_src_edc_ctrl_busecc_pend
19	SMMU_BUFFER2_WFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer2_wfifo_ramecc_pend
18	SMMU_BUFFER2_CFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer2_cfifo_ramecc_pend
17	NAVSS512L_VIRTSS_SMMU_BUFFER1_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_smmu_buffer1_src_edc_ctrl_busecc_pend
16	SMMU_BUFFER1_WFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer1_wfifo_ramecc_pend
15	SMMU_BUFFER1_CFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer1_cfifo_ramecc_pend
14	NAVSS512L_VIRTSS_SMMU_BUFFER0_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_smmu_buffer0_src_edc_ctrl_busecc_pend
13	SMMU_BUFFER0_WFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer0_wfifo_ramecc_pend
12	SMMU_BUFFER0_CFIFO_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for smmu_buffer0_cfifo_ramecc_pend
11	TCU_AXI2M_W_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_axi2m_w_busecc_pend
10	TCU_AXI2M_R_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_axi2m_r_busecc_pend
9	TCU_WCB_TAG3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag3_ramecc_pend
8	TCU_WCB_TAG2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag2_ramecc_pend
7	TCU_WCB_TAG1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag1_ramecc_pend
6	TCU_WCB_TAG0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_tag0_ramecc_pend
5	TCU_CCB_TAG3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag3_ramecc_pend
4	TCU_CCB_TAG2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag2_ramecc_pend
3	TCU_CCB_TAG1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag1_ramecc_pend
2	TCU_CCB_TAG0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_tag0_ramecc_pend

Table 5-337. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	TCU_WCB_ENT_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_wcb_ent_ramecc_pend
0	TCU_CCB_ENT_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for tcu_ccb_ent_ramecc_pend

Table 5-338. Register Call Summary for ECC_DED_ENABLE_CLR_REG1

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_CLR_REG1 Register \(Offset = 310021C4h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.29 ECC_DED_ENABLE_CLR_REG2 Register (Offset = 1C8h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG2 is shown in [Figure 5-168](#) and described in [Table 5-339](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 2

Figure 5-168. ECC_DED_ENABLE_CLR_REG2 Register

31	30	29	28	27	26	25	24
NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_1_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_SCR_S CR_NAVSS512 L_VIRTSS_DAT A_CBASS_SC R_SCR_EDC CTRL_BUSECC C_0_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_ECCAG GR_CFG_P2P BRIDGE_ECCA GGR_CFG_BRI DGE_BUSECC _ENABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER2_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER1_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ NAVSS512L_VI RTSS_DATA_C BASS_SMMU BUFFER0_IN_ M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_SRC_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 0_SRC_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU0_SRC M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT4_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 4_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT3_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 3_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT2_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 2_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT1_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 1_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_PAT0_S RC_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_PAT 0_SRC_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 3_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV3_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 2_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV2_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 1_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV1_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_NB_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_NB_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_DMA_SL V0_M2M_BRID GE_NAVSS512 L_VIRTSS_DAT A_CBASS_DM A_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_BU SECC_ENABL E_CLR	NAVSS512L_VI RTSS_DATA_C BASS_MOD_S LV0_M2M_BRI DGE_NAVSS51 2L_VIRTSS_DA TA_CBASS_M OD_SLV0_M2M_ BRIDGE_SRC_ EDC_CTRL_B USECC_ENAB LE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_AC_SLV 0_M2M_BRIDG E_NAVSS512L _VIRTSS_DATA _CBASS_AC_S LV0_M2M_BRI DGE_SRC_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS512L_VI RTSS_DATA_C BASS_VIRTSS _CFG_P2P_BR IDGE_VIRTSS_ CFG_BRIDGE_ BUSECC_ENA BLE_CLR	NAVSS512L_VI RTSS_DATA_C BASS_DMA_P VU1_DST_M2 M_BRIDGE_NA VSS512L_VIRT SS_DATA_CBA SS_DMA_PVU 1_DST_M2M_B RIDGE_SRC_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS512L_VI RTSS_DATA_C BASS_IO_PVU 1_DST_M2M_B RIDGE_NAVSS 512L_VIRTSS_ DATA_CBASS_ IO_PVU1_DST M2M_BRIDGE_ SRC_EDC_CT RL_BUSECC_E NABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0

Figure 5-168. ECC_DED_ENABLE_CLR_REG2 Register (continued)

NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-339. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_1_pend
30	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_0_pend
29	NAVSS512L_VIRTSS_DATA_CBASS_ECCAGGR_CFG_P2P_BRIDGE_ECCAGGR_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_eccaggr_cfg_p2p_bridge_eccaggr_cfg_bridge_busecc_pend
28	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER2_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer2_in_m2m_bridge_src_edc_ctrl_busecc_pend
27	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER1_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer1_in_m2m_bridge_src_edc_ctrl_busecc_pend
26	NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_SMMU_BUFFER0_IN_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_navss512l_virtss_data_cbass_smmu_buffer0_in_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-339. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
24	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_src_m2m_bridge_src_edc_ctrl_busecc_pend
23	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_src_m2m_bridge_src_edc_ctrl_busecc_pend
22	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat4_src_m2m_bridge_navss512l_virtss_data_cbass_pat4_src_m2m_bridge_src_edc_ctrl_busecc_pend
21	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat3_src_m2m_bridge_navss512l_virtss_data_cbass_pat3_src_m2m_bridge_src_edc_ctrl_busecc_pend
20	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat2_src_m2m_bridge_navss512l_virtss_data_cbass_pat2_src_m2m_bridge_src_edc_ctrl_busecc_pend
19	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat1_src_m2m_bridge_navss512l_virtss_data_cbass_pat1_src_m2m_bridge_src_edc_ctrl_busecc_pend
18	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_SRC_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat0_src_m2m_bridge_navss512l_virtss_data_cbass_pat0_src_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-339. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_navss512l_virtss_data_cbass_nb_slv3_m2m_bridge_src_edc_ctrl_busecc_pend
16	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV2_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_navss512l_virtss_data_cbass_nb_slv2_m2m_bridge_src_edc_ctrl_busecc_pend
15	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV1_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_navss512l_virtss_data_cbass_nb_slv1_m2m_bridge_src_edc_ctrl_busecc_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_navss512l_virtss_data_cbass_nb_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_navss512l_virtss_data_cbass_dma_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
12	NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_MOD_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_navss512l_virtss_data_cbass_mod_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_AC_SLV0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_navss512l_virtss_data_cbass_ac_slv0_m2m_bridge_src_edc_ctrl_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_VIRTSS_CFG_P2P_BRIDGE_VIRTSS_CFG_BRIDGE_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_virtss_cfg_p2p_bridge_virtss_cfg_bridge_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_dma_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-339. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_IO_PVU0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_navss512l_virtss_data_cbass_io_pvu0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT4_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_navss512l_virtss_data_cbass_pat4_dst_m2m_bridge_src_edc_ctrl_busecc_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT3_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_navss512l_virtss_data_cbass_pat3_dst_m2m_bridge_src_edc_ctrl_busecc_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT2_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_navss512l_virtss_data_cbass_pat2_dst_m2m_bridge_src_edc_ctrl_busecc_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT1_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_navss512l_virtss_data_cbass_pat1_dst_m2m_bridge_src_edc_ctrl_busecc_pend
2	NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_PAT0_DST_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_navss512l_virtss_data_cbass_pat0_dst_m2m_bridge_src_edc_ctrl_busecc_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_NB_MST0_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_navss512l_virtss_data_cbass_nb_mst0_m2m_bridge_src_edc_ctrl_busecc_pend

Table 5-339. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_NAVSS512L_VIRTSS_DATA_CBASS_DMA_MST3_M2M_BRIDGE_SRC_EDC_CTRL_BUSECC_PENDING	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_navss512l_virtss_data_cbass_dma_mst3_m2m_bridge_src_edc_ctrl_busecc_pending

Table 5-340. Register Call Summary for ECC_DED_ENABLE_CLR_REG2

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_CLR_REG2 Register \(Offset = 310021C8h\) \[reset = 0h\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.30 ECC_DED_ENABLE_CLR_REG3 Register (Offset = 1CCh) [reset = X]

ECC_DED_ENABLE_CLR_REG3 is shown in Figure 5-169 and described in Table 5-341.

Return to [Summary Table](#).

Interrupt Enable Clear Register 3

Figure 5-169. ECC_DED_ENABLE_CLR_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
NAVSS512L_VIRTSS_DATA_C BASS_GCLK_EDC_CTRL_CBA SS_INT_GBUSECC_1_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_GCLK_EDC_CTRL_CBA SS_INT_GBUSECC_0_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DS_T_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SR_C_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_CR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_CR_EDC_CTRL_BUSECC_1_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_CFG_SCR_CR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_CR_EDC_CTRL_BUSECC_0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_9_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_8_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_7_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_6_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_5_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_4_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_3_ENABLE_CLR	NAVSS512L_VIRTSS_DATA_C BASS_SCR_S_CR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_S_CR_SCR_EDC_CTRL_BUSECC_2_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-341. ECC_DED_ENABLE_CLR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_1_pend
14	NAVSS512L_VIRTSS_DATA_CBASS_GCLK_EDC_CTRL_CBASS_INT_GBUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_gclk_edc_ctrl_cbass_int_gbusecc_0_pend
13	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_INT_DMSC_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cbass_int_dmsc_scr_navss512l_virtss_data_cbass_cbass_int_dmsc_scr_edc_ctrl_busecc_pend

Table 5-341. ECC_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_dst_busecc_pend
11	NAVSS512L_VIRTSS_DATA_CBASS_DMSC_SLV_P2P_BRIDGE_DMSC_SLV_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_dmsc_slv_p2p_bridge_dmsc_slv_bridge_src_busecc_pend
10	NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_NAVSS512L_VIRTSS_DATA_CBASS_CBASS_DEFAULT_MMRS_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cbass_default_mmrs_navss512l_virtss_data_cbass_cbass_default_mmrs_edc_ctrl_busecc_pend
9	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_1_pend
8	NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_cfg_scr_scr_navss512l_virtss_data_cbass_cfg_scr_scr_edc_ctrl_busecc_0_pend
7	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_9_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_9_pend
6	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_8_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_8_pend
5	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_7_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_7_pend
4	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_6_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_6_pend
3	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_EDC_CTRL_BUSECC_5_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass_scr_scr_edc_ctrl_busecc_5_pend

Table 5-341. ECC_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_4_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_4_pend
1	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_3_pend
0	NAVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_N AVSS512L_VIRTSS_DATA_CBASS_SCR_SCR_ED C_CTRL_BUSECC_2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss512l_virtss_data_cbass_scr_scr_navss512l_virtss_data_cbass _scr_scr_edc_ctrl_busecc_2_pend

Table 5-342. Register Call Summary for ECC_DED_ENABLE_CLR_REG3

VIRTSS_ECCAGGR_CFG Registers

- [ECC_DED_ENABLE_CLR_REG3 Register \(Offset = 310021CCh\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.31 ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

ECC_AGGR_ENABLE_SET is shown in [Figure 5-170](#) and described in [Table 5-343](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Figure 5-170. ECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 5-343. ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

Table 5-344. Register Call Summary for ECC_AGGR_ENABLE_SET

VIRTSS_ECCAGGR_CFG Registers

- [ECC_AGGR_ENABLE_SET Register \(Offset = 31002200h\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.32 ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

ECC_AGGR_ENABLE_CLR is shown in [Figure 5-171](#) and described in [Table 5-345](#).

[Return to Summary Table.](#)

AGGR interrupt enable clear Register

Figure 5-171. ECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 5-345. ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

Table 5-346. Register Call Summary for ECC_AGGR_ENABLE_CLR

VIRTSS_ECCAGGR_CFG Registers

- [ECC_AGGR_ENABLE_CLR Register \(Offset = 31002204h\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.33 ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

ECC_AGGR_STATUS_SET is shown in [Figure 5-172](#) and described in [Table 5-347](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Figure 5-172. ECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 5-347. ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

Table 5-348. Register Call Summary for ECC_AGGR_STATUS_SET

VIRTSS_ECCAGGR_CFG Registers

- [ECC_AGGR_STATUS_SET Register \(Offset = 31002208h\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

5.2.34 ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

ECC_AGGR_STATUS_CLR is shown in [Figure 5-173](#) and described in [Table 5-349](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Figure 5-173. ECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 5-349. ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

Table 5-350. Register Call Summary for ECC_AGGR_STATUS_CLR

VIRTSS_ECCAGGR_CFG Registers

- [ECC_AGGR_STATUS_CLR Register \(Offset = 3100220Ch\) \[reset = X\]: \[0\]](#)
- [virtss_eccaggr_cfg_regs Registers: \[0\]](#)

6 PVU Registers

6.1 NAVSS_PVU_CFG Registers

Table 6-1 lists the memory-mapped registers for the NAVSS_PVU_CFG. All register offset addresses not listed in Table 6-1 should be considered as reserved locations and the register contents should not be modified.

KS3 DMA Virtual Address Translation Config Region

Table 6-1. NAVSS_PVU_CFG Instances

Instance	Base Address
NAVSS0_IO_PVU0_CFG	30F8 0000h
NAVSS0_IO_PVU1_CFG	30F8 1000h
NAVSS0_DMA_PVU1_CFG	30F8 3000h

Table 6-2. NAVSS_PVU_CFG Registers

Offset	Acronym	Register Name	NAVSS0_IO_PVU0_CFG Physical Address	NAVSS0_IO_PVU1_CFG Physical Address	NAVSS0_D MA_PVU1_ CFG Physical Address
0h	PVU_PID	Revision Register	30F8 0000h	30F8 1000h	30F8 3000h
4h	PVU_CONFIG	Config Register	30F8 0004h	30F8 1004h	30F8 3004h
10h	PVU_ENABLE	Enable Register	30F8 0010h	30F8 1010h	30F8 3010h
14h	PVU_VIRTID_MAP1	Map Register 1	30F8 0014h	30F8 1014h	30F8 3014h
18h	PVU_VIRTID_MAP2	Map Register 2	30F8 0018h	30F8 1018h	30F8 3018h
30h	PVU_EXCEPTION_LOGGING_DISABLE	Exception Logging Disable Register	30F8 0030h	30F8 1030h	30F8 3030h
104h	PVU_DESTINATION_ID	Destination ID Register	30F8 0104h	30F8 1104h	30F8 3104h
120h	PVU_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	30F8 0120h	30F8 1120h	30F8 3120h
124h	PVU_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	30F8 0124h	30F8 1124h	30F8 3124h
128h	PVU_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	30F8 0128h	30F8 1128h	30F8 3128h
12Ch	PVU_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	30F8 012Ch	30F8 112Ch	30F8 312Ch
130h	PVU_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	30F8 0130h	30F8 1130h	30F8 3130h
134h	PVU_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	30F8 0134h	30F8 1134h	30F8 3134h
138h	PVU_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	30F8 0138h	30F8 1138h	30F8 3138h
140h	PVU_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	30F8 0140h	30F8 1140h	30F8 3140h
144h	PVU_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	30F8 0144h	30F8 1144h	30F8 3144h
148h	PVU_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	30F8 0148h	30F8 1148h	30F8 3148h
14Ch	PVU_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	30F8 014Ch	30F8 114Ch	30F8 314Ch
150h	PVU_EOI_REG	EOI Register	30F8 0150h	30F8 1150h	30F8 3150h

6.1.1 PVU_PID Register (Offset = 0h) [reset = 668849C00h]

PVU_PID is shown in [Figure 6-1](#) and described in [Table 6-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 6-3. PVU_PID Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0000h
NAVSS0_IO_PVU1_CFG	30F8 1000h
NAVSS0_DMA_PVU1_CFG	30F8 3000h

Figure 6-1. PVU_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-2h		R-688h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-9h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 6-4. PVU_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	688h	Module ID
15-11	RTL	R	9h	RTL revision. Ch in this device.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

6.1.2 PVU_CONFIG Register (Offset = 4h) [reset = X]

PVU_CONFIG is shown in [Figure 6-2](#) and described in [Table 6-6](#).

Return to [Summary Table](#).

The Config Register contains the configuration values for the module.

Table 6-5. PVU_CONFIG Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0004h
NAVSS0_IO_PVU1_CFG	30F8 1004h
NAVSS0_DMA_PVU1_CFG	30F8 3004h

Figure 6-2. PVU_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								TLB_ENTRIES							
R-X								R-8h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TLBS															
R-100h															

LEGEND: R = Read Only; -n = value after reset

Table 6-6. PVU_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	TLB_ENTRIES	R	8h	Number of TLB entries per channel
15-0	TLBS	R	100h	Number of TLBs 40h in this device

6.1.3 PVU_ENABLE Register (Offset = 10h) [reset = X]

PVU_ENABLE is shown in [Figure 6-3](#) and described in [Table 6-8](#).

Return to [Summary Table](#).

The Enable Register enables the PVU.

Table 6-7. PVU_ENABLE Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0010h
NAVSS0_IO_PVU1_CFG	30F8 1010h
NAVSS0_DMA_PVU1_CFG	30F8 3010h

Figure 6-3. PVU_ENABLE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															EN
R/W-X															R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-8. PVU_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EN	R/W	0h	PVU Enable bit. 0 = PVU disabled 1 = PVU enabled

6.1.4 PVU_VIRTID_MAP1 Register (Offset = 14h) [reset = X]

PVU_VIRTID_MAP1 is shown in [Figure 6-4](#) and described in [Table 6-10](#).

Return to [Summary Table](#).

The Map Register 1 defines the virtid mapping for the PVU.

Table 6-9. PVU_VIRTID_MAP1 Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0014h
NAVSS0_IO_PVU1_CFG	30F8 1014h
NAVSS0_DMA_PVU1_CFG	30F8 3014h

Figure 6-4. PVU_VIRTID_MAP1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
DMA_CL3		DMA_CL2		DMA_CL1		DMA_CL0	
R/W-3h		R/W-2h		R/W-1h		R/W-0h	
15	14	13	12	11	10	9	8
RESERVED				DMA_CNT			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
DMA_CNT							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-10. PVU_VIRTID_MAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-22	DMA_CL3	R/W	3h	Map for DMA sub-class 3. Value is the final sub-class and selects TLB+n.
21-20	DMA_CL2	R/W	2h	Map for DMA sub-class 2. Value is the final sub-class and selects TLB+n.
19-18	DMA_CL1	R/W	1h	Map for DMA sub-class 1. Value is the final sub-class and selects TLB+n.
17-16	DMA_CL0	R/W	0h	Map for DMA sub-class 0. Value is the final sub-class and selects TLB+n.
15-12	RESERVED	R/W	X	
11-0	DMA_CNT	R/W	0h	VirtID count for DMA class that use sub-classes.

6.1.5 PVU_VIRTID_MAP2 Register (Offset = 18h) [reset = X]

PVU_VIRTID_MAP2 is shown in [Figure 6-5](#) and described in [Table 6-12](#).

Return to [Summary Table](#).

The Map Register 2 defines the virtid mapping for the PVU.

Table 6-11. PVU_VIRTID_MAP2 Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0018h
NAVSS0_IO_PVU1_CFG	30F8 1018h
NAVSS0_DMA_PVU1_CFG	30F8 3018h

Figure 6-5. PVU_VIRTID_MAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					MAX_CNT																
R/W-X																					R/W-0h																

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-12. PVU_VIRTID_MAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	MAX_CNT	R/W	0h	VirtID maximum for PVU.

6.1.6 PVU_EXCEPTION_LOGGING_DISABLE Register (Offset = 30h) [reset = X]

PVU_EXCEPTION_LOGGING_DISABLE is shown in [Figure 6-6](#) and described in [Table 6-14](#).

Return to [Summary Table](#).

The Exception Logging Disable Register defines which types of faults are disabled for logging.

Table 6-13. PVU_EXCEPTION_LOGGING_DISABLE Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0030h
NAVSS0_IO_PVU1_CFG	30F8 1030h
NAVSS0_DMA_PVU1_CFG	30F8 3030h

Figure 6-6. PVU_EXCEPTION_LOGGING_DISABLE Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	MISS_DIS	PREF_DIS	EXEC_DIS	WRITE_DIS	READ_DIS	RESERVED	VIRTID_DIS
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-14. PVU_EXCEPTION_LOGGING_DISABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	RESERVED	R/W	X	
6	MISS_DIS	R/W	0h	Disable for PVU miss fault logging. 0 = enable miss fault logging. 1 = disable miss fault logging.
5	PREF_DIS	R/W	0h	Disable for prefetch permissions fault logging. 0 = enable prefetch fault logging. 1 = disable prefetch fault logging.
4	EXEC_DIS	R/W	0h	Disable for execute permissions fault logging. 0 = enable execute fault logging. 1 = disable execute fault logging.
3	WRITE_DIS	R/W	0h	Disable for write permissions fault logging. 0 = enable write fault logging. 1 = disable write fault logging.
2	READ_DIS	R/W	0h	Disable for read permissions fault logging. 0 = enable read fault logging. 1 = disable read fault logging.
1	RESERVED	R/W	X	
0	VIRTID_DIS	R/W	0h	Disable for virtID permission fault logging. 0 = enable virtID fault logging. 1 = disable virtID fault logging.

6.1.7 PVU_DESTINATION_ID Register (Offset = 104h) [reset = X]

PVU_DESTINATION_ID is shown in [Figure 6-7](#) and described in [Table 6-16](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

Table 6-15. PVU_DESTINATION_ID Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0104h
NAVSS0_IO_PVU1_CFG	30F8 1104h
NAVSS0_DMA_PVU1_CFG	30F8 3104h

Figure 6-7. PVU_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEST_ID							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-16. PVU_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

6.1.8 PVU_EXCEPTION_LOGGING_CONTROL Register (Offset = 120h) [reset = X]

PVU_EXCEPTION_LOGGING_CONTROL is shown in [Figure 6-8](#) and described in [Table 6-18](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

Table 6-17. PVU_EXCEPTION_LOGGING_CONTROL Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0120h
NAVSS0_IO_PVU1_CFG	30F8 1120h
NAVSS0_DMA_PVU1_CFG	30F8 3120h

Figure 6-8. PVU_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-18. PVU_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set. This will not disable logging, so if cleared the current log should also be cleared to guarantee the next log generates the interrupt.
0	DISABLE_F	R/W	0h	Disables logging when set. This will also disable interrupts.

6.1.9 PVU_EXCEPTION_LOGGING_HEADER0 Register (Offset = 124h) [reset = 0h]

PVU_EXCEPTION_LOGGING_HEADER0 is shown in [Figure 6-9](#) and described in [Table 6-20](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Table 6-19. PVU_EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0124h
NAVSS0_IO_PVU1_CFG	30F8 1124h
NAVSS0_DMA_PVU1_CFG	30F8 3124h

Figure 6-9. PVU_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID								DEST_ID															
R-0h								R-0h								R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 6-20. PVU_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 6 = PVU.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

6.1.10 PVU_EXCEPTION_LOGGING_HEADER1 Register (Offset = 128h) [reset = X]

PVU_EXCEPTION_LOGGING_HEADER1 is shown in [Figure 6-10](#) and described in [Table 6-22](#).

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

Table 6-21. PVU_EXCEPTION_LOGGING_HEADER1 Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0128h
NAVSS0_IO_PVU1_CFG	30F8 1128h
NAVSS0_DMA_PVU1_CFG	30F8 3128h

Figure 6-10. PVU_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; -n = value after reset

Table 6-22. PVU_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 0 = PVU miss. 1 = Max virtid violation. 2 = reserved. 3 = read permission violation. 4 = write permission violation. 5 = execute permission violation. 6 = prefetch permission violation.
15-0	RESERVED	R	X	

6.1.11 PVU_EXCEPTION_LOGGING_DATA0 Register (Offset = 12Ch) [reset = 0h]

PVU_EXCEPTION_LOGGING_DATA0 is shown in [Figure 6-11](#) and described in [Table 6-24](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

**Table 6-23. PVU_EXCEPTION_LOGGING_DATA0
Instances**

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 012Ch
NAVSS0_IO_PVU1_CFG	30F8 112Ch
NAVSS0_DMA_PVU1_CFG	30F8 312Ch

Figure 6-11. PVU_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 6-24. PVU_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Input virtual address lower 32 bits.

6.1.12 PVU_EXCEPTION_LOGGING_DATA1 Register (Offset = 130h) [reset = X]

PVU_EXCEPTION_LOGGING_DATA1 is shown in [Figure 6-12](#) and described in [Table 6-26](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

Table 6-25. PVU_EXCEPTION_LOGGING_DATA1 Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0130h
NAVSS0_IO_PVU1_CFG	30F8 1130h
NAVSS0_DMA_PVU1_CFG	30F8 3130h

Figure 6-12. PVU_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 6-26. PVU_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Input virtual address upper 12 bits.

6.1.13 PVU_EXCEPTION_LOGGING_DATA2 Register (Offset = 134h) [reset = X]

PVU_EXCEPTION_LOGGING_DATA2 is shown in [Figure 6-13](#) and described in [Table 6-28](#).

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

**Table 6-27. PVU_EXCEPTION_LOGGING_DATA2
Instances**

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0134h
NAVSS0_IO_PVU1_CFG	30F8 1134h
NAVSS0_DMA_PVU1_CFG	30F8 3134h

Figure 6-13. PVU_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 6-28. PVU_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

6.1.14 PVU_EXCEPTION_LOGGING_DATA3 Register (Offset = 138h) [reset = X]

PVU_EXCEPTION_LOGGING_DATA3 is shown in [Figure 6-14](#) and described in [Table 6-30](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the third word of the data. Reading this register will clear the error pending bit except when emudbg is set.

Table 6-29. PVU_EXCEPTION_LOGGING_DATA3 Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0138h
NAVSS0_IO_PVU1_CFG	30F8 1138h
NAVSS0_DMA_PVU1_CFG	30F8 3138h

Figure 6-14. PVU_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						BYTECNT															
R-X																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 6-30. PVU_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

6.1.15 PVU_EXCEPTION_PEND_SET Register (Offset = 140h) [reset = X]

PVU_EXCEPTION_PEND_SET is shown in [Figure 6-15](#) and described in [Table 6-32](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Table 6-31. PVU_EXCEPTION_PEND_SET Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0140h
NAVSS0_IO_PVU1_CFG	30F8 1140h
NAVSS0_DMA_PVU1_CFG	30F8 3140h

Figure 6-15. PVU_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 6-32. PVU_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

6.1.16 PVU_EXCEPTION_PEND_CLEAR Register (Offset = 144h) [reset = X]

PVU_EXCEPTION_PEND_CLEAR is shown in [Figure 6-16](#) and described in [Table 6-34](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Table 6-33. PVU_EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0144h
NAVSS0_IO_PVU1_CFG	30F8 1144h
NAVSS0_DMA_PVU1_CFG	30F8 3144h

Figure 6-16. PVU_EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 6-34. PVU_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

6.1.17 PVU_EXCEPTION_ENABLE_SET Register (Offset = 148h) [reset = X]

PVU_EXCEPTION_ENABLE_SET is shown in [Figure 6-17](#) and described in [Table 6-36](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

**Table 6-35. PVU_EXCEPTION_ENABLE_SET
Instances**

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0148h
NAVSS0_IO_PVU1_CFG	30F8 1148h
NAVSS0_DMA_PVU1_CFG	30F8 3148h

Figure 6-17. PVU_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 6-36. PVU_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

6.1.18 PVU_EXCEPTION_ENABLE_CLEAR Register (Offset = 14Ch) [reset = X]

PVU_EXCEPTION_ENABLE_CLEAR is shown in [Figure 6-18](#) and described in [Table 6-38](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Table 6-37. PVU_EXCEPTION_ENABLE_CLEAR Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 014Ch
NAVSS0_IO_PVU1_CFG	30F8 114Ch
NAVSS0_DMA_PVU1_CFG	30F8 314Ch

Figure 6-18. PVU_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 6-38. PVU_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

6.1.19 PVU_EOI_REG Register (Offset = 150h) [reset = X]

PVU_EOI_REG is shown in [Figure 6-19](#) and described in [Table 6-40](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 6-39. PVU_EOI_REG Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG	30F8 0150h
NAVSS0_IO_PVU1_CFG	30F8 1150h
NAVSS0_DMA_PVU1_CFG	30F8 3150h

Figure 6-19. PVU_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EOI_WR															
R-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-40. PVU_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	EOI_WR	R/W	0h	EOI Register

6.2 NAVSS0_PVU_CFG_TLBIF Registers

Table 6-41 lists the memory-mapped registers for the NAVSS0_PVU_CFG_TLBIF. All register offset addresses not listed in Table 6-41 should be considered as reserved locations and the register contents should not be modified.

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Table 6-41. NAVSS0_PVU_CFG_TLBIF Instances

Instance	Base Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0000h
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0000h
NAVSS0_DMA_PVU0_CFG_TLBIF	3604 0000h
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0000h

Table 6-42. NAVSS0_PVU_CFG_TLBIF Registers

Offset	Acronym	Register Name	NAVSS0_IO_PVU0_CFG_TLBIF Physical Address	NAVSS0_IO_PVU1_CFG_TLBIF Physical Address	NAVSS0_DMA_PVU1_CFG_TLBIF Physical Address
0h + formula	PVU_CHAIN_j	TLB Chain Register	3600 0000h + formula	3604 0000h + formula	360C 0000h + formula
20h + formula	PVU_ENTRY0_j_k	TLB Entry Register	3600 0020h + formula	3604 0020h + formula	360C 0020h + formula
24h + formula	PVU_ENTRY1_j_k	TLB Entry Register	3600 0024h + formula	3604 0024h + formula	360C 0024h + formula
28h + formula	PVU_ENTRY2_j_k	TLB Entry Register	3600 0028h + formula	3604 0028h + formula	360C 0028h + formula
30h + formula	PVU_ENTRY4_j_k	TLB Entry Register	3600 0030h + formula	3604 0030h + formula	360C 0030h + formula
34h + formula	PVU_ENTRY5_j_k	TLB Entry Register	3600 0034h + formula	3604 0034h + formula	360C 0034h + formula
38h + formula	PVU_ENTRY6_j_k	TLB Entry Register	3600 0038h + formula	3604 0038h + formula	360C 0038h + formula

6.2.1 PVU_CHAIN_j Register (Offset = 0h + formula) [reset = X]

PVU_CHAIN_j is shown in [Figure 6-20](#) and described in [Table 6-44](#).

Return to [Summary Table](#).

The TLB chain points to another TLB. The j is the TLB number.

Offset = 0h + (j * 1000h); where j = 0h to 3Fh

Table 6-43. PVU_CHAIN_j Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0000h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0000h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0000h + formula

Figure 6-20. PVU_CHAIN_j Register

31	30	29	28	27	26	25	24
EN	LOG_DIS	FAULT	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-X				
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				CHAIN			
R/W-X				R/W-0h			
7	6	5	4	3	2	1	0
CHAIN							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-44. PVU_CHAIN_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the TLB. 0 = disable TLB. 1 = enable TLB.
30	LOG_DIS	R/W	0h	Disable Fault Logging for the TLB. 0 = enable fault logging. 1 = disable fault logging.
29	FAULT	R/W	0h	A fault has been detected from this TLB that could not be logged. Will be set by hardware, and can be cleared by software.
28-12	RESERVED	R/W	X	
11-0	CHAIN	R/W	0h	Chain to another TLB. 0 = no chain. >0 = chain to that TLB number.

6.2.2 PVU_ENTRY0_j_k Register (Offset = 20h + formula) [reset = 0h]

PVU_ENTRY0_j_k is shown in [Figure 6-21](#) and described in [Table 6-46](#).

Return to [Summary Table](#).

The TLB Entry. The j is the TLB number, and the k is the entry number within a TLB. The address must be aligned to the page size.

Offset = 20h + (j * 1000h) + (k * 20h); where j = 0h to 3Fh, k = 0h to 7h

Table 6-45. PVU_ENTRY0_j_k Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0020h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0020h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0020h + formula

Figure 6-21. PVU_ENTRY0_j_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VBASE_L																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-46. PVU_ENTRY0_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VBASE_L	R/W	0h	Virtual Base Address bits 31 to 0. The address must be aligned to the page size.

6.2.3 PVU_ENTRY1_j_k Register (Offset = 24h + formula) [reset = X]

PVU_ENTRY1_j_k is shown in [Figure 6-22](#) and described in [Table 6-48](#).

Return to [Summary Table](#).

The TLB Entry. The j is the TLB number, and the k is the entry number within a TLB. The address must be aligned to the page size.

Offset = 24h + (j * 1000h) + (k * 20h); where j = 0h to 3Fh, k = 0h to 7h

Table 6-47. PVU_ENTRY1_j_k Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0024h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0024h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0024h + formula

Figure 6-22. PVU_ENTRY1_j_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VBASE_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-48. PVU_ENTRY1_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	VBASE_H	R/W	0h	Virtual Base Address bits 47 to 32. The address must be aligned to the page size.

6.2.4 PVU_ENTRY2_j_k Register (Offset = 28h + formula) [reset = X]

PVU_ENTRY2_j_k is shown in [Figure 6-23](#) and described in [Table 6-50](#).

Return to [Summary Table](#).

The TLB Entry. The j is the TLB number, and the k is the entry number within a TLB.

Offset = 28h + (j * 1000h) + (k * 20h); where j = 0h to 3Fh, k = 0h to 7h

Table 6-49. PVU_ENTRY2_j_k Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0028h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0028h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0028h + formula

Figure 6-23. PVU_ENTRY2_j_k Register

31	30	29	28	27	26	25	24
MODE		SEC_DEM	RESERVED				
R/W-0h		R/W-0h	R/W-X				
23	22	21	20	19	18	17	16
RESERVED		PSECURE	RESERVED	PSIZE			
R/W-X		R/W-0h	R/W-X	R/W-0h			
15	14	13	12	11	10	9	8
PPERM						PMEMTYPE	
R/W-0h						R/W-0h	
7	6	5	4	3	2	1	0
RESERVED	PPREFETCH	PISABLE	POSABLE	PIALLOCPOL		POALLOCPOL	
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-50. PVU_ENTRY2_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	MODE	R/W	0h	Entry mode. 0 = invalid. 1 = reserved - do not use. 2 = valid. 3 = reserved - do not use.
29	SEC_DEM	R/W	0h	Enable Secure Transaction Demotion for the entry if the PVU is in secure mode. 0 = Secure Transactions are not affected. 1 = Secure Transactions that match the entry is demoted to non-secure out of the PVU.
28-22	RESERVED	R/W	X	
21	PSECURE	R/W	0h	LPAE Field for Secure Page
20	RESERVED	R/W	X	
19-16	PSIZE	R/W	0h	LPAE Field for Page Size. 0 = 4K. 1 = 16K. 2 = 64K. 3 = 2M. 4 = 32M. 5 = 512M. 6 = 1G. 7 = 16G.

Table 6-50. PVU_ENTRY2_j_k Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-10	PPERM	R/W	0h	LPAA Field for Page Permissions. Bit 0 = enable user read access UR. Bit 1 = enable user write access UW. Bit 2 = enable user execute access UX. Bit 3 = enable supervisor read access SR. Bit 4 = enable supervisor write access SW. Bit 5 = enable supervisor execute access SX.
9-8	PMENTYPE	R/W	0h	LPAA Field for Page Memory Type. 0 = device. 1 = write back. 2 = write through.
7	RESERVED	R/W	X	
6	PPREFETCH	R/W	0h	LPAA Field for Page Prefetch allowed
5	PISABLE	R/W	0h	LPAA Field for Page Inner Shareable allowed
4	POSABLE	R/W	0h	LPAA Field for Page Outer Shareable allowed
3-2	PIALLOCPOL	R/W	0h	LPAA Field for Page Inner Allocation Policy. 0 = no allocate. 1 = write allocate. 2 = read allocate. 3 = read and write allocate.
1-0	POALLOCPOL	R/W	0h	LPAA Field for Page Outer Allocation Policy. 0 = no allocate. 1 = write allocate. 2 = read allocate. 3 = read and write allocate.

6.2.5 PVU_ENTRY4_j_k Register (Offset = 30h + formula) [reset = 0h]

PVU_ENTRY4_j_k is shown in [Figure 6-24](#) and described in [Table 6-52](#).

Return to [Summary Table](#).

The TLB Entry. The j is the TLB number, and the k is the entry number within a TLB. The address must be aligned to the page size.

Offset = 30h + (j * 1000h) + (k * 20h); where j = 0h to 3Fh, k = 0h to 7h

Table 6-51. PVU_ENTRY4_j_k Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0030h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0030h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0030h + formula

Figure 6-24. PVU_ENTRY4_j_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PBASE_L																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-52. PVU_ENTRY4_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PBASE_L	R/W	0h	Physical Base Address bits 31 to 0. The address must be aligned to the page size.

6.2.6 PVU_ENTRY5_j_k Register (Offset = 34h + formula) [reset = X]

PVU_ENTRY5_j_k is shown in [Figure 6-25](#) and described in [Table 6-54](#).

Return to [Summary Table](#).

The TLB Entry. The j is the TLB number, and the k is the entry number within a TLB. The address must be aligned to the page size.

Offset = 34h + (j * 1000h) + (k * 20h); where j = 0h to 3Fh, k = 0h to 7h

Table 6-53. PVU_ENTRY5_j_k Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0034h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0034h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0034h + formula

Figure 6-25. PVU_ENTRY5_j_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PBASE_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-54. PVU_ENTRY5_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	PBASE_H	R/W	0h	Physical Base Address bits 47 to 32. The address must be aligned to the page size.

6.2.7 PVU_ENTRY6_j_k Register (Offset = 38h + formula) [reset = X]

PVU_ENTRY6_j_k is shown in [Figure 6-26](#) and described in [Table 6-56](#).

Return to [Summary Table](#).

The TLB Entry. The j is the TLB number, and the k is the entry number within a TLB.

Offset = 38h + (j * 1000h) + (k * 20h); where j = 0h to 3Fh, k = 0h to 7h

Table 6-55. PVU_ENTRY6_j_k Instances

Instance	Physical Address
NAVSS0_IO_PVU0_CFG_TLBIF	3600 0038h + formula
NAVSS0_IO_PVU1_CFG_TLBIF	3604 0038h + formula
NAVSS0_DMA_PVU1_CFG_TLBIF	360C 0038h + formula

Figure 6-26. PVU_ENTRY6_j_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			REPLACE	ORDERID			
R/W-X			R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-56. PVU_ENTRY6_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	X	
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value when matching this entry with the ORDERID field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the ORDERID field value for the destination transaction.
3-0	ORDERID	R/W	0h	Defines the bus orderid value for this entry if hit.

7 PAT Registers

7.1 PAT_CFG_MMRS Registers

Table 7-2 lists the memory-mapped registers for the pat0_cfg_mmrs registers. All register offset addresses not listed in Table 7-2 should be considered as reserved locations and the register contents should not be modified.

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Table 7-1. PAT_CFG_MMRS Instances

Instance	Base Address
PAT0_CFG_MMRS	31010000h
PAT1_CFG_MMRS	31011000h
PAT2_CFG_MMRS	31012000h
PAT3_CFG_MMRS	31013000h
PAT4_CFG_MMRS	31014000h

Table 7-2. PAT_CFG_MMRS Registers

Offset	Acronym	Register Name	PAT0_CFG_MMRS Physical Address	PAT1_CFG_MMRS Physical Address	PAT2_CFG_MMRS Physical Address
0h	PAT_PID	Revision Register	31010000h	31011000h	31012000h
4h	PAT_CONFIG	Config Register	31010004h	31011004h	31012004h
10h	PAT_CONTROL	Control Register	31010010h	31011010h	31012010h
84h	PAT_DESTINATION_ID	Destination ID Register	31010084h	31011084h	31012084h
A0h	PAT_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	310100A0h	310110A0h	310120A0h
A4h	PAT_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	310100A4h	310110A4h	310120A4h
A8h	PAT_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	310100A8h	310110A8h	310120A8h
ACH	PAT_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	310100ACH	310110ACH	310120ACH
B0h	PAT_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	310100B0h	310110B0h	310120B0h
B4h	PAT_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	310100B4h	310110B4h	310120B4h
B8h	PAT_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	310100B8h	310110B8h	310120B8h
C0h	PAT_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	310100C0h	310110C0h	310120C0h
C4h	PAT_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	310100C4h	310110C4h	310120C4h
C8h	PAT_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	310100C8h	310110C8h	310120C8h
CCh	PAT_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	310100CCh	310110CCh	310120CCh
D0h	PAT_EOI_REG	EOI Register	310100D0h	310110D0h	310120D0h

Table 7-3. PAT_CFG_MMRS Registers 2

Offset	Acronym	Register Name	PAT3_CFG_MMRS Physical Address	PAT4_CFG_MMRS Physical Address
0h	PAT_PID	Revision Register	31013000h	31014000h
4h	PAT_CONFIG	Config Register	31013004h	31014004h
10h	PAT_CONTROL	Control Register	31013010h	31014010h
84h	PAT_DESTINATION_ID	Destination ID Register	31013084h	31014084h
A0h	PAT_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	310130A0h	310140A0h

Table 7-3. PAT_CFG_MMRS Registers 2 (continued)

Offset	Acronym	Register Name	PAT3_CFG_MMRS Physical Address	PAT4_CFG_MMRS Physical Address
A4h	PAT_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	310130A4h	310140A4h
A8h	PAT_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	310130A8h	310140A8h
ACH	PAT_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	310130ACH	310140ACH
B0h	PAT_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	310130B0h	310140B0h
B4h	PAT_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	310130B4h	310140B4h
B8h	PAT_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	310130B8h	310140B8h
C0h	PAT_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register	310130C0h	310140C0h
C4h	PAT_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register	310130C4h	310140C4h
C8h	PAT_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register	310130C8h	310140C8h
CCh	PAT_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register	310130CCh	310140CCh
D0h	PAT_EOI_REG	EOI Register	310130D0h	310140D0h

7.1.1 PAT_PID Register (Offset = 0h) [reset = 66843100h]

PAT_PID is shown in [Figure 7-1](#) and described in [Table 7-5](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 7-4. PAT_PID Instances

Instance	Physical Address
PAT0_CFG_MMRS	31010000h
PAT1_CFG_MMRS	31011000h
PAT2_CFG_MMRS	31012000h
PAT3_CFG_MMRS	31013000h
PAT4_CFG_MMRS	31014000h

Figure 7-1. PAT_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-684h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-6h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 7-5. PAT_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	684h	Module ID
15-11	RTL	R	6h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

7.1.2 PAT_CONFIG Register (Offset = 4h) [reset = 4000h]

PAT_CONFIG is shown in [Figure 7-2](#) and described in [Table 7-7](#).

Return to [Summary Table](#).

The Config Register contains the configuration values for the module.

Table 7-6. PAT_CONFIG Instances

Instance	Physical Address
PAT0_CFG_MMRS	31010004h
PAT1_CFG_MMRS	31011004h
PAT2_CFG_MMRS	31012004h
PAT3_CFG_MMRS	31013004h
PAT4_CFG_MMRS	31014004h

Figure 7-2. PAT_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAGES																															
R-4000h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-7. PAT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PAGES	R	4000h	Number of pages 4000h: PAT0-2 800h: PAT3-4

7.1.3 PAT_CONTROL Register (Offset = 10h) [reset = X]

PAT_CONTROL is shown in [Figure 7-3](#) and described in [Table 7-9](#).

Return to [Summary Table](#).

The Control Register contains controls for the PAT.

Table 7-8. PAT_CONTROL Instances

Instance	Physical Address
PAT0_CFG_MMRS	31010010h
PAT1_CFG_MMRS	31011010h
PAT2_CFG_MMRS	31012010h
PAT3_CFG_MMRS	31013010h
PAT4_CFG_MMRS	31014010h

Figure 7-3. PAT_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
ARB_MODE		PAGE_SIZE		RESERVED		REPLACE_OR DERID_ENABL E	ENABLE
R/W-0h		R/W-0h		R/W-X		R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-9. PAT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	ARB_MODE	R/W	0h	Arbitration mode. 0 = updates first. 1 = reserved. 2 = round robin. 3 = reserved.
5-4	PAGE_SIZE	R/W	0h	Page Size. 0 = 4KB. 1 = 16KB. 2 = 64KB. 3 = 1MB.
3-2	RESERVED	R/W	X	
1	REPLACE_ORDERID_EN ABLE	R	0h	Globally enable the replace orderid feature allowing a hypervisor or OS to globally disable the feature if applications or VMs should not be able to modify orderid values. The page based enables are used if globally enabled and are always ignored if globally disabled. 0 = disabled. 1 = enabled

Table 7-9. PAT_CONTROL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ENABLE	R/W	0h	Enable bit. 0 = disabled. 1 = enabled

7.1.4 PAT_DESTINATION_ID Register (Offset = 84h) [reset = X]

PAT_DESTINATION_ID is shown in [Figure 7-4](#) and described in [Table 7-11](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

Table 7-10. PAT_DESTINATION_ID Instances

Instance	Physical Address
PAT0_CFG_MMRS	31010084h
PAT1_CFG_MMRS	31011084h
PAT2_CFG_MMRS	31012084h
PAT3_CFG_MMRS	31013084h
PAT4_CFG_MMRS	31014084h

Figure 7-4. PAT_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														DEST_ID																	
R/W-X														R/W-0h																	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-11. PAT_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

7.1.5 PAT_EXCEPTION_LOGGING_CONTROL Register (Offset = A0h) [reset = X]

PAT_EXCEPTION_LOGGING_CONTROL is shown in [Figure 7-5](#) and described in [Table 7-13](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

Table 7-12. PAT_EXCEPTION_LOGGING_CONTROL Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100A0h
PAT1_CFG_MMRS	310110A0h
PAT2_CFG_MMRS	310120A0h
PAT3_CFG_MMRS	310130A0h
PAT4_CFG_MMRS	310140A0h

Figure 7-5. PAT_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-13. PAT_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

7.1.6 PAT_EXCEPTION_LOGGING_HEADER0 Register (Offset = 310100A4h) [reset = 0h]

PAT_EXCEPTION_LOGGING_HEADER0 is shown in [Figure 7-6](#) and described in [Table 7-15](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Table 7-14. PAT_EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100A4h
PAT1_CFG_MMRS	310110A4h
PAT2_CFG_MMRS	310120A4h
PAT3_CFG_MMRS	310130A4h
PAT4_CFG_MMRS	310140A4h

Figure 7-6. PAT_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID								DEST_ID															
R-0h								R-0h								R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 7-15. PAT_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 5 = PAT.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

7.1.7 PAT_EXCEPTION_LOGGING_HEADER1 Register (Offset = A8h) [reset = X]

PAT_EXCEPTION_LOGGING_HEADER1 is shown in [Figure 7-7](#) and described in [Table 7-17](#).

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

**Table 7-16. PAT_EXCEPTION_LOGGING_HEADER1
Instances**

Instance	Physical Address
PAT0_CFG_MMRS	310100A8h
PAT1_CFG_MMRS	310110A8h
PAT2_CFG_MMRS	310120A8h
PAT3_CFG_MMRS	310130A8h
PAT4_CFG_MMRS	310140A8h

Figure 7-7. PAT_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; -n = value after reset

Table 7-17. PAT_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 1 = Boundary crossing error. 2 = Page not enabled error.
15-0	RESERVED	R	X	

7.1.8 PAT_EXCEPTION_LOGGING_DATA0 Register (Offset = ACh) [reset = 0h]

PAT_EXCEPTION_LOGGING_DATA0 is shown in [Figure 7-8](#) and described in [Table 7-19](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

Table 7-18. PAT_EXCEPTION_LOGGING_DATA0 Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100ACh
PAT1_CFG_MMRS	310110ACh
PAT2_CFG_MMRS	310120ACh
PAT3_CFG_MMRS	310130ACh
PAT4_CFG_MMRS	310140ACh

Figure 7-8. PAT_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 7-19. PAT_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

7.1.9 PAT_EXCEPTION_LOGGING_DATA1 Register (Offset = B0h) [reset = X]

PAT_EXCEPTION_LOGGING_DATA1 is shown in [Figure 7-9](#) and described in [Table 7-21](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

**Table 7-20. PAT_EXCEPTION_LOGGING_DATA1
Instances**

Instance	Physical Address
PAT0_CFG_MMRS	310100B0h
PAT1_CFG_MMRS	310110B0h
PAT2_CFG_MMRS	310120B0h
PAT3_CFG_MMRS	310130B0h
PAT4_CFG_MMRS	310140B0h

Figure 7-9. PAT_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 7-21. PAT_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 16 bits.

7.1.10 PAT_EXCEPTION_LOGGING_DATA2 Register (Offset = B4h) [reset = X]

PAT_EXCEPTION_LOGGING_DATA2 is shown in [Figure 7-10](#) and described in [Table 7-23](#).

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

Table 7-22. PAT_EXCEPTION_LOGGING_DATA2 Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100B4h
PAT1_CFG_MMRS	310110B4h
PAT2_CFG_MMRS	310120B4h
PAT3_CFG_MMRS	310130B4h
PAT4_CFG_MMRS	310140B4h

Figure 7-10. PAT_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 7-23. PAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

7.1.11 PAT_EXCEPTION_LOGGING_DATA3 Register (Offset = B8h) [reset = X]

PAT_EXCEPTION_LOGGING_DATA3 is shown in [Figure 7-11](#) and described in [Table 7-25](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the third word of the data. Reading this register will clear the error pending bit.

**Table 7-24. PAT_EXCEPTION_LOGGING_DATA3
Instances**

Instance	Physical Address
PAT0_CFG_MMRS	310100B8h
PAT1_CFG_MMRS	310110B8h
PAT2_CFG_MMRS	310120B8h
PAT3_CFG_MMRS	310130B8h
PAT4_CFG_MMRS	310140B8h

Figure 7-11. PAT_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						BYTECNT															
R-X																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 7-25. PAT_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

7.1.12 PAT_EXCEPTION_PEND_SET Register (Offset = C0h) [reset = X]

PAT_EXCEPTION_PEND_SET is shown in [Figure 7-12](#) and described in [Table 7-27](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Table 7-26. PAT_EXCEPTION_PEND_SET Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100C0h
PAT1_CFG_MMRS	310110C0h
PAT2_CFG_MMRS	310120C0h
PAT3_CFG_MMRS	310130C0h
PAT4_CFG_MMRS	310140C0h

Figure 7-12. PAT_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-27. PAT_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

7.1.13 PAT_EXCEPTION_PEND_CLEAR Register (Offset = C4h) [reset = X]

PAT_EXCEPTION_PEND_CLEAR is shown in [Figure 7-13](#) and described in [Table 7-29](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

**Table 7-28. PAT_EXCEPTION_PEND_CLEAR
Instances**

Instance	Physical Address
PAT0_CFG_MMRS	310100C4h
PAT1_CFG_MMRS	310110C4h
PAT2_CFG_MMRS	310120C4h
PAT3_CFG_MMRS	310130C4h
PAT4_CFG_MMRS	310140C4h

Figure 7-13. PAT_EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-29. PAT_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

7.1.14 PAT_EXCEPTION_ENABLE_SET Register (Offset = C8h) [reset = X]

PAT_EXCEPTION_ENABLE_SET is shown in [Figure 7-14](#) and described in [Table 7-31](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Table 7-30. PAT_EXCEPTION_ENABLE_SET Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100C8h
PAT1_CFG_MMRS	310110C8h
PAT2_CFG_MMRS	310120C8h
PAT3_CFG_MMRS	310130C8h
PAT4_CFG_MMRS	310140C8h

Figure 7-14. PAT_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-31. PAT_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

7.1.15 PAT_EXCEPTION_ENABLE_CLEAR Register (Offset = CCh) [reset = X]

PAT_EXCEPTION_ENABLE_CLEAR is shown in [Figure 7-15](#) and described in [Table 7-33](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

**Table 7-32. PAT_EXCEPTION_ENABLE_CLEAR
Instances**

Instance	Physical Address
PAT0_CFG_MMRS	310100CCh
PAT1_CFG_MMRS	310110CCh
PAT2_CFG_MMRS	310120CCh
PAT3_CFG_MMRS	310130CCh
PAT4_CFG_MMRS	310140CCh

Figure 7-15. PAT_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-33. PAT_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

7.1.16 PAT_EOI_REG Register (Offset = D0h) [reset = X]

PAT_EOI_REG is shown in [Figure 7-16](#) and described in [Table 7-35](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 7-34. PAT_EOI_REG Instances

Instance	Physical Address
PAT0_CFG_MMRS	310100D0h
PAT1_CFG_MMRS	310110D0h
PAT2_CFG_MMRS	310120D0h
PAT3_CFG_MMRS	310130D0h
PAT4_CFG_MMRS	310140D0h

Figure 7-16. PAT_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EOI_WR															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-35. PAT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EOI_WR	R/W	0h	EOI Register

7.2 PAT_CFG_SCRATCH Registers

Table 7-37 lists the memory-mapped registers for the pat_cfg_scratch registers. All register offset addresses not listed in Table 7-37 should be considered as reserved locations and the register contents should not be modified.

Page-Based Address Translation Table Scratch Region

Table 7-36. PAT_CFG_SCRATCH Instances

Instance	Base Address
PAT0_CFG_SCRATCH	36200000h
PAT1_CFG_SCRATCH	36210000h
PAT2_CFG_SCRATCH	36220000h
PAT3_CFG_SCRATCH	36230000h
PAT4_CFG_SCRATCH	36240000h

Table 7-37. PAT_CFG_SCRATCH Registers

Offset	Acronym	Register Name	PAT0_CFG_SCRATCH Physical Address	PAT1_CFG_SCRATCH Physical Address	PAT2_CFG_SCRATCH Physical Address
0h + formula	PAT_MEM_y	Scratch Memory Space	36200000h + formula	36210000h + formula	36220000h + formula

Table 7-38. PAT_CFG_SCRATCH Registers

Offset	Acronym	Register Name	PAT3_CFG_SCRATCH Physical Address	PAT4_CFG_SCRATCH Physical Address
0h + formula	PAT_MEM_y	Scratch Memory Space	36230000h + formula	36240000h + formula

7.2.1 PAT_MEM_y Register (Offset = 0h + formula) [reset = 0h]

PAT_MEM_y is shown in [Figure 7-17](#) and described in [Table 7-40](#).

Return to [Summary Table](#).

The Scratch Memory

Offset = 0h + (y * 4h); where y = 0h to 3FFFh

Table 7-39. PAT_MEM_y Instances

Instance	Physical Address
PAT0_CFG_SCRATCH	36200000h + formula
PAT1_CFG_SCRATCH	36210000h + formula
PAT2_CFG_SCRATCH	36220000h + formula
PAT3_CFG_SCRATCH	36230000h + formula
PAT4_CFG_SCRATCH	36240000h + formula

Figure 7-17. PAT_MEM_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-40. PAT_MEM_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MEM	R/W	0h	The Scratch Memory

7.3 PAT_CFG_TABLE Registers

Table 7-42 lists the memory-mapped registers for the pat0_cfg_table registers. All register offset addresses not listed in Table 7-42 should be considered as reserved locations and the register contents should not be modified.

Page-Based Address Translation Table Config Region

Table 7-41. PAT_CFG_TABLE Instances

Instance	Base Address
PAT0_CFG_TABLE	36400000h
PAT1_CFG_TABLE	36440000h
PAT2_CFG_TABLE	36480000h
PAT3_CFG_TABLE	364C0000h
PAT4_CFG_TABLE	36500000h

Table 7-42. PAT_CFG_TABLE Registers

Offset	Acronym	Register Name	PAT0_CFG_TABLE Physical Address	PAT1_CFG_TABLE Physical Address	PAT2_CFG_TABLE Physical Address
0h + formula	PAT_BASE_REG_L_j_k	Page Base Low Register	36400000h + formula	36440000h + formula	36480000h + formula
4h + formula	PAT_BASE_REG_H_j_k	Page Base High Register	36400004h + formula	36440004h + formula	36480004h + formula

Table 7-43. PAT_CFG_TABLE Registers 2

Offset	Acronym	Register Name	PAT3_CFG_TABLE Physical Address	PAT4_CFG_TABLE Physical Address
0h + formula	PAT_BASE_REG_L_j_k	Page Base Low Register	364C0000h + formula	36500000h + formula
4h + formula	PAT_BASE_REG_H_j_k	Page Base High Register	364C0004h + formula	36500004h + formula

7.3.1 PAT_BASE_REG_L_j_k Register (Offset = 0h + formula) [reset = 0h]

BASE_REG_L_j_k is shown in [Figure 7-18](#) and described in [Table 7-45](#).

Return to [Summary Table](#).

The Base Low Address bits 43 to 12 for Page. This register must be written as a full 32-bit word.

Offset = 0h + (j * 1000h) + (k * 8h); where j = 0h to 3Fh, k = 0h to FFh for PAT0, PAT1, and PAT2

Offset = 0h + (j * 1000h) + (k * 8h); where j = 0h to 7h, k = 0h to FFh for PAT3 and PAT4

Table 7-44. PAT_BASE_REG_L_j_k Instances

Instance	Physical Address
PAT0_CFG_TABLE	36400000h + formula
PAT1_CFG_TABLE	36440000h + formula
PAT2_CFG_TABLE	36480000h + formula
PAT3_CFG_TABLE	364C0000h + formula
PAT4_CFG_TABLE	36500000h + formula

Figure 7-18. PAT_BASE_REG_L_j_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE_L																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-45. PAT_BASE_REG_L_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE_L	R/W	0h	Translated Base Address bits 43 to 12 for Page. Always minimum 4KB aligned.

7.3.2 PAT_BASE_REG_H_j_k Register (Offset = 4h + formula) [reset = X]

PAT_BASE_REG_H_j_k is shown in [Figure 7-19](#) and described in [Table 7-47](#).

Return to [Summary Table](#).

The Base High Address bits 47 to 44 for Page. This register must be written as a full 32-bit word.

Offset = 4h + (j * 1000h) + (k * 8h); where j = 0h to 3Fh, k = 0h to FFh for PAT0, PAT1, and PAT2

Offset = 4h + (j * 1000h) + (k * 8h); where j = 0h to 7h, k = 0h to FFh for PAT3 and PAT4

Table 7-46. PAT_BASE_REG_H_j_k Instances

Instance	Physical Address
PAT0_CFG_TABLE	36400004h + formula
PAT1_CFG_TABLE	36440004h + formula
PAT2_CFG_TABLE	36480004h + formula
PAT3_CFG_TABLE	364C0004h + formula
PAT4_CFG_TABLE	36500004h + formula

Figure 7-19. PAT_BASE_REG_H_j_k Register

31	30	29	28	27	26	25	24
ENABLE	REPLACE_OID	RESERVED			ORDERID		
R/W-0h	R-0h	R/W-X			R-0h		
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				BASE_H			
R/W-X				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-47. PAT_BASE_REG_H_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	Translation Enable for Page. 0 = disabled. 1 = enabled.
30	REPLACE_OID	R	0h	OrderID replacement Enable for Page. It will be ignored if the global replace orderid is disabled. 0 = use input orderid. 1 = force replacement to orderid in page.
29-28	RESERVED	R/W	X	
27-24	ORDERID	R	0h	Translated orderid to use with translation address.
23-4	RESERVED	R/W	X	
3-0	BASE_H	R/W	0h	Translated Base Address bits 47 to 44 for Page

8 RAT Registers

Table 8-1 lists the memory-mapped registers for a RAT module. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Note

This section contains only the RAT register descriptions. For specific physical addresses associated with a RAT module, see the corresponding *Registers* section of the modules and subsystems listed in *Device Modules and Subsystems with RAT Module* that have integrated RAT.

Table 8-1. RAT Registers

Offset	Acronym	Register Name
0h	RAT_PID	Revision Register
4h	RAT_CONFIG	Configuration Register
20h + formula	RAT_CTRL_k	Region Control Register
24h + formula	RAT_BASE_k	Region Base Register
28h + formula	RAT_TRANS_L_k	Region Translated Lower Address
2Ch + formula	RAT_TRANS_U_k	Region Translated Upper Address
804h	RAT_DESTINATION_ID	Destination ID Register
820h	RAT_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register
824h	RAT_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register
828h	RAT_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register
82Ch	RAT_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register
830h	RAT_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register
834h	RAT_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register
838h	RAT_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register
840h	RAT_EXCEPTION_PEND_SET	Exception Logging Interrupt Pending Set Register
844h	RAT_EXCEPTION_PEND_CLEAR	Exception Logging Interrupt Pending Clear Register
848h	RAT_EXCEPTION_ENABLE_SET	Exception Logging Interrupt Enable Set Register
84Ch	RAT_EXCEPTION_ENABLE_CLEAR	Exception Logging Interrupt Enable Clear Register
850h	RAT_EOI_REG	EOI Register

8.1 RAT_PID Register (Offset = 0h) [reset = 66802900h]

RAT_PID is shown in [Figure 8-1](#) and described in [Table 8-2](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Figure 8-1. RAT_PID Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-680h			
23	22	21	20	19	18	17	16
FUNC							
R-680h							
15	14	13	12	11	10	9	8
RTL					MAJOR		
R-5h					R-1h		
7	6	5	4	3	2	1	0
CUSTOM		MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 8-2. RAT_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	Business Unit: 2h = Processors
27-16	FUNC	R	680h	Module ID
15-11	RTL	R	5h	RTL Revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor Revision

8.2 RAT_CONFIG Register (Offset = 4h) [reset = X]

RAT_CONFIG is shown in [Figure 8-2](#) and described in [Table 8-3](#).

Return to [Summary Table](#).

The Configuration Register contains the configuration values for the module.

Figure 8-2. RAT_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								ADDR_WIDTH							
R-X								R-30h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRS								REGIONS							
R-1h								R-10h							

LEGEND: R = Read Only; -n = value after reset

Table 8-3. RAT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23-16	ADDR_WIDTH	R	30h	Number of address bits
15-8	ADDRS	R	1h	Number of addresses
7-0	REGIONS	R	10h	Number of regions

8.3 RAT_CTRL_k Register (Offset = 20h + formula) [reset = X]

RAT_CTRL_k is shown in [Figure 8-3](#) and described in [Table 8-4](#).

Return to [Summary Table](#).

The Control for Region a

Offset = 1020h + (k * 10h); where k = 0h to Fh

Figure 8-3. RAT_CTRL_k Register

31	30	29	28	27	26	25	24
EN	RESERVED						
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				SIZE			
R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-4. RAT_CTRL_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Enable for the Region 0h = Region disabled 1h = Region enabled
30-6	RESERVED	R/W	X	
5-0	SIZE	R/W	0h	Size of the Region in Address Bits. 0h = 1 byte, 1h = 2B, 2h = 4B, 3h = 8B, etc. up to 20h = 4GB.

8.4 RAT_BASE_k Register (Offset = 24h + formula) [reset = 0h]

RAT_BASE_k is shown in [Figure 8-4](#) and described in [Table 8-5](#).

Return to [Summary Table](#).

The Base Address for Region a. This is the source address for matching to a region.

Offset = 1024h + (k * 10h); where k = 0h to Fh

Figure 8-4. RAT_BASE_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-5. RAT_BASE_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE	R/W	0h	Base Address for the Region. It must be aligned to the programmed size.

8.5 RAT_TRANS_L_k Register (Offset = 28h + formula) [reset = 0h]

RAT_TRANS_L_k is shown in [Figure 8-5](#) and described in [Table 8-6](#).

Return to [Summary Table](#).

The Translated Lower Address Bits for Region a

Offset = 1028h + (k * 10h); where k = 0h to Fh

Figure 8-5. RAT_TRANS_L_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOWER																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-6. RAT_TRANS_L_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOWER	R/W	0h	Translated Lower Address Bits for the Region. It must be aligned to the programmed size.

8.6 RAT_TRANS_U_k Register (Offset = 2Ch + formula) [reset = X]

RAT_TRANS_U_k is shown in [Figure 8-6](#) and described in [Table 8-7](#).

Return to [Summary Table](#).

The Translated Upper Address Bits for Region a

Offset = 102Ch + (k * 10h); where k = 0h to Fh

Figure 8-6. RAT_TRANS_U_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UPPER															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-7. RAT_TRANS_U_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	UPPER	R/W	0h	Translated Upper Address Bits for the Region

8.7 RAT_DESTINATION_ID Register (Offset = 1804h) [reset = X]

RAT_DESTINATION_ID is shown in [Figure 8-7](#) and described in [Table 8-8](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

Figure 8-7. RAT_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DEST_ID							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-8. RAT_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID. This field can be used for identifying a destination tag so that software can identify who should process the error message. In case of single consumer of the error messages this field is not useful and can be programmed to any value.

8.8 RAT_EXCEPTION_LOGGING_CONTROL Register (Offset = 1820h) [reset = X]

RAT_EXCEPTION_LOGGING_CONTROL is shown in [Figure 8-8](#) and described in [Table 8-9](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

Figure 8-8. RAT_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_INTR	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-9. RAT_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_INTR	R/W	0h	Disables logging interrupt when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

8.9 RAT_EXCEPTION_LOGGING_HEADER0 Register (Offset = 1824h) [reset = 0h]

RAT_EXCEPTION_LOGGING_HEADER0 is shown in [Figure 8-9](#) and described in [Table 8-10](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Figure 8-9. RAT_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24
TYPE_F							
R-0h							
23	22	21	20	19	18	17	16
SRC_ID							
R-0h							
15	14	13	12	11	10	9	8
SRC_ID							
R-0h							
7	6	5	4	3	2	1	0
DEST_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-10. RAT_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 4h = RAT.
23-8	SRC_ID	R	0h	Source ID. This field uniquely identifies the particular RAT and region that caused the error. Each RAT has a unique source ID value (see <i>RAT Source ID Mapping</i>). The error message increments that value by the region number associated with the error.
7-0	DEST_ID	R	0h	Destination ID.

8.10 RAT_EXCEPTION_LOGGING_HEADER1 Register (Offset = 1828h) [reset = X]

RAT_EXCEPTION_LOGGING_HEADER1 is shown in [Figure 8-10](#) and described in [Table 8-11](#).

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

Figure 8-10. RAT_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24
GROUP							
R-0h							
23	22	21	20	19	18	17	16
CODE							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							
R-X							

LEGEND: R = Read Only; -n = value after reset

Table 8-11. RAT_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code. 1h = Boundary crossing error.
15-0	RESERVED	R	X	

8.11 RAT_EXCEPTION_LOGGING_DATA0 Register (Offset = 182Ch) [reset = 0h]

RAT_EXCEPTION_LOGGING_DATA0 is shown in [Figure 8-11](#) and described in [Table 8-12](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

Figure 8-11. RAT_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 8-12. RAT_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	The lower 32 bits of the address attempted to be accessed.

8.12 RAT_EXCEPTION_LOGGING_DATA1 Register (Offset = 1830h) [reset = X]

RAT_EXCEPTION_LOGGING_DATA1 is shown in [Figure 8-12](#) and described in [Table 8-13](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

Figure 8-12. RAT_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_H															
R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 8-13. RAT_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	The upper 12 bits of the address attempted to be accessed.

8.13 RAT_EXCEPTION_LOGGING_DATA2 Register (Offset = 1834h) [reset = X]

RAT_EXCEPTION_LOGGING_DATA2 is shown in [Figure 8-13](#) and described in [Table 8-14](#).

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

Figure 8-13. RAT_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-14. RAT_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID transaction attribute.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Indicates write transaction. 0h = No write transaction 1h = Write transaction
12	READ	R	0h	Indicates read transaction. 0h = No read transaction 1h = Read transaction
11	DEBUG	R	0h	Indicates debug access. 0h = No debug access 1h = Debug access
10	CACHEABLE	R	0h	Cacheable transaction attribute. 0h = The transaction could not cache the data for the CPU 1h = The transaction could cache the data for the CPU
9	PRIV	R	0h	Indicates privilege access. 0h = No privilege access 1h = Privilege access
8	SECURE	R	0h	Indicates secure access. 0h = No secure access 1h = Secure access
7-0	PRIV_ID	R	0h	Priv ID transaction attribute.

8.14 RAT_EXCEPTION_LOGGING_DATA3 Register (Offset = 1838h) [reset = X]

RAT_EXCEPTION_LOGGING_DATA3 is shown in [Figure 8-14](#) and described in [Table 8-15](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Figure 8-14. RAT_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED						BYTECNT	
R-X						R-0h	
7	6	5	4	3	2	1	0
BYTECNT							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 8-15. RAT_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count transaction attribute.

8.15 RAT_EXCEPTION_PEND_SET Register (Offset = 1840h) [reset = X]

RAT_EXCEPTION_PEND_SET is shown in [Figure 8-15](#) and described in [Table 8-16](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Figure 8-15. RAT_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-16. RAT_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

8.16 RAT_EXCEPTION_PEND_CLEAR Register (Offset = 1844h) [reset = X]

RAT_EXCEPTION_PEND_CLEAR is shown in [Figure 8-16](#) and described in [Table 8-17](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Figure 8-16. RAT_EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-17. RAT_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

8.17 RAT_EXCEPTION_ENABLE_SET Register (Offset = 1848h) [reset = X]

RAT_EXCEPTION_ENABLE_SET is shown in [Figure 8-17](#) and described in [Table 8-18](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Figure 8-17. RAT_EXCEPTION_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-18. RAT_EXCEPTION_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_SET	R/W1S	0h	Write a 1 to set the exception interrupt enable signal.

8.18 RAT_EXCEPTION_ENABLE_CLEAR Register (Offset = 184Ch) [reset = X]

RAT_EXCEPTION_ENABLE_CLEAR is shown in [Figure 8-18](#) and described in [Table 8-19](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Figure 8-18. RAT_EXCEPTION_ENABLE_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-19. RAT_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLE_CLR	R/W1C	0h	Write a 1 to clear the exception interrupt enable signal.

8.19 RAT_EOI_REG Register (Offset = 850h) [reset = X]

RAT_EOI_REG is shown in [Figure 8-19](#) and described in [Table 8-20](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Figure 8-19. RAT_EOI_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EOI_WR															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-20. RAT_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EOI_WR	R/W	0h	EOI Register

9 CLEC Registers

Table 9-2 lists the memory-mapped registers for the CLEC registers. All register offset addresses not listed in Table 9-2 should be considered as reserved locations and the register contents should not be modified.

Table 9-1. CLEC Instances

Instance	Base Address
COMPUTE_CLUSTER0_CLEC_REGS	7800 0000h

Table 9-2. CLEC_REGS Registers

Offset	Acronym	Register Name	Register Type	COMPUTE_CLUSTER0_CLEC_REGS Physical Address
0h	CLEC_PID	CLEC PID register	Global	7800 0000h
C000h	CLEC_GELRS	CLEC global event lock register for secure claims	Global	7800 C000h
D000h	CLEC_GELRNS	CLEC global event lock register for non-secure claims	Global	7800 D000h
A000h + formula	CLEC_EFR_k	CLEC event flag register	Global	7800 A000h + formula
B000h + formula	CLEC_EDR_k	CLEC event drop register	Global	7800 B000h + formula
11000h + formula	CLEC_MRR_j	CLEC map and routing register	Per-event	7801 1000h + formula
13000h + formula	CLEC_ESR_j	CLEC event send register	Per-event	7801 3000h + formula
14000h + formula	CLEC_ECR_j	CLEC event clear register	Per-event	7801 4000h + formula

9.1 CLEC_PID Register (Offset = 0h) [reset = 60100100h]

CLEC_PID is shown in [Figure 9-1](#) and described in [Table 9-4](#).

Return to [Summary Table](#).

Peripheral identification register. Uniquely identifies the module and its specific revision.

Table 9-3. CLEC_PID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7800 0000h

Figure 9-1. CLEC_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-60100100h																															

Table 9-4. CLEC_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	60100100h	TI internal data. Identifies revision of peripheral.

9.2 CLEC_GELRS Register (Offset = C000h) [reset = 0h]

CLEC_GELRS is shown in [Figure 9-2](#) and described in [Table 9-6](#).

Return to [Summary Table](#).

Global event lock register for secure claims. The purpose of this register is to allow a hypervisor to expose an event to a virtual machine container, while preventing that virtual machine from changing the configuration. The hypervisor must provide a writeable page to the contained virtual machine so that the virtual machine can use the CLEC_ESR_j register. The CLEC_GELRS register acts as a global control, removing write permission to CLEC_MRR_j when CLEC_MRR_j[31] S = 1. Since only root supervisor has access to the global registers, only root supervisor may change the value of the CLEC_GELRS[0] LOCK bit.

Table 9-5. CLEC_GELRS Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7800 C000h

Figure 9-2. CLEC_GELRS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-0h							R/W-0h

Table 9-6. CLEC_GELRS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	Global event lock bit for secure claims. When set, all the event configurations that are marked with CLEC_MRR_j[31] S = 1 become read-only. Attempts to write the CLEC_MRR_j register for that event will return a privilege error. When cleared, CLEC_MRR_j may be read or written. This is an advisory lock to avoid spurious writes.

9.3 CLEC_GELRNS Register (Offset = D000h) [reset = 0h]

CLEC_GELRNS is shown in [Figure 9-3](#) and described in [Table 9-8](#).

Return to [Summary Table](#).

Global event lock register for non-secure claims. The purpose of this register is to allow a hypervisor to expose an event to a virtual machine container, while preventing that virtual machine from changing the configuration. The hypervisor must provide a writeable page to the contained virtual machine so that the virtual machine can use the CLEC_ESR_j register. The CLEC_GELRNS register acts as a global control, removing write permission to CLEC_MRR_j when CLEC_MRR_j[31] S = 0. Since only root supervisor has access to the global registers, only root supervisor may change the value of the CLEC_GELRNS[0] LOCK bit.

Table 9-7. CLEC_GELRNS Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7800 D000h

Figure 9-3. CLEC_GELRNS Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-0h							R/W-0h

Table 9-8. CLEC_GELRNS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	LOCK	R/W	0h	Global event lock bit for secure claims. When set, all the event configurations that are marked with CLEC_MRR_j[31] S = 0 become read-only. Attempts to write the CLEC_MRR_j register for that event will return a privilege error. When cleared, CLEC_MRR_j may be read or written. This is an advisory lock to avoid spurious writes.

9.4 CLEC_EFR_k Register (Offset = A000h + formula) [reset = 0h]

CLEC_EFR_k is shown in [Figure 9-4](#) and described in [Table 9-10](#).

Return to [Summary Table](#).

Event flag register. This is a read-only register which contains pending flag for all events queued by CLEC. This flag is set regardless if corresponding event is enabled or disabled.

Offset = A000h + (k * 4h); where k = 0h to 3Eh.

Table 9-9. CLEC_EFR_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7800 A000h + formula

Figure 9-4. CLEC_EFR_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNTFR																															
R-0h																															

Table 9-10. CLEC_EFR_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EVNTFR	R	0h	<p>Event pending flags for events 0 to N. For pulse events, an event flag is cleared as soon as corresponding event is sent. For level events, an event flag is cleared when corresponding interrupt event is deasserted. This is to support scenario where CPU wants to disable some event temporarily, while doing some important task, and then re-enable the event; however, when CPU re-enables the event, CPU does not want to miss any event that occurred when it was disabled temporarily.</p> <p>The event flag can be cleared by writing 0x1 to corresponding CLEC_ECR_j register before enabling the event; this will avoid any spurious event during power-up/power-down to reach to CPU.</p> <p>Flags for secure events can only be read by secure supervisor. Non-secure supervisor always gets value 0 for secure event flags.</p>

9.5 CLEC_EDR_k Register (Offset = B000h + formula) [reset = 0h]

CLEC_EDR_k is shown in [Figure 9-5](#) and described in [Table 9-12](#).

Return to [Summary Table](#).

Event drop register. This is a read-only register which contains dropped event flag for each event. For input events which are pulse and not level, if CLEC receives back to back pulses of event and second pulse comes before event flag for the first event is cleared (which means event is not sent from CLEC queue yet), there is no way to tell destination that there were two events requested. CLEC will generate dropped event interrupt in this case and will also set corresponding event dropped flag in CLEC_EDR_k register.

Offset = B000h + (k * 4h); where k = 0h to 3Eh.

Table 9-11. CLEC_EDR_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7800 B000h + formula

Figure 9-5. CLEC_EDR_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVNTFR																															
R-0h																															

Table 9-12. CLEC_EDR_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EVNTFR	R	0h	Dropped event flags for events 0 to N. This flag bit is set until SW clears it by writing 0x2 to the corresponding CLEC_ECR_j register.

9.6 CLEC_MRR_j Register (Offset = 11000h + formula) [reset = 81010000h]

CLEC_MRR_j is shown in [Figure 9-6](#) and described in [Table 9-14](#).

Return to [Summary Table](#).

Map and routing register. This register is readable by any privilege level. It is writeable by supervisor mode if unlocked by CLEC_GELRS or CLEC_GELRNS registers.

Offset = 11000h + (j * 00010000h); where j = 0h to 7FEh.

Table 9-13. CLEC_MRR_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7801 1000h + formula

Figure 9-6. CLEC_MRR_j Register

31	30	29	28	27	26	25	24
S	ESE	RSVD3				EVTPF	IS_LVL
R/W-1h	R/W-0h	R-0h				R-0h	R/W-1h
23	22	21	20	19	18	17	16
RSVD2		RTMAP					
R-0h		R/W-1h					
15	14	13	12	11	10	9	8
EXT_EVTNUM							
R/W-0h							
7	6	5	4	3	2	1	0
RSVD0		C7X_EVTNUM					
R-0h		R/W-0h					

Table 9-14. CLEC_MRR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	S	R/W	1h	Secure claim. If set to 1, a non-secure read/write to CLEC_MRR_j will generate a privilege error
30	ESE	R/W	0h	Event send enable. Controls whether CLEC sends this event when CLEC_ESR_j is written or event occurred on interrupt line
29-26	RESERVED	R	0h	Reserved
25	EVTPF	R	0h	Event pending flag. Same value as corresponding CLEC_EFR_k bit
24	IS_LVL	R/W	1h	Indicates if input event is level (1) or pulse (0). It is expected from firmware to initialize this information accurately for proper CLEC operation
23-22	RESERVED	R	0h	Reserved

Table 9-14. CLEC_MRR_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	RTMAP	R/W	1h	Routing table map.
				Bit [16] controls the disable/enable of the event routing. Bit [16] = 1 disables the event routing (that is, the event is not send anywhere), regardless of the configuration of the [21-17] bits. Bit [16] = 0 allows sending the event to any supported destination depending on the configuration of the [21-17] bits.
				Bit [17] controls the export of the event out of the Compute Cluster to the system (SoC). If bit [17] = 1 AND bit [16] = 0, the event is routed to the system.
				<p>Bits [21-18] controls the routing of the event to any Compute Cluster internal CPU corepac (Arm or DSP), as long as bit [16] = 0. The encoding of the [21-18] bits is generic and the actual available options depend on SoC integration. The encoding is as follows:</p> <p>0h = Send event to CPU Corepac 0 (= Arm Corepac 0). Although the device implements this Corepac (A72SS0), this option is not actually supported as the A72SS0 receives interrupt from GIC0 instead.</p> <p>1h = Send event to CPU Corepac 1 (= Arm Corepac 1). N/A in this device.</p> <p>2h = Send event to CPU Corepac 2 (= Arm Corepac 2). N/A in this device.</p> <p>3h = Send event to CPU Corepac 3 (= Arm Corepac 3). N/A in this device.</p> <p>4h = Send event to CPU Corepac 4 (= C7x Corepac 0). That is the only valid option for this device.</p> <p>5h = Send event to CPU Corepac 5 (= C7x Corepac 1). N/A in this device.</p> <p>6h = Send event to CPU Corepac 6 (= C7x Corepac 2). N/A in this device.</p> <p>7h = Send event to CPU Corepac 7 (= C7x Corepac 3). N/A in this device.</p> <p>...</p> <p>Fh = Send event to all CPU Corepacs.</p> <p>Note: For events mapped to DRU or Arm Corepac (via the [15-8] EXT_EVTNUM bit field), RTMAP is "don't care".</p>
15-8	EXT_EVTNUM	R/W	0h	Encoded external event number to send when this event is triggered
7-6	RESERVED	R	0h	Reserved
5-0	C7X_EVTNUM	R/W	0h	C7x event number to send when this event is triggered

Note

For DRU events, the default (reset) values for some of the CLEC_MRR_j register bit fields differ from the ones stated in the above table. These DRU events are enabled and routed to C7x DSP by default. Because DRU events are internal to MSMC_WRAP, bring up of MSMC/CLEC and DRU is done at the same time and synchronously, so there is no concern of glitch or spurious interrupt.

The following default values are valid for DRU events:

- For DRU complete events (event number 64 to 80):
 - ESE = 1
 - IS_LVL = 0
 - RTMAP = 3C
 - C7x_EVNUM = $n\%64$
 - For DRU error events (event number 128 to 144):
 - ESE = 1
 - IS_LVL = 0
 - RTMAP = 3C
 - C7x_EVNUM = $n\%64 + 16$
 - For DRU error events (event number 192 to 208):
 - ESE = 1
 - IS_LVL = 0
 - RTMAP = 3C
 - C7x_EVNUM = $n\%64 + 32$
-

9.7 CLEC_ESR_j Register (Offset = 13000h + formula) [reset = 0h]

CLEC_ESR_j is shown in [Figure 9-7](#) and described in [Table 9-16](#).

Return to [Summary Table](#).

Event send register. This is a write-only register. It ignores the value written (stateless). When written, the CLEC will:

- Generate an internal event specified by CLEC_MRR_j[5-0] C7x_EVNUM, if CLEC_MRR_j[30] ESE is set for that event
- Generate an external event specified by CLEC_MRR_j[13-8] EXT_EVNUM, if CLEC_MRR_j[30] ESE is set for that event

Otherwise, the CLEC does not send an event in response to the write; instead, it returns a privilege error for the write status.

Note

Corepac powerup/powerdown sequence should comprehend CLEC sequencing to avoid interrupt dropped events.

Offset = 13000h + (j * 00010000h); where j = 0h to 7FEh.

Table 9-15. CLEC_ESR_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7801 3000h + formula

Figure 9-7. CLEC_ESR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															
W-0h																															

Table 9-16. CLEC_ESR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	W	0h	Reserved

9.8 CLEC_ECR_j Register (Offset = 14000h + formula) [reset = 0h]

CLEC_ECR_j is shown in [Figure 9-8](#) and described in [Table 9-18](#).

Return to [Summary Table](#).

Event clear register. This is a write-only register. When written value 0x1, the CLEC will clear any level interrupt set for that event.

Offset = 14000h + (j * 00010000h); where j = 0h to 7FEh

Table 9-17. CLEC_ECR_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_CLEC_REGS	7801 4000h + formula

Figure 9-8. CLEC_ECR_j Register

31	30	29	28	27	26	25	24
RESERVED							
W-0h							
23	22	21	20	19	18	17	16
RESERVED							
W-0h							
15	14	13	12	11	10	9	8
RESERVED							
W-0h							
7	6	5	4	3	2	1	0
RESERVED						ECR_PFLAG	ECR_FLAG
W-0h						W-0h	W-0h

Table 9-18. CLEC_ECR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	W	0h	Reserved
1	ECR_PFLAG	W	0h	Writing 1 to this bit clears associated CLEC_EDR_k bit
0	ECR_FLAG	W	0h	Writing 1 to this bit clears event and associated CLEC_EFR_k bit

10 NAVSS Top-level Registers

10.1 NAVSS0_CFG Registers

Table 11-2 lists the memory-mapped registers for the NAVSS0_CFG registers. All register offset addresses not listed in Table 11-2 should be considered as reserved locations and the register contents should not be modified.

The modss_regs Register Address Space. The address map for this region is as follows:

Table 10-1. NAVSS0_CFG Instances

Instance	Base Address
NAVSS0_CFG	310C 0000h

Table 10-2. NAVSS0_CFG Registers

Offset	Acronym	Register Name	NAVSS0_CFG Physical Address
0h	NAVSS_PID	Revision Register	310C 0000h

10.1.1 NAVSS_PID Register (Offset = 0h) [reset = 6640AA00h]

NAVSS_PID is shown in [Figure 10-1](#) and described in [Table 10-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 10-3. NAVSS_PID Instances

Instance	Physical Address
NAVSS0_CFG	310C 0000h

Figure 10-1. NAVSS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R-1h		R-2h		R-640h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJREV			CUSTOM		MINREV					
R-15h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 10-4. NAVSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNCTION	R	640h	Module ID
15-11	RTL	R	15h	RTL revision. Will vary depending on release.
10-8	MAJREV	R	2h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINREV	R	0h	Minor revision

10.2 INTR0_INTR_ROUTER_CFG Registers

Table 10-6 lists the memory-mapped registers for the INTR0_INTR_ROUTER_CFG registers. All register offset addresses not listed in Table 10-6 should be considered as reserved locations and the register contents should not be modified.

Table 10-5. INTR0_INTR_ROUTER_CFG Instances

Instance	Base Address
NAVSS0_INTR0_INTR_ROUTER_CFG	310E 0000h
MCU_NAVSS0_INTR0_CFG	2854 0000h

Table 10-6. INTR0_INTR_ROUTER_CFG Registers

Offset	Acronym	Register Name	NAVSS0_INTR0_INTR_ROUTER_CFG Physical Address	MCU_NAVSS0_INTR0_CFG Physical Address
0h	INTR_ROUTER_PID	Interrupt router identification register	310E 0000h	2854 0000h
4h + formula	INTR_ROUTER_MUXCNTL_y	Interrupt router mux control	310E 0004h + formula	2854 0004h + formula

10.2.1 INTR_ROUTER_PID Register (Offset = 0h) [reset = 66948100h]

INTR_ROUTER_PID is shown in [Figure 10-2](#) and described in [Table 10-8](#).

Return to [Summary Table](#).

Identification register

Table 10-7. INTR_ROUTER_PID Instances

Instance	Physical Address
NAVSS0_INTR0_INTR_ROUTER_CFG	310E 0000h
MCU_NAVSS0_INTR0_CFG	2854 0000h

Figure 10-2. INTR_ROUTER_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R-1h		R-2h		R-694h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJREV			CUSTOM		MINREV					
R-10h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 10-8. INTR_ROUTER_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID scheme
29-28	BU	R	2h	bu
27-16	FUNCTION	R	694h	function
15-11	RTL	R	10h	RTL version 10h - NAVSS0 Fh - MCU_NAVSS0
10-8	MAJREV	R	1h	major version
7-6	CUSTOM	R	0h	custom id
5-0	MINREV	R	0h	minor version

10.2.2 INTR_ROUTER_MUXCNTL_y Register (Offset = 4h + formula) [reset = X]

INTR_ROUTER_MUXCNTL_y is shown in [Figure 10-3](#) and described in [Table 10-10](#).

Return to [Summary Table](#).

Interrupt mux control register

Offset = 4h + (y * 4); where y = 0h to 1FFh for NAVSS0

Offset = 4h + (y * 4); where y = 0h to 3Fh for MCU_NAVSS0

Table 10-9. INTR_ROUTER_MUXCNTL_y Instances

Instance	Physical Address
NAVSS0_INTR0_INTR_ROUTER_CFG	310E 0004h + formula
MCU_NAVSS0_INTR0_CFG	2854 0004h + formula

Figure 10-3. INTR_ROUTER_MUXCNTL_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							INT_ENABLE
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							MUX_CONTROL
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
MUX_CONTROL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-10. INTR_ROUTER_MUXCNTL_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R/W	X	
16	INT_ENABLE	R/W	0h	Interrupt output enable for interrupt y
15-9	RESERVED	R/W	X	
8-0	MUX_CONTROL	R/W	0h	Mux control for interrupt y Avoid programming the mux control when input interrupts are enabled via INT_ENABLE.

10.3 VIRTID_CFG_MMRS Registers

Table 10-12 lists the memory-mapped registers for the VIRTID_CFG_MMRS registers. All register offset addresses not listed in Table 10-12 should be considered as reserved locations and the register contents should not be modified.

VirtID Translation Config Region

Table 10-11. VIRTID_CFG_MMRS Instances

Instance	Base Address
NAV_DDR0_VIRTID_CFG_MMRS	30A0 2000h
NAV_DDR1_VIRTID_CFG_MMRS	30A0 3000h
NBSS_CFG_MSMC0_SLV_VIRTID_CFG_MMRS	0381 0000h

Table 10-12. VIRTID_CFG_MMRS Registers

Offset	Acronym	Register Name	NAV_DDR0_VIRTID_CFG_MMRS Physical Address	NAV_DDR1_VIRTID_CFG_MMRS Physical Address	NBSS_CFG_MSMC0_SLV_VIRTID_CFG_MMRS Physical Address
0h	VIRTID_PID	Revision Register	30A0 2000h	30A0 3000h	0381 0000h
10h + formula	VIRTID_WINDOW_y	VirtID Mapping Registers	30A0 2010h + formula	30A0 3010h + formula	0381 0010h + formula

10.3.1 VIRTID_PID Register (Offset = 0h) [reset = 66381100h]

VIRTID_PID is shown in [Figure 10-4](#) and described in [Table 10-14](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 10-13. VIRTID_PID Instances

Instance	Physical Address
NAV_DDR0_VIRTID_CFG_MMRS	30A0 2000h
NAV_DDR1_VIRTID_CFG_MMRS	30A0 3000h
NBSS_CFG_MSMC0_SLV_VIRTID_CFG_MMRS	0381 0000h

Figure 10-4. VIRTID_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R-1h		R-2h		R-638h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJREV			CUSTOM		MINREV					
R-2h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 10-14. VIRTID_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNCTION	R	638h	Module ID
15-11	RTL	R	2h	RTL revision. Will vary depending on release.
10-8	MAJREV	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINREV	R	0h	Minor revision

10.3.2 VIRTID_WINDOW_y Register (Offset = 30A02010h + formula) [reset = X]

VIRTID_WINDOW_y is shown in [Figure 10-5](#) and described in [Table 10-16](#).

Return to [Summary Table](#).

The VirtID for window y.

Offset = 30A02010h + (y * 4h); where y = 0h to Fh

Table 10-15. VIRTID_WINDOW_y Instances

Instance	Physical Address
NAV_DDR0_VIRTID_CFG_MMRS	30A0 2010h + formula
NAV_DDR1_VIRTID_CFG_MMRS	30A0 3010h + formula
NBSS_CFG_MSMC0_SLV_VIRTID_CFG_MMRS	0381 0010h + formula

Figure 10-5. VIRTID_WINDOW_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																					VIRTID																
R/W-X																					R/W-0h																

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-16. VIRTID_WINDOW_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	VIRTID	R/W	0h	VirtID for window y

11 MCU NAVSS Top-Level Registers

11.1 MCU_NAVSS0_CFG Registers

Table 11-2 lists the memory-mapped registers for the MCU_NAVSS0_CFG. All register offset addresses not listed in Table 11-2 should be considered as reserved locations and the register contents should not be modified.

The modss_regs Register Address Space. The address map for this region is as follows:

Table 11-1. MCU_NAVSS0_CFG Instances

Instance	Base Address
MCU_NAVSS0_CFG	2852 0000h

Table 11-2. MCU_NAVSS0_CFG Registers

Offset	Acronym	Register Name	MCU_NAVSS0_CFG Physical Address
0h	MCU_NAVSS_PID	Revision Register	2852 0000h

11.1.1 MCU_NAVSS_PID Register (Offset = 0h) [reset = 66486A00h]

MCU_NAVSS_PID is shown in [Figure 11-1](#) and described in [Table 11-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 11-3. MCU_NAVSS_PID Instances

Instance	Physical Address
MCU_NAVSS0_CFG	2852 0000h

Figure 11-1. MCU_NAVSS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-648h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 11-4. MCU_NAVSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	648h	Module ID
15-11	RTL	R	Dh	RTL revision. Will vary depending on release.
10-8	MAJOR	R	2h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

11.2 MCU_NAVSS0_UDMASS_ECCAGGR0 Registers

Table 11-6 lists the memory-mapped registers for the MCU_NAVSS0_UDMASS_ECCAGGR0. All register offset addresses not listed in Table 11-6 should be considered as reserved locations and the register contents should not be modified.

**Table 11-5. MCU_NAVSS0_UDMASS_ECCAGGR0
Instances**

Instance	Base Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1000h

Table 11-6. MCU_NAVSS0_UDMASS_ECCAGGR0 Registers

Offset	Acronym	Register Name	MCU_NAVSS0_UDMASS_ECCAGGR0 Physical Address
0h	MCU_NAVSS_REV	Aggregator Revision Register	2838 1000h
8h	MCU_NAVSS_VECTOR	ECC Vector Register	2838 1008h
Ch	MCU_NAVSS_STAT	Misc Status	2838 100Ch
3Ch	MCU_NAVSS_SEC_EOI_REG	EOI Register	2838 103Ch
40h	MCU_NAVSS_SEC_STATUS_REG0	Interrupt Status Register 0	2838 1040h
44h	MCU_NAVSS_SEC_STATUS_REG1	Interrupt Status Register 1	2838 1044h
48h	MCU_NAVSS_SEC_STATUS_REG2	Interrupt Status Register 2	2838 1048h
4Ch	MCU_NAVSS_SEC_STATUS_REG3	Interrupt Status Register 3	2838 104Ch
80h	MCU_NAVSS_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	2838 1080h
84h	MCU_NAVSS_SEC_ENABLE_SET_REG1	Interrupt Enable Set Register 1	2838 1084h
88h	MCU_NAVSS_SEC_ENABLE_SET_REG2	Interrupt Enable Set Register 2	2838 1088h
8Ch	MCU_NAVSS_SEC_ENABLE_SET_REG3	Interrupt Enable Set Register 3	2838 108Ch
C0h	MCU_NAVSS_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	2838 10C0h
C4h	MCU_NAVSS_SEC_ENABLE_CLR_REG1	Interrupt Enable Clear Register 1	2838 10C4h
C8h	MCU_NAVSS_SEC_ENABLE_CLR_REG2	Interrupt Enable Clear Register 2	2838 10C8h
CCh	MCU_NAVSS_SEC_ENABLE_CLR_REG3	Interrupt Enable Clear Register 3	2838 10CCh
13Ch	MCU_NAVSS_DED_EOI_REG	EOI Register	2838 113Ch
140h	MCU_NAVSS_DED_STATUS_REG0	Interrupt Status Register 0	2838 1140h
144h	MCU_NAVSS_DED_STATUS_REG1	Interrupt Status Register 1	2838 1144h
148h	MCU_NAVSS_DED_STATUS_REG2	Interrupt Status Register 2	2838 1148h
14Ch	MCU_NAVSS_DED_STATUS_REG3	Interrupt Status Register 3	2838 114Ch
180h	MCU_NAVSS_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	2838 1180h
184h	MCU_NAVSS_DED_ENABLE_SET_REG1	Interrupt Enable Set Register 1	2838 1184h
188h	MCU_NAVSS_DED_ENABLE_SET_REG2	Interrupt Enable Set Register 2	2838 1188h
18Ch	MCU_NAVSS_DED_ENABLE_SET_REG3	Interrupt Enable Set Register 3	2838 118Ch
1C0h	MCU_NAVSS_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	2838 11C0h
1C4h	MCU_NAVSS_DED_ENABLE_CLR_REG1	Interrupt Enable Clear Register 1	2838 11C4h
1C8h	MCU_NAVSS_DED_ENABLE_CLR_REG2	Interrupt Enable Clear Register 2	2838 11C8h
1CCh	MCU_NAVSS_DED_ENABLE_CLR_REG3	Interrupt Enable Clear Register 3	2838 11CCh
200h	MCU_NAVSS_AGGR_ENABLE_SET	AGGR interrupt enable set Register	2838 1200h
204h	MCU_NAVSS_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	2838 1204h
208h	MCU_NAVSS_AGGR_STATUS_SET	AGGR interrupt status set Register	2838 1208h
20Ch	MCU_NAVSS_AGGR_STATUS_CLR	AGGR interrupt status clear Register	2838 120Ch

11.2.1 MCU_NAVSS_REV Register (Offset = 0h) [reset = 66A0E200h]

MCU_NAVSS_REV is shown in [Figure 11-2](#) and described in [Table 11-8](#).

[Return to Summary Table.](#)

Revision parameters

Table 11-7. MCU_NAVSS_REV Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1000h

Figure 11-2. MCU_NAVSS_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Ch					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 11-8. MCU_NAVSS_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Ch	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

11.2.2 MCU_NAVSS_VECTOR Register (Offset = 8h) [reset = X]

MCU_NAVSS_VECTOR is shown in [Figure 11-3](#) and described in [Table 11-10](#).

Return to [Summary Table](#).

ECC Vector Register

Table 11-9. MCU_NAVSS_VECTOR Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1008h

Figure 11-3. MCU_NAVSS_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-10. MCU_NAVSS_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

11.2.3 MCU_NAVSS_STAT Register (Offset = Ch) [reset = X]

MCU_NAVSS_STAT is shown in [Figure 11-4](#) and described in [Table 11-12](#).

Return to [Summary Table](#).

Misc Status

Table 11-11. MCU_NAVSS_STAT Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 100Ch

Figure 11-4. MCU_NAVSS_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMs										
R-X																					R-78h										

LEGEND: R = Read Only; -n = value after reset

Table 11-12. MCU_NAVSS_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMs	R	78h	Indicates the number of RAMs serviced by the ECC aggregator

11.2.4 MCU_NAVSS_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

MCU_NAVSS_SEC_EOI_REG is shown in [Figure 11-5](#) and described in [Table 11-14](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 11-13. MCU_NAVSS_SEC_EOI_REG Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 103Ch

Figure 11-5. MCU_NAVSS_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-14. MCU_NAVSS_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

11.2.5 MCU_NAVSS_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MCU_NAVSS_SEC_STATUS_REG0 is shown in [Figure 11-6](#) and described in [Table 11-16](#).

[Return to Summary Table.](#)

Interrupt Status Register 0

**Table 11-15. MCU_NAVSS_SEC_STATUS_REG0
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1040h

Figure 11-6. MCU_NAVSS_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
UDMAP0_RPC F1_RAMECC_ PEND	UDMAP0_RPC F0_RAMECC_ PEND	UDMAP0_RFF W_RAMECC_P END	UDMAP0_TPC F4_RAMECC_ PEND	UDMAP0_TPC F1_RAMECC_ PEND	UDMAP0_TPC F0_RAMECC_ PEND	UDMAP0_TSTA TE_RAMECC_ PEND	UDMAP0_RPC U_CNTR_RAM ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
UDMAP0_RPC U_SB1_RAME CC_PEND	UDMAP0_RPC U_SB0_RAME CC_PEND	UDMAP0_RPT RCU_CNTR_R AMECC_PEND	UDMAP0_RPT RSB2_RAMEC C_PEND	UDMAP0_RPT RSB1_RAMEC C_PEND	UDMAP0_RPT RSB0_RAMEC C_PEND	UDMAP0_TPT RCU_CNTR_R AMECC_PEND	UDMAP0_TPT RSB2_RAMEC C_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_TPT RSB1_RAMEC C_PEND	UDMAP0_TPT RSB0_RAMEC C_PEND	UDMAP0_RPB UF_PF_RAME CC_PEND	UDMAP0_RPB UF_DF_RAME CC_PEND	UDMAP0_RPB UF_CF_RAME CC_PEND	UDMAP0_RPR Q_RAMECC_P END	UDMAP0_RPC FG_RAMECC_ PEND	UDMAP0_RPS TATE_RAMEC C_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_TPC U_CNTR_RAM ECC_PEND	UDMAP0_TPC U_RAMECC_P END	UDMAP0_TPB UF_PF_RAME CC_PEND	UDMAP0_TPB UF_DF_RAME CC_PEND	UDMAP0_TPB UF_CF_RAME CC_PEND	UDMAP0_TPC FG_RAMECC_ PEND	UDMAP0_TPS TATE_RAMEC C_PEND	ECCAGG_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-16. MCU_NAVSS_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMAP0_RPCF1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf1_amecc_pend
30	UDMAP0_RPCF0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf0_amecc_pend
29	UDMAP0_RFFW_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rffw_amecc_pend
28	UDMAP0_TPCF4_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcf4_amecc_pend
27	UDMAP0_TPCF1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcf1_amecc_pend
26	UDMAP0_TPCF0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcf0_amecc_pend
25	UDMAP0_TSTATE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tstate_amecc_pend
24	UDMAP0_RPCU_CNTR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcu_cntr_amecc_pend
23	UDMAP0_RPCU_SB1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcu_sb1_amecc_pend

Table 11-16. MCU_NAVSS_SEC_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	UDMAP0_RPCU_SB0_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcu_sb0_amecc_pend
21	UDMAP0_RPTRCU_CNT R_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrcu_cntr_amecc_pend
20	UDMAP0_RPTRSB2_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrsb2_amecc_pend
19	UDMAP0_RPTRSB1_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrsb1_amecc_pend
18	UDMAP0_RPTRSB0_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrsb0_amecc_pend
17	UDMAP0_TPTRCU_CNT R_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrcu_cntr_amecc_pend
16	UDMAP0_TPTRSB2_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrsb2_amecc_pend
15	UDMAP0_TPTRSB1_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrsb1_amecc_pend
14	UDMAP0_TPTRSB0_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrsb0_amecc_pend
13	UDMAP0_RPBUFF_PF_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpbuff_pf_amecc_pend
12	UDMAP0_RPBUFF_DF_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpbuff_df_amecc_pend
11	UDMAP0_RPBUFF_CF_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpbuff_cf_amecc_pend
10	UDMAP0_RPRQ_RAMEC C_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rprq_amecc_pend
9	UDMAP0_RPCFG_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcfg_amecc_pend
8	UDMAP0_RPSTATE_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpstate_amecc_pend
7	UDMAP0_TPCU_CNTR_ RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcu_cntr_amecc_pend
6	UDMAP0_TPCU_RAMEC C_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcu_amecc_pend
5	UDMAP0_TPBUFF_PF_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpbuff_pf_amecc_pend
4	UDMAP0_TPBUFF_DF_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpbuff_df_amecc_pend
3	UDMAP0_TPBUFF_CF_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpbuff_cf_amecc_pend
2	UDMAP0_TPCFG_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcfg_amecc_pend
1	UDMAP0_TPSTATE_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpstate_amecc_pend
0	ECCAGG_PEND	R/W1S	0h	Interrupt Pending Status for eccagg_pend

11.2.6 MCU_NAVSS_SEC_STATUS_REG1 Register (Offset = 44h) [reset = 0h]

MCU_NAVSS_SEC_STATUS_REG1 is shown in [Figure 11-7](#) and described in [Table 11-18](#).

Return to [Summary Table](#).

Interrupt Status Register 1

**Table 11-17. MCU_NAVSS_SEC_STATUS_REG1
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1044h

Figure 11-7. MCU_NAVSS_SEC_STATUS_REG1 Register

31	30	29	28	27	26	25	24
UDMASS_INTA0_SR_ECC_PEND	UDMASS_INTA0_IM_ECC_PEND	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_PEND	RINGACC0_ECC_PEND	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_PEND	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_PEND	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_2_PEND	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_1_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_0_PEND	UDMAP0_RRN_GOCC_RAMECC_C_PEND	UDMAP0_TRN_GOCC_RAMECC_C_PEND	UDMAP0_PSIL_TID_RAMECC_PEND	UDMAP0_PSIL_R_RAMECC_PEND	UDMAP0_SDE_C3_RAMECC_PEND	UDMAP0_SDE_C0_RAMECC_PEND	UDMAP0_RDE_C2_RAMECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_RDE_C1_RAMECC_PEND	UDMAP0_RDE_C0_RAMECC_PEND	UDMAP0_REV_TCNTN_RAMECC_PEND	UDMAP0_TEV_TCNTN_RAMECC_PEND	UDMAP0_STS_RAMECC3_PEND	UDMAP0_STS_RAMECC2_PEND	UDMAP0_STS_RAMECC1_PEND	UDMAP0_STS_RAMECC0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_EH_RAMECC_PEND	UDMAP0_PROXY_RAMECC_PEND	UDMAP0_RSTATE_RAMECC_PEND	UDMAP0_RFL_OW1_RAMECC_PEND	UDMAP0_RFL_OW0_RAMECC_PEND	UDMAP0_RPC_F4_RAMECC_PEND	UDMAP0_RPC_F3_RAMECC_PEND	UDMAP0_RPC_F2_RAMECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-18. MCU_NAVSS_SEC_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMASS_INTA0_SR_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_sr_ecc_pend
30	UDMASS_INTA0_IM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_im_ecc_pend
29	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmass_inta0_edc_ctrl_busecc_pend
28	RINGACC0_ECC_PEND	R/W1S	0h	Interrupt Pending Status for ringacc0_ecc_pend
27	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_1_pend
26	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_0_pend

Table 11-18. MCU_NAVSS_SEC_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_B USECC_2_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmap0_edc_ctrl_busecc_2_pend
24	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_B USECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmap0_edc_ctrl_busecc_1_pend
23	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_B USECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmap0_edc_ctrl_busecc_0_pend
22	UDMAP0_RRNGOCC_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rrngocc_amecc_pend
21	UDMAP0_TRNGOCC_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_trngocc_amecc_pend
20	UDMAP0_PSILTID_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_psiltid_amecc_pend
19	UDMAP0_PSILR_RAMECC C_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_psilr_amecc_pend
18	UDMAP0_SDEC3_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sdec3_amecc_pend
17	UDMAP0_SDEC0_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sdec0_amecc_pend
16	UDMAP0_RDEC2_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rdec2_amecc_pend
15	UDMAP0_RDEC1_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rdec1_amecc_pend
14	UDMAP0_RDEC0_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rdec0_amecc_pend
13	UDMAP0_REVTCNTR_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_revtntr_amecc_pend
12	UDMAP0_TEVTCNTR_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tevtntr_amecc_pend
11	UDMAP0_STS_RAMECC 3_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc3_pend
10	UDMAP0_STS_RAMECC 2_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc2_pend
9	UDMAP0_STS_RAMECC 1_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc1_pend
8	UDMAP0_STS_RAMECC 0_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc0_pend
7	UDMAP0_EH_RAMECC_ PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_eh_amecc_pend
6	UDMAP0_PROXY_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_proxy_amecc_pend
5	UDMAP0_RSTATE_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rstate_amecc_pend
4	UDMAP0_RFLOW1_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rflow1_amecc_pend
3	UDMAP0_RFLOW0_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rflow0_amecc_pend
2	UDMAP0_RPCF4_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf4_amecc_pend
1	UDMAP0_RPCF3_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf3_amecc_pend
0	UDMAP0_RPCF2_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf2_amecc_pend

11.2.7 MCU_NAVSS_SEC_STATUS_REG2 Register (Offset = 48h) [reset = 0h]

MCU_NAVSS_SEC_STATUS_REG2 is shown in [Figure 11-8](#) and described in [Table 11-20](#).

Return to [Summary Table](#).

Interrupt Status Register 2

**Table 11-19. MCU_NAVSS_SEC_STATUS_REG2
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1048h

Figure 11-8. MCU_NAVSS_SEC_STATUS_REG2 Register

31	30	29	28	27	26	25	24
NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDG E_DST_BUSECC_C_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDG E_SRC_BUSECC_C_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_DST_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_SRC_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_S DATA_BRIDG E_DST_BUSECC_C_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_S DATA_BRIDG E_SRC_BUSECC_C_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_S DATA_BRIDG E_SRC_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_S DATA_BRIDG E_SRC_BUSECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL BUSECC_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-8. MCU_NAVSS_SEC_STATUS_REG2 Register (continued)

NAVSS_MCU_UDMASS_PSS0_UDMAP0_STRM_SAFE_NAVSS_MCU_UDMASS_PSS0_UDMAP0_STRM_SAFE_EDC_CTRL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSS0_PDMA_MCU1_PSIL_SAFE_NAVSS_MCU_UDMASS_PSS0_PDMA_MCU1_PSIL_SAFE_EDC_CTRL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSS0_PDMA_MCU0_PSIL_SAFE_NAVSS_MCU_UDMASS_PSS0_PDMA_MCU0_PSIL_SAFE_EDC_CTRL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSS0_CPSW0_PSSIL_SAFE_NAVSS_MCU_UDMASS_PSS0_CPSW0_PSSIL_SAFE_EDC_CTRL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSS0_NAVSS_PSSIL_RT_BRIDGE_NAVSS_MCU_UDMASS_PSS0_NAVSS_PSSIL_RT_BRIDGE_EDC_CTRL_BUSECC_PEND	UDMASS_INTA0_GC_ECC_PEND	UDMASS_INTA0_MC_ECC_PEND	UDMASS_INTA0_LC_ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-20. MCU_NAVSS_SEC_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_SAFE_RT_PDMA_MCU1_PSIL_D_DATA_P2P_BRIDGE_SAFE_RT_PDMA_MCU1_PSIL_D_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_rt_pdma_mcu1_psil_d_data_p2p_bridge_safe_rt_pdma_mcu1_psil_d_data_bridge_dst_busecc_pend
30	NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_SAFE_RT_PDMA_MCU1_PSIL_D_DATA_P2P_BRIDGE_SAFE_RT_PDMA_MCU1_PSIL_D_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_rt_pdma_mcu1_psil_d_data_p2p_bridge_safe_rt_pdma_mcu1_psil_d_data_bridge_src_busecc_pend
29	NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_SAFE_RT_CPSW0_PSSIL_D_DATA_P2P_BRIDGE_SAFE_RT_CPSW0_PSSIL_D_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_rt_cpsw0_psil_d_data_p2p_bridge_safe_rt_cpsw0_psil_d_data_bridge_dst_busecc_pend
28	NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSS0_CBASS_DATA_SAFE_RT_CPSW0_PSSIL_D_DATA_P2P_BRIDGE_SAFE_RT_CPSW0_PSSIL_D_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_rt_cpsw0_psil_d_data_p2p_bridge_safe_rt_cpsw0_psil_d_data_bridge_src_busecc_pend

Table 11-20. MCU_NAVSS_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSIL_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_g_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_dst_busecc_pend
26	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSIL_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_g_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_src_busecc_pend
25	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSIL_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_g_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_dst_busecc_pend
24	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSIL_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safe_g_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_src_busecc_pend
23	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cfg_navss_mcu_udmass_psilss0_cfg_edc_ctrl_busecc_pend
22	NAVSS_MCU_UDMASS_PSILSS0_L2P_PSILCFG0_CFGSTRM_NAVSS_MCU_UDMASS_PSILSS0_L2P_PSILCFG0_CFGSTRM_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_edc_ctrl_busecc_pend

Table 11-20. MCU_NAVSS_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21	NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMAPO_CFGSTRM_ NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMAPO_CFGSTRM_ EDC_CTRL_BUSECC C_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmap0_cf gstrm_navss_mcu_udmass_psilss0_l2p_udm ap0_cfgstrm_edc_ctrl_busecc_pend
20	NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMASS_INTA0_MEV T_IN_NAVSS_MCU_ UDMASS_PSISS0_ L2P_UDMASS_INTA 0_MEVT_IN_EDC_C TRL_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmass_in ta0_mevt_in_navss_mcu_udmass_psilss0_l2 p_udmass_inta0_mevt_in_edc_ctrl_busecc_ pend
19	NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMASS_INTA0_CEV T_NAVSS_MCU_UD MASS_PSISS0_L2P UDMASS_INTA0_C EVT_EDC_CTRL_BU SECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmass_in ta0_cevt_navss_mcu_udmass_psilss0_l2p_u dmass_inta0_cevt_edc_ctrl_busecc_pend
18	NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMASS_INTA0_EVT _NAVSS_MCU_UDM ASS_PSISS0_L2P_ UDMASS_INTA0_EV T_EDC_CTRL_BUSE CC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmass_in ta0_evt_navss_mcu_udmass_psilss0_l2p_ud mass_inta0_evt_edc_ctrl_busecc_pend
17	NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMSC_EVT_NAVSS MCU_UDMASS_PSI SS0_L2P_DMSC_EV T_EDC_CTRL_BUSE CC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_dmesc_evt_ navss_mcu_udmass_psilss0_l2p_dmesc_evt_ edc_ctrl_busecc_pend
16	NAVSS_MCU_UDMA SS_PSISS0_L2P_U DMAPO_STRM_NAV SS_MCU_UDMASS_ PSISS0_L2P_UDM APO_STRM_EDC_CT RL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmap0_st rm_navss_mcu_udmass_psilss0_l2p_udmap 0_strm_edc_ctrl_busecc_pend
15	NAVSS_MCU_UDMA SS_PSISS0_L2P_P DMA_MCU1_PSI NAVSS_MCU_UDMAS S_PSISS0_L2P_PD MA_MCU1_PSI EDC_CTRL_BUSECC_P END	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_pdma_mcu 1_psil_navss_mcu_udmass_psilss0_l2p_pd ma_mcu1_psil_edc_ctrl_busecc_pend
14	NAVSS_MCU_UDMA SS_PSISS0_L2P_P DMA_MCU0_PSI NAVSS_MCU_UDMAS S_PSISS0_L2P_PD MA_MCU0_PSI EDC_CTRL_BUSECC_P END	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_pdma_mcu 0_psil_navss_mcu_udmass_psilss0_l2p_pd ma_mcu0_psil_edc_ctrl_busecc_pend

Table 11-20. MCU_NAVSS_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	NAVSS_MCU_UDMASS_PSILSS0_L2P_CPSW0_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_CPSW0_PSIL_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_cpsw0_psil_navss_mcu_udmass_psilss0_l2p_cpsw0_psil_edc_ctrl_busecc_pend
12	NAVSS_MCU_UDMASS_PSILSS0_L2P_NAVSS_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_NAVSS_PSIL_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_navss_psil_navss_mcu_udmass_psilss0_l2p_navss_psil_edc_ctrl_busecc_pend
11	NAVSS_MCU_UDMASS_PSILCFG0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSILCFG0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_edc_ctrl_busecc_pend
10	NAVSS_MCU_UDMASS_PSILSS0_UDMAP0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSILSS0_UDMAP0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_edc_ctrl_busecc_pend
9	NAVSS_MCU_UDMASS_PSILCFG0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSILCFG0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_edc_ctrl_busecc_pend
8	NAVSS_MCU_UDMASS_PSILSS0_UDMAP0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSILSS0_UDMAP0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_edc_ctrl_busecc_pend
7	NAVSS_MCU_UDMASS_PSILSS0_UDMAP0_STRM_SAFEG_NAVSS_MCU_UDMASS_PSILSS0_UDMAP0_STRM_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_udmap0_strm_safeg_navss_mcu_udmass_psilss0_udmap0_strm_safeg_edc_ctrl_busecc_pend
6	NAVSS_MCU_UDMASS_PSILSS0_PDMA_MCU1_PSIL_SAFEG_NAVSS_MCU_UDMASS_PSILSS0_PDMA_MCU1_PSIL_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_edc_ctrl_busecc_pend

Table 11-20. MCU_NAVSS_SEC_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	NAVSS_MCU_UDMASS_PSILSS0_PDMA_MCU0_PSIL_SAFE_G_NAVSS_MCU_UDMASS_PSILSS0_PDMA_MCU0_PSIL_SAFE_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_edc_ctrl_busecc_pend
4	NAVSS_MCU_UDMASS_PSILSS0_CPSW0_PSIL_SAFE_NAVSS_MCU_UDMASS_PSILSS0_CPSW0_PSIL_SAFE_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cpsw0_psil_safeg_navss_mcu_udmass_psilss0_cpsw0_psil_safeg_edc_ctrl_busecc_pend
3	NAVSS_MCU_UDMASS_PSILSS0_NAVSS_PSIL_RT_BRIDGE_NAVSS_MCU_UDMASS_PSILSS0_NAVSS_PSIL_RT_BRIDGE_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_navss_psil_rt_bridge_navss_mcu_udmass_psilss0_navss_psil_rt_bridge_edc_ctrl_busecc_pend
2	UDMASS_INTA0_GC_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_gc_ecc_pend
1	UDMASS_INTA0_MC_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_mc_ecc_pend
0	UDMASS_INTA0_LC_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_lc_ecc_pend

11.2.8 MCU_NAVSS_SEC_STATUS_REG3 Register (Offset = 4Ch) [reset = X]

MCU_NAVSS_SEC_STATUS_REG3 is shown in [Figure 11-9](#) and described in [Table 11-22](#).

Return to [Summary Table](#).

Interrupt Status Register 3

**Table 11-21. MCU_NAVSS_SEC_STATUS_REG3
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 104Ch

Figure 11-9. MCU_NAVSS_SEC_STATUS_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_4 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_3 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_2 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_1 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_0 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_D_DEF EVT_P2P_BRI DGE_D_DEF_E VT_BRIDGE_B USECC_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_D_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_D_ETL 0_BRIDGE_DS T_BUSECC_PE ND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_D_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_D_ETL 0_BRIDGE_SR C_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_S_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_S_ETL 0_BRIDGE_DS T_BUSECC_PE ND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_S_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_S_ETL 0_BRIDGE_SR C_BUSECC_P END	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_2_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_1_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_0_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSIL S_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSIL_S RESP_BRIDG E_DST_BUSEC C_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSIL S_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSIL_S RESP_BRIDG E_SRC_BUSE CC_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_CPSW 0_PSIL_S_RES P_P2P_BRIDG E_SAFEG_RT CPSW0_PSIL S_RESP_BRID GE_DST_BUS ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-9. MCU_NAVSS_SEC_STATUS_REG3 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_S_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI S_RESP_BRID GE_SRC_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSE C_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSE CC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI D_RESP_BRID GE_DST_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI D_RESP_BRID GE_SRC_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMASS_P SISS0_CBASS_R ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_2_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMASS_P SISS0_CBASS_R ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_1_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SISS0_CBASS_R SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMASS_P SISS0_CBASS_R ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-22. MCU_NAVSS_SEC_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_4_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_4_pend
22	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_3_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_3_pend
21	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_2_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_2_pend
20	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_1_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_1_pend

Table 11-22. MCU_NAVSS_SEC_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_P SILSS0_CBASS_ETL_N SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_0_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_0_pend
18	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_D DEF_EVT_P2P_BRIDGE_ D_DEF_EVT_BRIDGE_B USECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_d_def_evt_p2p_bridge_d_def_evt_bridge_busecc_pen d
17	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_DST_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_dst_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_SRC_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_src_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_DST_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_s_etl0_bridge_dst_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_SRC_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_s_etl0_bridge_src_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_CBASS_RESP_ NAVSS_MCU_UDMASS_ P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ EDC_CTRL_BUSECC_2_ PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psil ss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp _scr2_scr_edc_ctrl_busecc_2_pend

Table 11-22. MCU_NAVSS_SEC_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_1_pend
11	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_0_pend
10	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_dst_busecc_pend
9	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_src_busecc_pend
8	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_dst_busecc_pend
7	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_src_busecc_pend

Table 11-22. MCU_NAVSS_SEC_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_dst_busecc_pend
5	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_src_busecc_pend
4	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_D_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_dst_busecc_pend
3	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_D_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_src_busecc_pend
2	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_2_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_2_pend
1	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_1_pend

Table 11-22. MCU_NAVSS_SEC_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_0_pend

11.2.9 MCU_NAVSS_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MCU_NAVSS_SEC_ENABLE_SET_REG0 is shown in [Figure 11-10](#) and described in [Table 11-24](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 11-23.
MCU_NAVSS_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1080h

Figure 11-10. MCU_NAVSS_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
UDMAP0_RPCF1_RAMECC_ENABLE_SET	UDMAP0_RPCF0_RAMECC_ENABLE_SET	UDMAP0_RFFW_RAMECC_ENABLE_SET	UDMAP0_TPCF4_RAMECC_ENABLE_SET	UDMAP0_TPCF1_RAMECC_ENABLE_SET	UDMAP0_TPCF0_RAMECC_ENABLE_SET	UDMAP0_TSTATE_RAMECC_ENABLE_SET	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
UDMAP0_RPCU_SB1_RAMECC_ENABLE_SET	UDMAP0_RPCU_SB0_RAMECC_ENABLE_SET	UDMAP0_RPT_RCU_CNTR_RAMECC_ENABLE_SET	UDMAP0_RPT_RSB2_RAMECC_ENABLE_SET	UDMAP0_RPT_RSB1_RAMECC_ENABLE_SET	UDMAP0_RPT_RSB0_RAMECC_ENABLE_SET	UDMAP0_TPT_RCU_CNTR_RAMECC_ENABLE_SET	UDMAP0_TPT_RSB2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_TPT_RSB1_RAMECC_ENABLE_SET	UDMAP0_TPT_RSB0_RAMECC_ENABLE_SET	UDMAP0_RPB_UF_PF_RAMECC_ENABLE_SET	UDMAP0_RPB_UF_DF_RAMECC_ENABLE_SET	UDMAP0_RPB_UF_CF_RAMECC_ENABLE_SET	UDMAP0_RPR_Q_RAMECC_ENABLE_SET	UDMAP0_RPCFG_RAMECC_ENABLE_SET	UDMAP0_RPSTATE_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_TPCU_CNTR_RAMECC_ENABLE_SET	UDMAP0_TPCU_RAMECC_ENABLE_SET	UDMAP0_TPB_UF_PF_RAMECC_ENABLE_SET	UDMAP0_TPB_UF_DF_RAMECC_ENABLE_SET	UDMAP0_TPB_UF_CF_RAMECC_ENABLE_SET	UDMAP0_TPCFG_RAMECC_ENABLE_SET	UDMAP0_TPS_TATE_RAMECC_ENABLE_SET	ECCAGG_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-24. MCU_NAVSS_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMAP0_RPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf1_ramecc_pend
30	UDMAP0_RPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf0_ramecc_pend
29	UDMAP0_RFFW_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rffw_ramecc_pend
28	UDMAP0_TPCF4_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcf4_ramecc_pend
27	UDMAP0_TPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcf1_ramecc_pend
26	UDMAP0_TPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcf0_ramecc_pend
25	UDMAP0_TSTATE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tstate_ramecc_pend

Table 11-24. MCU_NAVSS_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcu_cntr_amecc_pend
23	UDMAP0_RPCU_SB1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcu_sb1_amecc_pend
22	UDMAP0_RPCU_SB0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcu_sb0_amecc_pend
21	UDMAP0_RPTRCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrcu_cntr_amecc_pend
20	UDMAP0_RPTRSB2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrsb2_amecc_pend
19	UDMAP0_RPTRSB1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrsb1_amecc_pend
18	UDMAP0_RPTRSB0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrsb0_amecc_pend
17	UDMAP0_TPTRCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrcu_cntr_amecc_pend
16	UDMAP0_TPTRSB2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrsb2_amecc_pend
15	UDMAP0_TPTRSB1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrsb1_amecc_pend
14	UDMAP0_TPTRSB0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrsb0_amecc_pend
13	UDMAP0_RPBUF_PF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpbuf_pf_amecc_pend
12	UDMAP0_RPBUF_DF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpbuf_df_amecc_pend
11	UDMAP0_RPBUF_CF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpbuf_cf_amecc_pend
10	UDMAP0_RPRQ_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rprq_amecc_pend
9	UDMAP0_RPCFG_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcfg_amecc_pend
8	UDMAP0_RPSTATE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpstate_amecc_pend
7	UDMAP0_TPCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcu_cntr_amecc_pend
6	UDMAP0_TPCU_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcu_amecc_pend
5	UDMAP0_TPBUF_PF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpbuf_pf_amecc_pend
4	UDMAP0_TPBUF_DF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpbuf_df_amecc_pend
3	UDMAP0_TPBUF_CF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpbuf_cf_amecc_pend
2	UDMAP0_TPCFG_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcfg_amecc_pend
1	UDMAP0_TPSTATE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpstate_amecc_pend
0	ECCAGG_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for eccagg_pend

11.2.10 MCU_NAVSS_SEC_ENABLE_SET_REG1 Register (Offset = 84h) [reset = 0h]

MCU_NAVSS_SEC_ENABLE_SET_REG1 is shown in [Figure 11-11](#) and described in [Table 11-26](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 1

Table 11-25.
MCU_NAVSS_SEC_ENABLE_SET_REG1 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1084h

Figure 11-11. MCU_NAVSS_SEC_ENABLE_SET_REG1 Register

31	30	29	28	27	26	25	24
UDMASS_INTA0_SR_ECC_ENABLE_SET	UDMASS_INTA0_IM_ECC_ENABLE_SET	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_SET	RINGACC0_ECC_ENABLE_SET	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_SET	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_SET	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_2_ENABLE_SET	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_1_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_0_ENABLE_SET	UDMAP0_RRNGOCC_RAMECC_ENABLE_SET	UDMAP0_TRNGOCC_RAMECC_ENABLE_SET	UDMAP0_PSILTID_RAMECC_ENABLE_SET	UDMAP0_PSILR_RAMECC_ENABLE_SET	UDMAP0_SDEC3_RAMECC_ENABLE_SET	UDMAP0_SDEC0_RAMECC_ENABLE_SET	UDMAP0_RDEC2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_RDEC1_RAMECC_ENABLE_SET	UDMAP0_RDEC0_RAMECC_ENABLE_SET	UDMAP0_REVTCNTR_RAMECC_ENABLE_SET	UDMAP0_TEVTCNTR_RAMECC_ENABLE_SET	UDMAP0_STS_RAMECC3_ENABLE_SET	UDMAP0_STS_RAMECC2_ENABLE_SET	UDMAP0_STS_RAMECC1_ENABLE_SET	UDMAP0_STS_RAMECC0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_EHRAMECC_ENABLE_SET	UDMAP0_PROXY_RAMECC_ENABLE_SET	UDMAP0_RSTATE_RAMECC_ENABLE_SET	UDMAP0_RFLOW1_RAMECC_ENABLE_SET	UDMAP0_RFLOW0_RAMECC_ENABLE_SET	UDMAP0_RPCF4_RAMECC_ENABLE_SET	UDMAP0_RPCF3_RAMECC_ENABLE_SET	UDMAP0_RPCF2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-26. MCU_NAVSS_SEC_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMASS_INTA0_SR_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_sr_ecc_pend
30	UDMASS_INTA0_IM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_im_ecc_pend
29	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmass_inta0_edc_ctrl_busecc_pend
28	RINGACC0_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ringacc0_ecc_pend
27	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_1_pend

Table 11-26. MCU_NAVSS_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_0_pend
25	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_2_pend
24	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_1_pend
23	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_0_pend
22	UDMAP0_RRNGOCC_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rrngocc_ramecc_pend
21	UDMAP0_TRNGOCC_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_trngocc_ramecc_pend
20	UDMAP0_PSILTID_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_psiltid_ramecc_pend
19	UDMAP0_PSILR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_psilr_ramecc_pend
18	UDMAP0_SDEC3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sdec3_ramecc_pend
17	UDMAP0_SDEC0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sdec0_ramecc_pend
16	UDMAP0_RDEC2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rdec2_ramecc_pend
15	UDMAP0_RDEC1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rdec1_ramecc_pend
14	UDMAP0_RDEC0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rdec0_ramecc_pend
13	UDMAP0_REVTCNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_revtntr_ramecc_pend
12	UDMAP0_TEVTCNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tevtntr_ramecc_pend
11	UDMAP0_STS_RAMECC3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc3_pend
10	UDMAP0_STS_RAMECC2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc2_pend
9	UDMAP0_STS_RAMECC1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc1_pend
8	UDMAP0_STS_RAMECC0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc0_pend
7	UDMAP0_EH_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_eh_ramecc_pend
6	UDMAP0_PROXY_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_proxy_ramecc_pend
5	UDMAP0_RSTATE_RAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rstate_ramecc_pend
4	UDMAP0_RFLOW1_RAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rflow1_ramecc_pend
3	UDMAP0_RFLOW0_RAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rflow0_ramecc_pend
2	UDMAP0_RPCF4_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf4_ramecc_pend

Table 11-26. MCU_NAVSS_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UDMAP0_RPCF3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf3_ramecc_pend
0	UDMAP0_RPCF2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf2_ramecc_pend

11.2.11 MCU_NAVSS_SEC_ENABLE_SET_REG2 Register (Offset = 88h) [reset = 0h]

MCU_NAVSS_SEC_ENABLE_SET_REG2 is shown in [Figure 11-12](#) and described in [Table 11-28](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 2

Table 11-27.
MCU_NAVSS_SEC_ENABLE_SET_REG2 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1088h

Figure 11-12. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register

31	30	29	28	27	26	25	24
NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL_D DATA_P2P_BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDGE E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL_D DATA_P2P_BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDGE E_SRC_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE A_P2P_BRIDGE_SAFE E_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDGE GE_DST_BUS ECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE A_P2P_BRIDGE_SAFE E_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDGE GE_SRC_BUS ECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE A_P2P_BRIDGE_SAFE E_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDGE GE_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE A_P2P_BRIDGE_SAFE E_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDGE GE_SRC_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE A_P2P_BRIDGE_SAFE E_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDGE GE_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE A_P2P_BRIDGE_SAFE E_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDGE GE_SRC_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_L2P_CFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-12. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_UDMAP0_ STRM_SAFEG _NAVSS_MCU _UDMASS_PSI LSS0_UDMAP0_ STRM_SAFE G_EDC_CTRL_ BUSECC_ENA BLE_SET	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU1_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU1_PSI SAFEG_EDC_ CTRL_BUSEC C_ENABLE_SE T	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU0_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU0_PSI SAFEG_EDC_ CTRL_BUSEC C_ENABLE_SE T	NAVSS_MCU_UDMASS_PSI SS0_CPSW0_P SIL_SAFEG_N AVSS_MCU_U DMASS_PSILS S0_CPSW0_PS IL_SAFEG_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS_MCU_UDMASS_PSI SS0_NAVSS_P SIL_RT_BRIDG E_NAVSS_MC U_UDMASS_P SILSS0_NAVS S_PSI_RT_BR IDGE_EDC_CT RL_BUSECC_E NABLE_SET	UDMASS_INTA 0_GC_ECC_EN ABLE_SET	UDMASS_INTA 0_MC_ECC_E NABLE_SET	UDMASS_INTA 0_LC_ECC_EN ABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-28. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFEG_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_DST_BUSECC_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_dst_busecc_pend
30	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFEG_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_SRC_BUSECC_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_src_busecc_pend
29	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE _SAFEG_RT_CPSW0_PS IL_D_DATA_BRIDGE_DS T_BUSECC_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_dst_busecc_pend
28	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE _SAFEG_RT_CPSW0_PS IL_D_DATA_BRIDGE_SR C_BUSECC_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_src_busecc_pend

Table 11-28. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_dst_busecc_pend
26	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_src_busecc_pend
25	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_dst_busecc_pend
24	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_src_busecc_pend
23	NAVSS_MCU_UDMASS_PSilSS0_CFG_NAVSS_MCU_UDMASS_PSilSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cfg_navss_mcu_udmass_psilss0_cfg_edc_ctrl_busecc_pend
22	NAVSS_MCU_UDMASS_PSilSS0_I2P_PSilCFG0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_I2P_PSilCFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_i2p_psilcfg0_cfgstrm_navss_mcu_udmass_psilss0_i2p_psilcfg0_cfgstrm_edc_ctrl_busecc_pend
21	NAVSS_MCU_UDMASS_PSilSS0_I2P_UDMAP0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_I2P_UDMAP0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_i2p_udmap0_cfgstrm_navss_mcu_udmass_psilss0_i2p_udmap0_cfgstrm_edc_ctrl_busecc_pend

Table 11-28. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NAVSS_MCU_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_MEVT_IN_NAVSS_ MCU_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_MEVT_IN_EDC_CTRL_B USECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_mevt_in_navss_mcu_u dmass_psilss0_l2p_udmass_inta0_mevt_in_edc_ctrl_busecc_pe nd
19	NAVSS_MCU_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_CEVN_NAVSS_M CU_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_CEVN_EDC_CTRL_B USECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_cevt_navss_mcu_u dmass_psilss0_l2p_udmass_inta0_cevt_edc_ctrl_busecc_pend
18	NAVSS_MCU_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_EVT_NAVSS_MCU UDMASS_P SILSS0_L2P_UDMASS_ INTA0_EVT_ EDC_CTRL_BUSECC_E NABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_evt_navss_mcu_ud mass_psilss0_l2p_udmass_inta0_evt_edc_ctrl_busecc_pend
17	NAVSS_MCU_UDMASS_P SILSS0_L2P_DMSC_EV T_NAVSS_MCU_UDMAS S_P SILSS0_L2P_DMSC_ EVT_EDC_CTRL_BUSECC ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_dmesc_evt_navss_mcu_udmass_p silss0_l2p_dmesc_evt_edc_ctrl_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_L2P_UDMAP0_ STRM_NAVSS_MCU_UD MASS_P SILSS0_L2P_UD MAP0_STRM_EDC_CTRL_ BUSECC_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmap0_strm_navss_mcu_udmas s_psilss0_l2p_udmap0_strm_edc_ctrl_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_L2P_PDMA_M CU1_P SIL_NAVSS_MCU_ UDMASS_P SILSS0_L2P_ PDMA_MCU1_P SIL_ED C_CTRL_BUSECC_ENAB LE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu1_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu1_psil_edc_ctrl_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_L2P_PDMA_M CU0_P SIL_NAVSS_MCU_ UDMASS_P SILSS0_L2P_ PDMA_MCU0_P SIL_ED C_CTRL_BUSECC_ENAB LE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu0_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu0_psil_edc_ctrl_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_L2P_CPSW0_P SIL_NAVSS_MCU_UDMA SS_P SILSS0_L2P_CPSW 0_P SIL_EDC_CTRL_B USECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_cpsw0_psil_navss_mcu_udmass_ psilss0_l2p_cpsw0_psil_edc_ctrl_busecc_pend
12	NAVSS_MCU_UDMASS_P SILSS0_L2P_NAVSS_P SIL_NAVSS_MCU_UDMA SS_P SILSS0_L2P_NAVS S_P SIL_EDC_CTRL_B USECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_navss_psil_navss_mcu_udmass_ psilss0_l2p_navss_psil_edc_ctrl_busecc_pend

Table 11-28. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_edc_ctrl_busecc_pend
10	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_edc_ctrl_busecc_pend
9	NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_edc_ctrl_busecc_pend
8	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_edc_ctrl_busecc_pend
7	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_STRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_STRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_udmap0_strm_safeg_navss_mcu_udmass_psilss0_udmap0_strm_safeg_edc_ctrl_busecc_pend
6	NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU1_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU1_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_edc_ctrl_busecc_pend
5	NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU0_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU0_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_edc_ctrl_busecc_pend
4	NAVSS_MCU_UDMASS_PSilSS0_CPSW0_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_CPSW0_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cpsw0_psil_safeg_navss_mcu_udmass_psilss0_cpsw0_psil_safeg_edc_ctrl_busecc_pend
3	NAVSS_MCU_UDMASS_PSilSS0_NAVSS_PSil_RT_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_NAVSS_PSil_RT_BRIDGE_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_navss_psil_rt_bridge_navss_mcu_udmass_psilss0_navss_psil_rt_bridge_edc_ctrl_busecc_pend

Table 11-28. MCU_NAVSS_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UDMASS_INTA0_GC_EC_C_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_gc_ecc_pend
1	UDMASS_INTA0_MC_EC_C_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_mc_ecc_pend
0	UDMASS_INTA0_LC_EC_C_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_lc_ecc_pend

11.2.12 MCU_NAVSS_SEC_ENABLE_SET_REG3 Register (Offset = 8Ch) [reset = X]

MCU_NAVSS_SEC_ENABLE_SET_REG3 is shown in [Figure 11-13](#) and described in [Table 11-30](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 3

Table 11-29.
MCU_NAVSS_SEC_ENABLE_SET_REG3 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 108Ch

Figure 11-13. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_4 _ENABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_3 _ENABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_2 _ENABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_1 _ENABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_0 _ENABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_D_DEF EVT_P2P_BRI DGE_D_DEF_E VT_BRIDGE_B USECC_ENAB LE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_D_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_D_ETL 0_BRIDGE_DS T_BUSECC_E NABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_D_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_D_ETL 0_BRIDGE_SR C_BUSECC_E NABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_S_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_S_ETL 0_BRIDGE_DS T_BUSECC_E NABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFEG RT_PDMA_M CU1_PSIL_S_E TL0_P2P_BRID GE_SAFEG_R T_PDMA_MCU 1_PSIL_S_ETL 0_BRIDGE_SR C_BUSECC_E NABLE_SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_2_ENABLE _SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_1_ENABLE _SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_0_ENABLE _SET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSIL S_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSIL_S RESP_BRIDG E_DST_BUSEC C_ENABLE_SE T	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSIL S_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSIL_S RESP_BRIDG E_SRC_BUSE CC_ENABLE_S ET	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_CPSW 0_PSIL_S_RES P_P2P_BRIDG E_SAFEG_RT CPSW0_PSIL S_RESP_BRID GE_DST_BUS ECC_ENABLE SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-13. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register (continued)

NAVSS_MCU_UDMASS_PSS0_CBASS_R ESP_NAVSS_MCU_UDMASS_PSS0_CBASS_R SS_RESP_SAFEG_RT_CPSW0_PSSIL_S_RESP_P2P_BRIDG E_SAFEG_RT_CPSW0_PSSIL_S_RESP_BRIDGE_SRC_BUS ECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_R ESP_NAVSS_MCU_UDMASS_PSS0_CBASS_R SS_RESP_SAFEG_RT_PDMA_MCU1_PSSIL_D_RESP_P2P_BRIDGE_SAFE_G_RT_PDMA_MCU1_PSSIL_D_RESP_BRIDGE_DST_BUSECC_ENABLE_SE T	NAVSS_MCU_UDMASS_PSS0_CBASS_R ESP_NAVSS_MCU_UDMASS_PSS0_CBASS_R SS_RESP_SAFEG_RT_PDMA_MCU1_PSSIL_D_RESP_P2P_BRIDGE_SAFE_G_RT_PDMA_MCU1_PSSIL_D_RESP_BRIDGE_DST_BUSECC_ENABLE_S ET	NAVSS_MCU_UDMASS_PSS0_CBASS_R ESP_NAVSS_MCU_UDMASS_PSS0_CBASS_R SS_RESP_SAFEG_RT_CPSW0_PSSIL_D_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_R ESP_NAVSS_MCU_UDMASS_PSS0_CBASS_R SS_RESP_SAFEG_RT_CPSW0_PSSIL_D_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBASS_D SS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_DATA_SC R1_SCR_EDC_CTRL_BUSECC_2_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBASS_D SS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_DATA_SC R1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBASS_D SS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_DATA_SC R1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-30. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_EDC_CTRL_BUSECC_4_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_edc_ctrl_busecc_4_pend
22	NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_EDC_CTRL_BUSECC_3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_edc_ctrl_busecc_3_pend
21	NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_edc_ctrl_busecc_2_pend
20	NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_PSSILSS0_CBASS_ETL_SCR3_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3_scr_edc_ctrl_busecc_1_pend

Table 11-30. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_P SILSS0_CBASS_ETL_N SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_0_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_0_pend
18	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_D DEF_EVT_P2P_BRIDGE_ D_DEF_EVT_BRIDGE_B USECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_d_def_evt_p2p_bridge_d_def_evt_bridge_busecc_pen d
17	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_DST_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_dst_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_src_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_DST_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_dst_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_src_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_CBASS_RESP_ NAVSS_MCU_UDMASS_ PSILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ EDC_CTRL_BUSECC_2_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psil ss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp _scr2_scr_edc_ctrl_busecc_2_pend

Table 11-30. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_1_pend
11	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_0_pend
10	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_dst_busecc_pend
9	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_src_busecc_pend
8	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_dst_busecc_pend
7	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_src_busecc_pend

Table 11-30. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_dst_busecc_pend
5	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_src_busecc_pend
4	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_D_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_dst_busecc_pend
3	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_D_RESP_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_src_busecc_pend
2	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_2_pend
1	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_1_pend

Table 11-30. MCU_NAVSS_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_0_pend

11.2.13 MCU_NAVSS_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MCU_NAVSS_SEC_ENABLE_CLR_REG0 is shown in [Figure 11-14](#) and described in [Table 11-32](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 11-31.
MCU_NAVSS_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 10C0h

Figure 11-14. MCU_NAVSS_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
UDMAP0_RPCF1_RAMECC_ENABLE_CLR	UDMAP0_RPCF0_RAMECC_ENABLE_CLR	UDMAP0_RFFW_RAMECC_ENABLE_CLR	UDMAP0_TPCF4_RAMECC_ENABLE_CLR	UDMAP0_TPCF1_RAMECC_ENABLE_CLR	UDMAP0_TPCF0_RAMECC_ENABLE_CLR	UDMAP0_TSTATE_RAMECC_ENABLE_CLR	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
UDMAP0_RPCU_SB1_RAMECC_ENABLE_CLR	UDMAP0_RPCU_SB0_RAMECC_ENABLE_CLR	UDMAP0_RPT_RCU_CNTR_RAMECC_ENABLE_CLR	UDMAP0_RPT_RSB2_RAMECC_ENABLE_CLR	UDMAP0_RPT_RSB1_RAMECC_ENABLE_CLR	UDMAP0_RPT_RSB0_RAMECC_ENABLE_CLR	UDMAP0_TPT_RCU_CNTR_RAMECC_ENABLE_CLR	UDMAP0_TPT_RSB2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
UDMAP0_TPT_RSB1_RAMECC_ENABLE_CLR	UDMAP0_TPT_RSB0_RAMECC_ENABLE_CLR	UDMAP0_RPB_UF_PF_RAMECC_ENABLE_CLR	UDMAP0_RPB_UF_DF_RAMECC_ENABLE_CLR	UDMAP0_RPB_UF_CF_RAMECC_ENABLE_CLR	UDMAP0_RPR_Q_RAMECC_ENABLE_CLR	UDMAP0_RPCFG_RAMECC_ENABLE_CLR	UDMAP0_RPSTATE_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
UDMAP0_TPCU_CNTR_RAMECC_ENABLE_CLR	UDMAP0_TPCU_RAMECC_ENABLE_CLR	UDMAP0_TPB_UF_PF_RAMECC_ENABLE_CLR	UDMAP0_TPB_UF_DF_RAMECC_ENABLE_CLR	UDMAP0_TPB_UF_CF_RAMECC_ENABLE_CLR	UDMAP0_TPCFG_RAMECC_ENABLE_CLR	UDMAP0_TPSTATE_RAMECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-32. MCU_NAVSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMAP0_RPCF1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf1_amecc_pend
30	UDMAP0_RPCF0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf0_amecc_pend
29	UDMAP0_RFFW_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rffw_amecc_pend
28	UDMAP0_TPCF4_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcf4_amecc_pend
27	UDMAP0_TPCF1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcf1_amecc_pend
26	UDMAP0_TPCF0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcf0_amecc_pend
25	UDMAP0_TSTATE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tstate_amecc_pend

Table 11-32. MCU_NAVSS_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcu_cntr_amecc_pend
23	UDMAP0_RPCU_SB1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcu_sb1_amecc_pend
22	UDMAP0_RPCU_SB0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcu_sb0_amecc_pend
21	UDMAP0_RPTRCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrcu_cntr_amecc_pend
20	UDMAP0_RPTRSB2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrsb2_amecc_pend
19	UDMAP0_RPTRSB1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrsb1_amecc_pend
18	UDMAP0_RPTRSB0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrsb0_amecc_pend
17	UDMAP0_TPTRCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrcu_cntr_amecc_pend
16	UDMAP0_TPTRSB2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrsb2_amecc_pend
15	UDMAP0_TPTRSB1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrsb1_amecc_pend
14	UDMAP0_TPTRSB0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrsb0_amecc_pend
13	UDMAP0_RPBUF_PF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdbuf_pf_amecc_pend
12	UDMAP0_RPBUF_DF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdbuf_df_amecc_pend
11	UDMAP0_RPBUF_CF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdbuf_cf_amecc_pend
10	UDMAP0_RPRQ_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rprq_amecc_pend
9	UDMAP0_RPCFG_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcfg_amecc_pend
8	UDMAP0_RPSTATE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpstate_amecc_pend
7	UDMAP0_TPCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcu_cntr_amecc_pend
6	UDMAP0_TPCU_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcu_amecc_pend
5	UDMAP0_TPBUF_PF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tdbuf_pf_amecc_pend
4	UDMAP0_TPBUF_DF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tdbuf_df_amecc_pend
3	UDMAP0_TPBUF_CF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tdbuf_cf_amecc_pend
2	UDMAP0_TPCFG_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcfg_amecc_pend
1	UDMAP0_TPSTATE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpstate_amecc_pend
0	ECCAGG_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for eccagg_pend

11.2.14 MCU_NAVSS_SEC_ENABLE_CLR_REG1 Register (Offset = C4h) [reset = 0h]

MCU_NAVSS_SEC_ENABLE_CLR_REG1 is shown in [Figure 11-15](#) and described in [Table 11-34](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 1

Table 11-33.
MCU_NAVSS_SEC_ENABLE_CLR_REG1 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 10C4h

Figure 11-15. MCU_NAVSS_SEC_ENABLE_CLR_REG1 Register

31	30	29	28	27	26	25	24
UDMASS_INTA0_SR_ECC_ENABLE_CLR	UDMASS_INTA0_IM_ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_CLR	RINGACC0_ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_CLR	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_CLR	NAVSS_MCU_UDMASS_UDMASS_AP0_EDC_CTRL_BUSECC_2_ENABLE_CLR	NAVSS_MCU_UDMASS_UDMASS_AP0_EDC_CTRL_BUSECC_1_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_UDMASS_AP0_EDC_CTRL_BUSECC_0_ENABLE_CLR	UDMAP0_RRNGOCC_RAMECC_ENABLE_CLR	UDMAP0_TRNGOCC_RAMECC_ENABLE_CLR	UDMAP0_PSILTID_RAMECC_ENABLE_CLR	UDMAP0_PSILR_RAMECC_ENABLE_CLR	UDMAP0_SDEC3_RAMECC_ENABLE_CLR	UDMAP0_SDEC0_RAMECC_ENABLE_CLR	UDMAP0_RDEC2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
UDMAP0_RDEC1_RAMECC_ENABLE_CLR	UDMAP0_RDEC0_RAMECC_ENABLE_CLR	UDMAP0_REVTCNTR_RAMECC_ENABLE_CLR	UDMAP0_TEVTCNTR_RAMECC_ENABLE_CLR	UDMAP0_STSRAMECC3_ENABLE_CLR	UDMAP0_STSRAMECC2_ENABLE_CLR	UDMAP0_STSRAMECC1_ENABLE_CLR	UDMAP0_STSRAMECC0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
UDMAP0_EHRAMECC_ENABLE_CLR	UDMAP0_PROXY_RAMECC_ENABLE_CLR	UDMAP0_RSTATE_RAMECC_ENABLE_CLR	UDMAP0_RFLOW1_RAMECC_ENABLE_CLR	UDMAP0_RFLOW0_RAMECC_ENABLE_CLR	UDMAP0_RPCF4_RAMECC_ENABLE_CLR	UDMAP0_RPCF3_RAMECC_ENABLE_CLR	UDMAP0_RPCF2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-34. MCU_NAVSS_SEC_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMASS_INTA0_SR_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_sr_ecc_pend
30	UDMASS_INTA0_IM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_im_ecc_pend
29	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmass_inta0_edc_ctrl_busecc_pend
28	RINGACC0_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ringacc0_ecc_pend
27	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_1_pend

Table 11-34. MCU_NAVSS_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_0_pend
25	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_2_pend
24	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_1_pend
23	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_0_pend
22	UDMAP0_RRNGOCC_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rrngocc_amecc_pend
21	UDMAP0_TRNGOCC_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_trngocc_amecc_pend
20	UDMAP0_PSILTID_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_psiltid_amecc_pend
19	UDMAP0_PSILR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_psilr_amecc_pend
18	UDMAP0_SDEC3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sdec3_amecc_pend
17	UDMAP0_SDEC0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sdec0_amecc_pend
16	UDMAP0_RDEC2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdec2_amecc_pend
15	UDMAP0_RDEC1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdec1_amecc_pend
14	UDMAP0_RDEC0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdec0_amecc_pend
13	UDMAP0_REVTCTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_revtctr_amecc_pend
12	UDMAP0_TEVTCTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tevtctr_amecc_pend
11	UDMAP0_STS_RAMECC3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc3_pend
10	UDMAP0_STS_RAMECC2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc2_pend
9	UDMAP0_STS_RAMECC1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc1_pend
8	UDMAP0_STS_RAMECC0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc0_pend
7	UDMAP0_EH_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_eh_amecc_pend
6	UDMAP0_PROXY_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_proxy_amecc_pend
5	UDMAP0_RSTATE_RAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rstate_amecc_pend
4	UDMAP0_RFLOW1_RAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rflow1_amecc_pend
3	UDMAP0_RFLOW0_RAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rflow0_amecc_pend
2	UDMAP0_RPCF4_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf4_amecc_pend

Table 11-34. MCU_NAVSS_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UDMAP0_RPCF3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf3_ramecc_pend
0	UDMAP0_RPCF2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf2_ramecc_pend

11.2.15 MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register (Offset = 283810C8h) [reset = 0h]

MCU_NAVSS_SEC_ENABLE_CLR_REG2 is shown in [Figure 11-16](#) and described in [Table 11-36](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 2

Table 11-35.
MCU_NAVSS_SEC_ENABLE_CLR_REG2 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 10C8h

Figure 11-16. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register

31	30	29	28	27	26	25	24
NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_PDMA _MCU1_PSIL_ D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_ MCU1_PSIL_D _DATA_BRIDG E_DST_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_PDMA _MCU1_PSIL_ D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_ MCU1_PSIL_D _DATA_BRIDG E_SRC_BUSE CC_ENABLE_C LR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_CPSW 0_PSIL_D_DAT A_P2P_BRIDG E_SAFEGR_RT_ CPSW0_PSIL_ D_DATA_BRID GE_DST_BUS ECC_ENABLE_ CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_CPSW 0_PSIL_D_DAT A_P2P_BRIDG E_SAFEGR_RT_ CPSW0_PSIL_ D_DATA_BRID GE_SRC_BUS ECC_ENABLE_ CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_PDMA _MCU1_PSIL_ S_DATA_P2P BRIDGE_SAFE G_RT_PDMA_ MCU1_PSIL_S _DATA_BRIDG E_DST_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_PDMA _MCU1_PSIL_ S_DATA_P2P BRIDGE_SAFE G_RT_PDMA_ MCU1_PSIL_S _DATA_BRIDG E_SRC_BUSE CC_ENABLE_C LR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_CPSW 0_PSIL_S_DAT A_P2P_BRIDG E_SAFEGR_RT_ CPSW0_PSIL_ S_DATA_BRID GE_DST_BUS ECC_ENABLE_ CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS_ PSILSS0_CBA SS_DATA_SAF EG_RT_CPSW 0_PSIL_S_DAT A_P2P_BRIDG E_SAFEGR_RT_ CPSW0_PSIL_ S_DATA_BRID GE_SRC_BUS ECC_ENABLE_ CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSI SS0_CFG_NAV SS_MCU_UDM ASS_PSISS0_ CFG_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_PSI CFG0_CFGST RM_NAVSS_M CU_UDMASS_ PSILSS0_L2P PSILCFG0_CF GSTRM_EDC CTRL_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_L2P_UDM AP0_CFGSTR M_NAVSS_MC U_UDMASS_P SILSS0_L2P_U DMAPO_CFGS TRM_EDC_CT RL_BUSECC_E NABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_UDM ASS_INTA0_M EVT_IN_NAVS S_MCU_UDMA SS_PSISS0_L 2P_UDMASS_I NTA0_MEVT_I N_EDC_CTRL_ BUSECC_ENA BLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_UDM ASS_INTA0_EV T_NAVSS_MC U_UDMASS_P PSILSS0_L2P UDMASS_INTA 0_EVT_EDC_CT CTRL_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_L2P_UDM ASS_INTA0_EV T_NAVSS_MC U_UDMASS_P S_PSISS0_L2 P_DMSC_EVT_ EDC_CTRL_BU SECC_ENABL E_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_DMS C_EVT_NAVSS _MCU_UDMAS S_PSISS0_L2 P_DMSC_EVT_ EDC_CTRL_BU SECC_ENABL E_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_UDM AP0_STRM_NA VSS_MCU_UD MASS_PSISS 0_L2P_UDMAP 0_STRM_EDC CTRL_BUSEC C_ENABLE_CL R
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSI SS0_L2P_PDM A_MCU1_PSIL _NAVSS_MCU_ UDMASS_PSI LSS0_L2P_PD MA_MCU1_PSI L_EDC_CTRL_ BUSECC_ENA BLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_PDM A_MCU0_PSIL _NAVSS_MCU_ UDMASS_PSI LSS0_L2P_PD MA_MCU0_PSI L_EDC_CTRL_ BUSECC_ENA BLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_CPS W0_PSIL_NAV SS_MCU_UDM ASS_PSISS0_ L2P_CPSW0_P SIL_EDC_CTL L_BUSECC_EN ABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_L2P_NAV SS_PSIL_NAV SS_MCU_UDM ASS_PSISS0_ L2P_NAVSS_P SIL_EDC_CTL L_BUSECC_EN ABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_PSIICFG 0_CFGGSTRM BRIDGE_NAVS S_MCU_UDMA SS_PSISS0_P SILCFG0_CFG STRM_BRIDGE _EDC_CTRL_B USECC_ENAB LE_CLR	NAVSS_MCU_UDMASS_PSI SS0_UDMAPO CFGGSTRM_BRI DGE_NAVSS_ MCU_UDMASS _PSISS0_P MAP0_CFGST RM_BRIDGE_E DC_CTRL_BUS ECC_ENABLE_ CLR	NAVSS_MCU_UDMASS_PSI SS0_PSIICFG 0_CFGGSTRM SAFEGR_NAVS S_MCU_UDMA SS_PSISS0_P SILCFG0_CFG STRM_SAFEGR _EDC_CTRL_B USECC_ENAB LE_CLR	NAVSS_MCU_UDMASS_PSI SS0_UDMAPO CFGGSTRM_SA FEG_NAVSS_ MCU_UDMASS _PSISS0_UD MAP0_CFGST RM_SAFEGR_E DC_CTRL_BUS ECC_ENABLE_ CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0

Figure 11-16. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_UDMAP0_ STRM_SAFE G_EDC_CTRL_ BUSECC_ENA BLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU1_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU1_PSI SAFE_EDC_ CTRL_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU0_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU0_PSI SAFE_EDC_ CTRL_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_CPSW0_P SIL_SAFE_N AVSS_MCU_U DMASS_PSIL S0_CPSW0_PS IL_SAFE_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS_MCU_UDMASS_PSI SS0_NAVSS_P SIL_RT_BRIDG E_NAVSS_MC U_UDMASS_P SILSS0_NAVS S_PSI_RT_BR IDGE_EDC_CT RL_BUSECC_E NABLE_CLR	UDMASS_INTA 0_GC_ECC_EN ABLE_CLR	UDMASS_INTA 0_MC_ECC_E NABLE_CLR	UDMASS_INTA 0_LC_ECC_EN ABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-36. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ SAFE_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFE_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_DST_BUSECC_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_dst_busecc_pend
30	NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ SAFE_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFE_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_SRC_BUSECC_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_src_busecc_pend
29	NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ SAFE_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE SAFE_RT_CPSW0_PS IL_D_DATA_BRIDGE_DS T_BUSECC_ENABLE_CL R	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_dst_busecc_pend
28	NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI SS0_CBASS_DATA_ SAFE_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE SAFE_RT_CPSW0_PS IL_D_DATA_BRIDGE_SR C_BUSECC_ENABLE_CL R	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_src_busecc_pend

Table 11-36. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_dst_busecc_pend
26	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_src_busecc_pend
25	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_dst_busecc_pend
24	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_src_busecc_pend
23	NAVSS_MCU_UDMASS_PSilSS0_CFG_NAVSS_MCU_UDMASS_PSilSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cfg_navss_mcu_udmass_psilss0_cfg_edc_ctrl_busecc_pend
22	NAVSS_MCU_UDMASS_PSilSS0_L2P_PSilCFG0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_L2P_PSilCFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_edc_ctrl_busecc_pend
21	NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMAP0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMAP0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmap0_cfgstrm_navss_mcu_udmass_psilss0_l2p_udmap0_cfgstrm_edc_ctrl_busecc_pend

Table 11-36. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMASS_INTA0_MEVT_IN_NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMASS_INTA0_MEVT_IN_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_mevt_in_navss_mcu_u_udmass_psilss0_l2p_udmass_inta0_mevt_in_edc_ctrl_busecc_pend
19	NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMASS_INTA0_CEV_T_NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMASS_INTA0_CEV_T_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_cevt_navss_mcu_u_dmass_psilss0_l2p_udmass_inta0_cevt_edc_ctrl_busecc_pend
18	NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMASS_INTA0_EVT_NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMASS_INTA0_EVT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_evt_navss_mcu_u_dmass_psilss0_l2p_udmass_inta0_evt_edc_ctrl_busecc_pend
17	NAVSS_MCU_UDMASS_PSilSS0_L2P_DMSC_EVT_NAVSS_MCU_UDMASS_PSilSS0_L2P_DMSC_EVT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_dmesc_evt_navss_mcu_udmass_psilss0_l2p_dmesc_evt_edc_ctrl_busecc_pend
16	NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMAP0_STRM_NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMAP0_STRM_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmap0_strm_navss_mcu_udmass_psilss0_l2p_udmap0_strm_edc_ctrl_busecc_pend
15	NAVSS_MCU_UDMASS_PSilSS0_L2P_PDMA_MCU1_PSil_NAVSS_MCU_UDMASS_PSilSS0_L2P_PDMA_MCU1_PSil_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu1_psil_navss_mcu_udmass_psilss0_l2p_pdma_mcu1_psil_edc_ctrl_busecc_pend
14	NAVSS_MCU_UDMASS_PSilSS0_L2P_PDMA_MCU0_PSil_NAVSS_MCU_UDMASS_PSilSS0_L2P_PDMA_MCU0_PSil_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu0_psil_navss_mcu_udmass_psilss0_l2p_pdma_mcu0_psil_edc_ctrl_busecc_pend
13	NAVSS_MCU_UDMASS_PSilSS0_L2P_CPSW0_PSil_NAVSS_MCU_UDMASS_PSilSS0_L2P_CPSW0_PSil_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_cpsw0_psil_navss_mcu_udmass_psilss0_l2p_cpsw0_psil_edc_ctrl_busecc_pend
12	NAVSS_MCU_UDMASS_PSilSS0_L2P_NAVSS_PSil_NAVSS_MCU_UDMASS_PSilSS0_L2P_NAVSS_PSil_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_navss_psil_navss_mcu_udmass_psilss0_l2p_navss_psil_edc_ctrl_busecc_pend

Table 11-36. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_edc_ctrl_busecc_pend
10	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_edc_ctrl_busecc_pend
9	NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_edc_ctrl_busecc_pend
8	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_edc_ctrl_busecc_pend
7	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_STRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_STRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_udmap0_strm_safeg_navss_mcu_udmass_psilss0_udmap0_strm_safeg_edc_ctrl_busecc_pend
6	NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU1_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU1_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_edc_ctrl_busecc_pend
5	NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU0_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU0_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_edc_ctrl_busecc_pend
4	NAVSS_MCU_UDMASS_PSilSS0_CPSW0_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_CPSW0_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cpsw0_psil_safeg_navss_mcu_udmass_psilss0_cpsw0_psil_safeg_edc_ctrl_busecc_pend
3	NAVSS_MCU_UDMASS_PSilSS0_NAVSS_PSil_RT_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_NAVSS_PSil_RT_BRIDGE_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_navss_psil_rt_bridge_navss_mcu_udmass_psilss0_navss_psil_rt_bridge_edc_ctrl_busecc_pend

Table 11-36. MCU_NAVSS_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UDMASS_INTA0_GC_EC_C_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_gc_ecc_pend
1	UDMASS_INTA0_MC_EC_C_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_mc_ecc_pend
0	UDMASS_INTA0_LC_EC_C_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_lc_ecc_pend

11.2.16 MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register (Offset = CCh) [reset = X]

MCU_NAVSS_SEC_ENABLE_CLR_REG3 is shown in [Figure 11-17](#) and described in [Table 11-38](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 3

Table 11-37.
MCU_NAVSS_SEC_ENABLE_CLR_REG3 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 10CCh

Figure 11-17. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_4_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_3_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_2_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_1_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_0_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_D_DEF_EVT_P2P_BRIDGE_D_DEF_EVT_BRIDGE_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_D_ETL0_BRIDGE_DSRT_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_D_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRT_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0

Figure 11-17. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_S_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI S_RESP_BRID GE_SRC_BUS ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSEC C_ENABLE_C LR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI D_RESP_BRID GE_DST_BUS ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI D_RESP_BRID GE_SRC_BUS ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SS0_CBASS_D SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_2_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SS0_CBASS_D SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_1_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SS0_CBASS_D SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-38. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_4_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_4_pend
22	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_3_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_3_pend
21	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_2_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_2_pend
20	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_1_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_1_pend

Table 11-38. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_P SILSS0_CBASS_ETL_N SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_0_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_0_pend
18	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_D DEF_EVT_P2P_BRIDGE_ D_DEF_EVT_BRIDGE_B USECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_d_def_evt_p2p_bridge_d_def_evt_bridge_busecc_pen d
17	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_DST_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_dst_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_src_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_DST_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_dst_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_src_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_CBASS_RESP_ NAVSS_MCU_UDMASS_ P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ EDC_CTRL_BUSECC_2_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psil ss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp _scr2_scr_edc_ctrl_busecc_2_pend

Table 11-38. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_1_pend
11	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_0_pend
10	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_dst_busecc_pend
9	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSIL_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_src_busecc_pend
8	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_dst_busecc_pend
7	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSIL_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSIL_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_src_busecc_pend

Table 11-38. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_dst_busecc_pend
5	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_src_busecc_pend
4	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_CPSW0_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_CPSW0_PSISS_D_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_dst_busecc_pend
3	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_CPSW0_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_CPSW0_PSISS_D_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_src_busecc_pend
2	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_2_pend
1	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_1_pend

Table 11-38. MCU_NAVSS_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_0_pend

11.2.17 MCU_NAVSS_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

MCU_NAVSS_DED_EOI_REG is shown in [Figure 11-18](#) and described in [Table 11-40](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 11-39. MCU_NAVSS_DED_EOI_REG Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 113Ch

Figure 11-18. MCU_NAVSS_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-40. MCU_NAVSS_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

11.2.18 MCU_NAVSS_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MCU_NAVSS_DED_STATUS_REG0 is shown in [Figure 11-19](#) and described in [Table 11-42](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 11-41. MCU_NAVSS_DED_STATUS_REG0 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1140h

Figure 11-19. MCU_NAVSS_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
UDMAP0_RPC F1_RAMECC_ PEND	UDMAP0_RPC F0_RAMECC_ PEND	UDMAP0_RFF W_RAMECC_P END	UDMAP0_TPC F4_RAMECC_ PEND	UDMAP0_TPC F1_RAMECC_ PEND	UDMAP0_TPC F0_RAMECC_ PEND	UDMAP0_TSTA TE_RAMECC_ PEND	UDMAP0_RPC U_CNTR_RAM ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
UDMAP0_RPC U_SB1_RAME CC_PEND	UDMAP0_RPC U_SB0_RAME CC_PEND	UDMAP0_RPT RCU_CNTR_R AMECC_PEND	UDMAP0_RPT RSB2_RAMEC C_PEND	UDMAP0_RPT RSB1_RAMEC C_PEND	UDMAP0_RPT RSB0_RAMEC C_PEND	UDMAP0_TPT RCU_CNTR_R AMECC_PEND	UDMAP0_TPT RSB2_RAMEC C_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_TPT RSB1_RAMEC C_PEND	UDMAP0_TPT RSB0_RAMEC C_PEND	UDMAP0_RPB UF_PF_RAME CC_PEND	UDMAP0_RPB UF_DF_RAME CC_PEND	UDMAP0_RPB UF_CF_RAME CC_PEND	UDMAP0_RPR Q_RAMECC_P END	UDMAP0_RPC FG_RAMECC_ PEND	UDMAP0_RPS TATE_RAMEC C_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_TPC U_CNTR_RAM ECC_PEND	UDMAP0_TPC U_RAMECC_P END	UDMAP0_TPB UF_PF_RAME CC_PEND	UDMAP0_TPB UF_DF_RAME CC_PEND	UDMAP0_TPB UF_CF_RAME CC_PEND	UDMAP0_TPC FG_RAMECC_ PEND	UDMAP0_TPS TATE_RAMEC C_PEND	ECCAGG_PEN D
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-42. MCU_NAVSS_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMAP0_RPCF1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf1_amecc_pend
30	UDMAP0_RPCF0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf0_amecc_pend
29	UDMAP0_RFFW_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rffw_amecc_pend
28	UDMAP0_TPCF4_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcf4_amecc_pend
27	UDMAP0_TPCF1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcf1_amecc_pend
26	UDMAP0_TPCF0_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcf0_amecc_pend
25	UDMAP0_TSTATE_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tstate_amecc_pend
24	UDMAP0_RPCU_CNTR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcu_cntr_amecc_pend
23	UDMAP0_RPCU_SB1_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcu_sb1_amecc_pend

Table 11-42. MCU_NAVSS_DED_STATUS_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22	UDMAP0_RPCU_SB0_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcu_sb0_amecc_pend
21	UDMAP0_RPTRCU_CNT_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrcu_cntr_amecc_pend
20	UDMAP0_RPTRSB2_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrsb2_amecc_pend
19	UDMAP0_RPTRSB1_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrsb1_amecc_pend
18	UDMAP0_RPTRSB0_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rptrsb0_amecc_pend
17	UDMAP0_TPTRCU_CNT_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrcu_cntr_amecc_pend
16	UDMAP0_TPTRSB2_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrsb2_amecc_pend
15	UDMAP0_TPTRSB1_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrsb1_amecc_pend
14	UDMAP0_TPTRSB0_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tptrsb0_amecc_pend
13	UDMAP0_RPBUFF_PF_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpbuff_pf_amecc_pend
12	UDMAP0_RPBUFF_DF_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpbuff_df_amecc_pend
11	UDMAP0_RPBUFF_CF_R_AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpbuff_cf_amecc_pend
10	UDMAP0_RPRQ_RAMECC_C_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rprq_amecc_pend
9	UDMAP0_RPCFG_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcfg_amecc_pend
8	UDMAP0_RPSTATE_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpstate_amecc_pend
7	UDMAP0_TPCU_CNTR_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcu_cntr_amecc_pend
6	UDMAP0_TPCU_RAMECC_C_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcu_amecc_pend
5	UDMAP0_TPBUFF_PF_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpbuff_pf_amecc_pend
4	UDMAP0_TPBUFF_DF_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpbuff_df_amecc_pend
3	UDMAP0_TPBUFF_CF_RA_MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpbuff_cf_amecc_pend
2	UDMAP0_TPCFG_RAMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpcfg_amecc_pend
1	UDMAP0_TPSTATE_RAM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tpstate_amecc_pend
0	ECCAGG_PEND	R/W1S	0h	Interrupt Pending Status for eccagg_pend

11.2.19 MCU_NAVSS_DED_STATUS_REG1 Register (Offset = 144h) [reset = 0h]

MCU_NAVSS_DED_STATUS_REG1 is shown in [Figure 11-20](#) and described in [Table 11-44](#).

Return to [Summary Table](#).

Interrupt Status Register 1

**Table 11-43. MCU_NAVSS_DED_STATUS_REG1
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1144h

Figure 11-20. MCU_NAVSS_DED_STATUS_REG1 Register

31	30	29	28	27	26	25	24
UDMASS_INTA0_SR_ECC_PEND	UDMASS_INTA0_IM_ECC_PEND	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_PEND	RINGACC0_ECC_PEND	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_PEND	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_PEND	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_2_PEND	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_1_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_0_PEND	UDMAP0_RRN_GOCC_RAMECC_C_PEND	UDMAP0_TRN_GOCC_RAMECC_C_PEND	UDMAP0_PSIL_TID_RAMECC_PEND	UDMAP0_PSIL_R_RAMECC_PEND	UDMAP0_SDE_C3_RAMECC_PEND	UDMAP0_SDE_C0_RAMECC_PEND	UDMAP0_RDE_C2_RAMECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_RDE_C1_RAMECC_PEND	UDMAP0_RDE_C0_RAMECC_PEND	UDMAP0_REV_TCNTN_RAMECC_PEND	UDMAP0_TEV_TCNTN_RAMECC_PEND	UDMAP0_STS_RAMECC3_PEND	UDMAP0_STS_RAMECC2_PEND	UDMAP0_STS_RAMECC1_PEND	UDMAP0_STS_RAMECC0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_EH_RAMECC_PEND	UDMAP0_PRO_XY_RAMECC_PEND	UDMAP0_RST_ATE_RAMECC_PEND	UDMAP0_RFL_OW1_RAMECC_PEND	UDMAP0_RFL_OW0_RAMECC_PEND	UDMAP0_RPC_F4_RAMECC_PEND	UDMAP0_RPC_F3_RAMECC_PEND	UDMAP0_RPC_F2_RAMECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-44. MCU_NAVSS_DED_STATUS_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMASS_INTA0_SR_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_sr_ecc_pend
30	UDMASS_INTA0_IM_ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_im_ecc_pend
29	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmass_inta0_edc_ctrl_busecc_pend
28	RINGACC0_ECC_PEND	R/W1S	0h	Interrupt Pending Status for ringacc0_ecc_pend
27	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_1_pend
26	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_0_pend

Table 11-44. MCU_NAVSS_DED_STATUS_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_B USECC_2_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmap0_edc_ctrl_busecc_2_pend
24	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_B USECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmap0_edc_ctrl_busecc_1_pend
23	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_B USECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_udmap0_edc_ctrl_busecc_0_pend
22	UDMAP0_RRNGOCC_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rrngocc_amecc_pend
21	UDMAP0_TRNGOCC_RA MECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_trngocc_amecc_pend
20	UDMAP0_PSILTID_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_psiltid_amecc_pend
19	UDMAP0_PSILR_RAMEC C_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_psilr_amecc_pend
18	UDMAP0_SDEC3_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sdec3_amecc_pend
17	UDMAP0_SDEC0_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sdec0_amecc_pend
16	UDMAP0_RDEC2_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rdec2_amecc_pend
15	UDMAP0_RDEC1_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rdec1_amecc_pend
14	UDMAP0_RDEC0_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rdec0_amecc_pend
13	UDMAP0_REVTCNTR_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_revtntr_amecc_pend
12	UDMAP0_TEVTCNTR_R AMECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_tevtntr_amecc_pend
11	UDMAP0_STS_RAMECC 3_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc3_pend
10	UDMAP0_STS_RAMECC 2_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc2_pend
9	UDMAP0_STS_RAMECC 1_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc1_pend
8	UDMAP0_STS_RAMECC 0_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_sts_amecc0_pend
7	UDMAP0_EH_RAMECC_ PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_eh_amecc_pend
6	UDMAP0_PROXY_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_proxy_amecc_pend
5	UDMAP0_RSTATE_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rstate_amecc_pend
4	UDMAP0_RFLOW1_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rflow1_amecc_pend
3	UDMAP0_RFLOW0_RAM ECC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rflow0_amecc_pend
2	UDMAP0_RPCF4_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf4_amecc_pend
1	UDMAP0_RPCF3_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf3_amecc_pend
0	UDMAP0_RPCF2_RAME CC_PEND	R/W1S	0h	Interrupt Pending Status for udmapi0_rpcf2_amecc_pend

11.2.20 MCU_NAVSS_DED_STATUS_REG2 Register (Offset = 148h) [reset = 0h]

MCU_NAVSS_DED_STATUS_REG2 is shown in [Figure 11-21](#) and described in [Table 11-46](#).

Return to [Summary Table](#).

Interrupt Status Register 2

**Table 11-45. MCU_NAVSS_DED_STATUS_REG2
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1148h

Figure 11-21. MCU_NAVSS_DED_STATUS_REG2 Register

31	30	29	28	27	26	25	24
NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDG E_DST_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDG E_SRC_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL D_DATA_BRIDG GE_DST_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL D_DATA_BRIDG GE_SRC_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL D_DATA_BRIDG E_DST_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL D_DATA_BRIDG E_SRC_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL D_DATA_BRIDG E_DST_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL D_DATA_BRIDG E_SRC_BUSECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTL RL_BUSECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM A_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDM MA_MCU1_PSIL_EDC_CTRL BUSECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-21. MCU_NAVSS_DED_STATUS_REG2 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_UDMAP0_ STRM_SAFE _NAVSS_MCU _UDMASS_PSI LSS0_UDMAP0_ STRM_SAFE G_EDC_CTRL_ BUSECC_PEN D	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU1_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU1_PSI SAFE_EDC_ CTRL_BUSEC C_PEND	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU0_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU0_PSI SAFE_EDC_ CTRL_BUSEC C_PEND	NAVSS_MCU_UDMASS_PSI SS0_CPSW0_P SI_SAFEG_N AVSS_MCU_U DMASS_PSILS S0_CPSW0_PS IL_SAFEG_ED C_CTRL_BUSE CC_PEND	NAVSS_MCU_UDMASS_PSI SS0_NAVSS_P SI_RT_BRIDG E_NAVSS_MC U_UDMASS_P SISS0_NAVS S_PSI_RT_BR IDGE_EDC_CT RL_BUSECC_P END	UDMASS_INTA 0_GC_ECC_PE ND	UDMASS_INTA 0_MC_ECC_PE ND	UDMASS_INTA 0_LC_ECC_PE ND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-46. MCU_NAVSS_DED_STATUS_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSI_D_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_D_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_data_bridge_dst_busecc_pend
30	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSI_D_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_D_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_data_bridge_src_busecc_pend
29	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_CPSW0_PSI_L_D_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_L_D_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt_cpsw0_psil_d_data_bridge_dst_busecc_pend
28	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_CPSW0_PSI_L_D_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_L_D_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt_cpsw0_psil_d_data_bridge_src_busecc_pend
27	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSI_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_dst_busecc_pend

Table 11-46. MCU_NAVSS_DED_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSI_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_src_busecc_pend
25	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_CPSW0_PSI_L_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_L_S_DATA_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_dst_busecc_pend
24	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SAFEG_RT_CPSW0_PSI_L_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_L_S_DATA_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_src_busecc_pend
23	NAVSS_MCU_UDMASS_PSISS0_CFG_NAVSS_MCU_UDMASS_PSISS0_CFG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cfg_navss_mcu_udmass_psilss0_cfg_edc_ctrl_busecc_pend
22	NAVSS_MCU_UDMASS_PSISS0_L2P_PSI_LCFG0_CFGSTRM_NAVSS_MCU_UDMASS_PSISS0_L2P_PSI_LCFG0_CFGSTRM_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_edc_ctrl_busecc_pend
21	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMAP0_CFGSTRM_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMAP0_CFGSTRM_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmap0_cfgstrm_navss_mcu_udmass_psilss0_l2p_udmap0_cfgstrm_edc_ctrl_busecc_pend
20	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_MEVT_IN_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_MEVT_IN_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmass_inta0_mevt_in_navss_mcu_udmass_psilss0_l2p_udmass_inta0_mevt_in_edc_ctrl_busecc_pend
19	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_C EVT_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_C EVT_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmass_inta0_cevt_navss_mcu_udmass_psilss0_l2p_udmass_inta0_cevt_edc_ctrl_busecc_pend

Table 11-46. MCU_NAVSS_DED_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	NAVSS_MCU_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_EVT_NAVSS_MC U_UDMASS_P SILSS0_L2P_UDMASS_ INTA0_EVT_ EDC_CTRL_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmass_inta0_evt_navss_mcu_ud mass_psilss0_l2p_udmass_inta0_evt_edc_ctrl_busecc_pend
17	NAVSS_MCU_UDMASS_P SILSS0_L2P_DMSC_EV T_NAVSS_MCU_UDMAS S_P SILSS0_L2P_DMSC_ EVT_EDC_CTRL_BUSEC C_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_dmesc_evt_navss_mcu_udmass_p silss0_l2p_dmesc_evt_edc_ctrl_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_L2P_UDMAP0_ STRM_NAVSS_MCU_UD MASS_P SILSS0_L2P_UD MAP0_STRM_EDC_CTR L_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_udmap0_strm_navss_mcu_udmas s_psilss0_l2p_udmap0_strm_edc_ctrl_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_L2P_PDMA_M CU1_P SIL_NAVSS_MCU_ UDMASS_P SILSS0_L2P_ PDMA_MCU1_P SIL_ED C_CTRL_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_pdma_mcu1_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu1_psil_edc_ctrl_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_L2P_PDMA_M CU0_P SIL_NAVSS_MCU_ UDMASS_P SILSS0_L2P_ PDMA_MCU0_P SIL_ED C_CTRL_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_pdma_mcu0_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu0_psil_edc_ctrl_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_L2P_CPSW0_P SIL_NAVSS_MCU_UDMA SS_P SILSS0_L2P_CPSW 0_P SIL_EDC_CTRL_BUS ECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_cpsw0_psil_navss_mcu_udmass_ psilss0_l2p_cpsw0_psil_edc_ctrl_busecc_pend
12	NAVSS_MCU_UDMASS_P SILSS0_L2P_NAVSS_P SIL_NAVSS_MCU_UDMA SS_P SILSS0_L2P_NAVS S_P SIL_EDC_CTRL_BUS ECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_l2p_navss_psil_navss_mcu_udmass_ psilss0_l2p_navss_psil_edc_ctrl_busecc_pend
11	NAVSS_MCU_UDMASS_P SILSS0_P SILCFG0_CFG GSTRM_BRIDGE_NAVSS_ MCU_UDMASS_P SILSS0_P SILCFG0_CFGSTRM_ BRIDGE_EDC_CTRL_B USECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_navss_mcu_u dmass_psilss0_psilcfg0_cfgstrm_bridge_edc_ctrl_busecc_pend
10	NAVSS_MCU_UDMASS_P SILSS0_UDMAP0_CFG STRM_BRIDGE_NAVSS_ MCU_UDMASS_P SILSS0_ UDMAP0_CFGSTRM_B RIDGE_EDC_CTRL_BUS ECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_navss_mcu_ udmass_psilss0_udmap0_cfgstrm_bridge_edc_ctrl_busecc_pend

Table 11-46. MCU_NAVSS_DED_STATUS_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	NAVSS_MCU_UDMASS_PSISS0_PSIICFG0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSISS0_PSIICFG0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_edc_ctrl_busecc_pend
8	NAVSS_MCU_UDMASS_PSISS0_UDMAP0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSISS0_UDMAP0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_edc_ctrl_busecc_pend
7	NAVSS_MCU_UDMASS_PSISS0_UDMAP0_STRM_SAFEG_NAVSS_MCU_UDMASS_PSISS0_UDMAP0_STRM_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_udmap0_strm_safeg_navss_mcu_udmass_psilss0_udmap0_strm_safeg_edc_ctrl_busecc_pend
6	NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU1_PSIIL_SAFEG_NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU1_PSIIL_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_edc_ctrl_busecc_pend
5	NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU0_PSIIL_SAFEG_NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU0_PSIIL_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_edc_ctrl_busecc_pend
4	NAVSS_MCU_UDMASS_PSISS0_CPSW0_PSIIL_SAFEG_NAVSS_MCU_UDMASS_PSISS0_CPSW0_PSIIL_SAFEG_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cpsw0_psil_safeg_navss_mcu_udmass_psilss0_cpsw0_psil_safeg_edc_ctrl_busecc_pend
3	NAVSS_MCU_UDMASS_PSISS0_NAVSS_PSIIL_RT_BRIDGE_NAVSS_MCU_UDMASS_PSISS0_NAVSS_PSIIL_RT_BRIDGE_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_navss_psil_rt_bridge_navss_mcu_udmass_psilss0_navss_psil_rt_bridge_edc_ctrl_busecc_pend
2	UDMASS_INTA0_GC_EC_C_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_gc_ecc_pend
1	UDMASS_INTA0_MC_EC_C_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_mc_ecc_pend
0	UDMASS_INTA0_LC_EC_C_PEND	R/W1S	0h	Interrupt Pending Status for udmass_inta0_lc_ecc_pend

11.2.21 MCU_NAVSS_DED_STATUS_REG3 Register (Offset = 14Ch) [reset = X]

MCU_NAVSS_DED_STATUS_REG3 is shown in [Figure 11-22](#) and described in [Table 11-48](#).

Return to [Summary Table](#).

Interrupt Status Register 3

**Table 11-47. MCU_NAVSS_DED_STATUS_REG3
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 114Ch

Figure 11-22. MCU_NAVSS_DED_STATUS_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_4 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_3 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_2 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_1 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SCR3 SCR_NAVSS MCU_UDMASS PSILSS0_CBA SS_ETL_SCR3 SCR_EDC_CT RL_BUSECC_0 PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_D_DEF EVT_P2P_BRI DGE_D_DEF_E VT_BRIDGE_B USECC_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFE RT_PDMA_M CU1_PSIL_D_E TL0_P2P_BRID GE_SAFE_R T_PDMA_MCU 1_PSIL_D_ETL 0_BRIDGE_DS T_BUSECC_PE ND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFE RT_PDMA_M CU1_PSIL_D_E TL0_P2P_BRID GE_SAFE_R T_PDMA_MCU 1_PSIL_D_ETL 0_BRIDGE_SR C_BUSECC_P END
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFE RT_PDMA_M CU1_PSIL_S_E TL0_P2P_BRID GE_SAFE_R T_PDMA_MCU 1_PSIL_S_ETL 0_BRIDGE_DS T_BUSECC_PE ND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_E TL_NAVSS_MC U_UDMASS_P SILSS0_CBAS S_ETL_SAFE RT_PDMA_M CU1_PSIL_S_E TL0_P2P_BRID GE_SAFE_R T_PDMA_MCU 1_PSIL_S_ETL 0_BRIDGE_DS T_BUSECC_P END	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_2_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_1_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SC R2_SCR_NAVS S_MCU_UDMA SS_PSILSS0_C BASS_RESP_S CR2_SCR_ED C_CTRL_BUSE CC_0_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSIL S_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSIL_S RESP_BRIDG E_DST_BUSEC C_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSIL S_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSIL_S RESP_BRIDG E_SRC_BUSE CC_PEND	NAVSS_MCU_UDMASS_PSIL SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_CPSW 0_PSIL_S_RES P_P2P_BRIDG E_SAFE_RT CPSW0_PSIL S_RESP_BRID GE_DST_BUS ECC_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-22. MCU_NAVSS_DED_STATUS_REG3 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_CPSW 0_PSI_S_RES P_P2P_BRIDG E_SAFEG_RT CPSW0_PSI S_RESP_BRID GE_SRC_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSE C_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSE CC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT CPSW0_PSI D_RESP_BRID GE_DST_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS MCU_UDMASS PSILSS0_CBA SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT CPSW0_PSI D_RESP_BRID GE_SRC_BUS ECC_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS PSILSS0_CBA SS_DATA_SCR 1_SCR_NAVSS MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_2_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS PSILSS0_CBA SS_DATA_SCR 1_SCR_NAVSS MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_1_PEND	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_M CU_UDMASS PSILSS0_CBA SS_DATA_SCR 1_SCR_NAVSS MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_0_PEND
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-48. MCU_NAVSS_DED_STATUS_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_4_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_4_pend
22	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_3_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_3_pend
21	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_2_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_2_pend
20	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_1_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_1_pend

Table 11-48. MCU_NAVSS_DED_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_P SILSS0_CBASS_ETL_N SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_0_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_0_pend
18	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_D DEF_EVT_P2P_BRIDGE_ D_DEF_EVT_BRIDGE_B USECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_d_def_evt_p2p_bridge_d_def_evt_bridge_busecc_pen d
17	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_DST_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_dst_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_SRC_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_src_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_DST_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_dst_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_SRC_BUSECC_PEN D	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_src_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_CBASS_RESP_ NAVSS_MCU_UDMASS_ P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ EDC_CTRL_BUSECC_2_ PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psil ss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp _scr2_scr_edc_ctrl_busecc_2_pend

Table 11-48. MCU_NAVSS_DED_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_1_pend
11	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_0_pend
10	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_dst_busecc_pend
9	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_src_busecc_pend
8	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_S_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_dst_busecc_pend
7	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_S_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_src_busecc_pend

Table 11-48. MCU_NAVSS_DED_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_dst_busecc_pend
5	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_D_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_src_busecc_pend
4	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_D_RESP_BRIDGE_DST_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_dst_busecc_pend
3	NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSilSS0_CBASS_RESP_SAFEG_RT_CPSW0_PSil_D_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_D_RESP_BRIDGE_SRC_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_src_busecc_pend
2	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_2_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_2_pend
1	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_1_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_1_pend

Table 11-48. MCU_NAVSS_DED_STATUS_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_0_PEND	R/W1S	0h	Interrupt Pending Status for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_0_pend

11.2.22 MCU_NAVSS_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MCU_NAVSS_DED_ENABLE_SET_REG0 is shown in [Figure 11-23](#) and described in [Table 11-50](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 11-49.
MCU_NAVSS_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1180h

Figure 11-23. MCU_NAVSS_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
UDMAP0_RPCF1_RAMECC_ENABLE_SET	UDMAP0_RPCF0_RAMECC_ENABLE_SET	UDMAP0_RFFW_RAMECC_ENABLE_SET	UDMAP0_TPCF4_RAMECC_ENABLE_SET	UDMAP0_TPCF1_RAMECC_ENABLE_SET	UDMAP0_TPCF0_RAMECC_ENABLE_SET	UDMAP0_TSTATE_RAMECC_ENABLE_SET	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
UDMAP0_RPCU_SB1_RAMECC_ENABLE_SET	UDMAP0_RPCU_SB0_RAMECC_ENABLE_SET	UDMAP0_RPT_RCU_CNTR_RAMECC_ENABLE_SET	UDMAP0_RPT_RSB2_RAMECC_ENABLE_SET	UDMAP0_RPT_RSB1_RAMECC_ENABLE_SET	UDMAP0_RPT_RSB0_RAMECC_ENABLE_SET	UDMAP0_TPT_RCU_CNTR_RAMECC_ENABLE_SET	UDMAP0_TPT_RSB2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_TPT_RSB1_RAMECC_ENABLE_SET	UDMAP0_TPT_RSB0_RAMECC_ENABLE_SET	UDMAP0_RPB_UF_PF_RAMECC_ENABLE_SET	UDMAP0_RPB_UF_DF_RAMECC_ENABLE_SET	UDMAP0_RPB_UF_CF_RAMECC_ENABLE_SET	UDMAP0_RPR_Q_RAMECC_ENABLE_SET	UDMAP0_RPCFG_RAMECC_ENABLE_SET	UDMAP0_RPSTATE_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_TPCU_CNTR_RAMECC_ENABLE_SET	UDMAP0_TPCU_RAMECC_ENABLE_SET	UDMAP0_TPB_UF_PF_RAMECC_ENABLE_SET	UDMAP0_TPB_UF_DF_RAMECC_ENABLE_SET	UDMAP0_TPB_UF_CF_RAMECC_ENABLE_SET	UDMAP0_TPCFG_RAMECC_ENABLE_SET	UDMAP0_TPS_TATE_RAMECC_ENABLE_SET	ECCAGG_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-50. MCU_NAVSS_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMAP0_RPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf1_ramecc_pend
30	UDMAP0_RPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf0_ramecc_pend
29	UDMAP0_RFFW_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rffw_ramecc_pend
28	UDMAP0_TPCF4_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcf4_ramecc_pend
27	UDMAP0_TPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcf1_ramecc_pend
26	UDMAP0_TPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcf0_ramecc_pend
25	UDMAP0_TSTATE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tstate_ramecc_pend

Table 11-50. MCU_NAVSS_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcu_cntr_amecc_pend
23	UDMAP0_RPCU_SB1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcu_sb1_amecc_pend
22	UDMAP0_RPCU_SB0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcu_sb0_amecc_pend
21	UDMAP0_RPTRCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrcu_cntr_amecc_pend
20	UDMAP0_RPTRSB2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrsb2_amecc_pend
19	UDMAP0_RPTRSB1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrsb1_amecc_pend
18	UDMAP0_RPTRSB0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rptrsb0_amecc_pend
17	UDMAP0_TPTRCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrcu_cntr_amecc_pend
16	UDMAP0_TPTRSB2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrsb2_amecc_pend
15	UDMAP0_TPTRSB1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrsb1_amecc_pend
14	UDMAP0_TPTRSB0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tptrsb0_amecc_pend
13	UDMAP0_RPBUF_PF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpbuf_pf_amecc_pend
12	UDMAP0_RPBUF_DF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpbuf_df_amecc_pend
11	UDMAP0_RPBUF_CF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpbuf_cf_amecc_pend
10	UDMAP0_RPRQ_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rprq_amecc_pend
9	UDMAP0_RPCFG_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcfg_amecc_pend
8	UDMAP0_RPSTATE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpstate_amecc_pend
7	UDMAP0_TPCU_CNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcu_cntr_amecc_pend
6	UDMAP0_TPCU_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcu_amecc_pend
5	UDMAP0_TPBUF_PF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpbuf_pf_amecc_pend
4	UDMAP0_TPBUF_DF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpbuf_df_amecc_pend
3	UDMAP0_TPBUF_CF_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpbuf_cf_amecc_pend
2	UDMAP0_TPCFG_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpcfg_amecc_pend
1	UDMAP0_TPSTATE_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tpstate_amecc_pend
0	ECCAGG_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for eccagg_pend

11.2.23 MCU_NAVSS_DED_ENABLE_SET_REG1 Register (Offset = 184h) [reset = 0h]

MCU_NAVSS_DED_ENABLE_SET_REG1 is shown in [Figure 11-24](#) and described in [Table 11-52](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 1

Table 11-51.
MCU_NAVSS_DED_ENABLE_SET_REG1 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1184h

Figure 11-24. MCU_NAVSS_DED_ENABLE_SET_REG1 Register

31	30	29	28	27	26	25	24
UDMASS_INTA0_SR_ECC_ENABLE_SET	UDMASS_INTA0_IM_ECC_ENABLE_SET	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_SET	RINGACC0_ECC_ENABLE_SET	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_SET	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_SET	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_2_ENABLE_SET	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_1_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_0_ENABLE_SET	UDMAP0_RRNGOCC_RAMECC_ENABLE_SET	UDMAP0_TRNGOCC_RAMECC_ENABLE_SET	UDMAP0_PSILTID_RAMECC_ENABLE_SET	UDMAP0_PSILR_RAMECC_ENABLE_SET	UDMAP0_SDEC3_RAMECC_ENABLE_SET	UDMAP0_SDEC0_RAMECC_ENABLE_SET	UDMAP0_RDEC2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
UDMAP0_RDEC1_RAMECC_ENABLE_SET	UDMAP0_RDEC0_RAMECC_ENABLE_SET	UDMAP0_REVTCNTR_RAMECC_ENABLE_SET	UDMAP0_TEVTCNTR_RAMECC_ENABLE_SET	UDMAP0_STS_RAMECC3_ENABLE_SET	UDMAP0_STS_RAMECC2_ENABLE_SET	UDMAP0_STS_RAMECC1_ENABLE_SET	UDMAP0_STS_RAMECC0_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0
UDMAP0_EHRAMECC_ENABLE_SET	UDMAP0_PROXY_RAMECC_ENABLE_SET	UDMAP0_RSTATE_RAMECC_ENABLE_SET	UDMAP0_RFLOW1_RAMECC_ENABLE_SET	UDMAP0_RFLOW0_RAMECC_ENABLE_SET	UDMAP0_RPCF4_RAMECC_ENABLE_SET	UDMAP0_RPCF3_RAMECC_ENABLE_SET	UDMAP0_RPCF2_RAMECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-52. MCU_NAVSS_DED_ENABLE_SET_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMASS_INTA0_SR_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_sr_ecc_pend
30	UDMASS_INTA0_IM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_im_ecc_pend
29	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmass_inta0_edc_ctrl_busecc_pend
28	RINGACC0_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for ringacc0_ecc_pend
27	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_1_pend

Table 11-52. MCU_NAVSS_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_0_pend
25	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_2_pend
24	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_1_pend
23	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_0_pend
22	UDMAP0_RRNGOCC_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rrngocc_ramecc_pend
21	UDMAP0_TRNGOCC_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_trngocc_ramecc_pend
20	UDMAP0_PSILTID_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_psiltid_ramecc_pend
19	UDMAP0_PSILR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_psilr_ramecc_pend
18	UDMAP0_SDEC3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sdec3_ramecc_pend
17	UDMAP0_SDEC0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sdec0_ramecc_pend
16	UDMAP0_RDEC2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rdec2_ramecc_pend
15	UDMAP0_RDEC1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rdec1_ramecc_pend
14	UDMAP0_RDEC0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rdec0_ramecc_pend
13	UDMAP0_REVTCNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_revtntr_ramecc_pend
12	UDMAP0_TEVTCNTR_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_tevtntr_ramecc_pend
11	UDMAP0_STS_RAMECC3_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc3_pend
10	UDMAP0_STS_RAMECC2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc2_pend
9	UDMAP0_STS_RAMECC1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc1_pend
8	UDMAP0_STS_RAMECC0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_sts_ramecc0_pend
7	UDMAP0_EH_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_ah_ramecc_pend
6	UDMAP0_PROXY_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_proxy_ramecc_pend
5	UDMAP0_RSTATE_RAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rstate_ramecc_pend
4	UDMAP0_RFLOW1_RAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rflow1_ramecc_pend
3	UDMAP0_RFLOW0_RAM_ECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rflow0_ramecc_pend
2	UDMAP0_RPCF4_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf4_ramecc_pend

Table 11-52. MCU_NAVSS_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UDMAP0_RPCF3_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf3_ramecc_pend
0	UDMAP0_RPCF2_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmapi0_rpcf2_ramecc_pend

11.2.24 MCU_NAVSS_DED_ENABLE_SET_REG2 Register (Offset = 188h) [reset = 0h]

MCU_NAVSS_DED_ENABLE_SET_REG2 is shown in [Figure 11-25](#) and described in [Table 11-54](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 2

Table 11-53.
MCU_NAVSS_DED_ENABLE_SET_REG2 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1188h

Figure 11-25. MCU_NAVSS_DED_ENABLE_SET_REG2 Register

31	30	29	28	27	26	25	24
NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_PDMA_MCU1_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_PDMA_MCU1_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_CPSW0_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_CPSW0_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_CPSW0_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_CPSW0_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_CPSW0_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_P2P_BRIDGE_SAFE_G_RT_CPSW0_PSIL_D DATA_BRIDGE_E_DST_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSS0_CFG_NAVSS_MCU_UDMASS_PSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-25. MCU_NAVSS_DED_ENABLE_SET_REG2 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_UDMAP0_ STRM_SAFEG _NAVSS_MCU _UDMASS_PSI LSS0_UDMAP0_ STRM_SAFE G_EDC_CTRL_ BUSECC_ENA BLE_SET	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU1_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU1_PSI SAFEG_EDC_ CTRL_BUSEC C_ENABLE_SE T	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU0_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU0_PSI SAFEG_EDC_ CTRL_BUSEC C_ENABLE_SE T	NAVSS_MCU_UDMASS_PSI SS0_CPSW0_P SIL_SAFEG_N AVSS_MCU_U DMASS_PSILS S0_CPSW0_PS IL_SAFEG_ED C_CTRL_BUSE CC_ENABLE_S ET	NAVSS_MCU_UDMASS_PSI SS0_NAVSS_P SIL_RT_BRIDG E_NAVSS_MC U_UDMASS_P SILSS0_NAVS S_PSI_RT_BR IDGE_EDC_CT RL_BUSECC_E NABLE_SET	UDMASS_INTA 0_GC_ECC_EN ABLE_SET	UDMASS_INTA 0_MC_ECC_E NABLE_SET	UDMASS_INTA 0_LC_ECC_EN ABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-54. MCU_NAVSS_DED_ENABLE_SET_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFEG_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_DST_BUSECC_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_dst_busecc_pend
30	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFEG_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_SRC_BUSECC_ ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_src_busecc_pend
29	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE _SAFEG_RT_CPSW0_PS IL_D_DATA_BRIDGE_DS T_BUSECC_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_dst_busecc_pend
28	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFEG_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE _SAFEG_RT_CPSW0_PS IL_D_DATA_BRIDGE_SR C_BUSECC_ENABLE_SE T	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_src_busecc_pend

Table 11-54. MCU_NAVSS_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_dst_busecc_pend
26	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_src_busecc_pend
25	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_dst_busecc_pend
24	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_src_busecc_pend
23	NAVSS_MCU_UDMASS_PSilSS0_CFG_NAVSS_MCU_UDMASS_PSilSS0_CFG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cfg_navss_mcu_udmass_psilss0_cfg_edc_ctrl_busecc_pend
22	NAVSS_MCU_UDMASS_PSilSS0_I2P_PSilCFG0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_I2P_PSilCFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_i2p_psilcfg0_cfgstrm_navss_mcu_udmass_psilss0_i2p_psilcfg0_cfgstrm_edc_ctrl_busecc_pend
21	NAVSS_MCU_UDMASS_PSilSS0_I2P_UDMAP0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_I2P_UDMAP0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_i2p_udmap0_cfgstrm_navss_mcu_udmass_psilss0_i2p_udmap0_cfgstrm_edc_ctrl_busecc_pend

Table 11-54. MCU_NAVSS_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_MEVT_IN_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_MEVT_IN_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_mevt_in_navss_mcu_u_udmass_psilss0_l2p_udmass_inta0_mevt_in_edc_ctrl_busecc_pend
19	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_C EVT_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_C EVT_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_cevt_navss_mcu_u dmass_psilss0_l2p_udmass_inta0_cevt_edc_ctrl_busecc_pend
18	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_EVT_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_EVT_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_evt_navss_mcu_ud mass_psilss0_l2p_udmass_inta0_evt_edc_ctrl_busecc_pend
17	NAVSS_MCU_UDMASS_PSISS0_L2P_DMSC_EVT_NAVSS_MCU_UDMASS_PSISS0_L2P_DMSC_EVT_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_dmesc_evt_navss_mcu_udmass_p silss0_l2p_dmesc_evt_edc_ctrl_busecc_pend
16	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMAP0_STRM_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMAP0_STRM_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_udmap0_strm_navss_mcu_udmas s_psilss0_l2p_udmap0_strm_edc_ctrl_busecc_pend
15	NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU1_PSI_NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU1_PSI_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu1_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu1_psil_edc_ctrl_busecc_pend
14	NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU0_PSI_NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU0_PSI_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu0_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu0_psil_edc_ctrl_busecc_pend
13	NAVSS_MCU_UDMASS_PSISS0_L2P_CPSW0_PSI_NAVSS_MCU_UDMASS_PSISS0_L2P_CPSW0_PSI_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_cpsw0_psil_navss_mcu_udmass_ psilss0_l2p_cpsw0_psil_edc_ctrl_busecc_pend
12	NAVSS_MCU_UDMASS_PSISS0_L2P_NAVSS_PSI_NAVSS_MCU_UDMASS_PSISS0_L2P_NAVSS_PSI_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_l2p_navss_psil_navss_mcu_udmass_ psilss0_l2p_navss_psil_edc_ctrl_busecc_pend

Table 11-54. MCU_NAVSS_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_edc_ctrl_busecc_pend
10	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_edc_ctrl_busecc_pend
9	NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PSilCFG0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_edc_ctrl_busecc_pend
8	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_edc_ctrl_busecc_pend
7	NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_STRM_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_UDMAP0_STRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_udmap0_strm_safeg_navss_mcu_udmass_psilss0_udmap0_strm_safeg_edc_ctrl_busecc_pend
6	NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU1_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU1_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_edc_ctrl_busecc_pend
5	NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU0_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_PDMA_MCU0_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_edc_ctrl_busecc_pend
4	NAVSS_MCU_UDMASS_PSilSS0_CPSW0_PSil_SAFEG_NAVSS_MCU_UDMASS_PSilSS0_CPSW0_PSil_SAFEG_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cpsw0_psil_safeg_navss_mcu_udmass_psilss0_cpsw0_psil_safeg_edc_ctrl_busecc_pend
3	NAVSS_MCU_UDMASS_PSilSS0_NAVSS_PSil_RT_BRIDGE_NAVSS_MCU_UDMASS_PSilSS0_NAVSS_PSil_RT_BRIDGE_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_navss_psil_rt_bridge_navss_mcu_udmass_psilss0_navss_psil_rt_bridge_edc_ctrl_busecc_pend

Table 11-54. MCU_NAVSS_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UDMASS_INTA0_GC_EC_C_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_gc_ecc_pend
1	UDMASS_INTA0_MC_EC_C_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_mc_ecc_pend
0	UDMASS_INTA0_LC_EC_C_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for udmass_inta0_lc_ecc_pend

11.2.25 MCU_NAVSS_DED_ENABLE_SET_REG3 Register (Offset = 18Ch) [reset = X]

MCU_NAVSS_DED_ENABLE_SET_REG3 is shown in [Figure 11-26](#) and described in [Table 11-56](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 3

Table 11-55.
MCU_NAVSS_DED_ENABLE_SET_REG3 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 118Ch

Figure 11-26. MCU_NAVSS_DED_ENABLE_SET_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_EDC_CTL_BUSECC_4_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_EDC_CTL_BUSECC_3_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_EDC_CTL_BUSECC_2_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_EDC_CTL_BUSECC_1_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SCR3_SCR_EDC_CTL_BUSECC_0_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_D_DEF_EVT_P2P_BRIDGE_D_DEF_EVT_P2P_BRIDGE_B_USECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_D_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_D_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_D_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_D_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBASS_ETL_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DS_T_BUSECC_ENABLE_SET
R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h
7	6	5	4	3	2	1	0

Figure 11-26. MCU_NAVSS_DED_ENABLE_SET_REG3 Register (continued)

[illegible]

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-56. MCU_NAVSS_DED_ENABLE_SET_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU_ UDMASS_PSILSS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_4_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_4_pend
22	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU_ UDMASS_PSILSS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_3_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_3_pend
21	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU_ UDMASS_PSILSS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_2_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_2_pend
20	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU_ UDMASS_PSILSS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_1_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_1_pend

Table 11-56. MCU_NAVSS_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_P SILSS0_CBASS_ETL_N SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_0_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_0_pend
18	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_D DEF_EVT_P2P_BRIDGE_ D_DEF_EVT_BRIDGE_B USECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_d_def_evt_p2p_bridge_d_def_evt_bridge_busecc_pen d
17	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_DST_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_dst_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_src_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_DST_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_dst_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_src_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_CBASS_RESP_ NAVSS_MCU_UDMASS_ PSILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ EDC_CTRL_BUSECC_2 _ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psil ss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp _scr2_scr_edc_ctrl_busecc_2_pend

Table 11-56. MCU_NAVSS_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_1_pend
11	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_0_pend
10	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_dst_busecc_pend
9	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_src_busecc_pend
8	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_S_RESP_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_dst_busecc_pend
7	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_src_busecc_pend

Table 11-56. MCU_NAVSS_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSISS0_CBASS_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSISS0_CBASS_RESP_P2P_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_dst_busecc_pend
5	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSISS0_CBASS_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSISS0_CBASS_RESP_P2P_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_src_busecc_pend
4	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSISS0_CBASS_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSISS0_CBASS_RESP_P2P_BRIDGE_DST_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_dst_busecc_pend
3	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSISS0_CBASS_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSISS0_CBASS_RESP_P2P_BRIDGE_SRC_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_src_busecc_pend
2	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_2_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_2_pend
1	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_1_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_1_pend

Table 11-56. MCU_NAVSS_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_0_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_0_pend

11.2.26 MCU_NAVSS_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MCU_NAVSS_DED_ENABLE_CLR_REG0 is shown in [Figure 11-27](#) and described in [Table 11-58](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 11-57.
MCU_NAVSS_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 11C0h

Figure 11-27. MCU_NAVSS_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
UDMAP0_RPCF1_RAMECC_ENABLE_CLR	UDMAP0_RPCF0_RAMECC_ENABLE_CLR	UDMAP0_RFFW_RAMECC_ENABLE_CLR	UDMAP0_TPCF4_RAMECC_ENABLE_CLR	UDMAP0_TPCF1_RAMECC_ENABLE_CLR	UDMAP0_TPCF0_RAMECC_ENABLE_CLR	UDMAP0_TSTATE_RAMECC_ENABLE_CLR	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
UDMAP0_RPCU_SB1_RAMECC_ENABLE_CLR	UDMAP0_RPCU_SB0_RAMECC_ENABLE_CLR	UDMAP0_RPT_RCU_CNTR_RAMECC_ENABLE_CLR	UDMAP0_RPT_RSB2_RAMECC_ENABLE_CLR	UDMAP0_RPT_RSB1_RAMECC_ENABLE_CLR	UDMAP0_RPT_RSB0_RAMECC_ENABLE_CLR	UDMAP0_TPT_RCU_CNTR_RAMECC_ENABLE_CLR	UDMAP0_TPT_RSB2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
UDMAP0_TPT_RSB1_RAMECC_ENABLE_CLR	UDMAP0_TPT_RSB0_RAMECC_ENABLE_CLR	UDMAP0_RPB_UF_PF_RAMECC_ENABLE_CLR	UDMAP0_RPB_UF_DF_RAMECC_ENABLE_CLR	UDMAP0_RPB_UF_CF_RAMECC_ENABLE_CLR	UDMAP0_RPR_Q_RAMECC_ENABLE_CLR	UDMAP0_RPCFG_RAMECC_ENABLE_CLR	UDMAP0_RPSTATE_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
UDMAP0_TPCU_CNTR_RAMECC_ENABLE_CLR	UDMAP0_TPCU_RAMECC_ENABLE_CLR	UDMAP0_TPB_UF_PF_RAMECC_ENABLE_CLR	UDMAP0_TPB_UF_DF_RAMECC_ENABLE_CLR	UDMAP0_TPB_UF_CF_RAMECC_ENABLE_CLR	UDMAP0_TPCFG_RAMECC_ENABLE_CLR	UDMAP0_TPS_TATE_RAMECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-58. MCU_NAVSS_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMAP0_RPCF1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf1_amecc_pend
30	UDMAP0_RPCF0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf0_amecc_pend
29	UDMAP0_RFFW_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rffw_amecc_pend
28	UDMAP0_TPCF4_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcf4_amecc_pend
27	UDMAP0_TPCF1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcf1_amecc_pend
26	UDMAP0_TPCF0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcf0_amecc_pend
25	UDMAP0_TSTATE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tstate_amecc_pend

Table 11-58. MCU_NAVSS_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	UDMAP0_RPCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcu_cntr_amecc_pend
23	UDMAP0_RPCU_SB1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcu_sb1_amecc_pend
22	UDMAP0_RPCU_SB0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcu_sb0_amecc_pend
21	UDMAP0_RPTRCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrcu_cntr_amecc_pend
20	UDMAP0_RPTRSB2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrsb2_amecc_pend
19	UDMAP0_RPTRSB1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrsb1_amecc_pend
18	UDMAP0_RPTRSB0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rptrsb0_amecc_pend
17	UDMAP0_TPTRCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrcu_cntr_amecc_pend
16	UDMAP0_TPTRSB2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrsb2_amecc_pend
15	UDMAP0_TPTRSB1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrsb1_amecc_pend
14	UDMAP0_TPTRSB0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tptrsb0_amecc_pend
13	UDMAP0_RPBUF_PF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdbuf_pf_amecc_pend
12	UDMAP0_RPBUF_DF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdbuf_df_amecc_pend
11	UDMAP0_RPBUF_CF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdbuf_cf_amecc_pend
10	UDMAP0_RPRQ_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rprq_amecc_pend
9	UDMAP0_RPCFG_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcfg_amecc_pend
8	UDMAP0_RPSTATE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpstate_amecc_pend
7	UDMAP0_TPCU_CNTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcu_cntr_amecc_pend
6	UDMAP0_TPCU_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcu_amecc_pend
5	UDMAP0_TPBUF_PF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tdbuf_pf_amecc_pend
4	UDMAP0_TPBUF_DF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tdbuf_df_amecc_pend
3	UDMAP0_TPBUF_CF_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tdbuf_cf_amecc_pend
2	UDMAP0_TPCFG_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpcfg_amecc_pend
1	UDMAP0_TPSTATE_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tpstate_amecc_pend
0	ECCAGG_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for eccagg_pend

11.2.27 MCU_NAVSS_DED_ENABLE_CLR_REG1 Register (Offset = 1C4h) [reset = 0h]

MCU_NAVSS_DED_ENABLE_CLR_REG1 is shown in [Figure 11-28](#) and described in [Table 11-60](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 1

Table 11-59.
MCU_NAVSS_DED_ENABLE_CLR_REG1 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 11C4h

Figure 11-28. MCU_NAVSS_DED_ENABLE_CLR_REG1 Register

31	30	29	28	27	26	25	24
UDMASS_INTA0_SR_ECC_ENABLE_CLR	UDMASS_INTA0_IM_ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_CLR	RINGACC0_ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_CLR	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_CLR	NAVSS_MCU_UDMASS_UDMASS_AP0_EDC_CTRL_BUSECC_2_ENABLE_CLR	NAVSS_MCU_UDMASS_UDMASS_AP0_EDC_CTRL_BUSECC_1_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_UDMASS_AP0_EDC_CTRL_BUSECC_0_ENABLE_CLR	UDMAP0_RRNGOCC_RAMECC_ENABLE_CLR	UDMAP0_TRNGOCC_RAMECC_ENABLE_CLR	UDMAP0_PSILTID_RAMECC_ENABLE_CLR	UDMAP0_PSILR_RAMECC_ENABLE_CLR	UDMAP0_SDEC3_RAMECC_ENABLE_CLR	UDMAP0_SDEC0_RAMECC_ENABLE_CLR	UDMAP0_RDEC2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
UDMAP0_RDEC1_RAMECC_ENABLE_CLR	UDMAP0_RDEC0_RAMECC_ENABLE_CLR	UDMAP0_REVTCNTR_RAMECC_ENABLE_CLR	UDMAP0_TEVTCNTR_RAMECC_ENABLE_CLR	UDMAP0_STSRAMECC3_ENABLE_CLR	UDMAP0_STSRAMECC2_ENABLE_CLR	UDMAP0_STSRAMECC1_ENABLE_CLR	UDMAP0_STSRAMECC0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0
UDMAP0_EHRAMECC_ENABLE_CLR	UDMAP0_PROXY_RAMECC_ENABLE_CLR	UDMAP0_RSTATE_RAMECC_ENABLE_CLR	UDMAP0_RFLOW1_RAMECC_ENABLE_CLR	UDMAP0_RFLOW0_RAMECC_ENABLE_CLR	UDMAP0_RPCF4_RAMECC_ENABLE_CLR	UDMAP0_RPCF3_RAMECC_ENABLE_CLR	UDMAP0_RPCF2_RAMECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-60. MCU_NAVSS_DED_ENABLE_CLR_REG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	UDMASS_INTA0_SR_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_sr_ecc_pend
30	UDMASS_INTA0_IM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_im_ecc_pend
29	NAVSS_MCU_UDMASS_UDMASS_INTA0_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmass_inta0_edc_ctrl_busecc_pend
28	RINGACC0_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for ringacc0_ecc_pend
27	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_1_pend

Table 11-60. MCU_NAVSS_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26	NAVSS_MCU_UDMASS_RINGACC0_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_ringacc0_edc_ctrl_busecc_0_pend
25	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_2_pend
24	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_1_pend
23	NAVSS_MCU_UDMASS_UDMAP0_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_udmap0_edc_ctrl_busecc_0_pend
22	UDMAP0_RRNGOCC_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rrngocc_amecc_pend
21	UDMAP0_TRNGOCC_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_trngocc_amecc_pend
20	UDMAP0_PSILTID_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_psiltid_amecc_pend
19	UDMAP0_PSILR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_psilr_amecc_pend
18	UDMAP0_SDEC3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sdec3_amecc_pend
17	UDMAP0_SDEC0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sdec0_amecc_pend
16	UDMAP0_RDEC2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdec2_amecc_pend
15	UDMAP0_RDEC1_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdec1_amecc_pend
14	UDMAP0_RDEC0_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rdec0_amecc_pend
13	UDMAP0_REVTCTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_revtctr_amecc_pend
12	UDMAP0_TEVTCTR_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_tevtctr_amecc_pend
11	UDMAP0_STS_RAMECC3_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc3_pend
10	UDMAP0_STS_RAMECC2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc2_pend
9	UDMAP0_STS_RAMECC1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc1_pend
8	UDMAP0_STS_RAMECC0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_sts_amecc0_pend
7	UDMAP0_EH_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_eh_amecc_pend
6	UDMAP0_PROXY_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_proxy_amecc_pend
5	UDMAP0_RSTATE_RAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rstate_amecc_pend
4	UDMAP0_RFLOW1_RAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rflow1_amecc_pend
3	UDMAP0_RFLOW0_RAM_ECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rflow0_amecc_pend
2	UDMAP0_RPCF4_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf4_amecc_pend

Table 11-60. MCU_NAVSS_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	UDMAP0_RPCF3_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf3_ramecc_pend
0	UDMAP0_RPCF2_RAMECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmapi0_rpcf2_ramecc_pend

11.2.28 MCU_NAVSS_DED_ENABLE_CLR_REG2 Register (Offset = 1C8h) [reset = 0h]

MCU_NAVSS_DED_ENABLE_CLR_REG2 is shown in [Figure 11-29](#) and described in [Table 11-62](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 2

Table 11-61.
MCU_NAVSS_DED_ENABLE_CLR_REG2 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 11C8h

Figure 11-29. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register

31	30	29	28	27	26	25	24
NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDG E_DST_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_PDMA_MCU1_PSIL D_DATA_P2P BRIDGE_SAFE G_RT_PDMA_MCU1_PSIL_D DATA_BRIDG E_SRC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_DST_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_SRC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_DST_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_SRC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_DST_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_D ATA_NAVSS_MCU_UDMASS_PSILSS0_CBA SS_DATA_SAFEG_RT_CPSW0_PSIL_D DATA_BRIDG E_SRC_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CFG_NAVSS_MCU_UDMASS_PSILSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSILSS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0

Figure 11-29. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_UDMAP0_ STRM_SAFE NAVSS_MCU_ UDMASS_PSI LSS0_UDMAP0_ STRM_SAFE G_EDC_CTRL_ BUSECC_ENA BLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU1_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU1_PSI SAFE_EDC_ CTRL_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_PDMA_M CU0_PSI_SAF EG_NAVSS_M CU_UDMASS_ PSILSS0_PDM A_MCU0_PSI SAFE_EDC_ CTRL_BUSEC C_ENABLE_CL R	NAVSS_MCU_UDMASS_PSI SS0_CPSW0_P SIL_SAFE_N AVSS_MCU_U DMASS_PSIL S0_CPSW0_PS IL_SAFE_ED C_CTRL_BUSE CC_ENABLE_C LR	NAVSS_MCU_UDMASS_PSI SS0_NAVSS_P SIL_RT_BRIDG E_NAVSS_MC U_UDMASS_P SILSS0_NAVS S_PSI_RT_BR IDGE_EDC_CT RL_BUSECC_E NABLE_CLR	UDMASS_INTA 0_GC_ECC_EN ABLE_CLR	UDMASS_INTA 0_MC_ECC_E NABLE_CLR	UDMASS_INTA 0_LC_ECC_EN ABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-62. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFE_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFE_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_DST_BUSECC_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_dst_busecc_pend
30	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFE_RT_PDMA_MCU 1_PSI_D_DATA_P2P_B RIDGE_SAFE_RT_PDM A_MCU1_PSI_D_DATA_ BRIDGE_SRC_BUSECC_ ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_pdma_mcu1_psil_d_data_p2p_bridge_saf eg_rt_pdma_mcu1_psil_d_data_bridge_src_busecc_pend
29	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFE_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE_ SAFE_RT_CPSW0_PS IL_D_DATA_BRIDGE_DS T_BUSECC_ENABLE_CL R	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_dst_busecc_pend
28	NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ NAVSS_MCU_UDMASS_PSI LSS0_CBASS_DATA_ SAFE_RT_CPSW0_PSI L_D_DATA_P2P_BRIDGE_ SAFE_RT_CPSW0_PS IL_D_DATA_BRIDGE_SR C_BUSECC_ENABLE_CL R	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psil ss0_cbass_data_safeg_rt_cpsw0_psil_d_data_p2p_bridge_safeg_rt _cpsw0_psil_d_data_bridge_src_busecc_pend

Table 11-62. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
27	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_dst_busecc_pend
26	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_pdma_mcu1_psil_s_data_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_data_bridge_src_busecc_pend
25	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_dst_busecc_pend
24	NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSilSS0_CBASS_DATA_SAFEG_RT_CPSW0_PSil_S_DATA_P2P_BRIDGE_SAFEG_RT_CPSW0_PSil_S_DATA_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_safeg_rt_cpsw0_psil_s_data_p2p_bridge_safeg_rt_cpsw0_psil_s_data_bridge_src_busecc_pend
23	NAVSS_MCU_UDMASS_PSilSS0_CFG_NAVSS_MCU_UDMASS_PSilSS0_CFG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cfg_navss_mcu_udmass_psilss0_cfg_edc_ctrl_busecc_pend
22	NAVSS_MCU_UDMASS_PSilSS0_L2P_PSilCFG0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_L2P_PSilCFG0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_navss_mcu_udmass_psilss0_l2p_psilcfg0_cfgstrm_edc_ctrl_busecc_pend
21	NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMAP0_CFGSTRM_NAVSS_MCU_UDMASS_PSilSS0_L2P_UDMAP0_CFGSTRM_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmap0_cfgstrm_navss_mcu_udmass_psilss0_l2p_udmap0_cfgstrm_edc_ctrl_busecc_pend

Table 11-62. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_MEVT_IN_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_MEVT_IN_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_mevt_in_navss_mcu_u_udmass_psilss0_l2p_udmass_inta0_mevt_in_edc_ctrl_busecc_pend
19	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_CEVT_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_CEVT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_cevt_navss_mcu_u dmass_psilss0_l2p_udmass_inta0_cevt_edc_ctrl_busecc_pend
18	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_EVT_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMASS_INTA0_EVT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmass_inta0_evt_navss_mcu_ud mass_psilss0_l2p_udmass_inta0_evt_edc_ctrl_busecc_pend
17	NAVSS_MCU_UDMASS_PSISS0_L2P_DMSC_EVT_NAVSS_MCU_UDMASS_PSISS0_L2P_DMSC_EVT_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_dmesc_evt_navss_mcu_udmass_p silss0_l2p_dmesc_evt_edc_ctrl_busecc_pend
16	NAVSS_MCU_UDMASS_PSISS0_L2P_UDMAP0_STRM_NAVSS_MCU_UDMASS_PSISS0_L2P_UDMAP0_STRM_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_udmap0_strm_navss_mcu_udmas s_psilss0_l2p_udmap0_strm_edc_ctrl_busecc_pend
15	NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU1_PSIL_NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU1_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu1_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu1_psil_edc_ctrl_busecc_pend
14	NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU0_PSIL_NAVSS_MCU_UDMASS_PSISS0_L2P_PDMA_MCU0_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_pdma_mcu0_psil_navss_mcu_ud mass_psilss0_l2p_pdma_mcu0_psil_edc_ctrl_busecc_pend
13	NAVSS_MCU_UDMASS_PSISS0_L2P_CPSW0_PSIL_NAVSS_MCU_UDMASS_PSISS0_L2P_CPSW0_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_cpsw0_psil_navss_mcu_udmass_ psilss0_l2p_cpsw0_psil_edc_ctrl_busecc_pend
12	NAVSS_MCU_UDMASS_PSISS0_L2P_NAVSS_PSIL_NAVSS_MCU_UDMASS_PSISS0_L2P_NAVSS_PSIL_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_l2p_navss_psil_navss_mcu_udmass_ psilss0_l2p_navss_psil_edc_ctrl_busecc_pend

Table 11-62. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	NAVSS_MCU_UDMASS_PSISS0_PSIICFG0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSISS0_PSIICFG0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_bridge_edc_ctrl_busecc_pend
10	NAVSS_MCU_UDMASS_PSISS0_UDMAP0_CFGSTRM_BRIDGE_NAVSS_MCU_UDMASS_PSISS0_UDMAP0_CFGSTRM_BRIDGE_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_navss_mcu_udmass_psilss0_udmap0_cfgstrm_bridge_edc_ctrl_busecc_pend
9	NAVSS_MCU_UDMASS_PSISS0_PSIICFG0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSISS0_PSIICFG0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_navss_mcu_udmass_psilss0_psilcfg0_cfgstrm_safeg_edc_ctrl_busecc_pend
8	NAVSS_MCU_UDMASS_PSISS0_UDMAP0_CFGSTRM_SAFEG_NAVSS_MCU_UDMASS_PSISS0_UDMAP0_CFGSTRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_navss_mcu_udmass_psilss0_udmap0_cfgstrm_safeg_edc_ctrl_busecc_pend
7	NAVSS_MCU_UDMASS_PSISS0_UDMAP0_STRM_SAFEG_NAVSS_MCU_UDMASS_PSISS0_UDMAP0_STRM_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_udmap0_strm_safeg_navss_mcu_udmass_psilss0_udmap0_strm_safeg_edc_ctrl_busecc_pend
6	NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU1_PSIIL_SAFEG_NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU1_PSIIL_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu1_psil_safeg_edc_ctrl_busecc_pend
5	NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU0_PSIIL_SAFEG_NAVSS_MCU_UDMASS_PSISS0_PDMA_MCU0_PSIIL_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_navss_mcu_udmass_psilss0_pdma_mcu0_psil_safeg_edc_ctrl_busecc_pend
4	NAVSS_MCU_UDMASS_PSISS0_CPSW0_PSIIL_SAFEG_NAVSS_MCU_UDMASS_PSISS0_CPSW0_PSIIL_SAFEG_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cpsw0_psil_safeg_navss_mcu_udmass_psilss0_cpsw0_psil_safeg_edc_ctrl_busecc_pend
3	NAVSS_MCU_UDMASS_PSISS0_NAVSS_PSIIL_RT_BRIDGE_NAVSS_MCU_UDMASS_PSISS0_NAVSS_PSIIL_RT_BRIDGE_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_navss_psil_rt_bridge_navss_mcu_udmass_psilss0_navss_psil_rt_bridge_edc_ctrl_busecc_pend

Table 11-62. MCU_NAVSS_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	UDMASS_INTA0_GC_EC_C_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_gc_ecc_pend
1	UDMASS_INTA0_MC_EC_C_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_mc_ecc_pend
0	UDMASS_INTA0_LC_EC_C_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for udmass_inta0_lc_ecc_pend

11.2.29 MCU_NAVSS_DED_ENABLE_CLR_REG3 Register (Offset = 1CCh) [reset = X]

MCU_NAVSS_DED_ENABLE_CLR_REG3 is shown in [Figure 11-30](#) and described in [Table 11-64](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 3

Table 11-63.
MCU_NAVSS_DED_ENABLE_CLR_REG3 Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 11CCh

Figure 11-30. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_4_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_3_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_2_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_1_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SCR3_SCR_NAVSS_MCU_UDMASS_P_SILSS0_CBA_SS_ETL_SCR3_SCR_EDC_CTL_BUSECC_0_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_D_DEF_EVT_P2P_BRIDGE_D_DEF_EVT_BRIDGE_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_D_ETL0_BRIDGE_DSRT_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_D_ETL0_BRIDGE_SRTC_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
15	14	13	12	11	10	9	8
NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRT_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSILSS0_CBASS_ETL_NAVSS_MCU_UDMASS_P_SILSS0_CBAS_S_ETL_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_P2P_BRIDGE_SAFEGRT_PDMA_MCU1_PSIL_S_ETL0_BRIDGE_DSRTC_BUSECC_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h
7	6	5	4	3	2	1	0

Figure 11-30. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register (continued)

NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_S_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI S_RESP_BRID GE_SRC_BUS ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSEC C_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_PDMA MCU1_PSI D_RESP_P2P BRIDGE_SAFE G_RT_PDMA MCU1_PSI_D RESP_BRIDG E_SRC_BUSEC C_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI D_RESP_BRID GE_DST_BUS ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_R ESP_NAVSS_MCU_UDMASS_P SS0_CBASS_R SS_RESP_SAF EG_RT_CPSW 0_PSI_D_RES P_P2P_BRIDG E_SAFEG_RT_CPSW0_PSI D_RESP_BRID GE_SRC_BUS ECC_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SS0_CBASS_D SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_2_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SS0_CBASS_D SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_1_ENABLE_CLR	NAVSS_MCU_UDMASS_PSI SS0_CBASS_D ATA_NAVSS_MCU_UDMASS_P SS0_CBASS_D SS_DATA_SCR 1_SCR_NAVSS_MCU_UDMAS S_PSISS0_CB ASS_DATA_SC R1_SCR_EDC CTRL_BUSEC C_0_ENABLE_CLR
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-64. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_4_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_4_pend
22	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_3_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_3_pend
21	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_2_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_2_pend
20	NAVSS_MCU_UDMASS_PSI SS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SISS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_PSISS0_CBA SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_1_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_1_pend

Table 11-64. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SC R3_SCR_NAVSS_MCU UDMASS_P SILSS0_CBASS_ETL_N SS_ETL_SCR3_SCR_ED C_CTRL_BUSECC_0_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_scr3_scr_navss_mcu_udmass_psilss0_cbass_etl_scr3 _scr_edc_ctrl_busecc_0_pend
18	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_D DEF_EVT_P2P_BRIDGE_ D_DEF_EVT_BRIDGE_B USECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_d_def_evt_p2p_bridge_d_def_evt_bridge_busecc_pen d
17	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_DST_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_dst_busecc_pend
16	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_D_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_D_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_d_etl0_p2p_bridge_safeg_r t_pdma_mcu1_psil_d_etl0_bridge_src_busecc_pend
15	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_DST_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_dst_busecc_pend
14	NAVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_N AVSS_MCU_UDMASS_P SILSS0_CBASS_ETL_SA FEG_RT_PDMA_MCU1_ PSIL_S_ETL0_P2P_BRID GE_SAFEG_RT_PDMA_ MCU1_PSIL_S_ETL0_BR IDGE_SRC_BUSECC_EN ABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_etl_navss_mcu_udmass_psilss 0_cbass_etl_safeg_rt_pdma_mcu1_psil_s_etl0_p2p_bridge_safeg_rt _pdma_mcu1_psil_s_etl0_bridge_src_busecc_pend
13	NAVSS_MCU_UDMASS_P SILSS0_CBASS_RESP_ NAVSS_MCU_UDMASS_ P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ SCR2_SCR_NAVSS_MC U_UDMASS_P SILSS0_CBASS_RESP_ EDC_CTRL_BUSECC_2 _ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psil ss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp _scr2_scr_edc_ctrl_busecc_2_pend

Table 11-64. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_1_pend
11	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SCR2_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_navss_mcu_udmass_psilss0_cbass_resp_scr2_scr_edc_ctrl_busecc_0_pend
10	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_dst_busecc_pend
9	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_PDMA_MCU1_PSI_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_s_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_s_resp_bridge_src_busecc_pend
8	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_S_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_dst_busecc_pend
7	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEG_RT_CPSW0_PSI_S_RESP_P2P_BRIDGE_SAFEG_RT_CPSW0_PSI_S_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_s_resp_p2p_bridge_safeg_rt_cpsw0_psil_s_resp_bridge_src_busecc_pend

Table 11-64. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_dst_busecc_pend
5	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_PDMA_MCU1_PSISS_D_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_pdma_mcu1_psil_d_resp_p2p_bridge_safeg_rt_pdma_mcu1_psil_d_resp_bridge_src_busecc_pend
4	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_CPSW0_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_CPSW0_PSISS_D_RESP_BRIDGE_DST_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_dst_busecc_pend
3	NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_NAVSS_MCU_UDMASS_PSISS0_CBASS_RESP_SAFEGR_RT_CPSW0_PSISS_D_RESP_P2P_BRIDGE_SAFEGR_RT_CPSW0_PSISS_D_RESP_BRIDGE_SRC_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_resp_navss_mcu_udmass_psilss0_cbass_resp_safeg_rt_cpsw0_psil_d_resp_p2p_bridge_safeg_rt_cpsw0_psil_d_resp_bridge_src_busecc_pend
2	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_2_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_2_pend
1	NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSISS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_1_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_1_pend

Table 11-64. MCU_NAVSS_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_NAVSS_MCU_UDMASS_PSILSS0_CBASS_DATA_SCR1_SCR_EDC_CTRL_BUSECC_0_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for navss_mcu_udmass_psilss0_cbass_data_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_navss_mcu_udmass_psilss0_cbass_data_scr1_scr_edc_ctrl_busecc_0_pend

11.2.30 MCU_NAVSS_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

MCU_NAVSS_AGGR_ENABLE_SET is shown in [Figure 11-31](#) and described in [Table 11-66](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

**Table 11-65. MCU_NAVSS_AGGR_ENABLE_SET
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1200h

Figure 11-31. MCU_NAVSS_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-66. MCU_NAVSS_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

11.2.31 MCU_NAVSS_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

MCU_NAVSS_AGGR_ENABLE_CLR is shown in [Figure 11-32](#) and described in [Table 11-68](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 11-67. MCU_NAVSS_AGGR_ENABLE_CLR Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1204h

Figure 11-32. MCU_NAVSS_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 11-68. MCU_NAVSS_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

11.2.32 MCU_NAVSS_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

MCU_NAVSS_AGGR_STATUS_SET is shown in [Figure 11-33](#) and described in [Table 11-70](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

**Table 11-69. MCU_NAVSS_AGGR_STATUS_SET
Instances**

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 1208h

Figure 11-33. MCU_NAVSS_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 11-70. MCU_NAVSS_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

11.2.33 MCU_NAVSS_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

MCU_NAVSS_AGGR_STATUS_CLR is shown in [Figure 11-34](#) and described in [Table 11-72](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 11-71. MCU_NAVSS_AGGR_STATUS_CLR Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_ECCAGGR0	2838 120Ch

Figure 11-34. MCU_NAVSS_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 11-72. MCU_NAVSS_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

11.3 MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Registers

[Table 13-58](#) lists the memory-mapped registers for the MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC. All register offset addresses not listed in [Table 13-58](#) should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Ring ISC Registers region is for security controls. The address map for this region is as follows:

Table 11-73.
MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC
Instances

Instance	Base Address
MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC	4582 0000h

Table 11-74. MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Registers

Offset	Acronym	Register Name	MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Physical Address
0h + formula	MCU_NAVSS_CONTROL_J	ISC a Region b Control Register	4582 0000h + formula
4h + formula	MCU_NAVSS_CONTROL2_J	ISC a Region b Control Register 2	4582 0004h + formula

11.3.1 MCU_NAVSS_CONTROL_J Register (Offset = 0h + formula) [reset = X]

MCU_NAVSS_CONTROL_J is shown in Figure 13-24 and described in Table 13-60.

Return to [Summary Table](#).

The ISC a Region b Control Register defines the control fields for the ISC.

Offset = 0h + (j * 20h); where j = 0h to 11Dh

Table 11-75. MCU_NAVSS_CONTROL_J Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_RINGACC0_I SC_ISC	4582 0000h + formula

Figure 11-35. MCU_NAVSS_CONTROL_J Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
R/W-X				R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
R/W-X		R/W-0h	R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 11-76. MCU_NAVSS_CONTROL_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Has precedence over priv set bits.
25-24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set.
23-22	RESERVED	R/W	X	
21	PASS	R/W	0h	No privID replacement, pass through value.
20	NONSEC	R/W	0h	Make outgoing non-secure. Has precedence over secure enable bits.
19-16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable.
15-8	PRIV_ID	R/W	X	Priv ID.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set the region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 11-77. Register Call Summary for MCU_NAVSS_CONTROL_J

MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Registers
<ul style="list-style-type: none">• MCU_NAVSS_CONTROL_J Register (Offset = 0h + formula) [reset = X]: [0]• MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Registers: [0]

11.3.2 MCU_NAVSS_CONTROL2_J Register (Offset = 4h + formula) [reset = X]

MCU_NAVSS_CONTROL2_J is shown in Figure 13-25 and described in Table 13-62.

Return to [Summary Table](#).

The ISC a Region b Control Register 2 defines the control fields for the ISC.

Offset = 4h + (j * 20h); where j = 0h to 11Dh

Table 11-78. MCU_NAVSS_CONTROL2_J Instances

Instance	Physical Address
MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC	4582 0004h + formula

Figure 11-36. MCU_NAVSS_CONTROL2_J Register

31	30	29	28	27	26	25	24
PASS_V	RESERVED			VIRTID			
R/W-0h	R/W-X			R/W-0h			
23	22	21	20	19	18	17	16
VIRTID							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-79. MCU_NAVSS_CONTROL2_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PASS_V	R/W	0h	No virtID replacement, pass through value.
30-28	RESERVED	R/W	X	
27-16	VIRTID	R/W	0h	Virt ID.
15-0	RESERVED	R/W	X	

Table 11-80. Register Call Summary for MCU_NAVSS_CONTROL2_J

MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Registers

- [MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Registers: \[0\]](#)
- [MCU_NAVSS_CONTROL2_J Register \(Offset = 4h + formula\) \[reset = X\]: \[0\]](#)

12 UDMA Registers

12.1 UDMASS_UDMAP0_CFG Registers

Table 12-2 lists the memory-mapped registers for the UDMASS_UDMAP0_CFG. All register offset addresses not listed in Table 12-2 should be considered as reserved locations and the register contents should not be modified.

The UDMA-P Control /Status Registers region. The address map for this region is as follows:

Table 12-1. UDMASS_UDMAP0_CFG Instances

Instance	Base Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0000h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0000h

Table 12-2. UDMASS_UDMAP0_CFG Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG Physical Address	MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG Physical Address
0h	UDMA_REVISION	Revision Register	3115 0000h	285C 0000h
4h	UDMA_PERF_CTRL	Performance Control Register	3115 0004h	285C 0004h
8h	UDMA_EMU_CTRL	Emulation Control Register	3115 0008h	285C 0008h
10h	UDMA_PSIL_TO	PSI-L Proxy Timeout Register	3115 0010h	285C 0010h
1Ch	UDMA.UTC_CTRL	External UTC Control Register	3115 001Ch	285C 001Ch
20h	UDMA_CAP0	Capabilities Register 0	3115 0020h	285C 0020h
24h	UDMA_CAP1	Capabilities Register 1	3115 0024h	285C 0024h
28h	UDMA_CAP2	Capabilities Register 2	3115 0028h	285C 0028h
2Ch	UDMA_CAP3	Capabilities Register 3	3115 002Ch	285C 002Ch
40h	UDMA_PERF0	mem0 Port Virtualization Tuning Register	3115 0040h	285C 0040h
44h	UDMA_PERF1	mem1 Port Virtualization Tuning Register	3115 0044h	285C 0044h
48h	UDMA_PERF2	memr Port Virtualization Tuning Register	3115 0048h	285C 0048h
4Ch	UDMA_PERF3	memw Port Virtualization Tuning Register	3115 004Ch	285C 004Ch
78h	UDMA_DBGADDR	Debug Address Register	3115 0078h	285C 0078h
7Ch	UDMA_DBGDATA	Debug Data Register	3115 007Ch	285C 007Ch
80h	UDMA_RFLOWFWOES	Rx Flow ID Firewall Output Event Steering Register	3115 0080h	285C 0080h
88h	UDMA_RFLOWFWSTAT	Rx Flow ID Firewall Status Register 0	3115 0088h	285C 0088h

12.1.1 UDMA_REVISION Register (Offset = 0h) [reset = 4E5A0200h]

UDMA_REVISION is shown in [Figure 12-1](#) and described in [Table 12-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 12-3. UDMA_REVISION Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0000h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0000h

Figure 12-1. UDMA_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-4E5Ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM			REVMIN				
R-0h				R-2h				R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 12-4. UDMA_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	4E5Ah	Module ID field
15-11	REVRTL	R	0h	RTL revision
10-8	REVMAJ	R	2h	Major
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor

12.1.2 UDMA_PERF_CTRL Register (Offset = 4h) [reset = X]

UDMA_PERF_CTRL is shown in [Figure 12-2](#) and described in [Table 12-6](#).

Return to [Summary Table](#).

The performance control register contains fields which can be used to adjust the performance of the UDMA-P in the system.

Table 12-5. UDMA_PERF_CTRL Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0004h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_G_CFG	285C 0004h

Figure 12-2. UDMA_PERF_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TIMEOUT_CNT															
R/W-X																R/W-40h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-6. UDMA_PERF_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TIMEOUT_CNT	R/W	40h	<p>This field sets the timeout duration in clock cycles.</p> <p>This field controls the minimum amount of time that an Rx channel will be required to wait when it encounters a buffer starvation condition and the Rx error handling bit is set to 1 (packet is to be preserved - no discard).</p> <p>If the Rx error handling bit in the flow table is cleared, this field will have no effect on the Rx operation.</p> <p>When this field is set to 0, the Rx engine will not force an Rx channel to wait after encountering a starvation event (the feature is disabled).</p> <p>When this field is set to a value other than 0, the Rx engine will force any channel whose associated flow had the Rx error handling bit asserted and which encounters starvation to wait for at least the specified # of clock cycles before coming into context again to check if entries have been added to the Free Queue.</p> <p>This is intended to control potentially debilitating effects on the Rx engine in the UDMA-P caused by scheduling channels which cannot perform work due to a lack of free descriptor/buffer resources.</p> <p>The exact # of clock cycles between scheduling attempts is not important and will not be exact.</p> <p>The only guarantee is that the # of cycles waited will be at least as large as the timeout_cnt.</p>

12.1.3 UDMA_EMU_CTRL Register (Offset = 8h) [reset = X]

UDMA_EMU_CTRL is shown in [Figure 12-3](#) and described in [Table 12-8](#).

Return to [Summary Table](#).

The emulation control register is used to control the behavior of the DMA when the emususp input is asserted.

Table 12-7. UDMA_EMU_CTRL Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0008h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0008h

Figure 12-3. UDMA_EMU_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						SOFT	FREE
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-8. UDMA_EMU_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	SOFT	R/W	0h	Soft
0	FREE	R/W	0h	Free

12.1.4 UDMA_PSIL_TO Register (Offset = 10h) [reset = X]

UDMA_PSIL_TO is shown in [Figure 12-4](#) and described in [Table 12-10](#).

Return to [Summary Table](#).

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrences on PSI-L configuration transactions issued by the built in PSI-L proxy.

Table 12-9. UDMA_PSIL_TO Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0010h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0010h

Figure 12-4. UDMA_PSIL_TO Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W-400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W-400h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-10. UDMA_PSIL_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a config access
30-16	RESERVED	R/W	X	
15-0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a configuration read or write transaction and asserting the tout bit

12.1.5 UDMA_UTC_CTRL Register (Offset = 1Ch) [reset = X]

UDMA_UTC_CTRL is shown in [Figure 12-5](#) and described in [Table 12-12](#).

Return to [Summary Table](#).

The external UTC control register provides a mapping of logical to physical thread IDs .

Table 12-11. UDMA_UTC_CTRL Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 001Ch
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 001Ch

Figure 12-5. UDMA_UTC_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																UTC_CHAN_START															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-12. UDMA_UTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	UTC_CHAN_START	R/W	0h	This field specifies the starting PSI-L thread number for the external UTC

12.1.6 UDMA_CAP0 Register (Offset = 20h) [reset = X]

UDMA_CAP0 is shown in [Figure 12-6](#) and described in [Table 12-14](#).

Return to [Summary Table](#).

The Capabilities Register 0 specifies which standard features this UDMA-P instance supports.

Table 12-13. UDMA_CAP0 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0020h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0020h

Figure 12-6. UDMA_CAP0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				GLOBAL_TRIG	LOCAL_TRIG	EOL	STATIC
R-X				R-1h	R-0h	R-1h	R-1h
15	14	13	12	11	10	9	8
TYPE15	TYPE14	TYPE13	TYPE12	TYPE11	TYPE10	TYPE9	TYPE8
R-1h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-1h	R-1h

LEGEND: R = Read Only; -n = value after reset

Table 12-14. UDMA_CAP0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19	GLOBAL_TRIG	R	1h	Global triggers 0 and 1 are supported
18	LOCAL_TRIG	R	0h	Dedicated local trigger is supported
17	EOL	R	1h	EOL field is supported
16	STATIC	R	1h	STATIC field is supported
15	TYPE15	R	1h	Type 15 TR is supported
14	TYPE14	R	0h	Type 14 TR is supported
13	TYPE13	R	0h	Type 13 TR is supported
12	TYPE12	R	0h	Type 12 TR is supported
11	TYPE11	R	0h	Type 11 TR is supported
10	TYPE10	R	0h	Type 10 TR is supported
9	TYPE9	R	0h	Type 9 TR is supported
8	TYPE8	R	0h	Type 8 TR is supported
7	TYPE7	R	0h	Type 7 TR is supported
6	TYPE6	R	0h	Type 6 TR is supported
5	TYPE5	R	0h	Type 5 TR is supported
4	TYPE4	R	0h	Type 4 TR is supported

Table 12-14. UDMA_CAP0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TYPE3	R	1h	Type 3 TR is supported
2	TYPE2	R	1h	Type 2 TR is supported
1	TYPE1	R	1h	Type 1 TR is supported
0	TYPE0	R	1h	Type 0 TR is supported

12.1.7 UDMA_CAP1 Register (Offset = 24h) [reset = X]

UDMA_CAP1 is shown in [Figure 12-7](#) and described in [Table 12-16](#).

Return to [Summary Table](#).

The Capabilities Register 1 specifies which standard features this UDMA-P instance supports.

Table 12-15. UDMA_CAP1 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0024h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_G_CFG	285C 0024h

Figure 12-7. UDMA_CAP1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				SECTR	DFMT	ELTYPE	AMODE
R-X				R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 12-16. UDMA_CAP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	SECTR	R	0h	Maximum second TR function that is supported
2	DFMT	R	0h	Maximum data reformatting function that is supported
1	ELTYPE	R	0h	Maximum element type value that is supported.
0	AMODE	R	0h	The maximum AMODE that is supported. If AMODE is supported then DIR field must be supported for that AMODE.

12.1.8 UDMA_CAP2 Register (Offset = 28h) [reset = X]

UDMA_CAP2 is shown in [Figure 12-8](#) and described in [Table 12-18](#).

Return to [Summary Table](#).

The Capabilities Register 2 specifies how many resources this UDMA-P instance supports.

Table 12-17. UDMA_CAP2 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0028h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0028h

Figure 12-8. UDMA_CAP2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					RCHAN_CNT								ECHAN_CNT								TCHAN_CNT										
R-X					R-X								R-X								R-X										

LEGEND: R = Read Only; -n = value after reset

Table 12-18. UDMA_CAP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R	X	
26-18	RCHAN_CNT	R	X	Rx internal channel count 8Ch in NAVSS0 30h in MCU_NAVSS0
17-9	ECHAN_CNT	R	X	Tx external channel count A0h in NAVSS0 0h in MCU_NAVSS0
8-0	TCHAN_CNT	R	X	Tx internal channel count 8Ch in NAVSS0 60h in MCU_NAVSS0

12.1.9 UDMA_CAP3 Register (Offset = 2Ch) [reset = X]

UDMA_CAP3 is shown in [Figure 12-9](#) and described in [Table 12-20](#).

Return to [Summary Table](#).

The Capabilities Register 3 specifies how many resources this UDMA-P instance supports.

Table 12-19. UDMA_CAP3 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 002Ch
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 002Ch

Figure 12-9. UDMA_CAP3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UCHAN_CNT								HCHAN_CNT								RFLOW_CNT															
R-X								R-X								R-X															

LEGEND: R = Read Only; -n = value after reset

Table 12-20. UDMA_CAP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	UCHAN_CNT	R	X	Tx ultra high capacity internal channel count 4h in NAVSS0 0h in MCU_NAVSS0
22-14	HCHAN_CNT	R	X	Tx high capacity internal channel count 10h in NAVSS0 2 in MCU_NAVSS0
13-0	RFLOW_CNT	R	X	Rx flow table entry count 12Ch in NAVSS0 60h in MCU_NAVSS0

12.1.10 UDMA_PERF0 Register (Offset = 31150040h) [reset = X]

UDMA_PERF0 is shown in [Figure 12-10](#) and described in [Table 12-22](#).

Return to [Summary Table](#).

This register provides thresholds for outstanding virtualized read/write commands from interface mem0

Table 12-21. UDMA_PERF0 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0040h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0040h

Figure 12-10. UDMA_PERF0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								VRD_THRESH0							
R/W-X								R/W-8h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VWR_THRESH0							
R/W-X								R/W-8h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-22. UDMA_PERF0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	VRD_THRESH0	R/W	8h	Virt read command throttling threshold for mem0. Dispatching will be disabled for virtualized channels whenever the current virtualized read count from this interface meets or exceeds this value.
15-8	RESERVED	R/W	X	
7-0	VWR_THRESH0	R/W	8h	Virt write command throttling threshold for mem0. Dispatching will be disabled for virtualized channels whenever the current virtualized write count from this interface meets or exceeds this value.

12.1.11 UDMA_PERF1 Register (Offset = 31150044h) [reset = X]

UDMA_PERF1 is shown in [Figure 12-11](#) and described in [Table 12-24](#).

Return to [Summary Table](#).

This register provides thresholds for outstanding virtualized read/write commands from interface mem1

Table 12-23. UDMA_PERF1 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0044h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0044h

Figure 12-11. UDMA_PERF1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								VRD_THRESH1							
R/W-X								R/W-8h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VWR_THRESH1							
R/W-X								R/W-8h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-24. UDMA_PERF1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	VRD_THRESH1	R/W	8h	Virt read command throttling threshold for mem1. Dispatching will be disabled for virtualized channels whenever the current virtualized read count from this interface meets or exceeds this value.
15-8	RESERVED	R/W	X	
7-0	VWR_THRESH1	R/W	8h	Virt write command throttling threshold for mem1. Dispatching will be disabled for virtualized channels whenever the current virtualized write count from this interface meets or exceeds this value.

12.1.12 UDMA_PERF2 Register (Offset = 31150048h) [reset = X]

UDMA_PERF2 is shown in [Figure 12-12](#) and described in [Table 12-26](#).

Return to [Summary Table](#).

This register provides thresholds for outstanding virtualized read commands from interface memr

Table 12-25. UDMA_PERF2 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0048h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0048h

Figure 12-12. UDMA_PERF2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED									VRD_THRESH2						
R/W-X									R/W-10h						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-X															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-26. UDMA_PERF2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	VRD_THRESH2	R/W	10h	Virt read command throttling threshold for memr. Dispatching will be disabled for virtualized channels whenever the current virtualized read count from this interface meets or exceeds this value.
15-0	RESERVED	R/W	X	

12.1.13 UDMA_PERF3 Register (Offset = 3115004Ch) [reset = X]

UDMA_PERF3 is shown in [Figure 12-13](#) and described in [Table 12-28](#).

Return to [Summary Table](#).

This register provides thresholds for outstanding virtualized write commands from interface memw

Table 12-27. UDMA_PERF3 Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 004Ch
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 004Ch

Figure 12-13. UDMA_PERF3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VWR_THRESH3							
R/W-X								R/W-10h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-28. UDMA_PERF3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	VWR_THRESH3	R/W	10h	Virt write command throttling threshold for memw. Dispatching will be disabled for virtualized channels whenever the current virtualized write count from this interface meets or exceeds this value.

12.1.14 UDMA_DBGADDR Register (Offset = 31150078h) [reset = X]

UDMA_DBGADDR is shown in [Figure 12-14](#) and described in [Table 12-30](#).

Return to [Summary Table](#).

This register provides a writable address which allows debug information to be read from the Debug Data Register

Table 12-29. UDMA_DBGADDR Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0078h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFG	285C 0078h

Figure 12-14. UDMA_DBGADDR Register

31	30	29	28	27	26	25	24
DBG_EN	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
DBG_UNIT							
R/W-0h							
7	6	5	4	3	2	1	0
DBG_ADDR							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-30. UDMA_DBGADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DBG_EN	R/W	0h	Debug enable
30-16	RESERVED	R/W	X	
15-8	DBG_UNIT	R/W	0h	Selects which unit to read debug information from
7-0	DBG_ADDR	R/W	0h	Selects offset within unit to access separate debug registers

12.1.15 UDMA_DBGDATA Register (Offset = 3115007Ch) [reset = 0h]

UDMA_DBGDATA is shown in [Figure 12-15](#) and described in [Table 12-32](#).

Return to [Summary Table](#).

This register provides read only debug data

Table 12-31. UDMA_DBGDATA Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 007Ch
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFCG	285C 007Ch

Figure 12-15. UDMA_DBGDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DBG_DATA																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 12-32. UDMA_DBGDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DBG_DATA	R	0h	Provides debug information from various internal units. The value which is read back depends on which unit and register are selected in the Debug Address Register

12.1.16 UDMA_RFLOWFWOES Register (Offset = 80h) [reset = X]

UDMA_RFLOWFWOES is shown in [Figure 12-16](#) and described in [Table 12-34](#).

Return to [Summary Table](#).

The Rx Flow FW OES Register specifies a destination event number to which an event should be sent if an out of range flow ID is received on a packet.

Table 12-33. UDMA_RFLOWFWOES Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0080h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_GCFCG	285C 0080h

Figure 12-16. UDMA_RFLOWFWOES Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT_NUM															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-34. UDMA_RFLOWFWOES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT_NUM	R/W	FFFFh	This is the global event number to be generated

12.1.17 UDMA_RFLOWFWSTAT Register (Offset = 88h) [reset = X]

UDMA_RFLOWFWSTAT is shown in [Figure 12-17](#) and described in [Table 12-36](#).

Return to [Summary Table](#).

The Rx Flow FW Status Register 0 captures information about the thread/channel and received flow ID which failed a range check. Values in this register will remain persistent once an exception has been detected until the pend bit is written back to 0

Table 12-35. UDMA_RFLOWFWSTAT Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG	3115 0088h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_G_CFG	285C 0088h

Figure 12-17. UDMA_RFLOWFWSTAT Register

31	30	29	28	27	26	25	24
PEND	RESERVED	FLOWID					
R/W-0h	R/W-X	R/W-0h					
23	22	21	20	19	18	17	16
FLOWID							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							CHANNEL
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
CHANNEL							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-36. UDMA_RFLOWFWSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PEND	R/W	0h	This bit is set whenever the Flow ID firewall detects a Flow ID is out of range for an incoming packet. Once this bit is set, the remaining fields in this register will not be modified. SW is required to write this bit to 0 to allow another exception to be captured.
30	RESERVED	R/W	X	
29-16	FLOWID	R/W	0h	This is the flow ID that was received on the trapped packet
15-9	RESERVED	R/W	X	
8-0	CHANNEL	R/W	0h	This is the channel number on which the trapped packet was received

12.2 UDMASS_UDMAP0_CFG_RCHAN Registers

Table 12-38 lists the memory-mapped registers for the UDMASS_UDMAP0_CFG_RCHAN. All register offset addresses not listed in Table 12-38 should be considered as reserved locations and the register contents should not be modified.

The UDMA-P Rx Channel Configuration Registers region is accessed by setting the cdma_cfg_rsel signal to 3 during the access. The address map for this region is as follows:

**Table 12-37. UDMASS_UDMAP0_CFG_RCHAN
Instances**

Instance	Base Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0000h
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0000h

Table 12-38. UDMASS_UDMAP0_CFG_RCHAN Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG_RCHAN Physical Address	MCU_NAVSS0_UDMASS_UDMAP0_RCHAN Physical Address
0h + formula	UDMA_RCFG_j	Rx Channel Configuration	30C0 0000h + formula	284C 0000h + formula
14h + formula	UDMA_RCQ_j	Rx Channel Completion Queue	30C0 0014h + formula	284C 0014h + formula
20h + formula	UDMA_ROES_j	Rx Channel Output Event Steering 0	30C0 0020h + formula	284C 0020h + formula
60h + formula	UDMA_REOES_j	Rx Channel Error Output Event Steering 0	30C0 0060h + formula	284C 0060h + formula
64h + formula	UDMA_RPRI_CTRL_j	Rx Channel Priority Control	30C0 0064h + formula	284C 0064h + formula
68h + formula	UDMA_THREAD_j	Rx Channel Destination ThreadID Mapping	30C0 0068h + formula	284C 0068h + formula
80h + formula	UDMA_RST_SCHED_j	Rx Channel Static Scheduler Config	30C0 0080h + formula	284C 0080h + formula
F0h + formula	UDMA_RFLOW_RNG_j	Rx Channel Flow Range	30C0 00F0h + formula	284C 00F0h + formula

12.2.1 UDMA_RCFG_j Register (Offset = 0h + formula) [reset = X]

UDMA_RCFG_j is shown in [Figure 12-18](#) and described in [Table 12-40](#).

Return to [Summary Table](#).

The Rx Channel Configuration Register is used to initialize static mode settings for the Rx DMA channel. This register may only be written when the channel is disabled (rx_enable in realtime control reg is 0).

Offset = 0h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-39. UDMA_RCFG_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0000h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0000h + formula

Figure 12-18. UDMA_RCFG_j Register

31	30	29	28	27	26	25	24
PAUSE_ON_ERR	RESERVED					ATYPE	
R/W-0h	R/W-X					R/W-0h	
23	22	21	20	19	18	17	16
RESERVED				CHAN_TYPE			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
IGNORE_SHORT	IGNORE_LONG	RESERVED		BURST_SIZE		RESERVED	
R/W-0h	R/W-0h	R/W-X		R/W-1h		R/W-X	
7	6	5	4	3	2	1	0
RESERVED		FETCH_SIZE					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-40. UDMA_RCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel.
30-26	RESERVED	R/W	X	

Table 12-40. UDMA_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25-24	ATYPE	R/W	0h	<p>This field controls how pointers will be interpreted for non Ring Accelerator accesses on this channel.</p> <p>The values are encoded as follows:</p> <ul style="list-style-type: none"> 0 = Pointers are physical addresses 1 = Pointers are intermediate addresses which require intermediate to physical transaction before they can be decoded 2 = Pointers are virtual addresses which require virtual to physical translation before they can be decoded. <p>All transactions from this channel which are not destined to the Ring Accelerator will have the mem*_catype attribute set equal to the value given in this register field.</p> <p>Accesses to the RA will always use physical addresses.</p>
23-20	RESERVED	R/W	X	
19-16	CHAN_TYPE	R/W	0h	<p>Rx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host.</p> <p>Available channel types are as follows:</p> <ul style="list-style-type: none"> 0 = RESERVED 1 = RESERVED 2 = Channel performs packet oriented data transfers using pass by reference rings. <p>Channels configured in this mode can only use Host and Monolithic descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator.</p> <ul style="list-style-type: none"> 3 = Channel performs packet oriented data transfers using pass by reference rings with single buffer packet mode enabled. <p>Channels configured in this mode can only use Host descriptors and each descriptor will be processed as an independent packet (no buffer chaining).</p> <p>This is the only packet oriented mode that can be used with data sources that are infinite streams (no EOP)</p> <ul style="list-style-type: none"> 4 - 9 = RESERVED 10 = Channel performs Third Party DMA control transfers using pass by reference rings. <p>Channels configured in this mode can only use TR descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator.</p> <ul style="list-style-type: none"> 11 = Channel performs Third Party DMA control transfers using pass by value rings. <p>Channels configured in this mode will directly pass individual Transfer Request/Transfer Response messages from/to SW using rings in the Ring Accelerator.</p> <ul style="list-style-type: none"> 12 = Channel performs Third Party Block Copy DMA control transfers using pass by reference rings. <p>Channels configured in this mode are linked to the same index Rx channel to form a bonded read/write channel</p> <ul style="list-style-type: none"> 13 = Channel performs Third Party Block Copy DMA data transfers using pass by reference rings. <p>Channels configured in this mode are linked to the same index Rx channel to form a bonded read/write channel</p> <ul style="list-style-type: none"> 14 = Channel performs Third Party DMA data transfers using TRs provided via PSI-L (not supported in UDMA-P). 15 = Channel performs Third Party DMA data transfers using TRs provided via QDMA channel (not supported in UDMA-P)
15	IGNORE_SHORT	R/W	0h	<p>This field controls whether or not short packets will be treated as exceptions or ignored for the channel.</p> <p>This field is only used when the channel is in split UTC mode.</p> <p>The values are encoded as follows:</p> <ul style="list-style-type: none"> 0 = Short packets are treated as exceptions and handled appropriately. 1 = Short packets are ignored and the TR will continue to execute even if an EOP is encountered prematurely or the TR does not have EOP set.

Table 12-40. UDMA_RCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	IGNORE_LONG	R/W	0h	This field controls whether or not long packets will be treated as exceptions or ignored for the channel. This field is only used when the channel is in split UTC mode. The values are encoded as follows: 0 = Long packets are treated as exceptions and handled appropriately. 1 = Long packets are ignored and the next TR will be fetched even if the current TR is marked or interpreted as EOP.
13-12	RESERVED	R/W	X	
11-10	BURST_SIZE	R/W	1h	Specifies the nominal burst size and alignment for data transfers on this channel. 0 = RESERVED 1 = 64 bytes 2 = 128 bytes 3 = 256 bytes This field may only be set to values for which the Rx Per Channel FIFO has sufficient storage. Receive Data fetches are not allowed to initiate unless sufficient accumulated data greater than or equal to the rx_burst_size value exists in the Rx Per Channel Buffer for that channel. Care must be taken to ensure that the nominal burst size field is not set larger than the implemented Rx Data Per Channel FIFO. Unless otherwise noted, it should be assumed that only HC/UHC channels can be programmed to use a burst size greater than 64 bytes.
9-7	RESERVED	R/W	X	
6-0	FETCH_SIZE	R/W	0h	Specifies the # of 32-bit descriptor words to fetch. This must be set to the maximum word count that can pass through the channel for any allowed descriptor type.

12.2.2 UDMA_RCQ_j Register (Offset = 14h + formula) [reset = X]

UDMA_RCQ_j is shown in [Figure 12-19](#) and described in [Table 12-42](#).

Return to [Summary Table](#).

The Rx Channel Completion Queue Register is used to specify which queue the Transfer Responses will be returned to when operating in the pass by value TR based channel mode. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Offset = 14h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-41. UDMA_RCQ_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0014h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0014h + formula

Figure 12-19. UDMA_RCQ_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RXCQ_QNUM															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-42. UDMA_RCQ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	RXCQ_QNUM	R/W	0h	Specifies the queue number to return pass by value Transfer Responses and teardown completion teardown messages to.

12.2.3 UDMA_ROES_j Register (Offset = 20h + formula) [reset = X]

UDMA_ROES_j is shown in [Figure 12-20](#) and described in [Table 12-44](#).

Return to [Summary Table](#).

The Output Event Steering Registers are used to specify a global event number to generate anytime the required event generation criteria specified in a TR are met. A single event with the event number set equal to the value in the corresponding register will be generated. This register is provided in order to allow security SW to lock down which events in the global space any given channel/ thread is allowed to generate.

Offset = 20h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-43. UDMA_ROES_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0020h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0020h + formula

Figure 12-20. UDMA_ROES_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT_NUM															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-44. UDMA_ROES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT_NUM	R/W	FFFFh	This is the global event number to be generated

12.2.4 UDMA_REOES_j Register (Offset = 60h + formula) [reset = X]

UDMA_REOES_j is shown in [Figure 12-21](#) and described in [Table 12-46](#).

Return to [Summary Table](#).

The Error Output Event Steering Registers are used to specify a global event number to generate anytime an error is encountered on the channel. A single event with the event number set equal to the value in the corresponding register will be generated. This register is provided in order to allow security SW to lock down which events in the global space any given channel/ thread is allowed to generate.

Offset = 60h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-45. UDMA_REOES_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0060h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0000h + formula

Figure 12-21. UDMA_REOES_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT_NUM															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-46. UDMA_REOES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT_NUM	R/W	FFFFh	This is the global event number to be generated

12.2.5 UDMA_RPRI_CTRL_j Register (Offset = 64h + formula) [reset = X]

UDMA_RPRI_CTRL_j is shown in [Figure 12-22](#) and described in [Table 12-48](#).

Return to [Summary Table](#).

The priority control register is used to control the priority of the transactions which the DMA generates on it's master interface.

Offset = 64h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-47. UDMA_RPRI_CTRL_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0064h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0064h + formula

Figure 12-22. UDMA_RPRI_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESE RVED	PRIORITY			RESERVED										QOS	
R/W-X	R/W-0h			R/W-X										R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ORDERID			
R/W-X												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-48. UDMA_RPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRIORITY	R/W	0h	Rx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem*_cepriority outputs during all transactions for this channel.
27-19	RESERVED	R/W	X	
18-16	QOS	R/W	0h	Rx Quality of Service Level: This field contains the 3-bit value which will be output on the mem*_cqos output during all transactions for this channel.
15-4	RESERVED	R/W	X	
3-0	ORDERID	R/W	0h	Rx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel.

12.2.6 UDMA_THREAD_j Register (Offset = 68h + formula) [reset = X]

UDMA_THREAD_j is shown in [Figure 12-23](#) and described in [Table 12-50](#).

Return to [Summary Table](#).

The thread ID mapping register is used to pair the Rx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Offset = 68h + (j * 100h); where j = 0h to 95h

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-49. UDMA_THREAD_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0068h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0068h + formula

Figure 12-23. UDMA_THREAD_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ID															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-50. UDMA_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	ID	R/W	0h	Thread ID: This field contains the 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel.

12.2.7 UDMA_RST_SCHED_j Register (Offset = 80h + formula) [reset = X]

UDMA_RST_SCHED_j is shown in [Figure 12-24](#) and described in [Table 12-52](#).

Return to [Summary Table](#).

The Rx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Offset = 80h + (j * 100h); where j = 0h to 95h

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-51. UDMA_RST_SCHED_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 0080h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 0080h + formula

Figure 12-24. UDMA_RST_SCHED_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-52. UDMA_RST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	

Table 12-52. UDMA_RST_SCHED_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PRIORITY	R/W	0h	<p>Rx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Rx DMA units.</p> <p>This field is encoded as follows:</p> <p>0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority</p> <p>Arbitration between bins is performed in a strict priority fashion.</p> <p>High priority channels will always be serviced first.</p> <p>If no high priority channels are requesting then all medium-high priority channels will be serviced next.</p> <p>If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next.</p> <p>When no other channels are requesting, the low priority channels will be serviced.</p> <p>All channels within a given bin are serviced in a round robin order.</p> <p>Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration.</p>

12.2.8 UDMA_RFLOW_RNG_j Register (Offset = F0h + formula) [reset = X]

UDMA_RFLOW_RNG_j is shown in [Figure 12-25](#) and described in [Table 12-54](#).

Return to [Summary Table](#).

The flow range register is used to control which flows other than the default flow (0x3FFF / channel_number) are allowed to be used with this DMA channel.

Offset = F0h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_RCHAN

Table 12-53. UDMA_RFLOW_RNG_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHAN	30C0 00F0h + formula
MCU_NAVSS0_UDMASS_UDMAP0_RCHAN	284C 00F0h + formula

Figure 12-25. UDMA_RFLOW_RNG_j Register

31	30	29	28	27	26	25	24
RESERVED	FLOWID_CNT						
R/W-X	R/W-4000h						
23	22	21	20	19	18	17	16
FLOWID_CNT							
R/W-4000h							
15	14	13	12	11	10	9	8
RESERVED	FLOWID_START						
R/W-X	R/W-0h						
7	6	5	4	3	2	1	0
FLOWID_START							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-54. UDMA_RFLOW_RNG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-16	FLOWID_CNT	R/W	4000h	Rx Flow ID Count: This field specifies how many flow IDs are in the additional contiguous range of legal flow IDs for this channel. A value of 0 indicates that no flow IDs other than the default are allowed for the channel..
15-14	RESERVED	R/W	X	
13-0	FLOWID_START	R/W	0h	Rx Starting Flow ID: Beyond the default flow ID, each channel can also make use of a single contiguous range of flow IDs and this field specifies the starting index for that range..

12.3 UDMASS_UDMAP0_CFG_RCHANRT Registers

Table 12-56 lists the memory-mapped registers for the UDMASS_UDMAP0_CFG_RCHANRT. All register offset addresses not listed in Table 12-56 should be considered as reserved locations and the register contents should not be modified.

The UDMA-P Rx Channel Realtime Registers region is accessed by setting the cdma_cfg_rsel signal to 5 during the access. The address map for this region is as follows:

Table 12-55. UDMASS_UDMAP0_CFG_RCHANRT Instances

Instance	Base Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT	3400 0000h
MCU_NAVSS0_UDMASS_UDMAP_RCHANRT	2A80 0000h

Table 12-56. UDMASS_UDMAP0_CFG_RCHANRT Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT Physical Address	MCU_NAVSS0_UDMASS_UDMAP_RCHANRT Physical Address
0h + formula	UDMA_RRT_CTL_j	Rx Channel Realtime Control Register	3400 0000h + formula	2A80 0000h + formula
8h + formula	UDMA_RRT_SWTRIG_j	Rx Channel Realtime Software Trigger Register	3400 0008h + formula	2A80 0008h + formula
80h + formula	UDMA_RRT_STDATA_j_y	Rx Channel Realtime State Data Register	3400 0080h + formula	2A80 0080h + formula
200h + formula	UDMA_RRT_PEER0_j	Rx Channel Real-time Remote Peer Register 0	3400 0200h + formula	2A80 0200h + formula
204h + formula	UDMA_RRT_PEER1_j	Rx Channel Real-time Remote Peer Register 1	3400 0204h + formula	2A80 0204h + formula
208h + formula	UDMA_RRT_PEER2_j	Rx Channel Real-time Remote Peer Register 2	3400 0208h + formula	2A80 0208h + formula
20Ch + formula	UDMA_RRT_PEER3_j	Rx Channel Real-time Remote Peer Register 3	3400 020Ch + formula	2A80 020Ch + formula
210h + formula	UDMA_RRT_PEER4_j	Rx Channel Real-time Remote Peer Register 4	3400 0210h + formula	2A80 0210h + formula
214h + formula	UDMA_RRT_PEER5_j	Rx Channel Real-time Remote Peer Register 5	3400 0214h + formula	2A80 0214h + formula
218h + formula	UDMA_RRT_PEER6_j	Rx Channel Real-time Remote Peer Register 6	3400 0218h + formula	2A80 0218h + formula
21Ch + formula	UDMA_RRT_PEER7_j	Rx Channel Real-time Remote Peer Register 7	3400 021Ch + formula	2A80 021Ch + formula
220h + formula	UDMA_RRT_PEER8_j	Rx Channel Real-time Remote Peer Register 8	3400 0220h + formula	2A80 0220h + formula
224h + formula	UDMA_RRT_PEER9_j	Rx Channel Real-time Remote Peer Register 9	3400 0224h + formula	2A80 0224h + formula
228h + formula	UDMA_RRT_PEER10_j	Rx Channel Real-time Remote Peer Register 10	3400 0228h + formula	2A80 0228h + formula
22Ch + formula	UDMA_RRT_PEER11_j	Rx Channel Real-time Remote Peer Register 11	3400 022Ch + formula	2A80 022Ch + formula
230h + formula	UDMA_RRT_PEER12_j	Rx Channel Real-time Remote Peer Register 12	3400 0230h + formula	2A80 0230h + formula
234h + formula	UDMA_RRT_PEER13_j	Rx Channel Real-time Remote Peer Register 13	3400 0234h + formula	2A80 0234h + formula
238h + formula	UDMA_RRT_PEER14_j	Rx Channel Real-time Remote Peer Register 14	3400 0238h + formula	2A80 0238h + formula
23Ch + formula	UDMA_RRT_PEER15_j	Rx Channel Real-time Remote Peer Register 15	3400 023Ch + formula	2A80 023Ch + formula

Table 12-56. UDMASS_UDMAP0_CFG_RCHANRT Registers (continued)

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT Physical Address	MCU_NAVSS0_UDMASS_UDMAP_RCHANRT Physical Address
400h + formula	UDMA_RRT_PCNT_J	Rx Channel Real-time Packet Count Statistics Register	3400 0400h + formula	2A80 0400h + formula
408h + formula	UDMA_RRT_BCNT_J	Rx Channel Real-time Completed Byte Count Statistics Register	3400 0408h + formula	2A80 0408h + formula
410h + formula	UDMA_RRT_SBCNT_J	Rx Channel Real-time Started Byte Count Statistics Register	3400 0410h + formula	2A80 0410h + formula

12.3.1 UDMA_RRT_CTL_j Register (Offset = 0h + formula) [reset = X]

UDMA_RRT_CTL_j is shown in [Figure 12-26](#) and described in [Table 12-58](#).

Return to [Summary Table](#).

The Rx Channel Realtime Control Register contains real-time control and status information for the Rx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Offset = 0h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-57. UDMA_RRT_CTL_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0000h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0000h + formula

Figure 12-26. UDMA_RRT_CTL_j Register

31	30	29	28	27	26	25	24
EN	TDOWN	PAUSE	FTDOWN	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ERROR
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-58. UDMA_RRT_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	<p>This field enables or disables the channel.</p> <p>Disabling a channel halts operation on the channel after the current block transfer is completed.</p> <p>Disabling a channel in the middle of a packet transfer may result in overflow conditions in the attached application and data loss.</p> <p>When a channel is disabled, the implementation may choose to reset all state for the channel.</p> <p>The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel.</p> <p>This field is encoded as follows:</p> <p>0 = channel is disabled</p> <p>1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete.</p> <p>If the host is enabling a channel that is just being set up, the host must initialize all of the other channel configuration fields before setting this bit.</p>

Table 12-58. UDMA_RRT_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	TDOWN	R/W	0h	This field indicates whether or not an Rx teardown operation is complete. This field should be cleared when a channel is initialized. This field will be set after a channel teardown is complete.
29	PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately.
28	FTDOWN	R/W	0h	Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events. When this bit is set, the implementation may choose to bypass data transfers and event generation. This bit is a modifier to the normal rx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the UDMA even if the trigger source is no longer functioning. Use of this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc. This bit should be set in addition to the rx_teardown bit in order to cause a forced teardown. This field will remain set after a channel teardown is complete.
27-1	RESERVED	R/W	X	
0	ERROR	R	0h	Channel error: This bit will be set anytime an error has occurred on the channel. This bit is cleared when the channel is disabled and re-enabled.

12.3.2 UDMA_RRT_SWTRIG_j Register (Offset = 8h + formula) [reset = X]

UDMA_RRT_SWTRIG_j is shown in [Figure 12-27](#) and described in [Table 12-60](#).

Return to [Summary Table](#).

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the rx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Offset = 8h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-59. UDMA_RRT_SWTRIG_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0008h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0008h + formula

Figure 12-27. UDMA_RRT_SWTRIG_j Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 12-60. UDMA_RRT_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TRIGGER	W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel

12.3.3 UDMA_RRT_STDATA_j_y Register (Offset = 80h + formula) [reset = 0h]

UDMA_RRT_STDATA_j_y is shown in [Figure 12-28](#) and described in [Table 12-62](#).

Return to [Summary Table](#).

The State Data Registers contain the current working state of the Rx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the UDMA-P is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Offset = 80h + (j * 1000h) + (y * 4h); where

j = 0h to 8Bh, y = 0h to 1Fh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh, y = 0h to 1Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-61. UDMA_RRT_STDATA_j_y Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0080h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0080h + formula

Figure 12-28. UDMA_RRT_STDATA_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATE_INFO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-62. UDMA_RRT_STDATA_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATE_INFO	R/W	0h	See Rx state mapping table

12.3.4 UDMA_RRT_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

UDMA_RRT_PEER0_j is shown in [Figure 12-29](#) and described in [Table 12-64](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x400.

Offset = 200h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-63. UDMA_RRT_PEER0_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0200h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0200h + formula

Figure 12-29. UDMA_RRT_PEER0_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-64. UDMA_RRT_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.5 UDMA_RRT_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

UDMA_RRT_PEER1_j is shown in [Figure 12-30](#) and described in [Table 12-66](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x401.

Offset = 204h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-65. UDMA_RRT_PEER1_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0204h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0204h + formula

Figure 12-30. UDMA_RRT_PEER1_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-66. UDMA_RRT_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.6 UDMA_RRT_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

UDMA_RRT_PEER2_j is shown in [Figure 12-31](#) and described in [Table 12-68](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x402.

Offset = 208h + (j * 1000h); where j = 0h to 95h

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-67. UDMA_RRT_PEER2_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0208h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0208h + formula

Figure 12-31. UDMA_RRT_PEER2_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-68. UDMA_RRT_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.7 UDMA_RRT_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

UDMA_RRT_PEER3_j is shown in [Figure 12-32](#) and described in [Table 12-70](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x403.

Offset = 20Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-69. UDMA_RRT_PEER3_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 020Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 020Ch + formula

Figure 12-32. UDMA_RRT_PEER3_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-70. UDMA_RRT_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.8 UDMA_RRT_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

UDMA_RRT_PEER4_j is shown in [Figure 12-33](#) and described in [Table 12-72](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x404.

Offset = 210h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-71. UDMA_RRT_PEER4_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0210h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0210h + formula

Figure 12-33. UDMA_RRT_PEER4_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-72. UDMA_RRT_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.9 UDMA_RRT_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

UDMA_RRT_PEER5_j is shown in [Figure 12-34](#) and described in [Table 12-74](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x405.

Offset = 214h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-73. UDMA_RRT_PEER5_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0214h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0214h + formula

Figure 12-34. UDMA_RRT_PEER5_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-74. UDMA_RRT_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.10 UDMA_RRT_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

UDMA_RRT_PEER6_j is shown in [Figure 12-35](#) and described in [Table 12-76](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x406.

Offset = 218h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-75. UDMA_RRT_PEER6_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0218h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0218h + formula

Figure 12-35. UDMA_RRT_PEER6_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-76. UDMA_RRT_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.11 UDMA_RRT_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

UDMA_RRT_PEER7_j is shown in [Figure 12-36](#) and described in [Table 12-78](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x407.

Offset = 21Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-77. UDMA_RRT_PEER7_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 021Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 021Ch + formula

Figure 12-36. UDMA_RRT_PEER7_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-78. UDMA_RRT_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.12 UDMA_RRT_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

UDMA_RRT_PEER8_j is shown in [Figure 12-37](#) and described in [Table 12-80](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x408.

Offset = 220h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-79. UDMA_RRT_PEER8_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0220h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0220h + formula

Figure 12-37. UDMA_RRT_PEER8_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-80. UDMA_RRT_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.13 UDMA_RRT_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

UDMA_RRT_PEER9_j is shown in [Figure 12-38](#) and described in [Table 12-82](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x409.

Offset = 224h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-81. UDMA_RRT_PEER9_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0224h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0224h + formula

Figure 12-38. UDMA_RRT_PEER9_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-82. UDMA_RRT_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.14 UDMA_RRT_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

UDMA_RRT_PEER10_j is shown in [Figure 12-39](#) and described in [Table 12-84](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40A.

Offset = 228h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-83. UDMA_RRT_PEER10_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0228h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0228h + formula

Figure 12-39. UDMA_RRT_PEER10_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-84. UDMA_RRT_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.15 UDMA_RRT_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

UDMA_RRT_PEER11_j is shown in [Figure 12-40](#) and described in [Table 12-86](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40B.

Offset = 22Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-85. UDMA_RRT_PEER11_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 022Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 022Ch + formula

Figure 12-40. UDMA_RRT_PEER11_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-86. UDMA_RRT_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.16 UDMA_RRT_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

UDMA_RRT_PEER12_j is shown in [Figure 12-41](#) and described in [Table 12-88](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40C.

Offset = 230h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-87. UDMA_RRT_PEER12_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0230h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0230h + formula

Figure 12-41. UDMA_RRT_PEER12_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-88. UDMA_RRT_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.17 UDMA_RRT_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

UDMA_RRT_PEER13_j is shown in [Figure 12-42](#) and described in [Table 12-90](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40D.

Offset = 234h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-89. UDMA_RRT_PEER13_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0234h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0234h + formula

Figure 12-42. UDMA_RRT_PEER13_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-90. UDMA_RRT_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.18 UDMA_RRT_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

UDMA_RRT_PEER14_j is shown in [Figure 12-43](#) and described in [Table 12-92](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40E.

Offset = 238h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-91. UDMA_RRT_PEER14_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT	3400 0238h + formula
MCU_NAVSS0_UDMASS_UDMAP_RCHANRT	2A80 0238h + formula

Figure 12-43. UDMA_RRT_PEER14_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-92. UDMA_RRT_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.19 UDMA_RRT_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

UDMA_RRT_PEER15_j is shown in [Figure 12-44](#) and described in [Table 12-94](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40F.

Offset = 23Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-93. UDMA_RRT_PEER15_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 023Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 023Ch + formula

Figure 12-44. UDMA_RRT_PEER15_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-94. UDMA_RRT_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.3.20 UDMA_RRT_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

UDMA_RRT_PCNT_j is shown in [Figure 12-45](#) and described in [Table 12-96](#).

Return to [Summary Table](#).

The statistics registers are supplied to give software applications operational progress status for the channel.

Offset = 400h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-95. UDMA_RRT_PCNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0400h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0400h + formula

Figure 12-45. UDMA_RRT_PCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-96. UDMA_RRT_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PCNT	R/W	0h	Current completed packet count for the channel.

12.3.21 UDMA_RRT_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

UDMA_RRT_BCNT_j is shown in [Figure 12-46](#) and described in [Table 12-98](#).

Return to [Summary Table](#).

The statistics registers are supplied to give software applications operational progress status for the channel.

Offset = 408h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-97. UDMA_RRT_BCNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0408h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0408h + formula

Figure 12-46. UDMA_RRT_BCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-98. UDMA_RRT_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCNT	R/W	0h	Current completed payload byte count for the channel.

12.3.22 UDMA_RRT_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

UDMA_RRT_SBCNT_j is shown in [Figure 12-47](#) and described in [Table 12-100](#).

Return to [Summary Table](#).

The statistics registers are supplied to give software applications operational progress status for the channel.

Offset = 410h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_RCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_RCHANRT

Table 12-99. UDMA_RRT_SBCNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RC HANRT	3400 0410h + formula
MCU_NAVSS0_UDMASS_UDMAP_RC HANRT	2A80 0410h + formula

Figure 12-47. UDMA_RRT_SBCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-100. UDMA_RRT_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SBCNT	R/W	0h	Current started byte count for the channel.

12.4 UDMASS_UDMAP0_CFG_RFLOW Registers

Table 12-102 lists the memory-mapped registers for the UDMASS_UDMAP0_CFG_RFLOW. All register offset addresses not listed in Table 12-102 should be considered as reserved locations and the register contents should not be modified.

The UDMA-P Rx Flow Table Registers region is accessed by setting the cdma_cfg_rsel signal to 1 during the access. The address map for this region is as follows:

**Table 12-101. UDMASS_UDMAP0_CFG_RFLOW
Instances**

Instance	Base Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0000h
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLO W	2840 0000h

Table 12-102. UDMASS_UDMAP0_CFG_RFLOW Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDM AP0_CFG_RFLOW Physical Address	MCU_NAVSS0_UDMASS _UDMAP0_CFG_RFLOW Physical Address
0h + formula	UDMA_RFA_j	Rx Flow Config Register A	30D0 0000h + formula	2840 0000h + formula
4h + formula	UDMA_RFB_j	Rx Flow Config Register B	30D0 0004h + formula	2840 0004h + formula
8h + formula	UDMA_RFC_j	Rx Flow Config Register C	30D0 0008h + formula	2840 0008h + formula
Ch + formula	UDMA_RFD_j	Rx Flow Config Register D	30D0 000Ch + formula	2840 000Ch + formula
10h + formula	UDMA_RFE_j	Rx Flow Config Register E	30D0 0010h + formula	2840 0010h + formula
14h + formula	UDMA_RFF_j	Rx Flow Config Register F	30D0 0014h + formula	2840 0014h + formula
18h + formula	UDMA_RFG_j	Rx Flow Config Register G	30D0 0018h + formula	2840 0018h + formula
1Ch + formula	UDMA_RFH_j	Rx Flow Config Register H	30D0 001Ch + formula	2840 001Ch + formula

12.4.1 UDMA_RFA_j Register (Offset = 0h + formula) [reset = X]

UDMA_RFA_j is shown in [Figure 12-48](#) and described in [Table 12-104](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register A contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

Offset = 0h + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-103. UDMA_RFA_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0000h + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 0000h + formula

Figure 12-48. UDMA_RFA_j Register

31	30	29	28	27	26	25	24
RESERVED	EINFO	PSINFO	ERR_HANDLING	DESC_TYPE		PS_LOC	SOP_OFF
R/W-X	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
SOP_OFF							
R/W-0h							
15	14	13	12	11	10	9	8
DEST_QNUM							
R/W-0h							
7	6	5	4	3	2	1	0
DEST_QNUM							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-104. UDMA_RFA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30	EINFO	R/W	0h	Rx Extended Packet Info Block Present: This bit controls whether or not the Extended Packet Info Block will be present in the Rx Packet Descriptor. If this bit is clear, the port DMA will clear the Extended Packet Info Present bit in the PD and will drop any Timestamp or SW Data words that are presented from the back end application. If this bit is set, the port DMA will set the Extended Packet Info Block Present bit in the PD and will copy any Timestamp or SW Data words that are presented across the Rx streaming interface into the Extended Packet Info Block words in the descriptor. If no Timestamp or SW Data words are presented from the back end application, the port DMA will overwrite the fields in the PD with zeroes.

Table 12-104. UDMA_RFA_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	PSINFO	R/W	0h	Rx PS Words Present: This bit controls whether or not the Protocol Specific words will be present in the Rx Packet Descriptor. If this bit is clear, the port DMA will set the PS word count to 0 in the PD and will drop any PS words that are presented from the back end application. If this bit is set, the port DMA will set the PS word count to the value given by the back end application and will copy the PS words from the back end application to the location
28	ERR_HANDLING	R/W	0h	Rx Error Handling Mode: This bit controls the error handling mode for the flow and is only used when channel errors (i.e. descriptor or buffer starvation occurs): 0 = Starvation errors result in dropping packet and reclaiming any used descriptor or buffer resources back to the original queues/pools they were allocated from 1 = Starvation errors result in subsequent re-try of the descriptor allocation operation. In this mode, the DMA will save it's internal operational state back to the internal state RAM without issuing an advance operation to it's internal FIFO buffers. This results in the DMA re-initiating the data transfer at a later time with the intention that additional free buffers and/or descriptors will have been added.
27-26	DESC_TYPE	R/W	0h	Rx Descriptor Type: This field indicates the descriptor type to use: 0 = Host 1 = RESERVED 2 = Monolithic 3 = RESERVED
25	PS_LOC	R/W	0h	Rx Protocol Specific Location: This bit controls where the Protocol Specific words will be placed in the Host Mode data structure. If this bit is cleared, the DMA will clear the Protocol Specific Region Location bit in the PD and will place the Protocol Specific Words at the end of the Packet Descriptor. If this bit is set, the DMA will set the Protocol Specific Region Location bit in the PD and will place the Protocol Specific Words at the beginning of the data buffer. When this mode is used, it is required that the resulting target data buffer pointer (which is calculated by adding the host_rx_sop_offset to the original buffer pointer in the Packet Descriptor) is aligned to a 32-bit boundary to avoid unwanted buffer truncation as the DMA will round up to the next 32-bit aligned boundary.
24-16	SOP_OFF	R/W	0h	Rx Start of Packet Offset: This field specifies the number of bytes that are to be skipped in the SOP buffer before beginning to write the payload or protocol specific bytes(if they are in the sop buffer). This value must be less than the minimum size of a buffer in the system. Valid values are 0 - 255 bytes. Note that for monolithic packets the value of this field must always be initialized to be greater than or equal to 4 times the maximum number of protocol specific 32-bit words that are required by any of the packet types that will be transferred by this channel. This is important as the primary purpose of this field is to ensure that space is left in the descriptor to place the protocol specific information without overwriting or being overwritten by the Rx data. The secondary purpose of this field is to allow space to be left prior to the data in the descriptor in case header information needs to be added as the packet is passed through the system.
15-0	DEST_QNUM	R/W	0h	Rx Destination Queue: This field indicates the default receive queue that packets on this flow should be placed onto.

12.4.2 UDMA_RFB_j Register (Offset = 4h + formula) [reset = 0h]

UDMA_RFB_j is shown in [Figure 12-49](#) and described in [Table 12-106](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register B contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

Offset = 4h + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-105. UDMA_RFB_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0004h + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 0004h + formula

Figure 12-49. UDMA_RFB_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRCTAG_HI								SRCTAG_LO							
R/W-0h								R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSTTAG_HI								DSTTAG_LO							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-106. UDMA_RFB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	SRCTAG_HI	R/W	0h	Rx Source Tag High Byte Constant Value: This is the value to insert into bits 15:8 of the source tag if the rx_src_tag_hi_sel is set to 1.
23-16	SRCTAG_LO	R/W	0h	Rx Source Tag Low Byte Constant Value: This is the value to insert into bits 7:0 of the source tag if the rx_src_tag_lo_sel is set to 1.
15-8	DSTTAG_HI	R/W	0h	Rx Destination Tag High Byte Constant Value: This is the value to insert into bits 15:8 of the destination tag if the rx_dest_tag_hi_sel is set to 1.
7-0	DSTTAG_LO	R/W	0h	Rx Destination Tag Low Byte Constant Value: This is the value to insert into bits 7:0 of the destination tag if the rx_dest_tag_lo_sel is set to 1.

12.4.3 UDMA_RFC_j Register (Offset = 8h + formula) [reset = X]

UDMA_RFC_j is shown in [Figure 12-50](#) and described in [Table 12-108](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register C contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

Offset = 8h + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-107. UDMA_RFC_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0008h + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 0008h + formula

Figure 12-50. UDMA_RFC_j Register

31	30	29	28	27	26	25	24
RESERVED	SRCTAG_HI_SEL			RESERVED	SRCTAG_LO_SEL		
R/W-X	R/W-0h			R/W-X	R/W-0h		
23	22	21	20	19	18	17	16
RESERVED	DSTTAG_HI_SEL			RESERVED	DSTTAG_LO_SEL		
R/W-X	R/W-0h			R/W-X	R/W-0h		
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED					SIZE_THRESH_EN		
R/W-X					R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-108. UDMA_RFC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	SRCTAG_HI_SEL	R/W	0h	Rx Source Tag Low Byte Selector: This field specifies the source for bits 7:0 of the source tag field in Word 3 of the output Packet Descriptor. This field is encoded as follows: 0 = do not overwrite 1 = overwrite with value given in rx_src_tag_hi 2 = overwrite with flow_id[7:0] from back end application 3 = RESERVED 4 = overwrite with src_tag[7:0] from back end application 5-7 = RESERVED
27	RESERVED	R/W	X	
26-24	SRCTAG_LO_SEL	R/W	0h	Rx Source Tag Low Byte Selector: This field specifies the source for bits 7:0 of the source tag field in Word 3 of the output Packet Descriptor. This field is encoded as follows: 0 = do not overwrite 1 = overwrite with value given in rx_src_tag_lo 2 = overwrite with flow_id[7:0] from back end application 3 = RESERVED 4 = overwrite with src_tag[7:0] from back end application 5-7 = RESERVED
23	RESERVED	R/W	X	

Table 12-108. UDMA_RFC_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
22-20	DSTTAG_HI_SEL	R/W	0h	Rx Destination Tag High Byte Selector: This field specifies the source for bits 15:8 of the destination tag field in the word 3 of the output Packet Descriptor. This field is encoded as follows: 0 = do not overwrite 1 = overwrite with value given in rx_dest_tag_hi 2 = overwrite with flow_id[7:0] from back end application 3 = RESERVED 4 = overwrite with dest_tag[7:0] from back end application 5 = overwrite with dest_tag[15:8] from back end application 6-7 = RESERVED
19	RESERVED	R/W	X	
18-16	DSTTAG_LO_SEL	R/W	0h	Rx Destination Tag Low Byte Selector: This field specifies the source for bits 7:0 of the destination tag field in word 3 of the output Packet Descriptor. This field is encoded as follows: 0 = do not overwrite 1 = overwrite with value given in rx_dest_tag_lo 2 = overwrite with flow_id[7:0] from back end application 3 = RESERVED 4 = overwrite with dest_tag[7:0] from back end application 5 = overwrite with dest_tag[15:8] from back end application 6-7 = RESERVED
15-3	RESERVED	R/W	X	
2-0	SIZE_THRESH_EN	R/W	0h	Rx Packet Sized Based Free Buffer Queue Enables: These bits control whether or not the flow will compare the packet size received from the back end application against the rx_size_threshN fields to determine which FDQ to allocate the SOP buffer from. Each bit in this field corresponds to 1 of the 3 potential size thresholds that can be compared against. Bit 0 corresponds to rx_size_thresh0 and bit 2 corresponds to rx_size_thresh2. The bits in this field is encoded as follows: 0 = Do not use the threshold. 1 = Use the thresholds to select between the 4 different potential SOP FDQs. If none of the thresholds are enabled, the DMA controller in the port will allocate the SOP buffer from the queue specified by the rx_fdq0_sz0_qnum field. Support for packet size based FDQ selection is OPTIONAL. If the port does not implement this feature, the bits of this field will be hardcoded to 0 and will not be writable by the host.

12.4.4 UDMA_RFD_j Register (Offset = Ch + formula) [reset = 0h]

UDMA_RFD_j is shown in [Figure 12-51](#) and described in [Table 12-110](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register D contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

Offset = Ch + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-109. UDMA_RFD_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 000Ch + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 000Ch + formula

Figure 12-51. UDMA_RFD_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDQ0_SZ0_QNUM																FDQ1_QNUM															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-110. UDMA_RFD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FDQ0_SZ0_QNUM	R/W	0h	Rx Free Descriptor 0 Queue Index - Size 0: This field specifies which Free Descriptor Queue should be used for the 1st Rx buffer in a packet whose size is less than or equal to the rx_size0 value.
15-0	FDQ1_QNUM	R/W	0h	Rx Free Descriptor 1 Queue Index: This field specifies which Free Descriptor Queue should be used for the 2nd Rx buffer in a host type packet

12.4.5 UDMA_RFE_j Register (Offset = 10h + formula) [reset = 0h]

UDMA_RFE_j is shown in [Figure 12-52](#) and described in [Table 12-112](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register E contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. The fields in this register are as follows:

Offset = 10h + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-111. UDMA_RFE_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0010h + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 0010h + formula

Figure 12-52. UDMA_RFE_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDQ2_QNUM																FDQ3_QNUM															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-112. UDMA_RFE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FDQ2_QNUM	R/W	0h	Rx Free Descriptor 2 Queue Index: This field specifies which Free Descriptor Queue should be used for the 3rd Rx buffer in a host type packet
15-0	FDQ3_QNUM	R/W	0h	Rx Free Descriptor 3 Queue Index: This field specifies which Free Descriptor Queue should be used for the 4th or later Rx buffers in a host type packet

12.4.6 UDMA_RFF_j Register (Offset = 14h + formula) [reset = 0h]

UDMA_RFF_j is shown in [Figure 12-53](#) and described in [Table 12-114](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register F contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. This register is OPTIONAL. The fields in this register are as follows:

Offset = 14h + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-113. UDMA_RFF_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0014h + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 0014h + formula

Figure 12-53. UDMA_RFF_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE_THRESH0																SIZE_THRESH1															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-114. UDMA_RFF_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIZE_THRESH0	R/W	0h	Rx Packet Size Threshold 0: This value is left shifted by 5 bits and compared against the packet size to determine which free descriptor queue should be used for the SOP buffer in the packet. If the packet size is less than or equal to the value given in this threshold, the DMA controller in the port will allocate the SOP buffer from the queue given by the rx_fdq0_sz0_qnum field. This field is OPTIONAL.
15-0	SIZE_THRESH1	R/W	0h	Rx Packet Size Threshold 1: This value is left shifted by 5 bits and compared against the packet size to determine which free descriptor queue should be used for the SOP buffer in the packet. If the packet size is greater than the rx_size_thresh0 but is less than or equal to the value given in this threshold, the DMA controller in the port will allocate the SOP buffer from the queue given by the rx_fdq0_sz1_qnum field. If enabled, this value must be greater than the value given in the rx_size_thresh0 field. This field is optional.

12.4.7 UDMA_RFG_j Register (Offset = 18h + formula) [reset = 0h]

UDMA_RFG_j is shown in [Figure 12-54](#) and described in [Table 12-116](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register G contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. This register is OPTIONAL. The fields in this register are as follows:

Offset = 18h + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-115. UDMA_RFG_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 0018h + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 0018h + formula

Figure 12-54. UDMA_RFG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIZE_THRESH2																FDQ0_SZ1_QNUM															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-116. UDMA_RFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SIZE_THRESH2	R/W	0h	Rx Packet Size Threshold 2: This value is left shifted by 5 bits and compared against the packet size to determine which free descriptor queue should be used for the SOP buffer in the packet. If the packet size is less than or equal to the value given in this threshold, the DMA controller in the port will allocate the SOP buffer from the queue given by the rx_fdq0_sz2_qnum field. If enabled, this value must be greater than the value given in the rx_size_thresh1 field. This field is optional.
15-0	FDQ0_SZ1_QNUM	R/W	0h	Rx Free Descriptor 0 Queue Index - Size 1: This field specifies which Free Descriptor Queue should be used for the 1st Rx buffer in a packet whose size is less than or equal to the rx_size0 value. This field is optional.

12.4.8 UDMA_RFH_j Register (Offset = 1Ch + formula) [reset = 0h]

UDMA_RFH_j is shown in [Figure 12-55](#) and described in [Table 12-118](#).

Return to [Summary Table](#).

The Rx Flow N Configuration Register H contains static configuration information for the Rx DMA flow. The fields in this register can only be changed when all of the DMA channels that use this flow have been disabled. This register is OPTIONAL. The fields in this register are as follows:

Offset = 1Ch + (j * 40h); where

j = 0h to 12Bh for NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

j = 0h to 5Fh for MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW

Table 12-117. UDMA_RFH_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	30D0 001Ch + formula
MCU_NAVSS0_UDMASS_UDMAP0_CFG_RFLOW	2840 001Ch + formula

Figure 12-55. UDMA_RFH_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDQ0_SZ2_QNUM																FDQ0_SZ3_QNUM															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-118. UDMA_RFH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	FDQ0_SZ2_QNUM	R/W	0h	Rx Free Descriptor 0 Queue Index - Size 2: This field specifies which Free Descriptor Queue should be used for the 1st Rx buffer in a packet whose size is less than or equal to the rx_size1 value. This field is optional.
15-0	FDQ0_SZ3_QNUM	R/W	0h	Rx Free Descriptor 0 Queue Index - Size 3: This field specifies which Free Descriptor Queue should be used for the 1st Rx buffer in a packet whose size is less than or equal to the rx_size2 value. This field is optional.

12.5 UDMASS_UDMAP0_CFG_TCHAN Registers

Table 12-120 lists the memory-mapped registers for the UDMASS_UDMAP0_CFG_TCHAN. All register offset addresses not listed in Table 12-120 should be considered as reserved locations and the register contents should not be modified.

The UDMA-P Tx Channel Configuration Registers region is accessed by setting the cdma_cfg_rsel signal to 2 during the access. The address map for this region is as follows:

**Table 12-119. UDMASS_UDMAP0_CFG_TCHAN
Instances**

Instance	Base Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0000h
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0000h

Table 12-120. UDMASS_UDMAP0_CFG_TCHAN Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG_TCHAN Physical Address	MCU_NAVSS0_UDMASS_UDMAP0_TCHAN Physical Address
0h + formula	UDMA_TCFG_j	Tx Channel Configuration	30B0 0000h + formula	284A 0000h + formula
4h + formula	UDMA_TCREDIT_j	Tx Channel Transfer Request Credit	30B0 0004h + formula	284A 0004h + formula
14h + formula	UDMA_TCQ_j	Tx Channel Completion Queue	30B0 0014h + formula	284A 0014h + formula
20h + formula	UDMA_TOES_j	Tx Channel Output Event Steering 0	30B0 0020h + formula	284A 0020h + formula
60h + formula	UDMA_TEOES_j	Tx Channel Error Output Event Steering 0	30B0 0060h + formula	284A 0060h + formula
64h + formula	UDMA_TPRI_CTRL_j	Tx Channel Priority Control	30B0 0064h + formula	284A 0064h + formula
68h + formula	UDMA_THREAD_j	Tx Channel Destination ThreadID Mapping	30B0 0068h + formula	284A 0068h + formula
70h + formula	UDMA_TFIFO_DEPTH_j	Tx Channel FIFO Depth	30B0 0070h + formula	284A 0070h + formula
80h + formula	UDMA_TST_SCHED_j	Tx Channel Static Scheduler Config	30B0 0080h + formula	284A 0080h + formula

12.5.1 UDMA_TCFG_j Register (Offset = 0h + formula) [reset = X]

UDMA_TCFG_j is shown in [Figure 12-56](#) and described in [Table 12-122](#).

Return to [Summary Table](#).

The Tx Channel Configuration Register is used to initialize static mode settings for the Tx DMA channel. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Offset = 0h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-121. UDMA_TCFG_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0000h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0000h + formula

Figure 12-56. UDMA_TCFG_j Register

31	30	29	28	27	26	25	24
PAUSE_ON_ERR	FILT_EINFO	FILT_PSWORDS	RESERVED			ATYPE	
R/W-0h	R/W-0h	R/W-0h	R/W-X			R/W-0h	
23	22	21	20	19	18	17	16
RESERVED				CHAN_TYPE			
R/W-X				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED				BURST_SIZE		TDYPE	NOTDPKT
R/W-X				R/W-1h		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	FETCH_SIZE						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-122. UDMA_TCFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PAUSE_ON_ERR	R/W	0h	Pause On Error: this field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel.
30	FILT_EINFO	R/W	0h	This field controls whether or not the DMA controller will pass the extended packet information fields (if present) from the descriptor to the back end application. This field is encoded as follows: 0=DMA controller will pass extended packet info words if they are present in the descriptor 1=DMA controller will filter extended packet info words.
29	FILT_PSWORDS	R/W	0h	This field controls whether or not the DMA controller will pass the protocol specific words (if present) from the descriptor to the back end application. This field is encoded as follows: 0=DMA controller will pass PS words if present in descriptor 1=DMA controller will filter PS words.

Table 12-122. UDMA_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28-26	RESERVED	R/W	X	
25-24	ATYPE	R/W	0h	<p>This field controls how pointers will be interpreted for non Ring Accelerator accesses on this channel.</p> <p>The values are encoded as follows:</p> <p>0 = Pointers are physical addresses</p> <p>1 = Pointers are intermediate addresses which require intermediate to physical transaction before they can be decoded</p> <p>2 = Pointers are virtual addresses which require virtual to physical translation before they can be decoded.</p> <p>All transactions from this channel which are not destined to the Ring Accelerator will have the mem*_catype attribute set equal to the value given in this register field.</p> <p>Accesses to the RA will always use physical addresses.</p>
23-20	RESERVED	R/W	X	
19-16	CHAN_TYPE	R/W	0h	<p>Tx Channel Type: this field controls and / or indicates the functional channel type for this channel and the work passing mechanism that the channel uses for communicating with the Host.</p> <p>Available channel types are as follows:</p> <p>0 = RESERVED</p> <p>1 = RESERVED</p> <p>2 = Channel performs packet oriented data transfers using pass by reference rings. Channels configured in this mode can only use Host and Monolithic descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator.</p> <p>3- 9 = RESERVED</p> <p>10 = Channel performs Third Party DMA transfers using pass by reference rings. Channels configured in this mode can only use TR descriptors and the pointers to those descriptors are passed from/to SW using rings in the Ring Accelerator.</p> <p>11 = Channel performs Third Party DMA transfers using pass by value rings. Channels configured in this mode will directly pass individual Transfer Request/Transfer Response messages from/to SW using rings in the Ring Accelerator.</p> <p>12 = Channel performs Third Party Block Copy DMA transfers using pass by reference rings. Channels configured in this mode are linked to the same index Rx channel to form a bonded read/write channel</p> <p>13 = Channel performs Third Party Block Copy DMA transfers using pass by value rings. Channels configured in this mode are linked to the same index Rx channel to form a bonded read/write channel</p> <p>14 = Channel performs Third Party DMA transfers using TRs provided via PSI-L (not supported in UDMA-P).</p> <p>15 = Channel performs Third Party DMA transfers using TRs provided via QDMA channel (not supported in UDMA-P)</p>
15-12	RESERVED	R/W	X	

Table 12-122. UDMA_TCFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	BURST_SIZE	R/W	1h	<p>Specifies the nominal burst size and alignment for data transfers on this channel.</p> <p>0 = RESERVED</p> <p>1 = 64 bytes</p> <p>2 = 128 bytes</p> <p>3 = 256 bytes</p> <p>This field may only be set to values for which the Tx Per Channel FIFO has sufficient storage.</p> <p>Transmit Data fetches are not allowed to initiate unless sufficient free space exists in the Tx Per Channel Buffer for that channel.</p> <p>Free space is calculated based on the value programmed into the Tx Channel FIFO Depth register.</p> <p>Care must be taken to ensure that the nominal burst size field (this field) meets the following restrictions:</p> <ol style="list-style-type: none"> For UTC mode channels: <ol style="list-style-type: none"> The Tx FIFO size must be at least 2 quad words larger than the burst size given in this field The Tx FIFO size must be less than or equal to the physically implemented storage for that channel class (UHC/HC/NC) For Packet mode channels: <ol style="list-style-type: none"> The Tx FIFO size must be at least 2 PSI-L data phases larger than the burst size given in this field in order to hold the packet info and extended packet info header which is placed at the front of the data packet in addition to the payload. The Tx FIFO size must be less than or equal to the physically implemented storage for that channel class (UHC/HC/NC) <p>Unless otherwise noted, it should be assumed that only HC/UHC channels can be programmed to use a burst size greater than 64 bytes.</p>
9	TDTYPE	R/W	0h	<p>Specifies whether or not the channel should immediately return a teardown completion response to the default completion queue or wait until a status message is returned from the remote PSI-L paired peripheral.</p> <p>0 = return immediately once all traffic is complete in UDMAP.</p> <p>1 = wait until remote peer sends back a completion message.</p>
8	NOTDPKT	R/W	0h	<p>Specifies whether or not the channel should suppress sending the single data phase teardown packet when teardown is complete.</p> <p>0 = TD packet is sent</p> <p>1 = Suppress sending TD packet</p>
7	RESERVED	R/W	X	
6-0	FETCH_SIZE	R/W	0h	<p>Specifies the # of 32-bit descriptor words to fetch.</p> <p>This must be set to the maximum word count that can pass through the channel for any allowed descriptor type.</p>

12.5.2 UDMA_TCREDIT_j Register (Offset = 4h + formula) [reset = X]

UDMA_TCREDIT_j is shown in [Figure 12-57](#) and described in [Table 12-124](#).

Return to [Summary Table](#).

The Transfer Request Credit Register indicates how many TR sized buffer slots exist in the associated UTC channel to which this channel is associated. This register only exists for external UTC channels. This field should not be changed while the channel is in operation.

Offset = 4h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-123. UDMA_TCREDIT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0004h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0004h + formula

Figure 12-57. UDMA_TCREDIT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													COUNT		
R/W-X													R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-124. UDMA_TCREDIT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	COUNT	R/W	0h	Transfer Request Credit Count: this field specifies how many credits for complete TRs are available. This field should be initialized before the channel is enabled and will then increment/decrement as TRs are submitted and responses are received.

12.5.3 UDMA_TCQ_j Register (Offset = 14h + formula) [reset = X]

UDMA_TCQ_j is shown in [Figure 12-58](#) and described in [Table 12-126](#).

Return to [Summary Table](#).

The Tx Channel Completion Queue Register is used to specify which queue the Transfer Responses will be returned to when operating in the pass by value channel mode. This register may only be written when the channel is disabled (tx_enable in realtime control reg is 0).

Offset = 14h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-125. UDMA_TCQ_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0014h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0014h + formula

Figure 12-58. UDMA_TCQ_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																TXCQ_QNUM															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-126. UDMA_TCQ_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	TXCQ_QNUM	R/W	0h	Specifies the queue number to return pass by value Transfer Responses and teardown completion teardown messages to.

12.5.4 UDMA_TOES_j Register (Offset = 20h + formula) [reset = X]

UDMA_TOES_j is shown in [Figure 12-59](#) and described in [Table 12-128](#).

Return to [Summary Table](#).

The Output Event Steering Registers are used to specify a global event number to generate anytime the required event generation criteria specified in a TR are met. A single event with the event number set equal to the value in the corresponding register will be generated. This register is provided in order to allow security SW to lock down which events in the global space any given channel/ thread is allowed to generate.

Offset = 20h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-127. UDMA_TOES_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HAN	30B0 0020h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TC HAN	284A 0020h + formula

Figure 12-59. UDMA_TOES_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT_NUM															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-128. UDMA_TOES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT_NUM	R/W	FFFFh	This is the global event number to be generated

12.5.5 UDMA_TEOES_j Register (Offset = 60h + formula) [reset = X]

UDMA_TEOES_j is shown in [Figure 12-60](#) and described in [Table 12-130](#).

Return to [Summary Table](#).

The Error Output Event Steering Registers are used to specify a global event number to generate anytime an error is encountered on the channel. A single event with the event number set equal to the value in the corresponding register will be generated. This register is provided in order to allow security SW to lock down which events in the global space any given channel/ thread is allowed to generate.

Offset = 60h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-129. UDMA_TEOES_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0060h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0060h + formula

Figure 12-60. UDMA_TEOES_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT_NUM															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-130. UDMA_TEOES_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT_NUM	R/W	FFFFh	This is the global event number to be generated

12.5.6 UDMA_TPRI_CTRL_j Register (Offset = 64h + formula) [reset = X]

UDMA_TPRI_CTRL_j is shown in [Figure 12-61](#) and described in [Table 12-132](#).

Return to [Summary Table](#).

The priority control register is used to control the priority of the transactions which the DMA generates on it's master interface.

Offset = 64h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-131. UDMA_TPRI_CTRL_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0064h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0064h + formula

Figure 12-61. UDMA_TPRI_CTRL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESE RVED	PRIORITY			RESERVED										QOS	
R/W-X	R/W-0h			R/W-X										R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ORDERID			
R/W-X												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-132. UDMA_TPRI_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	X	
30-28	PRIORITY	R/W	0h	Tx Priority: This field contains the 3-bit value which will be output on the mem*_cpriority and mem_cepriority outputs during all transactions for this channel.
27-19	RESERVED	R/W	X	
18-16	QOS	R/W	0h	Tx Quality of Service Level: This field contains the 3-bit value which will be output on the mem*_cqos output during all transactions for this channel.
15-4	RESERVED	R/W	X	
3-0	ORDERID	R/W	0h	Tx Order ID: This field contains the 4-bit value which will be output on the mem*_corderid output during all transactions for this channel.

12.5.7 UDMA_THREAD_j Register (Offset = 68h + formula) [reset = X]

UDMA_THREAD_j is shown in [Figure 12-62](#) and described in [Table 12-134](#).

Return to [Summary Table](#).

The thread ID mapping register is used to pair the Tx DMA channel to a specific destination thread. All traffic generated from this channel will be sent with a thread_id on the PSI-L interface with the value from this register.

Offset = 68h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-133. UDMA_THREAD_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0068h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0068h + formula

Figure 12-62. UDMA_THREAD_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ID															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-134. UDMA_THREAD_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	ID	R/W	0h	Thread ID: This field contains the 16-bit value which will be output on the strm_o_thread_id output during all transactions for this channel.

12.5.8 UDMA_TFIFO_DEPTH_j Register (Offset = 70h + formula) [reset = X]

UDMA_TFIFO_DEPTH_j is shown in [Figure 12-63](#) and described in [Table 12-136](#).

Return to [Summary Table](#).

The fifo depth register is used to specify how many FIFO data phases deep the Tx per channel FIFO will be for the channel. While the maximum depth of the Tx FIFO is set at design time, the FIFO depth can be artificially reduced in order to control the maximum latency which can be introduced due to buffering effects. This register is only present for internal channels.

Offset = 70h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-135. UDMA_TFIFO_DEPTH_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0070h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0070h + formula

Figure 12-63. UDMA_TFIFO_DEPTH_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			FDEPTH												
R/W-X																			R/W-1000h												

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-136. UDMA_TFIFO_DEPTH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12-0	FDEPTH	R/W	1000h	<p>FIFO Depth: This field contains the number of Tx FIFO bytes which will be allowed to be stored for the channel.</p> <p>The minimum value is equal to the PSI-L interface data path width (tstrm_wdth), the maximum value varies by channel class (ultra-high capacity/high capacity/normal capacity) and is equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L data path width (tstrm_wdth).</p> <p>The fdepth must always be an integer multiple of tstrm_wdth.</p> <p>The reset value of this register varies by channel class (ultra-high capacity/high capacity/normal capacity) but will be equal to the tubuf_size/thbuf_size/tbuf_size parameter respectively multiplied by the PSI-L interface data width (tstrm_wdth).</p>

12.5.9 UDMA_TST_SCHED_j Register (Offset = 80h + formula) [reset = X]

UDMA_TST_SCHED_j is shown in [Figure 12-64](#) and described in [Table 12-138](#).

Return to [Summary Table](#).

The Tx Channel N Static Scheduler Configuration Register contains static configuration information which affects the conditions under which each channel will be given an opportunity to use the Tx DMA unit(s). The fields in this register are as follows:

Offset = 80h + (j * 100h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHAN

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP0_TCHAN

Table 12-137. UDMA_TST_SCHED_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHAN	30B0 0080h + formula
MCU_NAVSS0_UDMASS_UDMAP0_TCHAN	284A 0080h + formula

Figure 12-64. UDMA_TST_SCHED_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PRIORITY	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-138. UDMA_TST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	

Table 12-138. UDMA_TST_SCHED_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	PRIORITY	R/W	0h	<p>Tx Scheduling Priority: These bits select which scheduling bin the channel will be placed in for bandwidth allocation of the Tx DMA units.</p> <p>This field is encoded as follows:</p> <p>0 = High priority 1 = Medium - high priority 2 = Medium - low priority 3 = Low priority</p> <p>Arbitration between bins is performed in a strict priority fashion.</p> <p>High priority channels will always be serviced first.</p> <p>If no high priority channels are requesting then all medium-high priority channels will be serviced next.</p> <p>If no high priority or medium-high priority channels are requesting then all medium-low priority channels will be serviced next.</p> <p>When no other channels are requesting, the low priority channels will be serviced.</p> <p>All channels within a given bin are serviced in a round robin order.</p> <p>Only channels which are enabled and which have sufficient free space in their Per Channel FIFO will be included in the round robin arbitration.</p>

12.6 UDMASS_UDMAP0_CFG_TCHANRT Registers

Table 12-140 lists the memory-mapped registers for the UDMASS_UDMAP0_CFG_TCHANRT. All register offset addresses not listed in Table 12-140 should be considered as reserved locations and the register contents should not be modified.

The UDMA-P Tx Channel Realtime Registers region is accessed by setting the cdma_cfg_rsel signal to 4 during the access. The address map for this region is as follows:

**Table 12-139. UDMASS_UDMAP0_CFG_TCHANRT
Instances**

Instance	Base Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT	3500 0000h
MCU_NAVSS0_UDMASS_UDMAP_TCHANRT	2AA0 0000h

Table 12-140. UDMASS_UDMAP0_CFG_TCHANRT Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT Physical Address	MCU_NAVSS0_UDMASS_UDMAP_TCHANRT Physical Address
0h + formula	UDMA_TRT_CTL_j	Tx Channel Realtime Control Register	3500 0000h + formula	2AA0 0000h + formula
8h + formula	UDMA_TRT_SWTRIG_j	Tx Channel Realtime Software Trigger Register	3500 0008h + formula	2AA0 0008h + formula
80h + formula	UDMA_TRT_STDATA_j_Y	Tx Channel Realtime State Data Register	3500 0080h + formula	2AA0 0080h + formula
200h + formula	UDMA_TRT_PEER0_j	Tx Channel Real-time Remote Peer Register 0	3500 0200h + formula	2AA0 0200h + formula
204h + formula	UDMA_TRT_PEER1_j	Tx Channel Real-time Remote Peer Register 1	3500 0204h + formula	2AA0 0204h + formula
208h + formula	UDMA_TRT_PEER2_j	Tx Channel Real-time Remote Peer Register 2	3500 0208h + formula	2AA0 0208h + formula
20Ch + formula	UDMA_TRT_PEER3_j	Tx Channel Real-time Remote Peer Register 3	3500 020Ch + formula	2AA0 020Ch + formula
210h + formula	UDMA_TRT_PEER4_j	Tx Channel Real-time Remote Peer Register 4	3500 0210h + formula	2AA0 0210h + formula
214h + formula	UDMA_TRT_PEER5_j	Tx Channel Real-time Remote Peer Register 5	3500 0214h + formula	2AA0 0214h + formula
218h + formula	UDMA_TRT_PEER6_j	Tx Channel Real-time Remote Peer Register 6	3500 0218h + formula	2AA0 0218h + formula
21Ch + formula	UDMA_TRT_PEER7_j	Tx Channel Real-time Remote Peer Register 7	3500 021Ch + formula	2AA0 021Ch + formula
220h + formula	UDMA_TRT_PEER8_j	Tx Channel Real-time Remote Peer Register 8	3500 0220h + formula	2AA0 0220h + formula
224h + formula	UDMA_TRT_PEER9_j	Tx Channel Real-time Remote Peer Register 9	3500 0224h + formula	2AA0 0224h + formula
228h + formula	UDMA_TRT_PEER10_j	Tx Channel Real-time Remote Peer Register 10	3500 0228h + formula	2AA0 0228h + formula
22Ch + formula	UDMA_TRT_PEER11_j	Tx Channel Real-time Remote Peer Register 11	3500 022Ch + formula	2AA0 022Ch + formula
230h + formula	UDMA_TRT_PEER12_j	Tx Channel Real-time Remote Peer Register 12	3500 0230h + formula	2AA0 0230h + formula
234h + formula	UDMA_TRT_PEER13_j	Tx Channel Real-time Remote Peer Register 13	3500 0234h + formula	2AA0 0234h + formula
238h + formula	UDMA_TRT_PEER14_j	Tx Channel Real-time Remote Peer Register 14	3500 0238h + formula	2AA0 0238h + formula
23Ch + formula	UDMA_TRT_PEER15_j	Tx Channel Real-time Remote Peer Register 15	3500 023Ch + formula	2AA0 023Ch + formula

Table 12-140. UDMASS_UDMAP0_CFG_TCHANRT Registers (continued)

Offset	Acronym	Register Name	NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT Physical Address	MCU_NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT Physical Address
400h + formula	UDMA_TRT_PCNT_j	Tx Channel Real-time Packet Count Statistics Register	3500 0400h + formula	2AA0 0400h + formula
408h + formula	UDMA_TRT_BCNT_j	Tx Channel Real-time Completed Byte Count Statistics Register	3500 0408h + formula	2AA0 0408h + formula
410h + formula	UDMA_TRT_SBCNT_j	Tx Channel Real-time Started Byte Count Statistics Register	3500 0410h + formula	2AA0 0410h + formula

12.6.1 UDMA_TRT_CTL_j Register (Offset = 0h + formula) [reset = X]

UDMA_TRT_CTL_j is shown in [Figure 12-65](#) and described in [Table 12-142](#).

Return to [Summary Table](#).

The Tx Channel Realtime Control Register contains real-time control and status information for the Tx DMA channel. The fields in this register can safely be changed while the channel is in operation.

Offset = 0h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-141. UDMA_TRT_CTL_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0000h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0000h + formula

Figure 12-65. UDMA_TRT_CTL_j Register

31	30	29	28	27	26	25	24
EN	TDOWN	PAUSE	FTDOWN	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ERROR
R/W-X							R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-142. UDMA_TRT_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. When a channel is disabled, the implementation may choose to reset all state for the channel. The pause bit should be asserted instead of clearing enable directly if the intent is to temporarily pause the channel. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled This field will be cleared by HW after a teardown is requested to indicate that the channel teardown is complete.
30	TDOWN	R/W	0h	Channel teardown: Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete.
29	PAUSE	R/W	0h	Channel pause: Setting this bit will cause the channel to pause processing immediately.

Table 12-142. UDMA_TRT_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FTDOWN	R/W	0h	<p>Channel forced teardown: Setting this bit will cause the channel to stop waiting on trigger events.</p> <p>When this bit is set, the implementation may choose to bypass data transfers and event generation.</p> <p>This bit is a modifier to the normal tx_teardown and is intended to flush the channel to recover any descriptor or TR references which are currently being held by the UDMA-P even if the trigger source is no longer functioning.</p> <p>Use of this bit is considered a 'catastrophic' condition and it is assumed that SW will need to perform some re-initialization in the system to re-align events, data buffers, etc.</p> <p>This bit should be set in addition to the tx_teardown bit in order to cause a forced teardown.</p> <p>This field will remain set after a channel teardown is complete.</p>
27-1	RESERVED	R/W	X	
0	ERROR	R	0h	<p>Channel error: This bit will be set anytime an error has occurred on the channel.</p> <p>This bit is cleared when the channel is disabled and re-enabled.</p>

12.6.2 UDMA_TRT_SWTRIG_j Register (Offset = 8h + formula) [reset = X]

UDMA_TRT_SWTRIG_j is shown in [Figure 12-66](#) and described in [Table 12-144](#).

Return to [Summary Table](#).

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way. This register is only used when the tx_chan_type is configured as a Third Party DMA channel. This register has no function when the channel is configured for packet mode transfers. A write to this register will cause an event to be sent to this channel.

Offset = 8h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-143. UDMA_TRT_SWTRIG_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0008h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0008h + formula

Figure 12-66. UDMA_TRT_SWTRIG_j Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TRIGGER
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 12-144. UDMA_TRT_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TRIGGER	W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel

12.6.3 UDMA_TRT_STDATA_j_Y Register (Offset = 80h + formula) [reset = 0h]

UDMA_TRT_STDATA_j_Y is shown in [Figure 12-67](#) and described in [Table 12-146](#).

Return to [Summary Table](#).

The State Data Registers contain the current working state of the Tx DMA channel. These registers are provided so that the Host can determine the potential cause of an error or exception condition which was reported by the channel. These registers should not be accessed without reason while the UDMA-P is operating as accesses will cause performance to decrease as these MMRs are just providing a window into the actual state RAM

Offset = 80h + (j * 1000h) + (y * 4h); where

j = 0h to 8Bh, y = 0h to 1Fh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh, y = 0h to 1Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-145. UDMA_TRT_STDATA_j_Y Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0080h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0080h + formula

Figure 12-67. UDMA_TRT_STDATA_j_Y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATE_INFO																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 12-146. UDMA_TRT_STDATA_j_Y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATE_INFO	R	0h	See Tx state mapping table

12.6.4 UDMA_TRT_PEER0_j Register (Offset = 200h + formula) [reset = 0h]

UDMA_TRT_PEER0_j is shown in [Figure 12-68](#) and described in [Table 12-148](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x400.

Offset = 200h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-147. UDMA_TRT_PEER0_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0200h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0200h + formula

Figure 12-68. UDMA_TRT_PEER0_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-148. UDMA_TRT_PEER0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.5 UDMA_TRT_PEER1_j Register (Offset = 204h + formula) [reset = 0h]

UDMA_TRT_PEER1_j is shown in [Figure 12-69](#) and described in [Table 12-150](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x401.

Offset = 204h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-149. UDMA_TRT_PEER1_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0204h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0204h + formula

Figure 12-69. UDMA_TRT_PEER1_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-150. UDMA_TRT_PEER1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.6 UDMA_TRT_PEER2_j Register (Offset = 208h + formula) [reset = 0h]

UDMA_TRT_PEER2_j is shown in [Figure 12-70](#) and described in [Table 12-152](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x402.

Offset = 208h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-151. UDMA_TRT_PEER2_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0208h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0208h + formula

Figure 12-70. UDMA_TRT_PEER2_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-152. UDMA_TRT_PEER2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.7 UDMA_TRT_PEER3_j Register (Offset = 20Ch + formula) [reset = 0h]

UDMA_TRT_PEER3_j is shown in [Figure 12-71](#) and described in [Table 12-154](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x403.

Offset = 20Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-153. UDMA_TRT_PEER3_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 020Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 020Ch + formula

Figure 12-71. UDMA_TRT_PEER3_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-154. UDMA_TRT_PEER3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.8 UDMA_TRT_PEER4_j Register (Offset = 210h + formula) [reset = 0h]

UDMA_TRT_PEER4_j is shown in [Figure 12-72](#) and described in [Table 12-156](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x404.

Offset = 210h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-155. UDMA_TRT_PEER4_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0210h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0210h + formula

Figure 12-72. UDMA_TRT_PEER4_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-156. UDMA_TRT_PEER4_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.9 UDMA_TRT_PEER5_j Register (Offset = 214h + formula) [reset = 0h]

UDMA_TRT_PEER5_j is shown in [Figure 12-73](#) and described in [Table 12-158](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x405.

Offset = 214h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-157. UDMA_TRT_PEER5_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0214h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0214h + formula

Figure 12-73. UDMA_TRT_PEER5_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-158. UDMA_TRT_PEER5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.10 UDMA_TRT_PEER6_j Register (Offset = 218h + formula) [reset = 0h]

UDMA_TRT_PEER6_j is shown in [Figure 12-74](#) and described in [Table 12-160](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x406.

Offset = 218h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-159. UDMA_TRT_PEER6_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0218h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0218h + formula

Figure 12-74. UDMA_TRT_PEER6_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-160. UDMA_TRT_PEER6_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.11 UDMA_TRT_PEER7_j Register (Offset = 21Ch + formula) [reset = 0h]

UDMA_TRT_PEER7_j is shown in [Figure 12-75](#) and described in [Table 12-162](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x407.

Offset = 21Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-161. UDMA_TRT_PEER7_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 021Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 021Ch + formula

Figure 12-75. UDMA_TRT_PEER7_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-162. UDMA_TRT_PEER7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.12 UDMA_TRT_PEER8_j Register (Offset = 220h + formula) [reset = 0h]

UDMA_TRT_PEER8_j is shown in [Figure 12-76](#) and described in [Table 12-164](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x408.

Offset = 220h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-163. UDMA_TRT_PEER8_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0220h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0220h + formula

Figure 12-76. UDMA_TRT_PEER8_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-164. UDMA_TRT_PEER8_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.13 UDMA_TRT_PEER9_j Register (Offset = 224h + formula) [reset = 0h]

UDMA_TRT_PEER9_j is shown in [Figure 12-77](#) and described in [Table 12-166](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x409.

Offset = 224h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-165. UDMA_TRT_PEER9_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT	3500 0224h + formula
MCU_NAVSS0_UDMASS_UDMAP_TCHANRT	2AA0 0224h + formula

Figure 12-77. UDMA_TRT_PEER9_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-166. UDMA_TRT_PEER9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.14 UDMA_TRT_PEER10_j Register (Offset = 228h + formula) [reset = 0h]

UDMA_TRT_PEER10_j is shown in [Figure 12-78](#) and described in [Table 12-168](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40A.

Offset = 228h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-167. UDMA_TRT_PEER10_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT	3500 0228h + formula
MCU_NAVSS0_UDMASS_UDMAP_TCHANRT	2AA0 0228h + formula

Figure 12-78. UDMA_TRT_PEER10_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-168. UDMA_TRT_PEER10_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.15 UDMA_TRT_PEER11_j Register (Offset = 22Ch + formula) [reset = 0h]

UDMA_TRT_PEER11_j is shown in [Figure 12-79](#) and described in [Table 12-170](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40B.

Offset = 22Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-169. UDMA_TRT_PEER11_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT	3500 022Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_TCHANRT	2AA0 022Ch + formula

Figure 12-79. UDMA_TRT_PEER11_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-170. UDMA_TRT_PEER11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.16 UDMA_TRT_PEER12_j Register (Offset = 230h + formula) [reset = 0h]

UDMA_TRT_PEER12_j is shown in [Figure 12-80](#) and described in [Table 12-172](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40C.

Offset = 230h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-171. UDMA_TRT_PEER12_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0230h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0230h + formula

Figure 12-80. UDMA_TRT_PEER12_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-172. UDMA_TRT_PEER12_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.17 UDMA_TRT_PEER13_j Register (Offset = 234h + formula) [reset = 0h]

UDMA_TRT_PEER13_j is shown in [Figure 12-81](#) and described in [Table 12-174](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40D.

Offset = 234h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-173. UDMA_TRT_PEER13_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0234h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0234h + formula

Figure 12-81. UDMA_TRT_PEER13_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-174. UDMA_TRT_PEER13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.18 UDMA_TRT_PEER14_j Register (Offset = 238h + formula) [reset = 0h]

UDMA_TRT_PEER14_j is shown in [Figure 12-82](#) and described in [Table 12-176](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40E.

Offset = 238h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-175. UDMA_TRT_PEER14_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT	3500 0238h + formula
MCU_NAVSS0_UDMASS_UDMAP_TCHANRT	2AA0 0238h + formula

Figure 12-82. UDMA_TRT_PEER14_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-176. UDMA_TRT_PEER14_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.19 UDMA_TRT_PEER15_j Register (Offset = 23Ch + formula) [reset = 0h]

UDMA_TRT_PEER15_j is shown in [Figure 12-83](#) and described in [Table 12-178](#).

Return to [Summary Table](#).

This register provides access to the remote peer's realtime register at 0x40F.

Offset = 23Ch + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-177. UDMA_TRT_PEER15_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 023Ch + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 023Ch + formula

Figure 12-83. UDMA_TRT_PEER15_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEER_DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-178. UDMA_TRT_PEER15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PEER_DATA	R/W	0h	Peer realtime register data (varies by paired peer).

12.6.20 UDMA_TRT_PCNT_j Register (Offset = 400h + formula) [reset = 0h]

UDMA_TRT_PCNT_j is shown in [Figure 12-84](#) and described in [Table 12-180](#).

Return to [Summary Table](#).

The statistics registers are supplied to give software applications operational progress status for the channel.

Offset = 400h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-179. UDMA_TRT_PCNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0400h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0400h + formula

Figure 12-84. UDMA_TRT_PCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PCNT																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-180. UDMA_TRT_PCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PCNT	R/W	0h	Current completed packet count for the channel.

12.6.21 UDMA_TRT_BCNT_j Register (Offset = 408h + formula) [reset = 0h]

UDMA_TRT_BCNT_j is shown in [Figure 12-85](#) and described in [Table 12-182](#).

Return to [Summary Table](#).

The statistics registers are supplied to give software applications operational progress status for the channel.

Offset = 408h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-181. UDMA_TRT_BCNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT	3500 0408h + formula
MCU_NAVSS0_UDMASS_UDMAP_TCHANRT	2AA0 0408h + formula

Figure 12-85. UDMA_TRT_BCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-182. UDMA_TRT_BCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BCNT	R/W	0h	Current completed payload byte count for the channel.

12.6.22 UDMA_TRT_SBCNT_j Register (Offset = 410h + formula) [reset = 0h]

UDMA_TRT_SBCNT_j is shown in [Figure 12-86](#) and described in [Table 12-184](#).

Return to [Summary Table](#).

The statistics registers are supplied to give software applications operational progress status for the channel.

Offset = 410h + (j * 1000h); where

j = 0h to 8Bh for NAVSS0_UDMASS_UDMAP0_CFG_TCHANRT

j = 0h to 2Fh for MCU_NAVSS0_UDMASS_UDMAP_TCHANRT

Table 12-183. UDMA_TRT_SBCNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_UDMAP0_CFG_TC HANRT	3500 0410h + formula
MCU_NAVSS0_UDMASS_UDMAP_TC HANRT	2AA0 0410h + formula

Figure 12-86. UDMA_TRT_SBCNT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-184. UDMA_TRT_SBCNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SBCNT	R/W	0h	Current started byte count for the channel.

13 RINGACC Registers

13.1 NAVSS0_UDMASS_RINGACC0_CFG Registers

Table 13-2 lists the memory-mapped registers for the NAVSS0_UDMASS_RINGACC0_CFG. All register offset addresses not listed in Table 13-2 should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Ring Control /Status Registers region is accessed by setting the cfg_rsel signal to 1 during the access. The address map for this region is as follows:

Table 13-1. NAVSS0_UDMASS_RINGACC0_CFG Instances

Instance	Base Address
NAVSS0_UDMASS_RINGACC0_CFG	3108 0000h
MCU_NAVSS0_UDMASS_RINGACC0_CFG	2844 0000h

Table 13-2. NAVSS0_UDMASS_RINGACC0_CFG Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_RINGACC0_CFG Physical Address	MCU_NAVSS0_UDMASS_RINGACC0_CFG Physical Address
40h + formula	RINGACC_BA_LO_J	Ring Base Address Lo Register	3108 0040h + formula	2844 0040h + formula
44h + formula	RINGACC_BA_HI_J	Ring Base Address Hi Register	3108 0044h + formula	2844 0044h + formula
48h + formula	RINGACC_SIZE_J	Ring Size Register	3108 0048h + formula	2844 0048h + formula
4Ch + formula	RINGACC_EVENT_J	Ring Event Register	3108 004Ch + formula	2844 004Ch + formula
50h + formula	RINGACC_ORDERID_J	Ring OrderID Register	3108 0050h + formula	2844 0050h + formula

13.1.1 RINGACC_BA_LO_J Register (Offset = 40h + formula) [reset = 0h]

RINGACC_BA_LO_J is shown in [Figure 13-1](#) and described in [Table 13-4](#).

Return to [Summary Table](#).

The Tx Ring Base Address Lo Register contains the 32 LSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Offset = 40h + (j * 100h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG

Table 13-3. RINGACC_BA_LO_J Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG	3108 0040h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG	2844 0040h + formula

Figure 13-1. RINGACC_BA_LO_J Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_LO																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-4. RINGACC_BA_LO_J Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_LO	R/W	0h	Tx Ring base address (LSBs)

13.1.2 RINGACC_BA_HI_j Register (Offset = 44h + formula) [reset = X]

RINGACC_BA_HI_j is shown in [Figure 13-2](#) and described in [Table 13-6](#).

Return to [Summary Table](#).

The Tx Ring Base Address Hi Register contains the 16 MSBs of the base address for the ring which is used to hand off pending work for the channel from the Host. The base address must be aligned to the element size of the ring, or to double the element size of the ring if the qmode is CREDENTIALS or QM modes. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Offset = 44h + (j * 100h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG

Table 13-5. RINGACC_BA_HI_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG	3108 0044h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG	2844 0044h + formula

Figure 13-2. RINGACC_BA_HI_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_HI															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-6. RINGACC_BA_HI_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	ADDR_HI	R/W	0h	Tx Ring base address (MSBs)

13.1.3 RINGACC_SIZE_j Register (Offset = 48h + formula) [reset = X]

RINGACC_SIZE_j is shown in [Figure 13-3](#) and described in [Table 13-8](#).

Return to [Summary Table](#).

The Tx Ring Size Register contains the element size and element counts for the ring which is used to hand off pending work for the channel from the Host. A write to this register will reset the associated ring to clear the occupancies and reset the pointers.

Offset = 48h + (j * 100h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG

Table 13-7. RINGACC_SIZE_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG	3108 0048h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG	2844 0048h + formula

Figure 13-3. RINGACC_SIZE_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
QMODE		RESERVED				ELSIZE			RESERVED				ELCNT		
R/W-0h		R/W-X				R/W-0h			R/W-X				R/W-0h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ELCNT															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-8. RINGACC_SIZE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	QMODE	R/W	0h	Defines the mode for this ring or queue. 0h = exposed ring mode for SW direct access 1h = messaging mode when all operations are through bus accesses, allowing multiple producers or consumers. 2h = credentials mode is message mode plus stores credentials with each message, requiring the ring size to be doubled to fit the credentials along with the same number of elements when using the first 2 modes. Any exposed memory should be protected by a firewall from unwanted access. 3h = QM mode where the elements include additional fields that the QM supported above messaging credentials mode. Must be used with 8 byte element size only. NOT SUPPORTED.
29-27	RESERVED	R/W	X	
26-24	ELSIZE	R/W	0h	Ring element size. This field is encoded as follows: 0 = 4 bytes 1 = 8 bytes 2 = 16 bytes 3 = 32 bytes 4 = 64 bytes 5 = 128 bytes 6 = 256 bytes 7 = RESERVED
23-20	RESERVED	R/W	X	

Table 13-8. RINGACC_SIZE_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-0	ELCNT	R/W	0h	Tx Ring element count. This field configures the size of the ring in elements. For rings in CREDENTIALS or QM modes the size must be an even number.

13.1.4 RINGACC_EVENT_j Register (Offset = 4Ch + formula) [reset = X]

RINGACC_EVENT_j is shown in [Figure 13-4](#) and described in [Table 13-10](#).

Return to [Summary Table](#).

The Ring Event Register contains the event number for the ring for when it is active or empty.

Offset = 4Ch + (j * 100h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG

Table 13-9. RINGACC_EVENT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG	3108 004Ch + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG	2844 004Ch + formula

Figure 13-4. RINGACC_EVENT_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVENT															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-10. RINGACC_EVENT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVENT	R/W	FFFFh	Defines the event for this ring or queue.

13.1.5 RINGACC_ORDERID_j Register (Offset = 50h + formula) [reset = X]

RINGACC_ORDERID_j is shown in [Figure 13-5](#) and described in [Table 13-12](#).

Return to [Summary Table](#).

The Ring OrderID Register contains the bus orderid value for the ring memory access.

Offset = 50h + (j * 100h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG

Table 13-11. RINGACC_ORDERID_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG	3108 0050h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG	2844 0050h + formula

Figure 13-5. RINGACC_ORDERID_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			REPLACE	ORDERID			
R/W-X			R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-12. RINGACC_ORDERID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	REPLACE	R/W	0h	Indicates to replace the bus orderid value for this ring or queue with the orderid MMR field. This allows control over the orderid value when it must be restricted due to the topology for QoS reasons. 0 = bypass and use the orderid from the source transaction for the destination transaction. 1 = use the orderid MMR field value for the destination transaction.
3-0	ORDERID	R/W	0h	Defines the bus orderid value for this ring or queue.

13.2 NAVSS0_UDMASS_RINGACC0_CFG_MON Registers

Table 13-14 lists the memory-mapped registers for the NAVSS0_UDMASS_RINGACC0_CFG_MON. All register offset addresses not listed in Table 13-14 should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Monitor Control / Status Registers region is accessed by setting the `cfg_rsel` signal to 3 during the access. The address map for this region is as follows:

Table 13-13.
NAVSS0_UDMASS_RINGACC0_CFG_MON
Instances

Instance	Base Address
NAVSS0_UDMASS_RINGACC0_CFG_MON	3200 0000h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_MON	2A28 0000h

Table 13-14. NAVSS0_UDMASS_RINGACC0_CFG_MON Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_RINGACC0_CFG_MON Physical Address	MCU_NAVSS0_UDMASS_RINGACC0_CFG_MON Physical Address
0h + formula	RINGACC_CONTROL_j	Monitor Control Register	3200 0000h + formula	2A280 000h + formula
4h + formula	RINGACC_QUEUE_j	Monitor Queue Register	3200 0004h + formula	2A280 004h + formula
8h + formula	RINGACC_DATA0_j	Monitor Data Register	3200 0008h + formula	2A280 008h + formula
Ch + formula	RINGACC_DATA1_j	Monitor Data Register	3200 000Ch + formula	2A280 00Ch + formula

13.2.1 RINGACC_CONTROL_j Register (Offset = 0h + formula) [reset = X]

RINGACC_CONTROL_j is shown in [Figure 13-6](#) and described in [Table 13-16](#).

Return to [Summary Table](#).

Monitor Control Register

Offset = 0h + (j * 1000h); where j = 0h to 1Fh

Table 13-15. RINGACC_CONTROL_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_MON	3200 0000h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_MON	2A28 0000h + formula

Figure 13-6. RINGACC_CONTROL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EVT															
R/W-FFFFh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SOURCE				RESERVED				MODE			
R/W-X				R/W-0h				R/W-X				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-16. RINGACC_CONTROL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	EVT	R/W	FFFFh	Event to produce.
15-12	RESERVED	R/W	X	
11-8	SOURCE	R/W	0h	Monitor source selection. 0 = element count 1 = reserved 2 = reserved
7-3	RESERVED	R/W	X	
2-0	MODE	R/W	0h	Monitor Mode. 0 = disabled. 1 = push/pop statistics capture. 2 = low/high threshold checks. 3 = low/high watermarking. 4 = starvation counting.

13.2.2 RINGACC_QUEUE_j Register (Offset = 4h + formula) [reset = X]

RINGACC_QUEUE_j is shown in [Figure 13-7](#) and described in [Table 13-18](#).

Return to [Summary Table](#).

Monitor Queue Register

Offset = 4h + (j * 1000h); where j = 0h to 1Fh

Table 13-17. RINGACC_QUEUE_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_MON	3200 0004h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_MON	2A28 0000h + formula

Figure 13-7. RINGACC_QUEUE_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-18. RINGACC_QUEUE_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	VAL	R/W	0h	Queue to monitor.

13.2.3 RINGACC_DATA0_j Register (Offset = 8h + formula) [reset = 0h]

RINGACC_DATA0_j is shown in [Figure 13-8](#) and described in [Table 13-20](#).

Return to [Summary Table](#).

Monitor Data Register

Offset = 8h + (j * 1000h); where j = 0h to 1Fh

Table 13-19. RINGACC_DATA0_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_MON	3200 0008h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_MON	2A28 0000h + formula

Figure 13-8. RINGACC_DATA0_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-20. RINGACC_DATA0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Monitor Data. For mode 1 this is read-only and number of pushes. For mode 2 this is read-write and the low threshold value. For mode 3 this is read only and the low watermark. For mode 4 this is read only and the starvation count.

13.2.4 RINGACC_DATA1_j Register (Offset = Ch + formula) [reset = 0h]

RINGACC_DATA1_j is shown in [Figure 13-9](#) and described in [Table 13-22](#).

Return to [Summary Table](#).

Monitor Data Register

Offset = Ch + (j * 1000h); where j = 0h to 1Fh

Table 13-21. RINGACC_DATA1_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_MON	3200 000Ch + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_MON	2A28 0000h + formula

Figure 13-9. RINGACC_DATA1_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-22. RINGACC_DATA1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Monitor Data. For mode 1 this is read-only and number of pops. For mode 2 this is read-write and the high threshold value. For mode 3 this is read only and the high watermark. For mode 4 this is not used.

13.3 NAVSS0_UDMASS_RINGACC0_CFG_RT Registers

Table 13-24 lists the memory-mapped registers for the NAVSS0_UDMASS_RINGACC0_CFG_RT. All register offset addresses not listed in Table 13-24 should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Control /Status Registers region is accessed by setting the cfg_rsel signal to 2 during the access. The address map for this region is as follows:

Table 13-23.
NAVSS0_UDMASS_RINGACC0_CFG_RT Instances

Instance	Base Address
NAVSS0_UDMASS_RINGACC0_CFG_RT	3C00 0000h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT	2B80 0000h

Table 13-24. NAVSS0_UDMASS_RINGACC0_CFG_RT Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_RINGACC0_CFG_RT Physical Address	MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT Physical Address
10h + formula	RINGACC_DB_j	Realtime Ring N Doorbell Register	3C00 0010h + formula	2B80 0010h + formula
18h + formula	RINGACC_OCC_j	Realtime Ring N Occupancy Register	3C00 0018h + formula	2B80 0018h + formula
1Ch + formula	RINGACC_INDX_j	Realtime Ring N Current Index Register	3C00 001Ch + formula	2B80 001Ch + formula
20h + formula	RINGACC_HWOCC_j	Realtime Ring N Hardware Occupancy Register	3C00 0020h + formula	2B80 0020h + formula
24h + formula	RINGACC_HWINDX_j	Realtime Ring N Current Index Register	3C00 0024h + formula	2B80 0024h + formula

13.3.1 RINGACC_DB_j Register (Offset = 10h + formula) [reset = X]

RINGACC_DB_j is shown in [Figure 13-10](#) and described in [Table 13-26](#).

Return to [Summary Table](#).

The Ring N Doorbell Register is written by software to increment or decrement the number of entries on a Ring. One or more entries as specified by the entry_cnt field can be added to a ring with a single write operation.

Offset = 10h + (j * 1000h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG_RT

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT

Table 13-25. RINGACC_DB_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_RT	3C00 0010h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT	2B80 0010h + formula

Figure 13-10. RINGACC_DB_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																CNT															
W-X																W-0h															

LEGEND: W = Write Only; -n = value after reset

Table 13-26. RINGACC_DB_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	W	X	
7-0	CNT	W	0h	Signed number of entries by which to increment the ring occupancy. For normal Tx Ring operation, this value should be a positive number. This occ value for the ring is increased by this value each time the doorbell register is written (occ absolute value will increase or decrease based on the sign of the tentry_cnt).

13.3.2 RINGACC_OCC_j Register (Offset = 18h + formula) [reset = X]

RINGACC_OCC_j is shown in [Figure 13-11](#) and described in [Table 13-28](#).

Return to [Summary Table](#).

The Ring N Occupancy Register can be read by software to determine the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Offset = 18h + (j * 1000h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG_RT

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT

Table 13-27. RINGACC_OCC_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_RT	3C00 0018h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT	2B80 0018h + formula

Figure 13-11. RINGACC_OCC_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CNT																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 13-28. RINGACC_OCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	X	
20-0	CNT	R	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed.

13.3.3 RINGACC_IND_j Register (Offset = 1Ch + formula) [reset = X]

RINGACC_IND_j is shown in [Figure 13-12](#) and described in [Table 13-30](#).

Return to [Summary Table](#).

The Ring N Current Index Register can be read by software for debug purposes to determine the current SW read index for the Ring for the channel.

Offset = 1Ch + (j * 1000h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG_RT

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT

Table 13-29. RINGACC_IND_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_RT	3C00 001Ch + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT	2B80 001Ch + formula

Figure 13-12. RINGACC_IND_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												IDX																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 13-30. RINGACC_IND_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-0	IDX	R	0h	Current SW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by SW each time SW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0.

13.3.4 RINGACC_HWOCC_j Register (Offset = 20h + formula) [reset = X]

RINGACC_HWOCC_j is shown in [Figure 13-13](#) and described in [Table 13-32](#).

Return to [Summary Table](#).

The Ring N Hardware Occupancy Register contains the early increment/decrement version of the the total number of valid entries on a ring. The contents of each of these registers are unary ORed in order to create a pending signal for the ring which can be used for triggering hardware operations and/or for generating interrupts to the host.

Offset = 20h + (j * 1000h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG_RT

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT

Table 13-31. RINGACC_HWOCC_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_RT	3C00 0020h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT	2B80 0020h + formula

Figure 13-13. RINGACC_HWOCC_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												CNT																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 13-32. RINGACC_HWOCC_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	X	
20-0	CNT	R	0h	Total number of valid entries on the ring. This value is generally intended to be incremented by doorbell pokes from software and is decremented by the DMA engine as entries are completed.

13.3.5 RINGACC_HWINDX_j Register (Offset = 24h + formula) [reset = X]

RINGACC_HWINDX_j is shown in [Figure 13-14](#) and described in [Table 13-34](#).

Return to [Summary Table](#).

The Ring N Current Index Register can be read by software for debug purposes to determine the current HW read index for the Ring for the channel.

Offset = 24h + (j * 1000h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_CFG_RT

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT

Table 13-33. RINGACC_HWINDX_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_CFG_RT	3C00 0024h + formula
MCU_NAVSS0_UDMASS_RINGACC0_CFG_RT	2B80 0024h + formula

Figure 13-14. RINGACC_HWINDX_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												IDX																			
R-X												R-0h																			

LEGEND: R = Read Only; -n = value after reset

Table 13-34. RINGACC_HWINDX_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-0	IDX	R	0h	Current HW owned read index for the ring. This value is initialized to 0 when the ring is set up and will be incremented by HW each time HW processes a ring entry. When the index is incremented to a value equal to the size field in the Ring Size Register for the ring the index will be reset back to 0.

13.4 NAVSS0_UDMASS_RINGACC0_GCFG Registers

Table 13-36 lists the memory-mapped registers for the NAVSS0_UDMASS_RINGACC0_GCFG. All register offset addresses not listed in Table 13-36 should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Global Control /Status Registers region is accessed by setting the cfg_rsel signal to 0 during the access. The address map for this region is as follows:

Table 13-35. NAVSS0_UDMASS_RINGACC0_GCFG Instances

Instance	Base Address
NAVSS0_UDMASS_RINGACC0_GCFG	3116 0000h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFG	285D 0000h

Table 13-36. NAVSS0_UDMASS_RINGACC0_GCFG Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_RINGACC0_GCFG Physical Address	MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFG Physical Address
0h	RINGACC_REVISION	Revision Register	3116 0000h	285D 0000h
10h	RINGACC_TRACE_CTL	Trace Control Register	3116 0010h	285D 0010h
20h	RINGACC_OVRFLOW	Overflow Queue Register	3116 0020h	285D 0020h
40h	RINGACC_ERROR_EVT	Error Event Register	3116 0040h	285D 0040h
44h	RINGACC_ERROR_LOG	Error Log Register	3116 0044h	285D 0044h

13.4.1 RINGACC_REVISION Register (Offset = 0h) [reset = 663C9900h]

RINGACC_REVISION is shown in [Figure 13-15](#) and described in [Table 13-38](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 13-37. RINGACC_REVISION Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_GCFG	3116 0000h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFG	285D 0000h

Figure 13-15. Revision Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-663Ch															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM			REVMIN				
R-13h				R-1h				R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 13-38. Revision Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MODID	R	663Ch	Module ID field
15-11	REVRTL	R	13h	RTL revision - 17h for this device.
10-8	REVMAJ	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor revision

13.4.2 RINGACC_TRACE_CTL Register (Offset = 10h) [reset = X]

RINGACC_TRACE_CTL is shown in [Figure 13-16](#) and described in [Table 13-40](#).

Return to [Summary Table](#).

Trace Control Register

Table 13-39. RINGACC_TRACE_CTL Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_GCFG	3116 0010h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFG	285D 0010h

Figure 13-16. RINGACC_TRACE_CTL Register

31	30	29	28	27	26	25	24
EN	ALL_QUEUES	MSG	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-X				
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
QUEUE							
R/W-0h							
7	6	5	4	3	2	1	0
QUEUE							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-40. RINGACC_TRACE_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EN	R/W	0h	Trace enable 0 = disable 1 = enable.
30	ALL_QUEUES	R/W	0h	Trace everything 0 = only the selected queue 1 = every queue.
29	MSG	R/W	0h	Trace message data 0 = include only the operation 1 = include message data.
28-16	RESERVED	R/W	X	
15-0	QUEUE	R/W	0h	Queue number when tracing a single queue.

13.4.3 RINGACC_OVRFLOW Register (Offset = 20h) [reset = X]

RINGACC_OVRFLOW is shown in [Figure 13-17](#) and described in [Table 13-42](#).

Return to [Summary Table](#).

Overflow Queue Register

Table 13-41. RINGACC_OVRFLOW Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_GCFCG	3116 0020h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFCG	285D 0020h

Figure 13-17. RINGACC_OVRFLOW Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																QUEUE															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-42. RINGACC_OVRFLOW Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	QUEUE	R/W	0h	Queue to send overflow messages. A value of 0xFFFF will disable the overflow function.

13.4.4 RINGACC_ERROR_EVT Register (Offset = 40h) [reset = X]

RINGACC_ERROR_EVT is shown in [Figure 13-18](#) and described in [Table 13-44](#).

Return to [Summary Table](#).

Error Event Register

Table 13-43. RINGACC_ERROR_EVT Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_GCFCG	3116 0040h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFCG	285D 0040h

Figure 13-18. RINGACC_ERROR_EVT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-44. RINGACC_ERROR_EVT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT	R/W	FFFFh	Event to send when detecting a bus error.

13.4.5 RINGACC_ERROR_LOG Register (Offset = 44h) [reset = X]

RINGACC_ERROR_LOG is shown in [Figure 13-19](#) and described in [Table 13-46](#).

Return to [Summary Table](#).

Error Log Register. A read of this register will clear the pending error log event and allow a new error to be captured. It does not clear the contents of this register which are only valid while the error event is pending.

Table 13-45. RINGACC_ERROR_LOG Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_GCFG	3116 0044h
MCU_NAVSS0_UDMASS_RINGACC0_CFG_GCFG	285D 0044h

Figure 13-19. RINGACC_ERROR_LOG Register

31	30	29	28	27	26	25	24
PUSH	RESERVED						
R-0h	R-X						
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
QUEUE							
R-0h							
7	6	5	4	3	2	1	0
QUEUE							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 13-46. RINGACC_ERROR_LOG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PUSH	R	0h	Bus error was caused by a push. 0 = pop. 1 = push.
30-16	RESERVED	R	X	
15-0	QUEUE	R	0h	Queue that received the bus error.

13.5 NAVSS0_UDMASS_RINGACC0_SRC_FIFOS Registers

Table 13-48 lists the memory-mapped registers for the NAVSS0_UDMASS_RINGACC0_SRC_FIFOS. All register offset addresses not listed in Table 13-48 should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Queues Registers region is accessed by setting the cfg_crsl signal to 0 during the access. This region provides a set of contiguous 512-byte windows for accessing the rings in a FIFO like manner. The address map for this region is as follows:

Table 13-47.
NAVSS0_UDMASS_RINGACC0_SRC_FIFOS
Instances

Instance	Base Address
NAVSS0_UDMASS_RINGACC0_SRC_FIFOS	3800 0000h
MCU_NAVSS0_UDMASS_RINGACC0_FIFOS	2B00 0000h

Table 13-48. NAVSS0_UDMASS_RINGACC0_SRC_FIFOS Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_RINGACC0_SRC_FIFOS Physical Address	MCU_NAVSS0_UDMASS_RINGACC0_FIFOS Physical Address
0h + formula	RINGACC_RINGHEADDATA_j_y	Ring Head Entry Data Registers	3800 0000h + formula	2B00 0000h + formula
200h + formula	RINGACC_RINGTAILDATA_j_y	Ring Tail Entry Data Registers	3800 0200h + formula	2B00 0200h + formula
400h + formula	RINGACC_PEEKHEADDATA_j_y	Ring Peek Head Entry Data Registers	3800 0400h + formula	2B00 0400h + formula
600h + formula	RINGACC_PEEKTAILDATA_j_y	Ring Peek Tail Entry Data Registers	3800 0600h + formula	2B00 0600h + formula

13.5.1 RINGACC_RINGHEADDATA_j_y Register (Offset = 0h + formula) [reset = 0h]

RINGACC_RINGHEADDATA_j_y is shown in [Figure 13-20](#) and described in [Table 13-50](#).

Return to [Summary Table](#).

The Ring Head Entry Data Registers contain the data which is to be written or which was read from the ring head. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring head element for reads or writes. The data is right justified.)

Offset = 0h + (j * 1000h) + (y * 4h); where

j = 0h to 331h, y = 0h to 7Fh for NAVSS0_UDMASS_RINGACC0_SRC_FIFOS

j = 0h to 11Dh, y = 0h to 7Fh for MCU_NAVSS0_UDMASS_RINGACC0_FIFOS

**Table 13-49. RINGACC_RINGHEADDATA_j_y
Instances**

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_SRC_FIFOS	3800 0000h + formula
MCU_NAVSS0_UDMASS_RINGACC0_FIFOS	2B00 0000h + formula

Figure 13-20. RINGACC_RINGHEADDATA_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-50. RINGACC_RINGHEADDATA_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Block of ring head element data

13.5.2 RINGACC_RINGTAILDATA_j_y Register (Offset = 200h + formula) [reset = 0h]

RINGACC_RINGTAILDATA_j_y is shown in [Figure 13-21](#) and described in [Table 13-52](#).

Return to [Summary Table](#).

The Ring Tail Entry Data Registers contain the data which is to be written or which was read from the ring tail. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring tail element for reads or writes. The data is right justified.)

Offset = 200h + (j * 1000h) + (y * 4h); where

j = 0h to 331h, y = 0h to 7Fh for NAVSS0_UDMASS_RINGACC0_SRC_FIFOS

j = 0h to 11Dh, y = 0h to 7Fh for MCU_NAVSS0_UDMASS_RINGACC0_FIFOS

**Table 13-51. RINGACC_RINGTAILDATA_j_y
Instances**

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_SRC_FIFOS	3800 0200h + formula
MCU_NAVSS0_UDMASS_RINGACC0_FIFOS	2B00 0200h + formula

Figure 13-21. RINGACC_RINGTAILDATA_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-52. RINGACC_RINGTAILDATA_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Block of ring tail element data

13.5.3 RINGACC_PEEKHEADDATA_j_y Register (Offset = 400h + formula) [reset = 0h]

RINGACC_PEEKHEADDATA_j_y is shown in [Figure 13-22](#) and described in [Table 13-54](#).

Return to [Summary Table](#).

The Ring Peek Head Entry Data Registers contain the data which is to be read from the ring head without removing the element. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring head element for reads. Writes are ignored. The data is right justified.)

Offset = 400h + (j * 1000h) + (y * 4h); where

j = 0h to 331h, y = 0h to 7Fh for NAVSS0_UDMASS_RINGACC0_SRC_FIFOS

j = 0h to 11Dh, y = 0h to 7Fh for MCU_NAVSS0_UDMASS_RINGACC0_FIFOS

**Table 13-53. RINGACC_PEEKHEADDATA_j_y
Instances**

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_SRC_FIFOS	3800 0400h + formula
MCU_NAVSS0_UDMASS_RINGACC0_FIFOS	2B00 0400h + formula

Figure 13-22. RINGACC_PEEKHEADDATA_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-54. RINGACC_PEEKHEADDATA_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Block of ring head element data. Not supported in ring mode.

13.5.4 RINGACC_PEEKTAILDATA_j_y Register (Offset = 600h + formula) [reset = 0h]

RINGACC_PEEKTAILDATA_j_y is shown in [Figure 13-23](#) and described in [Table 13-56](#).

Return to [Summary Table](#).

The Ring Peek Tail Entry Data Registers contain the data which is to be read from the ring tail without removing the element. These registers are virtual and non-static (i.e. they are just address locations that are used to access the ring tail element for reads. Writes are ignored. The data is right justified.)

Offset = 600h + (j * 1000h) + (y * 4h); where

j = 0h to 331h, y = 0h to 7Fh for NAVSS0_UDMASS_RINGACC0_SRC_FIFOS

j = 0h to 11Dh, y = 0h to 7Fh for MCU_NAVSS0_UDMASS_RINGACC0_FIFOS

**Table 13-55. RINGACC_PEEKTAILDATA_j_y
Instances**

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_SRC_FIFOS	3800 0600h + formula
MCU_NAVSS0_UDMASS_RINGACC0_FIFOS	2B00 0600h + formula

Figure 13-23. RINGACC_PEEKTAILDATA_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-56. RINGACC_PEEKTAILDATA_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Block of ring tail element data. Not supported in ring mode.

13.6 UDMASS_RINGACC0_ISC_ISC Registers

Table 13-58 lists the memory-mapped registers for the UDMASS_RINGACC0_ISC_ISC. All register offset addresses not listed in Table 13-58 should be considered as reserved locations and the register contents should not be modified.

The Ring Accelerator Ring ISC Registers region is for security controls. The address map for this region is as follows:

**Table 13-57. UDMASS_RINGACC0_ISC_ISC
Instances**

Instance	Base Address
NAVSS0_UDMASS_RINGACC0_ISC_ISC	458C 0000h
MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC	4582 0000h

Table 13-58. UDMASS_RINGACC0_ISC_ISC Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_RINGACC0_ISC_ISC Physical Address	MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC Physical Address
0h + formula	RINGACC_CONTROL_j	ISC a Region b Control Register	458C 0000h + formula	4582 0000h + formula
4h + formula	RINGACC_CONTROL2_j	ISC a Region b Control Register 2	458C 0004h + formula	4582 0004h + formula

13.6.1 RINGACC_CONTROL_j Register (Offset = 0h + formula) [reset = X]

RINGACC_CONTROL_j is shown in [Figure 13-24](#) and described in [Table 13-60](#).

Return to [Summary Table](#).

The ISC a Region b Control Register defines the control fields for the ISC.

Offset = 0h + (j * 20h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_ISC_ISC

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC

Table 13-59. RINGACC_CONTROL_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_ISC_ISC	458C 0000h + formula
MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC	4582 0000h + formula

Figure 13-24. RINGACC_CONTROL_j Register

31	30	29	28	27	26	25	24
RESERVED				NOPRIV		PRIV	
R/W-X				R/W-0h		R/W-0h	
23	22	21	20	19	18	17	16
RESERVED		PASS	NONSEC	SEC			
R/W-X		R/W-0h	R/W-0h	R/W-0h			
15	14	13	12	11	10	9	8
PRIV_ID							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-60. RINGACC_CONTROL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	X	
27-26	NOPRIV	R/W	0h	Clear output priv attribute. If each bit is set then the outgoing priv bit is cleared. Has precedence over priv set bits.
25-24	PRIV	R/W	0h	Set outgoing priv attribute. If each bit is set then the outgoing priv bit is set.
23-22	RESERVED	R/W	X	
21	PASS	R/W	0h	No privID replacement, pass through value.
20	NONSEC	R/W	0h	Make outgoing non-secure. Has precedence over secure enable bits.
19-16	SEC	R/W	0h	Make outgoing secure. A value of 0xA enables, others disable.
15-8	PRIV_ID	R/W	X	Priv ID.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set the region values cannot be modified.

Table 13-60. RINGACC_CONTROL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

13.6.2 RINGACC_CONTROL2_j Register (Offset = 4h + formula) [reset = X]

RINGACC_CONTROL2_j is shown in [Figure 13-25](#) and described in [Table 13-62](#).

Return to [Summary Table](#).

The ISC a Region b Control Register 2 defines the control fields for the ISC.

Offset = 4h + (j * 20h); where

j = 0h to 331h for NAVSS0_UDMASS_RINGACC0_ISC_ISC

j = 0h to 11Dh for MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC

Table 13-61. RINGACC_CONTROL2_j Instances

Instance	Physical Address
NAVSS0_UDMASS_RINGACC0_ISC_ISC	458C 0004h + formula
MCU_NAVSS0_UDMASS_RINGACC0_ISC_ISC	4582 0004h + formula

Figure 13-25. RINGACC_CONTROL2_j Register

31	30	29	28	27	26	25	24
PASS_V	RESERVED				VIRTID		
R/W-0h	R/W-X				R/W-0h		
23	22	21	20	19	18	17	16
VIRTID							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-62. RINGACC_CONTROL2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PASS_V	R/W	0h	No virtID replacement, pass through value.
30-28	RESERVED	R/W	X	
27-16	VIRTID	R/W	0h	Virt ID.
15-0	RESERVED	R/W	X	

14 Proxy Registers

14.1 NAVSS0_PROXY_BUF Registers

Table 14-2 lists the memory-mapped registers for the NAVSS0_PROXY_BUF. All register offset addresses not listed in Table 14-2 should be considered as reserved locations and the register contents should not be modified.

Proxy Buffer RAM Debug region.

Table 14-1. NAVSS0_PROXY_BUF Instances

Instance	Base Address
NAVSS0_PROXY_BUF	3113 0000h
MCU_NAVSS0_PROXY_CFG_BUF	285A 0000h

Table 14-2. NAVSS0_PROXY_BUF Registers

Offset	Acronym	Register Name	NAVSS0_PROXY_BUF Physical Address	MCU_NAVSS0_PROXY_CFG_BUF Physical Address
0h + formula	PROXY_DATA_y	Proxy Buffer Register	3113 0000h + formula	285A 0000h + formula

14.1.1 PROXY_DATA_y Register (Offset = 0h + formula) [reset = 0h]

PROXY_DATA_y is shown in [Figure 14-1](#) and described in [Table 14-4](#).

Return to [Summary Table](#).

The Proxy Buffer for the proxy

Offset = 0h + (y * 4h); where y = 0h to FFFh

Table 14-3. PROXY_DATA_y Instances

Instance	Physical Address
NAVSS0_PROXY_BUF	3113 0000h + formula
MCU_NAVSS0_PROXY_CFG_BUF	285A 0000h + formula

Figure 14-1. PROXY_DATA_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-4. PROXY_DATA_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Proxy Buffer Data

14.2 NAVSS0_PROXY_TARGET0_DATA Registers

Table 14-6 lists the memory-mapped registers for the NAVSS0_PROXY_TARGET0_DATA. All register offset addresses not listed in Table 14-6 should be considered as reserved locations and the register contents should not be modified.

Proxy Datapath Region for Target 0.

**Table 14-5. NAVSS0_PROXY_TARGET0_DATA
Instances**

Instance	Base Address
NAVSS0_PROXY_TARGET0_DATA	3300 0000h
MCU_NAVSS0_PROXY0_TARGET0_DATA	2A50 0000h

Table 14-6. NAVSS0_PROXY_TARGET0_DATA Registers

Offset	Acronym	Register Name	NAVSS0_PROXY_TARGET0_DATA Physical Address	MCU_NAVSS0_PROXY0_TARGET0_DATA Physical Address
0h + formula	PROXY_CTL_j	Proxy Control Register	3300 0000h + formula	2A50 0000h + formula
4h + formula	PROXY_STATUS_j	Proxy Status Register	3300 0004h + formula	2A50 0004h + formula
200h + formula	PROXY_DATA_j_y	Proxy Data Register	3300 0200h + formula	2A50 0200h + formula

14.2.1 PROXY_CTL_j Register (Offset = 0h + formula) [reset = X]

PROXY_CTL_j is shown in [Figure 14-2](#) and described in [Table 14-8](#).

Return to [Summary Table](#).

The Proxy Control for the proxy. **NOTE:** This register must be written only via 32-bit accesses. 64-bit writes are not supported and may result in data loss.

Offset = 0h + (j * 1000h); where j = 0h to 3Fh

Table 14-7. PROXY_CTL_j Instances

Instance	Physical Address
NAVSS0_PROXY_TARGET0_DATA	3300 0000h + formula
MCU_NAVSS0_PROXY0_TARGET0_D ATA	2A50 0000h + formula

Figure 14-2. PROXY_CTL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					ELSIZE				RESERVED					MODE	
R/W-X					R/W-0h				R/W-X					R/W-0h	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUEUE															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-8. PROXY_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	ELSIZE	R/W	0h	Queue element size. This field is encoded as follows: 0 = 4 bytes 1 = 8 bytes 2 = 16 bytes 3 = 32 bytes 4 = 64 bytes 5 = 128 bytes 6 = 256 bytes 7 = 512 bytes
23-18	RESERVED	R/W	X	
17-16	MODE	R/W	0h	Proxy Queue Mode that determines how to access the queue. 0h = access the head of the queue 1h = access the tail of the queue 2h = peek access the head of the queue 3h = peek access the tail of the queue. NOT SUPPORTED
15-0	QUEUE	R/W	0h	Proxy Queue

14.2.2 PROXY_STATUS_j Register (Offset = 4h + formula) [reset = X]

PROXY_STATUS_j is shown in [Figure 14-3](#) and described in [Table 14-10](#).

Return to [Summary Table](#).

The Proxy Status for the proxy. **NOTE:** This register must be written only via 32-bit accesses. 64-bit writes are not supported and may result in data loss.

Offset = 4h + (j * 1000h); where j = 0h to 3Fh

Table 14-9. PROXY_STATUS_j Instances

Instance	Physical Address
NAVSS0_PROXY_TARGET0_DATA	3300 0004h + formula
MCU_NAVSS0_PROXY0_TARGET0_D ATA	2A50 0004h + formula

Figure 14-3. PROXY_STATUS_j Register

31	30	29	28	27	26	25	24
ERROR	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-10. PROXY_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERROR	R/W	0h	Proxy Error status
30-0	RESERVED	R/W	X	

14.2.3 PROXY_DATA_j_y Register (Offset = 200h + formula) [reset = 0h]

PROXY_DATA_j_y is shown in [Figure 14-4](#) and described in [Table 14-12](#).

Return to [Summary Table](#).

The Proxy Data for the proxy, target and channel

Offset = 200h + (j * 1000h) + (y * 4h); where j = 0h to 3Fh, y = 0h to 7Fh

Table 14-11. PROXY_DATA_j_y Instances

Instance	Physical Address
NAVSS0_PROXY_TARGET0_DATA	3300 0200h + formula
MCU_NAVSS0_PROXY0_TARGET0_D ATA	2A50 0200h + formula

Figure 14-4. PROXY_DATA_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-12. PROXY_DATA_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R/W	0h	Proxy Data

14.3 NAVSS0_PROXY0_BUF_CFG Registers

Table 14-14 lists the memory-mapped registers for the NAVSS0_PROXY0_BUF_CFG. All register offset addresses not listed in Table 14-14 should be considered as reserved locations and the register contents should not be modified.

Proxy Config Region

Table 14-13. NAVSS0_PROXY0_BUF_CFG Instances

Instance	Base Address
NAVSS0_PROXY0_BUF_CFG	3340 0000h
MCU_NAVSS0_PROXY0_BUF_CFG	2A58 0000h

Table 14-14. NAVSS0_PROXY0_BUF_CFG Registers

Offset	Acronym	Register Name	NAVSS0_PROXY0_BUF_CFG Physical Address	MCU_NAVSS0_PROXY0_BUF_CFG Physical Address
0h + formula	PROXY_EVT_REG_j	Proxy Event Register	3340 0000h + formula	2A580 000h + formula

14.3.1 PROXY_EVT_REG_j Register (Offset = 0h + formula) [reset = X]

PROXY_EVT_REG_j is shown in [Figure 14-5](#) and described in [Table 14-16](#).

Return to [Summary Table](#).

The Proxy Event for the proxy

Offset = 0h + (j * 1000h); where j = 0h to 3Fh

Table 14-15. PROXY_EVT_REG_j Instances

Instance	Physical Address
NAVSS0_PROXY0_BUF_CFG	3340 0000h + formula
MCU_NAVSS0_PROXY0_BUF_CFG	2A58 0000h + formula

Figure 14-5. PROXY_EVT_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ERR_EVENT															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-16. PROXY_EVT_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	ERR_EVENT	R/W	FFFFh	Proxy Error Event

14.4 NAVSS0_PROXY0_CFG_BUF_CFG Registers

[Table 14-18](#) lists the memory-mapped registers for the NAVSS0_PROXY0_CFG_BUF_CFG. All register offset addresses not listed in [Table 14-18](#) should be considered as reserved locations and the register contents should not be modified.

Proxy Global Config Region.

Table 14-17. NAVSS0_PROXY0_CFG_BUF_CFG Instances

Instance	Base Address
NAVSS0_PROXY0_CFG_BUF_CFG	3112 0000h
MCU_NAVSS0_PROXY_CFG_GCFCG	2859 0000h

Table 14-18. NAVSS0_PROXY0_CFG_BUF_CFG Registers

Offset	Acronym	Register Name	NAVSS0_PROXY0_CFG_BUF_CFG Physical Address	MCU_NAVSS0_PROXY_CFG_GCFCG Physical Address
0h	PROXY_PID	Revision Register	3112 0000h	2859 0000h
4h	PROXY_CONFIG	Config Register	3112 0004h	2859 0004h

14.4.1 PROXY_PID Register (Offset = 0h) [reset = Xh]

PROXY_PID is shown in [Figure 14-6](#) and described in [Table 14-20](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Reset = 66344100h

Table 14-19. PROXY_PID Instances

Instance	Physical Address
NAVSS0_PROXY0_CFG_BUF_CFG	3112 0000h
MCU_NAVSS0_PROXY_CFG_GCFG	2859 0000h

Figure 14-6. PROXY_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-634h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-Xh					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 14-20. PROXY_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	634h	Module ID
15-11	RTL	R	Xh	RTL revision. 8h in this device.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

14.4.2 PROXY_CONFIG Register (Offset = 4h) [reset = X]

PROXY_CONFIG is shown in [Figure 14-7](#) and described in [Table 14-22](#).

Return to [Summary Table](#).

The Config Register shows configured params.

Table 14-21. PROXY_CONFIG Instances

Instance	Physical Address
NAVSS0_PROXY0_CFG_BUF_CFG	3112 0004h
MCU_NAVSS0_PROXY_CFG_GCFCG	2859 0004h

Figure 14-7. PROXY_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																THREADS															
R-X																R-40h															

LEGEND: R = Read Only; -n = value after reset

Table 14-22. PROXY_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	THREADS	R	40h	Number of proxy threads supported.

15 Secure Proxy Registers

15.1 NAVSS0_SEC_PROXY0_CFG_MMRS Registers

Table 15-2 lists the memory-mapped registers for the NAVSS0_SEC_PROXY0_CFG_MMRS. All register offset addresses not listed in Table 15-2 should be considered as reserved locations and the register contents should not be modified.

Sec Proxy Config Region

**Table 15-1. NAVSS0_SEC_PROXY0_CFG_MMRS
Instances**

Instance	Base Address
NAVSS0_SEC_PROXY0_CFG_MMRS	3114 0000h
MCU_NAVSS0_SEC_PROXY0_CFG	285B 0000h

Table 15-2. NAVSS0_SEC_PROXY0_CFG_MMRS Registers

Offset	Acronym	Register Name	NAVSS0_SEC_PROXY0_CFG_MMRS Physical Address	MCU_NAVSS0_SEC_PROXY0_CFG Physical Address
0h	SEC_PROXY_PID	Revision Register	3114 0000h	285B 0000h
4h	SEC_PROXY_CONFIG	Config Register	3114 0004h	285B 0004h

15.1.1 SEC_PROXY_PID Register (Offset = 0h) [reset = 66363100h]

SEC_PROXY_PID is shown in [Figure 15-1](#) and described in [Table 15-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 15-3. SEC_PROXY_PID Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_MMRS	3114 0000h
MCU_NAVSS0_SEC_PROXY0_CFG	285B 0000h

Figure 15-1. SEC_PROXY_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-636h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-6h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 15-4. SEC_PROXY_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	636h	Module ID
15-11	RTL	R	6h	RTL revision. 8h in this device.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

15.1.2 SEC_PROXY_CONFIG Register (Offset = 4h) [reset = 004000A0h]

SEC_PROXY_CONFIG is shown in [Figure 15-2](#) and described in [Table 15-6](#).

Return to [Summary Table](#).

The Config Register shows configured params.

Table 15-5. SEC_PROXY_CONFIG Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_MMRS	3114 0004h
MCU_NAVSS0_SEC_PROXY0_CFG	285B 0004h

Figure 15-2. SEC_PROXY_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSG_SIZE																THREADS															
R-40h																R-A0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-6. SEC_PROXY_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	MSG_SIZE	R	40h	Supported message size in bytes.
15-0	THREADS	R	A0h	Number of proxy threads supported.

15.2 NAVSS0_SEC_PROXY0_CFG_RT Registers

Table 15-8 lists the memory-mapped registers for the NAVSS0_SEC_PROXY0_CFG_RT. All register offset addresses not listed in Table 15-8 should be considered as reserved locations and the register contents should not be modified.

Sec Proxy Realtime Region.

**Table 15-7. NAVSS0_SEC_PROXY0_CFG_RT
Instances**

Instance	Base Address
NAVSS0_SEC_PROXY0_CFG_RT	3240 0000h
MCU_NAVSS0_SEC_PROXY0_CFG_RT	2A38 0000h

Table 15-8. SEC_PROXY0_CFG_RT Registers

Offset	Acronym	Register Name	NAVSS0_SEC_PROXY0_CFG_RT Physical Address	MCU_NAVSS0_SEC_PROXY0_CFG_RT Physical Address
0h + formula	SEC_PROXY_STATUS_j	Status Register	3240 0000h + formula	2A38 0000h + formula
4h + formula	SEC_PROXY_THR_j	Threshold Register	3240 0004h + formula	2A38 0004h + formula

15.2.1 SEC_PROXY_STATUS_j Register (Offset = 0h + formula) [reset = X]

SEC_PROXY_STATUS_j is shown in [Figure 15-3](#) and described in [Table 15-10](#).

Return to [Summary Table](#).

The Status Register gives status for proxy thread j.

Offset = 0h + (j * 1000h); where

j = 0h to 9Fh for NAVSS0_SEC_PROXY0_CFG_RT

j = 0h to 59h for MCU_NAVSS0_SEC_PROXY0_CFG_RT

Table 15-9. SEC_PROXY_STATUS_j Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_RT	3240 0000h + formula
MCU_NAVSS0_SEC_PROXY0_CFG_RT	2A38 0000h + formula

Figure 15-3. SEC_PROXY_STATUS_j Register

31	30	29	28	27	26	25	24
ERROR	DIR	RESERVED					
R/W-0h	R-0h	R/W-X					
23	22	21	20	19	18	17	16
MAX_CNT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
CUR_CNT							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-10. SEC_PROXY_STATUS_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ERROR	R/W	0h	Error detected on proxy thread. The error will also use the err_evt field to generate an error event which can generate an interrupt. While in error a proxy thread will not process any operations. Write a 0 to clear the error and reset the proxy thread.
30	DIR	R	0h	Direction for the proxy thread. 0 = outbound, write only. 1 = inbound, read only.
29-24	RESERVED	R/W	X	
23-16	MAX_CNT	R	0h	Max message count allowed for an outbound proxy thread.
15-8	RESERVED	R/W	X	
7-0	CUR_CNT	R	0h	Current message count for the proxy thread. For an inbound proxy this is the number of available messages. For an outbound proxy this is the number of free messages that can be written.

15.2.2 SEC_PROXY_THR_j Register (Offset = 4h + formula) [reset = X]

SEC_PROXY_THR_j is shown in [Figure 15-4](#) and described in [Table 15-12](#).

Return to [Summary Table](#).

The Threshold Register controls the threshold for proxy thread j events.

Offset = 4h + (j * 1000h); where

j = 0h to 9Fh for NAVSS0_SEC_PROXY0_CFG_RT

j = 0h to 59h for MCU_NAVSS0_SEC_PROXY0_CFG_RT

Table 15-11. SEC_PROXY_THR_j Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_RT	3240 0004h + formula
MCU_NAVSS0_SEC_PROXY0_CFG_RT	2A38 0004h + formula

Figure 15-4. SEC_PROXY_THR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								THR_CNT							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-12. SEC_PROXY_THR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	THR_CNT	R/W	0h	Threshold count that causes proxy thread events. For an outbound proxy this will be the number of free messages to cause an event. For an inbound proxy this will be the number of available messages to cause an event.

15.3 NAVSS0_SEC_PROXY0_CFG_SCFG Registers

Table 15-14 lists the memory-mapped registers for the NAVSS0_SEC_PROXY0_CFG_SCFG. All register offset addresses not listed in Table 15-14 should be considered as reserved locations and the register contents should not be modified.

Sec Proxy Secure Config Region

Table 15-13. NAVSS0_SEC_PROXY0_CFG_SCFG Instances

Instance	Base Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 0000h
MCU_NAVSS0_SEC_PROXY0_CFG_SCFG	2A40 0000h

Table 15-14. NAVSS0_SEC_PROXY0_CFG_SCFG Registers

Offset	Acronym	Register Name	NAVSS0_SEC_PROXY0_CFG_SCFG Physical Address	MCU_NAVSS0_SEC_PROXY0_CFG_SCFG Physical Address
0h	SEC_PROXY_BUFFER_L	Buffer Register	3280 0000h	2A40 0000h
4h	SEC_PROXY_BUFFER_H	Buffer Register	3280 0004h	2A40 0004h
8h	SEC_PROXY_TARGET_L	Target Register	3280 0008h	2A40 0008h
Ch	SEC_PROXY_TARGET_H	Target Register	3280 000Ch	2A40 000Ch
10h	SEC_PROXY_ORDERID	Buffer OrderID Register	3280 0010h	2A40 0010h
1000h + formula	SEC_PROXY_CTL_j	Control Register	3280 1000h + formula	2A40 1000h + formula
1004h + formula	SEC_PROXY_EVT_MAP_j	Event Map Register	3280 1004h + formula	2A40 1004h + formula
1008h + formula	SEC_PROXY_DST_j	Destination Register	3280 1008h + formula	2A40 1008h + formula

15.3.1 SEC_PROXY_BUFFER_L Register (Offset = 0h) [reset = 0h]

SEC_PROXY_BUFFER_L is shown in [Figure 15-5](#) and described in [Table 15-16](#).

Return to [Summary Table](#).

The Buffer Register defines the pointer for the external buffer.

Table 15-15. SEC_PROXY_BUFFER_L Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 0000h
MCU_NAVSS0_SEC_PROXY0_CFG_S CFG	2A40 0000h

Figure 15-5. SEC_PROXY_BUFFER_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE_L																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-16. SEC_PROXY_BUFFER_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE_L	R/W	0h	The base address for the external buffer, lower 32 bits.

15.3.2 SEC_PROXY_BUFFER_H Register (Offset = 4h) [reset = X]

SEC_PROXY_BUFFER_H is shown in [Figure 15-6](#) and described in [Table 15-18](#).

Return to [Summary Table](#).

The Buffer Register defines the pointer for the external buffer.

Table 15-17. SEC_PROXY_BUFFER_H Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 0004h
MCU_NAVSS0_SEC_PROXY0_CFG_SCFG	2A40 0004h

Figure 15-6. SEC_PROXY_BUFFER_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-18. SEC_PROXY_BUFFER_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	BASE_H	R/W	0h	The base address for the external buffer, upper 16 bits.

15.3.3 SEC_PROXY_TARGET_L Register (Offset = 8h) [reset = 38300000h]

SEC_PROXY_TARGET_L is shown in [Figure 15-7](#) and described in [Table 15-20](#).

Return to [Summary Table](#).

The Target Register defines the pointer for the external target.

Table 15-19. SEC_PROXY_TARGET_L Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 0008h
MCU_NAVSS0_SEC_PROXY0_CFG_S CFG	2A40 0008h

Figure 15-7. SEC_PROXY_TARGET_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE_L																															
R/W-38300000h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-20. SEC_PROXY_TARGET_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BASE_L	R/W	38300000h	The base address for the external target, lower 32 bits.

15.3.4 SEC_PROXY_TARGET_H Register (Offset = Ch) [reset = X]

SEC_PROXY_TARGET_H is shown in [Figure 15-8](#) and described in [Table 15-22](#).

Return to [Summary Table](#).

The Target Register defines the pointer for the external target.

Table 15-21. SEC_PROXY_TARGET_H Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 000Ch
MCU_NAVSS0_SEC_PROXY0_CFG_SCFG	2A40 000Ch

Figure 15-8. SEC_PROXY_TARGET_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																BASE_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-22. SEC_PROXY_TARGET_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	BASE_H	R/W	0h	The base address for the external target, upper 16 bits.

15.3.5 SEC_PROXY_ORDERID Register (Offset = 10h) [reset = X]

SEC_PROXY_ORDERID is shown in [Figure 15-9](#) and described in [Table 15-24](#).

Return to [Summary Table](#).

The Buffer OrderID Register contains the bus SEC_PROXY_ORDERID value for the buffer memory access.

Table 15-23. SEC_PROXY_ORDERID Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 0010h
MCU_NAVSS0_SEC_PROXY0_CFG_SCFG	2A40 0010h

Figure 15-9. SEC_PROXY_ORDERID Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			REPLACE	ORDERID			
R/W-X			R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-24. SEC_PROXY_ORDERID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4	REPLACE	R/W	0h	Indicates to replace the bus OrderID value for the buffer access with the ORDERID register field. 0 = bypass and use the OrderID from the source transaction for the destination transaction. 1 = use the ORDERID register field value for the destination transaction.
3-0	ORDERID	R/W	0h	Defines the bus OrderID value for the buffer access.

15.3.6 SEC_PROXY_CTL_j Register (Offset = 1000h + formula) [reset = X]

SEC_PROXY_CTL_j is shown in [Figure 15-10](#) and described in [Table 15-26](#).

Return to [Summary Table](#).

The Control Register defines controls for proxy thread a.

Offset = 1000h + (j * 1000h); where

j = 0h to 9Fh for NAVSS0_SEC_PROXY0_CFG_SCFG

j = 0h to 59h for MCU_NAVSS0_SEC_PROXY0_CFG_SCFG

Table 15-25. SEC_PROXY_CTL_j Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 1000h + formula
MCU_NAVSS0_SEC_PROXY0_CFG_SCFG	2A40 1000h + formula

Figure 15-10. SEC_PROXY_CTL_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIR	RESERVED							MAX_CNT							
R/W-0h	R/W-X							R/W-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QUEUE															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-26. SEC_PROXY_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DIR	R/W	0h	Direction for the proxy thread. 0 = outbound, write only. 1 = inbound, read only.
30-24	RESERVED	R/W	X	
23-16	MAX_CNT	R/W	0h	Max message count allowed for an outbound proxy thread. Is not used otherwise.
15-0	QUEUE	R/W	0h	Queue number in the target to use for the proxy thread. If the target base does not start at queue 0 then this is the relative queue number from that base queue.

15.3.7 SEC_PROXY_EVT_MAP_j Register (Offset = 1004h + formula) [reset = FFFFFFFFh]

SEC_PROXY_EVT_MAP_j is shown in [Figure 15-11](#) and described in [Table 15-28](#).

Return to [Summary Table](#).

The Event Map Register defines the event numbers for proxy thread a.

Offset = 1004h + (j * 1000h); where

j = 0h to 9Fh for NAVSS0_SEC_PROXY0_CFG_SCFG

j = 0h to 59h for MCU_NAVSS0_SEC_PROXY0_CFG_SCFG

Table 15-27. SEC_PROXY_EVT_MAP_j Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 1004h + formula
MCU_NAVSS0_SEC_PROXY0_CFG_S CFG	2A40 1004h + formula

Figure 15-11. SEC_PROXY_EVT_MAP_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR_EVT																THR_EVT															
R/W-FFFFh																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-28. SEC_PROXY_EVT_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	ERR_EVT	R/W	FFFFh	Event number for an error from the proxy thread.
15-0	THR_EVT	R/W	FFFFh	Event number for a threshold event from the proxy thread.

15.3.8 SEC_PROXY_DST_j Register (Offset = 1008h + formula) [reset = X]

SEC_PROXY_DST_j is shown in [Figure 15-12](#) and described in [Table 15-30](#).

Return to [Summary Table](#).

The Destination Register defines the destination proxy thread for outbound proxy thread a.

Offset = 1008h + (j * 1000h); where

j = 0h to 9Fh for NAVSS0_SEC_PROXY0_CFG_SCFG

j = 0h to 59h for MCU_NAVSS0_SEC_PROXY0_CFG_SCFG

Table 15-29. SEC_PROXY_DST_j Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_CFG_SCFG	3280 1008h + formula
MCU_NAVSS0_SEC_PROXY0_CFG_SCFG	2A40 1008h + formula

Figure 15-12. SEC_PROXY_DST_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																THREAD															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-30. SEC_PROXY_DST_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	THREAD	R/W	0h	The proxy thread that is the destination of messages from this outbound proxy thread, based on the queue numbers. This is ignored for inbound proxy threads.

15.4 NAVSS0_SEC_PROXY0_SRC_TARGET_DATA Registers

Table 15-32 lists the memory-mapped registers for the NAVSS0_SEC_PROXY0_SRC_TARGET_DATA. All register offset addresses not listed in Table 15-32 should be considered as reserved locations and the register contents should not be modified.

Proxy Datapath Region for Target

Table 15-31.
NAVSS0_SEC_PROXY0_SRC_TARGET_DATA
Instances

Instance	Base Address
NAVSS0_SEC_PROXY0_SRC_TARGET_DATA	32C0 0000h
MCU_NAVSS0_SEC_PROXY0_TARGET_DATA	2A48 0000h

Table 15-32. SEC_PROXY0_SRC_TARGET_DATA Registers

Offset	Acronym	Register Name	NAVSS0_SEC_PROXY0_SRC_TARGET_DATA Physical Address	MCU_NAVSS0_SEC_PROXY0_TARGET_DATA Physical Address
0h + formula	SEC_PROXY_DATA_j	Proxy Private Register	32C0 0000h + formula	2A48 0000h + formula
4h + formula	SEC_PROXY_MESSAGE_j_y	Proxy Message Register	32C0 0004h + formula	2A48 0004h + formula

15.4.1 SEC_PROXY_DATA_j Register (Offset = 0h + formula) [reset = X]

SEC_PROXY_DATA_j is shown in [Figure 15-13](#) and described in [Table 15-34](#).

Return to [Summary Table](#).

The Proxy Private register contains private information for the proxy thread a and should not be written, writes are ignored. Reads are allowed to know the source thread of the message.

Offset = 0h + (j * 1000h); where

j = 0h to 9Fh for NAVSS0_SEC_PROXY0_SRC_TARGET_DATA

j = 0h to 59h for MCU_NAVSS0_SEC_PROXY0_TARGET_DATA

Table 15-33. SEC_PROXY_DATA_j Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_SRC_TARGET_DATA	32C0 0000h + formula
MCU_NAVSS0_SEC_PROXY0_TARGET_DATA	2A48 0000h + formula

Figure 15-13. SEC_PROXY_DATA_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						SRC_THR															
R-X																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 15-34. SEC_PROXY_DATA_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	SRC_THR	R	0h	Proxy source thread of message.

15.4.2 SEC_PROXY_MESSAGE_j_y Register (Offset = 4h + formula) [reset = 0h]

SEC_PROXY_MESSAGE_j_y is shown in [Figure 15-14](#) and described in [Table 15-36](#).

Return to [Summary Table](#).

The Message Data for proxy thread a. The word with index b = 14 contains the completion final byte.

Offset = 4h + (j * 1000h) + (y * 4h); where

j = 0h to 9Fh, y = 0h to Eh for NAVSS0_SEC_PROXY0_SRC_TARGET_DATA

j = 0h to 59h, y = 0h to Eh for MCU_NAVSS0_SEC_PROXY0_TARGET_DATA

Table 15-35. SEC_PROXY_MESSAGE_j_y Instances

Instance	Physical Address
NAVSS0_SEC_PROXY0_SRC_TARGET_DATA	32C0 0004h + formula
MCU_NAVSS0_SEC_PROXY0_TARGET_DATA	2A48 0004h + formula

Figure 15-14. SEC_PROXY_MESSAGE_j_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-36. SEC_PROXY_MESSAGE_j_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Proxy Message Data

16 INTR_AGGR Registers

16.1 MODSS_INTA_CFG Registers

Table 16-2 lists the memory-mapped registers for the MODSS_INTA_CFG. All register offset addresses not listed in Table 16-2 should be considered as reserved locations and the register contents should not be modified.

The Interrupt Aggregator Global Registers region is accessed by setting the cfg_rsel signal to 0 during the access. The address map for this region is as follows:

Table 16-1. MODSS_INTA_CFG Instances

Instance	Base Address
NAVSS0_MODSS_INTA0_CFG	3080 0000h
NAVSS0_MODSS_INTA1_CFG	3080 1000h

Table 16-2. MODSS_INTA_CFG Registers

Offset	Acronym	Register Name	NAVSS0_MODSS_INTA 0_CFG Physical Address	NAVSS0_MODSS_INTA 1_CFG Physical Address
0h	INTA_REVISION	Revision Register	3080 0000h	3080 1000h
8h	INTA_INTCAP	Interrupt Capabilities	3080 0008h	3080 1008h
10h	INTA_AUXCAP	Auxiliary Capabilities	3080 0010h	3080 1010h

16.1.1 INTA_REVISION Register (Offset = 0h) [reset = X]

INTA_REVISION is shown in [Figure 16-1](#) and described in [Table 16-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 16-3. INTA_REVISION Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG	3080 0000h
NAVSS0_MODSS_INTA1_CFG	3080 1000h

Figure 16-1. INTA_REVISION Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-X															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED															
R-X															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-6696h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM			REVMIN				
R-Ah				R-1h				R-0h			R-0h				

LEGEND: R = Read Only; -n = value after reset

Table 16-4. INTA_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R	X	
31-16	MODID	R	6696h	Module ID field
15-11	REVRTL	R	Ah	RTL Revision. 10h - this SoC
10-8	REVMAJ	R	1h	Major Revision
7-6	CUSTOM	R	0h	Custom
5-0	REVMIN	R	0h	Minor Revision

16.1.2 INTA_INTCAP Register (Offset = 8h) [reset = X]

INTA_INTCAP is shown in [Figure 16-2](#) and described in [Table 16-6](#).

Return to [Summary Table](#).

The IntCap Register contains information on virtual interrupts.

Table 16-5. INTA_INTCAP Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG	3080 0008h
NAVSS0_MODSS_INTA1_CFG	3080 1008h

Figure 16-2. INTA_INTCAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																															
R-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VINTR_CNT																SEVT_CNT															
R-40h																R-400h															

LEGEND: R = Read Only; -n = value after reset

Table 16-6. INTA_INTCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R	X	
31-16	VINTR_CNT	R	40h	Virtual interrupt register/pin count
15-0	SEVT_CNT	R	400h	Number of 'event to virt int' mapping registers

16.1.3 INTA_AUXCAP Register (Offset = 10h) [reset = X]

INTA_AUXCAP is shown in [Figure 16-3](#) and described in [Table 16-8](#).

Return to [Summary Table](#).

The AuxCap Register contains information on additional capabilities.

Table 16-7. INTA_AUXCAP Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG	3080 0010h
NAVSS0_MODSS_INTA1_CFG	3080 1010h

Figure 16-3. INTA_AUXCAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																MEVI_CNT															
R-X																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVI_CNT																GEVI_CNT															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 16-8. INTA_AUXCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RESERVED	R	X	
47-32	MEVI_CNT	R	0h	Number of multicast event registers
31-16	LEVI_CNT	R	0h	Local input events for local to global translation
15-0	GEVI_CNT	R	0h	Number of event counting registers

16.2 MODSS_INTA_CFG_IMAP Registers

Table 16-10 lists the memory-mapped registers for the MODSS_INTA_CFG_IMAP. All register offset addresses not listed in Table 16-10 should be considered as reserved locations and the register contents should not be modified.

The Event to Interrupt Mapping Registers region is accessed by setting the cfg_rsel signal to 1 during the access. The address map for this region is as follows:

Table 16-9. MODSS_INTA_CFG_IMAP Instances

Instance	Base Address
NAVSS0_MODSS_INTA0_CFG_IMAP	3090 0000h
NAVSS0_MODSS_INTA1_CFG_IMAP	3090 8000h

Table 16-10. MODSS_INTA_CFG_IMAP Registers

Offset	Acronym	Register Name	NAVSS0_MODSS_INTA 0_CFG_IMAP Physical Address	NAVSS0_MODSS_INTA 1_CFG_IMAP Physical Address
0h + formula	INTA_IMAP_j	Interrupt Mapping Register	3090 0000h + formula	3090 8000h + formula

16.2.1 INTA_IMAP_j Register (Offset = 0h + formula) [reset = X]

INTA_IMAP_j is shown in [Figure 16-4](#) and described in [Table 16-12](#).

Return to [Summary Table](#).

The Interrupt Mapping Register controls which of N virtual interrupt source outputs this channels physical interrupt sources will map onto.

Offset = 0h + (j * 8h); where j = 0h to 3FFh

Table 16-11. INTA_IMAP_j Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG_IMAP	3090 0000h + formula
NAVSS0_MODSS_INTA1_CFG_IMAP	3090 8000h + formula

Figure 16-4. INTA_IMAP_j Register

63	62	61	60	59	58	57	56
RESERVED							
R/W-X							
55	54	53	52	51	50	49	48
RESERVED							
R/W-X							
47	46	45	44	43	42	41	40
RESERVED							
R/W-X							
39	38	37	36	35	34	33	32
RESERVED							
R/W-X							
31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							REGNUM
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
REGNUM							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		BITNUM					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-12. INTA_IMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-17	RESERVED	R/W	X	
16-8	REGNUM	R/W	0h	Virtual interrupt status register number: this field specifies which of the potential virtual interrupt cause registers the event pending bit will appear in.
7-6	RESERVED	R/W	X	

Table 16-12. INTA_IMAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	BITNUM	R/W	0h	Virtual interrupt cause register bit number: this field specifies which of the 64 bits in the specified virtual interrupt cause register the event pending bit will appear in.

16.3 MODSS_INTA_CFG_INTR Registers

Table 16-14 lists the memory-mapped registers for the MODSS_INTA_CFG_INTR. All register offset addresses not listed in Table 16-14 should be considered as reserved locations and the register contents should not be modified.

The Interrupt Control / Status Registers region is accessed by setting the cfg_rsel signal to 2 during the access. The address map for this region is as follows:

Table 16-13. MODSS_INTA_CFG_INTR Instances

Instance	Base Address
NAVSS0_MODSS_INTA0_CFG_INTR	33C0 0000h
NAVSS0_MODSS_INTA1_CFG_INTR	33C4 0000h

Table 16-14. MODSS_INTA_CFG_INTR Registers

Offset	Acronym	Register Name	NAVSS0_MODSS_INT A0_CFG_INTR Physical Address	NAVSS0_MODSS_INT A1_CFG_INTR Physical Address
0h + formula	INTA_ENABLE_SET_j	Interrupt Enable Set Register	33C0 0000h + formula	33C4 0000h + formula
8h + formula	INTA_ENABLE_CLEAR_j	Interrupt Enable Clear Register	33C0 0008h + formula	33C4 0008h + formula
10h + formula	INTA_STATUS_SET_j	Interrupt Status Set Register	33C0 0010h + formula	33C4 0010h + formula
18h + formula	INTA_STATUS_CLEAR_j	Interrupt Status Clear Register	33C0 0018h + formula	33C4 0018h + formula
20h + formula	INTA_STATUSM_j	Interrupt Masked Status Register	33C0 0020h + formula	33C4 0020h + formula

16.3.1 INTA_ENABLE_SET_j Register (Offset = 0h + formula) [reset = X]

INTA_ENABLE_SET_j is shown in [Figure 16-5](#) and described in [Table 16-16](#).

Return to [Summary Table](#).

The Interrupt Enable Set register is written by software to enable (i.e. unmask) specified bits to allow their current status to be considered in the generation of the corresponding level sensitive virtual interrupt output.

Offset = 0h + (j * 1000h); where j = 0h to 3Fh

Table 16-15. INTA_ENABLE_SET_j Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG_INTR	33C0 0000h + formula
NAVSS0_MODSS_INTA1_CFG_INTR	33C4 0000h + formula

Figure 16-5. INTA_ENABLE_SET_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ENABLE																															
R/W1S-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															
R/W1S-X																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 16-16. INTA_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ENABLE	R/W1S	X	Interrupt enable set value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be set. Reads will reflect back the current status of the internal interrupt enable register.

16.3.2 INTA_ENABLE_CLEAR_j Register (Offset = 8h + formula) [reset = X]

INTA_ENABLE_CLEAR_j is shown in [Figure 16-6](#) and described in [Table 16-18](#).

Return to [Summary Table](#).

The Interrupt Enable Clear register is written by software to disable (i.e. mask) specified bits to disallow their current status from be considered in the generation of the corresponding level sensitive virtual interrupt output.

Offset = 8h + (j * 1000h); where j = 0h to 3Fh

Table 16-17. INTA_ENABLE_CLEAR_j Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG_INTR	33C0 0008h + formula
NAVSS0_MODSS_INTA1_CFG_INTR	33C4 0008h + formula

Figure 16-6. INTA_ENABLE_CLEAR_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ENABLE																															
R/W1C-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															
R/W1C-X																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 16-18. INTA_ENABLE_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ENABLE	R/W1C	X	Interrupt enable clear value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be cleared. Reads will reflect back the current status of the internal interrupt enable register.

16.3.3 INTA_STATUS_SET_j Register (Offset = 10h + formula) [reset = X]

INTA_STATUS_SET_j is shown in [Figure 16-7](#) and described in [Table 16-20](#).

Return to [Summary Table](#).

The Interrupt Status register is read by software to determine the cause of an interrupt.

Offset = 10h + (j * 1000h); where j = 0h to 3Fh

Table 16-19. INTA_STATUS_SET_j Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG_INTR	33C0 0010h + formula
NAVSS0_MODSS_INTA1_CFG_INTR	33C4 0010h + formula

Figure 16-7. INTA_STATUS_SET_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
STATUS																															
R/W1S-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1S-X																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 16-20. INTA_STATUS_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	STATUS	R/W1S	X	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be set

16.3.4 INTA_STATUS_CLEAR_j Register (Offset = 18h + formula) [reset = X]

INTA_STATUS_CLEAR_j is shown in [Figure 16-8](#) and described in [Table 16-22](#).

Return to [Summary Table](#).

The Interrupt Status register is read by software to determine the cause of an interrupt.

Offset = 18h + (j * 1000h); where j = 0h to 3Fh

Table 16-21. INTA_STATUS_CLEAR_j Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG_INTR	33C0 0018h + formula
NAVSS0_MODSS_INTA1_CFG_INTR	33C4 0018h + formula

Figure 16-8. INTA_STATUS_CLEAR_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
STATUS																															
R/W1C-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-X																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 16-22. INTA_STATUS_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	STATUS	R/W1C	X	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be cleared

16.3.5 INTA_STATUSM_j Register (Offset = 20h + formula) [reset = X]

INTA_STATUSM_j is shown in [Figure 16-9](#) and described in [Table 16-24](#).

Return to [Summary Table](#).

The Interrupt Masked Status register can be read by software to determine the cause of an interrupt.

Offset = 20h + (j * 1000h); where j = 0h to 3Fh

Table 16-23. INTA_STATUSM_j Instances

Instance	Physical Address
NAVSS0_MODSS_INTA0_CFG_INTR	33C0 0020h + formula
NAVSS0_MODSS_INTA1_CFG_INTR	33C4 0020h + formula

Figure 16-9. INTA_STATUSM_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
STATUS																															
R-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

LEGEND: R = Read Only; -n = value after reset

Table 16-24. INTA_STATUSM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	STATUS	R	X	Masked state of bits in internal interrupt status register. This value is the result of bitwise ANDing the interrupt enable and status registers

16.4 UDMASS_INTA0_CFG Registers

Table 16-26 lists the memory-mapped registers for the UDMASS_INTA0_CFG. All register offset addresses not listed in Table 16-26 should be considered as reserved locations and the register contents should not be modified.

The Interrupt Aggregator Global Registers region is accessed by setting the cfg_rsel signal to 0 during the access. The address map for this region is as follows:

Table 16-25. UDMASS_INTA0_CFG Instances

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG	3080 2000h
MCU_NAVSS0_UDMASS_INTA0_CFG	283C 0000h

Table 16-26. UDMASS_INTA0_CFG Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_IN TA0_CFG Physical Address	MCU_NAVSS0_UDMA SS_INTA0_CFG Physical Address
0h	UDMA_INTA_REVISION	Revision Register	3080 2000h	283C 0000h
8h	UDMA_INTA_INTCAP	Interrupt Capabilities	3080 2008h	283C 0008h
10h	UDMA_INTA_AUXCAP	Auxiliary Capabilities	3080 2010h	283C 0010h

16.4.1 UDMA_INTA_REVISION Register (Offset = 0h) [reset = X]

UDMA_INTA_REVISION is shown in [Figure 16-10](#) and described in [Table 16-28](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 16-27. UDMA_INTA_REVISION Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG	3080 2000h
MCU_NAVSS0_UDMASS_INTA0_CFG	283C 0000h

Figure 16-10. UDMA_INTA_REVISION Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-X															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED															
R-X															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODID															
R-6696h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL				REVMAJ				CUSTOM				REVMIN			
R-Ah				R-1h				R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 16-28. UDMA_INTA_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R	X	
31-16	MODID	R	6696h	Module ID field
15-11	REVRTL	R	Ah	RTL revision
10-8	REVMAJ	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom revision
5-0	REVMIN	R	0h	Minor revision

16.4.2 UDMA_INTA_INTCAP Register (Offset = 8h) [reset = X]

UDMA_INTA_INTCAP is shown in [Figure 16-11](#) and described in [Table 16-30](#).

Return to [Summary Table](#).

The IntCap Register contains information on virtual interrupts.

Table 16-29. UDMA_INTA_INTCAP Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG	3080 2008h
MCU_NAVSS0_UDMASS_INTA0_CFG	283C 0008h

Figure 16-11. UDMA_INTA_INTCAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																															
R-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VINTR_CNT																SEVT_CNT															
R-100h																R-1200h															

LEGEND: R = Read Only; -n = value after reset

Table 16-30. UDMA_INTA_INTCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R	X	
31-16	VINTR_CNT	R	100h	Virtual interrupt register/pin count
15-0	SEVT_CNT	R	1200h	Number of 'event to virt int' mapping registers. NOTE: This value is 600h for MCU_NAVSS0_UDMASS_INTR_AGGR0

16.4.3 UDMA_INTA_AUXCAP Register (Offset = 10h) [reset = X]

UDMA_INTA_AUXCAP is shown in [Figure 16-12](#) and described in [Table 16-32](#).

Return to [Summary Table](#).

The AuxCap Register contains information on additional capabilities.

Table 16-31. UDMA_INTA_AUXCAP Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG	3080 2010h
MCU_NAVSS0_UDMASS_INTA0_CFG	283C 0010h

Figure 16-12. UDMA_INTA_AUXCAP Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																MEVI_CNT															
R-X																R-200h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEVI_CNT																GEVI_CNT															
R-54h																R-200h															

LEGEND: R = Read Only; -n = value after reset

Table 16-32. UDMA_INTA_AUXCAP Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RESERVED	R	X	
47-32	MEVI_CNT	R	200h	Number of multicast event registers NOTE: This value is 100h for MCU_NAVSS0_UDMASS_INTR_AGGR0
31-16	LEVI_CNT	R	54h	Local input events for local to global translation NOTE: This value is 4h for MCU_NAVSS0_UDMASS_INTR_AGGR0
15-0	GEVI_CNT	R	200h	Number of event counting registers NOTE: This value is 80h for MCU_NAVSS0_UDMASS_INTR_AGGR0

16.5 UDMASS_INTA0_CFG_GCNTCFG Registers

Table 16-34 lists the memory-mapped registers for the UDMASS_INTA0_CFG_GCNTCFG. All register offset addresses not listed in Table 16-34 should be considered as reserved locations and the register contents should not be modified.

The Global Event Count Registers CFG region is accessed by setting the cfg_rsel signal to 4 during the access. The address map for this region is as follows:

**Table 16-33. UDMASS_INTA0_CFG_GCNTCFG
Instances**

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG_GCNTCFG	3104 0000h
MCU_NAVSS0_UDMASS_INTA0_CFG_GCNTCFG	2848 0000h

Table 16-34. UDMASS_INTA0_CFG_GCNTCFG Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_INTA0_CFG_GCNTCFG Physical Address	MCU_NAVSS0_UDMASS_INTA0_CFG_GCNTCFG Physical Address
0h + formula	UDMA_INTA_MAP_j	Global Event Mapping Register	3104 0000h + formula	2848 0000h + formula

16.5.1 UDMA_INTA_MAP_j Register (Offset = 0h + formula) [reset = X]

UDMA_INTA_MAP_j is shown in [Figure 16-13](#) and described in [Table 16-36](#).

Return to [Summary Table](#).

The Global Event Mapping register controls the egress global event index for this event count.

Offset = 0h + (j * 20h); where

j = 0h to 1FFh for NAVSS0_UDMASS_INTA0_CFG_GCNTCFG

j = 0h to FFh for MCU_NAVSS0_UDMASS_INTA0_CFG_GCNTCFG

Table 16-35. UDMA_INTA_MAP_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_GCNTCFG	3104 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_GCNTCFG	2848 0000h + formula

Figure 16-13. UDMA_INTA_MAP_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																															
R/W-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																GEVIDX															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-36. UDMA_INTA_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-16	RESERVED	R/W	X	
15-0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable.

16.6 UDMASS_INTA0_CFG_GCNTRTI Registers

Table 16-38 lists the memory-mapped registers for the UDMASS_INTA0_CFG_GCNTRTI. All register offset addresses not listed in Table 16-38 should be considered as reserved locations and the register contents should not be modified.

The Global Event Count Registers RTI region is accessed by setting the cfg_rsel signal to 6 during the access. The address map for this region is as follows:

**Table 16-37. UDMASS_INTA0_CFG_GCNTRTI
Instances**

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG_GCNT RTI	3380 0000h
MCU_NAVSS0_UDMASS_INTA0_GCNT TRTI	2A60 0000h

Table 16-38. UDMASS_INTA0_CFG_GCNTRTI Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_INT A0_CFG_GCNTRTI Physical Address	MCU_NAVSS0_UDMAS S_INTA0_GCNTRTI Physical Address
0h + formula	UDMA_INTA_COUNT_j	ETL Count Register	3380 0000h + formula	2A60 0000h + formula

16.6.1 UDMA_INTA_COUNT_j Register (Offset = 0h + formula) [reset = X]

UDMA_INTA_COUNT_j is shown in [Figure 16-14](#) and described in [Table 16-40](#).

Return to [Summary Table](#).

The ETL Count register is read by software to determine how many times the event message has been received. This register can be written to decrement the count by a specified amount to acknowledge that a count has been processed by the host.

Offset = 0h + (j * 1000h); where

j = 0h to 1FFh for NAVSS0_UDMASS_INTA0_CFG_GCNTRTI

j = 0h to FFh for MCU_NAVSS0_UDMASS_INTA0_CFG_GCNTRTI

Table 16-39. UDMA_INTA_COUNT_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_GCNTRTI	3380 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_GCNTRTI	2A60 0000h + formula

Figure 16-14. UDMA_INTA_COUNT_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																															
R/W-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-40. UDMA_INTA_COUNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R/W	X	
31-0	CCNT	R/W	0h	Current count. This field is incremented by the event count for each message received with this event on the Counted ETL Interface. On write, this field will be decremented by the value written. Writing a value greater than the current count is illegal.

16.7 UDMASS_INTA0_CFG_IMAP Registers

Table 16-42 lists the memory-mapped registers for the UDMASS_INTA0_CFG_IMAP. All register offset addresses not listed in Table 16-42 should be considered as reserved locations and the register contents should not be modified.

The Event to Interrupt Mapping Registers region is accessed by setting the cfg_rsel signal to 1 during the access. The address map for this region is as follows:

Table 16-41. UDMASS_INTA0_CFG_IMAP Instances

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG_IMAP	3094 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_IMAP	2856 0000h + formula

Table 16-42. UDMASS_INTA0_CFG_IMAP Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_INTA0_CFG_IMAP Physical Address	MCU_NAVSS0_UDMASS_INTA0_CFG_IMAP Physical Address
0h + formula	UDMA_INTA_IMAP_j	Interrupt Mapping Register	3094 0000h + formula	2856 0000h + formula

16.7.1 UDMA_INTA_IMAP_j Register (Offset = 0h + formula) [reset = X]

UDMA_INTA_IMAP_j is shown in [Figure 16-15](#) and described in [Table 16-44](#).

Return to [Summary Table](#).

The Interrupt Mapping Register controls which of N virtual interrupt source outputs this channels physical interrupt sources will map onto.

Offset = 0h + (j * 8h); where

j = 0h to 11FFh for NAVSS0_UDMASS_INTA0_CFG_IMAP

j = 0h to 5FFh for MCU_NAVSS0_UDMASS_INTA0_CFG_IMAP

Table 16-43. UDMA_INTA_IMAP_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_IMAP	3094 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_IMAP	2856 0000h + formula

Figure 16-15. UDMA_INTA_IMAP_j Register

63	62	61	60	59	58	57	56
RESERVED							
R/W-X							
55	54	53	52	51	50	49	48
RESERVED							
R/W-X							
47	46	45	44	43	42	41	40
RESERVED							
R/W-X							
39	38	37	36	35	34	33	32
RESERVED							
R/W-X							
31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							REGNUM
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
REGNUM							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		BITNUM					
R/W-X		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-44. UDMA_INTA_IMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-17	RESERVED	R/W	X	

Table 16-44. UDMA_INTA_IMAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-8	REGNUM	R/W	0h	Virtual interrupt status register number: this field specifies which of the potential virtual interrupt cause registers the event pending bit will appear in.
7-6	RESERVED	R/W	X	
5-0	BITNUM	R/W	0h	Virtual interrupt cause register bit number: this field specifies which of the 64 bits in the specified virtual interrupt cause register the event pending bit will appear in.

16.8 UDMASS_INTA0_CFG_INTR Registers

Table 16-46 lists the memory-mapped registers for the UDMASS_INTA0_CFG_INTR. All register offset addresses not listed in Table 16-46 should be considered as reserved locations and the register contents should not be modified.

The Interrupt Control / Status Registers region is accessed by setting the `cfg_rsel` signal to 2 during the access. The address map for this region is as follows:

Table 16-45. UDMASS_INTA0_CFG_INTR Instances

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG_INTR	33D0 0000h
MCU_NAVSS0_UDMASS_INTA0_CFG_INTR	2A70 0000h

Table 16-46. UDMASS_INTA0_CFG_INTR Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_INTA0_CFG_INTR Physical Address	MCU_NAVSS0_UDMASS_INTA0_CFG_INTR Physical Address
0h + formula	UDMA_INTA_ENABLE_SET_j	Interrupt Enable Set Register	33D0 0000h + formula	2A70 0000h + formula
8h + formula	UDMA_INTA_ENABLE_CLEAR_j	Interrupt Enable Clear Register	33D0 0008h + formula	2A70 0008h + formula
10h + formula	UDMA_INTA_STATUS_SET_j	Interrupt Status Set Register	33D0 0010h + formula	2A70 0010h + formula
18h + formula	UDMA_INTA_STATUS_CLEAR_j	Interrupt Status Clear Register	33D0 0018h + formula	2A70 0018h + formula
20h + formula	UDMA_INTA_STATUSM_j	Interrupt Masked Status Register	33D0 0020h + formula	2A70 0020h + formula

16.8.1 UDMA_INTA_ENABLE_SET_j Register (Offset = 0h + formula) [reset = X]

UDMA_INTA_ENABLE_SET_j is shown in [Figure 16-16](#) and described in [Table 16-48](#).

Return to [Summary Table](#).

The Interrupt Enable Set register is written by software to enable (i.e. unmask) specified bits to allow their current status to be considered in the generation of the corresponding level sensitive virtual interrupt output.

Offset = 0h + (j * 1000h); where j = 0h to FFh

Table 16-47. UDMA_INTA_ENABLE_SET_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_INTR	33D0 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_INTR	2A70 0000h + formula

Figure 16-16. UDMA_INTA_ENABLE_SET_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ENABLE																															
R/W1S-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															
R/W1S-X																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 16-48. UDMA_INTA_ENABLE_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ENABLE	R/W1S	X	Interrupt enable set value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be set. Reads will reflect back the current status of the internal interrupt enable register.

16.8.2 UDMA_INTA_ENABLE_CLEAR_j Register (Offset = 8h + formula) [reset = X]

UDMA_INTA_ENABLE_CLEAR_j is shown in [Figure 16-17](#) and described in [Table 16-50](#).

Return to [Summary Table](#).

The Interrupt Enable Clear register is written by software to disable (i.e. mask) specified bits to disallow their current status from be considered in the generation of the corresponding level sensitive virtual interrupt output.

Offset = 8h + (j * 1000h); where j = 0h to FFh

**Table 16-49. UDMA_INTA_ENABLE_CLEAR_j
Instances**

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_INTR	33D0 0008h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_INTR	2A70 0008h + formula

Figure 16-17. UDMA_INTA_ENABLE_CLEAR_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ENABLE																															
R/W1C-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENABLE																															
R/W1C-X																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 16-50. UDMA_INTA_ENABLE_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	ENABLE	R/W1C	X	Interrupt enable clear value. On writes, set bits will cause corresponding bits in the internal interrupt enable register to be cleared. Reads will reflect back the current status of the internal interrupt enable register.

16.8.3 UDMA_INTA_STATUS_SET_j Register (Offset = 10h + formula) [reset = X]

UDMA_INTA_STATUS_SET_j is shown in [Figure 16-18](#) and described in [Table 16-52](#).

Return to [Summary Table](#).

The Interrupt Status register is read by software to determine the cause of an interrupt.

Offset = 10h + (j * 1000h); where j = 0h to FFh

Table 16-51. UDMA_INTA_STATUS_SET_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_INTR	33D0 0010h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_INTR	2A70 0010h + formula

Figure 16-18. UDMA_INTA_STATUS_SET_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
STATUS																															
R/W1S-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1S-X																															

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 16-52. UDMA_INTA_STATUS_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	STATUS	R/W1S	X	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be set

16.8.4 UDMA_INTA_STATUS_CLEAR_j Register (Offset = 18h + formula) [reset = X]

UDMA_INTA_STATUS_CLEAR_j is shown in [Figure 16-19](#) and described in [Table 16-54](#).

Return to [Summary Table](#).

The Interrupt Status register is read by software to determine the cause of an interrupt.

Offset = 18h + (j * 1000h); where j = 0h to FFh

**Table 16-53. UDMA_INTA_STATUS_CLEAR_j
Instances**

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_INTR	33D0 0018h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_INTR	2A70 0018h + formula

Figure 16-19. UDMA_INTA_STATUS_CLEAR_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
STATUS																															
R/W1C-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-X																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 16-54. UDMA_INTA_STATUS_CLEAR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	STATUS	R/W1C	X	Raw state (not enabled/masked) of bits in internal interrupt status register. Writing a 1 to any bit of this register will cause the corresponding raw status bit to be cleared

16.8.5 UDMA_INTA_STATUSM_j Register (Offset = 20h + formula) [reset = X]

UDMA_INTA_STATUSM_j is shown in [Figure 16-20](#) and described in [Table 16-56](#).

Return to [Summary Table](#).

The Interrupt Masked Status register can be read by software to determine the cause of an interrupt.

Offset = 20h + (j * 1000h); where j = 0h to FFh

Table 16-55. UDMA_INTA_STATUSM_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_INTR	33D0 0020h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_INTR	2A70 0020h + formula

Figure 16-20. UDMA_INTA_STATUSM_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
STATUS																															
R-X																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

LEGEND: R = Read Only; -n = value after reset

Table 16-56. UDMA_INTA_STATUSM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	STATUS	R	X	Masked state of bits in internal interrupt status register. This value is the result of bitwise ANDing the interrupt enable and status registers

16.9 UDMASS_INTA0_CFG_L2G Registers

Table 16-58 lists the memory-mapped registers for the UDMASS_INTA0_CFG_L2G. All register offset addresses not listed in Table 16-58 should be considered as reserved locations and the register contents should not be modified.

The 'Local to Global' Registers region is accessed by setting the cfg_rsel signal to 3 during the access. The address map for this region is as follows:

Table 16-57. UDMASS_INTA0_CFG_L2G Instances

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG_L2G	3110 0000h
MCU_NAVSS0_UDMASS_INTA0_CFG_L2G	2857 0000h

Table 16-58. UDMASS_INTA0_CFG_L2G Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_INTA0_CFG_L2G Physical Address	MCU_NAVSS0_UDMASS_INTA0_CFG_L2G Physical Address
0h + formula	UDMA_INTA_MAP_j	Local to global event mapping	3110 0000h + formula	28570000h + formula

16.9.1 UDMA_INTA_MAP_j Register (Offset = 0h + formula) [reset = X]

UDMA_INTA_MAP_j is shown in [Figure 16-21](#) and described in [Table 16-60](#).

Return to [Summary Table](#).

This register determines how the ordinal local event is translated to a global event on the outgoing event transport lane. Both pulse and rising edge local event types are supported. With pulsed events, the event count is determined by the number of cycles for which the event signal remains high. For rising edge events, the count represents the total number of rising edge transitions. The index field of the register determines the outgoing global event index, and the mode bit specifies either pulsed or rising edge local event detection.

Offset = 0h + (j * 20h); where j = 0h to 53h

Table 16-59. UDMA_INTA_MAP_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_L2G	3110 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_L2G	2857 0000h + formula

Figure 16-21. UDMA_INTA_MAP_j Register

63	62	61	60	59	58	57	56
RESERVED							
R/W-X							
55	54	53	52	51	50	49	48
RESERVED							
R/W-X							
47	46	45	44	43	42	41	40
RESERVED							
R/W-X							
39	38	37	36	35	34	33	32
RESERVED							
R/W-X							
31	30	29	28	27	26	25	24
MODE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
GEVIDX							
R/W-FFFFh							
7	6	5	4	3	2	1	0
GEVIDX							
R/W-FFFFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-60. UDMA_INTA_MAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	R/W	X	

Table 16-60. UDMA_INTA_MAP_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31	MODE	R/W	0h	Local event detection mode. This field is set to 0 for pulsed events, and to 1 for rising edge eventss
30-16	RESERVED	R/W	X	
15-0	GEVIDX	R/W	FFFFh	Global event index. This field specifies the index of the outgoing global event. Set to 0xFFFF to disable.

16.10 UDMASS_INTA0_CFG_MCAST Registers

Table 16-62 lists the memory-mapped registers for the UDMASS_INTA0_CFG_MCAST. All register offset addresses not listed in Table 16-62 should be considered as reserved locations and the register contents should not be modified.

The Global Event Multicast Registers region is accessed by setting the cfg_rsel signal to 5 during the access. The address map for this region is as follows:

**Table 16-61. UDMASS_INTA0_CFG_MCAST
Instances**

Instance	Base Address
NAVSS0_UDMASS_INTA0_CFG_MCAS T	3111 0000h
MCU_NAVSS0_UDMASS_INTA0_CFG_ MCAST	2858 0000h

Table 16-62. UDMASS_INTA0_CFG_MCAST Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_IN TA0_CFG_MCAST Physical Address	MCU_NAVSS0_UDMA SS_INTA0_CFG_MCA ST Physical Address
0h + formula	UDMA_INTA_MCMAP_j	Multicast event mapping	3111 0000h + formula	2858 0000h + formula

16.10.1 UDMA_INTA_MCMAP_j Register (Offset = 0h + formula) [reset = X]

UDMA_INTA_MCMAP_j is shown in [Figure 16-22](#) and described in [Table 16-64](#).

Return to [Summary Table](#).

This register determines how ingress global events from the ingress global event ETL are written out to the two egress global event ETL interfaces. The index of each of the two egress events is stored in this register, which is selected based in the ingress event index value.

Offset = 0h + (j * 20h); where

j = 0h to 1FFh for NAVSS0_UDMASS_INTA0_CFG_MCAST

j = 0h to 7Fh for MCU_NAVSS0_UDMASS_INTA0_CFG_MCAST

Table 16-63. UDMA_INTA_MCMAP_j Instances

Instance	Physical Address
NAVSS0_UDMASS_INTA0_CFG_MCAST	3111 0000h + formula
MCU_NAVSS0_UDMASS_INTA0_CFG_MCAST	2858 0000h + formula

Figure 16-22. UDMA_INTA_MCMAP_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED																GEVIDX1															
R/W-X																R/W-FFFFh															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																GEVIDX0															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-64. UDMA_INTA_MCMAP_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RESERVED	R/W	X	
47-32	GEVIDX1	R/W	FFFFh	Global event index 1. This field specifies the index of the outgoing global event on ETL 1. Set to 0xFFFF to disable.
31-16	RESERVED	R/W	X	
15-0	GEVIDX0	R/W	FFFFh	Global event index 0. This field specifies the index of the outgoing global event on ETL 0. Set to 0xFFFF to disable.

17 PSI-L Configuration Registers

Table 17-2 lists the PSI-L configuration registers (PSIL_CFG). They are not memory mapped and are accessed indirectly via CFG_PROXY modules in NAVSS0 and MCU_NAVSS0.

Table 17-1. PSIL_CFG Instances

Instance	Base Address
PSIL_CFG	N/A

Table 17-2. PSIL_CFG Registers

Offset	Acronym	Register Name	PSIL_CFG Physical Address
0h	PSIL_PEER_THREAD_ID_REG	Peer Thread ID Register	N/A
1h	PSIL_PEER_CREDIT_REG	Peer Credit Register	N/A
2h	PSIL_ENABLE_REG	Enable Register	N/A
40h	PSIL_LOCAL_CAPABILITIES_REG	Local Capabilities Register	N/A
400h to 407h	Real Time Registers	Real Time Registers (varies by module)	N/A
408h	PSIL_REAL_TIME_ENABLE_REG	Real Time Enable Register	N/A
409h to 40Fh	Real Time Registers	Real Time Registers (varies by module)	N/A

17.1 PSIL_PEER_THREAD_ID_REG Register (Offset = 0h) [reset = 0h]

PSIL_PEER_THREAD_ID_REG is shown in [Figure 17-1](#) and described in [Table 17-4](#).

Return to [Summary Table](#).

The Peer Thread ID register contains the thread ID of the thread destination which is used for routing the messages. This register is only implemented for source threads.

Table 17-3. PSIL_PEER_THREAD_ID_REG Instances

Instance	Physical Address
PSIL_CFG	N/A

Figure 17-1. PSIL_PEER_THREAD_ID_REG Register

31	30	29	28	27	26	25	24
THREAD_PRIORITY				PEER_THREAD_WIDTH			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PEER_THREAD_ID							
R/W-0h							
7	6	5	4	3	2	1	0
PEER_THREAD_ID							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-4. PSIL_PEER_THREAD_ID_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	THREAD_PRIORITY	R/W	0h	Priority level to use for this source thread in arbitration
28-24	PEER_THREAD_WIDTH	R	0h	Datapath width of paired peer destination thread. 0h - 32-bit 1h - 64-bit 2h - 128-bit 3h - 256-bit 4h - 512-bit
23-16	RESERVED	R/W	0h	Reserved
15-0	PEER_THREAD_ID	R/W	0h	Thread ID to which all nontransfer response, nonconfiguration messages from this thread are sent

17.2 PSIL_PEER_CREDIT_REG Register (Offset = 1h) [reset = 0h]

PSIL_PEER_CREDIT_REG is shown in [Figure 17-2](#) and described in [Table 17-6](#).

Return to [Summary Table](#).

This register contains a free credit count in completed destination data phases for the thread destination. This register is only implemented for source threads.

Table 17-5. PSIL_PEER_CREDIT_REG Instances

Instance	Physical Address
PSIL_CFG	N/A

Figure 17-2. PSIL_PEER_CREDIT_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CREDIT_CNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-6. PSIL_PEER_CREDIT_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	CREDIT_CNT	R/W	0h	Free entries in destination thread. This field is encoded as follows: 0h to 80h - Actual count in data phases 81h to FFh - Reserved

17.3 PSIL_ENABLE_REG Register (Offset = 2h) [reset = 0h]

PSIL_ENABLE_REG is shown in [Figure 17-3](#) and described in [Table 17-8](#).

Return to [Summary Table](#).

This register contains enable control for the thread.

Table 17-7. PSIL_ENABLE_REG Instances

Instance	Physical Address
PSIL_CFG	N/A

Figure 17-3. PSIL_ENABLE_REG Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-8. PSIL_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	Thread enable 0 = thread is disabled and should not perform data transfers. Any input data is discarded. 1 = thread is enabled and may perform data transfers Note: A 1 to 0 transition on this bit may completely reset the channel. Regardless, a channel that is manually disabled via this bit should be assumed to require a full reconfiguration.
30-0	RESERVED	R	0h	Reserved

17.4 PSIL_LOCAL_CAPABILITIES_REG Register (Offset = 40h) [reset = Xh]

PSIL_LOCAL_CAPABILITIES_REG is shown in [Figure 17-4](#) and described in [Table 17-10](#).

Return to [Summary Table](#).

The Local Capabilities Register provides the width and count of the credits for which buffering is available in the local thread. This register can be read by the system configuration software to determine what values to place in the PSIL_PEER_CREDIT_REG and PSIL_PEER_THREAD_ID_REG registers of the paired thread.

**Table 17-9. PSIL_LOCAL_CAPABILITIES_REG
Instances**

Instance	Physical Address
PSIL_CFG	N/A

Figure 17-4. PSIL_LOCAL_CAPABILITIES_REG Register

31	30	29	28	27	26	25	24
RESERVED				LOCAL_THREAD_WIDTH			
R-0h				R-Xh			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
LOCAL_CREDIT_CNT							
R-Xh							

LEGEND: R = Read Only; -n = value after reset

Table 17-10. PSIL_LOCAL_CAPABILITIES_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	LOCAL_THREAD_WIDTH	R	-h	Width for the local thread used for pairing purposes. 0h = 4 bytes 1h = 8 bytes 2h = 16 bytes 3h = 32 bytes 4h = 64 bytes 5h = 128 bytes 6h to 1Fh = Reserved
23-8	RESERVED	R	0h	Reserved
7-0	LOCAL_CREDIT_CNT	R	-h	Read only local thread free entry count used for pairing purposes. This field is encoded as follows: 0h to 80h - Available count in elements 81h to FFh - Reserved

17.5 PSIL_REAL_TIME_ENABLE_REG Register (Offset = 408h) [reset = 0h]

PSIL_REAL_TIME_ENABLE_REG is shown in [Figure 17-5](#) and described in [Table 17-12](#).

Return to [Summary Table](#).

Real Time Enable Register

Table 17-11. PSIL_REAL_TIME_ENABLE_REG Instances

Instance	Physical Address
PSIL_CFG	N/A

Figure 17-5. PSIL_REAL_TIME_ENABLE_REG Register

31	30	29	28	27	26	25	24
ENABLE	TDOWN	PAUSE	FLUSH	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE	RESERVED
R-0h						R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 17-12. PSIL_REAL_TIME_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	<p>Destination threads:</p> <p>When set, the thread is enabled and normal data transfers can occur. When cleared, the thread is disabled. When disabled, a thread is expected to discard all held data and new incoming data, clear any internal state (FIFO pointers/occupancies, DMA event counts) back to a reset condition. When disabled, a thread is required to respond to PSI-L transactions so that credit handshake is not disrupted even though data is discarded. A 'hard teardown' can be performed by directly clearing this bit.</p> <p>Source threads:</p> <p>When set, the thread is enabled and the source thread can initiate transfers. When cleared, the thread is disabled. When disabled, the thread is required to continue to track outstanding transactions so that the credit handshake is not disrupted. If the teardown bit is set, this bit is cleared automatically after the current packet is closed. Directly clearing this bit does not close out the current open packet. Thus the teardown bit should always be used to disable a source thread instead of manually clearing this bit. This bit should be manually cleared only if the source thread is to be reset before being re-enabled.</p>

Table 17-12. PSIL_REAL_TIME_ENABLE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
30	TDOWN	R/W	0h	<p>Destination threads:</p> <p>When set, the thread commences a teardown procedure. To perform a destination teardown, the teardown condition should be set in the source thread and it automatically propagates to this register bit with the normal flow of peripheral data via the TDOWN bit (this bit should not be set directly). Once the thread is fully stopped and ready to be reused (including returning all credits), the ENABLE bit is cleared.</p> <p>Source threads:</p> <p>When set, the thread commences a teardown procedure. It stops transferring data on a boundary which is appropriate for the type of attached peripheral and clear and mask any peripheral specific functionality (for example, DMA event counters). Note that a protocol conversion gasket may have limited visibility into the state of the peripheral and thus may complete teardown at seemingly arbitrary point in the data stream. After stopping data transfer, the source thread sends a 'NULL data' teardown message to the destination thread that also closes the current packet with an EOP. If no packet is open at the time of the teardown, the message also includes SOP (constitutes a new packet). Once the thread teardown is complete and ready to be reused, the ENABLE bit is cleared.</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: Before attempting to stop the clock of PSI-L associated module, software is required to teardown all active channels either via the UDMA_TRT_CTL_j[30] TDOWN bit or via the PSIL_REAL_TIME_ENABLE_REG[30] TDOWN bit. After completion software is also required to clear the PSIL_ENABLE_REG[31] ENABLE bit in both the PSI-L based peripherals and UDMA-P. Attempting to stop the clock without first performing the channel teardown or clearing the PSIL_ENABLE_REG[31] ENABLE bit may lead to undefined module behavior.</p> <hr/>
29	PAUSE	R/W	0h	<p>Destination threads:</p> <p>When set, the thread is in a paused state. It stops transferring data on a boundary which is appropriate for the type of attached peripheral. While paused, data transfers no longer occur but other application specific actions may still occur (for example, DMA event increments). The pause bit can be cleared and data transfers will resume.</p> <p>Source threads:</p> <p>When set, the thread is in a paused state. It stops transferring data on a boundary which is appropriate for the type of attached peripheral. While paused, data transfers no longer occur but other application specific actions may still occur (for example, DMA event increments). The pause bit can be cleared and data transfers will resume. PAUSE does not stop teardown from completing.</p>

Table 17-12. PSIL_REAL_TIME_ENABLE_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FLUSH	R/W	0h	Destination threads: When set, causes all destination thread data to be discarded instead of being written to the peripheral. This bit should be set only when a thread fails to complete its teardown procedure normally, because a peripheral is no longer functioning or because some other factor is causing a deadlock beyond the PSI-L interface. Source threads: Not used
27-2	RESERVED	R	0h	Reserved
1	IDLE	R	0h	Destination threads: This is a read-only bit that signifies that the disabled thread is also idle. This bit is read only and can only become set if the ENABLE bit is cleared. Source threads: This is a read-only bit that signifies that the Paused or Disabled channel is also idle. This bit is read only and can only become set if PAUSE is set or ENABLE is cleared.
0	RESERVED	R	0h	Reserved

18 PSI-L CFG_PROXY Registers

Table 18-2 lists the memory-mapped registers for the PSI-L CFG_PROXY modules which are used to read and write the PSI-L configuration registers described in Section 17. All register offset addresses not listed in Table 18-2 should be considered as reserved locations and the register contents should not be modified.

Table 18-1. PSI-L CFG_PROXY Instances

Instance	Base Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78000h
MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY	2A268000h

Table 18-2. PSI-L CFG_PROXY Registers

Offset	Acronym	Register Name	NAVSS0_UDMASS_PSILCFG0_CFG_PROXY Physical Address	MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY Physical Address
0h	PSIL_CFG_PROXY_REVISION	Revision Register	31F78000h	2A268000h
10h	PSIL_CFG_PROXY_TO	PSI-L Proxy Timeout Register	31F78010h	2A268010h
100h	PSIL_CFG_PROXY_CMDA	PSI-L Configuration Proxy Command Register A	31F78100h	2A268100h
104h	PSIL_CFG_PROXY_CMDB	PSI-L Configuration Proxy Command Register B	31F78104h	2A268104h
108h	PSIL_CFG_PROXY_WDATA	PSI-L Configuration Proxy Write Data Register	31F78108h	2A268108h
140h	PSIL_CFG_PROXY_RDATA	PSI-L Configuration Proxy Read Data Register	31F78140h	2A268140h

18.1 PSIL_CFG_PROXY_REVISION Register (Offset = 0h) [reset = 66C00100h]

PSIL_CFG_PROXY_REVISION is shown in [Figure 18-1](#) and described in [Table 18-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 18-3. PSIL_CFG_PROXY_REVISION Instances

Instance	Physical Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78000h
MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY	2A268000h

Figure 18-1. PSIL_CFG_PROXY_REVISION Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C00100h																															

LEGEND: R = Read Only; -n = value after reset

Table 18-4. PSIL_CFG_PROXY_REVISION Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C00100h	TI internal data.

18.2 PSIL_CFG_PROXY_TO Register (Offset = 10h) [reset = X]

PSIL_CFG_PROXY_TO is shown in [Figure 18-2](#) and described in [Table 18-6](#).

Return to [Summary Table](#).

The PSI-L proxy timeout register controls the timeout watchdog and reports timeout occurrences on PSI-L configuration transactions issued by the built in PSI-L proxy.

Table 18-5. PSIL_CFG_PROXY_TO Instances

Instance	Physical Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78010h
MCU_NAVSS0_UDMASS_PSILSS_CFG_PROXY	2A268010h

Figure 18-2. PSIL_CFG_PROXY_TO Register

31	30	29	28	27	26	25	24
TOUT	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
TOUT_CNT							
R/W-400h							
7	6	5	4	3	2	1	0
TOUT_CNT							
R/W-400h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-6. PSIL_CFG_PROXY_TO Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TOUT	R/W	0h	Timeout occurred. When set indicates that a timeout has occurred on a configuration access. Once set, this bit is persistent until manually cleared.
30-16	RESERVED	R/W	X	
15-0	TOUT_CNT	R/W	400h	Timeout period. Specifies how many cycles to wait before closing up a configuration read or write transaction and asserting the TOUT bit

18.3 PSIL_CFG_PROXY_CMDA Register (Offset = 100h) [reset = X]

PSIL_CFG_PROXY_CMDA is shown in [Figure 18-3](#) and described in [Table 18-8](#).

Return to [Summary Table](#).

The Command Register A contains the busy indicator, direction, and thread number for the configuration transaction.

Table 18-7. PSIL_CFG_PROXY_CMDA Instances

Instance	Physical Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78100h
MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY	2A268100h

Figure 18-3. PSIL_CFG_PROXY_CMDA Register

31	30	29	28	27	26	25	24
BUSY	DIR	TO	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-X				
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
THREAD_ID							
R/W-0h							
7	6	5	4	3	2	1	0
THREAD_ID							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-8. PSIL_CFG_PROXY_CMDA Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BUSY	R/W	0h	Indication that a configuration read or write is in progress 0h = No transaction is in progress 1h = Transaction is in progress
30	DIR	R/W	0h	Direction of configuration transaction 0h = Write transaction 1h = Read transaction
29	TO	R/W	0h	Indication that a timeout occurred. This bit should be written to 0h on each new transaction. 0h = Transaction completed normally 1h = Timeout occurred
28-16	RESERVED	R/W	X	
15-0	THREAD_ID	R/W	0h	Thread ID to which configuration read or write is being sent. The thread ID mapping is shown in <i>PSI-L System Thread Map (All NAVSS) of Navigator Subsystem (NAVSS)</i> .

18.4 PSIL_CFG_PROXY_CMDB Register (Offset = 104h) [reset = X]

PSIL_CFG_PROXY_CMDB is shown in [Figure 18-4](#) and described in [Table 18-10](#).

Return to [Summary Table](#).

The Command Register B contains the byte enables and word address for the configuration transaction.

Table 18-9. PSIL_CFG_PROXY_CMDB Instances

Instance	Physical Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78104h
MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY	2A268104h

Figure 18-4. PSIL_CFG_PROXY_CMDB Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BYTEN				RESERVED											
R/W-0h								R/W-X							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS															
R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-10. PSIL_CFG_PROXY_CMDB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	BYTEN	R/W	0h	Byte enables to use for configuration read or write
27-16	RESERVED	R/W	X	
15-0	ADDRESS	R/W	0h	Word (32-bit) address within thread configuration space for transaction 0h = Peer thread ID register (PSIL_PEER_THREAD_ID_REG). Implemented for source threads only. 1h = Peer credit register (PSIL_PEER_CREDIT_REG). Implemented for source threads only. 2h = Enable register (PSIL_ENABLE_REG) 40h = Capabilities register (PSIL_LOCAL_CAPABILITIES_REG) 400h = Static TR register

18.5 PSIL_CFG_PROXY_WDATA Register (Offset = 108h) [reset = 0h]

PSIL_CFG_PROXY_WDATA is shown in [Figure 18-5](#) and described in [Table 18-12](#).

Return to [Summary Table](#).

The Write Data Register contains the data which is to be written during the configuration transaction.

Table 18-11. PSIL_CFG_PROXY_WDATA Instances

Instance	Physical Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78108h
MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY	2A268108h

Figure 18-5. PSIL_CFG_PROXY_WDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-12. PSIL_CFG_PROXY_WDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	WDATA	R/W	0h	Configuration data word to be written

18.6 PSIL_CFG_PROXY_RDATA Register (Offset = 140h) [reset = 0h]

PSIL_CFG_PROXY_RDATA is shown in [Figure 18-6](#) and described in [Table 18-14](#).

Return to [Summary Table](#).

The Read Data Register contains the data which was read back during the configuration transaction.

Table 18-13. PSIL_CFG_PROXY_RDATA Instances

Instance	Physical Address
NAVSS0_UDMASS_PSILCFG0_CFG_PROXY	31F78140h
MCU_NAVSS0_UDMASS_PSILSS_CFG0_PROXY	2A268140h

Figure 18-6. PSIL_CFG_PROXY_RDATA Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-14. PSIL_CFG_PROXY_RDATA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RDATA	R/W	0h	Configuration data word that was read

19 PSILSS0_CFG_MMRS Registers

Table 19-2 lists the memory-mapped registers for the PSILSS0_CFG_MMRS. All register offset addresses not listed in Table 19-2 should be considered as reserved locations and the register contents should not be modified.

Table 19-1. PSILSS0_CFG_MMRS Instances

Instance	Base Address
	31170000h
	285E0000h

Table 19-2. PSILSS0_CFG_MMRS Registers

Offset	Acronym	Register Name	Physical Address	Physical Address	Section
0h	PSIL_CFG_PID	Revision Register	31170000h	285E0000h	Section 19.1
4h	PSIL_CFG_CONFIG	Config Register	31170004h	285E0004h	Section 19.2
10h	PSIL_CFG_EVENT	Event Register	31170010h	285E0010h	Section 19.3
20h	PSIL_CFG_LINK	Link Register	31170020h	285E0020h	Section 19.4
40h	PSIL_CFG_DOWN	Link Down Register	31170040h	285E0040h	Section 19.5

19.1 PSIL_CFG_PID Register (Offset = 0h) [reset = 66C44100h]

PSIL_CFG_PID is shown in [Figure 19-1](#) and described in [Table 19-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 19-3. PSIL_CFG_PID Instances

Instance	Base Address
	31170000h
	285E0000h

Figure 19-1. PSIL_CFG_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C44100h																															

LEGEND: R = Read Only; -n = value after reset

Table 19-4. PSIL_CFG_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C44100h	TI internal data.

19.2 PSIL_CFG_CONFIG Register (Offset = 4h) [reset = X]

PSIL_CFG_CONFIG is shown in [Figure 19-2](#) and described in [Table 19-6](#).

Return to [Summary Table](#).

The Config Register shows configured params.

Table 19-5. PSIL_CFG_CONFIG Instances

Instance	Base Address
	31170004h
	285E0004h

Figure 19-2. PSIL_CFG_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENDPOINTS															
R-X																R-1Ch															

LEGEND: R = Read Only; -n = value after reset

Table 19-6. PSIL_CFG_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ENDPOINTS	R	1Ch	Number of endpoints supported.

19.3 PSIL_CFG_EVENT Register (Offset = 10h) [reset = X]

PSIL_CFG_EVENT is shown in [Figure 19-3](#) and described in [Table 19-8](#).

Return to [Summary Table](#).

The Event Register defines the event to produce for a link down event.

Table 19-7. PSIL_CFG_EVENT Instances

Instance	Base Address
	31170010h
	285E0010h

Figure 19-3. PSIL_CFG_EVENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-8. PSIL_CFG_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	EVT	R/W	FFFFh	The event to produce.

19.4 PSIL_CFG_LINK Register (Offset = 20h) [reset = X]

PSIL_CFG_LINK is shown in [Figure 19-4](#) and described in [Table 19-10](#).

Return to [Summary Table](#).

The Link Register shows the current status of the endpoint links.

Table 19-9. PSIL_CFG_LINK Instances

Instance	Base Address
	31170020h
	285E0020h

Figure 19-4. PSIL_CFG_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

LEGEND: R = Read Only; -n = value after reset

Table 19-10. PSIL_CFG_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R	X	The status of the endpoint links.

19.5 PSIL_CFG_DOWN Register (Offset = 40h) [reset = 0h]

PSIL_CFG_DOWN is shown in [Figure 19-5](#) and described in [Table 19-12](#).

Return to [Summary Table](#).

The Link Down Register shows which links are down for the endpoints.

Table 19-11. PSIL_CFG_DOWN Instances

Instance	Base Address
	31170040h
	285E0040h

Figure 19-5. PSIL_CFG_DOWN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-0h																															

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-12. PSIL_CFG_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R/W1C	0h	The down status of the endpoint links.

20 PSILSS Registers

[Table 20-1](#) lists the PSILSS memory regions.

Table 20-1. PSILSS Memory Regions

Memory Region	Base Address
USART_PSILSS16_MMRS	0340 0000h
MISC_PSILSS12_MMRS	0340 4000h
DEBUG_PSILSS4_MMRS	0340 8000h
AASRC_PSILSS1_MMRS	0340 C000h
CSI_PSILSS0_MMRS	0341 0000h

20.1 CSI_PSILSS0 Registers

[Table 20-2](#) lists the CSI_PSILSS0 registers. All register offset addresses not listed in [Table 20-2](#) should be considered as reserved locations and the register contents should not be modified.

Table 20-2. CSI_PSILSS0 Registers

Offset	Acronym	Register Name	CSI_PSILSS0_MMRS Physical Address
0h	CSI_PSILSS0_PID	Revision Register	0341 0000h
4h	CSI_PSILSS0_CONFIG	Config Register	0341 0004h
10h	CSI_PSILSS0_EVENT	Event Register	0341 0010h
20h	CSI_PSILSS0_LINK	Link Register	0341 0020h
40h	CSI_PSILSS0_DOWN	Link Down Register	0341 0040h

20.1.1 CSI_PSILSS0_PID Register (Offset = 0h) [reset = 66C47100h]

CSI_PSILSS0_PID is shown in [Figure 20-1](#) and described in [Table 20-3](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Figure 20-1. CSI_PSILSS0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C47100h																															

Table 20-3. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C47100h	TI internal data. Identifies revision of peripheral.

20.1.2 CSI_PSILSS0_CONFIG Register (Offset = 4h) [reset = 4h]

CSI_PSILSS0_CONFIG is shown in [Figure 20-2](#) and described in [Table 20-4](#).

Return to the [Summary Table](#).

The Config Register shows configured parameters.

Figure 20-2. CSI_PSILSS0_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENDPOINTS															
R-0h																R-4h															

Table 20-4. CSI_PSILSS0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ENDPOINTS	R	4h	Number of endpoints supported

20.1.3 CSI_PSILSS0_EVENT Register (Offset = 10h) [reset = FFFFh]

CSI_PSILSS0_EVENT is shown in [Figure 20-3](#) and described in [Table 20-5](#).

Return to the [Summary Table](#).

The Event Register defines the event to produce for a link down event.

Figure 20-3. CSI_PSILSS0_EVENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT															
R-0h																R/W-FFFFh															

Table 20-5. CSI_PSILSS0_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	EVT	R/W	FFFFh	The event to produce

20.1.4 CSI_PSILSS0_LINK Register (Offset = 20h) [reset = X]

CSI_PSILSS0_LINK is shown in [Figure 20-4](#) and described in [Table 20-6](#).

Return to the [Summary Table](#).

The Link Register shows the current status of the endpoint links.

Figure 20-4. CSI_PSILSS0_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

Table 20-6. CSI_PSILSS0_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R	X	<p>The status of the endpoint links</p> <p>Bit [0]: CSI_STRM</p> <p>Bit [1]: TX0_STRM</p> <p>Bit [2]: RX0_STRM</p> <p>Bit [3]: RX1_STRM</p>

20.1.5 CSI_PSILSS0_DOWN Register (Offset = 40h) [reset = 0h]

CSI_PSILSS0_DOWN is shown in and described in .

Return to the [Summary Table](#).

The Link Down Register shows which links are down for the endpoints.

Figure 20-5. CSI_PSILSS0_DOWN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-0h																															

Table 20-7. CSI_PSILSS0_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R/W1C	0h	The down status of the endpoint links Bit [0]: CSI_STRM Bit [1]: TX0_STRM Bit [2]: RX0_STRM Bit [3]: RX1_STRM

20.2 PDMA_AASRC_PSILSS0 Registers

[Table 20-8](#) lists the PDMA_AASRC_PSILSS0 registers. All register offset addresses not listed in [Table 20-8](#) should be considered as reserved locations and the register contents should not be modified.

Table 20-8. PDMA_AASRC_PSILSS0 Registers

Offset	Acronym	Register Name	AASRC_PSILSS1_MMRS Physical Address
0h	PDMA_AASRC_PSILSS0_PID	Revision Register	0340 C000h
4h	PDMA_AASRC_PSILSS0_CONFIG	Config Register	0340 C004h
10h	PDMA_AASRC_PSILSS0_EVENT	Event Register	0340 C010h
20h	PDMA_AASRC_PSILSS0_LINK	Link Register	0340 C020h
40h	PDMA_AASRC_PSILSS0_DOWN	Link Down Register	0340 C040h

20.2.1 PDMA_AASRC_PSILSS0_PID Register (Offset = 0h) [reset = 66C46100h]

PDMA_AASRC_PSILSS0_PID is shown in [Figure 20-6](#) and described in [Table 20-9](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Figure 20-6. PDMA_AASRC_PSILSS0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C46100h																															

Table 20-9. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C46100h	TI internal data. Identifies revision of peripheral.

20.2.2 PDMA_AASRC_PSILSS0_CONFIG Register (Offset = 4h) [reset = 3h]

PDMA_AASRC_PSILSS0_CONFIG is shown in [Figure 20-7](#) and described in [Table 20-10](#).

Return to the [Summary Table](#).

The Config Register shows configured parameters.

Figure 20-7. PDMA_AASRC_PSILSS0_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENDPOINTS															
R-0h																R-3h															

Table 20-10. PDMA_AASRC_PSILSS0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ENDPOINTS	R	3h	Number of endpoints supported

20.2.3 PDMA_AASRC_PSILSS0_EVENT Register (Offset = 10h) [reset = FFFFh]

PDMA_AASRC_PSILSS0_EVENT is shown in [Figure 20-8](#) and described in [Table 20-11](#).

Return to the [Summary Table](#).

The Event Register defines the event to produce for a link down event.

Figure 20-8. PDMA_AASRC_PSILSS0_EVENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT															
R-0h																R/W-FFFFh															

Table 20-11. PDMA_AASRC_PSILSS0_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	EVT	R/W	FFFFh	The event to produce

20.2.4 PDMA_AASRC_PSILSS0_LINK Register (Offset = 20h) [reset = X]

PDMA_AASRC_PSILSS0_LINK is shown in [Figure 20-9](#) and described in [Table 20-12](#).

Return to the [Summary Table](#).

The Link Register shows the current status of the endpoint links.

Figure 20-9. PDMA_AASRC_PSILSS0_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

Table 20-12. PDMA_AASRC_PSILSS0_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R	X	The status of the endpoint links Bit [0]: PDMA_STRM Bit [1]: MCASP_G0_STRM Bit [2]: AASRC_STRM

20.2.5 PDMA_AASRC_PSILSS0_DOWN Register (Offset = 40h) [reset = 0h]

PDMA_AASRC_PSILSS0_DOWN is shown in and described in .

Return to the [Summary Table](#).

The Link Down Register shows which links are down for the endpoints.

Figure 20-10. PDMA_AASRC_PSILSS0_DOWN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-0h																															

Table 20-13. PDMA_AASRC_PSILSS0_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R/W1C	0h	The down status of the endpoint links Bit [0]: PDMA_STRM Bit [1]: MCASP_G0_STRM Bit [2]: AASRC_STRM

20.3 PDMA_DEBUG_PSILSS0 Registers

[Table 20-14](#) lists the PDMA_DEBUG_PSILSS0 registers. All register offset addresses not listed in [Table 20-14](#) should be considered as reserved locations and the register contents should not be modified.

Table 20-14. PDMA_DEBUG_PSILSS0 Registers

Offset	Acronym	Register Name	DEBUG_PSILSS4_MMRS Physical Address
0h	PDMA_DEBUG_PSILSS0_PID	Revision Register	0340 8000h
4h	PDMA_DEBUG_PSILSS0_CONFIG	Config Register	0340 8004h
10h	PDMA_DEBUG_PSILSS0_EVENT	Event Register	0340 8010h
20h	PDMA_DEBUG_PSILSS0_LINK	Link Register	0340 8020h
40h	PDMA_DEBUG_PSILSS0_DOWN	Link Down Register	0340 8030h

20.3.1 PDMA_DEBUG_PSILSS0_PID Register (Offset = 0h) [reset = 66C45900h]

PDMA_DEBUG_PSILSS0_PID is shown in [Figure 20-11](#) and described in [Table 20-15](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Figure 20-11. PDMA_DEBUG_PSILSS0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C45900h																															

Table 20-15. PDMA_DEBUG_PSILSS0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C45900h	TI internal data. Identifies revision of peripheral.

20.3.2 PDMA_DEBUG_PSILSS0_CONFIG Register (Offset = 4h) [reset = 3h]

PDMA_DEBUG_PSILSS0_CONFIG is shown in [Figure 20-12](#) and described in [Table 20-16](#).

Return to the [Summary Table](#).

The Config Register shows configured parameters.

Figure 20-12. PDMA_DEBUG_PSILSS0_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENDPOINTS															
R-0h																R-3h															

Table 20-16. PDMA_DEBUG_PSILSS0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ENDPOINTS	R	3h	Number of endpoints supported

20.3.3 PDMA_DEBUG_PSILSS0_EVENT Register (Offset = 10h) [reset = FFFFh]

PDMA_DEBUG_PSILSS0_EVENT is shown in [Figure 20-13](#) and described in [Table 20-17](#).

Return to the [Summary Table](#).

The Event Register defines the event to produce for a link down event.

Figure 20-13. PDMA_DEBUG_PSILSS0_EVENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																evt															
R-0h																R/W-FFFFh															

Table 20-17. PDMA_DEBUG_PSILSS0_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	evt	R/W	FFFFh	The event to produce

20.3.4 PDMA_DEBUG_PSILSS0_LINK Register (Offset = 20h) [reset = X]

PDMA_DEBUG_PSILSS0_LINK is shown in [Figure 20-14](#) and described in [Table 20-18](#).

Return to the [Summary Table](#).

The Link Register shows the current status of the endpoint links.

Figure 20-14. PDMA_DEBUG_PSILSS0_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

Table 20-18. PDMA_DEBUG_PSILSS0_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R	X	The status of the endpoint links Bit [0]: PDMA_STRM Bit [1]: CCMCU_STRM Bit [2]: MAINC66_STRM

20.3.5 PDMA_DEBUG_PSILSS0_DOWN Register (Offset = 40h) [reset = 0h]

PDMA_DEBUG_PSILSS0_DOWN is shown in [Figure 20-15](#) and described in [Table 20-19](#).

Return to the [Summary Table](#).

The Link Down Register shows which links are down for the endpoints.

Figure 20-15. PDMA_DEBUG_PSILSS0_DOWN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-0h																															

Table 20-19. PDMA_DEBUG_PSILSS0_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R/W1C	0h	The down status of the endpoint links

20.4 PDMA_MISC_PSILSS0 Registers

[Table 20-20](#) lists the PDMA_MISC_PSILSS0 registers. All register offset addresses not listed in [Table 20-20](#) should be considered as reserved locations and the register contents should not be modified.

Table 20-20. PDMA_MISC_PSILSS0 Registers

Offset	Acronym	Register Name	MISC_PSILSS12_MMRS Physical Address
0h	PDMA_MISC_PSILSS0_PID	Revision Register	0340 4000h
4h	PDMA_MISC_PSILSS0_CONFIG	Config Register	0340 4004h
10h	PDMA_MISC_PSILSS0_EVENT	Event Register	0340 4010h
20h	PDMA_MISC_PSILSS0_LINK	Link Register	0340 4020h
40h	PDMA_MISC_PSILSS0_DOWN	Link Down Register	0340 4040h

20.4.1 PDMA_MISC_PSILSS0_PID Register (Offset = 0h) [reset = 66C45900h]

PDMA_MISC_PSILSS0_PID is shown in [Figure 20-16](#) and described in [Table 20-21](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Figure 20-16. PDMA_MISC_PSILSS0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C45900h																															

Table 20-21. PDMA_MISC_PSILSS0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C45900h	TI internal data. Identifies revision of peripheral.

20.4.2 PDMA_MISC_PSILSS0_CONFIG Register (Offset = 4h) [reset = 5h]

PDMA_MISC_PSILSS0_CONFIG is shown in [Figure 20-17](#) and described in [Table 20-22](#).

Return to the [Summary Table](#).

The Config Register shows configured parameters.

Figure 20-17. PDMA_MISC_PSILSS0_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENDPOINTS															
R-0h																R-5h															

Table 20-22. PDMA_MISC_PSILSS0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ENDPOINTS	R	5h	Number of endpoints supported

20.4.3 PDMA_MISC_PSILSS0_EVENT Register (Offset = 10h) [reset = FFFFh]

PDMA_MISC_PSILSS0_EVENT is shown in [Figure 20-18](#) and described in [Table 20-23](#).

Return to the [Summary Table](#).

The Event Register defines the event to produce for a link down event.

Figure 20-18. PDMA_MISC_PSILSS0_EVENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT															
R-0h																R/W-FFFFh															

Table 20-23. PDMA_MISC_PSILSS0_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	EVT	R/W	FFFFh	The event to produce

20.4.4 PDMA_MISC_PSILSS0_LINK Register (Offset = 20h) [reset = X]

PDMA_MISC_PSILSS0_LINK is shown in [Figure 20-19](#) and described in [Table 20-24](#).

Return to the [Summary Table](#).

The Link Register shows the current status of the endpoint links.

Figure 20-19. PDMA_MISC_PSILSS0_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

Table 20-24. PDMA_MISC_PSILSS0_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R	X	<p>The status of the endpoint links</p> <p>Bit [0]: PDMA_STRM</p> <p>Bit [1]: MISC_G0_STRM</p> <p>Bit [2]: MISC_G1_STRM</p> <p>Bit [3]: MISC_G2_STRM</p> <p>Bit [4]: MISC_G3_STRM</p>

20.4.5 PDMA_MISC_PSILSS0_DOWN Register (Offset = 40h) [reset = 0h]

PDMA_MISC_PSILSS0_DOWN is shown in [Figure 20-20](#) and described in [Table 20-25](#).

Return to the [Summary Table](#).

The Link Down Register shows which links are down for the endpoints.

Figure 20-20. PDMA_MISC_PSILSS0_DOWN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-0h																															

Table 20-25. PDMA_MISC_PSILSS0_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R/W1C	0h	The down status of the endpoint links Bit [0]: PDMA_STRM Bit [1]: MISC_G0_STRM Bit [2]: MISC_G1_STRM Bit [3]: MISC_G2_STRM Bit [4]: MISC_G3_STRM

20.5 PDMA_USART_PSILSS0 Registers

[Table 20-26](#) lists the PDMA_USART_PSILSS0 registers. All register offset addresses not listed in [Table 20-26](#) should be considered as reserved locations and the register contents should not be modified.

Table 20-26. PDMA_USART_PSILSS0 Registers

Offset	Acronym	Register Name	USART_PSILSS16_MMRS Physical Address
0h	PDMA_USART_PSILSS0_PID	Revision Register	0340 0000h
4h	PDMA_USART_PSILSS0_CONFIG	Config Register	0340 0004h
10h	PDMA_USART_PSILSS0_EVENT	Event Register	0340 0010h
20h	PDMA_USART_PSILSS0_LINK	Link Register	0340 0020h
40h	PDMA_USART_PSILSS0_DOWN	Link Down Register	0340 0040h

20.5.1 PDMA_USART_PSILSS0_PID Register (Offset = 0h) [reset = 66C45900h]

PDMA_USART_PSILSS0_PID is shown in [Figure 20-21](#) and described in [Table 20-27](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Figure 20-21. PDMA_USART_PSILSS0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66C45900h																															

Table 20-27. PDMA_USART_PSILSS0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66C45900h	TI internal data. Identifies revision of peripheral.

20.5.2 PDMA_USART_PSILSS0_CONFIG Register (Offset = 4h) [reset = 5h]

PDMA_USART_PSILSS0_CONFIG is shown in [Figure 20-22](#) and described in [Table 20-28](#).

Return to the [Summary Table](#).

The Config Register shows configured parameters.

Figure 20-22. PDMA_USART_PSILSS0_CONFIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ENDPOINTS															
R-0h																R-5h															

Table 20-28. PDMA_USART_PSILSS0_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	ENDPOINTS	R	5h	Number of endpoints supported

20.5.3 PDMA_USART_PSILSS0_EVENT Register (Offset = 10h) [reset = FFFFh]

PDMA_USART_PSILSS0_EVENT is shown in [Figure 20-23](#) and described in [Table 20-29](#).

Return to the [Summary Table](#).

The Event Register defines the event to produce for a link down event.

Figure 20-23. PDMA_USART_PSILSS0_EVENT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																EVT															
R-0h																R/W-FFFFh															

Table 20-29. PDMA_USART_PSILSS0_EVENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	EVT	R/W	FFFFh	The event to produce

20.5.4 PDMA_USART_PSILSS0_LINK Register (Offset = 20h) [reset = X]

PDMA_USART_PSILSS0_LINK is shown in [Figure 20-24](#) and described in [Table 20-30](#).

Return to the [Summary Table](#).

The Link Register shows the current status of the endpoint links.

Figure 20-24. PDMA_USART_PSILSS0_LINK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R-X																															

Table 20-30. PDMA_USART_PSILSS0_LINK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R	X	<p>The status of the endpoint links</p> <p>Bit [0]: PDMA_STRM</p> <p>Bit [1]: USART_G0_STRM</p> <p>Bit [2]: USART_G1_STRM</p> <p>Bit [3]: USART_G2_STRM</p> <p>Bit [4]: MCAN_STRM</p>

20.5.5 PDMA_USART_PSILSS0_DOWN Register (Offset = 40h) [reset = 0h]

PDMA_USART_PSILSS0_DOWN is shown in [Figure 20-25](#) and described in [Table 20-31](#).

Return to the [Summary Table](#).

The Link Down Register shows which links are down for the endpoints.

Figure 20-25. PDMA_USART_PSILSS0_DOWN Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATUS																															
R/W1C-0h																															

Table 20-31. PDMA_USART_PSILSS0_DOWN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	STATUS	R/W1C	0h	The down status of the endpoint links Bit [0]: PDMA_STRM Bit [1]: USART_G0_STRM Bit [2]: USART_G1_STRM Bit [3]: USART_G2_STRM Bit [4]: MCAN_STRM

21 NB Registers

21.1 NAVSS0_NBSS_CFG_REGS0_MMRS Registers

Table 21-2 lists the memory-mapped registers for the NAVSS0_NBSS_CFG_REGS0_MMRS. All register offset addresses not listed in Table 21-2 should be considered as reserved locations and the register contents should not be modified.

The nbss_regs Register Address Space. The address map for this region is as follows:

**Table 21-1. NAVSS0_NBSS_CFG_REGS0_MMRS
Instances**

Instance	Base Address
NAVSS0_NBSS_CFG_REGS0_MMRS	0380 0000h

Table 21-2. NAVSS0_NBSS_CFG_REGS0_MMRS Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_CFG_REGS0_MMRS Physical Address
0h	NBSS_PID	Revision Register	0380 0000h

21.1.1 NBSS_PID Register (Offset = 0h) [reset = 66415200h]

NBSS_PID is shown in [Figure 21-1](#) and described in [Table 21-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 21-3. NBSS_PID Instances

Instance	Physical Address
NAVSS0_NBSS_CFG_REGS0_MMRS	0380 0000h

Figure 21-1. NBSS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-641h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-Ah					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 21-4. NBSS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	641h	Module ID
15-11	RTL	R	Ah	RTL revision. Will vary depending on release.
10-8	MAJOR	R	2h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

Table 21-5. Register Call Summary for NBSS_PID

NAVSS0_NBSS_CFG_REGS0_MMRS Registers

- [NBSS_PID Register \(Offset = 0h\) \[reset = 66415200h\]: \[0\]](#)
- [NAVSS0_NBSS_CFG_REGS0_MMRS Registers: \[0\]](#)

21.2 NAVSS0_NBSS_NB_CFG_MMRS Registers

Table 21-7 lists the memory-mapped registers for the NAVSS0_NBSS_NB_CFG_MMRS. All register offset addresses not listed in Table 21-7 should be considered as reserved locations and the register contents should not be modified.

Config port registers

**Table 21-6. NAVSS0_NBSS_NB_CFG_MMRS
Instances**

Instance	Base Address
NAVSS0_NBSS_NB0_CFG_MMRS	0380 2000h

Table 21-7. NAVSS0_NBSS_NB_CFG_MMRS Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_NB0_CFG_MMRS Physical Address	NAVSS0_NBSS_NB1_CFG_MMRS Physical Address
0h	NB_PID	Revision Register	0380 2000h	0380 3000h
10h	NB_THREADMAP	Thread Map Register	0380 2010h	0380 3010h

21.2.1 NB_PID Register (Offset = 0h) [reset = 6610A900h]

NB_PID is shown in [Figure 21-2](#) and described in [Table 21-9](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 21-8. NB_PID Instances

Instance	Physical Address
NAVSS0_NBSS_NB0_CFG_MMRS	0380 2000h
NAVSS0_NBSS_NB1_CFG_MMRS	0380 3000h

Figure 21-2. NB_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-2h		R-610h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-15h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 21-9. NB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	610h	Module ID
15-11	RTL	R	15h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

21.2.2 NB_THREADMAP Register (Offset = 10h) [reset = X]

NB_THREADMAP is shown in [Figure 21-3](#) and described in [Table 21-11](#).

Return to [Summary Table](#).

The Thread Map Register defines the VBUSM.C thread for each VBUSM source.

Table 21-10. NB_THREADMAP Instances

Instance	Physical Address
NAVSS0_NBSS_NB0_CFG_MMRS	0380 2010h
NAVSS0_NBSS_NB1_CFG_MMRS	0380 3010h

Figure 21-3. NB_THREADMAP Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						THREADMAP	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-11. NB_THREADMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	THREADMAP	R/W	0h	Thread map, each bit is for each VBUSM source. Bit [0] maps orderid 0-7 to VBUSM.C thread number. Bit [1] maps orderid 8-15 to VBUSM.C thread number. 0: VBUSM.C thread 0 (non-real time traffic) 1: VBUSM.C thread 2 (real-time traffic)

21.3 NAVSS0_NBSS_NB0_MEM_ATTR0_CFG Registers

Table 21-13 lists the memory-mapped registers for the NAVSS0_NBSS_NB0_MEM_ATTR0_CFG. All register offset addresses not listed in Table 21-13 should be considered as reserved locations and the register contents should not be modified.

Memory attributes for traffic using OrderID [0-7] on VBUSM0 slave interface.

Table 21-12.
NAVSS0_NBSS_NB0_MEM_ATTR0_CFG Instances

Instance	Base Address
NAVSS0_NBSS_NB0_MEM_ATTR0_CFG	0382 0000h

Table 21-13. NAVSS0_NBSS_NB0_MEM_ATTR0_CFG Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_NB0_MEM_ATTR0_CFG Physical Address
0h + formula	NB_MEMATTR64K_y	Memory Attributes for 64K regions	0382 0000h + formula

21.3.1 NB_MEMATTR64K_y Register (Offset = 0h + formula) [reset = X]

NB_MEMATTR64K_y is shown in Figure 21-4 and described in Table 21-15.

Return to [Summary Table](#).

The Memory Attribute register contains the attributes for all the 64K mapped regions.

Offset = 0h + (y * 4h); where y = 0h to 1FFFh

Table 21-14. NB_MEMATTR64K_y Instances

Instance	Physical Address
NAVSS0_NBSS_NB0_MEM_ATTR0_CFG	0382 0000h + formula

Figure 21-4. NB_MEMATTR64K_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
MEMTYPE		SDOMAIN		OUTER		INNER	
R/W-1h		R/W-1h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-15. NB_MEMATTR64K_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	MEMTYPE	R/W	1h	This defines the type for the memory. 0h = Device 1h = Writeback 2h = Writethrough 3h = Non-cacheable
5-4	SDOMAIN	R/W	1h	This defines the shareability domain of the memory. 0h = Non-shared 1h = Inner shared 2h = Outer shared 3h = System shared
3-2	OUTER	R/W	0h	This defines the outer allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate
1-0	INNER	R/W	0h	This defines the inner allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate

Table 21-16. Register Call Summary for NB_MEMATTR64K_y

NAVSS0_NBSS_NB0_MEM_ATTR0_CFG Registers

- [NB_MEMATTR64K_y Register \(Offset = 0h + formula\) \[reset = X\]: \[0\]](#)
- [NAVSS0_NBSS_NB0_MEM_ATTR0_CFG Registers: \[0\]](#)

21.4 NAVSS0_NBSS_NB0_MEM_ATTR1_CFG Registers

[Table 21-18](#) lists the memory-mapped registers for the NAVSS0_NBSS_NB0_MEM_ATTR1_CFG. All register offset addresses not listed in [Table 21-18](#) should be considered as reserved locations and the register contents should not be modified.

Memory attributes for traffic using OrderID [8-15] on VBUSM1 slave interface.

Table 21-17.
NAVSS0_NBSS_NB0_MEM_ATTR1_CFG Instances

Instance	Base Address
NAVSS0_NBSS_NB0_MEM_ATTR1_CFG	0382 8000h

Table 21-18. NAVSS0_NBSS_NB0_MEM_ATTR1_CFG Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_NB0_MEM_ATTR1_CFG Physical Address
0h + formula	NB_MEMATTR64K_y	Memory Attributes for 64K regions	0382 8000h + formula

21.4.1 NB_MEMATTR64K_y Register (Offset = 0h + formula) [reset = X]

NB_MEMATTR64K_y is shown in Figure 21-5 and described in Table 21-20.

Return to [Summary Table](#).

The Memory Attribute register contains the attributes for all the 64K mapped regions.

Offset = 0h + (y * 4h); where y = 0h to 1FFFh

Table 21-19. NB_MEMATTR64K_y Instances

Instance	Physical Address
NAVSS0_NBSS_NB0_MEM_ATTR1_CFG	0382 8000h + formula

Figure 21-5. NB_MEMATTR64K_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
MEMTYPE		SDOMAIN		OUTER		INNER	
R/W-1h		R/W-1h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-20. NB_MEMATTR64K_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	MEMTYPE	R/W	1h	This defines the type for the memory. 0h = Device 1h = Writeback 2h = Writethrough 3h = Non-cacheable
5-4	SDOMAIN	R/W	1h	This defines the shareability domain of the memory. 0h = Non-shared 1h = Inner shared 2h = Outer shared 3h = System shared
3-2	OUTER	R/W	0h	This defines the outer allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate
1-0	INNER	R/W	0h	This defines the inner allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate

Table 21-21. Register Call Summary for NB_MEMATTR64K_y

NAVSS0_NBSS_NB0_MEM_ATTR1_CFG Registers <ul style="list-style-type: none"> • NB_MEMATTR64K_y Register (Offset = 0h + formula) [reset = X]: [0] • NAVSS0_NBSS_NB0_MEM_ATTR1_CFG Registers: [0]

21.5 NAVSS0_NBSS_NB1_CFG_MMRS Registers

Table 21-23 lists the memory-mapped registers for the NAVSS0_NBSS_NB1_CFG_MMRS. All register offset addresses not listed in Table 21-23 should be considered as reserved locations and the register contents should not be modified.

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**Table 21-22. NAVSS0_NBSS_NB1_CFG_MMRS
Instances**

Instance	Base Address
NAVSS0_NBSS_NB1_CFG_MMRS	0380 3000h

Table 21-23. NAVSS0_NBSS_NB1_CFG_MMRS Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_NB1_CFG_MMRS Physical Address
0h	NB_PID	Revision Register	0380 3000h
10h	NB_THREADMAP	Thread Map Register	0380 3010h

21.5.1 NB_PID Register (Offset = 0h) [reset = 6610A900h]

NB_PID is shown in Figure 21-6 and described in Table 21-25.

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 21-24. NB_PID Instances

Instance	Physical Address
NAVSS0_NBSS_NB1_CFG_MMRS	0380 3000h

Figure 21-6. NB_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME				BU		FUNC									
R-1h				R-2h		R-610h									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-15h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 21-25. NB_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	610h	Module ID
15-11	RTL	R	15h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

Table 21-26. Register Call Summary for NB_PID

NAVSS0_NBSS_NB1_CFG_MMRS Registers

- [NB_PID Register \(Offset = 0h\) \[reset = 6610A900h\]: \[0\]](#)
- [NAVSS0_NBSS_NB1_CFG_MMRS Registers: \[0\]](#)

21.5.2 NB_THREADMAP Register (Offset = 3010h) [reset = X]

NB_THREADMAP is shown in [Figure 21-7](#) and described in [Table 21-28](#).

Return to [Summary Table](#).

The Thread Map Register defines the VBUSM.C thread for each VBUSM source.

Table 21-27. NB_THREADMAP Instances

Instance	Physical Address
NAVSS0_NBSS_NB1_CFG_MMRS	0380 3010h

Figure 21-7. NB_THREADMAP Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						THREADMAP	
R/W-X						R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-28. NB_THREADMAP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1-0	THREADMAP	R/W	0h	Thread map, each bit is for each VBUSM source. Bit [0] maps orderid 0-7 to VBUSM.C thread number. Bit [1] maps orderid 8-15 to VBUSM.C thread number. 0: VBUSM.C thread 0 (non-real time traffic) 1: VBUSM.C thread 2 (real-time traffic)

Table 21-29. Register Call Summary for NB_THREADMAP

NAVSS0_NBSS_NB1_CFG_MMRS Registers
<ul style="list-style-type: none"> NB_THREADMAP Register (Offset = 3010h) [reset = X]: [0] NAVSS0_NBSS_NB1_CFG_MMRS Registers: [0]

21.6 NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Registers

Table 21-31 lists the memory-mapped registers for the NAVSS0_NBSS_NB1_MEM_ATTR0_CFG. All register offset addresses not listed in Table 21-31 should be considered as reserved locations and the register contents should not be modified.

Memory attributes for traffic using OrderID [0-7] on VBUSM0 slave interface.

Table 21-30.
NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Instances

Instance	Base Address
NAVSS0_NBSS_NB1_MEM_ATTR0_CFG	0384 0000h

Table 21-31. NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Physical Address
0h + formula	NB_MEMATTR16M0_y	Memory Attributes for first 16M regions	0384 0000h + formula
200h + formula	NB_MEMATTR16M1_y	Memory Attributes for second 16M regions	0384 0200h + formula

21.6.1 NB_MEMATTR16M0_y Register (Offset = 0h + formula) [reset = X]

NB_MEMATTR16M0_y is shown in [Figure 21-8](#) and described in [Table 21-33](#).

Return to [Summary Table](#).

The Memory Attribute register contains the attributes for all the first 16M mapped regions.

Offset = 0h + (y * 4h); where y = 0h to 7Fh

Table 21-32. NB_MEMATTR16M0_y Instances

Instance	Physical Address
NAVSS0_NBSS_NB1_MEM_ATTR0_CF G	0384 0000h + formula

Figure 21-8. NB_MEMATTR16M0_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
MEMTYPE		SDOMAIN		OUTER		INNER	
R/W-1h		R/W-1h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-33. NB_MEMATTR16M0_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	MEMTYPE	R/W	1h	This defines the type for the memory. 0h = Device 1h = Writeback 2h = Writethrough 3h = Non-cacheable
5-4	SDOMAIN	R/W	1h	This defines the shareability domain of the memory. 0h = Non-shared 1h = Inner shared 2h = Outer shared 3h = System shared
3-2	OUTER	R/W	0h	This defines the outer allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate
1-0	INNER	R/W	0h	This defines the inner allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate

Table 21-34. Register Call Summary for NB_MEMATTR16M0_y

NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Registers
<ul style="list-style-type: none"> • NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Registers: [0] • NB_MEMATTR16M0_y Register (Offset = 0h + formula) [reset = X]: [0]

21.6.2 NB_MEMATTR16M1_y Register (Offset = 200h + formula) [reset = X]

NB_MEMATTR16M1_y is shown in Figure 21-9 and described in Table 21-36.

Return to [Summary Table](#).

The Memory Attribute register contains the attributes for all the second 16M mapped regions.

Offset = 200h + (y * 4h); where y = 0h to 1FFFh

Table 21-35. NB_MEMATTR16M1_y Instances

Instance	Physical Address
NAVSS0_NBSS_NB1_MEM_ATTR0_CF G	0384 0200h + formula

Figure 21-9. NB_MEMATTR16M1_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
MEMTYPE		SDOMAIN		OUTER		INNER	
R/W-1h		R/W-1h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-36. NB_MEMATTR16M1_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	MEMTYPE	R/W	1h	This defines the type for the memory. 0h = Device 1h = Writeback 2h = Writethrough 3h = Non-cacheable
5-4	SDOMAIN	R/W	1h	This defines the shareability domain of the memory. 0h = Non-shared 1h = Inner shared 2h = Outer shared 3h = System shared
3-2	OUTER	R/W	0h	This defines the outer allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate
1-0	INNER	R/W	0h	This defines the inner allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate

Table 21-37. Register Call Summary for NB_MEMATTR16M1_y

NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Registers
<ul style="list-style-type: none"> • NAVSS0_NBSS_NB1_MEM_ATTR0_CFG Registers: [0] • NB_MEMATTR16M1_y Register (Offset = 200h + formula) [reset = X]: [0]

21.7 NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Registers

[Table 21-39](#) lists the memory-mapped registers for the NAVSS0_NBSS_NB1_MEM_ATTR1_CFG. All register offset addresses not listed in [Table 21-39](#) should be considered as reserved locations and the register contents should not be modified.

Memory attributes for traffic using OrderID [8-15] on VBUSM1 slave interface.

Table 21-38.
NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Instances

Instance	Base Address
NAVSS0_NBSS_NB1_MEM_ATTR1_CFG	0385 0000h

Table 21-39. NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Registers

Offset	Acronym	Register Name	NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Physical Address
0h + formula	NB_MEMATTR16M0_y	Memory Attributes for first 16M regions	0385 0000h + formula
200h + formula	NB_MEMATTR16M1_y	Memory Attributes for second 16M regions	0385 0200h + formula

21.7.1 NB_MEMATTR16M0_y Register (Offset = 0h + formula) [reset = X]

NB_MEMATTR16M0_y is shown in Figure 21-10 and described in Table 21-41.

Return to [Summary Table](#).

The Memory Attribute register contains the attributes for all the first 16M mapped regions.

Offset = 0h + (y * 4h); where y = 0h to 7Fh

Table 21-40. NB_MEMATTR16M0_y Instances

Instance	Physical Address
NAVSS0_NBSS_NB1_MEM_ATTR1_CF G	0385 0000h + formula

Figure 21-10. NB_MEMATTR16M0_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
MEMTYPE		SDOMAIN		OUTER		INNER	
R/W-1h		R/W-1h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-41. NB_MEMATTR16M0_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	MEMTYPE	R/W	1h	This defines the type for the memory. 0h = Device 1h = Writeback 2h = Writethrough 3h = Non-cacheable
5-4	SDOMAIN	R/W	1h	This defines the shareability domain of the memory. 0h = Non-shared 1h = Inner shared 2h = Outer shared 3h = System shared
3-2	OUTER	R/W	0h	This defines the outer allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate
1-0	INNER	R/W	0h	This defines the inner allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate

Table 21-42. Register Call Summary for NB_MEMATTR16M0_y

NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Registers

- [NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Registers: \[0\]](#)
- [NB_MEMATTR16M0_y Register \(Offset = 0h + formula\) \[reset = X\]: \[0\]](#)

21.7.2 NB_MEMATTR16M1_y Register (Offset = 200h + formula) [reset = X]

NB_MEMATTR16M1_y is shown in Figure 21-11 and described in Table 21-44.

Return to [Summary Table](#).

The Memory Attribute register contains the attributes for all the second 16M mapped regions.

Offset = 200h + (y * 4h); where y = 0h to 1FFFh

Table 21-43. NB_MEMATTR16M1_y Instances

Instance	Physical Address
NAVSS0_NBSS_NB1_MEM_ATTR1_CF G	0385 0200h + formula

Figure 21-11. NB_MEMATTR16M1_y Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
MEMTYPE		SDOMAIN		OUTER		INNER	
R/W-1h		R/W-1h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 21-44. NB_MEMATTR16M1_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-6	MEMTYPE	R/W	1h	This defines the type for the memory. 0h = Device 1h = Writeback 2h = Writethrough 3h = Non-cacheable
5-4	SDOMAIN	R/W	1h	This defines the shareability domain of the memory. 0h = Non-shared 1h = Inner shared 2h = Outer shared 3h = System shared
3-2	OUTER	R/W	0h	This defines the outer allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate
1-0	INNER	R/W	0h	This defines the inner allocatability of the memory. 0h = Non-allocatable 1h = Writes allocate, reads do not 2h = Reads allocate, writes do not 3h = Reads and writes allocate

Table 21-45. Register Call Summary for NB_MEMATTR16M1_y

NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Registers

- [NAVSS0_NBSS_NB1_MEM_ATTR1_CFG Registers: \[0\]](#)
- [NB_MEMATTR16M1_y Register \(Offset = 200h + formula\) \[reset = X\]: \[0\]](#)

22 PDMA Registers

22.1 PDMA PSI-L RX Configuration Registers

Table 22-2 lists the PDMA PSI-L RX configuration registers (PDMA_PSILCFG_RX). These registers are not memory mapped and are accessed indirectly via CFG_PROXY modules in NAVSS.

Table 22-1. PDMA_PSILCFG_RX Instances

Instance	Base Address
PDMA_PSILCFG_RX	N/A

Table 22-2. PDMA_PSILCFG_RX Registers

Offset	Acronym	Register Name	PDMA_PSILCFG_RX Physical Address
0h	PDMA_PSILCFG_RX_PEER_THREAD_ID	RX peer thread ID register	N/A
1h	PDMA_PSILCFG_RX_PEER_CREDIT	RX peer credit register	N/A
2h	PDMA_PSILCFG_RX_ENABLE	RX enable register	N/A
400h	PDMA_PSILCFG_RX_STATIC_TR	RX static transfer request (X, Y) register	N/A
401h	PDMA_PSILCFG_RX_STATIC_TR_Z	RX static transfer request (Z) register	N/A
402h	PDMA_PSILCFG_RX_DEBUG_1	RX debug/state register 1	N/A
403h	PDMA_PSILCFG_RX_DEBUG_2	RX debug/state register 2	N/A
404h	PDMA_PSILCFG_RX_BYTE_COUNT	RX byte count register	N/A
405h	PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG	RX AASRC Rx FIFO configuration register	N/A
406h	PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0	RX AASRC Rx order table 0	N/A
407h	PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1	RX AASRC Rx order table 1	N/A
408h	PDMA_PSILCFG_RX_RT_ENABLE	RX real-time enable register	N/A
40Fh	PDMA_PSILCFG_RX_DEBUG_3	RX debug/state register 3	N/A

22.1.1 PDMA_PSILCFG_RX_PEER_THREAD_ID Register (Offset = 0h) [reset = 0h]

PDMA_PSILCFG_RX_PEER_THREAD_ID is shown in [Figure 22-1](#) and described in [Table 22-4](#).

Return to [Summary Table](#).

Peer Thread ID Register. This register contains the thread ID of the thread destination which is used for routing the messages. This register is only implemented for source threads.

Table 22-3. PDMA_PSILCFG_RX_PEER_THREAD_ID Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-1. PDMA_PSILCFG_RX_PEER_THREAD_ID

31	30	29	28	27	26	25	24
THREAD_PRIORITY				PEER_THREAD_WIDTH			
R-0h				R/W-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
PEER_THREAD_ID							
R/W-0h							
7	6	5	4	3	2	1	0
PEER_THREAD_ID							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-4. PDMA_PSILCFG_RX_PEER_THREAD_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	THREAD_PRIORITY	R	0h	Priority level to use for this source thread in arbitration. This field is hard coded to 0h and is not writable
28-24	PEER_THREAD_WIDTH	R/W	0h	Datapath width of paired peer destination thread. This field is encoded as follows: 0h = 32-bit 1h = 64-bit 2h = 128-bit 3h = 256-bit 4h = 512-bit
23-16	RESERVED	R	0h	Reserved
15-0	PEER_THREAD_ID	R/W	0h	Thread ID to which all nontransfer response, nonconfiguration messages from this thread are sent

22.1.2 PDMA_PSILCFG_RX_PEER_CREDIT Register (Offset = 1h) [reset = 0h]

PDMA_PSILCFG_RX_PEER_CREDIT is shown in [Figure 22-2](#) and described in [Table 22-6](#).

Return to [Summary Table](#).

Peer Credit Register. This register contains a free credit count in completed destination data phases for the thread destination. This register is only implemented for source threads.

Table 22-5. PDMA_PSILCFG_RX_PEER_CREDIT Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-2. PDMA_PSILCFG_RX_PEER_CREDIT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CREDIT_CNT							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-6. PDMA_PSILCFG_RX_PEER_CREDIT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	CREDIT_CNT	R/W	0h	Free entries in destination thread. This field is encoded as follows: 0h to 80h = Actual count in data phases 81h to FFh = Reserved

22.1.3 PDMA_PSILCFG_RX_ENABLE Register (Offset = 2h) [reset = 0h]

PDMA_PSILCFG_RX_ENABLE is shown in [Figure 22-3](#) and described in [Table 22-8](#).

Return to [Summary Table](#).

Enable Register. This register contains enable control for the thread.

Table 22-7. PDMA_PSILCFG_RX_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-3. PDMA_PSILCFG_RX_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-8. PDMA_PSILCFG_RX_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the RX channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all credit returns, and will not generate egress data. A one-to-zero transition on this bit fully resets the channel.
30-0	RESERVED	R	0h	Reserved

22.1.4 PDMA_PSILCFG_RX_STATIC_TR Register (Offset = 400h) [reset = 0h]

PDMA_PSILCFG_RX_STATIC_TR is shown in [Figure 22-4](#) and described in [Table 22-10](#).

Return to [Summary Table](#).

Static Transfer Request (X, Y) Register. This register is used to define the 'X' and 'Y' parameters in a static TR.

Table 22-9. PDMA_PSILCFG_RX_STATIC_TR Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-4. PDMA_PSILCFG_RX_STATIC_TR Register

31	30	29	28	27	26	25	24
BURST	ACC32	RESERVED				X	
R/W-0h	R/W-0h	R-0h				R/W-0h	
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				Y			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-10. PDMA_PSILCFG_RX_STATIC_TR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BURST	R/W	0h	X-Y FIFO mode static TR: When set, enables VBUSP burst mode on this channel. See the XY burst description for more information. MCAN mode static TR: When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information. AASRC mode static TR: Not used.
30	ACC32	R/W	0h	X-Y FIFO mode static TR: When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide. MCAN mode static TR: Not used. AASRC mode static TR: When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
29-27	RESERVED	R	0h	Reserved

Table 22-10. PDMA_PSILCFG_RX_STATIC_TR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	X	R/W	0h	<p>X-Y FIFO mode static TR: Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h = 16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.</p> <p>MCAN mode static TR: Not used.</p> <p>AASRC mode static TR: Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h = 16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.</p>
23-12	RESERVED	R	0h	Reserved
11-0	Y	R/W	0h	<p>X-Y FIFO mode static TR: Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.</p> <p>MCAN mode static TR: Buffer Size. This field specifies how many bytes should be read from an MCAN RX buffer. This field includes the 8 byte MCAN header on the initial packet fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.</p> <p>AASRC mode static TR: FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.</p>

22.1.5 PDMA_PSILCFG_RX_STATIC_TR_Z Register (Offset = 401h) [reset = 0h]

PDMA_PSILCFG_RX_STATIC_TR_Z is shown in [Figure 22-5](#) and described in [Table 22-12](#).

Return to [Summary Table](#).

Static Transfer Request (Z) Register. This register is used to define the 'Z' parameter in a static TR.

Table 22-11. PDMA_PSILCFG_RX_STATIC_TR_Z Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-5. PDMA_PSILCFG_RX_STATIC_TR_Z Register

31	30	29	28	27	26	25	24
EOL	RESERVED						
R/W-0h				R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				Z			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
Z							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-12. PDMA_PSILCFG_RX_STATIC_TR_Z Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EOL	R/W	0h	EOL mode. Normally, when the Z count of FIFO operations has been reached, the PDMA will close the packet with an 'EOP' indication. When this flag is set, the PDMA will instead trigger an EOL at the completion of Z.
30-12	RESERVED	R	0h	Reserved

Table 22-12. PDMA_PSILCFG_RX_STATIC_TR_Z Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-0	Z	R/W	0h	<p>X-Y FIFO mode static TR: FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an EOP indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.</p> <p>MCAN mode static TR: Buffer Count. This field specifies how many MCAN RX buffers should be read before closing the CPPI packet with an EOP indication. When this count is greater than 1, multiple MCAN RX buffers will be read into a single CPPI packet buffer. The 8-byte MCAN header will be skipped on subsequent MCAN buffer reads. Setting this field to NULL will suppress all packet delineation, and should be avoided.</p> <p>AASRC mode static TR: FIFO count. This field specifies how many full FIFO operations comprise a complete packet. When the count has been reached, the PDMA will close the packet with an EOP indication. If this parameter is set to NULL, then no packet delineation is supplied by the PDMA and all framing is controlled via the UDMA-P TR.</p>

22.1.6 PDMA_PSILCFG_RX_DEBUG_1 Register (Offset = 402h) [reset = 0h]

PDMA_PSILCFG_RX_DEBUG_1 is shown in [Figure 22-6](#) and described in [Table 22-14](#).

Return to [Summary Table](#).

Debug/State Register 1. The debug/state registers give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations.

**Table 22-13. PDMA_PSILCFG_RX_DEBUG_1
Instances**

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-6. PDMA_PSILCFG_RX_DEBUG_1 Register

31	30	29	28	27	26	25	24
Z							
R/W-0h							
23	22	21	20	19	18	17	16
Z							
R/W-0h							
15	14	13	12	11	10	9	8
Y							
R/W-0h							
7	6	5	4	3	2	1	0
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-14. PDMA_PSILCFG_RX_DEBUG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	Z	R/W	0h	This field holds the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.
15-0	Y	R/W	0h	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to be read from the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next read offset to use when read to the CAN RX buffer.

22.1.7 PDMA_PSILCFG_RX_DEBUG_2 Register (Offset = 403h) [reset = 0h]

PDMA_PSILCFG_RX_DEBUG_2 is shown in [Figure 22-7](#) and described in [Table 22-16](#).

Return to [Summary Table](#).

Debug/State Register 2. The debug/state registers give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations.

**Table 22-15. PDMA_PSILCFG_RX_DEBUG_2
Instances**

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-7. PDMA_PSILCFG_RX_DEBUG_2 Register

31	30	29	28	27	26	25	24
INEVENT	TDOWN	PAUSE	SPACE	XSPACE	BUFFER	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	
23	22	21	20	19	18	17	16
STATE				EVENTCNT			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-16. PDMA_PSILCFG_RX_DEBUG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INEVENT	R/W	0h	When set, the PDMA is in the middle of processing a FIFO event.
30	TDOWN	R/W	0h	When set, the PDMA is processing a teardown operation. This bit is set simultaneously with the teardown bit in the source (RX) RT enable register. This bit will clear when the teardown is complete, regardless as to if the teardown bit in the pairing register is cleared or not. The teardown will propagate to the UDMA-P and its full completion status can be checked there.
29	PAUSE	R/W	0h	When set, the PDMA is stopped in a paused state. This bit will clear if the channel is unpaused or disabled.
28	SPACE	R/W	0h	When set, there is a non-zero amount of internal FIFO space available to hold new read data.
27	XSPACE	R/W	0h	When set, there is enough internal FIFO space available to start servicing a peripheral DMA event.
26	BUFFER	R/W	0h	This is the current RX buffer (0/1) for the current MCAN receive operation.
25-24	RESERVED	R	0h	Reserved
23-20	STATE	R/W	0h	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
19-16	EVENTCNT	R/W	0h	This field holds the number of backlogged DMA events yet to be serviced.

Table 22-16. PDMA_PSILCFG_RX_DEBUG_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	RESERVED	R	0h	Reserved

22.1.8 PDMA_PSILCFG_RX_BYTE_COUNT Register (Offset = 404h) [reset = 0h]

PDMA_PSILCFG_RX_BYTE_COUNT is shown in [Figure 22-8](#) and described in [Table 22-18](#).

Return to [Summary Table](#).

Byte Count Register. This register contains the number of bytes that have been written to the VBUSP mapped peripheral.

Table 22-17. PDMA_PSILCFG_RX_BYTE_COUNT Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-8. PDMA_PSILCFG_RX_BYTE_COUNT Register

31	30	29	28	27	26	25	24
BYTES							
R/W-0h							
23	22	21	20	19	18	17	16
BYTES							
R/W-0h							
15	14	13	12	11	10	9	8
BYTES							
R/W-0h							
7	6	5	4	3	2	1	0
BYTES							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-18. PDMA_PSILCFG_RX_BYTE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BYTES	R/W	0h	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write-to-decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

22.1.9 PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register (Offset = 405h) [reset = 0h]

PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG is shown in [Figure 22-9](#) and described in [Table 22-20](#).

Return to [Summary Table](#).

AASRC Rx FIFO configuration register.

Table 22-19.
PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG
Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-9. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register

31	30	29	28	27	26	25	24
GROUPMODE	DMAREQRESET	RESERVED					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
LASTSLOT				FIRSTSLOT			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
DMAREQMASK							
R/W-0h							
7	6	5	4	3	2	1	0
DMAREQMASK							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-20. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GROUPMODE	R/W	0h	When set, the channel is in 'group mode'. It will look for group mode DMA requests, and access the group mode FIFOs. When clear, the channel is 'stream mode'. It will look for stream FIFO DMA requests, and access the stream mode FIFOs.
30	DMAREQRESET	R/W	0h	When set, resets any latched DMA request using the DMAREQMASK. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
29-24	RESERVED	R	0h	Reserved
23-20	LASTSLOT	R/W	0h	This is the index (0-15) of the last slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19-16	FIRSTSLOT	R/W	0h	This is the index (0-15) of the first slot in the RX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.

Table 22-20. PDMA_PSILCFG_RX_AASRC_RX_FIFO_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	DMAREQMASK	R/W	0h	<p>This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate.</p> <p>In steam mode, these 16 flags correspond to the 16 DMA requests for each RX FIFO. The flags corresponding to all RX FIFOs involved with the channel should be set to 1.</p> <p>In group mode, these flags indicate which group mode DMA requests must fire. In this case, only bits [3:0] are relevant and only one bit should be set to 1 as a DMA channel only services a single group.</p>

22.1.10 PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Register (Offset = 406h) [reset = 0h]

PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 is shown in [Figure 22-10](#) and described in [Table 22-22](#).

Return to [Summary Table](#).

AASRC RX order table 0 register.

Table 22-21.
PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0
Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-10. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Register

31	30	29	28	27	26	25	24
ENTRY7				ENTRY6			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
ENTRY5				ENTRY4			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
ENTRY3				ENTRY2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ENTRY1				ENTRY0			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 22-22. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ENTRY7	R/W	7h	RX FIFO index for slot 7
27-24	ENTRY6	R/W	6h	RX FIFO index for slot 6
23-20	ENTRY5	R/W	5h	RX FIFO index for slot 5
19-16	ENTRY4	R/W	4h	RX FIFO index for slot 4
15-12	ENTRY3	R/W	3h	RX FIFO index for slot 3
11-8	ENTRY2	R/W	2h	RX FIFO index for slot 2
7-4	ENTRY1	R/W	1h	RX FIFO index for slot 1
3-0	ENTRY0	R/W	0h	RX FIFO index for slot 0

22.1.11 PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Register (Offset = 407h) [reset = 0h]

PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 is shown in [Figure 22-11](#) and described in [Table 22-24](#).

Return to [Summary Table](#).

AASRC RX order table 1 register.

Table 22-23.
PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1
Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-11. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Register

31	30	29	28	27	26	25	24
ENTRY15				ENTRY14			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
ENTRY13				ENTRY12			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
ENTRY11				ENTRY10			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ENTRY9				ENTRY8			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 22-24. PDMA_PSILCFG_RX_AASRC_RX_ORDER_TABLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ENTRY15	R/W	Fh	RX FIFO index for slot 15
27-24	ENTRY14	R/W	Eh	RX FIFO index for slot 14
23-20	ENTRY13	R/W	Dh	RX FIFO index for slot 13
19-16	ENTRY12	R/W	Ch	RX FIFO index for slot 12
15-12	ENTRY11	R/W	Bh	RX FIFO index for slot 11
11-8	ENTRY10	R/W	Ah	RX FIFO index for slot 10
7-4	ENTRY9	R/W	9h	RX FIFO index for slot 9
3-0	ENTRY8	R/W	8h	RX FIFO index for slot 8

22.1.12 PDMA_PSILCFG_RX_RT_ENABLE Register (Offset = 408h) [reset = 0h]

PDMA_PSILCFG_RX_RT_ENABLE is shown in [Figure 22-12](#) and described in [Figure 22-12](#).

Return to [Summary Table](#).

Real Time Enable Register. This register allows enabling various channel settings in real time.

Table 22-25. PDMA_PSILCFG_RX_RT_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-12. PDMA_PSILCFG_RX_RT_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	TDOWN	PAUSE	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R-0h				
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						IDLE	FREE
R-0h						R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-26. PDMA_PSILCFG_RX_RT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the RX channel is enabled. When cleared, the RX channel is disabled. When disabled, the channel ignores all DMA events from the peripheral. It maintains proper data transfers with the UDMA-P such that the credit handshake is not disrupted. However, unlike teardown, it does not close out the current open packet. Thus the TDOWN bit should always be used to disable an RX channel instead of manually clearing this bit. Failing to use teardown may result in stale data remaining in the internal RX FIFO, which would also prevent the channel from going idle without a channel reset. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	TDOWN	R/W	0h	When set, the channel will commence a RX channel teardown procedure. It will stop on the next FIFO boundary. It then clears the DMA event count and ignores all future DMA events from the peripheral. After stopping peripheral reads, the PDMA sends a teardown message to the UDMA-P that also closes the current packet with an EOP. If no packet is open at the time of the teardown, the message also includes SOP. The EOP teardown message may or may not contain final packet data. Once the channel teardown is complete and ready to be reused, the ENABLE bit is cleared.

Table 22-26. PDMA_PSILCFG_RX_RT_ENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
29	PAUSE	R/W	0h	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals but will not act on them. The PAUSE bit can be cleared and data will resume. Pause will not stop teardown from completing.
28-2	RESERVED	R	0h	Reserved
1	IDLE	R	0h	This is a read-only bit that signifies that the paused or disabled channel is also idle. It can only become set if PAUSE is set or ENABLE is cleared.
0	FREE	R/W	0h	When cleared, the channel honors the debug suspend signal. When set, the channel will 'free run', regardless of the value of debug suspend.

22.1.13 PDMA_PSILCFG_RX_DEBUG_3 Register (Offset = 40Fh) [reset = 0h]

PDMA_PSILCFG_RX_DEBUG_3 is shown in [Figure 22-13](#) and described in [Table 22-28](#).

Return to [Summary Table](#).

Debug/State Register 3. The debug/state registers give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations.

**Table 22-27. PDMA_PSILCFG_RX_DEBUG_3
Instances**

Instance	Physical Address
PDMA_PSILCFG_RX	N/A

Figure 22-13. PDMA_PSILCFG_RX_DEBUG_3 Register

31	30	29	28	27	26	25	24
Z							
R/W-0h							
23	22	21	20	19	18	17	16
Z							
R/W-0h							
15	14	13	12	11	10	9	8
Z							
R/W-0h							
7	6	5	4	3	2	1	0
Z							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-28. PDMA_PSILCFG_RX_DEBUG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Z	R/W	0h	This field holds the full width value of the current Z count. In X-Y FIFO mode, this field holds the 1 based FIFO count of the FIFO being currently read, or the number of FIFO completions when the current operation completes. In MCAN mode, this field holds the zero based buffer index of the buffer currently being read, or the number of previously completed buffers.

22.2 PDMA PSI-L TX Configuration Registers

Table 22-30 lists the PDMA PSI-L TX configuration registers (PDMA_PSILCFG_TX). These registers are not memory mapped and are accessed indirectly via CFG_PROXY modules in NAVSS.

Table 22-29. PDMA_PSILCFG_TX Instances

Instance	Base Address
PDMA_PSILCFG_TX	N/A

Table 22-30. PDMA_PSILCFG_TX Registers

Offset	Acronym	Register Name	PDMA_PSILCFG_TX Physical Address
2h	PDMA_PSILCFG_TX_ENABLE	TX enable register	N/A
40h	PDMA_PSILCFG_TX_CAPABILITIES	TX local capabilities register	N/A
400h	PDMA_PSILCFG_TX_STATIC_TR	TX static transfer request (X, Y) register	N/A
402h	PDMA_PSILCFG_TX_DEBUG_1	TX debug/state register 1	N/A
403h	PDMA_PSILCFG_TX_DEBUG_2	TX debug/state register 2	N/A
404h	PDMA_PSILCFG_TX_BYTE_COUNT	TX byte count register	N/A
405h	PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG	TX AASRC Tx FIFO configuration register	N/A
406h	PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0	TX AASRC Tx order table 0	N/A
407h	PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1	TX AASRC Tx order table 1	N/A
408h	PDMA_PSILCFG_TX_RT_ENABLE	TX real-time enable register	N/A

22.2.1 PDMA_PSILCFG_TX_ENABLE Register (Offset = 2h) [reset = 0h]

PDMA_PSILCFG_TX_ENABLE is shown in [Figure 22-14](#) and described in [Table 22-32](#).

Return to [Summary Table](#).

Enable Register. This register contains enable control for the thread.

Table 22-31. PDMA_PSILCFG_TX_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-14. PDMA_PSILCFG_TX_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-32. PDMA_PSILCFG_TX_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the TX channel is enabled. When cleared, the TX channel is disabled. When disabled, the channel discards all ingress data. A one-to-zero transition on this bit fully resets the channel.
30-0	RESERVED	R	0h	Reserved

22.2.2 PDMA_PSILCFG_TX_CAPABILITIES Register (Offset = 40h) [reset = Xh]

PDMA_PSILCFG_TX_CAPABILITIES is shown in [Figure 22-15](#) and described in [Table 22-34](#).

Return to [Summary Table](#).

Local Capabilities Register. This register provides the width and count of the credits for which buffering is available in the local thread. This register can be read by the system configuration software to determine what values to place in the following registers of the source paired thread:

- PDMA_PSILCFG_RX_PEER_CREDIT and PDMA_PSILCFG_RX_PEER_THREAD_ID

This register is only implemented for destination threads.

**Table 22-33. PDMA_PSILCFG_TX_CAPABILITIES
Instances**

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-15. PDMA_PSILCFG_TX_CAPABILITIES Register

31	30	29	28	27	26	25	24
RESERVED				LOCAL_THREAD_WIDTH			
R-0h				R-2h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
LOCAL_CREDIT_CNT							
R-8h							

LEGEND: R = Read Only; -n = value after reset

Table 22-34. PDMA_PSILCFG_TX_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28-24	LOCAL_THREAD_WIDTH	R	2h	Read-only element width for the local thread used for pairing purposes. 0h = 4 bytes 1h = 8 bytes 2h = 16 bytes 3h to 1Fh = Reserved
23-8	RESERVED	R	0h	Reserved
7-0	LOCAL_CREDIT_CNT	R	7h	Read-only local thread free entry count used for pairing purposes. This field is encoded as follows: 0h to 80h = Available count in elements 81h to FFh = Reserved

22.2.3 PDMA_PSILCFG_TX_STATIC_TR Register (Offset = 400h) [reset = 0h]

PDMA_PSILCFG_TX_STATIC_TR is shown in [Figure 22-16](#) and described in [Table 22-36](#).

Return to [Summary Table](#).

Static Transfer Request (X, Y) Register. This register is used to define the 'X' and 'Y' parameters in a static TR.

Table 22-35. PDMA_PSILCFG_TX_STATIC_TR Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-16. PDMA_PSILCFG_TX_STATIC_TR Register

31	30	29	28	27	26	25	24
BURST	ACC32	RESERVED				X	
R/W-0h	R/W-0h	R-0h				R/W-0h	
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				Y			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-36. PDMA_PSILCFG_TX_STATIC_TR Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BURST	R/W	0h	X-Y FIFO mode static TR: When set, enables VBUSP burst mode on this channel. See the XY burst description for more information. MCAN mode static TR: When set, enables VBUSP burst mode on this channel. See the MCAN burst description for more information. AASRC mode static TR: Not used.
30	ACC32	R/W	0h	X-Y FIFO mode static TR: When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide. MCAN mode static TR: Not used. AASRC mode static TR: When set, enables 32-bit access mode. On a 32-bit PDMA, all accesses will have XCNT=4 to support legacy IP that is not fully VBUSP compliant. This bit is ignored if the PDMA VBUSP port is not 32 bits wide.
29-27	RESERVED	R	0h	Reserved

Table 22-36. PDMA_PSILCFG_TX_STATIC_TR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
26-24	X	R/W	0h	<p>X-Y FIFO mode static TR: Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h = 16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.</p> <p>MCAN mode static TR: Not used.</p> <p>AASRC mode static TR: Element size. This field specifies how much data is transferred in each write which is performed by the DMA. This field is encoded as follows: 0h = 8 bits; 1h = 16 bits; 2h = 24 bits; 3h = 32 bits; 4h = 64 bits; 5h-7h = RESERVED.</p>
23-12	RESERVED	R	0h	Reserved
11-0	Y	R/W	0h	<p>X-Y FIFO mode static TR: Element count. This field specifies how many elements to transfer each time a trigger is received on the channel.</p> <p>MCAN mode static TR: Buffer Size. This field specifies how many bytes should be written to an MCAN TX buffer. This field includes the 8-byte MCAN header on the initial packet fragment. The PDMA will break up the source packet into fragments of this buffer size, copying the 8-byte MCAN header for the initial fragment, and then skipping it for each additional fragment and thus reusing the header from the first fragment. A buffer size less than 16 is treated as 16, and a buffer size greater than 72 is treated as 72.</p> <p>AASRC mode static TR: FIFO element count. In AASRC mode, a channel can service multiple FIFOs using a list supplied in its FIFO configuration. This field specifies how many times to service the FIFO list, hence how many elements to transfer from each FIFO, each time a trigger is received on the channel. Note for each loop specified by the value of Y, the entire list is processed. For example, if the FIFO list is 0, 1, 2, 3, and Y is set to 2 loops, the FIFOs are serviced in the order: 0, 1, 2, 3, 0, 1, 2, 3.</p>

22.2.4 PDMA_PSILCFG_TX_DEBUG_1 Register (Offset = 402h) [reset = 0h]

PDMA_PSILCFG_TX_DEBUG_1 is shown in [Figure 22-17](#) and described in [Table 22-38](#).

Return to [Summary Table](#).

Debug/State Register 1. The debug/state registers give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations.

Table 22-37. PDMA_PSILCFG_TX_DEBUG_1 Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-17. PDMA_PSILCFG_TX_DEBUG_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
Y							
R/W-0h							
7	6	5	4	3	2	1	0
Y							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-38. PDMA_PSILCFG_TX_DEBUG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	Y	R/W	0h	This field holds the current Y count. In X-Y FIFO mode, this is the number of X sized samples yet to write to the peripheral for the DMA event being serviced. In MCAN mode, this field holds the next write offset to use when writing to the CAN TX buffer.

22.2.5 PDMA_PSILCFG_TX_DEBUG_2 Register (Offset = 403h) [reset = 0h]

PDMA_PSILCFG_TX_DEBUG_2 is shown in [Figure 22-18](#) and described in [Table 22-40](#).

Return to [Summary Table](#).

Debug/State Register 2. The debug/state registers give software applications additional information about the PDMA than they would need in regular operation, but which may be useful in debug situations.

**Table 22-39. PDMA_PSILCFG_TX_DEBUG_2
Instances**

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-18. PDMA_PSILCFG_TX_DEBUG_2 Register

31	30	29	28	27	26	25	24
INEVENT	FLUSH	PAUSE	DATA	XDATA	RESERVED		
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		
23	22	21	20	19	18	17	16
STATE				EVENTCNT			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-40. PDMA_PSILCFG_TX_DEBUG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	INEVENT	R/W	0h	When set, the PDMA is in the middle of processing a FIFO event.
30	FLUSH	R/W	0h	When set, the PDMA is processing in a flushing state, where it runs without waiting for DMA requests and without writing data to the peripheral. It is only operating its internal state machine to allow internal data pipes to drain properly.
29	PAUSE	R/W	0h	When set, the PDMA waiting in a paused state. This bit will clear when data starts flowing again from the UDMA-P.
28	DATA	R/W	0h	When set, there is a non-zero amount of data still waiting to be written to the peripheral.
27	XDATA	R/W	0h	When set, there is enough data still waiting to be written to the peripheral to start servicing a peripheral DMA event.
26-24	RESERVED	R	0h	Reserved
23-20	STATE	R/W	0h	This code reflects the current state of the PDMA channel, and is specific to the current implementation.
19-16	EVENTCNT	R/W	0h	This field holds the number of backlogged DMA events yet to be serviced.
15-0	RESERVED	R	0h	Reserved

22.2.6 PDMA_PSILCFG_TX_BYTE_COUNT Register (Offset = 404h) [reset = 0h]

PDMA_PSILCFG_TX_BYTE_COUNT is shown in [Figure 22-19](#) and described in [Table 22-42](#).

Return to [Summary Table](#).

Byte Count Register. This register contains the number of bytes that have been written to the VBUSP mapped peripheral.

Table 22-41. PDMA_PSILCFG_TX_BYTE_COUNT Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-19. PDMA_PSILCFG_TX_BYTE_COUNT Register

31	30	29	28	27	26	25	24
BYTES							
R/W-0h							
23	22	21	20	19	18	17	16
BYTES							
R/W-0h							
15	14	13	12	11	10	9	8
BYTES							
R/W-0h							
7	6	5	4	3	2	1	0
BYTES							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-42. PDMA_PSILCFG_TX_BYTE_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BYTES	R/W	0h	This register contains the number of bytes that have been read from the VBUSP mapped peripheral. The register is write-to-decrement, so running counts can be tracked by reading register and then writing back the value that was read. It will wrap on overflow. It will reset to zero on a channel reset.

22.2.7 PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG Register (Offset = 405h) [reset = 0h]

PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG is shown in [Figure 22-20](#) and described in [Table 22-44](#).

Return to [Summary Table](#).

AASRC Tx FIFO configuration register.

Table 22-43.
PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG
Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-20. PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG Register

31	30	29	28	27	26	25	24
GROUPMODE	DMAREQRESET	RESERVED					
R/W-0h	R/W-0h	R-0h					
23	22	21	20	19	18	17	16
LASTSLOT				FIRSTSLOT			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
DMAREQMASK							
R/W-0h							
7	6	5	4	3	2	1	0
DMAREQMASK							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-44. PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	GROUPMODE	R/W	0h	When set, the channel is in 'group mode'. It will look for group mode DMA requests, and access the group mode FIFOs. When clear, the channel is 'stream mode'. It will look for stream FIFO DMA requests, and access the stream mode FIFOs.
30	DMAREQRESET	R/W	0h	When set, resets any latched DMA request using the DMAREQMASK. This bit is self-clearing. It should be used to synchronize the AASRC event status with the PDMA in the event that the AASRC has been previously used and it is not known if the PDMA may have latched, and is holding, previous DMA requests.
29-24	RESERVED	R	0h	Reserved
23-20	LASTSLOT	R/W	0h	This is the index (0-15) of the last slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.
19-16	FIRSTSLOT	R/W	0h	This is the index (0-15) of the first slot in the TX FIFO ordering table used by this channel. The ordering table is read to get the FIFO index to access for each slot, starting with the first and ending with the last.

Table 22-44. PDMA_PSILCFG_TX_AASRC_TX_FIFO_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-0	DMAREQMASK	R/W	0h	<p>This field holds a set of flags indicating which AASRC DMA requests must fire in order for this channel to activate.</p> <p>In steam mode, these 16 flags correspond to the 16 DMA requests for each TX FIFO. The flags corresponding to all TX FIFOs involved with the channel should be set to 1.</p> <p>In group mode, these flags indicate which group mode DMA requests must fire. In this case, only bits [3:0] are relevant and only one bit should be set to 1 as a DMA channel only services a single group.</p>

22.2.8 PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0 Register (Offset = 406h) [reset = 0h]

PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0 is shown in [Figure 22-21](#) and described in [Table 22-46](#).

Return to [Summary Table](#).

AASRC TX order table 0 register.

Table 22-45.
PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0
Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-21. PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0 Register

31	30	29	28	27	26	25	24
ENTRY7				ENTRY6			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
ENTRY5				ENTRY4			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
ENTRY3				ENTRY2			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ENTRY1				ENTRY0			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 22-46. PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ENTRY7	R/W	7h	TX FIFO index for slot 7
27-24	ENTRY6	R/W	6h	TX FIFO index for slot 6
23-20	ENTRY5	R/W	5h	TX FIFO index for slot 5
19-16	ENTRY4	R/W	4h	TX FIFO index for slot 4
15-12	ENTRY3	R/W	3h	TX FIFO index for slot 3
11-8	ENTRY2	R/W	2h	TX FIFO index for slot 2
7-4	ENTRY1	R/W	1h	TX FIFO index for slot 1
3-0	ENTRY0	R/W	0h	TX FIFO index for slot 0

22.2.9 PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1 Register (Offset = 407h) [reset = 0h]

PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1 is shown in [Figure 22-22](#) and described in [Table 22-48](#).

Return to [Summary Table](#).

AASRC Tx order table 1 register.

Table 22-47.
PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1
Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-22. PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1 Register

31	30	29	28	27	26	25	24
ENTRY15				ENTRY14			
R/W-0h				R/W-0h			
23	22	21	20	19	18	17	16
ENTRY13				ENTRY12			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
ENTRY11				ENTRY10			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
ENTRY9				ENTRY8			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 22-48. PDMA_PSILCFG_TX_AASRC_TX_ORDER_TABLE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ENTRY15	R/W	Fh	TX FIFO index for slot 15
27-24	ENTRY14	R/W	Eh	TX FIFO index for slot 14
23-20	ENTRY13	R/W	Dh	TX FIFO index for slot 13
19-16	ENTRY12	R/W	Ch	TX FIFO index for slot 12
15-12	ENTRY11	R/W	Bh	TX FIFO index for slot 11
11-8	ENTRY10	R/W	Ah	TX FIFO index for slot 10
7-4	ENTRY9	R/W	9h	TX FIFO index for slot 9
3-0	ENTRY8	R/W	8h	TX FIFO index for slot 8

22.2.10 PDMA_PSILCFG_TX_RT_ENABLE Register (Offset = 408h) [reset = 0h]

PDMA_PSILCFG_TX_RT_ENABLE is shown in [Figure 22-23](#) and described in [Figure 22-23](#).

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Real Time Enable Register. This register allows enabling various channel settings in real time.

Table 22-49. PDMA_PSILCFG_TX_RT_ENABLE Instances

Instance	Physical Address
PDMA_PSILCFG_TX	N/A

Figure 22-23. PDMA_PSILCFG_TX_RT_ENABLE Register

31	30	29	28	27	26	25	24
ENABLE	TDOWN	PAUSE	FLUSH	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ERROR	IDLE	FREE
R-0h					R/W-0h	R-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 22-50. PDMA_PSILCFG_TX_RT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	When set, the TX channel is enabled. When cleared, the TX channel is disabled. When disabled, it discards all held data. It clears DMA event counts and ignores all future DMA events from the peripheral. It maintains data exchange with the UDMA-P so that credit handshake is not disrupted. A 'hard teardown' can be performed by directly clearing this bit. Note that this bit cannot be changed from 0 to 1 if the global enable bit in the peer enable register is 0.
30	TDOWN	R/W	0h	When set, the channel will commence a TX channel teardown procedure. To perform a TX teardown, the teardown bit should be set in the UDMA-P and it will automatically propagate to this register bit with the normal flow of peripheral data. Once the channel is fully stopped and ready to be reused (including returning all credits), the ENABLE bit is cleared.
29	PAUSE	R/W	0h	When set, the channel is in a paused state. It will stop on the next FIFO boundary. It continues to accept and count DMA events from the peripherals but will not act on them. The PAUSE bit can be cleared and data will resume.

Table 22-50. PDMA_PSILCFG_TX_RT_ENABLE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
28	FLUSH	R/W	0h	When set, causes all TX channel data to be discarded instead of being written to the peripheral. It essentially allows the TX engine to 'free run' without DMA requests from the peripheral (it will also override 'pause'). This bit should be set only when a channel fails to complete its teardown procedure normally because a peripheral is no longer functioning or because data flow was halted on a boundary that is not compatible with the static TR configuration.
27-3	RESERVED	R	0h	Reserved
2	ERROR	R/W	0h	When set, the channel has encountered a PSI-L protocol violation. The ERROR bit can only be set by hardware and can only be cleared by software. Once this bit is set, the channel should be fully reset and re-initialized via the PSI-L pairing registers.
1	IDLE	R	0h	This is a read-only bit that signifies that the disabled thread is also idle. This bit is read only and can only become set if the ENABLE bit is cleared.
0	FREE	R/W	0h	When cleared, the channel honors the debug suspend signal. When set, the channel will 'free run', regardless of the value of debug suspend.

22.3 PDMA5 ECC Registers

Table 22-52 lists the memory-mapped registers for the PDMA5. All register offset addresses not listed in Table 22-52 should be considered as reserved locations and the register contents should not be modified.

Table 22-51. PDMA5 Instances

Instance	Base Address
PDMA5_REGS	027E 0000h

Table 22-52. PDMA5 Registers

Offset	Acronym	Register Name	PDMA5_REGS Physical Address
0h	PDMA5_ECC_REV	Aggregator revision register	027E 0000h
8h	PDMA5_ECC_VECTOR	ECC vector register	027E 0008h
Ch	PDMA5_ECC_STAT	Misc status register	027E 000Ch
3Ch	PDMA5_ECC_SEC_EOI_REG	SEC EOI register	027E 003Ch
40h	PDMA5_ECC_SEC_STATUS_REG0	SEC interrupt status register 0	027E 0040h
80h	PDMA5_ECC_SEC_ENABLE_SET_REG0	SEC interrupt enable set register 0	027E 0080h
C0h	PDMA5_ECC_SEC_ENABLE_CLR_REG0	SEC interrupt enable clear register 0	027E 00C0h
13Ch	PDMA5_ECC_DED_EOI_REG	DED EOI register	027E 013Ch
140h	PDMA5_ECC_DED_STATUS_REG0	DED interrupt status register 0	027E 0140h
180h	PDMA5_ECC_DED_ENABLE_SET_REG0	DED interrupt enable set register 0	027E 0180h
1C0h	PDMA5_ECC_DED_ENABLE_CLR_REG0	DED interrupt enable clear register 0	027E 01C0h
200h	PDMA5_ECC_AGGR_ENABLE_SET	AGGR interrupt enable set register	027E 0200h
204h	PDMA5_ECC_AGGR_ENABLE_CLR	AGGR interrupt enable clear register	027E 0204h
208h	PDMA5_ECC_AGGR_STATUS_SET	AGGR interrupt status set register	027E 0208h
20Ch	PDMA5_ECC_AGGR_STATUS_CLR	AGGR interrupt status clear register	027E 020Ch

22.3.1 PDMA5_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

PDMA5_ECC_REV is shown in [Figure 22-24](#) and described in [Table 22-54](#).

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IP revision register.

Table 22-53. PDMA5_ECC_REV Instances

Instance	Physical Address
PDMA5_REGS	027E 0000h

Figure 22-24. PDMA5_ECC_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-66A0EA00h																															

LEGEND: R = Read Only; -n = value after reset

Table 22-54. PDMA5_ECC_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	66A0EA00h	TI internal data. Identifies revision of peripheral.

Table 22-55. Register Call Summary for PDMA5_ECC_REV

PDMA5 ECC Registers

- [PDMA5_ECC_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.2 PDMA5_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

PDMA5_ECC_VECTOR is shown in Figure 22-25 and described in Table 22-57.

Return to [Summary Table](#).

ECC vector register.

Table 22-56. PDMA5_ECC_VECTOR Instances

Instance	Physical Address
PDMA5_REGS	027E 0008h

Figure 22-25. PDMA5_ECC_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R-0h							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R-0h				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-57. PDMA5_ECC_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R	0h	Reserved
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

Table 22-58. Register Call Summary for PDMA5_ECC_VECTOR

PDMA5 ECC Registers
<ul style="list-style-type: none"> PDMA5 ECC Registers: [0] PDMA5_ECC_VECTOR Register (Offset = 8h) [reset = 0h]: [0]

22.3.3 PDMA5_ECC_STAT Register (Offset = Ch) [reset = 4h]

PDMA5_ECC_STAT is shown in [Figure 22-26](#) and described in [Table 22-60](#).

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Misc status register.

Table 22-59. PDMA5_ECC_STAT Instances

Instance	Physical Address
PDMA5_REGS	027E 000Ch

Figure 22-26. PDMA5_ECC_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												NUM_RAMs																			
R-0h												R-4h																			

LEGEND: R = Read Only; -n = value after reset

Table 22-60. PDMA5_ECC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-0	NUM_RAMs	R	4h	Indicates the number of RAMs serviced by the ECC aggregator

Table 22-61. Register Call Summary for PDMA5_ECC_STAT

PDMA5 ECC Registers

- [PDMA5_ECC_STAT Register \(Offset = Ch\) \[reset = 4h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.4 PDMA5_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

PDMA5_ECC_SEC_EOI_REG is shown in Figure 22-27 and described in Table 22-63.

Return to [Summary Table](#).

SEC EOI register. The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 22-62. PDMA5_ECC_SEC_EOI_REG Instances

Instance	Physical Address
PDMA5_REGS	027E 003Ch

Figure 22-27. PDMA5_ECC_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-63. PDMA5_ECC_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI value

Table 22-64. Register Call Summary for PDMA5_ECC_SEC_EOI_REG

PDMA5 ECC Registers

- [PDMA5 ECC Registers: \[0\]](#)
- [PDMA5_ECC_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = 0h\]: \[0\]](#)

22.3.5 PDMA5_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

PDMA5_ECC_SEC_STATUS_REG0 is shown in [Figure 22-28](#) and described in [Table 22-66](#).

Return to [Summary Table](#).

SEC interrupt status register 0.

**Table 22-65. PDMA5_ECC_SEC_STATUS_REG0
Instances**

Instance	Physical Address
PDMA5_REGS	027E 0040h

Figure 22-28. PDMA5_ECC_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAME CC_PEND	RPCF0_RAME CC_PEND	TPCF1_RAME CC_PEND	TPCF0_RAME CC_PEND
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-66. PDMA5_ECC_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1S	0h	Interrupt pending status for rpcf1_amecc_pend
2	RPCF0_RAMECC_PEND	R/W1S	0h	Interrupt pending status for rpcf0_amecc_pend
1	TPCF1_RAMECC_PEND	R/W1S	0h	Interrupt pending status for tpcf1_amecc_pend
0	TPCF0_RAMECC_PEND	R/W1S	0h	Interrupt pending status for tpcf0_amecc_pend

Table 22-67. Register Call Summary for PDMA5_ECC_SEC_STATUS_REG0

PDMA5 ECC Registers

- [PDMA5_ECC_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = 0h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.6 PDMA5_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

PDMA5_ECC_SEC_ENABLE_SET_REG0 is shown in Figure 22-29 and described in Table 22-69.

Return to [Summary Table](#).

SEC interrupt enable set register 0.

Table 22-68.
PDMA5_ECC_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
PDMA5_REGS	027E 0080h

Figure 22-29. PDMA5_ECC_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAME CC_ENABLE_S ET	RPCF0_RAME CC_ENABLE_S ET	TPCF1_RAME CC_ENABLE_S ET	TPCF0_RAME CC_ENABLE_S ET
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-69. PDMA5_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for rpcf1_amecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for rpcf0_amecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for tpcf1_amecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for tpcf0_amecc_pend

Table 22-70. Register Call Summary for PDMA5_ECC_SEC_ENABLE_SET_REG0

PDMA5 ECC Registers

- [PDMA5_ECC_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = 0h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.7 PDMA5_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

PDMA5_ECC_SEC_ENABLE_CLR_REG0 is shown in Figure 22-30 and described in Table 22-72.

Return to [Summary Table](#).

SEC interrupt enable clear register 0.

Table 22-71.
PDMA5_ECC_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PDMA5_REGS	027E 00C0h

Figure 22-30. PDMA5_ECC_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAME CC_ENABLE_C LR	RPCF0_RAME CC_ENABLE_C LR	TPCF1_RAME CC_ENABLE_C LR	TPCF0_RAME CC_ENABLE_C LR
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 22-72. PDMA5_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	0h	Reserved
3	RPCF1_RAMECC_ENAB LE_CLR	R/W1C	0h	Interrupt enable clear register for rpcf1_amecc_pend
2	RPCF0_RAMECC_ENAB LE_CLR	R/W1C	0h	Interrupt enable clear register for rpcf0_amecc_pend
1	TPCF1_RAMECC_ENABL E_CLR	R/W1C	0h	Interrupt enable clear register for tpcf1_amecc_pend
0	TPCF0_RAMECC_ENABL E_CLR	R/W1C	0h	Interrupt enable clear register for tpcf0_amecc_pend

Table 22-73. Register Call Summary for PDMA5_ECC_SEC_ENABLE_CLR_REG0

PDMA5 ECC Registers

- [PDMA5 ECC Registers: \[0\]](#)
- [PDMA5_ECC_SEC_ENABLE_CLR_REG0 Register \(Offset = C0h\) \[reset = 0h\]: \[0\]](#)

22.3.8 PDMA5_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

PDMA5_ECC_DED_EOI_REG is shown in [Figure 22-31](#) and described in [Table 22-75](#).

Return to [Summary Table](#).

DED EOI register. The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 22-74. PDMA5_ECC_DED_EOI_REG Instances

Instance	Physical Address
PDMA5_REGS	027E 013Ch

Figure 22-31. PDMA5_ECC_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R-0h							R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-75. PDMA5_ECC_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	0h	Reserved
0	EOI_WR	R/W1S	0h	EOI value

Table 22-76. Register Call Summary for PDMA5_ECC_DED_EOI_REG

PDMA5 ECC Registers

- [PDMA5 ECC Registers: \[0\]](#)
- [PDMA5_ECC_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = 0h\]: \[0\]](#)

22.3.9 PDMA5_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

PDMA5_ECC_DED_STATUS_REG0 is shown in [Figure 22-32](#) and described in [Table 22-78](#).

Return to [Summary Table](#).

DED interrupt status register 0.

**Table 22-77. PDMA5_ECC_DED_STATUS_REG0
Instances**

Instance	Physical Address
PDMA5_REGS	027E 0140h

Figure 22-32. PDMA5_ECC_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAME CC_PEND	RPCF0_RAME CC_PEND	TPCF1_RAME CC_PEND	TPCF0_RAME CC_PEND
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-78. PDMA5_ECC_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RPCF1_RAMECC_PEND	R/W1S	0h	Interrupt pending status for rpcf1_amecc_pend
2	RPCF0_RAMECC_PEND	R/W1S	0h	Interrupt pending status for rpcf0_amecc_pend
1	TPCF1_RAMECC_PEND	R/W1S	0h	Interrupt pending status for tpcf1_amecc_pend
0	TPCF0_RAMECC_PEND	R/W1S	0h	Interrupt pending status for tpcf0_amecc_pend

Table 22-79. Register Call Summary for PDMA5_ECC_DED_STATUS_REG0

PDMA5 ECC Registers

- [PDMA5_ECC_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = 0h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.10 PDMA5_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

PDMA5_ECC_DED_ENABLE_SET_REG0 is shown in Figure 22-33 and described in Table 22-81.

Return to [Summary Table](#).

DED interrupt enable set register 0.

Table 22-80.
PDMA5_ECC_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
PDMA5_REGS	027E 0180h

Figure 22-33. PDMA5_ECC_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAMECC_ENABLE_SET	RPCF0_RAMECC_ENABLE_SET	TPCF1_RAMECC_ENABLE_SET	TPCF0_RAMECC_ENABLE_SET
R-0h				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-81. PDMA5_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for rpcf1_amecc_pend
2	RPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for rpcf0_amecc_pend
1	TPCF1_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for tpcf1_amecc_pend
0	TPCF0_RAMECC_ENABLE_SET	R/W1S	0h	Interrupt enable set register for tpcf0_amecc_pend

Table 22-82. Register Call Summary for PDMA5_ECC_DED_ENABLE_SET_REG0

PDMA5 ECC Registers

- [PDMA5_ECC_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = 0h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.11 PDMA5_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

PDMA5_ECC_DED_ENABLE_CLR_REG0 is shown in Figure 22-34 and described in Table 22-84.

Return to [Summary Table](#).

DED interrupt enable clear register 0.

Table 22-83.
PDMA5_ECC_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
PDMA5_REGS	027E 01C0h

Figure 22-34. PDMA5_ECC_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				RPCF1_RAME CC_ENABLE_C LR	RPCF0_RAME CC_ENABLE_C LR	TPCF1_RAME CC_ENABLE_C LR	TPCF0_RAME CC_ENABLE_C LR
R-0h				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 22-84. PDMA5_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	RPCF1_RAMECC_ENAB LE_CLR	R/W1C	0h	Interrupt enable clear register for rpcf1_amecc_pend
2	RPCF0_RAMECC_ENAB LE_CLR	R/W1C	0h	Interrupt enable clear register for rpcf0_amecc_pend
1	TPCF1_RAMECC_ENABL E_CLR	R/W1C	0h	Interrupt enable clear register for tpcf1_amecc_pend
0	TPCF0_RAMECC_ENABL E_CLR	R/W1C	0h	Interrupt enable clear register for tpcf0_amecc_pend

Table 22-85. Register Call Summary for PDMA5_ECC_DED_ENABLE_CLR_REG0

PDMA5 ECC Registers

- [PDMA5 ECC Registers: \[0\]](#)
- [PDMA5_ECC_DED_ENABLE_CLR_REG0 Register \(Offset = 1C0h\) \[reset = 0h\]: \[0\]](#)

22.3.12 PDMA5_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

PDMA5_ECC_AGGR_ENABLE_SET is shown in Figure 22-35 and described in Table 22-87.

Return to [Summary Table](#).

AGGR interrupt enable set register.

Table 22-86. PDMA5_ECC_AGGR_ENABLE_SET Instances

Instance	Physical Address
PDMA5_REGS	027E 0200h

Figure 22-35. PDMA5_ECC_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1S-0h	R/W1S-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 22-87. PDMA5_ECC_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1S	0h	Interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	Interrupt enable set for parity errors

Table 22-88. Register Call Summary for PDMA5_ECC_AGGR_ENABLE_SET

PDMA5 ECC Registers

- [PDMA5 ECC Registers: \[0\]](#)
- [PDMA5_ECC_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = 0h\]: \[0\]](#)

22.3.13 PDMA5_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

PDMA5_ECC_AGGR_ENABLE_CLR is shown in [Figure 22-36](#) and described in [Table 22-90](#).

Return to [Summary Table](#).

AGGR interrupt enable clear register.

**Table 22-89. PDMA5_ECC_AGGR_ENABLE_CLR
Instances**

Instance	Physical Address
PDMA5_REGS	027E 0204h

Figure 22-36. PDMA5_ECC_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R-0h						R/W1C-0h	R/W1C-0h

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 22-90. PDMA5_ECC_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1	TIMEOUT	R/W1C	0h	Interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	Interrupt enable clear for parity errors

Table 22-91. Register Call Summary for PDMA5_ECC_AGGR_ENABLE_CLR

PDMA5 ECC Registers

- [PDMA5_ECC_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = 0h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.14 PDMA5_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

PDMA5_ECC_AGGR_STATUS_SET is shown in [Figure 22-37](#) and described in [Table 22-93](#).

Return to [Summary Table](#).

AGGR interrupt status set register.

Table 22-92. PDMA5_ECC_AGGR_STATUS_SET Instances

Instance	Physical Address
PDMA5_REGS	027E 0208h

Figure 22-37. PDMA5_ECC_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wincr-0h		R/Wincr-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 22-93. PDMA5_ECC_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wincr	0h	Interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	Interrupt status set for parity errors

Table 22-94. Register Call Summary for PDMA5_ECC_AGGR_STATUS_SET

PDMA5 ECC Registers

- [PDMA5_ECC_AGGR_STATUS_SET Register \(Offset = 208h\) \[reset = 0h\]: \[0\]](#)
- [PDMA5 ECC Registers: \[0\]](#)

22.3.15 PDMA5_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

PDMA5_ECC_AGGR_STATUS_CLR is shown in Figure 22-38 and described in Table 22-96.

Return to [Summary Table](#).

AGGR interrupt status clear register.

**Table 22-95. PDMA5_ECC_AGGR_STATUS_CLR
Instances**

Instance	Physical Address
PDMA5_REGS	027E 020Ch

Figure 22-38. PDMA5_ECC_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R-0h				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R = Read Only; R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 22-96. PDMA5_ECC_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-2	TIMEOUT	R/Wdecr	0h	Interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	Interrupt status clear for parity errors

Table 22-97. Register Call Summary for PDMA5_ECC_AGGR_STATUS_CLR

PDMA5 ECC Registers

- [PDMA5 ECC Registers: \[0\]](#)
- [PDMA5_ECC_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = 0h\]: \[0\]](#)

23 DRU Registers

Table 23-2 lists the DRU configuration registers. All register offset addresses not listed in Table 23-2 should be considered as reserved locations and the register contents should not be modified.

Table 23-1. DRU Instances

Instance	Base Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 0000h

Table 23-2. DRU Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU Physical Address
0h	DRU_PID	Peripheral ID Register	6D00 0000h
8h	DRU_CAPABILITIES	DRU Capabilities Register	6D00 0008h
4000h	DRU_SHARED_EVT_SET	DRU Shared Event Set Register	6D00 4000h
4040h	DRU_COMP_EVT_SET0	DRU Completion Event Set Register	6D00 4040h
4080h	DRU_ERR_EVT_SET0	DRU Error Event Set Register	6D00 4080h
40C0h	DRU_LOCAL_EVT_SET0	DRU Local Event Set Register	6D00 40C0h
8000h + formula	DRU_CFG_y	Configuration Register for Queue "y"	6D00 8000h
8040h + formula	DRU_STATUS_y	Status Register for Queue "y"	6D00 8040h
40000h + formula	DRU_CFG_j	Channel Configuration Register	6D04 0000h
40020h + formula	DRU_CHOES0_j	Output Event Steering Register	6D04 0020h
40060h + formula	DRU_CHST_SCHED_j	Channel Static Scheduler Config Register	6D04 0060h
60000h + formula	DRU_CHRT_CTL_j	Channel Realtime Control Register	6D06 0000h
60008h + formula	DRU_CHRT_SWTRIG_j	Software Trigger Register	6D06 0008h
60010h + formula	DRU_CHRT_STATUS_DET_j	Channel Status Details Register	6D06 0010h
60018h + formula	DRU_CHRT_STATUS_CNT_j	Channel Count Details Register	6D06 0018h
80000h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j	The first TR submission word	6D08 0000h
80008h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j	The second TR submission word	6D08 0008h
80010h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j	The third TR submission word	6D08 0010h
80018h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j	The fourth TR submission word	6D08 0018h
80020h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j	The fifth TR submission word	6D08 0020h
80028h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j	The sixth TR submission word	6D08 0028h
80030h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j	The seventh TR submission word	6D08 0030h
80038h + formula	DRU_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j	The eight TR submission word	6D08 0038h
80040h + formula	DRU_NEXT_TR_WORD0_1_j_k	The first TR submission word	6D08 0040h

Table 23-2. DRU Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_MMR_DRU_MM R_CFG_DRU Physical Address
80048h + formula	DRU_NEXT_TR_WORD2_3_j_k	The second TR submission word	6D08 0048h
80050h + formula	DRU_NEXT_TR_WORD4_5_j_k	The third TR submission word	6D08 0050h
80058h + formula	DRU_NEXT_TR_WORD6_7_j_k	The fourth TR submission word	6D08 0058h
80060h + formula	DRU_NEXT_TR_WORD8_9_j_k	The fifth TR submission word	6D08 0060h
80068h + formula	DRU_NEXT_TR_WORD10_11_j_k	The sixth TR submission word	6D08 0068h
80070h + formula	DRU_NEXT_TR_WORD12_13_j_k	The seventh TR submission word	6D08 0070h
80078h + formula	DRU_NEXT_TR_WORD14_15_j_k	The eight TR submission word	6D08 0078h
A0000h + formula	DRU_SUBMIT_WORD0_1_j_k	The first TR submission word	6D0A 0000h
A0008h + formula	DRU_SUBMIT_WORD2_3_j_k	The second TR submission word	6D0A 0008h
A0010h + formula	DRU_SUBMIT_WORD4_5_j_k	The third TR submission word	6D0A 0010h
A0018h + formula	DRU_SUBMIT_WORD6_7_j_k	The fourth TR submission word	6D0A 0018h
A0020h + formula	DRU_SUBMIT_WORD8_9_j_k	The fifth TR submission word	6D0A 0020h
A0028h + formula	DRU_SUBMIT_WORD10_11_j_k	The sixth TR submission word	6D0A 0028h
A0030h + formula	DRU_SUBMIT_WORD12_13_j_k	The seventh TR submission word	6D0A 0030h
A0038h + formula	DRU_SUBMIT_WORD14_15_j_k	The eight TR submission word	6D0A 0038h
E0000h + formula	DRU_CAUSE_y	Error Register cause for channels 0 + (16*y) to 15 + (16*y)	6D0E 0000h

23.1 DRU_PID Register (Offset = 0h) [reset = 662C0900h]

DRU_PID is shown in [Figure 23-1](#) and described in [Table 23-4](#).

Return to [Summary Table](#).

Peripheral ID Register

Table 23-3. DRU_PID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D00 0000h

Figure 23-1. DRU_PID Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																															
R-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVISION																															
R-662C0900h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-4. DRU_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RSVD	R	0h	Reserved
31-0	REVISION	R	662C0900h	PID Revision

23.2 DRU_CAPABILITIES Register (Offset = 8h) [reset = 959000D0F20h]

DRU_CAPABILITIES is shown in [Figure 23-2](#) and described in [Table 23-6](#).

Return to [Summary Table](#).

DRU Capabilities: Lists the capabilities of the channel for TR TYPE and formatting functions

Table 23-5. DRU_CAPABILITIES Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 0008h

Figure 23-2. DRU_CAPABILITIES Register

63	62	61	60	59	58	57	56
RSVD							
R-0h							
55	54	53	52	51	50	49	48
RSVD							
R-0h							
47	46	45	44	43	42	41	40
RSVD	SECTR			DFMT			
R-0h	R-1h			R-2h			
39	38	37	36	35	34	33	32
DFMT	ELTYPE			AMODE			
R-2h	R-Bh			R-1h			
31	30	29	28	27	26	25	24
RSVD_CONF_SPEC							
R-0h							
23	22	21	20	19	18	17	16
RSVD_CONF_SPEC				GLOBAL_TRIG	LOCAL_TRIG	EOL	TRSTATIC
R-0h				R-1h	R-1h	R-0h	R-1h
15	14	13	12	11	10	9	8
TYPE15	TYPE14	TYPE13	TYPE12	TYPE11	TYPE10	TYPE9	TYPE8
R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-1h	R-1h
7	6	5	4	3	2	1	0
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R-0h	R-0h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 23-6. DRU_CAPABILITIES Register Field Descriptions

Bit	Field	Type	Reset	Description
63-47	RSVD	R	0h	Reserved
46-43	SECTR	R	1h	Maximum second TR function that is supported
42-39	DFMT	R	2h	Maximum data reformatting function that is supported
38-35	ELTYPE	R	Bh	Maximum element type value that is supported
34-32	AMODE	R	1h	The maximum AMODE that is supported. If AMODE is supported then DIR field must be supported for that AMODE.
31-20	RSVD_CONF_SPEC	R	0h	Reserved for Configuration Specific Features. This implementation has no configuration specific features.

Table 23-6. DRU_CAPABILITIES Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19	GLOBAL_TRIG	R	1h	Global Triggers 0 and 1 are supported
18	LOCAL_TRIG	R	1h	Dedicated Local Trigger is supported
17	EOL	R	0h	EOL Field is supported
16	TRSTATIC	R	1h	STATIC Field is supported
15	TYPE15	R	0h	Type 15 TR is supported
14	TYPE14	R	0h	Type 14 TR is supported
13	TYPE13	R	0h	Type 13 TR is supported
12	TYPE12	R	0h	Type 12 TR is supported
11	TYPE11	R	1h	Type 11 TR is supported
10	TYPE10	R	1h	Type 10 TR is supported
9	TYPE9	R	1h	Type 9 TR is supported
8	TYPE8	R	1h	Type 8 TR is supported
7	TYPE7	R	0h	Type 7 TR is supported
6	TYPE6	R	0h	Type 6 TR is supported
5	TYPE5	R	1h	Type 5 TR is supported
4	TYPE4	R	0h	Type 4 TR is supported
3	TYPE3	R	0h	Type 3 TR is supported
2	TYPE2	R	0h	Type 2 TR is supported
1	TYPE1	R	0h	Type 1 TR is supported
0	TYPE0	R	0h	Type 0 TR is supported

23.3 DRU_SHARED_EVT_SET Register (Offset = 4000h) [reset = X]

DRU_SHARED_EVT_SET is shown in [Figure 23-3](#) and described in [Table 23-8](#).

Return to [Summary Table](#).

DRU Shared Event Set Register

Table 23-7. DRU_SHARED_EVT_SET Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 4000h

Figure 23-3. DRU_SHARED_EVT_SET Register

63	62	61	60	59	58	57	56
RSVD							
R-X							
55	54	53	52	51	50	49	48
RSVD							
R-X							
47	46	45	44	43	42	41	40
RSVD							
R-X							
39	38	37	36	35	34	33	32
RSVD							
R-X							
31	30	29	28	27	26	25	24
RSVD							
R-X							
23	22	21	20	19	18	17	16
RSVD							
R-X							
15	14	13	12	11	10	9	8
RSVD							
R-X							
7	6	5	4	3	2	1	0
RSVD							PROT_ERR
R-X							W-0h

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 23-8. DRU_SHARED_EVT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
63-1	RSVD	R	X	Reserved
0	PROT_ERR	W	0h	Set the protocol error event

23.4 DRU_COMP_EVT_SET0 Register (Offset = 4040h) [reset = 0h]

DRU_COMP_EVT_SET0 is shown in [Figure 23-4](#) and described in [Table 23-10](#).

Return to [Summary Table](#).

DRU Completion Event Set Register

Table 23-9. DRU_COMP_EVT_SET0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 4040h

Figure 23-4. DRU_COMP_EVT_SET0 Register

63	62	61	60	59	58	57	56
RESERVED							
W-0h							
55	54	53	52	51	50	49	48
RESERVED							
W-0h							
47	46	45	44	43	42	41	40
RESERVED							
W-0h							
39	38	37	36	35	34	33	32
RESERVED							
W-0h							
31	30	29	28	27	26	25	24
COMP_EVT31	COMP_EVT30	COMP_EVT29	COMP_EVT28	COMP_EVT27	COMP_EVT26	COMP_EVT25	COMP_EVT24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
COMP_EVT23	COMP_EVT22	COMP_EVT21	COMP_EVT20	COMP_EVT19	COMP_EVT18	COMP_EVT17	COMP_EVT16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
COMP_EVT15	COMP_EVT14	COMP_EVT13	COMP_EVT12	COMP_EVT11	COMP_EVT10	COMP_EVT9	COMP_EVT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
COMP_EVT7	COMP_EVT6	COMP_EVT5	COMP_EVT4	COMP_EVT3	COMP_EVT2	COMP_EVT1	COMP_EVT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 23-10. DRU_COMP_EVT_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	W	0h	
31	COMP_EVT31	W	0h	Set the Completion Event for channel 31
30	COMP_EVT30	W	0h	Set the Completion Event for channel 30
29	COMP_EVT29	W	0h	Set the Completion Event for channel 29
28	COMP_EVT28	W	0h	Set the Completion Event for channel 28
27	COMP_EVT27	W	0h	Set the Completion Event for channel 27
26	COMP_EVT26	W	0h	Set the Completion Event for channel 26
25	COMP_EVT25	W	0h	Set the Completion Event for channel 25

Table 23-10. DRU_COMP_EVT_SET0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	COMP_EVT24	W	0h	Set the Completion Event for channel 24
23	COMP_EVT23	W	0h	Set the Completion Event for channel 23
22	COMP_EVT22	W	0h	Set the Completion Event for channel 22
21	COMP_EVT21	W	0h	Set the Completion Event for channel 21
20	COMP_EVT20	W	0h	Set the Completion Event for channel 20
19	COMP_EVT19	W	0h	Set the Completion Event for channel 19
18	COMP_EVT18	W	0h	Set the Completion Event for channel 18
17	COMP_EVT17	W	0h	Set the Completion Event for channel 17
16	COMP_EVT16	W	0h	Set the Completion Event for channel 16
15	COMP_EVT15	W	0h	Set the Completion Event for channel 15
14	COMP_EVT14	W	0h	Set the Completion Event for channel 14
13	COMP_EVT13	W	0h	Set the Completion Event for channel 13
12	COMP_EVT12	W	0h	Set the Completion Event for channel 12
11	COMP_EVT11	W	0h	Set the Completion Event for channel 11
10	COMP_EVT10	W	0h	Set the Completion Event for channel 10
9	COMP_EVT9	W	0h	Set the Completion Event for channel 9
8	COMP_EVT8	W	0h	Set the Completion Event for channel 8
7	COMP_EVT7	W	0h	Set the Completion Event for channel 7
6	COMP_EVT6	W	0h	Set the Completion Event for channel 6
5	COMP_EVT5	W	0h	Set the Completion Event for channel 5
4	COMP_EVT4	W	0h	Set the Completion Event for channel 4
3	COMP_EVT3	W	0h	Set the Completion Event for channel 3
2	COMP_EVT2	W	0h	Set the Completion Event for channel 2
1	COMP_EVT1	W	0h	Set the Completion Event for channel 1
0	COMP_EVT0	W	0h	Set the Completion Event for channel 0

23.5 DRU_ERR_EVT_SET0 Register (Offset = 4080h) [reset = 0h]

DRU_ERR_EVT_SET0 is shown in [Figure 23-5](#) and described in [Table 23-12](#).

Return to [Summary Table](#).

DRU Error Event Set Register

Table 23-11. DRU_ERR_EVT_SET0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 4080h

Figure 23-5. DRU_ERR_EVT_SET0 Register

63	62	61	60	59	58	57	56
RESERVED							
W-0h							
55	54	53	52	51	50	49	48
RESERVED							
W-0h							
47	46	45	44	43	42	41	40
RESERVED							
W-0h							
39	38	37	36	35	34	33	32
RESERVED							
W-0h							
31	30	29	28	27	26	25	24
ERR_EVT31	ERR_EVT30	ERR_EVT29	ERR_EVT28	ERR_EVT27	ERR_EVT26	ERR_EVT25	ERR_EVT24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
ERR_EVT23	ERR_EVT22	ERR_EVT21	ERR_EVT20	ERR_EVT19	ERR_EVT18	ERR_EVT17	ERR_EVT16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
ERR_EVT15	ERR_EVT14	ERR_EVT13	ERR_EVT12	ERR_EVT11	ERR_EVT10	ERR_EVT9	ERR_EVT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
ERR_EVT7	ERR_EVT6	ERR_EVT5	ERR_EVT4	ERR_EVT3	ERR_EVT2	ERR_EVT1	ERR_EVT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 23-12. DRU_ERR_EVT_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	W	0h	
31	ERR_EVT31	W	0h	Set the Error Event for channel 31
30	ERR_EVT30	W	0h	Set the Error Event for channel 30
29	ERR_EVT29	W	0h	Set the Error Event for channel 29
28	ERR_EVT28	W	0h	Set the Error Event for channel 28
27	ERR_EVT27	W	0h	Set the Error Event for channel 27
26	ERR_EVT26	W	0h	Set the Error Event for channel 26
25	ERR_EVT25	W	0h	Set the Error Event for channel 25

Table 23-12. DRU_ERR_EVT_SET0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	ERR_EVT24	W	0h	Set the Error Event for channel 24
23	ERR_EVT23	W	0h	Set the Error Event for channel 23
22	ERR_EVT22	W	0h	Set the Error Event for channel 22
21	ERR_EVT21	W	0h	Set the Error Event for channel 21
20	ERR_EVT20	W	0h	Set the Error Event for channel 20
19	ERR_EVT19	W	0h	Set the Error Event for channel 19
18	ERR_EVT18	W	0h	Set the Error Event for channel 18
17	ERR_EVT17	W	0h	Set the Error Event for channel 17
16	ERR_EVT16	W	0h	Set the Error Event for channel 16
15	ERR_EVT15	W	0h	Set the Error Event for channel 15
14	ERR_EVT14	W	0h	Set the Error Event for channel 14
13	ERR_EVT13	W	0h	Set the Error Event for channel 13
12	ERR_EVT12	W	0h	Set the Error Event for channel 12
11	ERR_EVT11	W	0h	Set the Error Event for channel 11
10	ERR_EVT10	W	0h	Set the Error Event for channel 10
9	ERR_EVT9	W	0h	Set the Error Event for channel 9
8	ERR_EVT8	W	0h	Set the Error Event for channel 8
7	ERR_EVT7	W	0h	Set the Error Event for channel 7
6	ERR_EVT6	W	0h	Set the Error Event for channel 6
5	ERR_EVT5	W	0h	Set the Error Event for channel 5
4	ERR_EVT4	W	0h	Set the Error Event for channel 4
3	ERR_EVT3	W	0h	Set the Error Event for channel 3
2	ERR_EVT2	W	0h	Set the Error Event for channel 2
1	ERR_EVT1	W	0h	Set the Error Event for channel 1
0	ERR_EVT0	W	0h	Set the Error Event for channel 0

23.6 DRU_LOCAL_EVT_SET0 Register (Offset = 40C0h) [reset = 0h]

DRU_LOCAL_EVT_SET0 is shown in [Figure 23-6](#) and described in [Table 23-14](#).

Return to [Summary Table](#).

DRU Local Event Set Register

Table 23-13. DRU_LOCAL_EVT_SET0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 40C0h

Figure 23-6. DRU_LOCAL_EVT_SET0 Register

63	62	61	60	59	58	57	56
RESERVED							
W-0h							
55	54	53	52	51	50	49	48
RESERVED							
W-0h							
47	46	45	44	43	42	41	40
RESERVED							
W-0h							
39	38	37	36	35	34	33	32
RESERVED							
W-0h							
31	30	29	28	27	26	25	24
COMP_EVT31	COMP_EVT30	COMP_EVT29	COMP_EVT28	COMP_EVT27	COMP_EVT26	COMP_EVT25	COMP_EVT24
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
23	22	21	20	19	18	17	16
COMP_EVT23	COMP_EVT22	COMP_EVT21	COMP_EVT20	COMP_EVT19	COMP_EVT18	COMP_EVT17	COMP_EVT16
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
COMP_EVT15	COMP_EVT14	COMP_EVT13	COMP_EVT12	COMP_EVT11	COMP_EVT10	COMP_EVT9	COMP_EVT8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
COMP_EVT7	COMP_EVT6	COMP_EVT5	COMP_EVT4	COMP_EVT3	COMP_EVT2	COMP_EVT1	COMP_EVT0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: W = Write Only; -n = value after reset

Table 23-14. DRU_LOCAL_EVT_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RESERVED	W	0h	
31	COMP_EVT31	W	0h	Set the Local Event for channel 31
30	COMP_EVT30	W	0h	Set the Local Event for channel 30
29	COMP_EVT29	W	0h	Set the Local Event for channel 29
28	COMP_EVT28	W	0h	Set the Local Event for channel 28
27	COMP_EVT27	W	0h	Set the Local Event for channel 27
26	COMP_EVT26	W	0h	Set the Local Event for channel 26
25	COMP_EVT25	W	0h	Set the Local Event for channel 25

Table 23-14. DRU_LOCAL_EVT_SET0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
24	COMP_EVT24	W	0h	Set the Local Event for channel 24
23	COMP_EVT23	W	0h	Set the Local Event for channel 23
22	COMP_EVT22	W	0h	Set the Local Event for channel 22
21	COMP_EVT21	W	0h	Set the Local Event for channel 21
20	COMP_EVT20	W	0h	Set the Local Event for channel 20
19	COMP_EVT19	W	0h	Set the Local Event for channel 19
18	COMP_EVT18	W	0h	Set the Local Event for channel 18
17	COMP_EVT17	W	0h	Set the Local Event for channel 17
16	COMP_EVT16	W	0h	Set the Local Event for channel 16
15	COMP_EVT15	W	0h	Set the Local Event for channel 15
14	COMP_EVT14	W	0h	Set the Local Event for channel 14
13	COMP_EVT13	W	0h	Set the Local Event for channel 13
12	COMP_EVT12	W	0h	Set the Local Event for channel 12
11	COMP_EVT11	W	0h	Set the Local Event for channel 11
10	COMP_EVT10	W	0h	Set the Local Event for channel 10
9	COMP_EVT9	W	0h	Set the Local Event for channel 9
8	COMP_EVT8	W	0h	Set the Local Event for channel 8
7	COMP_EVT7	W	0h	Set the Local Event for channel 7
6	COMP_EVT6	W	0h	Set the Local Event for channel 6
5	COMP_EVT5	W	0h	Set the Local Event for channel 5
4	COMP_EVT4	W	0h	Set the Local Event for channel 4
3	COMP_EVT3	W	0h	Set the Local Event for channel 3
2	COMP_EVT2	W	0h	Set the Local Event for channel 2
1	COMP_EVT1	W	0h	Set the Local Event for channel 1
0	COMP_EVT0	W	0h	Set the Local Event for channel 0

23.7 DRU_CFG_y Register (Offset = 8000h + formula) [reset = X]

DRU_CFG_y is shown in [Figure 23-7](#) and described in [Table 23-16](#).

Return to [Summary Table](#).

Configuration Register for Queue "y"

Offset = 8000h + (y * 8h); where y = 0h to 4h

Table 23-15. DRU_CFG_y Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 8000h

Figure 23-7. DRU_CFG_y Register

63	62	61	60	59	58	57	56
RSVD							
R-0h							
55	54	53	52	51	50	49	48
RSVD							
R-0h							
47	46	45	44	43	42	41	40
RSVD							
R-0h							
39	38	37	36	35	34	33	32
RSVD							
R-0h							
31	30	29	28	27	26	25	24
REARB_WAIT							
R/W-0h							
23	22	21	20	19	18	17	16
CONSECUTIVE_TRANS							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED					QOS		
R/W-X					R/W-0h		
7	6	5	4	3	2	1	0
ORDERID				RESERVED	PRI		
R/W-0h				R/W-X	R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-16. DRU_CFG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RSVD	R	0h	Reserved.
31-24	REARB_WAIT	R/W	0h	This is the number of commands that will be sent by other queues before allowing the queue to arbitrate again for the right to send commands. This is only started when a queue exhausted its consecutive trans count.

Table 23-16. DRU_CFG_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-16	CONSECUTIVE_TRANS	R/W	0h	This is the number of consecutive transactions that will be sent before allowing another queue of equal level to arbitrate to send commands. This is the maximum number of commands that it can send. If the queue has any delays such as virtual address lookup then the arbitration will be forced regardless of the number of commands.
15-11	RESERVED	R/W	X	Reserved.
10-8	QOS	R/W	0h	This configures the QoS for Queue "y". This should only be set for fixed priority queues and the lower queue should have the lower QoS.
7-4	ORDERID	R/W	0h	This configures the Order ID for Queue "y".
3	RESERVED	R/W	X	Reserved.
2-0	PRI	R/W	0h	This configures the priority for Queue "y". This will be the priority that will be presented on the External bus for all commands from this queue.

23.8 DRU_STATUS_y Register (Offset = 8040h + formula) [reset = 0h]

DRU_STATUS_y is shown in [Figure 23-8](#) and described in [Table 23-18](#).

Return to [Summary Table](#).

Status Register for Queue "y"

Offset = 8040h + (y * 8h); where y = 0h to 4h

Table 23-17. DRU_STATUS_y Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D00 8040h

Figure 23-8. DRU_STATUS_y Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32				
RSVD																																RD_TOTAL			
R-0h																																R-0h			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
RD_TOTAL								RD_TOP								WR_TOTAL								WR_TOP											
R-0h								R-0h								R-0h								R-0h											

LEGEND: R = Read Only; -n = value after reset

Table 23-18. DRU_STATUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
63-36	RSVD	R	0h	Reserved
35-27	RD_TOTAL	R	0h	This is the channel that the read half is currently working on.
26-18	RD_TOP	R	0h	This is the channel that the read half is currently working on.
17-9	WR_TOTAL	R	0h	This is the channel that the write half is currently working on.
8-0	WR_TOP	R	0h	This is the channel that the write half is currently working on.

23.9 DRU_CFG_j Register (Offset = 40000h + formula) [reset = X]

DRU_CFG_j is shown in [Figure 23-9](#) and described in [Table 23-20](#).

Return to [Summary Table](#).

Channel Configuration Register. The Channel Configuration Register is used to initialize static mode settings for the DMA Channel. The register may only be written when the channel is disabled by setting to 0x0 the DRU_CHRT_CTL_j[31] ENABLE bit.

Offset = 40000h + (j * 100h); where j = 0h to 1Fh

Table 23-19. DRU_CFG_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D04 0000h

Figure 23-9. DRU_CFG_j Register

63	62	61	60	59	58	57	56
RSVD							
R-0h							
55	54	53	52	51	50	49	48
RSVD							
R-0h							
47	46	45	44	43	42	41	40
RSVD							
R-0h							
39	38	37	36	35	34	33	32
RSVD							
R-0h							
31	30	29	28	27	26	25	24
PAUSE_ON_ERR	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED				CHAN_TYPE_OWNER	CHAN_TYPE		
R/W-X				R/W-0h		R-0h	
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-20. DRU_CFG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RSVD	R	0h	Reserved

Table 23-20. DRU_CFG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31	PAUSE_ON_ERR	R/W	0h	Pause on Error. This field controls what the channel will do if an error or exception occurs during a data transfer. This field is encoded as follows: 0 = Channel will drop current work and move on 1 = Channel will pause and wait for SW to investigate and un-pause the channel.
30-20	RESERVED	R/W	X	Reserved
19	CHAN_TYPE_OWNER	R/W	0h	This field controls how the TR is received by the UTC. 0 = The DRU_SUBMIT_WORD0_1_j_k to DRU_SUBMIT_WORD14_15_j_k registers must be written to submit it. 1 = The TR will be received through PSI-L.
18-16	CHAN_TYPE	R	0h	This field states the TR type that is being used along with CHAN_TYPE_OWNER field make up the 4-bit CHAN_TYPE for an UTC. The value of this is all zeroes to reflect that the UTC DRU only does TRs through pass-by value mechanisms.
15-0	RESERVED	R/W	X	Reserved

23.10 DRU_CHOES0_j Register (Offset = 40020h + formula) [reset = 0h]

DRU_CHOES0_j is shown in [Figure 23-10](#) and described in [Table 23-22](#).

Return to [Summary Table](#).

The Output Event Steering Registers are used to specify a global event number to generate anytime the required event generation criteria specified in a TR are met. A single event with the event number set equal to the value in the corresponding register will be generated. This register is provided in order to allow security software to lock down which events in the global space any given channel or thread is allowed to generate.

Offset = 40020h + (j * 100h); where j = 0h to 1Fh

Table 23-21. DRU_CHOES0_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D04 0020h

Figure 23-10. DRU_CHOES0_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																															
R-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD																EVT_NUM															
R-0h																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-22. DRU_CHOES0_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-16	RSVD	R	0h	Reserved
15-0	EVT_NUM	R/W	0h	This is the global event number to be generated.

23.11 DRU_CHST_SCHED_j Register (Offset = 40060h + formula) [reset = X]

DRU_CHST_SCHED_j is shown in [Figure 23-11](#) and described in [Table 23-24](#).

Return to [Summary Table](#).

Channel Static Scheduler Config Register

Offset = 40060h + (j * 100h); where j = 0h to 1Fh

Table 23-23. DRU_CHST_SCHED_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D04 0060h

Figure 23-11. DRU_CHST_SCHED_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R/W-X															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED															
R/W-X															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													QUEUE		
R/W-X													R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-24. DRU_CHST_SCHED_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-3	RESERVED	R/W	X	
2-0	QUEUE	R/W	0h	Thus is the queue number that is written

23.12 DRU_CHRT_CTL_j Register (Offset = 60000h + formula) [reset = X]

DRU_CHRT_CTL_j is shown in [Figure 23-12](#) and described in [Table 23-26](#).

Return to [Summary Table](#).

The channel realtime control register contains real-time control and status information for the DMA Channel. The fields in this register can be changed while the channel is in operation.

Offset = 60000h + (j * 100h); where j = 0h to 1Fh

Table 23-25. DRU_CHRT_CTL_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D06 0000h

Figure 23-12. DRU_CHRT_CTL_j Register

63	62	61	60	59	58	57	56
RSVD							
R-0h							
55	54	53	52	51	50	49	48
RSVD							
R-0h							
47	46	45	44	43	42	41	40
RSVD							
R-0h							
39	38	37	36	35	34	33	32
RSVD							
R-0h							
31	30	29	28	27	26	25	24
ENABLE	TEARDOWN	PAUSE	RESERVED				
R/W-0h	R/W-0h	R/W-0h	R/W-X				
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-26. DRU_CHRT_CTL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	RSVD	R	0h	Reserved

Table 23-26. DRU_CHRT_CTL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
31	ENABLE	R/W	0h	This field enables or disables the channel. Disabling a channel halts operation on the channel after the current block transfer is completed. Disabling a channel in the middle of a packet transfer may result in underflow conditions in the attached application block and data loss. This field will be cleared after a channel teardown is complete. This field is encoded as follows: 0 = channel is disabled 1 = channel is enabled
30	TEARDOWN	R/W	0h	Channel teardown. Setting this bit will request the channel to be torn down. This field will remain set after a channel teardown is complete.
29	PAUSE	R/W	0h	Channel pause. Setting this bit will request the channel to pause processing at the next packet boundary. This is a more graceful method of halting processing than disabling the channel as it will not allow any current packets to underflow.
28-0	RESERVED	R/W	X	Reserved

23.13 DRU_CHRT_SWTRIG_j Register (Offset = 60008h + formula) [reset = X]

DRU_CHRT_SWTRIG_j is shown in [Figure 23-13](#) and described in [Table 23-28](#).

Return to [Summary Table](#).

The Software Trigger Register provides a mechanism by which software can directly trigger the channel in a secure way.

Offset = 60008h + (j * 100h); where j = 0h to 1Fh

Table 23-27. DRU_CHRT_SWTRIG_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D06 0008h

Figure 23-13. DRU_CHRT_SWTRIG_j Register

63	62	61	60	59	58	57	56
RSVD							
R-X							
55	54	53	52	51	50	49	48
RSVD							
R-X							
47	46	45	44	43	42	41	40
RSVD							
R-X							
39	38	37	36	35	34	33	32
RSVD							
R-X							
31	30	29	28	27	26	25	24
RSVD							
R-X							
23	22	21	20	19	18	17	16
RSVD							
R-X							
15	14	13	12	11	10	9	8
RSVD							
R-X							
7	6	5	4	3	2	1	0
RSVD					LOCAL_TRIGG ER0	GLOBAL_TRIG GER1	GLOBAL_TRIG GER0
R-X					R/W-0h	R/W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-28. DRU_CHRT_SWTRIG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-3	RSVD	R	X	Reserved
2	LOCAL_TRIGGER0	R/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel. This will trigger Local Event
1	GLOBAL_TRIGGER1	R/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel. This will trigger Global Event 1

Table 23-28. DRU_CHRT_SWTRIG_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GLOBAL_TRIGGER0	R/W	0h	Trigger: writing this bit with a value of 1 will cause the trigger event to be sent to this channel. This will trigger Global Event 0

23.14 DRU_CHRT_STATUS_DET_j Register (Offset = 60010h + formula) [reset = 0h]

DRU_CHRT_STATUS_DET_j is shown in [Figure 23-14](#) and described in [Table 23-30](#).

Return to [Summary Table](#).

The channel status details

Offset = 60010h + (j * 100h); where j = 0h to 1Fh

Table 23-29. DRU_CHRT_STATUS_DET_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D06 0010h

Figure 23-14. DRU_CHRT_STATUS_DET_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED															
R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD_ID								INFO				STATUS_TYPE			
R-0h								R-0h				R-0h			

LEGEND: R = Read Only; -n = value after reset

Table 23-30. DRU_CHRT_STATUS_DET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-16	RESERVED	R	0h	Reserved
15-8	CMD_ID	R	0h	The command id of the TR that had an error.
7-4	INFO	R	0h	The information of the type of status.
3-0	STATUS_TYPE	R	0h	The type of error that occurred. Submission Errors are not captured in this register

23.15 DRU_CHRT_STATUS_CNT_j Register (Offset = 60018h + formula) [reset = 0h]

DRU_CHRT_STATUS_CNT_j is shown in [Figure 23-15](#) and described in [Table 23-32](#).

Return to [Summary Table](#).

The channel count details

Offset = 60018h + (j * 100h); where j = 0h to 1Fh

Table 23-31. DRU_CHRT_STATUS_CNT_j Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D06 0018h

Figure 23-15. DRU_CHRT_STATUS_CNT_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT3																ICNT2															
R-0h																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICNT1																ICNT0															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-32. DRU_CHRT_STATUS_CNT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT3	R	0h	Value of outermost count when error occurred
47-32	ICNT2	R	0h	Value of second outermost count when error occurred
31-16	ICNT1	R	0h	The value of the second innermost count when error occurred
15-0	ICNT0	R	0h	The value of the innermost count when error occurred

23.16 DRU_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j Register (Offset = 80000h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j is shown in [Figure 23-16](#) and described in [Table 23-34](#).

Return to [Summary Table](#).

The first TR submission word

Offset = 80000h + (j * 100h); where j = 0h to 1Fh

Table 23-33.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D08 0000h

Figure 23-16. DRU_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT1																ICNT0															
R/W-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAGS																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-34. DRU_ATOMIC_SUBMIT_CURR_TR_WORD0_1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT1	R/W	0h	Lines in a transfer
47-32	ICNT0	R/W	0h	Bytes in a transfer
31-0	FLAGS	R/W	0h	Flags for the operation and type of descriptor

23.17 DRU_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j Register (Offset = 80008h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j is shown in [Figure 23-17](#) and described in [Table 23-36](#).

Return to [Summary Table](#).

The second TR submission word

Offset = 80008h + (j * 100h); where j = 0h to 1Fh

Table 23-35.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0008h

Figure 23-17. DRU_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																SRC_ADDR															
R-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_ADDR																															
R/W-0h																															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-36. DRU_ATOMIC_SUBMIT_CURR_TR_WORD2_3_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RSVD	R	0h	
47-0	SRC_ADDR	R/W	0h	Source transfer address virtual or physical allowed

23.18 DRU_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j Register (Offset = 80010h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j is shown in [Figure 23-18](#) and described in [Table 23-38](#).

Return to [Summary Table](#).

The third TR submission word

Offset = 80010h + (j * 100h); where j = 0h to 1Fh

Table 23-37.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0010h

Figure 23-18. DRU_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT3																ICNT2															
R/W-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-38. DRU_ATOMIC_SUBMIT_CURR_TR_WORD4_5_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT3	R/W	0h	The size of the 4th loop in the TR transfer
47-32	ICNT2	R/W	0h	The size of the 3rd loop in the TR transfer
31-0	DIM1	R/W	0h	The first dimension width of the source data

23.19 DRU_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j Register (Offset = 80018h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j is shown in [Figure 23-19](#) and described in [Table 23-40](#).

Return to [Summary Table](#).

The fourth TR submission word

Offset = 80018h + (j * 100h); where j = 0h to 1Fh

Table 23-39.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0018h

Figure 23-19. DRU_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DIM3																															
R/W-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-40. DRU_ATOMIC_SUBMIT_CURR_TR_WORD6_7_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DIM3	R/W	0h	The third dimension width of the source data
31-0	DIM2	R/W	0h	The second dimension width of the source data

23.20 DRU_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j Register (Offset = 80020h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j is shown in [Figure 23-20](#) and described in [Table 23-42](#).

Return to [Summary Table](#).

The fifth TR submission word

Offset = 80020h + (j * 100h); where j = 0h to 1Fh

Table 23-41.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D08 0020h

Figure 23-20. DRU_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DDIM1																															
R/W-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMTFLAGS																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-42. DRU_ATOMIC_SUBMIT_CURR_TR_WORD8_9_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DDIM1	R/W	0h	The first dimension width of the destination data
31-0	FMTFLAGS	R/W	0h	The data formatting flags to be used for the TR

23.21 DRU_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j Register (Offset = 80028h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j is shown in [Figure 23-21](#) and described in [Table 23-44](#).

Return to [Summary Table](#).

The sixth TR submission word

Offset = 80028h + (j * 100h); where j = 0h to 1Fh

Table 23-43.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D08 0028h

Figure 23-21. DRU_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																DADDR															
R-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DADDR															
																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-44. DRU_ATOMIC_SUBMIT_CURR_TR_WORD10_11_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RSVD	R	0h	
47-0	DADDR	R/W	0h	Destination transfer address virtual or physical allowed

23.22 DRU_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j Register (Offset = 80030h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j is shown in [Figure 23-22](#) and described in [Table 23-46](#).

Return to [Summary Table](#).

The seventh TR submission word

Offset = 80030h + (j * 100h); where j = 0h to 1Fh

Table 23-45.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0030h

Figure 23-22. DRU_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DDIM3																															
R/W-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDIM2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-46. DRU_ATOMIC_SUBMIT_CURR_TR_WORD12_13_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DDIM3	R/W	0h	The third dimension width of the destination data
31-0	DDIM2	R/W	0h	The second dimension width of the destination data

23.23 DRU_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j Register (Offset = 80038h + formula) [reset = 0h]

DRU_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j is shown in [Figure 23-23](#) and described in [Table 23-48](#).

Return to [Summary Table](#).

The eight TR submission word

Offset = 80038h + (j * 100h); where j = 0h to 1Fh

Table 23-47.
DRU_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0038h

Figure 23-23. DRU_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DICNT3																DICNT2															
R/W-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DICNT1																DICNT0															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-48. DRU_ATOMIC_SUBMIT_CURR_TR_WORD14_15_j Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	DICNT3	R/W	0h	The fourth count of the destination if different than the source
47-32	DICNT2	R/W	0h	The third count of the destination if different than the source
31-16	DICNT1	R/W	0h	The second innermost count of the destination if different than the source
15-0	DICNT0	R/W	0h	The innermost count of the destination if different than the source

23.24 DRU_NEXT_TR_WORD0_1_j_k Register (Offset = 80040h + formula) [reset = 0h]

DRU_NEXT_TR_WORD0_1_j_k is shown in [Figure 23-24](#) and described in [Table 23-50](#).

Return to [Summary Table](#).

The first TR submission word

Offset = 80040h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-49. DRU_NEXT_TR_WORD0_1_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D08 0040h

Figure 23-24. DRU_NEXT_TR_WORD0_1_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT1																ICNT0															
R-0h																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAGS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-50. DRU_NEXT_TR_WORD0_1_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT1	R	0h	Lines in a transfer
47-32	ICNT0	R	0h	Bytes in a transfer
31-0	FLAGS	R	0h	Flags for the operation and type of descriptor

23.25 DRU_NEXT_TR_WORD2_3_j_k Register (Offset = 80048h + formula) [reset = 0h]

DRU_NEXT_TR_WORD2_3_j_k is shown in [Figure 23-25](#) and described in [Table 23-52](#).

Return to [Summary Table](#).

The second TR submission word

Offset = 80048h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-51. DRU_NEXT_TR_WORD2_3_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D08 0048h

Figure 23-25. DRU_NEXT_TR_WORD2_3_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																SRC_ADDR															
R-0h																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_ADDR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-52. DRU_NEXT_TR_WORD2_3_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RSVD	R	0h	
47-0	SRC_ADDR	R	0h	Source transfer address virtual or physical allowed

23.26 DRU_NEXT_TR_WORD4_5_j_k Register (Offset = 80050h + formula) [reset = 0h]

DRU_NEXT_TR_WORD4_5_j_k is shown in [Figure 23-26](#) and described in [Table 23-54](#).

Return to [Summary Table](#).

The third TR submission word

Offset = 80050h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-53. DRU_NEXT_TR_WORD4_5_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0050h

Figure 23-26. DRU_NEXT_TR_WORD4_5_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT3																ICNT2															
R-0h																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM1																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-54. DRU_NEXT_TR_WORD4_5_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT3	R	0h	The size of the 4th loop in the TR transfer
47-32	ICNT2	R	0h	The size of the 3rd loop in the TR transfer
31-0	DIM1	R	0h	The first dimension width of the source data

23.27 DRU_NEXT_TR_WORD6_7_j_k Register (Offset = 80058h + formula) [reset = 0h]

DRU_NEXT_TR_WORD6_7_j_k is shown in [Figure 23-27](#) and described in [Table 23-56](#).

Return to [Summary Table](#).

The fourth TR submission word

Offset = 80058h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-55. DRU_NEXT_TR_WORD6_7_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0058h

Figure 23-27. DRU_NEXT_TR_WORD6_7_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DIM3																															
R-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-56. DRU_NEXT_TR_WORD6_7_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DIM3	R	0h	The third dimension width of the source data
31-0	DIM2	R	0h	The second dimension width of the source data

23.28 DRU_NEXT_TR_WORD8_9_j_k Register (Offset = 80060h + formula) [reset = 0h]

DRU_NEXT_TR_WORD8_9_j_k is shown in [Figure 23-28](#) and described in [Table 23-58](#).

Return to [Summary Table](#).

The fifth TR submission word

Offset = 80060h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-57. DRU_NEXT_TR_WORD8_9_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D08 0060h

Figure 23-28. DRU_NEXT_TR_WORD8_9_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DDIM1																															
R-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMTFLAGS																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-58. DRU_NEXT_TR_WORD8_9_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DDIM1	R	0h	The first dimension width of the destination data
31-0	FMTFLAGS	R	0h	The data formatting flags to be used for the TR

23.29 DRU_NEXT_TR_WORD10_11_j_k Register (Offset = 80068h + formula) [reset = 0h]

DRU_NEXT_TR_WORD10_11_j_k is shown in [Figure 23-29](#) and described in [Table 23-60](#).

Return to [Summary Table](#).

The sixth TR submission word

Offset = 80068h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-59. DRU_NEXT_TR_WORD10_11_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0068h

Figure 23-29. DRU_NEXT_TR_WORD10_11_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																DADDR															
R-0h																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DADDR																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-60. DRU_NEXT_TR_WORD10_11_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RSVD	R	0h	
47-0	DADDR	R	0h	Destination transfer address virtual or physical allowed

23.30 DRU_NEXT_TR_WORD12_13_j_k Register (Offset = 80070h + formula) [reset = 0h]

DRU_NEXT_TR_WORD12_13_j_k is shown in [Figure 23-30](#) and described in [Table 23-62](#).

Return to [Summary Table](#).

The seventh TR submission word

Offset = 80070h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-61. DRU_NEXT_TR_WORD12_13_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0070h

Figure 23-30. DRU_NEXT_TR_WORD12_13_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DDIM3																															
R-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDIM2																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-62. DRU_NEXT_TR_WORD12_13_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DDIM3	R	0h	The third dimension width of the destination data
31-0	DDIM2	R	0h	The second dimension width of the destination data

23.31 DRU_NEXT_TR_WORD14_15_j_k Register (Offset = 80078h + formula) [reset = 0h]

DRU_NEXT_TR_WORD14_15_j_k is shown in [Figure 23-31](#) and described in [Table 23-64](#).

Return to [Summary Table](#).

The eight TR submission word

Offset = 80078h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-63. DRU_NEXT_TR_WORD14_15_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D08 0078h

Figure 23-31. DRU_NEXT_TR_WORD14_15_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DICNT3																DICNT2															
R-0h																R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DICNT1																DICNT0															
R-0h																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-64. DRU_NEXT_TR_WORD14_15_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	DICNT3	R	0h	The fourth count of the destination if different than the source
47-32	DICNT2	R	0h	The third count of the destination if different than the source
31-16	DICNT1	R	0h	The second innermost count of the destination if different than the source
15-0	DICNT0	R	0h	The innermost count of the destination if different than the source

23.32 DRU_SUBMIT_WORD0_1_j_k Register (Offset = A0000h + formula) [reset = 0h]

DRU_SUBMIT_WORD0_1_j_k is shown in [Figure 23-32](#) and described in [Table 23-66](#).

Return to [Summary Table](#).

The first TR submission word

Offset = A0000h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-65. DRU_SUBMIT_WORD0_1_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_M MR_CFG_DRU	6D0A 0000h

Figure 23-32. DRU_SUBMIT_WORD0_1_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT1																ICNT0															
R/W-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAGS																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-66. DRU_SUBMIT_WORD0_1_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT1	R/W	0h	Lines in a transfer
47-32	ICNT0	R/W	0h	Bytes in a transfer
31-0	FLAGS	R/W	0h	Flags for the operation and type of descriptor

23.33 DRU_SUBMIT_WORD2_3_j_k Register (Offset = A0008h + formula) [reset = 0h]

DRU_SUBMIT_WORD2_3_j_k is shown in [Figure 23-33](#) and described in [Table 23-68](#).

Return to [Summary Table](#).

The second TR submission word

Offset = A0008h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-67. DRU_SUBMIT_WORD2_3_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0008h

Figure 23-33. DRU_SUBMIT_WORD2_3_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																SRC_ADDR															
R-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRC_ADDR																															
R/W-0h																															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-68. DRU_SUBMIT_WORD2_3_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RSVD	R	0h	
47-0	SRC_ADDR	R/W	0h	Source transfer address virtual or physical allowed

23.34 DRU_SUBMIT_WORD4_5_j_k Register (Offset = A0010h + formula) [reset = 0h]

DRU_SUBMIT_WORD4_5_j_k is shown in [Figure 23-34](#) and described in [Table 23-70](#).

Return to [Summary Table](#).

The third TR submission word

Offset = A0010h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-69. DRU_SUBMIT_WORD4_5_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0010h

Figure 23-34. DRU_SUBMIT_WORD4_5_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ICNT3																ICNT2															
R/W-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM1																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-70. DRU_SUBMIT_WORD4_5_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	ICNT3	R/W	0h	The size of the 4th loop in the TR transfer
47-32	ICNT2	R/W	0h	The size of the 3rd loop in the TR transfer
31-0	DIM1	R/W	0h	The first dimension width of the source data

23.35 DRU_SUBMIT_WORD6_7_j_k Register (Offset = A0018h + formula) [reset = 0h]

DRU_SUBMIT_WORD6_7_j_k is shown in [Figure 23-35](#) and described in [Table 23-72](#).

Return to [Summary Table](#).

The fourth TR submission word

Offset = A0018h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-71. DRU_SUBMIT_WORD6_7_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0018h

Figure 23-35. DRU_SUBMIT_WORD6_7_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DIM3																															
R/W-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-72. DRU_SUBMIT_WORD6_7_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DIM3	R/W	0h	The third dimension width of the source data
31-0	DIM2	R/W	0h	The second dimension width of the source data

23.36 DRU_SUBMIT_WORD8_9_j_k Register (Offset = A0020h + formula) [reset = 0h]

DRU_SUBMIT_WORD8_9_j_k is shown in [Figure 23-36](#) and described in [Table 23-74](#).

Return to [Summary Table](#).

The fifth TR submission word

Offset = A0020h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-73. DRU_SUBMIT_WORD8_9_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0020h

Figure 23-36. DRU_SUBMIT_WORD8_9_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DDIM1																															
R/W-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMTFLAGS																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-74. DRU_SUBMIT_WORD8_9_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DDIM1	R/W	0h	The first dimension width of the destination data
31-0	FMTFLAGS	R/W	0h	The data formatting flags to be used for the TR

23.37 DRU_SUBMIT_WORD10_11_j_k Register (Offset = A0028h + formula) [reset = 0h]

DRU_SUBMIT_WORD10_11_j_k is shown in [Figure 23-37](#) and described in [Table 23-76](#).

Return to [Summary Table](#).

The sixth TR submission word

Offset = A0028h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-75. DRU_SUBMIT_WORD10_11_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0028h

Figure 23-37. DRU_SUBMIT_WORD10_11_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RSVD																DADDR															
R-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																DADDR															
																R/W-0h															

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-76. DRU_SUBMIT_WORD10_11_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	RSVD	R	0h	
47-0	DADDR	R/W	0h	Destination transfer address virtual or physical allowed

23.38 DRU_SUBMIT_WORD12_13_j_k Register (Offset = A0030h + formula) [reset = 0h]

DRU_SUBMIT_WORD12_13_j_k is shown in [Figure 23-38](#) and described in [Table 23-78](#).

Return to [Summary Table](#).

The seventh TR submission word

Offset = A0030h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

**Table 23-77. DRU_SUBMIT_WORD12_13_j_k
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0030h

Figure 23-38. DRU_SUBMIT_WORD12_13_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DDIM3																															
R/W-0h																															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDIM2																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-78. DRU_SUBMIT_WORD12_13_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-32	DDIM3	R/W	0h	The third dimension width of the destination data
31-0	DDIM2	R/W	0h	The second dimension width of the destination data

23.39 DRU_SUBMIT_WORD14_15_j_k Register (Offset = A0038h + formula) [reset = 0h]

DRU_SUBMIT_WORD14_15_j_k is shown in [Figure 23-39](#) and described in [Table 23-80](#).

Return to [Summary Table](#).

The eight TR submission word

Offset = A0038h + (j * 100h) + (k * 40h); where j = 0h to 1Fh, k = 0h to 2h

Table 23-79. DRU_SUBMIT_WORD14_15_j_k Instances

Instance	Physical Address
COMPUTE_CLUSTER0_MMR_DRU_MR_CFG_DRU	6D0A 0038h

Figure 23-39. DRU_SUBMIT_WORD14_15_j_k Register

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
DICNT3																DICNT2															
R/W-0h																R/W-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DICNT1																DICNT0															
R/W-0h																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-80. DRU_SUBMIT_WORD14_15_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
63-48	DICNT3	R/W	0h	The fourth count of the destination if different than the source
47-32	DICNT2	R/W	0h	The third count of the destination if different than the source
31-16	DICNT1	R/W	0h	The second innermost count of the destination if different than the source
15-0	DICNT0	R/W	0h	The innermost count of the destination if different than the source

23.40 DRU_CAUSE_y Register (Offset = E0000h + formula) [reset = 0h]

DRU_CAUSE_y is shown in [Figure 23-40](#) and described in [Table 23-82](#).

Return to [Summary Table](#).

Offset = E0000h + (y * 8h); where y = 0h to 1h

Table 23-81. DRU_CAUSE_y Instances

Instance	Physical Address
DRU0	6D0E 0000h

Figure 23-40. DRU_CAUSE_y Register

63	62	61	60	59	58	57	56
R_ERR15	R_PEND15	T_ERR15	T_PEND15	R_ERR14	R_PEND14	T_ERR14	T_PEND14
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
55	54	53	52	51	50	49	48
R_ERR13	R_PEND13	T_ERR13	T_PEND13	R_ERR12	R_PEND12	T_ERR12	T_PEND12
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
47	46	45	44	43	42	41	40
R_ERR11	R_PEND11	T_ERR11	T_PEND11	R_ERR10	R_PEND10	T_ERR10	T_PEND10
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
39	38	37	36	35	34	33	32
R_ERR9	R_PEND9	T_ERR9	T_PEND9	R_ERR8	R_PEND8	T_ERR8	T_PEND8
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
31	30	29	28	27	26	25	24
R_ERR7	R_PEND7	T_ERR7	T_PEND7	R_ERR6	R_PEND6	T_ERR6	T_PEND6
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
23	22	21	20	19	18	17	16
R_ERR5	R_PEND5	T_ERR5	T_PEND5	R_ERR4	R_PEND4	T_ERR4	T_PEND4
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
15	14	13	12	11	10	9	8
R_ERR3	R_PEND3	T_ERR3	T_PEND3	R_ERR2	R_PEND2	T_ERR2	T_PEND2
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
R_ERR1	R_PEND1	T_ERR1	T_PEND1	R_ERR0	R_PEND0	T_ERR0	T_PEND0
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R = Read Only; -n = value after reset

Table 23-82. DRU_CAUSE_y Register Field Descriptions

Bit	Field	Type	Reset	Description
63	R_ERR15	R	0h	Masked error bit for Tx channel 16*y+15
62	R_PEND15	R	0h	Masked completion ring pending bit for Rx channel 16*y+15
61	T_ERR15	R	0h	Masked error bit for Tx channel 16*y+15
60	T_PEND15	R	0h	Masked completion ring pending bit for Tx channel 16*y+15
59	R_ERR14	R	0h	Masked error bit for Tx channel 16*y+14
58	R_PEND14	R	0h	Masked completion ring pending bit for Rx channel 16*y+14
57	T_ERR14	R	0h	Masked error bit for Tx channel 16*y+14

Table 23-82. DRU_CAUSE_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
56	T_PEND14	R	0h	Masked completion ring pending bit for Tx channel 16*y+14
55	R_ERR13	R	0h	Masked error bit for Tx channel 16*y+13
54	R_PEND13	R	0h	Masked completion ring pending bit for Rx channel 16*y+13
53	T_ERR13	R	0h	Masked error bit for Tx channel 16*y+13
52	T_PEND13	R	0h	Masked completion ring pending bit for Tx channel 16*y+13
51	R_ERR12	R	0h	Masked error bit for Tx channel 16*y+12
50	R_PEND12	R	0h	Masked completion ring pending bit for Rx channel 16*y+12
49	T_ERR12	R	0h	Masked error bit for Tx channel 16*y+12
48	T_PEND12	R	0h	Masked completion ring pending bit for Tx channel 16*y+12
47	R_ERR11	R	0h	Masked error bit for Tx channel 16*y+11
46	R_PEND11	R	0h	Masked completion ring pending bit for Rx channel 16*y+11
45	T_ERR11	R	0h	Masked error bit for Tx channel 16*y+11
44	T_PEND11	R	0h	Masked completion ring pending bit for Tx channel 16*y+11
43	R_ERR10	R	0h	Masked error bit for Tx channel 16*y+10
42	R_PEND10	R	0h	Masked completion ring pending bit for Rx channel 16*y+10
41	T_ERR10	R	0h	Masked error bit for Tx channel 16*y+10
40	T_PEND10	R	0h	Masked completion ring pending bit for Tx channel 16*y+10
39	R_ERR9	R	0h	Masked error bit for Tx channel 16*y+9
38	R_PEND9	R	0h	Masked completion ring pending bit for Rx channel 16*y+9
37	T_ERR9	R	0h	Masked error bit for Tx channel 16*y+9
36	T_PEND9	R	0h	Masked completion ring pending bit for Tx channel 16*y+9
35	R_ERR8	R	0h	Masked error bit for Tx channel 16*y+8
34	R_PEND8	R	0h	Masked completion ring pending bit for Rx channel 16*y+8
33	T_ERR8	R	0h	Masked error bit for Tx channel 16*y+8
32	T_PEND8	R	0h	Masked completion ring pending bit for Tx channel 16*y+8
31	R_ERR7	R	0h	Masked error bit for Tx channel 16*y+7
30	R_PEND7	R	0h	Masked completion ring pending bit for Rx channel 16*y+7
29	T_ERR7	R	0h	Masked error bit for Tx channel 16*y+7
28	T_PEND7	R	0h	Masked completion ring pending bit for Tx channel 16*y+7
27	R_ERR6	R	0h	Masked error bit for Tx channel 16*y+6
26	R_PEND6	R	0h	Masked completion ring pending bit for Rx channel 16*y+6
25	T_ERR6	R	0h	Masked error bit for Tx channel 16*y+6
24	T_PEND6	R	0h	Masked completion ring pending bit for Tx channel 16*y+6
23	R_ERR5	R	0h	Masked error bit for Tx channel 16*y+5
22	R_PEND5	R	0h	Masked completion ring pending bit for Rx channel 16*y+5
21	T_ERR5	R	0h	Masked error bit for Tx channel 16*y+5
20	T_PEND5	R	0h	Masked completion ring pending bit for Tx channel 16*y+5
19	R_ERR4	R	0h	Masked error bit for Tx channel 16*y+4
18	R_PEND4	R	0h	Masked completion ring pending bit for Rx channel 16*y+4
17	T_ERR4	R	0h	Masked error bit for Tx channel 16*y+4

Table 23-82. DRU_CAUSE_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	T_PEND4	R	0h	Masked completion ring pending bit for Tx channel 16*y+4
15	R_ERR3	R	0h	Masked error bit for Tx channel 16*y+3
14	R_PEND3	R	0h	Masked completion ring pending bit for Rx channel 16*y+3
13	T_ERR3	R	0h	Masked error bit for Tx channel 16*y+3
12	T_PEND3	R	0h	Masked completion ring pending bit for Tx channel 16*y+3
11	R_ERR2	R	0h	Masked error bit for Tx channel 16*y+2
10	R_PEND2	R	0h	Masked completion ring pending bit for Rx channel 16*y+2
9	T_ERR2	R	0h	Masked error bit for Tx channel 16*y+2
8	T_PEND2	R	0h	Masked completion ring pending bit for Tx channel 16*y+2
7	R_ERR1	R	0h	Masked error bit for Tx channel 16*y+1
6	R_PEND1	R	0h	Masked completion ring pending bit for Rx channel 16*y+1
5	T_ERR1	R	0h	Masked error bit for Tx channel 16*y+1
4	T_PEND1	R	0h	Masked completion ring pending bit for Tx channel 16*y+1
3	R_ERR0	R	0h	Masked error bit for Tx channel 16*y
2	R_PEND0	R	0h	Masked completion ring pending bit for Rx channel 16*y
1	T_ERR0	R	0h	Masked error bit for Tx channel 16*y
0	T_PEND0	R	0h	Masked completion ring pending bit for Tx channel 16*y

23.1 DRU_FW Registers

Table 23-84 lists the memory-mapped registers for the DRU_FW registers. All register offset addresses not listed in Table 23-84 should be considered as reserved locations and the register contents should not be modified.

Table 23-83. DRU_FW Instances

Instance	Base Address
COMPUTE_CLUSTER0_DRU_FW	4504 7000h

Table 23-84. DRU_FW Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_D RU_FW Physical Address
0h	FW0_FW_REGION_0_CONTROL	Firewall Region 0 Control Register	4504 7000h
4h	FW0_FW_REGION_0_PERMISSION_0	Firewall Region 0 Permission 0 Register	4504 7004h
8h	FW0_FW_REGION_0_PERMISSION_1	Firewall Region 0 Permission 1 Register	4504 7008h
Ch	FW0_FW_REGION_0_PERMISSION_2	Firewall Region 0 Permission 2 Register	4504 700Ch
10h	FW0_FW_REGION_0_START_ADDRESS_L	Firewall Region 0 Start Address Low Register	4504 7010h
14h	FW0_FW_REGION_0_START_ADDRESS_H	Firewall Region 0 Start Address High Register	4504 7014h
18h	FW0_FW_REGION_0_END_ADDRESS_L	Firewall Region 0 End Address Low Register	4504 7018h
1Ch	FW0_FW_REGION_0_END_ADDRESS_H	Firewall Region 0 End Address High Register	4504 701Ch
20h	FW0_FW_REGION_1_CONTROL	Firewall Region 1 Control Register	4504 7020h
24h	FW0_FW_REGION_1_PERMISSION_0	Firewall Region 1 Permission 0 Register	4504 7024h
28h	FW0_FW_REGION_1_PERMISSION_1	Firewall Region 1 Permission 1 Register	4504 7028h
2Ch	FW0_FW_REGION_1_PERMISSION_2	Firewall Region 1 Permission 2 Register	4504 702Ch
30h	FW0_FW_REGION_1_START_ADDRESS_L	Firewall Region 1 Start Address Low Register	4504 7030h
34h	FW0_FW_REGION_1_START_ADDRESS_H	Firewall Region 1 Start Address High Register	4504 7034h
38h	FW0_FW_REGION_1_END_ADDRESS_L	Firewall Region 1 End Address Low Register	4504 7038h
3Ch	FW0_FW_REGION_1_END_ADDRESS_H	Firewall Region 1 End Address High Register	4504 703Ch
40h	FW0_FW_REGION_2_CONTROL	Firewall Region 2 Control Register	4504 7040h
44h	FW0_FW_REGION_2_PERMISSION_0	Firewall Region 2 Permission 0 Register	4504 7044h
48h	FW0_FW_REGION_2_PERMISSION_1	Firewall Region 2 Permission 1 Register	4504 7048h
4Ch	FW0_FW_REGION_2_PERMISSION_2	Firewall Region 2 Permission 2 Register	4504 704Ch
50h	FW0_FW_REGION_2_START_ADDRESS_L	Firewall Region 2 Start Address Low Register	4504 7050h
54h	FW0_FW_REGION_2_START_ADDRESS_H	Firewall Region 2 Start Address High Register	4504 7054h
58h	FW0_FW_REGION_2_END_ADDRESS_L	Firewall Region 2 End Address Low Register	4504 7058h
5Ch	FW0_FW_REGION_2_END_ADDRESS_H	Firewall Region 2 End Address High Register	4504 705Ch
60h	FW0_FW_REGION_3_CONTROL	Firewall Region 3 Control Register	4504 7060h
64h	FW0_FW_REGION_3_PERMISSION_0	Firewall Region 3 Permission 0 Register	4504 7064h
68h	FW0_FW_REGION_3_PERMISSION_1	Firewall Region 3 Permission 1 Register	4504 7068h
6Ch	FW0_FW_REGION_3_PERMISSION_2	Firewall Region 3 Permission 2 Register	4504 706Ch
70h	FW0_FW_REGION_3_START_ADDRESS_L	Firewall Region 3 Start Address Low Register	4504 7070h
74h	FW0_FW_REGION_3_START_ADDRESS_H	Firewall Region 3 Start Address High Register	4504 7074h
78h	FW0_FW_REGION_3_END_ADDRESS_L	Firewall Region 3 End Address Low Register	4504 7078h
7Ch	FW0_FW_REGION_3_END_ADDRESS_H	Firewall Region 3 End Address High Register	4504 707Ch
80h	FW0_FW_REGION_4_CONTROL	Firewall Region 4 Control Register	4504 7080h
84h	FW0_FW_REGION_4_PERMISSION_0	Firewall Region 4 Permission 0 Register	4504 7084h
88h	FW0_FW_REGION_4_PERMISSION_1	Firewall Region 4 Permission 1 Register	4504 7088h
8Ch	FW0_FW_REGION_4_PERMISSION_2	Firewall Region 4 Permission 2 Register	4504 708Ch
90h	FW0_FW_REGION_4_START_ADDRESS_L	Firewall Region 4 Start Address Low Register	4504 7090h
94h	FW0_FW_REGION_4_START_ADDRESS_H	Firewall Region 4 Start Address High Register	4504 7094h
98h	FW0_FW_REGION_4_END_ADDRESS_L	Firewall Region 4 End Address Low Register	4504 7098h

Table 23-84. DRU_FW Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_D RU_FW Physical Address
9Ch	FW0_FW_REGION_4_END_ADDRESS_H	Firewall Region 4 End Address High Register	4504 709Ch
A0h	FW0_FW_REGION_5_CONTROL	Firewall Region 5 Control Register	4504 70A0h
A4h	FW0_FW_REGION_5_PERMISSION_0	Firewall Region 5 Permission 0 Register	4504 70A4h
A8h	FW0_FW_REGION_5_PERMISSION_1	Firewall Region 5 Permission 1 Register	4504 70A8h
ACH	FW0_FW_REGION_5_PERMISSION_2	Firewall Region 5 Permission 2 Register	4504 70ACH
B0h	FW0_FW_REGION_5_START_ADDRESS_L	Firewall Region 5 Start Address Low Register	4504 70B0h
B4h	FW0_FW_REGION_5_START_ADDRESS_H	Firewall Region 5 Start Address High Register	4504 70B4h
B8h	FW0_FW_REGION_5_END_ADDRESS_L	Firewall Region 5 End Address Low Register	4504 70B8h
BCh	FW0_FW_REGION_5_END_ADDRESS_H	Firewall Region 5 End Address High Register	4504 70BCh
C0h	FW0_FW_REGION_6_CONTROL	Firewall Region 6 Control Register	4504 70C0h
C4h	FW0_FW_REGION_6_PERMISSION_0	Firewall Region 6 Permission 0 Register	4504 70C4h
C8h	FW0_FW_REGION_6_PERMISSION_1	Firewall Region 6 Permission 1 Register	4504 70C8h
CCh	FW0_FW_REGION_6_PERMISSION_2	Firewall Region 6 Permission 2 Register	4504 70CCh
D0h	FW0_FW_REGION_6_START_ADDRESS_L	Firewall Region 6 Start Address Low Register	4504 70D0h
D4h	FW0_FW_REGION_6_START_ADDRESS_H	Firewall Region 6 Start Address High Register	4504 70D4h
D8h	FW0_FW_REGION_6_END_ADDRESS_L	Firewall Region 6 End Address Low Register	4504 70D8h
DCh	FW0_FW_REGION_6_END_ADDRESS_H	Firewall Region 6 End Address High Register	4504 70DCh
E0h	FW0_FW_REGION_7_CONTROL	Firewall Region 7 Control Register	4504 70E0h
E4h	FW0_FW_REGION_7_PERMISSION_0	Firewall Region 7 Permission 0 Register	4504 70E4h
E8h	FW0_FW_REGION_7_PERMISSION_1	Firewall Region 7 Permission 1 Register	4504 70E8h
ECh	FW0_FW_REGION_7_PERMISSION_2	Firewall Region 7 Permission 2 Register	4504 70ECh
F0h	FW0_FW_REGION_7_START_ADDRESS_L	Firewall Region 7 Start Address Low Register	4504 70F0h
F4h	FW0_FW_REGION_7_START_ADDRESS_H	Firewall Region 7 Start Address High Register	4504 70F4h
F8h	FW0_FW_REGION_7_END_ADDRESS_L	Firewall Region 7 End Address Low Register	4504 70F8h
FCh	FW0_FW_REGION_7_END_ADDRESS_H	Firewall Region 7 End Address High Register	4504 70FCh
100h	FW0_FW_REGION_8_CONTROL	Firewall Region 8 Control Register	4504 7100h
104h	FW0_FW_REGION_8_PERMISSION_0	Firewall Region 8 Permission 0 Register	4504 7104h
108h	FW0_FW_REGION_8_PERMISSION_1	Firewall Region 8 Permission 1 Register	4504 7108h
10Ch	FW0_FW_REGION_8_PERMISSION_2	Firewall Region 8 Permission 2 Register	4504 710Ch
110h	FW0_FW_REGION_8_START_ADDRESS_L	Firewall Region 8 Start Address Low Register	4504 7110h
114h	FW0_FW_REGION_8_START_ADDRESS_H	Firewall Region 8 Start Address High Register	4504 7114h
118h	FW0_FW_REGION_8_END_ADDRESS_L	Firewall Region 8 End Address Low Register	4504 7118h
11Ch	FW0_FW_REGION_8_END_ADDRESS_H	Firewall Region 8 End Address High Register	4504 711Ch
120h	FW0_FW_REGION_9_CONTROL	Firewall Region 9 Control Register	4504 7120h
124h	FW0_FW_REGION_9_PERMISSION_0	Firewall Region 9 Permission 0 Register	4504 7124h
128h	FW0_FW_REGION_9_PERMISSION_1	Firewall Region 9 Permission 1 Register	4504 7128h
12Ch	FW0_FW_REGION_9_PERMISSION_2	Firewall Region 9 Permission 2 Register	4504 712Ch
130h	FW0_FW_REGION_9_START_ADDRESS_L	Firewall Region 9 Start Address Low Register	4504 7130h
134h	FW0_FW_REGION_9_START_ADDRESS_H	Firewall Region 9 Start Address High Register	4504 7134h
138h	FW0_FW_REGION_9_END_ADDRESS_L	Firewall Region 9 End Address Low Register	4504 7138h
13Ch	FW0_FW_REGION_9_END_ADDRESS_H	Firewall Region 9 End Address High Register	4504 713Ch
140h	FW0_FW_REGION_10_CONTROL	Firewall Region 10 Control Register	4504 7140h
144h	FW0_FW_REGION_10_PERMISSION_0	Firewall Region 10 Permission 0 Register	4504 7144h
148h	FW0_FW_REGION_10_PERMISSION_1	Firewall Region 10 Permission 1 Register	4504 7148h
14Ch	FW0_FW_REGION_10_PERMISSION_2	Firewall Region 10 Permission 2 Register	4504 714Ch

Table 23-84. DRU_FW Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_D RU_FW Physical Address
150h	FW0_FW_REGION_10_START_ADDRESS_L	Firewall Region 10 Start Address Low Register	4504 7150h
154h	FW0_FW_REGION_10_START_ADDRESS_H	Firewall Region 10 Start Address High Register	4504 7154h
158h	FW0_FW_REGION_10_END_ADDRESS_L	Firewall Region 10 End Address Low Register	4504 7158h
15Ch	FW0_FW_REGION_10_END_ADDRESS_H	Firewall Region 10 End Address High Register	4504 715Ch
160h	FW0_FW_REGION_11_CONTROL	Firewall Region 11 Control Register	4504 7160h
164h	FW0_FW_REGION_11_PERMISSION_0	Firewall Region 11 Permission 0 Register	4504 7164h
168h	FW0_FW_REGION_11_PERMISSION_1	Firewall Region 11 Permission 1 Register	4504 7168h
16Ch	FW0_FW_REGION_11_PERMISSION_2	Firewall Region 11 Permission 2 Register	4504 716Ch
170h	FW0_FW_REGION_11_START_ADDRESS_L	Firewall Region 11 Start Address Low Register	4504 7170h
174h	FW0_FW_REGION_11_START_ADDRESS_H	Firewall Region 11 Start Address High Register	4504 7174h
178h	FW0_FW_REGION_11_END_ADDRESS_L	Firewall Region 11 End Address Low Register	4504 7178h
17Ch	FW0_FW_REGION_11_END_ADDRESS_H	Firewall Region 11 End Address High Register	4504 717Ch
180h	FW0_FW_REGION_12_CONTROL	Firewall Region 12 Control Register	4504 7180h
184h	FW0_FW_REGION_12_PERMISSION_0	Firewall Region 12 Permission 0 Register	4504 7184h
188h	FW0_FW_REGION_12_PERMISSION_1	Firewall Region 12 Permission 1 Register	4504 7188h
18Ch	FW0_FW_REGION_12_PERMISSION_2	Firewall Region 12 Permission 2 Register	4504 718Ch
190h	FW0_FW_REGION_12_START_ADDRESS_L	Firewall Region 12 Start Address Low Register	4504 7190h
194h	FW0_FW_REGION_12_START_ADDRESS_H	Firewall Region 12 Start Address High Register	4504 7194h
198h	FW0_FW_REGION_12_END_ADDRESS_L	Firewall Region 12 End Address Low Register	4504 7198h
19Ch	FW0_FW_REGION_12_END_ADDRESS_H	Firewall Region 12 End Address High Register	4504 719Ch
1A0h	FW0_FW_REGION_13_CONTROL	Firewall Region 13 Control Register	4504 71A0h
1A4h	FW0_FW_REGION_13_PERMISSION_0	Firewall Region 13 Permission 0 Register	4504 71A4h
1A8h	FW0_FW_REGION_13_PERMISSION_1	Firewall Region 13 Permission 1 Register	4504 71A8h
1ACh	FW0_FW_REGION_13_PERMISSION_2	Firewall Region 13 Permission 2 Register	4504 71ACh
1B0h	FW0_FW_REGION_13_START_ADDRESS_L	Firewall Region 13 Start Address Low Register	4504 71B0h
1B4h	FW0_FW_REGION_13_START_ADDRESS_H	Firewall Region 13 Start Address High Register	4504 71B4h
1B8h	FW0_FW_REGION_13_END_ADDRESS_L	Firewall Region 13 End Address Low Register	4504 71B8h
1BCh	FW0_FW_REGION_13_END_ADDRESS_H	Firewall Region 13 End Address High Register	4504 71BCh
1C0h	FW0_FW_REGION_14_CONTROL	Firewall Region 14 Control Register	4504 71C0h
1C4h	FW0_FW_REGION_14_PERMISSION_0	Firewall Region 14 Permission 0 Register	4504 71C4h
1C8h	FW0_FW_REGION_14_PERMISSION_1	Firewall Region 14 Permission 1 Register	4504 71C8h
1CCh	FW0_FW_REGION_14_PERMISSION_2	Firewall Region 14 Permission 2 Register	4504 71CCh
1D0h	FW0_FW_REGION_14_START_ADDRESS_L	Firewall Region 14 Start Address Low Register	4504 71D0h
1D4h	FW0_FW_REGION_14_START_ADDRESS_H	Firewall Region 14 Start Address High Register	4504 71D4h
1D8h	FW0_FW_REGION_14_END_ADDRESS_L	Firewall Region 14 End Address Low Register	4504 71D8h
1DCh	FW0_FW_REGION_14_END_ADDRESS_H	Firewall Region 14 End Address High Register	4504 71DCh
1E0h	FW0_FW_REGION_15_CONTROL	Firewall Region 15 Control Register	4504 71E0h
1E4h	FW0_FW_REGION_15_PERMISSION_0	Firewall Region 15 Permission 0 Register	4504 71E4h
1E8h	FW0_FW_REGION_15_PERMISSION_1	Firewall Region 15 Permission 1 Register	4504 71E8h
1ECh	FW0_FW_REGION_15_PERMISSION_2	Firewall Region 15 Permission 2 Register	4504 71ECh

Table 23-84. DRU_FW Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_D RU_FW Physical Address
1F0h	FW0_FW_REGION_15_START_ADDRESS_I	Firewall Region 15 Start Address Low Register	4504 71F0h
1F4h	FW0_FW_REGION_15_START_ADDRESS_H	Firewall Region 15 Start Address High Register	4504 71F4h
1F8h	FW0_FW_REGION_15_END_ADDRESS_I	Firewall Region 15 End Address Low Register	4504 71F8h
1FCh	FW0_FW_REGION_15_END_ADDRESS_H	Firewall Region 15 End Address High Register	4504 71FCh

23.1.1 FW0_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = X]

FW0_FW_REGION_0_CONTROL is shown in [Figure 23-41](#) and described in [Table 23-86](#).

Return to [Summary Table](#).

The FW Region 0 Control Register defines the control fields for the slave fw0 region 0 firewall.

Table 23-85. FW0_FW_REGION_0_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7000h

Figure 23-41. FW0_FW_REGION_0_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-86. FW0_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-87. Register Call Summary for FW0_FW_REGION_0_CONTROL

DRU_FW Registers
<ul style="list-style-type: none"> FW0_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = X]: [0] DRU_DMA_FW Registers: [0]

23.1.2 FW0_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = X]

FW0_FW_REGION_0_PERMISSION_0 is shown in Figure 23-42 and described in Table 23-89.

Return to [Summary Table](#).

The FW Region 0 Permission 0 Register defines the permissions for the slave fw0 region 0 firewall.

**Table 23-88. FW0_FW_REGION_0_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7004h

Figure 23-42. FW0_FW_REGION_0_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-89. FW0_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-89. FW0_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-90. Register Call Summary for FW0_FW_REGION_0_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_0_PERMISSION_0 Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.3 FW0_FW_REGION_0_PERMISSION_1 Register (Offset = 8h) [reset = X]

FW0_FW_REGION_0_PERMISSION_1 is shown in Figure 23-43 and described in Table 23-92.

Return to [Summary Table](#).

The FW Region 0 Permission 1 Register defines the permissions for the slave fw0 region 0 firewall.

**Table 23-91. FW0_FW_REGION_0_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7008h

Figure 23-43. FW0_FW_REGION_0_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-92. FW0_FW_REGION_0_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-92. FW0_FW_REGION_0_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-93. Register Call Summary for FW0_FW_REGION_0_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_0_PERMISSION_1 Register \(Offset = 8h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.4 FW0_FW_REGION_0_PERMISSION_2 Register (Offset = Ch) [reset = X]

FW0_FW_REGION_0_PERMISSION_2 is shown in Figure 23-44 and described in Table 23-95.

Return to [Summary Table](#).

The FW Region 0 Permission 2 Register defines the permissions for the slave fw0 region 0 firewall.

**Table 23-94. FW0_FW_REGION_0_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 700Ch

Figure 23-44. FW0_FW_REGION_0_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-95. FW0_FW_REGION_0_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-95. FW0_FW_REGION_0_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-96. Register Call Summary for FW0_FW_REGION_0_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_0_PERMISSION_2 Register \(Offset = Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.5 FW0_FW_REGION_0_START_ADDRESS_I Register (Offset = 10h) [reset = 0h]

[FW0_FW_REGION_0_START_ADDRESS_I](#) is shown in [Figure 23-45](#) and described in [Table 23-98](#).

Return to [Summary Table](#).

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 0 firewall.

Table 23-97.
FW0_FW_REGION_0_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7010h

Figure 23-45. FW0_FW_REGION_0_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-98. FW0_FW_REGION_0_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-99. Register Call Summary for FW0_FW_REGION_0_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_0_START_ADDRESS_I Register \(Offset = 10h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.6 FW0_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = X]

FW0_FW_REGION_0_START_ADDRESS_H is shown in Figure 23-46 and described in Table 23-101.

Return to [Summary Table](#).

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 0 firewall.

Table 23-100.
FW0_FW_REGION_0_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7014h

Figure 23-46. FW0_FW_REGION_0_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-101. FW0_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-102. Register Call Summary for FW0_FW_REGION_0_START_ADDRESS_H

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_0_START_ADDRESS_H Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

23.1.7 FW0_FW_REGION_0_END_ADDRESS_I Register (Offset = 18h) [reset = FFFh]

FW0_FW_REGION_0_END_ADDRESS_I is shown in [Figure 23-47](#) and described in [Table 23-104](#).

Return to [Summary Table](#).

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 0 firewall.

Table 23-103.
FW0_FW_REGION_0_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7018h

Figure 23-47. FW0_FW_REGION_0_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-104. FW0_FW_REGION_0_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-105. Register Call Summary for FW0_FW_REGION_0_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_0_END_ADDRESS_I Register \(Offset = 18h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.8 FW0_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = X]

FW0_FW_REGION_0_END_ADDRESS_H is shown in [Figure 23-48](#) and described in [Table 23-107](#).

Return to [Summary Table](#).

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 0 firewall.

Table 23-106.
FW0_FW_REGION_0_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 701Ch

Figure 23-48. FW0_FW_REGION_0_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-107. FW0_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-108. Register Call Summary for FW0_FW_REGION_0_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_0_END_ADDRESS_H Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.9 FW0_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = X]

FW0_FW_REGION_1_CONTROL is shown in [Figure 23-49](#) and described in [Table 23-110](#).

Return to [Summary Table](#).

The FW Region 1 Control Register defines the control fields for the slave fw0 region 1 firewall.

**Table 23-109. FW0_FW_REGION_1_CONTROL
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7020h

Figure 23-49. FW0_FW_REGION_1_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-110. FW0_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-111. Register Call Summary for FW0_FW_REGION_1_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_1_CONTROL Register \(Offset = 20h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.10 FW0_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = X]

FW0_FW_REGION_1_PERMISSION_0 is shown in Figure 23-50 and described in Table 23-113.

Return to [Summary Table](#).

The FW Region 1 Permission 0 Register defines the permissions for the slave fw0 region 1 firewall.

Table 23-112. FW0_FW_REGION_1_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7024h

Figure 23-50. FW0_FW_REGION_1_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-113. FW0_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-113. FW0_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-114. Register Call Summary for FW0_FW_REGION_1_PERMISSION_0

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_1_PERMISSION_0 Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)

23.1.11 FW0_FW_REGION_1_PERMISSION_1 Register (Offset = 28h) [reset = X]

FW0_FW_REGION_1_PERMISSION_1 is shown in Figure 23-51 and described in Table 23-116.

Return to [Summary Table](#).

The FW Region 1 Permission 1 Register defines the permissions for the slave fw0 region 1 firewall.

Table 23-115. FW0_FW_REGION_1_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7028h

Figure 23-51. FW0_FW_REGION_1_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-116. FW0_FW_REGION_1_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-116. FW0_FW_REGION_1_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-117. Register Call Summary for FW0_FW_REGION_1_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_1_PERMISSION_1 Register \(Offset = 28h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.12 FW0_FW_REGION_1_PERMISSION_2 Register (Offset = 2Ch) [reset = X]

FW0_FW_REGION_1_PERMISSION_2 is shown in Figure 23-52 and described in Table 23-119.

Return to [Summary Table](#).

The FW Region 1 Permission 2 Register defines the permissions for the slave fw0 region 1 firewall.

Table 23-118. FW0_FW_REGION_1_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 702Ch

Figure 23-52. FW0_FW_REGION_1_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-119. FW0_FW_REGION_1_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-119. FW0_FW_REGION_1_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-120. Register Call Summary for FW0_FW_REGION_1_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_1_PERMISSION_2 Register \(Offset = 2Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.13 FW0_FW_REGION_1_START_ADDRESS_I Register (Offset = 30h) [reset = 0h]

FW0_FW_REGION_1_START_ADDRESS_I is shown in [Figure 23-53](#) and described in [Table 23-122](#).

Return to [Summary Table](#).

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 1 firewall.

Table 23-121.
FW0_FW_REGION_1_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7030h

Figure 23-53. FW0_FW_REGION_1_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-122. FW0_FW_REGION_1_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-123. Register Call Summary for FW0_FW_REGION_1_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_1_START_ADDRESS_I Register \(Offset = 30h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.14 FW0_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = X]

FW0_FW_REGION_1_START_ADDRESS_H is shown in [Figure 23-54](#) and described in [Table 23-125](#).

Return to [Summary Table](#).

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 1 firewall.

Table 23-124.
FW0_FW_REGION_1_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7034h

Figure 23-54. FW0_FW_REGION_1_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-125. FW0_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-126. Register Call Summary for FW0_FW_REGION_1_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_1_START_ADDRESS_H Register \(Offset = 34h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.15 FW0_FW_REGION_1_END_ADDRESS_I Register (Offset = 38h) [reset = FFFh]

FW0_FW_REGION_1_END_ADDRESS_I is shown in [Figure 23-55](#) and described in [Table 23-128](#).

Return to [Summary Table](#).

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 1 firewall.

Table 23-127.
FW0_FW_REGION_1_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7038h

Figure 23-55. FW0_FW_REGION_1_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-128. FW0_FW_REGION_1_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-129. Register Call Summary for FW0_FW_REGION_1_END_ADDRESS_I

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_1_END_ADDRESS_I Register \(Offset = 38h\) \[reset = FFFh\]: \[0\]](#)

23.1.16 FW0_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = X]

FW0_FW_REGION_1_END_ADDRESS_H is shown in Figure 23-56 and described in Table 23-131.

Return to [Summary Table](#).

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 1 firewall.

Table 23-130.
FW0_FW_REGION_1_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 703Ch

Figure 23-56. FW0_FW_REGION_1_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-131. FW0_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-132. Register Call Summary for FW0_FW_REGION_1_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_1_END_ADDRESS_H Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.17 FW0_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = X]

FW0_FW_REGION_2_CONTROL is shown in [Figure 23-57](#) and described in [Table 23-134](#).

Return to [Summary Table](#).

The FW Region 2 Control Register defines the control fields for the slave fw0 region 2 firewall.

Table 23-133. FW0_FW_REGION_2_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7040h

Figure 23-57. FW0_FW_REGION_2_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-134. FW0_FW_REGION_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-135. Register Call Summary for FW0_FW_REGION_2_CONTROL

DRU_FW Registers
<ul style="list-style-type: none"> FW0_FW_REGION_2_CONTROL Register (Offset = 40h) [reset = X]: [0] DRU_DMA_FW Registers: [0]

23.1.18 FW0_FW_REGION_2_PERMISSION_0 Register (Offset = 44h) [reset = X]

FW0_FW_REGION_2_PERMISSION_0 is shown in Figure 23-58 and described in Table 23-137.

Return to [Summary Table](#).

The FW Region 2 Permission 0 Register defines the permissions for the slave fw0 region 2 firewall.

**Table 23-136. FW0_FW_REGION_2_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7044h

Figure 23-58. FW0_FW_REGION_2_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-137. FW0_FW_REGION_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-137. FW0_FW_REGION_2_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-138. Register Call Summary for FW0_FW_REGION_2_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_2_PERMISSION_0 Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.19 FW0_FW_REGION_2_PERMISSION_1 Register (Offset = 48h) [reset = X]

FW0_FW_REGION_2_PERMISSION_1 is shown in Figure 23-59 and described in Table 23-140.

Return to [Summary Table](#).

The FW Region 2 Permission 1 Register defines the permissions for the slave fw0 region 2 firewall.

**Table 23-139. FW0_FW_REGION_2_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7048h

Figure 23-59. FW0_FW_REGION_2_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-140. FW0_FW_REGION_2_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-140. FW0_FW_REGION_2_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-141. Register Call Summary for FW0_FW_REGION_2_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_2_PERMISSION_1 Register \(Offset = 48h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.20 FW0_FW_REGION_2_PERMISSION_2 Register (Offset = 4Ch) [reset = X]

FW0_FW_REGION_2_PERMISSION_2 is shown in Figure 23-60 and described in Table 23-143.

Return to [Summary Table](#).

The FW Region 2 Permission 2 Register defines the permissions for the slave fw0 region 2 firewall.

**Table 23-142. FW0_FW_REGION_2_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 704Ch

Figure 23-60. FW0_FW_REGION_2_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-143. FW0_FW_REGION_2_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-143. FW0_FW_REGION_2_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-144. Register Call Summary for FW0_FW_REGION_2_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_2_PERMISSION_2 Register \(Offset = 4Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.21 FW0_FW_REGION_2_START_ADDRESS_I Register (Offset = 50h) [reset = 0h]

FW0_FW_REGION_2_START_ADDRESS_I is shown in Figure 23-61 and described in Table 23-146.

Return to [Summary Table](#).

The FW Region 2 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 2 firewall.

Table 23-145.
FW0_FW_REGION_2_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7050h

Figure 23-61. FW0_FW_REGION_2_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-146. FW0_FW_REGION_2_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-147. Register Call Summary for FW0_FW_REGION_2_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_2_START_ADDRESS_I Register \(Offset = 50h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.22 FW0_FW_REGION_2_START_ADDRESS_H Register (Offset = 54h) [reset = X]

FW0_FW_REGION_2_START_ADDRESS_H is shown in [Figure 23-62](#) and described in [Table 23-149](#).

Return to [Summary Table](#).

The FW Region 2 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 2 firewall.

Table 23-148.
FW0_FW_REGION_2_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7054h

Figure 23-62. FW0_FW_REGION_2_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-149. FW0_FW_REGION_2_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-150. Register Call Summary for FW0_FW_REGION_2_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_2_START_ADDRESS_H Register \(Offset = 54h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.23 FW0_FW_REGION_2_END_ADDRESS_I Register (Offset = 58h) [reset = FFFh]

FW0_FW_REGION_2_END_ADDRESS_I is shown in [Figure 23-63](#) and described in [Table 23-152](#).

Return to [Summary Table](#).

The FW Region 2 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 2 firewall.

Table 23-151.
FW0_FW_REGION_2_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7058h

Figure 23-63. FW0_FW_REGION_2_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-152. FW0_FW_REGION_2_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-153. Register Call Summary for FW0_FW_REGION_2_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_2_END_ADDRESS_I Register \(Offset = 58h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.24 FW0_FW_REGION_2_END_ADDRESS_H Register (Offset = 5Ch) [reset = X]

FW0_FW_REGION_2_END_ADDRESS_H is shown in [Figure 23-64](#) and described in [Table 23-155](#).

Return to [Summary Table](#).

The FW Region 2 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 2 firewall.

Table 23-154.
FW0_FW_REGION_2_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 705Ch

Figure 23-64. FW0_FW_REGION_2_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-155. FW0_FW_REGION_2_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-156. Register Call Summary for FW0_FW_REGION_2_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_2_END_ADDRESS_H Register \(Offset = 5Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.25 FW0_FW_REGION_3_CONTROL Register (Offset = 60h) [reset = X]

FW0_FW_REGION_3_CONTROL is shown in [Figure 23-65](#) and described in [Table 23-158](#).

Return to [Summary Table](#).

The FW Region 3 Control Register defines the control fields for the slave fw0 region 3 firewall.

**Table 23-157. FW0_FW_REGION_3_CONTROL
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7060h

Figure 23-65. FW0_FW_REGION_3_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-158. FW0_FW_REGION_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-159. Register Call Summary for FW0_FW_REGION_3_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_3_CONTROL Register \(Offset = 60h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.26 FW0_FW_REGION_3_PERMISSION_0 Register (Offset = 64h) [reset = X]

FW0_FW_REGION_3_PERMISSION_0 is shown in Figure 23-66 and described in Table 23-161.

Return to [Summary Table](#).

The FW Region 3 Permission 0 Register defines the permissions for the slave fw0 region 3 firewall.

Table 23-160. FW0_FW_REGION_3_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7064h

Figure 23-66. FW0_FW_REGION_3_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-161. FW0_FW_REGION_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-161. FW0_FW_REGION_3_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-162. Register Call Summary for FW0_FW_REGION_3_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_3_PERMISSION_0 Register \(Offset = 64h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.27 FW0_FW_REGION_3_PERMISSION_1 Register (Offset = 68h) [reset = X]

FW0_FW_REGION_3_PERMISSION_1 is shown in Figure 23-67 and described in Table 23-164.

Return to [Summary Table](#).

The FW Region 3 Permission 1 Register defines the permissions for the slave fw0 region 3 firewall.

Table 23-163. FW0_FW_REGION_3_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7068h

Figure 23-67. FW0_FW_REGION_3_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-164. FW0_FW_REGION_3_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-164. FW0_FW_REGION_3_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-165. Register Call Summary for FW0_FW_REGION_3_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_3_PERMISSION_1 Register \(Offset = 68h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.28 FW0_FW_REGION_3_PERMISSION_2 Register (Offset = 6Ch) [reset = X]

FW0_FW_REGION_3_PERMISSION_2 is shown in Figure 23-68 and described in Table 23-167.

Return to [Summary Table](#).

The FW Region 3 Permission 2 Register defines the permissions for the slave fw0 region 3 firewall.

Table 23-166. FW0_FW_REGION_3_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 706Ch

Figure 23-68. FW0_FW_REGION_3_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-167. FW0_FW_REGION_3_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-167. FW0_FW_REGION_3_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-168. Register Call Summary for FW0_FW_REGION_3_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_3_PERMISSION_2 Register \(Offset = 6Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.29 FW0_FW_REGION_3_START_ADDRESS_I Register (Offset = 70h) [reset = 0h]

FW0_FW_REGION_3_START_ADDRESS_I is shown in [Figure 23-69](#) and described in [Table 23-170](#).

Return to [Summary Table](#).

The FW Region 3 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 3 firewall.

Table 23-169.
FW0_FW_REGION_3_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7070h

Figure 23-69. FW0_FW_REGION_3_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-170. FW0_FW_REGION_3_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-171. Register Call Summary for FW0_FW_REGION_3_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_3_START_ADDRESS_I Register \(Offset = 70h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.30 FW0_FW_REGION_3_START_ADDRESS_H Register (Offset = 74h) [reset = X]

FW0_FW_REGION_3_START_ADDRESS_H is shown in [Figure 23-70](#) and described in [Table 23-173](#).

Return to [Summary Table](#).

The FW Region 3 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 3 firewall.

Table 23-172.
FW0_FW_REGION_3_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7074h

Figure 23-70. FW0_FW_REGION_3_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-173. FW0_FW_REGION_3_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-174. Register Call Summary for FW0_FW_REGION_3_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_3_START_ADDRESS_H Register \(Offset = 74h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.31 FW0_FW_REGION_3_END_ADDRESS_I Register (Offset = 78h) [reset = FFFh]

FW0_FW_REGION_3_END_ADDRESS_I is shown in [Figure 23-71](#) and described in [Table 23-176](#).

Return to [Summary Table](#).

The FW Region 3 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 3 firewall.

Table 23-175.
FW0_FW_REGION_3_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7078h

Figure 23-71. FW0_FW_REGION_3_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-176. FW0_FW_REGION_3_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-177. Register Call Summary for FW0_FW_REGION_3_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_3_END_ADDRESS_I Register \(Offset = 78h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.32 FW0_FW_REGION_3_END_ADDRESS_H Register (Offset = 7Ch) [reset = X]

FW0_FW_REGION_3_END_ADDRESS_H is shown in Figure 23-72 and described in Table 23-179.

Return to [Summary Table](#).

The FW Region 3 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 3 firewall.

Table 23-178.
FW0_FW_REGION_3_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 707Ch

Figure 23-72. FW0_FW_REGION_3_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-179. FW0_FW_REGION_3_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-180. Register Call Summary for FW0_FW_REGION_3_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_3_END_ADDRESS_H Register \(Offset = 7Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.33 FW0_FW_REGION_4_CONTROL Register (Offset = 80h) [reset = X]

FW0_FW_REGION_4_CONTROL is shown in [Figure 23-73](#) and described in [Table 23-182](#).

Return to [Summary Table](#).

The FW Region 4 Control Register defines the control fields for the slave fw0 region 4 firewall.

Table 23-181. FW0_FW_REGION_4_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7080h

Figure 23-73. FW0_FW_REGION_4_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-182. FW0_FW_REGION_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-183. Register Call Summary for FW0_FW_REGION_4_CONTROL

DRU_FW Registers
<ul style="list-style-type: none"> FW0_FW_REGION_4_CONTROL Register (Offset = 80h) [reset = X]: [0] DRU_DMA_FW Registers: [0]

23.1.34 FW0_FW_REGION_4_PERMISSION_0 Register (Offset = 84h) [reset = X]

FW0_FW_REGION_4_PERMISSION_0 is shown in Figure 23-74 and described in Table 23-185.

Return to [Summary Table](#).

The FW Region 4 Permission 0 Register defines the permissions for the slave fw0 region 4 firewall.

**Table 23-184. FW0_FW_REGION_4_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7084h

Figure 23-74. FW0_FW_REGION_4_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-185. FW0_FW_REGION_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-185. FW0_FW_REGION_4_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-186. Register Call Summary for FW0_FW_REGION_4_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_4_PERMISSION_0 Register \(Offset = 84h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.35 FW0_FW_REGION_4_PERMISSION_1 Register (Offset = 88h) [reset = X]

FW0_FW_REGION_4_PERMISSION_1 is shown in Figure 23-75 and described in Table 23-188.

Return to [Summary Table](#).

The FW Region 4 Permission 1 Register defines the permissions for the slave fw0 region 4 firewall.

**Table 23-187. FW0_FW_REGION_4_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7088h

Figure 23-75. FW0_FW_REGION_4_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-188. FW0_FW_REGION_4_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-188. FW0_FW_REGION_4_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-189. Register Call Summary for FW0_FW_REGION_4_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_4_PERMISSION_1 Register \(Offset = 88h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.36 FW0_FW_REGION_4_PERMISSION_2 Register (Offset = 8Ch) [reset = X]

FW0_FW_REGION_4_PERMISSION_2 is shown in Figure 23-76 and described in Table 23-191.

Return to [Summary Table](#).

The FW Region 4 Permission 2 Register defines the permissions for the slave fw0 region 4 firewall.

**Table 23-190. FW0_FW_REGION_4_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 708Ch

Figure 23-76. FW0_FW_REGION_4_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-191. FW0_FW_REGION_4_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-191. FW0_FW_REGION_4_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-192. Register Call Summary for FW0_FW_REGION_4_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_4_PERMISSION_2 Register \(Offset = 8Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.37 FW0_FW_REGION_4_START_ADDRESS_I Register (Offset = 90h) [reset = 0h]

FW0_FW_REGION_4_START_ADDRESS_I is shown in [Figure 23-77](#) and described in [Table 23-194](#).

Return to [Summary Table](#).

The FW Region 4 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 4 firewall.

Table 23-193.
FW0_FW_REGION_4_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7090h

Figure 23-77. FW0_FW_REGION_4_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-194. FW0_FW_REGION_4_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-195. Register Call Summary for FW0_FW_REGION_4_START_ADDRESS_I

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_4_START_ADDRESS_I Register \(Offset = 90h\) \[reset = 0h\]: \[0\]](#)

23.1.38 FW0_FW_REGION_4_START_ADDRESS_H Register (Offset = 94h) [reset = X]

FW0_FW_REGION_4_START_ADDRESS_H is shown in [Figure 23-78](#) and described in [Table 23-197](#).

Return to [Summary Table](#).

The FW Region 4 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 4 firewall.

Table 23-196.
FW0_FW_REGION_4_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7094h

Figure 23-78. FW0_FW_REGION_4_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-197. FW0_FW_REGION_4_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-198. Register Call Summary for FW0_FW_REGION_4_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_4_START_ADDRESS_H Register \(Offset = 94h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.39 FW0_FW_REGION_4_END_ADDRESS_I Register (Offset = 98h) [reset = FFFh]

FW0_FW_REGION_4_END_ADDRESS_I is shown in [Figure 23-79](#) and described in [Table 23-200](#).

Return to [Summary Table](#).

The FW Region 4 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 4 firewall.

Table 23-199.
FW0_FW_REGION_4_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7098h

Figure 23-79. FW0_FW_REGION_4_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-200. FW0_FW_REGION_4_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-201. Register Call Summary for FW0_FW_REGION_4_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_4_END_ADDRESS_I Register \(Offset = 98h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.40 FW0_FW_REGION_4_END_ADDRESS_H Register (Offset = 9Ch) [reset = X]

FW0_FW_REGION_4_END_ADDRESS_H is shown in Figure 23-80 and described in Table 23-203.

Return to [Summary Table](#).

The FW Region 4 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 4 firewall.

Table 23-202.
FW0_FW_REGION_4_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 709Ch

Figure 23-80. FW0_FW_REGION_4_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-203. FW0_FW_REGION_4_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-204. Register Call Summary for FW0_FW_REGION_4_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_4_END_ADDRESS_H Register \(Offset = 9Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.41 FW0_FW_REGION_5_CONTROL Register (Offset = A0h) [reset = X]

FW0_FW_REGION_5_CONTROL is shown in [Figure 23-81](#) and described in [Table 23-206](#).

Return to [Summary Table](#).

The FW Region 5 Control Register defines the control fields for the slave fw0 region 5 firewall.

**Table 23-205. FW0_FW_REGION_5_CONTROL
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70A0h

Figure 23-81. FW0_FW_REGION_5_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-206. FW0_FW_REGION_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-207. Register Call Summary for FW0_FW_REGION_5_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_5_CONTROL Register \(Offset = A0h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.42 FW0_FW_REGION_5_PERMISSION_0 Register (Offset = A4h) [reset = X]

FW0_FW_REGION_5_PERMISSION_0 is shown in [Figure 23-82](#) and described in [Table 23-209](#).

Return to [Summary Table](#).

The FW Region 5 Permission 0 Register defines the permissions for the slave fw0 region 5 firewall.

Table 23-208. FW0_FW_REGION_5_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70A4h

Figure 23-82. FW0_FW_REGION_5_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-209. FW0_FW_REGION_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-209. FW0_FW_REGION_5_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-210. Register Call Summary for FW0_FW_REGION_5_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_5_PERMISSION_0 Register \(Offset = A4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.43 FW0_FW_REGION_5_PERMISSION_1 Register (Offset = A8h) [reset = X]

FW0_FW_REGION_5_PERMISSION_1 is shown in Figure 23-83 and described in Table 23-212.

Return to [Summary Table](#).

The FW Region 5 Permission 1 Register defines the permissions for the slave fw0 region 5 firewall.

Table 23-211. FW0_FW_REGION_5_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70A8h

Figure 23-83. FW0_FW_REGION_5_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-212. FW0_FW_REGION_5_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-212. FW0_FW_REGION_5_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-213. Register Call Summary for FW0_FW_REGION_5_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_5_PERMISSION_1 Register \(Offset = A8h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.44 FW0_FW_REGION_5_PERMISSION_2 Register (Offset = ACh) [reset = X]

FW0_FW_REGION_5_PERMISSION_2 is shown in Figure 23-84 and described in Table 23-215.

Return to [Summary Table](#).

The FW Region 5 Permission 2 Register defines the permissions for the slave fw0 region 5 firewall.

Table 23-214. FW0_FW_REGION_5_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70ACh

Figure 23-84. FW0_FW_REGION_5_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-215. FW0_FW_REGION_5_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-215. FW0_FW_REGION_5_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-216. Register Call Summary for FW0_FW_REGION_5_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_5_PERMISSION_2 Register \(Offset = ACh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.45 FW0_FW_REGION_5_START_ADDRESS_I Register (Offset = B0h) [reset = 0h]

FW0_FW_REGION_5_START_ADDRESS_I is shown in Figure 23-85 and described in Table 23-218.

Return to [Summary Table](#).

The FW Region 5 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 5 firewall.

Table 23-217.
FW0_FW_REGION_5_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70B0h

Figure 23-85. FW0_FW_REGION_5_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-218. FW0_FW_REGION_5_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-219. Register Call Summary for FW0_FW_REGION_5_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_5_START_ADDRESS_I Register \(Offset = B0h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.46 FW0_FW_REGION_5_START_ADDRESS_H Register (Offset = B4h) [reset = X]

FW0_FW_REGION_5_START_ADDRESS_H is shown in [Figure 23-86](#) and described in [Table 23-221](#).

Return to [Summary Table](#).

The FW Region 5 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 5 firewall.

Table 23-220.
FW0_FW_REGION_5_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70B4h

Figure 23-86. FW0_FW_REGION_5_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-221. FW0_FW_REGION_5_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-222. Register Call Summary for FW0_FW_REGION_5_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_5_START_ADDRESS_H Register \(Offset = B4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.47 FW0_FW_REGION_5_END_ADDRESS_I Register (Offset = B8h) [reset = FFFh]

FW0_FW_REGION_5_END_ADDRESS_I is shown in [Figure 23-87](#) and described in [Table 23-224](#).

Return to [Summary Table](#).

The FW Region 5 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 5 firewall.

Table 23-223.
FW0_FW_REGION_5_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70B8h

Figure 23-87. FW0_FW_REGION_5_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L								END_ADDRESS_LSB							
R/W-0h								R-FFFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-224. FW0_FW_REGION_5_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-225. Register Call Summary for FW0_FW_REGION_5_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_5_END_ADDRESS_I Register \(Offset = B8h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.48 FW0_FW_REGION_5_END_ADDRESS_H Register (Offset = BCh) [reset = X]

FW0_FW_REGION_5_END_ADDRESS_H is shown in [Figure 23-88](#) and described in [Table 23-227](#).

Return to [Summary Table](#).

The FW Region 5 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 5 firewall.

Table 23-226.
FW0_FW_REGION_5_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70BCh

Figure 23-88. FW0_FW_REGION_5_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-227. FW0_FW_REGION_5_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-228. Register Call Summary for FW0_FW_REGION_5_END_ADDRESS_H

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_5_END_ADDRESS_H Register \(Offset = BCh\) \[reset = X\]: \[0\]](#)

23.1.49 FW0_FW_REGION_6_CONTROL Register (Offset = C0h) [reset = X]

FW0_FW_REGION_6_CONTROL is shown in [Figure 23-89](#) and described in [Table 23-230](#).

Return to [Summary Table](#).

The FW Region 6 Control Register defines the control fields for the slave fw0 region 6 firewall.

Table 23-229. FW0_FW_REGION_6_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70C0h

Figure 23-89. FW0_FW_REGION_6_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-230. FW0_FW_REGION_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-231. Register Call Summary for FW0_FW_REGION_6_CONTROL

DRU_FW Registers
<ul style="list-style-type: none"> FW0_FW_REGION_6_CONTROL Register (Offset = C0h) [reset = X]: [0] DRU_DMA_FW Registers: [0]

23.1.50 FW0_FW_REGION_6_PERMISSION_0 Register (Offset = C4h) [reset = X]

FW0_FW_REGION_6_PERMISSION_0 is shown in Figure 23-90 and described in Table 23-233.

Return to [Summary Table](#).

The FW Region 6 Permission 0 Register defines the permissions for the slave fw0 region 6 firewall.

**Table 23-232. FW0_FW_REGION_6_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70C4h

Figure 23-90. FW0_FW_REGION_6_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-233. FW0_FW_REGION_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-233. FW0_FW_REGION_6_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-234. Register Call Summary for FW0_FW_REGION_6_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_6_PERMISSION_0 Register \(Offset = C4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.51 FW0_FW_REGION_6_PERMISSION_1 Register (Offset = C8h) [reset = X]

FW0_FW_REGION_6_PERMISSION_1 is shown in Figure 23-91 and described in Table 23-236.

Return to [Summary Table](#).

The FW Region 6 Permission 1 Register defines the permissions for the slave fw0 region 6 firewall.

**Table 23-235. FW0_FW_REGION_6_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70C8h

Figure 23-91. FW0_FW_REGION_6_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-236. FW0_FW_REGION_6_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-236. FW0_FW_REGION_6_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-237. Register Call Summary for FW0_FW_REGION_6_PERMISSION_1

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_6_PERMISSION_1 Register \(Offset = C8h\) \[reset = X\]: \[0\]](#)

23.1.52 FW0_FW_REGION_6_PERMISSION_2 Register (Offset = CCh) [reset = X]

FW0_FW_REGION_6_PERMISSION_2 is shown in Figure 23-92 and described in Table 23-239.

Return to [Summary Table](#).

The FW Region 6 Permission 2 Register defines the permissions for the slave fw0 region 6 firewall.

**Table 23-238. FW0_FW_REGION_6_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70CCh

Figure 23-92. FW0_FW_REGION_6_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-239. FW0_FW_REGION_6_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-239. FW0_FW_REGION_6_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-240. Register Call Summary for FW0_FW_REGION_6_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_6_PERMISSION_2 Register \(Offset = CCh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.53 FW0_FW_REGION_6_START_ADDRESS_I Register (Offset = D0h) [reset = 0h]

FW0_FW_REGION_6_START_ADDRESS_I is shown in [Figure 23-93](#) and described in [Table 23-242](#).

Return to [Summary Table](#).

The FW Region 6 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 6 firewall.

Table 23-241.
FW0_FW_REGION_6_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70D0h

Figure 23-93. FW0_FW_REGION_6_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-242. FW0_FW_REGION_6_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-243. Register Call Summary for FW0_FW_REGION_6_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_6_START_ADDRESS_I Register \(Offset = D0h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.54 FW0_FW_REGION_6_START_ADDRESS_H Register (Offset = D4h) [reset = X]

FW0_FW_REGION_6_START_ADDRESS_H is shown in Figure 23-94 and described in Table 23-245.

Return to [Summary Table](#).

The FW Region 6 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 6 firewall.

Table 23-244.
FW0_FW_REGION_6_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70D4h

Figure 23-94. FW0_FW_REGION_6_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-245. FW0_FW_REGION_6_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-246. Register Call Summary for FW0_FW_REGION_6_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_6_START_ADDRESS_H Register \(Offset = D4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.55 FW0_FW_REGION_6_END_ADDRESS_I Register (Offset = D8h) [reset = FFFh]

FW0_FW_REGION_6_END_ADDRESS_I is shown in [Figure 23-95](#) and described in [Table 23-248](#).

Return to [Summary Table](#).

The FW Region 6 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 6 firewall.

Table 23-247.
FW0_FW_REGION_6_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70D8h

Figure 23-95. FW0_FW_REGION_6_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-248. FW0_FW_REGION_6_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-249. Register Call Summary for FW0_FW_REGION_6_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_6_END_ADDRESS_I Register \(Offset = D8h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.56 FW0_FW_REGION_6_END_ADDRESS_H Register (Offset = DCh) [reset = X]

FW0_FW_REGION_6_END_ADDRESS_H is shown in [Figure 23-96](#) and described in [Table 23-251](#).

Return to [Summary Table](#).

The FW Region 6 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 6 firewall.

Table 23-250.
FW0_FW_REGION_6_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70DCh

Figure 23-96. FW0_FW_REGION_6_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-251. FW0_FW_REGION_6_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-252. Register Call Summary for FW0_FW_REGION_6_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_6_END_ADDRESS_H Register \(Offset = DCh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.57 FW0_FW_REGION_7_CONTROL Register (Offset = E0h) [reset = X]

FW0_FW_REGION_7_CONTROL is shown in [Figure 23-97](#) and described in [Table 23-254](#).

Return to [Summary Table](#).

The FW Region 7 Control Register defines the control fields for the slave fw0 region 7 firewall.

**Table 23-253. FW0_FW_REGION_7_CONTROL
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70E0h

Figure 23-97. FW0_FW_REGION_7_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-254. FW0_FW_REGION_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-255. Register Call Summary for FW0_FW_REGION_7_CONTROL

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_7_CONTROL Register \(Offset = E0h\) \[reset = X\]: \[0\]](#)

23.1.58 FW0_FW_REGION_7_PERMISSION_0 Register (Offset = E4h) [reset = X]

FW0_FW_REGION_7_PERMISSION_0 is shown in Figure 23-98 and described in Table 23-257.

Return to [Summary Table](#).

The FW Region 7 Permission 0 Register defines the permissions for the slave fw0 region 7 firewall.

Table 23-256. FW0_FW_REGION_7_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70E4h

Figure 23-98. FW0_FW_REGION_7_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-257. FW0_FW_REGION_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-257. FW0_FW_REGION_7_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-258. Register Call Summary for FW0_FW_REGION_7_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_7_PERMISSION_0 Register \(Offset = E4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.59 FW0_FW_REGION_7_PERMISSION_1 Register (Offset = E8h) [reset = X]

FW0_FW_REGION_7_PERMISSION_1 is shown in Figure 23-99 and described in Table 23-260.

Return to [Summary Table](#).

The FW Region 7 Permission 1 Register defines the permissions for the slave fw0 region 7 firewall.

Table 23-259. FW0_FW_REGION_7_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70E8h

Figure 23-99. FW0_FW_REGION_7_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-260. FW0_FW_REGION_7_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-260. FW0_FW_REGION_7_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-261. Register Call Summary for FW0_FW_REGION_7_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_7_PERMISSION_1 Register \(Offset = E8h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.60 FW0_FW_REGION_7_PERMISSION_2 Register (Offset = ECh) [reset = X]

FW0_FW_REGION_7_PERMISSION_2 is shown in Figure 23-100 and described in Table 23-263.

Return to [Summary Table](#).

The FW Region 7 Permission 2 Register defines the permissions for the slave fw0 region 7 firewall.

Table 23-262. FW0_FW_REGION_7_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70ECh

Figure 23-100. FW0_FW_REGION_7_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-263. FW0_FW_REGION_7_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-263. FW0_FW_REGION_7_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-264. Register Call Summary for FW0_FW_REGION_7_PERMISSION_2

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_7_PERMISSION_2 Register \(Offset = ECh\) \[reset = X\]: \[0\]](#)

23.1.61 FW0_FW_REGION_7_START_ADDRESS_I Register (Offset = F0h) [reset = 0h]

FW0_FW_REGION_7_START_ADDRESS_I is shown in [Figure 23-101](#) and described in [Table 23-266](#).

Return to [Summary Table](#).

The FW Region 7 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 7 firewall.

Table 23-265.
FW0_FW_REGION_7_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70F0h

Figure 23-101. FW0_FW_REGION_7_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-266. FW0_FW_REGION_7_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-267. Register Call Summary for FW0_FW_REGION_7_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_7_START_ADDRESS_I Register \(Offset = F0h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.62 FW0_FW_REGION_7_START_ADDRESS_H Register (Offset = F4h) [reset = X]

FW0_FW_REGION_7_START_ADDRESS_H is shown in [Figure 23-102](#) and described in [Table 23-269](#).

Return to [Summary Table](#).

The FW Region 7 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 7 firewall.

Table 23-268.
FW0_FW_REGION_7_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70F4h

Figure 23-102. FW0_FW_REGION_7_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-269. FW0_FW_REGION_7_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-270. Register Call Summary for FW0_FW_REGION_7_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_7_START_ADDRESS_H Register \(Offset = F4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.63 FW0_FW_REGION_7_END_ADDRESS_I Register (Offset = F8h) [reset = FFFh]

FW0_FW_REGION_7_END_ADDRESS_I is shown in [Figure 23-103](#) and described in [Table 23-272](#).

Return to [Summary Table](#).

The FW Region 7 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 7 firewall.

Table 23-271.
FW0_FW_REGION_7_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70F8h

Figure 23-103. FW0_FW_REGION_7_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-272. FW0_FW_REGION_7_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-273. Register Call Summary for FW0_FW_REGION_7_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_7_END_ADDRESS_I Register \(Offset = F8h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.64 FW0_FW_REGION_7_END_ADDRESS_H Register (Offset = FCh) [reset = X]

FW0_FW_REGION_7_END_ADDRESS_H is shown in [Figure 23-104](#) and described in [Table 23-275](#).

Return to [Summary Table](#).

The FW Region 7 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 7 firewall.

Table 23-274.
FW0_FW_REGION_7_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 70FCh

Figure 23-104. FW0_FW_REGION_7_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-275. FW0_FW_REGION_7_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-276. Register Call Summary for FW0_FW_REGION_7_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_7_END_ADDRESS_H Register \(Offset = FCh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.65 FW0_FW_REGION_8_CONTROL Register (Offset = 100h) [reset = X]

FW0_FW_REGION_8_CONTROL is shown in [Figure 23-105](#) and described in [Table 23-278](#).

Return to [Summary Table](#).

The FW Region 8 Control Register defines the control fields for the slave fw0 region 8 firewall.

Table 23-277. FW0_FW_REGION_8_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7100h

Figure 23-105. FW0_FW_REGION_8_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-278. FW0_FW_REGION_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-279. Register Call Summary for FW0_FW_REGION_8_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_8_CONTROL Register \(Offset = 100h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.66 FW0_FW_REGION_8_PERMISSION_0 Register (Offset = 104h) [reset = X]

FW0_FW_REGION_8_PERMISSION_0 is shown in Figure 23-106 and described in Table 23-281.

Return to [Summary Table](#).

The FW Region 8 Permission 0 Register defines the permissions for the slave fw0 region 8 firewall.

**Table 23-280. FW0_FW_REGION_8_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7104h

Figure 23-106. FW0_FW_REGION_8_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-281. FW0_FW_REGION_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-281. FW0_FW_REGION_8_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-282. Register Call Summary for FW0_FW_REGION_8_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_8_PERMISSION_0 Register \(Offset = 104h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.67 FW0_FW_REGION_8_PERMISSION_1 Register (Offset = 108h) [reset = X]

FW0_FW_REGION_8_PERMISSION_1 is shown in Figure 23-107 and described in Table 23-284.

Return to [Summary Table](#).

The FW Region 8 Permission 1 Register defines the permissions for the slave fw0 region 8 firewall.

**Table 23-283. FW0_FW_REGION_8_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7108h

Figure 23-107. FW0_FW_REGION_8_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-284. FW0_FW_REGION_8_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-284. FW0_FW_REGION_8_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-285. Register Call Summary for FW0_FW_REGION_8_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_8_PERMISSION_1 Register \(Offset = 108h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.68 FW0_FW_REGION_8_PERMISSION_2 Register (Offset = 10Ch) [reset = X]

FW0_FW_REGION_8_PERMISSION_2 is shown in Figure 23-108 and described in Table 23-287.

Return to [Summary Table](#).

The FW Region 8 Permission 2 Register defines the permissions for the slave fw0 region 8 firewall.

**Table 23-286. FW0_FW_REGION_8_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 710Ch

Figure 23-108. FW0_FW_REGION_8_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-287. FW0_FW_REGION_8_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-287. FW0_FW_REGION_8_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-288. Register Call Summary for FW0_FW_REGION_8_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_8_PERMISSION_2 Register \(Offset = 10Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.69 FW0_FW_REGION_8_START_ADDRESS_I Register (Offset = 110h) [reset = 0h]

FW0_FW_REGION_8_START_ADDRESS_I is shown in Figure 23-109 and described in Table 23-290.

Return to [Summary Table](#).

The FW Region 8 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 8 firewall.

Table 23-289.
FW0_FW_REGION_8_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7110h

Figure 23-109. FW0_FW_REGION_8_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-290. FW0_FW_REGION_8_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-291. Register Call Summary for FW0_FW_REGION_8_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_8_START_ADDRESS_I Register \(Offset = 110h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.70 FW0_FW_REGION_8_START_ADDRESS_H Register (Offset = 114h) [reset = X]

FW0_FW_REGION_8_START_ADDRESS_H is shown in Figure 23-110 and described in Table 23-293.

Return to [Summary Table](#).

The FW Region 8 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 8 firewall.

Table 23-292.
FW0_FW_REGION_8_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7114h

Figure 23-110. FW0_FW_REGION_8_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-293. FW0_FW_REGION_8_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-294. Register Call Summary for FW0_FW_REGION_8_START_ADDRESS_H

DRU_FW Registers

- [DRU_DMA_FW Registers](#): [0]
- [FW0_FW_REGION_8_START_ADDRESS_H Register \(Offset = 114h\) \[reset = X\]](#): [0]

23.1.71 FW0_FW_REGION_8_END_ADDRESS_I Register (Offset = 118h) [reset = FFFh]

FW0_FW_REGION_8_END_ADDRESS_I is shown in [Figure 23-111](#) and described in [Table 23-296](#).

Return to [Summary Table](#).

The FW Region 8 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 8 firewall.

Table 23-295.
FW0_FW_REGION_8_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7118h

Figure 23-111. FW0_FW_REGION_8_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-296. FW0_FW_REGION_8_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-297. Register Call Summary for FW0_FW_REGION_8_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_8_END_ADDRESS_I Register \(Offset = 118h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.72 FW0_FW_REGION_8_END_ADDRESS_H Register (Offset = 11Ch) [reset = X]

FW0_FW_REGION_8_END_ADDRESS_H is shown in [Figure 23-112](#) and described in [Table 23-299](#).

Return to [Summary Table](#).

The FW Region 8 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 8 firewall.

Table 23-298.
FW0_FW_REGION_8_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 711Ch

Figure 23-112. FW0_FW_REGION_8_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-299. FW0_FW_REGION_8_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-300. Register Call Summary for FW0_FW_REGION_8_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_8_END_ADDRESS_H Register \(Offset = 11Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.73 FW0_FW_REGION_9_CONTROL Register (Offset = 120h) [reset = X]

FW0_FW_REGION_9_CONTROL is shown in [Figure 23-113](#) and described in [Table 23-302](#).

Return to [Summary Table](#).

The FW Region 9 Control Register defines the control fields for the slave fw0 region 9 firewall.

**Table 23-301. FW0_FW_REGION_9_CONTROL
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7120h

Figure 23-113. FW0_FW_REGION_9_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-302. FW0_FW_REGION_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-303. Register Call Summary for FW0_FW_REGION_9_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_9_CONTROL Register \(Offset = 120h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.74 FW0_FW_REGION_9_PERMISSION_0 Register (Offset = 124h) [reset = X]

FW0_FW_REGION_9_PERMISSION_0 is shown in Figure 23-114 and described in Table 23-305.

Return to [Summary Table](#).

The FW Region 9 Permission 0 Register defines the permissions for the slave fw0 region 9 firewall.

Table 23-304. FW0_FW_REGION_9_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7124h

Figure 23-114. FW0_FW_REGION_9_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-305. FW0_FW_REGION_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-305. FW0_FW_REGION_9_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-306. Register Call Summary for FW0_FW_REGION_9_PERMISSION_0

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_9_PERMISSION_0 Register \(Offset = 124h\) \[reset = X\]: \[0\]](#)

23.1.75 FW0_FW_REGION_9_PERMISSION_1 Register (Offset = 128h) [reset = X]

FW0_FW_REGION_9_PERMISSION_1 is shown in Figure 23-115 and described in Table 23-308.

Return to [Summary Table](#).

The FW Region 9 Permission 1 Register defines the permissions for the slave fw0 region 9 firewall.

**Table 23-307. FW0_FW_REGION_9_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7128h

Figure 23-115. FW0_FW_REGION_9_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-308. FW0_FW_REGION_9_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-308. FW0_FW_REGION_9_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-309. Register Call Summary for FW0_FW_REGION_9_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_9_PERMISSION_1 Register \(Offset = 128h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.76 FW0_FW_REGION_9_PERMISSION_2 Register (Offset = 12Ch) [reset = X]

FW0_FW_REGION_9_PERMISSION_2 is shown in Figure 23-116 and described in Table 23-311.

Return to [Summary Table](#).

The FW Region 9 Permission 2 Register defines the permissions for the slave fw0 region 9 firewall.

**Table 23-310. FW0_FW_REGION_9_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 712Ch

Figure 23-116. FW0_FW_REGION_9_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-311. FW0_FW_REGION_9_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-311. FW0_FW_REGION_9_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-312. Register Call Summary for FW0_FW_REGION_9_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_9_PERMISSION_2 Register \(Offset = 12Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.77 FW0_FW_REGION_9_START_ADDRESS_I Register (Offset = 130h) [reset = 0h]

FW0_FW_REGION_9_START_ADDRESS_I is shown in Figure 23-117 and described in Table 23-314.

Return to [Summary Table](#).

The FW Region 9 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 9 firewall.

Table 23-313.
FW0_FW_REGION_9_START_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7130h

Figure 23-117. FW0_FW_REGION_9_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L								START_ADDRESS_LSB							
R/W-0h								R-0h							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-314. FW0_FW_REGION_9_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-315. Register Call Summary for FW0_FW_REGION_9_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_9_START_ADDRESS_I Register \(Offset = 130h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.78 FW0_FW_REGION_9_START_ADDRESS_H Register (Offset = 134h) [reset = X]

FW0_FW_REGION_9_START_ADDRESS_H is shown in [Figure 23-118](#) and described in [Table 23-317](#).

Return to [Summary Table](#).

The FW Region 9 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 9 firewall.

Table 23-316.
FW0_FW_REGION_9_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7134h

Figure 23-118. FW0_FW_REGION_9_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-317. FW0_FW_REGION_9_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-318. Register Call Summary for FW0_FW_REGION_9_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_9_START_ADDRESS_H Register \(Offset = 134h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.79 FW0_FW_REGION_9_END_ADDRESS_I Register (Offset = 138h) [reset = FFFh]

FW0_FW_REGION_9_END_ADDRESS_I is shown in [Figure 23-119](#) and described in [Table 23-320](#).

Return to [Summary Table](#).

The FW Region 9 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 9 firewall.

Table 23-319.
FW0_FW_REGION_9_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7138h

Figure 23-119. FW0_FW_REGION_9_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L								END_ADDRESS_LSB							
R/W-0h								R-FFFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-320. FW0_FW_REGION_9_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-321. Register Call Summary for FW0_FW_REGION_9_END_ADDRESS_I

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_9_END_ADDRESS_I Register \(Offset = 138h\) \[reset = FFFh\]: \[0\]](#)

23.1.80 FW0_FW_REGION_9_END_ADDRESS_H Register (Offset = 13Ch) [reset = X]

FW0_FW_REGION_9_END_ADDRESS_H is shown in Figure 23-120 and described in Table 23-323.

Return to [Summary Table](#).

The FW Region 9 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 9 firewall.

Table 23-322.
FW0_FW_REGION_9_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 713Ch

Figure 23-120. FW0_FW_REGION_9_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-323. FW0_FW_REGION_9_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-324. Register Call Summary for FW0_FW_REGION_9_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_9_END_ADDRESS_H Register \(Offset = 13Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.81 FW0_FW_REGION_10_CONTROL Register (Offset = 140h) [reset = X]

FW0_FW_REGION_10_CONTROL is shown in [Figure 23-121](#) and described in [Table 23-326](#).

Return to [Summary Table](#).

The FW Region 10 Control Register defines the control fields for the slave fw0 region 10 firewall.

Table 23-325. FW0_FW_REGION_10_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7140h

Figure 23-121. FW0_FW_REGION_10_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-326. FW0_FW_REGION_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-327. Register Call Summary for FW0_FW_REGION_10_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_10_CONTROL Register \(Offset = 140h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.82 FW0_FW_REGION_10_PERMISSION_0 Register (Offset = 144h) [reset = X]

FW0_FW_REGION_10_PERMISSION_0 is shown in Figure 23-122 and described in Table 23-329.

Return to [Summary Table](#).

The FW Region 10 Permission 0 Register defines the permissions for the slave fw0 region 10 firewall.

**Table 23-328. FW0_FW_REGION_10_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7144h

Figure 23-122. FW0_FW_REGION_10_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-329. FW0_FW_REGION_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-329. FW0_FW_REGION_10_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-330. Register Call Summary for FW0_FW_REGION_10_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_10_PERMISSION_0 Register \(Offset = 144h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.83 FW0_FW_REGION_10_PERMISSION_1 Register (Offset = 148h) [reset = X]

FW0_FW_REGION_10_PERMISSION_1 is shown in Figure 23-123 and described in Table 23-332.

Return to [Summary Table](#).

The FW Region 10 Permission 1 Register defines the permissions for the slave fw0 region 10 firewall.

Table 23-331. FW0_FW_REGION_10_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7148h

Figure 23-123. FW0_FW_REGION_10_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-332. FW0_FW_REGION_10_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-332. FW0_FW_REGION_10_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-333. Register Call Summary for FW0_FW_REGION_10_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_10_PERMISSION_1 Register \(Offset = 148h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.84 FW0_FW_REGION_10_PERMISSION_2 Register (Offset = 14Ch) [reset = X]

FW0_FW_REGION_10_PERMISSION_2 is shown in Figure 23-124 and described in Table 23-335.

Return to [Summary Table](#).

The FW Region 10 Permission 2 Register defines the permissions for the slave fw0 region 10 firewall.

**Table 23-334. FW0_FW_REGION_10_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 714Ch

Figure 23-124. FW0_FW_REGION_10_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-335. FW0_FW_REGION_10_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-335. FW0_FW_REGION_10_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-336. Register Call Summary for FW0_FW_REGION_10_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_10_PERMISSION_2 Register \(Offset = 14Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.85 FW0_FW_REGION_10_START_ADDRESS_I Register (Offset = 150h) [reset = 0h]

FW0_FW_REGION_10_START_ADDRESS_I is shown in Figure 23-125 and described in Table 23-338.

Return to [Summary Table](#).

The FW Region 10 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 10 firewall.

Table 23-337.
FW0_FW_REGION_10_START_ADDRESS_I
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7150h

Figure 23-125. FW0_FW_REGION_10_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-338. FW0_FW_REGION_10_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-339. Register Call Summary for FW0_FW_REGION_10_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_10_START_ADDRESS_I Register \(Offset = 150h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.86 FW0_FW_REGION_10_START_ADDRESS_H Register (Offset = 154h) [reset = X]

FW0_FW_REGION_10_START_ADDRESS_H is shown in Figure 23-126 and described in Table 23-341.

Return to [Summary Table](#).

The FW Region 10 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 10 firewall.

Table 23-340.
FW0_FW_REGION_10_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7154h

Figure 23-126. FW0_FW_REGION_10_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-341. FW0_FW_REGION_10_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-342. Register Call Summary for FW0_FW_REGION_10_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_10_START_ADDRESS_H Register \(Offset = 154h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.87 FW0_FW_REGION_10_END_ADDRESS_I Register (Offset = 158h) [reset = FFFh]

FW0_FW_REGION_10_END_ADDRESS_I is shown in Figure 23-127 and described in Table 23-344.

Return to [Summary Table](#).

The FW Region 10 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 10 firewall.

Table 23-343.
FW0_FW_REGION_10_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7158h

Figure 23-127. FW0_FW_REGION_10_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-344. FW0_FW_REGION_10_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-345. Register Call Summary for FW0_FW_REGION_10_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_10_END_ADDRESS_I Register \(Offset = 158h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.88 FW0_FW_REGION_10_END_ADDRESS_H Register (Offset = 15Ch) [reset = X]

FW0_FW_REGION_10_END_ADDRESS_H is shown in [Figure 23-128](#) and described in [Table 23-347](#).

Return to [Summary Table](#).

The FW Region 10 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 10 firewall.

Table 23-346.
FW0_FW_REGION_10_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 715Ch

Figure 23-128. FW0_FW_REGION_10_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-347. FW0_FW_REGION_10_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-348. Register Call Summary for FW0_FW_REGION_10_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_10_END_ADDRESS_H Register \(Offset = 15Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.89 FW0_FW_REGION_11_CONTROL Register (Offset = 160h) [reset = X]

FW0_FW_REGION_11_CONTROL is shown in [Figure 23-129](#) and described in [Table 23-350](#).

Return to [Summary Table](#).

The FW Region 11 Control Register defines the control fields for the slave fw0 region 11 firewall.

Table 23-349. FW0_FW_REGION_11_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7160h

Figure 23-129. FW0_FW_REGION_11_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-350. FW0_FW_REGION_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-351. Register Call Summary for FW0_FW_REGION_11_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_11_CONTROL Register \(Offset = 160h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.90 FW0_FW_REGION_11_PERMISSION_0 Register (Offset = 164h) [reset = X]

FW0_FW_REGION_11_PERMISSION_0 is shown in Figure 23-130 and described in Table 23-353.

Return to [Summary Table](#).

The FW Region 11 Permission 0 Register defines the permissions for the slave fw0 region 11 firewall.

Table 23-352. FW0_FW_REGION_11_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7164h

Figure 23-130. FW0_FW_REGION_11_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-353. FW0_FW_REGION_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-353. FW0_FW_REGION_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-354. Register Call Summary for FW0_FW_REGION_11_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_11_PERMISSION_0 Register \(Offset = 164h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.91 FW0_FW_REGION_11_PERMISSION_1 Register (Offset = 168h) [reset = X]

FW0_FW_REGION_11_PERMISSION_1 is shown in [Figure 23-131](#) and described in [Table 23-356](#).

Return to [Summary Table](#).

The FW Region 11 Permission 1 Register defines the permissions for the slave fw0 region 11 firewall.

Table 23-355. FW0_FW_REGION_11_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7168h

Figure 23-131. FW0_FW_REGION_11_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-356. FW0_FW_REGION_11_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-356. FW0_FW_REGION_11_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-357. Register Call Summary for FW0_FW_REGION_11_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_11_PERMISSION_1 Register \(Offset = 168h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.92 FW0_FW_REGION_11_PERMISSION_2 Register (Offset = 16Ch) [reset = X]

FW0_FW_REGION_11_PERMISSION_2 is shown in Figure 23-132 and described in Table 23-359.

Return to [Summary Table](#).

The FW Region 11 Permission 2 Register defines the permissions for the slave fw0 region 11 firewall.

Table 23-358. FW0_FW_REGION_11_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 716Ch

Figure 23-132. FW0_FW_REGION_11_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-359. FW0_FW_REGION_11_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-359. FW0_FW_REGION_11_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-360. Register Call Summary for FW0_FW_REGION_11_PERMISSION_2

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_11_PERMISSION_2 Register \(Offset = 16Ch\) \[reset = X\]: \[0\]](#)

23.1.93 FW0_FW_REGION_11_START_ADDRESS_I Register (Offset = 170h) [reset = 0h]

FW0_FW_REGION_11_START_ADDRESS_I is shown in Figure 23-133 and described in Table 23-362.

Return to [Summary Table](#).

The FW Region 11 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 11 firewall.

Table 23-361.
FW0_FW_REGION_11_START_ADDRESS_I
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7170h

Figure 23-133. FW0_FW_REGION_11_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-362. FW0_FW_REGION_11_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-363. Register Call Summary for FW0_FW_REGION_11_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_11_START_ADDRESS_I Register \(Offset = 170h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.94 FW0_FW_REGION_11_START_ADDRESS_H Register (Offset = 174h) [reset = X]

FW0_FW_REGION_11_START_ADDRESS_H is shown in [Figure 23-134](#) and described in [Table 23-365](#).

Return to [Summary Table](#).

The FW Region 11 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 11 firewall.

Table 23-364.
FW0_FW_REGION_11_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7174h

Figure 23-134. FW0_FW_REGION_11_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-365. FW0_FW_REGION_11_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-366. Register Call Summary for FW0_FW_REGION_11_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_11_START_ADDRESS_H Register \(Offset = 174h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.95 FW0_FW_REGION_11_END_ADDRESS_I Register (Offset = 178h) [reset = FFFh]

FW0_FW_REGION_11_END_ADDRESS_I is shown in Figure 23-135 and described in Table 23-368.

Return to [Summary Table](#).

The FW Region 11 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 11 firewall.

Table 23-367.
FW0_FW_REGION_11_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7178h

Figure 23-135. FW0_FW_REGION_11_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-368. FW0_FW_REGION_11_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-369. Register Call Summary for FW0_FW_REGION_11_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_11_END_ADDRESS_I Register \(Offset = 178h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.96 FW0_FW_REGION_11_END_ADDRESS_H Register (Offset = 17Ch) [reset = X]

FW0_FW_REGION_11_END_ADDRESS_H is shown in [Figure 23-136](#) and described in [Table 23-371](#).

Return to [Summary Table](#).

The FW Region 11 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 11 firewall.

Table 23-370.
FW0_FW_REGION_11_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 717Ch

Figure 23-136. FW0_FW_REGION_11_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-371. FW0_FW_REGION_11_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-372. Register Call Summary for FW0_FW_REGION_11_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_11_END_ADDRESS_H Register \(Offset = 17Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.97 FW0_FW_REGION_12_CONTROL Register (Offset = 180h) [reset = X]

FW0_FW_REGION_12_CONTROL is shown in [Figure 23-137](#) and described in [Table 23-374](#).

Return to [Summary Table](#).

The FW Region 12 Control Register defines the control fields for the slave fw0 region 12 firewall.

Table 23-373. FW0_FW_REGION_12_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7180h

Figure 23-137. FW0_FW_REGION_12_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-374. FW0_FW_REGION_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-375. Register Call Summary for FW0_FW_REGION_12_CONTROL

DRU_FW Registers
<ul style="list-style-type: none"> FW0_FW_REGION_12_CONTROL Register (Offset = 180h) [reset = X]: [0] DRU_DMA_FW Registers: [0]

23.1.98 FW0_FW_REGION_12_PERMISSION_0 Register (Offset = 184h) [reset = X]

FW0_FW_REGION_12_PERMISSION_0 is shown in Figure 23-138 and described in Table 23-377.

Return to [Summary Table](#).

The FW Region 12 Permission 0 Register defines the permissions for the slave fw0 region 12 firewall.

**Table 23-376. FW0_FW_REGION_12_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7184h

Figure 23-138. FW0_FW_REGION_12_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-377. FW0_FW_REGION_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-377. FW0_FW_REGION_12_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-378. Register Call Summary for FW0_FW_REGION_12_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_12_PERMISSION_0 Register \(Offset = 184h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.99 FW0_FW_REGION_12_PERMISSION_1 Register (Offset = 188h) [reset = X]

FW0_FW_REGION_12_PERMISSION_1 is shown in Figure 23-139 and described in Table 23-380.

Return to [Summary Table](#).

The FW Region 12 Permission 1 Register defines the permissions for the slave fw0 region 12 firewall.

**Table 23-379. FW0_FW_REGION_12_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7188h

Figure 23-139. FW0_FW_REGION_12_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-380. FW0_FW_REGION_12_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-380. FW0_FW_REGION_12_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-381. Register Call Summary for FW0_FW_REGION_12_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_12_PERMISSION_1 Register \(Offset = 188h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.100 FW0_FW_REGION_12_PERMISSION_2 Register (Offset = 18Ch) [reset = X]

FW0_FW_REGION_12_PERMISSION_2 is shown in Figure 23-140 and described in Table 23-383.

Return to [Summary Table](#).

The FW Region 12 Permission 2 Register defines the permissions for the slave fw0 region 12 firewall.

**Table 23-382. FW0_FW_REGION_12_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 718Ch

Figure 23-140. FW0_FW_REGION_12_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-383. FW0_FW_REGION_12_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-383. FW0_FW_REGION_12_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-384. Register Call Summary for FW0_FW_REGION_12_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_12_PERMISSION_2 Register \(Offset = 18Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.101 FW0_FW_REGION_12_START_ADDRESS_I Register (Offset = 190h) [reset = 0h]

FW0_FW_REGION_12_START_ADDRESS_I is shown in [Figure 23-141](#) and described in [Table 23-386](#).

Return to [Summary Table](#).

The FW Region 12 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 12 firewall.

Table 23-385.
FW0_FW_REGION_12_START_ADDRESS_I
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7190h

Figure 23-141. FW0_FW_REGION_12_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-386. FW0_FW_REGION_12_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-387. Register Call Summary for FW0_FW_REGION_12_START_ADDRESS_I

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_12_START_ADDRESS_I Register \(Offset = 190h\) \[reset = 0h\]: \[0\]](#)

23.1.102 FW0_FW_REGION_12_START_ADDRESS_H Register (Offset = 194h) [reset = X]

FW0_FW_REGION_12_START_ADDRESS_H is shown in [Figure 23-142](#) and described in [Table 23-389](#).

Return to [Summary Table](#).

The FW Region 12 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 12 firewall.

Table 23-388.
FW0_FW_REGION_12_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7194h

Figure 23-142. FW0_FW_REGION_12_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-389. FW0_FW_REGION_12_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-390. Register Call Summary for FW0_FW_REGION_12_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_12_START_ADDRESS_H Register \(Offset = 194h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.103 FW0_FW_REGION_12_END_ADDRESS_I Register (Offset = 198h) [reset = FFFh]

FW0_FW_REGION_12_END_ADDRESS_I is shown in Figure 23-143 and described in Table 23-392.

Return to [Summary Table](#).

The FW Region 12 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 12 firewall.

Table 23-391.
FW0_FW_REGION_12_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 7198h

Figure 23-143. FW0_FW_REGION_12_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-392. FW0_FW_REGION_12_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-393. Register Call Summary for FW0_FW_REGION_12_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_12_END_ADDRESS_I Register \(Offset = 198h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.104 FW0_FW_REGION_12_END_ADDRESS_H Register (Offset = 19Ch) [reset = X]

FW0_FW_REGION_12_END_ADDRESS_H is shown in Figure 23-144 and described in Table 23-395.

Return to [Summary Table](#).

The FW Region 12 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 12 firewall.

Table 23-394.
FW0_FW_REGION_12_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 719Ch

Figure 23-144. FW0_FW_REGION_12_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-395. FW0_FW_REGION_12_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-396. Register Call Summary for FW0_FW_REGION_12_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_12_END_ADDRESS_H Register \(Offset = 19Ch\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.105 FW0_FW_REGION_13_CONTROL Register (Offset = 1A0h) [reset = X]

FW0_FW_REGION_13_CONTROL is shown in [Figure 23-145](#) and described in [Table 23-398](#).

Return to [Summary Table](#).

The FW Region 13 Control Register defines the control fields for the slave fw0 region 13 firewall.

Table 23-397. FW0_FW_REGION_13_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71A0h

Figure 23-145. FW0_FW_REGION_13_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-398. FW0_FW_REGION_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-399. Register Call Summary for FW0_FW_REGION_13_CONTROL

DRU_FW Registers

- [FW0_FW_REGION_13_CONTROL Register \(Offset = 1A0h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.106 FW0_FW_REGION_13_PERMISSION_0 Register (Offset = 1A4h) [reset = X]

FW0_FW_REGION_13_PERMISSION_0 is shown in Figure 23-146 and described in Table 23-401.

Return to [Summary Table](#).

The FW Region 13 Permission 0 Register defines the permissions for the slave fw0 region 13 firewall.

Table 23-400. FW0_FW_REGION_13_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71A4h

Figure 23-146. FW0_FW_REGION_13_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-401. FW0_FW_REGION_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-401. FW0_FW_REGION_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-402. Register Call Summary for FW0_FW_REGION_13_PERMISSION_0

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_13_PERMISSION_0 Register \(Offset = 1A4h\) \[reset = X\]: \[0\]](#)

23.1.107 FW0_FW_REGION_13_PERMISSION_1 Register (Offset = 1A8h) [reset = X]

FW0_FW_REGION_13_PERMISSION_1 is shown in Figure 23-147 and described in Table 23-404.

Return to [Summary Table](#).

The FW Region 13 Permission 1 Register defines the permissions for the slave fw0 region 13 firewall.

Table 23-403. FW0_FW_REGION_13_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71A8h

Figure 23-147. FW0_FW_REGION_13_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-404. FW0_FW_REGION_13_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-404. FW0_FW_REGION_13_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-405. Register Call Summary for FW0_FW_REGION_13_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_13_PERMISSION_1 Register \(Offset = 1A8h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.108 FW0_FW_REGION_13_PERMISSION_2 Register (Offset = 1ACh) [reset = X]

FW0_FW_REGION_13_PERMISSION_2 is shown in Figure 23-148 and described in Table 23-407.

Return to [Summary Table](#).

The FW Region 13 Permission 2 Register defines the permissions for the slave fw0 region 13 firewall.

Table 23-406. FW0_FW_REGION_13_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71ACh

Figure 23-148. FW0_FW_REGION_13_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-407. FW0_FW_REGION_13_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-407. FW0_FW_REGION_13_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-408. Register Call Summary for FW0_FW_REGION_13_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_13_PERMISSION_2 Register \(Offset = 1ACh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.109 FW0_FW_REGION_13_START_ADDRESS_I Register (Offset = 1B0h) [reset = 0h]

FW0_FW_REGION_13_START_ADDRESS_I is shown in Figure 23-149 and described in Table 23-410.

Return to [Summary Table](#).

The FW Region 13 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 13 firewall.

Table 23-409.
FW0_FW_REGION_13_START_ADDRESS_I
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71B0h

Figure 23-149. FW0_FW_REGION_13_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-410. FW0_FW_REGION_13_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-411. Register Call Summary for FW0_FW_REGION_13_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_13_START_ADDRESS_I Register \(Offset = 1B0h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.110 FW0_FW_REGION_13_START_ADDRESS_H Register (Offset = 1B4h) [reset = X]

FW0_FW_REGION_13_START_ADDRESS_H is shown in [Figure 23-150](#) and described in [Table 23-413](#).

Return to [Summary Table](#).

The FW Region 13 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 13 firewall.

Table 23-412.
FW0_FW_REGION_13_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71B4h

Figure 23-150. FW0_FW_REGION_13_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-413. FW0_FW_REGION_13_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-414. Register Call Summary for FW0_FW_REGION_13_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_13_START_ADDRESS_H Register \(Offset = 1B4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.111 FW0_FW_REGION_13_END_ADDRESS_I Register (Offset = 1B8h) [reset = FFFh]

FW0_FW_REGION_13_END_ADDRESS_I is shown in Figure 23-151 and described in Table 23-416.

Return to [Summary Table](#).

The FW Region 13 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 13 firewall.

Table 23-415.
FW0_FW_REGION_13_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71B8h

Figure 23-151. FW0_FW_REGION_13_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-416. FW0_FW_REGION_13_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-417. Register Call Summary for FW0_FW_REGION_13_END_ADDRESS_I

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_13_END_ADDRESS_I Register \(Offset = 1B8h\) \[reset = FFFh\]: \[0\]](#)

23.1.112 FW0_FW_REGION_13_END_ADDRESS_H Register (Offset = 1BCh) [reset = X]

FW0_FW_REGION_13_END_ADDRESS_H is shown in [Figure 23-152](#) and described in [Table 23-419](#).

Return to [Summary Table](#).

The FW Region 13 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 13 firewall.

Table 23-418.
FW0_FW_REGION_13_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71BCh

Figure 23-152. FW0_FW_REGION_13_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-419. FW0_FW_REGION_13_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-420. Register Call Summary for FW0_FW_REGION_13_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_13_END_ADDRESS_H Register \(Offset = 1BCh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.113 FW0_FW_REGION_14_CONTROL Register (Offset = 1C0h) [reset = X]

FW0_FW_REGION_14_CONTROL is shown in [Figure 23-153](#) and described in [Table 23-422](#).

Return to [Summary Table](#).

The FW Region 14 Control Register defines the control fields for the slave fw0 region 14 firewall.

Table 23-421. FW0_FW_REGION_14_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71C0h

Figure 23-153. FW0_FW_REGION_14_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-422. FW0_FW_REGION_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-423. Register Call Summary for FW0_FW_REGION_14_CONTROL

DRU_FW Registers
<ul style="list-style-type: none"> FW0_FW_REGION_14_CONTROL Register (Offset = 1C0h) [reset = X]: [0] DRU_DMA_FW Registers: [0]

23.1.114 FW0_FW_REGION_14_PERMISSION_0 Register (Offset = 1C4h) [reset = X]

FW0_FW_REGION_14_PERMISSION_0 is shown in Figure 23-154 and described in Table 23-425.

Return to [Summary Table](#).

The FW Region 14 Permission 0 Register defines the permissions for the slave fw0 region 14 firewall.

**Table 23-424. FW0_FW_REGION_14_PERMISSION_0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71C4h

Figure 23-154. FW0_FW_REGION_14_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-425. FW0_FW_REGION_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-425. FW0_FW_REGION_14_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-426. Register Call Summary for FW0_FW_REGION_14_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_14_PERMISSION_0 Register \(Offset = 1C4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.115 FW0_FW_REGION_14_PERMISSION_1 Register (Offset = 1C8h) [reset = X]

FW0_FW_REGION_14_PERMISSION_1 is shown in Figure 23-155 and described in Table 23-428.

Return to [Summary Table](#).

The FW Region 14 Permission 1 Register defines the permissions for the slave fw0 region 14 firewall.

**Table 23-427. FW0_FW_REGION_14_PERMISSION_1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71C8h

Figure 23-155. FW0_FW_REGION_14_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-428. FW0_FW_REGION_14_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-428. FW0_FW_REGION_14_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-429. Register Call Summary for FW0_FW_REGION_14_PERMISSION_1

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_14_PERMISSION_1 Register \(Offset = 1C8h\) \[reset = X\]: \[0\]](#)

23.1.116 FW0_FW_REGION_14_PERMISSION_2 Register (Offset = 1CCh) [reset = X]

FW0_FW_REGION_14_PERMISSION_2 is shown in Figure 23-156 and described in Table 23-431.

Return to [Summary Table](#).

The FW Region 14 Permission 2 Register defines the permissions for the slave fw0 region 14 firewall.

**Table 23-430. FW0_FW_REGION_14_PERMISSION_2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71CCh

Figure 23-156. FW0_FW_REGION_14_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-431. FW0_FW_REGION_14_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-431. FW0_FW_REGION_14_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-432. Register Call Summary for FW0_FW_REGION_14_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_14_PERMISSION_2 Register \(Offset = 1CCh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.117 FW0_FW_REGION_14_START_ADDRESS_I Register (Offset = 1D0h) [reset = 0h]

FW0_FW_REGION_14_START_ADDRESS_I is shown in [Figure 23-157](#) and described in [Table 23-434](#).

Return to [Summary Table](#).

The FW Region 14 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 14 firewall.

Table 23-433.
FW0_FW_REGION_14_START_ADDRESS_I
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71D0h

Figure 23-157. FW0_FW_REGION_14_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-434. FW0_FW_REGION_14_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-435. Register Call Summary for FW0_FW_REGION_14_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_14_START_ADDRESS_I Register \(Offset = 1D0h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.118 FW0_FW_REGION_14_START_ADDRESS_H Register (Offset = 1D4h) [reset = X]

FW0_FW_REGION_14_START_ADDRESS_H is shown in [Figure 23-158](#) and described in [Table 23-437](#).

Return to [Summary Table](#).

The FW Region 14 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 14 firewall.

Table 23-436.
FW0_FW_REGION_14_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71D4h

Figure 23-158. FW0_FW_REGION_14_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-437. FW0_FW_REGION_14_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-438. Register Call Summary for FW0_FW_REGION_14_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_14_START_ADDRESS_H Register \(Offset = 1D4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.119 FW0_FW_REGION_14_END_ADDRESS_I Register (Offset = 1D8h) [reset = FFFh]

FW0_FW_REGION_14_END_ADDRESS_I is shown in Figure 23-159 and described in Table 23-440.

Return to [Summary Table](#).

The FW Region 14 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 14 firewall.

Table 23-439.
FW0_FW_REGION_14_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71D8h

Figure 23-159. FW0_FW_REGION_14_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-440. FW0_FW_REGION_14_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-441. Register Call Summary for FW0_FW_REGION_14_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_14_END_ADDRESS_I Register \(Offset = 1D8h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.120 FW0_FW_REGION_14_END_ADDRESS_H Register (Offset = 1DCh) [reset = X]

FW0_FW_REGION_14_END_ADDRESS_H is shown in Figure 23-160 and described in Table 23-443.

Return to [Summary Table](#).

The FW Region 14 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 14 firewall.

Table 23-442.
FW0_FW_REGION_14_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71DCh

Figure 23-160. FW0_FW_REGION_14_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-443. FW0_FW_REGION_14_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-444. Register Call Summary for FW0_FW_REGION_14_END_ADDRESS_H

DRU_FW Registers

- FW0_FW_REGION_14_END_ADDRESS_H Register (Offset = 1DCh) [reset = X]: [0]
- DRU_DMA_FW Registers: [0]

23.1.121 FW0_FW_REGION_15_CONTROL Register (Offset = 1E0h) [reset = X]

FW0_FW_REGION_15_CONTROL is shown in [Figure 23-161](#) and described in [Table 23-446](#).

Return to [Summary Table](#).

The FW Region 15 Control Register defines the control fields for the slave fw0 region 15 firewall.

Table 23-445. FW0_FW_REGION_15_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71E0h

Figure 23-161. FW0_FW_REGION_15_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-446. FW0_FW_REGION_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 backgroun region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-447. Register Call Summary for FW0_FW_REGION_15_CONTROL

DRU_FW Registers

- [DRU_DMA_FW Registers: \[0\]](#)
- [FW0_FW_REGION_15_CONTROL Register \(Offset = 1E0h\) \[reset = X\]: \[0\]](#)

23.1.122 FW0_FW_REGION_15_PERMISSION_0 Register (Offset = 1E4h) [reset = X]

FW0_FW_REGION_15_PERMISSION_0 is shown in Figure 23-162 and described in Table 23-449.

Return to [Summary Table](#).

The FW Region 15 Permission 0 Register defines the permissions for the slave fw0 region 15 firewall.

Table 23-448. FW0_FW_REGION_15_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71E4h

Figure 23-162. FW0_FW_REGION_15_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-449. FW0_FW_REGION_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-449. FW0_FW_REGION_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-450. Register Call Summary for FW0_FW_REGION_15_PERMISSION_0

DRU_FW Registers

- [FW0_FW_REGION_15_PERMISSION_0 Register \(Offset = 1E4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.123 FW0_FW_REGION_15_PERMISSION_1 Register (Offset = 1E8h) [reset = X]

FW0_FW_REGION_15_PERMISSION_1 is shown in Figure 23-163 and described in Table 23-452.

Return to [Summary Table](#).

The FW Region 15 Permission 1 Register defines the permissions for the slave fw0 region 15 firewall.

Table 23-451. FW0_FW_REGION_15_PERMISSION_1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71E8h

Figure 23-163. FW0_FW_REGION_15_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-452. FW0_FW_REGION_15_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-452. FW0_FW_REGION_15_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-453. Register Call Summary for FW0_FW_REGION_15_PERMISSION_1

DRU_FW Registers

- [FW0_FW_REGION_15_PERMISSION_1 Register \(Offset = 1E8h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.124 FW0_FW_REGION_15_PERMISSION_2 Register (Offset = 1ECh) [reset = X]

FW0_FW_REGION_15_PERMISSION_2 is shown in Figure 23-164 and described in Table 23-455.

Return to [Summary Table](#).

The FW Region 15 Permission 2 Register defines the permissions for the slave fw0 region 15 firewall.

Table 23-454. FW0_FW_REGION_15_PERMISSION_2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71ECh

Figure 23-164. FW0_FW_REGION_15_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-455. FW0_FW_REGION_15_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.

Table 23-455. FW0_FW_REGION_15_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-456. Register Call Summary for FW0_FW_REGION_15_PERMISSION_2

DRU_FW Registers

- [FW0_FW_REGION_15_PERMISSION_2 Register \(Offset = 1ECh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.125 FW0_FW_REGION_15_START_ADDRESS_I Register (Offset = 1F0h) [reset = 0h]

FW0_FW_REGION_15_START_ADDRESS_I is shown in Figure 23-165 and described in Table 23-458.

Return to [Summary Table](#).

The FW Region 15 Start Address Low Register defines the start address bits 31 to 0 for the slave fw0 region 15 firewall.

Table 23-457.
FW0_FW_REGION_15_START_ADDRESS_I
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71F0h

Figure 23-165. FW0_FW_REGION_15_START_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-458. FW0_FW_REGION_15_START_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-459. Register Call Summary for FW0_FW_REGION_15_START_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_15_START_ADDRESS_I Register \(Offset = 1F0h\) \[reset = 0h\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.126 FW0_FW_REGION_15_START_ADDRESS_H Register (Offset = 1F4h) [reset = X]

FW0_FW_REGION_15_START_ADDRESS_H is shown in [Figure 23-166](#) and described in [Table 23-461](#).

Return to [Summary Table](#).

The FW Region 15 Start Address High Register defines the start address bits 47 to 32 for the slave fw0 region 15 firewall.

Table 23-460.
FW0_FW_REGION_15_START_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71F4h

Figure 23-166. FW0_FW_REGION_15_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-461. FW0_FW_REGION_15_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-462. Register Call Summary for FW0_FW_REGION_15_START_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_15_START_ADDRESS_H Register \(Offset = 1F4h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.127 FW0_FW_REGION_15_END_ADDRESS_I Register (Offset = 1F8h) [reset = FFFh]

FW0_FW_REGION_15_END_ADDRESS_I is shown in Figure 23-167 and described in Table 23-464.

Return to [Summary Table](#).

The FW Region 15 End Address Low Register defines the end address bits 31 to 0 to include for the slave fw0 region 15 firewall.

Table 23-463.
FW0_FW_REGION_15_END_ADDRESS_I Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71F8h

Figure 23-167. FW0_FW_REGION_15_END_ADDRESS_I Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-0h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-464. FW0_FW_REGION_15_END_ADDRESS_I Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	0h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-465. Register Call Summary for FW0_FW_REGION_15_END_ADDRESS_I

DRU_FW Registers

- [FW0_FW_REGION_15_END_ADDRESS_I Register \(Offset = 1F8h\) \[reset = FFFh\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.1.128 FW0_FW_REGION_15_END_ADDRESS_H Register (Offset = 1FCh) [reset = X]

FW0_FW_REGION_15_END_ADDRESS_H is shown in [Figure 23-168](#) and described in [Table 23-467](#).

Return to [Summary Table](#).

The FW Region 15 End Address High Register defines the end address bits 47 to 32 to include for the slave fw0 region 15 firewall.

Table 23-466.
FW0_FW_REGION_15_END_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW	4504 71FCh

Figure 23-168. FW0_FW_REGION_15_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-467. FW0_FW_REGION_15_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-468. Register Call Summary for FW0_FW_REGION_15_END_ADDRESS_H

DRU_FW Registers

- [FW0_FW_REGION_15_END_ADDRESS_H Register \(Offset = 1FCh\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW Registers: \[0\]](#)

23.2 DRU_FW_GLB Registers

Table 23-470 lists the memory-mapped registers for the DRU_FW_GLB registers. All register offset addresses not listed in Table 23-470 should be considered as reserved locations and the register contents should not be modified.

Table 23-469. DRU_FW_GLB Instances

Instance	Base Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7000h

Table 23-470. DRU_FW_GLB Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_DRU_FW_GLB Physical Address
0h	PID	Revision Register	45B1 7000h
4h	DESTINATION_ID	Destination ID Register	45B1 7004h
20h	EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B1 7020h
24h	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B1 7024h
28h	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B1 7028h
2Ch	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B1 702Ch
30h	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B1 7030h
34h	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B1 7034h
38h	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B1 7038h
40h	EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B1 7040h
44h	EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B1 7044h

23.2.1 PID Register (Offset = 0h) [reset = 66083101h]

PID is shown in [Figure 23-169](#) and described in [Table 23-472](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 23-471. PID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GL B	45B1 7000h

Figure 23-169. PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME			BU		FUNC										
R-1h			R-2h		R-608h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-6h					R-1h			R-0h		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 23-472. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	Business Unit: 10 = Processors
27-16	FUNC	R	608h	Module ID
15-11	RTL	R	6h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	1h	Minor revision

Table 23-473. Register Call Summary for PID

DRU_FW_GLB Registers

- [DRU_DMA_FW_GLB Registers: \[0\]](#)
- [PID Register \(Offset = 0h\) \[reset = 66083101h\]: \[0\] \[1\]](#)

23.2.2 DESTINATION_ID Register (Offset = 4h) [reset = X]

DESTINATION_ID is shown in [Figure 23-170](#) and described in [Table 23-475](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

Table 23-474. DESTINATION_ID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7004h

Figure 23-170. DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEST_ID							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-475. DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

Table 23-476. Register Call Summary for DESTINATION_ID

DRU_FW_GLB Registers

- [DRU_DMA_FW_GLB Registers](#): [0]
- [DESTINATION_ID Register \(Offset = 4h\) \[reset = X\]](#): [0]

23.2.3 EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = X]

EXCEPTION_LOGGING_CONTROL is shown in [Figure 23-171](#) and described in [Table 23-478](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

**Table 23-477. EXCEPTION_LOGGING_CONTROL
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7020h

Figure 23-171. EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEN D	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-478. EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_PEND	R/W	0h	Disables logging pending when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

Table 23-479. Register Call Summary for EXCEPTION_LOGGING_CONTROL

DRU_FW_GLB Registers

- [EXCEPTION_LOGGING_CONTROL Register \(Offset = 20h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW_GLB Registers: \[0\]](#)

23.2.4 EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

EXCEPTION_LOGGING_HEADER0 is shown in [Figure 23-172](#) and described in [Table 23-481](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Table 23-480. EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7024h

Figure 23-172. EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID								DEST_ID															
R-0h								R-0h								R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-481. EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

Table 23-482. Register Call Summary for EXCEPTION_LOGGING_HEADER0

DRU_FW_GLB Registers

- EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]: [0]
- DRU_DMA_FW_GLB Registers: [0]

23.2.5 EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = X]

EXCEPTION_LOGGING_HEADER1 is shown in [Figure 23-173](#) and described in [Table 23-484](#).

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

**Table 23-483. EXCEPTION_LOGGING_HEADER1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7028h

Figure 23-173. EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; -n = value after reset

Table 23-484. EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code.
15-0	RESERVED	R	X	

Table 23-485. Register Call Summary for EXCEPTION_LOGGING_HEADER1

DRU_FW_GLB Registers

- EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = X]: [0]
- DRU_DMA_FW_GLB Registers: [0]

23.2.6 EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

EXCEPTION_LOGGING_DATA0 is shown in [Figure 23-174](#) and described in [Table 23-487](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

Table 23-486. EXCEPTION_LOGGING_DATA0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 702Ch

Figure 23-174. EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-487. EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

Table 23-488. Register Call Summary for EXCEPTION_LOGGING_DATA0

DRU_FW_GLB Registers

- [DRU_DMA_FW_GLB Registers: \[0\]](#)
- [EXCEPTION_LOGGING_DATA0 Register \(Offset = 2Ch\) \[reset = 0h\]: \[0\]](#)

23.2.7 EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = X]

EXCEPTION_LOGGING_DATA1 is shown in [Figure 23-175](#) and described in [Table 23-490](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

**Table 23-489. EXCEPTION_LOGGING_DATA1
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7030h

Figure 23-175. EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-490. EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 16 bits.

Table 23-491. Register Call Summary for EXCEPTION_LOGGING_DATA1

DRU_FW_GLB Registers

- EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = X]: [0]
- DRU_DMA_FW_GLB Registers: [0]

23.2.8 EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = X]

EXCEPTION_LOGGING_DATA2 is shown in [Figure 23-176](#) and described in [Table 23-493](#).

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

Table 23-492. EXCEPTION_LOGGING_DATA2 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7034h

Figure 23-176. EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 23-493. EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

Table 23-494. Register Call Summary for EXCEPTION_LOGGING_DATA2

DRU_FW_GLB Registers

- EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = X]: [0]
- DRU_DMA_FW_GLB Registers: [0]

23.2.9 EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = X]

EXCEPTION_LOGGING_DATA3 is shown in [Figure 23-177](#) and described in [Table 23-496](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the fourth word of the data.

**Table 23-495. EXCEPTION_LOGGING_DATA3
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7038h

Figure 23-177. EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						BYTECNT															
R-X																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-496. EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

Table 23-497. Register Call Summary for EXCEPTION_LOGGING_DATA3

DRU_FW_GLB Registers

- [EXCEPTION_LOGGING_DATA3 Register \(Offset = 38h\) \[reset = X\]: \[0\]](#)
- [DRU_DMA_FW_GLB Registers: \[0\]](#)

23.2.10 EXCEPTION_PEND_SET Register (Offset = 40h) [reset = X]

EXCEPTION_PEND_SET is shown in [Figure 23-178](#) and described in [Table 23-499](#).

Return to [Summary Table](#).

The Exception Logging Pending Set Register allows to set the pend signal.

Table 23-498. EXCEPTION_PEND_SET Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7040h

Figure 23-178. EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-499. EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

Table 23-500. Register Call Summary for EXCEPTION_PEND_SET

DRU_FW_GLB Registers

- [DRU_DMA_FW_GLB Registers: \[0\]](#)
- [EXCEPTION_PEND_SET Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)

23.2.11 EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = X]

EXCEPTION_PEND_CLEAR is shown in [Figure 23-179](#) and described in [Table 23-502](#).

Return to [Summary Table](#).

The Exception Logging Pending Clear Register allows to clear the pend signal.

Table 23-501. EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_FW_GLB	45B1 7044h

Figure 23-179. EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 23-502. EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

Table 23-503. Register Call Summary for EXCEPTION_PEND_CLEAR

DRU_FW_GLB Registers

- [DRU_DMA_FW_GLB Registers: \[0\]](#)
- [EXCEPTION_PEND_CLEAR Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)

23.3 DRU_MMR_FW Registers

Table 23-505 lists the memory-mapped registers for the DRU_MMR_FW registers. All register offset addresses not listed in Table 23-505 should be considered as reserved locations and the register contents should not be modified.

Table 23-504. DRU_MMR_FW Instances

Instance	Base Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 8000h

Table 23-505. DRU_MMR_FW Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0 DRU_MMR_FW Physical Address
0h	DRU_MMR_CFG_FW_REGION_0_CONTROL	Firewall Region 0 Control Register	4504 8000h
4h	DRU_MMR_CFG_FW_REGION_0_PERMISSION_0	Firewall Region 0 Permission 0 Register	4504 8004h
10h	DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L	Firewall Region 0 Start Address Low Register	4504 8010h
14h	DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H	Firewall Region 0 Start Address High Register	4504 8014h
18h	DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L	Firewall Region 0 End Address Low Register	4504 8018h
1Ch	DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H	Firewall Region 0 End Address High Register	4504 801Ch
20h	DRU_MMR_CFG_FW_REGION_1_CONTROL	Firewall Region 1 Control Register	4504 8020h
24h	DRU_MMR_CFG_FW_REGION_1_PERMISSION_0	Firewall Region 1 Permission 0 Register	4504 8024h
30h	DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L	Firewall Region 1 Start Address Low Register	4504 8030h
34h	DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H	Firewall Region 1 Start Address High Register	4504 8034h
38h	DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L	Firewall Region 1 End Address Low Register	4504 8038h
3Ch	DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H	Firewall Region 1 End Address High Register	4504 803Ch
4000h	DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL	Firewall Region 0 Channel 0 Control Register	4504 C000h
4004h	DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0	Firewall Region 0 Channel 0 Permission 0 Register	4504 C004h
4020h	DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL	Firewall Region 0 Channel 1 Control Register	4504 C020h
4024h	DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0	Firewall Region 0 Channel 1 Permission 0 Register	4504 C024h
4040h	DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL	Firewall Region 0 Channel 2 Control Register	4504 C040h
4044h	DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0	Firewall Region 0 Channel 2 Permission 0 Register	4504 C044h
4060h	DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL	Firewall Region 0 Channel 3 Control Register	4504 C060h
4064h	DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0	Firewall Region 0 Channel 3 Permission 0 Register	4504 C064h
4080h	DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL	Firewall Region 0 Channel 4 Control Register	4504 C080h
4084h	DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0	Firewall Region 0 Channel 4 Permission 0 Register	4504 C084h
40A0h	DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL	Firewall Region 0 Channel 5 Control Register	4504 C0A0h

Table 23-505. DRU_MMR_FW Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0 _DRU_MMR_FW Physical Address
40A4h	DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMIS SION_0	Firewall Region 0 Channel 5 Permission 0 Register	4504 C0A4h
40C0h	DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTR OL	Firewall Region 0 Channel 6 Control Register	4504 C0C0h
40C4h	DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMIS SION_0	Firewall Region 0 Channel 6 Permission 0 Register	4504 C0C4h
40E0h	DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTR OL	Firewall Region 0 Channel 7 Control Register	4504 C0E0h
40E4h	DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMIS SION_0	Firewall Region 0 Channel 7 Permission 0 Register	4504 C0E4h
4100h	DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTR OL	Firewall Region 0 Channel 8 Control Register	4504 C100h
4104h	DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMIS SION_0	Firewall Region 0 Channel 8 Permission 0 Register	4504 C104h
4120h	DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTR OL	Firewall Region 0 Channel 9 Control Register	4504 C120h
4124h	DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMIS SION_0	Firewall Region 0 Channel 9 Permission 0 Register	4504 C124h
4140h	DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTR OL	Firewall Region 0 Channel 10 Control Register	4504 C140h
4144h	DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMI SSION_0	Firewall Region 0 Channel 10 Permission 0 Register	4504 C144h
4160h	DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTR OL	Firewall Region 0 Channel 11 Control Register	4504 C160h
4164h	DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMI SSION_0	Firewall Region 0 Channel 11 Permission 0 Register	4504 C164h
4180h	DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTR OL	Firewall Region 0 Channel 12 Control Register	4504 C180h
4184h	DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMI SSION_0	Firewall Region 0 Channel 12 Permission 0 Register	4504 C184h
41A0h	DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTR OL	Firewall Region 0 Channel 13 Control Register	4504 C1A0h
41A4h	DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMI SSION_0	Firewall Region 0 Channel 13 Permission 0 Register	4504 C1A4h
41C0h	DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTR OL	Firewall Region 0 Channel 14 Control Register	4504 C1C0h
41C4h	DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMI SSION_0	Firewall Region 0 Channel 14 Permission 0 Register	4504 C1C4h
41E0h	DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTR OL	Firewall Region 0 Channel 15 Control Register	4504 C1E0h
41E4h	DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMI SSION_0	Firewall Region 0 Channel 15 Permission 0 Register	4504 C1E4h
4200h	DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTR OL	Firewall Region 0 Channel 16 Control Register	4504 C200h
4204h	DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMI SSION_0	Firewall Region 0 Channel 16 Permission 0 Register	4504 C204h
4220h	DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTR OL	Firewall Region 0 Channel 17 Control Register	4504 C220h
4224h	DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMI SSION_0	Firewall Region 0 Channel 17 Permission 0 Register	4504 C224h
4240h	DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTR OL	Firewall Region 0 Channel 18 Control Register	4504 C240h
4244h	DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMI SSION_0	Firewall Region 0 Channel 18 Permission 0 Register	4504 C244h

Table 23-505. DRU_MMR_FW Registers (continued)

Offset	Acronym	Register Name	COMPUTE_CLUSTER0 _DRU_MMR_FW Physical Address
4260h	DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL	Firewall Region 0 Channel 19 Control Register	4504 C260h
4264h	DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0	Firewall Region 0 Channel 19 Permission 0 Register	4504 C264h
4280h	DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL	Firewall Region 0 Channel 20 Control Register	4504 C280h
4284h	DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0	Firewall Region 0 Channel 20 Permission 0 Register	4504 C284h
42A0h	DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL	Firewall Region 0 Channel 21 Control Register	4504 C2A0h
42A4h	DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0	Firewall Region 0 Channel 21 Permission 0 Register	4504 C2A4h
42C0h	DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL	Firewall Region 0 Channel 22 Control Register	4504 C2C0h
42C4h	DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0	Firewall Region 0 Channel 22 Permission 0 Register	4504 C2C4h
42E0h	DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL	Firewall Region 0 Channel 23 Control Register	4504 C2E0h
42E4h	DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0	Firewall Region 0 Channel 23 Permission 0 Register	4504 C2E4h
4300h	DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL	Firewall Region 0 Channel 24 Control Register	4504 C300h
4304h	DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0	Firewall Region 0 Channel 24 Permission 0 Register	4504 C304h
4320h	DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL	Firewall Region 0 Channel 25 Control Register	4504 C320h
4324h	DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0	Firewall Region 0 Channel 25 Permission 0 Register	4504 C324h
4340h	DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL	Firewall Region 0 Channel 26 Control Register	4504 C340h
4344h	DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0	Firewall Region 0 Channel 26 Permission 0 Register	4504 C344h
4360h	DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL	Firewall Region 0 Channel 27 Control Register	4504 C360h
4364h	DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0	Firewall Region 0 Channel 27 Permission 0 Register	4504 C364h
4380h	DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL	Firewall Region 0 Channel 28 Control Register	4504 C380h
4384h	DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0	Firewall Region 0 Channel 28 Permission 0 Register	4504 C384h
43A0h	DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL	Firewall Region 0 Channel 29 Control Register	4504 C3A0h
43A4h	DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0	Firewall Region 0 Channel 29 Permission 0 Register	4504 C3A4h
43C0h	DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL	Firewall Region 0 Channel 30 Control Register	4504 C3C0h
43C4h	DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0	Firewall Region 0 Channel 30 Permission 0 Register	4504 C3C4h
43E0h	DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL	Firewall Region 0 Channel 31 Control Register	4504 C3E0h
43E4h	DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0	Firewall Region 0 Channel 31 Permission 0 Register	4504 C3E4h

23.3.1 DRU_MMR_CFG_FW_REGION_0_CONTROL Register (Offset = 0h) [reset = X]

DRU_MMR_CFG_FW_REGION_0_CONTROL is shown in Figure 23-180 and described in Table 23-507.

Return to [Summary Table](#).

The FW Region 0 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 firewall.

Table 23-506.
DRU_MMR_CFG_FW_REGION_0_CONTROL
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 8000h

Figure 23-180. DRU_MMR_CFG_FW_REGION_0_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-507. DRU_MMR_CFG_FW_REGION_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 background region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-508. Register Call Summary for DRU_MMR_CFG_FW_REGION_0_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_0_CONTROL Register \(Offset = 0h\) \[reset = X\]: \[0\]](#)

23.3.2 DRU_MMR_CFG_FW_REGION_0_PERMISSION_0 Register (Offset = 4h) [reset = X]

DRU_MMR_CFG_FW_REGION_0_PERMISSION_0 is shown in [Figure 23-181](#) and described in [Table 23-510](#).

Return to [Summary Table](#).

The FW Region 0 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 firewall.

Table 23-509.
DRU_MMR_CFG_FW_REGION_0_PERMISSION_0
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 8004h

Figure 23-181. DRU_MMR_CFG_FW_REGION_0_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-510. DRU_MMR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-510. DRU_MMR_CFG_FW_REGION_0_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-511. Register Call Summary for DRU_MMR_CFG_FW_REGION_0_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_0_PERMISSION_0 Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)

23.3.3 DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L Register (Offset = 10h) [reset = 0h]

DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L is shown in Figure 23-182 and described in Table 23-513.

Return to [Summary Table](#).

The FW Region 0 Start Address Low Register defines the start address bits 31 to 0 for the slave mmr.dru_mmr_cfg region 0 firewall.

Table 23-512. DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 8010h

Figure 23-182. DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-0h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-513. DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	0h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-514. Register Call Summary for DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_L Register \(Offset = 10h\) \[reset = 0h\]: \[0\]](#)

23.3.4 DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H Register (Offset = 14h) [reset = X]

DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H is shown in [Figure 23-183](#) and described in [Table 23-516](#).

Return to [Summary Table](#).

The FW Region 0 Start Address High Register defines the start address bits 47 to 32 for the slave mmr.dru_mmr_cfg region 0 firewall.

Table 23-515. DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 8014h

Figure 23-183. DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-516. DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-517. Register Call Summary for DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_0_START_ADDRESS_H Register \(Offset = 14h\) \[reset = X\]: \[0\]](#)

23.3.5 DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 3FFFh]

DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L is shown in Figure 23-184 and described in Table 23-519.

Return to [Summary Table](#).

The FW Region 0 End Address Low Register defines the end address bits 31 to 0 to include for the slave mmr.dru_mmr_cfg region 0 firewall.

Table 23-518.
DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 8018h

Figure 23-184. DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-3h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-3h				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-519. DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	3h	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-520. Register Call Summary for DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L

DRU_MMR_FW Registers	
•	DRU_MMR_FW Registers : [0]
•	DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_L Register (Offset = 18h) [reset = 3FFFh]: [0]

23.3.6 DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H Register (Offset = 1Ch) [reset = X]

DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H is shown in [Figure 23-185](#) and described in [Table 23-522](#).

Return to [Summary Table](#).

The FW Region 0 End Address High Register defines the end address bits 47 to 32 to include for the slave mmr.dru_mmr_cfg region 0 firewall.

Table 23-521.
DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 801Ch

Figure 23-185. DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-522. DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-523. Register Call Summary for DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_0_END_ADDRESS_H Register \(Offset = 1Ch\) \[reset = X\]: \[0\]](#)

23.3.7 DRU_MMR_CFG_FW_REGION_1_CONTROL Register (Offset = 20h) [reset = X]

DRU_MMR_CFG_FW_REGION_1_CONTROL is shown in Figure 23-186 and described in Table 23-525.

Return to [Summary Table](#).

The FW Region 1 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 1 firewall.

Table 23-524.
DRU_MMR_CFG_FW_REGION_1_CONTROL
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 8020h

Figure 23-186. DRU_MMR_CFG_FW_REGION_1_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-525. DRU_MMR_CFG_FW_REGION_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be 1 background region per FW and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-526. Register Call Summary for DRU_MMR_CFG_FW_REGION_1_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_1_CONTROL Register \(Offset = 20h\) \[reset = X\]: \[0\]](#)

23.3.8 DRU_MMR_CFG_FW_REGION_1_PERMISSION_0 Register (Offset = 24h) [reset = X]

DRU_MMR_CFG_FW_REGION_1_PERMISSION_0 is shown in [Figure 23-187](#) and described in [Table 23-528](#).

Return to [Summary Table](#).

The FW Region 1 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 1 firewall.

Table 23-527.
DRU_MMR_CFG_FW_REGION_1_PERMISSION_0
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 8024h

Figure 23-187. DRU_MMR_CFG_FW_REGION_1_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-528. DRU_MMR_CFG_FW_REGION_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-528. DRU_MMR_CFG_FW_REGION_1_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-529. Register Call Summary for DRU_MMR_CFG_FW_REGION_1_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_1_PERMISSION_0 Register \(Offset = 24h\) \[reset = X\]: \[0\]](#)

23.3.9 DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L Register (Offset = 30h) [reset = 8000h]

DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L is shown in Figure 23-188 and described in Table 23-531.

Return to [Summary Table](#).

The FW Region 1 Start Address Low Register defines the start address bits 31 to 0 for the slave mmr.dru_mmr_cfg region 1 firewall.

Table 23-530. DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 8030h

Figure 23-188. DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-8h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-8h				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-531. DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	8h	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

Table 23-532. Register Call Summary for DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_L Register \(Offset = 30h\) \[reset = 8000h\]: \[0\]](#)

23.3.10 DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H Register (Offset = 34h) [reset = X]

DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H is shown in [Figure 23-189](#) and described in [Table 23-534](#).

Return to [Summary Table](#).

The FW Region 1 Start Address High Register defines the start address bits 47 to 32 for the slave mmr.dru_mmr_cfg region 1 firewall.

Table 23-533. DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 8034h

Figure 23-189. DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-534. DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

Table 23-535. Register Call Summary for DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_1_START_ADDRESS_H Register \(Offset = 34h\) \[reset = X\]: \[0\]](#)

23.3.11 DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L Register (Offset = 38h) [reset = BFFFh]

DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L is shown in [Figure 23-190](#) and described in [Table 23-537](#).

Return to [Summary Table](#).

The FW Region 1 End Address Low Register defines the end address bits 31 to 0 to include for the slave mmr.dru_mmr_cfg region 1 firewall.

Table 23-536.
DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 8038h

Figure 23-190. DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-Bh															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-Bh								R-FFFh							

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 23-537. DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	Bh	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

Table 23-538. Register Call Summary for DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_L Register \(Offset = 38h\) \[reset = BFFFh\]: \[0\]](#)

23.3.12 DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H Register (Offset = 3Ch) [reset = X]

DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H is shown in [Figure 23-191](#) and described in [Table 23-540](#).

Return to [Summary Table](#).

The FW Region 1 End Address High Register defines the end address bits 47 to 32 to include for the slave mmr.dru_mmr_cfg region 1 firewall.

Table 23-539.
DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H
Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W	4504 803Ch

Figure 23-191. DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-540. DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

Table 23-541. Register Call Summary for DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FW_REGION_1_END_ADDRESS_H Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)

23.3.13 DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL Register (Offset = 4000h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL is shown in Figure 23-192 and described in Table 23-543.

Return to [Summary Table](#).

The FW Region 0 Channel 0 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 0 firewall.

Table 23-542. DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C000h

Figure 23-192. DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-543. DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-544. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_0_CONTROL Register \(Offset = 4000h\) \[reset = X\]: \[0\]](#)

23.3.14 DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 Register (Offset = 4004h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 is shown in Figure 23-193 and described in Table 23-546.

Return to [Summary Table](#).

The FW Region 0 Channel 0 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 0 firewall.

Table 23-545. DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C004h

Figure 23-193. DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-546. DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-546. DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-547. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_0_PERMISSION_0 Register \(Offset = 4004h\) \[reset = X\]: \[0\]](#)

23.3.15 DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL Register (Offset = 4020h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL is shown in Figure 23-194 and described in Table 23-549.

Return to [Summary Table](#).

The FW Region 0 Channel 1 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 1 firewall.

Table 23-548. DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C020h

Figure 23-194. DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-549. DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-550. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_1_CONTROL Register \(Offset = 4020h\) \[reset = X\]: \[0\]](#)

23.3.16 DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 Register (Offset = 4024h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 is shown in Figure 23-195 and described in Table 23-552.

Return to [Summary Table](#).

The FW Region 0 Channel 1 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 1 firewall.

Table 23-551. DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C024h

Figure 23-195. DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-552. DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-552. DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-553. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_1_PERMISSION_0 Register \(Offset = 4024h\) \[reset = X\]: \[0\]](#)

23.3.17 DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL Register (Offset = 4040h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL is shown in Figure 23-196 and described in Table 23-555.

Return to [Summary Table](#).

The FW Region 0 Channel 2 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 2 firewall.

Table 23-554. DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C040h

Figure 23-196. DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-555. DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-556. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_2_CONTROL Register \(Offset = 4040h\) \[reset = X\]: \[0\]](#)

23.3.18 DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 Register (Offset = 4044h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 is shown in Figure 23-197 and described in Table 23-558.

Return to [Summary Table](#).

The FW Region 0 Channel 2 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 2 firewall.

Table 23-557. DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C044h

Figure 23-197. DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-558. DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-558. DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-559. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_2_PERMISSION_0 Register \(Offset = 4044h\) \[reset = X\]: \[0\]](#)

23.3.19 DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL Register (Offset = 4060h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL is shown in Figure 23-198 and described in Table 23-561.

Return to [Summary Table](#).

The FW Region 0 Channel 3 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 3 firewall.

Table 23-560. DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C060h

Figure 23-198. DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-561. DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-562. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_3_CONTROL Register \(Offset = 4060h\) \[reset = X\]: \[0\]](#)

23.3.20 DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 Register (Offset = 4064h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 is shown in Figure 23-199 and described in Table 23-564.

Return to [Summary Table](#).

The FW Region 0 Channel 3 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 3 firewall.

Table 23-563. DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C064h

Figure 23-199. DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-564. DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-564. DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-565. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_3_PERMISSION_0 Register \(Offset = 4064h\) \[reset = X\]: \[0\]](#)

23.3.21 DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL Register (Offset = 4080h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL is shown in Figure 23-200 and described in Table 23-567.

Return to [Summary Table](#).

The FW Region 0 Channel 4 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 4 firewall.

Table 23-566. DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C080h

Figure 23-200. DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-567. DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-568. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_4_CONTROL Register \(Offset = 4080h\) \[reset = X\]: \[0\]](#)

23.3.22 DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 Register (Offset = 4084h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 is shown in Figure 23-201 and described in Table 23-570.

Return to [Summary Table](#).

The FW Region 0 Channel 4 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 4 firewall.

Table 23-569. DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C084h

Figure 23-201. DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-570. DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-570. DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-571. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_4_PERMISSION_0 Register \(Offset = 4084h\) \[reset = X\]: \[0\]](#)

23.3.23 DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL Register (Offset = 40A0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL is shown in Figure 23-202 and described in Table 23-573.

Return to [Summary Table](#).

The FW Region 0 Channel 5 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 5 firewall.

Table 23-572. DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C0A0h

Figure 23-202. DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-573. DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-574. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_5_CONTROL Register \(Offset = 40A0h\) \[reset = X\]: \[0\]](#)

23.3.24 DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 Register (Offset = 40A4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 is shown in Figure 23-203 and described in Table 23-576.

Return to [Summary Table](#).

The FW Region 0 Channel 5 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 5 firewall.

Table 23-575. DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C0A4h

Figure 23-203. DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-576. DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-576. DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-577. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_5_PERMISSION_0 Register \(Offset = 40A4h\) \[reset = X\]: \[0\]](#)

23.3.25 DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL Register (Offset = 40C0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL is shown in Figure 23-204 and described in Table 23-579.

Return to [Summary Table](#).

The FW Region 0 Channel 6 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 6 firewall.

Table 23-578. DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C0C0h

Figure 23-204. DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-579. DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-580. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_6_CONTROL Register \(Offset = 40C0h\) \[reset = X\]: \[0\]](#)

23.3.26 DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 Register (Offset = 40C4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 is shown in Figure 23-205 and described in Table 23-582.

Return to [Summary Table](#).

The FW Region 0 Channel 6 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 6 firewall.

Table 23-581. DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C0C4h

Figure 23-205. DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-582. DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-582. DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-583. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_6_PERMISSION_0 Register \(Offset = 40C4h\) \[reset = X\]: \[0\]](#)

23.3.27 DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL Register (Offset = 40E0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL is shown in Figure 23-206 and described in Table 23-585.

Return to [Summary Table](#).

The FW Region 0 Channel 7 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 7 firewall.

Table 23-584. DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C0E0h

Figure 23-206. DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-585. DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-586. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_7_CONTROL Register \(Offset = 40E0h\) \[reset = X\]: \[0\]](#)

23.3.28 DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 Register (Offset = 40E4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 is shown in [Figure 23-207](#) and described in [Table 23-588](#).

Return to [Summary Table](#).

The FW Region 0 Channel 7 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 7 firewall.

Table 23-587. DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C0E4h

Figure 23-207. DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-588. DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-588. DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-589. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_7_PERMISSION_0 Register \(Offset = 40E4h\) \[reset = X\]: \[0\]](#)

23.3.29 DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL Register (Offset = 4100h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL is shown in Figure 23-208 and described in Table 23-591.

Return to [Summary Table](#).

The FW Region 0 Channel 8 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 8 firewall.

Table 23-590. DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C100h

Figure 23-208. DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-591. DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-592. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_8_CONTROL Register \(Offset = 4100h\) \[reset = X\]: \[0\]](#)

23.3.30 DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 Register (Offset = 4104h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 is shown in Figure 23-209 and described in Table 23-594.

Return to [Summary Table](#).

The FW Region 0 Channel 8 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 8 firewall.

Table 23-593. DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C104h

Figure 23-209. DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-594. DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-594. DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-595. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_8_PERMISSION_0 Register \(Offset = 4104h\) \[reset = X\]: \[0\]](#)

23.3.31 DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL Register (Offset = 4120h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL is shown in Figure 23-210 and described in Table 23-597.

Return to [Summary Table](#).

The FW Region 0 Channel 9 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 9 firewall.

Table 23-596. DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C120h

Figure 23-210. DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-597. DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-598. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_9_CONTROL Register \(Offset = 4120h\) \[reset = X\]: \[0\]](#)

23.3.32 DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 Register (Offset = 4124h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 is shown in Figure 23-211 and described in Table 23-600.

Return to [Summary Table](#).

The FW Region 0 Channel 9 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 9 firewall.

Table 23-599. DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C124h

Figure 23-211. DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-600. DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-600. DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-601. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_9_PERMISSION_0 Register \(Offset = 4124h\) \[reset = X\]: \[0\]](#)

23.3.33 DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL Register (Offset = 4140h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL is shown in Figure 23-212 and described in Table 23-603.

Return to [Summary Table](#).

The FW Region 0 Channel 10 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 10 firewall.

Table 23-602. DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C140h

Figure 23-212. DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-603. DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-604. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_10_CONTROL Register \(Offset = 4140h\) \[reset = X\]: \[0\]](#)

23.3.34 DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 Register (Offset = 4144h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 is shown in Figure 23-213 and described in Table 23-606.

Return to [Summary Table](#).

The FW Region 0 Channel 10 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 10 firewall.

Table 23-605. DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C144h

Figure 23-213. DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-606. DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-606. DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-607. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_10_PERMISSION_0 Register \(Offset = 4144h\) \[reset = X\]: \[0\]](#)

23.3.35 DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL Register (Offset = 4160h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL is shown in [Figure 23-214](#) and described in [Table 23-609](#).

Return to [Summary Table](#).

The FW Region 0 Channel 11 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 11 firewall.

Table 23-608. DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C160h

Figure 23-214. DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-609. DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-610. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_11_CONTROL Register \(Offset = 4160h\) \[reset = X\]: \[0\]](#)

23.3.36 DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 Register (Offset = 4164h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 is shown in Figure 23-215 and described in Table 23-612.

Return to [Summary Table](#).

The FW Region 0 Channel 11 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 11 firewall.

Table 23-611. DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C164h

Figure 23-215. DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-612. DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-612. DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-613. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_11_PERMISSION_0 Register \(Offset = 4164h\) \[reset = X\]: \[0\]](#)

23.3.37 DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL Register (Offset = 4180h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL is shown in Figure 23-216 and described in Table 23-615.

Return to [Summary Table](#).

The FW Region 0 Channel 12 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 12 firewall.

Table 23-614. DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C180h

Figure 23-216. DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-615. DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-616. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_12_CONTROL Register \(Offset = 4180h\) \[reset = X\]: \[0\]](#)

23.3.38 DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 Register (Offset = 4184h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 is shown in Figure 23-217 and described in Table 23-618.

Return to [Summary Table](#).

The FW Region 0 Channel 12 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 12 firewall.

Table 23-617. DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C184h

Figure 23-217. DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-618. DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-618. DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-619. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_12_PERMISSION_0 Register \(Offset = 4184h\) \[reset = X\]: \[0\]](#)

23.3.39 DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL Register (Offset = 41A0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL is shown in Figure 23-218 and described in Table 23-621.

Return to [Summary Table](#).

The FW Region 0 Channel 13 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 13 firewall.

Table 23-620. DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C1A0h

Figure 23-218. DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-621. DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-622. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_13_CONTROL Register \(Offset = 41A0h\) \[reset = X\]: \[0\]](#)

23.3.40 DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 Register (Offset = 41A4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 is shown in Figure 23-219 and described in Table 23-624.

Return to [Summary Table](#).

The FW Region 0 Channel 13 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 13 firewall.

Table 23-623. DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C1A4h

Figure 23-219. DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-624. DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-624. DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-625. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_13_PERMISSION_0 Register \(Offset = 41A4h\) \[reset = X\]: \[0\]](#)

23.3.41 DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL Register (Offset = 41C0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL is shown in [Figure 23-220](#) and described in [Table 23-627](#).

Return to [Summary Table](#).

The FW Region 0 Channel 14 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 14 firewall.

Table 23-626. DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C1C0h

Figure 23-220. DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-627. DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-628. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_14_CONTROL Register \(Offset = 41C0h\) \[reset = X\]: \[0\]](#)

23.3.42 DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 Register (Offset = 41C4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 is shown in Figure 23-221 and described in Table 23-630.

Return to [Summary Table](#).

The FW Region 0 Channel 14 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 14 firewall.

Table 23-629. DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C1C4h

Figure 23-221. DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-630. DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-630. DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-631. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_14_PERMISSION_0 Register \(Offset = 41C4h\) \[reset = X\]: \[0\]](#)

23.3.43 DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL Register (Offset = 41E0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL is shown in Figure 23-222 and described in Table 23-633.

Return to [Summary Table](#).

The FW Region 0 Channel 15 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 15 firewall.

Table 23-632. DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C1E0h

Figure 23-222. DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-633. DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-634. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_15_CONTROL Register (Offset = 41E0h) [reset = X]: [0]

23.3.44 DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 Register (Offset = 41E4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 is shown in Figure 23-223 and described in Table 23-636.

Return to [Summary Table](#).

The FW Region 0 Channel 15 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 15 firewall.

Table 23-635. DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C1E4h

Figure 23-223. DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-636. DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-636. DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-637. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_15_PERMISSION_0 Register \(Offset = 41E4h\) \[reset = X\]: \[0\]](#)

23.3.45 DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL Register (Offset = 4200h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL is shown in [Figure 23-224](#) and described in [Table 23-639](#).

Return to [Summary Table](#).

The FW Region 0 Channel 16 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 16 firewall.

Table 23-638. DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C200h

Figure 23-224. DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-639. DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-640. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_16_CONTROL Register \(Offset = 4200h\) \[reset = X\]: \[0\]](#)

23.3.46 DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 Register (Offset = 4204h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 is shown in Figure 23-225 and described in Table 23-642.

Return to [Summary Table](#).

The FW Region 0 Channel 16 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 16 firewall.

Table 23-641. DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C204h

Figure 23-225. DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-642. DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-642. DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-643. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_16_PERMISSION_0 Register \(Offset = 4204h\) \[reset = X\]: \[0\]](#)

23.3.47 DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL Register (Offset = 4220h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL is shown in Figure 23-226 and described in Table 23-645.

Return to [Summary Table](#).

The FW Region 0 Channel 17 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 17 firewall.

Table 23-644. DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C220h

Figure 23-226. DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-645. DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-646. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_17_CONTROL Register (Offset = 4220h) [reset = X]: [0]

23.3.48 DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 Register (Offset = 4224h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 is shown in Figure 23-227 and described in Table 23-648.

Return to [Summary Table](#).

The FW Region 0 Channel 17 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 17 firewall.

Table 23-647. DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C224h

Figure 23-227. DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-648. DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-648. DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-649. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_17_PERMISSION_0 Register \(Offset = 4224h\) \[reset = X\]: \[0\]](#)

23.3.49 DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL Register (Offset = 4240h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL is shown in [Figure 23-228](#) and described in [Table 23-651](#).

Return to [Summary Table](#).

The FW Region 0 Channel 18 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 18 firewall.

Table 23-650. DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C240h

Figure 23-228. DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-651. DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-652. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_18_CONTROL Register \(Offset = 4240h\) \[reset = X\]: \[0\]](#)

23.3.50 DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 Register (Offset = 4244h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 is shown in Figure 23-229 and described in Table 23-654.

Return to [Summary Table](#).

The FW Region 0 Channel 18 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 18 firewall.

Table 23-653. DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C244h

Figure 23-229. DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-654. DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-654. DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-655. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_18_PERMISSION_0 Register \(Offset = 4244h\) \[reset = X\]: \[0\]](#)

23.3.51 DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL Register (Offset = 4260h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL is shown in Figure 23-230 and described in Table 23-657.

Return to [Summary Table](#).

The FW Region 0 Channel 19 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 19 firewall.

Table 23-656. DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C260h

Figure 23-230. DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-657. DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-658. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_19_CONTROL Register (Offset = 4260h) [reset = X]: [0]

23.3.52 DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 Register (Offset = 4264h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 is shown in Figure 23-231 and described in Table 23-660.

Return to [Summary Table](#).

The FW Region 0 Channel 19 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 19 firewall.

Table 23-659. DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C264h

Figure 23-231. DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-660. DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-660. DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-661. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_19_PERMISSION_0 Register \(Offset = 4264h\) \[reset = X\]: \[0\]](#)

23.3.53 DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL Register (Offset = 4280h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL is shown in Figure 23-232 and described in Table 23-663.

Return to [Summary Table](#).

The FW Region 0 Channel 20 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 20 firewall.

Table 23-662. DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C280h

Figure 23-232. DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-663. DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-664. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_20_CONTROL Register \(Offset = 4280h\) \[reset = X\]: \[0\]](#)

23.3.54 DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 Register (Offset = 4284h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 is shown in Figure 23-233 and described in Table 23-666.

Return to [Summary Table](#).

The FW Region 0 Channel 20 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 20 firewall.

Table 23-665. DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C284h

Figure 23-233. DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-666. DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-666. DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-667. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_20_PERMISSION_0 Register \(Offset = 4284h\) \[reset = X\]: \[0\]](#)

23.3.55 DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL Register (Offset = 42A0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL is shown in Figure 23-234 and described in Table 23-669.

Return to [Summary Table](#).

The FW Region 0 Channel 21 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 21 firewall.

Table 23-668. DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C2A0h

Figure 23-234. DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-669. DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-670. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> • DRU_MMR_FW Registers: [0] • DRU_MMR_CFG_FWCH_REGION_0_CH_21_CONTROL Register (Offset = 42A0h) [reset = X]: [0]

23.3.56 DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 Register (Offset = 42A4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 is shown in Figure 23-235 and described in Table 23-672.

Return to [Summary Table](#).

The FW Region 0 Channel 21 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 21 firewall.

Table 23-671. DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C2A4h

Figure 23-235. DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-672. DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-672. DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-673. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_21_PERMISSION_0 Register \(Offset = 42A4h\) \[reset = X\]: \[0\]](#)

23.3.57 DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL Register (Offset = 42C0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL is shown in Figure 23-236 and described in Table 23-675.

Return to [Summary Table](#).

The FW Region 0 Channel 22 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 22 firewall.

Table 23-674. DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C2C0h

Figure 23-236. DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-675. DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-676. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_22_CONTROL Register \(Offset = 42C0h\) \[reset = X\]: \[0\]](#)

23.3.58 DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 Register (Offset = 42C4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 is shown in Figure 23-237 and described in Table 23-678.

Return to [Summary Table](#).

The FW Region 0 Channel 22 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 22 firewall.

Table 23-677. DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C2C4h

Figure 23-237. DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-678. DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-678. DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-679. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_22_PERMISSION_0 Register \(Offset = 42C4h\) \[reset = X\]: \[0\]](#)

23.3.59 DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL Register (Offset = 42E0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL is shown in Figure 23-238 and described in Table 23-681.

Return to [Summary Table](#).

The FW Region 0 Channel 23 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 23 firewall.

Table 23-680. DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C2E0h

Figure 23-238. DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-681. DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-682. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_23_CONTROL Register (Offset = 42E0h) [reset = X]: [0]

23.3.60 DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 Register (Offset = 42E4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 is shown in Figure 23-239 and described in Table 23-684.

Return to [Summary Table](#).

The FW Region 0 Channel 23 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 23 firewall.

Table 23-683. DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C2E4h

Figure 23-239. DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-684. DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-684. DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 Register Field Descriptions
(continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-685. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_23_PERMISSION_0 Register \(Offset = 42E4h\) \[reset = X\]: \[0\]](#)

23.3.61 DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL Register (Offset = 4300h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL is shown in [Figure 23-240](#) and described in [Table 23-687](#).

Return to [Summary Table](#).

The FW Region 0 Channel 24 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 24 firewall.

Table 23-686. DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C300h

Figure 23-240. DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-687. DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-688. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_24_CONTROL Register \(Offset = 4300h\) \[reset = X\]: \[0\]](#)

23.3.62 DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 Register (Offset = 4304h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 is shown in Figure 23-241 and described in Table 23-690.

Return to [Summary Table](#).

The FW Region 0 Channel 24 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 24 firewall.

Table 23-689. DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C304h

Figure 23-241. DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-690. DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-690. DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-691. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_24_PERMISSION_0 Register \(Offset = 4304h\) \[reset = X\]: \[0\]](#)

23.3.63 DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL Register (Offset = 4320h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL is shown in Figure 23-242 and described in Table 23-693.

Return to [Summary Table](#).

The FW Region 0 Channel 25 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 25 firewall.

Table 23-692. DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C320h

Figure 23-242. DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-693. DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-694. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_25_CONTROL Register (Offset = 4320h) [reset = X]: [0]

23.3.64 DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 Register (Offset = 4324h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 is shown in Figure 23-243 and described in Table 23-696.

Return to [Summary Table](#).

The FW Region 0 Channel 25 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 25 firewall.

Table 23-695. DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C324h

Figure 23-243. DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-696. DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-696. DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-697. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_25_PERMISSION_0 Register \(Offset = 4324h\) \[reset = X\]: \[0\]](#)

23.3.65 DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL Register (Offset = 4340h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL is shown in [Figure 23-244](#) and described in [Table 23-699](#).

Return to [Summary Table](#).

The FW Region 0 Channel 26 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 26 firewall.

Table 23-698. DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C340h

Figure 23-244. DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-699. DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-700. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_26_CONTROL Register \(Offset = 4340h\) \[reset = X\]: \[0\]](#)

23.3.66 DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 Register (Offset = 4344h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 is shown in Figure 23-245 and described in Table 23-702.

Return to [Summary Table](#).

The FW Region 0 Channel 26 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 26 firewall.

Table 23-701. DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C344h

Figure 23-245. DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-702. DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-702. DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-703. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_26_PERMISSION_0 Register \(Offset = 4344h\) \[reset = X\]: \[0\]](#)

23.3.67 DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL Register (Offset = 4360h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL is shown in Figure 23-246 and described in Table 23-705.

Return to [Summary Table](#).

The FW Region 0 Channel 27 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 27 firewall.

Table 23-704. DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C360h

Figure 23-246. DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-705. DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-706. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_27_CONTROL Register (Offset = 4360h) [reset = X]: [0]

23.3.68 DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 Register (Offset = 4364h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 is shown in Figure 23-247 and described in Table 23-708.

Return to [Summary Table](#).

The FW Region 0 Channel 27 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 27 firewall.

Table 23-707. DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C364h

Figure 23-247. DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-708. DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-708. DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-709. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_27_PERMISSION_0 Register \(Offset = 4364h\) \[reset = X\]: \[0\]](#)

23.3.69 DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL Register (Offset = 4380h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL is shown in [Figure 23-248](#) and described in [Table 23-711](#).

Return to [Summary Table](#).

The FW Region 0 Channel 28 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 28 firewall.

Table 23-710. DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C380h

Figure 23-248. DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-711. DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-712. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_28_CONTROL Register \(Offset = 4380h\) \[reset = X\]: \[0\]](#)

23.3.70 DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 Register (Offset = 4384h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 is shown in Figure 23-249 and described in Table 23-714.

Return to [Summary Table](#).

The FW Region 0 Channel 28 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 28 firewall.

Table 23-713. DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C384h

Figure 23-249. DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-714. DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-714. DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-715. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_28_PERMISSION_0 Register \(Offset = 4384h\) \[reset = X\]: \[0\]](#)

23.3.71 DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL Register (Offset = 43A0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL is shown in Figure 23-250 and described in Table 23-717.

Return to [Summary Table](#).

The FW Region 0 Channel 29 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 29 firewall.

Table 23-716. DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C3A0h

Figure 23-250. DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-717. DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-718. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_29_CONTROL Register \(Offset = 43A0h\) \[reset = X\]: \[0\]](#)

23.3.72 DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 Register (Offset = 43A4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 is shown in Figure 23-251 and described in Table 23-720.

Return to [Summary Table](#).

The FW Region 0 Channel 29 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 29 firewall.

Table 23-719. DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C3A4h

Figure 23-251. DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-720. DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

Table 23-720. DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-721. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_29_PERMISSION_0 Register \(Offset = 43A4h\) \[reset = X\]: \[0\]](#)

23.3.73 DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL Register (Offset = 43C0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL is shown in [Figure 23-252](#) and described in [Table 23-723](#).

Return to [Summary Table](#).

The FW Region 0 Channel 30 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 30 firewall.

Table 23-722. DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C3C0h

Figure 23-252. DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-723. DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-724. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_30_CONTROL Register \(Offset = 43C0h\) \[reset = X\]: \[0\]](#)

23.3.74 DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 Register (Offset = 43C4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 is shown in Figure 23-253 and described in Table 23-726.

Return to [Summary Table](#).

The FW Region 0 Channel 30 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 30 firewall.

Table 23-725. DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C3C4h

Figure 23-253. DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-726. DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-726. DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-727. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_30_PERMISSION_0 Register \(Offset = 43C4h\) \[reset = X\]: \[0\]](#)

23.3.75 DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL Register (Offset = 43E0h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL is shown in Figure 23-254 and described in Table 23-729.

Return to [Summary Table](#).

The FW Region 0 Channel 31 Control Register defines the control fields for the slave mmr.dru_mmr_cfg region 0 channel 31 firewall.

Table 23-728. DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C3E0h

Figure 23-254. DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	RESERVED
R/W-X						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-729. DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

Table 23-730. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL

DRU_MMR_FW Registers
<ul style="list-style-type: none"> DRU_MMR_FW Registers: [0] DRU_MMR_CFG_FWCH_REGION_0_CH_31_CONTROL Register (Offset = 43E0h) [reset = X]: [0]

23.3.76 DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 Register (Offset = 43E4h) [reset = X]

DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 is shown in Figure 23-255 and described in Table 23-732.

Return to [Summary Table](#).

The FW Region 0 Channel 31 Permission 0 Register defines the permissions for the slave mmr.dru_mmr_cfg region 0 channel 31 firewall.

Table 23-731. DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW	4504 C3E4h

Figure 23-255. DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USE R_DEBUG	NONSEC_USE R_CACHEABL E	NONSEC_USE R_READ	NONSEC_USE R_WRITE	NONSEC_SUP V_DEBUG	NONSEC_SUP V_CACHEABL E	NONSEC_SUP V_READ	NONSEC_SUP V_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_D EBUG	SEC_USER_C ACHEABLE	SEC_USER_R EAD	SEC_USER_W RITE	SEC_SUPV_D EBUG	SEC_SUPV_C ACHEABLE	SEC_SUPV_R EAD	SEC_SUPV_W RITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-732. DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.
5	SEC_USER_READ	R/W	0h	Secure user read allowed.

**Table 23-732. DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 Register Field Descriptions
(continued)**

Bit	Field	Type	Reset	Description
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

Table 23-733. Register Call Summary for DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0

DRU_MMR_FW Registers

- [DRU_MMR_FW Registers: \[0\]](#)
- [DRU_MMR_CFG_FWCH_REGION_0_CH_31_PERMISSION_0 Register \(Offset = 43E4h\) \[reset = X\]: \[0\]](#)

23.4 DRU_MMR_FW_GLB Registers

Table 23-735 lists the memory-mapped registers for the DRU_MMR_FW_GLB registers. All register offset addresses not listed in Table 23-735 should be considered as reserved locations and the register contents should not be modified.

Table 23-734. DRU_MMR_FW_GLB Instances

Instance	Base Address
COMPUTE_CLUSTER0_DRU_MMR_F W_GLB	45B1 8000h

Table 23-735. DRU_MMR_FW_GLB Registers

Offset	Acronym	Register Name	COMPUTE_CLUSTER0_D RU_MMR_FW_GLB Physical Address
0h	PID	Revision Register	45B1 8000h
4h	DESTINATION_ID	Destination ID Register	45B1 8004h
20h	EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B1 8020h
24h	EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B1 8024h
28h	EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B1 8028h
2Ch	EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B1 802Ch
30h	EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B1 8030h
34h	EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B1 8034h
38h	EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B1 8038h
40h	EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B1 8040h
44h	EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B1 8044h

23.4.1 PID Register (Offset = 0h) [reset = 66001101h]

PID is shown in [Figure 23-256](#) and described in [Table 23-737](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 23-736. PID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8000h

Figure 23-256. PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME			BU		FUNC										
R-1h			R-2h		R-600h										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-2h					R-1h			R-0h		R-1h					

LEGEND: R = Read Only; -n = value after reset

Table 23-737. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	2h	Business Unit: 10 = Processors
27-16	FUNC	R	600h	Module ID
15-11	RTL	R	2h	RTL revision. Will vary depending on release.
10-8	MAJOR	R	1h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	1h	Minor revision

Table 23-738. Register Call Summary for PID

DRU_MMR_FW_GLB Registers

- [PID Register \(Offset = 0h\) \[reset = 66001101h\]: \[0\] \[1\]](#)
- [DRU_MMR_FW_GLB Registers: \[0\]](#)

23.4.2 DESTINATION_ID Register (Offset = 4h) [reset = X]

DESTINATION_ID is shown in [Figure 23-257](#) and described in [Table 23-740](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

Table 23-739. DESTINATION_ID Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W_GLB	45B1 8004h

Figure 23-257. DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEST_ID							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-740. DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

Table 23-741. Register Call Summary for DESTINATION_ID

DRU_MMR_FW_GLB Registers

- [DESTINATION_ID Register \(Offset = 4h\) \[reset = X\]: \[0\]](#)
- [DRU_MMR_FW_GLB Registers: \[0\]](#)

23.4.3 EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = X]

EXCEPTION_LOGGING_CONTROL is shown in [Figure 23-258](#) and described in [Table 23-743](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

Table 23-742. EXCEPTION_LOGGING_CONTROL Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8020h

Figure 23-258. EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEN D	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 23-743. EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_PEND	R/W	0h	Disables logging pending when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

Table 23-744. Register Call Summary for EXCEPTION_LOGGING_CONTROL

DRU_MMR_FW_GLB Registers
<ul style="list-style-type: none"> DRU_MMR_FW_GLB Registers: [0] EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = X]: [0]

23.4.4 EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

EXCEPTION_LOGGING_HEADER0 is shown in [Figure 23-259](#) and described in [Table 23-746](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Table 23-745. EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8024h

Figure 23-259. EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID								DEST_ID															
R-0h								R-0h								R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-746. EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

Table 23-747. Register Call Summary for EXCEPTION_LOGGING_HEADER0

DRU_MMR_FW_GLB Registers

- EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]: [0]
- DRU_MMR_FW_GLB Registers: [0]

23.4.5 EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = X]

EXCEPTION_LOGGING_HEADER1 is shown in [Figure 23-260](#) and described in [Table 23-749](#).

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

Table 23-748. EXCEPTION_LOGGING_HEADER1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8028h

Figure 23-260. EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; -n = value after reset

Table 23-749. EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code.
15-0	RESERVED	R	X	

Table 23-750. Register Call Summary for EXCEPTION_LOGGING_HEADER1

DRU_MMR_FW_GLB Registers

- [DRU_MMR_FW_GLB Registers: \[0\]](#)
- [EXCEPTION_LOGGING_HEADER1 Register \(Offset = 28h\) \[reset = X\]: \[0\]](#)

23.4.6 EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

EXCEPTION_LOGGING_DATA0 is shown in [Figure 23-261](#) and described in [Table 23-752](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

**Table 23-751. EXCEPTION_LOGGING_DATA0
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W_GLB	45B1 802Ch

Figure 23-261. EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 23-752. EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

Table 23-753. Register Call Summary for EXCEPTION_LOGGING_DATA0

DRU_MMR_FW_GLB Registers

- [DRU_MMR_FW_GLB Registers: \[0\]](#)
- [EXCEPTION_LOGGING_DATA0 Register \(Offset = 2Ch\) \[reset = 0h\]: \[0\]](#)

23.4.7 EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = X]

EXCEPTION_LOGGING_DATA1 is shown in [Figure 23-262](#) and described in [Table 23-755](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

Table 23-754. EXCEPTION_LOGGING_DATA1 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8030h

Figure 23-262. EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-755. EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 16 bits.

Table 23-756. Register Call Summary for EXCEPTION_LOGGING_DATA1

DRU_MMR_FW_GLB Registers

- [DRU_MMR_FW_GLB Registers](#): [0]
- [EXCEPTION_LOGGING_DATA1 Register \(Offset = 30h\) \[reset = X\]](#): [0]

23.4.8 EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = X]

EXCEPTION_LOGGING_DATA2 is shown in Figure 23-263 and described in Table 23-758.

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

**Table 23-757. EXCEPTION_LOGGING_DATA2
Instances**

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_F W_GLB	45B1 8034h

Figure 23-263. EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 23-758. EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

Table 23-759. Register Call Summary for EXCEPTION_LOGGING_DATA2

DRU_MMR_FW_GLB Registers

- [DRU_MMR_FW_GLB Registers: \[0\]](#)
- [EXCEPTION_LOGGING_DATA2 Register \(Offset = 34h\) \[reset = X\]: \[0\]](#)

23.4.9 EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = X]

EXCEPTION_LOGGING_DATA3 is shown in [Figure 23-264](#) and described in [Table 23-761](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the fourth word of the data.

Table 23-760. EXCEPTION_LOGGING_DATA3 Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8038h

Figure 23-264. EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						BYTECNT															
R-X																						R-0h															

LEGEND: R = Read Only; -n = value after reset

Table 23-761. EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

Table 23-762. Register Call Summary for EXCEPTION_LOGGING_DATA3

DRU_MMR_FW_GLB Registers

- EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = X]: [0]
- DRU_MMR_FW_GLB Registers: [0]

23.4.10 EXCEPTION_PEND_SET Register (Offset = 40h) [reset = X]

EXCEPTION_PEND_SET is shown in [Figure 23-265](#) and described in [Table 23-764](#).

Return to [Summary Table](#).

The Exception Logging Pending Set Register allows to set the pend signal.

Table 23-763. EXCEPTION_PEND_SET Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8040h

Figure 23-265. EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 23-764. EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

Table 23-765. Register Call Summary for EXCEPTION_PEND_SET

DRU_MMR_FW_GLB Registers

- [EXCEPTION_PEND_SET Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)
- [DRU_MMR_FW_GLB Registers: \[0\]](#)

23.4.11 EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = X]

EXCEPTION_PEND_CLEAR is shown in [Figure 23-266](#) and described in [Table 23-767](#).

Return to [Summary Table](#).

The Exception Logging Pending Clear Register allows to clear the pend signal.

Table 23-766. EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
COMPUTE_CLUSTER0_DRU_MMR_FW_GLB	45B1 8044h

Figure 23-266. EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 23-767. EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

Table 23-768. Register Call Summary for EXCEPTION_PEND_CLEAR

DRU_MMR_FW_GLB Registers

- [EXCEPTION_PEND_CLEAR Register \(Offset = 44h\) \[reset = X\]: \[0\]](#)
- [DRU_MMR_FW_GLB Registers: \[0\]](#)

24 CPTS Registers

Table 24-2 lists the memory-mapped registers for the NAVSS0_CPTS. All register offset addresses not listed in Table 24-2 should be considered as reserved locations and the register contents should not be modified.

Table 24-1. NAVSS0_CPTS Instances

Instance	Base Address
NAVSS0_CPTS	310D 0000h

Table 24-2. NAVSS0_CPTS Registers

Offset	Acronym	Register Name	NAVSS0_CPTS Physical Address
0h	CPTS_IDVER_REG	Identification and Version	310D 0000h
4h	CPTS_CONTROL_REG	Time Sync Control	310D 0004h
8h	CPTS_RFTCLK_SEL_REG	RFTCLK Select	310D 0008h
Ch	CPTS_TS_PUSH_REG	Time Stamp Event Push	310D 000Ch
10h	CPTS_TS_LOAD_VAL_REG	Time Stamp Load Low Value	310D 0010h
14h	CPTS_TS_LOAD_EN_REG	Time Stamp Load Enable	310D 0014h
18h	CPTS_TS_COMP_VAL_REG	Time Stamp Comparison Low Value	310D 0018h
1Ch	CPTS_TS_COMP_LEN_REG	Time Stamp Comparison Length	310D 001Ch
20h	CPTS_INTSTAT_RAW_REG	Interrupt Status Register Raw	310D 0020h
24h	CPTS_INTSTAT_MASKED_REG	Interrupt Status Register Masked	310D 0024h
28h	CPTS_INT_ENABLE_REG	Interrupt Enable Register	310D 0028h
2Ch	CPTS_TS_COMP_NUDGE_REG	Time Stamp Comparison Nudge	310D 002Ch
30h	CPTS_EVENT_POP_REG	Event Pop	310D 0030h
34h	CPTS_EVENT_0_REG	Event Register 0	310D 0034h
38h	CPTS_EVENT_1_REG	Event Register 1	310D 0038h
3Ch	CPTS_EVENT_2_REG	Event Register 2	310D 003Ch
40h	CPTS_EVENT_3_REG	Event Register 3	310D 0040h
44h	CPTS_TS_LOAD_HIGH_VAL_REG	Time Stamp Load High Value	310D 0044h
48h	CPTS_TS_COMP_HIGH_VAL_REG	Time Stamp Comparison High Value	310D 0048h
4Ch	CPTS_TS_ADD_VAL_REG	Time Stamp Add Value	310D 004Ch
50h	CPTS_TS_PPM_LOW_VAL_REG	Time Stamp PPM Low Value	310D 0050h
54h	CPTS_TS_PPM_HIGH_VAL_REG	Time Stamp PPM High Value	310D 0054h
58h	CPTS_TS_NUDGE_VAL_REG	Time Stamp Nudge Value	310D 0058h
E0h + formula	CPTS_TS_GENF_COMP_LOW_REG_j	Time Stamp Generate Function j Comparison Low Value	310D 00E0h + formula
E4h + formula	CPTS_TS_GENF_COMP_HIGH_REG_j	Time Stamp Generate Function j Comparison high Value	310D 00E4h + formula
E8h + formula	CPTS_TS_GENF_CONTROL_REG_j	Time Stamp Generate Function j Control	310D 00E8h + formula
ECh + formula	CPTS_TS_GENF_LENGTH_REG_j	Time Stamp Generate Function j Length Value	310D 00ECh + formula
F0h + formula	CPTS_TS_GENF_PPM_LOW_REG_j	Time Stamp Generate Function j PPM Low Value	310D 00F0h + formula
F4h + formula	CPTS_TS_GENF_PPM_HIGH_REG_j	Time Stamp Generate Function j PPM High Value	310D 00F4h + formula
F8h + formula	CPTS_TS_GENF_NUDGE_REG_j	Time Stamp Generate Function j Nudge Value	310D 00F8h + formula
200h	CPTS_TS_ESTF_COMP_LOW_REG	Time Stamp ESTF Generate Function Comparison Low Value	310D 0200h
204h	CPTS_TS_ESTF_COMP_HIGH_REG	Time Stamp ESTF Generate Function Comparison high Value	310D 0204h
208h	CPTS_TS_ESTF_CONTROL_REG	Time Stamp ESTF Generate Function Control	310D 0208h
20Ch	CPTS_TS_ESTF_LENGTH_REG	Time Stamp ESTF Generate Function Length Value	310D 020Ch

Table 24-2. NAVSS0_CPTS Registers (continued)

Offset	Acronym	Register Name	NAVSS0_CPTS Physical Address
210h	CPTS_TS_ESTF_PPM_LOW_REG	Time Stamp ESTF Generate Function PPM Low Value	310D 0210h
214h	CPTS_TS_ESTF_PPM_HIGH_REG	Time Stamp ESTF Generate Function PPM High Value	310D 0214h
218h	CPTS_TS_ESTF_NUDGE_REG	Time Stamp ESTF Generate Function Nudge Value	310D 0218h

24.1 CPTS_IDVER_REG Register (Offset = 0h) [reset = X]

CPTS_IDVER_REG is shown in [Figure 24-1](#) and described in [Table 24-4](#).

Return to [Summary Table](#).

Identification and Version Register

Table 24-3. CPTS_IDVER_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0000h

Figure 24-1. CPTS_IDVER_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TX_IDENT															
R-4E8Ah															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_VER					MINOR_VER					
R-0h					R-1h					R-Ah					

LEGEND: R = Read Only; -n = value after reset

Table 24-4. CPTS_IDVER_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	TX_IDENT	R	4E8Ah	Identification value
15-11	RTL_VER	R	0h	RTL version value
10-8	MAJOR_VER	R	1h	Major version value
7-0	MINOR_VER	R	Ah	Minor version value

24.2 CPTS_CONTROL_REG Register (Offset = 4h) [reset = X]

CPTS_CONTROL_REG is shown in [Figure 24-2](#) and described in [Table 24-6](#).

Return to [Summary Table](#).

Time Sync Control Register

Table 24-5. CPTS_CONTROL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0004h

Figure 24-2. CPTS_CONTROL_REG Register

31	30	29	28	27	26	25	24
TS_SYNC_SEL				RESERVED			
R/W-0h				R/W-X			
23	22	21	20	19	18	17	16
RESERVED							TS_RX_NO_EV ENT
R/W-X							R/W-0h
15	14	13	12	11	10	9	8
HW8_TS_PUS H_EN	HW7_TS_PUS H_EN	HW6_TS_PUS H_EN	HW5_TS_PUS H_EN	HW4_TS_PUS H_EN	HW3_TS_PUS H_EN	HW2_TS_PUS H_EN	HW1_TS_PUS H_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
TS_PPM_DIR	TS_COMP_TO G	MODE	SEQUENCE_E N	TSTAMP_EN	TS_COMP_PO LARITY	INT_TEST	CPTS_EN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-6. CPTS_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	TS_SYNC_SEL	R/W	0h	TS_SYNC output timestamp counter bit select 0000 – TS_SYNC disabled 0001 0001..1111 - TS_SYNC is timestamp counter bits 31 (1111) down to 17 (0001)
27-17	RESERVED	R/W	X	
16	TS_RX_NO_EVENT	R/W	0h	Timestamp Ethernet Receive produces no events 0 – Ethernet receive timesync events enabled 1 – Ethernet receive timesync events disabled
15	HW8_TS_PUSH_EN	R/W	0h	Hardware push 8 enable
14	HW7_TS_PUSH_EN	R/W	0h	Hardware push 7 enable
13	HW6_TS_PUSH_EN	R/W	0h	Hardware push 6 enable
12	HW5_TS_PUSH_EN	R/W	0h	Hardware push 5 enable
11	HW4_TS_PUSH_EN	R/W	0h	Hardware push 4 enable
10	HW3_TS_PUSH_EN	R/W	0h	Hardware push 3 enable
9	HW2_TS_PUSH_EN	R/W	0h	Hardware push 2 enable
8	HW1_TS_PUSH_EN	R/W	0h	Hardware push 1 enable
7	TS_PPM_DIR	R/W	0h	Timestamp PPM Direction 0 – Increase the time_stamp[63:0] value by the PPM value 1 – Decrease the time_stamp[63:0] value by the PPM value

Table 24-6. CPTS_CONTROL_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	TS_COMP_TOG	R/W	0h	Timestamp Compare Toggle mode: 0=TS_COMP is in non-toggle mode 1=TS_COMP is in toggle mode
5	MODE	R/W	0h	Timestamp mode 0 – The timestamp is 32-bits with the upper 32-bits forced to zero. 1 – The timestamp is 64-bits.
4	SEQUENCE_EN	R/W	0h	Sequence Enable 0 – The timestamp value increments with the selected RFTCLK 1 - The timestamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc).
3	TSTAMP_EN	R/W	0h	Host Receive Timestamp Enable 0 – Timestamps are disabled on received packets to host 1 – Timestamps enabled on received packets to host (cpts_en must be set)
2	TS_COMP_POLARITY	R/W	1h	TS_COMP polarity 0 – TS_COMP is asserted low 1 – TS_COMP is asserted high
1	INT_TEST	R/W	0h	Interrupt test When set, this bit allows the raw interrupt to be written to facilitate interrupt test.
0	CPTS_EN	R/W	0h	Time sync enable When disabled (cleared to zero), the RCLK domain is held in reset.

24.3 CPTS_RFTCLK_SEL_REG Register (Offset = 8h) [reset = X]

CPTS_RFTCLK_SEL_REG is shown in [Figure 24-3](#) and described in [Table 24-8](#).

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RFTCLK Select Register

Table 24-7. CPTS_RFTCLK_SEL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0008h

Figure 24-3. CPTS_RFTCLK_SEL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												RFTCLK_SEL			
R/W-X												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-8. CPTS_RFTCLK_SEL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R/W	X	
4-0	RFTCLK_SEL	R/W	0h	Reference clock select. NOT FUNCTIONAL. See CTRLMMR_NAVSS_CLKSEL[3-0] CPTS_CLKSEL instead.

24.4 CPTS_TS_PUSH_REG Register (Offset = Ch) [reset = X]

CPTS_TS_PUSH_REG is shown in [Figure 24-4](#) and described in [Table 24-10](#).

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Time Stamp Event Push Register

Table 24-9. CPTS_TS_PUSH_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 000Ch

Figure 24-4. CPTS_TS_PUSH_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PUSH
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 24-10. CPTS_TS_PUSH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_PUSH	W	0h	Time stamp event push When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time).

24.5 CPTS_TS_LOAD_VAL_REG Register (Offset = 10h) [reset = 0h]

CPTS_TS_LOAD_VAL_REG is shown in [Figure 24-5](#) and described in [Table 24-12](#).

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Time Stamp Load Low Value Register

Table 24-11. CPTS_TS_LOAD_VAL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0010h

Figure 24-5. CPTS_TS_LOAD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-12. CPTS_TS_LOAD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load low value Writing the ts_load_en bit causes ts_load[63:0] to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register.

24.6 CPTS_TS_LOAD_EN_REG Register (Offset = 14h) [reset = X]

CPTS_TS_LOAD_EN_REG is shown in [Figure 24-6](#) and described in [Table 24-14](#).

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Time Stamp Load Enable Register

Table 24-13. CPTS_TS_LOAD_EN_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0014h

Figure 24-6. CPTS_TS_LOAD_EN_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_LOAD_EN
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 24-14. CPTS_TS_LOAD_EN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	TS_LOAD_EN	W	0h	Time stamp load enable Writing a one to this bit enables the time stamp value to be written with the value in ts_load[63:0]. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the timestamp are forced to zero in 32-bit mode.

24.7 CPTS_TS_COMP_VAL_REG Register (Offset = 18h) [reset = 0h]

CPTS_TS_COMP_VAL_REG is shown in [Figure 24-7](#) and described in [Table 24-16](#).

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Time Stamp Comparison Low Value Register

Table 24-15. CPTS_TS_COMP_VAL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0018h

Figure 24-7. CPTS_TS_COMP_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-16. CPTS_TS_COMP_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_VAL	R/W	0h	Time stamp comparison low value Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val.

24.8 CPTS_TS_COMP_LEN_REG Register (Offset = 1Ch) [reset = 0h]

CPTS_TS_COMP_LEN_REG is shown in [Figure 24-8](#) and described in [Table 24-18](#).

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Time Stamp Comparison Length Register

Table 24-17. CPTS_TS_COMP_LEN_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 001Ch

Figure 24-8. CPTS_TS_COMP_LEN_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-18. CPTS_TS_COMP_LEN_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_LENGTH	R/W	0h	Time stamp comparison length Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the TS_Comp_Low and TS_Comp_High registers are written.

24.9 CPTS_INTSTAT_RAW_REG Register (Offset = 20h) [reset = X]

CPTS_INTSTAT_RAW_REG is shown in [Figure 24-9](#) and described in [Table 24-20](#).

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Interrupt Status Register Raw

Table 24-19. CPTS_INTSTAT_RAW_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0020h

Figure 24-9. CPTS_INTSTAT_RAW_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_RAW
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-20. CPTS_INTSTAT_RAW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_RAW	R/W	0h	TS_PEND_RAW int read (before enable) Writable when int_test = 1. A one in this bit indicates that there are one or more events in the event FIFO.

24.10 CPTS_INTSTAT_MASKED_REG Register (Offset = 24h) [reset = X]

CPTS_INTSTAT_MASKED_REG is shown in [Figure 24-10](#) and described in [Table 24-22](#).

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Interrupt Status Register Masked

**Table 24-21. CPTS_INTSTAT_MASKED_REG
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 0024h

Figure 24-10. CPTS_INTSTAT_MASKED_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND
R-X							R-0h

LEGEND: R = Read Only; -n = value after reset

Table 24-22. CPTS_INTSTAT_MASKED_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	TS_PEND	R	0h	TS_PEND masked interrupt read (after enable)

24.11 CPTS_INT_ENABLE_REG Register (Offset = 28h) [reset = X]

CPTS_INT_ENABLE_REG is shown in [Figure 24-11](#) and described in [Table 24-24](#).

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Interrupt Enable Register

Table 24-23. CPTS_INT_ENABLE_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0028h

Figure 24-11. CPTS_INT_ENABLE_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							TS_PEND_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-24. CPTS_INT_ENABLE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	TS_PEND_EN	R/W	0h	TS_PEND masked interrupt enable

24.12 CPTS_TS_COMP_NUDGE_REG Register (Offset = 2Ch) [reset = X]

CPTS_TS_COMP_NUDGE_REG is shown in [Figure 24-12](#) and described in [Table 24-26](#).

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Time Stamp Comparison Nudge Register

**Table 24-25. CPTS_TS_COMP_NUDGE_REG
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 002Ch

Figure 24-12. CPTS_TS_COMP_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-26. CPTS_TS_COMP_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	This 2s complement number is added to the ts_comp_length value to increase or decrease the TS_COMP length by the nudge amount Only a single high or low time is adjusted and the ts_comp_nudge value is cleared to zero when the nudge has occurred.

24.13 CPTS_EVENT_POP_REG Register (Offset = 30h) [reset = X]

CPTS_EVENT_POP_REG is shown in [Figure 24-13](#) and described in [Table 24-28](#).

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Event Pop Register

Table 24-27. CPTS_EVENT_POP_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0030h

Figure 24-13. CPTS_EVENT_POP_REG Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED							
W-X							
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED							EVENT_POP
W-X							W-0h

LEGEND: W = Write Only; -n = value after reset

Table 24-28. CPTS_EVENT_POP_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	W	X	
0	EVENT_POP	W	0h	Event pop When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the Event_0-3 registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt.

24.14 CPTS_EVENT_0_REG Register (Offset = 34h) [reset = 0h]

CPTS_EVENT_0_REG is shown in [Figure 24-14](#) and described in [Table 24-30](#).

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Event 0 Register

Table 24-29. CPTS_EVENT_0_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0034h

Figure 24-14. CPTS_EVENT_0_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 24-30. CPTS_EVENT_0_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types.

24.15 CPTS_EVENT_1_REG Register (Offset = 38h) [reset = X]

CPTS_EVENT_1_REG is shown in [Figure 24-15](#) and described in [Table 24-32](#).

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Event 1 Register

Table 24-31. CPTS_EVENT_1_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0038h

Figure 24-15. CPTS_EVENT_1_REG Register

31	30	29	28	27	26	25	24
RESERVED		PREMPT_QUEUE	PORT_NUMBER				
R-X		R-0h	R-0h				
23	22	21	20	19	18	17	16
EVENT_TYPE				MESSAGE_TYPE			
R-0h				R-0h			
15	14	13	12	11	10	9	8
SEQUENCE_ID							
R-0h							
7	6	5	4	3	2	1	0
SEQUENCE_ID							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 24-32. CPTS_EVENT_1_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	X	
29	PREMPT_QUEUE	R	0h	Prempt QUEUE 0 – The packet was received/transmitted on the express queue. 1 – The packet was received/transmitted on the preempt queue.
28-24	PORT_NUMBER	R	0h	Port number indicates the port number (encoded) of an Ethernet event or the encoded hardware timestamp number.
23-20	EVENT_TYPE	R	0h	Event type 0000 – Time Stamp Push Event 0001 – Time Stamp Rollover Event 0010 – Time Stamp Half Rollover Event 0011 – Hardware Time Stamp Push Event 0100 – Ethernet Receive Event 0101 – Ethernet Transmit Event 0110 – Time Stamp Compare Event 0111 – Host Transmit Event 1000 1111 reserved
19-16	MESSAGE_TYPE	R	0h	Message type The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.
15-0	SEQUENCE_ID	R	0h	Sequence ID The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

24.16 CPTS_EVENT_2_REG Register (Offset = 3Ch) [reset = X]

CPTS_EVENT_2_REG is shown in [Figure 24-16](#) and described in [Table 24-34](#).

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Event 2 Register

Table 24-33. CPTS_EVENT_2_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 003Ch

Figure 24-16. CPTS_EVENT_2_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DOMAIN							
R-X																								R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 24-34. CPTS_EVENT_2_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	X	
7-0	DOMAIN	R	0h	Domain The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.

24.17 CPTS_EVENT_3_REG Register (Offset = 40h) [reset = 0h]

CPTS_EVENT_3_REG is shown in [Figure 24-17](#) and described in [Table 24-36](#).

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Event 3 Register

Table 24-35. CPTS_EVENT_3_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0040h

Figure 24-17. CPTS_EVENT_3_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIME_STAMP																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 24-36. CPTS_EVENT_3_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TIME_STAMP	R	0h	Time Stamp The timestamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode.

24.18 CPTS_TS_LOAD_HIGH_VAL_REG Register (Offset = 44h) [reset = 0h]

CPTS_TS_LOAD_HIGH_VAL_REG is shown in [Figure 24-18](#) and described in [Table 24-38](#).

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Time Stamp Load High Value Register

**Table 24-37. CPTS_TS_LOAD_HIGH_VAL_REG
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 0044h

Figure 24-18. CPTS_TS_LOAD_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_LOAD_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-38. CPTS_TS_LOAD_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_LOAD_VAL	R/W	0h	Time stamp load high value Writing the ts_load_en bit causes the value contained in this register (and the ts_load[63:0]) to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode

24.19 CPTS_TS_COMP_HIGH_VAL_REG Register (Offset = 48h) [reset = 0h]

CPTS_TS_COMP_HIGH_VAL_REG is shown in [Figure 24-19](#) and described in [Table 24-40](#).

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Time Stamp Comparison High Value Register

Table 24-39. CPTS_TS_COMP_HIGH_VAL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0048h

Figure 24-19. CPTS_TS_COMP_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_COMP_HIGH_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-40. CPTS_TS_COMP_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_COMP_HIGH_VAL	R/W	0h	Time stamp comparison high value Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val[63:0]. This value is unused in 32-bit mode. The upper 32-bits in this register should be written before the lower 32-bits in the TS_Comp_Low register.

24.20 CPTS_TS_ADD_VAL_REG Register (Offset = 4Ch) [reset = X]

CPTS_TS_ADD_VAL_REG is shown in [Figure 24-20](#) and described in [Table 24-42](#).

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TS Add Value Register

Table 24-41. CPTS_TS_ADD_VAL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 004Ch

Figure 24-20. CPTS_TS_ADD_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED												ADD_VAL			
R/W-X												R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-42. CPTS_TS_ADD_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R/W	X	
2-0	ADD_VAL	R/W	0h	Add Value Add Value is added to 1 to comprise the timestamp increment value. The timestamp increment value is added to the current timestamp (time_stamp[63:0]) on each RCLK. The timestamp increment value can be adjusted by nudge and ppm also. The ts_add_val[2:0] value may be non-zero in 64-bit mode only.

24.21 CPTS_TS_PPM_LOW_VAL_REG Register (Offset = 50h) [reset = 0h]

CPTS_TS_PPM_LOW_VAL_REG is shown in [Figure 24-21](#) and described in [Table 24-44](#).

Return to [Summary Table](#).

Time Stamp PPM Low Value Register

Table 24-43. CPTS_TS_PPM_LOW_VAL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0050h

Figure 24-21. CPTS_TS_PPM_LOW_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS_PPM_LOW_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-44. CPTS_TS_PPM_LOW_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	TS_PPM_LOW_VAL	R/W	0h	Time stamp PPM Low value The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen

24.22 CPTS_TS_PPM_HIGH_VAL_REG Register (Offset = 54h) [reset = X]

CPTS_TS_PPM_HIGH_VAL_REG is shown in [Figure 24-22](#) and described in [Table 24-46](#).

Return to [Summary Table](#).

Time Stamp PPM High Value Register

**Table 24-45. CPTS_TS_PPM_HIGH_VAL_REG
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 0054h

Figure 24-22. CPTS_TS_PPM_HIGH_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_PPM_HIGH_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-46. CPTS_TS_PPM_HIGH_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TS_PPM_HIGH_VAL	R/W	0h	Time stamp PPM High value This value should be written first (before the low value is written). The minimum value of the ts_ppm is 0x400 (all 42 bits).

24.23 CPTS_TS_NUDGE_VAL_REG Register (Offset = 58h) [reset = X]

CPTS_TS_NUDGE_VAL_REG is shown in [Figure 24-23](#) and described in [Table 24-48](#).

Return to [Summary Table](#).

Time Stamp Nudge Value Register

Table 24-47. CPTS_TS_NUDGE_VAL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0058h

Figure 24-23. CPTS_TS_NUDGE_VAL_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								TS_NUDGE_VAL							
R/W-X								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-48. CPTS_TS_NUDGE_VAL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	TS_NUDGE_VAL	R/W	0h	Time stamp Nudge value This two's complement number is added to the time_stamp[63:0] value to increase or decrease the timestamp value by the ts_nudge amount. The ts_nudge value is cleared to zero when the nudge has occurred.

24.24 CPTS_TS_GENF_COMP_LOW_REG_j Register (Offset = E0h + formula) [reset = 0h]

CPTS_COMP_LOW_REG_j is shown in [Figure 24-24](#) and described in [Table 24-50](#).

Return to [Summary Table](#).

Time Stamp Generate Function Comparison Low Value

Offset = E0h + (j * 20h); where j = 0h to 5h

**Table 24-49. CPTS_TS_GENF_COMP_LOW_REG_j
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 00E0h + formula

Figure 24-24. CPTS_TS_GENF_COMP_LOW_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-50. CPTS_TS_GENF_COMP_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp Generate Function Comparison Low Value This value should be written after the upper 32-bits. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero.

24.25 CPTS_TS_GENF_COMP_HIGH_REG_j Register (Offset = E4h + formula) [reset = 0h]

CPTS_COMP_HIGH_REG_j is shown in [Figure 24-25](#) and described in [Table 24-52](#).

Return to [Summary Table](#).

Time Stamp Generate Function Comparison high Value

Offset = E4h + (j * 20h); where j = 0h to 5h

Table 24-51. CPTS_TS_GENF_COMP_HIGH_REG_j Instances

Instance	Physical Address
NAVSS0_CPTS	310D 00E4h + formula

Figure 24-25. CPTS_TS_GENF_COMP_HIGH_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-52. CPTS_TS_GENF_COMP_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp Generate Function Comparison High Value This value should be written before the lower 32-bits are written. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero.

24.26 CPTS_TS_GENF_CONTROL_REG_j Register (Offset = E8h + formula) [reset = X]

CPTS_CONTROL_REG_j is shown in [Figure 24-26](#) and described in [Table 24-54](#).

Return to [Summary Table](#).

Time Stamp Generate Function Control

Offset = E8h + (j * 20h); where j = 0h to 5h

**Table 24-53. CPTS_TS_GENF_CONTROL_REG_j
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 00E8h + formula

Figure 24-26. CPTS_TS_GENF_CONTROL_REG_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PPM_DIR	POLARITY_INV
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-54. CPTS_TS_GENF_CONTROL_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	PPM_DIR	R/W	0h	Time Stamp Generate Function PPM Direction 0 – A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1 – A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Time Stamp Generate Function Polarity Invert 0 – The output TS_GENFn signal asserts high 1 – The output TS_GENFn signal asserts low

24.27 CPTS_TS_GENF_LENGTH_REG_j Register (Offset = ECh + formula) [reset = 0h]

CPTS_LENGTH_REG_j is shown in [Figure 24-27](#) and described in [Table 24-56](#).

Return to [Summary Table](#).

Time Stamp Generate Function Length Value

Offset = ECh + (j * 20h); where j = 0h to 5h

**Table 24-55. CPTS_TS_GENF_LENGTH_REG_j
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 00ECh + formula

Figure 24-27. CPTS_TS_GENF_LENGTH_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-56. CPTS_TS_GENF_LENGTH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp Generate Function Length Value The minimum value is decimal 5

24.28 CPTS_TS_GENF_PPM_LOW_REG_j Register (Offset = F0h + formula) [reset = 0h]

CPTS_PPM_LOW_REG_j is shown in [Figure 24-28](#) and described in [Table 24-58](#).

Return to [Summary Table](#).

Time Stamp Generate Function PPM Low Value

Offset = F0h + (j * 20h); where j = 0h to 5h

**Table 24-57. CPTS_TS_GENF_PPM_LOW_REG_j
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 00F0h + formula

Figure 24-28. CPTS_TS_GENF_PPM_LOW_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-58. CPTS_TS_GENF_PPM_LOW_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp Generate Function PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first

24.29 CPTS_TS_GENF_PPM_HIGH_REG_j Register (Offset = F4h + formula) [reset = X]

CPTS_PPM_HIGH_REG_j is shown in [Figure 24-29](#) and described in [Table 24-60](#).

Return to [Summary Table](#).

Time Stamp Generate Function PPM High Value

Offset = F4h + (j * 20h); where j = 0h to 5h

**Table 24-59. CPTS_TS_GENF_PPM_HIGH_REG_j
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 00F4h + formula

Figure 24-29. CPTS_TS_GENF_PPM_HIGH_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-60. CPTS_TS_GENF_PPM_HIGH_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp Generate Function PPM High Value This value should be written first (before the low value is written).

24.30 CPTS_TS_GENF_NUDGE_REG_j Register (Offset = F8h + formula) [reset = X]

CPTS_NUDGE_REG_j is shown in [Figure 24-30](#) and described in [Table 24-62](#).

Return to [Summary Table](#).

Time Stamp Generate Function Nudge Value

Offset = F8h + (j * 20h); where j = 0h to 5h

**Table 24-61. CPTS_TS_GENF_NUDGE_REG_j
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 00F8h + formula

Figure 24-30. CPTS_TS_GENF_NUDGE_REG_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-62. CPTS_TS_GENF_NUDGE_REG_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp Generate Function Nudge Value This two's complement number is added to the generate counter value to increase or decrease the length by the ts_genfN_nudge amount. Only a single high or low time is adjusted and the ts_genfN_nudge value is cleared to zero when the nudge has occurred.

24.31 CPTS_TS_ESTF_COMP_LOW_REG Register (Offset = 200h) [reset = 0h]

CPTS_COMP_LOW_REG is shown in [Figure 24-31](#) and described in [Table 24-64](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Comparison Low Value

Table 24-63. CPTS_TS_ESTF_COMP_LOW_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0200h

Figure 24-31. CPTS_TS_ESTF_COMP_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-64. CPTS_TS_ESTF_COMP_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_LOW	R/W	0h	Time Stamp ESTF Generate Function Comparison Low Value This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero.

24.32 CPTS_TS_ESTF_COMP_HIGH_REG Register (Offset = 204h) [reset = 0h]

CPTS_COMP_HIGH_REG is shown in [Figure 24-32](#) and described in [Table 24-66](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Comparison high Value

Table 24-65. CPTS_TS_ESTF_COMP_HIGH_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0204h

Figure 24-32. CPTS_TS_ESTF_COMP_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP_HIGH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-66. CPTS_TS_ESTF_COMP_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COMP_HIGH	R/W	0h	Time Stamp ESTF Generate Function Comparison High Value This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero

24.33 CPTS_TS_ESTF_CONTROL_REG Register (Offset = 208h) [reset = X]

CPTS_CONTROL_REG is shown in [Figure 24-33](#) and described in [Table 24-68](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Control

Table 24-67. CPTS_TS_ESTF_CONTROL_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0208h

Figure 24-33. CPTS_TS_ESTF_CONTROL_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						PPM_DIR	POLARITY_INV
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-68. CPTS_TS_ESTF_CONTROL_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	PPM_DIR	R/W	0h	Time Stamp ESTF Generate Function PPM Direction 0 – A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount. 1 – A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount.
0	POLARITY_INV	R/W	0h	Time Stamp ESTF Generate Function Polarity Invert 0 – The output TS_ESTFn signal asserts low 1 – The output TS_ESTFn signal asserts high

24.34 CPTS_TS_ESTF_LENGTH_REG Register (Offset = 20Ch) [reset = 0h]

CPTS_LENGTH_REG is shown in [Figure 24-34](#) and described in [Table 24-70](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Length Value

**Table 24-69. CPTS_TS_ESTF_LENGTH_REG
Instances**

Instance	Physical Address
NAVSS0_CPTS	310D 020Ch

Figure 24-34. CPTS_TS_ESTF_LENGTH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LENGTH																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-70. CPTS_TS_ESTF_LENGTH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LENGTH	R/W	0h	Time Stamp ESTF Generate Function Length Value

24.35 CPTS_TS_ESTF_PPM_LOW_REG Register (Offset = 210h) [reset = 0h]

CPTS_PPM_LOW_REG is shown in [Figure 24-35](#) and described in [Table 24-72](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function PPM Low Value

Table 24-71. CPTS_TS_ESTF_PPM_LOW_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0210h

Figure 24-35. CPTS_TS_ESTF_PPM_LOW_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPM_LOW																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-72. CPTS_TS_ESTF_PPM_LOW_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PPM_LOW	R/W	0h	Time Stamp ESTF Generate Function PPM Low Value The 64-bit PPM value takes effect when this low value is written. The high value should be written first.

24.36 CPTS_TS_ESTF_PPM_HIGH_REG Register (Offset = 214h) [reset = X]

CPTS_PPM_HIGH_REG is shown in [Figure 24-36](#) and described in [Table 24-74](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function PPM High Value

Table 24-73. CPTS_TS_ESTF_PPM_HIGH_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0214h

Figure 24-36. CPTS_TS_ESTF_PPM_HIGH_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
RESERVED																						PPM_HIGH															
R/W-X																						R/W-0h															

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-74. CPTS_TS_ESTF_PPM_HIGH_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	PPM_HIGH	R/W	0h	Time Stamp ESTF Generate Function PPM High Value This value should be written first (before the low value is written).

24.37 CPTS_TS_ESTF_NUDGE_REG Register (Offset = 218h) [reset = X]

CPTS_NUDGE_REG is shown in [Figure 24-37](#) and described in [Table 24-76](#).

Return to [Summary Table](#).

Time Stamp ESTF Generate Function Nudge Value

Table 24-75. CPTS_TS_ESTF_NUDGE_REG Instances

Instance	Physical Address
NAVSS0_CPTS	310D 0218h

Figure 24-37. CPTS_TS_ESTF_NUDGE_REG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								NUDGE							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24-76. CPTS_TS_ESTF_NUDGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	NUDGE	R/W	0h	Time Stamp ESTF Generate Function Nudge Value This two's complement number is added to the generate counter value to increase or decrease the length by the ts_estfN_nudge amount. Only a single high or low time is adjusted and the ts_estfN_nudge value is cleared to zero when the nudge has occurred.

25 Timer Manager Registers

25.1 TIMERMGR_CFG_CFG Registers

Table 25-2 lists the memory-mapped registers for the TIMERMGR_CFG_CFG. All register offset addresses not listed in Table 25-2 should be considered as reserved locations and the register contents should not be modified.

CFG MMR definitions

Table 25-1. TIMERMGR_CFG_CFG Instances

Instance	Base Address
NAVSS0_TIMERMGR0_CFG	30E8 0000h
NAVSS0_TIMERMGR1_CFG	30E8 1000h

Table 25-2. TIMERMGR_CFG_CFG Registers

Offset	Acronym	Register Name	NAVSS0_TIMERMGR0_CFG Physical Address	NAVSS0_TIMERMGR1_CFG Physical Address
0h	TIMERMGR_PID	Peripheral ID register	30E8 0000h	30E8 1000h
4h	TIMERMGR_CNTL	Timer manager control	30E8 0004h	30E8 1004h
8h	TIMERMGR_COUNTER	The current counter value	30E8 0008h	30E8 1008h
A0h	TIMERMGR_TIMEOUT_STATUS0	Must be read whenever the timer interrupt fires	30E8 00A0h	30E8 10A0h
A4h	TIMERMGR_TIMEOUT_STATUS1	Contains the IDs of the second and third timers to expire	30E8 00A4h	30E8 10A4h
A8h	TIMERMGR_TIMEOUT_STATUS_BANK0	Contains the status of each timer bank for banks 31-0	30E8 00A8h	30E8 10A8h
100h + formula	TIMERMGR_STATUS_y	Each bit is the timeout status for an individual timer	30E8 0100h + formula	30E8 1100h + formula

25.1.1 TIMERMGR_PID Register (Offset = 0h) [reset = Xh]

TIMERMGR_PID is shown in [Figure 25-1](#) and described in [Table 25-4](#).

Return to [Summary Table](#).

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space

Reset = 66F8 B100h

Table 25-3. TIMERMGR_PID Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 0000h
NAVSS0_TIMERMGR1_CFG	30E8 1000h

Figure 25-1. TIMERMGR_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNCTION											
R-1h		R-2h		R-6F8h											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL_VER					MAJOR_REV			CUSTOM		MINOR_REV					
R-16h					R-1h			R-0h		R-0h					

LEGEND: R = Read Only; -n = value after reset

Table 25-4. TIMERMGR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	scheme
29-28	BU	R	2h	bu identifier
27-16	FUNCTION	R	6F8h	function identifier
15-11	RTL_VER	R	16h	RTL version number
10-8	MAJOR_REV	R	1h	Major revision number
7-6	CUSTOM	R	0h	custom
5-0	MINOR_REV	R	0h	Minor revision number

25.1.2 TIMERMGR_CNTL Register (Offset = 4h) [reset = X]

TIMERMGR_CNTL is shown in [Figure 25-2](#) and described in [Table 25-6](#).

Return to [Summary Table](#).

This register controls the overall behavior of the timer manager module

Table 25-5. TIMERMGR_CNTL Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 0004h
NAVSS0_TIMERMGR1_CFG	30E8 1004h

Figure 25-2. TIMERMGR_CNTL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			MASS_ENAB LE	RESERVED	MAX_TIMER		
R/W-X			W-0h	R/W-X	R/W-3FFh		
7	6	5	4	3	2	1	0
MAX_TIMER							ENABLE
R/W-3FFh							R/W-0h

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 25-6. TIMERMGR_CNTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12	MASS_ENABLE	W	0h	Always reads zero. When a 1 is written to this bit, all timers from 0 to the MAX_TIMER will be enabled. Useful for initial programming, to not need to loop over every TIMERMGR_CONTROL_j_k register to enable every timer if many or all are being used. This should only be used during initialization, or when ENABLE is set to 0, as this does not set the timers, only enable them
11	RESERVED	R/W	X	
10-1	MAX_TIMER	R/W	3FFh	The maximum timer that will be checked - e.g. if only using 512 timers, set this to 511. All timers above this number will be ignored. Should be set once during initialization
0	ENABLE	R/W	0h	Enables the timer manager. When this bit is zero, the timers will all be halted and will not count 0h = Timer Manager is disabled 1h = Timer Manager is enabled

25.1.3 TIMERMGR_COUNTER Register (Offset = 8h) [reset = 0h]

TIMERMGR_COUNTER is shown in [Figure 25-3](#) and described in [Table 25-8](#).

Return to [Summary Table](#).

This register contains the current TIMERMGR_COUNTER value

Table 25-7. TIMERMGR_COUNTER Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 0008h
NAVSS0_TIMERMGR1_CFG	30E8 1008h

Figure 25-3. TIMERMGR_COUNTER Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 25-8. TIMERMGR_COUNTER Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	The current timer_counter value, in the timebase being used by all timers in this module

25.1.4 TIMERMGR_TIMEOUT_STATUS0 Register (Offset = A0h) [reset = X]

TIMERMGR_TIMEOUT_STATUS0 is shown in [Figure 25-4](#) and described in [Table 25-10](#).

Return to [Summary Table](#).

This register should be read whenever the timer interrupt fires. It indicates the total number of timers that have expired and the ID of the first timer to expire. If NUM_EXPIRED_TIMERS is 1, this is the only register that needs to be read. Depending on the value of NUM_EXPIRED_TIMERS, either TIMERMGR_TIMEOUT_STATUS1 or TIMERMGR_TIMEOUT_STATUS_BANK0 may be read by the software to avoid needing to read all 32 TIMERMGR_STATUS_y registers.

**Table 25-9. TIMERMGR_TIMEOUT_STATUS0
Instances**

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 00A0h
NAVSS0_TIMERMGR1_CFG	30E8 10A0h

Figure 25-4. TIMERMGR_TIMEOUT_STATUS0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
VALID0	EXPIRED_TIMER0						
R-0h	R-0h						
15	14	13	12	11	10	9	8
EXPIRED_TIMER0				NUM_EXPIRED_TIMERS			
R-0h				R-0h			
7	6	5	4	3	2	1	0
NUM_EXPIRED_TIMERS							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 25-10. TIMERMGR_TIMEOUT_STATUS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23	VALID0	R	0h	1 indicates that expired_timer0 is a valid expired timer. If num_expired_timers > 0, this should always be a 1
22-12	EXPIRED_TIMER0	R	0h	The ID of the first timer to expire
11-0	NUM_EXPIRED_TIMERS	R	0h	The total number of expired timers

25.1.5 TIMERMGR_TIMEOUT_STATUS1 Register (Offset = A4h) [reset = X]

TIMERMGR_TIMEOUT_STATUS1 is shown in [Figure 25-5](#) and described in [Table 25-12](#).

Return to [Summary Table](#).

This register contains the IDs of the second and third timers to expire. It is intended as a more efficient way of finding the first few timers to expire rather than needing to read the status of all 1024 timers.

**Table 25-11. TIMERMGR_TIMEOUT_STATUS1
Instances**

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 00A4h
NAVSS0_TIMERMGR1_CFG	30E8 10A4h

Figure 25-5. TIMERMGR_TIMEOUT_STATUS1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
VALID2	EXPIRED_TIMER2						
R-0h	R-0h						
15	14	13	12	11	10	9	8
EXPIRED_TIMER2				VALID1	EXPIRED_TIMER1		
R-0h				R-0h	R-0h		
7	6	5	4	3	2	1	0
EXPIRED_TIMER1							
R-0h							

LEGEND: R = Read Only; -n = value after reset

Table 25-12. TIMERMGR_TIMEOUT_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	X	
23	VALID2	R	0h	1 indicates that expired_timer2 is valid
22-12	EXPIRED_TIMER2	R	0h	The ID of the third timer to expire
11	VALID1	R	0h	1 indicates that expired_timer1 is valid
10-0	EXPIRED_TIMER1	R	0h	The ID of the second timer to expire

25.1.6 TIMERMGR_TIMEOUT_STATUS_BANK0 Register (Offset = A8h) [reset = 0h]

TIMERMGR_TIMEOUT_STATUS_BANK0 is shown in [Figure 25-6](#) and described in [Table 25-14](#).

Return to [Summary Table](#).

This register contains the status of each timer bank for banks 31:0. When servicing the timer interrupt, if the num_expired_timers bit is greater than 3, this register may be read to see which banks contain expired timers. The TIMERMGR_STATUS_y registers corresponding to those banks may then be read.

**Table 25-13. TIMERMGR_TIMEOUT_STATUS_BANK0
Instances**

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 00A8h
NAVSS0_TIMERMGR1_CFG	30E8 10A8h

Figure 25-6. TIMERMGR_TIMEOUT_STATUS_BANK0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 25-14. TIMERMGR_TIMEOUT_STATUS_BANK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	A 1 in bit N indicates that the corresponding bank has expired timers

25.1.7 TIMERMGR_STATUS_y Register (Offset = 100h + formula) [reset = 0h]

TIMERMGR_STATUS_y is shown in [Figure 25-7](#) and described in [Table 25-16](#).

Return to [Summary Table](#).

Each bit is the timeout status for an individual timer. 0 = timer has not timed out or is disabled, 1 = timer has timed out

Offset = 100h + (y * 4h); where y = 0h to 1Fh

Table 25-15. TIMERMGR_STATUS_y Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG	30E8 0100h + formula
NAVSS0_TIMERMGR1_CFG	30E8 1100h + formula

Figure 25-7. TIMERMGR_STATUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL																															
R-0h																															

LEGEND: R = Read Only; -n = value after reset

Table 25-16. TIMERMGR_STATUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VAL	R	0h	Each bit is the timeout status for an individual timer

25.2 TIMERMGR_CFG_OES Registers

Table 25-18 lists the memory-mapped registers for the TIMERMGR_CFG_OES. All register offset addresses not listed in Table 25-18 should be considered as reserved locations and the register contents should not be modified.

Event index MMR definitions

Table 25-17. TIMERMGR_CFG_OES Instances

Instance	Base Address
NAVSS0_TIMERMGR0_CFG_OES	30F0 0000h
NAVSS0_TIMERMGR1_CFG_OES	30F0 1000h

Table 25-18. TIMERMGR_CFG_OES Registers

Offset	Acronym	Register Name	NAVSS0_TIMERMGR 0_CFG_OES Physical Address	NAVSS0_TIMERMGR 1_CFG_OES Physical Address
0h + formula	TIMERMGR_EVENTIDX_y	Programs the event index for a given timer	30F0 0000h + formula	30F0 1000h + formula

25.2.1 TIMERMGR_EVENTIDX_y Register (Offset = 0h + formula) [reset = X]

TIMERMGR_EVENTIDX_y is shown in [Figure 25-8](#) and described in [Table 25-20](#).

Return to [Summary Table](#).

This programs the event index for a given timer

Offset = 0h + (y * 4h); where y = 0h to 3FFh

Table 25-19. TIMERMGR_EVENTIDX_y Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG_OES	30F0 0000h
NAVSS0_TIMERMGR1_CFG_OES	30F0 1000h

Figure 25-8. TIMERMGR_EVENTIDX_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VAL															
R/W-X																R/W-FFFFh															

LEGEND: R/W = Read/Write; -n = value after reset

Table 25-20. TIMERMGR_EVENTIDX_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	VAL	R/W	FFFFh	The event index for a given timer to be used on the output event interface

25.3 TIMERMGR_CFG_TIMERS Registers

Table 25-22 lists the memory-mapped registers for the TIMERMGR_CFG_TIMERS. All register offset addresses not listed in Table 25-22 should be considered as reserved locations and the register contents should not be modified.

Timers MMR definitions - runtime region

Table 25-21. TIMERMGR_CFG_TIMERS Instances

Instance	Base Address
NAVSS0_TIMERMGR0_CFG_TIMERS	3220 0000h
NAVSS0_TIMERMGR1_CFG_TIMERS	3224 0000h

Table 25-22. TIMERMGR_CFG_TIMERS Registers

Offset	Acronym	Register Name	NAVSS0_TIMERMGR0_CFG_TIMERS Physical Address	NAVSS0_TIMERMGR1_CFG_TIMERS Physical Address
0h + formula	TIMERMGR_SETUP_j_k	This reprograms timer N with the written value	3220 0000h + formula	3224 0000h + formula
4h + formula	TIMERMGR_CONTROL_j_k	Modifies the behavior of timer N	3220 0004h + formula	3224 0004h + formula

25.3.1 TIMERMGR_SETUP_j_k Register (Offset = 0h + formula) [reset = 0h]

TIMERMGR_SETUP_j_k is shown in [Figure 25-9](#) and described in [Table 25-24](#).

Return to [Summary Table](#).

This reprograms timer N with the written value. This number will be the number of ticks of the timer_clock before the timer expires, if timer N and the timer manager itself are both enabled via TIMERMGR_CNTL and TIMERMGR_CONTROL_j_k

Offset = 0h + (j * 1000h) + (k * 100h); where j = 0h to 3Fh, k = 0h to Fh

Table 25-23. TIMERMGR_SETUP_j_k Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG_TIMERS	3220 0000h + formula
NAVSS0_TIMERMGR1_CFG_TIMERS	3224 0000h + formula

Figure 25-9. TIMERMGR_SETUP_j_k Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COUNT																															
R/W-0h																															

LEGEND: R/W = Read/Write; -n = value after reset

Table 25-24. TIMERMGR_SETUP_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COUNT	R/W	0h	The number of ticks of the timer_clock before this timer would expire when reprogrammed

25.3.2 TIMERMGR_CONTROL_j_k Register (Offset = 4h + formula) [reset = X]

TIMERMGR_CONTROL_j_k is shown in [Figure 25-10](#) and described in [Table 25-26](#).

Return to [Summary Table](#).

Modifies the behavior of timer N with control signals below

Offset = 4h + (j * 1000h) + (k * 100h); where j = 0h to 3Fh, k = 0h to Fh

Table 25-25. TIMERMGR_CONTROL_j_k Instances

Instance	Physical Address
NAVSS0_TIMERMGR0_CFG_TIMERS	3220 0004h + formula
NAVSS0_TIMERMGR1_CFG_TIMERS	3224 0004h + formula

Figure 25-10. TIMERMGR_CONTROL_j_k Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							AUTORESET
R/W-X							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					EXPIRED	SET	ENABLE
R/W-X					R-0h	W-0h	R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 25-26. TIMERMGR_CONTROL_j_k Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R/W	X	
8	AUTORESET	R/W	0h	Automatically reset the timer when it expires. Provides the option of a periodic timer, rather than one that needs to be cleared after each expiration. Added for hardware usage of the timers, so the expirations can occur regularly without software reprogramming them.
7-3	RESERVED	R/W	X	
2	EXPIRED	R	0h	The status of the current timer. 1 = expired
1	SET	W	0h	This may be used to touch/set a timer. When a 1 is written, the corresponding timer will be refreshed with the current value in its TIMERMGR_SETUP_j_k register. Will always read 0
0	ENABLE	R/W	0h	Write 1 to enable, 0 to disable the timer.

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