

Technical Reference Manual

J721E DRA829/TDA4VM/AM68P Processors Silicon Revision 1.1 Texas Instruments Families of Products



1 ECAP Registers

Table 1-2 lists the memory-mapped registers for the ECAP modules. All register offset addresses not listed in Table 1-2 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. ECAP Instances

| Instance | Base Address |
|---------------|--------------|
| ECAP0_CTL_STS | 0310 0000h |
| ECAP1_CTL_STS | 0311 0000h |
| ECAP2_CTL_STS | 0312 0000h |

Table 1-2. ECAP Registers

| Offset | Acronym | Register Name | ECAP0_CTL_STS Physical Address | ECAP1_CTL_STS Physical Address | ECAP2_CTL_STS Physical Address |
|--------|------------------------------------|---|--------------------------------------|--------------------------------------|--------------------------------------|
| 0h | ECAP_TSCNT | Time Stamp Counter Register | 0310 0000h | 0311 0000h | 0312 0000h |
| 4h | ECAP_CNTPHS | Counter Phase Control Register | 0310 0004h | 0311 0004h | 0312 0004h |
| 8h | ECAP_CAP1 | Capture-1 Register | 0310 0008h | 0311 0008h | 0312 0008h |
| Ch | ECAP_CAP2 | Capture-2 Register | 0310 000Ch | 0311 000Ch | 0312 000Ch |
| 10h | ECAP_CAP3 | Capture-3 Register | 0310 0010h | 0311 0010h | 0312 0010h |
| 14h | ECAP_CAP4 | Capture-4 Register | 0310 0014h | 0311 0014h | 0312 0014h |
| 28h | ECAP_ECCTL | ECAP Control Register | 0310 0028h | 0311 0028h | 0312 0028h |
| 2Ch | ECAP_ECINT_EN_FLG | ECAP Interrupt Enable and Flag Register | 0310 002Ch | 0311 002Ch | 0312 002Ch |
| 30h | ECAP_ECINT_CLR_FRC | ECAP Interrupt Clear and Forcing Register | 0310 0030h | 0311 0030h | 0312 0030h |
| 5Ch | ECAP_PID | Peripheral ID Register | 0310 005Ch | 0311 005Ch | 0312 005Ch |

1.1 ECAP_TSCNT Register (Offset = 0h) [reset = 0h]

ECAP_TSCNT is shown in [Figure 1-1](#) and described in [Table 1-4](#).

Return to [Summary Table](#).

Time Stamp Counter register

Table 1-3. ECAP_TSCNT Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0000h |
| ECAP1_CTL_STS | 0311 0000h |
| ECAP2_CTL_STS | 0312 0000h |

Figure 1-1. ECAP_TSCNT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TSCNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-4. ECAP_TSCNT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | TSCNT | R/W | 0h | Active 32-bit counter register which is used as the capture time-base. |

1.2 ECAP_CNTPHS Register (Offset = 4h) [reset = 0h]

ECAP_CNTPHS is shown in [Figure 1-2](#) and described in [Table 1-6](#).

[Return to Summary Table.](#)

Counter Phase Control register

Table 1-5. ECAP_CNTPHS Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0004h |
| ECAP1_CTL_STS | 0311 0004h |
| ECAP2_CTL_STS | 0312 0004h |

Figure 1-2. ECAP_CNTPHS Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CNTPHS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-6. ECAP_CNTPHS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|--|
| 31-0 | CNTPHS | R/W | 0h | Counter phase value register that can be programmed for phase Lag/Lead. This register "shadows" the ECAP_TSCNT register and is loaded into the ECAP_TSCNT register upon either a SYNCI event or software force via a control bit. Used to achieve phase control sync with respect to other ECAP and EPWM time-bases. |

1.3 ECAP_CAP1 Register (Offset = 8h) [reset = 0h]

ECAP_CAP1 is shown in [Figure 1-3](#) and described in [Table 1-8](#).

Return to [Summary Table](#).

Capture-1 register

Table 1-7. ECAP_CAP1 Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0008h |
| ECAP1_CTL_STS | 0311 0008h |
| ECAP2_CTL_STS | 0312 0008h |

Figure 1-3. ECAP_CAP1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAP1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-8. ECAP_CAP1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | CAP1 | R/W | 0h | This register can be loaded (written) by: 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes/initialisation. 3. APRD shadow register (ECAP_CAP3) when used in APWM mode. |

1.4 ECAP_CAP2 Register (Offset = Ch) [reset = 0h]

ECAP_CAP2 is shown in [Figure 1-4](#) and described in [Table 1-10](#).

[Return to Summary Table.](#)

Capture-2 register

Table 1-9. ECAP_CAP2 Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 000Ch |
| ECAP1_CTL_STS | 0311 000Ch |
| ECAP2_CTL_STS | 0312 000Ch |

Figure 1-4. ECAP_CAP2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAP2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-10. ECAP_CAP2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | CAP2 | R/W | 0h | This register can be loaded (written) by: <ol style="list-style-type: none"> 1. Time-Stamp (counter value) during a capture event. 2. Software - may be useful for test purposes. 3. ACMP shadow register (ECAP_CAP4) when used in APWM mode. |

1.5 ECAP_CAP3 Register (Offset = 10h) [reset = 0h]

ECAP_CAP3 is shown in [Figure 1-5](#) and described in [Table 1-12](#).

[Return to Summary Table.](#)

Capture-3 register

Table 1-11. ECAP_CAP3 Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0010h |
| ECAP1_CTL_STS | 0311 0010h |
| ECAP2_CTL_STS | 0312 0010h |

Figure 1-5. ECAP_CAP3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAP3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-12. ECAP_CAP3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | CAP3 | R/W | 0h | In CMP mode this is a time-stamp capture register. In APMW mode this is the period shadow (APER) register. User updates the PWM period value via this register. In this mode the ECAP_CAP3 (APRD) register shadows the ECAP_CAP1 register. |

1.6 ECAP_CAP4 Register (Offset = 14h) [reset = 0h]

ECAP_CAP4 is shown in [Figure 1-6](#) and described in [Table 1-14](#).

[Return to Summary Table.](#)

Capture-4 register

Table 1-13. ECAP_CAP4 Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0014h |
| ECAP1_CTL_STS | 0311 0014h |
| ECAP2_CTL_STS | 0312 0014h |

Figure 1-6. ECAP_CAP4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAP4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 1-14. ECAP_CAP4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | CAP4 | R/W | 0h | In CMP mode this is a time-stamp capture register. In APMW mode this is the compare shadow (ACMP) register. User updates the PWM Compare value via this register. In this mode the ECAP_CAP4 (ACMP) register shadows the ECAP_CAP2 register. |

1.7 ECAP_ECCTL Register (Offset = 28h) [reset = 00060000h]

ECAP_ECCTL is shown in [Figure 1-7](#) and described in [Table 1-16](#).

Return to [Summary Table](#).

ECAP Control register

Table 1-15. ECAP_ECCTL Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0028h |
| ECAP1_CTL_STS | 0311 0028h |
| ECAP2_CTL_STS | 0312 0028h |

Figure 1-7. ECAP_ECCTL Register

| | | | | | | | |
|-----------|---------|-----------|----------|-----------------|-----------|----------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FILTER | | | | | APWMPOL | CAP_APWM | SWSYNC |
| R-0h | | | | | R/W-0h | R/W-0h | WCap-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNCO_SEL | | SYNCL_EN | TSCNTSTP | REARM_RESE T | STOPVALUE | | CONT_ONESH T |
| R/W-0h | | R/W-0h | R/W-0h | WCap-0h | R/W-3h | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FREE_SOFT | | EVTFLTPTS | | | | | CAPLDEN |
| R/W-0h | | R/W-0h | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CTRRST4 | CAP4POL | CTRRST3 | CAP3POL | CTRRST2 | CAP2POL | CTRRST1 | CAP1POL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; WCap = Write to Capture; -n = value after reset

Table 1-16. ECAP_ECCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------|------|-------|---|
| 31-27 | FILTER | R | 0h | |
| 26 | APWMPOL | R/W | 0h | APWM Output Polarity Select: 0h = Output is Active High (Compare value defines High time) 1h = Output is Active Low (Compare value defines Low time) Note: This is applicable only in APWM operating mode. |

Table 1-16. ECAP_ECCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| 25 | CAP_APWM | R/W | 0h | <p>CAP/APWM Operating Mode Select:</p> <p>0h = ECAP module operates in Capture mode. This mode forces the following configuration:</p> <ol style="list-style-type: none"> 1. Inhibits the ECAP_TSCNT register resets via PRD event. 2. Inhibits the Shadow loads on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Permits user to enable the ECAP_CAP1 to ECAP_CAP4 register load. 4. CAPx/APWMx pin operates as a Capture input. <p>1h = ECAP module operates in APWM mode. This mode forces the following configuration:</p> <ol style="list-style-type: none"> 1. Resets the ECAP_TSCNT register on PRD event (period boundary) 2. Permits Shadow loading on the ECAP_CAP1 and ECAP_CAP2 registers. 3. Disables loading of Time-stamps into the ECAP_CAP1 - ECAP_CAP4 registers 4. CAPx/APWMx pin operates as a APWM output. |
| 24 | SWSYNC | WCap | 0h | <p>Software Forced Counter (ECAP_TSCNT) Synchronizing:</p> <p>0h = Writing a zero has no effect. Reading will always return a zero.</p> <p>1h = Writing a one will force a ECAP_TSCNT shadow load of current ECAP module and any ECAP modules "down-stream" providing the SYNCO_SEL bits are 0h.</p> <p>After writing a 1h this bit returns to a zero.</p> <p>Note: This provides a convenient software method to synchronize some or all ECAP Timebases.</p> <p>In APWM mode the synchronizing can also be done via the PRD event.</p> |
| 23-22 | SYNCO_SEL | R/W | 0h | <p>SyncOut Select:</p> <p>0h = Select SyncIn event to be the SyncOut signal (pass through)</p> <p>1h = Select PRD event to be the SyncOut signal</p> <p>2h = Disable SyncOut Signal</p> <p>3h = Disable SyncOut Signal</p> <p>Note: Selection PRD is meaningful only in APWM mode, however can still be chosen in CAP mode if user believes it to be useful.</p> |
| 21 | SYNCl_EN | R/W | 0h | <p>Counter (ECAP_TSCNT) SyncIn select mode:</p> <p>0h = Disable SyncIn option</p> <p>1h = Enable Counter (ECAP_TSCNT) to be loaded from the ECAP_CNTPHS register upon either a SYNCl signal or a software force event.</p> |
| 20 | TSCNTSTP | R/W | 0h | <p>Counter Stop (freeze) Control:</p> <p>0h = Counter Stopped</p> <p>1h = Counter Free Running</p> |

Table 1-16. ECAP_ECCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 19 | REARM_RESET | WCap | 0h | One-Shot "Re-arming" Control Wait for stop trigger: Write 0h = Has no effect. Reading always returns a 0h. Note: The RE-ARM function is valid in ONESHT or CONTINUOUS mode. Write 1h = Arms the One-Shot sequence: 1. Resets the Mod4 counter to zero. 2. Un-freezes the Mod4 counter. 3. Enables Capture Register Loads. |
| 18-17 | STOPVALUE | R/W | 3h | Stop Value for One-Shot Mode: This is the number (between 1 and 4) of captures allowed to occur before the ECAP_CAP1 through ECAP_CAP4 registers are frozen (capture sequence is stopped). 0h = Stop after Capture Event 1 1h = Stop after Capture Event 2 2h = Stop after Capture Event 3 3h = Stop after Capture Event 4 Notes: [1] STOPVALUE is compared to Mod4 counter, when equal, two actions occur: 1. Mod4 Counter is stopped (frozen) 2. Capture register loads are inhibited [2] In one shot mode, further interrupt events are blocked until we re-arm, once the number of events captured has been reached. |
| 16 | CONT_ONESHT | R/W | 0h | Continuous or One-shot Mode Control (applicable only in Capture mode): 0h = Operate in Continuous mode 1h = Operate in One-Shot mode |
| 15-14 | FREE_SOFT | R/W | 0h | Emulation Control 0h = ECAP_TSCNT Counter stops immediately on emulation suspend 1h = ECAP_TSCNT Counter runs until = 0h 3h = ECAP_TSCNT Counter is unaffected by emulation suspend (Run Free) |
| 13-9 | EVFTLTPS | R/W | 0h | Event Filter Prescale Select: 0h = Divide by 1 (no prescale, by-pass the prescaler) 1h = Divide by 2 2h = Divide by 4 3h = Divide by 6 4h = Divide by 8 5h = Divide by 10 1Eh = Divide by 60 1Fh = Divide by 62 |

Table 1-16. ECAP_ECCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 8 | CAPLDEN | R/W | 0h | Enable Loading of the ECAP_CAP1 to ECAP_CAP4 registers on a capture event: 0h = Disable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time. 1h = Enable ECAP_CAP1 to ECAP_CAP4 register loads at capture event time. |
| 7 | CTRRST4 | R/W | 0h | Counter Reset on Capture Event 4: 0h = Do Not reset Counter on Capture Event 4 (absolute time stamp) 1h = Reset counter after Event 4 time-stamp has been captured (used in Difference mode operation) |
| 6 | CAP4POL | R/W | 0h | Capture Event 4 Polarity Select: 0h = Capture event 4 triggered on a Rising Edge (RE) 1h = Capture event 4 triggered on a Falling Edge (FE) |
| 5 | CTRRST3 | R/W | 0h | Counter Reset on Capture Event 3: 0h = Do not reset counter on Capture Event 3 (absolute time stamp) 1h = Reset counter after Event 3 time-stamp has been captured (used in difference mode operation) |
| 4 | CAP3POL | R/W | 0h | Capture Event 3 Polarity Select: 0h = Capture event 3 triggered on a Rising Edge (RE) 1h = Capture event 3 triggered on a Falling Edge (FE) |
| 3 | CTRRST2 | R/W | 0h | Counter Reset on Capture Event 2: 0h = Do not reset counter on Capture Event 2 (absolute time stamp) 1h = Reset Counter after Event 2 time-stamp has been captured (used in difference mode operation) |
| 2 | CAP2POL | R/W | 0h | Capture Event 2 Polarity Select: 0h = Capture event 2 triggered on a Rising Edge (RE) 1h = Capture event 2 triggered on a Falling Edge (FE) |
| 1 | CTRRST1 | R/W | 0h | Counter Reset on Capture Event 1: 0h = Do not reset counter on Capture Event 1 (absolute time stamp) 1h = Reset counter after Event 1 time-stamp has been captured (used in difference mode operation) |
| 0 | CAP1POL | R/W | 0h | Capture Event 1 Polarity Select: 0h = Capture event 1 triggered on a Rising Edge (RE) 1h = Capture event 1 triggered on a Falling Edge (FE) |

1.8 ECAP_ECINT_EN_FLG Register (Offset = 2Ch) [reset = X]

ECAP_ECINT_EN_FLG is shown in [Figure 1-8](#) and described in [Table 1-18](#).

Return to [Summary Table](#).

ECAP Interrupt Enable and Flag register

Table 1-17. ECAP_ECINT_EN_FLG Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 002Ch |
| ECAP1_CTL_STS | 0311 002Ch |
| ECAP2_CTL_STS | 0312 002Ch |

Figure 1-8. ECAP_ECINT_EN_FLG Register

| | | | | | | | |
|-----------|-----------|------------|-----------|-----------|-----------|-----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMPEQ_FLG | PRDEQ_FLG | CNTOVF_FLG | CEVT4_FLG | CEVT3_FLG | CEVT2_FLG | CEVT1_FLG | INT_FLG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMPEQ_EN | PRDEQ_EN | CNTOVF_EN | CEVT4_EN | CEVT3_EN | CEVT2_EN | CEVT1_EN | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 1-18. ECAP_ECINT_EN_FLG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved |
| 23 | CMPEQ_FLG | R | 0h | Compare Equal Status Flag: Read 0h = Indicates no event occurred Read 1h = Indicates the counter (ECAP_TSCNT) reached the Compare register value (ACMP) Note: This flag is only active in APWM mode. |
| 22 | PRDEQ_FLG | R | 0h | Period Equal Status Flag: Read 0h = Indicates no event occurred Read 1h = Indicates the Counter (ECAP_TSCNT) reached the Period register value (APER) and was reset. Note: This flag is only active in APWM mode. |
| 21 | CNTOVF_FLG | R | 0h | Counter Overflow Status Flag: Read 0h = Indicates no event occurred. Read 1h = Indicates the Counter (ECAP_TSCNT) has made the transition from FFFF FFFFh to 0000 0000h Note: This flag is active in CAP and APWM mode. |
| 20 | CEVT4_FLG | R | 0h | Capture Event 4 Status Flag: Read 0h = Indicates no event occurred. Read 1h = Indicates the fourth event occurred at ECAPx pin. Note: This flag is only active in CAP mode. |

Table 1-18. ECAP_ECINT_EN_FLG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|--|
| 19 | CEVT3_FLG | R | 0h | Capture Event 3 Status Flag: Read 0h = Indicates no event occurred. Read 1h = Indicates the third event occurred at ECAPx pin. Note: This flag is only active in CAP mode. |
| 18 | CEVT2_FLG | R | 0h | Capture Event 2 Status Flag: Read 0h = Indicates no event occurred. Read 1h = Indicates the second event occurred at ECAPx pin. Note: This flag is only active in CAP mode. |
| 17 | CEVT1_FLG | R | 0h | Capture Event 1 Status Flag: Read 0h = Indicates no event occurred. Read 1h = Indicates the first event occurred at ECAPx pin. Note: This flag is only active in CAP mode. |
| 16 | INT_FLG | R | 0h | Global Interrupt Status Flag: Read 0h = Indicates no interrupt generated. Read 1h = Indicates that an interrupt was generated from one of the following events. |
| 15-8 | RESERVED | R | 0h | Reserved |
| 7 | CMPEQ_EN | R/W | 0h | Compare Equal Interrupt Enable: 0h = Disabled Compare Equal as an Interrupt source 1h = Enable Compare Equal as an Interrupt source |
| 6 | PRDEQ_EN | R/W | 0h | Period Equal Interrupt Enable: 0h = Disabled Period Equal as an Interrupt source 1h = Enable Period Equal as an Interrupt source |
| 5 | CNTOVF_EN | R/W | 0h | Counter Overflow Interrupt Enable: 0h = Disabled Counter Overflow as an Interrupt source 1h = Enable Counter Overflow as an Interrupt source |
| 4 | CEVT4_EN | R/W | 0h | Capture Event 4 Interrupt Enable: 0h = Disabled Capture Event 4 as an Interrupt source: 1h = Enable Capture Event 4 as an Interrupt source |
| 3 | CEVT3_EN | R/W | 0h | Capture Event 3 Interrupt Enable: 0h = Disabled Capture Event 3 as an Interrupt source: 1h = Enable Capture Event 3 as an Interrupt source |
| 2 | CEVT2_EN | R/W | 0h | Capture Event 2 Interrupt Enable: 0h = Disabled Capture Event 2 as an Interrupt source: 1h = Enable Capture Event 2 as an Interrupt source |
| 1 | CEVT1_EN | R/W | 0h | Capture Event 1 Interrupt Enable: 0h = Disabled Capture Event 1 as an Interrupt source: 1h = Enable Capture Event 1 as an Interrupt source |
| 0 | RESERVED | R | 0h | Reserved |

1.9 ECAP_ECINT_CLR_FRC Register (Offset = 30h) [reset = X]

ECAP_ECINT_CLR_FRC is shown in [Figure 1-9](#) and described in [Table 1-20](#).

Return to [Summary Table](#).

ECAP Interrupt Clear and Forcing register

Table 1-19. ECAP_ECINT_CLR_FRC Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 0030h |
| ECAP1_CTL_STS | 0311 0030h |
| ECAP2_CTL_STS | 0312 0030h |

Figure 1-9. ECAP_ECINT_CLR_FRC Register

| | | | | | | | |
|-----------|-----------|------------|-----------|-----------|-----------|-----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMPEQ_FRC | PRDEQ_FRC | CNTOVF_FRC | CEVT4_FRC | CEVT3_FRC | CEVT2_FRC | CEVT1_FRC | RESERVED |
| W1S-0h | W1S-0h | W1S-0h | W1S-0h | W1S-0h | W1S-0h | W1S-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMPEQ_CLR | PRDEQ_CLR | CNTOVF_CLR | CEVT4_CLR | CEVT3_CLR | CEVT2_CLR | CEVT1_CLR | INT_CLR |
| W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h |

LEGEND: W = Write Only; W1C = Write 1 to Clear Bit; W1S = Write 1 to Set Bit; -n = value after reset

Table 1-20. ECAP_ECINT_CLR_FRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved |
| 23 | CMPEQ_FRC | W1S | 0h | Force Compare Equal: Write 0h = No effect. Always reads back a 0h. 1h = Writing a 1h to this bit will set the CMPEQ_FLG flag bit. |
| 22 | PRDEQ_FRC | W1S | 0h | Force Period Equal: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h to this bit will set the PRDEQ_FLG flag bit. |
| 21 | CNTOVF_FRC | W1S | 0h | Force Counter Overflow: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h to this bit will set the CNTOVF_FLG flag bit. |
| 20 | CEVT4_FRC | W1S | 0h | Force Capture Event 4: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h to this bit will set the CEVT4_FLG flag bit. |
| 19 | CEVT3_FRC | W1S | 0h | Force Capture Event 3: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h to this bit will set the CEVT3_FLG flag bit. |
| 18 | CEVT2_FRC | W1S | 0h | Force Capture Event 2: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h to this bit will set the CEVT2_FLG flag bit. |

Table 1-20. ECAP_ECINT_CLR_FRC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 17 | CEVT1_FRC | W1S | 0h | Force Capture Event 1: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h to this bit will set the CEVT1_FLG flag bit. |
| 16-8 | RESERVED | R | 0h | Reserved |
| 7 | CMPEQ_CLR | W1C | 0h | Compare Equal Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the CMPEQ_FLG flag condition. |
| 6 | PRDEQ_CLR | W1C | 0h | Period Equal Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the PRDEQ_FLG flag condition. |
| 5 | CNTOVF_CLR | W1C | 0h | Counter Overflow Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the CNTOVF_FLG flag condition. |
| 4 | CEVT4_CLR | W1C | 0h | Capture Event 4 Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the CEVT4_FLG flag condition. |
| 3 | CEVT3_CLR | W1C | 0h | Capture Event 3 Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the CEVT3_FLG flag condition. |
| 2 | CEVT2_CLR | W1C | 0h | Capture Event 2 Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the CEVT2_FLG flag condition. |
| 1 | CEVT1_CLR | W1C | 0h | Capture Event 1 Status Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the CEVT1_FLG flag condition. |
| 0 | INT_CLR | W1C | 0h | Global Interrupt Clear Flag: Write 0h = No effect. Always reads back a 0. 1h = Writing a 1h will clear the INT_FLG flag and enable further interrupts to be generated if any of the event flags are set to 1h. |

1.10 ECAP_PID Register (Offset = 5Ch) [reset = 44D24100h]

ECAP_PID is shown in [Figure 1-10](#) and described in [Table 1-22](#).

[Return to Summary Table.](#)

Peripheral ID register

Table 1-21. ECAP_PID Instances

| Instance | Physical Address |
|---------------|------------------|
| ECAP0_CTL_STS | 0310 005Ch |
| ECAP1_CTL_STS | 0311 005Ch |
| ECAP2_CTL_STS | 0312 005Ch |

Figure 1-10. ECAP Revision ID Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 44D24100h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 1-22. ECAP_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-----------|--|
| 31-0 | REVISION | R | 44D24100h | TI internal data. Identifies revision of peripheral. |

2 EPWM Registers

Table 2-2 lists the memory-mapped registers for the EPWM modules. All register offset addresses not listed in Table 2-2 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. EPWM Instances

| Instance | Base Address |
|----------------|--------------|
| EHRPWM0_EPWM | 0300 0000h |
| EHRPWM1_EPWM | 0301 0000h |
| EHRPWM2_EPWM | 0302 0000h |
| EHRPWM3_EPWM | 0303 0000h |
| EHRPWM4_EPWM | 0304 0000h |
| EHRPWM5_EPWM | 0305 0000h |
| EHRPWM0_EHRPWM | 0300 8000h |
| EHRPWM1_EHRPWM | 0301 8000h |
| EHRPWM2_EHRPWM | 0302 8000h |
| EHRPWM3_EHRPWM | 0303 8000h |
| EHRPWM4_EHRPWM | 0304 8000h |
| EHRPWM5_EHRPWM | 0305 8000h |

Table 2-2. EPWM Registers

| Offset | Acronym | Register Name | EHRPWM0_ EPWM Physical Address | EHRPWM1_ EPWM Physical Address | EHRPWM2_ EPWM Physical Address |
|--------|-------------------------------|---|--------------------------------|--------------------------------|--------------------------------|
| 0h | EPWM_TBCTL | Time-Base Control Register | 0300 0000h | 0301 0000h | 0302 0000h |
| 2h | EPWM_TBSTS | Time-Base Status Register | 0300 0002h | 0301 0002h | 0302 0002h |
| 4h | HRPWM_TBPHSHR | Time-Base Phase High-Resolution PWM Register | 0300 0004h | 0301 0004h | 0302 0004h |
| 6h | EPWM_TBPHS | Time-Base Counter Phase Register | 0300 0006h | 0301 0006h | 0302 0006h |
| 8h | EPWM_TBCNT | Time-Base Counter Register | 0300 0008h | 0301 0008h | 0302 0008h |
| Ah | EPWM_TBPRD | Time-Base Period Register | 0300 000Ah | 0301 000Ah | 0302 000Ah |
| Eh | EPWM_CMPCTL | Counter-Compare Control Register | 0300 000Eh | 0301 000Eh | 0302 000Eh |
| 10h | HRPWM_CMPAHR | Counter-Compare A High-Resolution Register | 0300 0010h | 0301 0010h | 0302 0010h |
| 12h | EPWM_CMPA | Counter-Compare A Register | 0300 0012h | 0301 0012h | 0302 0012h |
| 14h | EPWM_CMPB | Counter-Compare B Register | 0300 0014h | 0301 0014h | 0302 0014h |
| 16h | EPWM_AQCTLA | Action Qualifier Control Register for Output A | 0300 0016h | 0301 0016h | 0302 0016h |
| 18h | EPWM_AQCTLB | Action Qualifier Control Register for Output B | 0300 0018h | 0301 0018h | 0302 0018h |
| 1Ah | EPWM_AQSFRC | Action Qualifier Software Force Register | 0300 001Ah | 0301 001Ah | 0302 001Ah |
| 1Ch | EPWM_AQCSFRC | Action Qualifier Continuous Software Force Register | 0300 001Ch | 0301 001Ch | 0302 001Ch |
| 1Eh | EPWM_DBCTL | Dead Band Generator Control Register | 0300 001Eh | 0301 001Eh | 0302 001Eh |
| 20h | EPWM_DBRED | Dead Band Generator Rising Edge Delay Count Register | 0300 0020h | 0301 0020h | 0302 0020h |
| 22h | EPWM_DBFED | Dead Band Generator Falling Edge Delay Count Register | 0300 0022h | 0301 0022h | 0302 0022h |
| 24h | EPWM_TZSEL | Trip-zone Select Register | 0300 0024h | 0301 0024h | 0302 0024h |
| 28h | EPWM_TZCTL | Trip-zone Control Register | 0300 0028h | 0301 0028h | 0302 0028h |
| 2Ah | EPWM_TZEINT | Trip-zone Enable Interrupt Register | 0300 002Ah | 0301 002Ah | 0302 002Ah |
| 2Ch | EPWM_TZFLG | Trip-zone Flag Register | 0300 002Ch | 0301 002Ch | 0302 002Ch |
| 2Eh | EPWM_TZCLR | Trip-zone Clear Register | 0300 002Eh | 0301 002Eh | 0302 002Eh |
| 30h | EPWM_TZFRC | Trip-zone Force Register | 0300 0030h | 0301 0030h | 0302 0030h |
| 32h | EPWM_ETSEL | Event Trigger Selection Register | 0300 0032h | 0301 0032h | 0302 0032h |
| 34h | EPWM_ETPS | Event Trigger Pre-Scale Register | 0300 0034h | 0301 0034h | 0302 0034h |
| 36h | EPWM_ETFLG | Event Trigger Flag Register | 0300 0036h | 0301 0036h | 0302 0036h |

Table 2-2. EPWM Registers (continued)

| Offset | Acronym | Register Name | EHRPWM0_ EPWM Physical Address | EHRPWM1_ EPWM Physical Address | EHRPWM2_ EPWM Physical Address |
|--------|----------------------------|------------------------------|---|---|---|
| 38h | EPWM_ETCLR | Event Trigger Clear Register | 0300 0038h | 0301 0038h | 0302 0038h |
| 3Ah | EPWM_ETFRC | Event Trigger Force Register | 0300 003Ah | 0301 003Ah | 0302 003Ah |
| 3Ch | EPWM_PCCTL | PWM Chopper Control Register | 0300 003Ch | 0301 003Ch | 0302 003Ch |
| 5Ch | EPWM_PID | Revision Register | 0300 005Ch | 0301 005Ch | 0302 005Ch |

Table 2-3. EPWM Registers

| Offset | Acronym | Register Name | EHRPWM3_ EPWM Physical Address | EHRPWM4_ EPWM Physical Address | EHRPWM5_ EPWM Physical Address |
|--------|-------------------------------|---|---|---|---|
| 0h | EPWM_TBCTL | Time-Base Control Register | 0303 0000h | 0304 0000h | 0305 0000h |
| 2h | EPWM_TBSTS | Time-Base Status Register | 0303 0002h | 0304 0002h | 0305 0002h |
| 4h | HRPWM_TBPHSHR | Time-Base Phase High-Resolution PWM Register | 0303 0004h | 0304 0004h | 0305 0004h |
| 6h | EPWM_TBPHS | Time-Base Counter Phase Register | 0303 0006h | 0304 0006h | 0305 0006h |
| 8h | EPWM_TBCNT | Time-Base Counter Register | 0303 0008h | 0304 0008h | 0305 0008h |
| Ah | EPWM_TBPRD | Time-Base Period Register | 0303 000Ah | 0304 000Ah | 0305 000Ah |
| Eh | EPWM_CMPCTL | Counter-Compare Control Register | 0303 000Eh | 0304 000Eh | 0305 000Eh |
| 10h | HRPWM_CMPAHR | Counter-Compare A High-Resolution Register | 0303 0010h | 0304 0010h | 0305 0010h |
| 12h | EPWM_CMPA | Counter-Compare A Register | 0303 0012h | 0304 0012h | 0305 0012h |
| 14h | EPWM_CMPB | Counter-Compare B Register | 0303 0014h | 0304 0014h | 0305 0014h |
| 16h | EPWM_AQCTLA | Action Qualifier Control Register for Output A | 0303 0016h | 0304 0016h | 0305 0016h |
| 18h | EPWM_AQCTLB | Action Qualifier Control Register for Output B | 0303 0018h | 0304 0018h | 0305 0018h |
| 1Ah | EPWM_AQSFRC | Action Qualifier Software Force Register | 0303 001Ah | 0304 001Ah | 0305 001Ah |
| 1Ch | EPWM_AQCSFRC | Action Qualifier Continuous Software Force Register | 0303 001Ch | 0304 001Ch | 0305 001Ch |
| 1Eh | EPWM_DBCTL | Dead Band Generator Control Register | 0303 001Eh | 0304 001Eh | 0305 001Eh |
| 20h | EPWM_DBRED | Dead Band Generator Rising Edge Delay Count Register | 0303 0020h | 0304 0020h | 0305 0020h |
| 22h | EPWM_DBFED | Dead Band Generator Falling Edge Delay Count Register | 0303 0022h | 0304 0022h | 0305 0022h |
| 24h | EPWM_TZSEL | Trip-zone Select Register | 0303 0024h | 0304 0024h | 0305 0024h |
| 28h | EPWM_TZCTL | Trip-zone Control Register | 0303 0028h | 0304 0028h | 0305 0028h |
| 2Ah | EPWM_TZEINT | Trip-zone Enable Interrupt Register | 0303 002Ah | 0304 002Ah | 0305 002Ah |
| 2Ch | EPWM_TZFLG | Trip-zone Flag Register | 0303 002Ch | 0304 002Ch | 0305 002Ch |
| 2Eh | EPWM_TZCLR | Trip-zone Clear Register | 0303 002Eh | 0304 002Eh | 0305 002Eh |
| 30h | EPWM_TZFRC | Trip-zone Force Register | 0303 0030h | 0304 0030h | 0305 0030h |
| 32h | EPWM_ETSEL | Event Trigger Selection Register | 0303 0032h | 0304 0032h | 0305 0032h |
| 34h | EPWM_ETPS | Event Trigger Pre-Scale Register | 0303 0034h | 0304 0034h | 0305 0034h |
| 36h | EPWM_ETFLG | Event Trigger Flag Register | 0303 0036h | 0304 0036h | 0305 0036h |
| 38h | EPWM_ETCLR | Event Trigger Clear Register | 0303 0038h | 0304 0038h | 0305 0038h |
| 3Ah | EPWM_ETFRC | Event Trigger Force Register | 0303 003Ah | 0304 003Ah | 0305 003Ah |
| 3Ch | EPWM_PCCTL | PWM Chopper Control Register | 0303 003Ch | 0304 003Ch | 0305 003Ch |
| 5Ch | EPWM_PID | Revision Register | 0303 005Ch | 0304 005Ch | 0305 005Ch |

Table 2-4. EPWM Registers

| Offset | Acronym | Register Name | EHRPWM0_ EHRPWM Physical Address | EHRPWM1_ EHRPWM Physical Address | EHRPWM2_ EHRPWM Physical Address |
|--------|-----------------------------|----------------------------------|---|---|---|
| 40h | HRPWM_HRCTL | High-Resolution Control Register | 0300 8040h | 0301 8040h | 0302 8040h |

Table 2-5. EPWM Registers

| Offset | Acronym | Register Name | EHRPWM3_ EHRPWM Physical Address | EHRPWM4_ EHRPWM Physical Address | EHRPWM5_ EHRPWM Physical Address |
|--------|-----------------------------|----------------------------------|---|---|---|
| 40h | HRPWM_HRCTL | High-Resolution Control Register | 0303 8040h | 0304 8040h | 0305 8040h |

2.1 EPWM_TBCTL Register (Offset = 0h) [reset = 83h]

EPWM_TBCTL is shown in [Figure 2-1](#) and described in [Table 2-7](#).

Return to [Summary Table](#).

Table 2-6. EPWM_TBCTL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0000h |
| EHRPWM1_EPWM | 0301 0000h |
| EHRPWM2_EPWM | 0302 0000h |
| EHRPWM3_EPWM | 0303 0000h |
| EHRPWM4_EPWM | 0304 0000h |
| EHRPWM5_EPWM | 0305 0000h |

Figure 2-1. EPWM_TBCTL Register

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----------|---------|----------|--------|--------|-----------|---------|---|
| FREE_SOFT | | PHSDIR | CLKDIV | | HSPCLKDIV | | |
| R/W-0h | | R/W-0h | R/W-0h | | R/W-1h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HSPCLKDIV | SWFSYNC | SYNCOSEL | | PRDLD | PHSEN | CTRMODE | |
| R/W-1h | R/W-0h | R/W-0h | | R/W-0h | R/W-0h | R/W-3h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-7. EPWM_TBCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| 15-14 | FREE_SOFT | R/W | 0h | <p>Emulation Mode Bits</p> <p>These bits select the behavior of the EPWM time-base counter during emulation events.</p> <p>0h: Stop after the next time-base counter increment or decrement</p> <p>1h: Stop when counter completes a whole cycle</p> <p>(a) Up-count mode: stop when the time-base counter = period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD).</p> <p>(b) Down-count mode: stop when the time-base counter = 0000 (EPWM_TBCNT[15-0] TBCNT = 0000h)</p> <p>(c) Up-down-count mode: stop when the time-base counter = 0000 (EPWM_TBCNT[15-0] TBCNT = 0000h)</p> <p>2h: Free run</p> <p>3h: Free run</p> |
| 13 | PHSDIR | R/W | 0h | <p>Phase Direction Bit</p> <p>This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter (EPWM_TBCNT) will count after a synchronization event occurs and a new phase value is loaded from the phase (EPWM_TBPHS) register. This is irrespective of the direction of the counter before the synchronization event. In the up-count and down-count modes this bit is ignored.</p> <p>0h: Count down after the synchronization event</p> <p>1h: Count up after the synchronization event</p> |

Table 2-7. EPWM_TBCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 12-10 | CLKDIV | R/W | 0h | Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value. $TBCLK = SYSCLKOUT / (HSPCLKDIV \times CLKDIV)$ 0h: /1 (default on reset) 1h: /2 2h: /4 3h: /8 4h: /16 5h: /32 6h: /64 7h: /128 |
| 9-7 | HSPCLKDIV | R/W | 1h | High-Speed Time-base Clock Prescale Bits These bits determine part of the time-base clock prescale value. $TBCLK = SYSCLKOUT / (HSPCLKDIV \times CLKDIV)$. 0h: /1 1h: /2 (default on reset) 2h: /4 3h: /6 4h: /8 5h: /10 6h: /12 7h: /14 |
| 6 | SWFSYNC | R/W | 0h | Software Forced Synchronization Pulse 0h: Writing a 0h has no effect and reads always return a 0h. 1h: Writing a 1h forces a one-time synchronization pulse to be generated. This event is ORed with the EPWMxSYNCl input of the EPWM module. SWFSYNC is valid (operates) only when EPWMxSYNCl is selected by SYNCOSSEL = 0h. |
| 5-4 | SYNCOSSEL | R/W | 0h | Synchronization Output Select These bits select the source of the EPWMxSYNCO signal. 0h: EPWMxSYNCO 1h: TBCNT = 0: Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 2h: TBCNT = CMPB: Time-base counter equal to counter-compare B (EPWM_TBCNT[15-0] TBCNT = EPWM_CMPB[15-0] CMPB) 3h: Disable EPWMxSYNCO signal |
| 3 | PRDL | R/W | 0h | Active Period Register Load From Shadow Register Select 0h: The period register (EPWM_TBPRD) is loaded from its shadow register when the time-base counter, EPWM_TBCNT[15-0] TBCNT, is equal to zero. A write or read to the EPWM_TBPRD register accesses the shadow register. 1h: Load the EPWM_TBPRD register immediately without using a shadow register. A write or read to the EPWM_TBPRD register directly accesses the active register. |
| 2 | PHSEN | R/W | 0h | Counter Register Load From Phase Register Enable 0h: Do not load the time-base counter (EPWM_TBCNT) from the time-base phase register (EPWM_TBPHS) 1h: Load the time-base counter with the phase register when an EPWMxSYNCl input signal occurs or when a software synchronization is forced by the SWFSYNC bit. |

Table 2-7. EPWM_TBCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 1-0 | CTRMODE | R/W | 3h | <p>Counter Mode</p> <p>The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows:</p> <p>0h: Up-count mode 1h: Down-count mode 2h: Up-down-count mode 3h: Stop-freeze counter operation (default on reset)</p> |

2.2 EPWM_TBSTS Register (Offset = 2h) [reset = 0h]

EPWM_TBSTS is shown in [Figure 2-2](#) and described in [Table 2-9](#).

Return to [Summary Table](#).

Table 2-8. EPWM_TBSTS Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0002h |
| EHRPWM1_EPWM | 0301 0002h |
| EHRPWM2_EPWM | 0302 0002h |
| EHRPWM3_EPWM | 0303 0002h |
| EHRPWM4_EPWM | 0304 0002h |
| EHRPWM5_EPWM | 0305 0002h |

Figure 2-2. EPWM_TBSTS Register

| | | | | | | | |
|----------|----|----|----|----|----------|----------|--------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | CTRMAX | SYNCl | CTRDIR |
| R-0h | | | | | R/W1C-0h | R/W1C-0h | R-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-9. EPWM_TBSTS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 15-3 | RESERVED | R | 0h | Reserved |
| 2 | CTRMAX | R/W1C | 0h | Time-Base Counter Max Latched Status Bit 0h = Reading a 0h indicates the time-base counter never reached its maximum value. Writing a 0h will have no effect. 1h = Reading a 1h on this bit indicates that the time-base counter reached the max value - 0xFFFF. Writing a 1h to this bit will clear the latched event. |
| 1 | SYNCl | R/W1C | 0h | Input Synchronization Latched Status Bit 0h = Writing a 0h will have no effect. Reading a 0h indicates no external synchronization event has occurred. 1h = Reading a 1h on this bit indicates that an external synchronization event has occurred (EPWMxSYNCl). Writing a 1h to this bit will clear the latched event. |
| 0 | CTRDIR | R | 0h | Time-Base Counter Direction Status Bit At reset, the counter is frozen, therefore, this bit has no meaning. To make this bit meaningful, you must first set the appropriate mode via the EPWM_TBCTL[1-0] CTRMODE bit field. 0h = Time-Base Counter is currently counting down 1h = Time-Base Counter is currently counting up |

2.3 HRPWM_TBPHSHR Register (Offset = 4h) [reset = 0h]

EPWM_TBPHSHR is shown in [Figure 2-3](#) and described in [Table 2-11](#).

Return to [Summary Table](#).

Table 2-10. HRPWM_TBPHSHR Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0004h |
| EHRPWM1_EPWM | 0301 0004h |
| EHRPWM2_EPWM | 0302 0004h |
| EHRPWM3_EPWM | 0303 0004h |
| EHRPWM4_EPWM | 0304 0004h |
| EHRPWM5_EPWM | 0305 0004h |

Figure 2-3. HRPWM_TBPHSHR Register

| | | | | | | | |
|----------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBPHSH | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-11. HRPWM_TBPHSHR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--------------------------------------|
| 15-8 | TBPHSH | R/W | 0h | Time-base phase high-resolution bits |
| 7-0 | RESERVED | R | 0h | Reserved |

2.4 EPWM_TBPHS Register (Offset = 6h) [reset = 0h]

EPWM_TBPHS is shown in [Figure 2-4](#) and described in [Table 2-13](#).

Return to [Summary Table](#).

This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension, otherwise, this location is reserved.

Table 2-12. EPWM_TBPHS Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0006h |
| EHRPWM1_EPWM | 0301 0006h |
| EHRPWM2_EPWM | 0302 0006h |
| EHRPWM3_EPWM | 0303 0006h |
| EHRPWM4_EPWM | 0304 0006h |
| EHRPWM5_EPWM | 0305 0006h |

Figure 2-4. EPWM_TBPHS Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBPHS | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-13. EPWM_TBPHS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 15-0 | TBPHS | R/W | 0h | <p>These bits set time-base counter phase of the selected ePWM relative to the time-base that is supplying the synchronization input signal:</p> <p>[a] If EPWM_TBCTL[PHSEN] = 0h, then the synchronization event is ignored and the time-base counter is not loaded with the phase</p> <p>[b] If EPWM_TBCTL[PHSEN] = 1h, then the time-base counter (EPWM_TBCNT) will be loaded with the phase (EPWM_TBPHS) when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal (EPWMxSYNCl) or by a software forced synchronization</p> <p>These bits set time-base counter phase of the selected EPWM relative to the time-base that is supplying the synchronization input signal.</p> <p>(a) If EPWM_TBCTL[2] PHSEN = 0h, then the synchronization event is ignored and the time-base counter is not loaded with the phase.</p> <p>(b) If EPWM_TBCTL[2] PHSEN = 1h, then the time-base counter (TBCNT) will be loaded with the phase (TBPHS) when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal (EPWMxSYNCl) or by a software forced synchronization.</p> |

2.5 EPWM_TBCNT Register (Offset = 8h) [reset = 0h]

EPWM_TBCNT is shown in [Figure 2-5](#) and described in [Table 2-15](#).

Return to [Summary Table](#).

Table 2-14. EPWM_TBCNT Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0008h |
| EHRPWM1_EPWM | 0301 0008h |
| EHRPWM2_EPWM | 0302 0008h |
| EHRPWM3_EPWM | 0303 0008h |
| EHRPWM4_EPWM | 0304 0008h |
| EHRPWM5_EPWM | 0305 0008h |

Figure 2-5. EPWM_TBCNT Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBCNT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-15. EPWM_TBCNT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 15-0 | TBCNT | R/W | 0h | Reading these bits gives the current time-base counter value. Writing to these bits sets the current time-base counter value. The update happens as soon as the write occurs. The write is NOT synchronized to the time-base clock (TBCLK) and the register is not shadowed. |

2.6 EPWM_TBPRD Register (Offset = Ah) [reset = 0h]

EPWM_TBPRD is shown in [Figure 2-6](#) and described in [Table 2-17](#).

Return to [Summary Table](#).

Table 2-16. EPWM_TBPRD Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 000Ah |
| EHRPWM1_EPWM | 0301 000Ah |
| EHRPWM2_EPWM | 0302 000Ah |
| EHRPWM3_EPWM | 0303 000Ah |
| EHRPWM4_EPWM | 0304 000Ah |
| EHRPWM5_EPWM | 0305 000Ah |

Figure 2-6. EPWM_TBPRD Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBPRD | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-17. EPWM_TBPRD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 15-0 | TBPRD | R/W | 0h | <p>These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the EPWM_TBCTL[3] PRDLD bit. By default this register is shadowed.</p> <p>(a) If EPWM_TBCTL[3] PRDLD = 0h, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals zero.</p> <p>(b) If EPWM_TBCTL[3] PRDLD = 1h, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.</p> <p>(c) The active and shadow registers share the same memory map address.</p> |

2.7 EPWM_CMPCTL Register (Offset = Eh) [reset = 0h]

EPWM_CMPCTL is shown in [Figure 2-7](#) and described in [Table 2-19](#).

Return to [Summary Table](#).

Table 2-18. EPWM_CMPCTL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 000Eh |
| EHRPWM1_EPWM | 0301 000Eh |
| EHRPWM2_EPWM | 0302 000Eh |
| EHRPWM3_EPWM | 0303 000Eh |
| EHRPWM4_EPWM | 0304 000Eh |
| EHRPWM5_EPWM | 0305 000Eh |

Figure 2-7. EPWM_CMPCTL Register

| | | | | | | | |
|----------|-----------|----------|-----------|-----------|----|-----------|-----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | SHDWBFULL | SHDWAFULL |
| R-0h | | | | | | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | SHDWBMODE | RESERVED | SHDWAMODE | LOADBMODE | | LOADAMODE | |
| R-0h | R/W-0h | R-0h | R/W-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-19. EPWM_CMPCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| 15-10 | RESERVED | R | 0h | Reserved |
| 9 | SHDWBFULL | R | 0h | Counter-compare B (EPWM_CMPB) Shadow Register Full Status Flag This bit self clears once a load-strobe occurs. 0h = CMPB shadow FIFO not full yet 1h = Indicates the CMPB shadow FIFO is full. A CPU write will overwrite current shadow value. |
| 8 | SHDWAFULL | R | 0h | Counter-compare A (EPWM_CMPA) Shadow Register Full Status Flag. The flag bit is set when a 32-bit write to EPWM_CMPA:HRPWM_CMPAHR register or a 16-bit write to the EPWM_CMPA register is made. A 16-bit write to the HRPWM_CMPAHR register will not affect the flag. This bit self clears once a load-strobe occurs. 0h = CMPA shadow FIFO not full yet 1h = Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value |
| 7 | RESERVED | R | 0h | Reserved |
| 6 | SHDWBMODE | R/W | 0h | Counter-compare B (EPWM_CMPB) Register Operating Mode 0h = Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h = Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action. |
| 5 | RESERVED | R | 0h | Reserved |

Table 2-19. EPWM_CMPCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 4 | SHDWAMODE | R/W | 0h | Counter-compare A (EPWM_CMPA) Register Operating Mode 0h = Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register. 1h = Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action. |
| 3-2 | LOADBMODE | R/W | 0h | Active Counter-Compare B (EPWM_CMPB) Load From Shadow Select Mode This bit has no effect in immediate mode (EPWM_CMPCTL[6] SHDWBMODE = 1h). 0h = Load on EPWM_TBCNT[15-0] TBCNT = 0h: Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT= 0000h) 1h = Load on EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD) 2h = Load on either EPWM_TBCNT[15-0] TBCNT = 0 or EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD 3h = Freeze (no loads possible) |
| 1-0 | LOADAMODE | R/W | 0h | Active Counter-Compare A (EPWM_CMPA) Load From Shadow Select Mode This bit has no effect in immediate mode (EPWM_CMPCTL[4] SHDWAMODE = 1h). 0h = Load on TBCNT = 0h: Time-base counter equal to zero (EPWM_TBCNT[15-0] TBCNT = 0000h) 1h = Load on TBCNT = TBPRD: Time-base counter equal to period (EPWM_TBCNT[15-0] TBCNT= EPWM_TBPRD[15-0] TBPRD) 2h = Load on either EPWM_TBCNT[15-0] TBCNT = 0h or EPWM_TBCNT[15-0] TBCNT = EPWM_TBPRD[15-0] TBPRD 3h = Freeze (no loads possible) |

2.8 HRPWM_CMPAHR Register (Offset = 10h) [reset = 0h]

EPWM_CMPAHR is shown in [Figure 2-8](#) and described in [Table 2-21](#).

Return to [Summary Table](#).

This register is only available on ePWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, this location is reserved.

Table 2-20. HRPWM_CMPAHR Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0010h |
| EHRPWM1_EPWM | 0301 0010h |
| EHRPWM2_EPWM | 0302 0010h |
| EHRPWM3_EPWM | 0303 0010h |
| EHRPWM4_EPWM | 0304 0010h |
| EHRPWM5_EPWM | 0305 0010h |

Figure 2-8. HRPWM_CMPAHR Register

| | | | | | | | |
|----------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPAHR | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-21. HRPWM_CMPAHR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-8 | CMPAHR | R/W | 0h | Compare A High-Resolution register bits for MEP step control. A minimum value of 1h is needed to enable HRPWM capabilities. Valid MEP range of operation: 1h to 255h. |
| 7-0 | RESERVED | R | 0h | Reserved |

2.9 EPWM_CMPA Register (Offset = 12h) [reset = 0h]

EPWM_CMPA is shown in [Figure 2-9](#) and described in [Table 2-23](#).

Return to [Summary Table](#).

Table 2-22. EPWM_CMPA Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0012h |
| EHRPWM1_EPWM | 0301 0012h |
| EHRPWM2_EPWM | 0302 0012h |
| EHRPWM3_EPWM | 0303 0012h |
| EHRPWM4_EPWM | 0304 0012h |
| EHRPWM5_EPWM | 0305 0012h |

Figure 2-9. EPWM_CMPA Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMPA | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-23. EPWM_CMPA Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 15-0 | CMPA | R/W | 0h | <p>The value in the active EPWM_CMPA register is continuously compared to the time-base counter (register EPWM_TBCNT). When the values are equal, the counter-compare module generates a "Time-Base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the EPWM_AQCTLA and EPWM_AQCTLB registers. The actions that can be defined in the EPWM_AQCTLA and EPWM_AQCTLB registers include the following.</p> <p>(a) Do nothing the event is ignored.</p> <p>(b) Clear: Pull the EPWMxA and/or EPWMxB signal low.</p> <p>(c) Set: Pull the EPWMxA and/or EPWMxB signal high.</p> <p>(d) Toggle the EPWMxA and/or EPWMxB signal.</p> <p>Shadowing of this register is enabled and disabled by the EPWM_CMPCTL[4] SHDWAMODE bit. By default this register is shadowed.</p> <p>(a) If EPWM_CMPCTL[4] SHDWAMODE = 0h, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the EPWM_CMPCTL[1-0] LOADAMODE bit field determines which event will load the active register from the shadow register.</p> <p>(b) Before a write, the EPWM_CMPCTL[8] SHDWAFULL bit can be read to determine if the shadow register is currently full.</p> <p>(c) If EPWM_CMPCTL[4] SHDWAMODE = 1h, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.</p> <p>(d) In either mode, the active and shadow registers share the same memory map address.</p> |

2.10 EPWM_CMPB Register (Offset = 14h) [reset = 0h]

EPWM_CMPB is shown in [Figure 2-10](#) and described in [Table 2-25](#).

Return to [Summary Table](#).

Table 2-24. EPWM_CMPB Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0014h |
| EHRPWM1_EPWM | 0301 0014h |
| EHRPWM2_EPWM | 0302 0014h |
| EHRPWM3_EPWM | 0303 0014h |
| EHRPWM4_EPWM | 0304 0014h |
| EHRPWM5_EPWM | 0305 0014h |

Figure 2-10. EPWM_CMPB Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMPB | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-25. EPWM_CMPB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 15-0 | CMPB | R/W | 0h | <p>The value in the active EPWM_CMPB register is continuously compared to the time-base counter (register EPWM_TBCNT). When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the EPWM_AQCTLA and EPWM_AQCTLB registers. The actions that can be defined in the EPWM_AQCTLA and EPWM_AQCTLB registers include the following.</p> <p>(a) Do nothing, the event is ignored.</p> <p>(b) Clear: Pull the EPWMxA and/or EPWMxB signal low.</p> <p>(c) Set: Pull the EPWMxA and/or EPWMxB signal high.</p> <p>(d) Toggle the EPWMxA and/or EPWMxB signal.</p> <p>Shadowing of this register is enabled and disabled by the EPWM_CMPCTL[6] SHDWBMODE bit. By default this register is shadowed.</p> <p>(a) If EPWM_CMPCTL[6] SHDWBMODE = 0h, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the EPWM_CMPCTL[3-2] LOADBMODE bit field determines which event will load the active register from the shadow register:</p> <p>(b) Before a write, the EPWM_CMPCTL[9] SHDWBFULL bit can be read to determine if the shadow register is currently full.</p> <p>(c) If EPWM_CMPCTL[6] SHDWBMODE = 1h, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.</p> <p>(d) In either mode, the active and shadow registers share the same memory map address.</p> |

2.11 EPWM_AQCTLA Register (Offset = 16h) [reset = 0h]

EPWM_AQCTLA is shown in [Figure 2-11](#) and described in [Table 2-27](#).

Return to [Summary Table](#).

Table 2-26. EPWM_AQCTLA Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0016h |
| EHRPWM1_EPWM | 0301 0016h |
| EHRPWM2_EPWM | 0302 0016h |
| EHRPWM3_EPWM | 0303 0016h |
| EHRPWM4_EPWM | 0304 0016h |
| EHRPWM5_EPWM | 0305 0016h |

Figure 2-11. EPWM_AQCTLA Register

| | | | | | | | |
|----------|----|--------|----|--------|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | CBD | | CBU | |
| R-0h | | | | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAD | | CAU | | PRD | | ZRO | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-27. EPWM_AQCTLA Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 15-12 | RESERVED | R | 0h | Reserved |
| 11-10 | CBD | R/W | 0h | Action when the Time-Base counter equals the active EPWM_CMPB register and the counter is decrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxA output low 2h = Set: force EPWMxA output high 3h = Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low |
| 9-8 | CBU | R/W | 0h | Action when the counter equals the active EPWM_CMPB register and the counter is incrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxA output low 2h = Set: force EPWMxA output high 3h = Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low |
| 7-6 | CAD | R/W | 0h | Action when the counter equals the active EPWM_CMPA register and the counter is decrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxA output low 2h = Set: force EPWMxA output high 3h = Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low |

Table 2-27. EPWM_AQCTLA Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 5-4 | CAU | R/W | 0h | Action when the counter equals the active EPWM_CMPA register and the counter is incrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxA output low 2h = Set: force EPWMxA output high 3h = Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low |
| 3-2 | PRD | R/W | 0h | Action when the counter equals the period. Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxA output low 2h = Set: force EPWMxA output high 3h = Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low |
| 1-0 | ZRO | R/W | 0h | Action when counter equals zero. Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxA output low 2h = Set: force EPWMxA output high 3h = Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low |

2.12 EPWM_AQCTLB Register (Offset = 18h) [reset = 0h]

EPWM_AQCTLB is shown in [Figure 2-12](#) and described in [Table 2-29](#).

Return to [Summary Table](#).

Table 2-28. EPWM_AQCTLB Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0018h |
| EHRPWM1_EPWM | 0301 0018h |
| EHRPWM2_EPWM | 0302 0018h |
| EHRPWM3_EPWM | 0303 0018h |
| EHRPWM4_EPWM | 0304 0018h |
| EHRPWM5_EPWM | 0305 0018h |

Figure 2-12. EPWM_AQCTLB Register

| | | | | | | | |
|----------|----|--------|----|--------|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | CBD | | CBU | |
| R-0h | | | | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAD | | CAU | | PRD | | ZRO | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-29. EPWM_AQCTLB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 15-12 | RESERVED | R | 0h | Reserved |
| 11-10 | CBD | R/W | 0h | Action when the counter equals the active EPWM_CMPB register and the counter is decrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxB output low 2h = Set: force EPWMxB output high 3h = Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low |
| 9-8 | CBU | R/W | 0h | Action when the counter equals the active EPWM_CMPB register and the counter is incrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxB output low 2h = Set: force EPWMxB output high 3h = Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low |
| 7-6 | CAD | R/W | 0h | Action when the counter equals the active EPWM_CMPA register and the counter is decrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxB output low 2h = Set: force EPWMxB output high 3h = Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low |

Table 2-29. EPWM_AQCTLB Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 5-4 | CAU | R/W | 0h | Action when the counter equals the active EPWM_CMPA register and the counter is incrementing. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxB output low 2h = Set: force EPWMxB output high 3h = Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low |
| 3-2 | PRD | R/W | 0h | Action when the counter equals the period. Note: By definition, in count up-down mode when the counter equals period the direction is defined as 0 or counting down. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxB output low 2h = Set: force EPWMxB output high 3h = Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low |
| 1-0 | ZRO | R/W | 0h | Action when counter equals zero. Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up. 0h = Do nothing (action disabled) 1h = Clear: force EPWMxB output low 2h = Set: force EPWMxB output high 3h = Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low |

2.13 EPWM_AQSFRC Register (Offset = 1Ah) [reset = 0h]

EPWM_AQSFRC is shown in [Figure 2-13](#) and described in [Table 2-31](#).

Return to [Summary Table](#).

Table 2-30. EPWM_AQSFRC Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 001Ah |
| EHRPWM1_EPWM | 0301 001Ah |
| EHRPWM2_EPWM | 0302 001Ah |
| EHRPWM3_EPWM | 0303 001Ah |
| EHRPWM4_EPWM | 0304 001Ah |
| EHRPWM5_EPWM | 0305 001Ah |

Figure 2-13. EPWM_AQSFRC Register

| | | | | | | | |
|----------|----------|--------|----------|--------|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RLDCSF | OTSFB | ACTSFB | OTSFA | ACTSFA | | | |
| R/W-0h | R/W1C-0h | R/W-0h | R/W1C-0h | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 2-31. EPWM_AQSFRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 15-8 | RESERVED | R | 0h | Reserved |
| 7-6 | RLDCSF | R/W | 0h | EPWM_AQCSFRC Active Register Reload From Shadow Options |
| 5 | OTSFB | R/W1C | 0h | One-Time Software Forced Event on Output B 0h = Writing a 0h (zero) has no effect. Always reads back a 0h. This bit is auto cleared once a write to this register is complete, that is, a forced event is initiated. This is a one-shot forced event. It can be overridden by another subsequent event on output B. 1h = Initiates a single s/w forced event |
| 4-3 | ACTSFB | R/W | 0h | Action when One-Time Software Force B Is Invoked 0h = Does nothing (action disabled) 1h = Clear (low) 2h = Set (high) 3h = Toggle (Low -> High, High -> Low). Note: This action is not qualified by counter direction (CNT_dir) |
| 2 | OTSFA | R/W1C | 0h | One-Time Software Forced Event on Output A 0h = Writing a 0 (zero) has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete (that is, a forced event is initiated). 1h = Initiates a single software forced event. |
| 1-0 | ACTSFA | R/W | 0h | Action When One-Time Software Force A Is Invoked 0h = Does nothing (action disabled). 1h = Clear (low). 2h = Set (high). 3h = Toggle (Low -> High, High -> Low). Note: This action is not qualified by counter direction (CNT_dir) |

2.14 EPWM_AQCSFRC Register (Offset = 1Ch) [reset = 0h]

EPWM_AQCSFRC is shown in [Figure 2-14](#) and described in [Table 2-33](#).

Return to [Summary Table](#).

Table 2-32. EPWM_AQCSFRC Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 001Ch |
| EHRPWM1_EPWM | 0301 001Ch |
| EHRPWM2_EPWM | 0302 001Ch |
| EHRPWM3_EPWM | 0303 001Ch |
| EHRPWM4_EPWM | 0304 001Ch |
| EHRPWM5_EPWM | 0305 001Ch |

Figure 2-14. EPWM_AQCSFRC Register

| | | | | | | | |
|----------|----|----|----|--------|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | CSFB | | CSFA | |
| R-0h | | | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-33. EPWM_AQCSFRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 15-4 | RESERVED | R | 0h | Reserved |
| 3-2 | CSFB | R/W | 0h | Continuous Software Force on Output B In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. To configure shadow mode, use the EPWM_AQSFRC[7-6] RLDCSF bit field. 0h = Forcing disabled, that is, has no effect 1h = Forces a continuous low on output B 2h = Forces a continuous high on output B 3h = Software forcing is disabled and has no effect |
| 1-0 | CSFA | R/W | 0h | Continuous Software Force on Output A In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. 0h = Forcing disabled, that is, has no effect 1h = Forces a continuous low on output A 2h = Forces a continuous high on output A 3h = Software forcing is disabled and has no effect |

2.15 EPWM_DBCTL Register (Offset = 1Eh) [reset = 0h]

EPWM_DBCTL is shown in [Figure 2-15](#) and described in [Table 2-35](#).

Return to [Summary Table](#).

Table 2-34. EPWM_DBCTL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 001Eh |
| EHRPWM1_EPWM | 0301 001Eh |
| EHRPWM2_EPWM | 0302 001Eh |
| EHRPWM3_EPWM | 0303 001Eh |
| EHRPWM4_EPWM | 0304 001Eh |
| EHRPWM5_EPWM | 0305 001Eh |

Figure 2-15. EPWM_DBCTL Register

| | | | | | | | |
|----------|----|---------|----|--------|----|----------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | IN_MODE | | POLSEL | | OUT_MODE | |
| R-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-35. EPWM_DBCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-6 | RESERVED | R | 0h | Reserved |
| 5-4 | IN_MODE | R/W | 0h | <p>Dead Band Input Mode Control</p> <p>Bit 5 controls the S5 switch and bit 4 controls the S4 switch. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms, the default is EPWMxA In is the source for both falling and rising-edge delays. 0h = EPWMxA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.</p> <p>1h = EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.</p> <p>2h = EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.</p> <p>3h = EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.</p> |

Table 2-35. EPWM_DBCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 3-2 | POLSEL | R/W | 0h | <p>Polarity Select Control</p> <p>Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that the EPWM_DBCTL[1-0] OUT_MODE = 0b11 and EPWM_DBCTL[5-4] IN_MODE = 0b00. Other enhanced modes are also possible, but not regarded as typical usage modes.</p> <p>0h = Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted (default).</p> <p>1h = Active low complementary (ALC) mode. EPWMxA is inverted.</p> <p>2h = Active high complementary (AHC). EPWMxB is inverted.</p> <p>3h = Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.</p> |
| 1-0 | OUT_MODE | R/W | 0h | <p>Dead-band Output Mode Control</p> <p>Bit 1 controls the S1 switch and bit 0 controls the S0 switch. This allows you to selectively enable or bypass the dead-band generation for the falling-edge and rising-edge delay.</p> <p>0h = Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule. In this mode, the POLSEL and IN_MODE bits have no effect.</p> <p>1h = Disable rising-edge delay. The EPWMxA signal from the action-qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.</p> <p>2h = Disable falling-edge delay. The EPWMxB signal from the action-qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule. The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.</p> <p>3h = Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by the EPWM_DBCTL[5-4] IN_MODE bit field.</p> |

2.16 EPWM_DBRED Register (Offset = 20h) [reset = 0h]

EPWM_DBRED is shown in [Figure 2-16](#) and described in [Table 2-37](#).

Return to [Summary Table](#).

Table 2-36. EPWM_DBRED Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0020h |
| EHRPWM1_EPWM | 0301 0020h |
| EHRPWM2_EPWM | 0302 0020h |
| EHRPWM3_EPWM | 0303 0020h |
| EHRPWM4_EPWM | 0304 0020h |
| EHRPWM5_EPWM | 0305 0020h |

Figure 2-16. EPWM_DBRED Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DEL | |
| R-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-37. EPWM_DBRED Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 15-10 | RESERVED | R | 0h | Reserved |
| 9-0 | DEL | R/W | 0h | Rising Edge Delay Count. 10-bit counter. |

2.17 EPWM_DBFED Register (Offset = 22h) [reset = 0h]

EPWM_DBFED is shown in [Figure 2-17](#) and described in [Table 2-39](#).

Return to [Summary Table](#).

Table 2-38. EPWM_DBFED Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0022h |
| EHRPWM1_EPWM | 0301 0022h |
| EHRPWM2_EPWM | 0302 0022h |
| EHRPWM3_EPWM | 0303 0022h |
| EHRPWM4_EPWM | 0304 0022h |
| EHRPWM5_EPWM | 0305 0022h |

Figure 2-17. EPWM_DBFED Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DEL | |
| R-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-39. EPWM_DBFED Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 15-10 | RESERVED | R | 0h | Reserved |
| 9-0 | DEL | R/W | 0h | Falling Edge Delay Count. 10-bit counter |

2.18 EPWM_TZSEL Register (Offset = 24h) [reset = 0h]

EPWM_TZSEL is shown in [Figure 2-18](#) and described in [Table 2-41](#).

Return to [Summary Table](#).

Table 2-40. EPWM_TZSEL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0024h |
| EHRPWM1_EPWM | 0301 0024h |
| EHRPWM2_EPWM | 0302 0024h |
| EHRPWM3_EPWM | 0303 0024h |
| EHRPWM4_EPWM | 0304 0024h |
| EHRPWM5_EPWM | 0305 0024h |

Figure 2-18. EPWM_TZSEL Register

| | | | | | | | |
|--------|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OSHTN | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CBCN | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 2-41. EPWM_TZSEL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 15-14 | RESERVED | R | 0h | Reserved |
| 13 | OSHT6 | R/W | 0h | <p>Trip-zone 5 (TZ5) select</p> <p>One-Shot (OSHT) trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until you clear the condition via the EPWM_TZCLR register.</p> <p>0h: Disable TZ5 as a one-shot trip source for this EPWM module</p> <p>1h: Enable TZ5 as a one-shot trip source for this EPWM module</p> |
| 12 | OSHT5 | R/W | 0h | <p>Trip-zone 4 (TZ4) select</p> <p>One-Shot (OSHT) trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until you clear the condition via the EPWM_TZCLR register.</p> <p>0h: Disable TZ4 as a one-shot trip source for this EPWM module</p> <p>1h: Enable TZ4 as a one-shot trip source for this EPWM module</p> |

Table 2-41. EPWM_TZSEL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 11 | OSHT4 | R/W | 0h | <p>Trip-zone 3 (TZ3) select</p> <p>One-Shot (OSHT) trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until you clear the condition via the EPWM_TZCLR register.</p> <p>0h: Disable TZ3 as a one-shot trip source for this EPWM module 1h: Enable TZ3 as a one-shot trip source for this EPWM module</p> |
| 10 | OSHT3 | R/W | 0h | <p>Trip-zone 2 (TZ2) Select</p> <p>One-Shot (OSHT) trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until you clear the condition via the EPWM_TZCLR register.</p> <p>0h: Disable TZ2 as a one-shot trip source for this EPWM module 1h: Enable TZ2 as a one-shot trip source for this EPWM module</p> |
| 9 | OSHT2 | R/W | 0h | <p>Trip-zone 1 (TZ1) select</p> <p>One-Shot (OSHT) trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until you clear the condition via the EPWM_TZCLR register.</p> <p>0h: Disable TZ1 as a one-shot trip source for this EPWM module 1h: Enable TZ1 as a one-shot trip source for this EPWM module</p> |
| 8 | OSHT1 | R/W | 0h | <p>Trip-zone 0 (TZ0) select</p> <p>One-Shot (OSHT) trip-zone enable/disable. When any of the enabled pins go low, a one-shot trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. The one-shot trip condition remains latched until you clear the condition via the EPWM_TZCLR register.</p> <p>0h: Disable TZ0 as a one-shot trip source for this EPWM module 1h: Enable TZ0 as a one-shot trip source for this EPWM module</p> |
| 7-6 | RESERVED | R | 0h | Reserved |
| 5 | CBC5 | R/W | 0h | <p>Trip-zone 5 (TZ5) select</p> <p>Cycle-by-Cycle (CBC) trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.</p> <p>0h: Disable TZ5 as a CBC trip source for this EPWM module 1h: Enable TZ5 as a CBC trip source for this EPWM module</p> |

Table 2-41. EPWM_TZSEL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 4 | CBC4 | R/W | 0h | <p>Trip-zone 4 (TZ4) select</p> <p>Cycle-by-Cycle (CBC) trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.</p> <p>0h: Disable TZ4 as a CBC trip source for this EPWM module 1h: Enable TZ4 as a CBC trip source for this EPWM module</p> |
| 3 | CBC3 | R/W | 0h | <p>Trip-zone 3 (TZ3) select</p> <p>Cycle-by-Cycle (CBC) trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.</p> <p>0h: Disable TZ3 as a CBC trip source for this EPWM module 1h: Enable TZ3 as a CBC trip source for this EPWM module</p> |
| 2 | CBC2 | R/W | 0h | <p>Trip-zone 2 (TZ2) select</p> <p>Cycle-by-Cycle (CBC) trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.</p> <p>0h: Disable TZ2 as a CBC trip source for this EPWM module 1h: Enable TZ2 as a CBC trip source for this EPWM module</p> |
| 1 | CBC1 | R/W | 0h | <p>Trip-zone 1 (TZ1) select</p> <p>Cycle-by-Cycle (CBC) trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.</p> <p>0h: Disable TZ1 as a CBC trip source for this EPWM module 1h: Enable TZ1 as a CBC trip source for this EPWM module</p> |
| 0 | CBC0 | R/W | 0h | <p>Trip-zone 0 (TZ0) select</p> <p>Cycle-by-Cycle (CBC) trip-zone enable/disable. When any of the enabled pins go low, a cycle-by-cycle trip event occurs for this EPWM module. When the event occurs, the action defined in the EPWM_TZCTL register is taken on the EPWMxA and EPWMxB outputs. A cycle-by-cycle trip condition is automatically cleared when the time-base counter reaches zero.</p> <p>0h: Disable TZ0 as a CBC trip source for this EPWM module 1h: Enable TZ0 as a CBC trip source for this EPWM module</p> |

2.19 EPWM_TZCTL Register (Offset = 28h) [reset = 0h]

EPWM_TZCTL is shown in [Figure 2-19](#) and described in [Table 2-43](#).

Return to [Summary Table](#).

Table 2-42. EPWM_TZCTL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0028h |
| EHRPWM1_EPWM | 0301 0028h |
| EHRPWM2_EPWM | 0302 0028h |
| EHRPWM3_EPWM | 0303 0028h |
| EHRPWM4_EPWM | 0304 0028h |
| EHRPWM5_EPWM | 0305 0028h |

Figure 2-19. EPWM_TZCTL Register

| | | | | | | | |
|----------|----|----|----|--------|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TZB | | TZA | |
| R-0h | | | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-43. EPWM_TZCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-4 | RESERVED | R | 0h | Reserved |
| 3-2 | TZB | R/W | 0h | When a trip event occurs the following action is taken on output EPWMxB. Which trip-zone pins can cause an event is defined in the EPWM_TZSEL register. 0h = High impedance (EPWMxB = High-impedance state) 1h = Force EPWMxB to a high state 2h = Force EPWMxB to a low state 3h = Do nothing, no action is taken on EPWMxB. |
| 1-0 | TZA | R/W | 0h | When a trip event occurs the following action is taken on output EPWMxA. Which trip-zone pins can cause an event is defined in the EPWM_TZSEL register. 0h = High impedance (EPWMxA = High-impedance state) 1h = Force EPWMxA to a high state 2h = Force EPWMxA to a low state 3h = Do nothing, no action is taken on EPWMxA. |

2.20 EPWM_TZEINT Register (Offset = 2Ah) [reset = 0h]

EPWM_TZEINT is shown in [Figure 2-20](#) and described in [Table 2-45](#).

Return to [Summary Table](#).

Table 2-44. EPWM_TZEINT Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 002Ah |
| EHRPWM1_EPWM | 0301 002Ah |
| EHRPWM2_EPWM | 0302 002Ah |
| EHRPWM3_EPWM | 0303 002Ah |
| EHRPWM4_EPWM | 0304 002Ah |
| EHRPWM5_EPWM | 0305 002Ah |

Figure 2-20. EPWM_TZEINT Register

| | | | | | | | |
|----------|----|----|----|----|--------|--------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | OST | CBC | RESERVED |
| R-0h | | | | | R/W-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-45. EPWM_TZEINT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 15-3 | RESERVED | R | 0h | Reserved |
| 2 | OST | R/W | 0h | Trip-zone One-Shot Interrupt Enable 0h = Disable one-shot interrupt generation 1h = Enable Interrupt generation a one-shot trip event will cause a EPWMxTZINT interrupt. |
| 1 | CBC | R/W | 0h | Trip-zone Cycle-by-Cycle Interrupt Enable 0h = Disable cycle-by-cycle interrupt generation 1h = Enable interrupt generation a cycle-by-cycle trip event will cause an EPWMxTZINT interrupt. |
| 0 | RESERVED | R | 0h | Reserved |

2.21 EPWM_TZFLG Register (Offset = 2Ch) [reset = 0h]

EPWM_TZFLG is shown in [Figure 2-21](#) and described in [Table 2-47](#).

Return to [Summary Table](#).

Table 2-46. EPWM_TZFLG Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 002Ch |
| EHRPWM1_EPWM | 0301 002Ch |
| EHRPWM2_EPWM | 0302 002Ch |
| EHRPWM3_EPWM | 0303 002Ch |
| EHRPWM4_EPWM | 0304 002Ch |
| EHRPWM5_EPWM | 0305 002Ch |

Figure 2-21. EPWM_TZFLG Register

| | | | | | | | |
|----------|----|----|----|----|------|------|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | OST | CBC | INT |
| R-0h | | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 2-47. EPWM_TZFLG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 15-3 | RESERVED | R | 0h | Reserved |
| 2 | OST | R | 0h | Latched Status Flag for A One-Shot Trip Event 0h = No one-shot trip event has occurred 1h = Indicates a trip event has occurred on a pin selected as a one-shot trip source. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register. |
| 1 | CBC | R | 0h | Latched Status Flag for Cycle-By-Cycle Trip Event 0h = No cycle-by-cycle trip event has occurred 1h = Indicates a trip event has occurred on a pin selected as a cycle-by-cycle trip source. The EPWM_TZFLG[1] CBC bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the pins is automatically cleared when the EPWM time-base counter reaches zero (EPWM_TBCNT[15-0] TBCNT = 0000h) if the trip condition is no longer present. The condition on the pins is only cleared when the TBCNT = 0000h no matter where in the cycle the CBC flag is cleared. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register. |
| 0 | INT | R | 0h | Latched Trip Interrupt Status Flag 0h = Indicates no interrupt has been generated 1h = Indicates an EPWMxTZINT interrupt was generated because of a trip condition. No further EPWMxTZINT interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by writing the appropriate value to the EPWM_TZCLR register. |

2.22 EPWM_TZCLR Register (Offset = 2Eh) [reset = 0h]

EPWM_TZCLR is shown in [Figure 2-22](#) and described in [Table 2-49](#).

Return to [Summary Table](#).

Table 2-48. EPWM_TZCLR Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 002Eh |
| EHRPWM1_EPWM | 0301 002Eh |
| EHRPWM2_EPWM | 0302 002Eh |
| EHRPWM3_EPWM | 0303 002Eh |
| EHRPWM4_EPWM | 0304 002Eh |
| EHRPWM5_EPWM | 0305 002Eh |

Figure 2-22. EPWM_TZCLR Register

| | | | | | | | |
|----------|----|----|----|----|--------|--------|--------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | OST | CBC | INT |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-49. EPWM_TZCLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 15-3 | RESERVED | R | 0h | Reserved |
| 2 | OST | R/W | 0h | Clear Flag for One-Shot Trip (OST) Latch 0h = Has no effect. Always reads back a 0h 1h = Clears this Trip (set) condition |
| 1 | CBC | R/W | 0h | Clear Flag for Cycle-By-Cycle (CBC) Trip Latch 0h = Has no effect. Always reads back a 0h 1h = Clears this Trip (set) condition |
| 0 | INT | R/W | 0h | Global Interrupt Clear Flag 0h = Has no effect. Always reads back a 0h 1h = Clears the trip-interrupt flag for this EPWM module (EPWM_TZFLG[0] INT) Note: No further EPWMxTZINT interrupts will be generated until the flag is cleared. If the EPWM_TZFLG[0] INT bit is cleared and any of the other flag bits are set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. |

2.23 EPWM_TZFRC Register (Offset = 30h) [reset = 0h]

EPWM_TZFRC is shown in [Figure 2-23](#) and described in [Table 2-51](#).

Return to [Summary Table](#).

Table 2-50. EPWM_TZFRC Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0030h |
| EHRPWM1_EPWM | 0301 0030h |
| EHRPWM2_EPWM | 0302 0030h |
| EHRPWM3_EPWM | 0303 0030h |
| EHRPWM4_EPWM | 0304 0030h |
| EHRPWM5_EPWM | 0305 0030h |

Figure 2-23. EPWM_TZFRC Register

| | | | | | | | |
|----------|----|----|----|----|--------|--------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | OST | CBC | RESERVED |
| R-0h | | | | | R/W-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-51. EPWM_TZFRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-3 | RESERVED | R | 0h | Reserved |
| 2 | OST | R/W | 0h | Force a One-Shot Trip Event via Software 0h = Writing of 0h is ignored. Always reads back a 0h. 1h = Forces a one-shot trip event and sets the EPWM_TZFLG[2] OST bit. |
| 1 | CBC | R/W | 0h | Force a Cycle-by-Cycle Trip Event via Software 0h = Writing of 0h is ignored. Always reads back a 0h. 1h = Forces a cycle-by-cycle trip event and sets the EPWM_TZFLG[1] CBC bit. |
| 0 | RESERVED | R | 0h | Reserved |

2.24 EPWM_ETSEL Register (Offset = 32h) [reset = 0h]

EPWM_ETSEL is shown in [Figure 2-24](#) and described in [Table 2-53](#).

Return to [Summary Table](#).

Table 2-52. EPWM_ETSEL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0032h |
| EHRPWM1_EPWM | 0301 0032h |
| EHRPWM2_EPWM | 0302 0032h |
| EHRPWM3_EPWM | 0303 0032h |
| EHRPWM4_EPWM | 0304 0032h |
| EHRPWM5_EPWM | 0305 0032h |

Figure 2-24. EPWM_ETSEL Register

| | | | | | | | |
|----------|----|----|----|--------|--------|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | INTEN | INTSEL | | |
| R-0h | | | | R/W-0h | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-53. EPWM_ETSEL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 15 | SOCB | R/W | 0h | Enable SOCB pulse when set to 1h. |
| 14-12 | SOCBSEL | R/W | 0h | EPWMxSOCB Selection Options 0h: Reserved 1h: Enable event time-base counter equal to zero (CNT_zero event) 2h: Enable event time-base counter equal to period (PRD_eq event) 3h: Reserved 4h: Enable event time-base counter equal to CMPA when the timer is incrementing (CMPA_eq_UC event) 5h: Enable event time-base counter equal to CMPA when the timer is decrementing (CMPA_eq_DC event) 6h: Enable event time-base counter equal to CMPB when the timer is incrementing (CMPB_eq_UC event) 7h: Enable event time-base counter equal to CMPB when the timer is decrementing (CMPB_eq_DC event) |
| 11 | SOCA | R/W | 0h | Enable SOCA pulse when set to 1h. |
| 10-8 | SOCASEL | R/W | 0h | EPWMxSOCA Selection Options 0h: Reserved 1h: Enable event time-base counter equal to zero (CNT_zero event) 2h: Enable event time-base counter equal to period (PRD_eq event) 3h: Reserved 4h: Enable event time-base counter equal to CMPA when the timer is incrementing (CMPA_eq_UC event) 5h: Enable event time-base counter equal to CMPA when the timer is decrementing (CMPA_eq_DC event) 6h: Enable event time-base counter equal to CMPB when the timer is incrementing (CMPB_eq_UC event) 7h: Enable event time-base counter equal to CMPB when the timer is decrementing (CMPB_eq_DC event) |
| 7-4 | RESERVED | R | 0h | Reserved |
| 3 | INTEN | R/W | 0h | Enable EPWM Interrupt (EPWMx_INT) Generation 0h: Disable EPWMx_INT generation 1h: Enable EPWMx_INT generation |

Table 2-53. EPWM_ETSEL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 2-0 | INTSEL | R/W | 0h | <p>EPWM Interrupt (EPWMx_INT) Selection Options</p> <p>0h: Reserved</p> <p>1h: Enable event time-base counter equal to zero. (EPWM_TBCNT = 0000h)</p> <p>2h: Enable event time-base counter equal to period (EPWM_TBCNT = EPWM_TBPRD)</p> <p>3h: Reserved</p> <p>4h: Enable event time-base counter equal to CMPA when the timer is incrementing</p> <p>5h: Enable event time-base counter equal to CMPA when the timer is decrementing</p> <p>6h: Enable event time-base counter equal to CMPB when the timer is incrementing</p> <p>7h: Enable event time-base counter equal to CMPB when the timer is decrementing</p> |

2.25 EPWM_ETPS Register (Offset = 34h) [reset = 0h]

EPWM_ETPS is shown in [Figure 2-25](#) and described in [Table 2-55](#).

Return to [Summary Table](#).

Table 2-54. EPWM_ETPS Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0034h |
| EHRPWM1_EPWM | 0301 0034h |
| EHRPWM2_EPWM | 0302 0034h |
| EHRPWM3_EPWM | 0303 0034h |
| EHRPWM4_EPWM | 0304 0034h |
| EHRPWM5_EPWM | 0305 0034h |

Figure 2-25. EPWM_ETPS Register

| | | | | | | | |
|----------|----|----|----|--------|----|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | INTCNT | | INTPRD | |
| R-0h | | | | R-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-55. EPWM_ETPS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 15-14 | SOCBCNT | R | 0h | EPWMxSOCB Counter Register These bits indicate how many selected events have occurred. 0h: No events 1h: 1 events 2h: 2 events 3h: 3 event |
| 13-12 | SOCBPRD | R/W | 0h | EPWMxSOCB Period Select These bits select how many selected event need to occur before an SOCB pulse is generated. 0h: Disable counter 1h: Generate pulse on SOCBCNT = 1 (1-st event) 2h: Generate pulse on SOCBCNT = 2 (2-nd event) 3h: Generate pulse on SOCBCNT = 3 (3-rd event) |
| 11-10 | SOCACNT | R | 0h | EPWMxSOCA Counter Register These bits indicate how many selected events have occurred. 0h: No events 1h: 1 events 2h: 2 events 3h: 3 events |
| 9-8 | SOCAPRD | R/W | 0h | EPWMxSOCA Period Select These bits select how many selected event need to occur before an SOCA pulse is generated. 0h: Disable counter 1h: Generate pulse on SOCACNT = 1 (1-st event) 2h: Generate pulse on SOCACNT = 2 (2-nd event) 3h: Generate pulse on SOCACNT = 3 (3-rd event) |
| 7-4 | RESERVED | R | 0h | Reserved |

Table 2-55. EPWM_ETPS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | INTCNT | R | 0h | <p>EPWM Interrupt Event (EPWMx_INT) Counter Register</p> <p>These bits indicate how many selected EPWM_ETSEL[2-0] INTSEL events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, EPWM_ETSEL[0] INT = 0h or the interrupt flag is set, EPWM_ETFLG[0] INT = 1h, the counter will stop counting events when it reaches the period value EPWM_ETPS[3-2] INTCNT = EPWM_ETPS[1-0] INTPRD.</p> <p>0h: No events have occurred 1h: 1 event has occurred 2h: 2 events have occurred 3h: 3 events have occurred</p> |
| 1-0 | INTPRD | R/W | 0h | <p>EPWM Interrupt (EPWMx_INT) Period Select</p> <p>These bits determine how many selected EPWM_ETSEL[2-0] INTSEL events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled (EPWM_ETSEL[0] INT = 1h). If the interrupt status flag is set from a previous interrupt (EPWM_ETFLG[0] INT = 1) then no interrupt will be generated until the flag is cleared via the EPWM_ETCLR[0] INT bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the EPWM_ETPS[3-2] INTCNT bits will automatically be cleared. Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear. Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented.</p> <p>0h: Disable the interrupt event counter. No interrupt will be generated and the EPWM ETFRC[0] INT bit is ignored. 1h: Generate an interrupt on the first event INTCNT = 0b01 (first event) 2h: Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b10 (second event) 3h: Generate interrupt on the EPWM_ETPS[3-2] INTCNT = 0b11 (third event)</p> |

2.26 EPWM_ETFLG Register (Offset = 36h) [reset = 0h]

EPWM_ETFLG is shown in [Figure 2-26](#) and described in [Table 2-57](#).

Return to [Summary Table](#).

Table 2-56. EPWM_ETFLG Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0036h |
| EHRPWM1_EPWM | 0301 0036h |
| EHRPWM2_EPWM | 0302 0036h |
| EHRPWM3_EPWM | 0303 0036h |
| EHRPWM4_EPWM | 0304 0036h |
| EHRPWM5_EPWM | 0305 0036h |

Figure 2-26. EPWM_ETFLG Register

| | | | | | | | |
|----------|----|----|----|----|----|---|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | INT |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 2-57. EPWM_ETFLG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-4 | RESERVED | R | 0h | Reserved |
| 3 | SOCB | R | 0h | Latched SOCB Flag Bit Status 0h: Indicates no event occurred 1h: Indicates that a start of conversion pulse was generated on EPWMxSOCB Note: Unlike the INT flag bit, the EPWMxSOCB output will continue to pulse even if the flag bit is set. |
| 2 | SOCA | R | 0h | Latched SOCA Flag Bit Status 0h: Indicates no event occurred 1h: Indicates that a start of conversion pulse was generated on EPWMxSOCA Note: Unlike the INT flag bit, the EPWMxSOCA output will continue to pulse even if the flag bit is set. |
| 1 | RESERVED | R | 0h | Reserved |
| 0 | INT | R | 0h | Latched EPWM Interrupt (EPWMx_INT) Status Flag 0h: Indicates no event occurred. 1h: Indicates that an EPWMx interrupt (EPWMx_INT) was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the EPWM_ETFLG[0] INT bit is still set. If an interrupt is pending, it will not be generated until after the EPWM_ETFLG[0] INT bit is cleared. |

2.27 EPWM_ETCLR Register (Offset = 38h) [reset = 0h]

EPWM_ETCLR is shown in [Figure 2-27](#) and described in [Table 2-59](#).

Return to [Summary Table](#).

Table 2-58. EPWM_ETCLR Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 0038h |
| EHRPWM1_EPWM | 0301 0038h |
| EHRPWM2_EPWM | 0302 0038h |
| EHRPWM3_EPWM | 0303 0038h |
| EHRPWM4_EPWM | 0304 0038h |
| EHRPWM5_EPWM | 0305 0038h |

Figure 2-27. EPWM_ETCLR Register

| | | | | | | | |
|----------|----|----|----|----|----|---|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | INT |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 2-59. EPWM_ETCLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 15-1 | RESERVED | R | 0h | Reserved |
| 0 | INT | R | 0h | ePWM Interrupt [EPWMx_INT] Flag Clear Bit |

2.28 EPWM_ETFRC Register (Offset = 3Ah) [reset = 0h]

EPWM_ETFRC is shown in [Figure 2-28](#) and described in [Table 2-61](#).

Return to [Summary Table](#).

Table 2-60. EPWM_ETFRC Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 003Ah |
| EHRPWM1_EPWM | 0301 003Ah |
| EHRPWM2_EPWM | 0302 003Ah |
| EHRPWM3_EPWM | 0303 003Ah |
| EHRPWM4_EPWM | 0304 003Ah |
| EHRPWM5_EPWM | 0305 003Ah |

Figure 2-28. EPWM_ETFRC Register

| | | | | | | | |
|----------|----|----|----|----|----|---|------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | INT |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 2-61. EPWM_ETFRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 15-4 | RESERVED | R | 0h | Reserved |
| 3 | SOCB | R/W | 0h | SOCB Flag Clear Bit 0h: Writing a 0h has no effect. Always reads back a 0h. 1h: Writing a 1h clears the EPWM_ETFLG[3] SOCB flag bit |
| 2 | SOCA | R/W | 0h | SOCA Flag Clear Bit 0h: Writing a 0h has no effect. Always reads back a 0h. 1h: Writing a 1h clears the EPWM_ETFLG[2] SOCA flag bit |
| 1 | RESERVED | R | 0h | Reserved |
| 0 | INT | R/W | 0h | EPWM Interrupt (EPWMx_INT) Flag Clear Bit 0h: Writing a 0 has no effect. Always reads back a 0h. 1h: Writing 1 clears the EPWM_ETFLG[0] INT flag bit and enable further interrupts pulses to be generated. |

2.29 EPWM_PCCTL Register (Offset = 3Ch) [reset = 0h]

EPWM_PCCTL is shown in [Figure 2-29](#) and described in [Table 2-63](#).

Return to [Summary Table](#).

Table 2-62. EPWM_PCCTL Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 003Ch |
| EHRPWM1_EPWM | 0301 003Ch |
| EHRPWM2_EPWM | 0302 003Ch |
| EHRPWM3_EPWM | 0303 003Ch |
| EHRPWM4_EPWM | 0304 003Ch |
| EHRPWM5_EPWM | 0305 003Ch |

Figure 2-29. EPWM_PCCTL Register

| | | | | | | | |
|----------|----|----|---------|----|----|---------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | CHPDUTY | |
| R-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHPFREQ | | | OSHTWTH | | | CHPEN | |
| R/W-0h | | | R/W-0h | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-63. EPWM_PCCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 15-11 | RESERVED | R | 0h | Reserved |
| 10-8 | CHPDUTY | R/W | 0h | Chopping Clock Duty Cycle 0h = Duty = 1/8 (12.5%) 1h = Duty = 2/8 (25.0%) 2h = Duty = 3/8 (37.5%) 3h = Duty = 4/8 (50.0%) 4h = Duty = 5/8 (62.5%) 5h = Duty = 6/8 (75.0%) 6h = Duty = 7/8 (87.5%) 7h = Reserved |
| 7-5 | CHPFREQ | R/W | 0h | Chopping Clock Frequency 0h = Divide by 1 (no prescale) 1h = Divide by 2 2h = Divide by 3 3h = Divide by 4 4h = Divide by 5 5h = Divide by 6 6h = Divide by 7 7h = Divide by 8 |
| 4-1 | OSHTWTH | R/W | 0h | One-Shot Pulse Width 0h = 1 - SYSCLKOUT/8 wide 1h = 2 - SYSCLKOUT/8 wide 2h = 3 - SYSCLKOUT/8 wide 3h = 4 - SYSCLKOUT/8 wide Fh = 16 - SYSCLKOUT/8 wide |

Table 2-63. EPWM_PCCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 0 | CHPEN | R/W | 0h | PWM-chopping Enable 0h = Disable (bypass) PWM chopping function 1h = Enable chopping function |

2.30 HRPWM_HRCTL Register (Offset = 40h) [reset = 0h]

EPWM_HRCTL is shown in [Figure 2-30](#) and described in [Table 2-65](#).

Return to [Summary Table](#).

This register is only available on EPWM instances that include the high-resolution PWM (HRPWM) extension. Otherwise, this location is reserved.

Table 2-64. HRPWM_HRCTL Instances

| Instance | Physical Address |
|----------------|------------------|
| EHRPWM0_EHRPWM | 0300 8040h |
| EHRPWM1_EHRPWM | 0301 8040h |
| EHRPWM2_EHRPWM | 0302 8040h |
| EHRPWM3_EHRPWM | 0303 8040h |
| EHRPWM4_EHRPWM | 0304 8040h |
| EHRPWM5_EHRPWM | 0305 8040h |

Figure 2-30. HRPWM_HRCTL Register

| | | | | | | | |
|----------|----|----|----|----------|-----------|---------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | PULSESEL | DELBUSSEL | DELMODE | |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 2-65. HRPWM_HRCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|--|
| 15-4 | RESERVED | R | 0h | Reserved |
| 3 | PULSESEL | R/W | 0h | Shadow Mode Bit Selects the time event that loads the CMPAHR shadow value into the active register. Note: Load mode selection is valid only if CTLMODE = 0 has been selected. The user should select this event to match the selection of the CMPA load mode EPWM_CMPCTL[LOADMODE] bits in the EPWM module as follows. 0h: Load on CTR = 0. Time-base counter equal to zero (EPWM_TBCNT = 0000h). 1h: Load on CTR = PRD. Time-base counter equal to period (EPWM_TBCNT = TEPWM_TBPRD) 2h: Load on either CTR = 0 or CTR = PRD (should not be used with HRPWM) 3h: Freeze (No loads possible should not be used with HRPWM) 0h = CTR = PRD (counter equal period) 1h = CTR = 0 (counter equals zero) |
| 2 | DELBUSSEL | R/W | 0h | Control Mode Bits Selects the register (CMP or TBPHS) that controls the MEP. 0h = Select CMPAHR(8) register controls the edge position. This is duty control mode (default on reset). 1h = Select TBPHSHR(8) register controls the edge position (this is phase control mode). |

Table 2-65. HRPWM_HRCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 1-0 | DELMODE | R/W | 0h | <p>Edge Mode Bits</p> <p>Selects the edge of the PWM that is controlled by the micro-edge position (MEP) logic.</p> <p>0h = HRPWM capability is disabled (default on reset)</p> <p>1h = MEP control of rising edge</p> <p>2h = MEP control of falling edge</p> <p>3h = MEP control of both edges</p> |

2.31 EPWM_PID Register (Offset = 5Ch) [reset = 44D10903h]

EPWM_PID is shown in [Figure 2-31](#) and described in [Table 2-67](#).

Return to [Summary Table](#).

The revision register is used by software to track features, bugs, and compatibility.

Table 2-66. EPWM_PID Instances

| Instance | Physical Address |
|--------------|------------------|
| EHRPWM0_EPWM | 0300 005Ch |
| EHRPWM1_EPWM | 0301 005Ch |
| EHRPWM2_EPWM | 0302 005Ch |
| EHRPWM3_EPWM | 0303 005Ch |
| EHRPWM4_EPWM | 0304 005Ch |
| EHRPWM5_EPWM | 0305 005Ch |

Figure 2-31. EPWM_PID Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 44D10903h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 2-67. EPWM_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-----------|--|
| 31-0 | REVISION | R | 44D10903h | TI Internal Data Identifies revision of peripheral. |

3 EQEP Registers

Table 3-2 lists the memory-mapped registers for the EQEP modules. All register offset addresses not listed in Table 3-2 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. EQEP Instances

| Instance | Base Address |
|-----------|--------------|
| EQEP0_REG | 0320 0000h |
| EQEP1_REG | 0321 0000h |
| EQEP2_REG | 0322 0000h |

Table 3-2. EQEP Registers

| Offset | Acronym | Register Name | EQEP0_RE G Physical Address | EQEP1_RE G Physical Address | EQEP2_RE G Physical Address |
|--------|------------------------------------|---|-----------------------------------|-----------------------------------|-----------------------------------|
| 0h | EQEP_QPOSCNT | QEP Position Counter Register | 0320 0000h | 0321 0000h | 0322 0000h |
| 4h | EQEP_QPOSINIT | Position Counter Initialization Register | 0320 0004h | 0321 0004h | 0322 0004h |
| 8h | EQEP_QPOSMAX | Maximum Position Count Register | 0320 0008h | 0321 0008h | 0322 0008h |
| Ch | EQEP_QPOSCMP | Position Compare Register | 0320 000Ch | 0321 000Ch | 0322 000Ch |
| 10h | EQEP_QPOSILAT | Index Position Latch Register | 0320 0010h | 0321 0010h | 0322 0010h |
| 14h | EQEP_QPOSSLAT | Strobe Position Latch Register | 0320 0014h | 0321 0014h | 0322 0014h |
| 18h | EQEP_QPOSLAT | QEP Position Counter Latch Register | 0320 0018h | 0321 0018h | 0322 0018h |
| 1Ch | EQEP_QUTMR | QEP Unit Timer Register | 0320 001Ch | 0321 001Ch | 0322 001Ch |
| 20h | EQEP_QUPRD | QEP Unit Period Register | 0320 0020h | 0321 0020h | 0322 0020h |
| 24h | EQEP_QWD_TMR_PRD | QEP Watchdog Timer and Period Register | 0320 0024h | 0321 0024h | 0322 0024h |
| 28h | EQEP_QDEC_QEP_CTL | Quadrature Decoder and QEP Control Register | 0320 0028h | 0321 0028h | 0322 0028h |
| 2Ch | EQEP_QCAP_QPOS_CTL | QEP Capture and Position Compare Control Register | 0320 002Ch | 0321 002Ch | 0322 002Ch |
| 30h | EQEP_QINT_EN_FLG | QEP Interrupt Control and Flag Register | 0320 0030h | 0321 0030h | 0322 0030h |
| 34h | EQEP_QINT_CLR_FRC | QEP Interrupt Clear and Forcing Register | 0320 0034h | 0321 0034h | 0322 0034h |
| 38h | EQEP_QEP_STS_CT | QEP Status and Capture Timer Register | 0320 0038h | 0321 0038h | 0322 0038h |
| 3Ch | EQEP_QC_PRD_TLAT | QEP Capture Period and Timer Latch Register | 0320 003Ch | 0321 003Ch | 0322 003Ch |
| 40h | EQEP_QCPRDLAT | QEP Capture Period Latch Register | 0320 0040h | 0321 0040h | 0322 0040h |
| 5Ch | EQEP_PID | Peripheral ID Register | 0320 005Ch | 0321 005Ch | 0322 005Ch |

3.1 EQEP_QPOSCNT Register (Offset = 0h) [reset = 0h]

EQEP_QPOSCNT is shown in [Figure 3-1](#) and described in [Table 3-4](#).

Return to [Summary Table](#).

QEP Position Counter register

Table 3-3. EQEP_QPOSCNT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0000h |
| EQEP1_REG | 0321 0000h |
| EQEP2_REG | 0322 0000h |

Figure 3-1. EQEP_QPOSCNT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POSCNT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-4. EQEP_QPOSCNT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|--|
| 31-0 | POSCNT | R/W | 0h | This 32-bit Position Counter register counts up/down on every QEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. |

3.2 EQEP_QPOSINIT Register (Offset = 4h) [reset = 0h]

EQEP_QPOSINIT is shown in [Figure 3-2](#) and described in [Table 3-6](#).

Return to [Summary Table](#).

Position Counter Initialization register

Table 3-5. EQEP_QPOSINIT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0004h |
| EQEP1_REG | 0321 0004h |
| EQEP2_REG | 0322 0004h |

Figure 3-2. EQEP_QPOSINIT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INITPOS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-6. EQEP_QPOSINIT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | INITPOS | R/W | 0h | This register contains the position value to be used to initialize the Position Counter based on external strobe or Index event. Position Counter can be initialized through software. |

3.3 EQEP_QPOS MAX Register (Offset = 8h) [reset = 0h]

EQEP_QPOS MAX is shown in [Figure 3-3](#) and described in [Table 3-8](#).

Return to [Summary Table](#).

Maximum Position Count register

Table 3-7. EQEP_QPOS MAX Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0008h |
| EQEP1_REG | 0321 0008h |
| EQEP2_REG | 0322 0008h |

Figure 3-3. EQEP_QPOS MAX Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MAXPOS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-8. EQEP_QPOS MAX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|---|
| 31-0 | MAXPOS | R/W | 0h | This register contains the maximum Position Counter value for error checking in index reset mode or to reset the Position Counter based on the maximum count value. |

3.4 EQEP_QPOSCMP Register (Offset = Ch) [reset = 0h]

EQEP_QPOSCMP is shown in [Figure 3-4](#) and described in [Table 3-10](#).

Return to [Summary Table](#).

Position Compare register

Table 3-9. EQEP_QPOSCMP Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 000Ch |
| EQEP1_REG | 0321 000Ch |
| EQEP2_REG | 0322 000Ch |

Figure 3-4. EQEP_QPOSCMP Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POSCMP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-10. EQEP_QPOSCMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|--|
| 31-0 | POSCMP | R/W | 0h | Position compare value in this register is compared with the Position Counter (EQEP_QPOSCNT[31-0] POSCNT) to optionally generate interrupt on compare match. |

3.5 EQEP_QPOSILAT Register (Offset = 10h) [reset = 0h]

EQEP_QPOSILAT is shown in [Figure 3-5](#) and described in [Table 3-12](#).

Return to [Summary Table](#).

Index Position Latch register

Table 3-11. EQEP_QPOSILAT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0010h |
| EQEP1_REG | 0321 0010h |
| EQEP2_REG | 0322 0010h |

Figure 3-5. EQEP_QPOSILAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IPOS LAT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 3-12. EQEP_QPOSILAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-0 | IPOS LAT | R | 0h | Position Counter value can be latched into this register on index event as defined by the EQEP_QDEC_QEP_CTL[21-20] IEL bit field. |

3.6 EQEP_QPOSSLAT Register (Offset = 14h) [reset = 0h]

EQEP_QPOSSLAT is shown in [Figure 3-6](#) and described in [Table 3-14](#).

Return to [Summary Table](#).

Strobe Position Latch register

Table 3-13. EQEP_QPOSSLAT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0014h |
| EQEP1_REG | 0321 0014h |
| EQEP2_REG | 0322 0014h |

Figure 3-6. EQEP_QPOSSLAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPOSLAT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 3-14. EQEP_QPOSSLAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---|
| 31-0 | SPOSLAT | R | 0h | Position Counter value can be latched into this register on strobe event as defined by the EQEP_QDEC_QEP_CTL[22] SEL bit. |

3.7 EQEP_QPOSLAT Register (Offset = 18h) [reset = 0h]

EQEP_QPOSLAT is shown in [Figure 3-7](#) and described in [Table 3-16](#).

Return to [Summary Table](#).

QEP Position Counter Latch register

Table 3-15. EQEP_QPOSLAT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0018h |
| EQEP1_REG | 0321 0018h |
| EQEP2_REG | 0322 0018h |

Figure 3-7. EQEP_QPOSLAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POSLAT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 3-16. EQEP_QPOSLAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|--|
| 31-0 | POSLAT | R | 0h | Position Counter value can be latched into this register on unit time out event. |

3.8 EQEP_QUTMR Register (Offset = 1Ch) [reset = 0h]

EQEP_QUTMR is shown in [Figure 3-8](#) and described in [Table 3-18](#).

Return to [Summary Table](#).

QEP Unit Timer register

Table 3-17. EQEP_QUTMR Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 001Ch |
| EQEP1_REG | 0321 001Ch |
| EQEP2_REG | 0322 001Ch |

Figure 3-8. EQEP_QUTMR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNITTMR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-18. EQEP_QUTMR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | UNITTMR | R/W | 0h | This register acts as time base for unit time event generation. When this timer value matches with unit time period value, unit time event is generated. |

3.9 EQEP_QUPRD Register (Offset = 20h) [reset = 0h]

EQEP_QUPRD is shown in [Figure 3-9](#) and described in [Table 3-20](#).

Return to [Summary Table](#).

QEP Unit Period register

Table 3-19. EQEP_QUPRD Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0020h |
| EQEP1_REG | 0321 0020h |
| EQEP2_REG | 0322 0020h |

Figure 3-9. EQEP_QUPRD Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNITPRD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-20. EQEP_QUPRD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | UNITPRD | R/W | 0h | This register contains the period count for unit timer to generate periodic unit time events to latch the EQEP position information at periodic interval and optionally to generate interrupt. |

3.10 EQEP_QWD_TMR_PRD Register (Offset = 24h) [reset = 0h]

EQEP_QWD_TMR_PRD is shown in [Figure 3-10](#) and described in [Table 3-22](#).

Return to [Summary Table](#).

QEP Watchdog Timer and Period register

Table 3-21. EQEP_QWD_TMR_PRD Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0024h |
| EQEP1_REG | 0321 0024h |
| EQEP2_REG | 0322 0024h |

Figure 3-10. EQEP_QWD_TMR_PRD Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| QWDPRD | | | | | | | | | | | | | | | | QWDTMR | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-22. EQEP_QWD_TMR_PRD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|--|
| 31-16 | QWDPRD | R/W | 0h | This field contains the time-out count for the QEP peripheral watch dog timer. When watch dog timer value matches with the watch dog period value, status flag is set to indicate the stall. |
| 15-0 | QWDTMR | R/W | 0h | This field acts as time base for watch dog to detect stalls. When this timer value matches with watch dog period value, watch dog timeout event is generated. This register is reset upon edge transition in Quadrature clock indicating the motion. |

3.11 EQEP_QDEC_QEP_CTL Register (Offset = 28h) [reset = 0h]

EQEP_QDEC_QEP_CTL is shown in [Figure 3-11](#) and described in [Table 3-24](#).

Return to [Summary Table](#).

Quadrature Decoder and QEP Control register

Table 3-23. EQEP_QDEC_QEP_CTL Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0028h |
| EQEP1_REG | 0321 0028h |
| EQEP2_REG | 0322 0028h |

Figure 3-11. EQEP_QDEC_QEP_CTL Register

| | | | | | | | |
|-----------|--------|--------|----------|--------|--------|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FREE_SOFT | | PCRM | | SEI | | IEI | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SWI | SEL | IEL | | QPEN | QCLM | UTE | WDE |
| R/W-0h | R/W-0h | R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QSRC | | SOEN | SPSEL | XCR | SWAP | IGATE | QAP |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| QBP | QIP | QSP | RESERVED | | | | |
| R/W-0h | R/W-0h | R/W-0h | R-0h | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-24. EQEP_QDEC_QEP_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| 31-30 | FREE_SOFT | R/W | 0h | <p>POSCNT Behavior:</p> <p>0h = Position Counter stops immediately on emulation suspend</p> <p>1h = Position Counter continues to count until the rollover</p> <p>1x = Position Counter is unaffected by emulation suspend</p> <p>QWDTMR Behavior:</p> <p>2h = Watchdog Counter stops immediately</p> <p>3h = Watchdog Counter counts until WD period match roll over</p> <p>1x = Watchdog Counter is unaffected by emulation suspend</p> <p>UNITTMR Behavior:</p> <p>2h = Unit Timer stops immediately</p> <p>3h = Unit Timer counts until period rollover</p> <p>1x = Unit Timer is unaffected by emulation suspend</p> <p>QCTMR Behavior:</p> <p>0h = Capture Timer stops immediately</p> <p>1h = Capture Timer counts until next unit period event</p> <p>1x = Capture Timer is unaffected by emulation suspend</p> |
| 29-28 | PCRM | R/W | 0h | <p>Position Counter Reset Mode:</p> <p>0h = Index event resets the Position Counter for each revolution</p> <p>1h = Maximum position event resets the Position Counter</p> <p>2h = RESET ONCE: First Index event resets the Position Counter</p> <p>3h = Unit Time event resets the Position Counter</p> |

Table 3-24. EQEP_QDEC_QEP_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|--|
| 27-26 | SEI | R/W | 0h | Strobe Event Initialization of Position Counter: 0h = Do nothing (action disabled) 2h = Initialize Position Counter on Rising edge of QEPS signal 3h = Clockwise Direction: Initialize Position Counter on Rising edge of QEPS strobe. Counter Clockwise Direction: Initialize Position Counter on Falling edge of QEPS strobe. |
| 25-24 | IEI | R/W | 0h | Index Event Initialization of Position Counter: 0h = Do nothing (action disabled) 2h = Initialize Position Counter on Rising edge of index signal 3h = Initialize Position Counter on Falling edge of index signal |
| 23 | SWI | R/W | 0h | Software Initialization of Position Counter: 0h = Do nothing (action disabled) 1h = Initialize Position Counter, this bit is cleared automatically |
| 22 | SEL | R/W | 0h | Strobe Event Latch of Position Counter: 0h = Latch Position Counter on Rising edge of strobe signal 1h = Clockwise Direction: Position Counter is latched on Rising edge of QEPS strobe. Counter Clockwise Direction: Position Counter is latched on Falling edge of QEPS strobe. |
| 21-20 | IEL | R/W | 0h | Index Event Latch of Position Counter (Software Index Marker): 0h = Reserved 1h = Latch Position Counter on Rising edge of index signal 2h = Latch Position Counter on Falling edge of index signal 3h = Software Index Marker Latch the Position Counter and Quadrature direction flag on index event marker. Position Counter is latched to the EQEP_QPOSILAT[31-0] IPOSLAT bit field and direction flag is latched in the EQEP_QEP_STS_CT[4] QDLF bit. |
| 19 | QPEN | R/W | 0h | Quadrature Position Counter Enable/Software Reset: 0h = Software Reset Initialize the internal operating Flag/read-only registers to reset value. Following registers and register bit fields are reset and EQEP control registers retains the same value after software reset: EQEP_QPOSSLAT, EQEP_QC_PRD_TLAT[31-16] QCTMRLAT, EQEP_QCPRDLAT, EQEP_EQEP_QEP_STS_CT 1h = QEP Position Counter is enabled |
| 18 | QCLM | R/W | 0h | EQEP Capture Latch Mode: 0h = Latch on Position Counter read by CPU Capture Timer and Capture Period values are latched into the EQEP_QC_PRD_TLAT and EQEP_QCPRDLAT registers when CPU reads the EQEP_QPOSCNT register. 1h = Latch on Unit Time Out. Position Counter, Capture Timer and Capture Period values are latched into the EQEP_QPOSILAT register, EQEP_QC_PRD_TLAT[31-16] QCTMRLAT bit field and EQEP_QCPRDLAT register on Unit Time out |
| 17 | UTE | R/W | 0h | QEP Unit Timer Enable: 0h = Disable QEP Unit Timer 1h = Enable Unit Timer |
| 16 | WDE | R/W | 0h | QEP Watchdog Enable: 0h = Disable QEP watchdog 1h = Enable QEP watchdog |

Table 3-24. EQEP_QDEC_QEP_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 15-14 | QSRC | R/W | 0h | Position Counter Source selection: 0h = Quadrature count mode (QCLK = iCLK, QDIR = iDIR) 1h = Direction count mode (QCLK = xCLK, QDIR = xDIR) 2h = UP count mode for frequency measurement (QCLK = xCLK, QDIR = 1) 3h = DOWN Count mode for frequency measurement (QCLK = xCLK, QDIR = 0) |
| 13 | SOEN | R/W | 0h | Enable Position Compare Sync Output: 0h = Disable position-compare sync output 1h = Enable position compare sync output |
| 12 | SPSEL | R/W | 0h | Sync Output Pin Selection: 0h = Index pin is used for sync output 1h = Strobe pin is used for sync output |
| 11 | XCR | R/W | 0h | External Clock Rate: 0h = 2× resolution: Count the rising/Falling edge 1h = 1× resolution: Count the Rising edge only |
| 10 | SWAP | R/W | 0h | CLK/DIR Signal Source for Position Counter: 0h = Quadrature clock inputs are not swapped 1h = Quadrature clock inputs are swapped |
| 9 | IGATE | R/W | 0h | Index Pulse Gating Option: 0h = Disable gating of Index pulse 1h = Gate the index pin with strobe |
| 8 | QAP | R/W | 0h | QEPA Input Polarity: 0h = No effect 1h = Negate QEPA input |
| 7 | QBP | R/W | 0h | QEPB Input Polarity: 0h = No effect 1h = Negate QEPB input |
| 6 | QIP | R/W | 0h | QEPI Input Polarity: 0h = No effect 1h = Negate QEPI input |
| 5 | QSP | R/W | 0h | QEPS Input Polarity: 0h = No effect 1h = Negate QEPS input |
| 4-0 | RESERVED | R | 0h | Reserved |

3.12 EQEP_QCAP_QPOS_CTL Register (Offset = 2Ch) [reset = 0h]

EQEP_QCAP_QPOS_CTL is shown in [Figure 3-12](#) and described in [Table 3-26](#).

Return to [Summary Table](#).

QEP Capture and Position Compare Control register

Table 3-25. EQEP_QCAP_QPOS_CTL Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 002Ch |
| EQEP1_REG | 0321 002Ch |
| EQEP2_REG | 0322 002Ch |

Figure 3-12. EQEP_QCAP_QPOS_CTL Register

| | | | | | | | |
|----------|----------|--------|--------|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PCSHDW | PCLOAD | PCPOL | PCE | PCSPW | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCSPW | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CEN | RESERVED | | | | | | |
| R/W-0h | R-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | CCPS | | | UPPS | | | |
| R-0h | R/W-0h | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 3-26. EQEP_QCAP_QPOS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 31 | PCSHDW | R/W | 0h | Position-Compare Shadow Enable: 0h = Shadow disabled, load Immediate 1h = Shadow enabled |
| 30 | PCLOAD | R/W | 0h | Position Compare Shadow Load Mode: 0h = Load On POSCNT = 0 1h = Load When POSCNT = POSCMP |
| 29 | PCPOL | R/W | 0h | Polarity of Sync Output: 0h = Active HIGH pulse output 1h = Active LOW pulse output |
| 28 | PCE | R/W | 0h | Position Compare Enable/Disable: 0h = Disable Mode (no inter or pulse) 1h = Enable Mode |
| 27-16 | PCSPW | R/W | 0h | Select Pulse Width Period in EQEP_FICLK Cycles: 0h = $1 \times 4 \times \text{EQEP_FICLK}$ cycles 1h = $2 \times 4 \times \text{EQEP_FICLK}$ cycles ... FFFh = $4096 \times 4 \times \text{EQEP_FICLK}$ cycles |
| 15 | CEN | R/W | 0h | Enable EQEP Capture: 0h = EQEP Capture unit is disabled 1h = EQEP Capture unit is enabled |

Table 3-26. EQEP_QCAP_QPOS_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 14-7 | RESERVED | R | 0h | Reserved |
| 6-4 | CCPS | R/W | 0h | EQEP Capture Timer Clock Prescaler: 0h = CAPCLK = EQEP_FICLK/1 1h = CAPCLK = EQEP_FICLK/2 2h = CAPCLK = EQEP_FICLK/4 3h = CAPCLK = EQEP_FICLK/8 4h = CAPCLK = EQEP_FICLK/16 5h = CAPCLK = EQEP_FICLK/32 6h = CAPCLK = EQEP_FICLK/64 7h = CAPCLK = EQEP_FICLK/128 |
| 3-0 | UPPS | R/W | 0h | Unit Position Event Prescaler: 0h = UPEVNT = QCLK/1 1h = UPEVNT = QCLK/2 2h = UPEVNT = QCLK/4 3h = UPEVNT = QCLK/8 4h = UPEVNT = QCLK/16 5h = UPEVNT = QCLK/32 6h = UPEVNT = QCLK/64 7h = UPEVNT = QCLK/128 8h = UPEVNT = QCLK/256 9h = UPEVNT = QCLK/512 Ah = UPEVNT = QCLK/1024 Bh = UPEVNT = QCLK/2048 Ch = Reserved Dh = Reserved Eh = Reserved Fh = Reserved |

3.13 EQEP_QINT_EN_FLG Register (Offset = 30h) [reset = 0h]

EQEP_QINT_EN_FLG is shown in [Figure 3-13](#) and described in [Table 3-28](#).

Return to [Summary Table](#).

QEP Interrupt Control and Flag register

Table 3-27. EQEP_QINT_EN_FLG Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0030h |
| EQEP1_REG | 0321 0030h |
| EQEP2_REG | 0322 0030h |

Figure 3-13. EQEP_QINT_EN_FLG Register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | UTOI_FLG | IELI_FLG | SELI_FLG | PCMI_FLG |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCRI_FLG | PCOI_FLG | PCUI_FLG | WTOI_FLG | QDCI_FLG | QPEI_FLG | PCEI_FLG | INT_FLG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | UTOI_EN | IELI_EN | SELI_EN | PCMI_EN |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCRI_EN | PCOI_EN | PCUI_EN | WTOI_EN | QDCI_EN | QPEI_EN | PCEI_EN | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-28. EQEP_QINT_EN_FLG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved |
| 27 | UTOI_FLG | R | 0h | Unit Time Out Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = Set by EQEP unit timer period match |
| 26 | IELI_FLG | R | 0h | Index Event Latch Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set after latching the EQEP_QPOSCNT[31-0] POSCNT bit filed to EQEP_QPOSILAT[31-0] IPOSLAT bit filed |
| 25 | SELI_FLG | R | 0h | Strobe Event Latch Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set after latching the EQEP_QPOSCNT[31-0] POSCNT bit filed to EQEP_QPOSSLAT[31-0] SPOSLAT bit filed |
| 24 | PCMI_FLG | R | 0h | EQEP Compare Match Event Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set on position compare match |
| 23 | PCRI_FLG | R | 0h | Position Compare Ready Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set on position compare FIFO level match |

Table 3-28. EQEP_QINT_EN_FLG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 22 | PCOI_FLG | R | 0h | Position Counter Overflow Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set during the EQEP_QPOSCNT[31-0] POSCNT bit field overflow |
| 21 | PCUI_FLG | R | 0h | Position Counter Underflow Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set during the EQEP_QPOSCNT[31-0] POSCNT bit field underflow |
| 20 | WTOI_FLG | R | 0h | Watchdog Timeout Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = Set by watch dog (monitoring QEPA & QEPB) timeout |
| 19 | QDCI_FLG | R | 0h | Quadrature Direction Change Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This bit is set during change of direction |
| 18 | QPEI_FLG | R | 0h | Quadrature Phase Error Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = Set on simultaneous transition of QEPA & QEPB |
| 17 | PCEI_FLG | R | 0h | Position Counter Error Interrupt Flag: Read 0h = Indicates no interrupt is generated 1h = This is set during error in position count between index |
| 16 | INT_FLG | R | 0h | Global Interrupt Status Flag: Read 0h = Indicates no interrupt is generated Read 1h on this bit indicates that an interrupt was generated from one of the following events. |
| 15-12 | RESERVED | R | 0h | Reserved |
| 11 | UTOI_EN | R/W | 0h | Unit Time Out Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 10 | IELI_EN | R/W | 0h | Index Event Latch Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 9 | SELI_EN | R/W | 0h | Strobe Event Latch Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 8 | PCMI_EN | R/W | 0h | Position Compare Match Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 7 | PCRI_EN | R/W | 0h | Position Compare Ready Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 6 | PCOI_EN | R/W | 0h | Position Counter Overflow Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 5 | PCUI_EN | R/W | 0h | Position Counter Underflow Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |

Table 3-28. EQEP_QINT_EN_FLG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 4 | WTOI_EN | R/W | 0h | Watchdog Time Out Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 3 | QDCI_EN | R/W | 0h | Quadrature Direction Change Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 2 | QPEI_EN | R/W | 0h | Quadrature Phase Error Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 1 | PCEI_EN | R/W | 0h | Position Counter Error Interrupt Enable: 0h = Interrupt is disabled 1h = Interrupt is enabled |
| 0 | RESERVED | R | 0h | Reserved |

3.14 EQEP_QINT_CLR_FRC Register (Offset = 34h) [reset = 0h]

EQEP_QINT_CLR_FRC is shown in [Figure 3-14](#) and described in [Table 3-30](#).

Return to [Summary Table](#).

QEP Interrupt Clear and Forcing register

Table 3-29. EQEP_QINT_CLR_FRC Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0034h |
| EQEP1_REG | 0321 0034h |
| EQEP2_REG | 0322 0034h |

Figure 3-14. EQEP_QINT_CLR_FRC Register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | UTOI_FRC | IELI_FRC | SELI_FRC | PCMI_FRC |
| R-0h | | | | W1S-0h | W1S-0h | W1S-0h | W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCRI_FRC | PCOI_FRC | PCUI_FRC | WTOI_FRC | QDCI_FRC | QPEI_FRC | PCEI_FRC | RESERVED |
| W1S-0h | W1S-0h | W1S-0h | W1S-0h | W1S-0h | W1S-0h | W1S-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | UTOI_CLR | IELI_CLR | SELI_CLR | PCMI_CLR |
| R-0h | | | | W1C-0h | W1C-0h | W1C-0h | W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCRI_CLR | PCOI_CLR | PCUI_CLR | WTOI_CLR | QDCI_CLR | QPEI_CLR | PCEI_CLR | INT_CLR |
| W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h | W1C-0h |

LEGEND: W = Write Only; W1C = Write 1 to Clear Bit; W1S = Write 1 to Set Bit; -n = value after reset

Table 3-30. EQEP_QINT_CLR_FRC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved |
| 27 | UTOI_FRC | W1S | 0h | Unit Time Out Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 26 | IELI_FRC | W1S | 0h | Index Event Latch Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 25 | SELI_FRC | W1S | 0h | Strobe Event Latch Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 24 | PCMI_FRC | W1S | 0h | Position Compare Match Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 23 | PCRI_FRC | W1S | 0h | Position Compare Ready Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 22 | PCOI_FRC | W1S | 0h | Position Counter Overflow Interrupt Force: 0h = No effect 1h = Force the interrupt |

Table 3-30. EQEP_QINT_CLR_FRC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 21 | PCUI_FRC | W1S | 0h | Position Counter Underflow Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 20 | WTOI_FRC | W1S | 0h | Watchdog Time Out Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 19 | QDCI_FRC | W1S | 0h | Quadrature Direction Change Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 18 | QPEI_FRC | W1S | 0h | Quadrature Phase Error Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 17 | PCEI_FRC | W1S | 0h | Position Counter Error Interrupt Force: 0h = No effect 1h = Force the interrupt |
| 16-12 | RESERVED | R | 0h | Reserved |
| 11 | UTOI_CLR | W1C | 0h | Clear Unit Time Out Interrupt Flag: Write 1h = Clears the interrupt flag |
| 10 | IELI_CLR | W1C | 0h | Clear Index Event Latch Interrupt Flag: Write 1h = Clears the interrupt flag |
| 9 | SELI_CLR | W1C | 0h | Clear Strobe Event Latch Interrupt Flag: Write 1h = Clears the interrupt flag |
| 8 | PCMI_CLR | W1C | 0h | Clear QEP Compare Match Event Interrupt Flag: Write 1h = Clears the interrupt flag |
| 7 | PCRI_CLR | W1C | 0h | Clear Position Compare Ready Interrupt Flag: Write 1h = Clears the interrupt flag |
| 6 | PCOI_CLR | W1C | 0h | Clear Position Counter Overflow Interrupt Flag: Write 1h = Clears the interrupt flag |
| 5 | PCUI_CLR | W1C | 0h | Clear Position Counter Underflow Interrupt Flag: Write 1h = Clears the interrupt flag |
| 4 | WTOI_CLR | W1C | 0h | Clear Watchdog Timeout Interrupt Flag: Write 1h = Clears the interrupt flag |
| 3 | QDCI_CLR | W1C | 0h | Clear Quadrature Direction Change Interrupt Flag: Write 1h = Clears the interrupt flag |
| 2 | QPEI_CLR | W1C | 0h | Clear Quadrature Phase Error Interrupt Flag: Write 1h = Clears the interrupt flag |
| 1 | PCEI_CLR | W1C | 0h | Clear Position Counter Error Interrupt Flag: Write 1h = Clears the interrupt flag |
| 0 | INT_CLR | W1C | 0h | Global Interrupt Clear Flag: Write 1h = Clear the interrupt flag and enable further interrupts to be generated if any of the event flags are set to 1h. |

3.15 EQEP_QEP_STS_CT Register (Offset = 38h) [reset = 0h]

EQEP_QEP_STS_CT is shown in [Figure 3-15](#) and described in [Table 3-32](#).

Return to [Summary Table](#).

QEP Status and Capture Timer register

Table 3-31. EQEP_QEP_STS_CT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0038h |
| EQEP1_REG | 0321 0038h |
| EQEP2_REG | 0322 0038h |

Figure 3-15. EQEP_QEP_STS_CT Register

| | | | | | | | |
|----------|------|------|------|----------|----------|----------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QCTMR | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QCTMR | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | FIDF | QDF | QDLF | COEF | CDEF | FIMF | PCEF |
| R-0h | R-0h | R-0h | R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 3-32. EQEP_QEP_STS_CT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|-------|-------|---|
| 31-16 | QCTMR | R/W | 0h | This field provides time base for edge capture unit. |
| 15-7 | RESERVED | R | 0h | Reserved |
| 6 | FIDF | R | 0h | Direction on First Index Marker Status of the direction is latched on first index event marker. |
| 5 | QDF | R | 0h | Quadrature Direction Flag 0h = Anti-clockwise rotation or reverse movement 1h = Clockwise rotation or forward movement |
| 4 | QDLF | R | 0h | EQEP Direction Latch Flag Status of direction is latched on every index event marker. |
| 3 | COEF | R/W1C | 0h | Capture Overflow Error Flag 0h = Sticky bit, cleared by writing 1h 1h = Overflow occurred in EQEP Capture Timer (QEPCTMR) |
| 2 | CDEF | R/W1C | 0h | Capture Direction Error Flag 0h = Sticky bit, cleared by writing 1h 1h = Direction change occurred between the capture position event |
| 1 | FIMF | R/W1C | 0h | First Index Marker Flag 0h = Sticky bit, cleared by writing 1h 1h = Set by first occurrence of index pulse |

Table 3-32. EQEP_QEP_STS_CT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | PCEF | R | 0h | Position Counter Error Flag This bit is not sticky bit and it is updated for every index event. 0h = No error occurred during the last index transition 1h = Position Counter error |

3.16 EQEP_QC_PRD_TLAT Register (Offset = 3Ch) [reset = 0h]

EQEP_QC_PRD_TLAT is shown in [Figure 3-16](#) and described in [Table 3-34](#).

Return to [Summary Table](#).

QEP Capture Period and Timer Latch register

Table 3-33. EQEP_QC_PRD_TLAT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 003Ch |
| EQEP1_REG | 0321 003Ch |
| EQEP2_REG | 0322 003Ch |

Figure 3-16. EQEP_QC_PRD_TLAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| QCTMRLAT | | | | | | | | | | | | | | | | QCPRD | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 3-34. EQEP_QC_PRD_TLAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | QCTMRLAT | R | 0h | EQEP Capture Timer value can be latched into this register on two events: 1) Unit Timeout event 2) Reading the EQEP Position Counter |
| 15-0 | QCPRD | R/W | 0h | This field holds the period count value between the last successive EQEP position events. |

3.17 EQEP_QCPRDLAT Register (Offset = 40h) [reset = 0h]

EQEP_QCPRDLAT is shown in [Figure 3-17](#) and described in [Table 3-36](#).

Return to [Summary Table](#).

QEP Capture Period Latch register

Table 3-35. EQEP_QCPRDLAT Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 0040h |
| EQEP1_REG | 0321 0040h |
| EQEP2_REG | 0322 0040h |

Figure 3-17. EQEP_QCPRDLAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | QCPRDLAT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 3-36. EQEP_QCPRDLAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15-0 | QCPRDLAT | R | 0h | EQEP capture period value can be latched into this register on two events: 1) Unit Timeout event 2) Reading the EQEP Position Counter |

3.18 EQEP_PID Register (Offset = 5Ch) [reset = 44D31903h]

EQEP_PID is shown in [Figure 3-18](#) and described in [Table 3-38](#).

[Return to Summary Table.](#)

Peripheral ID register

Table 3-37. EQEP_PID Instances

| Instance | Physical Address |
|-----------|------------------|
| EQEP0_REG | 0320 005Ch |
| EQEP1_REG | 0321 005Ch |
| EQEP2_REG | 0322 005Ch |

Figure 3-18. EQEP_PID Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 44D31903h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 3-38. EQEP_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-----------|--|
| 31-0 | REVISION | R | 44D31903h | TI Internal Data Identifies the revision of the peripheral. |

4 MCAN Registers

4.1 MCAN Subsystem Registers

Table 4-2 lists the memory-mapped registers for the MCAN Subsystem (MCANSS). All register offset addresses not listed in Table 4-2 should be considered as reserved locations and the register contents should not be modified.

Table 4-1. MCAN Subsystem Instances

| Instance | Base Address |
|--------------|--------------|
| MCU_MCAN0_SS | 4052 0000h |
| MCU_MCAN1_SS | 4056 0000h |
| MCAN0_SS | 0270 0000h |
| MCAN1_SS | 0271 0000h |
| MCAN2_SS | 0272 0000h |
| MCAN3_SS | 0273 0000h |
| MCAN4_SS | 0274 0000h |
| MCAN5_SS | 0275 0000h |
| MCAN6_SS | 0276 0000h |
| MCAN7_SS | 0277 0000h |
| MCAN8_SS | 0278 0000h |
| MCAN9_SS | 0279 0000h |
| MCAN10_SS | 027A 0000h |
| MCAN11_SS | 027B 0000h |
| MCAN12_SS | 027C 0000h |
| MCAN13_SS | 027D 0000h |

Table 4-2. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCU_MCAN0_SS Physical Address | MCU_MCAN1_SS Physical Address |
|--------|--|--|-------------------------------------|-------------------------------------|
| 0h | MCANSS_PID | Revision Register | 4052 0000h | 4056 0000h |
| 4h | MCANSS_CTRL | Control Register | 4052 0004h | 4056 0004h |
| 8h | MCANSS_STAT | Status Register | 4052 0008h | 4056 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 4052 000Ch | 4056 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 4052 0010h | 4056 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 4052 0014h | 4056 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 4052 0018h | 4056 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 4052 001Ch | 4056 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 4052 0020h | 4056 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 4052 0024h | 4056 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserviced Interrupt Counter Register | 4052 0028h | 4056 0028h |

Table 4-3. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN0_SS Physical Address | MCAN1_SS Physical Address |
|--------|-----------------------------|---------------------------------|---------------------------------|---------------------------------|
| 0h | MCANSS_PID | Revision Register | 0270 0000h | 0271 0000h |
| 4h | MCANSS_CTRL | Control Register | 0270 0004h | 0271 0004h |
| 8h | MCANSS_STAT | Status Register | 0270 0008h | 0271 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 0270 000Ch | 0271 000Ch |

Table 4-3. MCAN Subsystem Registers (continued)

| Offset | Acronym | Register Name | MCAN0_SS Physical Address | MCAN1_SS Physical Address |
|--------|--|--|---------------------------|---------------------------|
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 0270 0010h | 0271 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 0270 0014h | 0271 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 0270 0018h | 0271 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 0270 001Ch | 0271 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 0270 0020h | 0271 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 0270 0024h | 0271 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 0270 0028h | 0271 0028h |

Table 4-4. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN2_SS Physical Address | MCAN3_SS Physical Address |
|--------|--|--|---------------------------|---------------------------|
| 0h | MCANSS_PID | Revision Register | 0272 0000h | 0273 0000h |
| 4h | MCANSS_CTRL | Control Register | 0272 0004h | 0273 0004h |
| 8h | MCANSS_STAT | Status Register | 0272 0008h | 0273 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 0272 000Ch | 0273 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 0272 0010h | 0273 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 0272 0014h | 0273 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 0272 0018h | 0273 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 0272 001Ch | 0273 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 0272 0020h | 0273 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 0272 0024h | 0273 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 0272 0028h | 0273 0028h |

Table 4-5. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN4_SS Physical Address | MCAN5_SS Physical Address |
|--------|--|--|---------------------------|---------------------------|
| 0h | MCANSS_PID | Revision Register | 0274 0000h | 0275 0000h |
| 4h | MCANSS_CTRL | Control Register | 0274 0004h | 0275 0004h |
| 8h | MCANSS_STAT | Status Register | 0274 0008h | 0275 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 0274 000Ch | 0275 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 0274 0010h | 0275 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 0274 0014h | 0275 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 0274 0018h | 0275 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 0274 001Ch | 0275 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 0274 0020h | 0275 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 0274 0024h | 0275 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 0274 0028h | 0275 0028h |

Table 4-6. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN6_SS Physical Address | MCAN7_SS Physical Address |
|--------|--|--|---------------------------|---------------------------|
| 0h | MCANSS_PID | Revision Register | 0276 0000h | 0277 0000h |
| 4h | MCANSS_CTRL | Control Register | 0276 0004h | 0277 0004h |
| 8h | MCANSS_STAT | Status Register | 0276 0008h | 0277 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 0276 000Ch | 0277 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 0276 0010h | 0277 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 0276 0014h | 0277 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 0276 0018h | 0277 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 0276 001Ch | 0277 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 0276 0020h | 0277 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 0276 0024h | 0277 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 0276 0028h | 0277 0028h |

Table 4-7. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN8_SS Physical Address | MCAN9_SS Physical Address |
|--------|--|--|---------------------------|---------------------------|
| 0h | MCANSS_PID | Revision Register | 0278 0000h | 0279 0000h |
| 4h | MCANSS_CTRL | Control Register | 0278 0004h | 0279 0004h |
| 8h | MCANSS_STAT | Status Register | 0278 0008h | 0279 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 0278 000Ch | 0279 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 0278 0010h | 0279 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 0278 0014h | 0279 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 0278 0018h | 0279 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 0278 001Ch | 0279 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 0278 0020h | 0279 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 0278 0024h | 0279 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 0278 0028h | 0279 0028h |

Table 4-8. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN10_SS Physical Address | MCAN11_SS Physical Address |
|--------|---|--|----------------------------|----------------------------|
| 0h | MCANSS_PID | Revision Register | 027A 0000h | 027B 0000h |
| 4h | MCANSS_CTRL | Control Register | 027A 0004h | 027B 0004h |
| 8h | MCANSS_STAT | Status Register | 027A 0008h | 027B 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 027A 000Ch | 027B 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 027A 0010h | 027B 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 027A 0014h | 027B 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 027A 0018h | 027B 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 027A 001Ch | 027B 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 027A 0020h | 027B 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 027A 0024h | 027B 0024h |

Table 4-8. MCAN Subsystem Registers (continued)

| Offset | Acronym | Register Name | MCAN10_SS Physical Address | MCAN11_SS Physical Address |
|--------|--|---|----------------------------------|----------------------------------|
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 027A 0028h | 027B 0028h |

Table 4-9. MCAN Subsystem Registers

| Offset | Acronym | Register Name | MCAN12_SS Physical Address | MCAN13_SS Physical Address |
|--------|--|---|----------------------------------|----------------------------------|
| 0h | MCANSS_PID | Revision Register | 027C 0000h | 027D 0000h |
| 4h | MCANSS_CTRL | Control Register | 027C 0004h | 027D 0004h |
| 8h | MCANSS_STAT | Status Register | 027C 0008h | 027D 0008h |
| Ch | MCANSS_ICS | Interrupt Clear Shadow Register | 027C 000Ch | 027D 000Ch |
| 10h | MCANSS_IRS | Interrupt Raw Status Register | 027C 0010h | 027D 0010h |
| 14h | MCANSS_IECS | Interrupt Enable Clear Shadow Register | 027C 0014h | 027D 0014h |
| 18h | MCANSS_IE | Interrupt Enable Register | 027C 0018h | 027D 0018h |
| 1Ch | MCANSS_IES | Interrupt Enable Status Register | 027C 001Ch | 027D 001Ch |
| 20h | MCANSS_EOI | End Of Interrupt (EOI) Register | 027C 0020h | 027D 0020h |
| 24h | MCANSS_EXT_TS_PRESCALER | External Timestamp Prescaler Register | 027C 0024h | 027D 0024h |
| 28h | MCANSS_EXT_TS_UNSERVICED_INTR_CNTR | External Timestamp Unserved Interrupt Counter Register | 027C 0028h | 027D 0028h |

4.1.1 MCANSS_PID Register (Offset = 0h) [reset = 68E08101h]

MCANSS_PID is shown in [Figure 4-1](#) and described in [Table 4-11](#).

[Return to Summary Table.](#)

Revision Register

The Revision Register contains the major and minor revisions for the MCANSS.

Table 4-10. MCANSS_PID Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0000h |
| MCU_MCAN1_SS | 4056 0000h |
| MCAN0_SS | 0270 0000h |
| MCAN1_SS | 0271 0000h |
| MCAN2_SS | 0272 0000h |
| MCAN3_SS | 0273 0000h |
| MCAN4_SS | 0274 0000h |
| MCAN5_SS | 0275 0000h |
| MCAN6_SS | 0276 0000h |
| MCAN7_SS | 0277 0000h |
| MCAN8_SS | 0278 0000h |
| MCAN9_SS | 0279 0000h |
| MCAN10_SS | 027A 0000h |
| MCAN11_SS | 027B 0000h |
| MCAN12_SS | 027C 0000h |
| MCAN13_SS | 027D 0000h |

Figure 4-1. MCANSS_PID Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|-------|----|----|--------|----|----|-------|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-8E0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTL | | | | | MAJOR | | | CUSTOM | | | MINOR | | | | |
| R-10h | | | | | R-1h | | | R-0h | | | R-1h | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-11. MCANSS_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|------------------------------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | Business Unit (2h = Processors) |
| 27-16 | MODULE_ID | R | 8E0h | Module ID |
| 15-11 | RTL | R | 10h | RTL Revision |
| 10-8 | MAJOR | R | 1h | Major Revision |
| 7-6 | CUSTOM | R | 0h | Custom |
| 5-0 | MINOR | R | 1h | Minor Revision |

4.1.2 MCANSS_CTRL Register (Offset = 4h) [reset = 8h]

MCANSS_CTRL is shown in [Figure 4-2](#) and described in [Table 4-13](#).

Return to [Summary Table](#).

Control Register

The Control Register contains general control bits for the MCANSS.

Table 4-12. MCANSS_CTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0004h |
| MCU_MCAN1_SS | 4056 0004h |
| MCAN0_SS | 0270 0004h |
| MCAN1_SS | 0271 0004h |
| MCAN2_SS | 0272 0004h |
| MCAN3_SS | 0273 0004h |
| MCAN4_SS | 0274 0004h |
| MCAN5_SS | 0275 0004h |
| MCAN6_SS | 0276 0004h |
| MCAN7_SS | 0277 0004h |
| MCAN8_SS | 0278 0004h |
| MCAN9_SS | 0279 0004h |
| MCAN10_SS | 027A 0004h |
| MCAN11_SS | 027B 0004h |
| MCAN12_SS | 027C 0004h |
| MCAN13_SS | 027D 0004h |

Figure 4-2. MCANSS_CTRL Register

| | | | | | | | |
|----------|----------------|------------|-------------|---------------|----------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | EXT_TS_CNTR_EN | AUTOWAKEUP | WAKEUPREQEN | DBG_SUSP_FREE | RESERVED | | |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-13. MCANSS_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-----------------------------------|
| 31-7 | RESERVED | R | 0h | Reserved |
| 6 | EXT_TS_CNTR_EN | R/W | 0h | External Timestamp Counter Enable |
| 5 | AUTOWAKEUP | R/W | 0h | Automatic Wakeup Enable |
| 4 | WAKEUPREQEN | R/W | 0h | Wakeup Request Enable |

Table 4-13. MCANSS_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 3 | DBGSUSP_FREE | R/W | 1h | Debug Suspend 0h = Honor debug suspend 1h = Disregard debug suspend |
| 2-0 | RESERVED | R | 0h | Reserved |

4.1.3 MCANSS_STAT Register (Offset = 8h) [reset = -00h]

MCANSS_STAT is shown in [Figure 4-3](#) and described in [Table 4-15](#).

[Return to Summary Table.](#)

Status Register

The Status Register provides general status bits for the MCANSS.

Table 4-14. MCANSS_STAT Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0008h |
| MCU_MCAN1_SS | 4056 0008h |
| MCAN0_SS | 0270 0008h |
| MCAN1_SS | 0271 0008h |
| MCAN2_SS | 0272 0008h |
| MCAN3_SS | 0273 0008h |
| MCAN4_SS | 0274 0008h |
| MCAN5_SS | 0275 0008h |
| MCAN6_SS | 0276 0008h |
| MCAN7_SS | 0277 0008h |
| MCAN8_SS | 0278 0008h |
| MCAN9_SS | 0279 0008h |
| MCAN10_SS | 027A 0008h |
| MCAN11_SS | 027B 0008h |
| MCAN12_SS | 027C 0008h |
| MCAN13_SS | 027D 0008h |

Figure 4-3. MCANSS_STAT Register

| | | | | | | | |
|----------|----|----|----|----|-------------|---------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | ENABLE_FDOE | MEM_INIT_DONE | RESERVED |
| R-0h | | | | | R- | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 4-15. MCANSS_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-3 | RESERVED | R | 0h | Reserved |
| 2 | ENABLE_FDOE | R | -h | Enable FD (Flexible Data-Rate) Configuration Reflects the value of mcanss_enable_fdoe configuration port, -h = mcanss_enable_fdoe. |

Table 4-15. MCANSS_STAT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 1 | MEM_INIT_DONE | R | 0h | Memory Initialization 0h = Memory initialization is in progress 1h = Memory initialization done |
| 0 | RESERVED | R | 0h | Reserved |

4.1.4 MCANSS_ICS Register (Offset = Ch) [reset = 0h]

MCANSS_ICS is shown in [Figure 4-4](#) and described in [Table 4-17](#).

Return to [Summary Table](#).

Interrupt Clear Shadow Register

Write 1h to clear interrupt bits.

Table 4-16. MCANSS_ICS Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 000Ch |
| MCU_MCAN1_SS | 4056 000Ch |
| MCAN0_SS | 0270 000Ch |
| MCAN1_SS | 0271 000Ch |
| MCAN2_SS | 0272 000Ch |
| MCAN3_SS | 0273 000Ch |
| MCAN4_SS | 0274 000Ch |
| MCAN5_SS | 0275 000Ch |
| MCAN6_SS | 0276 000Ch |
| MCAN7_SS | 0277 000Ch |
| MCAN8_SS | 0278 000Ch |
| MCAN9_SS | 0279 000Ch |
| MCAN10_SS | 027A 000Ch |
| MCAN11_SS | 027B 000Ch |
| MCAN12_SS | 027C 000Ch |
| MCAN13_SS | 027D 000Ch |

Figure 4-4. MCANSS_ICS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EXT_TS_CNTR_OVFL |
| R-0h | | | | | | | W-0h |

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-17. MCANSS_ICS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | EXT_TS_CNTR_OVFL | W | 0h | External Timestamp Counter Overflow Interrupt Status Write 1h to clear bits. |

4.1.5 MCANSS_IRS Register (Offset = 10h) [reset = 0h]

MCANSS_IRS is shown in [Figure 4-5](#) and described in [Table 4-19](#).

Return to [Summary Table](#).

Interrupt Raw Status Register

Write 1h to set interrupt bits.

Table 4-18. MCANSS_IRS Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0010h |
| MCU_MCAN1_SS | 4056 0010h |
| MCAN0_SS | 0270 0010h |
| MCAN1_SS | 0271 0010h |
| MCAN2_SS | 0272 0010h |
| MCAN3_SS | 0273 0010h |
| MCAN4_SS | 0274 0010h |
| MCAN5_SS | 0275 0010h |
| MCAN6_SS | 0276 0010h |
| MCAN7_SS | 0277 0010h |
| MCAN8_SS | 0278 0010h |
| MCAN9_SS | 0279 0010h |
| MCAN10_SS | 027A 0010h |
| MCAN11_SS | 027B 0010h |
| MCAN12_SS | 027C 0010h |
| MCAN13_SS | 027D 0010h |

Figure 4-5. MCANSS_IRS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EXT_TS_CNTR_OVFL |
| R-0h | | | | | | | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-19. MCANSS_IRS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | EXT_TS_CNTR_OVFL | R/W1S | 0h | External Timestamp Counter Overflow Interrupt Status Write 1h to set bits. |

4.1.6 MCANSS_IECS Register (Offset = 14h) [reset = 0h]

MCANSS_IECS is shown in [Figure 4-6](#) and described in [Table 4-21](#).

Return to [Summary Table](#).

Interrupt Enable Clear Shadow Register

Write 1h to clear interrupt enable bits.

Table 4-20. MCANSS_IECS Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0014h |
| MCU_MCAN1_SS | 4056 0014h |
| MCAN0_SS | 0270 0014h |
| MCAN1_SS | 0271 0014h |
| MCAN2_SS | 0272 0014h |
| MCAN3_SS | 0273 0014h |
| MCAN4_SS | 0274 0014h |
| MCAN5_SS | 0275 0014h |
| MCAN6_SS | 0276 0014h |
| MCAN7_SS | 0277 0014h |
| MCAN8_SS | 0278 0014h |
| MCAN9_SS | 0279 0014h |
| MCAN10_SS | 027A 0014h |
| MCAN11_SS | 027B 0014h |
| MCAN12_SS | 027C 0014h |
| MCAN13_SS | 027D 0014h |

Figure 4-6. MCANSS_IECS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EXT_TS_CNTR_OVFL |
| R-0h | | | | | | | W1C-0h |

LEGEND: R = Read Only; W1C = Write 1 to Clear Bit; -n = value after reset

Table 4-21. MCANSS_IECS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | EXT_TS_CNTR_OVFL | W1C | 0h | External Timestamp Counter Overflow Interrupt Write 1h to clear bits. |

4.1.7 MCANSS_IE Register (Offset = 18h) [reset = 0h]

MCANSS_IE is shown in [Figure 4-7](#) and described in [Table 4-23](#).

Return to [Summary Table](#).

Interrupt Enable Register

Write 1h to set interrupt bits.

Table 4-22. MCANSS_IE Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0018h |
| MCU_MCAN1_SS | 4056 0018h |
| MCAN0_SS | 0270 0018h |
| MCAN1_SS | 0271 0018h |
| MCAN2_SS | 0272 0018h |
| MCAN3_SS | 0273 0018h |
| MCAN4_SS | 0274 0018h |
| MCAN5_SS | 0275 0018h |
| MCAN6_SS | 0276 0018h |
| MCAN7_SS | 0277 0018h |
| MCAN8_SS | 0278 0018h |
| MCAN9_SS | 0279 0018h |
| MCAN10_SS | 027A 0018h |
| MCAN11_SS | 027B 0018h |
| MCAN12_SS | 027C 0018h |
| MCAN13_SS | 027D 0018h |

Figure 4-7. MCANSS_IE Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EXT_TS_CNTR_OVFL |
| R-0h | | | | | | | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-23. MCANSS_IE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | EXT_TS_CNTR_OVFL | R/W1S | 0h | External Timestamp Counter Overflow Interrupt Write 1h to set bits. |

4.1.8 MCANSS_IES Register (Offset = 1Ch) [reset = 0h]

MCANSS_IES is shown in [Figure 4-8](#) and described in [Table 4-25](#).

[Return to Summary Table.](#)

Interrupt Enable Status Register

Read enabled interrupts.

Table 4-24. MCANSS_IES Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 001Ch |
| MCU_MCAN1_SS | 4056 001Ch |
| MCAN0_SS | 0270 001Ch |
| MCAN1_SS | 0271 001Ch |
| MCAN2_SS | 0272 001Ch |
| MCAN3_SS | 0273 001Ch |
| MCAN4_SS | 0274 001Ch |
| MCAN5_SS | 0275 001Ch |
| MCAN6_SS | 0276 001Ch |
| MCAN7_SS | 0277 001Ch |
| MCAN8_SS | 0278 001Ch |
| MCAN9_SS | 0279 001Ch |
| MCAN10_SS | 027A 001Ch |
| MCAN11_SS | 027B 001Ch |
| MCAN12_SS | 027C 001Ch |
| MCAN13_SS | 027D 001Ch |

Figure 4-8. MCANSS_IES Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EXT_TS_CNTR_OVFL |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 4-25. MCANSS_IES Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | EXT_TS_CNTR_OVFL | R | 0h | External Timestamp Counter Overflow Interrupt |

4.1.9 MCANSS_EOI Register (Offset = 20h) [reset = 0h]

MCANSS_EOI is shown in [Figure 4-9](#) and described in [Table 4-27](#).

[Return to Summary Table.](#)

End Of Interrupt (EOI) Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-26. MCANSS_EOI Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0020h |
| MCU_MCAN1_SS | 4056 0020h |
| MCAN0_SS | 0270 0020h |
| MCAN1_SS | 0271 0020h |
| MCAN2_SS | 0272 0020h |
| MCAN3_SS | 0273 0020h |
| MCAN4_SS | 0274 0020h |
| MCAN5_SS | 0275 0020h |
| MCAN6_SS | 0276 0020h |
| MCAN7_SS | 0277 0020h |
| MCAN8_SS | 0278 0020h |
| MCAN9_SS | 0279 0020h |
| MCAN10_SS | 027A 0020h |
| MCAN11_SS | 027B 0020h |
| MCAN12_SS | 027C 0020h |
| MCAN13_SS | 027D 0020h |

Figure 4-9. MCANSS_EOI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | EOI | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | W-0h | | | | | | | |

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 4-27. MCANSS_EOI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved |
| 7-0 | EOI | W | 0h | End Of Interrupt Write with bit position of the targeted interrupt (example: external timestamp is bit 0). Upon write, level interrupt will clear and if unserviced interrupt counter > 1h will issue another pulse interrupt. 0h = EOI value for external timestamp interrupt 1h = EOI value for mcan[0] interrupt 2h = EOI value for mcan[1] interrupt |

4.1.10 MCANSS_EXT_TS_PRESCALER Register (Offset = 24h) [reset = 0h]

MCANSS_EXT_TS_PRESCALER is shown in [Figure 4-10](#) and described in [Table 4-29](#).

Return to [Summary Table](#).

External Timestamp Prescaler Register

**Table 4-28. MCANSS_EXT_TS_PRESCALER
Instances**

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0024h |
| MCU_MCAN1_SS | 4056 0024h |
| MCAN0_SS | 0270 0024h |
| MCAN1_SS | 0271 0024h |
| MCAN2_SS | 0272 0024h |
| MCAN3_SS | 0273 0024h |
| MCAN4_SS | 0274 0024h |
| MCAN5_SS | 0275 0024h |
| MCAN6_SS | 0276 0024h |
| MCAN7_SS | 0277 0024h |
| MCAN8_SS | 0278 0024h |
| MCAN9_SS | 0279 0024h |
| MCAN10_SS | 027A 0024h |
| MCAN11_SS | 027B 0024h |
| MCAN12_SS | 027C 0024h |
| MCAN13_SS | 027D 0024h |

Figure 4-10. MCANSS_EXT_TS_PRESCALER Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | PRESCALER | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-29. MCANSS_EXT_TS_PRESCALER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved |
| 23-0 | PRESCALER | R/W | 0h | External Timestamp Prescaler Reload Value External timestamp count rate is host clock rate divided by this value with one exception - a value of 0h has the same effect as 1h. |

4.1.11 MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register (Offset = 28h) [reset = 0h]

MCANSS_EXT_TS_UNSERVICED_INTR_CNTR is shown in [Figure 4-11](#) and described in [Table 4-31](#).

Return to [Summary Table](#).

External Timestamp Unserviced Interrupts Counter Register

Table 4-30.
MCANSS_EXT_TS_UNSERVICED_INTR_CNTR
Instances

| Instance | Physical Address |
|--------------|------------------|
| MCU_MCAN0_SS | 4052 0028h |
| MCU_MCAN1_SS | 4056 0028h |
| MCAN0_SS | 0270 0028h |
| MCAN1_SS | 0271 0028h |
| MCAN2_SS | 0272 0028h |
| MCAN3_SS | 0273 0028h |
| MCAN4_SS | 0274 0028h |
| MCAN5_SS | 0275 0028h |
| MCAN6_SS | 0276 0028h |
| MCAN7_SS | 0277 0028h |
| MCAN8_SS | 0278 0028h |
| MCAN9_SS | 0279 0028h |
| MCAN10_SS | 027A 0028h |
| MCAN11_SS | 027B 0028h |
| MCAN12_SS | 027C 0028h |
| MCAN13_SS | 027D 0028h |

Figure 4-11. MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register

| | | | | | | | |
|----------|----|----|----|------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | EXT_TS_INTR_CNTR | | | |
| R-0h | | | | R-0h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-31. MCANSS_EXT_TS_UNSERVICED_INTR_CNTR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-5 | RESERVED | R | 0h | Reserved |
| 4-0 | EXT_TS_INTR_CNTR | R | 0h | Number of Unserviced Rollover Interrupts If > 1h an EOI write will issue another pulse interrupt. |

4.2 MCAN Core Registers

Table 4-33 lists the memory-mapped registers for the MCAN Core. All register offset addresses not listed in Table 4-33 should be considered as reserved locations and the register contents should not be modified.

Table 4-32. MCAN Core Instances

| Instance | Base Address |
|---------------|--------------|
| MCU_MCAN0_CFG | 4052 8000h |
| MCU_MCAN1_CFG | 4056 8000h |
| MCAN0_CFG | 0270 1000h |
| MCAN1_CFG | 0271 1000h |
| MCAN2_CFG | 0272 1000h |
| MCAN3_CFG | 0273 1000h |
| MCAN4_CFG | 0274 1000h |
| MCAN5_CFG | 0275 1000h |
| MCAN6_CFG | 0276 1000h |
| MCAN7_CFG | 0277 1000h |
| MCAN8_CFG | 0278 1000h |
| MCAN9_CFG | 0279 1000h |
| MCAN10_CFG | 027A 1000h |
| MCAN11_CFG | 027B 1000h |
| MCAN12_CFG | 027C 1000h |
| MCAN13_CFG | 027D 1000h |

Table 4-33. MCAN Core Registers

| Offset | Acronym | Register Name | MCU_MCAN0_CFG Physical Address | MCU_MCAN1_CFG Physical Address |
|--------|----------------------------|---|--------------------------------|--------------------------------|
| 0h | MCAN_CREL | Core Release Register | 4052 8000h | 4056 8000h |
| 4h | MCAN_ENDN | Endian Register | 4052 8004h | 4056 8004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 4052 800Ch | 4056 800Ch |
| 10h | MCAN_TEST | Test Register | 4052 8010h | 4056 8010h |
| 14h | MCAN_RWD | RAM Watchdog | 4052 8014h | 4056 8014h |
| 18h | MCAN_CCCR | CC Control Register | 4052 8018h | 4056 8018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 4052 801Ch | 4056 801Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 4052 8020h | 4056 8020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 4052 8024h | 4056 8024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 4052 8028h | 4056 8028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 4052 802Ch | 4056 802Ch |
| 40h | MCAN_ECR | Error Counter Register | 4052 8040h | 4056 8040h |
| 44h | MCAN_PSR | Protocol Status Register | 4052 8044h | 4056 8044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 4052 8048h | 4056 8048h |
| 50h | MCAN_IR | Interrupt Register | 4052 8050h | 4056 8050h |
| 54h | MCAN_IE | Interrupt Enable | 4052 8054h | 4056 8054h |
| 58h | MCAN_ILS | Interrupt Line Select | 4052 8058h | 4056 8058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 4052 805Ch | 4056 805Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 4052 8080h | 4056 8080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 4052 8084h | 4056 8084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 4052 8088h | 4056 8088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 4052 8090h | 4056 8090h |
| 94h | MCAN_HPMS | High Priority Message Status | 4052 8094h | 4056 8094h |

Table 4-33. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCU_MCAN0_CFG Physical Address | MCU_MCAN1_CFG Physical Address |
|--------|-----------------------------|--|--------------------------------|--------------------------------|
| 98h | MCAN_NDAT1 | New Data 1 | 4052 8098h | 4056 8098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 4052 809Ch | 4056 809Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 4052 80A0h | 4056 80A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 4052 80A4h | 4056 80A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 4052 80A8h | 4056 80A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 4052 80ACh | 4056 80ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 4052 80B0h | 4056 80B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 4052 80B4h | 4056 80B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 4052 80B8h | 4056 80B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 4052 80BCh | 4056 80BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 4052 80C0h | 4056 80C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 4052 80C4h | 4056 80C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 4052 80C8h | 4056 80C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 4052 80CCh | 4056 80CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 4052 80D0h | 4056 80D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 4052 80D4h | 4056 80D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 4052 80D8h | 4056 80D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 4052 80DCh | 4056 80DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 4052 80E0h | 4056 80E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 4052 80E4h | 4056 80E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 4052 80F0h | 4056 80F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 4052 80F4h | 4056 80F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 4052 80F8h | 4056 80F8h |

Table 4-34. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN0_CFG Physical Address | MCAN1_CFG Physical Address |
|--------|---------------------------|---|----------------------------|----------------------------|
| 0h | MCAN_CREL | Core Release Register | 0270 1000h | 0271 1000h |
| 4h | MCAN_ENDN | Endian Register | 0270 1004h | 0271 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 0270 100Ch | 0271 100Ch |
| 10h | MCAN_TEST | Test Register | 0270 1010h | 0271 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 0270 1014h | 0271 1014h |
| 18h | MCAN_CCCR | CC Control Register | 0270 1018h | 0271 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 0270 101Ch | 0271 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 0270 1020h | 0271 1020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 0270 1024h | 0271 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 0270 1028h | 0271 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 0270 102Ch | 0271 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 0270 1040h | 0271 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 0270 1044h | 0271 1044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 0270 1048h | 0271 1048h |
| 50h | MCAN_IR | Interrupt Register | 0270 1050h | 0271 1050h |
| 54h | MCAN_IE | Interrupt Enable | 0270 1054h | 0271 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 0270 1058h | 0271 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 0270 105Ch | 0271 105Ch |

Table 4-34. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN0_CFG Physical Address | MCAN1_CFG Physical Address |
|--------|-----------------------------|--|----------------------------------|----------------------------------|
| 80h | MCAN_GFC | Global Filter Configuration | 0270 1080h | 0271 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 0270 1084h | 0271 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 0270 1088h | 0271 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 0270 1090h | 0271 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 0270 1094h | 0271 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 0270 1098h | 0271 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 0270 109Ch | 0271 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 0270 10A0h | 0271 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 0270 10A4h | 0271 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 0270 10A8h | 0271 10A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 0270 10ACh | 0271 10ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 0270 10B0h | 0271 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 0270 10B4h | 0271 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 0270 10B8h | 0271 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 0270 10BCh | 0271 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 0270 10C0h | 0271 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 0270 10C4h | 0271 10C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 0270 10C8h | 0271 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 0270 10CCh | 0271 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 0270 10D0h | 0271 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 0270 10D4h | 0271 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 0270 10D8h | 0271 10D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 0270 10DCh | 0271 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 0270 10E0h | 0271 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 0270 10E4h | 0271 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 0270 10F0h | 0271 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 0270 10F4h | 0271 10F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 0270 10F8h | 0271 10F8h |

Table 4-35. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN2_CFG Physical Address | MCAN3_CFG Physical Address |
|--------|---------------------------|---|----------------------------------|----------------------------------|
| 0h | MCAN_CREL | Core Release Register | 0272 1000h | 0273 1000h |
| 4h | MCAN_ENDN | Endian Register | 0272 1004h | 0273 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 0272 100Ch | 0273 100Ch |
| 10h | MCAN_TEST | Test Register | 0272 1010h | 0273 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 0272 1014h | 0273 1014h |
| 18h | MCAN_CCCR | CC Control Register | 0272 1018h | 0273 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 0272 101Ch | 0273 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 0272 1020h | 0273 1020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 0272 1024h | 0273 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 0272 1028h | 0273 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 0272 102Ch | 0273 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 0272 1040h | 0273 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 0272 1044h | 0273 1044h |

Table 4-35. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN2_CFG Physical Address | MCAN3_CFG Physical Address |
|--------|-----------------------------|--|----------------------------------|----------------------------------|
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 0272 1048h | 0273 1048h |
| 50h | MCAN_IR | Interrupt Register | 0272 1050h | 0273 1050h |
| 54h | MCAN_IE | Interrupt Enable | 0272 1054h | 0273 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 0272 1058h | 0273 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 0272 105Ch | 0273 105Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 0272 1080h | 0273 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 0272 1084h | 0273 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 0272 1088h | 0273 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 0272 1090h | 0273 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 0272 1094h | 0273 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 0272 1098h | 0273 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 0272 109Ch | 0273 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 0272 10A0h | 0273 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 0272 10A4h | 0273 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 0272 10A8h | 0273 10A8h |
| ACCh | MCAN_RXBC | Rx Buffer Configuration | 0272 10ACCh | 0273 10ACCh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 0272 10B0h | 0273 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 0272 10B4h | 0273 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 0272 10B8h | 0273 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 0272 10BCh | 0273 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 0272 10C0h | 0273 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 0272 10C4h | 0273 10C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 0272 10C8h | 0273 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 0272 10CCh | 0273 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 0272 10D0h | 0273 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 0272 10D4h | 0273 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 0272 10D8h | 0273 10D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 0272 10DCh | 0273 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 0272 10E0h | 0273 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 0272 10E4h | 0273 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 0272 10F0h | 0273 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 0272 10F4h | 0273 10F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 0272 10F8h | 0273 10F8h |

Table 4-36. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN4_CFG Physical Address | MCAN5_CFG Physical Address |
|--------|---------------------------|---|----------------------------------|----------------------------------|
| 0h | MCAN_CREL | Core Release Register | 0274 1000h | 0275 1000h |
| 4h | MCAN_ENDN | Endian Register | 0274 1004h | 0275 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 0274 100Ch | 0275 100Ch |
| 10h | MCAN_TEST | Test Register | 0274 1010h | 0275 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 0274 1014h | 0275 1014h |
| 18h | MCAN_CCCR | CC Control Register | 0274 1018h | 0275 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 0274 101Ch | 0275 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 0274 1020h | 0275 1020h |

Table 4-36. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN4_CFG Physical Address | MCAN5_CFG Physical Address |
|--------|-----------------------------|--|----------------------------------|----------------------------------|
| 24h | MCAN_TSCV | Timestamp Counter Value | 0274 1024h | 0275 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 0274 1028h | 0275 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 0274 102Ch | 0275 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 0274 1040h | 0275 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 0274 1044h | 0275 1044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 0274 1048h | 0275 1048h |
| 50h | MCAN_IR | Interrupt Register | 0274 1050h | 0275 1050h |
| 54h | MCAN_IE | Interrupt Enable | 0274 1054h | 0275 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 0274 1058h | 0275 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 0274 105Ch | 0275 105Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 0274 1080h | 0275 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 0274 1084h | 0275 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 0274 1088h | 0275 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 0274 1090h | 0275 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 0274 1094h | 0275 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 0274 1098h | 0275 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 0274 109Ch | 0275 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 0274 10A0h | 0275 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 0274 10A4h | 0275 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 0274 10A8h | 0275 10A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 0274 10ACh | 0275 10ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 0274 10B0h | 0275 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 0274 10B4h | 0275 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 0274 10B8h | 0275 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 0274 10BCh | 0275 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 0274 10C0h | 0275 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 0274 10C4h | 0275 10C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 0274 10C8h | 0275 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 0274 10CCh | 0275 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 0274 10D0h | 0275 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 0274 10D4h | 0275 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 0274 10D8h | 0275 10D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 0274 10DCh | 0275 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 0274 10E0h | 0275 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 0274 10E4h | 0275 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 0274 10F0h | 0275 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 0274 10F4h | 0275 10F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 0274 10F8h | 0275 10F8h |

Table 4-37. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN6_CFG Physical Address | MCAN7_CFG Physical Address |
|--------|---------------------------|--------------------------------------|----------------------------------|----------------------------------|
| 0h | MCAN_CREL | Core Release Register | 0276 1000h | 0277 1000h |
| 4h | MCAN_ENDN | Endian Register | 0276 1004h | 0277 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 0276 100Ch | 0277 100Ch |

Table 4-37. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN6_CFG Physical Address | MCAN7_CFG Physical Address |
|--------|-----------------------------|--|----------------------------------|----------------------------------|
| 10h | MCAN_TEST | Test Register | 0276 1010h | 0277 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 0276 1014h | 0277 1014h |
| 18h | MCAN_CCCR | CC Control Register | 0276 1018h | 0277 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 0276 101Ch | 0277 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 0276 1020h | 0277 1020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 0276 1024h | 0277 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 0276 1028h | 0277 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 0276 102Ch | 0277 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 0276 1040h | 0277 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 0276 1044h | 0277 1044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 0276 1048h | 0277 1048h |
| 50h | MCAN_IR | Interrupt Register | 0276 1050h | 0277 1050h |
| 54h | MCAN_IE | Interrupt Enable | 0276 1054h | 0277 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 0276 1058h | 0277 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 0276 105Ch | 0277 105Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 0276 1080h | 0277 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 0276 1084h | 0277 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 0276 1088h | 0277 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 0276 1090h | 0277 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 0276 1094h | 0277 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 0276 1098h | 0277 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 0276 109Ch | 0277 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 0276 10A0h | 0277 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 0276 10A4h | 0277 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 0276 10A8h | 0277 10A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 0276 10ACh | 0277 10ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 0276 10B0h | 0277 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 0276 10B4h | 0277 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 0276 10B8h | 0277 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 0276 10BCh | 0277 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 0276 10C0h | 0277 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 0276 10C4h | 0277 10C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 0276 10C8h | 0277 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 0276 10CCh | 0277 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 0276 10D0h | 0277 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 0276 10D4h | 0277 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 0276 10D8h | 0277 10D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 0276 10DCh | 0277 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 0276 10E0h | 0277 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 0276 10E4h | 0277 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 0276 10F0h | 0277 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 0276 10F4h | 0277 10F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 0276 10F8h | 0277 10F8h |

Table 4-38. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN8_CFG Physical Address | MCAN9_CFG Physical Address |
|--------|-----------------------------|--|----------------------------------|----------------------------------|
| 0h | MCAN_CREL | Core Release Register | 0278 1000h | 0279 1000h |
| 4h | MCAN_ENDN | Endian Register | 0278 1004h | 0279 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 0278 100Ch | 0279 100Ch |
| 10h | MCAN_TEST | Test Register | 0278 1010h | 0279 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 0278 1014h | 0279 1014h |
| 18h | MCAN_CCCR | CC Control Register | 0278 1018h | 0279 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 0278 101Ch | 0279 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 0278 1020h | 0279 1020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 0278 1024h | 0279 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 0278 1028h | 0279 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 0278 102Ch | 0279 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 0278 1040h | 0279 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 0278 1044h | 0279 1044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 0278 1048h | 0279 1048h |
| 50h | MCAN_IR | Interrupt Register | 0278 1050h | 0279 1050h |
| 54h | MCAN_IE | Interrupt Enable | 0278 1054h | 0279 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 0278 1058h | 0279 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 0278 105Ch | 0279 105Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 0278 1080h | 0279 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 0278 1084h | 0279 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 0278 1088h | 0279 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 0278 1090h | 0279 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 0278 1094h | 0279 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 0278 1098h | 0279 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 0278 109Ch | 0279 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 0278 10A0h | 0279 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 0278 10A4h | 0279 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 0278 10A8h | 0279 10A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 0278 10ACh | 0279 10ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 0278 10B0h | 0279 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 0278 10B4h | 0279 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 0278 10B8h | 0279 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 0278 10BCh | 0279 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 0278 10C0h | 0279 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 0278 10C4h | 0279 10C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 0278 10C8h | 0279 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 0278 10CCh | 0279 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 0278 10D0h | 0279 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 0278 10D4h | 0279 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 0278 10D8h | 0279 10D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 0278 10DCh | 0279 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 0278 10E0h | 0279 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 0278 10E4h | 0279 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 0278 10F0h | 0279 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 0278 10F4h | 0279 10F4h |

Table 4-38. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN8_CFG Physical Address | MCAN9_CFG Physical Address |
|--------|----------------------------|---------------------------|----------------------------------|----------------------------------|
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 0278 10F8h | 0279 10F8h |

Table 4-39. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN10_CFG Physical Address | MCAN11_CFG Physical Address |
|--------|----------------------------|---|-----------------------------------|-----------------------------------|
| 0h | MCAN_CREL | Core Release Register | 027A 1000h | 027B 1000h |
| 4h | MCAN_ENDN | Endian Register | 027A 1004h | 027B 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 027A 100Ch | 027B 100Ch |
| 10h | MCAN_TEST | Test Register | 027A 1010h | 027B 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 027A 1014h | 027B 1014h |
| 18h | MCAN_CCCR | CC Control Register | 027A 1018h | 027B 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 027A 101Ch | 027B 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 027A 1020h | 027B 1020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 027A 1024h | 027B 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 027A 1028h | 027B 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 027A 102Ch | 027B 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 027A 1040h | 027B 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 027A 1044h | 027B 1044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 027A 1048h | 027B 1048h |
| 50h | MCAN_IR | Interrupt Register | 027A 1050h | 027B 1050h |
| 54h | MCAN_IE | Interrupt Enable | 027A 1054h | 027B 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 027A 1058h | 027B 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 027A 105Ch | 027B 105Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 027A 1080h | 027B 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 027A 1084h | 027B 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 027A 1088h | 027B 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 027A 1090h | 027B 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 027A 1094h | 027B 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 027A 1098h | 027B 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 027A 109Ch | 027B 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 027A 10A0h | 027B 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 027A 10A4h | 027B 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 027A 10A8h | 027B 10A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 027A 10ACh | 027B 10ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 027A 10B0h | 027B 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 027A 10B4h | 027B 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 027A 10B8h | 027B 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 027A 10BCh | 027B 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 027A 10C0h | 027B 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 027A 10C4h | 027B 10C4h |
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 027A 10C8h | 027B 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 027A 10CCh | 027B 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 027A 10D0h | 027B 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 027A 10D4h | 027B 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 027A 10D8h | 027B 10D8h |

Table 4-39. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN10_CFG Physical Address | MCAN11_CFG Physical Address |
|--------|-----------------------------|--|-----------------------------------|-----------------------------------|
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 027A 10DCh | 027B 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 027A 10E0h | 027B 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 027A 10E4h | 027B 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 027A 10F0h | 027B 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 027A 10F4h | 027B 10F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 027A 10F8h | 027B 10F8h |

Table 4-40. MCAN Core Registers

| Offset | Acronym | Register Name | MCAN12_CFG Physical Address | MCAN13_CFG Physical Address |
|--------|----------------------------|---|-----------------------------------|-----------------------------------|
| 0h | MCAN_CREL | Core Release Register | 027C 1000h | 027D 1000h |
| 4h | MCAN_ENDN | Endian Register | 027C 1004h | 027D 1004h |
| Ch | MCAN_DBTP | Data Bit Timing & Prescaler Register | 027C 100Ch | 027D 100Ch |
| 10h | MCAN_TEST | Test Register | 027C 1010h | 027D 1010h |
| 14h | MCAN_RWD | RAM Watchdog | 027C 1014h | 027D 1014h |
| 18h | MCAN_CCCR | CC Control Register | 027C 1018h | 027D 1018h |
| 1Ch | MCAN_NBTP | Nominal Bit Timing & Prescaler Register | 027C 101Ch | 027D 101Ch |
| 20h | MCAN_TSCC | Timestamp Counter Configuration | 027C 1020h | 027D 1020h |
| 24h | MCAN_TSCV | Timestamp Counter Value | 027C 1024h | 027D 1024h |
| 28h | MCAN_TOCC | Timeout Counter Configuration | 027C 1028h | 027D 1028h |
| 2Ch | MCAN_TOCV | Timeout Counter Value | 027C 102Ch | 027D 102Ch |
| 40h | MCAN_ECR | Error Counter Register | 027C 1040h | 027D 1040h |
| 44h | MCAN_PSR | Protocol Status Register | 027C 1044h | 027D 1044h |
| 48h | MCAN_TDCR | Transmitter Delay Compensation Register | 027C 1048h | 027D 1048h |
| 50h | MCAN_IR | Interrupt Register | 027C 1050h | 027D 1050h |
| 54h | MCAN_IE | Interrupt Enable | 027C 1054h | 027D 1054h |
| 58h | MCAN_ILS | Interrupt Line Select | 027C 1058h | 027D 1058h |
| 5Ch | MCAN_ILE | Interrupt Line Enable | 027C 105Ch | 027D 105Ch |
| 80h | MCAN_GFC | Global Filter Configuration | 027C 1080h | 027D 1080h |
| 84h | MCAN_SIDFC | Standard ID Filter Configuration | 027C 1084h | 027D 1084h |
| 88h | MCAN_XIDFC | Extended ID Filter Configuration | 027C 1088h | 027D 1088h |
| 90h | MCAN_XIDAM | Extended ID AND Mask | 027C 1090h | 027D 1090h |
| 94h | MCAN_HPMS | High Priority Message Status | 027C 1094h | 027D 1094h |
| 98h | MCAN_NDAT1 | New Data 1 | 027C 1098h | 027D 1098h |
| 9Ch | MCAN_NDAT2 | New Data 2 | 027C 109Ch | 027D 109Ch |
| A0h | MCAN_RXF0C | Rx FIFO 0 Configuration | 027C 10A0h | 027D 10A0h |
| A4h | MCAN_RXF0S | Rx FIFO 0 Status | 027C 10A4h | 027D 10A4h |
| A8h | MCAN_RXF0A | Rx FIFO 0 Acknowledge | 027C 10A8h | 027D 10A8h |
| ACh | MCAN_RXBC | Rx Buffer Configuration | 027C 10ACh | 027D 10ACh |
| B0h | MCAN_RXF1C | Rx FIFO 1 Configuration | 027C 10B0h | 027D 10B0h |
| B4h | MCAN_RXF1S | Rx FIFO 1 Status | 027C 10B4h | 027D 10B4h |
| B8h | MCAN_RXF1A | Rx FIFO 1 Acknowledge | 027C 10B8h | 027D 10B8h |
| BCh | MCAN_RXESC | Rx Buffer / FIFO Element Size Configuration | 027C 10BCh | 027D 10BCh |
| C0h | MCAN_TXBC | Tx Buffer Configuration | 027C 10C0h | 027D 10C0h |
| C4h | MCAN_TXFQS | Tx FIFO/Queue Status | 027C 10C4h | 027D 10C4h |

Table 4-40. MCAN Core Registers (continued)

| Offset | Acronym | Register Name | MCAN12_CFG Physical Address | MCAN13_CFG Physical Address |
|--------|-----------------------------|--|-----------------------------------|-----------------------------------|
| C8h | MCAN_TXESC | Tx Buffer Element Size Configuration | 027C 10C8h | 027D 10C8h |
| CCh | MCAN_TXBRP | Tx Buffer Request Pending | 027C 10CCh | 027D 10CCh |
| D0h | MCAN_TXBAR | Tx Buffer Add Request | 027C 10D0h | 027D 10D0h |
| D4h | MCAN_TXBCR | Tx Buffer Cancellation Request | 027C 10D4h | 027D 10D4h |
| D8h | MCAN_TXBTO | Tx Buffer Transmission Occurred | 027C 10D8h | 027D 10D8h |
| DCh | MCAN_TXBCF | Tx Buffer Cancellation Finished | 027C 10DCh | 027D 10DCh |
| E0h | MCAN_TXBTIE | Tx Buffer Transmission Interrupt Enable | 027C 10E0h | 027D 10E0h |
| E4h | MCAN_TXBCIE | Tx Buffer Cancellation Finished Interrupt Enable | 027C 10E4h | 027D 10E4h |
| F0h | MCAN_TXEFC | Tx Event FIFO Configuration | 027C 10F0h | 027D 10F0h |
| F4h | MCAN_TXEFS | Tx Event FIFO Status | 027C 10F4h | 027D 10F4h |
| F8h | MCAN_TXEFA | Tx Event FIFO Acknowledge | 027C 10F8h | 027D 10F8h |

4.2.1 MCAN_CREL Register (Offset = 0h) [reset = 32380608h]

MCAN_CREL is shown in [Figure 4-12](#) and described in [Table 4-42](#).

[Return to Summary Table.](#)

Core Release Register

Release dependent constant (version + date).

Table 4-41. MCAN_CREL Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8000h |
| MCU_MCAN1_CFG | 4056 8000h |
| MCAN0_CFG | 0270 1000h |
| MCAN1_CFG | 0271 1000h |
| MCAN2_CFG | 0272 1000h |
| MCAN3_CFG | 0273 1000h |
| MCAN4_CFG | 0274 1000h |
| MCAN5_CFG | 0275 1000h |
| MCAN6_CFG | 0276 1000h |
| MCAN7_CFG | 0277 1000h |
| MCAN8_CFG | 0278 1000h |
| MCAN9_CFG | 0279 1000h |
| MCAN10_CFG | 027A 1000h |
| MCAN11_CFG | 027B 1000h |
| MCAN12_CFG | 027C 1000h |
| MCAN13_CFG | 027D 1000h |

Figure 4-12. MCAN_CREL Register

| | | | | | | | | | | | | | | | |
|------|----|----|----|------|----|----|----|---------|----|----|----|------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REL | | | | STEP | | | | SUBSTEP | | | | YEAR | | | |
| R-3h | | | | R-2h | | | | R-3h | | | | R-8h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MON | | | | | | | | DAY | | | | | | | |
| R-6h | | | | | | | | R-8h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-42. MCAN_CREL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------|------|-------|---|
| 31-28 | REL | R | 3h | Core Release One digit, BCD-coded. |
| 27-24 | STEP | R | 2h | Step of Core Release One digit, BCD-coded. |
| 23-20 | SUBSTEP | R | 3h | Sub-step of Core Release One digit, BCD-coded. |
| 19-16 | YEAR | R | 8h | Time Stamp Year One digit, BCD-coded. |
| 15-8 | MON | R | 6h | Time Stamp Month Two digits, BCD-coded. |
| 7-0 | DAY | R | 8h | Time Stamp Day Two digits, BCD-coded. |

4.2.2 MCAN_ENDN Register (Offset = 4h) [reset = 8765 4321h]

MCAN_ENDN is shown in [Figure 4-13](#) and described in [Table 4-44](#).

[Return to Summary Table.](#)

Endian Register
Constant 8765 4321h.

Table 4-43. MCAN_ENDN Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8004h |
| MCU_MCAN1_CFG | 4056 8004h |
| MCAN0_CFG | 0270 1004h |
| MCAN1_CFG | 0271 1004h |
| MCAN2_CFG | 0272 1004h |
| MCAN3_CFG | 0273 1004h |
| MCAN4_CFG | 0274 1004h |
| MCAN5_CFG | 0275 1004h |
| MCAN6_CFG | 0276 1004h |
| MCAN7_CFG | 0277 1004h |
| MCAN8_CFG | 0278 1004h |
| MCAN9_CFG | 0279 1004h |
| MCAN10_CFG | 027A 1004h |
| MCAN11_CFG | 027B 1004h |
| MCAN12_CFG | 027C 1004h |
| MCAN13_CFG | 027D 1004h |

Figure 4-13. MCAN_ENDN Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ETV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-8765 4321h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-44. MCAN_ENDN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|------------|---|
| 31-0 | ETV | R | 8765 4321h | Endianness Test Value The endianness test value is 8765 4321h. |

4.2.3 MCAN_DBTP Register (Offset = Ch) [reset = A33h]

MCAN_DBTP is shown in [Figure 4-14](#) and described in [Table 4-46](#).

Return to [Summary Table](#).

Data Bit Timing & Prescaler Register

Configuration of data phase bit timing, transmitter delay compensation enable.

This register is only writable if the MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set. The CAN bit time may be programmed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 MCAN functional clock periods. $t_q = (\text{MCAN_DBTP}[20-16] \text{ DBRP} + 1) \text{ mtq}$ (minimum time quantum = CAN clock period (MCAN functional clock)).

The MCAN_DBTP[12-8] DTSEG1 field is the sum of Prop_Seg and Phase_Seg1. The MCAN_DBTP[7-4] DTSEG2 field is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [MCAN_DBTP[12-8] DTSEG1 + MCAN_DBTP[7-4] DTSEG2 + 3] t_q or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] t_q . The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Note: With a CAN clock (MCAN functional clock) of 8 MHz, the reset value of 0000 0A33h configures the MCAN module for a data phase bit rate of 500 kbit/s.

Note: The bit rate configured for the CAN FD data phase via the MCAN_DBTP register must be higher or equal to the bit rate configured for the arbitration phase via the MCAN_DBTP register.

Table 4-45. MCAN_DBTP Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 800Ch |
| MCU_MCAN1_CFG | 4056 800Ch |
| MCAN0_CFG | 0270 100Ch |
| MCAN1_CFG | 0271 100Ch |
| MCAN2_CFG | 0272 100Ch |
| MCAN3_CFG | 0273 100Ch |
| MCAN4_CFG | 0274 100Ch |
| MCAN5_CFG | 0275 100Ch |
| MCAN6_CFG | 0276 100Ch |
| MCAN7_CFG | 0277 100Ch |
| MCAN8_CFG | 0278 100Ch |
| MCAN9_CFG | 0279 100Ch |
| MCAN10_CFG | 027A 100Ch |
| MCAN11_CFG | 027B 100Ch |
| MCAN12_CFG | 027C 100Ch |
| MCAN13_CFG | 027D 100Ch |

Figure 4-14. MCAN_DBTP Register

| | | | | | | | |
|----------|----------|----|--------|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TDC | RESERVED | | | DBRP | | | |
| R/W-0h | R-0h | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | DTSEG1 | | | | |
| R-0h | | | R/W-Ah | | | | |

Figure 4-14. MCAN_DBTP Register (continued)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|---|---|---|--------|---|---|---|
| DTSEG2 | | | | DSJW | | | |
| R/W-3h | | | | R/W-3h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-46. MCAN_DBTP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved |
| 23 | TDC | R/W | 0h | Transmitter Delay Compensation 0h = Transmitter Delay Compensation disabled 1h = Transmitter Delay Compensation enabled |
| 22-21 | RESERVED | R | 0h | Reserved |
| 20-16 | DBRP | R/W | 0h | Data Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31 (0h-1Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 15-13 | RESERVED | R | 0h | Reserved |
| 12-8 | DTSEG1 | R/W | Ah | Data time segment before sample point Valid values are 0 to 31 (0h-1Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 7-4 | DTSEG2 | R/W | 3h | Data time segment after sample point Valid values are 0 to 15 (0h-Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 3-0 | DSJW | R/W | 3h | Data (Re)Synchronization Jump Width Valid values are 0 to 15 (0h-Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |

4.2.4 MCAN_TEST Register (Offset = 10h) [reset = 0h]

MCAN_TEST is shown in [Figure 4-15](#) and described in [Table 4-48](#).

Return to [Summary Table](#).

Test Register

Test mode selection.

Write access to the MCAN_TEST register has to be enabled by setting the MCAN_CCCR[7] TEST bit. All MCAN_TEST register functions are set to their reset values when the MCAN_CCCR[7] TEST bit is reset.

Loopback Mode and software control of the MCAN TX pin are hardware test modes. Programming of the MCAN_TEST[6-5] TX field \neq 00 may disturb the message transfer on the CAN bus.

Table 4-47. MCAN_TEST Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8010h |
| MCU_MCAN1_CFG | 4056 8010h |
| MCAN0_CFG | 0270 1010h |
| MCAN1_CFG | 0271 1010h |
| MCAN2_CFG | 0272 1010h |
| MCAN3_CFG | 0273 1010h |
| MCAN4_CFG | 0274 1010h |
| MCAN5_CFG | 0275 1010h |
| MCAN6_CFG | 0276 1010h |
| MCAN7_CFG | 0277 1010h |
| MCAN8_CFG | 0278 1010h |
| MCAN9_CFG | 0279 1010h |
| MCAN10_CFG | 027A 1010h |
| MCAN11_CFG | 027B 1010h |
| MCAN12_CFG | 027C 1010h |
| MCAN13_CFG | 027D 1010h |

Figure 4-15. MCAN_TEST Register

| | | | | | | | |
|----------|--------|----|--------|----------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RX | TX | | LBCK | RESERVED | | | |
| R-0h | R/W-0h | | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-48. MCAN_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-8 | RESERVED | R | 0h | Reserved |

Table 4-48. MCAN_TEST Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | RX | R | 0h | Receive Pin Monitors the actual value of the MCAN RX pin 0h = The CAN bus is dominant (MCAN RX = 0h) 1h = The CAN bus is recessive (MCAN RX = 1h) |
| 6-5 | TX | R/W | 0h | Control of Transmit Pin 0h = Reset value, the MCAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time 1h = Sample Point can be monitored at the MCAN TX pin 2h = Dominant ('0') level at the MCAN TX pin 3h = Recessive ('1') at the MCAN TX pin |
| 4 | LBCK | R/W | 0h | Loopback Mode 0h = Reset value, Loopback Mode is disabled 1h = Loopback Mode is enabled (see <i>Test Modes</i>) |
| 3-0 | RESERVED | R | 0h | Reserved |

4.2.5 MCAN_RWD Register (Offset = 14h) [reset = 0h]

MCAN_RWD is shown in [Figure 4-16](#) and described in [Table 4-50](#).

RAM Watchdog

Monitors the READY output of the Message RAM.

The RAM Watchdog monitors the READY output of the Message RAM. A Message RAM access starts the Message RAM Watchdog Counter with the value configured by the MCAN_RWD[7-0] WDC field. The counter is reloaded with the MCAN_RWD[7-0] WDC field when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag MCAN_IR[26] WDI is set. The RAM Watchdog Counter is clocked by the Host clock (MCAN interface clock).

Table 4-49. MCAN_RWD Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8014h |
| MCU_MCAN1_CFG | 4056 8014h |
| MCAN0_CFG | 0270 1014h |
| MCAN1_CFG | 0271 1014h |
| MCAN2_CFG | 0272 1014h |
| MCAN3_CFG | 0273 1014h |
| MCAN4_CFG | 0274 1014h |
| MCAN5_CFG | 0275 1014h |
| MCAN6_CFG | 0276 1014h |
| MCAN7_CFG | 0277 1014h |
| MCAN8_CFG | 0278 1014h |
| MCAN9_CFG | 0279 1014h |
| MCAN10_CFG | 027A 1014h |
| MCAN11_CFG | 027B 1014h |
| MCAN12_CFG | 027C 1014h |
| MCAN13_CFG | 027D 1014h |

Figure 4-16. MCAN_RWD Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|--------|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | WDV | | | | WDC | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | R/W-0h | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-50. MCAN_RWD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15-8 | WDV | R | 0h | Watchdog Value Actual Message RAM Watchdog Counter Value. |
| 7-0 | WDC | R/W | 0h | Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of 0h the counter is disabled. |

4.2.6 MCAN_CCCR Register (Offset = 18h) [reset = 1h]

MCAN_CCCR is shown in [Figure 4-17](#) and described in [Table 4-52](#).

Return to [Summary Table](#).

CC Control Register

Operation mode configuration.

For details about setting and resetting of single bits, see , *Software Initialization*.

Table 4-51. MCAN_CCCR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8018h |
| MCU_MCAN1_CFG | 4056 8018h |
| MCAN0_CFG | 0270 1018h |
| MCAN1_CFG | 0271 1018h |
| MCAN2_CFG | 0272 1018h |
| MCAN3_CFG | 0273 1018h |
| MCAN4_CFG | 0274 1018h |
| MCAN5_CFG | 0275 1018h |
| MCAN6_CFG | 0276 1018h |
| MCAN7_CFG | 0277 1018h |
| MCAN8_CFG | 0278 1018h |
| MCAN9_CFG | 0279 1018h |
| MCAN10_CFG | 027A 1018h |
| MCAN11_CFG | 027B 1018h |
| MCAN12_CFG | 027C 1018h |
| MCAN13_CFG | 027D 1018h |

Figure 4-17. MCAN_CCCR Register

| | | | | | | | |
|----------|--------|--------|--------|----------|--------|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NISO | TXP | EFBI | PXHD | RESERVED | | BRSE | FDOE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEST | DAR | MON | CSR | CSA | ASM | CCE | INIT |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R/W-0h | R/W-0h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-52. MCAN_CCCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15 | NISO | R/W | 0h | Non ISO Operation 0h = CAN FD frame format according to ISO 11898-1:2015. 1h = CAN FD frame format according to Bosch CAN FD Specification 1.0. |

Table 4-52. MCAN_CCCR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 14 | TXP | R/W | 0h | Transmit Pause If this bit is set, the MCAN module pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see <i>Tx Handling</i>) . 0h = Transmit pause disabled 1h = Transmit pause enabled |
| 13 | EFBI | R/W | 0h | Edge Filtering during Bus Integration 0h = Edge filtering disabled 1h = Two consecutive dominant t_q required to detect an edge for hard synchronization |
| 12 | PXHD | R/W | 0h | Protocol Exception Handling Disable 0h = Protocol exception handling enabled 1h = Protocol exception handling disabled Note: When protocol exception handling is disabled, the MCAN module will transmit an error frame when it detects a protocol exception condition. |
| 11-10 | RESERVED | R | 0h | Reserved |
| 9 | BRSE | R/W | 0h | Bit Rate Switch Enable 0h = Bit rate switching for transmissions disabled 1h = Bit rate switching for transmissions enabled Note: When CAN FD operation is disabled the MCAN_CCCR[8] FDOE = 0h, the MCAN_CCCR[9] BRSE bit is not evaluated. |
| 8 | FDOE | R/W | 0h | FD Operation Enable 0h = FD operation disabled 1h = FD operation enabled |
| 7 | TEST | R/W | 0h | Test Mode Enable 0h = Normal operation. The MCAN_TEST register holds reset values. 1h = Test Mode. Write access to the MCAN_TEST register enabled. |
| 6 | DAR | R/W | 0h | Disable Automatic Retransmission 0h = Automatic retransmission of messages not transmitted successfully enabled 1h = Automatic retransmission disabled |
| 5 | MON | R/W | 0h | Bus Monitoring Mode The MCAN_CCCR[5] MON bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time. 0h = Bus Monitoring Mode is disabled 1h = Bus Monitoring Mode is enabled |
| 4 | CSR | R/W | 0h | Clock Stop Request 0h = No clock stop is requested 1h = Clock stop requested. When clock stop is requested, first the MCAN_CCCR[0] INIT bit and then the MCAN_CCCR[3] CSA bit will be set after all pending transfer requests have been completed and the CAN bus reached idle. |
| 3 | CSA | R | 0h | Clock Stop Acknowledge 0h = No clock stop acknowledged 1h = The MCAN module may be set in power down by stopping MCAN interface clock and MCAN functional clock |

Table 4-52. MCAN_CCCR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 2 | ASM | R/W | 0h | <p>Restricted Operation Mode</p> <p>The MCAN_CCCR[2] ASM bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time.</p> <p>For a description of the Restricted Operation Mode, see <i>Restricted Operation Mode</i>.</p> <p>0h = Normal CAN operation 1h = Restricted Operation Mode active</p> |
| 1 | CCE | R/W | 0h | <p>Configuration Change Enable</p> <p>0h = The Host CPU has no write access to the protected configuration registers 1h = The Host CPU has write access to the protected configuration registers (while the MCAN_CCCR[0] INIT = 1h)</p> |
| 0 | INIT | R/W | 1h | <p>Initialization</p> <p>0h = Normal Operation 1h = Initialization is started</p> <p>Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to the MCAN_CCCR[0] INIT bit can be read back. Therefore the software has to assure that the previous value written to the MCAN_CCCR[0] INIT bit has been accepted by reading the MCAN_CCCR[0] INIT bit before setting the MCAN_CCCR[0] INIT bit to a new value.</p> |

4.2.7 MCAN_NBTP Register (Offset = 1Ch) [reset = 06000A03h]

MCAN_NBTP is shown in [Figure 4-18](#) and described in [Table 4-54](#).

Return to [Summary Table](#).

Nominal Bit Timing & Prescaler Register
Configuration of arbitration phase bit timing.

This register is only writable if the MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set. The CAN bit time may be programmed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 MCAN functional clock periods. $t_q = (\text{MCAN_NBTP}[24-16] \text{ NBRP} + 1) \text{ mtq}$. The MCAN_NBTP[15-8] NTSEG1 field is the sum of Prop_Seg and Phase_Seg1. The MCAN_NBTP[6-0] NTSEG2 field is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [MCAN_NBTP[15-8] NTSEG1 + MCAN_NBTP[6-0] NTSEG2 + 3] t_q or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] t_q .

The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Table 4-53. MCAN_NBTP Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 801Ch |
| MCU_MCAN1_CFG | 4056 801Ch |
| MCAN0_CFG | 0270 101Ch |
| MCAN1_CFG | 0271 101Ch |
| MCAN2_CFG | 0272 101Ch |
| MCAN3_CFG | 0273 101Ch |
| MCAN4_CFG | 0274 101Ch |
| MCAN5_CFG | 0275 101Ch |
| MCAN6_CFG | 0276 101Ch |
| MCAN7_CFG | 0277 101Ch |
| MCAN8_CFG | 0278 101Ch |
| MCAN9_CFG | 0279 101Ch |
| MCAN10_CFG | 027A 101Ch |
| MCAN11_CFG | 027B 101Ch |
| MCAN12_CFG | 027C 101Ch |
| MCAN13_CFG | 027D 101Ch |

Figure 4-18. MCAN_NBTP Register

| | | | | | | | |
|----------|--------|----|----|----|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NSJW | | | | | | NBRP | |
| R/W-3h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NBRP | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NTSEG1 | | | | | | | |
| R/W-Ah | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | NTSEG2 | | | | | | |
| R-0h | R/W-3h | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-54. MCAN_NBTP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-25 | NSJW | R/W | 3h | Nominal (Re)Synchronization Jump Width Valid values are 0 to 127 (0h-7Fh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 24-16 | NBRP | R/W | 0h | Nominal Baud Rate Prescaler The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 511 (0h-1FFh). The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 15-8 | NTSEG1 | R/W | Ah | Nominal Time segment before sample point Valid values are 1 to 255 (1h-FFh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. |
| 7 | RESERVED | R | 0h | Reserved |
| 6-0 | NTSEG2 | R/W | 3h | Nominal Time segment after sample point Valid values are 0 to 127 (0h-7Fh). The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Note: With a CAN clock (MCAN functional clock) of 8 MHz, the reset value of 0600 0A03h configures the MCAN module for a bit rate of 500 kbit/s. |

4.2.8 MCAN_TSCC Register (Offset = 20h) [reset = 0h]

MCAN_TSCC is shown in [Figure 4-19](#) and described in [Table 4-56](#).

Return to [Summary Table](#).

Timestamp Counter Configuration

Timestamp counter prescaler setting, selection of internal/external timestamp vector.

For a description of the Timestamp Counter, see , *Timestamp Generation*.

Table 4-55. MCAN_TSCC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8020h |
| MCU_MCAN1_CFG | 4056 8020h |
| MCAN0_CFG | 0270 1020h |
| MCAN1_CFG | 0271 1020h |
| MCAN2_CFG | 0272 1020h |
| MCAN3_CFG | 0273 1020h |
| MCAN4_CFG | 0274 1020h |
| MCAN5_CFG | 0275 1020h |
| MCAN6_CFG | 0276 1020h |
| MCAN7_CFG | 0277 1020h |
| MCAN8_CFG | 0278 1020h |
| MCAN9_CFG | 0279 1020h |
| MCAN10_CFG | 027A 1020h |
| MCAN11_CFG | 027B 1020h |
| MCAN12_CFG | 027C 1020h |
| MCAN13_CFG | 027D 1020h |

Figure 4-19. MCAN_TSCC Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|--------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | TCP | | | |
| R-0h | | | | | | | | | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | TSS | | |
| R-0h | | | | | | | | | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-56. MCAN_TSCC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-20 | RESERVED | R | 0h | Reserved |
| 19-16 | TCP | R/W | 0h | Timestamp Counter Prescaler Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1-16 (0h-Fh)]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Note: With CAN FD an external counter is required for timestamp generation (MCAN_TSCC[1-0] TSS = 2h) |
| 15-2 | RESERVED | R | 0h | Reserved |

Table 4-56. MCAN_TSCC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 1-0 | TSS | R/W | 0h | Timestamp Select 0h = Timestamp counter value always 0h 1h = Timestamp counter value incremented according to the MCAN_TSCC[19-16] TCP field 2h = External timestamp counter value used 3h = Same as 0h |

4.2.9 MCAN_TSCV Register (Offset = 24h) [reset = 0h]

MCAN_TSCV is shown in [Figure 4-20](#) and described in [Table 4-58](#).

Return to [Summary Table](#).

Timestamp Counter Value

Read/reset timestamp counter.

Table 4-57. MCAN_TSCV Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8024h |
| MCU_MCAN1_CFG | 4056 8024h |
| MCAN0_CFG | 0270 1024h |
| MCAN1_CFG | 0271 1024h |
| MCAN2_CFG | 0272 1024h |
| MCAN3_CFG | 0273 1024h |
| MCAN4_CFG | 0274 1024h |
| MCAN5_CFG | 0275 1024h |
| MCAN6_CFG | 0276 1024h |
| MCAN7_CFG | 0277 1024h |
| MCAN8_CFG | 0278 1024h |
| MCAN9_CFG | 0279 1024h |
| MCAN10_CFG | 027A 1024h |
| MCAN11_CFG | 027B 1024h |
| MCAN12_CFG | 027C 1024h |
| MCAN13_CFG | 027D 1024h |

Figure 4-20. MCAN_TSCV Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | TSC | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | RWTC-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; RWTC = Read/Write to Clear Field; -n = value after reset

Table 4-58. MCAN_TSCV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15-0 | TSC | RWTC | 0h | <p>Timestamp Counter</p> <p>The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx).</p> <p>When the MCAN_TSCC[1-0] TSS = 1h, the Timestamp Counter is incremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. A wrap around sets interrupt flag MCAN_IR[16] TSW.</p> <p>Write access resets the counter to zero. When the MCAN_TSCC[1-0] TSS = 2h, the MCAN_TSCV[15-0] TSC field reflects the external Timestamp Counter value. A write access has no impact.</p> <p>Note: A 'wrap around' is a change of the Timestamp Counter value from non-zero to zero not caused by write access to the MCAN_TSCV register.</p> |

4.2.10 MCAN_TOCC Register (Offset = 28h) [reset = FFFF0000h]

MCAN_TOCC is shown in [Figure 4-21](#) and described in [Table 4-60](#).

Return to [Summary Table](#).

Timeout Counter Configuration

Configuration of timeout period, selection of timeout counter operation mode.

For a description of the Timeout Counter, see , *Timeout Counter*.

Table 4-59. MCAN_TOCC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8028h |
| MCU_MCAN1_CFG | 4056 8028h |
| MCAN0_CFG | 0270 1028h |
| MCAN1_CFG | 0271 1028h |
| MCAN2_CFG | 0272 1028h |
| MCAN3_CFG | 0273 1028h |
| MCAN4_CFG | 0274 1028h |
| MCAN5_CFG | 0275 1028h |
| MCAN6_CFG | 0276 1028h |
| MCAN7_CFG | 0277 1028h |
| MCAN8_CFG | 0278 1028h |
| MCAN9_CFG | 0279 1028h |
| MCAN10_CFG | 027A 1028h |
| MCAN11_CFG | 027B 1028h |
| MCAN12_CFG | 027C 1028h |
| MCAN13_CFG | 027D 1028h |

Figure 4-21. MCAN_TOCC Register

| | | | | | | | |
|-----------|----|----|----|----|--------|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TOP | | | | | | | |
| R/W-FFFFh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TOP | | | | | | | |
| R/W-FFFFh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | TOS | | ETOC |
| R-0h | | | | | R/W-0h | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-60. MCAN_TOCC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | TOP | R/W | FFFFh | Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. |
| 15-3 | RESERVED | R | 0h | Reserved |

Table 4-60. MCAN_TOCC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 2-1 | TOS | R/W | 0h | <p>Timeout Select</p> <p>When operating in Continuous mode, a write to the MCAN_TOCV[15-0] TOC field presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored.</p> <p>0h = Continuous operation 1h = Timeout controlled by Tx Event FIFO 2h = Timeout controlled by Rx FIFO 0 3h = Timeout controlled by Rx FIFO 1</p> |
| 0 | ETOC | R/W | 0h | <p>Enable Timeout Counter</p> <p>0h = Timeout Counter disabled 1h = Timeout Counter enabled</p> |

4.2.11 MCAN_TOCV Register (Offset = 2Ch) [reset = FFFFh]

MCAN_TOCV is shown in [Figure 4-22](#) and described in [Table 4-62](#).

Return to [Summary Table](#).

Timeout Counter Value
Read/reset timeout counter.

Table 4-61. MCAN_TOCV Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 802Ch |
| MCU_MCAN1_CFG | 4056 802Ch |
| MCAN0_CFG | 0270 102Ch |
| MCAN1_CFG | 0271 102Ch |
| MCAN2_CFG | 0272 102Ch |
| MCAN3_CFG | 0273 102Ch |
| MCAN4_CFG | 0274 102Ch |
| MCAN5_CFG | 0275 102Ch |
| MCAN6_CFG | 0276 102Ch |
| MCAN7_CFG | 0277 102Ch |
| MCAN8_CFG | 0278 102Ch |
| MCAN9_CFG | 0279 102Ch |
| MCAN10_CFG | 027A 102Ch |
| MCAN11_CFG | 027B 102Ch |
| MCAN12_CFG | 027C 102Ch |
| MCAN13_CFG | 027D 102Ch |

Figure 4-22. MCAN_TOCV Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | TOC | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | RWTC-FFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; RWTC = Read/Write to Clear Field; -n = value after reset

Table 4-62. MCAN_TOCV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15-0 | TOC | RWTC | FFFFh | Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. When decremented to zero, interrupt flag MCAN_IR[18] TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via the MCAN_TOCC[2-1] TOS field. |

4.2.12 MCAN_ECR Register (Offset = 40h) [reset = 0h]

MCAN_ECR is shown in [Figure 4-23](#) and described in [Table 4-64](#).

Return to [Summary Table](#).

Error Counter Register

State of Rx/Tx Error Counter, CAN Error Logging.

Table 4-63. MCAN_ECR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8040h |
| MCU_MCAN1_CFG | 4056 8040h |
| MCAN0_CFG | 0270 1040h |
| MCAN1_CFG | 0271 1040h |
| MCAN2_CFG | 0272 1040h |
| MCAN3_CFG | 0273 1040h |
| MCAN4_CFG | 0274 1040h |
| MCAN5_CFG | 0275 1040h |
| MCAN6_CFG | 0276 1040h |
| MCAN7_CFG | 0277 1040h |
| MCAN8_CFG | 0278 1040h |
| MCAN9_CFG | 0279 1040h |
| MCAN10_CFG | 027A 1040h |
| MCAN11_CFG | 027B 1040h |
| MCAN12_CFG | 027C 1040h |
| MCAN13_CFG | 027D 1040h |

Figure 4-23. MCAN_ECR Register

| | | | | | | | | | | | | | | | |
|----------|----|------|----|----|----|----|----|------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | CEL | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RP | | REC | | | | | | TEC | | | | | | | |
| R-0h | | R-0h | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-64. MCAN_ECR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved |
| 23-16 | CEL | R | 0h | CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to the MCAN_ECR[23-16] CEL field. The counter stops at FFh; the next increment of the MCAN_ECR[7-0] TEC or MCAN_ECR[14-8] REC fields sets interrupt flag MCAN_IR[22] ELO. |
| 15 | RP | R | 0h | Receive Error Passive 0h = The Receive Error Counter is below the error passive level of 128 1h = The Receive Error Counter has reached the error passive level of 128 |

Table 4-64. MCAN_ECR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 14-8 | REC | R | 0h | Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127. |
| 7-0 | TEC | R | 0h | Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255. Note: When the MCAN_CCCR[2] ASM bit is set, the CAN protocol controller does not increment the MCAN_ECR[7-0] TEC and MCAN_ECR[14-8] REC fields when a CAN protocol error is detected, but the MCAN_ECR[23-16] CEL field is still incremented. |

4.2.13 MCAN_PSR Register (Offset = 44h) [reset = 707h]

MCAN_PSR is shown in [Figure 4-24](#) and described in [Table 4-66](#).

Return to [Summary Table](#).

Protocol Status Register

CAN protocol controller status, transmitter delay compensation value.

Table 4-65. MCAN_PSR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8044h |
| MCU_MCAN1_CFG | 4056 8044h |
| MCAN0_CFG | 0270 1044h |
| MCAN1_CFG | 0271 1044h |
| MCAN2_CFG | 0272 1044h |
| MCAN3_CFG | 0273 1044h |
| MCAN4_CFG | 0274 1044h |
| MCAN5_CFG | 0275 1044h |
| MCAN6_CFG | 0276 1044h |
| MCAN7_CFG | 0277 1044h |
| MCAN8_CFG | 0278 1044h |
| MCAN9_CFG | 0279 1044h |
| MCAN10_CFG | 027A 1044h |
| MCAN11_CFG | 027B 1044h |
| MCAN12_CFG | 027C 1044h |
| MCAN13_CFG | 027D 1044h |

Figure 4-24. MCAN_PSR Register

| | | | | | | | |
|----------|------|------|------|------|------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | TDCV | | | | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | PXE | RFDF | RBRS | RESI | DLEC | | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-7h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BO | EW | EP | ACT | | LEC | | |
| R-0h | R-0h | R-0h | R-0h | | R-7h | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-66. MCAN_PSR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-23 | RESERVED | R | 0h | Reserved |

Table 4-66. MCAN_PSR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 22-16 | TDCV | R | 0h | Transmitter Delay Compensation Value Position of the secondary sample point, defined by the sum of the measured delay from the MCAN TX to MCAN RX pins and the MCAN_TDCR[14-8] TDCO field. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq (0h-7Fh). |
| 15 | RESERVED | R | 0h | Reserved |
| 14 | PXE | R | 0h | Protocol Exception Event 0h = No protocol exception event occurred since last read access 1h = Protocol exception event occurred |
| 13 | RFDF | R | 0h | Received a CAN FD Message This bit is set independent of acceptance filtering. 0h = Since this bit was reset by the Host CPU, no CAN FD message has been received 1h = Message in CAN FD format with FDF flag set has been received |
| 12 | RBRS | R | 0h | BRS flag of last received CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. 0h = Last received CAN FD message did not have its BRS flag set 1h = Last received CAN FD message had its BRS flag set |
| 11 | RESI | R | 0h | ESI flag of last received CAN FD Message This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering. 0h = Last received CAN FD message did not have its ESI flag set 1h = Last received CAN FD message had its ESI flag set |
| 10-8 | DLEC | R | 7h | Data Phase Last Error Code Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for the MCAN_PSR[2-0] LEC field. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. |
| 7 | BO | R | 0h | Bus_Off Status 0h = The MCAN module is not Bus_Off 1h = The MCAN module is in Bus_Off state |
| 6 | EW | R | 0h | Warning Status 0h = Both error counters are below the Error_Warning limit of 96 1h = At least one of error counter has reached the Error_Warning limit of 96 |
| 5 | EP | R | 0h | Error Passive 0h = The MCAN module is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1h = The MCAN module is in the Error_Passive state |

Table 4-66. MCAN_PSR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 4-3 | ACT | R | 0h | <p>Activity</p> <p>Monitors the module's CAN communication state.</p> <p>0h = Synchronizing - node is synchronizing on CAN communication</p> <p>1h = Idle - node is neither receiver nor transmitter</p> <p>2h = Receiver - node is operating as receiver</p> <p>3h = Transmitter - node is operating as transmitter</p> <p>Note: ACT is set to 0h by a Protocol Exception Event.</p> |
| 2-0 | LEC | R | 7h | <p>Last Error Code</p> <p>The MCAN_PSR[2-0] LEC field indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0h when a message has been transferred (reception or transmission) without error.</p> <p>0h = No Error: No error occurred since the MCAN_PSR[2-0] LEC field has been reset by successful reception or transmission.</p> <p>1h = Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.</p> <p>2h = Form Error: A fixed format part of a received frame has the wrong format.</p> <p>3h = AckError: The message transmitted by the MCAN module was not acknowledged by another node.</p> <p>4h = Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.</p> <p>5h = Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the Host CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).</p> <p>6h = CRCErrror: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.</p> <p>7h = NoChange: Any read access to the Protocol Status Register re-initializes the MCAN_PSR[2-0] LEC field to 7h. When the MCAN_PSR[2-0] LEC field shows the value 7h, no CAN bus event was detected since the last Host CPU read access to the Protocol Status Register.</p> <p>Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in the MCAN_PSR[10-8] DLEC field instead of the MCAN_PSR[2-0] LEC field. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.</p> |

4.2.14 MCAN_TDCR Register (Offset = 48h) [reset = 0h]

MCAN_TDCR is shown in [Figure 4-25](#) and described in [Table 4-68](#).

Return to [Summary Table](#).

Transmitter Delay Comensation Register

Configuration of transmitter delay compensation offset and filter window length.

Table 4-67. MCAN_TDCR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8048h |
| MCU_MCAN1_CFG | 4056 8048h |
| MCAN0_CFG | 0270 1048h |
| MCAN1_CFG | 0271 1048h |
| MCAN2_CFG | 0272 1048h |
| MCAN3_CFG | 0273 1048h |
| MCAN4_CFG | 0274 1048h |
| MCAN5_CFG | 0275 1048h |
| MCAN6_CFG | 0276 1048h |
| MCAN7_CFG | 0277 1048h |
| MCAN8_CFG | 0278 1048h |
| MCAN9_CFG | 0279 1048h |
| MCAN10_CFG | 027A 1048h |
| MCAN11_CFG | 027B 1048h |
| MCAN12_CFG | 027C 1048h |
| MCAN13_CFG | 027D 1048h |

Figure 4-25. MCAN_TDCR Register

| | | | | | | | |
|----------|--------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | TDCO | | | | | | |
| R-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | TDCF | | | | | | |
| R-0h | R/W-0h | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-68. MCAN_TDCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-15 | RESERVED | R | 0h | Reserved |
| 14-8 | TDCO | R/W | 0h | Transmitter Delay Compensation Offset Offset value defining the distance between the measured delay from the MCAN RX and MCAN TX pins and the secondary sample point. Valid values are 0 to 127 mtq (0h-7Fh). |
| 7 | RESERVED | R | 0h | Reserved |

Table 4-68. MCAN_TDCR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 6-0 | TDCF | R/W | 0h | Transmitter Delay Compensation Filter Window Length Defines the minimum value for the SSP position, dominant edges on the MCAN RX pin that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when the MCAN_TDCR[6-0] TDCF field is configured to a value greater than the MCAN_TDCR[14-8] TDCO field. Valid values are 0 to 127 mtq (0h-7Fh). |

4.2.15 MCAN_IR Register (Offset = 50h) [reset = 0h]

MCAN_IR is shown in [Figure 4-26](#) and described in [Table 4-70](#).

[Return to Summary Table.](#)

Interrupt Register

The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host CPU clears them. A flag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register. The configuration of the MCAN_IE register controls whether an interrupt is generated. The configuration of the MCAN_ILS register controls on which interrupt line an interrupt is signalled.

Table 4-69. MCAN_IR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8050h |
| MCU_MCAN1_CFG | 4056 8050h |
| MCAN0_CFG | 0270 1050h |
| MCAN1_CFG | 0271 1050h |
| MCAN2_CFG | 0272 1050h |
| MCAN3_CFG | 0273 1050h |
| MCAN4_CFG | 0274 1050h |
| MCAN5_CFG | 0275 1050h |
| MCAN6_CFG | 0276 1050h |
| MCAN7_CFG | 0277 1050h |
| MCAN8_CFG | 0278 1050h |
| MCAN9_CFG | 0279 1050h |
| MCAN10_CFG | 027A 1050h |
| MCAN11_CFG | 027B 1050h |
| MCAN12_CFG | 027C 1050h |
| MCAN13_CFG | 027D 1050h |

Figure 4-26. MCAN_IR Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RESERVED | | ARA | PED | PEA | WDI | BO | EW |
| R-0h | | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EP | ELO | BEU | RESERVED | DRX | TOO | MRAF | TSW |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | R-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TEFL | TEFF | TEFW | TEFN | TFE | TCF | TC | HPM |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RF1L | RF1F | RF1W | RF1N | RF0L | RF0F | RF0W | RF0N |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |

LEGEND: R = Read Only; RW1TC = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-70. MCAN_IR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-30 | RESERVED | R | 0h | Reserved |

Table 4-70. MCAN_IR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|-------|-------|---|
| 29 | ARA | RW1TC | 0h | Access to Reserved Address 0h = No access to reserved address occurred 1h = Access to reserved address occurred |
| 28 | PED | RW1TC | 0h | Protocol Error in Data Phase 0h = No protocol error in data phase 1h = Protocol error in data phase detected (MCAN_PSR[10-8] DLEC \neq 0.7) |
| 27 | PEA | RW1TC | 0h | Protocol Error in Arbitration Phase 0h = No protocol error in arbitration phase 1h = Protocol error in arbitration phase detected (MCAN_PSR[2-0] LEC \neq 0.7) |
| 26 | WDI | RW1TC | 0h | Watchdog Interrupt 0h = No Message RAM Watchdog event occurred 1h = Message RAM Watchdog event due to missing READY |
| 25 | BO | RW1TC | 0h | Bus_Off Status 0h = Bus_Off status unchanged 1h = Bus_Off status changed |
| 24 | EW | RW1TC | 0h | Warning Status 0h = Error_Warning status unchanged 1h = Error_Warning status changed |
| 23 | EP | RW1TC | 0h | Error Passive 0h = Error_Passive status unchanged 1h = Error_Passive status changed |
| 22 | ELO | RW1TC | 0h | Error Logging Overflow 0h = CAN Error Logging Counter did not overflow 1h = Overflow of CAN Error Logging Counter occurred |
| 21 | BEU | RW1TC | 0h | Bit Error Uncorrected Message RAM bit error detected, uncorrected. Controlled by input signal generated by parity/ECC logic attached to the Message RAM. An uncorrected Message RAM bit error sets the MCAN_CCCR[0] INIT bit to 1. This is done to avoid transmission of corrupted data. 0h = No bit error detected when reading from Message RAM 1h = Bit error detected, uncorrected (example: parity logic) |
| 20 | RESERVED | R | 0h | Reserved |
| 19 | DRX | RW1TC | 0h | Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0h = No Rx Buffer updated 1h = At least one received message stored into an Rx Buffer |
| 18 | TOO | RW1TC | 0h | Timeout Occurred 0h = No timeout 1h = Timeout reached |

Table 4-70. MCAN_IR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|--|
| 17 | MRAF | RW1TC | 0h | <p>Message RAM Access Failure</p> <p>The flag is set, when the Rx Handler:</p> <ul style="list-style-type: none"> a) has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. b) was not able to write a message to the Message RAM. In this case message storage is aborted. <p>In both cases the FIFO put index is not updated respectively the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location.</p> <p>The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN module is switched into Restricted Operation Mode (see <i>Restricted Operation Mode</i>). To leave Restricted Operation Mode, the Host CPU has to reset the MCAN_CCCR[2] ASM bit.</p> <p>0h = No Message RAM access failure occurred 1h = Message RAM access failure occurred</p> |
| 16 | TSW | RW1TC | 0h | <p>Timestamp Wraparound</p> <p>0h = No timestamp counter wrap-around 1h = Timestamp counter wrapped around</p> |
| 15 | TEFL | RW1TC | 0h | <p>Tx Event FIFO Element Lost</p> <p>0h = No Tx Event FIFO element lost 1h = Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero</p> |
| 14 | TEFF | RW1TC | 0h | <p>Tx Event FIFO Full</p> <p>0h = Tx Event FIFO not full 1h = Tx Event FIFO full</p> |
| 13 | TEFW | RW1TC | 0h | <p>Tx Event FIFO Watermark Reached</p> <p>0h = Tx Event FIFO fill level below watermark 1h = Tx Event FIFO fill level reached watermark</p> |
| 12 | TEFN | RW1TC | 0h | <p>Tx Event FIFO New Entry</p> <p>0h = Tx Event FIFO unchanged 1h = Tx Handler wrote Tx Event FIFO element</p> |
| 11 | TFE | RW1TC | 0h | <p>Tx FIFO Empty</p> <p>0h = Tx FIFO non-empty 1h = Tx FIFO empty</p> |
| 10 | TCF | RW1TC | 0h | <p>Transmission Cancellation Finished</p> <p>0h = No transmission cancellation finished 1h = Transmission cancellation finished</p> |
| 9 | TC | RW1TC | 0h | <p>Transmission Completed</p> <p>0h = No transmission completed 1h = Transmission completed</p> |
| 8 | HPM | RW1TC | 0h | <p>High Priority Message</p> <p>0h = No high priority message received 1h = High priority message received</p> |

Table 4-70. MCAN_IR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 7 | RF1L | RW1TC | 0h | Rx FIFO 1 Message Lost 0h = No Rx FIFO 1 message lost 1h = Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero |
| 6 | RF1F | RW1TC | 0h | Rx FIFO 1 Full 0h = Rx FIFO 1 not full 1h = Rx FIFO 1 full |
| 5 | RF1W | RW1TC | 0h | Rx FIFO 1 Watermark Reached 0h = Rx FIFO 1 fill level below watermark 1h = Rx FIFO 1 fill level reached watermark |
| 4 | RF1N | RW1TC | 0h | Rx FIFO 1 New Message 0h = No new message written to Rx FIFO 1 1h = New message written to Rx FIFO 1 |
| 3 | RF0L | RW1TC | 0h | Rx FIFO 0 Message Lost 0h = No Rx FIFO 0 message lost 1h = Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero |
| 2 | RF0F | RW1TC | 0h | Rx FIFO 0 Full 0h = Rx FIFO 0 not full 1h = Rx FIFO 0 full |
| 1 | RF0W | RW1TC | 0h | Rx FIFO 0 Watermark Reached 0h = Rx FIFO 0 fill level below watermark 1h = Rx FIFO 0 fill level reached watermark |
| 0 | RF0N | RW1TC | 0h | Rx FIFO 0 New Message 0h = No new message written to Rx FIFO 0 1h = New message written to Rx FIFO 0 |

4.2.16 MCAN_IE Register (Offset = 54h) [reset = 0h]

MCAN_IE is shown in [Figure 4-27](#) and described in [Table 4-72](#).

Return to [Summary Table](#).

Interrupt Enable

The settings in the Interrupt Enable register determine which status changes in the MCAN_IR register are signalled on an interrupt line.

Table 4-71. MCAN_IE Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8054h |
| MCU_MCAN1_CFG | 4056 8054h |
| MCAN0_CFG | 0270 1054h |
| MCAN1_CFG | 0271 1054h |
| MCAN2_CFG | 0272 1054h |
| MCAN3_CFG | 0273 1054h |
| MCAN4_CFG | 0274 1054h |
| MCAN5_CFG | 0275 1054h |
| MCAN6_CFG | 0276 1054h |
| MCAN7_CFG | 0277 1054h |
| MCAN8_CFG | 0278 1054h |
| MCAN9_CFG | 0279 1054h |
| MCAN10_CFG | 027A 1054h |
| MCAN11_CFG | 027B 1054h |
| MCAN12_CFG | 027C 1054h |
| MCAN13_CFG | 027D 1054h |

Figure 4-27. MCAN_IE Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|--------|--------|--------|--------|--------|--------|--------|
| RESERVED | | ARAE | PEDE | PEAE | WDIE | BOE | EWE |
| R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EPE | ELOE | BEUE | BECE | DRX | TOOE | MRAFE | TSWE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TEFLE | TEFFE | TEFWE | TEFNE | TFEE | TCFE | TCE | HPME |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RF1LE | RF1FE | RF1WE | RF1NE | RF0LE | RF0FE | RF0WE | RF0NE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-72. MCAN_IE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-30 | RESERVED | R | 0h | Reserved |
| 29 | ARAE | R/W | 0h | Access to Reserved Address Enable 0h = Interrupt disabled 1h = Interrupt enabled |

Table 4-72. MCAN_IE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 28 | PEDE | R/W | 0h | Protocol Error in Data Phase Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 27 | PEAE | R/W | 0h | Protocol Error in Arbitration Phase Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 26 | WDIE | R/W | 0h | Watchdog Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 25 | BOE | R/W | 0h | Bus_Off Status Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 24 | EWE | R/W | 0h | Warning Status Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 23 | EPE | R/W | 0h | Error Passive Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 22 | ELOE | R/W | 0h | Error Logging Overflow Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 21 | BEUE | R/W | 0h | Bit Error Uncorrected Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 20 | BECE | R/W | 0h | Bit Error Corrected Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 19 | DRX | R/W | 0h | Message stored to Dedicated Rx Buffer Interrupt Enable |
| 18 | TOOE | R/W | 0h | Timeout Occurred Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 17 | MRAFE | R/W | 0h | Message RAM Access Failure Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 16 | TSWE | R/W | 0h | Timestamp Wraparound Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 15 | TEFLE | R/W | 0h | Tx Event FIFO Event Lost Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 14 | TEFFE | R/W | 0h | Tx Event FIFO Full Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 13 | TEFWE | R/W | 0h | Tx Event FIFO Watermark Reached Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |

Table 4-72. MCAN_IE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 12 | TEFNE | R/W | 0h | Tx Event FIFO New Entry Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 11 | TFEE | R/W | 0h | Tx FIFO Empty Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 10 | TCFE | R/W | 0h | Transmission Cancellation Finished Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 9 | TCE | R/W | 0h | Transmission Completed Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 8 | HPME | R/W | 0h | High Priority Message Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 7 | RF1LE | R/W | 0h | Rx FIFO 1 Message Lost Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 6 | RF1FE | R/W | 0h | Rx FIFO 1 Full Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 5 | RF1WE | R/W | 0h | Rx FIFO 1 Watermark Reached Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 4 | RF1NE | R/W | 0h | Rx FIFO 1 New Message Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 3 | RF0LE | R/W | 0h | Rx FIFO 0 Message Lost Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 2 | RF0FE | R/W | 0h | Rx FIFO 0 Full Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 1 | RF0WE | R/W | 0h | Rx FIFO 0 Watermark Reached Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |
| 0 | RF0NE | R/W | 0h | Rx FIFO 0 New Message Interrupt Enable 0h = Interrupt disabled 1h = Interrupt enabled |

4.2.17 MCAN_ILS Register (Offset = 58h) [reset = 0h]

MCAN_ILS is shown in [Figure 4-28](#) and described in [Table 4-74](#).

Return to [Summary Table](#).

Interrupt Line Select

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the MCAN_IR register to one of the two module interrupt lines. For interrupt generation the respective interrupt line has to be enabled via the MCAN_ILE[0] EINT0 and MCAN_ILE[1] EINT1 bits.

Table 4-73. MCAN_ILS Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8058h |
| MCU_MCAN1_CFG | 4056 8058h |
| MCAN0_CFG | 0270 1058h |
| MCAN1_CFG | 0271 1058h |
| MCAN2_CFG | 0272 1058h |
| MCAN3_CFG | 0273 1058h |
| MCAN4_CFG | 0274 1058h |
| MCAN5_CFG | 0275 1058h |
| MCAN6_CFG | 0276 1058h |
| MCAN7_CFG | 0277 1058h |
| MCAN8_CFG | 0278 1058h |
| MCAN9_CFG | 0279 1058h |
| MCAN10_CFG | 027A 1058h |
| MCAN11_CFG | 027B 1058h |
| MCAN12_CFG | 027C 1058h |
| MCAN13_CFG | 027D 1058h |

Figure 4-28. MCAN_ILS Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|--------|--------|--------|--------|--------|--------|--------|
| RESERVED | | ARAL | PEDL | PEAL | WDIL | BOL | EWL |
| R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EPL | ELOL | BEUL | BECL | DRXL | TOOL | MRAFL | TSWL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TEFLL | TEFFL | TEFWL | TEFNL | TFEL | TCFL | TCL | HPML |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RF1LL | RF1FL | RF1WL | RF1NL | RF0LL | RF0FL | RF0WL | RF0NL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-74. MCAN_ILS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved |
| 29 | ARAL | R/W | 0h | Access to Reserved Address Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |

Table 4-74. MCAN_ILS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 28 | PEDL | R/W | 0h | Protocol Error in Data Phase Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 27 | PEAL | R/W | 0h | Protocol Error in Arbitration Phase Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 26 | WDIL | R/W | 0h | Watchdog Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 25 | BOL | R/W | 0h | Bus_Off Status Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 24 | EWL | R/W | 0h | Warning Status Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 23 | EPL | R/W | 0h | Error Passive Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 22 | ELOL | R/W | 0h | Error Logging Overflow Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 21 | BEUL | R/W | 0h | Bit Error Uncorrected Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 20 | BECL | R/W | 0h | Bit Error Corrected Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 19 | DRXL | R/W | 0h | Message stored to Dedicated Rx Buffer Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 18 | TOOL | R/W | 0h | Timeout Occurred Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 17 | MRAFL | R/W | 0h | Message RAM Access Failure Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 16 | TSWL | R/W | 0h | Timestamp Wraparound Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 15 | TEFLL | R/W | 0h | Tx Event FIFO Event Lost Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 14 | TEFFL | R/W | 0h | Tx Event FIFO Full Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |
| 13 | TEFWL | R/W | 0h | Tx Event FIFO Watermark Reached Interrupt Line 0h = Interrupt assigned to interrupt line INTO 1h = Interrupt assigned to interrupt line INT1 |

Table 4-74. MCAN_ILS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 12 | TEFNL | R/W | 0h | Tx Event FIFO New Entry Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 11 | TFEL | R/W | 0h | Tx FIFO Empty Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 10 | TCFL | R/W | 0h | Transmission Cancellation Finished Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 9 | TCL | R/W | 0h | Transmission Completed Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 8 | HPML | R/W | 0h | High Priority Message Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 7 | RF1LL | R/W | 0h | Rx FIFO 1 Message Lost Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 6 | RF1FL | R/W | 0h | Rx FIFO 1 Full Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 5 | RF1WL | R/W | 0h | Rx FIFO 1 Watermark Reached Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 4 | RF1NL | R/W | 0h | Rx FIFO 1 New Message Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 3 | RF0LL | R/W | 0h | Rx FIFO 0 Message Lost Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 2 | RF0FL | R/W | 0h | Rx FIFO 0 Full Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 1 | RF0WL | R/W | 0h | Rx FIFO 0 Watermark Reached Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |
| 0 | RF0NL | R/W | 0h | Rx FIFO 0 New Message Interrupt Line 0h = Interrupt assigned to interrupt line INT0 1h = Interrupt assigned to interrupt line INT1 |

4.2.18 MCAN_ILE Register (Offset = 5Ch) [reset = 0h]

MCAN_ILE is shown in [Figure 4-29](#) and described in [Table 4-76](#).

Return to [Summary Table](#).

Interrupt Line Enable

Enable/disable interrupt lines INT0/INT1.

Each of the two interrupt lines to the Host CPU can be enabled/disabled separately by programming the MCAN_ILE[0] EINT0 and MCAN_ILE[1] EINT1 bits.

Table 4-75. MCAN_ILE Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 805Ch |
| MCU_MCAN1_CFG | 4056 805Ch |
| MCAN0_CFG | 0270 105Ch |
| MCAN1_CFG | 0271 105Ch |
| MCAN2_CFG | 0272 105Ch |
| MCAN3_CFG | 0273 105Ch |
| MCAN4_CFG | 0274 105Ch |
| MCAN5_CFG | 0275 105Ch |
| MCAN6_CFG | 0276 105Ch |
| MCAN7_CFG | 0277 105Ch |
| MCAN8_CFG | 0278 105Ch |
| MCAN9_CFG | 0279 105Ch |
| MCAN10_CFG | 027A 105Ch |
| MCAN11_CFG | 027B 105Ch |
| MCAN12_CFG | 027C 105Ch |
| MCAN13_CFG | 027D 105Ch |

Figure 4-29. MCAN_ILE Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | EINT1 | EINT0 |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-76. MCAN_ILE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | EINT1 | R/W | 0h | Enable Interrupt Line 1 0h = Interrupt line INT1 disabled 1h = Interrupt line INT1 enabled |

Table 4-76. MCAN_ILE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | EINT0 | R/W | 0h | Enable Interrupt Line 0 0h = Interrupt line INT0 disabled 1h = Interrupt line INT0 enabled |

4.2.19 MCAN_GFC Register (Offset = 80h) [reset = 0h]

MCAN_GFC is shown in [Figure 4-30](#) and described in [Table 4-78](#).

Return to [Summary Table](#).

Global Filter Configuration

Handling of non-matching frames and remote frames.

Global settings for Message ID filtering. The MCAN_GFC register controls the filter path for standard and extended messages (see and).

Table 4-77. MCAN_GFC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8080h |
| MCU_MCAN1_CFG | 4056 8080h |
| MCAN0_CFG | 0270 1080h |
| MCAN1_CFG | 0271 1080h |
| MCAN2_CFG | 0272 1080h |
| MCAN3_CFG | 0273 1080h |
| MCAN4_CFG | 0274 1080h |
| MCAN5_CFG | 0275 1080h |
| MCAN6_CFG | 0276 1080h |
| MCAN7_CFG | 0277 1080h |
| MCAN8_CFG | 0278 1080h |
| MCAN9_CFG | 0279 1080h |
| MCAN10_CFG | 027A 1080h |
| MCAN11_CFG | 027B 1080h |
| MCAN12_CFG | 027C 1080h |
| MCAN13_CFG | 027D 1080h |

Figure 4-30. MCAN_GFC Register

| | | | | | | | |
|----------|----|--------|----|--------|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ANFS | | ANFE | | RRFS | RRFE |
| R-0h | | R/W-0h | | R/W-0h | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-78. MCAN_GFC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-6 | RESERVED | R | 0h | Reserved |

Table 4-78. MCAN_GFC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 5-4 | ANFS | R/W | 0h | Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 0h = Accept in Rx FIFO 0 1h = Accept in Rx FIFO 1 2h = Reject 3h = Reject |
| 3-2 | ANFE | R/W | 0h | Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 0h = Accept in Rx FIFO 0 1h = Accept in Rx FIFO 1 2h = Reject 3h = Reject |
| 1 | RRFS | R/W | 0h | Reject Remote Frames Standard 0h = Filter remote frames with 11-bit standard IDs 1h = Reject all remote frames with 11-bit standard IDs |
| 0 | RRFE | R/W | 0h | Reject Remote Frames Extended 0h = Filter remote frames with 29-bit extended IDs 1h = Reject all remote frames with 29-bit extended IDs |

4.2.20 MCAN_SIDFC Register (Offset = 84h) [reset = 0h]

MCAN_SIDFC is shown in [Figure 4-31](#) and described in [Table 4-80](#).

Return to [Summary Table](#).

Standard ID Filter Configuration

Number of filter elements, pointer to start of filter list.

Settings for 11-bit standard Message ID filtering. The Standard ID Filter Configuration controls the filter path for standard messages (see).

Table 4-79. MCAN_SIDFC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8084h |
| MCU_MCAN1_CFG | 4056 8084h |
| MCAN0_CFG | 0270 1084h |
| MCAN1_CFG | 0271 1084h |
| MCAN2_CFG | 0272 1084h |
| MCAN3_CFG | 0273 1084h |
| MCAN4_CFG | 0274 1084h |
| MCAN5_CFG | 0275 1084h |
| MCAN6_CFG | 0276 1084h |
| MCAN7_CFG | 0277 1084h |
| MCAN8_CFG | 0278 1084h |
| MCAN9_CFG | 0279 1084h |
| MCAN10_CFG | 027A 1084h |
| MCAN11_CFG | 027B 1084h |
| MCAN12_CFG | 027C 1084h |
| MCAN13_CFG | 027D 1084h |

Figure 4-31. MCAN_SIDFC Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LSS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FLSSA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FLSSA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-80. MCAN_SIDFC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-24 | RESERVED | R | 0h | Reserved |

Table 4-80. MCAN_SIDFC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 23-16 | LSS | R/W | 0h | List Size Standard 0h = No standard Message ID filter 1h-80h (1-128) = Number of standard Message ID filter elements > 80h (128) = Values greater than 128 are interpreted as 128 |
| 15-2 | FLSSA | R/W | 0h | Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see <i>Message RAM Configuration</i>). |
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.21 MCAN_XIDFC Register (Offset = 88h) [reset = 0h]

MCAN_XIDFC is shown in [Figure 4-32](#) and described in [Table 4-82](#).

Return to [Summary Table](#).

Extended ID Filter Configuration

Number of filter elements, pointer to start of filter list.

Settings for 29-bit extended Message ID filtering. The Extended ID Filter Configuration controls the filter path for standard messages (see).

Table 4-81. MCAN_XIDFC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8088h |
| MCU_MCAN1_CFG | 4056 8088h |
| MCAN0_CFG | 0270 1088h |
| MCAN1_CFG | 0271 1088h |
| MCAN2_CFG | 0272 1088h |
| MCAN3_CFG | 0273 1088h |
| MCAN4_CFG | 0274 1088h |
| MCAN5_CFG | 0275 1088h |
| MCAN6_CFG | 0276 1088h |
| MCAN7_CFG | 0277 1088h |
| MCAN8_CFG | 0278 1088h |
| MCAN9_CFG | 0279 1088h |
| MCAN10_CFG | 027A 1088h |
| MCAN11_CFG | 027B 1088h |
| MCAN12_CFG | 027C 1088h |
| MCAN13_CFG | 027D 1088h |

Figure 4-32. MCAN_XIDFC Register

| | | | | | | | |
|----------|----|-----|----|--------|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | LSE | | | | | |
| R-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FLESA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FLESA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-82. MCAN_XIDFC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-23 | RESERVED | R | 0h | Reserved |

Table 4-82. MCAN_XIDFC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 22-16 | LSE | R/W | 0h | List Size Extended 0h = No extended Message ID filter 1h-40h (1-64) = Number of extended Message ID filter elements > 40h (64) = Values greater than 64 are interpreted as 64 |
| 15-2 | FLESA | R/W | 0h | Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see <i>Message RAM Configuration</i>). |
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.22 MCAN_XIDAM Register (Offset = 90h) [reset = 1FFFFFFFh]

MCAN_XIDAM is shown in [Figure 4-33](#) and described in [Table 4-84](#).

Return to [Summary Table](#).

Extended ID AND Mask

29-bit logical AND mask for J1939.

Table 4-83. MCAN_XIDAM Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8090h |
| MCU_MCAN1_CFG | 4056 8090h |
| MCAN0_CFG | 0270 1090h |
| MCAN1_CFG | 0271 1090h |
| MCAN2_CFG | 0272 1090h |
| MCAN3_CFG | 0273 1090h |
| MCAN4_CFG | 0274 1090h |
| MCAN5_CFG | 0275 1090h |
| MCAN6_CFG | 0276 1090h |
| MCAN7_CFG | 0277 1090h |
| MCAN8_CFG | 0278 1090h |
| MCAN9_CFG | 0279 1090h |
| MCAN10_CFG | 027A 1090h |
| MCAN11_CFG | 027B 1090h |
| MCAN12_CFG | 027C 1090h |
| MCAN13_CFG | 027D 1090h |

Figure 4-33. MCAN_XIDAM Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | EIDM | | | | | | | | | | | |
| R-0h | | | | R/W-1FFFFFFFh | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EIDM | | | | | | | | | | | | | | | |
| R/W-1FFFFFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-84. MCAN_XIDAM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-----------|---|
| 31-29 | RESERVED | R | 0h | Reserved |
| 28-0 | EIDM | R/W | 1FFFFFFFh | Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. |

4.2.23 MCAN_HPMS Register (Offset = 94h) [reset = 0h]

MCAN_HPMS is shown in [Figure 4-34](#) and described in [Table 4-86](#).

Return to [Summary Table](#).

High Priority Message Status

Status monitoring of incoming high priority messages.

This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Table 4-85. MCAN_HPMS Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8094h |
| MCU_MCAN1_CFG | 4056 8094h |
| MCAN0_CFG | 0270 1094h |
| MCAN1_CFG | 0271 1094h |
| MCAN2_CFG | 0272 1094h |
| MCAN3_CFG | 0273 1094h |
| MCAN4_CFG | 0274 1094h |
| MCAN5_CFG | 0275 1094h |
| MCAN6_CFG | 0276 1094h |
| MCAN7_CFG | 0277 1094h |
| MCAN8_CFG | 0278 1094h |
| MCAN9_CFG | 0279 1094h |
| MCAN10_CFG | 027A 1094h |
| MCAN11_CFG | 027B 1094h |
| MCAN12_CFG | 027C 1094h |
| MCAN13_CFG | 027D 1094h |

Figure 4-34. MCAN_HPMS Register

| | | | | | | | |
|----------|----|------|----|------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FLST | | | | FIDX | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSI | | BIDX | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-86. MCAN_HPMS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-16 | RESERVED | R | 0h | Reserved |

Table 4-86. MCAN_HPMS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 15 | FLST | R | 0h | Filter List Indicates the filter list of the matching filter element. 0h = Standard Filter List 1h = Extended Filter List |
| 14-8 | FIDX | R | 0h | Filter Index Index of matching filter element. Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1. |
| 7-6 | MSI | R | 0h | Message Storage Indicator 0h = No FIFO selected 1h = FIFO message lost 2h = Message stored in FIFO 0 3h = Message stored in FIFO 1 |
| 5-0 | BIDX | R | 0h | Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when the MCAN_HPMS[7-6] MSI = 1h. |

4.2.24 MCAN_NDAT1 Register (Offset = 98h) [reset = 0h]

MCAN_NDAT1 is shown in [Figure 4-35](#) and described in [Table 4-88](#).

Return to [Summary Table](#).

New Data 1

NewDat flags of dedicated Rx buffers 0-31.

The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host CPU clears them. Aflag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register.

Table 4-87. MCAN_NDAT1 Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 8098h |
| MCU_MCAN1_CFG | 4056 8098h |
| MCAN0_CFG | 0270 1098h |
| MCAN1_CFG | 0271 1098h |
| MCAN2_CFG | 0272 1098h |
| MCAN3_CFG | 0273 1098h |
| MCAN4_CFG | 0274 1098h |
| MCAN5_CFG | 0275 1098h |
| MCAN6_CFG | 0276 1098h |
| MCAN7_CFG | 0277 1098h |
| MCAN8_CFG | 0278 1098h |
| MCAN9_CFG | 0279 1098h |
| MCAN10_CFG | 027A 1098h |
| MCAN11_CFG | 027B 1098h |
| MCAN12_CFG | 027C 1098h |
| MCAN13_CFG | 027D 1098h |

Figure 4-35. MCAN_NDAT1 Register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ND31 | ND30 | ND29 | ND28 | ND27 | ND26 | ND25 | ND24 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ND23 | ND22 | ND21 | ND20 | ND19 | ND18 | ND17 | ND16 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ND15 | ND14 | ND13 | ND12 | ND11 | ND10 | ND9 | ND8 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ND7 | ND6 | ND5 | ND4 | ND3 | ND2 | ND1 | ND0 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |

LEGEND: RW1TC = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-88. MCAN_NDAT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 31 | ND31 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |

Table 4-88. MCAN_NDAT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 30 | ND30 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 29 | ND29 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 28 | ND28 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 27 | ND27 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 26 | ND26 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 25 | ND25 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 24 | ND24 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 23 | ND23 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 22 | ND22 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 21 | ND21 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 20 | ND20 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 19 | ND19 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 18 | ND18 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 17 | ND17 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 16 | ND16 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 15 | ND15 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |

Table 4-88. MCAN_NDAT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 14 | ND14 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 13 | ND13 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 12 | ND12 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 11 | ND11 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 10 | ND10 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 9 | ND9 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 8 | ND8 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 7 | ND7 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 6 | ND6 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 5 | ND5 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 4 | ND4 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 3 | ND3 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 2 | ND2 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 1 | ND1 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 0 | ND0 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |

4.2.25 MCAN_NDAT2 Register (Offset = 9Ch) [reset = 0h]

MCAN_NDAT2 is shown in [Figure 4-36](#) and described in [Table 4-90](#).

Return to [Summary Table](#).

New Data 2

NewDat flags of dedicated Rx buffers 32-63.

The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host CPU clears them. A flag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register.

Table 4-89. MCAN_NDAT2 Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 809Ch |
| MCU_MCAN1_CFG | 4056 809Ch |
| MCAN0_CFG | 0270 109Ch |
| MCAN1_CFG | 0271 109Ch |
| MCAN2_CFG | 0272 109Ch |
| MCAN3_CFG | 0273 109Ch |
| MCAN4_CFG | 0274 109Ch |
| MCAN5_CFG | 0275 109Ch |
| MCAN6_CFG | 0276 109Ch |
| MCAN7_CFG | 0277 109Ch |
| MCAN8_CFG | 0278 109Ch |
| MCAN9_CFG | 0279 109Ch |
| MCAN10_CFG | 027A 109Ch |
| MCAN11_CFG | 027B 109Ch |
| MCAN12_CFG | 027C 109Ch |
| MCAN13_CFG | 027D 109Ch |

Figure 4-36. MCAN_NDAT2 Register

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ND63 | ND62 | ND61 | ND60 | ND59 | ND58 | ND57 | ND56 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ND55 | ND54 | ND53 | ND52 | ND51 | ND50 | ND49 | ND48 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ND47 | ND46 | ND45 | ND44 | ND43 | ND42 | ND41 | ND40 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ND39 | ND38 | ND37 | ND36 | ND35 | ND34 | ND33 | ND32 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |

LEGEND: RW1TC = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-90. MCAN_NDAT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 31 | ND63 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |

Table 4-90. MCAN_NDAT2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 30 | ND62 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 29 | ND61 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 28 | ND60 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 27 | ND59 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 26 | ND58 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 25 | ND57 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 24 | ND56 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 23 | ND55 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 22 | ND54 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 21 | ND53 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 20 | ND52 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 19 | ND51 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 18 | ND50 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 17 | ND49 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 16 | ND48 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 15 | ND47 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |

Table 4-90. MCAN_NDAT2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 14 | ND46 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 13 | ND45 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 12 | ND44 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 11 | ND43 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 10 | ND42 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 9 | ND41 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 8 | ND40 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 7 | ND39 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 6 | ND38 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 5 | ND37 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 4 | ND36 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 3 | ND35 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 2 | ND34 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 1 | ND33 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |
| 0 | ND32 | RW1TC | 0h | New Data 0h = Rx Buffer not updated 1h = Rx Buffer updated from new message |

4.2.26 MCAN_RXF0C Register (Offset = A0h) [reset = 0h]

MCAN_RXF0C is shown in [Figure 4-37](#) and described in [Table 4-92](#).

Return to [Summary Table](#).

Rx FIFO 0 Configuration

FIFO 0 operation mode, watermark, size and start address.

Table 4-91. MCAN_RXF0C Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80A0h |
| MCU_MCAN1_CFG | 4056 80A0h |
| MCAN0_CFG | 0270 10A0h |
| MCAN1_CFG | 0271 10A0h |
| MCAN2_CFG | 0272 10A0h |
| MCAN3_CFG | 0273 10A0h |
| MCAN4_CFG | 0274 10A0h |
| MCAN5_CFG | 0275 10A0h |
| MCAN6_CFG | 0276 10A0h |
| MCAN7_CFG | 0277 10A0h |
| MCAN8_CFG | 0278 10A0h |
| MCAN9_CFG | 0279 10A0h |
| MCAN10_CFG | 027A 10A0h |
| MCAN11_CFG | 027B 10A0h |
| MCAN12_CFG | 027C 10A0h |
| MCAN13_CFG | 027D 10A0h |

Figure 4-37. MCAN_RXF0C Register

| | | | | | | | |
|----------|------|----|----|--------|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| F0OM | F0WM | | | | | | |
| R/W-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | F0S | | | | | | |
| R-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| F0SA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| F0SA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-92. MCAN_RXF0C Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 31 | F0OM | R/W | 0h | FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see , Rx FIFOs). 0h = FIFO 0 blocking mode 1h = FIFO 0 overwrite mode |

Table 4-92. MCAN_RXF0C Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 30-24 | F0WM | R/W | 0h | Rx FIFO 0 Watermark 0h = Watermark interrupt disabled 1h-40h (1-64) = Level for Rx FIFO 0 watermark interrupt (MCAN_IR[1] RF0W) > 40h (64) = Watermark interrupt disabled |
| 23 | RESERVED | R | 0h | Reserved |
| 22-16 | F0S | R/W | 0h | Rx FIFO 0 Size 0h = No Rx FIFO 0 1h-40h (1-64) = Number of Rx FIFO 0 elements > 40h (64) = Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to MCAN_RXF0C[22-16] F0S - 1. |
| 15-2 | F0SA | R/W | 0h | Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see , <i>Message RAM Configuration</i>). |
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.27 MCAN_RXF0S Register (Offset = A4h) [reset = 0h]

MCAN_RXF0S is shown in [Figure 4-38](#) and described in [Table 4-94](#).

Return to [Summary Table](#).

Rx FIFO 0 Status

FIFO 0 message lost/full indication, put index, get index and fill level.

Table 4-93. MCAN_RXF0S Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80A4h |
| MCU_MCAN1_CFG | 4056 80A4h |
| MCAN0_CFG | 0270 10A4h |
| MCAN1_CFG | 0271 10A4h |
| MCAN2_CFG | 0272 10A4h |
| MCAN3_CFG | 0273 10A4h |
| MCAN4_CFG | 0274 10A4h |
| MCAN5_CFG | 0275 10A4h |
| MCAN6_CFG | 0276 10A4h |
| MCAN7_CFG | 0277 10A4h |
| MCAN8_CFG | 0278 10A4h |
| MCAN9_CFG | 0279 10A4h |
| MCAN10_CFG | 027A 10A4h |
| MCAN11_CFG | 027B 10A4h |
| MCAN12_CFG | 027C 10A4h |
| MCAN13_CFG | 027D 10A4h |

Figure 4-38. MCAN_RXF0S Register

| | | | | | | | |
|----------|----|------|----|------|----|------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | RF0L | F0F |
| R-0h | | | | | | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | F0PI | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | F0GI | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | F0FL | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-94. MCAN_RXF0S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-26 | RESERVED | R | 0h | Reserved |

Table 4-94. MCAN_RXF0S Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 25 | RF0L | R | 0h | <p>Rx FIFO 0 Message Lost</p> <p>This bit is a copy of interrupt flag MCAN_IR[3] RF0L. When the MCAN_IR[3] RF0L flag is reset, this bit is also reset.</p> <p>0h = No Rx FIFO 0 message lost</p> <p>1h = Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero</p> <p>Note: Overwriting the oldest message when the MCAN_RXF0C[31] F0OM = 1h will not set this flag.</p> |
| 24 | F0F | R | 0h | <p>Rx FIFO 0 Full</p> <p>0h = Rx FIFO 0 not full</p> <p>1h = Rx FIFO 0 full</p> |
| 23-22 | RESERVED | R | 0h | Reserved |
| 21-16 | F0PI | R | 0h | <p>Rx FIFO 0 Put Index</p> <p>Rx FIFO 0 write index pointer, range 0 to 63.</p> |
| 15-14 | RESERVED | R | 0h | Reserved |
| 13-8 | F0GI | R | 0h | <p>Rx FIFO 0 Get Index</p> <p>Rx FIFO 0 read index pointer, range 0 to 63.</p> |
| 7 | RESERVED | R | 0h | Reserved |
| 6-0 | F0FL | R | 0h | <p>Rx FIFO 0 Fill Level</p> <p>Number of elements stored in Rx FIFO 0, range 0 to 64.</p> |

4.2.28 MCAN_RXF0A Register (Offset = A8h) [reset = 0h]

MCAN_RXF0A is shown in [Figure 4-39](#) and described in [Table 4-96](#).

Return to [Summary Table](#).

Rx FIFO 0 Acknowledge

FIFO 0 acknowledge last index of read buffers, updates get index and fill level.

Table 4-95. MCAN_RXF0A Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80A8h |
| MCU_MCAN1_CFG | 4056 80A8h |
| MCAN0_CFG | 0270 10A8h |
| MCAN1_CFG | 0271 10A8h |
| MCAN2_CFG | 0272 10A8h |
| MCAN3_CFG | 0273 10A8h |
| MCAN4_CFG | 0274 10A8h |
| MCAN5_CFG | 0275 10A8h |
| MCAN6_CFG | 0276 10A8h |
| MCAN7_CFG | 0277 10A8h |
| MCAN8_CFG | 0278 10A8h |
| MCAN9_CFG | 0279 10A8h |
| MCAN10_CFG | 027A 10A8h |
| MCAN11_CFG | 027B 10A8h |
| MCAN12_CFG | 027C 10A8h |
| MCAN13_CFG | 027D 10A8h |

Figure 4-39. MCAN_RXF0A Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|--------|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | F0AI | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-96. MCAN_RXF0A Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R | 0h | Reserved |
| 5-0 | F0AI | R/W | 0h | Rx FIFO 0 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to the MCAN_RXF0A[5-0] F0AI field. This will set the Rx FIFO 0 Get Index MCAN_RXF0S[13-8] F0GI field to the MCAN_RXF0A[5-0] F0AI field + 1 and update the FIFO 0 Fill Level MCAN_RXF0S[6-0] F0FL field. |

4.2.29 MCAN_RXBC Register (Offset = ACh) [reset = 0h]

MCAN_RXBC is shown in [Figure 4-40](#) and described in [Table 4-98](#).

Return to [Summary Table](#).

Rx Buffer Configuration

Start address of Rx buffer section.

Table 4-97. MCAN_RXBC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80ACh |
| MCU_MCAN1_CFG | 4056 80ACh |
| MCAN0_CFG | 0270 10ACh |
| MCAN1_CFG | 0271 10ACh |
| MCAN2_CFG | 0272 10ACh |
| MCAN3_CFG | 0273 10ACh |
| MCAN4_CFG | 0274 10ACh |
| MCAN5_CFG | 0275 10ACh |
| MCAN6_CFG | 0276 10ACh |
| MCAN7_CFG | 0277 10ACh |
| MCAN8_CFG | 0278 10ACh |
| MCAN9_CFG | 0279 10ACh |
| MCAN10_CFG | 027A 10ACh |
| MCAN11_CFG | 027B 10ACh |
| MCAN12_CFG | 027C 10ACh |
| MCAN13_CFG | 027D 10ACh |

Figure 4-40. MCAN_RXBC Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RBSA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBSA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-98. MCAN_RXBC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15-2 | RBSA | R/W | 0h | <p>Rx Buffer Start Address</p> <p>Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address, see).</p> <p>Also used to reference debug messages A, B, C.</p> <p>Note: Debug feature is not supported.</p> |

Table 4-98. MCAN_RXBC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.30 MCAN_RXF1C Register (Offset = B0h) [reset = 0h]

MCAN_RXF1C is shown in [Figure 4-41](#) and described in [Table 4-100](#).

Return to [Summary Table](#).

Rx FIFO 1 Configuration

FIFO 1 operation mode, watermark, size and start address.

Table 4-99. MCAN_RXF1C Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80B0h |
| MCU_MCAN1_CFG | 4056 80B0h |
| MCAN0_CFG | 0270 10B0h |
| MCAN1_CFG | 0271 10B0h |
| MCAN2_CFG | 0272 10B0h |
| MCAN3_CFG | 0273 10B0h |
| MCAN4_CFG | 0274 10B0h |
| MCAN5_CFG | 0275 10B0h |
| MCAN6_CFG | 0276 10B0h |
| MCAN7_CFG | 0277 10B0h |
| MCAN8_CFG | 0278 10B0h |
| MCAN9_CFG | 0279 10B0h |
| MCAN10_CFG | 027A 10B0h |
| MCAN11_CFG | 027B 10B0h |
| MCAN12_CFG | 027C 10B0h |
| MCAN13_CFG | 027D 10B0h |

Figure 4-41. MCAN_RXF1C Register

| | | | | | | | |
|----------|--------|----|----|----|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| F1OM | F1WM | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | F1S | | | | | | |
| R-0h | R/W-0h | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| F1SA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| F1SA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-100. MCAN_RXF1C Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 31 | F1OM | R/W | 0h | FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see , Rx FIFOs). 0h = FIFO 1 blocking mode 1h = FIFO 1 overwrite mode |

Table 4-100. MCAN_RXF1C Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 30-24 | F1WM | R/W | 0h | Rx FIFO 1 Watermark 0h = Watermark interrupt disabled 1h-40h (1-64) = Level for Rx FIFO 1 watermark interrupt (MCAN_IR[5] RF1W) > 40h (64) = Watermark interrupt disabled |
| 23 | RESERVED | R | 0h | Reserved |
| 22-16 | F1S | R/W | 0h | Rx FIFO 1 Size 0h = No Rx FIFO 1 1h-40h (1-64) = Number of Rx FIFO 1 elements > 40h (64) = Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to MCAN_RXF1C[22-16] F1S - 1. |
| 15-2 | F1SA | R/W | 0h | Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see , <i>Message RAM Configuration</i>). |
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.31 MCAN_RXF1S Register (Offset = B4h) [reset = 0h]

MCAN_RXF1S is shown in [Figure 4-42](#) and described in [Table 4-102](#).

Return to [Summary Table](#).

Rx FIFO 1 Status

FIFO 1 message lost/full indication, put index, get index and fill level.

Table 4-101. MCAN_RXF1S Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80B4h |
| MCU_MCAN1_CFG | 4056 80B4h |
| MCAN0_CFG | 0270 10B4h |
| MCAN1_CFG | 0271 10B4h |
| MCAN2_CFG | 0272 10B4h |
| MCAN3_CFG | 0273 10B4h |
| MCAN4_CFG | 0274 10B4h |
| MCAN5_CFG | 0275 10B4h |
| MCAN6_CFG | 0276 10B4h |
| MCAN7_CFG | 0277 10B4h |
| MCAN8_CFG | 0278 10B4h |
| MCAN9_CFG | 0279 10B4h |
| MCAN10_CFG | 027A 10B4h |
| MCAN11_CFG | 027B 10B4h |
| MCAN12_CFG | 027C 10B4h |
| MCAN13_CFG | 027D 10B4h |

Figure 4-42. MCAN_RXF1S Register

| | | | | | | | |
|----------|----------|----|----|------|----|------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DMS | RESERVED | | | | | RF1L | F1F |
| R-0h | R-0h | | | | | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | F1PI | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | F1GI | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | F1FL | | | |
| R-0h | | | | R-0h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-102. MCAN_RXF1S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|--|
| 31-30 | DMS | R | 0h | <p>Debug Message Status</p> <p>0h = Idle state, wait for reception of debug messages, DMA request is cleared</p> <p>1h = Debug message A received</p> <p>2h = Debug messages A, B received</p> <p>3h = Debug messages A, B, C received, DMA request is set</p> <p>Note: Debug feature is not supported.</p> |

Table 4-102. MCAN_RXF1S Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 29-26 | RESERVED | R | 0h | Reserved |
| 25 | RF1L | R | 0h | <p>Rx FIFO 1 Message Lost</p> <p>This bit is a copy of interrupt flag MCAN_IR[7] RF1L. When the MCAN_IR[7] RF1L flag is reset, this bit is also reset.</p> <p>0h = No Rx FIFO 1 message lost</p> <p>1h = Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero</p> <p>Note: Overwriting the oldest message when the MCAN_RXF1C[31] F1OM = 1h will not set this flag.</p> |
| 24 | F1F | R | 0h | <p>Rx FIFO 1 Full</p> <p>0h = Rx FIFO 1 not full</p> <p>1h = Rx FIFO 1 full</p> |
| 23-22 | RESERVED | R | 0h | Reserved |
| 21-16 | F1PI | R | 0h | <p>Rx FIFO 1 Put Index</p> <p>Rx FIFO 1 write index pointer, range 0 to 63.</p> |
| 15-14 | RESERVED | R | 0h | Reserved |
| 13-8 | F1GI | R | 0h | <p>Rx FIFO 1 Get Index</p> <p>Rx FIFO 1 read index pointer, range 0 to 63.</p> |
| 7 | RESERVED | R | 0h | Reserved |
| 6-0 | F1FL | R | 0h | <p>Rx FIFO 1 Fill Level</p> <p>Number of elements stored in Rx FIFO 1, range 0 to 64.</p> |

4.2.32 MCAN_RXF1A Register (Offset = B8h) [reset = 0h]

MCAN_RXF1A is shown in [Figure 4-43](#) and described in [Table 4-104](#).

Return to [Summary Table](#).

Rx FIFO 1 Acknowledge

FIFO 1 acknowledge last index of read buffers, updates get index and fill level.

Table 4-103. MCAN_RXF1A Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80B8h |
| MCU_MCAN1_CFG | 4056 80B8h |
| MCAN0_CFG | 0270 10B8h |
| MCAN1_CFG | 0271 10B8h |
| MCAN2_CFG | 0272 10B8h |
| MCAN3_CFG | 0273 10B8h |
| MCAN4_CFG | 0274 10B8h |
| MCAN5_CFG | 0275 10B8h |
| MCAN6_CFG | 0276 10B8h |
| MCAN7_CFG | 0277 10B8h |
| MCAN8_CFG | 0278 10B8h |
| MCAN9_CFG | 0279 10B8h |
| MCAN10_CFG | 027A 10B8h |
| MCAN11_CFG | 027B 10B8h |
| MCAN12_CFG | 027C 10B8h |
| MCAN13_CFG | 027D 10B8h |

Figure 4-43. MCAN_RXF1A Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | F1AI | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-104. MCAN_RXF1A Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R | 0h | Reserved |
| 5-0 | F1AI | R/W | 0h | Rx FIFO 1 Acknowledge Index After the Host CPU has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to the MCAN_RXF1A[5-0] F1AI field. This will set the Rx FIFO 1 Get Index MCAN_RXF1S[13-8] F1GI field to the MCAN_RXF1A[5-0] F1AI field + 1 and update the FIFO 1 Fill Level MCAN_RXF1S[6-0] F1FL field. |

4.2.33 MCAN_RXESC Register (Offset = BCh) [reset = 0h]

MCAN_RXESC is shown in [Figure 4-44](#) and described in [Table 4-106](#).

Return to [Summary Table](#).

Rx Buffer/FIFO Element Size Configuration

Configure data field size for storage of accepted frames.

Table 4-105. MCAN_RXESC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80BCh |
| MCU_MCAN1_CFG | 4056 80BCh |
| MCAN0_CFG | 0270 10BCh |
| MCAN1_CFG | 0271 10BCh |
| MCAN2_CFG | 0272 10BCh |
| MCAN3_CFG | 0273 10BCh |
| MCAN4_CFG | 0274 10BCh |
| MCAN5_CFG | 0275 10BCh |
| MCAN6_CFG | 0276 10BCh |
| MCAN7_CFG | 0277 10BCh |
| MCAN8_CFG | 0278 10BCh |
| MCAN9_CFG | 0279 10BCh |
| MCAN10_CFG | 027A 10BCh |
| MCAN11_CFG | 027B 10BCh |
| MCAN12_CFG | 027C 10BCh |
| MCAN13_CFG | 027D 10BCh |

Figure 4-44. MCAN_RXESC Register

| | | | | | | | |
|----------|--------|----|----|----------|--------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | RBDS | | |
| R-0h | | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | F1DS | | | RESERVED | F0DS | | |
| R-0h | R/W-0h | | | R-0h | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-106. MCAN_RXESC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-11 | RESERVED | R | 0h | Reserved |

Table 4-106. MCAN_RXESC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 10-8 | RBDS | R/W | 0h | Rx Buffer Data Field Size 0h = 8 byte data field 1h = 12 byte data field 2h = 16 byte data field 3h = 20 byte data field 4h = 24 byte data field 5h = 32 byte data field 6h = 48 byte data field 7h = 64 byte data field |
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | F1DS | R/W | 0h | Rx FIFO 1 Data Field Size 0h = 8 byte data field 1h = 12 byte data field 2h = 16 byte data field 3h = 20 byte data field 4h = 24 byte data field 5h = 32 byte data field 6h = 48 byte data field 7h = 64 byte data field |
| 3 | RESERVED | R | 0h | Reserved |
| 2-0 | F0DS | R/W | 0h | Rx FIFO 0 Data Field Size 0h = 8 byte data field 1h = 12 byte data field 2h = 16 byte data field 3h = 20 byte data field 4h = 24 byte data field 5h = 32 byte data field 6h = 48 byte data field 7h = 64 byte data field Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by the MCAN_RXESC register are stored to the Rx Buffer respectively Rx FIFO element. The rest of the frame's data field is ignored. |

4.2.34 MCAN_TXBC Register (Offset = C0h) [reset = 0h]

MCAN_TXBC is shown in [Figure 4-45](#) and described in [Table 4-108](#).

Return to [Summary Table](#).

Tx Buffer Configuration

Configure Tx FIFO/Queue mode, Tx FIFO/Queue size, number of dedicated Tx buffers, Tx buffer start address.

Table 4-107. MCAN_TXBC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80C0h |
| MCU_MCAN1_CFG | 4056 80C0h |
| MCAN0_CFG | 0270 10C0h |
| MCAN1_CFG | 0271 10C0h |
| MCAN2_CFG | 0272 10C0h |
| MCAN3_CFG | 0273 10C0h |
| MCAN4_CFG | 0274 10C0h |
| MCAN5_CFG | 0275 10C0h |
| MCAN6_CFG | 0276 10C0h |
| MCAN7_CFG | 0277 10C0h |
| MCAN8_CFG | 0278 10C0h |
| MCAN9_CFG | 0279 10C0h |
| MCAN10_CFG | 027A 10C0h |
| MCAN11_CFG | 027B 10C0h |
| MCAN12_CFG | 027C 10C0h |
| MCAN13_CFG | 027D 10C0h |

Figure 4-45. MCAN_TXBC Register

| | | | | | | | |
|----------|--------|--------|----|----|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | TFQM | TFQS | | | | | |
| R-0h | R/W-0h | R/W-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | NDTB | | | | | |
| R-0h | | R/W-0h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBSA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBSA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-108. MCAN_TXBC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 31 | RESERVED | R | 0h | Reserved |
| 30 | TFQM | R/W | 0h | Tx FIFO/Queue Mode 0h = Tx FIFO operation 1h = Tx Queue operation |

Table 4-108. MCAN_TXBC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 29-24 | TFQS | R/W | 0h | Transmit FIFO/Queue Size 0h = No Tx FIFO/Queue 1h-20h (1-32) = Number of Tx Buffers used for Tx FIFO/Queue > 20h (32) = Values greater than 32 are interpreted as 32 |
| 23-22 | RESERVED | R | 0h | Reserved |
| 21-16 | NDTB | R/W | 0h | Number of Dedicated Transmit Buffers 0h = No Dedicated Tx Buffers 1h-20h (1-32) = Number of Dedicated Tx Buffers > 20h (32) = Values greater than 32 are interpreted as 32 |
| 15-2 | TBSA | R/W | 0h | Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see , <i>Message RAM Configuration</i>). Note: Be aware that the sum of the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers. |
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.35 MCAN_TXFQS Register (Offset = C4h) [reset = 0h]

MCAN_TXFQS is shown in [Figure 4-46](#) and described in [Table 4-110](#).

Return to [Summary Table](#).

Tx FIFO/Queue Status

Tx FIFO/Queue full indication and put index, Tx FIFO get index and fill level.

The Tx FIFO/Queue status is related to the pending Tx requests listed in the MCAN_TXBRP register. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (the MCAN_TXBRP register not yet updated).

Table 4-109. MCAN_TXFQS Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80C4h |
| MCU_MCAN1_CFG | 4056 80C4h |
| MCAN0_CFG | 0270 10C4h |
| MCAN1_CFG | 0271 10C4h |
| MCAN2_CFG | 0272 10C4h |
| MCAN3_CFG | 0273 10C4h |
| MCAN4_CFG | 0274 10C4h |
| MCAN5_CFG | 0275 10C4h |
| MCAN6_CFG | 0276 10C4h |
| MCAN7_CFG | 0277 10C4h |
| MCAN8_CFG | 0278 10C4h |
| MCAN9_CFG | 0279 10C4h |
| MCAN10_CFG | 027A 10C4h |
| MCAN11_CFG | 027B 10C4h |
| MCAN12_CFG | 027C 10C4h |
| MCAN13_CFG | 027D 10C4h |

Figure 4-46. MCAN_TXFQS Register

| | | | | | | | |
|----------|----|------|-------|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | TFQF | TFQPI | | | | |
| R-0h | | R-0h | R-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | TFGI | | | | |
| R-0h | | | R-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | TFFL | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-110. MCAN_TXFQS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-22 | RESERVED | R | 0h | Reserved |

Table 4-110. MCAN_TXFQS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 21 | TFQF | R | 0h | Tx FIFO/Queue Full 0h = Tx FIFO/Queue not full 1h = Tx FIFO/Queue full |
| 20-16 | TFQPI | R | 0h | Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. |
| 15-13 | RESERVED | R | 0h | Reserved |
| 12-8 | TFGI | R | 0h | Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1h). |
| 7-6 | RESERVED | R | 0h | Reserved |
| 5-0 | TFFL | R | 0h | Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from the MCAN_TXFQS[12-8] TFGI field, range 0 to 32. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1h). Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. |

4.2.36 MCAN_TXESC Register (Offset = C8h) [reset = 0h]

MCAN_TXESC is shown in [Figure 4-47](#) and described in [Table 4-112](#).

Return to [Summary Table](#).

Tx Buffer Element Size Configuration

Configure data field size for frame transmission.

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Table 4-111. MCAN_TXESC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80C8h |
| MCU_MCAN1_CFG | 4056 80C8h |
| MCAN0_CFG | 0270 10C8h |
| MCAN1_CFG | 0271 10C8h |
| MCAN2_CFG | 0272 10C8h |
| MCAN3_CFG | 0273 10C8h |
| MCAN4_CFG | 0274 10C8h |
| MCAN5_CFG | 0275 10C8h |
| MCAN6_CFG | 0276 10C8h |
| MCAN7_CFG | 0277 10C8h |
| MCAN8_CFG | 0278 10C8h |
| MCAN9_CFG | 0279 10C8h |
| MCAN10_CFG | 027A 10C8h |
| MCAN11_CFG | 027B 10C8h |
| MCAN12_CFG | 027C 10C8h |
| MCAN13_CFG | 027D 10C8h |

Figure 4-47. MCAN_TXESC Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | TBDS | | | |
| R-0h | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-112. MCAN_TXESC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-3 | RESERVED | R | 0h | Reserved |

Table 4-112. MCAN_TXESC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 2-0 | TBDS | R/W | 0h | <p>Tx Buffer Data Field Size</p> <p>0h = 8 byte data field</p> <p>1h = 12 byte data field</p> <p>2h = 16 byte data field</p> <p>3h = 20 byte data field</p> <p>4h = 24 byte data field</p> <p>5h = 32 byte data field</p> <p>6h = 48 byte data field</p> <p>7h = 64 byte data field</p> <p>Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size MCAN_TXESC[2-0] TBDS, the bytes not defined by the Tx Buffer are transmitted as CCh (padding bytes).</p> |

4.2.37 MCAN_TXBRP Register (Offset = CCh) [reset = 0h]

MCAN_TXBRP is shown in [Figure 4-48](#) and described in [Table 4-114](#).

Return to [Summary Table](#).

Tx Buffer Request Pending

Tx buffers with pending transmission request.

Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via the MCAN_TXBAR register. The bits are reset after a requested transmission has completed or has been cancelled via the MCAN_TXBCR register.

The MCAN_TXBRP bits are set only for those Tx Buffers configured via the MCAN_TXBC register. After a MCAN_TXBRP bit has been set, a Tx scan (see , *Tx Handling*) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).

A cancellation request resets the corresponding transmission request pending bit of register the MCAN_TXBRP register. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding MCAN_TXBRP bit has been reset.

After a cancellation has been requested, a finished cancellation is signalled via the MCAN_TXBCF flag

- after successful transmission together with the corresponding MCAN_TXBTO bit
- when the transmission has not yet been started at the point of cancellation
- when the transmission has been aborted due to lost arbitration
- when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding MCAN_TXBCF bit is set for all unsuccessful transmissions.

Note: The MCAN_TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is cancelled immediately, the corresponding MCAN_TXBRP bit is reset.

Table 4-113. MCAN_TXBRP Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80CCh |
| MCU_MCAN1_CFG | 4056 80CCh |
| MCAN0_CFG | 0270 10CCh |
| MCAN1_CFG | 0271 10CCh |
| MCAN2_CFG | 0272 10CCh |
| MCAN3_CFG | 0273 10CCh |
| MCAN4_CFG | 0274 10CCh |
| MCAN5_CFG | 0275 10CCh |
| MCAN6_CFG | 0276 10CCh |
| MCAN7_CFG | 0277 10CCh |
| MCAN8_CFG | 0278 10CCh |
| MCAN9_CFG | 0279 10CCh |
| MCAN10_CFG | 027A 10CCh |
| MCAN11_CFG | 027B 10CCh |
| MCAN12_CFG | 027C 10CCh |
| MCAN13_CFG | 027D 10CCh |

Figure 4-48. MCAN_TXBRP Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TRP31 | TRP30 | TRP29 | TRP28 | TRP27 | TRP26 | TRP25 | TRP24 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

Figure 4-48. MCAN_TXBRP Register (continued)

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TRP23 | TRP22 | TRP21 | TRP20 | TRP19 | TRP18 | TRP17 | TRP16 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TRP15 | TRP14 | TRP13 | TRP12 | TRP11 | TRP10 | TRP9 | TRP8 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TRP7 | TRP6 | TRP5 | TRP4 | TRP3 | TRP2 | TRP1 | TRP0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 4-114. MCAN_TXBRP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 31 | TRP31 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 30 | TRP30 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 29 | TRP29 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 28 | TRP28 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 27 | TRP27 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 26 | TRP26 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 25 | TRP25 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 24 | TRP24 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 23 | TRP23 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 22 | TRP22 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 21 | TRP21 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |

Table 4-114. MCAN_TXBRP Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 20 | TRP20 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 19 | TRP19 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 18 | TRP18 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 17 | TRP17 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 16 | TRP16 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 15 | TRP15 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 14 | TRP14 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 13 | TRP13 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 12 | TRP12 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 11 | TRP11 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 10 | TRP10 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 9 | TRP9 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 8 | TRP8 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 7 | TRP7 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 6 | TRP6 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 5 | TRP5 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |

Table 4-114. MCAN_TXBRP Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 4 | TRP4 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 3 | TRP3 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 2 | TRP2 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 1 | TRP1 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |
| 0 | TRP0 | R | 0h | Transmission Request Pending 0h = No transmission request pending 1h = Transmission request pending |

4.2.38 MCAN_TXBAR Register (Offset = D0h) [reset = 0h]

MCAN_TXBAR is shown in [Figure 4-49](#) and described in [Table 4-116](#).

Return to [Summary Table](#).

Tx Buffer Add Request
Add transmission requests.

Each Tx Buffer has its own Add Request bit. Writing 1h will set the corresponding Add Request bit; writing a 0h has no impact. This enables the Host CPU to set transmission requests for multiple Tx Buffers with one write to the MCAN_TXBAR register. The MCAN_TXBAR bits are set only for those Tx Buffers configured via the MCAN_TXBC register. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed.

Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding MCAN_TXBRP bit already set), this add request is ignored.

Table 4-115. MCAN_TXBAR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80D0h |
| MCU_MCAN1_CFG | 4056 80D0h |
| MCAN0_CFG | 0270 10D0h |
| MCAN1_CFG | 0271 10D0h |
| MCAN2_CFG | 0272 10D0h |
| MCAN3_CFG | 0273 10D0h |
| MCAN4_CFG | 0274 10D0h |
| MCAN5_CFG | 0275 10D0h |
| MCAN6_CFG | 0276 10D0h |
| MCAN7_CFG | 0277 10D0h |
| MCAN8_CFG | 0278 10D0h |
| MCAN9_CFG | 0279 10D0h |
| MCAN10_CFG | 027A 10D0h |
| MCAN11_CFG | 027B 10D0h |
| MCAN12_CFG | 027C 10D0h |
| MCAN13_CFG | 027D 10D0h |

Figure 4-49. MCAN_TXBAR Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| AR31 | AR30 | AR29 | AR28 | AR27 | AR26 | AR25 | AR24 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| AR23 | AR22 | AR21 | AR20 | AR19 | AR18 | AR17 | AR16 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AR15 | AR14 | AR13 | AR12 | AR11 | AR10 | AR9 | AR8 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |

LEGEND: RW1TC = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-116. MCAN_TXBAR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|--|
| 31 | AR31 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 30 | AR30 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 29 | AR29 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 28 | AR28 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 27 | AR27 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 26 | AR26 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 25 | AR25 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 24 | AR24 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 23 | AR23 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 22 | AR22 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 21 | AR21 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 20 | AR20 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 19 | AR19 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 18 | AR18 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 17 | AR17 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 16 | AR16 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |

Table 4-116. MCAN_TXBAR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|--|
| 15 | AR15 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 14 | AR14 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 13 | AR13 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 12 | AR12 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 11 | AR11 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 10 | AR10 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 9 | AR9 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 8 | AR8 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 7 | AR7 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 6 | AR6 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 5 | AR5 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 4 | AR4 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 3 | AR3 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 2 | AR2 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 1 | AR1 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |
| 0 | AR0 | RW1TC | 0h | Add Request 0h = No transmission request added 1h = Transmission requested added |

4.2.39 MCAN_TXBCR Register (Offset = D4h) [reset = 0h]

MCAN_TXBCR is shown in [Figure 4-50](#) and described in [Table 4-118](#).

Return to [Summary Table](#).

Tx Buffer Cancellation Request

Request cancellation of pending transmissions.

Each Tx Buffer has its own Cancellation Request bit. Writing a 1h will set the corresponding Cancellation Request bit; writing a 0h has no impact. This enables the Host CPU to set cancellation requests for multiple Tx Buffers with one write to the MCAN_TXBCR register. The MCAN_TXBCR bits are set only for those Tx Buffers configured via the MCAN_TXBC register. The bits remain set until the corresponding bit of the MCAN_TXBRP register is reset.

Table 4-117. MCAN_TXBCR Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80D4h |
| MCU_MCAN1_CFG | 4056 80D4h |
| MCAN0_CFG | 0270 10D4h |
| MCAN1_CFG | 0271 10D4h |
| MCAN2_CFG | 0272 10D4h |
| MCAN3_CFG | 0273 10D4h |
| MCAN4_CFG | 0274 10D4h |
| MCAN5_CFG | 0275 10D4h |
| MCAN6_CFG | 0276 10D4h |
| MCAN7_CFG | 0277 10D4h |
| MCAN8_CFG | 0278 10D4h |
| MCAN9_CFG | 0279 10D4h |
| MCAN10_CFG | 027A 10D4h |
| MCAN11_CFG | 027B 10D4h |
| MCAN12_CFG | 027C 10D4h |
| MCAN13_CFG | 027D 10D4h |

Figure 4-50. MCAN_TXBCR Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| CR31 | CR30 | CR29 | CR28 | CR27 | CR26 | CR25 | CR24 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CR23 | CR22 | CR21 | CR20 | CR19 | CR18 | CR17 | CR16 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CR15 | CR14 | CR13 | CR12 | CR11 | CR10 | CR9 | CR8 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |
| RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h | RW1TC-0h |

LEGEND: RW1TC = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-118. MCAN_TXBCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 31 | CR31 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 30 | CR30 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 29 | CR29 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 28 | CR28 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 27 | CR27 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 26 | CR26 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 25 | CR25 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 24 | CR24 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 23 | CR23 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 22 | CR22 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 21 | CR21 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 20 | CR20 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 19 | CR19 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 18 | CR18 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 17 | CR17 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 16 | CR16 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |

Table 4-118. MCAN_TXBCR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|---|
| 15 | CR15 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 14 | CR14 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 13 | CR13 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 12 | CR12 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 11 | CR11 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 10 | CR10 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 9 | CR9 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 8 | CR8 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 7 | CR7 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 6 | CR6 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 5 | CR5 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 4 | CR4 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 3 | CR3 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 2 | CR2 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 1 | CR1 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |
| 0 | CR0 | RW1TC | 0h | Cancellation Request 0h = No cancellation pending 1h = Cancellation pending |

4.2.40 MCAN_TXBTO Register (Offset = D8h) [reset = 0h]

MCAN_TXBTO is shown in [Figure 4-51](#) and described in [Table 4-120](#).

Return to [Summary Table](#).

Tx Buffer Transmission Occurred

Signals successful transmissions, set when corresponding MCAN_TXBRP flag is cleared.

Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding MCAN_TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1h to the corresponding bit of register the MCAN_TXBAR register.

Table 4-119. MCAN_TXBTO Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80D8h |
| MCU_MCAN1_CFG | 4056 80D8h |
| MCAN0_CFG | 0270 10D8h |
| MCAN1_CFG | 0271 10D8h |
| MCAN2_CFG | 0272 10D8h |
| MCAN3_CFG | 0273 10D8h |
| MCAN4_CFG | 0274 10D8h |
| MCAN5_CFG | 0275 10D8h |
| MCAN6_CFG | 0276 10D8h |
| MCAN7_CFG | 0277 10D8h |
| MCAN8_CFG | 0278 10D8h |
| MCAN9_CFG | 0279 10D8h |
| MCAN10_CFG | 027A 10D8h |
| MCAN11_CFG | 027B 10D8h |
| MCAN12_CFG | 027C 10D8h |
| MCAN13_CFG | 027D 10D8h |

Figure 4-51. MCAN_TXBTO Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------|------|------|------|------|------|------|
| TO31 | TO30 | TO29 | TO28 | TO27 | TO26 | TO25 | TO24 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TO23 | TO22 | TO21 | TO20 | TO19 | TO18 | TO17 | TO16 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TO15 | TO14 | TO13 | TO12 | TO11 | TO10 | TO9 | TO8 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TO7 | TO6 | TO5 | TO4 | TO3 | TO2 | TO1 | TO0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 4-120. MCAN_TXBTO Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 31 | TO31 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |

Table 4-120. MCAN_TXBTO Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 30 | TO30 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 29 | TO29 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 28 | TO28 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 27 | TO27 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 26 | TO26 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 25 | TO25 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 24 | TO24 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 23 | TO23 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 22 | TO22 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 21 | TO21 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 20 | TO20 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 19 | TO19 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 18 | TO18 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 17 | TO17 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 16 | TO16 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 15 | TO15 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |

Table 4-120. MCAN_TXBTO Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 14 | TO14 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 13 | TO13 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 12 | TO12 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 11 | TO11 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 10 | TO10 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 9 | TO9 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 8 | TO8 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 7 | TO7 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 6 | TO6 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 5 | TO5 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 4 | TO4 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 3 | TO3 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 2 | TO2 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 1 | TO1 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |
| 0 | TO0 | R | 0h | Transmission Occurred 0h = No transmission occurred 1h = Transmission occurred |

4.2.41 MCAN_TXBCF Register (Offset = DCh) [reset = 0h]

MCAN_TXBCF is shown in [Figure 4-52](#) and described in [Table 4-122](#).

Return to [Summary Table](#).

Tx Buffer Cancellation Finished

Signals successful transmit cancellation, set when corresponding MCAN_TXBRP flag is cleared after cancellation request.

Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding MCAN_TXBRP bit is cleared after a cancellation was requested via the MCAN_TXBCR register. In case the corresponding MCAN_TXBRP bit was not set at the point of cancellation, MCAN_TXBCF[n] CF bit is set immediately. The bits are reset when a new transmission is requested by writing a 1h to the corresponding bit of the MCAN_TXBAR register.

Table 4-121. MCAN_TXBCF Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80DCh |
| MCU_MCAN1_CFG | 4056 80DCh |
| MCAN0_CFG | 0270 10DCh |
| MCAN1_CFG | 0271 10DCh |
| MCAN2_CFG | 0272 10DCh |
| MCAN3_CFG | 0273 10DCh |
| MCAN4_CFG | 0274 10DCh |
| MCAN5_CFG | 0275 10DCh |
| MCAN6_CFG | 0276 10DCh |
| MCAN7_CFG | 0277 10DCh |
| MCAN8_CFG | 0278 10DCh |
| MCAN9_CFG | 0279 10DCh |
| MCAN10_CFG | 027A 10DCh |
| MCAN11_CFG | 027B 10DCh |
| MCAN12_CFG | 027C 10DCh |
| MCAN13_CFG | 027D 10DCh |

Figure 4-52. MCAN_TXBCF Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------|------|------|------|------|------|------|------|
| CF31 | CF30 | CF29 | CF28 | CF27 | CF26 | CF25 | CF24 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CF23 | CF22 | CF21 | CF20 | CF19 | CF18 | CF17 | CF16 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CF15 | CF14 | CF13 | CF12 | CF11 | CF10 | CF9 | CF8 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CF7 | CF6 | CF5 | CF4 | CF3 | CF2 | CF1 | CF0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 4-122. MCAN_TXBCF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 31 | CF31 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 30 | CF30 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 29 | CF29 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 28 | CF28 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 27 | CF27 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 26 | CF26 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 25 | CF25 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 24 | CF24 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 23 | CF23 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 22 | CF22 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 21 | CF21 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 20 | CF20 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 19 | CF19 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 18 | CF18 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 17 | CF17 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 16 | CF16 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |

Table 4-122. MCAN_TXBCF Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 15 | CF15 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 14 | CF14 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 13 | CF13 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 12 | CF12 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 11 | CF11 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 10 | CF10 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 9 | CF9 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 8 | CF8 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 7 | CF7 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 6 | CF6 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 5 | CF5 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 4 | CF4 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 3 | CF3 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 2 | CF2 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 1 | CF1 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |
| 0 | CF0 | R | 0h | Cancellation Finished 0h = No transmit buffer cancellation 1h = Transmit buffer cancellation finished |

4.2.42 MCAN_TXBTIE Register (Offset = E0h) [reset = 0h]

MCAN_TXBTIE is shown in [Figure 4-53](#) and described in [Table 4-124](#).

Return to [Summary Table](#).

Tx Buffer Transmission Interrupt Enable

Enable transmit interrupts for selected Tx buffers.

Table 4-123. MCAN_TXBTIE Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80E0h |
| MCU_MCAN1_CFG | 4056 80E0h |
| MCAN0_CFG | 0270 10E0h |
| MCAN1_CFG | 0271 10E0h |
| MCAN2_CFG | 0272 10E0h |
| MCAN3_CFG | 0273 10E0h |
| MCAN4_CFG | 0274 10E0h |
| MCAN5_CFG | 0275 10E0h |
| MCAN6_CFG | 0276 10E0h |
| MCAN7_CFG | 0277 10E0h |
| MCAN8_CFG | 0278 10E0h |
| MCAN9_CFG | 0279 10E0h |
| MCAN10_CFG | 027A 10E0h |
| MCAN11_CFG | 027B 10E0h |
| MCAN12_CFG | 027C 10E0h |
| MCAN13_CFG | 027D 10E0h |

Figure 4-53. MCAN_TXBTIE Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| TIE31 | TIE30 | TIE29 | TIE28 | TIE27 | TIE26 | TIE25 | TIE24 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TIE23 | TIE22 | TIE21 | TIE20 | TIE19 | TIE18 | TIE17 | TIE16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TIE15 | TIE14 | TIE13 | TIE12 | TIE11 | TIE10 | TIE9 | TIE8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TIE7 | TIE6 | TIE5 | TIE4 | TIE3 | TIE2 | TIE1 | TIE0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-124. MCAN_TXBTIE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 31 | TIE31 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 30 | TIE30 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |

Table 4-124. MCAN_TXBTIE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 29 | TIE29 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 28 | TIE28 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 27 | TIE27 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 26 | TIE26 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 25 | TIE25 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 24 | TIE24 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 23 | TIE23 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 22 | TIE22 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 21 | TIE21 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 20 | TIE20 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 19 | TIE19 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 18 | TIE18 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 17 | TIE17 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 16 | TIE16 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 15 | TIE15 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 14 | TIE14 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |

Table 4-124. MCAN_TXBTIE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 13 | TIE13 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 12 | TIE12 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 11 | TIE11 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 10 | TIE10 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 9 | TIE9 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 8 | TIE8 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 7 | TIE7 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 6 | TIE6 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 5 | TIE5 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 4 | TIE4 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 3 | TIE3 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 2 | TIE2 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 1 | TIE1 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |
| 0 | TIE0 | R/W | 0h | Transmission Interrupt Enable 0h = Transmission interrupt disabled 1h = Transmission interrupt enable |

4.2.43 MCAN_TXBCIE Register (Offset = E4h) [reset = 0h]

MCAN_TXBCIE is shown in [Figure 4-54](#) and described in [Table 4-126](#).

Return to [Summary Table](#).

Tx Buffer Cancellation Finished Interrupt Enable

Enable cancellation finished interrupts for selected Tx buffers.

Table 4-125. MCAN_TXBCIE Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80E4h |
| MCU_MCAN1_CFG | 4056 80E4h |
| MCAN0_CFG | 0270 10E4h |
| MCAN1_CFG | 0271 10E4h |
| MCAN2_CFG | 0272 10E4h |
| MCAN3_CFG | 0273 10E4h |
| MCAN4_CFG | 0274 10E4h |
| MCAN5_CFG | 0275 10E4h |
| MCAN6_CFG | 0276 10E4h |
| MCAN7_CFG | 0277 10E4h |
| MCAN8_CFG | 0278 10E4h |
| MCAN9_CFG | 0279 10E4h |
| MCAN10_CFG | 027A 10E4h |
| MCAN11_CFG | 027B 10E4h |
| MCAN12_CFG | 027C 10E4h |
| MCAN13_CFG | 027D 10E4h |

Figure 4-54. MCAN_TXBCIE Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| CFIE31 | CFIE30 | CFIE29 | CFIE28 | CFIE27 | CFIE26 | CFIE25 | CFIE24 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CFIE23 | CFIE22 | CFIE21 | CFIE20 | CFIE19 | CFIE18 | CFIE17 | CFIE16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CFIE15 | CFIE14 | CFIE13 | CFIE12 | CFIE11 | CFIE10 | CFIE9 | CFIE8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CFIE7 | CFIE6 | CFIE5 | CFIE4 | CFIE3 | CFIE2 | CFIE1 | CFIE0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 4-126. MCAN_TXBCIE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 31 | CFIE31 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 30 | CFIE30 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |

Table 4-126. MCAN_TXBCIE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 29 | CFIE29 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 28 | CFIE28 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 27 | CFIE27 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 26 | CFIE26 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 25 | CFIE25 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 24 | CFIE24 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 23 | CFIE23 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 22 | CFIE22 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 21 | CFIE21 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 20 | CFIE20 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 19 | CFIE19 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 18 | CFIE18 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 17 | CFIE17 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 16 | CFIE16 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 15 | CFIE15 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 14 | CFIE14 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |

Table 4-126. MCAN_TXBCIE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 13 | CFIE13 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 12 | CFIE12 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 11 | CFIE11 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 10 | CFIE10 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 9 | CFIE9 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 8 | CFIE8 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 7 | CFIE7 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 6 | CFIE6 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 5 | CFIE5 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 4 | CFIE4 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 3 | CFIE3 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 2 | CFIE2 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 1 | CFIE1 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |
| 0 | CFIE0 | R/W | 0h | Cancellation Finished Interrupt Enable 0h = Cancellation finished interrupt disabled 1h = Cancellation finished interrupt enabled |

4.2.44 MCAN_TXEFC Register (Offset = F0h) [reset = 0h]

MCAN_TXEFC is shown in [Figure 4-55](#) and described in [Table 4-128](#).

Return to [Summary Table](#).

Tx Event FIFO Configuration

Tx event FIFO watermark, size and start address.

Table 4-127. MCAN_TXEFC Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80F0h |
| MCU_MCAN1_CFG | 4056 80F0h |
| MCAN0_CFG | 0270 10F0h |
| MCAN1_CFG | 0271 10F0h |
| MCAN2_CFG | 0272 10F0h |
| MCAN3_CFG | 0273 10F0h |
| MCAN4_CFG | 0274 10F0h |
| MCAN5_CFG | 0275 10F0h |
| MCAN6_CFG | 0276 10F0h |
| MCAN7_CFG | 0277 10F0h |
| MCAN8_CFG | 0278 10F0h |
| MCAN9_CFG | 0279 10F0h |
| MCAN10_CFG | 027A 10F0h |
| MCAN11_CFG | 027B 10F0h |
| MCAN12_CFG | 027C 10F0h |
| MCAN13_CFG | 027D 10F0h |

Figure 4-55. MCAN_TXEFC Register

| | | | | | | | |
|----------|----|----|----|--------|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | EFWM | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | EFS | | | |
| R-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| EFSA | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EFSA | | | | | | RESERVED | |
| R/W-0h | | | | | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-128. MCAN_TXEFC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-30 | RESERVED | R | 0h | Reserved |
| 29-24 | EFWM | R/W | 0h | Event FIFO Watermark 0h = Watermark interrupt disabled 1h-20h (1-32) = Level for Tx Event FIFO watermark interrupt (MCAN_IR[13] TEFW) > 20h (32) = Watermark interrupt disabled |

Table 4-128. MCAN_TXEFC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 23-22 | RESERVED | R | 0h | Reserved |
| 21-16 | EFS | R/W | 0h | Event FIFO Size 0h = Tx Event FIFO disabled 1h-20h (1-32) = Number of Tx Event FIFO elements > 20h (32) = Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to MCAN_TXEFC[21-16] EFS field - 1. |
| 15-2 | EFSA | R/W | 0h | Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see , <i>Message RAM Configuration</i>). |
| 1-0 | RESERVED | R | 0h | Reserved |

4.2.45 MCAN_TXEFS Register (Offset = F4h) [reset = 0h]

MCAN_TXEFS is shown in [Figure 4-56](#) and described in [Table 4-130](#).

Return to [Summary Table](#).

Tx Event FIFO Status

Tx event FIFO element lost/full indication, put index, get index, and fill level.

Table 4-129. MCAN_TXEFS Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80F4h |
| MCU_MCAN1_CFG | 4056 80F4h |
| MCAN0_CFG | 0270 10F4h |
| MCAN1_CFG | 0271 10F4h |
| MCAN2_CFG | 0272 10F4h |
| MCAN3_CFG | 0273 10F4h |
| MCAN4_CFG | 0274 10F4h |
| MCAN5_CFG | 0275 10F4h |
| MCAN6_CFG | 0276 10F4h |
| MCAN7_CFG | 0277 10F4h |
| MCAN8_CFG | 0278 10F4h |
| MCAN9_CFG | 0279 10F4h |
| MCAN10_CFG | 027A 10F4h |
| MCAN11_CFG | 027B 10F4h |
| MCAN12_CFG | 027C 10F4h |
| MCAN13_CFG | 027D 10F4h |

Figure 4-56. MCAN_TXEFS Register

| | | | | | | | |
|----------|----|----|------|------|----|------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | TEFL | EFF |
| R-0h | | | | | | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | EFPI | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | EFGI | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | EFFL | | | | |
| R-0h | | | R-0h | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-130. MCAN_TXEFS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-26 | RESERVED | R | 0h | Reserved |
| 25 | TEFL | R | 0h | This bit is a copy of interrupt flag MCAN_IR[15] TEFL. When the MCAN_IR[15] TEFL flag is reset, this bit is also reset. 0h = No Tx Event FIFO element lost 1h = Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. |

Table 4-130. MCAN_TXEFS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 24 | EFF | R | 0h | Event FIFO Full 0h = Tx Event FIFO not full 1h = Tx Event FIFO full |
| 23-21 | RESERVED | R | 0h | Reserved |
| 20-16 | EFPI | R | 0h | Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. |
| 15-13 | RESERVED | R | 0h | Reserved |
| 12-8 | EFGL | R | 0h | Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. |
| 7-6 | RESERVED | R | 0h | Reserved |
| 5-0 | EFFL | R | 0h | Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. |

4.2.46 MCAN_TXEFA Register (Offset = F8h) [reset = 0h]

MCAN_TXEFA is shown in [Figure 4-57](#) and described in [Table 4-132](#).

Return to [Summary Table](#).

Tx Event FIFO Acknowledge

Tx event FIFO acknowledge last index of read elements, updates get index and fill level.

Table 4-131. MCAN_TXEFA Instances

| Instance | Physical Address |
|---------------|------------------|
| MCU_MCAN0_CFG | 4052 80F8h |
| MCU_MCAN1_CFG | 4056 80F8h |
| MCAN0_CFG | 0270 10F8h |
| MCAN1_CFG | 0271 10F8h |
| MCAN2_CFG | 0272 10F8h |
| MCAN3_CFG | 0273 10F8h |
| MCAN4_CFG | 0274 10F8h |
| MCAN5_CFG | 0275 10F8h |
| MCAN6_CFG | 0276 10F8h |
| MCAN7_CFG | 0277 10F8h |
| MCAN8_CFG | 0278 10F8h |
| MCAN9_CFG | 0279 10F8h |
| MCAN10_CFG | 027A 10F8h |
| MCAN11_CFG | 027B 10F8h |
| MCAN12_CFG | 027C 10F8h |
| MCAN13_CFG | 027D 10F8h |

Figure 4-57. MCAN_TXEFA Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|--------|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | EFAI | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 4-132. MCAN_TXEFA Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-5 | RESERVED | R | 0h | Reserved |
| 4-0 | EFAI | R/W | 0h | After the Host CPU has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to the MCAN_TXEFA[4-0] EFAI field. This will set the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field to the MCAN_TXEFA[4-0] EFAI field + 1 and update the Event FIFO Fill Level MCAN_TXEFS[5-0] EFFL field. |

4.3 MCAN ECC Aggregator Registers

Table 4-134 lists the memory-mapped registers for the MCAN ECC Aggregator. All register offset addresses not listed in Table 4-134 should be considered as reserved locations and the register contents should not be modified.

Table 4-133. MCAN ECC Aggregator Instances

| Instance | Base Address |
|--------------------|--------------|
| MCU_MCAN0_ECC_AGGR | 4070 0000h |
| MCU_MCAN1_ECC_AGGR | 4070 1000h |
| MCAN0_ECC_AGGR | 02A7 8000h |
| MCAN1_ECC_AGGR | 02A7 9000h |
| MCAN2_ECC_AGGR | 02A7 A000h |
| MCAN3_ECC_AGGR | 02A7 B000h |
| MCAN4_ECC_AGGR | 02A7 C000h |
| MCAN5_ECC_AGGR | 02A7 D000h |
| MCAN6_ECC_AGGR | 02A7 E000h |
| MCAN7_ECC_AGGR | 02A7 F000h |
| MCAN8_ECC_AGGR | 02A4 0000h |
| MCAN9_ECC_AGGR | 02A4 1000h |
| MCAN10_ECC_AGGR | 02A4 2000h |
| MCAN11_ECC_AGGR | 02A4 3000h |
| MCAN12_ECC_AGGR | 02A4 4000h |
| MCAN13_ECC_AGGR | 02A4 5000h |

Table 4-134. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCU_MCAN0_ECC_AGGR Physical Address | MCU_MCAN1_ECC_AGGR Physical Address |
|--------|--|--|-------------------------------------|-------------------------------------|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 4070 0000h | 4070 1000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 4070 0008h | 4070 1008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 4070 000Ch | 4070 100Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 4070 003Ch | 4070 103Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 4070 0040h | 4070 1040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 4070 0080h | 4070 1080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 4070 00C0h | 4070 10C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 4070 013Ch | 4070 113Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 4070 0140h | 4070 1140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 4070 0180h | 4070 1180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 4070 01C0h | 4070 11C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 4070 0200h | 4070 1200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 4070 0204h | 4070 1204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 4070 0208h | 4070 1208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 4070 020Ch | 4070 120Ch |

Table 4-135. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN0_ECC_A GGR Physical Address | MCAN1_ECC_A GGR Physical Address |
|--------|--|--|--|--|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A7 8000h | 02A7 9000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A7 8008h | 02A7 9008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A7 800Ch | 02A7 900Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A7 803Ch | 02A7 903Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A7 8040h | 02A7 9040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A7 8080h | 02A7 9080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A7 80C0h | 02A7 90C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A7 813Ch | 02A7 913Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A7 8140h | 02A7 9140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A7 8180h | 02A7 9180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A7 81C0h | 02A7 91C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A7 8200h | 02A7 9200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A7 8204h | 02A7 9204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A7 8208h | 02A7 9208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A7 820Ch | 02A7 920Ch |

Table 4-136. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN2_ECC_A GGR Physical Address | MCAN3_ECC_A GGR Physical Address |
|--------|--|--|--|--|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A7 A000h | 02A7 B000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A7 A008h | 02A7 B008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A7 A00Ch | 02A7 B00Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A7 A03Ch | 02A7 B03Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A7 A040h | 02A7 B040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A7 A080h | 02A7 B080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A7 A0C0h | 02A7 B0C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A7 A13Ch | 02A7 B13Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A7 A140h | 02A7 B140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A7 A180h | 02A7 B180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A7 A1C0h | 02A7 B1C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A7 A200h | 02A7 B200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A7 A204h | 02A7 B204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A7 A208h | 02A7 B208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A7 A20Ch | 02A7 B20Ch |

Table 4-137. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN4_ECC_A GGR Physical Address | MCAN5_ECC_A GGR Physical Address |
|--------|--|--|--|--|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A7 C000h | 02A7 D000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A7 C008h | 02A7 D008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A7 C00Ch | 02A7 D00Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A7 C03Ch | 02A7 D03Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A7 C040h | 02A7 D040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A7 C080h | 02A7 D080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A7 C0C0h | 02A7 D0C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A7 C13Ch | 02A7 D13Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A7 C140h | 02A7 D140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A7 C180h | 02A7 D180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A7 C1C0h | 02A7 D1C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A7 C200h | 02A7 D200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A7 C204h | 02A7 D204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A7 C208h | 02A7 D208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A7 C20Ch | 02A7 D20Ch |

Table 4-138. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN6_ECC_A GGR Physical Address | MCAN7_ECC_A GGR Physical Address |
|--------|--|--|--|--|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A7 E000h | 02A7 F000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A7 E008h | 02A7 F008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A7 E00Ch | 02A7 F00Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A7 E03Ch | 02A7 F03Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A7 E040h | 02A7 F040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A7 E080h | 02A7 F080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A7 E0C0h | 02A7 F0C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A7 E13Ch | 02A7 F13Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A7 E140h | 02A7 F140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A7 E180h | 02A7 F180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A7 E1C0h | 02A7 F1C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A7 E200h | 02A7 F200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A7 E204h | 02A7 F204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A7 E208h | 02A7 F208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A7 E20Ch | 02A7 F20Ch |

Table 4-139. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN8_ECC_A GGR Physical Address | MCAN9_ECC_A GGR Physical Address |
|--------|--|--|--|--|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A4 0000h | 02A4 1000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A4 0008h | 02A4 1008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A4 000Ch | 02A4 100Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A4 003Ch | 02A4 103Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A4 0040h | 02A4 1040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A4 0080h | 02A4 1080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A4 00C0h | 02A4 10C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A4 013Ch | 02A4 113Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A4 0140h | 02A4 1140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A4 0180h | 02A4 1180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A4 01C0h | 02A4 11C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A4 0200h | 02A4 1200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A4 0204h | 02A4 1204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A4 0208h | 02A4 1208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A4 020Ch | 02A4 120Ch |

Table 4-140. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN10_ECC_ AGGR Physical Address | MCAN11_ECC_ AGGR Physical Address |
|--------|--|--|---|---|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A4 2000h | 02A4 3000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A4 2008h | 02A4 3008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A4 200Ch | 02A4 300Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A4 203Ch | 02A4 303Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A4 2040h | 02A4 3040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A4 2080h | 02A4 3080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A4 20C0h | 02A4 30C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A4 213Ch | 02A4 313Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A4 2140h | 02A4 3140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A4 2180h | 02A4 3180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A4 21C0h | 02A4 31C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A4 2200h | 02A4 3200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A4 2204h | 02A4 3204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A4 2208h | 02A4 3208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A4 220Ch | 02A4 320Ch |

Table 4-141. MCAN ECC Aggregator Registers

| Offset | Acronym | Register Name | MCAN12_ECC_ AGGR Physical Address | MCAN13_ECC_ AGGR Physical Address |
|--------|--|--|---|---|
| 0h | MCANSS_ECC_REV | Aggregator Revision Register | 02A4 4000h | 02A4 5000h |
| 8h | MCANSS_ECC_VECTOR | ECC Vector Register | 02A4 4008h | 02A4 5008h |
| Ch | MCANSS_ECC_STAT | Misc Status Register | 02A4 400Ch | 02A4 500Ch |
| 3Ch | MCANSS_ECC_SEC_EOI_REG | SEC EOI Register | 02A4 403Ch | 02A4 503Ch |
| 40h | MCANSS_ECC_SEC_STATUS_REG0 | SEC Interrupt Status Register 0 | 02A4 4040h | 02A4 5040h |
| 80h | MCANSS_ECC_SEC_ENABLE_SET_REG0 | SEC Interrupt Enable Set Register 0 | 02A4 4080h | 02A4 5080h |
| C0h | MCANSS_ECC_SEC_ENABLE_CLR_REG0 | SEC Interrupt Enable Clear Register 0 | 02A4 40C0h | 02A4 50C0h |
| 13Ch | MCANSS_ECC_DED_EOI_REG | DED EOI Register | 02A4 413Ch | 02A4 513Ch |
| 140h | MCANSS_ECC_DED_STATUS_REG0 | DED Interrupt Status Register 0 | 02A4 4140h | 02A4 5140h |
| 180h | MCANSS_ECC_DED_ENABLE_SET_REG0 | DED Interrupt Enable Set Register 0 | 02A4 4180h | 02A4 5180h |
| 1C0h | MCANSS_ECC_DED_ENABLE_CLR_REG0 | DED Interrupt Enable Clear Register 0 | 02A4 41C0h | 02A4 51C0h |
| 200h | MCANSS_ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Set Register | 02A4 4200h | 02A4 5200h |
| 204h | MCANSS_ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Enable Clear Register | 02A4 4204h | 02A4 5204h |
| 208h | MCANSS_ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register | 02A4 4208h | 02A4 5208h |
| 20Ch | MCANSS_ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register | 02A4 420Ch | 02A4 520Ch |

4.3.1 MCANSS_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

MCANSS_ECC_REV is shown in [Figure 4-58](#) and described in [Table 4-143](#).

Return to [Summary Table](#).

Aggregator Revision Register

The Aggregator Revision Register contains the revision parameters for the ECC Aggregator.

Table 4-142. MCANSS_ECC_REV Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0000h |
| MCU_MCAN1_ECC_AGGR | 4070 1000h |
| MCAN0_ECC_AGGR | 02A7 8000h |
| MCAN1_ECC_AGGR | 02A7 9000h |
| MCAN2_ECC_AGGR | 02A7 A000h |
| MCAN3_ECC_AGGR | 02A7 B000h |
| MCAN4_ECC_AGGR | 02A7 C000h |
| MCAN5_ECC_AGGR | 02A7 D000h |
| MCAN6_ECC_AGGR | 02A7 E000h |
| MCAN7_ECC_AGGR | 02A7 F000h |
| MCAN8_ECC_AGGR | 02A4 0000h |
| MCAN9_ECC_AGGR | 02A4 1000h |
| MCAN10_ECC_AGGR | 02A4 2000h |
| MCAN11_ECC_AGGR | 02A4 3000h |
| MCAN12_ECC_AGGR | 02A4 4000h |
| MCAN13_ECC_AGGR | 02A4 5000h |

Figure 4-58. MCANSS_ECC_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|------|--------|-----------|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | | | BU | | MODULE_ID | | | | | | | | | |
| R-1h | | | | R-2h | | R-6A0h | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-143. MCANSS_ECC_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | Business Unit |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL Version |
| 10-8 | REVMAJ | R | 2h | Major Version |
| 7-6 | CUSTOM | R | 0h | Custom Version |
| 5-0 | REVMIN | R | 0h | Minor Version |

4.3.2 MCANSS_ECC_VECTOR Register (Offset = 8h) [reset = 0h]

MCANSS_ECC_VECTOR is shown in [Figure 4-59](#) and described in [Table 4-145](#).

Return to [Summary Table](#).

ECC Vector Register

Table 4-144. MCANSS_ECC_VECTOR Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0008h |
| MCU_MCAN1_ECC_AGGR | 4070 1008h |
| MCAN0_ECC_AGGR | 02A7 8008h |
| MCAN1_ECC_AGGR | 02A7 9008h |
| MCAN2_ECC_AGGR | 02A7 A008h |
| MCAN3_ECC_AGGR | 02A7 B008h |
| MCAN4_ECC_AGGR | 02A7 C008h |
| MCAN5_ECC_AGGR | 02A7 D008h |
| MCAN6_ECC_AGGR | 02A7 E008h |
| MCAN7_ECC_AGGR | 02A7 F008h |
| MCAN8_ECC_AGGR | 02A4 0008h |
| MCAN9_ECC_AGGR | 02A4 1008h |
| MCAN10_ECC_AGGR | 02A4 2008h |
| MCAN11_ECC_AGGR | 02A4 3008h |
| MCAN12_ECC_AGGR | 02A4 4008h |
| MCAN13_ECC_AGGR | 02A4 5008h |

Figure 4-59. MCANSS_ECC_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_D ONE |
| R-0h | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R-0h | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-145. MCANSS_ECC_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R | 0h | Reserved |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Read Done Status to indicate if read on the serial ECC interface is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read Address |

Table 4-145. MCANSS_ECC_VECTOR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|------------|-------|-------|--|
| 15 | RD_SVBUS | R/W1S | 0h | Read Trigger Write 1h to trigger a read on the serial ECC interface. |
| 14-11 | RESERVED | R | 0h | Reserved |
| 10-0 | ECC_VECTOR | R/W | 0h | ECC RAM ID Value written to select the corresponding ECC RAM for control or status. |

4.3.3 MCANSS_ECC_STAT Register (Offset = Ch) [reset = 2h]

MCANSS_ECC_STAT is shown in [Figure 4-60](#) and described in [Table 4-147](#).

Return to [Summary Table](#).

Misc Status Register

Table 4-146. MCANSS_ECC_STAT Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 000Ch |
| MCU_MCAN1_ECC_AGGR | 4070 100Ch |
| MCAN0_ECC_AGGR | 02A7 800Ch |
| MCAN1_ECC_AGGR | 02A7 900Ch |
| MCAN2_ECC_AGGR | 02A7 A00Ch |
| MCAN3_ECC_AGGR | 02A7 B00Ch |
| MCAN4_ECC_AGGR | 02A7 C00Ch |
| MCAN5_ECC_AGGR | 02A7 D00Ch |
| MCAN6_ECC_AGGR | 02A7 E00Ch |
| MCAN7_ECC_AGGR | 02A7 F00Ch |
| MCAN8_ECC_AGGR | 02A4 000Ch |
| MCAN9_ECC_AGGR | 02A4 100Ch |
| MCAN10_ECC_AGGR | 02A4 200Ch |
| MCAN11_ECC_AGGR | 02A4 300Ch |
| MCAN12_ECC_AGGR | 02A4 400Ch |
| MCAN13_ECC_AGGR | 02A4 500Ch |

Figure 4-60. MCANSS_ECC_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | R-2h | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 4-147. MCANSS_ECC_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-11 | RESERVED | R | 0h | Reserved |
| 10-0 | NUM_RAMs | R | 2h | Number of RAMs Indicates the number of RAMs serviced by the ECC Aggregator. |

4.3.4 MCANSS_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

MCANSS_ECC_SEC_EOI_REG is shown in [Figure 4-61](#) and described in [Table 4-149](#).

Return to [Summary Table](#).

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 4-148. MCANSS_ECC_SEC_EOI_REG
Instances**

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 003Ch |
| MCU_MCAN1_ECC_AGGR | 4070 103Ch |
| MCAN0_ECC_AGGR | 02A7 803Ch |
| MCAN1_ECC_AGGR | 02A7 903Ch |
| MCAN2_ECC_AGGR | 02A7 A03Ch |
| MCAN3_ECC_AGGR | 02A7 B03Ch |
| MCAN4_ECC_AGGR | 02A7 C03Ch |
| MCAN5_ECC_AGGR | 02A7 D03Ch |
| MCAN6_ECC_AGGR | 02A7 E03Ch |
| MCAN7_ECC_AGGR | 02A7 F03Ch |
| MCAN8_ECC_AGGR | 02A4 003Ch |
| MCAN9_ECC_AGGR | 02A4 103Ch |
| MCAN10_ECC_AGGR | 02A4 203Ch |
| MCAN11_ECC_AGGR | 02A4 303Ch |
| MCAN12_ECC_AGGR | 02A4 403Ch |
| MCAN13_ECC_AGGR | 02A4 503Ch |

Figure 4-61. MCANSS_ECC_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R-0h | | | | | | | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-149. MCANSS_ECC_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-1 | RESERVED | R | 0h | Reserved |

Table 4-149. MCANSS_ECC_SEC_EOI_REG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|-------|-------|--|
| 0 | EOI_WR | R/W1S | 0h | Single Error Correction End Of Interrupt (SEC EOI) |

4.3.5 MCANSS_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

MCANSS_ECC_SEC_STATUS_REG0 is shown in [Figure 4-62](#) and described in [Table 4-151](#).

Return to [Summary Table](#).

SEC Interrupt Status Register 0

**Table 4-150. MCANSS_ECC_SEC_STATUS_REG0
Instances**

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0040h |
| MCU_MCAN1_ECC_AGGR | 4070 1040h |
| MCAN0_ECC_AGGR | 02A7 8040h |
| MCAN1_ECC_AGGR | 02A7 9040h |
| MCAN2_ECC_AGGR | 02A7 A040h |
| MCAN3_ECC_AGGR | 02A7 B040h |
| MCAN4_ECC_AGGR | 02A7 C040h |
| MCAN5_ECC_AGGR | 02A7 D040h |
| MCAN6_ECC_AGGR | 02A7 E040h |
| MCAN7_ECC_AGGR | 02A7 F040h |
| MCAN8_ECC_AGGR | 02A4 0040h |
| MCAN9_ECC_AGGR | 02A4 1040h |
| MCAN10_ECC_AGGR | 02A4 2040h |
| MCAN11_ECC_AGGR | 02A4 3040h |
| MCAN12_ECC_AGGR | 02A4 4040h |
| MCAN13_ECC_AGGR | 02A4 5040h |

Figure 4-62. MCANSS_ECC_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------------------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CTRL_EDC_VB USS_PEND | MSGMEM_PEN D |
| R-0h | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-151. MCANSS_ECC_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CTRL_EDC_VBUSS_PEN D | R/W1S | 0h | Interrupt Pending Status for CTRL_EDC_VBUSS_PEND |
| 0 | MSGMEM_PEND | R/W1S | 0h | Interrupt Pending Status for MSGMEM_PEND |

4.3.6 MCANSS_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

MCANSS_ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 4-63](#) and described in [Table 4-153](#).

Return to [Summary Table](#).

SEC Interrupt Enable Set Register 0

Table 4-152.
MCANSS_ECC_SEC_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0080h |
| MCU_MCAN1_ECC_AGGR | 4070 1080h |
| MCAN0_ECC_AGGR | 02A7 8080h |
| MCAN1_ECC_AGGR | 02A7 9080h |
| MCAN2_ECC_AGGR | 02A7 A080h |
| MCAN3_ECC_AGGR | 02A7 B080h |
| MCAN4_ECC_AGGR | 02A7 C080h |
| MCAN5_ECC_AGGR | 02A7 D080h |
| MCAN6_ECC_AGGR | 02A7 E080h |
| MCAN7_ECC_AGGR | 02A7 F080h |
| MCAN8_ECC_AGGR | 02A4 0080h |
| MCAN9_ECC_AGGR | 02A4 1080h |
| MCAN10_ECC_AGGR | 02A4 2080h |
| MCAN11_ECC_AGGR | 02A4 3080h |
| MCAN12_ECC_AGGR | 02A4 4080h |
| MCAN13_ECC_AGGR | 02A4 5080h |

Figure 4-63. MCANSS_ECC_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CTRL_EDC_VB USS_ENABLE_ SET | MSGMEM_ENA BLE_SET |
| R-0h | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-153. MCANSS_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CTRL_EDC_VBUSS_ENA BLE_SET | R/W1S | 0h | Interrupt Enable Set for CTRL_EDC_VBUSS_PEND |

Table 4-153. MCANSS_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--------------------------------------|
| 0 | MSGMEM_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set for MSGMEM_PEND |

4.3.7 MCANSS_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

MCANSS_ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 4-64](#) and described in [Table 4-155](#).

Return to [Summary Table](#).

SEC Interrupt Enable Clear Register 0

Table 4-154.
MCANSS_ECC_SEC_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 00C0h |
| MCU_MCAN1_ECC_AGGR | 4070 10C0h |
| MCAN0_ECC_AGGR | 02A7 80C0h |
| MCAN1_ECC_AGGR | 02A7 90C0h |
| MCAN2_ECC_AGGR | 02A7 A0C0h |
| MCAN3_ECC_AGGR | 02A7 B0C0h |
| MCAN4_ECC_AGGR | 02A7 C0C0h |
| MCAN5_ECC_AGGR | 02A7 D0C0h |
| MCAN6_ECC_AGGR | 02A7 E0C0h |
| MCAN7_ECC_AGGR | 02A7 F0C0h |
| MCAN8_ECC_AGGR | 02A4 00C0h |
| MCAN9_ECC_AGGR | 02A4 10C0h |
| MCAN10_ECC_AGGR | 02A4 20C0h |
| MCAN11_ECC_AGGR | 02A4 30C0h |
| MCAN12_ECC_AGGR | 02A4 40C0h |
| MCAN13_ECC_AGGR | 02A4 50C0h |

Figure 4-64. MCANSS_ECC_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CTRL_EDC_VB USS_ENABLE_ CLR | MSGMEM_ENA BLE_CLR |
| R-0h | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-155. MCANSS_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CTRL_EDC_VBUSS_ENA BLE_CLR | R/W1C | 0h | Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND |

Table 4-155. MCANSS_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 0 | MSGMEM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear for MSGMEM_PEND |

4.3.8 MCANSS_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

MCANSS_ECC_DED_EOI_REG is shown in [Figure 4-65](#) and described in [Table 4-157](#).

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 4-156. MCANSS_ECC_DED_EOI_REG Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 013Ch |
| MCU_MCAN1_ECC_AGGR | 4070 113Ch |
| MCAN0_ECC_AGGR | 02A7 813Ch |
| MCAN1_ECC_AGGR | 02A7 913Ch |
| MCAN2_ECC_AGGR | 02A7 A13Ch |
| MCAN3_ECC_AGGR | 02A7 B13Ch |
| MCAN4_ECC_AGGR | 02A7 C13Ch |
| MCAN5_ECC_AGGR | 02A7 D13Ch |
| MCAN6_ECC_AGGR | 02A7 E13Ch |
| MCAN7_ECC_AGGR | 02A7 F13Ch |
| MCAN8_ECC_AGGR | 02A4 013Ch |
| MCAN9_ECC_AGGR | 02A4 113Ch |
| MCAN10_ECC_AGGR | 02A4 213Ch |
| MCAN11_ECC_AGGR | 02A4 313Ch |
| MCAN12_ECC_AGGR | 02A4 413Ch |
| MCAN13_ECC_AGGR | 02A4 513Ch |

Figure 4-65. MCANSS_ECC_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R-0h | | | | | | | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-157. MCANSS_ECC_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-1 | RESERVED | R | 0h | Reserved |

Table 4-157. MCANSS_ECC_DED_EOI_REG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|-------|-------|--|
| 0 | EOI_WR | R/W1S | 0h | Double Error Correction End Of Interrupt (DED EOI) |

4.3.9 MCANSS_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

MCANSS_ECC_DED_STATUS_REG0 is shown in [Figure 4-66](#) and described in [Table 4-159](#).

Return to [Summary Table](#).

DED Interrupt Status Register 0

Table 4-158. MCANSS_ECC_DED_STATUS_REG0 Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0140h |
| MCU_MCAN1_ECC_AGGR | 4070 1140h |
| MCAN0_ECC_AGGR | 02A7 8140h |
| MCAN1_ECC_AGGR | 02A7 9140h |
| MCAN2_ECC_AGGR | 02A7 A140h |
| MCAN3_ECC_AGGR | 02A7 B140h |
| MCAN4_ECC_AGGR | 02A7 C140h |
| MCAN5_ECC_AGGR | 02A7 D140h |
| MCAN6_ECC_AGGR | 02A7 E140h |
| MCAN7_ECC_AGGR | 02A7 F140h |
| MCAN8_ECC_AGGR | 02A4 0140h |
| MCAN9_ECC_AGGR | 02A4 1140h |
| MCAN10_ECC_AGGR | 02A4 2140h |
| MCAN11_ECC_AGGR | 02A4 3140h |
| MCAN12_ECC_AGGR | 02A4 4140h |
| MCAN13_ECC_AGGR | 02A4 5140h |

Figure 4-66. MCANSS_ECC_DED_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------------------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CTRL_EDC_VB USS_PEND | MSGMEM_PEN D |
| R-0h | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-159. MCANSS_ECC_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CTRL_EDC_VBUSS_PEN D | R/W1S | 0h | Interrupt Pending Status for CTRL_EDC_VBUSS_PEND |
| 0 | MSGMEM_PEND | R/W1S | 0h | Interrupt Pending Status for MSGMEM_PEND |

4.3.10 MCANSS_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

MCANSS_ECC_DED_ENABLE_SET_REG0 is shown in [Figure 4-67](#) and described in [Table 4-161](#).

Return to [Summary Table](#).

DED Interrupt Enable Set Register 0

Table 4-160.
MCANSS_ECC_DED_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0180h |
| MCU_MCAN1_ECC_AGGR | 4070 1180h |
| MCAN0_ECC_AGGR | 02A7 8180h |
| MCAN1_ECC_AGGR | 02A7 9180h |
| MCAN2_ECC_AGGR | 02A7 A180h |
| MCAN3_ECC_AGGR | 02A7 B180h |
| MCAN4_ECC_AGGR | 02A7 C180h |
| MCAN5_ECC_AGGR | 02A7 D180h |
| MCAN6_ECC_AGGR | 02A7 E180h |
| MCAN7_ECC_AGGR | 02A7 F180h |
| MCAN8_ECC_AGGR | 02A4 0180h |
| MCAN9_ECC_AGGR | 02A4 1180h |
| MCAN10_ECC_AGGR | 02A4 2180h |
| MCAN11_ECC_AGGR | 02A4 3180h |
| MCAN12_ECC_AGGR | 02A4 4180h |
| MCAN13_ECC_AGGR | 02A4 5180h |

Figure 4-67. MCANSS_ECC_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CTRL_EDC_VB USS_ENABLE_ SET | MSGMEM_ENA BLE_SET |
| R-0h | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-161. MCANSS_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CTRL_EDC_VBUSS_ENA BLE_SET | R/W1S | 0h | Interrupt Enable Set for CTRL_EDC_VBUSS_PEND |

Table 4-161. MCANSS_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--------------------------------------|
| 0 | MSGMEM_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set for MSGMEM_PEND |

4.3.11 MCANSS_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

MCANSS_ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 4-68](#) and described in [Table 4-163](#).

Return to [Summary Table](#).

DED Interrupt Enable Clear Register 0

Table 4-162.
MCANSS_ECC_DED_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 01C0h |
| MCU_MCAN1_ECC_AGGR | 4070 11C0h |
| MCAN0_ECC_AGGR | 02A7 81C0h |
| MCAN1_ECC_AGGR | 02A7 91C0h |
| MCAN2_ECC_AGGR | 02A7 A1C0h |
| MCAN3_ECC_AGGR | 02A7 B1C0h |
| MCAN4_ECC_AGGR | 02A7 C1C0h |
| MCAN5_ECC_AGGR | 02A7 D1C0h |
| MCAN6_ECC_AGGR | 02A7 E1C0h |
| MCAN7_ECC_AGGR | 02A7 F1C0h |
| MCAN8_ECC_AGGR | 02A4 01C0h |
| MCAN9_ECC_AGGR | 02A4 11C0h |
| MCAN10_ECC_AGGR | 02A4 21C0h |
| MCAN11_ECC_AGGR | 02A4 31C0h |
| MCAN12_ECC_AGGR | 02A4 41C0h |
| MCAN13_ECC_AGGR | 02A4 51C0h |

Figure 4-68. MCANSS_ECC_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CTRL_EDC_VB USS_ENABLE_ CLR | MSGMEM_ENA BLE_CLR |
| R-0h | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-163. MCANSS_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CTRL_EDC_VBUSS_ENA BLE_CLR | R/W1C | 0h | Interrupt Enable Clear for CTRL_EDC_VBUSS_PEND |

Table 4-163. MCANSS_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 0 | MSGMEM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear for MSGMEM_PEND |

4.3.12 MCANSS_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

MCANSS_ECC_AGGR_ENABLE_SET is shown in [Figure 4-69](#) and described in [Table 4-165](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Table 4-164. MCANSS_ECC_AGGR_ENABLE_SET Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0200h |
| MCU_MCAN1_ECC_AGGR | 4070 1200h |
| MCAN0_ECC_AGGR | 02A7 8200h |
| MCAN1_ECC_AGGR | 02A7 9200h |
| MCAN2_ECC_AGGR | 02A7 A200h |
| MCAN3_ECC_AGGR | 02A7 B200h |
| MCAN4_ECC_AGGR | 02A7 C200h |
| MCAN5_ECC_AGGR | 02A7 D200h |
| MCAN6_ECC_AGGR | 02A7 E200h |
| MCAN7_ECC_AGGR | 02A7 F200h |
| MCAN8_ECC_AGGR | 02A4 0200h |
| MCAN9_ECC_AGGR | 02A4 1200h |
| MCAN10_ECC_AGGR | 02A4 2200h |
| MCAN11_ECC_AGGR | 02A4 3200h |
| MCAN12_ECC_AGGR | 02A4 4200h |
| MCAN13_ECC_AGGR | 02A4 5200h |

Figure 4-69. MCANSS_ECC_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R-0h | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 4-165. MCANSS_ECC_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | TIMEOUT | R/W1S | 0h | Interrupt Enable Set for Serial ECC Interface Timeout Errors |
| 0 | PARITY | R/W1S | 0h | Interrupt Enable Set for Parity Errors |

4.3.13 MCANSS_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

MCANSS_ECC_AGGR_ENABLE_CLR is shown in [Figure 4-70](#) and described in [Table 4-167](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Table 4-166. MCANSS_ECC_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0204h |
| MCU_MCAN1_ECC_AGGR | 4070 1204h |
| MCAN0_ECC_AGGR | 02A7 8204h |
| MCAN1_ECC_AGGR | 02A7 9204h |
| MCAN2_ECC_AGGR | 02A7 A204h |
| MCAN3_ECC_AGGR | 02A7 B204h |
| MCAN4_ECC_AGGR | 02A7 C204h |
| MCAN5_ECC_AGGR | 02A7 D204h |
| MCAN6_ECC_AGGR | 02A7 E204h |
| MCAN7_ECC_AGGR | 02A7 F204h |
| MCAN8_ECC_AGGR | 02A4 0204h |
| MCAN9_ECC_AGGR | 02A4 1204h |
| MCAN10_ECC_AGGR | 02A4 2204h |
| MCAN11_ECC_AGGR | 02A4 3204h |
| MCAN12_ECC_AGGR | 02A4 4204h |
| MCAN13_ECC_AGGR | 02A4 5204h |

Figure 4-70. MCANSS_ECC_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R-0h | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 4-167. MCANSS_ECC_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | TIMEOUT | R/W1C | 0h | Interrupt Enable Clear for Serial ECC Interface Timeout Errors |
| 0 | PARITY | R/W1C | 0h | Interrupt Enable Clear for Parity Errors |

4.3.14 MCANSS_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

MCANSS_ECC_AGGR_STATUS_SET is shown in [Figure 4-71](#) and described in [Table 4-169](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Table 4-168. MCANSS_ECC_AGGR_STATUS_SET Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 0208h |
| MCU_MCAN1_ECC_AGGR | 4070 1208h |
| MCAN0_ECC_AGGR | 02A7 8208h |
| MCAN1_ECC_AGGR | 02A7 9208h |
| MCAN2_ECC_AGGR | 02A7 A208h |
| MCAN3_ECC_AGGR | 02A7 B208h |
| MCAN4_ECC_AGGR | 02A7 C208h |
| MCAN5_ECC_AGGR | 02A7 D208h |
| MCAN6_ECC_AGGR | 02A7 E208h |
| MCAN7_ECC_AGGR | 02A7 F208h |
| MCAN8_ECC_AGGR | 02A4 0208h |
| MCAN9_ECC_AGGR | 02A4 1208h |
| MCAN10_ECC_AGGR | 02A4 2208h |
| MCAN11_ECC_AGGR | 02A4 3208h |
| MCAN12_ECC_AGGR | 02A4 4208h |
| MCAN13_ECC_AGGR | 02A4 5208h |

Figure 4-71. MCANSS_ECC_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R-0h | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R = Read Only; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 4-169. MCANSS_ECC_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved |
| 3-2 | TIMEOUT | R/Wincr | 0h | Interrupt Status Set for Serial ECC Interface Timeout Errors |
| 1-0 | PARITY | R/Wincr | 0h | Interrupt Status Set for Parity Errors |

4.3.15 MCANSS_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

MCANSS_ECC_AGGR_STATUS_CLR is shown in [Figure 4-72](#) and described in [Table 4-171](#).

[Return to Summary Table.](#)

Aggregator Interrupt Status Clear Register

Table 4-170. MCANSS_ECC_AGGR_STATUS_CLR Instances

| Instance | Physical Address |
|--------------------|------------------|
| MCU_MCAN0_ECC_AGGR | 4070 020Ch |
| MCU_MCAN1_ECC_AGGR | 4070 120Ch |
| MCAN0_ECC_AGGR | 02A7 820Ch |
| MCAN1_ECC_AGGR | 02A7 920Ch |
| MCAN2_ECC_AGGR | 02A7 A20Ch |
| MCAN3_ECC_AGGR | 02A7 B20Ch |
| MCAN4_ECC_AGGR | 02A7 C20Ch |
| MCAN5_ECC_AGGR | 02A7 D20Ch |
| MCAN6_ECC_AGGR | 02A7 E20Ch |
| MCAN7_ECC_AGGR | 02A7 F20Ch |
| MCAN8_ECC_AGGR | 02A4 020Ch |
| MCAN9_ECC_AGGR | 02A4 120Ch |
| MCAN10_ECC_AGGR | 02A4 220Ch |
| MCAN11_ECC_AGGR | 02A4 320Ch |
| MCAN12_ECC_AGGR | 02A4 420Ch |
| MCAN13_ECC_AGGR | 02A4 520Ch |

Figure 4-72. MCANSS_ECC_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R-0h | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R = Read Only; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 4-171. MCANSS_ECC_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved |
| 3-2 | TIMEOUT | R/Wdecr | 0h | Interrupt Status Clear for Serial ECC Interface Timeout Errors |
| 1-0 | PARITY | R/Wdecr | 0h | Interrupt Status Clear for Parity Errors |

5 ATL Registers

Table 5-2 lists the ATL registers. All register locations not listed in Table 5-2 should be considered as reserved locations and the register contents should not be modified.

The ATL Control Registers region is accessed by setting the req signal to 1 during the access. The address map for this region is as follows:

Table 5-1. ATL Instances

| Instance | Base Address |
|----------|--------------|
| ATL0_REG | 031F 0000h |

Table 5-2. ATL Registers

| Offset | Acronym | Register Name | ATL0_REG Physical Address |
|--------|------------------------------|---------------------------------|---------------------------------|
| 0h | ATL_REVISION | Peripheral Revision Register | 031F 0000h |
| 200h | ATL0_PPMR | ATL0 Parts Per Million Register | 031F 0200h |
| 204h | ATL0_BBSR | ATL0 Baseband Sampler Register | 031F 0204h |
| 208h | ATL0_ATLCR | ATL0 Configuration Register | 031F 0208h |
| 210h | ATL0_SWEN | ATL0 Software Enable | 031F 0210h |
| 214h | ATL0_BWSMUX | ATL0 BWS Mux Select | 031F 0214h |
| 218h | ATL0_AWSMUX | ATL0 AWS Mux Select | 031F 0218h |
| 21Ch | ATL0_PCLKMUX | ATL PCLK Mux Select | 031F 021Ch |
| 280h | ATL1_PPMR | ATL1 Parts Per Million Register | 031F 0280h |
| 284h | ATL1_BBSR | ATL1 Baseband Sampler Register | 031F 0284h |
| 288h | ATL1_ATLCR | ATL1 Configuration Register | 031F 0288h |
| 290h | ATL1_SWEN | ATL1 Software Enable | 031F 0290h |
| 294h | ATL1_BWSMUX | ATL1 BWS Mux Select | 031F 0294h |
| 298h | ATL1_AWSMUX | ATL1 AWS Mux Select | 031F 0298h |
| 29Ch | ATL1_PCLKMUX | ATL1 PCLK Mux Select | 031F 029Ch |
| 300h | ATL2_PPMR | ATL2 Parts Per Million Register | 031F 0300h |
| 304h | ATL2_BBSR | ATL2 Baseband Sampler Register | 031F 0304h |
| 308h | ATL2_ATLCR | ATL2 Configuration Register | 031F 0308h |
| 310h | ATL2_SWEN | ATL2 Software Enable | 031F 0310h |
| 314h | ATL2_BWSMUX | ATL2 BWS Mux Select | 031F 0314h |
| 318h | ATL2_AWSMUX | ATL2 AWS Mux Select | 031F 0318h |
| 31Ch | ATL2_PCLKMUX | ATL2 PCLK Mux Select | 031F 031Ch |
| 380h | ATL3_PPMR | ATL3 Parts Per Million Register | 031F 0380h |
| 384h | ATL3_BBSR | ATL3 Baseband Sampler Register | 031F 0384h |
| 388h | ATL3_ATLCR | ATL3 Configuration Register | 031F 0388h |
| 390h | ATL3_SWEN | ATL3 Software Enable | 031F 0390h |
| 394h | ATL3_BWSMUX | ATL3 BWS Mux Select | 031F 0394h |
| 398h | ATL3_AWSMUX | ATL3 AWS Mux Select | 031F 0398h |
| 39Ch | ATL3_PCLKMUX | ATL3 PCLK Mux Select | 031F 039Ch |

5.1 ATL_REVISION Register (Offset = 0h) [reset = 0A072100h]

ATL_REVISION is shown in [Figure 5-1](#) and described in [Table 5-4](#).

Return to the [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 5-3. ATL_REVISION Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0000h |

Figure 5-1. ATL_REVISION Register

| | | | | | | | |
|----------|----|----------|----|----------|-------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SCHEME | | RESERVED | | FUNCTION | | | |
| R-0h | | R-0h | | R-A07h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FUNCTION | | | | | | | |
| R-A07h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RTL | | | | | MAJOR | | |
| R-4h | | | | | R-1h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM | | MINOR | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 5-4. ATL_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-30 | SCHEME | R | 0h | PID register scheme |
| 29-28 | RESERVED | R | 0h | Reserved |
| 27-16 | FUNCTION | R | A07h | Module ID |
| 15-11 | RTL | R | 4h | RTL ATL_REVISION. Will vary depending on release. |
| 10-8 | MAJOR | R | 1h | Major ATL_REVISION |
| 7-6 | CUSTOM | R | 0h | Custom |
| 5-0 | MINOR | R | 0h | Minor ATL_REVISION |

5.2 ATL0_PPMR Register (Offset = 200h) [reset = X]

ATL0_PPMR is shown in [Figure 5-2](#) and described in [Table 5-6](#).

Return to the [Summary Table](#).

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

Table 5-5. ATL0_PPMR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0200h |

Figure 5-2. ATL0_PPMR Register

| | | | | | | | |
|----------|----------|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PPM_SD | RESERVED | | | | | | PPM_SET |
| R/W-0h | R/W-X | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPM_SET | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-6. ATL0_PPMR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15 | PPM_SD | R/W | 0h | 1 = Slow down 0 = Speed up |
| 14-9 | RESERVED | R/W | X | |
| 8-0 | PPM_SET | R/W | 0h | This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2 ²⁰ |

5.3 ATL0_BBSR Register (Offset = 204h) [reset = X]

ATL0_BBSR is shown in [Figure 5-3](#) and described in [Table 5-8](#).

Return to the [Summary Table](#).

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

Table 5-7. ATL0_BBSR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0204h |

Figure 5-3. ATL0_BBSR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | SMP_CNT | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 5-8. ATL0_BBSR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | SMP_CNT | R | 0h | This is the 16-bit sample count from the measuring circuit |

5.4 ATL0_ATLCR Register (Offset = 208h) [reset = X]

ATL0_ATLCR is shown in [Figure 5-4](#) and described in [Table 5-10](#).

Return to the [Summary Table](#).

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

Table 5-9. ATL0_ATLCR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0208h |

Figure 5-4. ATL0_ATLCR Register

| | | | | | | | |
|----------|----|-------------|---------|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CLK_DIV_SEL | INT_DIV | | | | |
| R/W-X | | R/W-0h | R/W-18h | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-10. ATL0_ATLCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | CLK_DIV_SEL | R/W | 0h | 0: MODCLK = AWS divided by 2^{16} 1: MODCLK = AWS divided by 2^{12} |
| 4-0 | INT_DIV | R/W | 18h | Sets ratio of ATLPCLK to ATCLK |

5.5 ATL0_SWEN Register (Offset = 210h) [reset = X]

ATL0_SWEN is shown in [Figure 5-5](#) and described in [Table 5-12](#).

Return to the [Summary Table](#).

The software enable register is used to enable/disable the ATL.

Table 5-11. ATL0_SWEN Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0210h |

Figure 5-5. ATL0_SWEN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-12. ATL0_SWEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | ENABLE | R/W | 0h | When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) |

5.6 ATL0_BWSMUX Register (Offset = 214h) [reset = X]

ATL0_BWSMUX is shown in [Figure 5-6](#) and described in [Table 5-14](#).

Return to the [Summary Table](#).

The Baseband IIS Word Select mux select control register

Table 5-13. ATL0_BWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0214h |

Figure 5-6. ATL0_BWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-14. ATL0_BWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] |

5.7 ATL0_AWSMUX Register (Offset = 218h) [reset = X]

ATL0_AWSMUX is shown in [Figure 5-7](#) and described in [Table 5-16](#).

Return to the [Summary Table](#).

The Audio IIS Word Select mux select control register

Table 5-15. ATL0_AWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0218h |

Figure 5-7. ATL0_AWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-16. ATL0_AWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] |

5.8 ATL0_PCLKMUX Register (Offset = 21Ch) [reset = X]

ATL0_PCLKMUX is shown in [Figure 5-8](#) and described in [Table 5-18](#).

Return to the [Summary Table](#).

ATL core input clock mux select control register

Table 5-17. ATL0_PCLKMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 021Ch |

Figure 5-8. ATL0_PCLKMUX Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SELECT |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-18. ATL0_PCLKMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | SELECT | R/W | 0h | ATL [0-3] core clock select: 0: vbus_clk 1: atl_clk |

5.9 ATL1_PPMR Register (Offset = 280h) [reset = X]

ATL1_PPMR is shown in [Figure 5-9](#) and described in [Table 5-20](#).

Return to the [Summary Table](#).

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

Table 5-19. ATL1_PPMR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0280h |

Figure 5-9. ATL1_PPMR Register

| | | | | | | | |
|----------|----------|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PPM_SD | RESERVED | | | | | | PPM_SET |
| R/W-0h | R/W-X | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPM_SET | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-20. ATL1_PPMR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15 | PPM_SD | R/W | 0h | 1 = Slow down 0 = Speed up |
| 14-9 | RESERVED | R/W | X | |
| 8-0 | PPM_SET | R/W | 0h | This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2 ²⁰ |

5.10 ATL1_BBSR Register (Offset = 284h) [reset = X]

ATL1_BBSR is shown in [Figure 5-10](#) and described in [Table 5-22](#).

Return to the [Summary Table](#).

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

Table 5-21. ATL1_BBSR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0284h |

Figure 5-10. ATL1_BBSR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | SMP_CNT | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 5-22. ATL1_BBSR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | SMP_CNT | R | 0h | This is the 16-bit sample count from the measuring circuit |

5.11 ATL1_ATLCR Register (Offset = 288h) [reset = X]

ATL1_ATLCR is shown in [Figure 5-11](#) and described in [Table 5-24](#).

Return to the [Summary Table](#).

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

Table 5-23. ATL1_ATLCR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0288h |

Figure 5-11. ATL1_ATLCR Register

| | | | | | | | |
|----------|----|-------------|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CLK_DIV_SEL | | INT_DIV | | | |
| R/W-X | | R/W-0h | | R/W-18h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-24. ATL1_ATLCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | CLK_DIV_SEL | R/W | 0h | 0: MODCLK = AWS divided by 2^{16} 1: MODCLK = AWS divided by 2^{12} |
| 4-0 | INT_DIV | R/W | 18h | Sets ratio of ATLPCLK to ATCLK |

5.12 ATL1_SWEN Register (Offset = 290h) [reset = X]

ATL1_SWEN is shown in [Figure 5-12](#) and described in [Table 5-26](#).

Return to the [Summary Table](#).

The software enable register is used to enable/disable the ATL.

Table 5-25. ATL1_SWEN Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0290h |

Figure 5-12. ATL1_SWEN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-26. ATL1_SWEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | ENABLE | R/W | 0h | When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) |

5.13 ATL1_BWSMUX Register (Offset = 294h) [reset = X]

ATL1_BWSMUX is shown in [Figure 5-13](#) and described in [Table 5-28](#).

Return to the [Summary Table](#).

The Baseband IIS Word Select mux select control register

Table 5-27. ATL1_BWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0294h |

Figure 5-13. ATL1_BWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-28. ATL1_BWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] |

5.14 ATL1_AWSMUX Register (Offset = 298h) [reset = X]

ATL1_AWSMUX is shown in [Figure 5-14](#) and described in [Table 5-30](#).

Return to the [Summary Table](#).

The Audio IIS Word Select mux select control register

Table 5-29. ATL1_AWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0298h |

Figure 5-14. ATL1_AWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-30. ATL1_AWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] |

5.15 ATL1_PCLKMUX Register (Offset = 29Ch) [reset = X]

ATL1_PCLKMUX is shown in [Figure 5-15](#) and described in [Table 5-32](#).

Return to the [Summary Table](#).

ATL core input clock mux select control register

Table 5-31. ATL1_PCLKMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 029Ch |

Figure 5-15. ATL1_PCLKMUX Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SELECT |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-32. ATL1_PCLKMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|----------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | SELECT | R/W | 0h | Non-functional |

5.16 ATL2_PPMR Register (Offset = 300h) [reset = X]

ATL2_PPMR is shown in [Figure 5-16](#) and described in [Table 5-34](#).

Return to the [Summary Table](#).

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

Table 5-33. ATL2_PPMR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0300h |

Figure 5-16. ATL2_PPMR Register

| | | | | | | | |
|----------|----------|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PPM_SD | RESERVED | | | | | | PPM_SET |
| R/W-0h | R/W-X | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPM_SET | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-34. ATL2_PPMR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15 | PPM_SD | R/W | 0h | 1 = Slow down 0 = Speed up |
| 14-9 | RESERVED | R/W | X | |
| 8-0 | PPM_SET | R/W | 0h | This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2 ²⁰ |

5.17 ATL2_BBSR Register (Offset = 304h) [reset = X]

ATL2_BBSR is shown in [Figure 5-17](#) and described in [Table 5-36](#).

Return to the [Summary Table](#).

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

Table 5-35. ATL2_BBSR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0304h |

Figure 5-17. ATL2_BBSR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | SMP_CNT | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 5-36. ATL2_BBSR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | SMP_CNT | R | 0h | This is the 16-bit sample count from the measuring circuit |

5.18 ATL2_ATLCR Register (Offset = 308h) [reset = X]

ATL2_ATLCR is shown in [Figure 5-18](#) and described in [Table 5-38](#).

Return to the [Summary Table](#).

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

Table 5-37. ATL2_ATLCR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0308h |

Figure 5-18. ATL2_ATLCR Register

| | | | | | | | |
|----------|----|-------------|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CLK_DIV_SEL | | INT_DIV | | | |
| R/W-X | | R/W-0h | | R/W-18h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-38. ATL2_ATLCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | CLK_DIV_SEL | R/W | 0h | 0: MODCLK = AWS divided by 2^{16} 1: MODCLK = AWS divided by 2^{12} |
| 4-0 | INT_DIV | R/W | 18h | Sets ratio of ATLPCLK to ATCLK |

5.19 ATL2_SWEN Register (Offset = 310h) [reset = X]

ATL2_SWEN is shown in [Figure 5-19](#) and described in [Table 5-40](#).

Return to the [Summary Table](#).

The software enable register is used to enable/disable the ATL.

Table 5-39. ATL2_SWEN Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0310h |

Figure 5-19. ATL2_SWEN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-40. ATL2_SWEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | ENABLE | R/W | 0h | When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) |

5.20 ATL2_BWSMUX Register (Offset = 314h) [reset = X]

ATL2_BWSMUX is shown in [Figure 5-20](#) and described in [Table 5-42](#).

Return to the [Summary Table](#).

The Baseband IIS Word Select mux select control register

Table 5-41. ATL2_BWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0314h |

Figure 5-20. ATL2_BWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-42. ATL2_BWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] |

5.21 ATL2_AWSMUX Register (Offset = 318h) [reset = X]

ATL2_AWSMUX is shown in [Figure 5-21](#) and described in [Table 5-44](#).

Return to the [Summary Table](#).

The Audio IIS Word Select mux select control register

Table 5-43. ATL2_AWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0318h |

Figure 5-21. ATL2_AWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-44. ATL2_AWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] |

5.22 ATL2_PCLKMUX Register (Offset = 31Ch) [reset = X]

ATL2_PCLKMUX is shown in [Figure 5-22](#) and described in [Table 5-46](#).

Return to the [Summary Table](#).

ATL core input clock mux select control register

Table 5-45. ATL2_PCLKMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 031Ch |

Figure 5-22. ATL2_PCLKMUX Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SELECT |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-46. ATL2_PCLKMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|----------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | SELECT | R/W | 0h | Non-functional |

5.23 ATL3_PPMR Register (Offset = 380h) [reset = X]

ATL3_PPMR is shown in [Figure 5-23](#) and described in [Table 5-48](#).

Return to the [Summary Table](#).

The PPM register is used by the Audio re-timing code. The DAC over-sampling clock will slow down or speed up by the PPM written to bits [8:0].

Table 5-47. ATL3_PPMR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0380h |

Figure 5-23. ATL3_PPMR Register

| | | | | | | | |
|----------|----------|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PPM_SD | RESERVED | | | | | | PPM_SET |
| R/W-0h | R/W-X | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPM_SET | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-48. ATL3_PPMR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15 | PPM_SD | R/W | 0h | 1 = Slow down 0 = Speed up |
| 14-9 | RESERVED | R/W | X | |
| 8-0 | PPM_SET | R/W | 0h | This is the 9-bit parts-per-million value in the adjusting circuit. PPM adjustment = PPMSET/2 ²⁰ |

5.24 ATL3_BBSR Register (Offset = 384h) [reset = X]

ATL3_BBSR is shown in [Figure 5-24](#) and described in [Table 5-50](#).

Return to the [Summary Table](#).

The measuring circuit produces a 16-bit Sample Count. Its inputs are the Audio IIS Word Select (AWS) and the Baseband IIS Word Select (BWS) from their respective MCASP pins. The sample count is a read-only register.

Table 5-49. ATL3_BBSR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0384h |

Figure 5-24. ATL3_BBSR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | SMP_CNT | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 5-50. ATL3_BBSR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | SMP_CNT | R | 0h | This is the 16-bit sample count from the measuring circuit |

5.25 ATL3_ATLCR Register (Offset = 388h) [reset = X]

ATL3_ATLCR is shown in [Figure 5-25](#) and described in [Table 5-52](#).

Return to the [Summary Table](#).

The modem Clock Divide Select bit is used during factory calibration of the radio to match latency between the analog and digital signal paths. The ATL Internal Divider divides down the ATL master clock to make ATCLK.

Table 5-51. ATL3_ATLCR Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0388h |

Figure 5-25. ATL3_ATLCR Register

| | | | | | | | |
|----------|----|-------------|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CLK_DIV_SEL | | INT_DIV | | | |
| R/W-X | | R/W-0h | | R/W-18h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-52. ATL3_ATLCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | CLK_DIV_SEL | R/W | 0h | 0: MODCLK = AWS divided by 2^{16} 1: MODCLK = AWS divided by 2^{12} |
| 4-0 | INT_DIV | R/W | 18h | Sets ratio of ATLPCLK to ATCLK |

5.26 ATL3_SWEN Register (Offset = 390h) [reset = X]

ATL3_SWEN is shown in [Figure 5-26](#) and described in [Table 5-54](#).

Return to the [Summary Table](#).

The software enable register is used to enable/disable the ATL.

Table 5-53. ATL3_SWEN Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0390h |

Figure 5-26. ATL3_SWEN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-54. ATL3_SWEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | ENABLE | R/W | 0h | When disabled the ATL registers are forced to known states for simulation purposes. Runtime startup doesn't require initial values because measurement is relative to an arbitrary initial value. All registers are reset to zero except ATLCR.INT_DIV which is resets to 24 (divide-by-25, because zero is not a legal divide ratio.) |

5.27 ATL3_BWSMUX Register (Offset = 394h) [reset = X]

ATL3_BWSMUX is shown in [Figure 5-27](#) and described in [Table 5-56](#).

Return to the [Summary Table](#).

The Baseband IIS Word Select mux select control register

Table 5-55. ATL3_BWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0394h |

Figure 5-27. ATL3_BWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-56. ATL3_BWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | BWS input select: 0000: atl_io_port_bws[0] 0001: atl_io_port_bws[1] 0010: atl_io_port_bws[2] 0011: atl_io_port_bws[3] 0100: atl_io_port_bws[4] 0101: atl_io_port_bws[5] 0110: atl_io_port_bws[6] 0111: atl_io_port_bws[7] 1000: atl_io_port_bws[8] 1001: atl_io_port_bws[9] 1010: atl_io_port_bws[10] 1011: atl_io_port_bws[11] 1100: atl_io_port_bws[12] 1101: atl_io_port_bws[13] 1110: atl_io_port_bws[14] 1111: atl_io_port_bws[15] |

5.28 ATL3_AWSMUX Register (Offset = 398h) [reset = X]

ATL3_AWSMUX is shown in [Figure 5-28](#) and described in [Table 5-58](#).

Return to the [Summary Table](#).

The Audio IIS Word Select mux select control register

Table 5-57. ATL3_AWSMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 0398h |

Figure 5-28. ATL3_AWSMUX Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | SELECT | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-58. ATL3_AWSMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-0 | SELECT | R/W | 0h | AWS input select: 0000: atl_io_port_aws[0] 0001: atl_io_port_aws[1] 0010: atl_io_port_aws[2] 0011: atl_io_port_aws[3] 0100: atl_io_port_aws[4] 0101: atl_io_port_aws[5] 0110: atl_io_port_aws[6] 0111: atl_io_port_aws[7] 1000: atl_io_port_aws[8] 1001: atl_io_port_aws[9] 1010: atl_io_port_aws[10] 1011: atl_io_port_aws[11] 1100: atl_io_port_aws[12] 1101: atl_io_port_aws[13] 1110: atl_io_port_aws[14] 1111: atl_io_port_aws[15] |

5.29 ATL3_PCLKMUX Register (Offset = 39Ch) [reset = X]

ATL3_PCLKMUX is shown in [Figure 5-29](#) and described in [Table 5-60](#).

Return to the [Summary Table](#).

ATL core input clock mux select control register

Table 5-59. ATL3_PCLKMUX Instances

| Instance | Physical Address |
|----------|------------------|
| ATL0_REG | 031F 039Ch |

Figure 5-29. ATL3_PCLKMUX Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SELECT |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 5-60. ATL3_PCLKMUX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|----------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | SELECT | R/W | 0h | Non-functional |

6 MCASP Registers

6.1 MCASP_CFG Registers

Table 6-2 lists the memory-mapped registers for the MCASP_CFG registers. All register offset addresses not listed in Table 6-2 should be considered as reserved locations and the register contents should not be modified.

Table 6-1. MCASP_CFG Instances

| Instance | Base Address |
|------------|--------------|
| MCASP0_CFG | 02B0 0000h |
| MCASP1_CFG | 02B1 0000h |
| MCASP2_CFG | 02B2 0000h |

Table 6-2. MCASP_CFG Registers

| Offset | Acronym | Register Name | MCASP0_ CFG Physical Address | MCASP1_ CFG Physical Address | MCASP2_ CFG Physical Address |
|--------|--|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 0h | MCASP_PID | Peripheral Identification Register | 02B0 0000h | 02B1 0000h | 02B2 0000h |
| 4h | MCASP_PWRIDLESYSCONFIG | Power Idle SYSCONFIG Register | 02B0 0004h | 02B1 0004h | 02B2 0004h |
| 10h | MCASP_PFUNC | Pin Function Register | 02B0 0010h | 02B1 0010h | 02B2 0010h |
| 14h | MCASP_PDIR | Pin Direction Register | 02B0 0014h | 02B1 0014h | 02B2 0014h |
| 18h | MCASP_PDOUT | Pin Data Output Register | 02B0 0018h | 02B1 0018h | 02B2 0018h |
| 1Ch | MCASP_PDIN | Pin Data Input Register | 02B0 001Ch | 02B1 001Ch | 02B2 001Ch |
| 1Ch | MCASP_PDSET | Pin Data Set Register | 02B0 001Ch | 02B1 001Ch | 02B2 001Ch |
| 20h | MCASP_PDCLR | Pin Data Clear Register | 02B0 0020h | 02B1 0020h | 02B2 0020h |
| 30h | MCASP_TLGC | IODFT Register | 02B0 0030h | 02B1 0030h | 02B2 0030h |
| 34h | MCASP_TLMR | IODFT Register | 02B0 0034h | 02B1 0034h | 02B2 0034h |
| 38h | MCASP_TLEC | IODFT Register | 02B0 0038h | 02B1 0038h | 02B2 0038h |
| 44h | MCASP_GBLCTL | Global Control Register | 02B0 0044h | 02B1 0044h | 02B2 0044h |
| 48h | MCASP_AMUTE | Audio Mute Control Register | 02B0 0048h | 02B1 0048h | 02B2 0048h |
| 4Ch | MCASP_LBCTL | Loopback Control Register | 02B0 004Ch | 02B1 004Ch | 02B2 004Ch |
| 50h | MCASP_TXDITCTL | Transmit DIT Mode Control Register | 02B0 0050h | 02B1 0050h | 02B2 0050h |
| 60h | MCASP_GBLCTLR | Receiver Global Control Register | 02B0 0060h | 02B1 0060h | 02B2 0060h |
| 64h | MCASP_RXMASK | Receive Format Unit Bit Mask Register | 02B0 0064h | 02B1 0064h | 02B2 0064h |
| 68h | MCASP_RXFMT | Receive Bit Stream Format Register | 02B0 0068h | 02B1 0068h | 02B2 0068h |
| 6Ch | MCASP_RXFMCTL | Receive Frame Sync Control Register | 02B0 006Ch | 02B1 006Ch | 02B2 006Ch |
| 70h | MCASP_ACLKRCTL | Receive Clock Control Register | 02B0 0070h | 02B1 0070h | 02B2 0070h |

Table 6-2. MCASP_CFG Registers (continued)

| Offset | Acronym | Register Name | MCASP0_ CFG Physical Address | MCASP1_ CFG Physical Address | MCASP2_ CFG Physical Address |
|--------|---------------------------------|---|------------------------------------|------------------------------------|------------------------------------|
| 74h | MCASP_AHCLKRCTL | Receive High-Frequency Clock Control Register | 02B0 0074h | 02B1 0074h | 02B2 0074h |
| 78h | MCASP_RXTDM | Receive TDM Time Slot 0-31 Register | 02B0 0078h | 02B1 0078h | 02B2 0078h |
| 7Ch | MCASP_EVTCTLR | Receiver DMA Event Control Register | 02B0 007Ch | 02B1 007Ch | 02B2 007Ch |
| 80h | MCASP_RXSTAT | Receiver Status Register | 02B0 0080h | 02B1 0080h | 02B2 0080h |
| 84h | MCASP_RXTDMSLOT | Current Receive TDM Time Slot Register | 02B0 0084h | 02B1 0084h | 02B2 0084h |
| 88h | MCASP_RXCLKCHK | Receive Clock Check Control Register | 02B0 0088h | 02B1 0088h | 02B2 0088h |
| 8Ch | MCASP_REVTCTL | Receiver DMA Event Control Register | 02B0 008Ch | 02B1 008Ch | 02B2 008Ch |
| A0h | MCASP_GBLCTLX | Transmitter Global Control Register | 02B0 00A0h | 02B1 00A0h | 02B2 00A0h |
| A4h | MCASP_TXMASK | Transmit Format Unit Bit Mask Register | 02B0 00A4h | 02B1 00A4h | 02B2 00A4h |
| A8h | MCASP_TXFMT | Transmit Bit Stream Format Register | 02B0 00A8h | 02B1 00A8h | 02B2 00A8h |
| ACh | MCASP_TXFMCTL | Transmit Frame Sync Control Register | 02B0 00ACh | 02B1 00ACh | 02B2 00ACh |
| B0h | MCASP_ACLKXCTL | Transmit Clock Control Register | 02B0 00B0h | 02B1 00B0h | 02B2 00B0h |
| B4h | MCASP_AHCLKXCTL | Transmit High- Frequency Clock Control Register | 02B0 00B4h | 02B1 00B4h | 02B2 00B4h |
| B8h | MCASP_TXTDM | Transmit TDM Time Slot 0-31 Register | 02B0 00B8h | 02B1 00B8h | 02B2 00B8h |
| BCh | MCASP_EVTCTLX | Transmitter Interrupt Control Register | 02B0 00BCh | 02B1 00BCh | 02B2 00BCh |
| C0h | MCASP_TXSTAT | Transmitter Status Register | 02B0 00C0h | 02B1 00C0h | 02B2 00C0h |
| C4h | MCASP_TXTDMSLOT | Current Transmit TDM Time Slot Register | 02B0 00C4h | 02B1 00C4h | 02B2 00C4h |
| C8h | MCASP_TXCLKCHK | Transmit Clock Check Control Register | 02B0 00C8h | 02B1 00C8h | 02B2 00C8h |
| CCh | MCASP_XEVTCTL | Transmitter DMA Event Control Register | 02B0 00CCh | 02B1 00CCh | 02B2 00CCh |
| D0h | MCASP_CLKADJEN | One-Shot Clock Adjustment Enable Register | 02B0 00D0h | 02B1 00D0h | 02B2 00D0h |
| 100h | MCASP_DITCSRA0 | Left (Even TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0100h | 02B1 0100h | 02B2 0100h |
| 104h | MCASP_DITCSRA1 | Left (Even TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0104h | 02B1 0104h | 02B2 0104h |
| 108h | MCASP_DITCSRA2 | Left (Even TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0108h | 02B1 0108h | 02B2 0108h |
| 10Ch | MCASP_DITCSRA3 | Left (Even TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 010Ch | 02B1 010Ch | 02B2 010Ch |
| 110h | MCASP_DITCSRA4 | Left (Even TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0110h | 02B1 0110h | 02B2 0110h |
| 114h | MCASP_DITCSRA5 | Left (Even TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0114h | 02B1 0114h | 02B2 0114h |

Table 6-2. MCASP_CFG Registers (continued)

| Offset | Acronym | Register Name | MCASP0_ CFG Physical Address | MCASP1_ CFG Physical Address | MCASP2_ CFG Physical Address |
|--------|--------------------------------|--|---------------------------------------|---------------------------------------|---------------------------------------|
| 118h | MCASP_DITCSRB0 | Right (Odd TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0118h | 02B1 0118h | 02B2 0118h |
| 11Ch | MCASP_DITCSRB1 | Right (Odd TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 011Ch | 02B1 011Ch | 02B2 011Ch |
| 120h | MCASP_DITCSRB2 | Right (Odd TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0120h | 02B1 0120h | 02B2 0120h |
| 124h | MCASP_DITCSRB3 | Right (Odd TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0124h | 02B1 0124h | 02B2 0124h |
| 128h | MCASP_DITCSRB4 | Right (Odd TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 0128h | 02B1 0128h | 02B2 0128h |
| 12Ch | MCASP_DITCSRB5 | Right (Odd TDM Time Slot) Channel Status Registers (DIT Mode) | 02B0 012Ch | 02B1 012Ch | 02B2 012Ch |
| 130h | MCASP_DITUDRA0 | Left (Even TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0130h | 02B1 0130h | 02B2 0130h |
| 134h | MCASP_DITUDRA1 | Left (Even TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0134h | 02B1 0134h | 02B2 0134h |
| 138h | MCASP_DITUDRA2 | Left (Even TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0138h | 02B1 0138h | 02B2 0138h |
| 13Ch | MCASP_DITUDRA3 | Left (Even TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 013Ch | 02B1 013Ch | 02B2 013Ch |
| 140h | MCASP_DITUDRA4 | Left (Even TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0140h | 02B1 0140h | 02B2 0140h |
| 144h | MCASP_DITUDRA5 | Left (Even TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0144h | 02B1 0144h | 02B2 0144h |
| 148h | MCASP_DITUDRB0 | Right (Odd TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0148h | 02B1 0148h | 02B2 0148h |
| 14Ch | MCASP_DITUDRB1 | Right (Odd TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 014Ch | 02B1 014Ch | 02B2 014Ch |
| 150h | MCASP_DITUDRB2 | Right (Odd TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0150h | 02B1 0150h | 02B2 0150h |
| 154h | MCASP_DITUDRB3 | Right (Odd TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0154h | 02B1 0154h | 02B2 0154h |
| 158h | MCASP_DITUDRB4 | Right (Odd TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 0158h | 02B1 0158h | 02B2 0158h |
| 15Ch | MCASP_DITUDRB5 | Right (Odd TDM Time Slot) Channel User Data Registers (DIT Mode) | 02B0 015Ch | 02B1 015Ch | 02B2 015Ch |
| 180h | MCASP_XRSRCTL0 | Serializer Control Registers | 02B0 0180h | 02B1 0180h | 02B2 0180h |
| 184h | MCASP_XRSRCTL1 | Serializer Control Registers | 02B0 0184h | 02B1 0184h | 02B2 0184h |
| 188h | MCASP_XRSRCTL2 | Serializer Control Registers | 02B0 0188h | 02B1 0188h | 02B2 0188h |
| 18Ch | MCASP_XRSRCTL3 | Serializer Control Registers | 02B0 018Ch | 02B1 018Ch | 02B2 018Ch |
| 190h | MCASP_XRSRCTL4 | Serializer Control Registers | 02B0 0190h | 02B1 0190h | 02B2 0190h |
| 194h | MCASP_XRSRCTL5 | Serializer Control Registers | 02B0 0194h | 02B1 0194h | 02B2 0194h |
| 198h | MCASP_XRSRCTL6 | Serializer Control Registers | 02B0 0198h | 02B1 0198h | 02B2 0198h |
| 19Ch | MCASP_XRSRCTL7 | Serializer Control Registers | 02B0 019Ch | 02B1 019Ch | 02B2 019Ch |

Table 6-2. MCASP_CFG Registers (continued)

| Offset | Acronym | Register Name | MCASP0_ CFG Physical Address | MCASP1_ CFG Physical Address | MCASP2_ CFG Physical Address |
|--------|---------------------------------|--|---------------------------------------|---------------------------------------|---------------------------------------|
| 1A0h | MCASP_XRSRCTL8 | Serializer Control Registers | 02B0 01A0h | 02B1 01A0h | 02B2 01A0h |
| 1A4h | MCASP_XRSRCTL9 | Serializer Control Registers | 02B0 01A4h | 02B1 01A4h | 02B2 01A4h |
| 1A8h | MCASP_XRSRCTL10 | Serializer Control Registers | 02B0 01A8h | 02B1 01A8h | 02B2 01A8h |
| 1ACh | MCASP_XRSRCTL11 | Serializer Control Registers | 02B0 01ACh | 02B1 01ACh | 02B2 01ACh |
| 1B0h | MCASP_XRSRCTL12 | Serializer Control Registers | 02B0 01B0h | 02B1 01B0h | 02B2 01B0h |
| 1B4h | MCASP_XRSRCTL13 | Serializer Control Registers | 02B0 01B4h | 02B1 01B4h | 02B2 01B4h |
| 1B8h | MCASP_XRSRCTL14 | Serializer Control Registers | 02B0 01B8h | 02B1 01B8h | 02B2 01B8h |
| 1BCh | MCASP_XRSRCTL15 | Serializer Control Registers | 02B0 01BCh | 02B1 01BCh | 02B2 01BCh |
| 200h | MCASP_TXBUF0 | Transmit Buffer Register for Serializers | 02B0 0200h | 02B1 0200h | 02B2 0200h |
| 204h | MCASP_TXBUF1 | Transmit Buffer Register for Serializers | 02B0 0204h | 02B1 0204h | 02B2 0204h |
| 208h | MCASP_TXBUF2 | Transmit Buffer Register for Serializers | 02B0 0208h | 02B1 0208h | 02B2 0208h |
| 20Ch | MCASP_TXBUF3 | Transmit Buffer Register for Serializers | 02B0 020Ch | 02B1 020Ch | 02B2 020Ch |
| 210h | MCASP_TXBUF4 | Transmit Buffer Register for Serializers | 02B0 0210h | 02B1 0210h | 02B2 0210h |
| 214h | MCASP_TXBUF5 | Transmit Buffer Register for Serializers | 02B0 0214h | 02B1 0214h | 02B2 0214h |
| 218h | MCASP_TXBUF6 | Transmit Buffer Register for Serializers | 02B0 0218h | 02B1 0218h | 02B2 0218h |
| 21Ch | MCASP_TXBUF7 | Transmit Buffer Register for Serializers | 02B0 021Ch | 02B1 021Ch | 02B2 021Ch |
| 220h | MCASP_TXBUF8 | Transmit Buffer Register for Serializers | 02B0 0220h | 02B1 0220h | 02B2 0220h |
| 224h | MCASP_TXBUF9 | Transmit Buffer Register for Serializers | 02B0 0224h | 02B1 0224h | 02B2 0224h |
| 228h | MCASP_TXBUF10 | Transmit Buffer Register for Serializers | 02B0 0228h | 02B1 0228h | 02B2 0228h |
| 22Ch | MCASP_TXBUF11 | Transmit Buffer Register for Serializers | 02B0 022Ch | 02B1 022Ch | 02B2 022Ch |
| 230h | MCASP_TXBUF12 | Transmit Buffer Register for Serializers | 02B0 0230h | 02B1 0230h | 02B2 0230h |
| 234h | MCASP_TXBUF13 | Transmit Buffer Register for Serializers | 02B0 0234h | 02B1 0234h | 02B2 0234h |
| 238h | MCASP_TXBUF14 | Transmit Buffer Register for Serializers | 02B0 0238h | 02B1 0238h | 02B2 0238h |
| 23Ch | MCASP_TXBUF15 | Transmit Buffer Register for Serializers | 02B0 023Ch | 02B1 023Ch | 02B2 023Ch |
| 280h | MCASP_RXBUF0 | Receive Buffer Register for Serializers | 02B0 0280h | 02B1 0280h | 02B2 0280h |
| 284h | MCASP_RXBUF1 | Receive Buffer Register for Serializers | 02B0 0284h | 02B1 0284h | 02B2 0284h |

Table 6-2. MCASP_CFG Registers (continued)

| Offset | Acronym | Register Name | MCASP0_ CFG Physical Address | MCASP1_ CFG Physical Address | MCASP2_ CFG Physical Address |
|--------|-------------------------------|---|---------------------------------------|---------------------------------------|---------------------------------------|
| 288h | MCASP_RXBUF2 | Receive Buffer Register for Serializers | 02B0 0288h | 02B1 0288h | 02B2 0288h |
| 28Ch | MCASP_RXBUF3 | Receive Buffer Register for Serializers | 02B0 028Ch | 02B1 028Ch | 02B2 028Ch |
| 290h | MCASP_RXBUF4 | Receive Buffer Register for Serializers | 02B0 0290h | 02B1 0290h | 02B2 0290h |
| 294h | MCASP_RXBUF5 | Receive Buffer Register for Serializers | 02B0 0294h | 02B1 0294h | 02B2 0294h |
| 298h | MCASP_RXBUF6 | Receive Buffer Register for Serializers | 02B0 0298h | 02B1 0298h | 02B2 0298h |
| 29Ch | MCASP_RXBUF7 | Receive Buffer Register for Serializers | 02B0 029Ch | 02B1 029Ch | 02B2 029Ch |
| 2A0h | MCASP_RXBUF8 | Receive Buffer Register for Serializers | 02B0 02A0h | 02B1 02A0h | 02B2 02A0h |
| 2A4h | MCASP_RXBUF9 | Receive Buffer Register for Serializers | 02B0 02A4h | 02B1 02A4h | 02B2 02A4h |
| 2A8h | MCASP_RXBUF10 | Receive Buffer Register for Serializers | 02B0 02A8h | 02B1 02A8h | 02B2 02A8h |
| 2ACh | MCASP_RXBUF11 | Receive Buffer Register for Serializers | 02B0 02ACh | 02B1 02ACh | 02B2 02ACh |
| 2B0h | MCASP_RXBUF12 | Receive Buffer Register for Serializers | 02B0 02B0h | 02B1 02B0h | 02B2 02B0h |
| 2B4h | MCASP_RXBUF13 | Receive Buffer Register for Serializers | 02B0 02B4h | 02B1 02B4h | 02B2 02B4h |
| 2B8h | MCASP_RXBUF14 | Receive Buffer Register for Serializers | 02B0 02B8h | 02B1 02B8h | 02B2 02B8h |
| 2BCh | MCASP_RXBUF15 | Receive Buffer Register for Serializers | 02B0 02BCh | 02B1 02BCh | 02B2 02BCh |

6.2 MCASP_PID Register (Offset = 0h) [reset = 44307B02h]

MCASP_PID is shown in [Figure 6-1](#) and described in [Table 6-4](#).

Return to [Summary Table](#).

Table 6-3. MCASP_PID Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0000h |
| MCASP1_CFG | 02B1 0000h |
| MCASP2_CFG | 02B2 0000h |

Figure 6-1. MCASP_PID Register

| | | | | | | | | | | | | | | | |
|--------|----|----------|----|----------|----------|----|----|--------|----|----------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | RESERVED | | FUNCTION | | | | | | | | | | | |
| R-1h | | R-0h | | R-430h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTL | | | | | REVMajor | | | CUSTOM | | REVMINOR | | | | | |
| R-Fh | | | | | R-3h | | | R-0h | | R-2h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 6-4. MCASP_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-30 | SCHEME | R | 1h | Distinguishes between old scheme and current. |
| 29-28 | RESERVED | R | 0h | Reserved |
| 27-16 | FUNCTION | R | 430h | Indicates a software-compatible module family. |
| 15-11 | RTL | R | Fh | RTL version. |
| 10-8 | REVMajor | R | 3h | Major revision number. |
| 7-6 | CUSTOM | R | 0h | Indicates a special version for a given device. |
| 5-0 | REVMINOR | R | 2h | Minor revision number. |

6.3 MCASP_PWRIDLESYSCONFIG Register (Offset = 4h) [reset = 2h]

MCASP_PWRIDLESYSCONFIG is shown in [Figure 6-2](#) and described in [Table 6-6](#).

[Return to Summary Table.](#)

Power Idle SYSCONFIG register.

Table 6-5. MCASP_PWRIDLESYSCONFIG Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0004h |
| MCASP1_CFG | 02B1 0004h |
| MCASP2_CFG | 02B2 0004h |

Figure 6-2. MCASP_PWRIDLESYSCONFIG Register

| | | | | | | | |
|----------|----|--------|----|----|----|-----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | OTHER | | | | IDLE_MODE | |
| R-0h | | R/W-0h | | | | R/W-2h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-6. MCASP_PWRIDLESYSCONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-6 | RESERVED | R | 0h | Reserved |
| 5-2 | OTHER | R/W | 0h | Reserved for future programming. |
| 1-0 | IDLE_MODE | R/W | 2h | Power management Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0h = Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements. Backup mode, for debug only. 1h = No-idle mode: local target never enters idle state. Backup mode, for debug only. 2h = Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements. IP module shall not generate (IRQor DMA-request-related) wakeup events. 3h = Reserved. |

6.4 MCASP_PFUNC Register (Offset = 10h) [reset = 0h]

MCASP_PFUNC is shown in [Figure 6-3](#) and described in [Table 6-8](#).

Return to [Summary Table](#).

Table 6-7. MCASP_PFUNC Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0010h |
| MCASP1_CFG | 02B1 0010h |
| MCASP2_CFG | 02B2 0010h |

Figure 6-3. MCASP_PFUNC Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|--------|--------|--------|--------|--------|--------|----------|
| AFSR | AHCLKR | ACLKR | AFSX | AHCLKX | ACLKX | AMUTE | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AXR15 | AXR14 | AXR13 | AXR12 | AXR11 | AXR10 | AXR9 | AXR8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AXR7 | AXR6 | AXR5 | AXR4 | AXR3 | AXR2 | AXR1 | AXR0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-8. MCASP_PFUNC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31 | AFSR | R/W | 0h | Determines if AFSR pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 30 | AHCLKR | R/W | 0h | Determines if AHCLKR pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 29 | ACLKR | R/W | 0h | Determines if ACLKR pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 28 | AFSX | R/W | 0h | Determines if AFSX pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 27 | AHCLKX | R/W | 0h | Determines if AHCLKX pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 26 | ACLKX | R/W | 0h | Determines if ACLKX pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 25 | AMUTE | R/W | 0h | Determines if AMUTE pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 24-16 | RESERVED | R | 0h | Reserved |

Table 6-8. MCASP_PFUNC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 15 | AXR15 | R/W | 0h | Determines if AXR15 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 14 | AXR14 | R/W | 0h | Determines if AXR14 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 13 | AXR13 | R/W | 0h | Determines if AXR13 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 12 | AXR12 | R/W | 0h | Determines if AXR12 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 11 | AXR11 | R/W | 0h | Determines if AXR11 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 10 | AXR10 | R/W | 0h | Determines if AXR10 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 9 | AXR9 | R/W | 0h | Determines if AXR9 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 8 | AXR8 | R/W | 0h | Determines if AXR8 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 7 | AXR7 | R/W | 0h | Determines if AXR7 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 6 | AXR6 | R/W | 0h | Determines if AXR6 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 5 | AXR5 | R/W | 0h | Determines if AXR5 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 4 | AXR4 | R/W | 0h | Determines if AXR4 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 3 | AXR3 | R/W | 0h | Determines if AXR3 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 2 | AXR2 | R/W | 0h | Determines if AXR2 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 1 | AXR1 | R/W | 0h | Determines if AXR1 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |
| 0 | AXR0 | R/W | 0h | Determines if AXR0 pin functions as McASP or GPIO. 0h = Pin functions as McASP pin. 1h = Pin functions as GPIO pin. |

6.5 MCASP_PDIR Register (Offset = 14h) [reset = 0h]

MCASP_PDIR is shown in [Figure 6-4](#) and described in [Table 6-10](#).

Return to [Summary Table](#).

Table 6-9. MCASP_PDIR Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0014h |
| MCASP1_CFG | 02B1 0014h |
| MCASP2_CFG | 02B2 0014h |

Figure 6-4. MCASP_PDIR Register

| | | | | | | | |
|----------|--------|--------|--------|--------|--------|--------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| AFSR | AHCLKR | ACLKR | AFSX | AHCLKX | ACLKX | AMUTE | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AXR15 | AXR14 | AXR13 | AXR12 | AXR11 | AXR10 | AXR9 | AXR8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AXR7 | AXR6 | AXR5 | AXR4 | AXR3 | AXR2 | AXR1 | AXR0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-10. MCASP_PDIR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31 | AFSR | R/W | 0h | Determines if AFSR pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 30 | AHCLKR | R/W | 0h | Determines if AHCLKR pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 29 | ACLKR | R/W | 0h | Determines if ACLKR pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 28 | AFSX | R/W | 0h | Determines if AFSX pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 27 | AHCLKX | R/W | 0h | Determines if AHCLKX pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 26 | ACLKX | R/W | 0h | Determines if ACLKX pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 25 | AMUTE | R/W | 0h | Determines if AMUTE pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 24-16 | RESERVED | R | 0h | Reserved |

Table 6-10. MCASP_PDIR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 15 | AXR15 | R/W | 0h | Determines if AXR15 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 14 | AXR14 | R/W | 0h | Determines if AXR14 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 13 | AXR13 | R/W | 0h | Determines if AXR13 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 12 | AXR12 | R/W | 0h | Determines if AXR12 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 11 | AXR11 | R/W | 0h | Determines if AXR11 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 10 | AXR10 | R/W | 0h | Determines if AXR10 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 9 | AXR9 | R/W | 0h | Determines if AXR9 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 8 | AXR8 | R/W | 0h | Determines if AXR8 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 7 | AXR7 | R/W | 0h | Determines if AXR7 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 6 | AXR6 | R/W | 0h | Determines if AXR6 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 5 | AXR5 | R/W | 0h | Determines if AXR5 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 4 | AXR4 | R/W | 0h | Determines if AXR4 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 3 | AXR3 | R/W | 0h | Determines if AXR3 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 2 | AXR2 | R/W | 0h | Determines if AXR2 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 1 | AXR1 | R/W | 0h | Determines if AXR1 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |
| 0 | AXR0 | R/W | 0h | Determines if AXR0 pin functions as an input or output. 0h = Pin functions as input. 1h = Pin functions as output. |

6.6 MCASP_PDOUT Register (Offset = 18h) [reset = 0h]

MCASP_PDOUT is shown in [Figure 6-5](#) and described in [Table 6-12](#).

Return to [Summary Table](#).

Table 6-11. MCASP_PDOUT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0018h |
| MCASP1_CFG | 02B1 0018h |
| MCASP2_CFG | 02B2 0018h |

Figure 6-5. MCASP_PDOUT Register

| | | | | | | | |
|----------|--------|--------|--------|--------|--------|--------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| AFSR | AHCLKR | ACLKR | AFSX | AHCLKX | ACLKX | AMUTE | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AXR15 | AXR14 | AXR13 | AXR12 | AXR11 | AXR10 | AXR9 | AXR8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AXR7 | AXR6 | AXR5 | AXR4 | AXR3 | AXR2 | AXR1 | AXR0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-12. MCASP_PDOUT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 31 | AFSR | R/W | 0h | Determines drive on AFSR output pin when the corresponding MCASP_PFUNC[31] and MCASP_PDIR[31] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 30 | AHCLKR | R/W | 0h | Determines drive on AHCLKR output pin when the corresponding MCASP_PFUNC[30] and MCASP_PDIR[30] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 29 | ACLKR | R/W | 0h | Determines drive on ACLKR output pin when the corresponding MCASP_PFUNC[29] and MCASP_PDIR[29] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 28 | AFSX | R/W | 0h | Determines drive on AFSX output pin when the corresponding MCASP_PFUNC[28] and MCASP_PDIR[28] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 27 | AHCLKX | R/W | 0h | Determines drive on AHCLKX output pin when the corresponding MCASP_PFUNC[27] and MCASP_PDIR[27] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 26 | ACLKX | R/W | 0h | Determines drive on ACLKX output pin when the corresponding MCASP_PFUNC[26] and MCASP_PDIR[26] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |

Table 6-12. MCASP_PDOUT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 25 | AMUTE | R/W | 0h | Determines drive on AMUTE output pin when the corresponding MCASP_PFUNC[25] and MCASP_PDIR[25] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 24-16 | RESERVED | R | 0h | Reserved |
| 15 | AXR15 | R/W | 0h | Determines drive on AXR15 output pin when the corresponding MCASP_PFUNC[15] and MCASP_PDIR[15] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 14 | AXR14 | R/W | 0h | Determines drive on AXR14 output pin when the corresponding MCASP_PFUNC[14] and MCASP_PDIR[14] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 13 | AXR13 | R/W | 0h | Determines drive on AXR13 output pin when the corresponding MCASP_PFUNC[13] and MCASP_PDIR[13] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 12 | AXR12 | R/W | 0h | Determines drive on AXR12 output pin when the corresponding MCASP_PFUNC[12] and MCASP_PDIR[12] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 11 | AXR11 | R/W | 0h | Determines drive on AXR11 output pin when the corresponding MCASP_PFUNC[11] and MCASP_PDIR[11] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 10 | AXR10 | R/W | 0h | Determines drive on AXR10 output pin when the corresponding MCASP_PFUNC[10] and MCASP_PDIR[10] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 9 | AXR9 | R/W | 0h | Determines drive on AXR9 output pin when the corresponding MCASP_PFUNC[9] and MCASP_PDIR[9] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 8 | AXR8 | R/W | 0h | Determines drive on AXR8 output pin when the corresponding MCASP_PFUNC[8] and MCASP_PDIR[8] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 7 | AXR7 | R/W | 0h | Determines drive on AXR7 output pin when the corresponding MCASP_PFUNC[7] and MCASP_PDIR[7] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 6 | AXR6 | R/W | 0h | Determines drive on AXR6 output pin when the corresponding MCASP_PFUNC[6] and MCASP_PDIR[6] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 5 | AXR5 | R/W | 0h | Determines drive on AXR5 output pin when the corresponding MCASP_PFUNC[5] and MCASP_PDIR[5] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 4 | AXR4 | R/W | 0h | Determines drive on AXR4 output pin when the corresponding MCASP_PFUNC[4] and MCASP_PDIR[4] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |

Table 6-12. MCASP_PDOUT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 3 | AXR3 | R/W | 0h | Determines drive on AXR3 output pin when the corresponding MCASP_PFUNC[3] and MCASP_PDIR[3] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 2 | AXR2 | R/W | 0h | Determines drive on AXR2 output pin when the corresponding MCASP_PFUNC[2] and MCASP_PDIR[2] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 1 | AXR1 | R/W | 0h | Determines drive on AXR1 output pin when the corresponding MCASP_PFUNC[1] and MCASP_PDIR[1] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |
| 0 | AXR0 | R/W | 0h | Determines drive on AXR0 output pin when the corresponding MCASP_PFUNC[0] and MCASP_PDIR[0] bits are set to 1. 0h = Pin drives low. 1h = Pin drives high. |

6.7 MCASP_PDIN Register (Offset = 1Ch) [reset = 0h]

MCASP_PDIN is shown in [Figure 6-6](#) and described in [Table 6-14](#).

Return to [Summary Table](#).

The pin data input register (PDIN) holds the I/O pin state of each of the McASP pins. PDIN allows the actual value of the pin to be read, regardless of the state of PFUNC and PDIR.

Table 6-13. MCASP_PDIN Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 001Ch |
| MCASP1_CFG | 02B1 001Ch |
| MCASP2_CFG | 02B2 001Ch |

Figure 6-6. MCASP_PDIN Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|--------|-------|-------|--------|-------|-------|----------|
| AFSR | AHCLKR | ACLKR | AFSX | AHCLKX | ACLKX | AMUTE | RESERVED |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AXR15 | AXR14 | AXR13 | AXR12 | AXR11 | AXR10 | AXR9 | AXR8 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AXR7 | AXR6 | AXR5 | AXR4 | AXR3 | AXR2 | AXR1 | AXR0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 6-14. MCASP_PDIN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 31 | AFSR | R | 0h | Logic level on AFSR pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 30 | AHCLKR | R | 0h | Logic level on AHCLKR pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 29 | ACLKR | R | 0h | Logic level on ACLKR pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 28 | AFSX | R | 0h | Logic level on AFSX pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 27 | AHCLKX | R | 0h | Logic level on AHCLKX pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 26 | ACLKX | R | 0h | Logic level on ACLKX pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 25 | AMUTE | R | 0h | Logic level on AMUTE pin. 0h = Pin is logic low. 1h = Pin is logic high. |

Table 6-14. MCASP_PDIN Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 24-16 | RESERVED | R | 0h | Reserved |
| 15 | AXR15 | R | 0h | Logic level on AXR15 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 14 | AXR14 | R | 0h | Logic level on AXR14 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 13 | AXR13 | R | 0h | Logic level on AXR13 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 12 | AXR12 | R | 0h | Logic level on AXR12 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 11 | AXR11 | R | 0h | Logic level on AXR11 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 10 | AXR10 | R | 0h | Logic level on AXR10 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 9 | AXR9 | R | 0h | Logic level on AXR9 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 8 | AXR8 | R | 0h | Logic level on AXR8 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 7 | AXR7 | R | 0h | Logic level on AXR7 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 6 | AXR6 | R | 0h | Logic level on AXR6 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 5 | AXR5 | R | 0h | Logic level on AXR5 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 4 | AXR4 | R | 0h | Logic level on AXR4 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 3 | AXR3 | R | 0h | Logic level on AXR3 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 2 | AXR2 | R | 0h | Logic level on AXR2 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 1 | AXR1 | R | 0h | Logic level on AXR1 pin. 0h = Pin is logic low. 1h = Pin is logic high. |
| 0 | AXR0 | R | 0h | Logic level on AXR0 pin. 0h = Pin is logic low. 1h = Pin is logic high. |

6.8 MCASP_PDSET Register (Offset = 1Ch) [reset = 0h]

MCASP_PDSET is shown in [Figure 6-7](#) and described in [Table 6-16](#).

Return to [Summary Table](#).

The pin data set register (PDSET) is an alias of the pin data output register (PDOUT) for writes only. Writing a 1 to the PDSET bit sets the corresponding bit in PDOUT and, if PFUNC = 1 (GPIO function) and PDIR = 1 (output), drives a logic high on the pin.

Table 6-15. MCASP_PDSET Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 001Ch |
| MCASP1_CFG | 02B1 001Ch |
| MCASP2_CFG | 02B2 001Ch |

Figure 6-7. MCASP_PDSET Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|--------|-------|-------|--------|-------|-------|----------|
| AFSR | AHCLKR | ACLKR | AFSX | AHCLKX | ACLKX | AMUTE | RESERVED |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AXR15 | AXR14 | AXR13 | AXR12 | AXR11 | AXR10 | AXR9 | AXR8 |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AXR7 | AXR6 | AXR5 | AXR4 | AXR3 | AXR2 | AXR1 | AXR0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 6-16. MCASP_PDSET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 31 | AFSR | W | 0h | Allows the corresponding AFSR bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[31] bit is set to 1. |
| 30 | AHCLKR | W | 0h | Allows the corresponding AHCLKR bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[30] bit is set to 1. |
| 29 | ACLKR | W | 0h | Allows the corresponding ACLKR bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[29] bit is set to 1. |
| 28 | AFSX | W | 0h | Allows the corresponding AFSX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[28] bit is set to 1. |

Table 6-16. MCASP_PDSET Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 27 | AHCLKX | W | 0h | Allows the corresponding AHCLKX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[27] bit is set to 1. |
| 26 | ACLKX | W | 0h | Allows the corresponding ACLKX bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[26] bit is set to 1. |
| 25 | AMUTE | W | 0h | Allows the corresponding AMUTE bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[25] bit is set to 1. |
| 24-16 | RESERVED | R | 0h | Reserved |
| 15 | AXR15 | W | 0h | Allows the corresponding AXR15 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[15] bit is set to 1. |
| 14 | AXR14 | W | 0h | Allows the corresponding AXR14 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[14] bit is set to 1. |
| 13 | AXR13 | W | 0h | Allows the corresponding AXR13 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[13] bit is set to 1. |
| 12 | AXR12 | W | 0h | Allows the corresponding AXR12 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[12] bit is set to 1. |
| 11 | AXR11 | W | 0h | Allows the corresponding AXR11 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[11] bit is set to 1. |
| 10 | AXR10 | W | 0h | Allows the corresponding AXR10 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[10] bit is set to 1. |
| 9 | AXR9 | W | 0h | Allows the corresponding AXR9 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[9] bit is set to 1. |
| 8 | AXR8 | W | 0h | Allows the corresponding AXR8 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[8] bit is set to 1. |

Table 6-16. MCASP_PDSET Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 7 | AXR7 | W | 0h | Allows the corresponding AXR7 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[7] bit is set to 1. |
| 6 | AXR6 | W | 0h | Allows the corresponding AXR6 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[6] bit is set to 1. |
| 5 | AXR5 | W | 0h | Allows the corresponding AXR5 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[5] bit is set to 1. |
| 4 | AXR4 | W | 0h | Allows the corresponding AXR4 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[4] bit is set to 1. |
| 3 | AXR3 | W | 0h | Allows the corresponding AXR3 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[3] bit is set to 1. |
| 2 | AXR2 | W | 0h | Allows the corresponding AXR2 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[2] bit is set to 1. |
| 1 | AXR1 | W | 0h | Allows the corresponding AXR1 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[1] bit is set to 1. |
| 0 | AXR0 | W | 0h | Allows the corresponding AXR0 bit in MCASP_PDOUT to be set to a logic high without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[0] bit is set to 1. |

6.9 MCASP_PDCLR Register (Offset = 20h) [reset = 0h]

MCASP_PDCLR is shown in [Figure 6-8](#) and described in [Table 6-18](#).

Return to [Summary Table](#).

The pin data clear register (PDCLR) is an alias of the pin data output register (PDOUT) for writes only. Writing a 1 to the PDCLR bit clears the corresponding bit in PDOUT and, if PFUNC = 1 (GPIO function) and PDIR = 1 (output), drives a logic low on the pin.

Table 6-17. MCASP_PDCLR Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0020h |
| MCASP1_CFG | 02B1 0020h |
| MCASP2_CFG | 02B2 0020h |

Figure 6-8. MCASP_PDCLR Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|--------|--------|--------|--------|--------|--------|----------|
| AFSR | AHCLKR | ACLKR | AFSX | AHCLKX | ACLKX | AMUTE | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AXR15 | AXR14 | AXR13 | AXR12 | AXR11 | AXR10 | AXR9 | AXR8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AXR7 | AXR6 | AXR5 | AXR4 | AXR3 | AXR2 | AXR1 | AXR0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-18. MCASP_PDCLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 31 | AFSR | R/W | 0h | Allows the corresponding AFSR bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[31] bit is cleared to 0. |
| 30 | AHCLKR | R/W | 0h | Allows the corresponding AHCLKR bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[30] bit is cleared to 0. |
| 29 | ACLKR | R/W | 0h | Allows the corresponding ACLKR bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[29] bit is cleared to 0. |
| 28 | AFSX | R/W | 0h | Allows the corresponding AFSX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[28] bit is cleared to 0. |

Table 6-18. MCASP_PDCLR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 27 | AHCLKX | R/W | 0h | Allows the corresponding AHCLKX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[27] bit is cleared to 0. |
| 26 | ACLKX | R/W | 0h | Allows the corresponding ACLKX bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[26] bit is cleared to 0. |
| 25 | AMUTE | R/W | 0h | Allows the corresponding AMUTE bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[25] bit is cleared to 0. |
| 24-16 | RESERVED | R | 0h | Reserved |
| 15 | AXR15 | R/W | 0h | Allows the corresponding AXR[15] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[15] bit is cleared to 0. |
| 14 | AXR14 | R/W | 0h | Allows the corresponding AXR[14] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[14] bit is cleared to 0. |
| 13 | AXR13 | R/W | 0h | Allows the corresponding AXR[13] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[13] bit is cleared to 0. |
| 12 | AXR12 | R/W | 0h | Allows the corresponding AXR[12] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[12] bit is cleared to 0. |
| 11 | AXR11 | R/W | 0h | Allows the corresponding AXR[11] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[11] bit is cleared to 0. |
| 10 | AXR10 | R/W | 0h | Allows the corresponding AXR[10] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[10] bit is cleared to 0. |
| 9 | AXR9 | R/W | 0h | Allows the corresponding AXR[9] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[9] bit is cleared to 0. |
| 8 | AXR8 | R/W | 0h | Allows the corresponding AXR[8] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[8] bit is cleared to 0. |

Table 6-18. MCASP_PDCLR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 7 | AXR7 | R/W | 0h | Allows the corresponding AXR[7] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[7] bit is cleared to 0. |
| 6 | AXR6 | R/W | 0h | Allows the corresponding AXR[6] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[6] bit is cleared to 0. |
| 5 | AXR5 | R/W | 0h | Allows the corresponding AXR[5] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[5] bit is cleared to 0. |
| 4 | AXR4 | R/W | 0h | Allows the corresponding AXR[4] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[4] bit is cleared to 0. |
| 3 | AXR3 | R/W | 0h | Allows the corresponding AXR[3] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[3] bit is cleared to 0. |
| 2 | AXR2 | R/W | 0h | Allows the corresponding AXR[2] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[2] bit is cleared to 0. |
| 1 | AXR1 | R/W | 0h | Allows the corresponding AXR[1] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[1] bit is cleared to 0. |
| 0 | AXR0 | R/W | 0h | Allows the corresponding AXR[0] bit in MCASP_PDOUT to be cleared to a logic low without affecting other I/O pins controlled by the same port. 0h = No effect. 1h = MCASP_PDOUT[0] bit is cleared to 0. |

6.10 MCASP_TLGC Register (Offset = 30h) [reset = C091h]

MCASP_TLGC is shown in [Figure 6-9](#) and described in [Table 6-20](#).

Return to [Summary Table](#).

for IODFT

Table 6-19. MCASP_TLGC Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0030h |
| MCASP1_CFG | 02B1 0030h |
| MCASP2_CFG | 02B2 0030h |

Figure 6-9. MCASP_TLGC Register

| | | | | | | | |
|----------|--------|----------|----|--------|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MT | | RESERVED | | | | | MMS |
| R/W-0h | | R-0h | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ESEL | TOEN | MC | | PC | | TM | |
| R/W-0h | R/W-0h | R/W-0h | | R/W-0h | | R/W-1h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-20. MCASP_TLGC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved |
| 15-14 | MT | R/W | 3h | MISR on/off trigger command. These monitor trigger codes only are affective for the MISR signature capture when MC = 3h. MT Code effect on MISR: 0h = MISR capture start on the first active cycle decode of the IP bus activity and continues to update the signature for every active cycle. 1h = MISR capture start on the first active cycle decode of IP bus activity and continues to update the signature until the Execution Counter expires (TLEC). 2h = inactive/no effect 3h = inactive/no effect (default) |
| 13-9 | RESERVED | R | 0h | Reserved |
| 8 | MMS | R/W | 0h | Chooses the source of the MISR input: 0h = output register 1h = input capture |
| 7 | ESEL | R/W | 1h | Output enable select: 0h = test mode, and the functional OEN is gated off 1h = normal functional mode |
| 6 | TOEN | R/W | 0h | Test output enable control. This signal is paired with ESEL. TOEN is never 1 when ESEL is 1. When ESEL is 0 (test mode), TOEN is: 0h = output enabled 1h = output disabled Note: In boundary scan mode this signal is not selected, and the BSR controls output enables. |

Table 6-20. MCASP_TLGC Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 5-4 | MC | R/W | 1h | This defines the states of the MISR: 0h = download results 1h = hold current value 2h = load initial value (from PC bits) 3h = MISR enable to capture signature |
| 3-1 | PC | R/W | 0h | Pattern code defines the type of pattern that is selected for the artificial pattern generation logic in the IODFT. Modes: 0h = functional (default) 1h = random XOR 2h = random XNOR 3h = shift register 4h = hold current value Note: McASP does not have an input pattern generator (PG). |
| 0 | TM | R/W | 1h | At reset the value is 1 for normal functional mode. This bit is tied high, and should not be written to. |

6.11 MCASP_TLMR Register (Offset = 34h) [reset = 0h]

MCASP_TLMR is shown in [Figure 6-10](#) and described in [Table 6-22](#).

Return to [Summary Table](#).

for IODFT

Table 6-21. MCASP_TLMR Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0034h |
| MCASP1_CFG | 02B1 0034h |
| MCASP2_CFG | 02B2 0034h |

Figure 6-10. MCASP_TLMR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TLMR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-22. MCASP_TLMR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | TLMR | R/W | 0h | This contains the result signature of a given test after the download function is executed. |

6.12 MCASP_TLEC Register (Offset = 38h) [reset = 0h]

MCASP_TLEC is shown in [Figure 6-11](#) and described in [Table 6-24](#).

Return to [Summary Table](#).

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Table 6-23. MCASP_TLEC Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0038h |
| MCASP1_CFG | 02B1 0038h |
| MCASP2_CFG | 02B2 0038h |

Figure 6-11. MCASP_TLEC Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TLEC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-24. MCASP_TLEC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | TLEC | R/W | 0h | Contains the number of cycles during which the MISR signature will be accumulated. |

6.13 MCASP_GBLCTL Register (Offset = 44h) [reset = 0h]

MCASP_GBLCTL is shown in [Figure 6-12](#) and described in [Table 6-26](#).

Return to [Summary Table](#).

Table 6-25. MCASP_GBLCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0044h |
| MCASP1_CFG | 02B1 0044h |
| MCASP2_CFG | 02B2 0044h |

Figure 6-12. MCASP_GBLCTL Register

| | | | | | | | |
|----------|----|----|--------|--------|--------|----------|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | XFRST | XSMRST | XSRLR | XHCLKRST | XCLKRST |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RFRST | RSMRST | RSRLR | RHCLKRST | RCLKRST |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-26. MCASP_GBLCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-13 | RESERVED | R | 0h | Reserved |
| 12 | XFRST | R/W | 0h | Transmit frame sync generator reset enable bit. 0h = Transmit frame sync generator is reset. 1h = Transmit frame sync generator is active. When released from reset, the transmit frame sync generator begins counting serial clocks and generating frame sync as programmed. |
| 11 | XSMRST | R/W | 0h | Transmit state machine reset enable bit. 0h = Transmit state machine is held in reset. AXRn pin state: If MCASP_PFUNC[n] = 0 and MCASP_PDIR[n] = 1; then the serializer drives the AXRn pin to the state specified for inactive time slot (as determined by DISMOD bits in SRCTL). 1h = Transmit state machine is released from reset. When released from reset, the transmit state machine immediately transfers data from XRBUF[n] to XRSR[n]. The transmit state machine sets the underrun flag (XUNDRN) in MCASP_XSTAT, if XRBUF[n] have not been preloaded with data before reset is released. The transmit state machine also immediately begins detecting frame sync and is ready to transmit. Transmit TDM time slot begins at slot 0 after reset is released. |

Table 6-26. MCASP_GBLCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 10 | XSRCLR | R/W | 0h | Transmit serializer clear enable bit. By clearing then setting this bit, the transmit buffer is flushed to an empty state [XDATA = 1]. If XSMRST = 1, XSRCLR = 1, XDATA = 1, and XBUF is not loaded with new data before the start of the next active time slot, an underrun will occur. 0h = Transmit serializers are cleared. 1h = Transmit serializers are active. When the transmit serializers are first taken out of reset (XSRCLR changes from 0 to 1), the transmit data ready bit (XDATA) in MCASP_XSTAT is set to indicate XBUF is ready to be written. |
| 9 | XHCLKRST | R/W | 0h | Transmit high-frequency clock divider reset enable bit. 0h = Transmit high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1h = Transmit high-frequency clock divider is running. |
| 8 | XCLKRST | R/W | 0h | Transmit clock divider reset enable bit. 0h = Transmit clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 1h = Transmit clock divider is running. |
| 7-5 | RESERVED | R | 0h | Reserved |
| 4 | RFRST | R/W | 0h | Receive frame sync generator reset enable bit. 0h = Receive frame sync generator is reset. 1h = Receive frame sync generator is active. When released from reset, the receive frame sync generator begins counting serial clocks and generating frame sync as programmed. |
| 3 | RSMRST | R/W | 0h | Receive state machine reset enable bit. 0h = Receive state machine is held in reset. 1h = Receive state machine is released from reset. When released from reset, the receive state machine immediately begins detecting frame sync and is ready to receive. Receive TDM time slot begins at slot 0 after reset is released. |
| 2 | RSRCLR | R/W | 0h | Receive serializer clear enable bit. By clearing then setting this bit, the receive buffer is flushed. 0h = Receive serializers are cleared. 1h = Receive serializers are active. |
| 1 | RHCLKRST | R/W | 0h | Receive high-frequency clock divider reset enable bit. 0h = Receive high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1h = Receive high-frequency clock divider is running. |
| 0 | RCLKRST | R/W | 0h | Receive high-frequency clock divider reset enable bit. 0h = Receive clock divider is held in reset. When the clock divider is in reset, it passes through a divide-by-1 of its input. 1h = Receive clock divider is running. |

6.14 MCASP_AMUTE Register (Offset = 48h) [reset = 0h]

MCASP_AMUTE is shown in [Figure 6-13](#) and described in [Table 6-28](#).

Return to [Summary Table](#).

Table 6-27. MCASP_AMUTE Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0048h |
| MCASP1_CFG | 02B1 0048h |
| MCASP2_CFG | 02B2 0048h |

Figure 6-13. MCASP_AMUTE Register

| | | | | | | | |
|----------|--------|--------|---------|---------|---------|---------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | XDMAERR | RDMAERR | XCKFAIL | RCKFAIL | XSUNCERR |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RSUNCERR | XUNDRN | ROVRN | INSTAT | INEN | INPOL | MUTEN | |
| R/W-0h | R/W-0h | R/W-0h | R-0h | R/W-0h | R/W-0h | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-28. MCASP_AMUTE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-13 | RESERVED | R/W | 0h | Reserved |
| 12 | XDMAERR | R/W | 0h | If transmit DMA error [XDMAERR], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of transmit DMA error is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of transmit DMA error, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 11 | RDMAERR | R/W | 0h | If receive DMA error [RDMAERR], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of receive DMA error is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of receive DMA error, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 10 | XCKFAIL | R/W | 0h | If transmit clock failure [XCKFAIL], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of transmit clock failure is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of transmit clock failure, MCASP_AMUTE is active and is driven according to MUTEN bit. |

Table 6-28. MCASP_AMUTE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 9 | RCKFAIL | R/W | 0h | If receive clock failure [RCKFAIL], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of receive clock failure is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of receive clock failure, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 8 | XSYNCERR | R/W | 0h | If unexpected transmit frame sync error [XSYNCERR], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of unexpected transmit frame sync error is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of unexpected transmit frame sync error, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 7 | RSYNCERR | R/W | 0h | If unexpected receive frame sync error [RSYNCERR], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of unexpected receive frame sync error is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of unexpected receive frame sync error, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 6 | XUNDRN | R/W | 0h | If transmit underrun error [XUNDRN], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of transmit underrun error is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of transmit underrun error, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 5 | ROVRN | R/W | 0h | If receiver overrun error [ROVRN], drive MCASP_AMUTE active enable bit. 0h = Drive is disabled. Detection of receiver overrun error is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). Upon detection of receiver overrun error, MCASP_AMUTE is active and is driven according to MUTEN bit. |
| 4 | INSTAT | R | 0h | Determines drive on AXRn pin when MCASP_PFUNC[n] and MCASP_PDIR[n] bits are set to 1. 0h = AMUTEIN pin is inactive. 1h = AMUTEIN pin is active. Audio mute in error is detected. |
| 3 | INEN | R/W | 0h | Drive MCASP_AMUTE active when AMUTEIN error is active [INSTAT = 1]. 0h = Drive is disabled. AMUTEIN is ignored by MCASP_AMUTE. 1h = Drive is enabled (active). INSTAT = 1 drives MCASP_AMUTE active. |
| 2 | INPOL | R/W | 0h | Audio mute in [AMUTEIN] polarity select bit. 0h = Polarity is active high. A high on AMUTEIN sets INSTAT to 1. 1h = Polarity is active low. A low on AMUTEIN sets INSTAT to 1. |
| 1-0 | MUTEN | R/W | 0h | MCASP_AMUTE pin enable bit [unless overridden by GPIO registers]. 0h = MCASP_AMUTE pin is disabled, pin goes to tri-state condition. 1h = MCASP_AMUTE pin is driven high if error is detected. 2h = MCASP_AMUTE pin is driven low if error is detected. 3h = Reserved |

6.15 MCASP_LBCTL Register (Offset = 4Ch) [reset = 0h]

MCASP_LBCTL is shown in [Figure 6-14](#) and described in [Table 6-30](#).

Return to [Summary Table](#).

Table 6-29. MCASP_LBCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 004Ch |
| MCASP1_CFG | 02B1 004Ch |
| MCASP2_CFG | 02B2 004Ch |

Figure 6-14. MCASP_LBCTL Register

| | | | | | | | |
|----------|----|----|--------|--------|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | IOLBEN | MODE | | ORD | DLBEN |
| R/W-0h | | | R/W-0h | R/W-0h | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-30. MCASP_LBCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-5 | RESERVED | R/W | 0h | |
| 4 | IOLBEN | R/W | 0h | I/O loopback enable. Chip-level loopback; looped back through I/O buffers. 0h = I/O loopback disabled 1h = I/O loopback enabled Note: These are only valid if LBEN = 1. If LBEN = 0, neither internal nor I/O loopback will be selected. |
| 3-2 | MODE | R/W | 0h | Loopback generator mode bits. Applies only when loopback mode is enabled [DLBEN = 1]. 0h = Default and reserved on loopback mode (DLBEN = 1). When in non-loopback mode (DLBEN = 0), MODE should be left at default (00). When in loopback mode (DLBEN = 1), MODE = 00 is reserved and is not applicable. 1h = Transmit clock and frame sync generators used by both transmit and receive sections. When in loopback mode (DLBEN = 1), MODE must be 01. 2h = Reserved. 3h = Reserved. |
| 1 | ORD | R/W | 0h | Loopback order bit when loopback mode is enabled [DLBEN = 1]. 0h = Odd serializers N + 1 transmit to even serializers N that receive. The corresponding serializers must be programmed properly. 1h = Even serializers N transmit to odd serializers N + 1 that receive. The corresponding serializers must be programmed properly. |

Table 6-30. MCASP_LBCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | DLBEN | R/W | 0h | Loopback mode enable bit. 0h = Loopback mode is disabled. 1h = Loopback mode is enabled. |

6.16 MCASP_TXDITCTL Register (Offset = 50h) [reset = 0h]

MCASP_TXDITCTL is shown in [Figure 6-15](#) and described in [Table 6-32](#).

Return to [Summary Table](#).

Table 6-31. MCASP_TXDITCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0050h |
| MCASP1_CFG | 02B1 0050h |
| MCASP2_CFG | 02B2 0050h |

Figure 6-15. MCASP_TXDITCTL Register

| | | | | | | | |
|----------|----|----|----|--------|--------|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | VB | VA | RESERVED | DITEN |
| R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-32. MCASP_TXDITCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R/W | 0h | Reserved |
| 3 | VB | R/W | 0h | Valid bit for odd time slots [DIT right subframe]. 0h = V bit is 0 during odd DIT subframes. 1h = V bit is 1 during odd DIT subframes. |
| 2 | VA | R/W | 0h | Valid bit for even time slots [DIT left subframe]. 0h = V bit is 0 during even DIT subframes. 1h = V bit is 1 during even DIT subframes. |
| 1 | RESERVED | R/W | 0h | Reserved |
| 0 | DITEN | R/W | 0h | DIT mode enable bit. DITEN should only be changed while the XSMRST bit in MCASP_GBLCTL is in reset [and for startup, XSRCLR also in reset]. However, it is not necessary to reset the XCLKRST or XHCLKRST bits in MCASP_GBLCTL to change DITEN. 0h = DIT mode is disabled. Transmitter operates in TDM or burst mode. 1h = DIT mode is enabled. Transmitter operates in DIT encoded mode. |

6.17 MCASP_GBLCTLR Register (Offset = 60h) [reset = 0h]

MCASP_GBLCTLR is shown in [Figure 6-16](#) and described in [Table 6-34](#).

Return to [Summary Table](#).

Table 6-33. MCASP_GBLCTLR Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0060h |
| MCASP1_CFG | 02B1 0060h |
| MCASP2_CFG | 02B2 0060h |

Figure 6-16. MCASP_GBLCTLR Register

| | | | | | | | |
|----------|----|----|--------|--------|--------|----------|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | XFRST | XSMRST | XSRCLR | XHCLKRST | XCLKRST |
| R/W-0h | | | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RFRST | RSMRST | RSRCLR | RHCLKRST | RCLKRST |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-34. MCASP_GBLCTLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-13 | RESERVED | R/W | 0h | Reserved |
| 12 | XFRST | R | 0h | Transmit frame sync generator reset enable bit. A read of this bit returns the XFRST bit value of MCASP_GBLCTL. Writes have no effect. |
| 11 | XSMRST | R | 0h | Transmit state machine reset enable bit. A read of this bit returns the XSMRST bit value of MCASP_GBLCTL. Writes have no effect. |
| 10 | XSRCLR | R | 0h | Transmit serializer clear enable bit. A read of this bit returns the XSRCLR bit value of MCASP_GBLCTL. Writes have no effect. |
| 9 | XHCLKRST | R | 0h | Transmit high-frequency clock divider reset enable bit. A read of this bit returns the XHCLKRST bit value of MCASP_GBLCTL. Writes have no effect. |
| 8 | XCLKRST | R | 0h | Transmit clock divider reset enable bit. A read of this bit returns the XCLKRST bit value of MCASP_GBLCTL. Writes have no effect. |
| 7-5 | RESERVED | R/W | 0h | Reserved |
| 4 | RFRST | R/W | 0h | Receive frame sync generator reset enable bit. A write to this bit affects the RFRST bit of MCASP_GBLCTL. 0h = Receive frame sync generator is reset. 1h = Receive frame sync generator is active. |

Table 6-34. MCASP_GBLCTLR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 3 | RSMRST | R/W | 0h | Receive state machine reset enable bit. A write to this bit affects the RSMRST bit of MCASP_GBLCTL. 0h = Receive state machine is held in reset. 1h = Receive state machine is released from reset. |
| 2 | RSRCLR | R/W | 0h | Receive serializer clear enable bit. A write to this bit affects the RSRCLR bit of MCASP_GBLCTL. 0h = Receive serializers are cleared. 1h = Receive serializers are active. |
| 1 | RHCLKRST | R/W | 0h | Receive high-frequency clock divider reset enable bit. A write to this bit affects the RHCLKRST bit of MCASP_GBLCTL. 0h = Receive high-frequency clock divider is held in reset and passes through its input as divide-by-1. 1h = Receive high-frequency clock divider is running. |
| 0 | RCLKRST | R/W | 0h | Receive clock divider reset enable bit. A write to this bit affects the RCLKRST bit of MCASP_GBLCTL. 0h = Receive clock divider is held in reset. 1h = Receive clock divider is running. |

6.18 MCASP_RXMASK Register (Offset = 64h) [reset = 0h]

MCASP_RXMASK is shown in [Figure 6-17](#) and described in [Table 6-36](#).

Return to [Summary Table](#).

Table 6-35. MCASP_RXMASK Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0064h |
| MCASP1_CFG | 02B1 0064h |
| MCASP2_CFG | 02B2 0064h |

Figure 6-17. MCASP_RXMASK Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| RMASK31 | RMASK30 | RMASK29 | RMASK28 | RMASK27 | RMASK26 | RMASK25 | RMASK24 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RMASK23 | RMASK22 | RMASK21 | RMASK20 | RMASK19 | RMASK18 | RMASK17 | RMASK16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RMASK15 | RMASK14 | RMASK13 | RMASK12 | RMASK11 | RMASK10 | RMASK9 | RMASK8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RMASK7 | RMASK6 | RMASK5 | RMASK4 | RMASK3 | RMASK2 | RMASK1 | RMASK0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-36. MCASP_RXMASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 31 | RMASK31 | R/W | 0h | Receive data mask 31 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 30 | RMASK30 | R/W | 0h | Receive data mask 30 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 29 | RMASK29 | R/W | 0h | Receive data mask 29 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 28 | RMASK28 | R/W | 0h | Receive data mask 28 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |

Table 6-36. MCASP_RXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 27 | RMASK27 | R/W | 0h | Receive data mask 27 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 26 | RMASK26 | R/W | 0h | Receive data mask 26 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 25 | RMASK25 | R/W | 0h | Receive data mask 25 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 24 | RMASK24 | R/W | 0h | Receive data mask 24 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 23 | RMASK23 | R/W | 0h | Receive data mask 23 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 22 | RMASK22 | R/W | 0h | Receive data mask 22 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 21 | RMASK21 | R/W | 0h | Receive data mask 21 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 20 | RMASK20 | R/W | 0h | Receive data mask 20 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |

Table 6-36. MCASP_RXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 19 | RMASK19 | R/W | 0h | Receive data mask 19 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 18 | RMASK18 | R/W | 0h | Receive data mask 18 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 17 | RMASK17 | R/W | 0h | Receive data mask 17 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 16 | RMASK16 | R/W | 0h | Receive data mask 16 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 15 | RMASK15 | R/W | 0h | Receive data mask 15 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 14 | RMASK14 | R/W | 0h | Receive data mask 14 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 13 | RMASK13 | R/W | 0h | Receive data mask 13 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 12 | RMASK12 | R/W | 0h | Receive data mask 12 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |

Table 6-36. MCASP_RXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 11 | RMASK11 | R/W | 0h | Receive data mask 11 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 10 | RMASK10 | R/W | 0h | Receive data mask 10 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 9 | RMASK9 | R/W | 0h | Receive data mask 9 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 8 | RMASK8 | R/W | 0h | Receive data mask 8 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 7 | RMASK7 | R/W | 0h | Receive data mask 7 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 6 | RMASK6 | R/W | 0h | Receive data mask 6 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 5 | RMASK5 | R/W | 0h | Receive data mask 5 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 4 | RMASK4 | R/W | 0h | Receive data mask 4 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |

Table 6-36. MCASP_RXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 3 | RMASK3 | R/W | 0h | Receive data mask 3 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 2 | RMASK2 | R/W | 0h | Receive data mask 2 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 1 | RMASK1 | R/W | 0h | Receive data mask 1 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |
| 0 | RMASK0 | R/W | 0h | Receive data mask 0 enable bit. 0h = Corresponding bit of receive data (after passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (RPAD and RPBIT bits in MCASP_RFMT). 1h = Corresponding bit of receive data (after passing through reverse and rotate units) is returned to CPU or DMA. |

6.19 MCASP_RXFMT Register (Offset = 68h) [reset = 0h]

MCASP_RXFMT is shown in [Figure 6-18](#) and described in [Table 6-38](#).

Return to [Summary Table](#).

Table 6-37. MCASP_RXFMT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0068h |
| MCASP1_CFG | 02B1 0068h |
| MCASP2_CFG | 02B2 0068h |

Figure 6-18. MCASP_RXFMT Register

| | | | | | | | |
|----------|------|--------|--------|--------|--------|---------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | RDATDLY | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RRVRS | RPAD | | RPBIT | | | | |
| R/W-0h | | R/W-0h | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RSSZ | | | | RBUSEL | RROT | | |
| R/W-0h | | | R/W-0h | | R/W-0h | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-38. MCASP_RXFMT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-18 | RESERVED | R/W | 0h | Reserved |
| 17-16 | RDATDLY | R/W | 0h | Receive bit delay. 0h = 0-bit delay. The first receive data bit, AXRn, occurs in same ACLKR cycle as the receive frame sync (AFSR). 1h = 1-bit delay. The first receive data bit, AXRn, occurs one ACLKR cycle after the receive frame sync (AFSR). 2h = 2-bit delay. The first receive data bit, AXRn, occurs two ACLKR cycles after the receive frame sync (AFSR). 3h = Reserved. |
| 15 | RRVRS | R/W | 0h | Receive serial bitstream order. 0h = Bitstream is LSB first. No bit reversal is performed in receive format bit reverse unit. 1h = Bitstream is MSB first. Bit reversal is performed in receive format bit reverse unit. |
| 14-13 | RPAD | R/W | 0h | Pad value for extra bits in slot not belonging to the word. This field only applies to bits when MCASP_RMASK[n] = 0. 0h = Pad extra bits with 0. 1h = Pad extra bits with 1. 2h = Pad extra bits with one of the bits from the word as specified by RPBIT bits. 3h = Reserved. |

Table 6-38. MCASP_RXFMT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|---|
| 12-8 | RPBIT | R/W | 0h | RPBIT value determines which bit [as read by the CPU or DMA from RBUF[n]] is used to pad the extra bits. This field only applies when RPAD = 2h. 0h = Pad with bit 0 value. 1h = Pad with bit 1 to bit 31 value from 1h to 1Fh. |
| 7-4 | RSSZ | R/W | 0h | Receive slot size. 0h = Reserved. 1h = Reserved. 2h = Reserved. 3h = Slot size is 8 bits. 4h = Reserved 5h = Slot size is 12 bits. 6h = Reserved 7h = Slot size is 16 bits. 8h = Reserved 9h = Slot size is 20 bits. Ah = Reserved Bh = Slot size is 24 bits Ch = Reserved Dh = Slot size is 28 bits. Eh = Reserved Fh = Slot size is 32 bits. |
| 3 | RBUSEL | R/W | 0h | Selects whether reads from serializer buffer XRBUF[n] originate from the configuration bus [CFG] or the data [DAT] port. 0h = Reads from XRBUF[n] originate on data port. Reads from XRBUF[n] on configuration bus are ignored. 1h = Reads from XRBUF[n] originate on configuration bus. Reads from XRBUF[n] on data port are ignored. |
| 2-0 | RROT | R/W | 0h | Right-rotation value for receive rotate right format unit. 0h = Rotate right by 0 (no rotation). 1h = Rotate right by 4 bit positions. 2h = Rotate right by 8 bit positions. 3h = Rotate right by 12 bit positions. 4h = Rotate right by 16 bit positions. 5h = Rotate right by 20 bit positions. 6h = Rotate right by 24 bit positions. 7h = Rotate right by 28 bit positions. |

6.20 MCASP_RXFMCTL Register (Offset = 6Ch) [reset = 0h]

MCASP_RXFMCTL is shown in [Figure 6-19](#) and described in [Table 6-40](#).

Return to [Summary Table](#).

Table 6-39. MCASP_RXFMCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 006Ch |
| MCASP1_CFG | 02B1 006Ch |
| MCASP2_CFG | 02B2 006Ch |

Figure 6-19. MCASP_RXFMCTL Register

| | | | | | | | |
|----------|----------|----|--------|----------|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RMOD | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RMOD | RESERVED | | FRWID | RESERVED | | FSRM | FSRP |
| R/W-0h | R/W-0h | | R/W-0h | R/W-0h | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-40. MCASP_RXFMCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | 0h | Reserved |
| 15-7 | RMOD | R/W | 0h | Receive frame sync mode select bits. 1FFh = Reserved from 181h to 1FFh. 0h = Burst mode. 1h = Reserved. 2h = 2-slot TDM (I2S mode) to 32-slot TDM from 2h to 20h. 21h = Reserved from 21h to 17Fh. 180h = 384-slot TDM (external DIR IC inputting 384-slot DIR frames to McASP over I2S interface). 181h = Reserved from 181h to 1FFh. |
| 6-5 | RESERVED | R/W | 0h | Reserved |
| 4 | FRWID | R/W | 0h | Receive frame sync width select bit indicates the width of the receive frame sync [AFSR] during its active period. 0h = Single bit. 1h = Single word. |
| 3-2 | RESERVED | R/W | 0h | Reserved |
| 1 | FSRM | R/W | 0h | Receive frame sync generation select bit. 0h = Externally-generated receive frame sync. 1h = Internally-generated receive frame sync. |

Table 6-40. MCASP_RXFMCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | FSRP | R/W | 0h | Receive frame sync polarity select bit. 0h = A rising edge on receive frame sync (AFSR) indicates the beginning of a frame. 1h = A falling edge on receive frame sync (AFSR) indicates the beginning of a frame. |

6.21 MCASP_ACLKRCTL Register (Offset = 70h) [reset = 0h]

MCASP_ACLKRCTL is shown in [Figure 6-20](#) and described in [Table 6-42](#).

Return to [Summary Table](#).

Table 6-41. MCASP_ACLKRCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0070h |
| MCASP1_CFG | 02B1 0070h |
| MCASP2_CFG | 02B2 0070h |

Figure 6-20. MCASP_ACLKRCTL Register

| | | | | | | | |
|----------|----------|--------|---------|---------|---------|---------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | BUSY | DIVBUSY | ADJBUSY | CLKRADJ | |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLKRP | RESERVED | CLKRM | CLKRDIV | | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | | |

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 6-42. MCASP_ACLKRCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-21 | RESERVED | R/W | 0h | Reserved |
| 20 | BUSY | R/W | 0h | The OR of bits 18 and 19, indicating that some clk change is in progress when high. |
| 19 | DIVBUSY | R/W | 0h | Divider change in progress (same behavior as bit 18) |
| 18 | ADJBUSY | R/W | 0h | One-shot adj in progress (a BUSY bit that is set when an adj is in progress, cleared when the adjustment has taken effect) |
| 17-16 | CLKRADJ | W | 0h | CLKRDIV one-shot adjustment control. If CLKRDIV is set such that there are "m" input clocks per one output clock, then for one output cycle: 0h = (m+0) input clocks per output clock, no adjustment 1h = (m-1) input clocks per output clock 2h = (m+1) input clocks per output clock 3h = (m+0) input clocks per output clock, no adjustment |
| 15-8 | RESERVED | R/W | 0h | Reserved |
| 7 | CLKRP | R/W | 0h | Bitstream clock polarity for receive section: 0h = Falling Edge. Receiver captures sample data on the falling edge of the serial clock, so the EXTERNAL transmitter driving this receiver must shift data out on the rising edge of the serial clock. 1h = Rising Edge. Receiver captures sample data on the rising edge of the serial clock, so the EXTERNAL transmitter driving this receiver must shift data out on the falling edge of the serial clock. |
| 6 | RESERVED | R/W | 0h | Reserved |
| 5 | CLKRM | R/W | 0h | Receive clock source: 0h = External Transmit Clock From ACLKR pin 1h = Internal (output of divider), output clock on ACLKR pin. |

Table 6-42. MCASP_ACLKRCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 4-0 | CLKRDIV | R/W | 0h | Receive clock divide ratio from high frequency transmit clock: 00000b = /1 00001b = /2 ... 11111b = /32 All values between /1 and /32 are supported. |

6.22 MCASP_AHCLKRCTL Register (Offset = 74h) [reset = 0h]

MCASP_AHCLKRCTL is shown in [Figure 6-21](#) and described in [Table 6-44](#).

Return to [Summary Table](#).

Table 6-43. MCASP_AHCLKRCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0074h |
| MCASP1_CFG | 02B1 0074h |
| MCASP2_CFG | 02B2 0074h |

Figure 6-21. MCASP_AHCLKRCTL Register

| | | | | | | | |
|----------|--------|----------|--------|----------|---------|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | BUSY | DIVBUSY | ADJBUSY | HCLKRADJ | |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| HCLKRM | HCLKRP | RESERVED | | HCLKRDIV | | | |
| R/W-0h | R/W-0h | R/W-0h | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HCLKRDIV | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 6-44. MCASP_AHCLKRCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-21 | RESERVED | R/W | 0h | Reserved |
| 20 | BUSY | R/W | 0h | The OR of bits 18 and 19, indicating that some clk change is in progress when high. |
| 19 | DIVBUSY | R/W | 0h | Divider change in progress (same behavior as bit 18) |
| 18 | ADJBUSY | R/W | 0h | One-shot adj in progress (a BUSY bit that is set when an adj is in progress, cleared when the adjustment has taken effect). |
| 17-16 | HCLKRADJ | W | 0h | HCLKRDIV one-shot adjustment control If HCLKRDIV is set such that there are "m" input clocks per one output clock, then for one output cycle: 0h = (m+0) input clocks per output clock 1h = (m-1) input clocks per output clock 2h = (m+1) input clocks per output clock 3h = (m+0) input clocks per output clock |
| 15 | HCLKRM | R/W | 0h | High frequency receive clock source: 0h = External Clock on AHCLKR pin passes through divider (typically set to /1). 1h = Internal, CPU Clock passed through divider. Divider output on AHCLKR pin. |
| 14 | HCLKRP | R/W | 0h | high frequency clock polarity: 0h = AHCLKR not inverted before divider. Rising Edge of AHCLKR causes edges on ACLKR when internally generated. 1h = AHCLKR inverted before divider. Falling Edge of AHCLKR causes edges on ACLKR when internally generated. For the /1 clock divider case, AHCLKR is just passed through to ACLKR. For odd dividers, both edges of AHCLKR cause ACLKR to toggle but this polarity bit defines which is first edge of AHCLKR to affect ACLKR. |
| 13-12 | RESERVED | R/W | 0h | Reserved |

Table 6-44. MCASP_AHCLKRCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 11-0 | HCLKRDIV | R/W | 0h | Receive clock divide ratio from CPU master clock or external high frequency clock: 0000 0000 0000b = /1 0000 0000 0001b = /2 ... 1111 1111 1111b = /4096 All values between /1, and /4096 are supported. |

6.23 MCASP_RXTDM Register (Offset = 78h) [reset = 0h]

MCASP_RXTDM is shown in [Figure 6-22](#) and described in [Table 6-46](#).

Return to [Summary Table](#).

Table 6-45. MCASP_RXTDM Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0078h |
| MCASP1_CFG | 02B1 0078h |
| MCASP2_CFG | 02B2 0078h |

Figure 6-22. MCASP_RXTDM Register

| | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RTDMS31 | RTDMS30 | RTDMS29 | RTDMS28 | RTDMS27 | RTDMS26 | RTDMS25 | RTDMS24 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RTDMS23 | RTDMS22 | RTDMS21 | RTDMS20 | RTDMS19 | RTDMS18 | RTDMS17 | RTDMS16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RTDMS15 | RTDMS14 | RTDMS13 | RTDMS12 | RTDMS11 | RTDMS10 | RTDMS9 | RTDMS8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTDMS7 | RTDMS6 | RTDMS5 | RTDMS4 | RTDMS3 | RTDMS2 | RTDMS1 | RTDMS0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-46. MCASP_RXTDM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 31 | RTDMS31 | R/W | 0h | Receiver mode during TDM time slot 31. 0h = Receive TDM time slot 31 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 31 is active. The receive serializer shifts in data during this slot. |
| 30 | RTDMS30 | R/W | 0h | Receiver mode during TDM time slot 30. 0h = Receive TDM time slot 30 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 30 is active. The receive serializer shifts in data during this slot. |
| 29 | RTDMS29 | R/W | 0h | Receiver mode during TDM time slot 29. 0h = Receive TDM time slot 29 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 29 is active. The receive serializer shifts in data during this slot. |
| 28 | RTDMS28 | R/W | 0h | Receiver mode during TDM time slot 28. 0h = Receive TDM time slot 28 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 28 is active. The receive serializer shifts in data during this slot. |

Table 6-46. MCASP_RXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 27 | RTDMS27 | R/W | 0h | Receiver mode during TDM time slot 27. 0h = Receive TDM time slot 27 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 27 is active. The receive serializer shifts in data during this slot. |
| 26 | RTDMS26 | R/W | 0h | Receiver mode during TDM time slot 26. 0h = Receive TDM time slot 26 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 26 is active. The receive serializer shifts in data during this slot. |
| 25 | RTDMS25 | R/W | 0h | Receiver mode during TDM time slot 25. 0h = Receive TDM time slot 25 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 25 is active. The receive serializer shifts in data during this slot. |
| 24 | RTDMS24 | R/W | 0h | Receiver mode during TDM time slot 24. 0h = Receive TDM time slot 24 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 24 is active. The receive serializer shifts in data during this slot. |
| 23 | RTDMS23 | R/W | 0h | Receiver mode during TDM time slot 23. 0h = Receive TDM time slot 23 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 23 is active. The receive serializer shifts in data during this slot. |
| 22 | RTDMS22 | R/W | 0h | Receiver mode during TDM time slot 22. 0h = Receive TDM time slot 22 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 22 is active. The receive serializer shifts in data during this slot. |
| 21 | RTDMS21 | R/W | 0h | Receiver mode during TDM time slot 21. 0h = Receive TDM time slot 21 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 21 is active. The receive serializer shifts in data during this slot. |
| 20 | RTDMS20 | R/W | 0h | Receiver mode during TDM time slot 20. 0h = Receive TDM time slot 20 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 20 is active. The receive serializer shifts in data during this slot. |
| 19 | RTDMS19 | R/W | 0h | Receiver mode during TDM time slot 19. 0h = Receive TDM time slot 19 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 19 is active. The receive serializer shifts in data during this slot. |
| 18 | RTDMS18 | R/W | 0h | Receiver mode during TDM time slot 18. 0h = Receive TDM time slot 18 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 18 is active. The receive serializer shifts in data during this slot. |

Table 6-46. MCASP_RXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 17 | RTDMS17 | R/W | 0h | Receiver mode during TDM time slot 17. 0h = Receive TDM time slot 17 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 17 is active. The receive serializer shifts in data during this slot. |
| 16 | RTDMS16 | R/W | 0h | Receiver mode during TDM time slot 16. 0h = Receive TDM time slot 16 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 16 is active. The receive serializer shifts in data during this slot. |
| 15 | RTDMS15 | R/W | 0h | Receiver mode during TDM time slot 15. 0h = Receive TDM time slot 15 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 15 is active. The receive serializer shifts in data during this slot. |
| 14 | RTDMS14 | R/W | 0h | Receiver mode during TDM time slot 14. 0h = Receive TDM time slot 14 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 14 is active. The receive serializer shifts in data during this slot. |
| 13 | RTDMS13 | R/W | 0h | Receiver mode during TDM time slot 13. 0h = Receive TDM time slot 13 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 13 is active. The receive serializer shifts in data during this slot. |
| 12 | RTDMS12 | R/W | 0h | Receiver mode during TDM time slot 12. 0h = Receive TDM time slot 12 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 12 is active. The receive serializer shifts in data during this slot. |
| 11 | RTDMS11 | R/W | 0h | Receiver mode during TDM time slot 11. 0h = Receive TDM time slot 11 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 11 is active. The receive serializer shifts in data during this slot. |
| 10 | RTDMS10 | R/W | 0h | Receiver mode during TDM time slot 10. 0h = Receive TDM time slot 10 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 10 is active. The receive serializer shifts in data during this slot. |
| 9 | RTDMS9 | R/W | 0h | Receiver mode during TDM time slot 9. 0h = Receive TDM time slot 9 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 9 is active. The receive serializer shifts in data during this slot. |
| 8 | RTDMS8 | R/W | 0h | Receiver mode during TDM time slot 8. 0h = Receive TDM time slot 8 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 8 is active. The receive serializer shifts in data during this slot. |

Table 6-46. MCASP_RXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 7 | RTDMS7 | R/W | 0h | Receiver mode during TDM time slot 7. 0h = Receive TDM time slot 7 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 7 is active. The receive serializer shifts in data during this slot. |
| 6 | RTDMS6 | R/W | 0h | Receiver mode during TDM time slot 6. 0h = Receive TDM time slot 6 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 6 is active. The receive serializer shifts in data during this slot. |
| 5 | RTDMS5 | R/W | 0h | Receiver mode during TDM time slot 5. 0h = Receive TDM time slot 5 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 5 is active. The receive serializer shifts in data during this slot. |
| 4 | RTDMS4 | R/W | 0h | Receiver mode during TDM time slot 4. 0h = Receive TDM time slot 4 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 4 is active. The receive serializer shifts in data during this slot. |
| 3 | RTDMS3 | R/W | 0h | Receiver mode during TDM time slot 3. 0h = Receive TDM time slot 3 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 3 is active. The receive serializer shifts in data during this slot. |
| 2 | RTDMS2 | R/W | 0h | Receiver mode during TDM time slot 2. 0h = Receive TDM time slot 2 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 2 is active. The receive serializer shifts in data during this slot. |
| 1 | RTDMS1 | R/W | 0h | Receiver mode during TDM time slot 1. 0h = Receive TDM time slot 1 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 1 is active. The receive serializer shifts in data during this slot. |
| 0 | RTDMS0 | R/W | 0h | Receiver mode during TDM time slot 0. 0h = Receive TDM time slot 0 is inactive. The receive serializer does not shift in data during this slot. 1h = Receive TDM time slot 0 is active. The receive serializer shifts in data during this slot. |

6.24 MCASP_EVTCTLR Register (Offset = 7Ch) [reset = 0h]

MCASP_EVTCTLR is shown in [Figure 6-23](#) and described in [Table 6-48](#).

Return to [Summary Table](#).

Table 6-47. MCASP_EVTCTLR Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 007Ch |
| MCASP1_CFG | 02B1 007Ch |
| MCASP2_CFG | 02B2 007Ch |

Figure 6-23. MCASP_EVTCTLR Register

| | | | | | | | |
|----------|----------|--------|--------|---------|---------|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RSTAFRM | RESERVED | RDATA | RLAST | RDMAERR | RCKFAIL | RSYNCERR | ROVRN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-48. MCASP_EVTCTLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-8 | RESERVED | R/W | 0h | Reserved |
| 7 | RSTAFRM | R/W | 0h | Receive start of frame interrupt enable bit. 0h = Interrupt is disabled. A receive start of frame interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. A receive start of frame interrupt generates a MCASP receive interrupt (RINT). |
| 6 | RESERVED | R/W | 0h | Reserved |
| 5 | RDATA | R/W | 0h | Receive data ready interrupt enable bit. 0h = Interrupt is disabled. A receive data ready interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. A receive data ready interrupt generates a MCASP receive interrupt (RINT). |
| 4 | RLAST | R/W | 0h | Receive last slot interrupt enable bit. 0h = Interrupt is disabled. A receive last slot interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. A receive last slot interrupt generates a MCASP receive interrupt (RINT). |
| 3 | RDMAERR | R/W | 0h | Receive DMA error interrupt enable bit. 0h = Interrupt is disabled. A receive DMA error interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. A receive DMA error interrupt generates a MCASP receive interrupt (RINT). |

Table 6-48. MCASP_EVTCTLR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 2 | RCKFAIL | R/W | 0h | Receive clock failure interrupt enable bit. 0h = Interrupt is disabled. A receive clock failure interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. A receive clock failure interrupt generates a MCASP receive interrupt (RINT). |
| 1 | RSYNCERR | R/W | 0h | Unexpected receive frame sync interrupt enable bit. 0h = Interrupt is disabled. An unexpected receive frame sync interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. An unexpected receive frame sync interrupt generates a MCASP receive interrupt (RINT). |
| 0 | ROVRN | R/W | 0h | Receiver overrun interrupt enable bit. 0h = Interrupt is disabled. A receiver overrun interrupt does not generate a MCASP receive interrupt (RINT). 1h = Interrupt is enabled. A receiver overrun interrupt generates a MCASP receive interrupt (RINT). |

6.25 MCASP_RXSTAT Register (Offset = 80h) [reset = 0h]

MCASP_RXSTAT is shown in [Figure 6-24](#) and described in [Table 6-50](#).

Return to [Summary Table](#).

Table 6-49. MCASP_RXSTAT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0080h |
| MCASP1_CFG | 02B1 0080h |
| MCASP2_CFG | 02B2 0080h |

Figure 6-24. MCASP_RXSTAT Register

| | | | | | | | |
|----------|---------|--------|--------|----------|---------|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | RERR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RDMAERR | RSTAFRM | RDATA | RLAST | RTDMSLOT | RCKFAIL | RSYNCERR | ROVRN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-50. MCASP_RXSTAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-9 | RESERVED | R/W | 0h | Reserved |
| 8 | RERR | R/W | 0h | RERR bit always returns a logic-OR of: ROVRN OR RSYNCERR OR RCKFAIL OR RDMAERR. Allows a single bit to be checked to determine if a receiver error interrupt has occurred. 0h = No errors have occurred. 1h = An error has occurred. |
| 7 | RDMAERR | R/W | 0h | Receive DMA error flag. RDMAERR is set when the CPU or DMA reads more serializers through the data port in a given time slot than were programmed as receivers. Causes a receive interrupt [RINT], if this bit is set and RDMAERR in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = Receive DMA error did not occur. 1h = Receive DMA error did occur. |
| 6 | RSTAFRM | R/W | 0h | Receive start of frame flag. Causes a receive interrupt [RINT], if this bit is set and RSTAFRM in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = No new receive frame sync (AFSR) is detected. 1h = A new receive frame sync (AFSR) is detected. |

Table 6-50. MCASP_RXSTAT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 5 | RDATA | R/W | 0h | Receive data ready flag. Causes a receive interrupt [RINT], if this bit is set and RDATA in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = No new data in RBUF. 1h = Data is transferred from XRSR to RBUF and ready to be serviced by the CPU or DMA. When RDATA is set, it always causes a DMA event (AREVT). |
| 4 | RLAST | R/W | 0h | Receive last slot flag. RLAST is set along with RDATA, if the current slot is the last slot in a frame. Causes a receive interrupt [RINT], if this bit is set and RLAST in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = Current slot is not the last slot in a frame. 1h = Current slot is the last slot in a frame. RDATA is also set. |
| 3 | RTDMSLOT | R/W | 0h | Returns the LSB of MCASP_RSLOT. Allows a single read of MCASP_RSTAT to determine whether the current TDM time slot is even or odd. 0h = Current TDM time slot is odd. 1h = Current TDM time slot is even. |
| 2 | RCKFAIL | R/W | 0h | Receive clock failure flag. RCKFAIL is set when the receive clock failure detection circuit reports an error. Causes a receive interrupt [RINT], if this bit is set and RCKFAIL in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = Receive clock failure did not occur. 1h = Receive clock failure did occur. |
| 1 | RSYNCERR | R/W | 0h | Unexpected receive frame sync flag. RSYNCERR is set when a new receive frame sync [AFSR] occurs before it is expected. Causes a receive interrupt [RINT], if this bit is set and RSYNCERR in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = Unexpected receive frame sync did not occur. 1h = Unexpected receive frame sync did occur. |
| 0 | ROVRN | R/W | 0h | Receiver overrun flag. ROVRN is set when the receive serializer is instructed to transfer data from XRSR to RBUF, but the former data in RBUF has not yet been read by the CPU or DMA. Causes a receive interrupt [RINT], if this bit is set and ROVRN in MCASP_RINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 to this bit has no effect. 0h = Receiver overrun did not occur. 1h = Receiver overrun did occur. |

6.26 MCASP_RXTDMSLOT Register (Offset = 84h) [reset = 0h]

MCASP_RXTDMSLOT is shown in [Figure 6-25](#) and described in [Table 6-52](#).

Return to [Summary Table](#).

Table 6-51. MCASP_RXTDMSLOT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0084h |
| MCASP1_CFG | 02B1 0084h |
| MCASP2_CFG | 02B2 0084h |

Figure 6-25. MCASP_RXTDMSLOT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | RSLOTCNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 6-52. MCASP_RXTDMSLOT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved |
| 9-0 | RSLOTCNT | R | 0h | 0-17Fh = Current receive time slot count. Legal values: 0 to 383 [17Fh]. TDM function is not supported for > 32 time slots. However, TDM time slot counter may count to 383 when used to receive a DIR block [transferred over TDM format]. |

6.27 MCASP_RXCLKCHK Register (Offset = 88h) [reset = 0h]

MCASP_RXCLKCHK is shown in [Figure 6-26](#) and described in [Table 6-54](#).

Return to [Summary Table](#).

Table 6-53. MCASP_RXCLKCHK Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0088h |
| MCASP1_CFG | 02B1 0088h |
| MCASP2_CFG | 02B2 0088h |

Figure 6-26. MCASP_RXCLKCHK Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----------|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RCNT | | | | | | | | RMAX | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RMIN | | | | | | | | RESERVED | | | | RPS | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-54. MCASP_RXCLKCHK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-24 | RCNT | R | 0h | Receive clock count value [from previous measurement]. The clock circuit continually counts the number of system clocks for every 32 receive high-frequency master clock [AHCLKR] signals, and stores the count in RCNT until the next measurement is taken. |
| 23-16 | RMAX | R/W | 0h | Receive clock maximum boundary. This 8 bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 receive high-frequency master clock [AHCLKR] signals have been received. If the current counter value is greater than RMAX after counting 32 AHCLKR signals, RCKFAIL in MCASP_RSTAT is set. The comparison is performed using unsigned arithmetic. |
| 15-8 | RMIN | R/W | 0h | Receive clock minimum boundary. This 8 bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 receive high-frequency master clock [AHCLKR] signals have been received. If RCNT is less than RMIN after counting 32 AHCLKR signals, RCKFAIL in MCASP_RSTAT is set. The comparison is performed using unsigned arithmetic. |
| 7-4 | RESERVED | R/W | 0h | Reserved |
| 3-0 | RPS | R/W | 0h | Receive clock check prescaler value. 0h = MCASP system clock divided by 1. 1h = MCASP system clock divided by 2. 2h = MCASP system clock divided by 4. 3h = MCASP system clock divided by 8. 4h = MCASP system clock divided by 16. 5h = MCASP system clock divided by 32. 6h = MCASP system clock divided by 64. 7h = MCASP system clock divided by 128. 8h = MCASP system clock divided by 256. 9h = Reserved from 9h to Fh. |

6.28 MCASP_REVTCTL Register (Offset = 8Ch) [reset = 0h]

MCASP_REVTCTL is shown in [Figure 6-27](#) and described in [Table 6-56](#).

Return to [Summary Table](#).

Table 6-55. MCASP_REVTCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 008Ch |
| MCASP1_CFG | 02B1 008Ch |
| MCASP2_CFG | 02B2 008Ch |

Figure 6-27. MCASP_REVTCTL Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | RDATDMA |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-56. MCASP_REVTCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | 0h | Reserved |
| 0 | RDATDMA | R/W | 0h | Receive data DMA request enable bit. If writing to this bit, always write the default value of 0. 0h = Receive data DMA request is enabled. 1h = Reserved |

6.29 MCASP_GBLCTLX Register (Offset = A0h) [reset = 0h]

MCASP_GBLCTLX is shown in [Figure 6-28](#) and described in [Table 6-58](#).

Return to [Summary Table](#).

Table 6-57. MCASP_GBLCTLX Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00A0h |
| MCASP1_CFG | 02B1 00A0h |
| MCASP2_CFG | 02B2 00A0h |

Figure 6-28. MCASP_GBLCTLX Register

| | | | | | | | |
|----------|----|----|--------|--------|---------|----------|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | XFRST | XSMRST | XSRCLR | XHCLKRST | XCLKRST |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RFRST | RSMRST | RSRCLKR | RHCLKRST | RCLKRST |
| R/W-0h | | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-58. MCASP_GBLCTLX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-13 | RESERVED | R/W | 0h | Reserved |
| 12 | XFRST | R/W | 0h | Transmit frame sync generator reset enable bit. A write to this bit affects the XFRST bit of MCASP_GBLCTL. 0h = Transmit frame sync generator is reset. 1h = Transmit frame sync generator is active. |
| 11 | XSMRST | R/W | 0h | Transmit state machine reset enable bit. A write to this bit affects the XSMRST bit of MCASP_GBLCTL. 0h = Transmit state machine is held in reset. 1h = Transmit state machine is released from reset. |
| 10 | XSRCLR | R/W | 0h | Transmit serializer clear enable bit. A write to this bit affects the XSRCLR bit of MCASP_GBLCTL. 0h = Transmit serializers are cleared. 1h = Transmit serializers are active. |
| 9 | XHCLKRST | R/W | 0h | Transmit high-frequency clock divider reset enable bit. A write to this bit affects the XHCLKRST bit of MCASP_GBLCTL. 0h = Transmit high-frequency clock divider is held in reset. 1h = Transmit high-frequency clock divider is running. |
| 8 | XCLKRST | R/W | 0h | Transmit clock divider reset enable bit. A write to this bit affects the XCLKRST bit of MCASP_GBLCTL. 0h = Transmit clock divider is held in reset. 1h = Transmit clock divider is running. |
| 7-5 | RESERVED | R/W | 0h | Reserved |
| 4 | RFRST | R | 0h | Receive frame sync generator reset enable bit. A read of this bit returns the RFRST bit value of MCASP_GBLCTL. Writes have no effect. |

Table 6-58. MCASP_GBLCTLX Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 3 | RSMRST | R | 0h | Receive state machine reset enable bit. A read of this bit returns the RSMRST bit value of MCASP_GBLCTL. Writes have no effect. |
| 2 | RSRCLKR | R | 0h | Receive serializer clear enable bit. A read of this bit returns the RSRCLKR bit value of MCASP_GBLCTL. Writes have no effect. |
| 1 | RHCLKRST | R | 0h | Receive high-frequency clock divider reset enable bit. A read of this bit returns the RHCLKRST bit value of MCASP_GBLCTL. Writes have no effect. |
| 0 | RCLKRST | R | 0h | Receive clock divider reset enable bit. A read of this bit returns the RCLKRST bit value of MCASP_GBLCTL. Writes have no effect. |

6.30 MCASP_TXMASK Register (Offset = A4h) [reset = 0h]

MCASP_TXMASK is shown in [Figure 6-29](#) and described in [Table 6-60](#).

Return to [Summary Table](#).

Table 6-59. MCASP_TXMASK Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00A4h |
| MCASP1_CFG | 02B1 00A4h |
| MCASP2_CFG | 02B2 00A4h |

Figure 6-29. MCASP_TXMASK Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| XMASK31 | XMASK30 | XMASK29 | XMASK28 | XMASK27 | XMASK26 | XMASK25 | XMASK24 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XMASK23 | XMASK22 | XMASK21 | XMASK20 | XMASK19 | XMASK18 | XMASK17 | XMASK16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XMASK15 | XMASK14 | XMASK13 | XMASK12 | XMASK11 | XMASK10 | XMASK9 | XMASK8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XMASK7 | XMASK6 | XMASK5 | XMASK4 | XMASK3 | XMASK2 | XMASK1 | XMASK0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-60. MCASP_TXMASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 31 | XMASK31 | R/W | 0h | Transmit data mask 31 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 30 | XMASK30 | R/W | 0h | Transmit data mask 30 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 29 | XMASK29 | R/W | 0h | Transmit data mask 29 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |

Table 6-60. MCASP_TXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 28 | XMASK28 | R/W | 0h | Transmit data mask 28 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 27 | XMASK27 | R/W | 0h | Transmit data mask 27 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 26 | XMASK26 | R/W | 0h | Transmit data mask 26 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 25 | XMASK25 | R/W | 0h | Transmit data mask 25 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 24 | XMASK24 | R/W | 0h | Transmit data mask 24 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 23 | XMASK23 | R/W | 0h | Transmit data mask 23 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 22 | XMASK22 | R/W | 0h | Transmit data mask 22 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |

Table 6-60. MCASP_TXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 21 | XMASK21 | R/W | 0h | Transmit data mask 21 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 20 | XMASK20 | R/W | 0h | Transmit data mask 20 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 19 | XMASK19 | R/W | 0h | Transmit data mask 19 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 18 | XMASK18 | R/W | 0h | Transmit data mask 18 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 17 | XMASK17 | R/W | 0h | Transmit data mask 17 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 16 | XMASK16 | R/W | 0h | Transmit data mask 16 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 15 | XMASK15 | R/W | 0h | Transmit data mask 15 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |

Table 6-60. MCASP_TXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 14 | XMASK14 | R/W | 0h | Transmit data mask 14 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 13 | XMASK13 | R/W | 0h | Transmit data mask 13 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 12 | XMASK12 | R/W | 0h | Transmit data mask 12 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 11 | XMASK11 | R/W | 0h | Transmit data mask 11 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 10 | XMASK10 | R/W | 0h | Transmit data mask 10 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 9 | XMASK9 | R/W | 0h | Transmit data mask 9 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 8 | XMASK8 | R/W | 0h | Transmit data mask 8 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |

Table 6-60. MCASP_TXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 7 | XMASK7 | R/W | 0h | Transmit data mask 7 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 6 | XMASK6 | R/W | 0h | Transmit data mask 6 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 5 | XMASK5 | R/W | 0h | Transmit data mask 5 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 4 | XMASK4 | R/W | 0h | Transmit data mask 4 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 3 | XMASK3 | R/W | 0h | Transmit data mask 3 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 2 | XMASK2 | R/W | 0h | Transmit data mask 2 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |
| 1 | XMASK1 | R/W | 0h | Transmit data mask 1 enable bit. 0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit. 1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP. |

Table 6-60. MCASP_TXMASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 0 | XMASK0 | R/W | 0h | <p>Transmit data mask 0 enable bit.</p> <p>0h = Corresponding bit of transmit data (before passing through reverse and rotate units) is masked out and then padded with the selected bit pad value (XPAD and XPBIT bits in MCASP_XFMT), which is transmitted out the McASP in place of the original bit.</p> <p>1h = Corresponding bit of transmit data (before passing through reverse and rotate units) is transmitted out the McASP.</p> |

6.31 MCASP_TXFMT Register (Offset = A8h) [reset = 0h]

MCASP_TXFMT is shown in [Figure 6-30](#) and described in [Table 6-62](#).

Return to [Summary Table](#).

Table 6-61. MCASP_TXFMT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00A8h |
| MCASP1_CFG | 02B1 00A8h |
| MCASP2_CFG | 02B2 00A8h |

Figure 6-30. MCASP_TXFMT Register

| | | | | | | | |
|----------|------|--------|--------|--------|--------|---------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | XDATDLY | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XRVS | XPAD | | XPBIT | | | | |
| R/W-0h | | R/W-0h | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XSSZ | | | | XBUSEL | XROT | | |
| R/W-0h | | | R/W-0h | | R/W-0h | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-62. MCASP_TXFMT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-18 | RESERVED | R/W | 0h | Reserved |
| 17-16 | XDATDLY | R/W | 0h | Transmit sync bit delay. 0h = 0-bit delay. The first transmit data bit, AXRn, occurs in same ACLKX cycle as the transmit frame sync (AFSX). 1h = 1-bit delay. The first transmit data bit, AXRn, occurs one ACLKX cycle after the transmit frame sync (AFSX). 2h = 2-bit delay. The first transmit data bit, AXRn, occurs two ACLKX cycles after the transmit frame sync (AFSX). 3h = Reserved. |
| 15 | XRVRS | R/W | 0h | Transmit serial bitstream order. 0h = Bitstream is LSB first. No bit reversal is performed in transmit format bit reverse unit. 1h = Bitstream is MSB first. Bit reversal is performed in transmit format bit reverse unit. |
| 14-13 | XPAD | R/W | 0h | Pad value for extra bits in slot not belonging to word defined by MCASP_XMASK. This field only applies to bits when MCASP_XMASK[n] = 0. 0h = Pad extra bits with 0. 1h = Pad extra bits with 1. 2h = Pad extra bits with one of the bits from the word as specified by XPBIT bits. 3h = Reserved. |

Table 6-62. MCASP_TXFMT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|--|
| 12-8 | XPBIT | R/W | 0h | XPBIT value determines which bit [as written by the CPU or DMA to XBUF[n]] is used to pad the extra bits before shifting. This field only applies when XPAD = 2h. 0h = Pad with bit 0 value. 1h = Pad with bit 1 to bit 31 value from 1h to 1Fh. |
| 7-4 | XSSZ | R/W | 0h | Transmit slot size. 0h = Reserved. 1h = Reserved. 2h = Reserved. 3h = Slot size is 8 bits. 4h = Reserved. 5h = Slot size is 12 bits. 6h = Reserved. 7h = Slot size is 16 bits. 8h = Reserved. 9h = Slot size is 20 bits. Ah = Reserved. Bh = Slot size is 24 bits. Ch = Reserved. Dh = Slot size is 28 bits. Eh = Reserved. Fh = Slot size is 32 bits. |
| 3 | XBUSEL | R/W | 0h | Selects whether writes to serializer buffer XRBUFF[n] originate from the configuration bus [CFG] or the data [DAT] port. 0h = Writes to XRBUFF[n] originate from the data port. Writes to XRBUFF[n] from the configuration bus are ignored with no effect to the McASP. 1h = Writes to XRBUFF[n] originate from the configuration bus. Writes to XRBUFF[n] from the data port are ignored with no effect to the McASP. |
| 2-0 | XROT | R/W | 0h | Right-rotation value for transmit rotate right format unit. 0h = Rotate right by 0 (no rotation). 1h = Rotate right by 4 bit positions. 2h = Rotate right by 8 bit positions. 3h = Rotate right by 12 bit positions. 4h = Rotate right by 16 bit positions. 5h = Rotate right by 20 bit positions. 6h = Rotate right by 24 bit positions. 7h = Rotate right by 28 bit positions. |

6.32 MCASP_TXFMCTL Register (Offset = ACh) [reset = 0h]

MCASP_TXFMCTL is shown in [Figure 6-31](#) and described in [Table 6-64](#).

Return to [Summary Table](#).

Table 6-63. MCASP_TXFMCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00ACh |
| MCASP1_CFG | 02B1 00ACh |
| MCASP2_CFG | 02B2 00ACh |

Figure 6-31. MCASP_TXFMCTL Register

| | | | | | | | |
|----------|----------|----|--------|----------|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XMOD | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XMOD | RESERVED | | FXWID | RESERVED | | FSXM | FSXP |
| R/W-0h | R/W-0h | | R/W-0h | R/W-0h | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-64. MCASP_TXFMCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | 0h | Reserved |
| 15-7 | XMOD | R/W | 0h | Transmit frame sync mode select bits. 1FFh = Reserved from 181h to 1FFh. 0h = Burst mode. 1h = Reserved. 2h = 2-slot TDM (I2S mode) to 32-slot TDM from 2h to 20h. 21h = Reserved from 21h to 17Fh. 180h = 384-slot DIT mode. 181h = Reserved from 181h to 1FFh. |
| 6-5 | RESERVED | R/W | 0h | Reserved |
| 4 | FXWID | R/W | 0h | Transmit frame sync width select bit indicates the width of the transmit frame sync [AFSX] during its active period. 0h = Single bit. 1h = Single word. |
| 3-2 | RESERVED | R/W | 0h | Reserved |
| 1 | FSXM | R/W | 0h | Transmit frame sync generation select bit. 0h = Externally-generated transmit frame sync. 1h = Internally-generated transmit frame sync. |
| 0 | FSXP | R/W | 0h | Transmit frame sync polarity select bit. 0h = A rising edge on transmit frame sync (AFSX) indicates the beginning of a frame. 1h = A falling edge on transmit frame sync (AFSX) indicates the beginning of a frame. |

6.33 MCASP_ACLKXCTL Register (Offset = B0h) [reset = 0h]

MCASP_ACLKXCTL is shown in [Figure 6-32](#) and described in [Table 6-66](#).

Return to [Summary Table](#).

Table 6-65. MCASP_ACLKXCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00B0h |
| MCASP1_CFG | 02B1 00B0h |
| MCASP2_CFG | 02B2 00B0h |

Figure 6-32. MCASP_ACLKXCTL Register

| | | | | | | | |
|----------|--------|--------|---------|---------|---------|---------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | BUSY | DIVBUSY | ADJBUSY | CLKXADJ | |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLKXP | ASYN | CLKXM | CLKXDIV | | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | | |

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 6-66. MCASP_ACLKXCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-21 | RESERVED | R/W | 0h | Reserved |
| 20 | BUSY | R/W | 0h | The logic OR of bits 18 and 19, indicating that some clk change is in progress when high |
| 19 | DIVBUSY | R/W | 0h | Divider change in progress (same behavior as bit 18) |
| 18 | ADJBUSY | R/W | 0h | one-shot adj in progress (a BUSY bit that is set when an adj is in progress, cleared when the adjustment has taken effect) |
| 17-16 | CLKXADJ | W | 0h | CLKXDIV one-shot adjustment control. If CLKXDIV is set such that there are "m" input clocks per one output clock, then for one output cycle: 0h = (m+0) input clocks per output clock 1h = (m-1) input clocks per output clock 2h = (m+1) input clocks per output clock 3h = (m+0) input clocks per output clock |
| 15-8 | RESERVED | R/W | 0h | Reserved |
| 7 | CLKXP | R/W | 0h | Transmit bitstream clock polarity select bit. 0h = Rising edge. External receiver samples data on the falling edge of the serial clock, so the transmitter must shift data out on the rising edge of the serial clock. 1h = Falling edge. External receiver samples data on the rising edge of the serial clock, so the transmitter must shift data out on the falling edge of the serial clock. |

Table 6-66. MCASP_ACLKXCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 6 | ASYNC | R/W | 0h | Transmit/receive operation asynchronous enable bit. 0h = Synchronous. Transmit clock and frame sync provides the source for both the transmit and receive sections. 1h = Asynchronous. Separate clock and frame sync used by transmit and receive sections. |
| 5 | CLKXM | R/W | 0h | Transmit bit clock source bit. 0h = External transmit clock source from ACLKX pin. 1h = Internal transmit clock source from output of programmable bit clock divider. |
| 4-0 | CLKXDIV | R/W | 0h | Transmit bit clock divide ratio bits determine the divide-down ratio from AHCLKX to ACLKX. 0h = Divide-by-1. 1h = Divide-by-2. 2h = Divide-by-3 to divide-by-32 from 2h to 1Fh. |

6.34 MCASP_AHCLKXCTL Register (Offset = B4h) [reset = 0h]

MCASP_AHCLKXCTL is shown in [Figure 6-33](#) and described in [Table 6-68](#).

Return to [Summary Table](#).

Table 6-67. MCASP_AHCLKXCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00B4h |
| MCASP1_CFG | 02B1 00B4h |
| MCASP2_CFG | 02B2 00B4h |

Figure 6-33. MCASP_AHCLKXCTL Register

| | | | | | | | |
|----------|--------|----------|--------|----------|---------|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | BUSY | DIVBUSY | ADJBUSY | HCLKXADJ | |
| R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| HCLKXM | HCLKXP | RESERVED | | HCLKXDIV | | | |
| R/W-0h | R/W-0h | R/W-0h | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HCLKXDIV | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; W = Write Only; -n = value after reset

Table 6-68. MCASP_AHCLKXCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-21 | RESERVED | R/W | 0h | Reserved |
| 20 | BUSY | R/W | 0h | The logic OR of bits 18 and 19, indicating that some clk change is in progress when high |
| 19 | DIVBUSY | R/W | 0h | Divider change in progress (same behavior as bit 18) |
| 18 | ADJBUSY | R/W | 0h | one-shot adj in progress (a BUSY bit that is set when an adj is in progress, cleared when the adjustment has taken effect) |
| 17-16 | HCLKXADJ | W | 0h | CLKXDIV one-shot adjustment control. If CLKXDIV is set such that there are "m" input clocks per one output clock, then for one output cycle: 0h = (m+0) input clocks per output clock 1h = (m-1) input clocks per output clock 2h = (m+1) input clocks per output clock 3h = (m+0) input clocks per output clock |
| 15 | HCLKXM | R/W | 0h | Transmit high-frequency clock source bit. 0h = External transmit high-frequency clock source from AHCLKX pin. 1h = Internal transmit high-frequency clock source from output of programmable high clock divider. |

Table 6-68. MCASP_AHCLKXCTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 14 | HCLKXP | R/W | 0h | Transmit bitstream high-frequency clock polarity select bit. 0h = AHCLKX is not inverted before programmable bit clock divider. In the special case where the transmit bit clock (ACLKX) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKXDIV = 0 in MCASP_ACLKXCTL), AHCLKX is directly passed through to the ACLKX pin. 1h = AHCLKX is inverted before programmable bit clock divider. In the special case where the transmit bit clock (ACLKX) is internally generated and the programmable bit clock divider is set to divide-by-1 (CLKXDIV = 0 in MCASP_ACLKXCTL), AHCLKX is directly passed through to the ACLKX pin. |
| 13-12 | RESERVED | R/W | 0h | Reserved |
| 11-0 | HCLKXDIV | R/W | 0h | Transmit high-frequency clock divide ratio bits determine the divide-down ratio from AUXCLK to AHCLKX. 0h = Divide-by-1. 1h = Divide-by-2. 2h = Divide-by-3 to divide-by-4096 from 2h to FFFh. |

6.35 MCASP_TXTDM Register (Offset = B8h) [reset = 0h]

MCASP_TXTDM is shown in [Figure 6-34](#) and described in [Table 6-70](#).

Return to [Summary Table](#).

Table 6-69. MCASP_TXTDM Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00B8h |
| MCASP1_CFG | 02B1 00B8h |
| MCASP2_CFG | 02B2 00B8h |

Figure 6-34. MCASP_TXTDM Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| XTDMS31 | XTDMS30 | XTDMS29 | XTDMS28 | XTDMS27 | XTDMS26 | XTDMS25 | XTDMS24 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XTDMS23 | XTDMS22 | XTDMS21 | XTDMS20 | XTDMS19 | XTDMS18 | XTDMS17 | XTDMS16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XTDMS15 | XTDMS14 | XTDMS13 | XTDMS12 | XTDMS11 | XTDMS10 | XTDMS9 | XTDMS8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XTDMS7 | XTDMS6 | XTDMS5 | XTDMS4 | XTDMS3 | XTDMS2 | XTDMS1 | XTDMS0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-70. MCASP_TXTDM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 31 | XTDMS31 | R/W | 0h | Transmitter mode during TDM time slot 31. 0h = Transmit TDM time slot 31 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 31 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 30 | XTDMS30 | R/W | 0h | Transmitter mode during TDM time slot 30. 0h = Transmit TDM time slot 30 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 30 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 29 | XTDMS29 | R/W | 0h | Transmitter mode during TDM time slot 29. 0h = Transmit TDM time slot 29 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 29 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 28 | XTDMS28 | R/W | 0h | Transmitter mode during TDM time slot 28. 0h = Transmit TDM time slot 28 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 28 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |

Table 6-70. MCASP_TXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 27 | XTDMS27 | R/W | 0h | Transmitter mode during TDM time slot 27. 0h = Transmit TDM time slot 27 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 27 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 26 | XTDMS26 | R/W | 0h | Transmitter mode during TDM time slot 26. 0h = Transmit TDM time slot 26 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 26 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 25 | XTDMS25 | R/W | 0h | Transmitter mode during TDM time slot 25. 0h = Transmit TDM time slot 25 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 25 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 24 | XTDMS24 | R/W | 0h | Transmitter mode during TDM time slot 24. 0h = Transmit TDM time slot 24 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 24 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 23 | XTDMS23 | R/W | 0h | Transmitter mode during TDM time slot 23. 0h = Transmit TDM time slot 23 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 23 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 22 | XTDMS22 | R/W | 0h | Transmitter mode during TDM time slot 22. 0h = Transmit TDM time slot 22 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 22 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 21 | XTDMS21 | R/W | 0h | Transmitter mode during TDM time slot 21. 0h = Transmit TDM time slot 21 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 21 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 20 | XTDMS20 | R/W | 0h | Transmitter mode during TDM time slot 20. 0h = Transmit TDM time slot 20 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 20 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |

Table 6-70. MCASP_TXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 19 | XTDMS19 | R/W | 0h | Transmitter mode during TDM time slot 19. 0h = Transmit TDM time slot 19 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 19 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 18 | XTDMS18 | R/W | 0h | Transmitter mode during TDM time slot 18. 0h = Transmit TDM time slot 18 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 18 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 17 | XTDMS17 | R/W | 0h | Transmitter mode during TDM time slot 17. 0h = Transmit TDM time slot 17 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 17 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 16 | XTDMS16 | R/W | 0h | Transmitter mode during TDM time slot 16. 0h = Transmit TDM time slot 16 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 16 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 15 | XTDMS15 | R/W | 0h | Transmitter mode during TDM time slot 15. 0h = Transmit TDM time slot 15 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 15 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 14 | XTDMS14 | R/W | 0h | Transmitter mode during TDM time slot 14. 0h = Transmit TDM time slot 14 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 14 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 13 | XTDMS13 | R/W | 0h | Transmitter mode during TDM time slot 13. 0h = Transmit TDM time slot 13 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 13 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 12 | XTDMS12 | R/W | 0h | Transmitter mode during TDM time slot 12. 0h = Transmit TDM time slot 12 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 12 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |

Table 6-70. MCASP_TXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 11 | XTDMS11 | R/W | 0h | Transmitter mode during TDM time slot 11. 0h = Transmit TDM time slot 11 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 11 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 10 | XTDMS10 | R/W | 0h | Transmitter mode during TDM time slot 10. 0h = Transmit TDM time slot 10 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 10 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 9 | XTDMS9 | R/W | 0h | Transmitter mode during TDM time slot 9. 0h = Transmit TDM time slot 9 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 9 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 8 | XTDMS8 | R/W | 0h | Transmitter mode during TDM time slot 8. 0h = Transmit TDM time slot 8 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 8 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 7 | XTDMS7 | R/W | 0h | Transmitter mode during TDM time slot 7. 0h = Transmit TDM time slot 7 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 7 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 6 | XTDMS6 | R/W | 0h | Transmitter mode during TDM time slot 6. 0h = Transmit TDM time slot 6 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 6 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 5 | XTDMS5 | R/W | 0h | Transmitter mode during TDM time slot 5. 0h = Transmit TDM time slot 5 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 5 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 4 | XTDMS4 | R/W | 0h | Transmitter mode during TDM time slot 4. 0h = Transmit TDM time slot 4 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 4 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |

Table 6-70. MCASP_TXTDM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 3 | XTDMS3 | R/W | 0h | Transmitter mode during TDM time slot 3. 0h = Transmit TDM time slot 3 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 3 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 2 | XTDMS2 | R/W | 0h | Transmitter mode during TDM time slot 2. 0h = Transmit TDM time slot 2 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 2 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 1 | XTDMS1 | R/W | 0h | Transmitter mode during TDM time slot 1. 0h = Transmit TDM time slot 1 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 1 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |
| 0 | XTDMS0 | R/W | 0h | Transmitter mode during TDM time slot 0. 0h = Transmit TDM time slot 0 is inactive. The transmit serializer does not shift out data during this slot. 1h = Transmit TDM time slot 0 is active. The transmit serializer shifts out data during this slot according to the serializer control register (SRCTL). |

6.36 MCASP_EVTCTLX Register (Offset = BCh) [reset = 0h]

MCASP_EVTCTLX is shown in [Figure 6-35](#) and described in [Table 6-72](#).

Return to [Summary Table](#).

Table 6-71. MCASP_EVTCTLX Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00BCh |
| MCASP1_CFG | 02B1 00BCh |
| MCASP2_CFG | 02B2 00BCh |

Figure 6-35. MCASP_EVTCTLX Register

| | | | | | | | |
|----------|----------|--------|--------|---------|---------|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XSTAFRM | RESERVED | XDATA | XLAST | XDMAERR | XCKFAIL | XSYNCERR | XUNDRN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-72. MCASP_EVTCTLX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-8 | RESERVED | R/W | 0h | Reserved |
| 7 | XSTAFRM | R/W | 0h | Transmit start of frame interrupt enable bit. 0h = Interrupt is disabled. A transmit start of frame interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. A transmit start of frame interrupt generates a McASP transmit interrupt (XINT). |
| 6 | RESERVED | R/W | 0h | Reserved |
| 5 | XDATA | R/W | 0h | Transmit data ready interrupt enable bit. 0h = Interrupt is disabled. A transmit data ready interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. A transmit data ready interrupt generates a McASP transmit interrupt (XINT). |
| 4 | XLAST | R/W | 0h | Transmit last slot interrupt enable bit. 0h = Interrupt is disabled. A transmit last slot interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. A transmit last slot interrupt generates a McASP transmit interrupt (XINT). |
| 3 | XDMAERR | R/W | 0h | Transmit DMA error interrupt enable bit. 0h = Interrupt is disabled. A transmit DMA error interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. A transmit DMA error interrupt generates a McASP transmit interrupt (XINT). |

Table 6-72. MCASP_EVTCTLX Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 2 | XCKFAIL | R/W | 0h | Transmit clock failure interrupt enable bit. 0h = Interrupt is disabled. A transmit clock failure interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. A transmit clock failure interrupt generates a McASP transmit interrupt (XINT). |
| 1 | XSYNCERR | R/W | 0h | Unexpected transmit frame sync interrupt enable bit. 0h = Interrupt is disabled. An unexpected transmit frame sync interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. An unexpected transmit frame sync interrupt generates a McASP transmit interrupt (XINT). |
| 0 | XUNDRN | R/W | 0h | Transmitter underrun interrupt enable bit. 0h = Interrupt is disabled. A transmitter underrun interrupt does not generate a McASP transmit interrupt (XINT). 1h = Interrupt is enabled. A transmitter underrun interrupt generates a McASP transmit interrupt (XINT). |

6.37 MCASP_TXSTAT Register (Offset = C0h) [reset = 0h]

MCASP_TXSTAT is shown in [Figure 6-36](#) and described in [Table 6-74](#).

Return to [Summary Table](#).

Table 6-73. MCASP_TXSTAT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00C0h |
| MCASP1_CFG | 02B1 00C0h |
| MCASP2_CFG | 02B2 00C0h |

Figure 6-36. MCASP_TXSTAT Register

| | | | | | | | |
|----------|---------|--------|--------|----------|---------|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | XERR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XDMAERR | XSTAFRM | XDATA | XLAST | XTDMSLOT | XCKFAIL | XSYNCERR | XUNDRN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-74. MCASP_TXSTAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-9 | RESERVED | R/W | 0h | Reserved |
| 8 | XERR | R/W | 0h | XERR bit always returns a logic-OR of: XUNDRN OR XSYNCERR OR XCKFAIL OR XDMAERR. Allows a single bit to be checked to determine if a transmitter error interrupt has occurred. 0h = No errors have occurred. 1h = An error has occurred. |
| 7 | XDMAERR | R/W | 0h | Transmit DMA error flag. XDMAERR is set when the CPU or DMA writes more serializers through the data port in a given time slot than were programmed as transmitters. Causes a transmit interrupt [XINT], if this bit is set and XDMAERR in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = Transmit DMA error did not occur. 1h = Transmit DMA error did occur. |
| 6 | XSTAFRM | R/W | 0h | Transmit start of frame flag. Causes a transmit interrupt [XINT], if this bit is set and XSTAFRM in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = No new transmit frame sync (AFSX) is detected. 1h = A new transmit frame sync (AFSX) is detected. |

Table 6-74. MCASP_TXSTAT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 5 | XDATA | R/W | 0h | Transmit data ready flag. Causes a transmit interrupt [XINT], if this bit is set and XDATA in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = XBUF is written and is full. 1h = Data is copied from XBUF to XRSR. XBUF is empty and ready to be written. XDATA is also set when the transmit serializers are taken out of reset. When XDATA is set, it always causes a DMA event (AXEVT). |
| 4 | XLAST | R/W | 0h | Transmit last slot flag. XLAST is set along with XDATA, if the current slot is the last slot in a frame. Causes a transmit interrupt [XINT], if this bit is set and XLAST in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = Current slot is not the last slot in a frame. 1h = Current slot is the last slot in a frame. XDATA is also set. |
| 3 | XTDMSLOT | R/W | 0h | Returns the LSB of MCASP_XSLOT. Allows a single read of MCASP_XSTAT to determine whether the current TDM time slot is even or odd. 0h = Current TDM time slot is odd. 1h = Current TDM time slot is even. |
| 2 | XCKFAIL | R/W | 0h | Transmit clock failure flag. XCKFAIL is set when the transmit clock failure detection circuit reports an error. Causes a transmit interrupt [XINT], if this bit is set and XCKFAIL in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = Transmit clock failure did not occur. 1h = Transmit clock failure did occur. |
| 1 | XSYNCERR | R/W | 0h | Unexpected transmit frame sync flag. XSYNCERR is set when a new transmit frame sync [AFSX] occurs before it is expected. Causes a transmit interrupt [XINT], if this bit is set and XSYNCERR in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = Unexpected transmit frame sync did not occur. 1h = Unexpected transmit frame sync did occur. |
| 0 | XUNDRN | R/W | 0h | Transmitter underrun flag. XUNDRN is set when the transmit serializer is instructed to transfer data from XBUF to XRSR, but XBUF has not yet been serviced with new data since the last transfer. Causes a transmit interrupt [XINT], if this bit is set and XUNDRN in MCASP_XINTCTL is set. This bit is cleared by writing a 1 to this bit. Writing a 0 has no effect. 0h = Transmitter underrun did not occur. 1h = Transmitter underrun did occur. For details on McASP action upon underrun conditions, see Buffer Underrun Error - Transmitter. |

6.38 MCASP_TXTDMSLOT Register (Offset = C4h) [reset = 0h]

MCASP_TXTDMSLOT is shown in [Figure 6-37](#) and described in [Table 6-76](#).

Return to [Summary Table](#).

Table 6-75. MCASP_TXTDMSLOT Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00C4h |
| MCASP1_CFG | 02B1 00C4h |
| MCASP2_CFG | 02B2 00C4h |

Figure 6-37. MCASP_TXTDMSLOT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | XSLOTCNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 6-76. MCASP_TXTDMSLOT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-10 | RESERVED | R | 0h | Reserved |
| 9-0 | XSLOTCNT | R | 0h | Current transmit time slot count. Legal values: 0 to 383 [17Fh]. During reset, this counter value is 383 so the next count value, which is used to encode the first DIT group of data, will be 0 and encodes the B preamble. TDM function is not supported for >32 time slots. However, TDM time slot counter may count to 383 when used to transmit a DIT block. |

6.39 MCASP_TXCLKCHK Register (Offset = C8h) [reset = 0h]

MCASP_TXCLKCHK is shown in [Figure 6-38](#) and described in [Table 6-78](#).

Return to [Summary Table](#).

Table 6-77. MCASP_TXCLKCHK Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00C8h |
| MCASP1_CFG | 02B1 00C8h |
| MCASP2_CFG | 02B2 00C8h |

Figure 6-38. MCASP_TXCLKCHK Register

| | | | | | | | |
|----------|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCNT | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XMAX | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XMIN | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | XPS | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-78. MCASP_TXCLKCHK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-24 | XCNT | R | 0h | Transmit clock count value [from previous measurement]. The clock circuit continually counts the number of system clocks for every 32 transmit high-frequency master clock [AHCLKX] signals, and stores the count in XCNT until the next measurement is taken. |
| 23-16 | XMAX | R/W | 0h | Transmit clock maximum boundary. This 8 bit unsigned value sets the maximum allowed boundary for the clock check counter after 32 transmit high-frequency master clock [AHCLKX] signals have been received. If the current counter value is greater than XMAX after counting 32 AHCLKX signals, XCKFAIL in MCASP_XSTAT is set. The comparison is performed using unsigned arithmetic. |
| 15-8 | XMIN | R/W | 0h | Transmit clock minimum boundary. This 8 bit unsigned value sets the minimum allowed boundary for the clock check counter after 32 transmit high-frequency master clock [AHCLKX] signals have been received. If XCNT is less than XMIN after counting 32 AHCLKX signals, XCKFAIL in MCASP_XSTAT is set. The comparison is performed using unsigned arithmetic. |
| 7-4 | RESERVED | R | 0h | Reserved |

Table 6-78. MCASP_TXCLKCHK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 3-0 | XPS | R/W | 0h | Transmit clock check prescaler value. Fh = Reserved from 9h to Fh. 0h = MCASP system clock divided by 1. 1h = MCASP system clock divided by 2. 2h = MCASP system clock divided by 4. 3h = MCASP system clock divided by 8. 4h = MCASP system clock divided by 16. 5h = MCASP system clock divided by 32. 6h = MCASP system clock divided by 64. 7h = MCASP system clock divided by 128. 8h = MCASP system clock divided by 256. 9h = Reserved from 9h to Fh. |

6.40 MCASP_XEVTCTL Register (Offset = CCh) [reset = 0h]

MCASP_XEVTCTL is shown in [Figure 6-39](#) and described in [Table 6-80](#).

Return to [Summary Table](#).

Table 6-79. MCASP_XEVTCTL Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00CCh |
| MCASP1_CFG | 02B1 00CCh |
| MCASP2_CFG | 02B2 00CCh |

Figure 6-39. MCASP_XEVTCTL Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | XDATDMA |
| R-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-80. MCASP_XEVTCTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | XDATDMA | R/W | 0h | Transmit data DMA request enable bit. If writing to this bit, always write the default value of 0. 0h = Transmit data DMA request is enabled. 1h = Reserved |

6.41 MCASP_CLKADJEN Register (Offset = D0h) [reset = 0h]

MCASP_CLKADJEN is shown in [Figure 6-40](#) and described in [Table 6-82](#).

Return to [Summary Table](#).

Table 6-81. MCASP_CLKADJEN Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 00D0h |
| MCASP1_CFG | 02B1 00D0h |
| MCASP2_CFG | 02B2 00D0h |

Figure 6-40. MCASP_CLKADJEN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE |
| R-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-82. MCASP_CLKADJEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | ENABLE | R/W | 0h | One-shot clock adjustment enable. 0 = One-shot clock adjustment is DISABLED. Writes to bits 17:16 of MCASP_AHCLKXCTL, MCASP_AHCLKRCTL, MCASP_ACLKXCTL, and MCASP_ACLKRCTL are ineffective. 1 = One-shot clock adjustment is ENABLED. Writes to bits 17:16 of MCASP_AHCLKXCTL, MCASP_AHCLKRCTL, MCASP_ACLKXCTL, and MCASP_ACLKRCTL are allowed. |

6.42 MCASP_DITCSRA0 Register (Offset = 100h) [reset = 0h]

MCASP_DITCSRA0 is shown in [Figure 6-41](#) and described in [Table 6-84](#).

Return to [Summary Table](#).

Table 6-83. MCASP_DITCSRA0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0100h |
| MCASP1_CFG | 02B1 0100h |
| MCASP2_CFG | 02B2 0100h |

Figure 6-41. MCASP_DITCSRA0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRA0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-84. MCASP_DITCSRA0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|------------------------------------|
| 31-0 | DITCSRA0 | R/W | 0h | DIT left channel status registers. |

6.43 MCASP_DITCSRA1 Register (Offset = 104h) [reset = 0h]

MCASP_DITCSRA1 is shown in [Figure 6-42](#) and described in [Table 6-86](#).

Return to [Summary Table](#).

Table 6-85. MCASP_DITCSRA1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0104h |
| MCASP1_CFG | 02B1 0104h |
| MCASP2_CFG | 02B2 0104h |

Figure 6-42. MCASP_DITCSRA1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRA1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-86. MCASP_DITCSRA1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|------------------------------------|
| 31-0 | DITCSRA1 | R/W | 0h | DIT left channel status registers. |

6.44 MCASP_DITCSRA2 Register (Offset = 108h) [reset = 0h]

MCASP_DITCSRA2 is shown in [Figure 6-43](#) and described in [Table 6-88](#).

Return to [Summary Table](#).

Table 6-87. MCASP_DITCSRA2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0108h |
| MCASP1_CFG | 02B1 0108h |
| MCASP2_CFG | 02B2 0108h |

Figure 6-43. MCASP_DITCSRA2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRA2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-88. MCASP_DITCSRA2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|------------------------------------|
| 31-0 | DITCSRA2 | R/W | 0h | DIT left channel status registers. |

6.45 MCASP_DITCSRA3 Register (Offset = 10Ch) [reset = 0h]

MCASP_DITCSRA3 is shown in [Figure 6-44](#) and described in [Table 6-90](#).

Return to [Summary Table](#).

Table 6-89. MCASP_DITCSRA3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 010Ch |
| MCASP1_CFG | 02B1 010Ch |
| MCASP2_CFG | 02B2 010Ch |

Figure 6-44. MCASP_DITCSRA3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRA3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-90. MCASP_DITCSRA3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|------------------------------------|
| 31-0 | DITCSRA3 | R/W | 0h | DIT left channel status registers. |

6.46 MCASP_DITCSRA4 Register (Offset = 110h) [reset = 0h]

MCASP_DITCSRA4 is shown in [Figure 6-45](#) and described in [Table 6-92](#).

Return to [Summary Table](#).

Table 6-91. MCASP_DITCSRA4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0110h |
| MCASP1_CFG | 02B1 0110h |
| MCASP2_CFG | 02B2 0110h |

Figure 6-45. MCASP_DITCSRA4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRA4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-92. MCASP_DITCSRA4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|------------------------------------|
| 31-0 | DITCSRA4 | R/W | 0h | DIT left channel status registers. |

6.47 MCASP_DITCSRA5 Register (Offset = 114h) [reset = 0h]

MCASP_DITCSRA5 is shown in [Figure 6-46](#) and described in [Table 6-94](#).

Return to [Summary Table](#).

Table 6-93. MCASP_DITCSRA5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0114h |
| MCASP1_CFG | 02B1 0114h |
| MCASP2_CFG | 02B2 0114h |

Figure 6-46. MCASP_DITCSRA5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRA5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-94. MCASP_DITCSRA5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|------------------------------------|
| 31-0 | DITCSRA5 | R/W | 0h | DIT left channel status registers. |

6.48 MCASP_DITCSRB0 Register (Offset = 118h) [reset = 0h]

MCASP_DITCSRB0 is shown in [Figure 6-47](#) and described in [Table 6-96](#).

Return to [Summary Table](#).

Table 6-95. MCASP_DITCSRB0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0118h |
| MCASP1_CFG | 02B1 0118h |
| MCASP2_CFG | 02B2 0118h |

Figure 6-47. MCASP_DITCSRB0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRB0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-96. MCASP_DITCSRB0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------------------------------|
| 31-0 | DITCSRB0 | R/W | 0h | DIT right channel status registers. |

6.49 MCASP_DITCSRB1 Register (Offset = 11Ch) [reset = 0h]

MCASP_DITCSRB1 is shown in [Figure 6-48](#) and described in [Table 6-98](#).

Return to [Summary Table](#).

Table 6-97. MCASP_DITCSRB1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 011Ch |
| MCASP1_CFG | 02B1 011Ch |
| MCASP2_CFG | 02B2 011Ch |

Figure 6-48. MCASP_DITCSRB1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRB1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-98. MCASP_DITCSRB1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------------------------------|
| 31-0 | DITCSRB1 | R/W | 0h | DIT right channel status registers. |

6.50 MCASP_DITCSRB2 Register (Offset = 120h) [reset = 0h]

MCASP_DITCSRB2 is shown in [Figure 6-49](#) and described in [Table 6-100](#).

Return to [Summary Table](#).

Table 6-99. MCASP_DITCSRB2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0120h |
| MCASP1_CFG | 02B1 0120h |
| MCASP2_CFG | 02B2 0120h |

Figure 6-49. MCASP_DITCSRB2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRB2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-100. MCASP_DITCSRB2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------------------------------|
| 31-0 | DITCSRB2 | R/W | 0h | DIT right channel status registers. |

6.51 MCASP_DITCSRB3 Register (Offset = 124h) [reset = 0h]

MCASP_DITCSRB3 is shown in [Figure 6-50](#) and described in [Table 6-102](#).

Return to [Summary Table](#).

Table 6-101. MCASP_DITCSRB3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0124h |
| MCASP1_CFG | 02B1 0124h |
| MCASP2_CFG | 02B2 0124h |

Figure 6-50. MCASP_DITCSRB3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRB3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-102. MCASP_DITCSRB3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------------------------------|
| 31-0 | DITCSRB3 | R/W | 0h | DIT right channel status registers. |

6.52 MCASP_DITCSRB4 Register (Offset = 128h) [reset = 0h]

MCASP_DITCSRB4 is shown in [Figure 6-51](#) and described in [Table 6-104](#).

Return to [Summary Table](#).

Table 6-103. MCASP_DITCSRB4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0128h |
| MCASP1_CFG | 02B1 0128h |
| MCASP2_CFG | 02B2 0128h |

Figure 6-51. MCASP_DITCSRB4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRB4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-104. MCASP_DITCSRB4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------------------------------|
| 31-0 | DITCSRB4 | R/W | 0h | DIT right channel status registers. |

6.53 MCASP_DITCSRB5 Register (Offset = 12Ch) [reset = 0h]

MCASP_DITCSRB5 is shown in [Figure 6-52](#) and described in [Table 6-106](#).

Return to [Summary Table](#).

Table 6-105. MCASP_DITCSRB5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 012Ch |
| MCASP1_CFG | 02B1 012Ch |
| MCASP2_CFG | 02B2 012Ch |

Figure 6-52. MCASP_DITCSRB5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITCSRB5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-106. MCASP_DITCSRB5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------------------------------|
| 31-0 | DITCSRB5 | R/W | 0h | DIT right channel status registers. |

6.54 MCASP_DITUDRA0 Register (Offset = 130h) [reset = 0h]

MCASP_DITUDRA0 is shown in [Figure 6-53](#) and described in [Table 6-108](#).

Return to [Summary Table](#).

Table 6-107. MCASP_DITUDRA0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0130h |
| MCASP1_CFG | 02B1 0130h |
| MCASP2_CFG | 02B2 0130h |

Figure 6-53. MCASP_DITUDRA0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRA0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-108. MCASP_DITUDRA0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------------------------|
| 31-0 | DITUDRA0 | R/W | 0h | DIT left channel user data registers. |

6.55 MCASP_DITUDRA1 Register (Offset = 134h) [reset = 0h]

MCASP_DITUDRA1 is shown in [Figure 6-54](#) and described in [Table 6-110](#).

Return to [Summary Table](#).

Table 6-109. MCASP_DITUDRA1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0134h |
| MCASP1_CFG | 02B1 0134h |
| MCASP2_CFG | 02B2 0134h |

Figure 6-54. MCASP_DITUDRA1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRA1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-110. MCASP_DITUDRA1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------------------------|
| 31-0 | DITUDRA1 | R/W | 0h | DIT left channel user data registers. |

6.56 MCASP_DITUDRA2 Register (Offset = 138h) [reset = 0h]

MCASP_DITUDRA2 is shown in [Figure 6-55](#) and described in [Table 6-112](#).

Return to [Summary Table](#).

Table 6-111. MCASP_DITUDRA2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0138h |
| MCASP1_CFG | 02B1 0138h |
| MCASP2_CFG | 02B2 0138h |

Figure 6-55. MCASP_DITUDRA2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRA2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-112. MCASP_DITUDRA2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------------------------|
| 31-0 | DITUDRA2 | R/W | 0h | DIT left channel user data registers. |

6.57 MCASP_DITUDRA3 Register (Offset = 13Ch) [reset = 0h]

MCASP_DITUDRA3 is shown in [Figure 6-56](#) and described in [Table 6-114](#).

Return to [Summary Table](#).

Table 6-113. MCASP_DITUDRA3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 013Ch |
| MCASP1_CFG | 02B1 013Ch |
| MCASP2_CFG | 02B2 013Ch |

Figure 6-56. MCASP_DITUDRA3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRA3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-114. MCASP_DITUDRA3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------------------------|
| 31-0 | DITUDRA3 | R/W | 0h | DIT left channel user data registers. |

6.58 MCASP_DITUDRA4 Register (Offset = 140h) [reset = 0h]

MCASP_DITUDRA4 is shown in [Figure 6-57](#) and described in [Table 6-116](#).

Return to [Summary Table](#).

Table 6-115. MCASP_DITUDRA4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0140h |
| MCASP1_CFG | 02B1 0140h |
| MCASP2_CFG | 02B2 0140h |

Figure 6-57. MCASP_DITUDRA4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRA4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-116. MCASP_DITUDRA4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------------------------|
| 31-0 | DITUDRA4 | R/W | 0h | DIT left channel user data registers. |

6.59 MCASP_DITUDRA5 Register (Offset = 144h) [reset = 0h]

MCASP_DITUDRA5 is shown in [Figure 6-58](#) and described in [Table 6-118](#).

Return to [Summary Table](#).

Table 6-117. MCASP_DITUDRA5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0144h |
| MCASP1_CFG | 02B1 0144h |
| MCASP2_CFG | 02B2 0144h |

Figure 6-58. MCASP_DITUDRA5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRA5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-118. MCASP_DITUDRA5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------------------------|
| 31-0 | DITUDRA5 | R/W | 0h | DIT left channel user data registers. |

6.60 MCASP_DITUDRB0 Register (Offset = 148h) [reset = 0h]

MCASP_DITUDRB0 is shown in [Figure 6-59](#) and described in [Table 6-120](#).

Return to [Summary Table](#).

Table 6-119. MCASP_DITUDRB0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0148h |
| MCASP1_CFG | 02B1 0148h |
| MCASP2_CFG | 02B2 0148h |

Figure 6-59. MCASP_DITUDRB0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRB0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-120. MCASP_DITUDRB0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | DITUDRB0 | R/W | 0h | DIT right channel user data registers. |

6.61 MCASP_DITUDRB1 Register (Offset = 14Ch) [reset = 0h]

MCASP_DITUDRB1 is shown in [Figure 6-60](#) and described in [Table 6-122](#).

Return to [Summary Table](#).

Table 6-121. MCASP_DITUDRB1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 014Ch |
| MCASP1_CFG | 02B1 014Ch |
| MCASP2_CFG | 02B2 014Ch |

Figure 6-60. MCASP_DITUDRB1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRB1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-122. MCASP_DITUDRB1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | DITUDRB1 | R/W | 0h | DIT right channel user data registers. |

6.62 MCASP_DITUDRB2 Register (Offset = 150h) [reset = 0h]

MCASP_DITUDRB2 is shown in [Figure 6-61](#) and described in [Table 6-124](#).

Return to [Summary Table](#).

Table 6-123. MCASP_DITUDRB2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0150h |
| MCASP1_CFG | 02B1 0150h |
| MCASP2_CFG | 02B2 0150h |

Figure 6-61. MCASP_DITUDRB2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRB2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-124. MCASP_DITUDRB2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | DITUDRB2 | R/W | 0h | DIT right channel user data registers. |

6.63 MCASP_DITUDRB3 Register (Offset = 154h) [reset = 0h]

MCASP_DITUDRB3 is shown in [Figure 6-62](#) and described in [Table 6-126](#).

Return to [Summary Table](#).

Table 6-125. MCASP_DITUDRB3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0154h |
| MCASP1_CFG | 02B1 0154h |
| MCASP2_CFG | 02B2 0154h |

Figure 6-62. MCASP_DITUDRB3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRB3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-126. MCASP_DITUDRB3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | DITUDRB3 | R/W | 0h | DIT right channel user data registers. |

6.64 MCASP_DITUDRB4 Register (Offset = 158h) [reset = 0h]

MCASP_DITUDRB4 is shown in [Figure 6-63](#) and described in [Table 6-128](#).

Return to [Summary Table](#).

Table 6-127. MCASP_DITUDRB4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0158h |
| MCASP1_CFG | 02B1 0158h |
| MCASP2_CFG | 02B2 0158h |

Figure 6-63. MCASP_DITUDRB4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRB4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-128. MCASP_DITUDRB4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | DITUDRB4 | R/W | 0h | DIT right channel user data registers. |

6.65 MCASP_DITUDRB5 Register (Offset = 15Ch) [reset = 0h]

MCASP_DITUDRB5 is shown in [Figure 6-64](#) and described in [Table 6-130](#).

Return to [Summary Table](#).

Table 6-129. MCASP_DITUDRB5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 015Ch |
| MCASP1_CFG | 02B1 015Ch |
| MCASP2_CFG | 02B2 015Ch |

Figure 6-64. MCASP_DITUDRB5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DITUDRB5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-130. MCASP_DITUDRB5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | DITUDRB5 | R/W | 0h | DIT right channel user data registers. |

6.66 MCASP_XRSRCTL0 Register (Offset = 180h) [reset = 0h]

MCASP_XRSRCTL0 is shown in [Figure 6-65](#) and described in [Table 6-132](#).

Return to [Summary Table](#).

Table 6-131. MCASP_XRSRCTL0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0180h |
| MCASP1_CFG | 02B1 0180h |
| MCASP2_CFG | 02B2 0180h |

Figure 6-65. MCASP_XRSRCTL0 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-132. MCASP_XRSRCTL0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-132. MCASP_XRSRCTL0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.67 MCASP_XRSRCTL1 Register (Offset = 184h) [reset = 0h]

MCASP_XRSRCTL1 is shown in [Figure 6-66](#) and described in [Table 6-134](#).

Return to [Summary Table](#).

Table 6-133. MCASP_XRSRCTL1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0184h |
| MCASP1_CFG | 02B1 0184h |
| MCASP2_CFG | 02B2 0184h |

Figure 6-66. MCASP_XRSRCTL1 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-134. MCASP_XRSRCTL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-134. MCASP_XRSRCTL1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.68 MCASP_XRSRCTL2 Register (Offset = 188h) [reset = 0h]

MCASP_XRSRCTL2 is shown in [Figure 6-67](#) and described in [Table 6-136](#).

Return to [Summary Table](#).

Table 6-135. MCASP_XRSRCTL2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0188h |
| MCASP1_CFG | 02B1 0188h |
| MCASP2_CFG | 02B2 0188h |

Figure 6-67. MCASP_XRSRCTL2 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-136. MCASP_XRSRCTL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-136. MCASP_XRSRCTL2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.69 MCASP_XRSRCTL3 Register (Offset = 18Ch) [reset = 0h]

MCASP_XRSRCTL3 is shown in [Figure 6-68](#) and described in [Table 6-138](#).

Return to [Summary Table](#).

Table 6-137. MCASP_XRSRCTL3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 018Ch |
| MCASP1_CFG | 02B1 018Ch |
| MCASP2_CFG | 02B2 018Ch |

Figure 6-68. MCASP_XRSRCTL3 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-138. MCASP_XRSRCTL3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-138. MCASP_XRSRCTL3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.70 MCASP_XRSRCTL4 Register (Offset = 190h) [reset = 0h]

MCASP_XRSRCTL4 is shown in [Figure 6-69](#) and described in [Table 6-140](#).

Return to [Summary Table](#).

Table 6-139. MCASP_XRSRCTL4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0190h |
| MCASP1_CFG | 02B1 0190h |
| MCASP2_CFG | 02B2 0190h |

Figure 6-69. MCASP_XRSRCTL4 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-140. MCASP_XRSRCTL4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-140. MCASP_XRSRCTL4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.71 MCASP_XRSRCTL5 Register (Offset = 194h) [reset = 0h]

MCASP_XRSRCTL5 is shown in [Figure 6-70](#) and described in [Table 6-142](#).

Return to [Summary Table](#).

Table 6-141. MCASP_XRSRCTL5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0194h |
| MCASP1_CFG | 02B1 0194h |
| MCASP2_CFG | 02B2 0194h |

Figure 6-70. MCASP_XRSRCTL5 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-142. MCASP_XRSRCTL5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-142. MCASP_XRSRCTL5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.72 MCASP_XRSRCTL6 Register (Offset = 198h) [reset = 0h]

MCASP_XRSRCTL6 is shown in [Figure 6-71](#) and described in [Table 6-144](#).

Return to [Summary Table](#).

Table 6-143. MCASP_XRSRCTL6 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0198h |
| MCASP1_CFG | 02B1 0198h |
| MCASP2_CFG | 02B2 0198h |

Figure 6-71. MCASP_XRSRCTL6 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-144. MCASP_XRSRCTL6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-144. MCASP_XRSRCTL6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.73 MCASP_XRSRCTL7 Register (Offset = 19Ch) [reset = 0h]

MCASP_XRSRCTL7 is shown in [Figure 6-72](#) and described in [Table 6-146](#).

Return to [Summary Table](#).

Table 6-145. MCASP_XRSRCTL7 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 019Ch |
| MCASP1_CFG | 02B1 019Ch |
| MCASP2_CFG | 02B2 019Ch |

Figure 6-72. MCASP_XRSRCTL7 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-146. MCASP_XRSRCTL7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-146. MCASP_XRSRCTL7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.74 MCASP_XRSRCTL8 Register (Offset = 1A0h) [reset = 0h]

MCASP_XRSRCTL8 is shown in [Figure 6-73](#) and described in [Table 6-148](#).

Return to [Summary Table](#).

Table 6-147. MCASP_XRSRCTL8 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01A0h |
| MCASP1_CFG | 02B1 01A0h |
| MCASP2_CFG | 02B2 01A0h |

Figure 6-73. MCASP_XRSRCTL8 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-148. MCASP_XRSRCTL8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-148. MCASP_XRSRCTL8 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.75 MCASP_XRSRCTL9 Register (Offset = 1A4h) [reset = 0h]

MCASP_XRSRCTL9 is shown in [Figure 6-74](#) and described in [Table 6-150](#).

Return to [Summary Table](#).

Table 6-149. MCASP_XRSRCTL9 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01A4h |
| MCASP1_CFG | 02B1 01A4h |
| MCASP2_CFG | 02B2 01A4h |

Figure 6-74. MCASP_XRSRCTL9 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-150. MCASP_XRSRCTL9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-150. MCASP_XRSRCTL9 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.76 MCASP_XRSRCTL10 Register (Offset = 1A8h) [reset = 0h]

MCASP_XRSRCTL10 is shown in [Figure 6-75](#) and described in [Table 6-152](#).

Return to [Summary Table](#).

Table 6-151. MCASP_XRSRCTL10 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01A8h |
| MCASP1_CFG | 02B1 01A8h |
| MCASP2_CFG | 02B2 01A8h |

Figure 6-75. MCASP_XRSRCTL10 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-152. MCASP_XRSRCTL10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-152. MCASP_XRSRCTL10 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.77 MCASP_XRSRCTL11 Register (Offset = 1ACh) [reset = 0h]

MCASP_XRSRCTL11 is shown in [Figure 6-76](#) and described in [Table 6-154](#).

Return to [Summary Table](#).

Table 6-153. MCASP_XRSRCTL11 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01ACh |
| MCASP1_CFG | 02B1 01ACh |
| MCASP2_CFG | 02B2 01ACh |

Figure 6-76. MCASP_XRSRCTL11 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-154. MCASP_XRSRCTL11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-154. MCASP_XRSRCTL11 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.78 MCASP_XRSRCTL12 Register (Offset = 1B0h) [reset = 0h]

MCASP_XRSRCTL12 is shown in [Figure 6-77](#) and described in [Table 6-156](#).

Return to [Summary Table](#).

Table 6-155. MCASP_XRSRCTL12 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01B0h |
| MCASP1_CFG | 02B1 01B0h |
| MCASP2_CFG | 02B2 01B0h |

Figure 6-77. MCASP_XRSRCTL12 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-156. MCASP_XRSRCTL12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-156. MCASP_XRSRCTL12 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.79 MCASP_XRSRCTL13 Register (Offset = 1B4h) [reset = 0h]

MCASP_XRSRCTL13 is shown in [Figure 6-78](#) and described in [Table 6-158](#).

Return to [Summary Table](#).

Table 6-157. MCASP_XRSRCTL13 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01B4h |
| MCASP1_CFG | 02B1 01B4h |
| MCASP2_CFG | 02B2 01B4h |

Figure 6-78. MCASP_XRSRCTL13 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-158. MCASP_XRSRCTL13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-158. MCASP_XRSRCTL13 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.80 MCASP_XRSRCTL14 Register (Offset = 1B8h) [reset = 0h]

MCASP_XRSRCTL14 is shown in [Figure 6-79](#) and described in [Table 6-160](#).

Return to [Summary Table](#).

Table 6-159. MCASP_XRSRCTL14 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01B8h |
| MCASP1_CFG | 02B1 01B8h |
| MCASP2_CFG | 02B2 01B8h |

Figure 6-79. MCASP_XRSRCTL14 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-160. MCASP_XRSRCTL14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-160. MCASP_XRSRCTL14 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.81 MCASP_XRSRCTL15 Register (Offset = 1BCh) [reset = 0h]

MCASP_XRSRCTL15 is shown in [Figure 6-80](#) and described in [Table 6-162](#).

Return to [Summary Table](#).

Table 6-161. MCASP_XRSRCTL15 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 01BCh |
| MCASP1_CFG | 02B1 01BCh |
| MCASP2_CFG | 02B2 01BCh |

Figure 6-80. MCASP_XRSRCTL15 Register

| | | | | | | | |
|----------|----|------|------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RRDY | XRDY | DISMOD | | SRMOD | |
| R/W-0h | | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 6-162. MCASP_XRSRCTL15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-6 | RESERVED | R/W | 0h | Reserved |
| 5 | RRDY | R | 0h | Receive buffer ready bit. RRDY indicates the current receive buffer state. Always reads 0 when programmed as a transmitter or as inactive. If SRMOD bit is set to receive [2h], RRDY switches from 0 to 1 whenever data is transferred from XRSR to RBUF. 0h = Receive buffer (RBUF) is empty. 1h = Receive buffer (RBUF) contains data and needs to be read before the start of the next time slot or a receiver overrun occurs. |
| 4 | XRDY | R | 0h | Transmit buffer ready bit. XRDY indicates the current transmit buffer state. Always reads 0 when programmed as a receiver or as inactive. If SRMOD bit is set to transmit [1h], XRDY switches from 0 to 1 when XSRCLR in MCASP_GBLCTL is switched from 0 to 1 to indicate an empty transmitter. XRDY remains set until XSRCLR is forced to 0, data is written to the corresponding transmit buffer, or SRMOD bit is changed to receive [2h] or inactive [0]. 0h = Transmit buffer (XBUF) contains data. 1h = Transmit buffer (XBUF) is empty and needs to be written before the start of the next time slot or a transmit underrun occurs. |

Table 6-162. MCASP_XRSRCTL15 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 3-2 | DISMOD | R/W | 0h | <p>Serializer pin drive mode bit.</p> <p>Drive on pin when in inactive TDM slot of transmit mode or when serializer is inactive.</p> <p>This field only applies if the pin is configured as a McASP pin [MCASP_PFUNC = 0].</p> <p>0h = Drive on pin is 3-state.</p> <p>1h = Reserved.</p> <p>2h = Drive on pin is logic low.</p> <p>3h = Drive on pin is logic high.</p> |
| 1-0 | SRMOD | R/W | 0h | <p>Serializer mode bit.</p> <p>0h = Serializer is inactive.</p> <p>1h = Serializer is transmitter.</p> <p>2h = Serializer is receiver.</p> <p>3h = Reserved.</p> |

6.82 MCASP_TXBUF0 Register (Offset = 200h) [reset = 0h]

MCASP_TXBUF0 is shown in [Figure 6-81](#) and described in [Table 6-164](#).

Return to [Summary Table](#).

Table 6-163. MCASP_TXBUF0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0200h |
| MCASP1_CFG | 02B1 0200h |
| MCASP2_CFG | 02B2 0200h |

Figure 6-81. MCASP_TXBUF0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-164. MCASP_TXBUF0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF0 | R/W | 0h | Transmit buffers for serializers. |

6.83 MCASP_TXBUF1 Register (Offset = 204h) [reset = 0h]

MCASP_TXBUF1 is shown in [Figure 6-82](#) and described in [Table 6-166](#).

Return to [Summary Table](#).

Table 6-165. MCASP_TXBUF1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0204h |
| MCASP1_CFG | 02B1 0204h |
| MCASP2_CFG | 02B2 0204h |

Figure 6-82. MCASP_TXBUF1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-166. MCASP_TXBUF1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF1 | R/W | 0h | Transmit buffers for serializers. |

6.84 MCASP_TXBUF2 Register (Offset = 208h) [reset = 0h]

MCASP_TXBUF2 is shown in [Figure 6-83](#) and described in [Table 6-168](#).

Return to [Summary Table](#).

Table 6-167. MCASP_TXBUF2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0208h |
| MCASP1_CFG | 02B1 0208h |
| MCASP2_CFG | 02B2 0208h |

Figure 6-83. MCASP_TXBUF2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-168. MCASP_TXBUF2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF2 | R/W | 0h | Transmit buffers for serializers. |

6.85 MCASP_TXBUF3 Register (Offset = 20Ch) [reset = 0h]

MCASP_TXBUF3 is shown in [Figure 6-84](#) and described in [Table 6-170](#).

Return to [Summary Table](#).

Table 6-169. MCASP_TXBUF3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 020Ch |
| MCASP1_CFG | 02B1 020Ch |
| MCASP2_CFG | 02B2 020Ch |

Figure 6-84. MCASP_TXBUF3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-170. MCASP_TXBUF3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF3 | R/W | 0h | Transmit buffers for serializers. |

6.86 MCASP_TXBUF4 Register (Offset = 210h) [reset = 0h]

MCASP_TXBUF4 is shown in [Figure 6-85](#) and described in [Table 6-172](#).

Return to [Summary Table](#).

Table 6-171. MCASP_TXBUF4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0210h |
| MCASP1_CFG | 02B1 0210h |
| MCASP2_CFG | 02B2 0210h |

Figure 6-85. MCASP_TXBUF4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-172. MCASP_TXBUF4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF4 | R/W | 0h | Transmit buffers for serializers. |

6.87 MCASP_TXBUF5 Register (Offset = 214h) [reset = 0h]

MCASP_TXBUF5 is shown in [Figure 6-86](#) and described in [Table 6-174](#).

Return to [Summary Table](#).

Table 6-173. MCASP_TXBUF5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0214h |
| MCASP1_CFG | 02B1 0214h |
| MCASP2_CFG | 02B2 0214h |

Figure 6-86. MCASP_TXBUF5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-174. MCASP_TXBUF5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF5 | R/W | 0h | Transmit buffers for serializers. |

6.88 MCASP_TXBUF6 Register (Offset = 218h) [reset = 0h]

MCASP_TXBUF6 is shown in [Figure 6-87](#) and described in [Table 6-176](#).

Return to [Summary Table](#).

Table 6-175. MCASP_TXBUF6 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0218h |
| MCASP1_CFG | 02B1 0218h |
| MCASP2_CFG | 02B2 0218h |

Figure 6-87. MCASP_TXBUF6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-176. MCASP_TXBUF6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF6 | R/W | 0h | Transmit buffers for serializers. |

6.89 MCASP_TXBUF7 Register (Offset = 21Ch) [reset = 0h]

MCASP_TXBUF7 is shown in [Figure 6-88](#) and described in [Table 6-178](#).

Return to [Summary Table](#).

Table 6-177. MCASP_TXBUF7 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 021Ch |
| MCASP1_CFG | 02B1 021Ch |
| MCASP2_CFG | 02B2 021Ch |

Figure 6-88. MCASP_TXBUF7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-178. MCASP_TXBUF7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF7 | R/W | 0h | Transmit buffers for serializers. |

6.90 MCASP_TXBUF8 Register (Offset = 220h) [reset = 0h]

MCASP_TXBUF8 is shown in [Figure 6-89](#) and described in [Table 6-180](#).

Return to [Summary Table](#).

Table 6-179. MCASP_TXBUF8 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0220h |
| MCASP1_CFG | 02B1 0220h |
| MCASP2_CFG | 02B2 0220h |

Figure 6-89. MCASP_TXBUF8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-180. MCASP_TXBUF8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF8 | R/W | 0h | Transmit buffers for serializers. |

6.91 MCASP_TXBUF9 Register (Offset = 224h) [reset = 0h]

MCASP_TXBUF9 is shown in [Figure 6-90](#) and described in [Table 6-182](#).

Return to [Summary Table](#).

Table 6-181. MCASP_TXBUF9 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0224h |
| MCASP1_CFG | 02B1 0224h |
| MCASP2_CFG | 02B2 0224h |

Figure 6-90. MCASP_TXBUF9 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-182. MCASP_TXBUF9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | XBUF9 | R/W | 0h | Transmit buffers for serializers. |

6.92 MCASP_TXBUF10 Register (Offset = 228h) [reset = 0h]

MCASP_TXBUF10 is shown in [Figure 6-91](#) and described in [Table 6-184](#).

Return to [Summary Table](#).

Table 6-183. MCASP_TXBUF10 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0228h |
| MCASP1_CFG | 02B1 0228h |
| MCASP2_CFG | 02B2 0228h |

Figure 6-91. MCASP_TXBUF10 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-184. MCASP_TXBUF10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-----------------------------------|
| 31-0 | XBUF10 | R/W | 0h | Transmit buffers for serializers. |

6.93 MCASP_TXBUF11 Register (Offset = 22Ch) [reset = 0h]

MCASP_TXBUF11 is shown in [Figure 6-92](#) and described in [Table 6-186](#).

Return to [Summary Table](#).

Table 6-185. MCASP_TXBUF11 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 022Ch |
| MCASP1_CFG | 02B1 022Ch |
| MCASP2_CFG | 02B2 022Ch |

Figure 6-92. MCASP_TXBUF11 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-186. MCASP_TXBUF11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-----------------------------------|
| 31-0 | XBUF11 | R/W | 0h | Transmit buffers for serializers. |

6.94 MCASP_TXBUF12 Register (Offset = 230h) [reset = 0h]

MCASP_TXBUF12 is shown in [Figure 6-93](#) and described in [Table 6-188](#).

Return to [Summary Table](#).

Table 6-187. MCASP_TXBUF12 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0230h |
| MCASP1_CFG | 02B1 0230h |
| MCASP2_CFG | 02B2 0230h |

Figure 6-93. MCASP_TXBUF12 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-188. MCASP_TXBUF12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-----------------------------------|
| 31-0 | XBUF12 | R/W | 0h | Transmit buffers for serializers. |

6.95 MCASP_TXBUF13 Register (Offset = 234h) [reset = 0h]

MCASP_TXBUF13 is shown in [Figure 6-94](#) and described in [Table 6-190](#).

Return to [Summary Table](#).

Table 6-189. MCASP_TXBUF13 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0234h |
| MCASP1_CFG | 02B1 0234h |
| MCASP2_CFG | 02B2 0234h |

Figure 6-94. MCASP_TXBUF13 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-190. MCASP_TXBUF13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-----------------------------------|
| 31-0 | XBUF13 | R/W | 0h | Transmit buffers for serializers. |

6.96 MCASP_TXBUF14 Register (Offset = 238h) [reset = 0h]

MCASP_TXBUF14 is shown in [Figure 6-95](#) and described in [Table 6-192](#).

Return to [Summary Table](#).

Table 6-191. MCASP_TXBUF14 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0238h |
| MCASP1_CFG | 02B1 0238h |
| MCASP2_CFG | 02B2 0238h |

Figure 6-95. MCASP_TXBUF14 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-192. MCASP_TXBUF14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-----------------------------------|
| 31-0 | XBUF14 | R/W | 0h | Transmit buffers for serializers. |

6.97 MCASP_TXBUF15 Register (Offset = 23Ch) [reset = 0h]

MCASP_TXBUF15 is shown in [Figure 6-96](#) and described in [Table 6-194](#).

Return to [Summary Table](#).

Table 6-193. MCASP_TXBUF15 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 023Ch |
| MCASP1_CFG | 02B1 023Ch |
| MCASP2_CFG | 02B2 023Ch |

Figure 6-96. MCASP_TXBUF15 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XBUF15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-194. MCASP_TXBUF15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-----------------------------------|
| 31-0 | XBUF15 | R/W | 0h | Transmit buffers for serializers. |

6.98 MCASP_RXBUF0 Register (Offset = 280h) [reset = 0h]

MCASP_RXBUF0 is shown in [Figure 6-97](#) and described in [Table 6-196](#).

Return to [Summary Table](#).

Table 6-195. MCASP_RXBUF0 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0280h |
| MCASP1_CFG | 02B1 0280h |
| MCASP2_CFG | 02B2 0280h |

Figure 6-97. MCASP_RXBUF0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-196. MCASP_RXBUF0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF0 | R/W | 0h | Receive buffers for serializers. |

6.99 MCASP_RXBUF1 Register (Offset = 284h) [reset = 0h]

MCASP_RXBUF1 is shown in [Figure 6-98](#) and described in [Table 6-198](#).

Return to [Summary Table](#).

Table 6-197. MCASP_RXBUF1 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0284h |
| MCASP1_CFG | 02B1 0284h |
| MCASP2_CFG | 02B2 0284h |

Figure 6-98. MCASP_RXBUF1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-198. MCASP_RXBUF1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF1 | R/W | 0h | Receive buffers for serializers. |

6.100 MCASP_RXBUF2 Register (Offset = 288h) [reset = 0h]

MCASP_RXBUF2 is shown in [Figure 6-99](#) and described in [Table 6-200](#).

Return to [Summary Table](#).

Table 6-199. MCASP_RXBUF2 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0288h |
| MCASP1_CFG | 02B1 0288h |
| MCASP2_CFG | 02B2 0288h |

Figure 6-99. MCASP_RXBUF2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-200. MCASP_RXBUF2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF2 | R/W | 0h | Receive buffers for serializers. |

6.101 MCASP_RXBUF3 Register (Offset = 28Ch) [reset = 0h]

MCASP_RXBUF3 is shown in [Figure 6-100](#) and described in [Table 6-202](#).

Return to [Summary Table](#).

Table 6-201. MCASP_RXBUF3 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 028Ch |
| MCASP1_CFG | 02B1 028Ch |
| MCASP2_CFG | 02B2 028Ch |

Figure 6-100. MCASP_RXBUF3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-202. MCASP_RXBUF3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF3 | R/W | 0h | Receive buffers for serializers. |

6.102 MCASP_RXBUF4 Register (Offset = 290h) [reset = 0h]

MCASP_RXBUF4 is shown in [Figure 6-101](#) and described in [Table 6-204](#).

Return to [Summary Table](#).

Table 6-203. MCASP_RXBUF4 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0290h |
| MCASP1_CFG | 02B1 0290h |
| MCASP2_CFG | 02B2 0290h |

Figure 6-101. MCASP_RXBUF4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-204. MCASP_RXBUF4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF4 | R/W | 0h | Receive buffers for serializers. |

6.103 MCASP_RXBUF5 Register (Offset = 294h) [reset = 0h]

MCASP_RXBUF5 is shown in [Figure 6-102](#) and described in [Table 6-206](#).

Return to [Summary Table](#).

Table 6-205. MCASP_RXBUF5 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0294h |
| MCASP1_CFG | 02B1 0294h |
| MCASP2_CFG | 02B2 0294h |

Figure 6-102. MCASP_RXBUF5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-206. MCASP_RXBUF5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF5 | R/W | 0h | Receive buffers for serializers. |

6.104 MCASP_RXBUF6 Register (Offset = 298h) [reset = 0h]

MCASP_RXBUF6 is shown in [Figure 6-103](#) and described in [Table 6-208](#).

Return to [Summary Table](#).

Table 6-207. MCASP_RXBUF6 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 0298h |
| MCASP1_CFG | 02B1 0298h |
| MCASP2_CFG | 02B2 0298h |

Figure 6-103. MCASP_RXBUF6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-208. MCASP_RXBUF6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF6 | R/W | 0h | Receive buffers for serializers. |

6.105 MCASP_RXBUF7 Register (Offset = 29Ch) [reset = 0h]

MCASP_RXBUF7 is shown in [Figure 6-104](#) and described in [Table 6-210](#).

Return to [Summary Table](#).

Table 6-209. MCASP_RXBUF7 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 029Ch |
| MCASP1_CFG | 02B1 029Ch |
| MCASP2_CFG | 02B2 029Ch |

Figure 6-104. MCASP_RXBUF7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-210. MCASP_RXBUF7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF7 | R/W | 0h | Receive buffers for serializers. |

6.106 MCASP_RXBUF8 Register (Offset = 2A0h) [reset = 0h]

MCASP_RXBUF8 is shown in [Figure 6-105](#) and described in [Table 6-212](#).

Return to [Summary Table](#).

Table 6-211. MCASP_RXBUF8 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02A0h |
| MCASP1_CFG | 02B1 02A0h |
| MCASP2_CFG | 02B2 02A0h |

Figure 6-105. MCASP_RXBUF8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-212. MCASP_RXBUF8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF8 | R/W | 0h | Receive buffers for serializers. |

6.107 MCASP_RXBUF9 Register (Offset = 2A4h) [reset = 0h]

MCASP_RXBUF9 is shown in [Figure 6-106](#) and described in [Table 6-214](#).

Return to [Summary Table](#).

Table 6-213. MCASP_RXBUF9 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02A4h |
| MCASP1_CFG | 02B1 02A4h |
| MCASP2_CFG | 02B2 02A4h |

Figure 6-106. MCASP_RXBUF9 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-214. MCASP_RXBUF9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|----------------------------------|
| 31-0 | RBUF9 | R/W | 0h | Receive buffers for serializers. |

6.108 MCASP_RXBUF10 Register (Offset = 2A8h) [reset = 0h]

MCASP_RXBUF10 is shown in [Figure 6-107](#) and described in [Table 6-216](#).

Return to [Summary Table](#).

Table 6-215. MCASP_RXBUF10 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02A8h |
| MCASP1_CFG | 02B1 02A8h |
| MCASP2_CFG | 02B2 02A8h |

Figure 6-107. MCASP_RXBUF10 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-216. MCASP_RXBUF10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|----------------------------------|
| 31-0 | RBUF10 | R/W | 0h | Receive buffers for serializers. |

6.109 MCASP_RXBUF11 Register (Offset = 2ACh) [reset = 0h]

MCASP_RXBUF11 is shown in [Figure 6-108](#) and described in [Table 6-218](#).

Return to [Summary Table](#).

Table 6-217. MCASP_RXBUF11 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02ACh |
| MCASP1_CFG | 02B1 02ACh |
| MCASP2_CFG | 02B2 02ACh |

Figure 6-108. MCASP_RXBUF11 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-218. MCASP_RXBUF11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|----------------------------------|
| 31-0 | RBUF11 | R/W | 0h | Receive buffers for serializers. |

6.110 MCASP_RXBUF12 Register (Offset = 2B0h) [reset = 0h]

MCASP_RXBUF12 is shown in [Figure 6-109](#) and described in [Table 6-220](#).

Return to [Summary Table](#).

Table 6-219. MCASP_RXBUF12 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02B0h |
| MCASP1_CFG | 02B1 02B0h |
| MCASP2_CFG | 02B2 02B0h |

Figure 6-109. MCASP_RXBUF12 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF12 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-220. MCASP_RXBUF12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|----------------------------------|
| 31-0 | RBUF12 | R/W | 0h | Receive buffers for serializers. |

6.111 MCASP_RXBUF13 Register (Offset = 2B4h) [reset = 0h]

MCASP_RXBUF13 is shown in [Figure 6-110](#) and described in [Table 6-222](#).

Return to [Summary Table](#).

Table 6-221. MCASP_RXBUF13 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02B4h |
| MCASP1_CFG | 02B1 02B4h |
| MCASP2_CFG | 02B2 02B4h |

Figure 6-110. MCASP_RXBUF13 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF13 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-222. MCASP_RXBUF13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|----------------------------------|
| 31-0 | RBUF13 | R/W | 0h | Receive buffers for serializers. |

6.112 MCASP_RXBUF14 Register (Offset = 2B8h) [reset = 0h]

MCASP_RXBUF14 is shown in [Figure 6-111](#) and described in [Table 6-224](#).

Return to [Summary Table](#).

Table 6-223. MCASP_RXBUF14 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02B8h |
| MCASP1_CFG | 02B1 02B8h |
| MCASP2_CFG | 02B2 02B8h |

Figure 6-111. MCASP_RXBUF14 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF14 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-224. MCASP_RXBUF14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|----------------------------------|
| 31-0 | RBUF14 | R/W | 0h | Receive buffers for serializers. |

6.113 MCASP_RXBUF15 Register (Offset = 2BCh) [reset = 0h]

MCASP_RXBUF15 is shown in [Figure 6-112](#) and described in [Table 6-226](#).

Return to [Summary Table](#).

Table 6-225. MCASP_RXBUF15 Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_CFG | 02B0 02BCh |
| MCASP1_CFG | 02B1 02BCh |
| MCASP2_CFG | 02B2 02BCh |

Figure 6-112. MCASP_RXBUF15 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RBUF15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 6-226. MCASP_RXBUF15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|----------------------------------|
| 31-0 | RBUF15 | R/W | 0h | Receive buffers for serializers. |

6.114 MCASP_DMA Registers

lists the memory-mapped registers for the MCASP_DMA. All register offset addresses not listed in should be considered as reserved locations and the register contents should not be modified.

Table 6-227. MCASP_DMA Instances

| Instance | Base Address |
|------------|--------------|
| MCASP0_DMA | 02B0 8000h |
| MCASP1_DMA | 02B1 8000h |
| MCASP2_DMA | 02B2 8000h |

Table 6-228. MCASP_DMA Registers

| Offset | Acronym | Register Name | MCASP0_DM A Physical Address | MCASP1_DM A Physical Address | MCASP2_DM A Physical Address |
|--------------------|-----------------------------|----------------|------------------------------------|------------------------------------|------------------------------------|
| N/A ⁽¹⁾ | MCASP_TXBUF | Tx Buffer Data | 02B0 8000h | 02B1 8000h | 02B2 8000h |
| N/A ⁽¹⁾ | MCASP_RXBUF | Rx Buffer Data | 02B0 8000h | 02B1 8000h | 02B2 8000h |

- (1) N/A denotes an example for DATA port offset value. Actually, whatever the offset value is added to base address, it is ignored (don't care) when Arm performs accesses to XRBUFFn RX/TX buffers through the McASP DATA port.

Note

For MCASP_TXBUF and MCASP_RXBUF buffer accesses through the MCASP DATA port, the destination physical address is always the same regardless of current channel index or transfer direction. The MCASP_TXFMT[3] XBUSEL bit must be set to 0b0, to allow write transfers through the DATA port. The MCASP_RXFMT[3] RBUSEL bit must be set to 0b0, to allow read transfers through the DATA port.

Note

The MCASP DATA port is exclusively assigned for DMAs / device CPUs accesses to the MCASP channels transmit and receive buffer registers. All other MCASP module registers must be accessed through the MCASP CFG (peripheral) port.

6.115 MCASP_TXBUF Register (Offset = 0h) [reset = 0h]

MCASP_TXBUF is shown in [Figure 6-113](#) and described in [Table 6-230](#).

Through the DATA port, the Host can service all serializers through a single address and the MCASP automatically cycles through the appropriate serializers. For transmit operations through the DATA port, the Host should write to the same DATA port address to service all of the active transmit serializers upon each transmit data ready event. To enable accesses from the Host to the MCASP_TXBUF_n registers through the DATA port, one must clear the XBUSEL bits to 0 in the respective MCASP_TXFMT registers.

Table 6-229. MCASP_TXBUF Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_DMA | 02B0 8000h |
| MCASP1_DMA | 02B1 8000h |
| MCASP2_DMA | 02B2 8000h |

Figure 6-113. MCASP_TXBUF Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TXBUF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 6-230. MCASP_TXBUF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------|
| 31-0 | TXBUF | W | 0h | Tx buffer data. |

6.116 MCASP_RXBUF Register (Offset = 0h) [reset = 0h]

MCASP_RXBUF is shown in [Figure 6-114](#) and described in [Table 6-232](#).

Through the DATA port, the Host can service all serializers through a single address and the MCASP automatically cycles through the appropriate serializers. For receive operations through the DATA port, the Host should read from the same MCASP_RXBUF DATA port address to service all of the active receive serializers upon each receive data ready event. To enable accesses from the Host to the MCASP_RXBUF_n registers through the DATA port, one must clear the RBUSEL bits to 0 in the respective MCASP_RXFMT registers.

Table 6-231. MCASP_RXBUF Instances

| Instance | Physical Address |
|------------|------------------|
| MCASP0_DMA | 02B0 8000h |
| MCASP1_DMA | 02B1 8000h |
| MCASP2_DMA | 02B2 8000h |

Figure 6-114. MCASP_RXBUF Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RXBUF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 6-232. MCASP_RXBUF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------|
| 31-0 | RXBUF | R | 0h | Rx buffer data. |

7 DSI Registers

7.1 DSI_ECC_AGGR Registers

Table 7-2 lists the memory-mapped registers for the DSI_ECC_AGGR. All register offset addresses not listed in Table 7-2 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. DSI_ECC_AGGR Instances

| Instance | Base Address |
|-----------------------------------|--------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SYS_CFG | 0470 0000h |

Table 7-2. DSI_ECC_AGGR Registers

| Offset | Acronym | Register Name | DSS_DSI0_DSI_TOP_ECC_AGGR_SYS_CFG Physical Address |
|---------------|---|---|--|
| 0h | DSI_ECC_REV | Aggregator Revision Register | 0470 0000h |
| 8h | DSI_ECC_VECTOR | ECC Vector Register | 0470 0008h |
| Ch | DSI_ECC_STAT | Misc Status | 0470 000Ch |
| 10h + formula | DSI_ECC_RESERVED_SVBUS_y | Reserved Area for Serial VBUS Registers | 0470 0010h + formula |
| 3Ch | DSI_ECC_SEC_EOI_REG | EOI Register | 0470 003Ch |
| 40h | DSI_ECC_SEC_STATUS_REG0 | Interrupt Status Register 0 | 0470 0040h |
| 80h | DSI_ECC_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 0470 0080h |
| C0h | DSI_ECC_SEC_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 0470 00C0h |
| 13Ch | DSI_ECC_DED_EOI_REG | EOI Register | 0470 013Ch |
| 140h | DSI_ECC_DED_STATUS_REG0 | Interrupt Status Register 0 | 0470 0140h |
| 180h | DSI_ECC_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 0470 0180h |
| 1C0h | DSI_ECC_DED_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 0470 01C0h |
| 200h | DSI_ECC_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 0470 0200h |
| 204h | DSI_ECC_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 0470 0204h |
| 208h | DSI_ECC_AGGR_STATUS_SET | AGGR interrupt status set Register | 0470 0208h |
| 20Ch | DSI_ECC_AGGR_STATUS_CLR | AGGR interrupt status clear Register | 0470 020Ch |

7.1.1 DSI_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

DSI_ECC_REV is shown in [Figure 7-1](#) and described in [Table 7-4](#).

Return to [Summary Table](#).

Revision parameters

Table 7-3. DSI_ECC_REV Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0000h |

Figure 7-1. DSI_ECC_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-4. DSI_ECC_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

Table 7-5. Register Call Summary for DSI_ECC_REV

DSI_ECC_AGGR Registers

- [DSI_ECC_REV Register \(Offset = 0h\) \[reset = 66A0EA00h\]: \[0\]](#)
- [DSI_ECC_AGGR Registers: \[0\]](#)

7.1.2 DSI_ECC_VECTOR Register (Offset = 8h) [reset = X]

DSI_ECC_VECTOR is shown in Figure 7-2 and described in Table 7-7.

Return to [Summary Table](#).

ECC DSI_ECC_VECTOR Register

Table 7-6. DSI_ECC_VECTOR Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0008h |

Figure 7-2. DSI_ECC_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_D ONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R/W-X | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-7. DSI_ECC_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or status |

Table 7-8. Register Call Summary for DSI_ECC_VECTOR

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_VECTOR Register \(Offset = 8h\) \[reset = X\]: \[0\] \[1\]](#)

7.1.3 DSI_ECC_STAT Register (Offset = Ch) [reset = X]

DSI_ECC_STAT is shown in [Figure 7-3](#) and described in [Table 7-10](#).

[Return to Summary Table.](#)

Misc Status

Table 7-9. DSI_ECC_STAT Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 000Ch |

Figure 7-3. DSI_ECC_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | NUM_RAMs | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | | | | R-1h | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-10. DSI_ECC_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 1h | Indicates the number of RAMs serviced by the ECC aggregator |

Table 7-11. Register Call Summary for DSI_ECC_STAT

| |
|---|
| DSI_ECC_AGGR Registers |
| <ul style="list-style-type: none"> • DSI_ECC_AGGR Registers: [0] • DSI_ECC_STAT Register (Offset = Ch) [reset = X]: [0] |

7.1.4 DSI_ECC_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

DSI_ECC_RESERVED_SVBUS_y is shown in Figure 7-4 and described in Table 7-13.

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 7-12. DSI_ECC_RESERVED_SVBUS_y
Instances**

| Instance | Physical Address |
|---------------------------------------|----------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0010h + formula |

Figure 7-4. DSI_ECC_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-13. DSI_ECC_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

Table 7-14. Register Call Summary for DSI_ECC_RESERVED_SVBUS_y

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_RESERVED_SVBUS_y Register \(Offset = 10h + formula\) \[reset = 0h\]: \[0\]](#)

7.1.5 DSI_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

DSI_ECC_SEC_EOI_REG is shown in Figure 7-5 and described in Table 7-16.

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 7-15. DSI_ECC_SEC_EOI_REG Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 003Ch |

Figure 7-5. DSI_ECC_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-16. DSI_ECC_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

Table 7-17. Register Call Summary for DSI_ECC_SEC_EOI_REG

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_SEC_EOI_REG Register \(Offset = 3Ch\) \[reset = X\]: \[0\]](#)

7.1.6 DSI_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

DSI_ECC_SEC_STATUS_REG0 is shown in [Figure 7-6](#) and described in [Table 7-19](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 7-18. DSI_ECC_SEC_STATUS_REG0 Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGREGATION_CFG | 0470 0040h |

Figure 7-6. DSI_ECC_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EDC_CTRL_SYS_PEND |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-19. DSI_ECC_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|-------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | EDC_CTRL_SYS_PEND | R/W1S | 0h | Interrupt Pending Status for edc_ctrl_sys_pend |

Table 7-20. Register Call Summary for DSI_ECC_SEC_STATUS_REG0

DSI_ECC_AGGREGATION Registers

- [DSI_ECC_AGGREGATION Registers: \[0\]](#)
- [DSI_ECC_SEC_STATUS_REG0 Register \(Offset = 40h\) \[reset = X\]: \[0\]](#)

7.1.7 DSI_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

DSI_ECC_SEC_ENABLE_SET_REG0 is shown in Figure 7-7 and described in Table 7-22.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

**Table 7-21. DSI_ECC_SEC_ENABLE_SET_REG0
Instances**

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0080h |

Figure 7-7. DSI_ECC_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EDC_CTRL_SY S_ENABLE_SE T |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-22. DSI_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | EDC_CTRL_SYS_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for edc_ctrl_sys_pend |

Table 7-23. Register Call Summary for DSI_ECC_SEC_ENABLE_SET_REG0

DSI_ECC_AGGR Registers

- [DSI_ECC_SEC_ENABLE_SET_REG0 Register \(Offset = 80h\) \[reset = X\]: \[0\]](#)
- [DSI_ECC_AGGR Registers: \[0\]](#)

7.1.8 DSI_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

DSI_ECC_SEC_ENABLE_CLR_REG0 is shown in Figure 7-8 and described in Table 7-25.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 7-24. DSI_ECC_SEC_ENABLE_CLR_REG0 Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 00C0h |

Figure 7-8. DSI_ECC_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EDC_CTRL_SY S_ENABLE_CLR |
| R/W-X | | | | | | | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-25. DSI_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | EDC_CTRL_SYS_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for edc_ctrl_sys_pend |

Table 7-26. Register Call Summary for DSI_ECC_SEC_ENABLE_CLR_REG0

| |
|---|
| DSI_ECC_AGGR Registers |
| <ul style="list-style-type: none"> DSI_ECC_AGGR Registers: [0] DSI_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]: [0] |

7.1.9 DSI_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

DSI_ECC_DED_EOI_REG is shown in [Figure 7-9](#) and described in [Table 7-28](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 7-27. DSI_ECC_DED_EOI_REG Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 013Ch |

Figure 7-9. DSI_ECC_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-28. DSI_ECC_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

Table 7-29. Register Call Summary for DSI_ECC_DED_EOI_REG

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_DED_EOI_REG Register \(Offset = 13Ch\) \[reset = X\]: \[0\]](#)

7.1.10 DSI_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

DSI_ECC_DED_STATUS_REG0 is shown in [Figure 7-10](#) and described in [Table 7-31](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 7-30. DSI_ECC_DED_STATUS_REG0
Instances**

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0140h |

Figure 7-10. DSI_ECC_DED_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EDC_CTRL_SY S_PEND |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-31. DSI_ECC_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|-------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | EDC_CTRL_SYS_PEND | R/W1S | 0h | Interrupt Pending Status for edc_ctrl_sys_pend |

Table 7-32. Register Call Summary for DSI_ECC_DED_STATUS_REG0

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_DED_STATUS_REG0 Register \(Offset = 140h\) \[reset = X\]: \[0\]](#)

7.1.11 DSI_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

DSI_ECC_DED_ENABLE_SET_REG0 is shown in Figure 7-11 and described in Table 7-34.

Return to [Summary Table](#).

Interrupt Enable Set Register 0

**Table 7-33. DSI_ECC_DED_ENABLE_SET_REG0
Instances**

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0180h |

Figure 7-11. DSI_ECC_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EDC_CTRL_SY S_ENABLE_SE T |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-34. DSI_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | EDC_CTRL_SYS_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for edc_ctrl_sys_pend |

Table 7-35. Register Call Summary for DSI_ECC_DED_ENABLE_SET_REG0

DSI_ECC_AGGR Registers

- [DSI_ECC_DED_ENABLE_SET_REG0 Register \(Offset = 180h\) \[reset = X\]: \[0\]](#)
- [DSI_ECC_AGGR Registers: \[0\]](#)

7.1.12 DSI_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

DSI_ECC_DED_ENABLE_CLR_REG0 is shown in Figure 7-12 and described in Table 7-37.

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

**Table 7-36. DSI_ECC_DED_ENABLE_CLR_REG0
Instances**

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 01C0h |

Figure 7-12. DSI_ECC_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EDC_CTRL_SY S_ENABLE_CLR R |
| R/W-X | | | | | | | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-37. DSI_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | EDC_CTRL_SYS_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for edc_ctrl_sys_pend |

Table 7-38. Register Call Summary for DSI_ECC_DED_ENABLE_CLR_REG0

| |
|--|
| DSI_ECC_AGGR Registers |
| <ul style="list-style-type: none"> DSI_ECC_AGGR Registers: [0] DSI_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]: [0] |

7.1.13 DSI_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

DSI_ECC_AGGR_ENABLE_SET is shown in Figure 7-13 and described in Table 7-40.

Return to [Summary Table](#).

AGGR interrupt enable set Register

**Table 7-39. DSI_ECC_AGGR_ENABLE_SET
Instances**

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0200h |

Figure 7-13. DSI_ECC_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 7-40. DSI_ECC_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

Table 7-41. Register Call Summary for DSI_ECC_AGGR_ENABLE_SET

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_AGGR_ENABLE_SET Register \(Offset = 200h\) \[reset = X\]: \[0\]](#)

7.1.14 DSI_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

DSI_ECC_AGGR_ENABLE_CLR is shown in Figure 7-14 and described in Table 7-43.

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 7-42. DSI_ECC_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0204h |

Figure 7-14. DSI_ECC_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-43. DSI_ECC_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

Table 7-44. Register Call Summary for DSI_ECC_AGGR_ENABLE_CLR

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_AGGR_ENABLE_CLR Register \(Offset = 204h\) \[reset = X\]: \[0\]](#)

7.1.15 DSI_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

DSI_ECC_AGGR_STATUS_SET is shown in Figure 7-15 and described in Table 7-46.

Return to [Summary Table](#).

AGGR interrupt status set Register

**Table 7-45. DSI_ECC_AGGR_STATUS_SET
Instances**

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 0208h |

Figure 7-15. DSI_ECC_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 7-46. DSI_ECC_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt status set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt status set for parity errors |

Table 7-47. Register Call Summary for DSI_ECC_AGGR_STATUS_SET

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_AGGR_STATUS_SET Register \(Offset = 208h\) \[reset = X\]: \[0\]](#)

7.1.16 DSI_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

DSI_ECC_AGGR_STATUS_CLR is shown in Figure 7-16 and described in Table 7-49.

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 7-48. DSI_ECC_AGGR_STATUS_CLR Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_ECC_AGGR_SY S_CFG | 0470 020Ch |

Figure 7-16. DSI_ECC_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 7-49. DSI_ECC_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt status clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt status clear for parity errors |

Table 7-50. Register Call Summary for DSI_ECC_AGGR_STATUS_CLR

DSI_ECC_AGGR Registers

- [DSI_ECC_AGGR Registers: \[0\]](#)
- [DSI_ECC_AGGR_STATUS_CLR Register \(Offset = 20Ch\) \[reset = X\]: \[0\]](#)

7.2 DSI_TOP Registers

Table 7-52 lists the memory-mapped registers for the DSI_TOP registers. All register offset addresses not listed in Table 7-52 should be considered as reserved locations and the register contents should not be modified.

N/A

Table 7-51. DSI_TOP Instances

| Instance | Base Address |
|--|--------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0000h |

Table 7-52. DSI_TOP Registers

| Offset | Acronym | Register Name | DSS_DSI0_DSI_TOP_VBUSP_CFG_ DSI_0_DSI Physical Address |
|--------|---|---------------|--|
| 0h | DSI_IP_CONF | | 0480 0000h |
| 4h | DSI_MCTL_MAIN_DATA_CTL | | 0480 0004h |
| 8h | DSI_MCTL_MAIN_PHY_CTL | | 0480 0008h |
| Ch | DSI_MCTL_MAIN_EN | | 0480 000Ch |
| 10h | DSI_MCTL_DPHY_CFG0 | | 0480 0010h |
| 14h | DSI_MCTL_DPHY_TIMEOUT1 | | 0480 0014h |
| 18h | DSI_MCTL_DPHY_TIMEOUT2 | | 0480 0018h |
| 1Ch | DSI_MCTL_ULPOUT_TIME | | 0480 001Ch |
| 20h | DSI_MCTL_3DVIDEO_CTL | | 0480 0020h |
| 24h | DSI_MCTL_MAIN_STS | | 0480 0024h |
| 28h | DSI_MCTL_DPHY_ERR | | 0480 0028h |
| 2Ch | DSI_MCTL_LANE_STS | | 0480 002Ch |
| 30h | DSI_DSC_MODE_CTL | | 0480 0030h |
| 34h | DSI_DSC_CMD_SEND | | 0480 0034h |
| 38h | DSI_DSC_PPS_WRDAT | | 0480 0038h |
| 3Ch | DSI_DSC_MODE_STS | | 0480 003Ch |
| 40h | DSI_MCTL_DPHY_SKEWCAL_TIMEOUT | | 0480 0040h |
| 70h | DSI_CMD_MODE_CTL | | 0480 0070h |
| 74h | DSI_CMD_MODE_CTL2 | | 0480 0074h |
| 78h | DSI_CMD_MODE_STS | | 0480 0078h |
| 80h | DSI_DIRECT_CMD_SEND | | 0480 0080h |
| 84h | DSI_DIRECT_CMD_MAIN_SETTINGS | | 0480 0084h |
| 88h | DSI_DIRECT_CMD_STS | | 0480 0088h |
| 8Ch | DSI_DIRECT_CMD_RD_INIT | | 0480 008Ch |
| 90h | DSI_DIRECT_CMD_WRDAT | | 0480 0090h |
| 94h | DSI_DIRECT_CMD_FIFO_RST | | 0480 0094h |
| A0h | DSI_DIRECT_CMD_RDDAT | | 0480 00A0h |
| A4h | DSI_DIRECT_CMD_RD_PROPERTY | | 0480 00A4h |
| A8h | DSI_DIRECT_CMD_RD_STS | | 0480 00A8h |
| B0h | DSI_VID_MAIN_CTL | | 0480 00B0h |
| B4h | DSI_VID_VSIZE1 | | 0480 00B4h |
| B8h | DSI_VID_VSIZE2 | | 0480 00B8h |
| C0h | DSI_VID_HSIZE1 | | 0480 00C0h |
| C4h | DSI_VID_HSIZE2 | | 0480 00C4h |
| CCh | DSI_VID_BLKSIZE1 | | 0480 00CCh |
| D0h | DSI_VID_BLKSIZE2 | | 0480 00D0h |

Table 7-52. DSI_TOP Registers (continued)

| Offset | Acronym | Register Name | DSS_DSI0_DSI_TOP_VBUSP_CFG_ DSI_0_DSI Physical Address |
|--------|--|---------------|--|
| D8h | DSI_VID_PCK_TIME | | 0480 00D8h |
| DCh | DSI_VID_DPHY_TIME | | 0480 00DCh |
| E0h | DSI_VID_ERR_COLOR1 | | 0480 00E0h |
| E4h | DSI_VID_ERR_COLOR2 | | 0480 00E4h |
| E8h | DSI_VID_VPOS | | 0480 00E8h |
| ECh | DSI_VID_HPOS | | 0480 00ECh |
| F0h | DSI_VID_MODE_STS | | 0480 00F0h |
| F4h | DSI_VID_VCA_SETTING1 | | 0480 00F4h |
| F8h | DSI_VID_VCA_SETTING2 | | 0480 00F8h |
| FCh | DSI_TVG_CTL | | 0480 00FCh |
| 100h | DSI_TVG_IMG_SIZE | | 0480 0100h |
| 104h | DSI_TVG_COLOR1 | | 0480 0104h |
| 108h | DSI_TVG_COLOR1_BIS | | 0480 0108h |
| 10Ch | DSI_TVG_COLOR2 | | 0480 010Ch |
| 110h | DSI_TVG_COLOR2_BIS | | 0480 0110h |
| 114h | DSI_TVG_STS | | 0480 0114h |
| 130h | DSI_MCTL_MAIN_STS_CTL | | 0480 0130h |
| 134h | DSI_CMD_MODE_STS_CTL | | 0480 0134h |
| 138h | DSI_DIRECT_CMD_STS_CTL | | 0480 0138h |
| 13Ch | DSI_DIRECT_CMD_RD_STS_CTL | | 0480 013Ch |
| 140h | DSI_VID_MODE_STS_CTL | | 0480 0140h |
| 144h | DSI_TVG_STS_CTL | | 0480 0144h |
| 148h | DSI_MCTL_DPHY_ERR_CTL1 | | 0480 0148h |
| 14Ch | DSI_MCTL_DPHY_ERR_CTL2 | | 0480 014Ch |
| 150h | DSI_MCTL_MAIN_STS_CLR | | 0480 0150h |
| 154h | DSI_CMD_MODE_STS_CLR | | 0480 0154h |
| 158h | DSI_DIRECT_CMD_STS_CLR | | 0480 0158h |
| 15Ch | DSI_DIRECT_CMD_RD_STS_CLR | | 0480 015Ch |
| 160h | DSI_VID_MODE_STS_CLR | | 0480 0160h |
| 164h | DSI_TG_STS_CLR | | 0480 0164h |
| 168h | DSI_MCTL_DPHY_ERR_CLR | | 0480 0168h |
| 170h | DSI_MCTL_MAIN_STS_FLAG | | 0480 0170h |
| 174h | DSI_CMD_MODE_STS_FLAG | | 0480 0174h |
| 178h | DSI_DIRECT_CMD_STS_FLAG | | 0480 0178h |
| 17Ch | DSI_DIRECT_CMD_RD_STS_FLAG | | 0480 017Ch |
| 180h | DSI_VID_MODE_STS_FLAG | | 0480 0180h |
| 184h | DSI_TG_STS_FLAG | | 0480 0184h |
| 188h | DSI_MCTL_DPHY_ERR_FLAG | | 0480 0188h |
| 1A0h | DSI_DPI_IRQ_EN | | 0480 01A0h |
| 1A4h | DSI_DPI_IRQ_CLR | | 0480 01A4h |
| 1A8h | DSI_DPI_IRQ_STS | | 0480 01A8h |
| 1ACh | DSI_DPI_CFG | | 0480 01ACh |
| 1F0h | DSI_TEST_GENERIC | | 0480 01F0h |
| 1FCh | DSI_ID_REG | | 0480 01FCh |
| 200h | DSI_ASF_INT_STATUS | | 0480 0200h |

Table 7-52. DSI_TOP Registers (continued)

| Offset | Acronym | Register Name | DSS_DSI0_DSI_TOP_VBUSP_CFG_ DSI_0_DSI Physical Address |
|--------|--|---------------|--|
| 204h | DSI_ASF_INT_RAW_STATUS | | 0480 0204h |
| 208h | DSI_ASF_INT_MASK | | 0480 0208h |
| 20Ch | DSI_ASF_INT_TEST | | 0480 020Ch |
| 210h | DSI_ASF_FATAL_NONFATAL_SELECT | | 0480 0210h |
| 220h | DSI_ASF_SRAM_CORR_FAULT_STATUS | | 0480 0220h |
| 224h | DSI_ASF_SRAM_UNCORR_FAULT_STATUS | | 0480 0224h |
| 228h | DSI_ASF_SRAM_FAULT_STATS | | 0480 0228h |
| 230h | DSI_ASF_TRANS_TO_CTRL | | 0480 0230h |
| 234h | DSI_ASF_TRANS_TO_FAULT_MASK | | 0480 0234h |
| 238h | DSI_ASF_TRANS_TO_FAULT_STATUS | | 0480 0238h |
| 240h | DSI_ASF_PROTOCOL_FAULT_MASK | | 0480 0240h |
| 244h | DSI_ASF_PROTOCOL_FAULT_STATUS | | 0480 0244h |

7.2.1 DSI_IP_CONF Register (Offset = 0h) [reset = 948490D0h]

DSI_IP_CONF is shown in [Figure 7-17](#) and described in [Table 7-54](#).

Return to [Summary Table](#).

IP Configuration for Controller

Table 7-53. DSI_IP_CONF Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0000h |

Figure 7-17. DSI_IP_CONF Register

| | | | | | | | |
|-------------------|------------------|---------------|------------------------|---------------|----|------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_CONFIG | SP_HS_FIFO_DEPTH | | | | | SP_LP_FIFO_DEPTH | |
| R-1h | R-5h | | | | | R-4h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SP_LP_FIFO_DEPTH | | | VRS_FIFO_DEPTH | | | | |
| R-4h | | | R-4h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DIRCMD_FIFO_DEPTH | | | INTERFACE_D ATASIZE | DATAPATH_SIZE | | NUM_INTERFACE | |
| R-4h | | | R-1h | R-0h | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MAX_LANE_NB | | RX_FIFO_DEPTH | | | | | |
| R-3h | | R-10h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-54. DSI_IP_CONF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31 | ASF_CONFIG | R | 1h | Active Safety Features [ASF] Configuration: 0 = None 1 = Full ASF. |
| 30-26 | SP_HS_FIFO_DEPTH | R | 5h | SP_HS_FIFO_DEPTH : HS FIFO depth in sending path. |
| 25-21 | SP_LP_FIFO_DEPTH | R | 4h | SP_LP_FIFO_DEPTH : LP FIFO depth in sending path. |
| 20-16 | VRS_FIFO_DEPTH | R | 4h | VRS_FIFO_DEPTH : FIFO depth in the VRS block. |
| 15-13 | DIRCMD_FIFO_DEPTH | R | 4h | Direct Command FIFO Depth [2:0]. Depth in bytes = 2 ^[(value)+2] |
| 12 | INTERFACE_DATASIZE | R | 1h | SDI interface data width: 0 = 16 bit, 1 = 32bit |
| 11-10 | DATAPATH_SIZE | R | 0h | Internal Datapath.width 00 - 32 bit, 01 - 16bit, 11 - 8 Bits. |
| 9-8 | NUM_INTERFACE | R | 0h | Max Number of SDI interfaces [1-4] = [(value)+1] |
| 7-6 | MAX_LANE_NB | R | 3h | Max Number of Lanes [1-4] = [(value)+1] |

Table 7-54. DSI_IP_CONF Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|------------------------|
| 5-0 | RX_FIFO_DEPTH | R | 10h | RX FIFO Depth [5:0] |

7.2.2 DSI_MCTL_MAIN_DATA_CTL Register (Offset = 4h) [reset = X]

DSI_MCTL_MAIN_DATA_CTL is shown in [Figure 7-18](#) and described in [Table 7-56](#).

Return to [Summary Table](#).

Main Control - main control setting for datapath

Table 7-55. DSI_MCTL_MAIN_DATA_CTL Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0004h |

Figure 7-18. DSI_MCTL_MAIN_DATA_CTL Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------|---------|---------|-----------|---------------|------------------|--------------------|-------------------|
| RESERVED | | | | | | TE_MIPI_POLLING_EN | TE_HW_POLLING_EN |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | DISP_EOT_GEN | HOST_EOT_GEN | DISP_GEN_CHECKSUM |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DISP_GEN_ECC | BTA_EN | READ_EN | REG_TE_EN | RESERVED | SPLIT_PANEL_MODE | IF3_TE_EN | IF1_TE_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | TVG_SEL | VID_EN | RESERVED | VID_IF_SELECT | | SDI_IF_VID_MODE | LINK_EN |
| R/W-X | R/W-0h | R/W-0h | R/W-X | R/W-0h | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-56. DSI_MCTL_MAIN_DATA_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-26 | RESERVED | R/W | X | |
| 25 | TE_MIPI_POLLING_EN | R/W | 0h | TE_MIPI_POLLING_EN: enables TE Polling feature following MIPI recommendations [polling by software] |
| 24 | TE_HW_POLLING_EN | R/W | 0h | TE_HW_POLLING_EN: enables TE Polling feature following internal solution |
| 23-19 | RESERVED | R/W | X | |
| 18 | DISP_EOT_GEN | R/W | 0h | DISP_EOT_GEN: display adds an EOT packet to its LPDT transfers |
| 17 | HOST_EOT_GEN | R/W | 0h | HOST_EOT_GEN: generates or not the EOT packet after a transfer in HS. |
| 16 | DISP_GEN_CHECKSUM | R/W | 0h | DISP_GEN_CHECKSUM: display generates checksum on its response packets. |
| 15 | DISP_GEN_ECC | R/W | 0h | DISP_GEN_ECC: display generates ECC on its response packets |
| 14 | BTA_EN | R/W | 0h | BTA_EN: enables BTA |
| 13 | READ_EN | R/W | 0h | READ_EN: enables read operation |
| 12 | REG_TE_EN | R/W | 0h | REG_TE_EN: enables Tearing Effect from register |
| 11 | RESERVED | R/W | X | |

Table 7-56. DSI_MCTL_MAIN_DATA_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 10 | SPLIT_PANEL_MODE | R/W | 0h | SPLIT_PANEL_MODE: when enabled, DSC stage controls data for split panel single DPHY link |
| 9 | IF3_TE_EN | R/W | 0h | IF3_TE_EN: enables Tearing Effect on interface 3. Note TE on all SDI interfaces is not supported and should be avoided |
| 8 | IF1_TE_EN | R/W | 0h | IF1_TE_EN: enables Tearing Effect on interface 1. Note TE on all SDI interfaces is not supported and should be avoided |
| 7 | RESERVED | R/W | X | |
| 6 | TVG_SEL | R/W | 0h | TVG_SEL: Test Video Generator is enabled [it is not the start signal!] - should not be set if if1_en = 1 and if1_mode = 1 [see DSI_MCTL_MAIN_EN register] |
| 5 | VID_EN | R/W | 0h | VID_EN: enables the video stream generator |
| 4 | RESERVED | R/W | X | |
| 3-2 | VID_IF_SELECT | R/W | 0h | VID_IF_SELECT: Determines which video interface is active [00 : SDI , 01 : DPI, 10 : DSC] |
| 1 | SDI_IF_VID_MODE | R/W | 0h | SDI_IF_VID_MODE: 1: selected interface is in video mode, 0: selected interface is in command mode] |
| 0 | LINK_EN | R/W | 0h | LINK_EN: enables [or not] the link] |

7.2.3 DSI_MCTL_MAIN_PHY_CTL Register (Offset = 8h) [reset = X]

DSI_MCTL_MAIN_PHY_CTL is shown in [Figure 7-19](#) and described in [Table 7-58](#).

Return to [Summary Table](#).

Main control setting for the physical lanes and drive the static signals for D-PHY clock lane

Table 7-57. DSI_MCTL_MAIN_PHY_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0008h |

Figure 7-19. DSI_MCTL_MAIN_PHY_CTL Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------|-----------------------|---------------------|-----------------|----------------|----------------|----------------|----------------|
| RESERVED | HS_SKEWCAL_TIMEOUT_EN | HS_SKEWCAL_FORCE_EN | HS_SKEWCAL_EN | RESERVED | RESERVED | HS_INVERT_DAT4 | SWAP_PINS_DAT4 |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-X | R/W-X | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HS_INVERT_DAT3 | SWAP_PINS_DAT3 | HS_INVERT_DAT2 | SWAP_PINS_DAT2 | HS_INVERT_DAT1 | SWAP_PINS_DAT1 | HS_INVERT_CLK | SWAP_PINS_CLK |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | RESERVED | RESERVED | WAIT_BURST_TIME | RESERVED | RESERVED | DAT4_ULPM_EN | DAT3_ULPM_EN |
| R/W-X | R/W-X | R/W-X | R/W-0h | R/W-X | R/W-X | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DAT2_ULPM_EN | DAT1_ULPM_EN | CLK_ULPM_EN | CLK_CONTINUOUS | RESERVED | LANE4_EN | LANE3_EN | LANE2_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-58. DSI_MCTL_MAIN_PHY_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31 | RESERVED | R/W | X | |
| 30 | HS_SKEWCAL_TIMEOUT_EN | R/W | 0h | HS_SKEWCAL_TIMEOUT_EN: Activate the HS SkewCal Control to occur after a timeout. |
| 29 | HS_SKEWCAL_FORCE_EN | R/W | 0h | HS_SKEWCAL_FORCE_EN: Force the HS SkewCal Control to occur immediately |
| 28 | HS_SKEWCAL_EN | R/W | 0h | HS_SKEWCAL_EN: activate the HS SkewCal Control at start of HS Transmission |
| 27-26 | RESERVED | R/W | X | |
| 25 | HS_INVERT_DAT4 | R/W | 0h | HS_INVERT_DAT4: invert HS signal on data lane 4 |
| 24 | SWAP_PINS_DAT4 | R/W | 0h | SWAP_PINS_DAT4: swap pins on clock lane 4 |
| 23 | HS_INVERT_DAT3 | R/W | 0h | HS_INVERT_DAT3: invert HS signal on data lane 3 |
| 22 | SWAP_PINS_DAT3 | R/W | 0h | SWAP_PINS_DAT3: swap pins on clock lane 3 |
| 21 | HS_INVERT_DAT2 | R/W | 0h | HS_INVERT_DAT2: invert HS signal on data lane 2 |

Table 7-58. DSI_MCTL_MAIN_PHY_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 20 | SWAP_PINS_DAT2 | R/W | 0h | SWAP_PINS_DAT 2: swap pins on clock lane 2 |
| 19 | HS_INVERT_DAT1 | R/W | 0h | HS_INVERT_DAT 1: invert HS signal on data lane 1 |
| 18 | SWAP_PINS_DAT1 | R/W | 0h | SWAP_PINS_DAT 1: swap pins on data lane 1 |
| 17 | HS_INVERT_CLK | R/W | 0h | HS_INVERT_CLK: invert HS signal on clock lane |
| 16 | SWAP_PINS_CLK | R/W | 0h | SWAP_PINS_CLK: swap pins on clock lane |
| 15-14 | RESERVED | R/W | X | |
| 13-10 | WAIT_BURST_TIME | R/W | 0h | WAIT_BURST_TIME: delay to respect between two HS bursts. Value 0 is forbidden |
| 9 | DAT4_ULPM_EN | R/W | 0h | DAT4_ULPM_EN: data lane 4 can be switched in ULP mode |
| 8 | DAT3_ULPM_EN | R/W | 0h | DAT3_ULPM_EN: data lane 3 can be switched in ULP mode |
| 7 | DAT2_ULPM_EN | R/W | 0h | DAT2_ULPM_EN: data lane 2 can be switched in ULP mode |
| 6 | DAT1_ULPM_EN | R/W | 0h | DAT1_ULPM_EN: data lane 1 can be switched in ULP mode |
| 5 | CLK_ULPM_EN | R/W | 0h | CLK_ULPM_EN: specifies that clock lane can be switched in ULP mode [on demand] |
| 4 | CLK_CONTINUOUS | R/W | 0h | CLK_CONTINUOUS: clock lane should remain in HS sending mode [no return in STOP state] |
| 3 | RESERVED | R/W | X | |
| 2 | LANE4_EN | R/W | 0h | LANE4_EN: enables the fourth lane [controls DCB FSM] |
| 1 | LANE3_EN | R/W | 0h | LANE3_EN: enables the third lane [controls DCB FSM] |
| 0 | LANE2_EN | R/W | 0h | LANE2_EN: enables the second lane [controls DCB FSM] |

7.2.4 DSI_MCTL_MAIN_EN Register (Offset = Ch) [reset = X]

DSI_MCTL_MAIN_EN is shown in [Figure 7-20](#) and described in [Table 7-60](#).

Return to [Summary Table](#).

Control start/stop of the DSI link

Table 7-59. DSI_MCTL_MAIN_EN Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 000Ch |

Figure 7-20. DSI_MCTL_MAIN_EN Register

| | | | | | | | |
|----------|---------|---------|---------------|---------------|---------------|-----------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | FORCE_STOP_MODE | CLK_FORCE_STOP |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IF3_EN | IF2_EN | IF1_EN | DAT4_ULPM_REQ | DAT3_ULPM_REQ | DAT2_ULPM_REQ | DAT1_ULPM_REQ | CLKLANE_ULPM_REQ |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DAT4_EN | DAT3_EN | DAT2_EN | DAT1_EN | CKLANE_EN | RESERVED | | PLL_START |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-60. DSI_MCTL_MAIN_EN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-18 | RESERVED | R/W | X | |
| 17 | FORCE_STOP_MODE | R/W | 0h | FORCE_STOP_MODE: when enabled, data lanes are forced back in STOP mode - this value should remain asserted for 10 us minimum |
| 16 | CLK_FORCE_STOP | R/W | 0h | CLK_FORCE_STOP : force clock lanes back in STOP mode - this value should remain asserted for 10 us minimum |
| 15 | IF3_EN | R/W | 0h | IF3_EN: enables DSC interface [i.e. removes stall signal] |
| 14 | IF2_EN | R/W | 0h | IF2_EN: enables DPI interface [i.e. removes stall signal] |
| 13 | IF1_EN | R/W | 0h | IF1_EN: enables SDI interface [i.e. removes stall signal] |
| 12 | DAT4_ULPM_REQ | R/W | 0h | DAT4_ULPM_REQ: switches data lane 4 in ULP mode |
| 11 | DAT3_ULPM_REQ | R/W | 0h | DAT3_ULPM_REQ: switches data lane 3 in ULP mode |
| 10 | DAT2_ULPM_REQ | R/W | 0h | DAT2_ULPM_REQ: switches data lane 2 in ULP mode |
| 9 | DAT1_ULPM_REQ | R/W | 0h | DAT1_ULPM_REQ: switches data lane 1 in ULP mode |
| 8 | CLKLANE_ULPM_REQ | R/W | 0h | CLKLANE_ULPM_REQ: switches clock lane in ULP mode |
| 7 | DAT4_EN | R/W | 0h | DAT4_EN: 1: starts data lane 4 [FSM data lane 4 is stuck in start mode if 0] |

Table 7-60. DSI_MCTL_MAIN_EN Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 6 | DAT3_EN | R/W | 0h | DAT3_EN: 1: starts data lane 3 [FSM data lane 3 is stuck in start mode if 0] |
| 5 | DAT2_EN | R/W | 0h | DAT2_EN: 1: starts data lane 2 [FSM data lane 2 is stuck in start mode if 0] |
| 4 | DAT1_EN | R/W | 0h | DAT1_EN: 1: starts data lane 1 [FSM data lane 1 is stuck in start mode if 0] |
| 3 | CKLANE_EN | R/W | 0h | CKLANE_EN: 1: starts the clock lane |
| 2-1 | RESERVED | R/W | X | |
| 0 | PLL_START | R/W | 0h | PLL_START: enables the PLL [when set, the PLL is started] |

7.2.5 DSI_MCTL_DPHY_CFG0 Register (Offset = 10h) [reset = X]

DSI_MCTL_DPHY_CFG0 is shown in [Figure 7-21](#) and described in [Table 7-62](#).

Return to [Summary Table](#).

DPHY Power and Reset Control

Table 7-61. DSI_MCTL_DPHY_CFG0 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0010h |

Figure 7-21. DSI_MCTL_DPHY_CFG0 Register

| | | | | | | | |
|------------|----|----|-----------------|-------------|------------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | DPHY_C_RST B | DPHY_D_RSTB | | | |
| R/W-X | | | R/W-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | DPHY_PLL_PD N | DPHY_CMN_P DN | DPHY_C_PDN |
| R/W-X | | | | | R/W-1h | R/W-1h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPHY_D_PDN | | | | RESERVED | | DPHY_PLL_PS O | DPHY_CMN_P SO |
| R/W-0h | | | | R/W-X | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-62. DSI_MCTL_DPHY_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|----------------------------|
| 31-21 | RESERVED | R/W | X | |
| 20 | DPHY_C_RSTB | R/W | 0h | Drives dphy_c_rstb output |
| 19-16 | DPHY_D_RSTB | R/W | 0h | Drives dphy_d_rstb output |
| 15-11 | RESERVED | R/W | X | |
| 10 | DPHY_PLL_PDN | R/W | 1h | Drives dphy_pll_pdn output |
| 9 | DPHY_CMN_PDN | R/W | 1h | Drives dphy_cmn_pdn output |
| 8 | DPHY_C_PDN | R/W | 0h | Drives dphy_c_pdn output |
| 7-4 | DPHY_D_PDN | R/W | 0h | Drives dphy_d_pdn output |
| 3-2 | RESERVED | R/W | X | |
| 1 | DPHY_PLL_PSO | R/W | 0h | Drives dphy_pll_pso output |
| 0 | DPHY_CMN_PSO | R/W | 0h | Drives dphy_cmn_pso output |

7.2.6 DSI_MCTL_DPHY_TIMEOUT1 Register (Offset = 14h) [reset = X]

DSI_MCTL_DPHY_TIMEOUT1 is shown in [Figure 7-22](#) and described in [Table 7-64](#).

Return to [Summary Table](#).

Main DPHY time-out settings. To better understand the way this register is used, please refer to Section :
DSI checks (DC) - the counters are based on tx_byte_hs_clk and NOT on sys_clk

Table 7-63. DSI_MCTL_DPHY_TIMEOUT1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0014h |

Figure 7-22. DSI_MCTL_DPHY_TIMEOUT1 Register

| | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | HSTX_TO_VAL | | | | | |
| R/W-X | | | | | | | | | | R/W-0h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HSTX_TO_VAL | | | | | | | | | | CLK_DIV | | | | | |
| R/W-0h | | | | | | | | | | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-64. DSI_MCTL_DPHY_TIMEOUT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-22 | RESERVED | R/W | X | |
| 21-4 | HSTX_TO_VAL | R/W | 0h | HSTX_TO_VAL: HS TX time-out detection value |
| 3-0 | CLK_DIV | R/W | 0h | CLK_DIV: clock division ratio |

7.2.7 DSI_MCTL_DPHY_TIMEOUT2 Register (Offset = 18h) [reset = X]

DSI_MCTL_DPHY_TIMEOUT2 is shown in [Figure 7-23](#) and described in [Table 7-66](#).

Return to [Summary Table](#).

To better understand the way this register is used, please refer to Section : DSI checks (DC) - the counters are on tx_byte_hs_clk and not on sys_clk

Table 7-65. DSI_MCTL_DPHY_TIMEOUT2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0018h |

Figure 7-23. DSI_MCTL_DPHY_TIMEOUT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | LPRX_TO_VAL | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-66. DSI_MCTL_DPHY_TIMEOUT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-18 | RESERVED | R/W | X | |
| 17-0 | LPRX_TO_VAL | R/W | 0h | LPRX_TO_VAL: LP RX time-out detection value |

7.2.8 DSI_MCTL_ULPOUT_TIME Register (Offset = 1Ch) [reset = X]

DSI_MCTL_ULPOUT_TIME is shown in [Figure 7-24](#) and described in [Table 7-68](#).

Return to [Summary Table](#).

Specify time to leave ULP mode. The time-out is reached when the ulpout counter reaches 1000x xxx_ulpout_time and is based upon the system clock

Table 7-67. DSI_MCTL_ULPOUT_TIME Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 001Ch |

Figure 7-24. DSI_MCTL_ULPOUT_TIME Register

| | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | DATA_ULPOUT_TIME | |
| R/W-X | | | | | | | | | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA_ULPOUT_TIME | | | | | | | | CKLANE_ULPOUT_TIME | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-68. DSI_MCTL_ULPOUT_TIME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-18 | RESERVED | R/W | X | |
| 17-9 | DATA_ULPOUT_TIME | R/W | 0h | DATA_ULPOUT_TIME: specify what the duration is to leave ULP mode is [for data lane[s] in system clock cycles |
| 8-0 | CKLANE_ULPOUT_TIME | R/W | 0h | CKLANE_ULPOUT_TIME: specify what the duration is to leave ULP mode is [for clock lane] in system clock cycles |

7.2.9 DSI_MCTL_3DVIDEO_CTL Register (Offset = 20h) [reset = X]

DSI_MCTL_3DVIDEO_CTL is shown in [Figure 7-25](#) and described in [Table 7-70](#).

Return to [Summary Table](#).

3D Video mode stream control

Table 7-69. DSI_MCTL_3DVIDEO_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0020h |

Figure 7-25. DSI_MCTL_3DVIDEO_CTL Register

| | | | | | | | |
|-----------------|----------|-----------------|------------------------|--------------------|----|------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VID_VSYNC_3D_EN | RESERVED | VID_VSYNC_3D_LR | VID_VSYNC_3D_SECOND_EN | VID_VSYNC_3DFORMAT | | VID_VSYNC_3DMODE | |
| R/W-0h | R/W-X | R/W-0h | R/W-1h | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-70. DSI_MCTL_3DVIDEO_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | VID_VSYNC_3D_EN | R/W | 0h | VID_VSYNC_3D_EN: Enable 3D Control this selects the 3D operation for VSYNC and video data control |
| 6 | RESERVED | R/W | X | |
| 5 | VID_VSYNC_3D_LR | R/W | 0h | VID_VSYNC_3D_LR: When 3D mode is enabled, this allows to choose which field to start the video stream '0' - Data is sent Left first then right '1' - Data is sent Right first then left |
| 4 | VID_VSYNC_3D_SECOND_EN | R/W | 1h | VID_VSYNC_3D_SECOND_EN: When 3D mode is enabled, this allows to choose if a second VSYNC is enabled between L and R images '0' - No sync pulses between left and right data '1' - Sync pulse [HSYNC, VSYNC, Blanking] between left and right image data |
| 3-2 | VID_VSYNC_3DFORMAT | R/W | 0h | VID_VSYNC_3DFORMAT: video 3D Format for VSYNC Control Parameter1 '00' - Line Format, alternating line of left and right data '01' - Frame Format, alternating frames of left and right data '10' - Pixel Format, alternating pixels of left and right data '11' - Reserved |

Table 7-70. DSI_MCTL_3DVIDEO_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 1-0 | VID_VSYNC_3DMODE | R/W | 0h | VID_VSYNC_3DMODE: video 3D mode for VSYNC Control Parameter1 '00' - 3D mode Off - 2D Mode only '01' - 3D On - Portrait Orientation '10' - 3D On - Landscape Orientation '11' - Reserved |

7.2.10 DSI_MCTL_MAIN_STS Register (Offset = 24h) [reset = X]

DSI_MCTL_MAIN_STS is shown in [Figure 7-26](#) and described in [Table 7-72](#).

Return to [Summary Table](#).

Status of the DSI link

Table 7-71. DSI_MCTL_MAIN_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0024h |

Figure 7-26. DSI_MCTL_MAIN_STS Register

| | | | | | | | |
|-------------|-------------|------------|------------|-----------------|----------------|----------------|----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | HS_SKEWCAL_DONE | IF3_UNTERM_PCK | IF2_UNTERM_PCK | IF1_UNTERM_PCK |
| R-X | | | | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LPRX_TO_ERR | HSTX_TO_ERR | DAT4_READY | DAT3_READY | DAT2_READY | DAT1_READY | CLKLANE_READY | PLL_LCK |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-72. DSI_MCTL_MAIN_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-12 | RESERVED | R | X | |
| 11 | HS_SKEWCAL_DONE | R | 0h | HS_SKEWCAL_DONE: HS SkewCal Control Done at start of HS Transmission |
| 10 | IF3_UNTERM_PCK | R | 0h | IF3_UNTERM_PCK: Indicates an unterminated packet on DSC interface |
| 9 | IF2_UNTERM_PCK | R | 0h | IF2_UNTERM_PCK: Indicates an unterminated packet on DPI interface |
| 8 | IF1_UNTERM_PCK | R | 0h | IF1_UNTERM_PCK: Indicates an unterminated packet on SDI Interface |
| 7 | LPRX_TO_ERR | R | 0h | LPRX_TO_ERR: Indicates an LP_RX time-out error |
| 6 | HSTX_TO_ERR | R | 0h | HSTX_TO_ERR: Indicates an HS_TX time-out error |
| 5 | DAT4_READY | R | 0h | DAT4_READY: Indicates data lane 4 is ready |
| 4 | DAT3_READY | R | 0h | DAT3_READY: Indicates data lane 3 is ready |
| 3 | DAT2_READY | R | 0h | DAT2_READY: Indicates data lane 2 is ready |
| 2 | DAT1_READY | R | 0h | DAT1_READY: Indicates data lane 1 is ready |
| 1 | CLKLANE_READY | R | 0h | CLKLANE_READY: Indicates the clock lane is ready [normal DSI operation can start] |

Table 7-72. DSI_MCTL_MAIN_STS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 0 | PLL_LCK | R | 0h | PLL_LCK: Indicates PLL is locked - data coming from DCB [if DSI link is PLL master] or copy of pll_en [if DSI link is slave] |

7.2.11 DSI_MCTL_DPHY_ERR Register (Offset = 28h) [reset = X]

DSI_MCTL_DPHY_ERR is shown in [Figure 7-27](#) and described in [Table 7-74](#).

Return to [Summary Table](#).

Errors reported from DPHY lanes - See description in DPHY inputs and outputs

Table 7-73. DSI_MCTL_DPHY_ERR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0028h |

Figure 7-27. DSI_MCTL_DPHY_ERR Register

| | | | | | | | |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ERR_CONT_L P1_4 | ERR_CONT_L P1_3 |
| R-X | | | | | | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_CONT_L P1_2 | ERR_CONT_L P1_1 | ERR_CONT_L P0_4 | ERR_CONT_L P0_3 | ERR_CONT_L P0_2 | ERR_CONT_L P0_1 | ERR_CONTRO L_4 | ERR_CONTRO L_3 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ERR_CONTRO L_2 | ERR_CONTRO L_1 | ERR_SYNCES C_4 | ERR_SYNCES C_3 | ERR_SYNCES C_2 | ERR_SYNCES C_1 | ERR_ESC_4 | ERR_ESC_3 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_ESC_2 | ERR_ESC_1 | RESERVED | | | | | |
| R-0h | R-0h | R-X | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-74. DSI_MCTL_DPHY_ERR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|----------------|
| 31-26 | RESERVED | R | X | |
| 25 | ERR_CONT_LP1_4 | R | 0h | ERR_CONT_LP1_4 |
| 24 | ERR_CONT_LP1_3 | R | 0h | ERR_CONT_LP1_3 |
| 23 | ERR_CONT_LP1_2 | R | 0h | ERR_CONT_LP1_2 |
| 22 | ERR_CONT_LP1_1 | R | 0h | ERR_CONT_LP1_1 |
| 21 | ERR_CONT_LP0_4 | R | 0h | ERR_CONT_LP0_4 |
| 20 | ERR_CONT_LP0_3 | R | 0h | ERR_CONT_LP0_3 |
| 19 | ERR_CONT_LP0_2 | R | 0h | ERR_CONT_LP0_2 |
| 18 | ERR_CONT_LP0_1 | R | 0h | ERR_CONT_LP0_1 |
| 17 | ERR_CONTROL_4 | R | 0h | ERR_CONTROL_4 |
| 16 | ERR_CONTROL_3 | R | 0h | ERR_CONTROL_3 |
| 15 | ERR_CONTROL_2 | R | 0h | ERR_CONTROL_2 |
| 14 | ERR_CONTROL_1 | R | 0h | ERR_CONTROL_1 |
| 13 | ERR_SYNCESC_4 | R | 0h | ERR_SYNCESC_4 |
| 12 | ERR_SYNCESC_3 | R | 0h | ERR_SYNCESC_3 |
| 11 | ERR_SYNCESC_2 | R | 0h | ERR_SYNCESC_2 |

Table 7-74. DSI_MCTL_DPHY_ERR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---------------|
| 10 | ERR_SYNCESC_1 | R | 0h | ERR_SYNCESC_1 |
| 9 | ERR_ESC_4 | R | 0h | ERR_ESC_4 |
| 8 | ERR_ESC_3 | R | 0h | ERR_ESC_3 |
| 7 | ERR_ESC_2 | R | 0h | ERR_ESC_2 |
| 6 | ERR_ESC_1 | R | 0h | ERR_ESC_1 |
| 5-0 | RESERVED | R | X | |

7.2.12 DSI_MCTL_LANE_STS Register (Offset = 2Ch) [reset = X]

DSI_MCTL_LANE_STS is shown in [Figure 7-28](#) and described in [Table 7-76](#).

Return to [Summary Table](#).

DPHY Lane and PLL status information

Table 7-75. DSI_MCTL_LANE_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 002Ch |

Figure 7-28. DSI_MCTL_LANE_STS Register

| | | | | | | | |
|--------------------|----------------|----|----------------|----------|-----------------------|-------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | PPI_C_TX_RE ADY_HS | DPHY_PLL_LO CK | RESERVED |
| R-X | | | | | R-0h | R-0h | R-X |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PPI_D_RX_ULPS_ESC | | | | RESERVED | DATLANE4_STATE | | DATLANE3_ST ATE |
| R-0h | | | | R-X | R-0h | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATLANE3_ST ATE | DATLANE2_STATE | | DATLANE1_STATE | | | CLKLANE_STATE | |
| R-0h | R-0h | | R-0h | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 7-76. DSI_MCTL_LANE_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-19 | RESERVED | R | X | |
| 18 | PPI_C_TX_READY_HS | R | 0h | Value of ppi_c_tx_ready_hs input |
| 17 | DPHY_PLL_LOCK | R | 0h | Value of dphy_pll_lock input |
| 16 | RESERVED | R | X | |
| 15-12 | PPI_D_RX_ULPS_ESC | R | 0h | Value of ppi_d_rx_ulps_esc input |
| 11 | RESERVED | R | X | |
| 10-9 | DATLANE4_STATE | R | 0h | DATLANE4_STATE: state of the data lane 4 [00: start / 01: idle / 10: write / 11: ULPM] |
| 8-7 | DATLANE3_STATE | R | 0h | DATLANE3_STATE: state of the data lane 3 [00: start / 01: idle / 10: write / 11: ULPM] |

Table 7-76. DSI_MCTL_LANE_STS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 6-5 | DATLANE2_STATE | R | 0h | DATLANE2_STATE: state of the data lane 2 [00: start / 01: idle / 10: write / 11: ULPM] |
| 4-2 | DATLANE1_STATE | R | 0h | DATLANE1_STATE: state of the data lane 1 [000: start / 001: idle / 010: write / 011: ULPM / 100: read] |
| 1-0 | CLKLANE_STATE | R | 0h | CLKLANE_STATE: state of the clock lane [00: start / 01: idle / 10: HS / 11: ULPM] |

7.2.13 DSI_DSC_MODE_CTL Register (Offset = 30h) [reset = X]

DSI_DSC_MODE_CTL is shown in [Figure 7-29](#) and described in [Table 7-78](#).

Return to [Summary Table](#).

DSC Mode Control register

Table 7-77. DSI_DSC_MODE_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0030h |

Figure 7-29. DSI_DSC_MODE_CTL Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | DSC_MODE_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-78. DSI_DSC_MODE_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--------------------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | DSC_MODE_EN | R/W | 0h | Enable DSC Mode Controls |

7.2.14 DSI_DSC_CMD_SEND Register (Offset = 34h) [reset = X]

DSI_DSC_CMD_SEND is shown in [Figure 7-30](#) and described in [Table 7-80](#).

Return to [Summary Table](#).

DSC Command Control register. Write one to perform PPS set transfer or Execute Queue commands

Table 7-79. DSI_DSC_CMD_SEND Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0034h |

Figure 7-30. DSI_DSC_CMD_SEND Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DSC_SEND_P PS | DSC_EXECUT E_QUEUE |
| W-X | | | | | | W-0h | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-80. DSI_DSC_CMD_SEND Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|---|
| 31-2 | RESERVED | W | X | |
| 1 | DSC_SEND_PPS | W | 0h | Send PPS Command and Payload to the display |
| 0 | DSC_EXECUTE_QUEUE | W | 0h | Send Execute Queue Command to Synchronise the display drivers |

7.2.15 DSI_DSC_PPS_WRDAT Register (Offset = 38h) [reset = 0h]

DSI_DSC_PPS_WRDAT is shown in [Figure 7-31](#) and described in [Table 7-82](#).

Return to [Summary Table](#).

DSC PPS Write data to outgoing FIFO Buffer, byte 0 to 3; applicable to either Write or Read commands.

Note that any writes to this register that exceed the programmed command payload size or the configured FIFO depth (whichever is smaller) will be ignored.

Conversely, if the writes to this register are less than the programmed command payload size when the instruction to send the payload is given, the command payload

will contain data from the previous contents of the FIFO for all unwritten bytes, and will therefore be corrupt.

Table 7-81. DSI_DSC_PPS_WRDAT Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0038h |

Figure 7-31. DSI_DSC_PPS_WRDAT Register

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PPS_WRDAT3 | | | | | | | | PPS_WRDAT2 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPS_WRDAT1 | | | | | | | | PPS_WRDAT0 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-82. DSI_DSC_PPS_WRDAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-24 | PPS_WRDAT3 | R/W | 0h | WRDAT 3: 4th byte to be sent as part of PPS payload [stored in a FIFO] |
| 23-16 | PPS_WRDAT2 | R/W | 0h | WRDAT 2: 3rd byte to be sent as part of PPS payload [stored in a FIFO] |
| 15-8 | PPS_WRDAT1 | R/W | 0h | WRDAT 1: 2nd byte to be sent as part of PPS payload [stored in a FIFO] |
| 7-0 | PPS_WRDAT0 | R/W | 0h | WRDAT 0: 1st byte to be sent as part of PPS payload [stored in a FIFO] |

7.2.16 DSI_DSC_MODE_STS Register (Offset = 3Ch) [reset = X]

DSI_DSC_MODE_STS is shown in [Figure 7-32](#) and described in [Table 7-84](#).

Return to [Summary Table](#).

DSC Event Status Register

Table 7-83. DSI_DSC_MODE_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 003Ch |

Figure 7-32. DSI_DSC_MODE_STS Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DSC_PPS_DONE | DSC_EXEC_DONE |
| R-X | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-84. DSI_DSC_MODE_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--------------------------|
| 31-2 | RESERVED | R | X | |
| 1 | DSC_PPS_DONE | R | 0h | DSC PPS Command Sent |
| 0 | DSC_EXEC_DONE | R | 0h | DSC Execute Command Sent |

7.2.17 DSI_MCTL_DPHY_SKEWCAL_TIMEOUT Register (Offset = 40h) [reset = 0h]

DSI_MCTL_DPHY_SKEWCAL_TIMEOUT is shown in [Figure 7-33](#) and described in [Table 7-86](#).

Return to [Summary Table](#).

Used in conjunction with HS_SKEWCAL_TIMEOUT_EN from DSI_MCTL_MAIN_PHY_CTL to control periodic skew calibration

Table 7-85. DSI_MCTL_DPHY_SKEWCAL_TIMEOUT Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0040h |

Figure 7-33. DSI_MCTL_DPHY_SKEWCAL_TIMEOUT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SKEWCAL_TO_VAL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-86. DSI_MCTL_DPHY_SKEWCAL_TIMEOUT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------------------------|
| 31-0 | SKEWCAL_TO_VAL | R/W | 0h | SKEWCAL_TO_VAL: Timeout value |

7.2.18 DSI_CMD_MODE_CTL Register (Offset = 70h) [reset = X]

DSI_CMD_MODE_CTL is shown in [Figure 7-34](#) and described in [Table 7-88](#).

Return to [Summary Table](#).

Command mode control

Table 7-87. DSI_CMD_MODE_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0070h |

Figure 7-34. DSI_CMD_MODE_CTL Register

| | | | | | | | |
|----------|----|----|----|--------|-----------|-----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | IF3_LP_EN | IF1_LP_EN | RESERVED |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-X |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | IF3_ID | | IF1_ID | |
| R/W-X | | | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-88. DSI_CMD_MODE_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 31-11 | RESERVED | R/W | X | |
| 10 | IF3_LP_EN | R/W | 0h | IF3_LP_EN: enable to send command from DSC interface in LP if possible |
| 9 | IF1_LP_EN | R/W | 0h | IF1_LP_EN: enable to send command from SDI interface in LP if possible |
| 8-4 | RESERVED | R/W | X | |
| 3-2 | IF3_ID | R/W | 0h | IF3_ID: Virtual Channel ID of request from DSC interface command |
| 1-0 | IF1_ID | R/W | 0h | IF1_ID: Virtual Channel ID of request from SDI interface command |

7.2.19 DSI_CMD_MODE_CTL2 Register (Offset = 74h) [reset = X]

DSI_CMD_MODE_CTL2 is shown in [Figure 7-35](#) and described in [Table 7-90](#).

Return to [Summary Table](#).

Command mode control

Table 7-89. DSI_CMD_MODE_CTL2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0074h |

Figure 7-35. DSI_CMD_MODE_CTL2 Register

| | | | | | | | |
|------------|------------|----|----|----|-----------|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | TE_TIMEOUT | | | | | | |
| R/W-X | R/W-FFFh | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TE_TIMEOUT | | | | | FIL_VALUE | | |
| R/W-FFFh | | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIL_VALUE | | | | | ARB_PRI | | ARB_MODE |
| R/W-0h | | | | | R/W-0h | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-90. DSI_CMD_MODE_CTL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-23 | RESERVED | R/W | X | |
| 22-11 | TE_TIMEOUT | R/W | FFFh | TE_TIMEOUT : on TE request - length of TE response window before timeout. |
| 10-3 | FIL_VALUE | R/W | 0h | FIL_VALUE: value to use to fill packet during data underrun or to complete unterminated packet [referred as padding value] |
| 2-1 | ARB_PRI | R/W | 0h | ARB_PRI: in fixed mode, specify interface with higher priority SDI 01, DSC 10 |
| 0 | ARB_MODE | R/W | 0h | ARB_MODE: arbitration mode [1: round robin, 0: fixed] |

7.2.20 DSI_CMD_MODE_STS Register (Offset = 78h) [reset = X]

DSI_CMD_MODE_STS is shown in [Figure 7-36](#) and described in [Table 7-92](#).

Return to [Summary Table](#).

Command Mode status

Table 7-91. DSI_CMD_MODE_STS Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0078h |

Figure 7-36. DSI_CMD_MODE_STS Register

| | | | | | | | |
|----------|----|----|----------------------|---------------------|-------------|-----------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ERR_IF1_UNDE RRUN | ERR_UNWANT ED_RD | ERR_TE_MISS | ERR_NO_TE | CSM_RUNNIN G |
| R-X | | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-92. DSI_CMD_MODE_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-5 | RESERVED | R | X | |
| 4 | ERR_IF1_UNDEERRUN | R | 0h | ERR_IF1_UNDEERRUN: Indicates a data shortage occurs on IF1 |
| 3 | ERR_UNWANTED_RD | R | 0h | ERR_UNWANTED_RD: Indicates a read request was received while read capability was not enabled |
| 2 | ERR_TE_MISS | R | 0h | ERR_TE_MISS: error: TE window time-out |
| 1 | ERR_NO_TE | R | 0h | ERR_NO_TE: error: no TE generated by display |
| 0 | CSM_RUNNING | R | 0h | CSM_RUNNING: Indicates CSM is running - command[s] are being proceeded |

7.2.21 DSI_DIRECT_CMD_SEND Register (Offset = 80h) [reset = 0h]

DSI_DIRECT_CMD_SEND is shown in [Figure 7-37](#) and described in [Table 7-94](#).

Return to [Summary Table](#).

DSI_DIRECT_CMD_SEND is not a real register. When this address is written (whatever its value is), it signals to the link that a direct command has to be sent.

It is then a write only register. No specific mechanism is implemented to prevent the application sending two direct commands back-to-back. It is then applications responsibility to verify the completion of a first direct command before starting another direct command. Interlacing of command or video with direct command is managed by the DSI link using the different arbiters (see Command and register arbiter (CRA) and Video/command arbiter (VCA))

Table 7-93. DSI_DIRECT_CMD_SEND Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0080h |

Figure 7-37. DSI_DIRECT_CMD_SEND Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIRECT_CMD_SEND | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 7-94. DSI_DIRECT_CMD_SEND Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-0 | DIRECT_CMD_SEND | W | 0h | Initiate the direct command send operation |

7.2.22 DSI_DIRECT_CMD_MAIN_SETTINGS Register (Offset = 84h) [reset = X]

DSI_DIRECT_CMD_MAIN_SETTINGS is shown in [Figure 7-38](#) and described in [Table 7-96](#).

Return to [Summary Table](#).

Main control of the Direct Command function.

**Table 7-95. DSI_DIRECT_CMD_MAIN_SETTINGS
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0084h |

Figure 7-38. DSI_DIRECT_CMD_MAIN_SETTINGS Register

| | | | | | | | |
|----------|----|----------|----|----------------------|----|---------|-----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | TRIGGER_VAL | | | CMD_LP_EN |
| R/W-X | | | | R/W-0h | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMD_SIZE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMD_ID | | CMD_HEAD | | | | | |
| R/W-0h | | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | CMD_LONGNO TSHORT | | CMD_NAT | |
| R/W-X | | | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-96. DSI_DIRECT_CMD_MAIN_SETTINGS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-29 | RESERVED | R/W | X | |
| 28-25 | TRIGGER_VAL | R/W | 0h | TRIGGER_VAL: trigger value if trigger request [see Note about trigger mapping] - signal is one hot encoding [only one bit out of the 4 should be set to 1]. |
| 24 | CMD_LP_EN | R/W | 0h | CMD_LP_EN: enables LP sending for the command request |
| 23-16 | CMD_SIZE | R/W | 0h | CMD_SIZE: size, in bytes, of the command payload. Note that the value written here by software should comply with certain limits. For write operations, any value written which is larger than the FIFO depth [direct_cmd_fifodepth parameter] will be ignored and the command payload will be truncated to the maximum FIFO depth. For read operations, any value written which is larger than 2 bytes will be ignored and the command payload will be truncated to 2 bytes. |
| 15-14 | CMD_ID | R/W | 0h | CMD_ID: For a read/write command, Virtual Channel of the command |
| 13-8 | CMD_HEAD | R/W | 0h | CMD_HEAD: For a read/write command, datatype of the command |
| 7-4 | RESERVED | R/W | X | |

Table 7-96. DSI_DIRECT_CMD_MAIN_SETTINGS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 3 | CMD_LONGNOTSHORT | R/W | 0h | CMD_LONGNOTSHORT: Tie this to '1' if a long packet has to be generated. |
| 2-0 | CMD_NAT | R/W | 0h | CMD_NAT: Type of the direct command: 000: write command 001: read command 100: TE request 101: trigger request 110: BTA request |

7.2.23 DSI_DIRECT_CMD_STS Register (Offset = 88h) [reset = X]

DSI_DIRECT_CMD_STS is shown in [Figure 7-39](#) and described in [Table 7-98](#).

Return to [Summary Table](#).

Direct Command Status: To ensure that the observed status bits are coherent and applicable to the last command message sent, it is recommended to clear this register between accesses by writing to direct_cmd_clr, otherwise the status of the different commands is logically ORed, making it difficult to differentiate between the status of each message.

Table 7-97. DSI_DIRECT_CMD_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0088h |

Figure 7-39. DSI_DIRECT_CMD_STS Register

| | | | | | | | |
|-------------|----------------------|---------------------------|------------------|--------------------|---------------------------------|---------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ACK_VAL | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ACK_VAL | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | TRIGGER_VAL | | | | READ_COMPL ETED_WITH_E RR | BTA_FINISHED | BTA_COMPLE TED |
| R-X | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TE_RECEIVED | TRIGGER_REC EIVED | ACK_WITH_ER R_RECEIVED | ACK_RECEIVE D | READ_COMPL ETED | TRIGGER_CO MPLETED | WRITE_COMP LETED | CMD_TRANSM ISSION |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-98. DSI_DIRECT_CMD_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 31-16 | ACK_VAL | R | 0h | ACK_VAL: if an acknowledge with error has been received, this field reports its value |
| 15 | RESERVED | R | X | |
| 14-11 | TRIGGER_VAL | R | 0h | TRIGGER_VAL: if a trigger has been received, this field reports its value - refer to Note regarding trigger mapping |
| 10 | READ_COMPLETED_WI TH_ERR | R | 0h | READ_COMPLETED_WITH_ERR: read command terminated with error |
| 9 | BTA_FINISHED | R | 0h | BTA_FINISHED: DSI link recovered link master role after a BTA request |
| 8 | BTA_COMPLETED | R | 0h | BTA_COMPLETED: indicates that BTA request completed |
| 7 | TE_RECEIVED | R | 0h | TE_RECEIVED: TE received |
| 6 | TRIGGER_RECEIVED | R | 0h | TRIGGER_RECEIVED: If command with BTA, this bit is set if an trigger was received |
| 5 | ACK_WITH_ERR_RECEI VED | R | 0h | ACKNOWLEDGE_WITH_ERR_RECEIVED: If command with BTA, this bit is set if an acknowledge with error was received |

Table 7-98. DSI_DIRECT_CMD_STS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 4 | ACK_RECEIVED | R | 0h | ACKNOWLEDGE_RECEIVED: If command with BTA, this bit is set if an acknowledge with no error was received |
| 3 | READ_COMPLETED | R | 0h | READ_COMPLETED: read command request completed |
| 2 | TRIGGER_COMPLETED | R | 0h | TRIGGER_COMPLETED: trigger command request completed |
| 1 | WRITE_COMPLETED | R | 0h | WRITE_COMPLETED: write command request completed |
| 0 | CMD_TRANSMISSION | R | 0h | CMD_TRANSMISSION: a command is being sent |

7.2.24 DSI_DIRECT_CMD_RD_INIT Register (Offset = 8Ch) [reset = 0h]

DSI_DIRECT_CMD_RD_INIT is shown in [Figure 7-40](#) and described in [Table 7-100](#).

Return to [Summary Table](#).

This register is not a real register - when written it stops the read command process by emptying the FIFO and by stopping the reception of the data (RP does not consider the data that it receives and the system waits for the D-PHY to return to Tx STOP state).

Table 7-99. DSI_DIRECT_CMD_RD_INIT Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 008Ch |

Figure 7-40. DSI_DIRECT_CMD_RD_INIT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STOP_READ_OPERATION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 7-100. DSI_DIRECT_CMD_RD_INIT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---------------------|
| 31-0 | STOP_READ_OPERATION | W | 0h | Stop Read Operation |

7.2.25 DSI_DIRECT_CMD_WRDAT Register (Offset = 90h) [reset = 0h]

DSI_DIRECT_CMD_WRDAT is shown in [Figure 7-41](#) and described in [Table 7-102](#).

Return to [Summary Table](#).

Write data to outgoing Direct Command FIFO, byte 0 to 3; applicable to either Write or Read commands. Note that any writes to this register that exceed the programmed command payload size or the configured FIFO depth (whichever is smaller) will be ignored. Conversely, if the writes to this register are less than the programmed command payload size when the instruction to send the payload is given, the command payload will contain data from the previous contents of the FIFO for all unwritten bytes, and will therefore be corrupt. Note also that values written to the FIFO which are intended for transmission of single parameter write transaction must set the MS bytes to zero to comply with DSI standard requirements.

Table 7-101. DSI_DIRECT_CMD_WRDAT Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0090h |

Figure 7-41. DSI_DIRECT_CMD_WRDAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WRDAT3 | | | | | | | | WRDAT2 | | | | | | | | WRDAT1 | | | | | | | | WRDAT0 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-102. DSI_DIRECT_CMD_WRDAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|--|
| 31-24 | WRDAT3 | R/W | 0h | WRDAT 3: 4th byte to be sent as part of Direct Command [stored in a FIFO] |
| 23-16 | WRDAT2 | R/W | 0h | WRDAT 2: 3rd byte to be sent as part of Direct Command [stored in a FIFO] |
| 15-8 | WRDAT1 | R/W | 0h | WRDAT 1: 2nd byte to be sent as part of Direct Command [stored in a FIFO] |
| 7-0 | WRDAT0 | R/W | 0h | WRDAT 0: 1st byte to be sent as part of Direct Command [stored in a FIFO] |

7.2.26 DSI_DIRECT_CMD_FIFO_RST Register (Offset = 94h) [reset = 0h]

DSI_DIRECT_CMD_FIFO_RST is shown in [Figure 7-42](#) and described in [Table 7-104](#).

Return to [Summary Table](#).

Reset the write FIFO. This register is not a real register - when written it reset the FIFO pointer

**Table 7-103. DSI_DIRECT_CMD_FIFO_RST
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0094h |

Figure 7-42. DSI_DIRECT_CMD_FIFO_RST Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMD_FIFO_RST | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 7-104. DSI_DIRECT_CMD_FIFO_RST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---------------------------|
| 31-0 | CMD_FIFO_RST | W | 0h | Direct Command FIFO Reset |

7.2.27 DSI_DIRECT_CMD_RDDAT Register (Offset = A0h) [reset = 0h]

DSI_DIRECT_CMD_RDDAT is shown in [Figure 7-43](#) and described in [Table 7-106](#).

Return to [Summary Table](#).

Data from incoming Direct Command receive path, byte 0 to 3.

NOTE: SW must mask any bytes which are in excess of the actual message size (e.g. for a 2-byte message payload, take data from bytes [1:0] and mask off bytes [3:2])

Table 7-105. DSI_DIRECT_CMD_RDDAT Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00A0h |

Figure 7-43. DSI_DIRECT_CMD_RDDAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RDDAT3 | | | | | | | | RDDAT2 | | | | | | | | RDDAT1 | | | | | | | | RDDAT0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-106. DSI_DIRECT_CMD_RDDAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|--|
| 31-24 | RDDAT3 | R | 0h | RDDAT 3: 4th byte from incoming Direct Command receive path |
| 23-16 | RDDAT2 | R | 0h | RDDAT 2: 3rd byte from incoming Direct Command receive path |
| 15-8 | RDDAT1 | R | 0h | RDDAT 1: 2nd byte from incoming Direct Command receive path |
| 7-0 | RDDAT0 | R | 0h | RDDAT 0: 1st byte from incoming Direct Command receive path |

7.2.28 DSI_DIRECT_CMD_RD_PROPERTY Register (Offset = A4h) [reset = X]

DSI_DIRECT_CMD_RD_PROPERTY is shown in [Figure 7-44](#) and described in [Table 7-108](#).

Return to [Summary Table](#).

read command characteristics

**Table 7-107. DSI_DIRECT_CMD_RD_PROPERTY
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00A4h |

Figure 7-44. DSI_DIRECT_CMD_RD_PROPERTY Register

| | | | | | | | |
|----------|----|----|----|----|----------------------|-------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | RD_DCSNOTG ENERIC | RD_ID | |
| R-X | | | | | R-0h | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SIZE | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RD_SIZE | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-108. DSI_DIRECT_CMD_RD_PROPERTY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-19 | RESERVED | R | X | |
| 18 | RD_DCSNOTGENERIC | R | 0h | RD_DCSNOTGENERIC: Type of read command [DCS or generic] |
| 17-16 | RD_ID | R | 0h | RD_ID: Virtual channel of the read received |
| 15-0 | RD_SIZE | R | 0h | RD_SIZE: Size of the read data received |

7.2.29 DSI_DIRECT_CMD_RD_STS Register (Offset = A8h) [reset = X]

DSI_DIRECT_CMD_RD_STS is shown in [Figure 7-45](#) and described in [Table 7-110](#).

Return to [Summary Table](#).

Status of the read command received. It is recommended to clear DSI_DIRECT_CMD_RD_STS between two direct commands (at least between 2 read) in order to see coherent status

Table 7-109. DSI_DIRECT_CMD_RD_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00A8h |

Figure 7-45. DSI_DIRECT_CMD_RD_STS Register

| | | | | | | | |
|---------------------|----------------------|------------------|-------------|---------------------|------------------|-----------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ERR_EOT_WIT H_ERR |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_MISSING _EOT | ERR_WRONG_ LENGTH | ERR_OVERSIZ E | ERR_RECEIVE | ERR_UNDECO DABLE | ERR_CHECKS UM | ERR_UNCORR ECTABLE | ERR_FIXED |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-110. DSI_DIRECT_CMD_RD_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-9 | RESERVED | R | X | |
| 8 | ERR_EOT_WITH_ERR | R | 0h | ERR_EOT_WITH_ERR: EOT received with error |
| 7 | ERR_MISSING_EOT | R | 0h | ERR_MISSING_EOT: EOT requested but not received |
| 6 | ERR_WRONG_LENGTH | R | 0h | ERR_WRONG_LENGTH : length error has been detected. This error indicates that a packet has been received which was shorter than the expected length [longer packets than expected will result in ERR_RECEIVE field being set, as it is difficult to distinguish the extra information from other types of reception errors]. |
| 5 | ERR_OVERSIZE | R | 0h | ERR_OVERSIZE : packet size exceeds maximum |
| 4 | ERR_RECEIVE | R | 0h | ERR_RECEIVE : received packet not complete. This is a general error flag indicated that packet reception did not complete for some reason. Example conditions: signalling errors [e.g. unexpected change in PPI direction signal] longer packet received than expected. |
| 3 | ERR_UNDECODABLE | R | 0h | ERR_UNDECODABLE : command opcode not understood |
| 2 | ERR_CHECKSUM | R | 0h | ERR_CHECKSUM: error[s] detected by checksum |
| 1 | ERR_UNCORRECTABLE | R | 0h | ERR_UNCORRECTABLE : more than 1 error detected by ECC |

Table 7-110. DSI_DIRECT_CMD_RD_STS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 0 | ERR_FIXED | R | 0h | ERR_FIXED : one error detected and fixed by ECC |

7.2.30 DSI_VID_MAIN_CTL Register (Offset = B0h) [reset = X]

DSI_VID_MAIN_CTL is shown in [Figure 7-46](#) and described in [Table 7-112](#).

Return to [Summary Table](#).

Video mode main control

Table 7-111. DSI_VID_MAIN_CTL Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 00B0h |

Figure 7-46. DSI_VID_MAIN_CTL Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|------------------|--------|-----------------------|-------------------|---------------|----------------|-----------------|
| VID_IGNORE_MISS_VSYNC | RESERVED | | | | RECOVERY_MODE | | REG_BLKEOL_MODE |
| R/W-1h | R/W-X | | | | R/W-0h | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REG_BLKEOL_MODE | REG_BLKLINE_MODE | | SYNC_PULSE_HORIZONTAL | SYNC_PULSE_ACTIVE | BURST_MODE | VID_PIXEL_MODE | |
| R/W-0h | R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VID_PIXEL_MODE | | HEADER | | | | | |
| R/W-0h | | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | VID_ID | | STOP_MODE | | START_MODE | |
| R/W-X | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-112. DSI_VID_MAIN_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31 | VID_IGNORE_MISS_VSYNC | R/W | 1h | VID_IGNORE_MISSING_SYNC: When mode is enabled, this allows the video stream to go to IDLE during VFP and wait for new VSYNC without link failing to recovery |
| 30-27 | RESERVED | R/W | X | |
| 26-25 | RECOVERY_MODE | R/W | 0h | RECOVERY_MODE: specify recovery mode |
| 24-23 | REG_BLKEOL_MODE | R/W | 0h | REG_BLKEOL_MODE: behavior during end of line in burst mode - same coding as reg_blkline_mode |
| 22-21 | REG_BLKLINE_MODE | R/W | 0h | REG_BLKLINE_MODE : behavior during blanking time [1x: LP, 01: blanking packet - 00: NULL packet] |
| 20 | SYNC_PULSE_HORIZONTAL | R/W | 0h | SYNC_PULSE_HORIZONTAL: syncs are pulse [1] or event [0] all the time [DSI protocol v1.00..._r6 and later] - to be set only when sync_pulse_active = 1 |
| 19 | SYNC_PULSE_ACTIVE | R/W | 0h | SYNC_PULSE_ACTIVE: syncs are pulse [1] or event [0] during active area [DSI protocol v1.00..._r3 and before] |
| 18 | BURST_MODE | R/W | 0h | BURST_MODE: signals if system works in burst mode or not |

Table 7-112. DSI_VID_MAIN_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 17-14 | VID_PIXEL_MODE | R/W | 0h | VID_PIXEL_MODE: 0000: 16 bits RGB - 0001: 18 bits RGB 0010: 18 bits RGB[loose] - 0011: 24 bits RGB 0100: 30 bits RGB - 0101: 36 bits RGB 1000: 12 bits YCbCr - 1001: 16 bits YCbCr 1010: 20 bits YCbCr - 1011: 24 bits YCbCr 1100: DSC Compressed |
| 13-8 | HEADER | R/W | 0h | HEADER : specify the datatype of RGB packets |
| 7-6 | RESERVED | R/W | X | |
| 5-4 | VID_ID | R/W | 0h | VID_ID : specify the Virtual Channel Identifier of the video packets |
| 3-2 | STOP_MODE | R/W | 0h | STOP_MODE : video stop point [see description in Video Stream Generator [VSG] section] .[The configurations where the frame stops at the end of any line and at the end of the last active line - start_mode in [1 2] - are being deprecated, thus not verified anymore] |
| 1-0 | START_MODE | R/W | 0h | START_MODE: video entry point [see description in Video Stream Generator [VSG] section][The configuration where the frame starts with a VFP - start_mode= 1 - is being deprecated, thus not verified anymore] |

7.2.31 DSI_VID_VSIZE1 Register (Offset = B4h) [reset = X]

DSI_VID_VSIZE1 is shown in [Figure 7-47](#) and described in [Table 7-114](#).

[Return to Summary Table.](#)

Image vertical Sync and Blanking settings

Table 7-113. DSI_VID_VSIZE1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00B4h |

Figure 7-47. DSI_VID_VSIZE1 Register

| | | | | | | | | | | | | | | | |
|------------|----|----|----|------------|----|----|----|----|----|------------|----|------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | VFP_LENGTH | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VFP_LENGTH | | | | VBP_LENGTH | | | | | | VSA_LENGTH | | | | | |
| R/W-0h | | | | R/W-0h | | | | | | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-114. DSI_VID_VSIZE1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19-12 | VFP_LENGTH | R/W | 0h | VFP_LENGTH: length of the VFP [in lines] |
| 11-6 | VBP_LENGTH | R/W | 0h | VBP_LENGTH: length of the VBP [in lines] |
| 5-0 | VSA_LENGTH | R/W | 0h | VSA_LENGTH: duration of the VSYNC pulse [in lines] |

7.2.32 DSI_VID_VSIZE2 Register (Offset = B8h) [reset = X]

DSI_VID_VSIZE2 is shown in [Figure 7-48](#) and described in [Table 7-116](#).

Return to [Summary Table](#).

Image vertical active line setting

Table 7-115. DSI_VID_VSIZE2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00B8h |

Figure 7-48. DSI_VID_VSIZE2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | VACT_LENGTH | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-116. DSI_VID_VSIZE2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-13 | RESERVED | R/W | X | |
| 12-0 | VACT_LENGTH | R/W | 0h | VACT_LENGTH: vertical length of active area [in line] |

7.2.33 DSI_VID_HSIZE1 Register (Offset = C0h) [reset = X]

DSI_VID_HSIZE1 is shown in [Figure 7-49](#) and described in [Table 7-118](#).

Return to [Summary Table](#).

Image horizontal sync and Blanking setting

Active line Pulse Mode:

|__hsync__|__hbp__|__hact__|__hfp__|
|_HSS_HSA_HSE_|_HDR_HBP_CRC_|_HDR_HACT_CRC_|
HDR_HFP_CRC_|_HSS_|

Active line Event Mode:

|__hsync__|__hbp__|__hact__|__hfp__|
|_HSS_|_HDR_HSA+HBP_CRC_|_HDR_HACT_CRC_|
HDR_HFP_CRC_|_HSS_|

Table 7-117. DSI_VID_HSIZE1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00C0h |

Figure 7-49. DSI_VID_HSIZE1 Register

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HBP_LENGTH | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | HSA_LENGTH | | | | | | | | | |
| R/W-X | | | | | | R/W-0h | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-118. DSI_VID_HSIZE1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | HBP_LENGTH | R/W | 0h | HBP_LENGTH: length of HBP [in bytes] - if 0, HBP packet is sent with 0 payload |
| 15-10 | RESERVED | R/W | X | |
| 9-0 | HSA_LENGTH | R/W | 0h | HSA_LENGTH: duration of HSYNC pulse [in bytes] |

7.2.34 DSI_VID_HSIZE2 Register (Offset = C4h) [reset = X]

DSI_VID_HSIZE2 is shown in [Figure 7-50](#) and described in [Table 7-120](#).

Return to [Summary Table](#).

Image horizontal byte size setting

Table 7-119. DSI_VID_HSIZE2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00C4h |

Figure 7-50. DSI_VID_HSIZE2 Register

| | | | | | | | |
|------------|----------|----|----|----|------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | HFP_LENGTH | | |
| R/W-X | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HFP_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | RGB_SIZE | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RGB_SIZE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-120. DSI_VID_HSIZE2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-27 | RESERVED | R/W | X | |
| 26-16 | HFP_LENGTH | R/W | 0h | HFP_LENGTH: length of HFP [in bytes] - if 0, no HFP packet is sent |
| 15 | RESERVED | R/W | X | |
| 14-0 | RGB_SIZE | R/W | 0h | RGB_SIZE: size [in byte] of the RGB packet |

7.2.35 DSI_VID_BLKSIZE1 Register (Offset = CCh) [reset = X]

DSI_VID_BLKSIZE1 is shown in [Figure 7-51](#) and described in [Table 7-122](#).

Return to [Summary Table](#).

blanking packet size

Table 7-121. DSI_VID_BLKSIZE1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00CCh |

Figure 7-51. DSI_VID_BLKSIZE1 Register

| | | | | | | | | | | | | | | | |
|------------|----|-------------------|----|------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | BLKEOL_PCK | | | | | | | | | | | |
| R/W-X | | | | R/W-0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BLKEOL_PCK | | BLKLINE_EVENT_PCK | | | | | | | | | | | | | |
| R/W-0h | | R/W-0h | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-122. DSI_VID_BLKSIZE1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31-30 | RESERVED | R/W | X | |
| 29-15 | BLKEOL_PCK | R/W | 0h | BLKEOL_PCK: packet length [in byte] on end of line if burst mode [reg_blkeol_mode = 0b0x] |
| 14-0 | BLKLINE_EVENT_PCK | R/W | 0h | BLKLINE_EVENT_PCK: packet length [in byte] in blanking line if line has to be filled with a packet [reg_blkline_mode = 0b0x] and sync is an event Event mode Blank line _____ _____ _HSS_ HDR_____ _____ CRC _HSS_ |

7.2.36 DSI_VID_BLKSIZE2 Register (Offset = D0h) [reset = X]

DSI_VID_BLKSIZE2 is shown in [Figure 7-52](#) and described in [Table 7-124](#).

Return to [Summary Table](#).

Pulse Mode blanking packet size

Table 7-123. DSI_VID_BLKSIZE2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00D0h |

Figure 7-52. DSI_VID_BLKSIZE2 Register

| | | | | | | | | | | | | | | | |
|--------------|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESE RVED | BLKLINE_PULSE_PCK | | | | | | | | | | | | | | |
| R/W-X | R/W-0h | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-124. DSI_VID_BLKSIZE2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-15 | RESERVED | R/W | X | |
| 14-0 | BLKLINE_PULSE_PCK | R/W | 0h | <p>BLKLINE_PULSE_PCK: packet length in blanking line if line has to be filled with a packet [reg_blkline_mode = 0b0x] and sync is a pulse</p> <p>Pulse mode Blank line</p> <p> _____ </p> <p>_____blkline_pulse_pck_____</p> <p> _____ </p> <p> _HSS_HSA_HSE_ </p> <p>HDR_____</p> <p>_____CRC _HSS_</p> |

7.2.37 DSI_VID_PCK_TIME Register (Offset = D8h) [reset = X]

DSI_VID_PCK_TIME is shown in [Figure 7-53](#) and described in [Table 7-126](#).

Return to [Summary Table](#).

Packet duration

Table 7-125. DSI_VID_PCK_TIME Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00D8h |

Figure 7-53. DSI_VID_PCK_TIME Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | BLKEOL_DURATION | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-126. DSI_VID_PCK_TIME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-15 | RESERVED | R/W | X | |
| 14-0 | BLKEOL_DURATION | R/W | 0h | BLKEOL_DURATION: specify the duration in clock cycles of the BLLP period [used for burst mode] |

7.2.38 DSI_VID_DPHY_TIME Register (Offset = DCh) [reset = X]

DSI_VID_DPHY_TIME is shown in [Figure 7-54](#) and described in [Table 7-128](#).

Return to [Summary Table](#).

Time of D-PHY behavior for wakeup time and Line duration for LP during horizontal blanking lines

Table 7-127. DSI_VID_DPHY_TIME Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00DCh |

Figure 7-54. DSI_VID_DPHY_TIME Register

| | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|-----------------|----|----|----|----|----|----|----|----|----|----|----|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | |
| RESERVED | | | | REG_WAKEUP_TIME | | | | | | | | | | | | REG_L INE_D URATI ON |
| R/W-X | | | | R/W-0h | | | | | | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| REG_LINE_DURATION | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-128. DSI_VID_DPHY_TIME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-28 | RESERVED | R/W | X | |
| 27-17 | REG_WAKEUP_TIME | R/W | 0h | REG_WAKEUP_TIME: estimated time [in clock cycles] to perform LP->HS on D-PHY _____reg_wakeup_time_____ Clk Request -----> Clk Ready Data Request -----> Data Ready |

Table 7-128. DSI_VID_DPHY_TIME Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 16-0 | REG_LINE_DURATION | R/W | 0h | <p>REG_LINE_DURATION: duration -in clock cycles - of the blanking area for VSA/VBP and VFP lines - considered when reg_blkline_mode = 1b1x</p> <p>Pulse mode Blank LP line EOT disabled</p> <p>_____ _____ reg_line_duration _____</p> <p>_____ _HSS_HSA_HSE_ _____ LP _____</p> <p>_____ _HSS_ Pulse mode Blank LP line EOT enabled</p> <p>_____ _____ reg_line_duration _____</p> <p>_____ _HSS_HSA_HSE_ EoT _____ LP _____</p> <p>_____ _HSS_ Event mode Blank LP line EOT enabled</p> <p>_____ _____ reg_line_duration _____</p> <p>_____ _HSS EoT _____ LP _____</p> <p>_____ _HSS_</p> |

7.2.39 DSI_VID_ERR_COLOR1 Register (Offset = E0h) [reset = X]

DSI_VID_ERR_COLOR1 is shown in [Figure 7-55](#) and described in [Table 7-130](#).

Return to [Summary Table](#).

error color (green and red)

Table 7-129. DSI_VID_ERR_COLOR1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00E0h |

Figure 7-55. DSI_VID_ERR_COLOR1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COL_GREEN | | | | | | | | COL_RED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-130. DSI_VID_ERR_COLOR1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-12 | COL_GREEN | R/W | 0h | COL_GREEN: green component of the fill color |
| 11-0 | COL_RED | R/W | 0h | COL_RED: red component of the fill color |

7.2.40 DSI_VID_ERR_COLOR2 Register (Offset = E4h) [reset = X]

DSI_VID_ERR_COLOR2 is shown in [Figure 7-56](#) and described in [Table 7-132](#).

Return to [Summary Table](#).

error color (blue and padding)

Table 7-131. DSI_VID_ERR_COLOR2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00E4h |

Figure 7-56. DSI_VID_ERR_COLOR2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | PAD_VALUE | | | | | | | | COL_BLUE | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-132. DSI_VID_ERR_COLOR2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-12 | PAD_VALUE | R/W | 0h | PAD_VALUE: byte used to pad data [when system does not know exactly where it is] |
| 11-0 | COL_BLUE | R/W | 0h | COL_BLUE: blue component of the fill color |

7.2.41 DSI_VID_VPOS Register (Offset = E8h) [reset = X]

DSI_VID_VPOS is shown in [Figure 7-57](#) and described in [Table 7-134](#).

Return to [Summary Table](#).

vertical position

Table 7-133. DSI_VID_VPOS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00E8h |

Figure 7-57. DSI_VID_VPOS Register

| | | | | | | | |
|----------|----------|----|----|----|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | LINE_VAL | | | | | | |
| R-X | R-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_VAL | | | | | | LINE_POS | |
| R-0h | | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 7-134. DSI_VID_VPOS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-15 | RESERVED | R | X | |
| 14-2 | LINE_VAL | R | 0h | LINE_VAL: line number of the current area |
| 1-0 | LINE_POS | R | 0h | LINE_POS: position in the frame [see description in Video Stream Generator] |

7.2.42 DSI_VID_HPOS Register (Offset = ECh) [reset = X]

DSI_VID_HPOS is shown in [Figure 7-58](#) and described in [Table 7-136](#).

Return to [Summary Table](#).

Horizontal Position

Table 7-135. DSI_VID_HPOS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00ECh |

Figure 7-58. DSI_VID_HPOS Register

| | | | | | | | |
|----------------|----|----|----|----|----------------|----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | HORIZONTAL_VAL | |
| R-X | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| HORIZONTAL_VAL | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HORIZONTAL_VAL | | | | | HORIZONTAL_POS | | |
| R-0h | | | | | R-0h | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-136. DSI_VID_HPOS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-18 | RESERVED | R | X | |
| 17-3 | HORIZONTAL_VAL | R | 0h | HORIZONTAL_VAL: position in the current horizontal area [in clock cycles] |
| 2-0 | HORIZONTAL_POS | R | 0h | HORIZONTAL_POS: position in the line [see description in Video Stream Generator] |

7.2.43 DSI_VID_MODE_STS Register (Offset = F0h) [reset = X]

DSI_VID_MODE_STS is shown in [Figure 7-59](#) and described in [Table 7-138](#).

Return to [Summary Table](#).

Video mode status and error reporting

Table 7-137. DSI_VID_MODE_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00F0h |

Figure 7-59. DSI_VID_MODE_STS Register

| | | | | | | | |
|-------------------|--------------------|--------------------------|--------------------------|-----------------------|-----------------------|--------------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | VSG_RECOVER RY | ERR_VRS_WR ONG_LENGTH | ERR_LONGRE AD |
| R-X | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_LINEWR ITE | ERR_BURSTW RITE | REG_ERR_SM ALL_HEIGHT | REG_ERR_SM ALL_LENGTH | ERR_MISSING _VSYNC | ERR_MISSING _HSYNC | ERR_MISSING _DATA | VSG_RUNNIN G |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-138. DSI_VID_MODE_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10 | VSG_RECOVERY | R | 0h | VSG_RECOVERY: specifies whether the VSG is in recovery mode or not |
| 9 | ERR_VRS_WRONG_LENGTH | R | 0h | ERR_VRS_WRONG_LENGTH: signals that packets in SDI interface differ from the expected size [as specified by rgb_size] |
| 8 | ERR_LONGREAD | R | 0h | ERR_LONGREAD: signals the read was too long |
| 7 | ERR_LINEWRITE | R | 0h | ERR_LINEWRITE: signals the long packet is too long to pass during a long slot |
| 6 | ERR_BURSTWRITE | R | 0h | ERR_BURSTWRITE: signals a long packet has been sent during active area |
| 5 | REG_ERR_SMALL_HEIGHT | R | 0h | REG_ERR_SMALL_HEIGHT: fewer lines than expected between 2 VSYNC |
| 4 | REG_ERR_SMALL_LENGTH | R | 0h | REG_ERR_SMALL_LENGTH: fewer bytes received than expected between 2 HSYNC. Note that MISSING_DATA error may occur instead of SMALL_LENGTH, dependent upon timing. |
| 3 | ERR_MISSING_VSYNC | R | 0h | ERR_MISSING_VSYNC: missing VSYNC |
| 2 | ERR_MISSING_HSYNC | R | 0h | ERR_MISSING_HSYNC: missing HSYNC |

Table 7-138. DSI_VID_MODE_STS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 1 | ERR_MISSING_DATA | R | 0h | ERR_MISSING_DATA: data starvation at input of the VSG. Note that this error report may also be triggered instead of the SMALL_LENGTH error, dependent upon timing. |
| 0 | VSG_RUNNING | R | 0h | VSG_RUNNING: VSG is running [1] or stopped [0] |

7.2.44 DSI_VID_VCA_SETTING1 Register (Offset = F4h) [reset = X]

DSI_VID_VCA_SETTING1 is shown in [Figure 7-60](#) and described in [Table 7-140](#).

Return to [Summary Table](#).

VCA control register 1

Table 7-139. DSI_VID_VCA_SETTING1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00F4h |

Figure 7-60. DSI_VID_VCA_SETTING1 Register

| | | | | | | | |
|-----------------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | BURST_LP |
| R/W-X | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MAX_BURST_LIMIT | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MAX_BURST_LIMIT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-140. DSI_VID_VCA_SETTING1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-17 | RESERVED | R/W | X | |
| 16 | BURST_LP | R/W | 0h | BURST_LP: after an active line, the system can switch in LP [1] or should complete the line with NULL packet [0] |
| 15-0 | MAX_BURST_LIMIT | R/W | 0h | MAX_BURST_LIMIT: size of the 'biggest' burst packet [packet that fits after RGB in burst mode] |

7.2.45 DSI_VID_VCA_SETTING2 Register (Offset = F8h) [reset = 0h]

DSI_VID_VCA_SETTING2 is shown in [Figure 7-61](#) and described in [Table 7-142](#).

Return to [Summary Table](#).

VCA control register 2

Table 7-141. DSI_VID_VCA_SETTING2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00F8h |

Figure 7-61. DSI_VID_VCA_SETTING2 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_LINE_LIMIT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EXACT_BURST_LIMIT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-142. DSI_VID_VCA_SETTING2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-16 | MAX_LINE_LIMIT | R/W | 0h | MAX_LINE_LIMIT: maximum size of the line packet [packet that fits in blanking line] |
| 15-0 | EXACT_BURST_LIMIT | R/W | 0h | EXACT_BURST_LIMIT: exact maximum size of the burst packet [packet that fits after RGB in burst mode] |

7.2.46 DSI_TVG_CTL Register (Offset = FCh) [reset = X]

DSI_TVG_CTL is shown in [Figure 7-62](#) and described in [Table 7-144](#).

[Return to Summary Table.](#)

Main control of the TVG

Table 7-143. DSI_TVG_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 00FCh |

Figure 7-62. DSI_TVG_CTL Register

| | | | | | | | |
|-----------------|----|----|----------|----|--------------|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TVG_STRIPE_SIZE | | | TVG_MODE | | TVG_STOPMODE | | TVG_RUN |
| R/W-0h | | | R/W-0h | | R/W-0h | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-144. DSI_TVG_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7-5 | TVG_STRIPE_SIZE | R/W | 0h | TVG_STRIPE_SIZE: size of the stripe [in pixels] - defined by $2^{\text{reg_tvg_stripe_size}}$ |
| 4-3 | TVG_MODE | R/W | 0h | TVG_MODE: TVG display mode : 00 : single color 01 : reserved 10 : vertical stripes 11 horizontal stripes |
| 2-1 | TVG_STOPMODE | R/W | 0h | TVG_STOPMODE: stop mode: 00: at end of frame, 01: at end of line, 1x: immediate |
| 0 | TVG_RUN | R/W | 0h | TVG_RUN: start/stop of the TVG |

7.2.47 DSI_TVG_IMG_SIZE Register (Offset = 100h) [reset = X]

DSI_TVG_IMG_SIZE is shown in [Figure 7-63](#) and described in [Table 7-146](#).

Return to [Summary Table](#).

TVG Generated image size

Table 7-145. DSI_TVG_IMG_SIZE Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0100h |

Figure 7-63. DSI_TVG_IMG_SIZE Register

| | | | | | | | |
|---------------|---------------|----|----|------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | TVG_NBLINE | | | |
| R/W-X | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TVG_NBLINE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | TVG_LINE_SIZE | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TVG_LINE_SIZE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-146. DSI_TVG_IMG_SIZE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-29 | RESERVED | R/W | X | |
| 28-16 | TVG_NBLINE | R/W | 0h | TVG_NBLINE: Number of lines per frame |
| 15 | RESERVED | R/W | X | |
| 14-0 | TVG_LINE_SIZE | R/W | 0h | TVG_LINE_SIZE: Number of bytes per line |

7.2.48 DSI_TVG_COLOR1 Register (Offset = 104h) [reset = X]

DSI_TVG_COLOR1 is shown in [Figure 7-64](#) and described in [Table 7-148](#).

Return to [Summary Table](#).

Color 1 of the dummy frame G, R

Table 7-147. DSI_TVG_COLOR1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0104h |

Figure 7-64. DSI_TVG_COLOR1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COL1_GREEN | | | | | | | | COL1_RED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-148. DSI_TVG_COLOR1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-12 | COL1_GREEN | R/W | 0h | COL1_GREEN: green component of the color 1 |
| 11-0 | COL1_RED | R/W | 0h | COL1_RED: red component of the color 1 |

7.2.49 DSI_TVG_COLOR1_BIS Register (Offset = 108h) [reset = X]

DSI_TVG_COLOR1_BIS is shown in [Figure 7-65](#) and described in [Table 7-150](#).

Return to [Summary Table](#).

Color 1 of the dummy frame , B

Table 7-149. DSI_TVG_COLOR1_BIS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0108h |

Figure 7-65. DSI_TVG_COLOR1_BIS Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | COL1_BLUE | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-150. DSI_TVG_COLOR1_BIS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | COL1_BLUE | R/W | 0h | COL1_BLUE: blue component of the color 1 |

7.2.50 DSI_TVG_COLOR2 Register (Offset = 10Ch) [reset = X]

DSI_TVG_COLOR2 is shown in [Figure 7-66](#) and described in [Table 7-152](#).

Return to [Summary Table](#).

Color 2 of the dummy frame, G, R

Table 7-151. DSI_TVG_COLOR2 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 010Ch |

Figure 7-66. DSI_TVG_COLOR2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COL2_GREEN | | | | | | | | COL2_RED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-152. DSI_TVG_COLOR2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-12 | COL2_GREEN | R/W | 0h | COL2_GREEN: green component of the color 2 |
| 11-0 | COL2_RED | R/W | 0h | COL2_RED: red component of the color 2 |

7.2.51 DSI_TVG_COLOR2_BIS Register (Offset = 110h) [reset = X]

DSI_TVG_COLOR2_BIS is shown in [Figure 7-67](#) and described in [Table 7-154](#).

Return to [Summary Table](#).

Color 2 of the dummy frame, B

Table 7-153. DSI_TVG_COLOR2_BIS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0110h |

Figure 7-67. DSI_TVG_COLOR2_BIS Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | COL2_BLUE | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-154. DSI_TVG_COLOR2_BIS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | COL2_BLUE | R/W | 0h | COL2_BLUE: blue component of the color 2 |

7.2.52 DSI_TVG_STS Register (Offset = 114h) [reset = X]

DSI_TVG_STS is shown in [Figure 7-68](#) and described in [Table 7-156](#).

Return to [Summary Table](#).

TVG status register

Table 7-155. DSI_TVG_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0114h |

Figure 7-68. DSI_TVG_STS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | TVG_RUNNIN G |
| R-X | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-156. DSI_TVG_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--------------------------------|
| 31-1 | RESERVED | R | X | |
| 0 | TVG_RUNNING | R | 0h | TVG_RUNNING: status of the TVG |

7.2.53 DSI_MCTL_MAIN_STS_CTL Register (Offset = 130h) [reset = X]

DSI_MCTL_MAIN_STS_CTL is shown in [Figure 7-69](#) and described in [Table 7-158](#).

Return to [Summary Table](#).

Controls the enabling and edge detection of main ctrl status bits

EDGE = 0 captures the rising edge of the event, EDGE= 1 captures falling edge.

Table 7-157. DSI_MCTL_MAIN_STS_CTL Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0130h |

Figure 7-69. DSI_MCTL_MAIN_STS_CTL Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-------------------------|-------------------------|
| RESERVED | | | | | | IF3_UNTERM_PCK_ERR_EDGE | IF1_UNTERM_PCK_ERR_EDGE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LPRX_TO_ERR_EDGE | HSTX_TO_ERR_EDGE | DAT4_READY_EDGE | DAT3_READY_EDGE | DAT2_READY_EDGE | DAT1_READY_EDGE | CLKLANE_READY_EDGE | PLL_LOCK_EDGE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | IF3_UNTERM_PCK_ERR_EN | IF1_UNTERM_PCK_ERR_EN |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LPRX_TO_ERR_EN | HSTX_TO_ERR_EN | DAT4_READY_EN | DAT3_READY_EN | DAT2_READY_EN | DAT1_READY_EN | CLKLANE_READY_EN | PLL_LOCK_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-158. DSI_MCTL_MAIN_STS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-26 | RESERVED | R/W | X | |
| 25 | IF3_UNTERM_PCK_ERR_EDGE | R/W | 0h | IF3_UNTERM_PCK_ERR_EDGE: edge detection of if3_unterm_pck_err |
| 24 | IF1_UNTERM_PCK_ERR_EDGE | R/W | 0h | IF1_UNTERM_PCK_ERR_EDGE: edge detection of if1_unterm_pck_err |
| 23 | LPRX_TO_ERR_EDGE | R/W | 0h | LPRX_TO_ERR_EDGE: edge detection of LP_RX time-out error |
| 22 | HSTX_TO_ERR_EDGE | R/W | 0h | HSTX_TO_ERR_EDGE: edge detection of HS_TX time-out error |
| 21 | DAT4_READY_EDGE | R/W | 0h | DAT4_READY_EDGE: edge detection of dat4_ready |
| 20 | DAT3_READY_EDGE | R/W | 0h | DAT3_READY_EDGE: edge detection of dat3_ready |
| 19 | DAT2_READY_EDGE | R/W | 0h | DAT2_READY_EDGE: edge detection of dat2_ready |
| 18 | DAT1_READY_EDGE | R/W | 0h | DAT1_READY_EDGE: edge detection of dat1_ready |
| 17 | CLKLANE_READY_EDGE | R/W | 0h | CLKLANE_READY_EDGE: edge detection of clklane_ready |
| 16 | PLL_LOCK_EDGE | R/W | 0h | PLL_LOCK_EDGE: edge detection of PLL lock |
| 15-10 | RESERVED | R/W | X | |

Table 7-158. DSI_MCTL_MAIN_STS_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 9 | IF3_UNTERM_PCK_ERR_EN | R/W | 0h | IF3_UNTERM_PCK_ERR_EN: enables if3_unterm_pck_err |
| 8 | IF1_UNTERM_PCK_ERR_EN | R/W | 0h | IF1_UNTERM_PCK_ERR_EN: enables if1_unterm_pck_err |
| 7 | LPRX_TO_ERR_EN | R/W | 0h | LPRX_TO_ERR_EN: enables lprx_to_err |
| 6 | HSTX_TO_ERR_EN | R/W | 0h | HSTX_TO_ERR_EN: enables hstx_to_err |
| 5 | DAT4_READY_EN | R/W | 0h | DAT4_READY_EN: enables dat4_ready |
| 4 | DAT3_READY_EN | R/W | 0h | DAT3_READY_EN: enables dat3_ready |
| 3 | DAT2_READY_EN | R/W | 0h | DAT2_READY_EN: enables dat2_ready |
| 2 | DAT1_READY_EN | R/W | 0h | DAT1_READY_EN: enables dat1_ready |
| 1 | CLKLANE_READY_EN | R/W | 0h | CLKLANE_READY_EN: enables clklane_ready |
| 0 | PLL_LOCK_EN | R/W | 0h | PLL_LOCK_EN: enables PLL lock |

7.2.54 DSI_CMD_MODE_STS_CTL Register (Offset = 134h) [reset = X]

DSI_CMD_MODE_STS_CTL is shown in [Figure 7-70](#) and described in [Table 7-160](#).

Return to [Summary Table](#).

Controls the enabling and edge detection of command status bits

EDGE = 0 captures the rising edge of the event, EDGE= 1 captures falling edge.

Table 7-159. DSI_CMD_MODE_STS_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0134h |

Figure 7-70. DSI_CMD_MODE_STS_CTL Register

| | | | | | | | |
|----------|---------------------------|---------------------------|--------------------------|----------------------|--------------------|----------------------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | ERR_IF3_UND ERRUN_EDGE | ERR_IF1_UND ERRUN_EDGE | ERR_UNWANT ED_RD_EDGE | ERR_TE_MISS _EDGE | ERR_NO_TE_E DGE | CSM_RUNNIN G_EDGE | |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ERR_IF3_UND ERRUN_EN | ERR_IF1_UND ERRUN_EN | ERR_UNWANT ED_RD_EN | ERR_TE_MISS _EN | ERR_NO_TE_E N | CSM_RUNNIN G_EN | |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-160. DSI_CMD_MODE_STS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-22 | RESERVED | R/W | X | |
| 21 | ERR_IF3_UNDERRUN_E DGE | R/W | 0h | ERR_IF3_UNDERRUN_EDGE: edge detection of err_IF3_underrun |
| 20 | ERR_IF1_UNDERRUN_E DGE | R/W | 0h | ERR_IF1_UNDERRUN_EDGE: edge detection of err_IF1_underrun |
| 19 | ERR_UNWANTED_RD_E DGE | R/W | 0h | ERR_UNWANTED_RD_EDGE: edge detection of err_unwanted_rd |
| 18 | ERR_TE_MISS_EDGE | R/W | 0h | ERR_TE_MISS_EDGE: edge detection of err_te_miss |
| 17 | ERR_NO_TE_EDGE | R/W | 0h | ERR_NO_TE_EDGE: edge detection of err_no_te |
| 16 | CSM_RUNNING_EDGE | R/W | 0h | CSM_RUNNING_EDGE: edge detection of CSM running |
| 15-6 | RESERVED | R/W | X | |
| 5 | ERR_IF3_UNDERRUN_E N | R/W | 0h | ERR_IF3_UNDERRUN_EN: enables err_IF3_underrun |
| 4 | ERR_IF1_UNDERRUN_E N | R/W | 0h | ERR_IF1_UNDERRUN_EN: enables err_IF1_underrun |
| 3 | ERR_UNWANTED_RD_E N | R/W | 0h | ERR_UNWANTED_RD_EN: enables err_unwanted_rd |
| 2 | ERR_TE_MISS_EN | R/W | 0h | ERR_TE_MISS_EN: enables err_te_miss |
| 1 | ERR_NO_TE_EN | R/W | 0h | ERR_NO_TE_EN: enables err_no_te |

Table 7-160. DSI_CMD_MODE_STS_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 0 | CSM_RUNNING_EN | R/W | 0h | CSM_RUNNING_EN: enables signaling of CSM running |

7.2.55 DSI_DIRECT_CMD_STS_CTL Register (Offset = 138h) [reset = X]

DSI_DIRECT_CMD_STS_CTL is shown in [Figure 7-71](#) and described in [Table 7-162](#).

Return to [Summary Table](#).

Controls the enabling and edge detection of Direct Command status bits

Table 7-161. DSI_DIRECT_CMD_STS_CTL Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0138h |

Figure 7-71. DSI_DIRECT_CMD_STS_CTL Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|---------------------------|-----------------------------------|-----------------------------------|-------------------------|--------------------------------------|--------------------------|---------------------------|
| RESERVED | | | | | READ_COMPL ETED_WITH_E RR_EDGE | BTA_FINISHED _EDGE | BTA_COMPLE TED_EDGE |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TE_RECEIVED _EDGE | TRIGGER_REC EIVED_EDGE | ACKNOWLEDG E_WITH_ERR_ EDGE | ACKNOWLEDG E_RECEIVED_ EDGE | READ_COMPL ETED_EDGE | TRIGGER_CO MPLETED_ED GE | WRITE_COMP LETED_EDGE | CMD_TRANSM ISSIÖN_EDGE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | READ_COMPL ETED_WITH_E RR_EN | BTA_FINISHED _EN | BTA_COMPLE TED_EN |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TE_RECEIVED _EN | TRIGGER_REC EIVED_EN | ACKNOWLEDG E_WITH_ERR_ EN | ACKNOWLEDG E_RECEIVED_ EN | READ_COMPL ETED_EN | TRIGGER_CO MPLETED_EN | WRITE_COMP LETED_EN | CMD_TRANSM ISSIÖN_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-162. DSI_DIRECT_CMD_STS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--|
| 31-27 | RESERVED | R/W | X | |
| 26 | READ_COMPLETED_WI TH_ERR_EDGE | R/W | 0h | READ_COMPLETED_WITH_ERR_EDGE: edge detection of read detection completed with errors |
| 25 | BTA_FINISHED_EDGE | R/W | 0h | BTA_FINISHED_EDGE: edge detection of BTA completion detection |
| 24 | BTA_COMPLETED_EDG E | R/W | 0h | BTA_COMPLETED_EDGE: edge detection of BTA request completed |
| 23 | TE_RECEIVED_EDGE | R/W | 0h | TE_RECEIVED_EDGE: edge detection of TE received |
| 22 | TRIGGER_RECEIVED_E DGE | R/W | 0h | TRIGGER_RECEIVED_EDGE: edge detection of trigger |
| 21 | ACKNOWLEDGE_WITH_ ERR_EDGE | R/W | 0h | ACKNOWLEDGE_WITH_ERR_EDGE: edge detection of acknowledge with error |
| 20 | ACKNOWLEDGE_RECEI VED_EDGE | R/W | 0h | ACKNOWLEDGE_RECEIVED_EDGE: edge detection of acknowledge |
| 19 | READ_COMPLETED_ED GE | R/W | 0h | READ_COMPLETED_EDGE: edge detection of read request completed |

Table 7-162. DSI_DIRECT_CMD_STS_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 18 | TRIGGER_COMPLETED_EDGE | R/W | 0h | TRIGGER_COMPLETED_EDGE: edge detection of trigger request completed |
| 17 | WRITE_COMPLETED_EDGE | R/W | 0h | WRITE_COMPLETED_EDGE: edge detection of detection of write request completed |
| 16 | CMD_TRANSMISSION_EDGE | R/W | 0h | CMD_TRANSMISSION_EDGE: edge detection of cmd_transmission |
| 15-11 | RESERVED | R/W | X | |
| 10 | READ_COMPLETED_WITH_ERR_EN | R/W | 0h | READ_COMPLETED_WITH_ERR_EN: enables detection of read completed with errors |
| 9 | BTA_FINISHED_EN | R/W | 0h | BTA_FINISHED_EN: enables BTA completion detection |
| 8 | BTA_COMPLETED_EN | R/W | 0h | BTA_COMPLETED_EN: enables BTA request completed |
| 7 | TE_RECEIVED_EN | R/W | 0h | TE_RECEIVED_EN: enables TE received |
| 6 | TRIGGER_RECEIVED_EN | R/W | 0h | TRIGGER_RECEIVED_EN: enables trigger |
| 5 | ACKNOWLEDGE_WITH_ERR_EN | R/W | 0h | ACKNOWLEDGE_WITH_ERR_EN: enables acknowledge with error |
| 4 | ACKNOWLEDGE_RECEIVED_EN | R/W | 0h | ACKNOWLEDGE_RECEIVED_EN: enables acknowledge |
| 3 | READ_COMPLETED_EN | R/W | 0h | READ_COMPLETED_EN: enables read request completed |
| 2 | TRIGGER_COMPLETED_EN | R/W | 0h | TRIGGER_COMPLETED_EN: enables trigger_completed |
| 1 | WRITE_COMPLETED_EN | R/W | 0h | WRITE_COMPLETED_EN: enables write_completed |
| 0 | CMD_TRANSMISSION_EN | R/W | 0h | CMD_TRANSMISSION_EN: enables detection of cmd_transmission |

7.2.56 DSI_DIRECT_CMD_RD_STS_CTL Register (Offset = 13Ch) [reset = X]

DSI_DIRECT_CMD_RD_STS_CTL is shown in [Figure 7-72](#) and described in [Table 7-164](#).

Return to [Summary Table](#).

Controls the enabling and edge detection of read commands error

Table 7-163. DSI_DIRECT_CMD_RD_STS_CTL Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 013Ch |

Figure 7-72. DSI_DIRECT_CMD_RD_STS_CTL Register

| | | | | | | | |
|----------------------|-----------------------|-------------------|------------------|----------------------|-------------------|------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | ERR_EOT_WITH_ERR_EDGE |
| R/W-X | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_MISSING_EOT_EDGE | ERR_WRONG_LENGTH_EDGE | ERR_OVERSIZE_EDGE | ERR_RECEIVE_EDGE | ERR_UNDECODABLE_EDGE | ERR_CHECKSUM_EDGE | ERR_UNCORRECTABLE_EDGE | ERR_FIXED_EDGE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ERR_EOT_WITH_ERR_EN |
| R/W-X | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_MISSING_EOT_EN | ERR_WRONG_LENGTH_EN | ERR_OVERSIZE_EN | ERR_RECEIVE_EN | ERR_UNDECODABLE_EN | ERR_CHECKSUM_EN | ERR_UNCORRECTABLE_EN | ERR_FIXED_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-164. DSI_DIRECT_CMD_RD_STS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-25 | RESERVED | R/W | X | |
| 24 | ERR_EOT_WITH_ERR_EDGE | R/W | 0h | ERR_EOT_WITH_ERR_EDGE: edge detection of err_eot_with_err |
| 23 | ERR_MISSING_EOT_EDGE | R/W | 0h | ERR_MISSING_EOT_EDGE: edge detection of err_missing_eot |
| 22 | ERR_WRONG_LENGTH_EDGE | R/W | 0h | ERR_WRONG_LENGTH_EDGE: edge detection of err_wrong_length |
| 21 | ERR_OVERSIZE_EDGE | R/W | 0h | ERR_OVERSIZE_EDGE: edge detection of err_oversize |
| 20 | ERR_RECEIVE_EDGE | R/W | 0h | ERR_RECEIVE_EDGE: edge detection of err_receive |
| 19 | ERR_UNDECODABLE_EDGE | R/W | 0h | ERR_UNDECODABLE_EDGE: edge detection of err_undecodable |
| 18 | ERR_CHECKSUM_EDGE | R/W | 0h | ERR_CHECKSUM_EDGE: edge detection of err_checksum |
| 17 | ERR_UNCORRECTABLE_EDGE | R/W | 0h | ERR_UNCORRECTABLE_EDGE: edge detection of err_uncorrectable |
| 16 | ERR_FIXED_EDGE | R/W | 0h | ERR_FIXED_EDGE: edge detection of err_fixed |
| 15-9 | RESERVED | R/W | X | |

Table 7-164. DSI_DIRECT_CMD_RD_STS_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 8 | ERR_EOT_WITH_ERR_EN | R/W | 0h | ERR_EOT_WITH_ERR_EN: enables err_eot_with_err |
| 7 | ERR_MISSING_EOT_EN | R/W | 0h | ERR_MISSING_EOT_EN: enables err_missing_eot |
| 6 | ERR_WRONG_LENGTH_EN | R/W | 0h | ERR_WRONG_LENGTH_EN: enables err_wrong_length |
| 5 | ERR_OVERSIZE_EN | R/W | 0h | ERR_OVERSIZE_EN: enables err_oversize |
| 4 | ERR_RECEIVE_EN | R/W | 0h | ERR_RECEIVE_EN: enables err_receive |
| 3 | ERR_UNDECODABLE_EN | R/W | 0h | ERR_UNDECODABLE_EN: enables err_undecodable |
| 2 | ERR_CHECKSUM_EN | R/W | 0h | ERR_CHECKSUM_EN: enables err_checksum |
| 1 | ERR_UNCORRECTABLE_EN | R/W | 0h | ERR_UNCORRECTABLE_EN: enables err_uncorrectable |
| 0 | ERR_FIXED_EN | R/W | 0h | ERR_FIXED_EN: enables err_fixed |

7.2.57 DSI_VID_MODE_STS_CTL Register (Offset = 140h) [reset = X]

DSI_VID_MODE_STS_CTL is shown in [Figure 7-73](#) and described in [Table 7-166](#).

Return to [Summary Table](#).

Control the enabling and edge detection of VSG status bits

Table 7-165. DSI_VID_MODE_STS_CTL Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0140h |

Figure 7-73. DSI_VID_MODE_STS_CTL Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------|---------------------|-----------------------|-----------------------|------------------------|------------------------|---------------------------|-------------------|
| RESERVED | | | | | VSG_RECOVERY_EDGE | ERR_VRS_WRONG_LENGTH_EDGE | ERR_LONGREAD_EDGE |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_LINEWRITE_EDGE | ERR_BURSTWRITE_EDGE | ERR_SMALL_HEIGHT_EDGE | ERR_SMALL_LENGTH_EDGE | ERR_MISSING_VSYNC_EDGE | ERR_MISSING_HSYNC_EDGE | ERR_MISSING_DATA_EDGE | VSG_RUNNING_EDGE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | VSG_RECOVERY_EN | ERR_VRS_WRONG_LENGTH_EN | ERR_LONGREAD_EN |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_LINEWRITE_EN | ERR_BURSTWRITE_EN | ERR_SMALL_HEIGHT_EN | ERR_SMALL_LENGTH_EN | ERR_MISSING_VSYNC_EN | ERR_MISSING_HSYNC_EN | ERR_MISSING_DATA_EN | VSG_RUNNING_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-166. DSI_VID_MODE_STS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|--|
| 31-27 | RESERVED | R/W | X | |
| 26 | VSG_RECOVERY_EDGE | R/W | 0h | VSG_RECOVERY_EDGE: edge detection of vsg_recovery |
| 25 | ERR_VRS_WRONG_LENGTH_EDGE | R/W | 0h | ERR_VRS_WRONG_LENGTH_EDGE: edge detection of err_vrs_wrong_length |
| 24 | ERR_LONGREAD_EDGE | R/W | 0h | ERR_LONGREAD_EDGE: edge detection of err_longread |
| 23 | ERR_LINEWRITE_EDGE | R/W | 0h | ERR_LINEWRITE_EDGE: edge detection of err_line_write |
| 22 | ERR_BURSTWRITE_EDGE | R/W | 0h | ERR_BURSTWRITE_EDGE: edge detection of err_burst_write |
| 21 | ERR_SMALL_HEIGHT_EDGE | R/W | 0h | ERR_SMALL_HEIGHT_EDGE: edge detection of unaligned line number |
| 20 | ERR_SMALL_LENGTH_EDGE | R/W | 0h | ERR_SMALL_LENGTH_EDGE: edge detection of unaligned size |
| 19 | ERR_MISSING_VSYNC_EDGE | R/W | 0h | ERR_MISSING_VSYNC_EDGE: edge detection of detection of missing VSYNC |
| 18 | ERR_MISSING_HSYNC_EDGE | R/W | 0h | ERR_MISSING_HSYNC_EDGE: edge detection of detection of missing HSYNC |

Table 7-166. DSI_VID_MODE_STS_CTL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 17 | ERR_MISSING_DATA_EDGE | R/W | 0h | ERR_MISSING_DATA_EDGE: edge detection of data miss detection |
| 16 | VSG_RUNNING_EDGE | R/W | 0h | VSG_RUNNING_EDGE: edge detection of VSG status observation |
| 15-11 | RESERVED | R/W | X | |
| 10 | VSG_RECOVERY_EN | R/W | 0h | VSG_RECOVERY_EN: enables vsg_recovery |
| 9 | ERR_VRS_WRONG_LENGTH_EN | R/W | 0h | ERR_VRS_WRONG_LENGTH_EN: enables err_vrs_wrong_length |
| 8 | ERR_LONGREAD_EN | R/W | 0h | ERR_LONGREAD_EN: enables err_longread |
| 7 | ERR_LINEWRITE_EN | R/W | 0h | ERR_LINEWRITE_EN: enables err_line_write |
| 6 | ERR_BURSTWRITE_EN | R/W | 0h | ERR_BURSTWRITE_EN: enables err_burst_write |
| 5 | ERR_SMALL_HEIGHT_EN | R/W | 0h | ERR_SMALL_HEIGHT_EN: enables detection of unaligned line number |
| 4 | ERR_SMALL_LENGTH_EN | R/W | 0h | ERR_SMALL_LENGTH_EN: enables detection of unaligned size |
| 3 | ERR_MISSING_VSYNC_EN | R/W | 0h | ERR_MISSING_VSYNC_EN: enables detection of missing VSYNC |
| 2 | ERR_MISSING_HSYNC_EN | R/W | 0h | ERR_MISSING_HSYNC_EN: enables detection of missing HSYNC |
| 1 | ERR_MISSING_DATA_EN | R/W | 0h | ERR_MISSING_DATA_EN: enables data miss detection |
| 0 | VSG_RUNNING_EN | R/W | 0h | VSG_RUNNING_EN: enables VSG status observation |

7.2.58 DSI_TVG_STS_CTL Register (Offset = 144h) [reset = X]

DSI_TVG_STS_CTL is shown in [Figure 7-74](#) and described in [Table 7-168](#).

Return to [Summary Table](#).

Control the enabling and edge detection of TVG status bits

Table 7-167. DSI_TVG_STS_CTL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0144h |

Figure 7-74. DSI_TVG_STS_CTL Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | TVG_STS_EDGE |
| R/W-X | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | TVG_STS_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-168. DSI_TVG_STS_CTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-17 | RESERVED | R/W | X | |
| 16 | TVG_STS_EDGE | R/W | 0h | TVG_STS_EDGE: edge detection of TVG status observation |
| 15-1 | RESERVED | R/W | X | |
| 0 | TVG_STS_EN | R/W | 0h | TVG_STS_EN: enables TVG status observation |

7.2.59 DSI_MCTL_DPHY_ERR_CTL1 Register (Offset = 148h) [reset = X]

DSI_MCTL_DPHY_ERR_CTL1 is shown in [Figure 7-75](#) and described in [Table 7-170](#).

Return to [Summary Table](#).

Controls the enabling and edge detection of the DPHY errors

Table 7-169. DSI_MCTL_DPHY_ERR_CTL1 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0148h |

Figure 7-75. DSI_MCTL_DPHY_ERR_CTL1 Register

| | | | | | | | |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ERR_CONT_L P1_4_EN | ERR_CONT_L P1_3_EN |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_CONT_L P1_2_EN | ERR_CONT_L P1_1_EN | ERR_CONT_L P0_4_EN | ERR_CONT_L P0_3_EN | ERR_CONT_L P0_2_EN | ERR_CONT_L P0_1_EN | ERR_CONTRO L_4_EN | ERR_CONTRO L_3_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ERR_CONTRO L_2_EN | ERR_CONTRO L_1_EN | ERR_SYNCES C_4_EN | ERR_SYNCES C_3_EN | ERR_SYNCES C_2_EN | ERR_SYNCES C_1_EN | ERR_ESC_4_E N | ERR_ESC_3_E N |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_ESC_2_E N | ERR_ESC_1_E N | RESERVED | | | | | |
| R/W-0h | R/W-0h | R/W-X | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-170. DSI_MCTL_DPHY_ERR_CTL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|-------------------|
| 31-26 | RESERVED | R/W | X | |
| 25 | ERR_CONT_LP1_4_EN | R/W | 0h | ERR_CONT_LP1_4_EN |
| 24 | ERR_CONT_LP1_3_EN | R/W | 0h | ERR_CONT_LP1_3_EN |
| 23 | ERR_CONT_LP1_2_EN | R/W | 0h | ERR_CONT_LP1_2_EN |
| 22 | ERR_CONT_LP1_1_EN | R/W | 0h | ERR_CONT_LP1_1_EN |
| 21 | ERR_CONT_LP0_4_EN | R/W | 0h | ERR_CONT_LP0_4_EN |
| 20 | ERR_CONT_LP0_3_EN | R/W | 0h | ERR_CONT_LP0_3_EN |
| 19 | ERR_CONT_LP0_2_EN | R/W | 0h | ERR_CONT_LP0_2_EN |
| 18 | ERR_CONT_LP0_1_EN | R/W | 0h | ERR_CONT_LP0_1_EN |
| 17 | ERR_CONTROL_4_EN | R/W | 0h | ERR_CONTROL_4_EN |
| 16 | ERR_CONTROL_3_EN | R/W | 0h | ERR_CONTROL_3_EN |
| 15 | ERR_CONTROL_2_EN | R/W | 0h | ERR_CONTROL_2_EN |
| 14 | ERR_CONTROL_1_EN | R/W | 0h | ERR_CONTROL_1_EN |
| 13 | ERR_SYNCESC_4_EN | R/W | 0h | ERR_SYNCESC_4_EN |
| 12 | ERR_SYNCESC_3_EN | R/W | 0h | ERR_SYNCESC_3_EN |
| 11 | ERR_SYNCESC_2_EN | R/W | 0h | ERR_SYNCESC_2_EN |

Table 7-170. DSI_MCTL_DPHY_ERR_CTL1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|------------------|
| 10 | ERR_SYNCESC_1_EN | R/W | 0h | ERR_SYNCESC_1_EN |
| 9 | ERR_ESC_4_EN | R/W | 0h | ERR_ESC_4_EN |
| 8 | ERR_ESC_3_EN | R/W | 0h | ERR_ESC_3_EN |
| 7 | ERR_ESC_2_EN | R/W | 0h | ERR_ESC_2_EN |
| 6 | ERR_ESC_1_EN | R/W | 0h | ERR_ESC_1_EN |
| 5-0 | RESERVED | R/W | X | |

7.2.60 DSI_MCTL_DPHY_ERR_CTL2 Register (Offset = 14Ch) [reset = X]

DSI_MCTL_DPHY_ERR_CTL2 is shown in [Figure 7-76](#) and described in [Table 7-172](#).

Return to [Summary Table](#).

Controls the enabling and edge detection of the DPHY errors

Table 7-171. DSI_MCTL_DPHY_ERR_CTL2 Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 014Ch |

Figure 7-76. DSI_MCTL_DPHY_ERR_CTL2 Register

| | | | | | | | |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | ERR_CONT_L P1_4_EDGE | ERR_CONT_L P1_3_EDGE | ERR_CONT_L P1_2_EDGE | ERR_CONT_L P1_1_EDGE |
| R/W-X | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ERR_CONT_L P0_4_EDGE | ERR_CONT_L P0_3_EDGE | ERR_CONT_L P0_2_EDGE | ERR_CONT_L P0_1_EDGE | ERR_CONTRO L_4_EDGE | ERR_CONTRO L_3_EDGE | ERR_CONTRO L_2_EDGE | ERR_CONTRO L_1_EDGE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_SYNCE C_4_EDGE | ERR_SYNCE C_3_EDGE | ERR_SYNCE C_2_EDGE | ERR_SYNCE C_1_EDGE | ERR_ESC_4_E DGE | ERR_ESC_3_E DGE | ERR_ESC_2_E DGE | ERR_ESC_1_E DGE |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-172. DSI_MCTL_DPHY_ERR_CTL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---------------------|
| 31-20 | RESERVED | R/W | X | |
| 19 | ERR_CONT_LP1_4_EDG E | R/W | 0h | ERR_CONT_LP1_4_EDGE |
| 18 | ERR_CONT_LP1_3_EDG E | R/W | 0h | ERR_CONT_LP1_3_EDGE |
| 17 | ERR_CONT_LP1_2_EDG E | R/W | 0h | ERR_CONT_LP1_2_EDGE |
| 16 | ERR_CONT_LP1_1_EDG E | R/W | 0h | ERR_CONT_LP1_1_EDGE |
| 15 | ERR_CONT_LP0_4_EDG E | R/W | 0h | ERR_CONT_LP0_4_EDGE |
| 14 | ERR_CONT_LP0_3_EDG E | R/W | 0h | ERR_CONT_LP0_3_EDGE |
| 13 | ERR_CONT_LP0_2_EDG E | R/W | 0h | ERR_CONT_LP0_2_EDGE |
| 12 | ERR_CONT_LP0_1_EDG E | R/W | 0h | ERR_CONT_LP0_1_EDGE |
| 11 | ERR_CONTROL_4_EDG E | R/W | 0h | ERR_CONTROL_4_EDGE |
| 10 | ERR_CONTROL_3_EDG E | R/W | 0h | ERR_CONTROL_3_EDGE |

Table 7-172. DSI_MCTL_DPHY_ERR_CTL2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--------------------|
| 9 | ERR_CONTROL_2_EDGE | R/W | 0h | ERR_CONTROL_2_EDGE |
| 8 | ERR_CONTROL_1_EDGE | R/W | 0h | ERR_CONTROL_1_EDGE |
| 7 | ERR_SYNCESC_4_EDGE | R/W | 0h | ERR_SYNCESC_4_EDGE |
| 6 | ERR_SYNCESC_3_EDGE | R/W | 0h | ERR_SYNCESC_3_EDGE |
| 5 | ERR_SYNCESC_2_EDGE | R/W | 0h | ERR_SYNCESC_2_EDGE |
| 4 | ERR_SYNCESC_1_EDGE | R/W | 0h | ERR_SYNCESC_1_EDGE |
| 3 | ERR_ESC_4_EDGE | R/W | 0h | ERR_ESC_4_EDGE |
| 2 | ERR_ESC_3_EDGE | R/W | 0h | ERR_ESC_3_EDGE |
| 1 | ERR_ESC_2_EDGE | R/W | 0h | ERR_ESC_2_EDGE |
| 0 | ERR_ESC_1_EDGE | R/W | 0h | ERR_ESC_1_EDGE |

7.2.61 DSI_MCTL_MAIN_STS_CLR Register (Offset = 150h) [reset = X]

DSI_MCTL_MAIN_STS_CLR is shown in [Figure 7-77](#) and described in [Table 7-174](#).

Return to [Summary Table](#).

Main control status register clear function. These bits are spread across different register banks.
The exact use of the set and reset is described in the section : Error and status bits. Write '1' to clear

Table 7-173. DSI_MCTL_MAIN_STS_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0150h |

Figure 7-77. DSI_MCTL_MAIN_STS_CLR Register

| | | | | | | | |
|-----------------|-----------------|----------------|----------------|----------------|----------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | IF3_UNTERM_PCK_ERR_CLR | IF1_UNTERM_PCK_ERR_CLR |
| W-X | | | | | | W-0h | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LPRX_TO_ERR_CLR | HSTX_TO_ERR_CLR | DAT4_READY_CLR | DAT3_READY_CLR | DAT2_READY_CLR | DAT1_READY_CLR | CLKLANE_READY_CLR | PLL_LOCK_CLR |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-174. DSI_MCTL_MAIN_STS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-10 | RESERVED | W | X | |
| 9 | IF3_UNTERM_PCK_ERR_CLR | W | 0h | IF3_UNTERM_PCK_ERR_CLR: clears if3_unterm_pck_err |
| 8 | IF1_UNTERM_PCK_ERR_CLR | W | 0h | IF1_UNTERM_PCK_ERR_CLR: clears if1_unterm_pck_err |
| 7 | LPRX_TO_ERR_CLR | W | 0h | LPRX_TO_ERR_CLR: clears lprx_to_err |
| 6 | HSTX_TO_ERR_CLR | W | 0h | HSTX_TO_ERR_CLR: clears hstx_to_err |
| 5 | DAT4_READY_CLR | W | 0h | DAT4_READY_CLR: clears dat4_ready |
| 4 | DAT3_READY_CLR | W | 0h | DAT3_READY_CLR: clears dat3_ready |
| 3 | DAT2_READY_CLR | W | 0h | DAT2_READY_CLR: clears dat2_ready |
| 2 | DAT1_READY_CLR | W | 0h | DAT1_READY_CLR: clears dat1_ready |
| 1 | CLKLANE_READY_CLR | W | 0h | CLKLANE_READY_CLR: clears clklane_ready |
| 0 | PLL_LOCK_CLR | W | 0h | PLL_LOCK_CLR: clears PLL lock |

7.2.62 DSI_CMD_MODE_STS_CLR Register (Offset = 154h) [reset = X]

DSI_CMD_MODE_STS_CLR is shown in [Figure 7-78](#) and described in [Table 7-176](#).

Return to [Summary Table](#).

Command status register clear function. Write '1' to clear

Table 7-175. DSI_CMD_MODE_STS_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0154h |

Figure 7-78. DSI_CMD_MODE_STS_CLR Register

| | | | | | | | |
|----------|----|--------------------------|--------------------------|-------------------------|---------------------|-------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ERR_IF3_UND ERRUN_CLR | ERR_IF1_UND ERRUN_CLR | ERR_UNWANT ED_RD_CLR | ERR_TE_MISS _CLR | ERR_NO_TE_ CLR | CSM_RUNNIN G_CLR |
| R/W-X | | R-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 7-176. DSI_CMD_MODE_STS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|---|
| 31-6 | RESERVED | R/W | X | |
| 5 | ERR_IF3_UNDERRUN_C LR | R | 0h | ERR_IF3_UNDERRUN_CLR: clears err_if3_underrun |
| 4 | ERR_IF1_UNDERRUN_C LR | W | 0h | ERR_IF1_UNDERRUN_CLR: clears err_if1_underrun |
| 3 | ERR_UNWANTED_RD_C LR | W | 0h | ERR_UNWANTED_RD_CLR: clears err_unwanted_rd |
| 2 | ERR_TE_MISS_CLR | W | 0h | ERR_TE_MISS_CLR: clears err_te_miss |
| 1 | ERR_NO_TE_CLR | W | 0h | ERR_NO_TE_CLR: clears err_no_te |
| 0 | CSM_RUNNING_CLR | W | 0h | CSM_RUNNING_CLR: clears CSM running bit |

7.2.63 DSI_DIRECT_CMD_STS_CLR Register (Offset = 158h) [reset = X]

DSI_DIRECT_CMD_STS_CLR is shown in [Figure 7-79](#) and described in [Table 7-178](#).

Return to [Summary Table](#).

Direct command status register clear function. Write '1' to clear

Table 7-177. DSI_DIRECT_CMD_STS_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0158h |

Figure 7-79. DSI_DIRECT_CMD_STS_CLR Register

| | | | | | | | |
|---------------------|--------------------------|----------------------|----------------------|------------------------|-------------------------------------|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | READ_COMPL ETED_WITH_E RR_CLR | BTA_FINISHED _CLR | BTA_COMPLE TED_CLR |
| W-X | | | | | W-0h | W-0h | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TE_RECEIVED _CLR | TRIGGER_REC EIVED_CLR | ACK_WITH_ER R_CLR | ACK_RECEIVE D_CLR | READ_COMPL ETED_CLR | TRIGGER_CO MPLETED_CL R | WRITE_COMP LETED_CLR | CMD_TRANSM ISSION_CLR |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-178. DSI_DIRECT_CMD_STS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-11 | RESERVED | W | X | |
| 10 | READ_COMPLETED_WI TH_ERR_CLR | W | 0h | READ_COMPLETED_WITH_ERR_CLR: clears detection of read completed with errors |
| 9 | BTA_FINISHED_CLR | W | 0h | BTA_FINISHED_CLR: clears BTA completion detection |
| 8 | BTA_COMPLETED_CLR | W | 0h | BTA_COMPLETED_CLR: clears BTA request completed |
| 7 | TE_RECEIVED_CLR | W | 0h | TE_RECEIVED_CLR: clears TE received |
| 6 | TRIGGER_RECEIVED_C LR | W | 0h | TRIGGER_RECEIVED_CLR: clears trigger |
| 5 | ACK_WITH_ERR_CLR | W | 0h | ACKNOWLEDGE_WITH_ERR_CLR: clears acknowledge with errors |
| 4 | ACK_RECEIVED_CLR | W | 0h | ACKNOWLEDGE_RECEIVED_CLR: clears acknowledge |
| 3 | READ_COMPLETED_CL R | W | 0h | READ_COMPLETED_CLR: clears read request completed |
| 2 | TRIGGER_COMPLETED_ CLR | W | 0h | TRIGGER_COMPLETED_CLR: clears trigger request completed |
| 1 | WRITE_COMPLETED_CL R | W | 0h | WRITE_COMPLETED_CLR: clears detection of write request completed |
| 0 | CMD_TRANSMISSION_C LR | W | 0h | CMD_TRANSMISSION_CLR: clears cmd_transmission |

7.2.64 DSI_DIRECT_CMD_RD_STS_CLR Register (Offset = 15Ch) [reset = X]

DSI_DIRECT_CMD_RD_STS_CLR is shown in [Figure 7-80](#) and described in [Table 7-180](#).

Return to [Summary Table](#).

Direct command read status register clear function. Write '1' to clear

Table 7-179. DSI_DIRECT_CMD_RD_STS_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 015Ch |

Figure 7-80. DSI_DIRECT_CMD_RD_STS_CLR Register

| | | | | | | | |
|-------------------------|--------------------------|----------------------|---------------------|-------------------------|----------------------|---------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ERR_EOT_WIT H_ERR_CLR |
| W-X | | | | | | | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_MISSING _EOT_CLR | ERR_WRONG_ LENGTH_CLR | ERR_OVERSIZ E_CLR | ERR_RECEIVE _CLR | ERR_UNDECO DABLE_CLR | ERR_CHECKS UM_CLR | ERR_UNCORR ECTABLE_CLR | ERR_FIXED_C LR |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-180. DSI_DIRECT_CMD_RD_STS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|---|
| 31-9 | RESERVED | W | X | |
| 8 | ERR_EOT_WITH_ERR_C LR | W | 0h | ERR_EOT_WITH_ERR_CLR: clears err_eot_with_err |
| 7 | ERR_MISSING_EOT_CL R | W | 0h | ERR_MISSING_EOT_CLR: clears err_missing_eot |
| 6 | ERR_WRONG_LENGTH_ CLR | W | 0h | ERR_WRONG_LENGTH_CLR: clears err_wrong_length |
| 5 | ERR_OVERSIZE_CLR | W | 0h | ERR_OVERSIZE_CLR: clears err_oversize |
| 4 | ERR_RECEIVE_CLR | W | 0h | ERR_RECEIVE_CLR: clears err_receive |
| 3 | ERR_UNDECODABLE_C LR | W | 0h | ERR_UNDECODABLE_CLR: clears err_undecodable |
| 2 | ERR_CHECKSUM_CLR | W | 0h | ERR_CHECKSUM_CLR: clears err_checksum |
| 1 | ERR_UNCORRECTABLE _CLR | W | 0h | ERR_UNCORRECTABLE_CLR: clears err_uncorrectable |
| 0 | ERR_FIXED_CLR | W | 0h | ERR_FIXED_CLR: clears err_fixed |

7.2.65 DSI_VID_MODE_STS_CLR Register (Offset = 160h) [reset = X]

DSI_VID_MODE_STS_CLR is shown in [Figure 7-81](#) and described in [Table 7-182](#).

Return to [Summary Table](#).

VSG status register clear function

Table 7-181. DSI_VID_MODE_STS_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0160h |

Figure 7-81. DSI_VID_MODE_STS_CLR Register

| | | | | | | | |
|-----------------------|------------------------|--------------------------|--------------------------|---------------------------|---------------------------|----------------------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | VSG_RECOVER RY_CLR | ERR_VRS_WR ONG_LENGTH _CLR | ERR_LONGRE AD_CLR |
| W-X | | | | | W-0h | W-0h | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_LINEWR ITE_CLR | ERR_BURSTW RITE_CLR | ERR_SMALL_H EIGHT_CLR | ERR_SMALL_L ENGTH_CLR | ERR_MISSING _VSYNC_CLR | ERR_MISSING _HSYNC_CLR | ERR_MISSING _DATA_CLR | VSG_STS_CLR |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-182. DSI_VID_MODE_STS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-11 | RESERVED | W | X | |
| 10 | VSG_RECOVERY_CLR | W | 0h | VSG_RECOVERY_CLR: clears the bit vsg_recovery |
| 9 | ERR_VRS_WRONG_LEN GTH_CLR | W | 0h | ERR_VRS_WRONG_LENGTH_CLR: clears the bit err_vid_wrong_length |
| 8 | ERR_LONGREAD_CLR | W | 0h | ERR_LONGREAD_CLR: clears err_longread |
| 7 | ERR_LINEWRITE_CLR | W | 0h | ERR_LINEWRITE_CLR: clears err_linewrite |
| 6 | ERR_BURSTWRITE_CLR | W | 0h | ERR_BURSTWRITE_CLR: clears err_burstwrite |
| 5 | ERR_SMALL_HEIGHT_C LR | W | 0h | ERR_SMALL_HEIGHT_CLR: clears unaligned line number |
| 4 | ERR_SMALL_LENGTH_C LR | W | 0h | ERR_SMALL_LENGTH_CLR: clears analigned size |
| 3 | ERR_MISSING_VSYNC_ CLR | W | 0h | ERR_MISSING_VSYNC_CLR: clears missing VSYNC |
| 2 | ERR_MISSING_HSYNC_ CLR | W | 0h | ERR_MISSING_HSYNC_CLR: clears missing HSYNC |
| 1 | ERR_MISSING_DATA_CL R | W | 0h | ERR_MISSING_DATA_CLR: clears data miss |
| 0 | VSG_STS_CLR | W | 0h | VSG_STS_CLR: clears VSG status |

7.2.66 DSI_TG_STS_CLR Register (Offset = 164h) [reset = X]

DSI_TG_STS_CLR is shown in [Figure 7-82](#) and described in [Table 7-184](#).

Return to [Summary Table](#).

TVG status register clear function. Write '1' to clear

Table 7-183. DSI_TG_STS_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0164h |

Figure 7-82. DSI_TG_STS_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | TVG_STS_CLR |
| W-X | | | | | | | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-184. DSI_TG_STS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-1 | RESERVED | W | X | |
| 0 | TVG_STS_CLR | W | 0h | TVG_STS_CLR: clears TVG status observation |

7.2.67 DSI_MCTL_DPHY_ERR_CLR Register (Offset = 168h) [reset = X]

DSI_MCTL_DPHY_ERR_CLR is shown in [Figure 7-83](#) and described in [Table 7-186](#).

Return to [Summary Table](#).

D_PHY lanes output register clear function. Write '1' to clear

Table 7-185. DSI_MCTL_DPHY_ERR_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0168h |

Figure 7-83. DSI_MCTL_DPHY_ERR_CLR Register

| | | | | | | | |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ERR_CONT_L P1_4_CLR | ERR_CONT_L P1_3_CLR |
| W-X | | | | | | W-0h | W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_CONT_L P1_2_CLR | ERR_CONT_L P1_1_CLR | ERR_CONT_L P0_4_CLR | ERR_CONT_L P0_3_CLR | ERR_CONT_L P0_2_CLR | ERR_CONT_L P0_1_CLR | ERR_CONTRO L_4_CLR | ERR_CONTRO L_3_CLR |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ERR_CONTRO L_2_CLR | ERR_CONTRO L_1_CLR | ERR_SYNCES C_4_CLR | ERR_SYNCES C_3_CLR | ERR_SYNCES C_2_CLR | ERR_SYNCES C_1_CLR | ERR_ESC_4_C LR | ERR_ESC_3_C LR |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_ESC_2_C LR | ERR_ESC_1_C LR | RESERVED | | | | | |
| W-0h | W-0h | W-X | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 7-186. DSI_MCTL_DPHY_ERR_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--------------------|
| 31-26 | RESERVED | W | X | |
| 25 | ERR_CONT_LP1_4_CLR | W | 0h | ERR_CONT_LP1_4_CLR |
| 24 | ERR_CONT_LP1_3_CLR | W | 0h | ERR_CONT_LP1_3_CLR |
| 23 | ERR_CONT_LP1_2_CLR | W | 0h | ERR_CONT_LP1_2_CLR |
| 22 | ERR_CONT_LP1_1_CLR | W | 0h | ERR_CONT_LP1_1_CLR |
| 21 | ERR_CONT_LP0_4_CLR | W | 0h | ERR_CONT_LP0_4_CLR |
| 20 | ERR_CONT_LP0_3_CLR | W | 0h | ERR_CONT_LP0_3_CLR |
| 19 | ERR_CONT_LP0_2_CLR | W | 0h | ERR_CONT_LP0_2_CLR |
| 18 | ERR_CONT_LP0_1_CLR | W | 0h | ERR_CONT_LP0_1_CLR |
| 17 | ERR_CONTROL_4_CLR | W | 0h | ERR_CONTROL_4_CLR |
| 16 | ERR_CONTROL_3_CLR | W | 0h | ERR_CONTROL_3_CLR |
| 15 | ERR_CONTROL_2_CLR | W | 0h | ERR_CONTROL_2_CLR |
| 14 | ERR_CONTROL_1_CLR | W | 0h | ERR_CONTROL_1_CLR |
| 13 | ERR_SYNCESC_4_CLR | W | 0h | ERR_SYNCESC_4_CLR |
| 12 | ERR_SYNCESC_3_CLR | W | 0h | ERR_SYNCESC_3_CLR |
| 11 | ERR_SYNCESC_2_CLR | W | 0h | ERR_SYNCESC_2_CLR |

Table 7-186. DSI_MCTL_DPHY_ERR_CLR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|-------------------|
| 10 | ERR_SYNCESC_1_CLR | W | 0h | ERR_SYNCESC_1_CLR |
| 9 | ERR_ESC_4_CLR | W | 0h | ERR_ESC_4_CLR |
| 8 | ERR_ESC_3_CLR | W | 0h | ERR_ESC_3_CLR |
| 7 | ERR_ESC_2_CLR | W | 0h | ERR_ESC_2_CLR |
| 6 | ERR_ESC_1_CLR | W | 0h | ERR_ESC_1_CLR |
| 5-0 | RESERVED | W | X | |

7.2.68 DSI_MCTL_MAIN_STS_FLAG Register (Offset = 170h) [reset = X]

DSI_MCTL_MAIN_STS_FLAG is shown in [Figure 7-84](#) and described in [Table 7-188](#).

Return to [Summary Table](#).

Main control status Flag registers. The use of these registers is related to status and error bits management (and interrupt too).

These bits are spread across different register banks. The exact use of the flag bit is described in the section : Error and status bits.

Table 7-187. DSI_MCTL_MAIN_STS_FLAG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0170h |

Figure 7-84. DSI_MCTL_MAIN_STS_FLAG Register

| | | | | | | | |
|------------------|------------------|-----------------|-----------------|-----------------|-----------------|-------------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | IF3_UNTERM_PCK_ERR_FLAG | IF1_UNTERM_PCK_ERR_FLAG |
| R-X | | | | | | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LPRX_TO_ERR_FLAG | HSTX_TO_ERR_FLAG | DAT4_READY_FLAG | DAT3_READY_FLAG | DAT2_READY_FLAG | DAT1_READY_FLAG | CLKLANE_READY_FLAG | PLL_LOCK_FLAG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-188. DSI_MCTL_MAIN_STS_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-10 | RESERVED | R | X | |
| 9 | IF3_UNTERM_PCK_ERR_FLAG | R | 0h | IF3_UNTERM_PCK_ERR_FLAG: flags if3_unterm_pck_err |
| 8 | IF1_UNTERM_PCK_ERR_FLAG | R | 0h | IF1_UNTERM_PCK_ERR_FLAG: flags if1_unterm_pck_err |
| 7 | LPRX_TO_ERR_FLAG | R | 0h | LPRX_TO_ERR_FLAG: flags lprx_to_err |
| 6 | HSTX_TO_ERR_FLAG | R | 0h | HSTX_TO_ERR_FLAG: flags hstx_to_err |
| 5 | DAT4_READY_FLAG | R | 0h | DAT4_READY_FLAG: flags dat4_ready |
| 4 | DAT3_READY_FLAG | R | 0h | DAT3_READY_FLAG: flags dat3_ready |
| 3 | DAT2_READY_FLAG | R | 0h | DAT2_READY_FLAG: flags dat2_ready |
| 2 | DAT1_READY_FLAG | R | 0h | DAT1_READY_FLAG: flags dat1_ready |
| 1 | CLKLANE_READY_FLAG | R | 0h | CLKLANE_READY_FLAG: flags clklane_ready |
| 0 | PLL_LOCK_FLAG | R | 0h | PLL_LOCK_FLAG: flags PLL lock |

7.2.69 DSI_CMD_MODE_STS_FLAG Register (Offset = 174h) [reset = X]

DSI_CMD_MODE_STS_FLAG is shown in [Figure 7-85](#) and described in [Table 7-190](#).

Return to [Summary Table](#).

Command Mode status

Table 7-189. DSI_CMD_MODE_STS_FLAG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0174h |

Figure 7-85. DSI_CMD_MODE_STS_FLAG Register

| | | | | | | | |
|----------|----|---------------------------|---------------------------|--------------------------|----------------------|--------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ERR_IF3_UND ERRUN_FLAG | ERR_IF1_UND ERRUN_FLAG | ERR_UNWANT ED_RD_FLAG | ERR_TE_MISS _FLAG | ERR_NO_TE_F LAG | CSM_RUNNIN G_FLAG |
| R-X | | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-190. DSI_CMD_MODE_STS_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|---|
| 31-6 | RESERVED | R | X | |
| 5 | ERR_IF3_UNDERRUN_F LAG | R | 0h | ERR_IF3_UNDERRUN_FLAG: flags err_if3_underrun |
| 4 | ERR_IF1_UNDERRUN_F LAG | R | 0h | ERR_IF1_UNDERRUN_FLAG: flags err_if1_underrun |
| 3 | ERR_UNWANTED_RD_F LAG | R | 0h | ERR_UNWANTED_RD_FLAG: flags fixed_err |
| 2 | ERR_TE_MISS_FLAG | R | 0h | ERR_TE_MISS_FLAG: flags err_te_miss |
| 1 | ERR_NO_TE_FLAG | R | 0h | ERR_NO_TE_FLAG: flags err_no_te |
| 0 | CSM_RUNNING_FLAG | R | 0h | CSM_RUNNING_FLAG: flags remaining_err |

7.2.70 DSI_DIRECT_CMD_STS_FLAG Register (Offset = 178h) [reset = X]

DSI_DIRECT_CMD_STS_FLAG is shown in [Figure 7-86](#) and described in [Table 7-192](#).

Return to [Summary Table](#).

Direct command mode status

**Table 7-191. DSI_DIRECT_CMD_STS_FLAG
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0178h |

Figure 7-86. DSI_DIRECT_CMD_STS_FLAG Register

| | | | | | | | |
|----------------------|---------------------------|------------------------------------|-----------------------------------|-------------------------|--------------------------------------|--------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | READ_COMPL ETED_WITH_E RR_FLAG | BTA_FINISHED _FLAG | BTA_COMPLE TED_FLAG |
| R-X | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TE_RECEIVED _FLAG | TRIGGER_REC EIVED_FLAG | ACK_WITH_ER R_RECEIVED_ FLAG | ACKNOWLEDG E_RECEIVED_ FLAG | READ_COMPL ETED_FLAG | TRIGGER_CO MPLETED_FLA G | WRITE_COMP LETED_FLAG | CMD_TRANSM ISSION_FLAG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-192. DSI_DIRECT_CMD_STS_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10 | READ_COMPLETED_WI TH_ERR_FLAG | R | 0h | READ_COMPLETED_WITH_ERR_FLAG: flags detection of read completed with errors |
| 9 | BTA_FINISHED_FLAG | R | 0h | BTA_FINISHED_FLAG: flags BTA completion detection |
| 8 | BTA_COMPLETED_FLAG | R | 0h | BTA_COMPLETED_FLAG: flags BTA request completed |
| 7 | TE_RECEIVED_FLAG | R | 0h | TE_RECEIVED_FLAG: flags TE received |
| 6 | TRIGGER_RECEIVED_F LAG | R | 0h | TRIGGER_RECEIVED_FLAG: flags trigger |
| 5 | ACK_WITH_ERR_RECEI VED_FLAG | R | 0h | ACK_WITH_ERR_RECEIVED_FLAG: flag acknowledge with error detection |
| 4 | ACKNOWLEDGE_RECEI VED_FLAG | R | 0h | ACKNOWLEDGE_RECEIVED_FLAG: flags acknowledge |
| 3 | READ_COMPLETED_FL AG | R | 0h | READ_COMPLETED_FLAG: flags read request completed |
| 2 | TRIGGER_COMPLETED_ FLAG | R | 0h | TRIGGER_COMPLETED_FLAG: flags trigger request completed |
| 1 | WRITE_COMPLETED_FL AG | R | 0h | WRITE_COMPLETED_FLAG: flags detection of write request completed |

Table 7-192. DSI_DIRECT_CMD_STS_FLAG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 0 | CMD_TRANSMISSION_FLAG | R | 0h | CMD_TRANSMISSION_FLAG: flags cmd_transmission |

7.2.71 DSI_DIRECT_CMD_RD_STS_FLAG Register (Offset = 17Ch) [reset = X]

DSI_DIRECT_CMD_RD_STS_FLAG is shown in [Figure 7-87](#) and described in [Table 7-194](#).

Return to [Summary Table](#).

Direct command read status bits

**Table 7-193. DSI_DIRECT_CMD_RD_STS_FLAG
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 017Ch |

Figure 7-87. DSI_DIRECT_CMD_RD_STS_FLAG Register

| | | | | | | | |
|--------------------------|---------------------------|-----------------------|----------------------|--------------------------|-----------------------|--------------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ERR_EOT_WIT H_ERR_FLAG |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_MISSING _EOT_FLAG | ERR_WRONG_ LENGTH_FLAG | ERR_OVERSIZ E_FLAG | ERR_RECEIVE _FLAG | ERR_UNDECO DABLE_FLAG | ERR_CHECKS UM_FLAG | ERR_UNCORR ECTABLE_FLA G | ERR_FIXED_F LAG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-194. DSI_DIRECT_CMD_RD_STS_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|---|
| 31-9 | RESERVED | R | X | |
| 8 | ERR_EOT_WITH_ERR_F LAG | R | 0h | ERR_EOT_WITH_ERR_FLAG: flags err_eot_with_err |
| 7 | ERR_MISSING_EOT_FLA G | R | 0h | ERR_MISSING_EOT_FLAG: flags err_missing_eot |
| 6 | ERR_WRONG_LENGTH_ FLAG | R | 0h | ERR_WRONG_LENGTH_FLAG: flags err_wrong_length |
| 5 | ERR_OVERSIZE_FLAG | R | 0h | ERR_OVERSIZE_FLAG: flags err_oversize |
| 4 | ERR_RECEIVE_FLAG | R | 0h | ERR_RECEIVE_FLAG: flags err_receive |
| 3 | ERR_UNDECODABLE_F LAG | R | 0h | ERR_UNDECODABLE_FLAG: flags err_undecodable |
| 2 | ERR_CHECKSUM_FLAG | R | 0h | ERR_CHECKSUM_FLAG: flags err_checksum |
| 1 | ERR_UNCORRECTABLE _FLAG | R | 0h | ERR_UNCORRECTABLE_FLAG: flags err_uncorrectable |
| 0 | ERR_FIXED_FLAG | R | 0h | ERR_FIXED_FLAG: flags err_fixed |

7.2.72 DSI_VID_MODE_STS_FLAG Register (Offset = 180h) [reset = X]

DSI_VID_MODE_STS_FLAG is shown in [Figure 7-88](#) and described in [Table 7-196](#).

Return to [Summary Table](#).

Video Mode status flag

Table 7-195. DSI_VID_MODE_STS_FLAG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0180h |

Figure 7-88. DSI_VID_MODE_STS_FLAG Register

| | | | | | | | |
|--------------------|---------------------|-----------------------|-----------------------|---------------------|------------------------|---------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | FLAG_VSG_RECOVERY | ERR_VRS_WRONG_LENGTH_FLAG | ERR_LONGREAD_FLAG |
| R-X | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_LONGWRITE_FLAG | ERR_SHORTWRITE_FLAG | ERR_SMALL_HEIGHT_FLAG | ERR_SMALL_LENGTH_FLAG | ERR_MISS_VSYNC_FLAG | ERR_MISSING_HSYNC_FLAG | ERR_MISSING_DATA_FLAG | VSG_STS_FLAG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-196. DSI_VID_MODE_STS_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10 | FLAG_VSG_RECOVERY | R | 0h | FLAG_VSG_RECOVERY: lags vsg_recovery |
| 9 | ERR_VRS_WRONG_LENGTH_FLAG | R | 0h | ERR_VRS_WRONG_LENGTH_FLAG: flags err_vrs_wrong_length |
| 8 | ERR_LONGREAD_FLAG | R | 0h | ERR_LONGREAD_FLAG: flags err_longread |
| 7 | ERR_LONGWRITE_FLAG | R | 0h | ERR_LONGWRITE_FLAG: flags err_longwrite |
| 6 | ERR_SHORTWRITE_FLAG | R | 0h | ERR_SHORTWRITE_FLAG: flags err_shortwrite |
| 5 | ERR_SMALL_HEIGHT_FLAG | R | 0h | ERR_SMALL_HEIGHT_FLAG: flags the detection of unaligned line number |
| 4 | ERR_SMALL_LENGTH_FLAG | R | 0h | ERR_SMALL_LENGTH_FLAG: flags the detection of unaligned size |
| 3 | ERR_MISS_VSYNC_FLAG | R | 0h | ERR_MISS_VSYNC_FLAG: flags missing VSYNC |
| 2 | ERR_MISSING_HSYNC_FLAG | R | 0h | ERR_MISSING_HSYNC_FLAG: flags missing HSYNC |
| 1 | ERR_MISSING_DATA_FLAG | R | 0h | ERR_MISSING_DATA_FLAG: flags data miss |
| 0 | VSG_STS_FLAG | R | 0h | VSG_STS_FLAG: flags VSG status |

7.2.73 DSI_TG_STS_FLAG Register (Offset = 184h) [reset = X]

DSI_TG_STS_FLAG is shown in [Figure 7-89](#) and described in [Table 7-198](#).

Return to [Summary Table](#).

TVG status Flags

Table 7-197. DSI_TG_STS_FLAG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0184h |

Figure 7-89. DSI_TG_STS_FLAG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | TVG_STS_FLAG |
| R-X | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-198. DSI_TG_STS_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-1 | RESERVED | R | X | |
| 0 | TVG_STS_FLAG | R | 0h | TVG_STS_FLAG: Indicates TVG status observation |

7.2.74 DSI_MCTL_DPHY_ERR_FLAG Register (Offset = 188h) [reset = X]

DSI_MCTL_DPHY_ERR_FLAG is shown in [Figure 7-90](#) and described in [Table 7-200](#).

Return to [Summary Table](#).

Errors output from D_PHY lanes - flags error bit

Table 7-199. DSI_MCTL_DPHY_ERR_FLAG Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0188h |

Figure 7-90. DSI_MCTL_DPHY_ERR_FLAG Register

| | | | | | | | |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ERR_CONT_L P1_4_FLAG | ERR_CONT_L P1_3_FLAG |
| R-X | | | | | | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_CONT_L P1_2_FLAG | ERR_CONT_L P1_1_FLAG | ERR_CONT_L P0_4_FLAG | ERR_CONT_L P0_3_FLAG | ERR_CONT_L P0_2_FLAG | ERR_CONT_L P0_1_FLAG | ERR_CONTRO L_4_FLAG | ERR_CONTRO L_3_FLAG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ERR_CONTRO L_2_FLAG | ERR_CONTRO L_1_FLAG | ERR_SYNCES C_4_FLAG | ERR_SYNCES C_3_FLAG | ERR_SYNCES C_2_FLAG | ERR_SYNCES C_1_FLAG | ERR_ESC_4_F LAG | ERR_ESC_3_F LAG |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_ESC_2_F LAG | ERR_ESC_1_F LAG | RESERVED | | | | | |
| R-0h | R-0h | R-X | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-200. DSI_MCTL_DPHY_ERR_FLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---------------------|
| 31-26 | RESERVED | R | X | |
| 25 | ERR_CONT_LP1_4_FLAG | R | 0h | ERR_CONT_LP1_4_FLAG |
| 24 | ERR_CONT_LP1_3_FLAG | R | 0h | ERR_CONT_LP1_3_FLAG |
| 23 | ERR_CONT_LP1_2_FLAG | R | 0h | ERR_CONT_LP1_2_FLAG |
| 22 | ERR_CONT_LP1_1_FLAG | R | 0h | ERR_CONT_LP1_1_FLAG |
| 21 | ERR_CONT_LP0_4_FLAG | R | 0h | ERR_CONT_LP0_4_FLAG |
| 20 | ERR_CONT_LP0_3_FLAG | R | 0h | ERR_CONT_LP0_3_FLAG |
| 19 | ERR_CONT_LP0_2_FLAG | R | 0h | ERR_CONT_LP0_2_FLAG |
| 18 | ERR_CONT_LP0_1_FLAG | R | 0h | ERR_CONT_LP0_1_FLAG |
| 17 | ERR_CONTROL_4_FLAG | R | 0h | ERR_CONTROL_4_FLAG |
| 16 | ERR_CONTROL_3_FLAG | R | 0h | ERR_CONTROL_3_FLAG |

Table 7-200. DSI_MCTL_DPHY_ERR_FLAG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--------------------|
| 15 | ERR_CONTROL_2_FLAG | R | 0h | ERR_CONTROL_2_FLAG |
| 14 | ERR_CONTROL_1_FLAG | R | 0h | ERR_CONTROL_1_FLAG |
| 13 | ERR_SYNCESC_4_FLAG | R | 0h | ERR_SYNCESC_4_FLAG |
| 12 | ERR_SYNCESC_3_FLAG | R | 0h | ERR_SYNCESC_3_FLAG |
| 11 | ERR_SYNCESC_2_FLAG | R | 0h | ERR_SYNCESC_2_FLAG |
| 10 | ERR_SYNCESC_1_FLAG | R | 0h | ERR_SYNCESC_1_FLAG |
| 9 | ERR_ESC_4_FLAG | R | 0h | ERR_ESC_4_FLAG |
| 8 | ERR_ESC_3_FLAG | R | 0h | ERR_ESC_3_FLAG |
| 7 | ERR_ESC_2_FLAG | R | 0h | ERR_ESC_2_FLAG |
| 6 | ERR_ESC_1_FLAG | R | 0h | ERR_ESC_1_FLAG |
| 5-0 | RESERVED | R | X | |

7.2.75 DSI_DPI_IRQ_EN Register (Offset = 1A0h) [reset = X]

DSI_DPI_IRQ_EN is shown in [Figure 7-91](#) and described in [Table 7-202](#).

Return to [Summary Table](#).

DPI interrupt enable

Table 7-201. DSI_DPI_IRQ_EN Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 01A0h |

Figure 7-91. DSI_DPI_IRQ_EN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PIXEL_BUF_OVERFLOW_IRQ_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-202. DSI_DPI_IRQ_EN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|------------------------------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | PIXEL_BUF_OVERFLOW_IRQ_EN | R/W | 0h | Enable DPI FIFO Overflow interrupt |

7.2.76 DSI_DPI_IRQ_CLR Register (Offset = 1A4h) [reset = X]

DSI_DPI_IRQ_CLR is shown in [Figure 7-92](#) and described in [Table 7-204](#).

Return to [Summary Table](#).

DPI interrupt clear register

Table 7-203. DSI_DPI_IRQ_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 01A4h |

Figure 7-92. DSI_DPI_IRQ_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PIXEL_BUF_O VERFLOW_IR Q_CLR |
| W-X | | | | | | | W-0h |

LEGEND: W = Write Only; -n = value after reset

Table 7-204. DSI_DPI_IRQ_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------|------|-------|-----------------------------------|
| 31-1 | RESERVED | W | X | |
| 0 | PIXEL_BUF_OVERFLOW _IRQ_CLR | W | 0h | Clear DPI FIFO Overflow interrupt |

7.2.77 DSI_DPI_IRQ_STS Register (Offset = 1A8h) [reset = X]

DSI_DPI_IRQ_STS is shown in [Figure 7-93](#) and described in [Table 7-206](#).

Return to [Summary Table](#).

DPI interrupt status

Table 7-205. DSI_DPI_IRQ_STS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 01A8h |

Figure 7-93. DSI_DPI_IRQ_STS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PIXEL_BUF_O VERFLOW_ST S |
| R-X | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-206. DSI_DPI_IRQ_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|---------------------------------------|
| 31-1 | RESERVED | R | X | |
| 0 | PIXEL_BUF_OVERFLOW_STS | R | 0h | Status of DPI FIFO Overflow interrupt |

7.2.78 DSI_DPI_CFG Register (Offset = 1ACh) [reset = 08000000h]

DSI_DPI_CFG is shown in [Figure 7-94](#) and described in [Table 7-208](#).

Return to [Summary Table](#).

DPI interface configuration information

Table 7-207. DSI_DPI_CFG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 01ACh |

Figure 7-94. DSI_DPI_CFG Register

| | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DPI_CFG_FIFODEPTH | | | | | | | | | | | | | | | |
| R-800h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPI_CFG_FIFO_LEVEL | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-208. DSI_DPI_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-16 | DPI_CFG_FIFODEPTH | R | 800h | DPI FIFO depth - configuration paramter |
| 15-0 | DPI_CFG_FIFO_LEVEL | R | 0h | DPI FIFO fill level - can be read mid-line for debug purposes, to allow adjustment of settings |

7.2.79 DSI_TEST_GENERIC Register (Offset = 1F0h) [reset = 0h]

DSI_TEST_GENERIC is shown in [Figure 7-95](#) and described in [Table 7-210](#).

Return to [Summary Table](#).

Generic test control and status register

Table 7-209. DSI_TEST_GENERIC Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 01F0h |

Figure 7-95. DSI_TEST_GENERIC Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| STATUS | | | | | | | | | | | | | | | | CTRL | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-210. DSI_TEST_GENERIC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|--|
| 31-16 | STATUS | R | 0h | Test status - Value of test_generic_status input |
| 15-0 | CTRL | R/W | 0h | Test control - Drives test_generic_ctrl output |

7.2.80 DSI_ID_REG Register (Offset = 1FCh) [reset = CADD5131h]

DSI_ID_REG is shown in [Figure 7-96](#) and described in [Table 7-212](#).

Return to [Summary Table](#).

ID register for Controller

Table 7-211. DSI_ID_REG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 01FCh |

Figure 7-96. DSI_ID_REG Register

| | | | | | | | | | | | | | | | |
|----------------|----|----|----|--------------|----|----|----|-------|----|----|----|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REV_VENDOR_ID | | | | | | | | | | | | REV_PRODUCT_ID | | | |
| R-CADh | | | | | | | | | | | | R-D5h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REV_PRODUCT_ID | | | | REV_HARDWARE | | | | REV_X | | | | REV_Y | | | |
| R-D5h | | | | R-1h | | | | R-3h | | | | R-1h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-212. DSI_ID_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-20 | REV_VENDOR_ID | R | CADh | VENDOR_ID: IP vendor ID affected to IP [reset = 0xCAD]. |
| 19-12 | REV_PRODUCT_ID | R | D5h | PRODUCT_ID: unique IP identifier within IP portfolio [reset = 0xD5]. |
| 11-8 | REV_HARDWARE | R | 1h | H: Hardware revision number [reset = 0x1]. |
| 7-4 | REV_X | R | 3h | X: Major revision value [reset = 0x3]. |
| 3-0 | REV_Y | R | 1h | Y: Minor revision value [reset = 0x1]. |

7.2.81 DSI_ASF_INT_STATUS Register (Offset = 200h) [reset = 0h]

DSI_ASF_INT_STATUS is shown in [Figure 7-97](#) and described in [Table 7-214](#).

Return to [Summary Table](#).

ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_int_fatal or asf_int_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 7-213. DSI_ASF_INT_STATUS Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0200h |

Figure 7-97. DSI_ASF_INT_STATUS Register

| | | | | | | | |
|----------|-------------------|------------------|-----------------------------|-------------|-------------|----------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_TIMEOUT_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORRECTABLE_ERR | ASF_SRAM_CORRECTABLE_ERR |
| R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-214. DSI_ASF_INT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W1C | 0h | Integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR | R/W1C | 0h | Protocol error interrupt |
| 4 | ASF_TRANSACTION_TIMEOUT_ERR | R/W1C | 0h | Transaction timeouts error interrupt |
| 3 | ASF_CSR_ERR | R/W1C | 0h | Configuration and status registers error interrupt |
| 2 | ASF_DAP_ERR | R/W1C | 0h | Data and address paths parity error interrupt |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR | R/W1C | 0h | SRAM uncorrectable error interrupt |
| 0 | ASF_SRAM_CORRECTABLE_ERR | R/W1C | 0h | SRAM correctable error interrupt |

7.2.82 DSI_ASF_INT_RAW_STATUS Register (Offset = 204h) [reset = 0h]

DSI_ASF_INT_RAW_STATUS is shown in [Figure 7-98](#) and described in [Table 7-216](#).

Return to [Summary Table](#).

ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 7-215. DSI_ASF_INT_RAW_STATUS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0204h |

Figure 7-98. DSI_ASF_INT_RAW_STATUS Register

| | | | | | | | |
|----------|-------------------|------------------|-----------------------------|-------------|-------------|----------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_TIMEOUT_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORRECTABLE_ERR | ASF_SRAM_CORRECTABLE_ERR |
| R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-216. DSI_ASF_INT_RAW_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W1C | 0h | Integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR | R/W1C | 0h | Protocol error interrupt |
| 4 | ASF_TRANSACTION_TIMEOUT_ERR | R/W1C | 0h | Transaction timeouts error interrupt |
| 3 | ASF_CSR_ERR | R/W1C | 0h | Configuration and status registers error interrupt |
| 2 | ASF_DAP_ERR | R/W1C | 0h | Data and address paths parity error interrupt |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR | R/W1C | 0h | SRAM uncorrectable error interrupt |
| 0 | ASF_SRAM_CORRECTABLE_ERR | R/W1C | 0h | SRAM correctable error interrupt |

7.2.83 DSI_ASF_INT_MASK Register (Offset = 208h) [reset = 7Fh]

DSI_ASF_INT_MASK is shown in [Figure 7-99](#) and described in [Table 7-218](#).

Return to [Summary Table](#).

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt.

Table 7-217. DSI_ASF_INT_MASK Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0208h |

Figure 7-99. DSI_ASF_INT_MASK Register

| | | | | | | | |
|----------|------------------------|-----------------------|--------------------------|------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR_MASK | ASF_PROTOCOL_ERR_MASK | ASF_TRANSACTION_ERR_MASK | ASF_CSR_ERR_MASK | ASF_DAP_ERR_MASK | ASF_SRAM_UNCORR_ERR_MASK | ASF_SRAM_CORR_ERR_MASK |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-218. DSI_ASF_INT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR_MASK | R/W | 1h | Mask bit for integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR_MASK | R/W | 1h | Mask bit for protocol error interrupt. |
| 4 | ASF_TRANSACTION_ERR_MASK | R/W | 1h | Mask bit for transaction timeouts error interrupt. |
| 3 | ASF_CSR_ERR_MASK | R/W | 1h | Mask bit for configuration and status registers error interrupt. |
| 2 | ASF_DAP_ERR_MASK | R/W | 1h | Mask bit for data and address paths parity error interrupt. |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR_MASK | R/W | 1h | Mask bit for SRAM uncorrectable error interrupt. |
| 0 | ASF_SRAM_CORRECTABLE_ERR_MASK | R/W | 1h | Mask bit for SRAM correctable error interrupt. |

7.2.84 DSI_ASF_INT_TEST Register (Offset = 20Ch) [reset = 0h]

DSI_ASF_INT_TEST is shown in [Figure 7-100](#) and described in [Table 7-220](#).

Return to [Summary Table](#).

The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrupt accordingly.

Table 7-219. DSI_ASF_INT_TEST Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 020Ch |

Figure 7-100. DSI_ASF_INT_TEST Register

| | | | | | | | |
|----------|------------------------|-----------------------|----------------------------------|------------------|------------------|---------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR_TEST | ASF_PROTOCOL_ERR_TEST | ASF_TRANSACTION_TIMEOUT_ERR_TEST | ASF_CSR_ERR_TEST | ASF_DAP_ERR_TEST | ASF_SRAM_UNCORRECTABLE_ERR_TEST | ASF_SRAM_CORRECTABLE_ERR_TEST |
| R-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 7-220. DSI_ASF_INT_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR_TEST | W | 0h | Test bit for integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR_TEST | W | 0h | Test bit for protocol error interrupt. |
| 4 | ASF_TRANSACTION_TIMEOUT_ERR_TEST | W | 0h | Test bit for transaction timeouts error interrupt. |
| 3 | ASF_CSR_ERR_TEST | W | 0h | Test bit for configuration and status registers error interrupt. |
| 2 | ASF_DAP_ERR_TEST | W | 0h | Test bit for data and address paths parity error interrupt. |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR_TEST | W | 0h | Test bit for SRAM uncorrectable error interrupt. |
| 0 | ASF_SRAM_CORRECTABLE_ERR_TEST | W | 0h | Test bit for SRAM correctable error interrupt. |

7.2.85 DSI_ASF_FATAL_NONFATAL_SELECT Register (Offset = 210h) [reset = 7Fh]

DSI_ASF_FATAL_NONFATAL_SELECT is shown in [Figure 7-101](#) and described in [Table 7-222](#).

Return to [Summary Table](#).

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered.

Table 7-221. DSI_ASF_FATAL_NONFATAL_SELECT Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0210h |

Figure 7-101. DSI_ASF_FATAL_NONFATAL_SELECT Register

| | | | | | | | |
|----------|-------------------|------------------|-----------------------------|-------------|-------------|----------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_TIMEOUT_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORRECTABLE_ERR | ASF_SRAM_CORRECTABLE_ERR |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 7-222. DSI_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|---|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W | 1h | Enable integrity error interrupt as fatal |
| 5 | ASF_PROTOCOL_ERR | R/W | 1h | Enable protocol error interrupt as fatal. |
| 4 | ASF_TRANSACTION_TIMEOUT_ERR | R/W | 1h | Enable transaction timeouts error interrupt as fatal. |
| 3 | ASF_CSR_ERR | R/W | 1h | Enable configuration and status registers error interrupt as fatal. |
| 2 | ASF_DAP_ERR | R/W | 1h | Enable data and address paths parity error interrupt as fatal. |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR | R/W | 1h | Enable SRAM uncorrectable error interrupt as fatal. |
| 0 | ASF_SRAM_CORRECTABLE_ERR | R/W | 1h | Enable SRAM correctable error interrupt as fatal. |

7.2.86 DSI_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 220h) [reset = 0h]

DSI_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 7-102](#) and described in [Table 7-224](#).

Return to [Summary Table](#).

Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active.

Table 7-223.
DSI_ASF_SRAM_CORR_FAULT_STATUS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0220h |

Figure 7-102. DSI_ASF_SRAM_CORR_FAULT_STATUS Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|--------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_CORR_FAULT_INST | | | | | | | | ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-224. DSI_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-24 | ASF_SRAM_CORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. |
| 23-0 | ASF_SRAM_CORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault. |

7.2.87 DSI_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 224h) [reset = 0h]

DSI_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 7-103](#) and described in [Table 7-226](#).

Return to [Summary Table](#).

Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active.

Table 7-225.
DSI_ASF_SRAM_UNCORR_FAULT_STATUS
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0224h |

Figure 7-103. DSI_ASF_SRAM_UNCORR_FAULT_STATUS Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_SRAM_UNCORR_FAULT_INST | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-226. DSI_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-24 | ASF_SRAM_UNCORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. |
| 23-0 | ASF_SRAM_UNCORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault. |

7.2.88 DSI_ASF_SRAM_FAULT_STATS Register (Offset = 228h) [reset = 0h]

DSI_ASF_SRAM_FAULT_STATS is shown in [Figure 7-104](#) and described in [Table 7-228](#).

Return to [Summary Table](#).

Statistics register for SRAM faults. Note that this register clears when software writes to any field.

Table 7-227. DSI_ASF_SRAM_FAULT_STATS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0228h |

Figure 7-104. DSI_ASF_SRAM_FAULT_STATS Register

| | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_FAULT_CORR_STATS | | | | | | | | | | | | | | | |
| R/W1C-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-228. DSI_ASF_SRAM_FAULT_STATS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|-------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 15-0 | ASF_SRAM_FAULT_CORR_STATS | R/W1C | 0h | Count of number of correctable errors if implemented. Count value will saturate at 0xffff. |

7.2.89 DSI_ASF_TRANS_TO_CTRL Register (Offset = 230h) [reset = X]

DSI_ASF_TRANS_TO_CTRL is shown in [Figure 7-105](#) and described in [Table 7-230](#).

Return to [Summary Table](#).

Control register to configure the ASF transaction timeout monitors.

Table 7-229. DSI_ASF_TRANS_TO_CTRL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0230h |

Figure 7-105. DSI_ASF_TRANS_TO_CTRL Register

| | | | | | | | |
|---------------------|----------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_TRANS_T O_EN | RESERVED | | | | | | |
| R/W-0h | R/W-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-230. DSI_ASF_TRANS_TO_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31 | ASF_TRANS_TO_EN | R/W | 0h | Enable transaction timeout monitoring. |
| 30-16 | RESERVED | R/W | X | |
| 15-0 | ASF_TRANS_TO_CTRL | R/W | 0h | Timer value to use for transaction timeout monitor. |

7.2.90 DSI_ASF_TRANS_TO_FAULT_MASK Register (Offset = 234h) [reset = X]

DSI_ASF_TRANS_TO_FAULT_MASK is shown in [Figure 7-106](#) and described in [Table 7-232](#).

Return to [Summary Table](#).

Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 7-231. DSI_ASF_TRANS_TO_FAULT_MASK Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0234h |

Figure 7-106. DSI_ASF_TRANS_TO_FAULT_MASK Register

| | | | | | | | |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ASF_TRANS_TO_FAULT_3_MASK | ASF_TRANS_TO_FAULT_2_MASK | ASF_TRANS_TO_FAULT_1_MASK | ASF_TRANS_TO_FAULT_0_MASK |
| R/W-X | | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-232. DSI_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3 | ASF_TRANS_TO_FAULT_3_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 2 | ASF_TRANS_TO_FAULT_2_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 1 | ASF_TRANS_TO_FAULT_1_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 0 | ASF_TRANS_TO_FAULT_0_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |

7.2.91 DSI_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 238h) [reset = X]

DSI_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 7-107](#) and described in [Table 7-234](#).

Return to [Summary Table](#).

Status register for transaction timeouts fault. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit.

Table 7-233. DSI_ASF_TRANS_TO_FAULT_STATUS Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0238h |

Figure 7-107. DSI_ASF_TRANS_TO_FAULT_STATUS Register

| | | | | | | | |
|----------|----|----|----|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ASF_TRANS_TO_FAULT_3_STATUS | ASF_TRANS_TO_FAULT_2_STATUS | ASF_TRANS_TO_FAULT_1_STATUS | ASF_TRANS_TO_FAULT_0_STATUS |
| R/W-X | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-234. DSI_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3 | ASF_TRANS_TO_FAULT_3_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 2 | ASF_TRANS_TO_FAULT_2_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 1 | ASF_TRANS_TO_FAULT_1_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 0 | ASF_TRANS_TO_FAULT_0_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |

7.2.92 DSI_ASF_PROTOCOL_FAULT_MASK Register (Offset = 240h) [reset = X]

DSI_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 7-108](#) and described in [Table 7-236](#).

Return to [Summary Table](#).

Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

**Table 7-235. DSI_ASF_PROTOCOL_FAULT_MASK
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_D SI_0_DSI | 0480 0240h |

Figure 7-108. DSI_ASF_PROTOCOL_FAULT_MASK Register

| | | | | | | | |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ASF_PROTOL_FAULT_3_MASK | ASF_PROTOL_FAULT_2_MASK | ASF_PROTOL_FAULT_1_MASK | ASF_PROTOL_FAULT_0_MASK |
| R/W-X | | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-236. DSI_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3 | ASF_PROTOCOL_FAULT_3_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 2 | ASF_PROTOCOL_FAULT_2_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 1 | ASF_PROTOCOL_FAULT_1_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 0 | ASF_PROTOCOL_FAULT_0_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |

7.2.93 DSI_ASF_PROTOCOL_FAULT_STATUS Register (Offset = 244h) [reset = X]

DSI_ASF_PROTOCOL_FAULT_STATUS is shown in [Figure 7-109](#) and described in [Table 7-238](#).

Return to [Summary Table](#).

Status register for protocol faults. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit

Table 7-237. DSI_ASF_PROTOCOL_FAULT_STATUS Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| DSS_DSI0_DSI_TOP_VBUSP_CFG_DSI_0_DSI | 0480 0244h |

Figure 7-109. DSI_ASF_PROTOCOL_FAULT_STATUS Register

| | | | | | | | |
|----------|----|----|----|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ASF_PROTOCOL_FAULT_3_STATUS | ASF_PROTOCOL_FAULT_2_STATUS | ASF_PROTOCOL_FAULT_1_STATUS | ASF_PROTOCOL_FAULT_0_STATUS |
| R/W-X | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-238. DSI_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|----------------------------------|
| 31-4 | RESERVED | R/W | X | |
| 3 | ASF_PROTOCOL_FAULT_3_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 2 | ASF_PROTOCOL_FAULT_2_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 1 | ASF_PROTOCOL_FAULT_1_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 0 | ASF_PROTOCOL_FAULT_0_STATUS | R/W1C | 0h | Status bits for protocol faults. |

7.3 DSI_WRAP Registers

Table 7-240 lists the memory-mapped registers for the DSI_WRAP. All register offset addresses not listed in Table 7-240 should be considered as reserved locations and the register contents should not be modified.

MMR registers for DSS DSI wrapper

Table 7-239. DSI_WRAP Instances

| Instance | Base Address |
|--|--------------|
| DSS_DSI0_DSI_WRAP_MMR_VBUSB_CFG_DSI_WRAP | 0471 0000h |

Table 7-240. DSI_WRAP Registers

| Offset | Acronym | Register Name | DSS_DSI0_DSI_WRAP_MMR_VBUSB_CFG_DSI_WRAP Physical Address |
|--------|---|------------------|---|
| 0h | DSI_WRAP_REVISION | Revision | 0471 0000h |
| 4h | DSI_WRAP_DPI_CONTROL | DPI Control | 0471 0004h |
| 8h | DSI_WRAP_DSC_CONTROL | DSC Control | 0471 0008h |
| Ch | DSI_WRAP_DPI_SECURE | DPI Secure | 0471 000Ch |
| 10h | DSI_WRAP_DSI_0_ASF_STATUS | DSI 0 ASF status | 0471 0010h |

7.3.1 DSI_WRAP_REVISION Register (Offset = 0h) [reset = 640A1101h]

DSI_WRAP_REVISION is shown in [Figure 7-110](#) and described in [Table 7-242](#).

Return to [Summary Table](#).

The REVISION register contains the DSI revision number and PID

Table 7-241. DSI_WRAP_REVISION Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_WRAP_MMR_VBUSP_CFG_DSI_WRAP | 0471 0000h |

Figure 7-110. DSI_WRAP_REVISION Register

| | | | | | | | | | | | | | | | |
|---------|----|----|----|----------|----|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MODID | | | | | | | | | | | | | | | |
| R-640Ah | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | REVMAJOR | | | | CUSTOM | | REVMIN | | | | | |
| R-2h | | | | R-1h | | | | R-0h | | R-1h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 7-242. DSI_WRAP_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-----------------|
| 31-16 | MODID | R | 640Ah | Module ID Field |
| 15-11 | REVRTL | R | 2h | RTL Revision |
| 10-8 | REVMAJOR | R | 1h | Major Revision |
| 7-6 | CUSTOM | R | 0h | Custom |
| 5-0 | REVMIN | R | 1h | Minor Revision |

7.3.2 DSI_WRAP_DPI_CONTROL Register (Offset = 4h) [reset = X]

DSI_WRAP_DPI_CONTROL is shown in [Figure 7-111](#) and described in [Table 7-244](#).

Return to [Summary Table](#).

Controls the DPI Video Input ports of the DSI Wrapper

Table 7-243. DSI_WRAP_DPI_CONTROL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_WRAP_MMR_VBUSP_CFG_DSI_WRAP | 0471 0004h |

Figure 7-111. DSI_WRAP_DPI_CONTROL Register

| | | | | | | | |
|----------|----|----|--------------|----------|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | RESERVED |
| R/W-X | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | DSI2_MUX_SEL | RESERVED | | | DPI_0_EN |
| R/W-X | | | R/W-0h | R/W-X | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-244. DSI_WRAP_DPI_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-9 | RESERVED | R/W | X | |
| 8 | RESERVED | R/W | 0h | Reserved |
| 7-5 | RESERVED | R/W | X | |
| 4 | DSI2_MUX_SEL | R/W | 0h | Select between DPI-1 and DPI-2 to drive the DPI input of DSITX2 0h = DPI-1 is selected 1h = DPI-2 is selected |
| 3-1 | RESERVED | R/W | X | |
| 0 | DPI_0_EN | R/W | 0h | Enable for DPI-0 input 0h = DPI-0 is disabled 1h = DPI-0 is enabled |

7.3.3 DSI_WRAP_DSC_CONTROL Register (Offset = 8h) [reset = X]

DSI_WRAP_DSC_CONTROL is shown in [Figure 7-112](#) and described in [Table 7-246](#).

Return to [Summary Table](#).

Controls the DSC Encoder for DSI

Table 7-245. DSI_WRAP_DSC_CONTROL Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_WRAP_MMR_VBUSP_CFG_DSI_WRAP | 0471 0008h |

Figure 7-112. DSI_WRAP_DSC_CONTROL Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |

LEGEND:-n = value after reset

Table 7-246. DSI_WRAP_DSC_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-0 | RESERVED | R/W | X | |

7.3.4 DSI_WRAP_DPI_SECURE Register (Offset = Ch) [reset = X]

DSI_WRAP_DPI_SECURE is shown in [Figure 7-113](#) and described in [Table 7-248](#).

Return to [Summary Table](#).

Controls the DPI Video Input ports SECURE settings

Table 7-247. DSI_WRAP_DPI_SECURE Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_WRAP_MMR_VBUSP_CFG_DSI_WRAP | 0471 000Ch |

Figure 7-113. DSI_WRAP_DPI_SECURE Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------------|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DPI_0_SECURE_VIOLATION | DPI_0_SECURE |
| R/W-X | | | | | | R/W1C-0h | R/W-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 7-248. DSI_WRAP_DPI_SECURE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|--|
| 31-2 | RESERVED | R/W | X | |
| 1 | DPI_0_SECURE_VIOLATION | R/W1C | 0h | SECURE VIOLATION status for DPI-0 input. Write-1 to clear the status 0h = DPI-0 secure settings are ok 1h = DPI-0 secure settings are not ok, data is discarded |
| 0 | DPI_0_SECURE | R/W | 0h | SECURE bit for DPI-0 input 0h = DPI-0 is non-secure 1h = DPI-0 is secure |

7.3.5 DSI_WRAP_DSI_0_ASF_STATUS Register (Offset = 10h) [reset = X]

DSI_WRAP_DSI_0_ASF_STATUS is shown in [Figure 7-114](#) and described in [Table 7-250](#).

Return to [Summary Table](#).

ASF Status

Table 7-249. DSI_WRAP_DSI_0_ASF_STATUS Instances

| Instance | Physical Address |
|--|------------------|
| DSS_DSI0_DSI_WRAP_MMR_VBUSP_CFG_DSI_WRAP | 0471 0010h |

Figure 7-114. DSI_WRAP_DSI_0_ASF_STATUS Register

| | | | | | | | |
|----------|---------------|--------------|--------------|---------|---------|-----------------|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | INTEGRITY_ERR | PROTOCOL_ERR | TRANS_TO_ERR | CSR_ERR | DAP_ERR | SRAM_UNCORR_ERR | SRAM_CORR_ERR |
| R-X | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 7-250. DSI_WRAP_DSI_0_ASF_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-----------------|
| 31-7 | RESERVED | R | X | |
| 6 | INTEGRITY_ERR | R | 0h | INTEGRITY_ERR |
| 5 | PROTOCOL_ERR | R | 0h | PROTOCOL_ERR |
| 4 | TRANS_TO_ERR | R | 0h | TRANS_TO_ERR |
| 3 | CSR_ERR | R | 0h | CSR_ERR |
| 2 | DAP_ERR | R | 0h | DAP_ERR |
| 1 | SRAM_UNCORR_ERR | R | 0h | SRAM_UNCORR_ERR |
| 0 | SRAM_CORR_ERR | R | 0h | SRAM_CORR_ERR |

8 EDP Registers

This section describes the EDP registers.

8.1 EDP_ECC_CORE Registers

Table 8-2 lists the memory-mapped registers for the EDP_ECC_CORE. All register offset addresses not listed in Table 8-2 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. EDP_ECC_CORE Instances

| Instance | Base Address |
|---|--------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0000h |

Table 8-2. EDP_ECC_CORE Registers

| Offset | Acronym | Register Name | DSS_EDP0_MHDPTX_WRAPPER_ECC_AGGR_CORE_CFG Physical Address |
|---------------|--|---|---|
| 0h | EDP_ECC_CORE_REV | Aggregator Revision Register | 02AC 0000h |
| 8h | EDP_ECC_CORE_VECTOR | ECC Vector Register | 02AC 0008h |
| Ch | EDP_ECC_CORE_STAT | Misc Status | 02AC 000Ch |
| 10h + formula | EDP_ECC_CORE_RESERVED_SVBUS_y | Reserved Area for Serial VBUS Registers | 02AC 0010h + formula |
| 3Ch | EDP_ECC_CORE_SEC_EOI_REG | EOI Register | 02AC 003Ch |
| 40h | EDP_ECC_CORE_SEC_STATUS_REG0 | Interrupt Status Register 0 | 02AC 0040h |
| 80h | EDP_ECC_CORE_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02AC 0080h |
| C0h | EDP_ECC_CORE_SEC_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02AC 00C0h |
| 13Ch | EDP_ECC_CORE_DED_EOI_REG | EOI Register | 02AC 013Ch |
| 140h | EDP_ECC_CORE_DED_STATUS_REG0 | Interrupt Status Register 0 | 02AC 0140h |
| 180h | EDP_ECC_CORE_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02AC 0180h |
| 1C0h | EDP_ECC_CORE_DED_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02AC 01C0h |
| 200h | EDP_ECC_CORE_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 02AC 0200h |
| 204h | EDP_ECC_CORE_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 02AC 0204h |
| 208h | EDP_ECC_CORE_AGGR_STATUS_SET | AGGR interrupt status set Register | 02AC 0208h |
| 20Ch | EDP_ECC_CORE_AGGR_STATUS_CLR | AGGR interrupt status clear Register | 02AC 020Ch |

8.1.1 EDP_ECC_CORE_REV Register (Offset = 0h) [reset = 66A0EA00h]

EDP_ECC_CORE_REV is shown in [Figure 8-1](#) and described in [Table 8-4](#).

Return to [Summary Table](#).

Revision parameters

Table 8-3. EDP_ECC_CORE_REV Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0000h |

Figure 8-1. EDP_ECC_CORE_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-4. EDP_ECC_CORE_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

8.1.2 EDP_ECC_CORE_VECTOR Register (Offset = 8h) [reset = X]

EDP_ECC_CORE_VECTOR is shown in [Figure 8-2](#) and described in [Table 8-6](#).

Return to [Summary Table](#).

ECC EDP_ECC_CORE_VECTOR Register

Table 8-5. EDP_ECC_CORE_VECTOR Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0008h |

Figure 8-2. EDP_ECC_CORE_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_D ONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R/W-X | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-6. EDP_ECC_CORE_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or status |

8.1.3 EDP_ECC_CORE_STAT Register (Offset = Ch) [reset = X]

EDP_ECC_CORE_STAT is shown in [Figure 8-3](#) and described in [Table 8-8](#).

[Return to Summary Table.](#)

Misc Status

Table 8-7. EDP_ECC_CORE_STAT Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 000Ch |

Figure 8-3. EDP_ECC_CORE_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | | | | R-3h | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-8. EDP_ECC_CORE_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 3h | Indicates the number of RAMs serviced by the ECC aggregator |

8.1.4 EDP_ECC_CORE_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

EDP_ECC_CORE_RESERVED_SVBUS_y is shown in [Figure 8-4](#) and described in [Table 8-10](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

**Table 8-9. EDP_ECC_CORE_RESERVED_SVBUS_y
Instances**

| Instance | Physical Address |
|---|----------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0010h + formula |

Figure 8-4. EDP_ECC_CORE_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-10. EDP_ECC_CORE_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

8.1.5 EDP_ECC_CORE_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

EDP_ECC_CORE_SEC_EOI_REG is shown in [Figure 8-5](#) and described in [Table 8-12](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-11. EDP_ECC_CORE_SEC_EOI_REG Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 003Ch |

Figure 8-5. EDP_ECC_CORE_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-12. EDP_ECC_CORE_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

8.1.6 EDP_ECC_CORE_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

EDP_ECC_CORE_SEC_STATUS_REG0 is shown in [Figure 8-6](#) and described in [Table 8-14](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 8-13. EDP_ECC_CORE_SEC_STATUS_REG0
Instances**

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0040h |

Figure 8-6. EDP_ECC_CORE_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|---------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | EDC_CTRL_PEND | RAMECC_DRAM_PEND | RAMECC_IRAM_PEND |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-14. EDP_ECC_CORE_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|---|
| 31-3 | RESERVED | R/W | X | |
| 2 | EDC_CTRL_PEND | R/W1S | 0h | Interrupt Pending Status for edc_ctrl_pend |
| 1 | RAMECC_DRAM_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_dram_pend |
| 0 | RAMECC_IRAM_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_iram_pend |

8.1.7 EDP_ECC_CORE_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

EDP_ECC_CORE_SEC_ENABLE_SET_REG0 is shown in [Figure 8-7](#) and described in [Table 8-16](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 8-15.
EDP_ECC_CORE_SEC_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0080h |

Figure 8-7. EDP_ECC_CORE_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|--------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | EDC_CTRL_EN ABLE_SET | RAMECC_DRA M_ENABLE_SE T | RAMECC_IRA M_ENABLE_SE T |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-16. EDP_ECC_CORE_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | EDC_CTRL_ENABLE_SE T | R/W1S | 0h | Interrupt Enable Set Register for edc_ctrl_pend |
| 1 | RAMECC_DRAM_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_dram_pend |
| 0 | RAMECC_IRAM_ENABLE _SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_iram_pend |

8.1.8 EDP_ECC_CORE_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

EDP_ECC_CORE_SEC_ENABLE_CLR_REG0 is shown in [Figure 8-8](#) and described in [Table 8-18](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 8-17.
EDP_ECC_CORE_SEC_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 00C0h |

Figure 8-8. EDP_ECC_CORE_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|--------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | EDC_CTRL_EN ABLE_CLR | RAMECC_DRA M_ENABLE_CL R | RAMECC_IRA M_ENABLE_CL R |
| R/W-X | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-18. EDP_ECC_CORE_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | EDC_CTRL_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for edc_ctrl_pend |
| 1 | RAMECC_DRAM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_dram_pend |
| 0 | RAMECC_IRAM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_iram_pend |

8.1.9 EDP_ECC_CORE_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

EDP_ECC_CORE_DED_EOI_REG is shown in [Figure 8-9](#) and described in [Table 8-20](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-19. EDP_ECC_CORE_DED_EOI_REG Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 013Ch |

Figure 8-9. EDP_ECC_CORE_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-20. EDP_ECC_CORE_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

8.1.10 EDP_ECC_CORE_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

EDP_ECC_CORE_DED_STATUS_REG0 is shown in [Figure 8-10](#) and described in [Table 8-22](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 8-21. EDP_ECC_CORE_DED_STATUS_REG0
Instances**

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0140h |

Figure 8-10. EDP_ECC_CORE_DED_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|---------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | EDC_CTRL_PEND | RAMECC_DRAM_PEND | RAMECC_IRAM_PEND |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-22. EDP_ECC_CORE_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|---|
| 31-3 | RESERVED | R/W | X | |
| 2 | EDC_CTRL_PEND | R/W1S | 0h | Interrupt Pending Status for edc_ctrl_pend |
| 1 | RAMECC_DRAM_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_dram_pend |
| 0 | RAMECC_IRAM_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_iram_pend |

8.1.11 EDP_ECC_CORE_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

EDP_ECC_CORE_DED_ENABLE_SET_REG0 is shown in [Figure 8-11](#) and described in [Table 8-24](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 8-23.
EDP_ECC_CORE_DED_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0180h |

Figure 8-11. EDP_ECC_CORE_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|--------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | EDC_CTRL_EN ABLE_SET | RAMECC_DRA M_ENABLE_SE T | RAMECC_IRA M_ENABLE_SE T |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-24. EDP_ECC_CORE_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | EDC_CTRL_ENABLE_SE T | R/W1S | 0h | Interrupt Enable Set Register for edc_ctrl_pend |
| 1 | RAMECC_DRAM_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_dram_pend |
| 0 | RAMECC_IRAM_ENABLE _SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_iram_pend |

8.1.12 EDP_ECC_CORE_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

EDP_ECC_CORE_DED_ENABLE_CLR_REG0 is shown in [Figure 8-12](#) and described in [Table 8-26](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 8-25.
EDP_ECC_CORE_DED_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 01C0h |

Figure 8-12. EDP_ECC_CORE_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|--------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | EDC_CTRL_EN ABLE_CLR | RAMECC_DRA M_ENABLE_CL R | RAMECC_IRA M_ENABLE_CL R |
| R/W-X | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-26. EDP_ECC_CORE_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | EDC_CTRL_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for edc_ctrl_pend |
| 1 | RAMECC_DRAM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_dram_pend |
| 0 | RAMECC_IRAM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_iram_pend |

8.1.13 EDP_ECC_CORE_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

EDP_ECC_CORE_AGGR_ENABLE_SET is shown in [Figure 8-13](#) and described in [Table 8-28](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 8-27. EDP_ECC_CORE_AGGR_ENABLE_SET Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 0200h |

Figure 8-13. EDP_ECC_CORE_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-28. EDP_ECC_CORE_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

8.1.14 EDP_ECC_CORE_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

EDP_ECC_CORE_AGGR_ENABLE_CLR is shown in [Figure 8-14](#) and described in [Table 8-30](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 8-29. EDP_ECC_CORE_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC_C_AGGR_CORE_CFG | 02AC 0204h |

Figure 8-14. EDP_ECC_CORE_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-30. EDP_ECC_CORE_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

8.1.15 EDP_ECC_CORE_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

EDP_ECC_CORE_AGGR_STATUS_SET is shown in [Figure 8-15](#) and described in [Table 8-32](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 8-31. EDP_ECC_CORE_AGGR_STATUS_SET Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC_C_AGGR_CORE_CFG | 02AC 0208h |

Figure 8-15. EDP_ECC_CORE_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 8-32. EDP_ECC_CORE_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt status set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt status set for parity errors |

8.1.16 EDP_ECC_CORE_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

EDP_ECC_CORE_AGGR_STATUS_CLR is shown in [Figure 8-16](#) and described in [Table 8-34](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

**Table 8-33. EDP_ECC_CORE_AGGR_STATUS_CLR
Instances**

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_CORE_CFG | 02AC 020Ch |

Figure 8-16. EDP_ECC_CORE_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 8-34. EDP_ECC_CORE_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt status clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt status clear for parity errors |

8.2 EDP_ECC_DSC Registers

Table 8-36 lists the memory-mapped registers for the EDP_ECC_DSC. All register offset addresses not listed in Table 8-36 should be considered as reserved locations and the register contents should not be modified.

Table 8-35. EDP_ECC_DSC Instances

| Instance | Base Address |
|--|--------------|
| DSS_EDP0_MHDPTX_WRAPPER_ECC_AGGR_DSC_CFG | 02AC 2000h |

Table 8-36. EDP_ECC_DSC Registers

| Offset | Acronym | Register Name | DSS_EDP0_MHDPTX_WRAPPER_ECC_AGGR_DSC_CFG Physical Address |
|-----------------|---|---|--|
| 2000h | EDP_ECC_DSC_REV | Aggregator Revision Register | 02AC 2000h |
| 2008h | EDP_ECC_DSC_VECTOR | ECC Vector Register | 02AC 2008h |
| 200Ch | EDP_ECC_DSC_STAT | Misc Status | 02AC 200Ch |
| 2010h + formula | EDP_ECC_DSC_RESERVED_SVBUS_y | Reserved Area for Serial VBUS Registers | 02AC 2010h + formula |
| 203Ch | EDP_ECC_DSC_SEC_EOI_REG | EOI Register | 02AC 203Ch |
| 2040h | EDP_ECC_DSC_SEC_STATUS_REG0 | Interrupt Status Register 0 | 02AC 2040h |
| 2080h | EDP_ECC_DSC_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02AC 2080h |
| 20C0h | EDP_ECC_DSC_SEC_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02AC 20C0h |
| 213Ch | EDP_ECC_DSC_DED_EOI_REG | EOI Register | 02AC 213Ch |
| 2140h | EDP_ECC_DSC_DED_STATUS_REG0 | Interrupt Status Register 0 | 02AC 2140h |
| 2180h | EDP_ECC_DSC_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02AC 2180h |
| 21C0h | EDP_ECC_DSC_DED_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02AC 21C0h |
| 2200h | EDP_ECC_DSC_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 02AC 2200h |
| 2204h | EDP_ECC_DSC_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 02AC 2204h |
| 2208h | EDP_ECC_DSC_AGGR_STATUS_SET | AGGR interrupt status set Register | 02AC 2208h |
| 220Ch | EDP_ECC_DSC_AGGR_STATUS_CLR | AGGR interrupt status clear Register | 02AC 220Ch |

8.2.1 EDP_ECC_DSC_REV Register (Offset = 2000h) [reset = 66A0EA00h]

EDP_ECC_DSC_REV is shown in [Figure 8-17](#) and described in [Table 8-38](#).

[Return to Summary Table.](#)

Revision parameters

Table 8-37. EDP_ECC_DSC_REV Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2000h |

Figure 8-17. EDP_ECC_DSC_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-38. EDP_ECC_DSC_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

8.2.2 EDP_ECC_DSC_VECTOR Register (Offset = 2008h) [reset = X]

EDP_ECC_DSC_VECTOR is shown in [Figure 8-18](#) and described in [Table 8-40](#).

Return to [Summary Table](#).

ECC EDP_ECC_DSC_VECTOR Register

Table 8-39. EDP_ECC_DSC_VECTOR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2008h |

Figure 8-18. EDP_ECC_DSC_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_D ONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R/W-X | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-40. EDP_ECC_DSC_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or status |

8.2.3 EDP_ECC_DSC_STAT Register (Offset = 200Ch) [reset = X]

EDP_ECC_DSC_STAT is shown in [Figure 8-19](#) and described in [Table 8-42](#).

Return to [Summary Table](#).

Misc Status

Table 8-41. EDP_ECC_DSC_STAT Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 200Ch |

Figure 8-19. EDP_ECC_DSC_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | | | | R-8h | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-42. EDP_ECC_DSC_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 8h | Indicates the number of RAMs serviced by the ECC aggregator |

8.2.4 EDP_ECC_DSC_RESERVED_SVBUS_y Register (Offset = 2010h + formula) [reset = 0h]

EDP_ECC_DSC_RESERVED_SVBUS_y is shown in [Figure 8-20](#) and described in [Table 8-44](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 2010h + (y * 4h); where y = 0h to 7h

Table 8-43. EDP_ECC_DSC_RESERVED_SVBUS_y Instances

| Instance | Physical Address |
|--|----------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGRESSIVE_CFG | 02AC 2010h + formula |

Figure 8-20. EDP_ECC_DSC_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-44. EDP_ECC_DSC_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

8.2.5 EDP_ECC_DSC_SEC_EOI_REG Register (Offset = 203Ch) [reset = X]

EDP_ECC_DSC_SEC_EOI_REG is shown in [Figure 8-21](#) and described in [Table 8-46](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 8-45. EDP_ECC_DSC_SEC_EOI_REG
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 203Ch |

Figure 8-21. EDP_ECC_DSC_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-46. EDP_ECC_DSC_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

8.2.6 EDP_ECC_DSC_SEC_STATUS_REG0 Register (Offset = 2040h) [reset = X]

EDP_ECC_DSC_SEC_STATUS_REG0 is shown in [Figure 8-22](#) and described in [Table 8-48](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 8-47. EDP_ECC_DSC_SEC_STATUS_REG0 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2040h |

Figure 8-22. EDP_ECC_DSC_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------------------|------------------------|------------------------|---------------------|----------------------|------------------------|------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMECC_ENC1_OB0_PEND | RAMECC_ENC1_SSM_D_PEND | RAMECC_ENC1_SSM_S_PEND | RAMECC_ENC1_LB_PEND | RAMECC_ENC0_OB0_PEND | RAMECC_ENC0_SSM_D_PEND | RAMECC_ENC0_SSM_S_PEND | RAMECC_ENC0_LB_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-48. EDP_ECC_DSC_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | RAMECC_ENC1_OB0_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_ob0_pending |
| 6 | RAMECC_ENC1_SSM_D_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_ssm_d_pending |
| 5 | RAMECC_ENC1_SSM_S_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_ssm_s_pending |
| 4 | RAMECC_ENC1_LB_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_lb_pending |
| 3 | RAMECC_ENC0_OB0_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_ob0_pending |
| 2 | RAMECC_ENC0_SSM_D_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_ssm_d_pending |
| 1 | RAMECC_ENC0_SSM_S_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_ssm_s_pending |
| 0 | RAMECC_ENC0_LB_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_lb_pending |

8.2.7 EDP_ECC_DSC_SEC_ENABLE_SET_REG0 Register (Offset = 2080h) [reset = X]

EDP_ECC_DSC_SEC_ENABLE_SET_REG0 is shown in [Figure 8-23](#) and described in [Table 8-50](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 8-49.
EDP_ECC_DSC_SEC_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2080h |

Figure 8-23. EDP_ECC_DSC_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|--------------------------------|----------------------------------|----------------------------------|-------------------------------|--------------------------------|----------------------------------|----------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMECC_ENC1_OB0_ENAB LE_SET | RAMECC_ENC1_SSM_D_ENA BLE_SET | RAMECC_ENC1_SSM_S_ENA BLE_SET | RAMECC_ENC1_LB_ENAB LE_SET | RAMECC_ENC0_OB0_ENAB LE_SET | RAMECC_ENC0_SSM_D_ENA BLE_SET | RAMECC_ENC0_SSM_S_ENA BLE_SET | RAMECC_ENC0_LB_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-50. EDP_ECC_DSC_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | RAMECC_ENC1_OB0_E NABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_ob0_pend |
| 6 | RAMECC_ENC1_SSM_D _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_ssm_d_pend |
| 5 | RAMECC_ENC1_SSM_S _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_ssm_s_pend |
| 4 | RAMECC_ENC1_LB_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_lb_pend |
| 3 | RAMECC_ENC0_OB0_E NABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_ob0_pend |
| 2 | RAMECC_ENC0_SSM_D _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_ssm_d_pend |
| 1 | RAMECC_ENC0_SSM_S _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_ssm_s_pend |
| 0 | RAMECC_ENC0_LB_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_lb_pend |

8.2.8 EDP_ECC_DSC_SEC_ENABLE_CLR_REG0 Register (Offset = 20C0h) [reset = X]

EDP_ECC_DSC_SEC_ENABLE_CLR_REG0 is shown in [Figure 8-24](#) and described in [Table 8-52](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 8-51.
EDP_ECC_DSC_SEC_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 20C0h |

Figure 8-24. EDP_ECC_DSC_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------------------------|------------------------------|------------------------------|---------------------------|----------------------------|------------------------------|------------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMECC_ENC1_OB0_ENABLE_CLR | RAMECC_ENC1_SSM_D_ENABLE_CLR | RAMECC_ENC1_SSM_S_ENABLE_CLR | RAMECC_ENC1_LB_ENABLE_CLR | RAMECC_ENC0_OB0_ENABLE_CLR | RAMECC_ENC0_SSM_D_ENABLE_CLR | RAMECC_ENC0_SSM_S_ENABLE_CLR | RAMECC_ENC0_LB_ENABLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-52. EDP_ECC_DSC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | RAMECC_ENC1_OB0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_ob0_pend |
| 6 | RAMECC_ENC1_SSM_D_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_ssm_d_pend |
| 5 | RAMECC_ENC1_SSM_S_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_ssm_s_pend |
| 4 | RAMECC_ENC1_LB_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_lb_pend |
| 3 | RAMECC_ENC0_OB0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_ob0_pend |
| 2 | RAMECC_ENC0_SSM_D_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_ssm_d_pend |
| 1 | RAMECC_ENC0_SSM_S_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_ssm_s_pend |
| 0 | RAMECC_ENC0_LB_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_lb_pend |

8.2.9 EDP_ECC_DSC_DED_EOI_REG Register (Offset = 213Ch) [reset = X]

EDP_ECC_DSC_DED_EOI_REG is shown in [Figure 8-25](#) and described in [Table 8-54](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 8-53. EDP_ECC_DSC_DED_EOI_REG
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 213Ch |

Figure 8-25. EDP_ECC_DSC_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-54. EDP_ECC_DSC_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

8.2.10 EDP_ECC_DSC_DED_STATUS_REG0 Register (Offset = 2140h) [reset = X]

EDP_ECC_DSC_DED_STATUS_REG0 is shown in [Figure 8-26](#) and described in [Table 8-56](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 8-55. EDP_ECC_DSC_DED_STATUS_REG0 Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2140h |

Figure 8-26. EDP_ECC_DSC_DED_STATUS_REG0 Register

| | | | | | | | |
|----------------------|------------------------|------------------------|---------------------|----------------------|------------------------|------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMECC_ENC1_OB0_PEND | RAMECC_ENC1_SSM_D_PEND | RAMECC_ENC1_SSM_S_PEND | RAMECC_ENC1_LB_PEND | RAMECC_ENC0_OB0_PEND | RAMECC_ENC0_SSM_D_PEND | RAMECC_ENC0_SSM_S_PEND | RAMECC_ENC0_LB_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-56. EDP_ECC_DSC_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | RAMECC_ENC1_OB0_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_ob0_pending |
| 6 | RAMECC_ENC1_SSM_D_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_ssm_d_pending |
| 5 | RAMECC_ENC1_SSM_S_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_ssm_s_pending |
| 4 | RAMECC_ENC1_LB_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc1_lb_pending |
| 3 | RAMECC_ENC0_OB0_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_ob0_pending |
| 2 | RAMECC_ENC0_SSM_D_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_ssm_d_pending |
| 1 | RAMECC_ENC0_SSM_S_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_ssm_s_pending |
| 0 | RAMECC_ENC0_LB_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_enc0_lb_pending |

8.2.11 EDP_ECC_DSC_DED_ENABLE_SET_REG0 Register (Offset = 2180h) [reset = X]

EDP_ECC_DSC_DED_ENABLE_SET_REG0 is shown in [Figure 8-27](#) and described in [Table 8-58](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 8-57.
EDP_ECC_DSC_DED_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2180h |

Figure 8-27. EDP_ECC_DSC_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|--------------------------------|----------------------------------|----------------------------------|-------------------------------|--------------------------------|----------------------------------|----------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMECC_ENC1_OB0_ENAB LE_SET | RAMECC_ENC1_SSM_D_ENA BLE_SET | RAMECC_ENC1_SSM_S_ENA BLE_SET | RAMECC_ENC1_LB_ENAB LE_SET | RAMECC_ENC0_OB0_ENAB LE_SET | RAMECC_ENC0_SSM_D_ENA BLE_SET | RAMECC_ENC0_SSM_S_ENA BLE_SET | RAMECC_ENC0_LB_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-58. EDP_ECC_DSC_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | RAMECC_ENC1_OB0_E NABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_ob0_pend |
| 6 | RAMECC_ENC1_SSM_D _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_ssm_d_pend |
| 5 | RAMECC_ENC1_SSM_S _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_ssm_s_pend |
| 4 | RAMECC_ENC1_LB_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc1_lb_pend |
| 3 | RAMECC_ENC0_OB0_E NABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_ob0_pend |
| 2 | RAMECC_ENC0_SSM_D _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_ssm_d_pend |
| 1 | RAMECC_ENC0_SSM_S _ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_ssm_s_pend |
| 0 | RAMECC_ENC0_LB_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_enc0_lb_pend |

8.2.12 EDP_ECC_DSC_DED_ENABLE_CLR_REG0 Register (Offset = 21C0h) [reset = X]

EDP_ECC_DSC_DED_ENABLE_CLR_REG0 is shown in [Figure 8-28](#) and described in [Table 8-60](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 8-59.
EDP_ECC_DSC_DED_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 21C0h |

Figure 8-28. EDP_ECC_DSC_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------------------------|------------------------------|------------------------------|---------------------------|----------------------------|------------------------------|------------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAMECC_ENC1_OB0_ENABLE_CLR | RAMECC_ENC1_SSM_D_ENABLE_CLR | RAMECC_ENC1_SSM_S_ENABLE_CLR | RAMECC_ENC1_LB_ENABLE_CLR | RAMECC_ENC0_OB0_ENABLE_CLR | RAMECC_ENC0_SSM_D_ENABLE_CLR | RAMECC_ENC0_SSM_S_ENABLE_CLR | RAMECC_ENC0_LB_ENABLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-60. EDP_ECC_DSC_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | RAMECC_ENC1_OB0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_ob0_pend |
| 6 | RAMECC_ENC1_SSM_D_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_ssm_d_pend |
| 5 | RAMECC_ENC1_SSM_S_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_ssm_s_pend |
| 4 | RAMECC_ENC1_LB_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc1_lb_pend |
| 3 | RAMECC_ENC0_OB0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_ob0_pend |
| 2 | RAMECC_ENC0_SSM_D_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_ssm_d_pend |
| 1 | RAMECC_ENC0_SSM_S_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_ssm_s_pend |
| 0 | RAMECC_ENC0_LB_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_enc0_lb_pend |

8.2.13 EDP_ECC_DSC_AGGR_ENABLE_SET Register (Offset = 2200h) [reset = X]

EDP_ECC_DSC_AGGR_ENABLE_SET is shown in [Figure 8-29](#) and described in [Table 8-62](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

**Table 8-61. EDP_ECC_DSC_AGGR_ENABLE_SET
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2200h |

Figure 8-29. EDP_ECC_DSC_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-62. EDP_ECC_DSC_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

8.2.14 EDP_ECC_DSC_AGGR_ENABLE_CLR Register (Offset = 2204h) [reset = X]

EDP_ECC_DSC_AGGR_ENABLE_CLR is shown in [Figure 8-30](#) and described in [Table 8-64](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 8-63. EDP_ECC_DSC_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2204h |

Figure 8-30. EDP_ECC_DSC_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-64. EDP_ECC_DSC_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

8.2.15 EDP_ECC_DSC_AGGR_STATUS_SET Register (Offset = 2208h) [reset = X]

EDP_ECC_DSC_AGGR_STATUS_SET is shown in [Figure 8-31](#) and described in [Table 8-66](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 8-65. EDP_ECC_DSC_AGGR_STATUS_SET Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_DSC_CFG | 02AC 2208h |

Figure 8-31. EDP_ECC_DSC_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 8-66. EDP_ECC_DSC_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt status set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt status set for parity errors |

8.2.16 EDP_ECC_DSC_AGGR_STATUS_CLR Register (Offset = 220Ch) [reset = X]

EDP_ECC_DSC_AGGR_STATUS_CLR is shown in [Figure 8-32](#) and described in [Table 8-68](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 8-67. EDP_ECC_DSC_AGGR_STATUS_CLR Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC_C_AGGR_DSC_CFG | 02AC 220Ch |

Figure 8-32. EDP_ECC_DSC_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 8-68. EDP_ECC_DSC_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt status clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt status clear for parity errors |

8.3 EDP_ECC_PHY Registers

Table 8-70 lists the memory-mapped registers for the EDP_ECC_PHY. All register offset addresses not listed in Table 8-70 should be considered as reserved locations and the register contents should not be modified.

Table 8-69. EDP_ECC_PHY Instances

| Instance | Base Address |
|--|--------------|
| DSS_EDP0_MHDPTX_WRAPPER_ECC_AGGR_PHY_CFG | 02AC 1000h |

Table 8-70. EDP_ECC_PHY Registers

| Offset | Acronym | Register Name | DSS_EDP0_MHDPTX_WRAPPER_ECC_AGGR_PHY_CFG Physical Address |
|-----------------|---|---|--|
| 1000h | EDP_ECC_PHY_REV | Aggregator Revision Register | 02AC 1000h |
| 1008h | EDP_ECC_PHY_VECTOR | ECC Vector Register | 02AC 1008h |
| 100Ch | EDP_ECC_PHY_STAT | Misc Status | 02AC 100Ch |
| 1010h + formula | EDP_ECC_PHY_RESERVED_SVBUS_y | Reserved Area for Serial VBUS Registers | 02AC 1010h + formula |
| 103Ch | EDP_ECC_PHY_SEC_EOI_REG | EOI Register | 02AC 103Ch |
| 1040h | EDP_ECC_PHY_SEC_STATUS_REG0 | Interrupt Status Register 0 | 02AC 1040h |
| 1080h | EDP_ECC_PHY_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02AC 1080h |
| 10C0h | EDP_ECC_PHY_SEC_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02AC 10C0h |
| 113Ch | EDP_ECC_PHY_DED_EOI_REG | EOI Register | 02AC 113Ch |
| 1140h | EDP_ECC_PHY_DED_STATUS_REG0 | Interrupt Status Register 0 | 02AC 1140h |
| 1180h | EDP_ECC_PHY_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02AC 1180h |
| 11C0h | EDP_ECC_PHY_DED_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02AC 11C0h |
| 1200h | EDP_ECC_PHY_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 02AC 1200h |
| 1204h | EDP_ECC_PHY_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 02AC 1204h |
| 1208h | EDP_ECC_PHY_AGGR_STATUS_SET | AGGR interrupt status set Register | 02AC 1208h |
| 120Ch | EDP_ECC_PHY_AGGR_STATUS_CLR | AGGR interrupt status clear Register | 02AC 120Ch |

8.3.1 EDP_ECC_PHY_REV Register (Offset = 1000h) [reset = 66A0EA00h]

EDP_ECC_PHY_REV is shown in [Figure 8-33](#) and described in [Table 8-72](#).

Return to [Summary Table](#).

Revision parameters

Table 8-71. EDP_ECC_PHY_REV Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1000h |

Figure 8-33. EDP_ECC_PHY_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-72. EDP_ECC_PHY_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

8.3.2 EDP_ECC_PHY_VECTOR Register (Offset = 1008h) [reset = X]

EDP_ECC_PHY_VECTOR is shown in [Figure 8-34](#) and described in [Table 8-74](#).

Return to [Summary Table](#).

ECC EDP_ECC_PHY_VECTOR Register

Table 8-73. EDP_ECC_PHY_VECTOR Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1008h |

Figure 8-34. EDP_ECC_PHY_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_D ONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R/W-X | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-74. EDP_ECC_PHY_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or status |

8.3.3 EDP_ECC_PHY_STAT Register (Offset = 100Ch) [reset = X]

EDP_ECC_PHY_STAT is shown in [Figure 8-35](#) and described in [Table 8-76](#).

[Return to Summary Table.](#)

Misc Status

Table 8-75. EDP_ECC_PHY_STAT Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 100Ch |

Figure 8-35. EDP_ECC_PHY_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | R-5h | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-76. EDP_ECC_PHY_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 5h | Indicates the number of RAMs serviced by the ECC aggregator |

8.3.4 EDP_ECC_PHY_RESERVED_SVBUS_y Register (Offset = 1010h + formula) [reset = 0h]

EDP_ECC_PHY_RESERVED_SVBUS_y is shown in [Figure 8-36](#) and described in [Table 8-78](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 1010h + (y * 4h); where y = 0h to 7h

**Table 8-77. EDP_ECC_PHY_RESERVED_SVBUS_y
Instances**

| Instance | Physical Address |
|--|----------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1010h + formula |

Figure 8-36. EDP_ECC_PHY_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-78. EDP_ECC_PHY_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

8.3.5 EDP_ECC_PHY_SEC_EOI_REG Register (Offset = 103Ch) [reset = X]

EDP_ECC_PHY_SEC_EOI_REG is shown in [Figure 8-37](#) and described in [Table 8-80](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-79. EDP_ECC_PHY_SEC_EOI_REG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 103Ch |

Figure 8-37. EDP_ECC_PHY_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-80. EDP_ECC_PHY_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

8.3.6 EDP_ECC_PHY_SEC_STATUS_REG0 Register (Offset = 1040h) [reset = X]

EDP_ECC_PHY_SEC_STATUS_REG0 is shown in [Figure 8-38](#) and described in [Table 8-82](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 8-81. EDP_ECC_PHY_SEC_STATUS_REG0
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1040h |

Figure 8-38. EDP_ECC_PHY_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|-------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RAMECC_AIF_ MEM_PEND | RAMECC_PKT_ _MEM_3_PEN D | RAMECC_PKT_ _MEM_2_PEN D | RAMECC_PKT_ _MEM_1_PEN D | RAMECC_PKT_ _MEM_0_PEN D |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-82. EDP_ECC_PHY_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | RAMECC_AIF_MEM_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_aif_mem_pend |
| 3 | RAMECC_PKT_MEM_3_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_3_pend |
| 2 | RAMECC_PKT_MEM_2_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_2_pend |
| 1 | RAMECC_PKT_MEM_1_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_1_pend |
| 0 | RAMECC_PKT_MEM_0_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_0_pend |

8.3.7 EDP_ECC_PHY_SEC_ENABLE_SET_REG0 Register (Offset = 1080h) [reset = X]

EDP_ECC_PHY_SEC_ENABLE_SET_REG0 is shown in [Figure 8-39](#) and described in [Table 8-84](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 8-83.
EDP_ECC_PHY_SEC_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1080h |

Figure 8-39. EDP_ECC_PHY_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|---------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RAMECC_AIF_MEM_ENABLE_SET | RAMECC_PKT_MEM_3_ENABLE_SET | RAMECC_PKT_MEM_2_ENABLE_SET | RAMECC_PKT_MEM_1_ENABLE_SET | RAMECC_PKT_MEM_0_ENABLE_SET |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-84. EDP_ECC_PHY_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | RAMECC_AIF_MEM_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_aif_mem_pend |
| 3 | RAMECC_PKT_MEM_3_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_3_pend |
| 2 | RAMECC_PKT_MEM_2_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_2_pend |
| 1 | RAMECC_PKT_MEM_1_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_1_pend |
| 0 | RAMECC_PKT_MEM_0_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_0_pend |

8.3.8 EDP_ECC_PHY_SEC_ENABLE_CLR_REG0 Register (Offset = 10C0h) [reset = X]

EDP_ECC_PHY_SEC_ENABLE_CLR_REG0 is shown in [Figure 8-40](#) and described in [Table 8-86](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 8-85.
EDP_ECC_PHY_SEC_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 10C0h |

Figure 8-40. EDP_ECC_PHY_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|---------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RAMECC_AIF_MEM_ENABLE_CLR | RAMECC_PKT_MEM_3_ENA_BLE_CLR | RAMECC_PKT_MEM_2_ENA_BLE_CLR | RAMECC_PKT_MEM_1_ENA_BLE_CLR | RAMECC_PKT_MEM_0_ENA_BLE_CLR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-86. EDP_ECC_PHY_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | RAMECC_AIF_MEM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_aif_mem_pend |
| 3 | RAMECC_PKT_MEM_3_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_3_pend |
| 2 | RAMECC_PKT_MEM_2_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_2_pend |
| 1 | RAMECC_PKT_MEM_1_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_1_pend |
| 0 | RAMECC_PKT_MEM_0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_0_pend |

8.3.9 EDP_ECC_PHY_DED_EOI_REG Register (Offset = 113Ch) [reset = X]

EDP_ECC_PHY_DED_EOI_REG is shown in [Figure 8-41](#) and described in [Table 8-88](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 8-87. EDP_ECC_PHY_DED_EOI_REG Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 113Ch |

Figure 8-41. EDP_ECC_PHY_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-88. EDP_ECC_PHY_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

8.3.10 EDP_ECC_PHY_DED_STATUS_REG0 Register (Offset = 1140h) [reset = X]

EDP_ECC_PHY_DED_STATUS_REG0 is shown in [Figure 8-42](#) and described in [Table 8-90](#).

Return to [Summary Table](#).

Interrupt Status Register 0

**Table 8-89. EDP_ECC_PHY_DED_STATUS_REG0
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1140h |

Figure 8-42. EDP_ECC_PHY_DED_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|-------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RAMECC_AIF_ MEM_PEND | RAMECC_PKT_ _MEM_3_PEN D | RAMECC_PKT_ _MEM_2_PEN D | RAMECC_PKT_ _MEM_1_PEN D | RAMECC_PKT_ _MEM_0_PEN D |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-90. EDP_ECC_PHY_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | RAMECC_AIF_MEM_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_aif_mem_pend |
| 3 | RAMECC_PKT_MEM_3_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_3_pend |
| 2 | RAMECC_PKT_MEM_2_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_2_pend |
| 1 | RAMECC_PKT_MEM_1_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_1_pend |
| 0 | RAMECC_PKT_MEM_0_PEND | R/W1S | 0h | Interrupt Pending Status for ramecc_pkt_mem_0_pend |

8.3.11 EDP_ECC_PHY_DED_ENABLE_SET_REG0 Register (Offset = 1180h) [reset = X]

EDP_ECC_PHY_DED_ENABLE_SET_REG0 is shown in [Figure 8-43](#) and described in [Table 8-92](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 8-91.
EDP_ECC_PHY_DED_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1180h |

Figure 8-43. EDP_ECC_PHY_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|---------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RAMECC_AIF_MEM_ENABLE_SET | RAMECC_PKT_MEM_3_ENABLE_SET | RAMECC_PKT_MEM_2_ENABLE_SET | RAMECC_PKT_MEM_1_ENABLE_SET | RAMECC_PKT_MEM_0_ENABLE_SET |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-92. EDP_ECC_PHY_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | RAMECC_AIF_MEM_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_aif_mem_pend |
| 3 | RAMECC_PKT_MEM_3_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_3_pend |
| 2 | RAMECC_PKT_MEM_2_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_2_pend |
| 1 | RAMECC_PKT_MEM_1_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_1_pend |
| 0 | RAMECC_PKT_MEM_0_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ramecc_pkt_mem_0_pend |

8.3.12 EDP_ECC_PHY_DED_ENABLE_CLR_REG0 Register (Offset = 11C0h) [reset = X]

EDP_ECC_PHY_DED_ENABLE_CLR_REG0 is shown in [Figure 8-44](#) and described in [Table 8-94](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 8-93.
EDP_ECC_PHY_DED_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 11C0h |

Figure 8-44. EDP_ECC_PHY_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|---------------------------|------------------------------|------------------------------|------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | RAMECC_AIF_MEM_ENABLE_CLR | RAMECC_PKT_MEM_3_ENA_BLE_CLR | RAMECC_PKT_MEM_2_ENA_BLE_CLR | RAMECC_PKT_MEM_1_ENA_BLE_CLR | RAMECC_PKT_MEM_0_ENA_BLE_CLR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-94. EDP_ECC_PHY_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | RAMECC_AIF_MEM_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_aif_mem_pend |
| 3 | RAMECC_PKT_MEM_3_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_3_pend |
| 2 | RAMECC_PKT_MEM_2_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_2_pend |
| 1 | RAMECC_PKT_MEM_1_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_1_pend |
| 0 | RAMECC_PKT_MEM_0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ramecc_pkt_mem_0_pend |

8.3.13 EDP_ECC_PHY_AGGR_ENABLE_SET Register (Offset = 1200h) [reset = X]

EDP_ECC_PHY_AGGR_ENABLE_SET is shown in [Figure 8-45](#) and described in [Table 8-96](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 8-95. EDP_ECC_PHY_AGGR_ENABLE_SET Instances

| Instance | Physical Address |
|---|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC_C_AGGR_PHY_CFG | 02AC 1200h |

Figure 8-45. EDP_ECC_PHY_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 8-96. EDP_ECC_PHY_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

8.3.14 EDP_ECC_PHY_AGGR_ENABLE_CLR Register (Offset = 1204h) [reset = X]

EDP_ECC_PHY_AGGR_ENABLE_CLR is shown in [Figure 8-46](#) and described in [Table 8-98](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

**Table 8-97. EDP_ECC_PHY_AGGR_ENABLE_CLR
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1204h |

Figure 8-46. EDP_ECC_PHY_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 8-98. EDP_ECC_PHY_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

8.3.15 EDP_ECC_PHY_AGGR_STATUS_SET Register (Offset = 1208h) [reset = X]

EDP_ECC_PHY_AGGR_STATUS_SET is shown in [Figure 8-47](#) and described in [Table 8-100](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

Table 8-99. EDP_ECC_PHY_AGGR_STATUS_SET Instances

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 1208h |

Figure 8-47. EDP_ECC_PHY_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 8-100. EDP_ECC_PHY_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt status set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt status set for parity errors |

8.3.16 EDP_ECC_PHY_AGGR_STATUS_CLR Register (Offset = 120Ch) [reset = X]

EDP_ECC_PHY_AGGR_STATUS_CLR is shown in [Figure 8-48](#) and described in [Table 8-102](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

**Table 8-101. EDP_ECC_PHY_AGGR_STATUS_CLR
Instances**

| Instance | Physical Address |
|--|------------------|
| DSS_EDP0_MHDPTX_WRAPPER_EC C_AGGR_PHY_CFG | 02AC 120Ch |

Figure 8-48. EDP_ECC_PHY_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 8-102. EDP_ECC_PHY_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt status clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt status clear for parity errors |

8.4 EDP_CFG Registers

Table 8-104 lists the memory-mapped registers for the EDP_CFG registers. All register offset addresses not listed in Table 8-104 should be considered as reserved locations and the register contents should not be modified.

MMR registers for eDP wrapper MMR

Table 8-103. EDP_CFG Instances

| Instance | Base Address |
|----------------------|--------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0000h |

Table 8-104. EDP_CFG Registers

| Offset | Acronym | Register Name | DSS_EDP0_INTG_CFG_VP Physical Address |
|--------|--|---------------|--|
| 0h | EDP_REVISION | | 04F4 0000h |
| 4h | EDP_DPTX_IPCFG | | 04F4 0004h |
| 8h | EDP_ECC_MEM_CFG | | 04F4 0008h |
| Ch | EDP_DPTX_DSC_CFG | | 04F4 000Ch |
| 10h | EDP_DPTX_SRC_CFG | | 04F4 0010h |
| 14h | EDP_DPTX_VIF_SECURE_MODE_CFG | | 04F4 0014h |
| 18h | EDP_DPTX_VIF_CONN_STATUS | | 04F4 0018h |
| 1Ch | EDP_PHY_CLK_STATUS | | 04F4 001Ch |

8.4.1 EDP_REVISION Register (Offset = 0h) [reset = 640C4100h]

EDP_REVISION is shown in [Figure 8-49](#) and described in [Table 8-106](#).

Return to [Summary Table](#).

The EDP_REVISION Register contains the major and minor revisions for the VPAC dptx HWA module.

Table 8-105. EDP_REVISION Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0000h |

Figure 8-49. EDP_REVISION Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|--------|-------|----|----|--------|----|-------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | FUNC | | | | | | | | | | | |
| R-1h | | R-2h | | R-40Ch | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTL | | | | | MAJOR | | | CUSTOM | | MINOR | | | | | |
| R-8h | | | | | R-1h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-106. EDP_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 31-30 | SCHEME | R | 1h | Used to distinguish between old scheme and new scheme. Spare bit to encode future schemes |
| 29-28 | BU | R | 2h | BU indicator DSPS ==> 0x0 WTBU ==> 0x1 Processors ==> 0x2 |
| 27-16 | FUNC | R | 40Ch | Function indicates a software compatible module family. If there is no level of software compatibility a new FUNC number, and hence PID, should be assigned. |
| 15-11 | RTL | R | 8h | RTL Version. R as described in PDR with additional clarifications and definitions below. Must be easily ECO-able or controlled during fabrication. Ideally through a top level metal mask or e-fuse. This number is maintained/owned by IP design owner. RTL follows a numbering such as X.Y.R.Z which are explained in this table. R changes ONLY when : (1) PDS uploads occur which may have been due to spec changes (2) Bug fixes occur (3) Resets to '0' when X or Y changes. Design team has an internal 'Z' (customer invisible) number which increments on every drop that happens due to DV and RTL updates. Z resets to 0 when R increments. |

Table 8-106. EDP_REVISION Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|--|
| 10-8 | MAJOR | R | 1h | <p>Major EDP_REVISION.</p> <p>X as described in PDR with additional clarifications/definitions below.</p> <p>This number is owned/maintained by IP specification owner.</p> <p>X is part of IP numbering X.Y.R.Z. X changes ONLY when:</p> <p>(1) There is a major feature addition.</p> <p>An example would be adding Master Mode to Utopia Level2.</p> <p>The Func field (or Class/Type in old PID format) will remain the same.</p> <p>X does NOT change due to:</p> <p>(1) Bug fixes</p> <p>(2) Change in feature parameters.\n</p> |
| 7-6 | CUSTOM | R | 0h | <p>Indicates a special version for a particular device.</p> <p>Consequence of use may avoid use of standard Chip Support Library (CSL) / Drivers.</p> <p>0 if non-c ustom.</p> |
| 5-0 | MINOR | R | 0h | <p>Minor EDP_REVISION.</p> <p>Y as described in PDR with additional clarifications/definitions below.</p> <p>This number is owned/maintained by IP specification owner.</p> <p>Y changes ONLY when:</p> <p>(1) Features are scaled (up or down).</p> <p>Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available.</p> <p>(2) When feature creeps from Is-Not list to Is list.</p> <p>But this may not be the case once it sees silicon - in which case X will change.</p> <p>Y does NOT change due to :</p> <p>(1) Bug fixes</p> <p>(2) Typos or clarifications</p> <p>(3) major functional/feature change/addition/deletion.</p> <p>Instead these changes may be reflected via R, S, X as applicable.</p> <p>Spec owner maintains a customer-invisible number 'S' which changes due to:</p> <p>(1) Typos/clarifications</p> <p>(2) Bug documentation.</p> <p>Note that this bug is not due to a spec change but due to implementation.</p> <p>Nevertheless, the spec tracks the IP bugs.</p> <p>An RTL release (say for silicon PG1.1) that occurs due to bug fix should document the corresponding spec number (X.Y.S) in its release notes.</p> |

8.4.2 EDP_DPTX_IPCFG Register (Offset = 4h) [reset = X]

EDP_DPTX_IPCFG is shown in [Figure 8-50](#) and described in [Table 8-108](#).

Return to [Summary Table](#).

The EDP_DPTX_IPCFG Register - Configures DPTX Core security mode and fw memory clock enable.

Table 8-107. EDP_DPTX_IPCFG Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0004h |

Figure 8-50. EDP_DPTX_IPCFG Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | FW_MEM_CLK_EN | APB_SECURE_REG_BLOCK_EN |
| R/W-X | | | | | | R/W-1h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-108. EDP_DPTX_IPCFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | FW_MEM_CLK_EN | R/W | 1h | DPTX firmware memory (I/Dram) clock enable (set to 1 by default after a reset) 0: Disable Clock (can be set to 0 when not in use for power saving) 1: Enable Clock (must for normal operation) |
| 0 | APB_SECURE_REG_BLOCK_EN | R/W | 0h | DPTX - APB secure region access block enable mode 0: Not Enabled (full access to DPTX memory space including uCPU FW memory regions are permitted) 1: Enabled (only Mailbox and non-secure APB region accesses are permitted via APB). On reset, this bit is set 0 to allow FW to be loaded during the initial configuration. To prevent any tempering of the FW and other secure regions, this bit should be set to 1 (if the configuration firewall setting allows access by a non-secure host) to limit the access only to the mailbox and general cfg space by APB accesses |

8.4.3 EDP_ECC_MEM_CFG Register (Offset = 8h) [reset = X]

EDP_ECC_MEM_CFG is shown in [Figure 8-51](#) and described in [Table 8-110](#).

Return to [Summary Table](#).

The EDP_ECC_MEM_CFG Register - Enables clocks to the ECC-aggregator/memories for ECC logic access. The setting of 1 forces the functional clock gating to be bypassed during memory ECC CTRL/Aggregator accesses during ECC diagnostic mode.

Table 8-109. EDP_ECC_MEM_CFG Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0008h |

Figure 8-51. EDP_ECC_MEM_CFG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | CLK_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-110. EDP_ECC_MEM_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | CLK_EN | R/W | 0h | Clk Force Enable for ECC access 0: Disable 1: Enable (all clock gatings for the ECC memories/aggregator are bypassed). PHY/IO clocks may not be running during the ECC access. These clocks will still be off even when this parameter is set to 1 |

8.4.4 EDP_DPTX_DSC_CFG Register (Offset = Ch) [reset = X]

EDP_DPTX_DSC_CFG is shown in [Figure 8-52](#) and described in [Table 8-112](#).

Return to [Summary Table](#).

The EDP_DPTX_DSC_CFG Register - Configures DSC usaged of the DPTX Core. The settings are used by the wrapper to control the source clock gating for DSC sub-module and also to force enable vif memory clocks as necessary.

Table 8-111. EDP_DPTX_DSC_CFG Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 000Ch |

Figure 8-52. EDP_DPTX_DSC_CFG Register

| | | | | | | | |
|----------|-------------|-------------|-------------|----------|----------------|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | DSC_1_10BPC | DSC_0_10BPC | BOTH_CLK_EN | RESERVED | SPLIT_PANEL_EN | MODE_SEL | |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-X | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-112. EDP_DPTX_DSC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-7 | RESERVED | R/W | X | |
| 6 | DSC_1_10BPC | R/W | 0h | DPTX - DSC encoder 1 - 10-bit input enable 0: 8-bit (default) 1: 10-bit This setting must match the DSC_ENC1 input_bpc[0] configuration |
| 5 | DSC_0_10BPC | R/W | 0h | DPTX - DSC encoder 0 - 10-bit input enable 0: 8-bit (default)\n 1: 10-bit This setting must match the DSC_ENC0 input_bpc[0] configuration |
| 4 | BOTH_CLK_EN | R/W | 0h | DPTX - DSC force both clock on whenever DSC is active 0: Disabled (Normal setting - DSC clock enable is controlled based on mode_sel) 1: Enabled (Reserved) |
| 3 | RESERVED | R/W | X | |
| 2 | SPLIT_PANEL_EN | R/W | 0h | DPTX - DSC encoder mode select 0: Dual Panel (two independent streams) 1: Split Panel (L/R channels of a single source In Split Panel mode, the selected vif_0 and vif_1 stream must be "video timing" synchronized. Both split/dual panel modes require clocks to be in sync/phase.) |

Table 8-112. EDP_DPTX_DSC_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 1-0 | MODE_SEL | R/W | 0h | DPTX - DSC encoder mode select 2'b00: Both encoders Disabled (not used) 2'b01: Single Encoder (only enc0 is used) 2'b1x: Both Encoders Enabled When both Encoders are enabled, it can either be in split panel or dual panel mode. |

8.4.5 EDP_DPTX_SRC_CFG Register (Offset = 10h) [reset = X]

EDP_DPTX_SRC_CFG is shown in [Figure 8-53](#) and described in [Table 8-114](#).

Return to [Summary Table](#).

The EDP_DPTX_SRC_CFG Register - Configures VIF and AIF port channel enables (for memory clock gating) and VIF source mux selection (for mapping DPI to VIF ports). \n\nThe VIF_#_en also enables the clock for the # channel PIF memory. If a PIF channel is enabled, the vif_#_en must be set regardless of whether the associated video channel has the video enabled or not.\n\nNote that these settings are only used in the K3_DSS_eDP wrapper level (for controlling the memory clocks). The DPTX core requires separate configuration for enabling the video/audio streams for transmission. The enable settings between the core and wrapper should match for proper operation.

Table 8-113. EDP_DPTX_SRC_CFG Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0010h |

Figure 8-53. EDP_DPTX_SRC_CFG Register

| | | | | | | | |
|-------------|-----------|-----------|-----------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VIF_FMT_SEL | | | | RESERVED | | | |
| R/W-0h | | | | R/W-X | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | AIF_EN |
| R/W-X | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | VIF_3_IN30B | VIF_2_IN30B | VIF_1_IN30B | VIF_0_IN30B |
| R/W-X | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VIF_3_SEL | VIF_2_SEL | VIF_1_SEL | VIF_0_SEL | VIF_3_EN | VIF_2_EN | VIF_1_EN | VIF_0_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-114. EDP_DPTX_SRC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-28 | VIF_FMT_SEL | R/W | 0h | Reserved - must be set to 0 |
| 27-17 | RESERVED | R/W | X | |
| 16 | AIF_EN | R/W | 0h | DPTX Audio I2S channel memory clk enable 0 : Disable 1: Enable |
| 15-12 | RESERVED | R/W | X | |
| 11 | VIF_3_IN30B | R/W | 0h | DPTX vif_3 source data width is 30 bits 0: 36 bits (default) 1: 30 bits |
| 10 | VIF_2_IN30B | R/W | 0h | DPTX vif_2 source data width is 30 bits 0: 36 bits (default) 1: 30 bits |
| 9 | VIF_1_IN30B | R/W | 0h | DPTX vif_1 source data width is 30 bits 0: 36 bits (default) 1: 30 bits |

Table 8-114. EDP_DPTX_SRC_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 8 | VIF_0_IN30B | R/W | 0h | DPTX vif_0 source data width is 30 bits 0: 36 bits (default) 1: 30 bits |
| 7 | VIF_3_SEL | R/W | 0h | DPTX vif_3 source select - between dpi_3 or dpi_5 0: dpi_3 1: dpi_5 |
| 6 | VIF_2_SEL | R/W | 0h | DPTX vif_2 source select - between dpi_2 or dpi_4 0: dpi_2 1: dpi_4 |
| 5 | VIF_1_SEL | R/W | 0h | DPTX vif_1 source select - between dpi_1 or dpi_3 0: dpi_1 \n 1: dpi_3 |
| 4 | VIF_0_SEL | R/W | 0h | DPTX vif_0 source select - between dpi_0 or dpi_2\n 0: dpi_0 1: dpi_2 |
| 3 | VIF_3_EN | R/W | 0h | DPTX vif_3 channel memory clk enable 0: Disable 1: Enable |
| 2 | VIF_2_EN | R/W | 0h | DPTX vif_2 channel memory clk enable 0: Disable 1: Enable |
| 1 | VIF_1_EN | R/W | 0h | DPTX vif_1 channel memory clk enable 0: Disable 1: Enable |
| 0 | VIF_0_EN | R/W | 0h | DPTX vif_0 channel memory clk enable 0: Disable 1: Enable |

8.4.6 EDP_DPTX_VIF_SECURE_MODE_CFG Register (Offset = 14h) [reset = X]

EDP_DPTX_VIF_SECURE_MODE_CFG is shown in [Figure 8-54](#) and described in [Table 8-116](#).

Return to [Summary Table](#).

The EDP_DPTX_VIF_SECURE_MODE_CFG Register - Configures the security level of the VIF channel (for protecting secure content from going to a non-protected display interface). \nWhen a VIF channel is configured as "non-secure", the K3_DSS_eDP wrapper prevents secure DPI source data to be mapped to the VIF input. When this condition is detected, the wrapper forces the VIF source input to be 0x0. Therefore, if the DPI source from DSS is "secure", then the mapped VIF channel must also be configured as "secure".

**Table 8-115. EDP_DPTX_VIF_SECURE_MODE_CFG
Instances**

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0014h |

Figure 8-54. EDP_DPTX_VIF_SECURE_MODE_CFG Register

| | | | | | | | |
|----------|----|----|----|--------|--------|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | VIF_3 | VIF_2 | VIF_1 | VIF_0 |
| R/W-X | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-116. EDP_DPTX_VIF_SECURE_MODE_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3 | VIF_3 | R/W | 0h | vif_3 channel secure mode: 0: Non-Secure 1: Secure |
| 2 | VIF_2 | R/W | 0h | vif_2 channel secure mode: 0: Non-Secure 1: Secure |
| 1 | VIF_1 | R/W | 0h | vif_1 channel secure mode: 0: Non-Secure 1: Secure |
| 0 | VIF_0 | R/W | 0h | vif_0 channel secure mode: 0: Non-Secure 1: Secure |

8.4.7 EDP_DPTX_VIF_CONN_STATUS Register (Offset = 18h) [reset = X]

EDP_DPTX_VIF_CONN_STATUS is shown in [Figure 8-55](#) and described in [Table 8-118](#).

Return to [Summary Table](#).

The EDP_DPTX_VIF_CONN_STATUS Register - Returns the status of DPI-VIF connection based on the security mode check.
 0 indicates that the connection is allowed
 1 indicates that the connection is not allowed due to security setting mismatch
 When a security mode mismatch is found on a VIF input channel, the source data signals for the channel are forced to 0 - resulting in black color output

Table 8-117. EDP_DPTX_VIF_CONN_STATUS Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 0018h |

Figure 8-55. EDP_DPTX_VIF_CONN_STATUS Register

| | | | | | | | |
|----------|----|----|----|-------|-------|-------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | VIF_3 | VIF_2 | VIF_1 | VIF_0 |
| R-X | | | | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-118. EDP_DPTX_VIF_CONN_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R | X | |
| 3 | VIF_3 | R | 0h | vif_0 security check status: 0: Conn Allowed - no security issue 1: Connection Not Allowed due to security mismatch |
| 2 | VIF_2 | R | 0h | vif_0 security check status: 0: Conn Allowed - no security issue 1: Connection Not Allowed due to security mismatch |
| 1 | VIF_1 | R | 0h | vif_0 security check status: 0: Conn Allowed - no security issue 1: Connection Not Allowed due to security mismatch |
| 0 | VIF_0 | R | 0h | vif_0 security check status: 0: Conn Allowed - no security issue 1: Connection Not Allowed due to security mismatch |

8.4.8 EDP_PHY_CLK_STATUS Register (Offset = 1Ch) [reset = X]

EDP_PHY_CLK_STATUS is shown in [Figure 8-56](#) and described in [Table 8-120](#).

Return to [Summary Table](#).

The EDP_PHY_CLK_STATUS Register - Returns the current status of the phy data clock from DP phy. When the clock is not running, the ECC_aggr_PHY_cfg_regs will return 0x0 on a read

Table 8-119. EDP_PHY_CLK_STATUS Instances

| Instance | Physical Address |
|----------------------|------------------|
| DSS_EDP0_INTG_CFG_VP | 04F4 001Ch |

Figure 8-56. EDP_PHY_CLK_STATUS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VALID |
| R-X | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-120. EDP_PHY_CLK_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-1 | RESERVED | R | X | |
| 0 | VALID | R | 0h | Phy Data Clock Valid Status 0: Clock is not valid/not running 1: Clock is running |

8.5 EDP_CORE_APB Registers

Table 8-122 lists the memory-mapped registers for the EDP_CORE_APB. All register offset addresses not listed in Table 8-122 should be considered as reserved locations and the register contents should not be modified.

MMR registers for eDP Core APB domain

Table 8-121. EDP_CORE_APB Instances

| Instance | Base Address |
|-----------------------------------|--------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0000h |

Table 8-122. EDP_CORE_APB Registers

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|--------|---|---------------|--|
| 0h | EDP_CORE_APB_CTRL_P | | 0A00 0000h |
| 4h | EDP_CORE_XT_INT_CTRL_P | | 0A00 0004h |
| 8h | EDP_CORE_MAILBOX_FULL_ADDR_P | | 0A00 0008h |
| Ch | EDP_CORE_MAILBOX_EMPTY_ADDR_P | | 0A00 000Ch |
| 10h | EDP_CORE_MAILBOX0_WR_DATA_P | | 0A00 0010h |
| 14h | EDP_CORE_MAILBOX0_RD_DATA_P | | 0A00 0014h |
| 18h | EDP_CORE_KEEP_ALIVE_P | | 0A00 0018h |
| 1Ch | EDP_CORE_VER_I_P | | 0A00 001Ch |
| 20h | EDP_CORE_VER_H_P | | 0A00 0020h |
| 24h | EDP_CORE_VER_LIB_L_ADDR_P | | 0A00 0024h |
| 28h | EDP_CORE_VER_LIB_H_ADDR_P | | 0A00 0028h |
| 2Ch | EDP_CORE_SW_DEBUG_I_P | | 0A00 002Ch |
| 30h | EDP_CORE_SW_DEBUG_H_P | | 0A00 0030h |
| 34h | EDP_CORE_MAILBOX_INT_MASK_P | | 0A00 0034h |
| 38h | EDP_CORE_MAILBOX_INT_STATUS_P | | 0A00 0038h |
| 3Ch | EDP_CORE_SW_CLK_I_P | | 0A00 003Ch |
| 40h | EDP_CORE_SW_CLK_H_P | | 0A00 0040h |
| 44h | EDP_CORE_SW_EVENTS0_P | | 0A00 0044h |
| 48h | EDP_CORE_SW_EVENTS1_P | | 0A00 0048h |
| 4Ch | EDP_CORE_SW_EVENTS2_P | | 0A00 004Ch |
| 50h | EDP_CORE_SW_EVENTS3_P | | 0A00 0050h |
| 60h | EDP_CORE_XT_OCD_CTRL_P | | 0A00 0060h |
| 64h | EDP_CORE_XT_OCD_CTRL_RO_P | | 0A00 0064h |
| 6Ch | EDP_CORE_APB_INT_MASK_P | | 0A00 006Ch |
| 70h | EDP_CORE_APB_INT_STATUS_P | | 0A00 0070h |
| A0h | EDP_CORE_CDNS_DID_P | | 0A00 00A0h |
| A4h | EDP_CORE_CDNS_RID0_P | | 0A00 00A4h |
| A8h | EDP_CORE_CDNS_RID1_P | | 0A00 00A8h |
| ACh | EDP_CORE_CDNS_CFGS0_P | | 0A00 00ACh |
| B0h | EDP_CORE_CDNS_CFGS1_P | | 0A00 00B0h |
| 800h | EDP_CORE_SHIFT_PATTERN_IN_3_0_P | | 0A00 0800h |
| 804h | EDP_CORE_SHIFT_PATTERN_IN_4_7_P | | 0A00 0804h |
| 808h | EDP_CORE_SHIFT_PATTERN_IN9_8_P | | 0A00 0808h |
| 80Ch | EDP_CORE_PRBS_CNTRL_P | | 0A00 080Ch |
| 810h | EDP_CORE_PRBS_ERR_INSERTION_P | | 0A00 0810h |
| 814h | EDP_CORE_LANES_CONFIG_P | | 0A00 0814h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|----------------|---|---------------|---|
| 818h | EDP_CORE_PHY_DATA_SEL_P | | 0A00 0818h |
| 81Ch | EDP_CORE_LANES_DEL_VAL_P | | 0A00 081Ch |
| 904h | EDP_CORE_SOURCE_DPTX_CAR_P | | 0A00 0904h |
| 908h | EDP_CORE_SOURCE_PHY_CAR_P | | 0A00 0908h |
| 918h | EDP_CORE_SOURCE_PKT_CAR_P | | 0A00 0918h |
| 91Ch | EDP_CORE_SOURCE_AIF_CAR_P | | 0A00 091Ch |
| 920h | EDP_CORE_SOURCE_CIPHER_CAR_P | | 0A00 0920h |
| 924h | EDP_CORE_SOURCE_CRYPTO_CAR_P | | 0A00 0924h |
| 928h | EDP_CORE_SOURCE_SPDIF_CAR_P | | 0A00 0928h |
| A00h | EDP_CORE_CM_CTRL_P | | 0A00 0A00h |
| A04h | EDP_CORE_CM_I2S_CTRL_P | | 0A00 0A04h |
| A08h | EDP_CORE_CM_SPDIF_CTRL_P | | 0A00 0A08h |
| A0Ch | EDP_CORE_CM_VID_CTRL_P | | 0A00 0A0Ch |
| A10h | EDP_CORE_CM_LANE_CTRL_P | | 0A00 0A10h |
| A14h | EDP_CORE_I2S_NM_STABLE_P | | 0A00 0A14h |
| A18h | EDP_CORE_I2S_NCTS_STABLE_P | | 0A00 0A18h |
| A1Ch | EDP_CORE_SPDIF_NM_STABLE_P | | 0A00 0A1Ch |
| A20h | EDP_CORE_SPDIF_NCTS_STABLE_P | | 0A00 0A20h |
| A24h | EDP_CORE_NMVID_MEAS_STABLE_P | | 0A00 0A24h |
| A28h | EDP_CORE_CM_VID_MEAS_P | | 0A00 0A28h |
| A2Ch | EDP_CORE_CM_AUD_MEAS_P | | 0A00 0A2Ch |
| A30h | EDP_CORE_I2S_MEAS_P | | 0A00 0A30h |
| A34h | EDP_CORE_SPDIF_MEAS_P | | 0A00 0A34h |
| A38h | EDP_CORE_NMVID_MEAS_P | | 0A00 0A38h |
| A40h + formula | EDP_CORE_CM_CTRL_P_j | | 0A00 0A40h + formula |
| A4Ch + formula | EDP_CORE_CM_VID_CTRL_P_j | | 0A00 0A4Ch + formula |
| A64h + formula | EDP_CORE_NMVID_MEAS_STABLE_P_J | | 0A00 0A64h + formula |
| A68h + formula | EDP_CORE_CM_VID_MEAS_P_J | | 0A00 0A68h + formula |
| A78h + formula | EDP_CORE_NMVID_MEAS_P_J | | 0A00 0A78h + formula |
| B00h + formula | EDP_CORE_BND_HSYNC2VSYNC_P_j | | 0A00 0B00h + formula |
| B04h + formula | EDP_CORE_HSYNC2VSYNC_F1_L1_P_J | | 0A00 0B04h + formula |
| B08h + formula | EDP_CORE_HSYNC2VSYNC_F2_L1_P_J | | 0A00 0B08h + formula |
| B0Ch + formula | EDP_CORE_HSYNC2VSYNC_STATUS_P_j | | 0A00 0B0Ch + formula |
| B10h + formula | EDP_CORE_HSYNC2VSYNC_POL_CTRL_P_j | | 0A00 0B10h + formula |
| B14h + formula | EDP_CORE_DSC_CTRL_P_j | | 0A00 0B14h + formula |
| 2000h | EDP_CORE_DP_TX_PHY_CONFIG_REG_P | | 0A00 2000h |
| 2004h | EDP_CORE_DP_TX_PHY_SW_RESET_P | | 0A00 2004h |
| 2008h | EDP_CORE_DP_TX_PHY_SCRAMBLER_SEED_P | | 0A00 2008h |
| 200Ch | EDP_CORE_DP_TX_PHY_TRAINING_01_04_P | | 0A00 200Ch |
| 2010h | EDP_CORE_DP_TX_PHY_TRAINING_05_08_P | | 0A00 2010h |
| 2014h | EDP_CORE_DP_TX_PHY_TRAINING_09_10_P | | 0A00 2014h |
| 2018h | EDP_CORE_DP_TX_PHY_SR_INTERVAL_P | | 0A00 2018h |
| 201Ch | EDP_CORE_DP_TX_PHY_FEC_TEST_P | | 0A00 201Ch |
| 2100h | EDP_CORE_HPD_IRQ_DET_MIN_TIMER_P | | 0A00 2100h |
| 2104h | EDP_CORE_HPD_IRQ_DET_MAX_TIMER_P | | 0A00 2104h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|--------|--|---------------|--|
| 2108h | EDP_CORE_HPD_UNPLGED_DET_MIN_TIMER_P | | 0A00 2108h |
| 210Ch | EDP_CORE_HPD_STABLE_TIMER_P | | 0A00 210Ch |
| 2110h | EDP_CORE_HPD_FILTER_TIMER_P | | 0A00 2110h |
| 2114h | EDP_CORE_HPD_DBNC_TIMER_P | | 0A00 2114h |
| 211Ch | EDP_CORE_HPD_EVENT_MASK_P | | 0A00 211Ch |
| 2120h | EDP_CORE_HPD_EVENT_DET_P | | 0A00 2120h |
| 2200h | EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P | | 0A00 2200h |
| 2204h | EDP_CORE_DP_SW_RESET_P | | 0A00 2204h |
| 2208h | EDP_CORE_DP_FRAMER_TU_P | | 0A00 2208h |
| 2218h | EDP_CORE_DP_FRAMER_BS_SR_INTRVL_P | | 0A00 2218h |
| 2258h | EDP_CORE_DP_MTPH_ECF_SLOTS_31_0_P | | 0A00 2258h |
| 225Ch | EDP_CORE_DP_MTPH_ECF_SLOTS_63_32_P | | 0A00 225Ch |
| 2260h | EDP_CORE_DP_MTPH_LVP_SYMBOL_P | | 0A00 2260h |
| 2264h | EDP_CORE_DP_MTPH_CONTROL_P | | 0A00 2264h |
| 226Ch | EDP_CORE_DP_MTPH_STATUS_P | | 0A00 226Ch |
| 2300h | EDP_CORE_DPTX_LANE_EN_P | | 0A00 2300h |
| 2304h | EDP_CORE_DPTX_ENHNCD_P | | 0A00 2304h |
| 2308h | EDP_CORE_DPTX_INT_MASK_P | | 0A00 2308h |
| 230Ch | EDP_CORE_DPTX_INT_STATUS_P | | 0A00 230Ch |
| 2310h | EDP_CORE_DPTX_FEC_CTRL_P | | 0A00 2310h |
| 2314h | EDP_CORE_DPTX_FEC_STATUS_P | | 0A00 2314h |
| 2400h | EDP_CORE_HDCP_DP_STATUS_P | | 0A00 2400h |
| 2404h | EDP_CORE_HDCP_DP_CONFIG_P | | 0A00 2404h |
| 2408h | EDP_CORE_HDCP_DP_SW_RST_P | | 0A00 2408h |
| 240Ch | EDP_CORE_HDCP_DP_FIFO_STATUS_P | | 0A00 240Ch |
| 2800h | EDP_CORE_DP_AUX_HOST_CONTROL_P | | 0A00 2800h |
| 2804h | EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P | | 0A00 2804h |
| 2808h | EDP_CORE_DP_AUX_INTERRUPT_MASK_P | | 0A00 2808h |
| 280Ch | EDP_CORE_DP_AUX_SWAP_INVERSION_CONTROL_P | | 0A00 280Ch |
| 2810h | EDP_CORE_DP_AUX_SEND_NACK_TRANSACTION_P | | 0A00 2810h |
| 2814h | EDP_CORE_DP_AUX_CLEAR_RX_P | | 0A00 2814h |
| 2818h | EDP_CORE_DP_AUX_CLEAR_TX_P | | 0A00 2818h |
| 281Ch | EDP_CORE_DP_AUX_TIMER_STOP_P | | 0A00 281Ch |
| 2820h | EDP_CORE_DP_AUX_TIMER_CLEAR_P | | 0A00 2820h |
| 2824h | EDP_CORE_DP_AUX_RESET_SW_P | | 0A00 2824h |
| 2828h | EDP_CORE_DP_AUX_DIVIDE_2M_P | | 0A00 2828h |
| 282Ch | EDP_CORE_DP_AUX_TX_PRECHARGE_LENGTH_P | | 0A00 282Ch |
| 2830h | EDP_CORE_DP_AUX_FREQUENCY_1M_MAX_P | | 0A00 2830h |
| 2834h | EDP_CORE_DP_AUX_FREQUENCY_1M_MIN_P | | 0A00 2834h |
| 2838h | EDP_CORE_DP_AUX_RX_PRE_MIN_P | | 0A00 2838h |
| 283Ch | EDP_CORE_DP_AUX_RX_PRE_MAX_P | | 0A00 283Ch |
| 2840h | EDP_CORE_DP_AUX_TIMER_PRESET_P | | 0A00 2840h |
| 2844h | EDP_CORE_DP_AUX_NACK_FORMAT_P | | 0A00 2844h |
| 2848h | EDP_CORE_DP_AUX_TX_DATA_P | | 0A00 2848h |
| 284Ch | EDP_CORE_DP_AUX_RX_DATA_P | | 0A00 284Ch |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|--------|--|---------------|---|
| 2850h | EDP_CORE_DP_AUX_TX_STATUS_P | | 0A00 2850h |
| 2854h | EDP_CORE_DP_AUX_RX_STATUS_P | | 0A00 2854h |
| 2858h | EDP_CORE_DP_AUX_RX_CYCLE_COUNTER_P | | 0A00 2858h |
| 285Ch | EDP_CORE_DP_AUX_MAIN_STATES_P | | 0A00 285Ch |
| 2860h | EDP_CORE_DP_AUX_MAIN_TIMER_P | | 0A00 2860h |
| 2864h | EDP_CORE_DP_AUX_AFE_OUT_P | | 0A00 2864h |
| 4000h | EDP_CORE_CRYPT0_HDCP_REVISION_P | | 0A00 4000h |
| 4004h | EDP_CORE_HDCP_CRYPT0_CONFIG_P | | 0A00 4004h |
| 4008h | EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P | | 0A00 4008h |
| 400Ch | EDP_CORE_CRYPT0_INTERRUPT_MASK_P | | 0A00 400Ch |
| 4018h | EDP_CORE_CRYPT022_CONFIG_P | | 0A00 4018h |
| 401Ch | EDP_CORE_CRYPT022_STATUS_P | | 0A00 401Ch |
| 403Ch | EDP_CORE_SHA_256_DATA_IN_P | | 0A00 403Ch |
| 4050h | EDP_CORE_SHA_256_DATA_OUT_0_P | | 0A00 4050h |
| 4054h | EDP_CORE_SHA_256_DATA_OUT_1_P | | 0A00 4054h |
| 4058h | EDP_CORE_SHA_256_DATA_OUT_2_P | | 0A00 4058h |
| 405Ch | EDP_CORE_SHA_256_DATA_OUT_3_P | | 0A00 405Ch |
| 4060h | EDP_CORE_SHA_256_DATA_OUT_4_P | | 0A00 4060h |
| 4064h | EDP_CORE_SHA_256_DATA_OUT_5_P | | 0A00 4064h |
| 4068h | EDP_CORE_SHA_256_DATA_OUT_6_P | | 0A00 4068h |
| 406Ch | EDP_CORE_SHA_256_DATA_OUT_7_P | | 0A00 406Ch |
| 4070h | EDP_CORE_AES_32_KEY_0_P | | 0A00 4070h |
| 4074h | EDP_CORE_AES_32_KEY_1_P | | 0A00 4074h |
| 4078h | EDP_CORE_AES_32_KEY_2_P | | 0A00 4078h |
| 407Ch | EDP_CORE_AES_32_KEY_3_P | | 0A00 407Ch |
| 4080h | EDP_CORE_AES_32_DATA_IN_P | | 0A00 4080h |
| 4084h | EDP_CORE_AES_32_DATA_OUT_0_P | | 0A00 4084h |
| 4088h | EDP_CORE_AES_32_DATA_OUT_1_P | | 0A00 4088h |
| 408Ch | EDP_CORE_AES_32_DATA_OUT_2_P | | 0A00 408Ch |
| 4090h | EDP_CORE_AES_32_DATA_OUT_3_P | | 0A00 4090h |
| 40A0h | EDP_CORE_CRYPT014_CONFIG_P | | 0A00 40A0h |
| 40A4h | EDP_CORE_CRYPT014_STATUS_P | | 0A00 40A4h |
| 40A8h | EDP_CORE_CRYPT014_PRNM_OUT_P | | 0A00 40A8h |
| 40ACh | EDP_CORE_CRYPT014_KM_0_P | | 0A00 40ACh |
| 40B0h | EDP_CORE_CRYPT014_KM_1_P | | 0A00 40B0h |
| 40B4h | EDP_CORE_CRYPT014_AN_0_P | | 0A00 40B4h |
| 40B8h | EDP_CORE_CRYPT014_AN_1_P | | 0A00 40B8h |
| 40BCh | EDP_CORE_CRYPT014_YOUR_KSV_0_P | | 0A00 40BCh |
| 40C0h | EDP_CORE_CRYPT014_YOUR_KSV_1_P | | 0A00 40C0h |
| 40C4h | EDP_CORE_CRYPT014_MI_0_P | | 0A00 40C4h |
| 40C8h | EDP_CORE_CRYPT014_MI_1_P | | 0A00 40C8h |
| 40CCh | EDP_CORE_CRYPT014_TI_0_P | | 0A00 40CCh |
| 40D0h | EDP_CORE_CRYPT014_KI_0_P | | 0A00 40D0h |
| 40D4h | EDP_CORE_CRYPT014_KI_1_P | | 0A00 40D4h |
| 40D8h | EDP_CORE_CRYPT014_BLOCKS_NUM_P | | 0A00 40D8h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|------------------------|--|---------------|---|
| 40DCh | EDP_CORE_CRYPT014_KEY_MEM_DATA_0_P | | 0A00 40DCh |
| 40E0h | EDP_CORE_CRYPT014_KEY_MEM_DATA_1_P | | 0A00 40E0h |
| 40E4h | EDP_CORE_CRYPT014_SHA1_MSG_DATA_P | | 0A00 40E4h |
| 40E8h | EDP_CORE_CRYPT014_SHA1_V_VALUE_0_P | | 0A00 40E8h |
| 40ECh | EDP_CORE_CRYPT014_SHA1_V_VALUE_1_P | | 0A00 40ECh |
| 40F0h | EDP_CORE_CRYPT014_SHA1_V_VALUE_2_P | | 0A00 40F0h |
| 40F4h | EDP_CORE_CRYPT014_SHA1_V_VALUE_3_P | | 0A00 40F4h |
| 40F8h | EDP_CORE_CRYPT014_SHA1_V_VALUE_4_P | | 0A00 40F8h |
| 3000h + formula | EDP_CORE_MSA_HORIZONTAL_0_P_J | | 0A00 3000h + formula |
| 3004h + formula | EDP_CORE_MSA_HORIZONTAL_1_P_J | | 0A00 3004h + formula |
| 3008h + formula | EDP_CORE_MSA_VERTICAL_0_P_J | | 0A00 3008h + formula |
| 300Ch + formula | EDP_CORE_MSA_VERTICAL_1_P_J | | 0A00 300Ch + formula |
| 3010h + formula | EDP_CORE_MSA_MISC_P_J | | 0A00 3010h + formula |
| 3014h + formula | EDP_CORE_STREAM_CONFIG_P_J | | 0A00 3014h + formula |
| 3018h + formula | EDP_CORE_AUDIO_PACK_STATUS_P_J | | 0A00 3018h + formula |
| 301Ch + formula | EDP_CORE_VIF_STATUS_P_J | | 0A00 301Ch + formula |
| 3020h + formula | EDP_CORE_PCK_STUFF_STATUS_0_P_J | | 0A00 3020h + formula |
| 3024h + formula | EDP_CORE_PCK_STUFF_STATUS_1_P_J | | 0A00 3024h + formula |
| 3028h + formula | EDP_CORE_INFO_PACK_STATUS_P_J | | 0A00 3028h + formula |
| 302Ch + formula | EDP_CORE_STREAM_CONFIG_2_P_J | | 0A00 302Ch + formula |
| 3030h + formula | EDP_CORE_DP_HORIZONTAL_P_J | | 0A00 3030h + formula |
| 3034h + formula | EDP_CORE_DP_VERTICAL_0_P_J | | 0A00 3034h + formula |
| 3038h + formula | EDP_CORE_DP_VERTICAL_1_P_J | | 0A00 3038h + formula |
| 303Ch + formula | EDP_CORE_DP_BLOCK_SDP_P_J | | 0A00 303Ch + formula |
| 3044h + formula | EDP_CORE_DP_MST_SLOT_ALLOCATE_P_J | | 0A00 3044h + formula |
| 3048h + formula | EDP_CORE_RATE_GOVERNING_CTRL_P_J | | 0A00 3048h + formula |
| 304Ch + formula | EDP_CORE_DP_FRAMER_PXL_REPR_P_J | | 0A00 304Ch + formula |
| 3050h + formula | EDP_CORE_DP_FRAMER_SP_P_J | | 0A00 3050h + formula |
| 3054h + formula | EDP_CORE_AUDIO_PACK_CONTROL_P_J | | 0A00 3054h + formula |
| 3064h + formula | EDP_CORE_LINE_THRESH_P_J | | 0A00 3064h + formula |
| 3068h + formula | EDP_CORE_DP_VB_ID_P_J | | 0A00 3068h + formula |
| 306Ch + formula | EDP_CORE_DP_FIELDSEQ_3D_P_J | | 0A00 306Ch + formula |
| 3078h + formula | EDP_CORE_DP_FRONT_BACK_PORCH_P_J | | 0A00 3078h + formula |
| 307Ch + formula | EDP_CORE_DP_BYTE_COUNT_P_J | | 0A00 307Ch + formula |
| 00010000h + formula | EDP_CORE_IRAM_REG_P_y | | 0A01 0000h + formula |
| 00020000h + formula | EDP_CORE_DRAM_REG_P_y | | 0A02 0000h + formula |
| 00030A00h | EDP_CORE_AUX_CONFIG_P | | 0A03 0A00h |
| 00030A04h | EDP_CORE_AUX_CTRL_P | | 0A03 0A04h |
| 00030A08h | EDP_CORE_AUX_ATBSEL_P | | 0A03 0A08h |
| 00030A0Ch | EDP_CORE_AUX_TESTMODE_CTL_P | | 0A03 0A0Ch |
| 00030A10h | EDP_CORE_AUX_TESTMODE_ST_P | | 0A03 0A10h |
| 00030A20h | EDP_CORE_PHY_RESET_P | | 0A03 0A20h |
| 00030A24h | EDP_CORE_PMA_PLLCLK_EN_P | | 0A03 0A24h |
| 00030A28h | EDP_CORE_PMA_PLLCLK_EN_ACK_P | | 0A03 0A28h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|-----------|--|---------------|---|
| 00030A2Ch | EDP_CORE_PMA_POWER_STATE_REQ_P | | 0A03 0A2Ch |
| 00030A30h | EDP_CORE_PMA_POWER_STATE_ACK_P | | 0A03 0A30h |
| 00030A34h | EDP_CORE_PMA_CMN_READY_P | | 0A03 0A34h |
| 00030A38h | EDP_CORE_PMA_TX_VMARGIN_P | | 0A03 0A38h |
| 00030A3Ch | EDP_CORE_PMA_TX_DEEMPH_P | | 0A03 0A3Ch |
| 00030A60h | EDP_CORE_ASF_IPS_CTRL | | 0A03 0A60h |
| 00030B00h | EDP_CORE_ASF_INT_STATUS | | 0A03 0B00h |
| 00030B04h | EDP_CORE_ASF_INT_RAW_STATUS | | 0A03 0B04h |
| 00030B08h | EDP_CORE_ASF_INT_MASK | | 0A03 0B08h |
| 00030B0Ch | EDP_CORE_ASF_INT_TEST | | 0A03 0B0Ch |
| 00030B10h | EDP_CORE_ASF_FATAL_NONFATAL_SELECT | | 0A03 0B10h |
| 00030B20h | EDP_CORE_ASF_SRAM_CORR_FAULT_STATUS | | 0A03 0B20h |
| 00030B24h | EDP_CORE_ASF_SRAM_UNCORR_FAULT_STATUS | | 0A03 0B24h |
| 00030B28h | EDP_CORE_ASF_SRAM_FAULT_STATUS | | 0A03 0B28h |
| 00030B30h | EDP_CORE_ASF_TRANS_TO_CTRL | | 0A03 0B30h |
| 00030B34h | EDP_CORE_ASF_TRANS_TO_FAULT_MASK | | 0A03 0B34h |
| 00030B38h | EDP_CORE_ASF_TRANS_TO_FAULT_STATUS | | 0A03 0B38h |
| 00030B40h | EDP_CORE_ASF_PROTOCOL_FAULT_MASK | | 0A03 0B40h |
| 00030B44h | EDP_CORE_ASF_PROTOCOL_FAULT_STATUS | | 0A03 0B44h |
| 00030C00h | EDP_CORE_COM_MAIN_CONF_P | | 0A03 0C00h |
| 00030D20h | EDP_CORE_ENC0_MAIN_CONF_P | | 0A03 0D20h |
| 00030D24h | EDP_CORE_ENC0_PICTURE_SIZE_P | | 0A03 0D24h |
| 00030D28h | EDP_CORE_ENC0_SLICE_SIZE_P | | 0A03 0D28h |
| 00030D2Ch | EDP_CORE_ENC0_MISC_SIZE_P | | 0A03 0D2Ch |
| 00030D30h | EDP_CORE_ENC0_HRD_DELAYS_P | | 0A03 0D30h |
| 00030D34h | EDP_CORE_ENC0_RC_SCALE_P | | 0A03 0D34h |
| 00030D38h | EDP_CORE_ENC0_RC_SCALE_INC_DEC_P | | 0A03 0D38h |
| 00030D3Ch | EDP_CORE_ENC0_RC_OFFSETS_1_P | | 0A03 0D3Ch |
| 00030D40h | EDP_CORE_ENC0_RC_OFFSETS_2_P | | 0A03 0D40h |
| 00030D44h | EDP_CORE_ENC0_RC_OFFSETS_3_P | | 0A03 0D44h |
| 00030D48h | EDP_CORE_ENC0_FLATNESS_DETECTION_P | | 0A03 0D48h |
| 00030D4Ch | EDP_CORE_ENC0_RC_MODEL_SIZE_P | | 0A03 0D4Ch |
| 00030D50h | EDP_CORE_ENC0_RC_CONFIG_P | | 0A03 0D50h |
| 00030D54h | EDP_CORE_ENC0_RC_BUF_THRESH_0_P | | 0A03 0D54h |
| 00030D58h | EDP_CORE_ENC0_RC_BUF_THRESH_1_P | | 0A03 0D58h |
| 00030D5Ch | EDP_CORE_ENC0_RC_BUF_THRESH_2_P | | 0A03 0D5Ch |
| 00030D60h | EDP_CORE_ENC0_RC_BUF_THRESH_3_P | | 0A03 0D60h |
| 00030D64h | EDP_CORE_ENC0_RC_MIN_QP_0_P | | 0A03 0D64h |
| 00030D68h | EDP_CORE_ENC0_RC_MIN_QP_1_P | | 0A03 0D68h |
| 00030D6Ch | EDP_CORE_ENC0_RC_MIN_QP_2_P | | 0A03 0D6Ch |
| 00030D70h | EDP_CORE_ENC0_RC_MAX_QP_0_P | | 0A03 0D70h |
| 00030D74h | EDP_CORE_ENC0_RC_MAX_QP_1_P | | 0A03 0D74h |
| 00030D78h | EDP_CORE_ENC0_RC_MAX_QP_2_P | | 0A03 0D78h |
| 00030D7Ch | EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_0_P | | 0A03 0D7Ch |
| 00030D80h | EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_1_P | | 0A03 0D80h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|-----------|--|---------------|---|
| 00030D84h | EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_2_P | | 0A03 0D84h |
| 00030D88h | EDP_CORE_ENC0_DPI_CTRL_OUT_DELAY_P | | 0A03 0D88h |
| 00030DC0h | EDP_CORE_ENC0_GENERAL_STATUS_P | | 0A03 0DC0h |
| 00030DC4h | EDP_CORE_ENC0_HSLICE_STATUS_P | | 0A03 0DC4h |
| 00030DC8h | EDP_CORE_ENC0_OUT_STATUS_P | | 0A03 0DC8h |
| 00030DCCh | EDP_CORE_ENC0_INT_STAT_P | | 0A03 0DCCh |
| 00030DD0h | EDP_CORE_ENC0_INT_CLR_P | | 0A03 0DD0h |
| 00030DD4h | EDP_CORE_ENC0_INT_MASK_P | | 0A03 0DD4h |
| 00030DD8h | EDP_CORE_ENC0_INT_TEST_P | | 0A03 0DD8h |
| 00030E20h | EDP_CORE_ENC1_MAIN_CONF_P | | 0A03 0E20h |
| 00030E24h | EDP_CORE_ENC1_PICTURE_SIZE_P | | 0A03 0E24h |
| 00030E28h | EDP_CORE_ENC1_SLICE_SIZE_P | | 0A03 0E28h |
| 00030E2Ch | EDP_CORE_ENC1_MISC_SIZE_P | | 0A03 0E2Ch |
| 00030E30h | EDP_CORE_ENC1_HRD_DELAYS_P | | 0A03 0E30h |
| 00030E34h | EDP_CORE_ENC1_RC_SCALE_P | | 0A03 0E34h |
| 00030E38h | EDP_CORE_ENC1_RC_SCALE_INC_DEC_P | | 0A03 0E38h |
| 00030E3Ch | EDP_CORE_ENC1_RC_OFFSETS_1_P | | 0A03 0E3Ch |
| 00030E40h | EDP_CORE_ENC1_RC_OFFSETS_2_P | | 0A03 0E40h |
| 00030E44h | EDP_CORE_ENC1_RC_OFFSETS_3_P | | 0A03 0E44h |
| 00030E48h | EDP_CORE_ENC1_FLATNESS_DETECTION_P | | 0A03 0E48h |
| 00030E4Ch | EDP_CORE_ENC1_RC_MODEL_SIZE_P | | 0A03 0E4Ch |
| 00030E50h | EDP_CORE_ENC1_RC_CONFIG_P | | 0A03 0E50h |
| 00030E54h | EDP_CORE_ENC1_RC_BUF_THRESH_0_P | | 0A03 0E54h |
| 00030E58h | EDP_CORE_ENC1_RC_BUF_THRESH_1_P | | 0A03 0E58h |
| 00030E5Ch | EDP_CORE_ENC1_RC_BUF_THRESH_2_P | | 0A03 0E5Ch |
| 00030E60h | EDP_CORE_ENC1_RC_BUF_THRESH_3_P | | 0A03 0E60h |
| 00030E64h | EDP_CORE_ENC1_RC_MIN_QP_0_P | | 0A03 0E64h |
| 00030E68h | EDP_CORE_ENC1_RC_MIN_QP_1_P | | 0A03 0E68h |
| 00030E6Ch | EDP_CORE_ENC1_RC_MIN_QP_2_P | | 0A03 0E6Ch |
| 00030E70h | EDP_CORE_ENC1_RC_MAX_QP_0_P | | 0A03 0E70h |
| 00030E74h | EDP_CORE_ENC1_RC_MAX_QP_1_P | | 0A03 0E74h |
| 00030E78h | EDP_CORE_ENC1_RC_MAX_QP_2_P | | 0A03 0E78h |
| 00030E7Ch | EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_0_P | | 0A03 0E7Ch |
| 00030E80h | EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_1_P | | 0A03 0E80h |
| 00030E84h | EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_2_P | | 0A03 0E84h |
| 00030E88h | EDP_CORE_ENC1_DPI_CTRL_OUT_DELAY_P | | 0A03 0E88h |
| 00030EC0h | EDP_CORE_ENC1_GENERAL_STATUS_P | | 0A03 0EC0h |
| 00030EC4h | EDP_CORE_ENC1_HSLICE_STATUS_P | | 0A03 0EC4h |
| 00030EC8h | EDP_CORE_ENC1_OUT_STATUS_P | | 0A03 0EC8h |
| 00030ECCh | EDP_CORE_ENC1_INT_STAT_P | | 0A03 0ECCh |
| 00030ED0h | EDP_CORE_ENC1_INT_CLR_P | | 0A03 0ED0h |
| 00030ED4h | EDP_CORE_ENC1_INT_MASK_P | | 0A03 0ED4h |
| 00030ED8h | EDP_CORE_ENC1_INT_TEST_P | | 0A03 0ED8h |
| 00030F00h | EDP_CORE_ENC_ASF_INT_STAT_P | | 0A03 0F00h |
| 00030F04h | EDP_CORE_ENC_ASF_INT_MASK_P | | 0A03 0F04h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|-----------|---|---------------|---|
| 00030F08h | EDP_CORE_ENC_ASF_INT_CLR_P | | 0A03 0F08h |
| 00030F0Ch | EDP_CORE_ENC_ASF_INT_TEST_P | | 0A03 0F0Ch |
| 00030F20h | EDP_CORE_ENC0_ASF_SRAM_CORR_P | | 0A03 0F20h |
| 00030F24h | EDP_CORE_ENC0_ASF_SRAM_UNCORR_P | | 0A03 0F24h |
| 00030F28h | EDP_CORE_ENC1_ASF_SRAM_CORR_P | | 0A03 0F28h |
| 00030F2Ch | EDP_CORE_ENC1_ASF_SRAM_UNCORR_P | | 0A03 0F2Ch |
| 00030F30h | EDP_CORE_ENC0_ASF_CSR_CHK_TEST_P | | 0A03 0F30h |
| 00030F34h | EDP_CORE_ENC1_ASF_CSR_CHK_TEST_P | | 0A03 0F34h |
| 00030F38h | EDP_CORE_ENC0_ASF_SELF_CHK_TEST_P | | 0A03 0F38h |
| 00030F3Ch | EDP_CORE_ENC1_ASF_SELF_CHK_TEST_P | | 0A03 0F3Ch |
| 00030F40h | EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P | | 0A03 0F40h |
| 00030F44h | EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P | | 0A03 0F44h |
| 00030000h | EDP_CORE_AUDIO_SRC_CNTL_P | | 0A03 0000h |
| 00030004h | EDP_CORE_AUDIO_SRC_CNFG_P | | 0A03 0004h |
| 00030008h | EDP_CORE_COM_CH_STTS_BITS_P | | 0A03 0008h |
| 0003000Ch | EDP_CORE_STTS_BIT_CH01_P | | 0A03 000Ch |
| 00030010h | EDP_CORE_STTS_BIT_CH23_P | | 0A03 0010h |
| 00030014h | EDP_CORE_STTS_BIT_CH45_P | | 0A03 0014h |
| 00030018h | EDP_CORE_STTS_BIT_CH67_P | | 0A03 0018h |
| 0003001Ch | EDP_CORE_STTS_BIT_CH89_P | | 0A03 001Ch |
| 00030020h | EDP_CORE_STTS_BIT_CH1011_P | | 0A03 0020h |
| 00030024h | EDP_CORE_STTS_BIT_CH1213_P | | 0A03 0024h |
| 00030028h | EDP_CORE_STTS_BIT_CH1415_P | | 0A03 0028h |
| 0003002Ch | EDP_CORE_STTS_BIT_CH1617_P | | 0A03 002Ch |
| 00030030h | EDP_CORE_STTS_BIT_CH1819_P | | 0A03 0030h |
| 00030034h | EDP_CORE_STTS_BIT_CH2021_P | | 0A03 0034h |
| 00030038h | EDP_CORE_STTS_BIT_CH2223_P | | 0A03 0038h |
| 0003003Ch | EDP_CORE_STTS_BIT_CH2425_P | | 0A03 003Ch |
| 00030040h | EDP_CORE_STTS_BIT_CH2627_P | | 0A03 0040h |
| 00030044h | EDP_CORE_STTS_BIT_CH2829_P | | 0A03 0044h |
| 00030048h | EDP_CORE_STTS_BIT_CH3031_P | | 0A03 0048h |
| 0003004Ch | EDP_CORE_SPDIF_CTRL_ADDR_P | | 0A03 004Ch |
| 00030050h | EDP_CORE_SPDIF_CH1_CS_3100_ADDR_P | | 0A03 0050h |
| 00030054h | EDP_CORE_SPDIF_CH1_CS_6332_ADDR_P | | 0A03 0054h |
| 00030058h | EDP_CORE_SPDIF_CH1_CS_9564_ADDR_P | | 0A03 0058h |
| 0003005Ch | EDP_CORE_SPDIF_CH1_CS_12796_ADDR_P | | 0A03 005Ch |
| 00030060h | EDP_CORE_SPDIF_CH1_CS_159128_ADDR_P | | 0A03 0060h |
| 00030064h | EDP_CORE_SPDIF_CH1_CS_191160_ADDR_P | | 0A03 0064h |
| 00030068h | EDP_CORE_SPDIF_CH2_CS_3100_ADDR_P | | 0A03 0068h |
| 0003006Ch | EDP_CORE_SPDIF_CH2_CS_6332_ADDR_P | | 0A03 006Ch |
| 00030070h | EDP_CORE_SPDIF_CH2_CS_9564_ADDR_P | | 0A03 0070h |
| 00030074h | EDP_CORE_SPDIF_CH2_CS_12796_ADDR_P | | 0A03 0074h |
| 00030078h | EDP_CORE_SPDIF_CH2_CS_159128_ADDR_P | | 0A03 0078h |
| 0003007Ch | EDP_CORE_SPDIF_CH2_CS_191160_ADDR_P | | 0A03 007Ch |
| 00030080h | EDP_CORE_SMPL2PKT_CNTL_P | | 0A03 0080h |

Table 8-122. EDP_CORE_APB Registers (continued)

| Offset | Acronym | Register Name | DSS_EDP0_V2A_CORE_VP_REGS_ APB Physical Address |
|------------------------|--|---------------|---|
| 00030084h | EDP_CORE_SMPL2PKT_CNFG_P | | 0A03 0084h |
| 00030088h | EDP_CORE_FIFO_CNTL_P | | 0A03 0088h |
| 0003008Ch | EDP_CORE_FIFO_STTS_P | | 0A03 008Ch |
| 00030090h | EDP_CORE_SUB_PCKT_THRSH_P | | 0A03 0090h |
| 00030800h + formula | EDP_CORE_SOURCE_PIF_WR_ADDR_P_j | | 0A03 0800h + formula |
| 00030804h + formula | EDP_CORE_SOURCE_PIF_WR_REQ_P_j | | 0A03 0804h + formula |
| 00030808h + formula | EDP_CORE_SOURCE_PIF_RD_ADDR_P_j | | 0A03 0808h + formula |
| 0003080Ch + formula | EDP_CORE_SOURCE_PIF_RD_REQ_P_j | | 0A03 080Ch + formula |
| 00030810h + formula | EDP_CORE_SOURCE_PIF_DATA_WR_P_j | | 0A03 0810h + formula |
| 00030814h + formula | EDP_CORE_SOURCE_PIF_DATA_RD_P_j | | 0A03 0814h + formula |
| 00030818h + formula | EDP_CORE_SOURCE_PIF_FIFO1_FLUSH_P_j | | 0A03 0818h + formula |
| 0003081Ch + formula | EDP_CORE_SOURCE_PIF_FIFO2_FLUSH_P_j | | 0A03 081Ch + formula |
| 00030820h + formula | EDP_CORE_SOURCE_PIF_STATUS_P_j | | 0A03 0820h + formula |
| 00030824h + formula | EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P_j | | 0A03 0824h + formula |
| 00030828h + formula | EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_j | | 0A03 0828h + formula |
| 0003082Ch + formula | EDP_CORE_SOURCE_PIF_PKT_ALLOC_REG_P_j | | 0A03 082Ch + formula |
| 00030830h + formula | EDP_CORE_SOURCE_PIF_PKT_ALLOC_WR_EN_P_j | | 0A03 0830h + formula |
| 00030834h + formula | EDP_CORE_SOURCE_PIF_SW_RESET_P_j | | 0A03 0834h + formula |
| 00030838h + formula | EDP_CORE_SOURCE_PIF_PPS_HEADER_P_j | | 0A03 0838h + formula |
| 0003083Ch + formula | EDP_CORE_SOURCE_PIF_PPS_P_j | | 0A03 083Ch + formula |

8.5.1 EDP_CORE_APB_CTRL_P Register (Offset = 0h) [reset = Fh]

EDP_CORE_APB_CTRL_P is shown in [Figure 8-57](#) and described in [Table 8-124](#).

Return to [Summary Table](#).

APB main control register

Table 8-123. EDP_CORE_APB_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0000h |

Figure 8-57. EDP_CORE_APB_CTRL_P Register

| | | | | | | | |
|----------|----|----|----|---------------------|-------------------|-------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | APB_XT_RUNS TALL | APB_IRAM_PA TH | APB_DRAM_P ATH | APB_XT_RESE T |
| R-0h | | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-124. EDP_CORE_APB_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 3 | APB_XT_RUNSTALL | R/W | 1h | When 1 stalls the CPU from executing further instructions. This bit must be set HIGH during firmware load. |
| 2 | APB_IRAM_PATH | R/W | 1h | Unused. Kept RW for software backward compatibility. |
| 1 | APB_DRAM_PATH | R/W | 1h | Unused. Kept RW for software backward compatibility. |
| 0 | APB_XT_RESET | R/W | 1h | Internal uCPU reset. Active High. Must be cleared to enable firmware load and normal operation of the uCPU. |

8.5.2 EDP_CORE_XT_INT_CTRL_P Register (Offset = 4h) [reset = 0h]

EDP_CORE_XT_INT_CTRL_P is shown in [Figure 8-58](#) and described in [Table 8-126](#).

Return to [Summary Table](#).

Internal CPU Interrupt Polarity Control Register.

Table 8-125. EDP_CORE_XT_INT_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0004h |

Figure 8-58. EDP_CORE_XT_INT_CTRL_P Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | XT_INT_POLARITY | |
| R-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-126. EDP_CORE_XT_INT_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1-0 | XT_INT_POLARITY | R/W | 0h | Each bit inverts appropriate interrupt signal provided do internal CPU interrupt input. |

8.5.3 EDP_CORE_MAILBOX_FULL_ADDR_P Register (Offset = 8h) [reset = 0h]

EDP_CORE_MAILBOX_FULL_ADDR_P is shown in [Figure 8-59](#) and described in [Table 8-128](#).

Return to [Summary Table](#).

Mailbox full indication status register. This register provides a status of the mailbox that is used to send messages from the Host processor to internal uCPU.

Mailbox full flag can be a source of mailbox interrupt.

**Table 8-127. EDP_CORE_MAILBOX_FULL_ADDR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0008h |

Figure 8-59. EDP_CORE_MAILBOX_FULL_ADDR_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | MAILBOX_FULL |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-128. EDP_CORE_MAILBOX_FULL_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 0 | MAILBOX_FULL | R | 0h | Mailbox full indication. 0x 1-mailbox full. No more messages can be sent to mailbox 0x 0-mailbox not-full. At least 1 write can be performed to mailbox |

8.5.4 EDP_CORE_MAILBOX_EMPTY_ADDR_P Register (Offset = Ch) [reset = 1h]

EDP_CORE_MAILBOX_EMPTY_ADDR_P is shown in [Figure 8-60](#) and described in [Table 8-130](#).

Return to [Summary Table](#).

Mailbox empty indication status register. This register provides a status of the mailbox that is used to send responses from the internal uCPU to host processor as a result of previously sent message. Mailbox empty flag can be a source of not-empty mailbox interrupt.

Table 8-129.
EDP_CORE_MAILBOX_EMPTY_ADDR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 000Ch |

Figure 8-60. EDP_CORE_MAILBOX_EMPTY_ADDR_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | MAILBOX_EMPTY |
| R-0h | | | | | | | R-1h |

LEGEND: R = Read Only; -n = value after reset

Table 8-130. EDP_CORE_MAILBOX_EMPTY_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 0 | MAILBOX_EMPTY | R | 1h | Mailbox empty indication. 0x 1-mailbox empty. No response available 0x 0-mailbox not-empty. There is at least 1 byte of a response in mailbox available to read by Host processor |

8.5.5 EDP_CORE_MAILBOX0_WR_DATA_P Register (Offset = 10h) [reset = 0h]

EDP_CORE_MAILBOX0_WR_DATA_P is shown in [Figure 8-61](#) and described in [Table 8-132](#).

Return to [Summary Table](#).

Mailbox write data register.

Table 8-131. EDP_CORE_MAILBOX0_WR_DATA_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0010h |

Figure 8-61. EDP_CORE_MAILBOX0_WR_DATA_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | MAILBOX0_WR_DATA | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-132. EDP_CORE_MAILBOX0_WR_DATA_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | MAILBOX0_WR_DATA | R/W | 0h | Mailbox write data. |

8.5.6 EDP_CORE_MAILBOX0_RD_DATA_P Register (Offset = 14h) [reset = 0h]

EDP_CORE_MAILBOX0_RD_DATA_P is shown in [Figure 8-62](#) and described in [Table 8-134](#).

Return to [Summary Table](#).

Mailbox Read data register.

Table 8-133. EDP_CORE_MAILBOX0_RD_DATA_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0014h |

Figure 8-62. EDP_CORE_MAILBOX0_RD_DATA_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | MAILBOX0_RD_DATA | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-134. EDP_CORE_MAILBOX0_RD_DATA_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | MAILBOX0_RD_DATA | R | 0h | Mailbox Read data. |

8.5.7 EDP_CORE_KEEP_ALIVE_P Register (Offset = 18h) [reset = 0h]

EDP_CORE_KEEP_ALIVE_P is shown in [Figure 8-63](#) and described in [Table 8-136](#).

Return to [Summary Table](#).

Software keep alive counter.

Table 8-135. EDP_CORE_KEEP_ALIVE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0018h |

Figure 8-63. EDP_CORE_KEEP_ALIVE_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | KEEP_ALIVE_CNT | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-136. EDP_CORE_KEEP_ALIVE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | KEEP_ALIVE_CNT | R | 0h | Software keep alive counter. Counter is initialized to 0x0 after reset and incremented by 0x1 with every FW kernel loop. It can be used to determine if internal CPU started running correctly. |

8.5.8 EDP_CORE_VER_I_P Register (Offset = 1Ch) [reset = 0h]

EDP_CORE_VER_I_P is shown in [Figure 8-64](#) and described in [Table 8-138](#).

[Return to Summary Table.](#)

Software Version Register.

Table 8-137. EDP_CORE_VER_I_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 001Ch |

Figure 8-64. EDP_CORE_VER_I_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | VER_LSB | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-138. EDP_CORE_VER_I_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | VER_LSB | R | 0h | Software Version lower byte. Loaded by Firmware at the beginning of firmware operation. |

8.5.9 EDP_CORE_VER_H_P Register (Offset = 20h) [reset = 0h]

EDP_CORE_VER_H_P is shown in [Figure 8-65](#) and described in [Table 8-140](#).

Return to [Summary Table](#).

Software Version Register.

Table 8-139. EDP_CORE_VER_H_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0020h |

Figure 8-65. EDP_CORE_VER_H_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | VER_MSB | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-140. EDP_CORE_VER_H_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | VER_MSB | R | 0h | Software Version higher byte. Loaded by Firmware at the beginning of firmware operation. |

8.5.10 EDP_CORE_VER_LIB_L_ADDR_P Register (Offset = 24h) [reset = 0h]

EDP_CORE_VER_LIB_L_ADDR_P is shown in [Figure 8-66](#) and described in [Table 8-142](#).

Return to [Summary Table](#).

Software Library Version Register.

Table 8-141. EDP_CORE_VER_LIB_L_ADDR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0024h |

Figure 8-66. EDP_CORE_VER_LIB_L_ADDR_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_LIB_VER_L | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-142. EDP_CORE_VER_LIB_L_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_LIB_VER_L | R | 0h | Software Library Version lower byte. Loaded by Firmware at the beginning of firmware operation. |

8.5.11 EDP_CORE_VER_LIB_H_ADDR_P Register (Offset = 28h) [reset = 0h]

EDP_CORE_VER_LIB_H_ADDR_P is shown in [Figure 8-67](#) and described in [Table 8-144](#).

Return to [Summary Table](#).

Software Library Version Register.

**Table 8-143. EDP_CORE_VER_LIB_H_ADDR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0028h |

Figure 8-67. EDP_CORE_VER_LIB_H_ADDR_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_LIB_VER_H | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-144. EDP_CORE_VER_LIB_H_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_LIB_VER_H | R | 0h | Software Library Version higher byte. Loaded by Firmware at the beginning of firmware operation. |

8.5.12 EDP_CORE_SW_DEBUG_I_P Register (Offset = 2Ch) [reset = 0h]

EDP_CORE_SW_DEBUG_I_P is shown in [Figure 8-68](#) and described in [Table 8-146](#).

[Return to Summary Table.](#)

Software/Firmware Debug Register.

Table 8-145. EDP_CORE_SW_DEBUG_I_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 002Ch |

Figure 8-68. EDP_CORE_SW_DEBUG_I_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_DEBUG_7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-146. EDP_CORE_SW_DEBUG_I_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_DEBUG_7_0 | R | 0h | Register used for debug purposes [lower byte]. Can be written internally by firmware to allow Core Driver to read the internal status. Not used during normal operation since it requires a special version of firmware with a debug capabilities. |

8.5.13 EDP_CORE_SW_DEBUG_H_P Register (Offset = 30h) [reset = 0h]

EDP_CORE_SW_DEBUG_H_P is shown in [Figure 8-69](#) and described in [Table 8-148](#).

Return to [Summary Table](#).

Software/Firmware Debug Register.

**Table 8-147. EDP_CORE_SW_DEBUG_H_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0030h |

Figure 8-69. EDP_CORE_SW_DEBUG_H_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_DEBUG_15_8 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-148. EDP_CORE_SW_DEBUG_H_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_DEBUG_15_8 | R | 0h | Register used for debug purposes [higher byte]. Can be written internally by firmware to allow Core Driver to read the internal status. Not used during normal operation since it requires a special version of firmware with a debug capabilities. |

8.5.14 EDP_CORE_MAILBOX_INT_MASK_P Register (Offset = 34h) [reset = 0h]

EDP_CORE_MAILBOX_INT_MASK_P is shown in [Figure 8-70](#) and described in [Table 8-150](#).

Return to [Summary Table](#).

Mailbox Interrupt mask register.

Table 8-149. EDP_CORE_MAILBOX_INT_MASK_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0034h |

Figure 8-70. EDP_CORE_MAILBOX_INT_MASK_P Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | MAILBOX_FULL_INT_MASK | MAILBOX_EMPTY_INT_MASK |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-150. EDP_CORE_MAILBOX_INT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | MAILBOX_FULL_INT_MASK | R/W | 0h | Mailbox Full Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 0 | MAILBOX_EMPTY_INT_MASK | R/W | 0h | Mailbox Not-empty Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.5.15 EDP_CORE_MAILBOX_INT_STATUS_P Register (Offset = 38h) [reset = 0h]

EDP_CORE_MAILBOX_INT_STATUS_P is shown in [Figure 8-71](#) and described in [Table 8-152](#).

Return to [Summary Table](#).

Mailbox Interrupt Status register.

**Table 8-151. EDP_CORE_MAILBOX_INT_STATUS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0038h |

Figure 8-71. EDP_CORE_MAILBOX_INT_STATUS_P Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | MAILBOX_FULL_INT_STATUS | MAILBOX_EMPTY_INT_STATUS |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-152. EDP_CORE_MAILBOX_INT_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | MAILBOX_FULL_INT_STATUS | R | 0h | Mailbox full interrupt. Active HIGH. Cleared on read. This interrupt is set when mailbox becomes full which means there is no more space for messages sent from Host processor to internal uCPU and when this interrupt is enabled in EDP_CORE_MAILBOX_INT_MASK_P register. It is set when mailbox_full bit transitions from 0 to 1. |
| 0 | MAILBOX_EMPTY_INT_STATUS | R | 0h | Mailbox not-empty interrupt. Active HIGH. Cleared on read. This interrupt is set when mailbox becomes not-empty which means there is a response in the mailbox available to read by the Host processor and when interrupt is enabled in EDP_CORE_MAILBOX_INT_MASK_P register. It is set when mailbox_empty bit transitions from 1 to 0. |

8.5.16 EDP_CORE_SW_CLK_I_P Register (Offset = 3Ch) [reset = 0h]

EDP_CORE_SW_CLK_I_P is shown in [Figure 8-72](#) and described in [Table 8-154](#).

Return to [Summary Table](#).

Core Clock frequency

Table 8-153. EDP_CORE_SW_CLK_I_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 003Ch |

Figure 8-72. EDP_CORE_SW_CLK_I_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_CLOCK_VAL_L | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-154. EDP_CORE_SW_CLK_I_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_CLOCK_VAL_L | R/W | 0h | Fractional of the clock decimal value. Should be loaded by API to the value that reflects the frequency of clock provided to core clock input. |

8.5.17 EDP_CORE_SW_CLK_H_P Register (Offset = 40h) [reset = 64h]

EDP_CORE_SW_CLK_H_P is shown in [Figure 8-73](#) and described in [Table 8-156](#).

Return to [Summary Table](#).

Core Clock frequency

Table 8-155. EDP_CORE_SW_CLK_H_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0040h |

Figure 8-73. EDP_CORE_SW_CLK_H_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_CLOCK_VAL_H | | | | | | | |
| R-0h | | | | | | | | R/W-64h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-156. EDP_CORE_SW_CLK_H_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_CLOCK_VAL_H | R/W | 64h | Clock frequency in decimal values. Should be loaded by API to the value that reflects the frequency of clock provided to core clock input. |

8.5.18 EDP_CORE_SW_EVENTS0_P Register (Offset = 44h) [reset = 0h]

EDP_CORE_SW_EVENTS0_P is shown in [Figure 8-74](#) and described in [Table 8-158](#).

Return to [Summary Table](#).

Bits [7:0] of the software events status vector. This register is used to report internal events that have been detected by the firmware to the host processor. Register is written by the internal uCPU. It is cleared upon read by the Host processor. Reported events can be source of interrupt reported in APB_INT_STATUS[1] register if this interrupt is enabled.

Detailed description of the currently supported events can be found in HD Display TX Controller Programming Interface document.

Table 8-157. EDP_CORE_SW_EVENTS0_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0044h |

Figure 8-74. EDP_CORE_SW_EVENTS0_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-158. EDP_CORE_SW_EVENTS0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS7_0 | R | 0h | Each bit represents a separate event reported by the internal uCPU. If bit is set to 1 event is reported. All events are cleared upon read. Detailed description in HD Display TX Controller Programming Interface document. |

8.5.19 EDP_CORE_SW_EVENTS1_P Register (Offset = 48h) [reset = 0h]

EDP_CORE_SW_EVENTS1_P is shown in [Figure 8-75](#) and described in [Table 8-160](#).

Return to [Summary Table](#).

SW Event 1 register

Table 8-159. EDP_CORE_SW_EVENTS1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0048h |

Figure 8-75. EDP_CORE_SW_EVENTS1_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS15_8 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-160. EDP_CORE_SW_EVENTS1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS15_8 | R | 0h | Each bit represents a separate event reported by the internal uCPU. If bit is set to 1 event is reported. All events are cleared upon read. Detailed description in HD Display TX Controller Programming Interface document. |

8.5.20 EDP_CORE_SW_EVENTS2_P Register (Offset = 4Ch) [reset = 0h]

EDP_CORE_SW_EVENTS2_P is shown in [Figure 8-76](#) and described in [Table 8-162](#).

Return to [Summary Table](#).

SW Event 2 register

Table 8-161. EDP_CORE_SW_EVENTS2_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 004Ch |

Figure 8-76. EDP_CORE_SW_EVENTS2_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS23_16 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-162. EDP_CORE_SW_EVENTS2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS23_16 | R | 0h | Each bit represents a separate event reported by the internal uCPU. If bit is set to 1 event is reported. All events are cleared upon read. Detailed description in HD Display TX Controller Programming Interface document. |

8.5.21 EDP_CORE_SW_EVENTS3_P Register (Offset = 50h) [reset = 0h]

EDP_CORE_SW_EVENTS3_P is shown in [Figure 8-77](#) and described in [Table 8-164](#).

Return to [Summary Table](#).

SW Event 3 register

Table 8-163. EDP_CORE_SW_EVENTS3_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0050h |

Figure 8-77. EDP_CORE_SW_EVENTS3_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS31_24 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-164. EDP_CORE_SW_EVENTS3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS31_24 | R | 0h | Each bit represents a separate event reported by the internal uCPU. If bit is set to 1 event is reported. All events are cleared upon read. Detailed description in HD Display TX Controller Programming Interface document. |

8.5.22 EDP_CORE_XT_OCD_CTRL_P Register (Offset = 60h) [reset = 3h]

EDP_CORE_XT_OCD_CTRL_P is shown in [Figure 8-78](#) and described in [Table 8-166](#).

Return to [Summary Table](#).

Internal CPU - On Chip Debug (OCD) Ctrl Register

**Table 8-165. EDP_CORE_XT_OCD_CTRL_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0060h |

Figure 8-78. EDP_CORE_XT_OCD_CTRL_P Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|-----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | XT_OCDHALT ONRESET | XT_DRESET |
| R-0h | | | | | | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-166. EDP_CORE_XT_OCD_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | XT_OCDHALTONRESET | R/W | 1h | Internal CPU - Halt On Reget configuration register |
| 0 | XT_DRESET | R/W | 1h | Internal CPU - Dreset control register |

8.5.23 EDP_CORE_XT_OCD_CTRL_RO_P Register (Offset = 64h) [reset = 0h]

EDP_CORE_XT_OCD_CTRL_RO_P is shown in [Figure 8-79](#) and described in [Table 8-168](#).

Return to [Summary Table](#).

Internal CPU - OCD R0 mode configuration

Table 8-167. EDP_CORE_XT_OCD_CTRL_RO_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0064h |

Figure 8-79. EDP_CORE_XT_OCD_CTRL_RO_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | XT_XOCDMODE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-168. EDP_CORE_XT_OCD_CTRL_RO_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 0 | XT_XOCDMODE | R | 0h | Internal CPU - OCD mode configuration |

8.5.24 EDP_CORE_APB_INT_MASK_P Register (Offset = 6Ch) [reset = Fh]

EDP_CORE_APB_INT_MASK_P is shown in [Figure 8-80](#) and described in [Table 8-170](#).

Return to [Summary Table](#).

APB Interrupt Mask Register

Table 8-169. EDP_CORE_APB_INT_MASK_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 006Ch |

Figure 8-80. EDP_CORE_APB_INT_MASK_P Register

| | | | | | | | |
|----------|----|----|----|-----------------------|-----------------------|----------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | APB_CEC_INT R_MASK | APB_PIF_INTR _MASK | APB_SW_INTR _MASK | APB_MAILBOX _INTR_MASK |
| R-0h | | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-170. EDP_CORE_APB_INT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 3 | APB_CEC_INTR_MASK | R/W | 1h | Reserved field. 0x0 when read. Writes ignored. |
| 2 | APB_PIF_INTR_MASK | R/W | 1h | PIF module Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 1 | APB_SW_INTR_MASK | R/W | 1h | SW Event Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |

Table 8-170. EDP_CORE_APB_INT_MASK_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 0 | APB_MAILBOX_INTR_MASK | R/W | 1h | Mailbox Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.5.25 EDP_CORE_APB_INT_STATUS_P Register (Offset = 70h) [reset = 0h]

EDP_CORE_APB_INT_STATUS_P is shown in [Figure 8-81](#) and described in [Table 8-172](#).

Return to [Summary Table](#).

APB interrupt status register

Table 8-171. EDP_CORE_APB_INT_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0070h |

Figure 8-81. EDP_CORE_APB_INT_STATUS_P Register

| | | | | | | | |
|----------|----|----|----|---------------------|---------------------|--------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | APB_CEC_INTR_STATUS | APB_PIF_INTR_STATUS | APB_SW_INTR_STATUS | APB_MAILBOX_INTR_STATUS |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-172. EDP_CORE_APB_INT_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 3 | APB_CEC_INTR_STATUS | R | 0h | Reserved. |
| 2 | APB_PIF_INTR_STATUS | R | 0h | PIF module Interrupt status. Active HIGH. If this bit is set further status should be read from SOURCE_PIF_INTERRUPT_SOURCE register. This bit is cleared automatically on read from SOURCE_PIF_INTERRUPT_SOURCE register. |
| 1 | APB_SW_INTR_STATUS | R | 0h | SW Events Interrupt status. Active HIGH. If this bit is set further status should be read from SW_EVENTS _n registers. This bit is cleared automatically on read from SW_EVENTS _n registers if there are no more events. |

Table 8-172. EDP_CORE_APB_INT_STATUS_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 0 | APB_MAILBOX_INTR_STATUS | R | 0h | <p>Mailbox Interrupt status.</p> <p>Active HIGH.</p> <p>If this bit is set further status should be read from MAILBOX_INT_STATUS register.</p> <p>This bit is cleared automatically on read from MAILBOX_INT_STATUS register.</p> |

8.5.26 EDP_CORE_CDNS_DID_P Register (Offset = A0h) [reset = 8546h]

EDP_CORE_CDNS_DID_P is shown in [Figure 8-82](#) and described in [Table 8-174](#).

Return to [Summary Table](#).

Number identifying the IP.

Corresponds to IP Part Number.

Table 8-173. EDP_CORE_CDNS_DID_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 00A0h |

Figure 8-82. EDP_CORE_CDNS_DID_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IPVER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-8546h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-174. EDP_CORE_CDNS_DID_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | IPVER | R | 8546h | 0x8546 - DisplayPort 1.4/EmbeddedDisplayPort 1.4 Tx Combo Controller |

8.5.27 EDP_CORE_CDNS_RID0_P Register (Offset = A4h) [reset = 2000h]

EDP_CORE_CDNS_RID0_P is shown in [Figure 8-83](#) and described in [Table 8-176](#).

Return to [Summary Table](#).

Number identifying IP version.

Table 8-175. EDP_CORE_CDNS_RID0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 00A4h |

Figure 8-83. EDP_CORE_CDNS_RID0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | IP_VERSION | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-2000h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-176. EDP_CORE_CDNS_RID0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | IP_VERSION | R | 2000h | IP version: r [15:4]v [3:0] |

8.5.28 EDP_CORE_CDNS_RID1_P Register (Offset = A8h) [reset = 10001100h]

EDP_CORE_CDNS_RID1_P is shown in [Figure 8-84](#) and described in [Table 8-178](#).

Return to [Summary Table](#).

Numbers identifying PHY and AUX version

Table 8-177. EDP_CORE_CDNS_RID1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 00A8h |

Figure 8-84. EDP_CORE_CDNS_RID1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_VERSION | | | | | | | | | | | | | | | | PHY_VERSION | | | | | | | | | | | | | | | |
| R-1000h | | | | | | | | | | | | | | | | R-1100h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-178. EDP_CORE_CDNS_RID1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---------------------------------------|
| 31-16 | AUX_VERSION | R | 1000h | AUX version: r [31:20]v [19:16] |
| 15-0 | PHY_VERSION | R | 1100h | PHY version: r [15:4]v [3:0] |

8.5.29 EDP_CORE_CDNS_CFGS0_P Register (Offset = ACh) [reset = 01450002h]

EDP_CORE_CDNS_CFGS0_P is shown in [Figure 8-85](#) and described in [Table 8-180](#).

Return to [Summary Table](#).

Numbers identifying the capabilities/configuration of the MHDP controller. Values not explicitly listed below are reserved for future use.

Table 8-179. EDP_CORE_CDNS_CFGS0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 00ACh |

Figure 8-85. EDP_CORE_CDNS_CFGS0_P Register

| | | | | | | | |
|-------------------------|----|----|----|---------------------|----|-------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | AUDIO_STREAM_NUMBER | | | |
| R-0h | | | | R-1h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VIDEO_STREAM_NUMBER | | | | ASF_SUPPORT | | DSC_SUPPORT | |
| R-4h | | | | R-1h | | R-1h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IP_NUMBER_FAMILY | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IP_NUMBER_CONFIGURATION | | | | | | | |
| R-2h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-180. EDP_CORE_CDNS_CFGS0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved |
| 27-24 | AUDIO_STREAM_NUMBER | R | 1h | Secondary configuration. Number of audio streams supported |
| 23-20 | VIDEO_STREAM_NUMBER | R | 4h | Secondary configuration. Number of video streams supported |
| 19-18 | ASF_SUPPORT | R | 1h | Secondary configuration. ASF support. 0x 0: ASF not supported, 0x 1: ASF supported |
| 17-16 | DSC_SUPPORT | R | 1h | Secondary configuration. DSC support. 0x 0: DSC not supported, 0x 1: DSC supported |
| 15-8 | IP_NUMBER_FAMILY | R | 0h | Main configuration. IP Family Code. 0x 00: Display TX Controller, 0x 01: Display RX Controller |

Table 8-180. EDP_CORE_CDNS_CFGS0_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 7-0 | IP_NUMBER_CONFIGURATION | R | 2h | Main configuration. IP configuration. 0x 00 - HDMI+DP+HDPC 0x 01 - HDMI+HDCP 0x 02 - DP+HDCP 0x 03 - HDMI+DP |

8.5.30 EDP_CORE_CDNS_CFGS1_P Register (Offset = B0h) [reset = 08100801h]

EDP_CORE_CDNS_CFGS1_P is shown in [Figure 8-86](#) and described in [Table 8-182](#).

Return to [Summary Table](#).

Numbers identifying type of PHY and AUX are integrated in the IPS. Fixed for a given IPS configuration.

Table 8-181. EDP_CORE_CDNS_CFGS1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 00B0h |

Figure 8-86. EDP_CORE_CDNS_CFGS1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_NUMBER | | | | | | | | | | | | | | | | PHY_NUMBER | | | | | | | | | | | | | | | |
| R-810h | | | | | | | | | | | | | | | | R-801h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-182. EDP_CORE_CDNS_CFGS1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | AUX_NUMBER | R | 810h | AUX IP Number, according to versioning scheme. |
| 15-0 | PHY_NUMBER | R | 801h | PHY IP Number, according to versioning scheme. |

8.5.31 EDP_CORE_SHIFT_PATTERN_IN_3_0_P Register (Offset = 800h) [reset = 0h]

EDP_CORE_SHIFT_PATTERN_IN_3_0_P is shown in [Figure 8-87](#) and described in [Table 8-184](#).

Return to [Summary Table](#).

HDMI shift pattern 3-0

Table 8-183.
EDP_CORE_SHIFT_PATTERN_IN_3_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0800h |

Figure 8-87. EDP_CORE_SHIFT_PATTERN_IN_3_0_P Register

| | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SOURCE_PHY_SHIFT_PATTERN3 | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SOURCE_PHY_SHIFT_PATTERN2 | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PHY_SHIFT_PATTERN1 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PHY_SHIFT_PATTERN0 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-184. EDP_CORE_SHIFT_PATTERN_IN_3_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|-----------------------------|
| 31-24 | SOURCE_PHY_SHIFT_P ATTERN3 | R/W | 0h | Input to hdmi_pattern_shift |
| 23-16 | SOURCE_PHY_SHIFT_P ATTERN2 | R/W | 0h | Input to hdmi_pattern_shift |
| 15-8 | SOURCE_PHY_SHIFT_P ATTERN1 | R/W | 0h | Input to hdmi_pattern_shift |
| 7-0 | SOURCE_PHY_SHIFT_P ATTERN0 | R/W | 0h | Input to hdmi_pattern_shift |

8.5.32 EDP_CORE_SHIFT_PATTERN_IN_4_7_P Register (Offset = 804h) [reset = 0h]

EDP_CORE_SHIFT_PATTERN_IN_4_7_P is shown in [Figure 8-88](#) and described in [Table 8-186](#).

Return to [Summary Table](#).

HDMI shift pattern 4-7

Table 8-185.
EDP_CORE_SHIFT_PATTERN_IN_4_7_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0804h |

Figure 8-88. EDP_CORE_SHIFT_PATTERN_IN_4_7_P Register

| | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SOURCE_PHY_SHIFT_PATTERN7 | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SOURCE_PHY_SHIFT_PATTERN6 | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PHY_SHIFT_PATTERN5 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PHY_SHIFT_PATTERN4 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-186. EDP_CORE_SHIFT_PATTERN_IN_4_7_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|-----------------------------|
| 31-24 | SOURCE_PHY_SHIFT_P ATTERN7 | R/W | 0h | Input to hdmi_pattern_shift |
| 23-16 | SOURCE_PHY_SHIFT_P ATTERN6 | R/W | 0h | Input to hdmi_pattern_shift |
| 15-8 | SOURCE_PHY_SHIFT_P ATTERN5 | R/W | 0h | Input to hdmi_pattern_shift |
| 7-0 | SOURCE_PHY_SHIFT_P ATTERN4 | R/W | 0h | Input to hdmi_pattern_shift |

8.5.33 EDP_CORE_SHIFT_PATTERN_IN9_8_P Register (Offset = 808h) [reset = 0h]

EDP_CORE_SHIFT_PATTERN_IN9_8_P is shown in [Figure 8-89](#) and described in [Table 8-188](#).

Return to [Summary Table](#).

HDMI shift pattern 9-8 with control bits

Table 8-187. EDP_CORE_SHIFT_PATTERN_IN9_8_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0808h |

Figure 8-89. EDP_CORE_SHIFT_PATTERN_IN9_8_P Register

| | | | | | | | |
|---------------------------|----|----|-----------------------------|----|---------------------|-----------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | SOURCE_PHY_SHIFT_REPETITION | | SOURCE_PHY_SHIFT_EN | SOURCE_PHY_SHIFT_LOAD | |
| R-0h | | | R/W-0h | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PHY_SHIFT_PATTERN9 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PHY_SHIFT_PATTERN8 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-188. EDP_CORE_SHIFT_PATTERN_IN9_8_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-21 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 20-18 | SOURCE_PHY_SHIFT_REPETITION | R/W | 0h | Shift repetition Number |
| 17 | SOURCE_PHY_SHIFT_EN | R/W | 0h | When 1 enable the Shift pattern Mechanism |
| 16 | SOURCE_PHY_SHIFT_LOAD | R/W | 0h | When 1 load the 80 bits of data |
| 15-8 | SOURCE_PHY_SHIFT_PATTERN9 | R/W | 0h | Input to hdmi_pattern_shift |
| 7-0 | SOURCE_PHY_SHIFT_PATTERN8 | R/W | 0h | Input to hdmi_pattern_shift |

8.5.34 EDP_CORE_PRBS_CNTRL_P Register (Offset = 80Ch) [reset = 2222h]

EDP_CORE_PRBS_CNTRL_P is shown in [Figure 8-90](#) and described in [Table 8-190](#).

Return to [Summary Table](#).

PRBS control

Table 8-189. EDP_CORE_PRBS_CNTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 080Ch |

Figure 8-90. EDP_CORE_PRBS_CNTRL_P Register

| | | | | | | | |
|-------------------------------|-----------------------|----|-------------------------------|----|-----------------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PHY_PRBS3_OUT_M ODE | SOURCE_PHY_PRBS3_MODE | | SOURCE_PHY_PRBS2_OUT_M ODE | | SOURCE_PHY_PRBS2_MODE | | |
| R/W-0h | R/W-2h | | R/W-0h | | R/W-2h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PHY_PRBS1_OUT_M ODE | SOURCE_PHY_PRBS1_MODE | | SOURCE_PHY_PRBS0_OUT_M ODE | | SOURCE_PHY_PRBS0_MODE | | |
| R/W-0h | R/W-2h | | R/W-0h | | R/W-2h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-190. EDP_CORE_PRBS_CNTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 15-14 | SOURCE_PHY_PRBS3_OUT_MODE | R/W | 0h | 00 = idle, output all zeros 01 = output 8 bits on pattern [7:0] 10 = output 1 bit on pattern[9] and output inverted bit on pattern[8] 11 = output 10 bits on pattern [9:0] |
| 13-12 | SOURCE_PHY_PRBS3_MODE | R/W | 2h | 00 = PRBS11 01 = PRBS15 10 = PRBS7 11 = PRBS31 |
| 11-10 | SOURCE_PHY_PRBS2_OUT_MODE | R/W | 0h | 00 = idle, output all zeros 01 = output 8 bits on pattern [7:0] 10 = output 1 bit on pattern[9] and output inverted bit on pattern[8] 11 = output 10 bits on pattern [9:0] |

Table 8-190. EDP_CORE_PRBS_CNTRL_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|---|
| 9-8 | SOURCE_PHY_PRBS2_MODE | R/W | 2h | 00 = PRBS11 01 = PRBS15 10 = PRBS7 11 = PRBS31 |
| 7-6 | SOURCE_PHY_PRBS1_OUT_MODE | R/W | 0h | 00 = idle, output all zeros 01 = output 8 bits on pattern [7:0] 10 = output 1 bit on pattern[9] and output inverted bit on pattern[8] 11 = output 10 bits on pattern [9:0] |
| 5-4 | SOURCE_PHY_PRBS1_MODE | R/W | 2h | 00 = PRBS11 01 = PRBS15 10 = PRBS7 11 = PRBS31 |
| 3-2 | SOURCE_PHY_PRBS0_OUT_MODE | R/W | 0h | 00 = idle, output all zeros 01 = output 8 bits on pattern [7:0] 10 = output 1 bit on pattern[9] and output inverted bit on pattern[8] 11 = output 10 bits on pattern [9:0] |
| 1-0 | SOURCE_PHY_PRBS0_MODE | R/W | 2h | 00 = PRBS11 01 = PRBS15 10 = PRBS7 11 = PRBS31 |

8.5.35 EDP_CORE_PRBS_ERR_INSERTION_P Register (Offset = 810h) [reset = 0h]

EDP_CORE_PRBS_ERR_INSERTION_P is shown in [Figure 8-91](#) and described in [Table 8-192](#).

Return to [Summary Table](#).

PRBS error insertion

Table 8-191. EDP_CORE_PRBS_ERR_INSERTION_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0810h |

Figure 8-91. EDP_CORE_PRBS_ERR_INSERTION_P Register

| | | | | | | | |
|-------------------|------------|-------------------|------------|-------------------|----|-------------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NUMBER_OF_ERRORS3 | | | | ADD_ERROR3 | | NUMBER_OF_ERRORS2 | |
| R/W-0h | | | | R/W-0h | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NUMBER_OF_ERRORS2 | | | ADD_ERROR2 | NUMBER_OF_ERRORS1 | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NUMBER_OF_ERRORS1 | ADD_ERROR1 | NUMBER_OF_ERRORS0 | | | | | ADD_ERROR0 |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-192. EDP_CORE_PRBS_ERR_INSERTION_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 23-19 | NUMBER_OF_ERRORS3 | R/W | 0h | The number of errors to be inserted when add_error is high. |
| 18 | ADD_ERROR3 | R/W | 0h | When high the PRBS generator inserts the number of errors written in number_of_errors field. |
| 17-13 | NUMBER_OF_ERRORS2 | R/W | 0h | The number of errors to be inserted when add_error is high. |
| 12 | ADD_ERROR2 | R/W | 0h | When high the PRBS generator inserts the number of errors written in number_of_errors field. |
| 11-7 | NUMBER_OF_ERRORS1 | R/W | 0h | The number of errors to be inserted when add_error is high. |
| 6 | ADD_ERROR1 | R/W | 0h | When high the PRBS generator inserts the number of errors written in number_of_errors field. |
| 5-1 | NUMBER_OF_ERRORS0 | R/W | 0h | The number of errors to be inserted when add_error is high. |
| 0 | ADD_ERROR0 | R/W | 0h | When high the PRBS generator inserts the number of errors written in number_of_errors field. |

8.5.36 EDP_CORE_LANES_CONFIG_P Register (Offset = 814h) [reset = 0060001Bh]

EDP_CORE_LANES_CONFIG_P is shown in [Figure 8-92](#) and described in [Table 8-194](#).

Return to [Summary Table](#).

Lane control register: swap, order, polarity

Table 8-193. EDP_CORE_LANES_CONFIG_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0814h |

Figure 8-92. EDP_CORE_LANES_CONFIG_P Register

| | | | | | | | |
|-----------------------|-----------------------|------------------------|--------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | SOURCE_PHY_20_10 | SOURCE_PHY_COMB_BYPASS | SOURCE_PHY_DATA_DELAY_EN | SOURCE_PHY_LANE3_POLARITY | SOURCE_PHY_LANE2_POLARITY | SOURCE_PHY_LANE1_POLARITY | SOURCE_PHY_LANE0_POLARITY |
| R-0h | R/W-1h | R/W-1h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PHY_AUX_SPARE | | | | SOURCE_PHY_LANE3_LSB_MSB | SOURCE_PHY_LANE2_LSB_MSB | SOURCE_PHY_LANE1_LSB_MSB | SOURCE_PHY_LANE0_LSB_MSB |
| R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PHY_LANE3_SWAP | SOURCE_PHY_LANE2_SWAP | | SOURCE_PHY_LANE1_SWAP | | SOURCE_PHY_LANE0_SWAP | | |
| R/W-0h | R/W-1h | | R/W-2h | | R/W-3h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-194. EDP_CORE_LANES_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-23 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 22 | SOURCE_PHY_20_10 | R/W | 1h | 1'b 0: Data to PHY is 10 bit with char clock 1'd 1: Data to PHY is 20 bit with data clock |
| 21 | SOURCE_PHY_COMB_BYPASS | R/W | 1h | Bypass swap invert and all combination |
| 20 | SOURCE_PHY_DATA_DELAY_EN | R/W | 0h | enable configurable delay of lanes to be activated.if this bit is 0 the delay is only activated for DisplayPort mode with source_phy_data_sel=prbs or shift-mem |
| 19 | SOURCE_PHY_LANE3_POLARITY | R/W | 0h | Reverse polarity of data, lane3 |
| 18 | SOURCE_PHY_LANE2_POLARITY | R/W | 0h | Reverse polarity of data, lane2 |
| 17 | SOURCE_PHY_LANE1_POLARITY | R/W | 0h | Reverse polarity of data, lane1 |

Table 8-194. EDP_CORE_LANES_CONFIG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---------------------------------|
| 16 | SOURCE_PHY_LANE0_POLARITY | R/W | 0h | Reverse polarity of data, lane0 |
| 15-12 | SOURCE_PHY_AUX_SPARE | R/W | 0h | Spare bits for aux **1.1** |
| 11 | SOURCE_PHY_LANE3_LSB_MSB | R/W | 0h | Reverse order of data, lane3 |
| 10 | SOURCE_PHY_LANE2_LSB_MSB | R/W | 0h | Reverse order of data, lane2 |
| 9 | SOURCE_PHY_LANE1_LSB_MSB | R/W | 0h | Reverse order of data, lane1 |
| 8 | SOURCE_PHY_LANE0_LSB_MSB | R/W | 0h | Reverse order of data, lane0 |
| 7-6 | SOURCE_PHY_LANE3_SWAP | R/W | 0h | Swap control lane3 |
| 5-4 | SOURCE_PHY_LANE2_SWAP | R/W | 1h | Swap control lane2 |
| 3-2 | SOURCE_PHY_LANE1_SWAP | R/W | 2h | Swap control lane1 |
| 1-0 | SOURCE_PHY_LANE0_SWAP | R/W | 3h | Swap control lane0 |

8.5.37 EDP_CORE_PHY_DATA_SEL_P Register (Offset = 818h) [reset = 0h]

EDP_CORE_PHY_DATA_SEL_P is shown in [Figure 8-93](#) and described in [Table 8-196](#).

Return to [Summary Table](#).

PHY data select DP/HDMI and HDMI data source

Table 8-195. EDP_CORE_PHY_DATA_SEL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0818h |

Figure 8-93. EDP_CORE_PHY_DATA_SEL_P Register

| | | | | | | | |
|----------|----|----|---------------------|----|---------------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | SOURCE_PHY_MHDP_SEL | | SOURCE_PHY_DATA_SEL | | |
| R-0h | | | R/W-0h | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-196. EDP_CORE_PHY_DATA_SEL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-5 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 4-3 | SOURCE_PHY_MHDP_SEL | R/W | 0h | 3'd 0: tx_data = DP 3'd 1: tx_data = HDMI 3'd 2: tx_data = RSRV 3'd 3: tx_data = RSRV |
| 2-0 | SOURCE_PHY_DATA_SEL | R/W | 0h | 3'd 0: tx_data = phy_dout 3'd 1: tx_data = phy_dout_bypass 3'd 2: tx_data = source_phy_prbs_pout 3'd 3: tx_data = source_phy_shift_pout |

8.5.38 EDP_CORE_LANES_DEL_VAL_P Register (Offset = 81Ch) [reset = 6420h]

EDP_CORE_LANES_DEL_VAL_P is shown in [Figure 8-94](#) and described in [Table 8-198](#).

Return to [Summary Table](#).

Lane delay control

**Table 8-197. EDP_CORE_LANES_DEL_VAL_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 081Ch |

Figure 8-94. EDP_CORE_LANES_DEL_VAL_P Register

| | | | | | | | |
|--------------------------|----|----|----|--------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PHY_LANE3_DEL_VAL | | | | SOURCE_PHY_LANE2_DEL_VAL | | | |
| R/W-6h | | | | R/W-4h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PHY_LANE1_DEL_VAL | | | | SOURCE_PHY_LANE0_DEL_VAL | | | |
| R/W-2h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-198. EDP_CORE_LANES_DEL_VAL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 15-12 | SOURCE_PHY_LANE3_DEL_VAL | R/W | 6h | delay for lane 3 this parameter can take values from 0 up to 8. All other values are reserved |
| 11-8 | SOURCE_PHY_LANE2_DEL_VAL | R/W | 4h | delay for lane 2 this parameter can take values from 0 up to 8. All other values are reserved |
| 7-4 | SOURCE_PHY_LANE1_DEL_VAL | R/W | 2h | delay for lane 1 this parameter can take values from 0 up to 8. All other values are reserved |
| 3-0 | SOURCE_PHY_LANE0_DEL_VAL | R/W | 0h | delay for lane 0 this parameter can take values from 0 up to 8. All other values are reserved |

8.5.39 EDP_CORE_SOURCE_DPTX_CAR_P Register (Offset = 904h) [reset = 0h]

EDP_CORE_SOURCE_DPTX_CAR_P is shown in [Figure 8-95](#) and described in [Table 8-200](#).

Return to [Summary Table](#).

DP TX clock and reset ctrl register

Table 8-199. EDP_CORE_SOURCE_DPTX_CAR_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0904h |

Figure 8-95. EDP_CORE_SOURCE_DPTX_CAR_P Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------|---------------------------|----------------------------|-----------------------|----------------------------|-----------------------|---------------------------|----------------------|
| RESERVED | | | | | | CFG_DPTX_VIF_CLK_RSTN_EN7 | CFG_DPTX_VIF_CLK_EN7 |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CFG_DPTX_VIF_CLK_RSTN_EN6 | CFG_DPTX_VIF_CLK_EN6 | CFG_DPTX_VIF_CLK_RSTN_EN5 | CFG_DPTX_VIF_CLK_EN5 | CFG_DPTX_VIF_CLK_RSTN_EN4 | CFG_DPTX_VIF_CLK_EN4 | CFG_DPTX_VIF_CLK_RSTN_EN3 | CFG_DPTX_VIF_CLK_EN3 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CFG_DPTX_VIF_CLK_RSTN_EN2 | CFG_DPTX_VIF_CLK_EN2 | CFG_DPTX_VIF_CLK_RSTN_EN1 | CFG_DPTX_VIF_CLK_EN1 | DPTX_FRMR_DATA_CLK_RSTN_EN | DPTX_FRMR_DATA_CLK_EN | DPTX_PHY_DATA_RSTN_EN | DPTX_PHY_DATA_CLK_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPTX_PHY_CHARACTER_RSTN_EN | DPTX_PHY_CHARACTER_CLK_EN | SOURCE_AUX_SYS_CLK_RSTN_EN | SOURCE_AUX_SYS_CLK_EN | DPTX_SYS_CLK_RSTN_EN | DPTX_SYS_CLK_EN | CFG_DPTX_VIF_CLK_RSTN_EN | CFG_DPTX_VIF_CLK_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-200. EDP_CORE_SOURCE_DPTX_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 25 | CFG_DPTX_VIF_CLK_RSTN_EN7 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 7 - active low |
| 24 | CFG_DPTX_VIF_CLK_EN7 | R/W | 0h | dptx_vif_clk enable for stream number 7 - active high |
| 23 | CFG_DPTX_VIF_CLK_RSTN_EN6 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 6 - active low |
| 22 | CFG_DPTX_VIF_CLK_EN6 | R/W | 0h | dptx_vif_clk enable for stream number 6 - active high |
| 21 | CFG_DPTX_VIF_CLK_RSTN_EN5 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 5 - active low |

Table 8-200. EDP_CORE_SOURCE_DPTX_CAR_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 20 | CFG_DPTX_VIF_CLK_EN5 | R/W | 0h | dptx_vif_clk enable for stream number 5 - active high |
| 19 | CFG_DPTX_VIF_CLK_RSTN_EN4 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 4 - active low |
| 18 | CFG_DPTX_VIF_CLK_EN4 | R/W | 0h | dptx_vif_clk enable for stream number 4 - active high |
| 17 | CFG_DPTX_VIF_CLK_RSTN_EN3 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 3 - active low |
| 16 | CFG_DPTX_VIF_CLK_EN3 | R/W | 0h | dptx_vif_clk enable for stream number 3 - active high |
| 15 | CFG_DPTX_VIF_CLK_RSTN_EN2 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 2 - active low |
| 14 | CFG_DPTX_VIF_CLK_EN2 | R/W | 0h | dptx_vif_clk enable for stream number 2 - active high |
| 13 | CFG_DPTX_VIF_CLK_RSTN_EN1 | R/W | 0h | dptx_vif_clk_rstn enable for stream number 1 - active low |
| 12 | CFG_DPTX_VIF_CLK_EN1 | R/W | 0h | dptx_vif_clk enable for stream number 1 - active high |
| 11 | DPTX_FRMR_DATA_CLK_RSTN_EN | R/W | 0h | dptx_frmr_data_clk_rstn enable - active low |
| 10 | DPTX_FRMR_DATA_CLK_EN | R/W | 0h | dptx_frmr_data_clk enable - active high |
| 9 | DPTX_PHY_DATA_RSTN_EN | R/W | 0h | dptx_phy_data_rstn enable - active low |
| 8 | DPTX_PHY_DATA_CLK_EN | R/W | 0h | dptx_phy_data_clk enable - active high |
| 7 | DPTX_PHY_CHAR_RSTN_EN | R/W | 0h | dptx_phy_char_rstn enable - active low |
| 6 | DPTX_PHY_CHAR_CLK_EN | R/W | 0h | dptx_phy_char_clk enable - active high |
| 5 | SOURCE_AUX_SYS_CLK_RSTN_EN | R/W | 0h | source_aux_sys_clk_rstn enable - active low |
| 4 | SOURCE_AUX_SYS_CLK_EN | R/W | 0h | source_aux_sys_clk enable - active high |
| 3 | DPTX_SYS_CLK_RSTN_EN | R/W | 0h | dptx_sys_clk_rstn enable - active low |
| 2 | DPTX_SYS_CLK_EN | R/W | 0h | dptx_sys_clk enable - active high |
| 1 | CFG_DPTX_VIF_CLK_RSTN_EN | R/W | 0h | dptx_vif_clk_rstn enable - active low |
| 0 | CFG_DPTX_VIF_CLK_EN | R/W | 0h | dptx_vif_clk enable - active high |

8.5.40 EDP_CORE_SOURCE_PHY_CAR_P Register (Offset = 908h) [reset = 0h]

EDP_CORE_SOURCE_PHY_CAR_P is shown in [Figure 8-96](#) and described in [Table 8-202](#).

Return to [Summary Table](#).

Source PHY clock and reset ctrl register

Table 8-201. EDP_CORE_SOURCE_PHY_CAR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0908h |

Figure 8-96. EDP_CORE_SOURCE_PHY_CAR_P Register

| | | | | | | | |
|----------|----|----|----|---------------------------------|----------------------------|---------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | SOURCE_PHY_CHAR_OUT_CLK_RSTN_EN | SOURCE_PHY_CHAR_OUT_CLK_EN | SOURCE_PHY_DATA_OUT_CLK_RSTN_EN | SOURCE_PHY_DATA_OUT_CLK_EN |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-202. EDP_CORE_SOURCE_PHY_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | SOURCE_PHY_CHAR_OUT_CLK_RSTN_EN | R/W | 0h | source_phy_char_out_clk_rstn enable - active low |
| 2 | SOURCE_PHY_CHAR_OUT_CLK_EN | R/W | 0h | source_phy_char_out_clk enable - active high |
| 1 | SOURCE_PHY_DATA_OUT_CLK_RSTN_EN | R/W | 0h | source_phy_data_out_clk_rstn enable - active low |
| 0 | SOURCE_PHY_DATA_OUT_CLK_EN | R/W | 0h | source_phy_data_out_clk enable - active high |

8.5.41 EDP_CORE_SOURCE_PKT_CAR_P Register (Offset = 918h) [reset = 0h]

EDP_CORE_SOURCE_PKT_CAR_P is shown in [Figure 8-97](#) and described in [Table 8-204](#).

Return to [Summary Table](#).

PKT clock and reset ctrl register

**Table 8-203. EDP_CORE_SOURCE_PKT_CAR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0918h |

Figure 8-97. EDP_CORE_SOURCE_PKT_CAR_P Register

| | | | | | | | |
|----------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------------|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | SOURCE_PKT _DATA_RSTN_ EN7 | SOURCE_PKT _DATA_CLK_E N7 |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_PKT _DATA_RSTN_ EN6 | SOURCE_PKT _DATA_CLK_E N6 | SOURCE_PKT _DATA_RSTN_ EN5 | SOURCE_PKT _DATA_CLK_E N5 | SOURCE_PKT _DATA_RSTN_ EN4 | SOURCE_PKT _DATA_CLK_E N4 | SOURCE_PKT _DATA_RSTN_ EN3 | SOURCE_PKT _DATA_CLK_E N3 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SOURCE_PKT _DATA_RSTN_ EN2 | SOURCE_PKT _DATA_CLK_E N2 | SOURCE_PKT _DATA_RSTN_ EN1 | SOURCE_PKT _DATA_CLK_E N1 | SOURCE_PKT _SYS_RSTN_E N | SOURCE_PKT _SYS_CLK_EN | SOURCE_PKT _DATA_RSTN_ EN | SOURCE_PKT _DATA_CLK_E N |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-204. EDP_CORE_SOURCE_PKT_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 17 | SOURCE_PKT_DATA_RS TN_EN7 | R/W | 0h | source_pkt_data_rstn_en 7 - active low |
| 16 | SOURCE_PKT_DATA_CL K_EN7 | R/W | 0h | source_pkt_data_clk_en 7 - active high |
| 15 | SOURCE_PKT_DATA_RS TN_EN6 | R/W | 0h | source_pkt_data_rstn_en 6 - active low |
| 14 | SOURCE_PKT_DATA_CL K_EN6 | R/W | 0h | source_pkt_data_clk_en 6 - active high |
| 13 | SOURCE_PKT_DATA_RS TN_EN5 | R/W | 0h | source_pkt_data_rstn_en 5 - active low |
| 12 | SOURCE_PKT_DATA_CL K_EN5 | R/W | 0h | source_pkt_data_clk_en 5 - active high |

Table 8-204. EDP_CORE_SOURCE_PKT_CAR_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|---|
| 11 | SOURCE_PKT_DATA_RSTN_EN4 | R/W | 0h | source_pkt_data_rstn_en 4 - active low |
| 10 | SOURCE_PKT_DATA_CLK_EN4 | R/W | 0h | source_pkt_data_clk_en 4 - active high |
| 9 | SOURCE_PKT_DATA_RSTN_EN3 | R/W | 0h | source_pkt_data_rstn_en 3 - active low |
| 8 | SOURCE_PKT_DATA_CLK_EN3 | R/W | 0h | source_pkt_data_clk_en 3 - active high |
| 7 | SOURCE_PKT_DATA_RSTN_EN2 | R/W | 0h | source_pkt_data_rstn_en 2 - active low |
| 6 | SOURCE_PKT_DATA_CLK_EN2 | R/W | 0h | source_pkt_data_clk_en 2 - active high |
| 5 | SOURCE_PKT_DATA_RSTN_EN1 | R/W | 0h | source_pkt_data_rstn_en 1 - active low |
| 4 | SOURCE_PKT_DATA_CLK_EN1 | R/W | 0h | source_pkt_data_clk_en 1 - active high |
| 3 | SOURCE_PKT_SYS_RSTN_EN | R/W | 0h | source_pkt_sys_rstn_en - active low |
| 2 | SOURCE_PKT_SYS_CLK_EN | R/W | 0h | source_pkt_sys_clk_en - active high |
| 1 | SOURCE_PKT_DATA_RSTN_EN | R/W | 0h | source_pkt_data_rstn_en - active low |
| 0 | SOURCE_PKT_DATA_CLK_EN | R/W | 0h | source_pkt_data_clk_en - active high |

8.5.42 EDP_CORE_SOURCE_AIF_CAR_P Register (Offset = 91Ch) [reset = 0h]

EDP_CORE_SOURCE_AIF_CAR_P is shown in [Figure 8-98](#) and described in [Table 8-206](#).

Return to [Summary Table](#).

AIF clock and reset ctrl register

**Table 8-205. EDP_CORE_SOURCE_AIF_CAR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 091Ch |

Figure 8-98. EDP_CORE_SOURCE_AIF_CAR_P Register

| | | | | | | | |
|----------|----|----|----|----------------------------|---------------------------|------------------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | SOURCE_AIF_ SYS_RSTN_EN | SOURCE_AIF_ SYS_CLK_EN | SOURCE_AIF_ PKT_CLK_RST N_EN | SOURCE_AIF_ PKT_CLK_EN |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-206. EDP_CORE_SOURCE_AIF_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | SOURCE_AIF_SYS_RSTN_EN | R/W | 0h | source_aif_sys_rstn enable - active low |
| 2 | SOURCE_AIF_SYS_CLK_EN | R/W | 0h | source_aif_sys_clk enable - active high |
| 1 | SOURCE_AIF_PKT_CLK_RSTN_EN | R/W | 0h | source_aif_pkt_clk_rstn enable - active low |
| 0 | SOURCE_AIF_PKT_CLK_EN | R/W | 0h | source_aif_pkt_clk enable - active high |

8.5.43 EDP_CORE_SOURCE_CIPHER_CAR_P Register (Offset = 920h) [reset = 0h]

EDP_CORE_SOURCE_CIPHER_CAR_P is shown in [Figure 8-99](#) and described in [Table 8-208](#).

Return to [Summary Table](#).

Cipher clock and reset ctrl register

Table 8-207. EDP_CORE_SOURCE_CIPHER_CAR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0920h |

Figure 8-99. EDP_CORE_SOURCE_CIPHER_CAR_P Register

| | | | | | | | |
|----------|----|----|----|----------------------------------|--------------------------|--------------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | SOURCE_CIPHER_SYSTEM_CLK_RSTN_EN | SOURCE_CIPHER_SYS_CLK_EN | SOURCE_CIPHER_CHAR_CLK_RSTN_EN | SOURCE_CIPHER_CHAR_CLK_EN |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-208. EDP_CORE_SOURCE_CIPHER_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | SOURCE_CIPHER_SYSTEM_CLK_RSTN_EN | R/W | 0h | source_cipher_system_clk_rstn enable - active low [Only when HDCP used] |
| 2 | SOURCE_CIPHER_SYS_CLK_EN | R/W | 0h | source_cipher_sys_clk enable - active high [Only when HDCP used] |
| 1 | SOURCE_CIPHER_CHAR_CLK_RSTN_EN | R/W | 0h | source_cipher_char_clk_rstn enable - active low [Only when HDCP used] |
| 0 | SOURCE_CIPHER_CHAR_CLK_EN | R/W | 0h | source_cipher_char_clk enable - active high [Only when HDCP used] |

8.5.44 EDP_CORE_SOURCE_CRYPTO_CAR_P Register (Offset = 924h) [reset = 0h]

EDP_CORE_SOURCE_CRYPTO_CAR_P is shown in [Figure 8-100](#) and described in [Table 8-210](#).

Return to [Summary Table](#).

Crypto clock and reset ctrl register

**Table 8-209. EDP_CORE_SOURCE_CRYPTO_CAR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0924h |

Figure 8-100. EDP_CORE_SOURCE_CRYPTO_CAR_P Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | SOURCE_CRY PTO_SYS_CLK _RSTN_EN | SOURCE_CRY PTO_SYS_CLK _EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-210. EDP_CORE_SOURCE_CRYPTO_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | SOURCE_CRYPTO_SYS _CLK_RSTN_EN | R/W | 0h | source_crypto_sys_clk_rstn enable - active low [Only when HDCP used] |
| 0 | SOURCE_CRYPTO_SYS _CLK_EN | R/W | 0h | source_crypto_sys_clk enable - active high [Only when HDCP used] |

8.5.45 EDP_CORE_SOURCE_SPDIF_CAR_P Register (Offset = 928h) [reset = 0h]

EDP_CORE_SOURCE_SPDIF_CAR_P is shown in [Figure 8-101](#) and described in [Table 8-212](#).

Return to [Summary Table](#).

SPDIF clock and reset ctrl register

Table 8-211. EDP_CORE_SOURCE_SPDIF_CAR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0928h |

Figure 8-101. EDP_CORE_SOURCE_SPDIF_CAR_P Register

| | | | | | | | |
|----------|----|----|----|---------------------|----------------|------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | SPDIF_MCLK_RSTN_EN0 | SPDIF_MCLK_EN0 | SPDIF_CDR_CLK_RSTN_EN0 | SPDIF_CDR_CLK_EN0 |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-212. EDP_CORE_SOURCE_SPDIF_CAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | SPDIF_MCLK_RSTN_EN0 | R/W | 0h | spdif_mclk_rstn enable 0 - active low |
| 2 | SPDIF_MCLK_EN0 | R/W | 0h | spdif_mclk enable 0 - active high |
| 1 | SPDIF_CDR_CLK_RSTN_EN0 | R/W | 0h | spdif_cdr_clk_rstn enable 0 - active low |
| 0 | SPDIF_CDR_CLK_EN0 | R/W | 0h | spdif_cdr_clk enable 0 - active high |

8.5.46 EDP_CORE_CM_CTRL_P Register (Offset = A00h) [reset = 0h]

EDP_CORE_CM_CTRL_P is shown in [Figure 8-102](#) and described in [Table 8-214](#).

Return to [Summary Table](#).

Clock Meter control

Table 8-213. EDP_CORE_CM_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A00h |

Figure 8-102. EDP_CORE_CM_CTRL_P Register

| | | | | | | | |
|----------|----------|----|----|------------------|------------------|--------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | I2S_MULT | | | SEL_AUD_LANE_REF | I2S_SEL_EXTERNAL | SPDIF_SEL_EXTERNAL | NMVID_SEL_EXTERNAL |
| R-0h | R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-214. EDP_CORE_CM_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6-4 | I2S_MULT | R/W | 0h | Select the division of N value for different I2S TDM configuration |
| 3 | SEL_AUD_LANE_REF | R/W | 0h | When 1 Select Audio CLK as a reference [HDMI] When 0 Select LANE CLK as a reference [DP] |
| 2 | I2S_SEL_EXTERNAL | R/W | 0h | When 1 Select external values of NMAUD [N/A] for I2S |
| 1 | SPDIF_SEL_EXTERNAL | R/W | 0h | When 1 Select external values of NMAUD [N/A] for SPDIF |
| 0 | NMVID_SEL_EXTERNAL | R/W | 0h | When 1 Select external values of NMVID [N/A] |

8.5.47 EDP_CORE_CM_I2S_CTRL_P Register (Offset = A04h) [reset = 04001000h]

EDP_CORE_CM_I2S_CTRL_P is shown in [Figure 8-103](#) and described in [Table 8-216](#).

Return to [Summary Table](#).

I2S clock control

Table 8-215. EDP_CORE_CM_I2S_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A04h |

Figure 8-103. EDP_CORE_CM_I2S_CTRL_P Register

| | | | | | | | |
|-------------|----|----|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | I2S_MEAS_TOLERANCE | | | |
| R-0h | | | | R/W-4h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| I2S_REF_CYC | | | | | | | |
| R/W-1000h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| I2S_REF_CYC | | | | | | | |
| R/W-1000h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I2S_REF_CYC | | | | | | | |
| R/W-1000h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-216. EDP_CORE_CM_I2S_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 27-24 | I2S_MEAS_TOLERANCE | R/W | 4h | Measurement tolerance of Audio clock to be stable in clocks |
| 23-0 | I2S_REF_CYC | R/W | 1000h | Reference cycles for I2S Audio meter |

8.5.48 EDP_CORE_CM_SPDIF_CTRL_P Register (Offset = A08h) [reset = 04001000h]

EDP_CORE_CM_SPDIF_CTRL_P is shown in [Figure 8-104](#) and described in [Table 8-218](#).

Return to [Summary Table](#).

SPDIF clock control

Table 8-217. EDP_CORE_CM_SPDIF_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A08h |

Figure 8-104. EDP_CORE_CM_SPDIF_CTRL_P Register

| | | | | | | | |
|---------------|----|----|----|----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | SPDIF_MEAS_TOLERANCE | | | |
| R-0h | | | | R/W-4h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SPDIF_REF_CYC | | | | | | | |
| R/W-1000h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SPDIF_REF_CYC | | | | | | | |
| R/W-1000h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_REF_CYC | | | | | | | |
| R/W-1000h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-218. EDP_CORE_CM_SPDIF_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 27-24 | SPDIF_MEAS_TOLERANCE | R/W | 4h | SPDIF measurement tolerance to be stable in clocks |
| 23-0 | SPDIF_REF_CYC | R/W | 1000h | Reference cycles of SPDIF measurement |

8.5.49 EDP_CORE_CM_VID_CTRL_P Register (Offset = A0Ch) [reset = 04008000h]

EDP_CORE_CM_VID_CTRL_P is shown in [Figure 8-105](#) and described in [Table 8-220](#).

Return to [Summary Table](#).

Video clock control

**Table 8-219. EDP_CORE_CM_VID_CTRL_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A0Ch |

Figure 8-105. EDP_CORE_CM_VID_CTRL_P Register

| | | | | | | | |
|---------------|----|----|----|----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | NMVID_MEAS_TOLERANCE | | | |
| R-0h | | | | R/W-4h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NMVID_REF_CYC | | | | | | | |
| R/W-8000h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NMVID_REF_CYC | | | | | | | |
| R/W-8000h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NMVID_REF_CYC | | | | | | | |
| R/W-8000h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-220. EDP_CORE_CM_VID_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 27-24 | NMVID_MEAS_TOLERANCE | R/W | 4h | Video measurement tolerance in pixel clock cycles |
| 23-0 | NMVID_REF_CYC | R/W | 8000h | Video Reference cycles |

8.5.50 EDP_CORE_CM_LANE_CTRL_P Register (Offset = A10h) [reset = 0h]

EDP_CORE_CM_LANE_CTRL_P is shown in [Figure 8-106](#) and described in [Table 8-222](#).

Return to [Summary Table](#).

Lane control

Table 8-221. EDP_CORE_CM_LANE_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A10h |

Figure 8-106. EDP_CORE_CM_LANE_CTRL_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | LANE_REF_CYC | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-222. EDP_CORE_CM_LANE_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | LANE_REF_CYC | R/W | 0h | Reference cycles when using lane clock as Reference [DP] |

8.5.51 EDP_CORE_I2S_NM_STABLE_P Register (Offset = A14h) [reset = 0h]

EDP_CORE_I2S_NM_STABLE_P is shown in [Figure 8-107](#) and described in [Table 8-224](#).

Return to [Summary Table](#).

I2S clock stable, audio clock measured

Table 8-223. EDP_CORE_I2S_NM_STABLE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A14h |

Figure 8-107. EDP_CORE_I2S_NM_STABLE_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | I2S_MNAUD_S TABLE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-224. EDP_CORE_I2S_NM_STABLE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | I2S_MNAUD_STABLE | R | 0h | I2S NMAUD Mesurment stable |

8.5.52 EDP_CORE_I2S_NCTS_STABLE_P Register (Offset = A18h) [reset = 0h]

EDP_CORE_I2S_NCTS_STABLE_P is shown in [Figure 8-108](#) and described in [Table 8-226](#).

Return to [Summary Table](#).

I2S clock stable, lane clock measured

**Table 8-225. EDP_CORE_I2S_NCTS_STABLE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A18h |

Figure 8-108. EDP_CORE_I2S_NCTS_STABLE_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | I2S_NCTS_STA BLE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-226. EDP_CORE_I2S_NCTS_STABLE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | I2S_NCTS_STABLE | R | 0h | i2s CTS measurement stable |

8.5.53 EDP_CORE_SPDIF_NM_STABLE_P Register (Offset = A1Ch) [reset = 0h]

EDP_CORE_SPDIF_NM_STABLE_P is shown in [Figure 8-109](#) and described in [Table 8-228](#).

Return to [Summary Table](#).

SPDIF clock stable, audio clock measured

Table 8-227. EDP_CORE_SPDIF_NM_STABLE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A1Ch |

Figure 8-109. EDP_CORE_SPDIF_NM_STABLE_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SPDIF_MNAUD_STABLE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-228. EDP_CORE_SPDIF_NM_STABLE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | SPDIF_MNAUD_STABLE | R | 0h | SPDIF NMAUD measurement stable |

8.5.54 EDP_CORE_SPDIF_NCTS_STABLE_P Register (Offset = A20h) [reset = 0h]

EDP_CORE_SPDIF_NCTS_STABLE_P is shown in [Figure 8-110](#) and described in [Table 8-230](#).

Return to [Summary Table](#).

SPDIF clock stable, lane clock measured

**Table 8-229. EDP_CORE_SPDIF_NCTS_STABLE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A20h |

Figure 8-110. EDP_CORE_SPDIF_NCTS_STABLE_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SPDIF_NCTS_ STABLE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-230. EDP_CORE_SPDIF_NCTS_STABLE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | SPDIF_NCTS_STABLE | R | 0h | SPDIF CTS measurement stable |

8.5.55 EDP_CORE_NMVID_MEAS_STABLE_P Register (Offset = A24h) [reset = 0h]

EDP_CORE_NMVID_MEAS_STABLE_P is shown in [Figure 8-111](#) and described in [Table 8-232](#).

[Return to Summary Table.](#)

Video clock stable

Table 8-231. EDP_CORE_NMVID_MEAS_STABLE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A24h |

Figure 8-111. EDP_CORE_NMVID_MEAS_STABLE_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ST_NMVID_MEAS_STABLE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-232. EDP_CORE_NMVID_MEAS_STABLE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | ST_NMVID_MEAS_STABLE | R | 0h | Pixel clock NMVID measurement stable |

8.5.56 EDP_CORE_CM_VID_MEAS_P Register (Offset = A28h) [reset = 0h]

EDP_CORE_CM_VID_MEAS_P is shown in [Figure 8-112](#) and described in [Table 8-234](#).

Return to [Summary Table](#).

Video cycles measure

**Table 8-233. EDP_CORE_CM_VID_MEAS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A28h |

Figure 8-112. EDP_CORE_CM_VID_MEAS_P Register

| | | | | | | | |
|----------------|----|----|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | NMVID_MEAS_VALID_INDC |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NMVID_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NMVID_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NMVID_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-234. EDP_CORE_CM_VID_MEAS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 24 | NMVID_MEAS_VALID_INDC | R/W | 0h | When Toggle Valid pulse is generated to sample MNVID fix value |
| 23-0 | NMVID_MEAS_CYC | R/W | 0h | Fixed Value for NVID , The MVID is nmvid_ref_cyc [23:0] |

8.5.57 EDP_CORE_CM_AUD_MEAS_P Register (Offset = A2Ch) [reset = 0h]

EDP_CORE_CM_AUD_MEAS_P is shown in [Figure 8-113](#) and described in [Table 8-236](#).

Return to [Summary Table](#).

Audio cycles measure

Table 8-235. EDP_CORE_CM_AUD_MEAS_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A2Ch |

Figure 8-113. EDP_CORE_CM_AUD_MEAS_P Register

| | | | | | | | |
|----------------|----|----|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | NMAUD_MEAS_VALID_INDC |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NMAUD_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NMAUD_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NMAUD_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-236. EDP_CORE_CM_AUD_MEAS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 24 | NMAUD_MEAS_VALID_INDC | R/W | 0h | When Toggle Valid pulse is generated to sample MNAUD fix value |
| 23-0 | NMAUD_MEAS_CYC | R/W | 0h | Fixed Value for NAUD, The MAUD is lane_ref_cyc [23:0] |

8.5.58 EDP_CORE_I2S_MEAS_P Register (Offset = A30h) [reset = 0h]

EDP_CORE_I2S_MEAS_P is shown in [Figure 8-114](#) and described in [Table 8-238](#).

Return to [Summary Table](#).

I2S clock measurement HDMI

Table 8-237. EDP_CORE_I2S_MEAS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A30h |

Figure 8-114. EDP_CORE_I2S_MEAS_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | I2_MEAS | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-238. EDP_CORE_I2S_MEAS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | I2_MEAS | R | 0h | I2S measurement value |

8.5.59 EDP_CORE_SPDIF_MEAS_P Register (Offset = A34h) [reset = 0h]

EDP_CORE_SPDIF_MEAS_P is shown in [Figure 8-115](#) and described in [Table 8-240](#).

Return to [Summary Table](#).

SPDIF clock measurement HDMI

Table 8-239. EDP_CORE_SPDIF_MEAS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A34h |

Figure 8-115. EDP_CORE_SPDIF_MEAS_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SPDIF_MEAS | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-240. EDP_CORE_SPDIF_MEAS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | SPDIF_MEAS | R | 0h | SPDIF Clock Meter measurement value [in DP] |

8.5.60 EDP_CORE_NMVID_MEAS_P Register (Offset = A38h) [reset = 0h]

EDP_CORE_NMVID_MEAS_P is shown in [Figure 8-116](#) and described in [Table 8-242](#).

Return to [Summary Table](#).

Video clock measurement

Table 8-241. EDP_CORE_NMVID_MEAS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A38h |

Figure 8-116. EDP_CORE_NMVID_MEAS_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | NMVID_MEAS | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-242. EDP_CORE_NMVID_MEAS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | NMVID_MEAS | R | 0h | Video clock measurement value |

8.5.61 EDP_CORE_CM_CTRL_P_j Register (Offset = A40h + formula) [reset = 0h]

EDP_CORE_CM_CTRL_P_j is shown in [Figure 8-117](#) and described in [Table 8-244](#).

Return to [Summary Table](#).

Clock Meter control

Offset = A40h + (j * 40h); where j = 0h to 2h

Table 8-243. EDP_CORE_CM_CTRL_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A40h + formula |

Figure 8-117. EDP_CORE_CM_CTRL_P_j Register

| | | | | | | | |
|----------|----------|----|----|-----------------------|----------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | I2S_MULT | | | SEL_AUD_LANE E_REF | I2S_SEL_EXT ERNAL | SPDIF_SEL_E XTERNAL | NMVID_SEL_E XTERNAL |
| R-0h | R/W-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-244. EDP_CORE_CM_CTRL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6-4 | I2S_MULT | R/W | 0h | Select the division of N value for different I2S TDM configuration |
| 3 | SEL_AUD_LANE_REF | R/W | 0h | When 1 Select Audio CLK as a reference [HDMI] When 0 Select LANE CLK as a reference [DP] |
| 2 | I2S_SEL_EXTERNAL | R/W | 0h | When 1 Select external values of NMAUD [N/A] for I2S |
| 1 | SPDIF_SEL_EXTERNAL | R/W | 0h | When 1 Select external values of NMAUD [N/A] for SPDIF |
| 0 | NMVID_SEL_EXTERNAL | R/W | 0h | When 1 Select external values of NMVID [N/A] |

8.5.62 EDP_CORE_CM_VID_CTRL_P_j Register (Offset = A4Ch + formula) [reset = 04008000h]

EDP_CORE_CM_VID_CTRL_P_j is shown in [Figure 8-118](#) and described in [Table 8-246](#).

Return to [Summary Table](#).

Video clock control

Offset = A4Ch + (j * 40h); where j = 0h to 2h

**Table 8-245. EDP_CORE_CM_VID_CTRL_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A4Ch + formula |

Figure 8-118. EDP_CORE_CM_VID_CTRL_P_j Register

| | | | | | | | |
|---------------|----|----|----|----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | NMVID_MEAS_TOLERANCE | | | |
| R-0h | | | | R/W-4h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NMVID_REF_CYC | | | | | | | |
| R/W-8000h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NMVID_REF_CYC | | | | | | | |
| R/W-8000h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NMVID_REF_CYC | | | | | | | |
| R/W-8000h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-246. EDP_CORE_CM_VID_CTRL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 27-24 | NMVID_MEAS_TOLERANCE | R/W | 4h | Video measurement tolerance in pixel clock cycles |
| 23-0 | NMVID_REF_CYC | R/W | 8000h | Video Reference cycles |

8.5.63 EDP_CORE_NMVID_MEAS_STABLE_P_J Register (Offset = A64h + formula) [reset = 0h]

EDP_CORE_NMVID_MEAS_STABLE_P_J is shown in [Figure 8-119](#) and described in [Table 8-248](#).

Return to [Summary Table](#).

Video clock stable

Offset = A64h + (j * 40h); where j = 0h to 2h

Table 8-247.
EDP_CORE_NMVID_MEAS_STABLE_P_J Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A64h + formula |

Figure 8-119. EDP_CORE_NMVID_MEAS_STABLE_P_J Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ST_NMVID_MEAS_STABLE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-248. EDP_CORE_NMVID_MEAS_STABLE_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | ST_NMVID_MEAS_STABLE | R | 0h | Pixel clock NMVID measurement stable |

8.5.64 EDP_CORE_CM_VID_MEAS_P_J Register (Offset = A68h + formula) [reset = 0h]

EDP_CORE_CM_VID_MEAS_P_J is shown in [Figure 8-120](#) and described in [Table 8-250](#).

Return to [Summary Table](#).

Video cycles measure

Offset = A68h + (j * 40h); where j = 0h to 2h

**Table 8-249. EDP_CORE_CM_VID_MEAS_P_J
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A68h + formula |

Figure 8-120. EDP_CORE_CM_VID_MEAS_P_J Register

| | | | | | | | |
|----------------|----|----|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | NMVID_MEAS_VALID_INDC |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NMVID_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NMVID_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NMVID_MEAS_CYC | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-250. EDP_CORE_CM_VID_MEAS_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 24 | NMVID_MEAS_VALID_INDC | R/W | 0h | When Toggle Valid pulse is generated to sample MNVID fix value |
| 23-0 | NMVID_MEAS_CYC | R/W | 0h | Fixed Value for NVID , The MVID is nmvid_ref_cyc [23:0] |

8.5.65 EDP_CORE_NMVID_MEAS_P_J Register (Offset = A78h + formula) [reset = 0h]

EDP_CORE_NMVID_MEAS_P_J is shown in [Figure 8-121](#) and described in [Table 8-252](#).

Return to [Summary Table](#).

Video clock measurement

Offset = A78h + (j * 40h); where j = 0h to 2h

Table 8-251. EDP_CORE_NMVID_MEAS_P_J Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0A78h + formula |

Figure 8-121. EDP_CORE_NMVID_MEAS_P_J Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | NMVID_MEAS | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-252. EDP_CORE_NMVID_MEAS_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | NMVID_MEAS | R | 0h | Video clock measurement value |

8.5.66 EDP_CORE_BND_HSYNC2VSYNC_P_j Register (Offset = B00h + formula) [reset = 2000h]

EDP_CORE_BND_HSYNC2VSYNC_P_j is shown in [Figure 8-122](#) and described in [Table 8-254](#).

Return to [Summary Table](#).

Video Input Interface Setting Register

Offset = B00h + (j * 20h); where j = 0h to 3h

Table 8-253. EDP_CORE_BND_HSYNC2VSYNC_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0B00h + formula |

Figure 8-122. EDP_CORE_BND_HSYNC2VSYNC_P_j Register

| | | | | | | | |
|-------------|----------------------|-------------------|-----------|-------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | IP_VIF_ALIGN MENT | IP_VIF_BYPAS S | IP_DET_EN | IP_DTCT_WIN | | | |
| R-0h | R/W-0h | R/W-1h | R/W-0h | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IP_DTCT_WIN | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-254. EDP_CORE_BND_HSYNC2VSYNC_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-15 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 14 | IP_VIF_ALIGNMENT | R/W | 0h | Alignment of the input pixel data at the pixel interface: 0-MSB alignment 1-LSB alignment. |
| 13 | IP_VIF_BYPASS | R/W | 1h | Bypass video interface. |
| 12 | IP_DET_EN | R/W | 0h | Enable detection of Interlace formats after decided if the polarity is Automatic or Manual detection. |
| 11-0 | IP_DTCT_WIN | R/W | 0h | Bound for HSYNC to VSYNC for all fields. |

8.5.67 EDP_CORE_HSYNC2VSYNC_F1_L1_P_J Register (Offset = B04h + formula) [reset = 0h]

EDP_CORE_HSYNC2VSYNC_F1_L1_P_J is shown in [Figure 8-123](#) and described in [Table 8-256](#).

Return to [Summary Table](#).

Status of HSYNC to VSYNC Distance Counter 1.

Offset = B04h + (j * 20h); where j = 0h to 3h

Table 8-255.
EDP_CORE_HSYNC2VSYNC_F1_L1_P_J Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0B04h + formula |

Figure 8-123. EDP_CORE_HSYNC2VSYNC_F1_L1_P_J Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IP_DTCT_HSYNC2VSYNC_F1 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-256. EDP_CORE_HSYNC2VSYNC_F1_L1_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | IP_DTCT_HSYNC2VSYN C_F1 | R | 0h | Value of HSYNC to VSYNC field 1. |

8.5.68 EDP_CORE_HSYNC2VSYNC_F2_L1_P_J Register (Offset = B08h + formula) [reset = 0h]

EDP_CORE_HSYNC2VSYNC_F2_L1_P_J is shown in [Figure 8-124](#) and described in [Table 8-258](#).

Return to [Summary Table](#).

Status of HSYNC to VSYNC Distance Counter 2

Offset = B08h + (j * 20h); where j = 0h to 3h

Table 8-257.

EDP_CORE_HSYNC2VSYNC_F2_L1_P_J Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0B08h + formula |

Figure 8-124. EDP_CORE_HSYNC2VSYNC_F2_L1_P_J Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IP_DTCT_HSYNC2VSYNC_F2 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-258. EDP_CORE_HSYNC2VSYNC_F2_L1_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | IP_DTCT_HSYNC2VSYN C_F2 | R | 0h | Value of HSYNC to VSYNC field 2. |

8.5.69 EDP_CORE_HSYNC2VSYNC_STATUS_P_j Register (Offset = B0Ch + formula) [reset = 0h]

EDP_CORE_HSYNC2VSYNC_STATUS_P_j is shown in [Figure 8-125](#) and described in [Table 8-260](#).

Return to [Summary Table](#).

Video Interface Status Register

Offset = B0Ch + (j * 20h); where j = 0h to 3h

Table 8-259.
EDP_CORE_HSYNC2VSYNC_STATUS_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0B0Ch + formula |

Figure 8-125. EDP_CORE_HSYNC2VSYNC_STATUS_P_j Register

| | | | | | | | |
|----------|----|----|----|---------------------|---------------------|-----------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | IP_DTCT_HJIT TER | IP_DTCT_VJIT TER | IP_DCT_IP | IP_DTCT_ERR |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-260. EDP_CORE_HSYNC2VSYNC_STATUS_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | IP_DTCT_HJITTER | R | 0h | Asserted when jitter is observed on htotal i.e. HSYNC rising edge to next HSYNC rising edge delay count. Clear on Read. |
| 2 | IP_DTCT_VJITTER | R | 0h | Asserted when jitter is observed on vtotal i.e. VSYNC rising edge to next VSYNC rising edge delay count. Clear on Read. |
| 1 | IP_DCT_IP | R | 0h | When asserted interlaced format is detected else progressive format. |
| 0 | IP_DTCT_ERR | R | 0h | Asserted when HSYNC to VSYNC bound is violated. Clear on Read. |

8.5.70 EDP_CORE_HSYNC2VSYNC_POL_CTRL_P_j Register (Offset = B10h + formula) [reset = 0h]

EDP_CORE_HSYNC2VSYNC_POL_CTRL_P_j is shown in [Figure 8-126](#) and described in [Table 8-262](#).

Return to [Summary Table](#).

Setting Polarity of HSYNC and VSYNC

Offset = B10h + (j * 20h); where j = 0h to 3h

Table 8-261.
EDP_CORE_HSYNC2VSYNC_POL_CTRL_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0B10h + formula |

Figure 8-126. EDP_CORE_HSYNC2VSYNC_POL_CTRL_P_j Register

| | | | | | | | |
|----------|----|----|----|----|--------|--------|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | VPOL | HPOL | VIF_AUTO_MODE |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-262. EDP_CORE_HSYNC2VSYNC_POL_CTRL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 2 | VPOL | R/W | 0h | VSYNC polarity: 0-active HIGH 1-active LOW. |
| 1 | HPOL | R/W | 0h | HSYNC polarity: 0-active HIGH 1-active LOW. |
| 0 | VIF_AUTO_MODE | R/W | 0h | Automatic or Manual configuration of the polarity: 0-vpol and hpol settings are used 1-automatic detection of polarity of input VSYNC and HSYNC |

8.5.71 EDP_CORE_DSC_CTRL_P_j Register (Offset = B14h + formula) [reset = 0h]

EDP_CORE_DSC_CTRL_P_j is shown in [Figure 8-127](#) and described in [Table 8-264](#).

Return to [Summary Table](#).

DSC Setting Register

Offset = B14h + (j * 20h); where j = 0h to 3h

Table 8-263. EDP_CORE_DSC_CTRL_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 0B14h + formula |

Figure 8-127. EDP_CORE_DSC_CTRL_P_j Register

| | | | | | | | |
|----------|----|----|----|----|--------------------|------------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | DSC_REG_UP DATE | DSC_SW_RST | DSC_EN |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-264. EDP_CORE_DSC_CTRL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 2 | DSC_REG_UPDATE | R/W | 0h | DSC registers update: active HIGH. |
| 1 | DSC_SW_RST | R/W | 0h | DSC software reset: active HIGH. |
| 0 | DSC_EN | R/W | 0h | DSC enable bit: 1-DSC is enabled 0-DSC is disabled |

8.5.72 EDP_CORE_DP_TX_PHY_CONFIG_REG_P Register (Offset = 2000h) [reset = 0h]

EDP_CORE_DP_TX_PHY_CONFIG_REG_P is shown in [Figure 8-128](#) and described in [Table 8-266](#).

Return to [Summary Table](#).

DPTX PHY control

Table 8-265.
EDP_CORE_DP_TX_PHY_CONFIG_REG_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2000h |

Figure 8-128. EDP_CORE_DP_TX_PHY_CONFIG_REG_P Register

| | | | | | | | |
|---------------------------|----------------------------------|------------------------------------|-------------------------|----|----------------------|--------------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | DP_TX_PHY_1 0BIT_ENABLE | DP_TX_PHY_LANE3_SKEW | | DP_TX_PHY_LANE2_SKEW | | |
| R-0h | | R/W-0h | R/W-0h | | R/W-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DP_TX_PHY_L ANE2_SKEW | DP_TX_PHY_LANE1_SKEW | | DP_TX_PHY_LANE0_SKEW | | | DP_TX_PHY_T RAINING_AUT OMATIC | |
| R/W-0h | R/W-0h | | R/W-0h | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP_TX_PHY_S KEW_BYPASS | DP_TX_PHY_E NCODER_BYP ASS | DP_TX_PHY_S CRAMBLER_B YPASS | DP_TX_PHY_TRAINING_TYPE | | | DP_TX_PHY_T RAINING_ENA BLE | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-266. EDP_CORE_DP_TX_PHY_CONFIG_REG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-22 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 21 | DP_TX_PHY_10BIT_ENA BLE | R/W | 0h | Used to enable the 10-bit mode. Active high. |
| 20-18 | DP_TX_PHY_LANE3_SK EW | R/W | 0h | Specifies the programmable lane3 skew. |
| 17-15 | DP_TX_PHY_LANE2_SK EW | R/W | 0h | Specifies the programmable lane2 skew. |
| 14-12 | DP_TX_PHY_LANE1_SK EW | R/W | 0h | Specifies the programmable lane1 skew. |
| 11-9 | DP_TX_PHY_LANE0_SK EW | R/W | 0h | Specifies the programmable lane0 skew. |

Table 8-266. EDP_CORE_DP_TX_PHY_CONFIG_REG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|---|
| 8 | DP_TX_PHY_TRAINING_AUTOMATIC | R/W | 0h | When set, the dp_tx_phy_scrambler_bypass and the dp_tx_phy_encoder_bypass bits are ignored during training pattern generation. This is a debug feature. |
| 7 | DP_TX_PHY_SKEW_BYPASS | R/W | 0h | Used to bypass the lane skew. Active high. This is a debug feature. |
| 6 | DP_TX_PHY_ENCODER_BYPASS | R/W | 0h | Used to bypass the encoder. Active high. This is a debug feature. |
| 5 | DP_TX_PHY_SCRAMBLER_BYPASS | R/W | 0h | Used to bypass the scrambler. Active high. This is a debug feature. |
| 4-1 | DP_TX_PHY_TRAINING_TYPE | R/W | 0h | Specifies the training pattern type used as follows: 0000 PRBS7 0001 TPS1 0010 TPS2 0011 TPS3 0100 TPS4 0101 custom 80-bit pattern 0110 D10.2 training pattern 0111 Symbol Error Rate Measurement pattern 1000 CP2520 pattern1 1001 CP2520 pattern2 1010 CP2520 pattern3 others reserved |
| 0 | DP_TX_PHY_TRAINING_ENABLE | R/W | 0h | Enables the training sequence [when set to 1]. |

8.5.73 EDP_CORE_DP_TX_PHY_SW_RESET_P Register (Offset = 2004h) [reset = 0h]

EDP_CORE_DP_TX_PHY_SW_RESET_P is shown in [Figure 8-129](#) and described in [Table 8-268](#).

Return to [Summary Table](#).

DPTC PHY software reset

Table 8-267.
EDP_CORE_DP_TX_PHY_SW_RESET_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2004h |

Figure 8-129. EDP_CORE_DP_TX_PHY_SW_RESET_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | DP_TX_PHY_S W_RST |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-268. EDP_CORE_DP_TX_PHY_SW_RESET_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | DP_TX_PHY_SW_RST | R/W | 0h | Software reset. Active high. |

8.5.74 EDP_CORE_DP_TX_PHY_SCRAMBLER_SEED_P Register (Offset = 2008h) [reset = FFFFh]

EDP_CORE_DP_TX_PHY_SCRAMBLER_SEED_P is shown in [Figure 8-130](#) and described in [Table 8-270](#).

Return to [Summary Table](#).

Scrambler seed

Table 8-269.
EDP_CORE_DP_TX_PHY_SCRAMBLER_SEED_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2008h |

Figure 8-130. EDP_CORE_DP_TX_PHY_SCRAMBLER_SEED_P Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP_TX_PHY_SCRAMBLER_SEED | | | | | | | | | | | | | | | |
| R/W-FFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-270. EDP_CORE_DP_TX_PHY_SCRAMBLER_SEED_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | DP_TX_PHY_SCRAMBLE R_SEED | R/W | FFFFh | Scrambler seed range 0-0xFFFF |

8.5.75 EDP_CORE_DP_TX_PHY_TRAINING_01_04_P Register (Offset = 200Ch) [reset = 0h]

EDP_CORE_DP_TX_PHY_TRAINING_01_04_P is shown in [Figure 8-131](#) and described in [Table 8-272](#).

Return to [Summary Table](#).

Custom training value bytes 1-4

Table 8-271.
EDP_CORE_DP_TX_PHY_TRAINING_01_04_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 200Ch |

Figure 8-131. EDP_CORE_DP_TX_PHY_TRAINING_01_04_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|-----------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DP_TX_PHY_TRAINING_04 | | | | | | | | DP_TX_PHY_TRAINING_03 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP_TX_PHY_TRAINING_02 | | | | | | | | DP_TX_PHY_TRAINING_01 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-272. EDP_CORE_DP_TX_PHY_TRAINING_01_04_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-24 | DP_TX_PHY_TRAINING_04 | R/W | 0h | Byte 4 of the 80-bit custom training data. |
| 23-16 | DP_TX_PHY_TRAINING_03 | R/W | 0h | Byte 3 of the 80-bit custom training data. |
| 15-8 | DP_TX_PHY_TRAINING_02 | R/W | 0h | Byte 2 of the 80-bit custom training data. |
| 7-0 | DP_TX_PHY_TRAINING_01 | R/W | 0h | Byte 1 of the 80-bit custom training data. |

8.5.76 EDP_CORE_DP_TX_PHY_TRAINING_05_08_P Register (Offset = 2010h) [reset = 0h]

EDP_CORE_DP_TX_PHY_TRAINING_05_08_P is shown in [Figure 8-132](#) and described in [Table 8-274](#).

Return to [Summary Table](#).

Custom training value bytes 5-8

Table 8-273.
EDP_CORE_DP_TX_PHY_TRAINING_05_08_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2010h |

Figure 8-132. EDP_CORE_DP_TX_PHY_TRAINING_05_08_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|-----------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DP_TX_PHY_TRAINING_08 | | | | | | | | DP_TX_PHY_TRAINING_07 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP_TX_PHY_TRAINING_06 | | | | | | | | DP_TX_PHY_TRAINING_05 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-274. EDP_CORE_DP_TX_PHY_TRAINING_05_08_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-24 | DP_TX_PHY_TRAINING_08 | R/W | 0h | Byte 8 of the 80-bit custom training data. |
| 23-16 | DP_TX_PHY_TRAINING_07 | R/W | 0h | Byte 7 of the 80-bit custom training data. |
| 15-8 | DP_TX_PHY_TRAINING_06 | R/W | 0h | Byte 6 of the 80-bit custom training data. |
| 7-0 | DP_TX_PHY_TRAINING_05 | R/W | 0h | Byte 5 of the 80-bit custom training data. |

8.5.77 EDP_CORE_DP_TX_PHY_TRAINING_09_10_P Register (Offset = 2014h) [reset = 0h]

EDP_CORE_DP_TX_PHY_TRAINING_09_10_P is shown in [Figure 8-133](#) and described in [Table 8-276](#).

Return to [Summary Table](#).

Custom training value bytes 9-10

Table 8-275.
EDP_CORE_DP_TX_PHY_TRAINING_09_10_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2014h |

Figure 8-133. EDP_CORE_DP_TX_PHY_TRAINING_09_10_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|-----------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP_TX_PHY_TRAINING_10 | | | | | | | | DP_TX_PHY_TRAINING_09 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-276. EDP_CORE_DP_TX_PHY_TRAINING_09_10_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-8 | DP_TX_PHY_TRAINING_10 | R/W | 0h | Byte 10 of the 80-bit custom training data. |
| 7-0 | DP_TX_PHY_TRAINING_09 | R/W | 0h | Byte 9 of the 80-bit custom training data. |

8.5.78 EDP_CORE_DP_TX_PHY_SR_INTERVAL_P Register (Offset = 2018h) [reset = FCh]

EDP_CORE_DP_TX_PHY_SR_INTERVAL_P is shown in [Figure 8-134](#) and described in [Table 8-278](#).

Return to [Summary Table](#).

Custom CP2520 SR interval

Table 8-277.
EDP_CORE_DP_TX_PHY_SR_INTERVAL_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2018h |

Figure 8-134. EDP_CORE_DP_TX_PHY_SR_INTERVAL_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DP_TX_PHY_SR_INTERVAL | | | | | | | | | | | | | | | |
| R/W-FCh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-278. EDP_CORE_DP_TX_PHY_SR_INTERVAL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | DP_TX_PHY_SR_INTER VAL | R/W | FCh | CP2520 test pattern SR Interval definition |

8.5.79 EDP_CORE_DP_TX_PHY_FEC_TEST_P Register (Offset = 201Ch) [reset = 0h]

EDP_CORE_DP_TX_PHY_FEC_TEST_P is shown in [Figure 8-135](#) and described in [Table 8-280](#).

Return to [Summary Table](#).

FEC IP test register. Used for fault injection into the FEC IP to test diagnostic mechanisms.

Table 8-279. EDP_CORE_DP_TX_PHY_FEC_TEST_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 201Ch |

Figure 8-135. EDP_CORE_DP_TX_PHY_FEC_TEST_P Register

| | | | | | | | |
|------------------------|-----------------------------|-----------------------------|----------------------------------|------------------------|-----------------------------|----------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | FEC_L23_EXT _DIAG_TEST_ EN | FEC_L01_EXT _DIAG_TEST_ EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FEC_L23_8B10 B_TEST | FEC_L23_PARI TY_ENC_TEST | FEC_L23_PARI TY_GEN_TEST | FEC_L23_DAT A_BYPASS_TE ST | FEC_L01_8B10 B_TEST | FEC_L01_PARI TY_ENC_TEST | FEC_L01_PARI TY_GEN_TEST | FEC_L01_DAT A_BYPASS_TE ST |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-280. EDP_CORE_DP_TX_PHY_FEC_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9 | FEC_L23_EXT_DIAG_TE ST_EN | R/W | 0h | Encoder 1 external diagnostic test enable. When asserted, a corruption is injected in the external diagnostic reference module which generate an external diagnostic support module fault. To perform external diagnostic test this bit must be set first and then one of the bits 7-4 must be set. Both must be a separate writes. NOTE: This bit cannot be set when bypass, encoder, decoder or 8b10b tests are performed. |

Table 8-280. EDP_CORE_DP_TX_PHY_FEC_TEST_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|--|
| 8 | FEC_L01_EXT_DIAG_TEST_EN | R/W | 0h | Encoder 0 external diagnostic test enable. When asserted, a corruption is injected in the external diagnostic reference module which generate an external diagnostic support module fault. To perform external diagnostic test this bit must be set first and then one of the bits 3-0 must be set. Both must be a separate writes. NOTE: This bit cannot be set when bypass, encoder, decoder or 8b10b tests are performed. |
| 7 | FEC_L23_8B10B_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the 8b10b check of the FEC IP datapath for lanes 2 and 3. Bit is self cleared. |
| 6 | FEC_L23_PARITY_ENC_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the parity enc check of the FEC IP datapath for lanes 2 and 3. Bit is self cleared. |
| 5 | FEC_L23_PARITY_GEN_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the parity gen check of the FEC IP datapaths for lanes 2 and 3. Bit is self cleared. |
| 4 | FEC_L23_DATA_BYPASS_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the bypass check for of the FEC IP datapath for lanes 2 and 3. Bit is self cleared. |
| 3 | FEC_L01_8B10B_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the 8b10b check of the FEC IP datapath for lanes 0 and 1. Bit is self cleared. |
| 2 | FEC_L01_PARITY_ENC_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the parity enc check of the FEC IP datapath for lanes 0 and 1. Bit is self cleared. |
| 1 | FEC_L01_PARITY_GEN_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the parity gen check of the FEC IP datapath for lanes 0 and 1. Bit is self cleared. |
| 0 | FEC_L01_DATA_BYPASS_TEST | R/W | 0h | When asserted, a corruption is injected at the interface of the internal diagnostic module which generate a fault in the bypass check for of the FEC IP datapath for lanes 0 and 1. Bit is self cleared. |

8.5.80 EDP_CORE_HPD_IRQ_DET_MIN_TIMER_P Register (Offset = 2100h) [reset = C350h]

EDP_CORE_HPD_IRQ_DET_MIN_TIMER_P is shown in [Figure 8-136](#) and described in [Table 8-282](#).

Return to [Summary Table](#).

HPD min timer for irq, define the minimum pclk cycles that the HPD pulse will be considered as IRQ

Table 8-281.
EDP_CORE_HPD_IRQ_DET_MIN_TIMER_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2100h |

Figure 8-136. EDP_CORE_HPD_IRQ_DET_MIN_TIMER_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | HPD_IRQ_DET_MIN_TIMER | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-C350h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-282. EDP_CORE_HPD_IRQ_DET_MIN_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | HPD_IRQ_DET_MIN_TIMER | R/W | C350h | HPD min timer for interrupt. |

8.5.81 EDP_CORE_HPD_IRQ_DET_MAX_TIMER_P Register (Offset = 2104h) [reset = 000186A0h]

EDP_CORE_HPD_IRQ_DET_MAX_TIMER_P is shown in [Figure 8-137](#) and described in [Table 8-284](#).

Return to [Summary Table](#).

HPD max timer for irq, define the maximum pclk cycles that the HPD pulse will be considered as IRQ

Table 8-283.
EDP_CORE_HPD_IRQ_DET_MAX_TIMER_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2104h |

Figure 8-137. EDP_CORE_HPD_IRQ_DET_MAX_TIMER_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | HPD_IRQ_DET_MAX_TIMER | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-000186A0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-284. EDP_CORE_HPD_IRQ_DET_MAX_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-----------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | HPD_IRQ_DET_MAX_TIMER | R/W | 000186A0h | HPD max timer |

8.5.82 EDP_CORE_HPD_UNPLGED_DET_MIN_TIMER_P Register (Offset = 2108h) [reset = 00030D40h]

EDP_CORE_HPD_UNPLGED_DET_MIN_TIMER_P is shown in [Figure 8-138](#) and described in [Table 8-286](#).

Return to [Summary Table](#).

HPD min timer for HPD detect, define the minimum pclk cycles that the HPD is low

Table 8-285.
EDP_CORE_HPD_UNPLGED_DET_MIN_TIMER_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2108h |

Figure 8-138. EDP_CORE_HPD_UNPLGED_DET_MIN_TIMER_P Register

| | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|---------------------------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | HPD_UNPLGED_DET_MIN_TIMER | | | | | | |
| R-0h | | | | | | | | | R/W-00030D40h | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HPD_UNPLGED_DET_MIN_TIMER | | | | | | | | | | | | | | | |
| R/W-00030D40h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-286. EDP_CORE_HPD_UNPLGED_DET_MIN_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-----------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | HPD_UNPLGED_DET_MIN_TIMER | R/W | 00030D40h | HPD unplugged timer |

8.5.83 EDP_CORE_HPD_STABLE_TIMER_P Register (Offset = 210Ch) [reset = 000186A0h]

EDP_CORE_HPD_STABLE_TIMER_P is shown in [Figure 8-139](#) and described in [Table 8-288](#).

Return to [Summary Table](#).

Timer for detecting HPD stable, count in system clock cycles.

Table 8-287. EDP_CORE_HPD_STABLE_TIMER_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 210Ch |

Figure 8-139. EDP_CORE_HPD_STABLE_TIMER_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | HPD_STABLE_TIMER | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-000186A0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-288. EDP_CORE_HPD_STABLE_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-----------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | HPD_STABLE_TIMER | R/W | 000186A0h | HPD stable timer counter setup. |

8.5.84 EDP_CORE_HPD_FILTER_TIMER_P Register (Offset = 2110h) [reset = 7A12h]

EDP_CORE_HPD_FILTER_TIMER_P is shown in [Figure 8-140](#) and described in [Table 8-290](#).

Return to [Summary Table](#).

Timer for filtering small pulses on HPD input.

**Table 8-289. EDP_CORE_HPD_FILTER_TIMER_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2110h |

Figure 8-140. EDP_CORE_HPD_FILTER_TIMER_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | HPD_FILTER_TIMER | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-7A12h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-290. EDP_CORE_HPD_FILTER_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 23-0 | HPD_FILTER_TIMER | R/W | 7A12h | HPD glitch filter counter setup. |

8.5.85 EDP_CORE_HPD_DBNC_TIMER_P Register (Offset = 2114h) [reset = 0h]

EDP_CORE_HPD_DBNC_TIMER_P is shown in [Figure 8-141](#) and described in [Table 8-292](#).

Return to [Summary Table](#).

HPD debouncer control

Table 8-291. EDP_CORE_HPD_DBNC_TIMER_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2114h |

Figure 8-141. EDP_CORE_HPD_DBNC_TIMER_P Register

| | | | | | | | |
|--------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | SEL_HPDTX_D B_22 |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HPD_DEBOUNCE_TIMER | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| HPD_DEBOUNCE_TIMER | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HPD_DEBOUNCE_TIMER | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-292. EDP_CORE_HPD_DBNC_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 24 | SEL_HPDTX_DB_22 | R/W | 0h | Debouncer enable 0 - debouncer disabled 1 - debouncer enabled |
| 23-0 | HPD_DEBOUNCE_TIMER | R/W | 0h | HPD debounce timer setup. |

8.5.86 EDP_CORE_HPD_EVENT_MASK_P Register (Offset = 211Ch) [reset = 0h]

EDP_CORE_HPD_EVENT_MASK_P is shown in [Figure 8-142](#) and described in [Table 8-294](#).

Return to [Summary Table](#).

Mask of HPD interrupt and status

**Table 8-293. EDP_CORE_HPD_EVENT_MASK_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 211Ch |

Figure 8-142. EDP_CORE_HPD_EVENT_MASK_P Register

| | | | | | | | |
|----------|----|----|----|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | HPD_EVENTS_MASK | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-294. EDP_CORE_HPD_EVENT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3-0 | HPD_EVENTS_MASK | R/W | 0h | HPD mask events |

8.5.87 EDP_CORE_HPDP_EVENT_DET_P Register (Offset = 2120h) [reset = 4h]

EDP_CORE_HPDP_EVENT_DET_P is shown in [Figure 8-143](#) and described in [Table 8-296](#).

Return to [Summary Table](#).

HPD interrupt and status

Table 8-295. EDP_CORE_HPDP_EVENT_DET_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2120h |

Figure 8-143. EDP_CORE_HPDP_EVENT_DET_P Register

| | | | | | | | |
|----------|----|----|-------------|--------------------------------|--------------------------------|------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | HPD_IN_SYNC | HPD_RE_PLG ED_DET_EVEN T | HPD_UNPLUG GED_DET_ACL K | HPD_STABLE | HPD_IRQ_DET _EVENT |
| R-0h | | | R-0h | R-0h | R-1h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-296. EDP_CORE_HPDP_EVENT_DET_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 4 | HPD_IN_SYNC | R | 0h | HDP in sync detected |
| 3 | HPD_RE_PLGED_DET_E VENT | R | 0h | HPD Re-Plugged event detected. |
| 2 | HPD_UNPLUGGED_DET _ACLK | R | 1h | HPD Un-Plugged event detected. |
| 1 | HPD_STABLE | R | 0h | HPD Stable indication |
| 0 | HPD_IRQ_DET_EVENT | R | 0h | Bit 0 - HPD irq event |

8.5.88 EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P Register (Offset = 2200h) [reset = 63h]

EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P is shown in [Figure 8-144](#) and described in [Table 8-298](#).

Return to [Summary Table](#).

Global configuration of the framer module.

Table 8-297.
EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2200h |

Figure 8-144. EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P Register

| | | | | | | | |
|----------------|-------------|----------|----------|-----------|---------|-----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WR_VHSYNC_FALL | ENC_RST_DIS | NO_VIDEO | RESERVED | GLOBAL_EN | MST_SST | NUM_LANES | |
| R/W-0h | R/W-1h | R/W-1h | R-0h | R/W-0h | R/W-0h | R/W-3h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-298. EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 7 | WR_VHSYNC_FALL | R/W | 0h | When set to 1 change the write state machine to sync on falling edge of vsync. Used only for debug purpose. |
| 6 | ENC_RST_DIS | R/W | 1h | Unused. Kept RW for software backward compatibility. |
| 5 | NO_VIDEO | R/W | 1h | No-video mode configuration bit. Relevant only in SST mode. When this bit is set high and framer is enabled then IP operates in no-video mode i.e. BS symbol is generated every 8192 link symbols. In this mode audio data can be transmitted. |
| 4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |

Table 8-298. EDP_CORE_DP_FRAMER_GLOBAL_CONFIG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 3 | GLOBAL_EN | R/W | 0h | Global enable for complete Framer module, active high. It is deasserted during configuration phase. Once configuration is finished, it is asserted. |
| 2 | MST_SST | R/W | 0h | Mode select: 0 - SST mode 1 - MST mode Static configuration bit that must be set before link training. |
| 1-0 | NUM_LANES | R/W | 3h | Number of lanes: 0h - One lane [Lane 0 only] 1h - Two lanes [Lanes 0 and 1 only] 2h - Reserved 3h - Four lanes [Lanes 0, 1, 2, and 3]. This value can only be changed before link training and further it can be modified during link training in case link training for a given lane configuration fails. This field must not be changed after link training. |

8.5.89 EDP_CORE_DP_SW_RESET_P Register (Offset = 2204h) [reset = 0h]

EDP_CORE_DP_SW_RESET_P is shown in [Figure 8-145](#) and described in [Table 8-300](#).

Return to [Summary Table](#).

Unused. Bit [0] kept RW for software backward compatibility.

**Table 8-299. EDP_CORE_DP_SW_RESET_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2204h |

Figure 8-145. EDP_CORE_DP_SW_RESET_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SW_RST |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-300. EDP_CORE_DP_SW_RESET_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | SW_RST | R/W | 0h | Unused. Kept RW for software backward compatibility. |

8.5.90 EDP_CORE_DP_FRAMER_TU_P Register (Offset = 2208h) [reset = A002h]

EDP_CORE_DP_FRAMER_TU_P is shown in [Figure 8-146](#) and described in [Table 8-302](#).

Return to [Summary Table](#).

Transfer Unit configuration register. Relevant only in SST mode. These register must be set before transitioning to video mode.

Table 8-301. EDP_CORE_DP_FRAMER_TU_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2208h |

Figure 8-146. EDP_CORE_DP_FRAMER_TU_P Register

| | | | | | | | |
|------------------------|-------------------|------------------|----|----|----|----|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | BS_SR_REPLACE_POSITION |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BS_SR_REPLACE_POSITION | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TU_CNT_RST_EN | TU_SIZE | | | | | | |
| R/W-1h | R/W-20h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | TU_SST_FAST_DRAIN | TU_VALID_SYMBOLS | | | | | |
| R-0h | R/W-0h | R/W-2h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-302. EDP_CORE_DP_FRAMER_TU_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 24-16 | BS_SR_REPLACE_POSITION | R/W | 0h | Static debug register. When set to non-zero value, the BS counter will be reinitialized to this value that will result in earlier initial SR insertion. |
| 15 | TU_CNT_RST_EN | R/W | 1h | Unused. Kept RW for software backward compatibility. |
| 14-8 | TU_SIZE | R/W | 20h | Transfer Unit size. Even values between 32 and 64 are supported. |
| 7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | TU_SST_FAST_DRAIN | R/W | 0h | Allow the video FIFO to drain faster at end of line. This setting applies only to SST mode. |

Table 8-302. EDP_CORE_DP_FRAMER_TU_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 5-0 | TU_VALID_SYMBOLS | R/W | 2h | <p>Number of valid symbols per Transfer Unit [TU]. Rounded down to lower integer value [refer to equation in DP specification]. Allowed values are 1 to [TU_size-1]. TU valid smaller than one that would result this register to be set to 0 are not supported by the IP. This setting applies only to SST mode.</p> |

8.5.91 EDP_CORE_DP_FRAMER_BS_SR_INTRVL_P Register (Offset = 2218h) [reset = 200h]

EDP_CORE_DP_FRAMER_BS_SR_INTRVL_P is shown in [Figure 8-147](#) and described in [Table 8-304](#).

Return to [Summary Table](#).

SR insertion interval for SST mode.

Table 8-303.
EDP_CORE_DP_FRAMER_BS_SR_INTRVL_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2218h |

Figure 8-147. EDP_CORE_DP_FRAMER_BS_SR_INTRVL_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | BS_SR_INTERVAL | | | | | | | |
| R-0h | | | | | | | | R/W-200h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-304. EDP_CORE_DP_FRAMER_BS_SR_INTRVL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9-0 | BS_SR_INTERVAL | R/W | 200h | Static debug register. Controls how often BS is replaced by SR in SST mode. Default value of 512 results in every 512th BS being replaced by SR as per DP spec. This register can only be changed for a test purposes in order to speed up BS-SR replacement. |

8.5.92 EDP_CORE_DP_MTPH_ECF_SLOTS_31_0_P Register (Offset = 2258h) [reset = 0h]

EDP_CORE_DP_MTPH_ECF_SLOTS_31_0_P is shown in [Figure 8-148](#) and described in [Table 8-306](#).

Return to [Summary Table](#).

Bits [31:1] contains which MST timeslot 31-1 should be encrypted.

Bit [0] must be set to 1 to enable encryption.

Relevant only in MST mode.

Table 8-305.
EDP_CORE_DP_MTPH_ECF_SLOTS_31_0_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2258h |

Figure 8-148. EDP_CORE_DP_MTPH_ECF_SLOTS_31_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TSLOT_ENCRYPT31_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-306. EDP_CORE_DP_MTPH_ECF_SLOTS_31_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|----------------------|
| 31-0 | TSLOT_ENCRYPT31_0 | R/W | 0h | tslot_encrypt 31 - 0 |

8.5.93 EDP_CORE_DP_MTPH_ECF_SLOTS_63_32_P Register (Offset = 225Ch) [reset = 0h]

EDP_CORE_DP_MTPH_ECF_SLOTS_63_32_P is shown in [Figure 8-149](#) and described in [Table 8-308](#).

Return to [Summary Table](#).

Contains which MST timeslot 63-32 should be encrypted. This register must be set properly before ECF sequence is triggered. Relevant only in MST mode.

Table 8-307.
EDP_CORE_DP_MTPH_ECF_SLOTS_63_32_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 225Ch |

Figure 8-149. EDP_CORE_DP_MTPH_ECF_SLOTS_63_32_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TSLOT_ENCRYPT63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-308. EDP_CORE_DP_MTPH_ECF_SLOTS_63_32_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|-----------------------|
| 31-0 | TSLOT_ENCRYPT63_32 | R/W | 0h | tslot_encrypt 63 - 32 |

8.5.94 EDP_CORE_DP_MTPH_LVP_SYMBOL_P Register (Offset = 2260h) [reset = 531Fh]

EDP_CORE_DP_MTPH_LVP_SYMBOL_P is shown in [Figure 8-150](#) and described in [Table 8-310](#).

Return to [Summary Table](#).

Link Verification Pattern value to be inserted in the MTP header. Relevant only in MST mode.

Table 8-309.
EDP_CORE_DP_MTPH_LVP_SYMBOL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2260h |

Figure 8-150. EDP_CORE_DP_MTPH_LVP_SYMBOL_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | MTPH_LVP_SYM | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-531Fh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-310. EDP_CORE_DP_MTPH_LVP_SYMBOL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | MTPH_LVP_SYM | R/W | 531Fh | Symbol value for LINK VERIFICATION PATTERN [LVP] |

8.5.95 EDP_CORE_DP_MTPH_CONTROL_P Register (Offset = 2264h) [reset = 0h]

EDP_CORE_DP_MTPH_CONTROL_P is shown in [Figure 8-151](#) and described in [Table 8-312](#).

Return to [Summary Table](#).

MTP header control. Relevant only in MST mode.

Table 8-311. EDP_CORE_DP_MTPH_CONTROL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2264h |

Figure 8-151. EDP_CORE_DP_MTPH_CONTROL_P Register

| | | | | | | | |
|----------|----|----|----|----|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | MTPH_LVP_EN | MTPH_ACT_EN | MTPH_ECF_EN |
| R-0h | | | | | R/W-0h | W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 8-312. EDP_CORE_DP_MTPH_CONTROL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 2 | MTPH_LVP_EN | R/W | 0h | Unused. Kept RW for software backward compatibility. |
| 1 | MTPH_ACT_EN | W | 0h | MST feature when written with value 1, an ACT sequence will be triggered for slot allocation control. This bit is write only. |
| 0 | MTPH_ECF_EN | R/W | 0h | Unused. Kept RW for software backward compatibility. |

8.5.96 EDP_CORE_DP_MTPH_STATUS_P Register (Offset = 226Ch) [reset = 0h]

EDP_CORE_DP_MTPH_STATUS_P is shown in [Figure 8-152](#) and described in [Table 8-314](#).

Return to [Summary Table](#).

MTP header status. Relevant only in MST mode.

Table 8-313. EDP_CORE_DP_MTPH_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 226Ch |

Figure 8-152. EDP_CORE_DP_MTPH_STATUS_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | MTPH_ACT_ST ATUS |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-314. EDP_CORE_DP_MTPH_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | MTPH_ACT_STATUS | R | 0h | Status of ACT insertion. Returns 1 until ACT sequence completes. |

8.5.97 EDP_CORE_DPTX_LANE_EN_P Register (Offset = 2300h) [reset = 0h]

EDP_CORE_DPTX_LANE_EN_P is shown in [Figure 8-153](#) and described in [Table 8-316](#).

Return to [Summary Table](#).

DPTX lane enable

Table 8-315. EDP_CORE_DPTX_LANE_EN_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2300h |

Figure 8-153. EDP_CORE_DPTX_LANE_EN_P Register

| | | | | | | | |
|----------|----|----|----|------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | DPTX_LANE_ENABLE | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-316. EDP_CORE_DPTX_LANE_EN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3-0 | DPTX_LANE_ENABLE | R/W | 0h | DPTX lane enable each lane as a bit when 1 lane is enabled |

8.5.98 EDP_CORE_DPTX_ENHNCD_P Register (Offset = 2304h) [reset = 0h]

EDP_CORE_DPTX_ENHNCD_P is shown in [Figure 8-154](#) and described in [Table 8-318](#).

Return to [Summary Table](#).

DPTX enhanced mode control register. Relevant only in SST mode. In MST mode it is ignored.

**Table 8-317. EDP_CORE_DPTX_ENHNCD_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2304h |

Figure 8-154. EDP_CORE_DPTX_ENHNCD_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | DPTX_ENHAN CED_MODE |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-318. EDP_CORE_DPTX_ENHNCD_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | DPTX_ENHANCED_MODE | R/W | 0h | Enhanced mode control 0x 0 - enhanced mode disabled 0x 1 - enhanced mode enabled. Enhanced mode should always be enabled if Sink supports it. |

8.5.99 EDP_CORE_DPTX_INT_MASK_P Register (Offset = 2308h) [reset = 3h]

EDP_CORE_DPTX_INT_MASK_P is shown in [Figure 8-155](#) and described in [Table 8-320](#).

Return to [Summary Table](#).

DPTX Interrupt mask.

Table 8-319. EDP_CORE_DPTX_INT_MASK_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2308h |

Figure 8-155. EDP_CORE_DPTX_INT_MASK_P Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | FRAMER_SRC _INT_MASK | HPD_SRC_INT _MASK |
| R-0h | | | | | | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-320. EDP_CORE_DPTX_INT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | FRAMER_SRC_INT_MAS K | R/W | 1h | Framer mask interrupt 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 0 | HPD_SRC_INT_MASK | R/W | 1h | HPD mask interrupt 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.5.100 EDP_CORE_DPTX_INT_STATUS_P Register (Offset = 230Ch) [reset = 0h]

EDP_CORE_DPTX_INT_STATUS_P is shown in [Figure 8-156](#) and described in [Table 8-322](#).

Return to [Summary Table](#).

DPTX interrupt status register. This interrupts are tracked by firmware and not accessible directly to the Host processor.

**Table 8-321. EDP_CORE_DPTX_INT_STATUS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 230Ch |

Figure 8-156. EDP_CORE_DPTX_INT_STATUS_P Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | FRAMER_SRC _INT | HPD_SRC_INT |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-322. EDP_CORE_DPTX_INT_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | FRAMER_SRC_INT | R | 0h | Framer interrupt - not used. |
| 0 | HPD_SRC_INT | R | 0h | HPD interrupt. Active HIGH. If set further status can be read from HPD_EVENT_DET register. This bit is automatically cleared on read from HPD_EVENT_DET register. |

8.5.101 EDP_CORE_DPTX_FEC_CTRL_P Register (Offset = 2310h) [reset = 0h]

EDP_CORE_DPTX_FEC_CTRL_P is shown in [Figure 8-157](#) and described in [Table 8-324](#).

Return to [Summary Table](#).

DPTX FEC control register.

Table 8-323. EDP_CORE_DPTX_FEC_CTRL_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2310h |

Figure 8-157. EDP_CORE_DPTX_FEC_CTRL_P Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CFG_FEC_READY | CFG_FEC_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-324. EDP_CORE_DPTX_FEC_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | CFG_FEC_READY | R/W | 0h | Equivalent DPCD register FEC_READY, enable alternative CP coding. This bit must be set high before link training if FEC is going to be enabled. |
| 0 | CFG_FEC_EN | R/W | 0h | FEC Enable 1-enabled 0-disabled. This bit can be changed on when there is no video transmission [and cfg_fec_ready was set before link training]. |

8.5.102 EDP_CORE_DPTX_FEC_STATUS_P Register (Offset = 2314h) [reset = 2h]

EDP_CORE_DPTX_FEC_STATUS_P is shown in [Figure 8-158](#) and described in [Table 8-326](#).

Return to [Summary Table](#).

FEC status register.

**Table 8-325. EDP_CORE_DPTX_FEC_STATUS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2314h |

Figure 8-158. EDP_CORE_DPTX_FEC_STATUS_P Register

| | | | | | | | |
|----------|----|----|----------------|----|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | FEC_FSM_STATUS | | | FEC_BUSY | |
| R-0h | | | R-1h | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 8-326. EDP_CORE_DPTX_FEC_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 4-1 | FEC_FSM_STATUS | R | 1h | FEC FSM status, 1-FEC is off, 2-generate enable sequence, 4-normal work, 8-generate disable sequence. Used for debug purposes only. |
| 0 | FEC_BUSY | R | 0h | FEC Active status. Set in line with first symbol of FEC_DECODE_EN sequence and de-asserts in line with last symbol of FEC_DECODE_DIS sequence. |

8.5.103 EDP_CORE_HDCP_DP_STATUS_P Register (Offset = 2400h) [reset = 0h]

EDP_CORE_HDCP_DP_STATUS_P is shown in [Figure 8-159](#) and described in [Table 8-328](#).

Return to [Summary Table](#).

HDCP DP status register.

Table 8-327. EDP_CORE_HDCP_DP_STATUS_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2400h |

Figure 8-159. EDP_CORE_HDCP_DP_STATUS_P Register

| | | | | | | | |
|----------|----|------------------|---------------------------|----|----|---------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | PSLVERR_HD CP | HDCP_DP_ENCRYPTION_ENABLE | | | HDCP_DP_AU THENTICATED | |
| R-0h | | R-0h | R-0h | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 8-328. EDP_CORE_HDCP_DP_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5 | PSLVERR_HDCP | R | 0h | APB slave error status from HDCP module has been reported when this bit is set to 1. |
| 4-1 | HDCP_DP_ENCRYPTION_ENABLE | R | 0h | Encryption is enabled when this bit is set to 1. |
| 0 | HDCP_DP_AUTHENTICATED | R | 0h | HDCP 1.3 authentication is enabled when this bit is set to 1. |

8.5.104 EDP_CORE_HDCP_DP_CONFIG_P Register (Offset = 2404h) [reset = 9h]

EDP_CORE_HDCP_DP_CONFIG_P is shown in [Figure 8-160](#) and described in [Table 8-330](#).

Return to [Summary Table](#).

HDCP DP config register.

**Table 8-329. EDP_CORE_HDCP_DP_CONFIG_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2404h |

Figure 8-160. EDP_CORE_HDCP_DP_CONFIG_P Register

| | | | | | | | |
|----------|----------------------|----------------------|----------------|----|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | SST_HDCP_ENCRYPT_DIS | HDCP_VBID5_ALIGN_DIS | HDCP_DP_BYPASS | | HDCP_DP_VERSION | | |
| R-0h | R/W-0h | R/W-0h | R/W-1h | | R/W-1h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-330. EDP_CORE_HDCP_DP_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | SST_HDCP_ENCRYPT_DIS | R/W | 0h | Disable automatic HDCP encryption in SST mode when cipher is authenticated. This bit can also be set to 1 to disable encryption |
| 5 | HDCP_VBID5_ALIGN_DIS | R/W | 0h | Debug register, no longer used. |
| 4-3 | HDCP_DP_BYPASS | R/W | 1h | HDCP DP bypass. No-bypass must be set prior link training if HDCP is going to be used. This field must not be changed during operation. 0x 0-No bypass 0x 1-Bypass enabled All other combinations reserved. |

Table 8-330. EDP_CORE_HDCP_DP_CONFIG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 2-0 | HDCP_DP_VERSION | R/W | 1h | HDCP version. 0x 1-HDCP2.2 0x 2-HDCP1.4 Other-Reserved |

8.5.105 EDP_CORE_HDCP_DP_SW_RST_P Register (Offset = 2408h) [reset = 0h]

EDP_CORE_HDCP_DP_SW_RST_P is shown in [Figure 8-161](#) and described in [Table 8-332](#).

Return to [Summary Table](#).

HDCP DP software reset register

**Table 8-331. EDP_CORE_HDCP_DP_SW_RST_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2408h |

Figure 8-161. EDP_CORE_HDCP_DP_SW_RST_P Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CIPHER_CTRL _SW_RST | SW_RST |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-332. EDP_CORE_HDCP_DP_SW_RST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | CIPHER_CTRL_SW_RST | R/W | 0h | Software reset of cipher control logic only. |
| 0 | SW_RST | R/W | 0h | Software reset. |

8.5.106 EDP_CORE_HDCP_DP_FIFO_STATUS_P Register (Offset = 240Ch) [reset = 0h]

EDP_CORE_HDCP_DP_FIFO_STATUS_P is shown in [Figure 8-162](#) and described in [Table 8-334](#).

Return to [Summary Table](#).

HDCP DP FIFO status register.

Table 8-333.
EDP_CORE_HDCP_DP_FIFO_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 240Ch |

Figure 8-162. EDP_CORE_HDCP_DP_FIFO_STATUS_P Register

| | | | | | | | |
|---|--|---|--|---|--|---|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | HDCP_DP_SS T_1_4_FIFO1_ UNDERFLOW | HDCP_DP_SS T_1_4_FIFO1_ OVERFLOW | HDCP_DP_SS T_1_4_FIFO0_ UNDERFLOW | HDCP_DP_SS T_1_4_FIFO0_ OVERFLOW |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HDCP_DP_SS T_2_2_FIFO3_ UNDERFLOW | HDCP_DP_SS T_2_2_FIFO3_ OVERFLOW | HDCP_DP_SS T_2_2_FIFO2_ UNDERFLOW | HDCP_DP_SS T_2_2_FIFO2_ OVERFLOW | HDCP_DP_SS T_2_2_FIFO1_ UNDERFLOW | HDCP_DP_SS T_2_2_FIFO1_ OVERFLOW | HDCP_DP_SS T_2_2_FIFO0_ UNDERFLOW | HDCP_DP_SS T_2_2_FIFO0_ OVERFLOW |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-334. EDP_CORE_HDCP_DP_FIFO_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-12 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 11 | HDCP_DP_SST_1_4_FIF O1_UNDERFLOW | R | 0h | SST HDCP1.4 fifo1 underflow. |
| 10 | HDCP_DP_SST_1_4_FIF O1_OVERFLOW | R | 0h | SST HDCP1.4 fifo1 overflow. |
| 9 | HDCP_DP_SST_1_4_FIF O0_UNDERFLOW | R | 0h | SST HDCP1.4 fifo0 underflow. |
| 8 | HDCP_DP_SST_1_4_FIF O0_OVERFLOW | R | 0h | SST HDCP1.4 fifo0 overflow. |
| 7 | HDCP_DP_SST_2_2_FIF O3_UNDERFLOW | R | 0h | SST HDCP2.2 fifo3 underflow. |
| 6 | HDCP_DP_SST_2_2_FIF O3_OVERFLOW | R | 0h | SST HDCP2.2 fifo3 overflow. |
| 5 | HDCP_DP_SST_2_2_FIF O2_UNDERFLOW | R | 0h | SST HDCP2.2 fifo2 underflow. |
| 4 | HDCP_DP_SST_2_2_FIF O2_OVERFLOW | R | 0h | SST HDCP2.2 fifo2 overflow. |

Table 8-334. EDP_CORE_HDCP_DP_FIFO_STATUS_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------------|------|-------|------------------------------|
| 3 | HDCP_DP_SST_2_2_FIFO1_UNDERFLOW | R | 0h | SST HDCP2.2 fifo1 underflow. |
| 2 | HDCP_DP_SST_2_2_FIFO1_OVERFLOW | R | 0h | SST HDCP2.2 fifo1 overflow. |
| 1 | HDCP_DP_SST_2_2_FIFO0_UNDERFLOW | R | 0h | SST HDCP2.2 fifo0 underflow. |
| 0 | HDCP_DP_SST_2_2_FIFO0_OVERFLOW | R | 0h | SST HDCP2.2 fifo0 overflow. |

8.5.107 EDP_CORE_DP_AUX_HOST_CONTROL_P Register (Offset = 2800h) [reset = 4h]

EDP_CORE_DP_AUX_HOST_CONTROL_P is shown in [Figure 8-163](#) and described in [Table 8-336](#).

Return to [Summary Table](#).

DP AUX control register.

Table 8-335.
EDP_CORE_DP_AUX_HOST_CONTROL_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2800h |

Figure 8-163. EDP_CORE_DP_AUX_HOST_CONTROL_P Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------------------|-----------------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | AUX_HOST_T RANSMIT_IMM EDIATE | AUX_HOST_P RECHARGE_E NABLE | AUX_HOST_AL WAYS_READ |
| R-0h | | | | | R/W-1h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-336. EDP_CORE_DP_AUX_HOST_CONTROL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|--|
| 31-3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 2 | AUX_HOST_TRANSMIT_I MMEDIATE | R/W | 1h | This bit is used only in DP_OUT mode. If SET, a transaction that comes from the adapter will be sent immediately without waiting for send_external_transaction pulse. If CLEAR, the MC controls the traffic to/from the adapter. |
| 1 | AUX_HOST_PRECHARG E_ENABLE | R/W | 0h | According to the current standard the tx precharge is done by sending 10 to 16 data_0 on the line before the SYNC. Old standard define the precharge by forcing the AFE to be in precharge mode before transmitting the SYNC. |
| 0 | AUX_HOST_ALWAYS_RE AD | R/W | 0h | Normally, the aux_rx is disabled during transmit. Setting this bit allow loopback operation and all transmit transactions will go to the receiver. Used for debug purpose. |

8.5.108 EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P Register (Offset = 2804h) [reset = 0h]

EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P is shown in [Figure 8-164](#) and described in [Table 8-338](#).

Return to [Summary Table](#).

Status of the DP_AUX interrupt sources. These interrupts are tracked by firmware and not accessible directly to the Host processor.

Table 8-337.
EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2804h |

Figure 8-164. EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P Register

| | | | | | | | |
|------------------------------|-----------------------------|---------------------------------|-----------------------------------|-------------------------|---------------------------|--------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | AUX_MAIN_EXPIRE_TX | AUX_RX_ERROR_CYCLE_TIME |
| R-0h | | | | | | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_MAIN_RX_STATUS_CORRUPTED | AUX_MAIN_RX_STATUS_LOG_DATA | AUX_MAIN_RX_STATUS_LOG_PREAMBLE | AUX_MAIN_RX_STATUS_SHORT_PREAMBLE | AUX_MAIN_RX_STATUS_DONE | AUX_RX_DATA_TRANSFER_INIT | AUX_TX_DONE | PSLVERR_DPAUX |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-338. EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9 | AUX_MAIN_EXPIRE_TX | R | 0h | Timer expire [external] in DP_OUT. Active HIGH. Clear on read. |
| 8 | AUX_RX_ERROR_CYCLE_TIME | R | 0h | Cycle time error. Asserted if aux_rx_last_cycle is less then aux_host_1m_min or greater then aux_host_1m_max. Active HIGH. Clear on read. |
| 7 | AUX_MAIN_RX_STATUS_CORRUPTED | R | 0h | The received transaction corrupted during the data phase [bad STOP, or unaligned STOP]. Active HIGH. Clear on read. |

Table 8-338. EDP_CORE_DP_AUX_INTERRUPT_SOURCE_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------------|------|-------|--|
| 6 | AUX_MAIN_RX_STATUS_LONG_DATA | R | 0h | The received transaction had more than 20 data bytes. Active HIGH. Clear on read. |
| 5 | AUX_MAIN_RX_STATUS_LONG_PREAMBLE | R | 0h | The received transaction had preamble greater than the preamble_max. Active HIGH. Clear on read. |
| 4 | AUX_MAIN_RX_STATUS_SHORT_PREAMBLE | R | 0h | The received transaction had preamble shorter than the preamble_max. Active HIGH. Clear on read. |
| 3 | AUX_MAIN_RX_STATUS_DONE | R | 0h | This module control the packet extraction and packet read from the memory. Active HIGH. Clear on read. |
| 2 | AUX_RX_DATA_TRANSFER_INIT | R | 0h | Rx data transfer may be initiated. Falling edge of the aux_mailbox_empty. Active HIGH. Clear on read. |
| 1 | AUX_TX_DONE | R | 0h | Tx data transfer finished. Active HIGH. Clear on read. |
| 0 | PSLVERR_DPAUX | R | 0h | APB slave error interrupt from DP AUX module. Active HIGH. Clear on read. |

8.5.109 EDP_CORE_DP_AUX_INTERRUPT_MASK_P Register (Offset = 2808h) [reset = 0h]

EDP_CORE_DP_AUX_INTERRUPT_MASK_P is shown in [Figure 8-165](#) and described in [Table 8-340](#).

Return to [Summary Table](#).

Mask vector of the DP_AUX interrupt sources.

Table 8-339.
EDP_CORE_DP_AUX_INTERRUPT_MASK_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2808h |

Figure 8-165. EDP_CORE_DP_AUX_INTERRUPT_MASK_P Register

| | | | | | | | |
|-----------------------------------|-----------------------------------|---------------------------------------|--|------------------------------|--------------------------------|-------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | AUX_MAIN_EXPIRE_TX_MASK | AUX_RX_ERROR_CYCLE_TIME_MASK |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_MAIN_RX_STATUS_CORRUPTED_MASK | AUX_MAIN_RX_STATUS_LONG_DATA_MASK | AUX_MAIN_RX_STATUS_LONG_PREAMBLE_MASK | AUX_MAIN_RX_STATUS_SHORT_PREAMBLE_MASK | AUX_MAIN_RX_STATUS_DONE_MASK | AUX_RX_DATA_TRANSFER_INIT_MASK | AUX_TX_DONE_MASK | PSLVERR_MASK |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-340. EDP_CORE_DP_AUX_INTERRUPT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9 | AUX_MAIN_EXPIRE_TX_MASK | R/W | 0h | aux_main_expire_external mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 8 | AUX_RX_ERROR_CYCLE_TIME_MASK | R/W | 0h | aux_rx_error_cycle_time mask 0x 0-interrupt enabled 0x 1-interrupt disabled |

Table 8-340. EDP_CORE_DP_AUX_INTERRUPT_MASK_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--|------|-------|---|
| 7 | AUX_MAIN_RX_STATUS_CORRUPTED_MASK | R/W | 0h | aux_main_rx_status_corrupted_mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 6 | AUX_MAIN_RX_STATUS_LONG_DATA_MASK | R/W | 0h | aux_main_rx_status_long_data_mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 5 | AUX_MAIN_RX_STATUS_LONG_PREAMBLE_MASK | R/W | 0h | aux_main_rx_status_long_preamble_mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 4 | AUX_MAIN_RX_STATUS_SHORT_PREAMBLE_MASK | R/W | 0h | aux_main_rx_status_short_preamble_mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 3 | AUX_MAIN_RX_STATUS_DONE_MASK | R/W | 0h | aux_main_rx_status_done_mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 2 | AUX_RX_DATA_TRANSFER_INIT_MASK | R/W | 0h | rx_data_transfer_init mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 1 | AUX_TX_DONE_MASK | R/W | 0h | aux_tx_done_mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 0 | PSLVERR_MASK | R/W | 0h | Mask for pslverr_dpaux interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.5.110 EDP_CORE_DP_AUX_SWAP_INVERSION_CONTROL_P Register (Offset = 280Ch) [reset = 0h]

EDP_CORE_DP_AUX_SWAP_INVERSION_CONTROL_P is shown in [Figure 8-166](#) and described in [Table 8-342](#).

Return to [Summary Table](#).

Ordering and inversion of transmit/receive on Auxiliary Channel.

Table 8-341.
EDP_CORE_DP_AUX_SWAP_INVERSION_CONTROL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 280Ch |

Figure 8-166. EDP_CORE_DP_AUX_SWAP_INVERSION_CONTROL_P Register

| | | | | | | | |
|----------|----|----|----|------------------|------------------|--------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | AUX_HOST_RX_SWAP | AUX_HOST_TX_SWAP | AUX_HOST_RX_INVERT | AUX_HOST_TX_INVERT |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-342. EDP_CORE_DP_AUX_SWAP_INVERSION_CONTROL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | AUX_HOST_RX_SWAP | R/W | 0h | Shift right [LSB first] of the income data |
| 2 | AUX_HOST_TX_SWAP | R/W | 0h | Shift right the output data [LSB first] |
| 1 | AUX_HOST_RX_INVERT | R/W | 0h | Invert rx input and output data to AUXILIARY CHANNEL |
| 0 | AUX_HOST_TX_INVERT | R/W | 0h | Invert tx input and output data to AUXILIARY CHANNEL |

8.5.111 EDP_CORE_DP_AUX_SEND_NACK_TRANSACTION_P Register (Offset = 2810h) [reset = 0h]

EDP_CORE_DP_AUX_SEND_NACK_TRANSACTION_P is shown in [Figure 8-167](#) and described in [Table 8-344](#).

Return to [Summary Table](#).

NACK transaction send

Table 8-343.
EDP_CORE_DP_AUX_SEND_NACK_TRANSACTION_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2810h |

Figure 8-167. EDP_CORE_DP_AUX_SEND_NACK_TRANSACTION_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | AUX_HOST_SEND_NACK_TRANSACTION |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-344. EDP_CORE_DP_AUX_SEND_NACK_TRANSACTION_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | AUX_HOST_SEND_NACK_TRANSACTION | R/W | 0h | Send nack transaction by AUX_TX. This bit is automatically cleared when operation is completed. |

8.5.112 EDP_CORE_DP_AUX_CLEAR_RX_P Register (Offset = 2814h) [reset = 0h]

EDP_CORE_DP_AUX_CLEAR_RX_P is shown in [Figure 8-168](#) and described in [Table 8-346](#).

Return to [Summary Table](#).

RX bits clear.

**Table 8-345. EDP_CORE_DP_AUX_CLEAR_RX_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2814h |

Figure 8-168. EDP_CORE_DP_AUX_CLEAR_RX_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | AUX_HOST_CLEAR_RX |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-346. EDP_CORE_DP_AUX_CLEAR_RX_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | AUX_HOST_CLEAR_RX | R/W | 0h | Clear all rx bits in register 64,65. This command is an indication that the processing of last receive transaction was completed and the AUX_RX can start looking for new receive transaction. This bit is automatically cleared when operation is completed. |

8.5.113 EDP_CORE_DP_AUX_CLEAR_TX_P Register (Offset = 2818h) [reset = 0h]

EDP_CORE_DP_AUX_CLEAR_TX_P is shown in [Figure 8-169](#) and described in [Table 8-348](#).

Return to [Summary Table](#).

TX bits clear.

Table 8-347. EDP_CORE_DP_AUX_CLEAR_TX_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2818h |

Figure 8-169. EDP_CORE_DP_AUX_CLEAR_TX_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | AUX_HOST_CLEAR_TX |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-348. EDP_CORE_DP_AUX_CLEAR_TX_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | AUX_HOST_CLEAR_TX | R/W | 0h | Clear all external bits in registers 64,67. This command used in DP_IN mode. It is an indication that the processing of last external transaction was completed and the DP_AUX can start receive new external transaction from the adapter. This bit is automatically cleared when operation in completed. |

8.5.114 EDP_CORE_DP_AUX_TIMER_STOP_P Register (Offset = 281Ch) [reset = 0h]

EDP_CORE_DP_AUX_TIMER_STOP_P is shown in [Figure 8-170](#) and described in [Table 8-350](#).

Return to [Summary Table](#).

Stop timer operation.

**Table 8-349. EDP_CORE_DP_AUX_TIMER_STOP_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 281Ch |

Figure 8-170. EDP_CORE_DP_AUX_TIMER_STOP_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | AUX_HOST_ST OP_TIMER |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-350. EDP_CORE_DP_AUX_TIMER_STOP_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | AUX_HOST_STOP_TIME R | R/W | 0h | Stop timer operation. |

8.5.115 EDP_CORE_DP_AUX_TIMER_CLEAR_P Register (Offset = 2820h) [reset = 0h]

EDP_CORE_DP_AUX_TIMER_CLEAR_P is shown in [Figure 8-171](#) and described in [Table 8-352](#).

Return to [Summary Table](#).

Clear timer operation.

Table 8-351.
EDP_CORE_DP_AUX_TIMER_CLEAR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2820h |

Figure 8-171. EDP_CORE_DP_AUX_TIMER_CLEAR_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | AUX_HOST_CLEAR_TIMER |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-352. EDP_CORE_DP_AUX_TIMER_CLEAR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | AUX_HOST_CLEAR_TIMER | R/W | 0h | Stop timer operation. This bit is automatically cleared when operation in completed. |

8.5.116 EDP_CORE_DP_AUX_RESET_SW_P Register (Offset = 2824h) [reset = 0h]

EDP_CORE_DP_AUX_RESET_SW_P is shown in [Figure 8-172](#) and described in [Table 8-354](#).

Return to [Summary Table](#).

Soft reset of the DP_AUX.

Table 8-353. EDP_CORE_DP_AUX_RESET_SW_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2824h |

Figure 8-172. EDP_CORE_DP_AUX_RESET_SW_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | AUX_HOST_SW_RESET |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-354. EDP_CORE_DP_AUX_RESET_SW_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | AUX_HOST_SW_RESET | R/W | 0h | Reset all DP_AUX state machines and clear all the status bits. The registers value remains. [S/W reset]. This bit is automatically cleared when operation in completed. |

8.5.117 EDP_CORE_DP_AUX_DIVIDE_2M_P Register (Offset = 2828h) [reset = Bh]

EDP_CORE_DP_AUX_DIVIDE_2M_P is shown in [Figure 8-173](#) and described in [Table 8-356](#).

Return to [Summary Table](#).

SYS_CLK and 2 MHz clock ratio. This register is used to ensure correct AUX channel bitrate for different values of a system clock.

Table 8-355. EDP_CORE_DP_AUX_DIVIDE_2M_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2828h |

Figure 8-173. EDP_CORE_DP_AUX_DIVIDE_2M_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | AUX_HOST_DIVIDE_2M | | | | | | | |
| R-0h | | | | | | | | R/W-Bh | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-356. EDP_CORE_DP_AUX_DIVIDE_2M_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 7-0 | AUX_HOST_DIVIDE_2M | R/W | Bh | The ratio between sys_clk and 2MHz, $[(\text{sys_clk frequency}/2\text{MHz}) - 1]$, for 25MHz sys_clk the value is 11. This register is used by AUX_TX for generating the AUX_TX clock. |

8.5.118 EDP_CORE_DP_AUX_TX_PRECHARGE_LENGTH_P Register (Offset = 282Ch) [reset = 10h]

EDP_CORE_DP_AUX_TX_PRECHARGE_LENGTH_P is shown in [Figure 8-174](#) and described in [Table 8-358](#).

Return to [Summary Table](#).

Pre charge field length.

Table 8-357.
EDP_CORE_DP_AUX_TX_PRECHARGE_LENGTH_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 282Ch |

Figure 8-174. EDP_CORE_DP_AUX_TX_PRECHARGE_LENGTH_P Register

| | | | | | | | |
|----------|----|---------------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | AUX_HOST_PRECHARGE_LENGTH | | | | | |
| R-0h | | R/W-10h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-358. EDP_CORE_DP_AUX_TX_PRECHARGE_LENGTH_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5-0 | AUX_HOST_PRECHARGE_LENGTH | R/W | 10h | Length of pre charge field, standard definition is 10 to 16 bits/clocks. |

8.5.119 EDP_CORE_DP_AUX_FREQUENCY_1M_MAX_P Register (Offset = 2830h) [reset = 22h]

EDP_CORE_DP_AUX_FREQUENCY_1M_MAX_P is shown in [Figure 8-175](#) and described in [Table 8-360](#).

Return to [Summary Table](#).

Maximum legal receiving frequency.

Table 8-359.
EDP_CORE_DP_AUX_FREQUENCY_1M_MAX_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2830h |

Figure 8-175. EDP_CORE_DP_AUX_FREQUENCY_1M_MAX_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | AUX_HOST_1M_MAX | | | | | | | | | |
| R-0h | | | | | | R/W-22h | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-360. EDP_CORE_DP_AUX_FREQUENCY_1M_MAX_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 10-0 | AUX_HOST_1M_MAX | R/W | 22h | The maximum legal frequency receiving from the line by the standard is 1.25MHz.The calculation is:[1.25 MHz cycle time]/[sys_clk[-15%] cycle time] 800/46 =17 |

8.5.120 EDP_CORE_DP_AUX_FREQUENCY_1M_MIN_P Register (Offset = 2834h) [reset = 9h]

EDP_CORE_DP_AUX_FREQUENCY_1M_MIN_P is shown in [Figure 8-176](#) and described in [Table 8-362](#).

Return to [Summary Table](#).

Minimum legal receiving frequency.

Table 8-361.
EDP_CORE_DP_AUX_FREQUENCY_1M_MIN_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2834h |

Figure 8-176. EDP_CORE_DP_AUX_FREQUENCY_1M_MIN_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | AUX_HOST_1M_MIN | | | | | | | | | |
| R-0h | | | | | | R/W-9h | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-362. EDP_CORE_DP_AUX_FREQUENCY_1M_MIN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 10-0 | AUX_HOST_1M_MIN | R/W | 9h | The minimum legal frequency receiving from the line by the standard is 0.83MHz.The calculation is:[0.83 MHz cycle time]/[sys_clk[+15%] cycle time] 1200/ 34 =35 |

8.5.121 EDP_CORE_DP_AUX_RX_PRE_MIN_P Register (Offset = 2838h) [reset = 1Ah]

EDP_CORE_DP_AUX_RX_PRE_MIN_P is shown in [Figure 8-177](#) and described in [Table 8-364](#).

Return to [Summary Table](#).

Minimum received preamble length

Table 8-363. EDP_CORE_DP_AUX_RX_PRE_MIN_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2838h |

Figure 8-177. EDP_CORE_DP_AUX_RX_PRE_MIN_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | AUX_HOST_PRE_MIN | | | | | |
| R-0h | | | | | | | | | | R/W-1Ah | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-364. EDP_CORE_DP_AUX_RX_PRE_MIN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5-0 | AUX_HOST_PRE_MIN | R/W | 1Ah | Valid minimum length of preamble during receive. The standard defines pre_min=26 The value of this register should be greater then the average_number_of_cycles defined in reg 0 [2 , 4 or 8] |

8.5.122 EDP_CORE_DP_AUX_RX_PRE_MAX_P Register (Offset = 283Ch) [reset = 20h]

EDP_CORE_DP_AUX_RX_PRE_MAX_P is shown in [Figure 8-178](#) and described in [Table 8-366](#).

Return to [Summary Table](#).

Maximum received preamble length.

**Table 8-365. EDP_CORE_DP_AUX_RX_PRE_MAX_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 283Ch |

Figure 8-178. EDP_CORE_DP_AUX_RX_PRE_MAX_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | AUX_HOST_PRE_MAX | | | | | |
| R-0h | | | | | | | | | | R/W-20h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-366. EDP_CORE_DP_AUX_RX_PRE_MAX_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5-0 | AUX_HOST_PRE_MAX | R/W | 20h | Valid maximum length of preamble during receive. The standard defines pre_max = 32 |

8.5.123 EDP_CORE_DP_AUX_TIMER_PRESET_P Register (Offset = 2840h) [reset = 1D4Ch]

EDP_CORE_DP_AUX_TIMER_PRESET_P is shown in [Figure 8-179](#) and described in [Table 8-368](#).

Return to [Summary Table](#).

DP_AUX_MAIN start value

Table 8-367.
EDP_CORE_DP_AUX_TIMER_PRESET_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2840h |

Figure 8-179. EDP_CORE_DP_AUX_TIMER_PRESET_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_HOST_TIMER_PRESET | | | | | | | | | | | | | | | |
| R/W-1D4Ch | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-368. EDP_CORE_DP_AUX_TIMER_PRESET_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | AUX_HOST_TIMER_PRESET | R/W | 1D4Ch | The preset value of the timer in DP_IN mode. With sys_clk= 25MHz the Timer can measure up to ~2500 micro seconds. The defaults value is 300us [0x1D4c] |

8.5.124 EDP_CORE_DP_AUX_NACK_FORMAT_P Register (Offset = 2844h) [reset = 20h]

EDP_CORE_DP_AUX_NACK_FORMAT_P is shown in [Figure 8-180](#) and described in [Table 8-370](#).

Return to [Summary Table](#).

Transmit pattern.

Table 8-369.
EDP_CORE_DP_AUX_NACK_FORMAT_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2844h |

Figure 8-180. EDP_CORE_DP_AUX_NACK_FORMAT_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | AUX_HOST_NACK_FORMAT | | | | | | | |
| R-0h | | | | | | | | R/W-20h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-370. EDP_CORE_DP_AUX_NACK_FORMAT_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 7-0 | AUX_HOST_NACK_FOR MAT | R/W | 20h | Nack or defer pattern for transmit [00100000 for defer, 00010000 for nack] |

8.5.125 EDP_CORE_DP_AUX_TX_DATA_P Register (Offset = 2848h) [reset = 0h]

EDP_CORE_DP_AUX_TX_DATA_P is shown in [Figure 8-181](#) and described in [Table 8-372](#).

Return to [Summary Table](#).

AUX Mailbox write data.

Table 8-371. EDP_CORE_DP_AUX_TX_DATA_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2848h |

Figure 8-181. EDP_CORE_DP_AUX_TX_DATA_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | MAILBOX_TX_DATA | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-372. EDP_CORE_DP_AUX_TX_DATA_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9-0 | MAILBOX_TX_DATA | R/W | 0h | TX data byte written to the mailbox. It is written 20 times and directly transferred into TX mailbox. First 8 bits are regular data. When the first data is transferred into mailbox mailbox_tx_data[8] [frame_start] is set to 1. When the last data is transferred into mailbox, mailbox_tx_data[9] [frame_end] is set to 1. |

8.5.126 EDP_CORE_DP_AUX_RX_DATA_P Register (Offset = 284Ch) [reset = 0h]

EDP_CORE_DP_AUX_RX_DATA_P is shown in [Figure 8-182](#) and described in [Table 8-374](#).

Return to [Summary Table](#).

AUX Mailbox read data.

**Table 8-373. EDP_CORE_DP_AUX_RX_DATA_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 284Ch |

Figure 8-182. EDP_CORE_DP_AUX_RX_DATA_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | MAILBOX_RX_DATA | | | | | | | | | |
| R-0h | | | | | | R-0h | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-374. EDP_CORE_DP_AUX_RX_DATA_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9-0 | MAILBOX_RX_DATA | R | 0h | Read data from the mailbox. Whenever read to this register occurs, aux_mailbox_read to RX Mailbox shall be asserted for one clock cycle. |

8.5.127 EDP_CORE_DP_AUX_TX_STATUS_P Register (Offset = 2850h) [reset = 101h]

EDP_CORE_DP_AUX_TX_STATUS_P is shown in [Figure 8-183](#) and described in [Table 8-376](#).

Return to [Summary Table](#).

AUX_TX status.

Table 8-375. EDP_CORE_DP_AUX_TX_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2850h |

Figure 8-183. EDP_CORE_DP_AUX_TX_STATUS_P Register

| | | | | | | | |
|----------------------|--------------|----|----|----|----|-----------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | MAILBOX_TX_FULL | MAILBOX_TX_EMPTY |
| R-0h | | | | | | R-0h | R-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUX_TX_FRAME_ONGOING | AUX_TX_STATE | | | | | | |
| R-0h | R-1h | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-376. EDP_CORE_DP_AUX_TX_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9 | MAILBOX_TX_FULL | R | 0h | AUX Mailbox TX full flag. |
| 8 | MAILBOX_TX_EMPTY | R | 1h | AUX Mailbox TX empty flag. |
| 7 | AUX_TX_FRAME_ONGOING | R | 0h | Frame transmission status. |
| 6-0 | AUX_TX_STATE | R | 1h | Aux_tx state machine register. |

8.5.128 EDP_CORE_DP_AUX_RX_STATUS_P Register (Offset = 2854h) [reset = 01010141h]

EDP_CORE_DP_AUX_RX_STATUS_P is shown in [Figure 8-184](#) and described in [Table 8-378](#).

Return to [Summary Table](#).

AUX_RX status

**Table 8-377. EDP_CORE_DP_AUX_RX_STATUS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2854h |

Figure 8-184. EDP_CORE_DP_AUX_RX_STATUS_P Register

| | | | | | | | |
|-------------------------------|------------------|-----------------------|-------------------|-------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| AUX_RX_DATA_STATE | | | | | | | |
| R-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| AUX_MAIN_RX_STATUS_LAST_EQUAL | RESERVED | | | AUX_RX_HHLL_STATE | | | |
| R-0h | R-0h | | | R-1h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | AUX_RX_PREAMBLE_STATE | | | | | |
| R-0h | | R-1h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MAILBOX_RX_FULL | MAILBOX_RX_EMPTY | AUX_RX_FRAME_ONGOING | AUX_RX_MAIN_STATE | | | | |
| R-0h | R-1h | R-0h | R-1h | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-378. EDP_CORE_DP_AUX_RX_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|---|
| 31-24 | AUX_RX_DATA_STATE | R | 1h | AUX_RX SM state. |
| 23 | AUX_MAIN_RX_STATUS_LAST_EQUAL | R | 0h | The receive transaction is equal to the previous transaction. |
| 22-20 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 19-16 | AUX_RX_HHLL_STATE | R | 1h | AUX_RX hhll state machine register. |
| 15-14 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 13-8 | AUX_RX_PREAMBLE_STATE | R | 1h | AUX_RX preamble state machine register. Used only for debug. |
| 7 | MAILBOX_RX_FULL | R | 0h | AUX Mailbox RX full flag. |
| 6 | MAILBOX_RX_EMPTY | R | 1h | AUX Mailbox RX empty flag. |
| 5 | AUX_RX_FRAME_ONGOING | R | 0h | Frame reception status. |

Table 8-378. EDP_CORE_DP_AUX_RX_STATUS_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 4-0 | AUX_RX_MAIN_STATE | R | 1h | AUX_RX main state machine register. Used only for debug purpose. |

8.5.129 EDP_CORE_DP_AUX_RX_CYCLE_COUNTER_P Register (Offset = 2858h) [reset = 0h]

EDP_CORE_DP_AUX_RX_CYCLE_COUNTER_P is shown in [Figure 8-185](#) and described in [Table 8-380](#).

Return to [Summary Table](#).

AUX RX counter status.

Table 8-379.
EDP_CORE_DP_AUX_RX_CYCLE_COUNTER_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2858h |

Figure 8-185. EDP_CORE_DP_AUX_RX_CYCLE_COUNTER_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----------------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | AUX_RX_CYCLE_COUNTER | | | | | | | | | |
| R-0h | | | | | | R-0h | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-380. EDP_CORE_DP_AUX_RX_CYCLE_COUNTER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 10-0 | AUX_RX_CYCLE_COUNTER | R | 0h | Count system clocks from last change in the auxiliary line input. |

8.5.130 EDP_CORE_DP_AUX_MAIN_STATES_P Register (Offset = 285Ch) [reset = 0h]

EDP_CORE_DP_AUX_MAIN_STATES_P is shown in [Figure 8-186](#) and described in [Table 8-382](#).

Return to [Summary Table](#).

DP_AUX MAIN State Machines status. Used only for debug purpose.

Table 8-381. EDP_CORE_DP_AUX_MAIN_STATES_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 285Ch |

Figure 8-186. EDP_CORE_DP_AUX_MAIN_STATES_P Register

| | | | | | | | |
|----------|----|-------------------------|----|-------------------|----|----------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | AUX_MAIN_EXTERNAL_STATE | | | | AUX_MAIN_TIMER_STATE | |
| R-0h | | R-0h | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | AUX_MAIN_DP_STATE | | AUX_MAIN_RX_STATE | | AUX_MAIN_TX_STATE | |
| R-0h | | R-0h | | R-0h | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 8-382. EDP_CORE_DP_AUX_MAIN_STATES_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-14 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 13-10 | AUX_MAIN_EXTERNAL_STATE | R | 0h | AUX_MAIN external state machine register. |
| 9-8 | AUX_MAIN_TIMER_STATE | R | 0h | AUX_MAIN timer state machine. |
| 7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6-5 | AUX_MAIN_DP_STATE | R | 0h | AUX_MAIN dp state machine. |
| 4-2 | AUX_MAIN_RX_STATE | R | 0h | AUX_MAIN rx state machine. |
| 1-0 | AUX_MAIN_TX_STATE | R | 0h | AUX_MAIN tx state machine. |

8.5.131 EDP_CORE_DP_AUX_MAIN_TIMER_P Register (Offset = 2860h) [reset = 0h]

EDP_CORE_DP_AUX_MAIN_TIMER_P is shown in [Figure 8-187](#) and described in [Table 8-384](#).

Return to [Summary Table](#).

DP_AUX MAIN timer status.

**Table 8-383. EDP_CORE_DP_AUX_MAIN_TIMER_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2860h |

Figure 8-187. EDP_CORE_DP_AUX_MAIN_TIMER_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | AUX_MAIN_TIMER | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-384. EDP_CORE_DP_AUX_MAIN_TIMER_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | AUX_MAIN_TIMER | R | 0h | DP_AUX MAIN timer status. |

8.5.132 EDP_CORE_DP_AUX_AFE_OUT_P Register (Offset = 2864h) [reset = 0h]

EDP_CORE_DP_AUX_AFE_OUT_P is shown in [Figure 8-188](#) and described in [Table 8-386](#).

Return to [Summary Table](#).

Test mode configuration.

Table 8-385. EDP_CORE_DP_AUX_AFE_OUT_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 2864h |

Figure 8-188. EDP_CORE_DP_AUX_AFE_OUT_P Register

| | | | | | | | |
|----------|----|----|----|------------------------|-----------------------|----------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | AUX_HOST_AUX_AFE_PRECH | AUX_HOST_AUX_AFE_DATA | AUX_HOST_AUX_AFE_CLK | AUX_HOST_AFE_IF_TEST_EN |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-386. EDP_CORE_DP_AUX_AFE_OUT_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | AUX_HOST_AUX_AFE_PRECH | R/W | 0h | Drive the aux_data_prech output to the AFE when aux_host_afe_if_test_en [bit 0] is set. |
| 2 | AUX_HOST_AUX_AFE_DATA | R/W | 0h | Drive the aux_data_out output to the AFE when aux_host_afe_if_test_en [bit 0] is set. |
| 1 | AUX_HOST_AUX_AFE_CLK | R/W | 0h | Drive the aux_clk_out output to the AFE when aux_host_afe_if_test_en [bit 0] is set. |
| 0 | AUX_HOST_AFE_IF_TEST_EN | R/W | 0h | TESTER mode enable. Give the TESTER direct interface to the AFE_AUX. |

8.5.133 EDP_CORE_CRYPT0_HDCP_REVISION_P Register (Offset = 4000h) [reset = 0h]

EDP_CORE_CRYPT0_HDCP_REVISION_P is shown in [Figure 8-189](#) and described in [Table 8-388](#).

Return to [Summary Table](#).

Contains the revision of the internal HDCP 1.4 and 2.2 module.

Table 8-387.
EDP_CORE_CRYPT0_HDCP_REVISION_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4000h |

Figure 8-189. EDP_CORE_CRYPT0_HDCP_REVISION_P Register

| | | | | | | | |
|--------------------|----|----|----|--------------------|----|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | HDCP_Cryp_REV | | | |
| R-0h | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HDCP_Cryp_REV | | | | CRYPTO_HDCP_22_REV | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CRYPTO_HDCP_22_REV | | | | | | CRYPTO_HDCP_14_REV | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO_HDCP_14_REV | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-388. EDP_CORE_CRYPT0_HDCP_REVISION_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 29-20 | HDCP_Cryp_REV | R | 0h | Revision of the HDCP Crypto block. |
| 19-10 | CRYPTO_HDCP_22_REV | R | 0h | Revision of the HDCP Crypto 2.2 block. |
| 9-0 | CRYPTO_HDCP_14_REV | R | 0h | Revision of the HDCP Crypto 1.4 block. |

8.5.134 EDP_CORE_HDCP_CRYPT0_CONFIG_P Register (Offset = 4004h) [reset = 0h]

EDP_CORE_HDCP_CRYPT0_CONFIG_P is shown in [Figure 8-190](#) and described in [Table 8-390](#).

Return to [Summary Table](#).

Contains global configuration information for the HDCP Crypto module.

Table 8-389.
EDP_CORE_HDCP_CRYPT0_CONFIG_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4004h |

Figure 8-190. EDP_CORE_HDCP_CRYPT0_CONFIG_P Register

| | | | | | | | |
|----------|----|----|----|---------------|----------------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | CRYPTO_SW_RST | CRYPTO_HDCP_FUNCTION | | |
| R-0h | | | | R/W-0h | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-390. EDP_CORE_HDCP_CRYPT0_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | CRYPTO_SW_RST | R/W | 0h | Software reset for the Crypto module. |
| 2-0 | CRYPTO_HDCP_FUNC TION | R/W | 0h | Enables a version of the Crypto function: 0x 0 - HDCP 1.4 0x 1 - HDCP 2.2 Other - Reserved |

8.5.135 EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P Register (Offset = 4008h) [reset = 0h]

EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P is shown in [Figure 8-191](#) and described in [Table 8-392](#).

Return to [Summary Table](#).

Contains the status of the HDCP interrupt sources. These interrupts are used by firmware and not directly visible to the Host processor.

Table 8-391.
EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4008h |

Figure 8-191. EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P Register

| | | | | | | | |
|----------|----|----|----|----|------------------------|----------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | CRYPTO14_PR NM_DONE | CRYPTO14_K M_DONE | AES_32_DONE |
| R-0h | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | APB_SLVERR | SHA256_NEXT _MESSAGE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-392. EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 10 | CRYPTO14_PRNM_DON E | R | 0h | LFSR and block output finished calculation. Active HIGH. Clear on read. |
| 9 | CRYPTO14_KM_DONE | R | 0h | Done reading/calculating Km. Active HIGH. Clear on read. |
| 8 | AES_32_DONE | R | 0h | Asserted when the rising edge of the AES-32 done output is detected. Active HIGH. Clear on read. |
| 7-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. Active HIGH. Clear on read. |

Table 8-392. EDP_CORE_CRYPT0_INTERRUPT_SOURCE_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 1 | APB_SLVERR | R | 0h | APB slave error. Asserted when APB address is out of address range. Active HIGH. Clear on read. |
| 0 | SHA256_NEXT_MESSAGE | R | 0h | Asserted when the rising edge of the SHA256 done output is detected. Active HIGH. Clear on read. |

8.5.136 EDP_CORE_CRYPT0_INTERRUPT_MASK_P Register (Offset = 400Ch) [reset = 703h]

EDP_CORE_CRYPT0_INTERRUPT_MASK_P is shown in [Figure 8-192](#) and described in [Table 8-394](#).

Return to [Summary Table](#).

Contains the mask vector of the HDCP interrupt sources.

Table 8-393.
EDP_CORE_CRYPT0_INTERRUPT_MASK_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 400Ch |

Figure 8-192. EDP_CORE_CRYPT0_INTERRUPT_MASK_P Register

| | | | | | | | |
|----------|----|----|----|----|---------------------------------|-------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | CRYPTO14_PR NM_DONE_MA SK | CRYPTO14_K M_DONE_MAS K | AES_32_DONE _MASK |
| R-0h | | | | | R/W-1h | R/W-1h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | APB_SLVERR_ MASK | SHA256_NEXT _MESSAGE_M ASK |
| R-0h | | | | | | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-394. EDP_CORE_CRYPT0_INTERRUPT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 10 | CRYPTO14_PRNM_DON E_MASK | R/W | 1h | Set to 1 to mask the crypto14_prnm_done interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 9 | CRYPTO14_KM_DONE_ MASK | R/W | 1h | Set to 1 to mask the crypto14_km_done interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 8 | AES_32_DONE_MASK | R/W | 1h | Set to 1 to mask the AES32_done interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |

Table 8-394. EDP_CORE_CRYPT0_INTERRUPT_MASK_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|--|
| 7-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | APB_SLVERR_MASK | R/W | 1h | Set to 1 for the apb_slvrr interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 0 | SHA256_NEXT_MESSAGE_MASK | R/W | 1h | Set to 1 to mask the SHA256_done interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.5.137 EDP_CORE_CRYPT022_CONFIG_P Register (Offset = 4018h) [reset = 0h]

EDP_CORE_CRYPT022_CONFIG_P is shown in [Figure 8-193](#) and described in [Table 8-396](#).

Return to [Summary Table](#).

Contains global configuration information for the HDCP 2.2 Crypto module

**Table 8-395. EDP_CORE_CRYPT022_CONFIG_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4018h |

Figure 8-193. EDP_CORE_CRYPT022_CONFIG_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SHA_256_STA RT |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-396. EDP_CORE_CRYPT022_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | SHA_256_START | R/W | 0h | Set to 1 for Sha-256 start. |

8.5.138 EDP_CORE_CRYPT022_STATUS_P Register (Offset = 401Ch) [reset = 0h]

EDP_CORE_CRYPT022_STATUS_P is shown in [Figure 8-194](#) and described in [Table 8-398](#).

Return to [Summary Table](#).

Crypto 2.2 global status register.

Table 8-397. EDP_CORE_CRYPT022_STATUS_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 401Ch |

Figure 8-194. EDP_CORE_CRYPT022_STATUS_P Register

| | | | | | | | |
|--------------|----|----|----|---------------|----|----------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | AES_32_DONE_ST | SHA256_NEXT_MESSAGE_ST |
| R-0h | | | | | | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_STATE | | | | SHA_256_STATE | | | |
| R-0h | | | | R-0h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-398. EDP_CORE_CRYPT022_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 9 | AES_32_DONE_ST | R | 0h | Asserted when the rising edge of the AES-32 done output is detected. |
| 8 | SHA256_NEXT_MESSAGE_ST | R | 0h | Asserted when the SHA-256 module is ready to receive the next message. |
| 7-4 | AES_32_STATE | R | 0h | AES-32 current state. |
| 3-0 | SHA_256_STATE | R | 0h | SHA-256 current state. |

8.5.139 EDP_CORE_SHA_256_DATA_IN_P Register (Offset = 403Ch) [reset = 0h]

EDP_CORE_SHA_256_DATA_IN_P is shown in [Figure 8-195](#) and described in [Table 8-400](#).

Return to [Summary Table](#).

Holds 32-bit input data word of the SHA-256 module.

**Table 8-399. EDP_CORE_SHA_256_DATA_IN_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 403Ch |

Figure 8-195. EDP_CORE_SHA_256_DATA_IN_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_IN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-400. EDP_CORE_SHA_256_DATA_IN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-0 | SHA_256_DATA_IN | R/W | 0h | Holds the 32-bit input data word of the SHA-256 module. |

8.5.140 EDP_CORE_SHA_256_DATA_OUT_0_P Register (Offset = 4050h) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_0_P is shown in [Figure 8-196](#) and described in [Table 8-402](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 1' dw

Table 8-401. EDP_CORE_SHA_256_DATA_OUT_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4050h |

Figure 8-196. EDP_CORE_SHA_256_DATA_OUT_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-402. EDP_CORE_SHA_256_DATA_OUT_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-0 | SHA_256_DATA_OUT_0 | R | 0h | Holds the least significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.141 EDP_CORE_SHA_256_DATA_OUT_1_P Register (Offset = 4054h) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_1_P is shown in [Figure 8-197](#) and described in [Table 8-404](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 2' dw

**Table 8-403. EDP_CORE_SHA_256_DATA_OUT_1_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4054h |

Figure 8-197. EDP_CORE_SHA_256_DATA_OUT_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-404. EDP_CORE_SHA_256_DATA_OUT_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-0 | SHA_256_DATA_OUT_1 | R | 0h | Holds the next significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.142 EDP_CORE_SHA_256_DATA_OUT_2_P Register (Offset = 4058h) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_2_P is shown in [Figure 8-198](#) and described in [Table 8-406](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 3' dw

Table 8-405. EDP_CORE_SHA_256_DATA_OUT_2_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4058h |

Figure 8-198. EDP_CORE_SHA_256_DATA_OUT_2_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-406. EDP_CORE_SHA_256_DATA_OUT_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-0 | SHA_256_DATA_OUT_2 | R | 0h | Holds the next significant 32-bits word of the 256-bits output data word of the SHA-256 module |

8.5.143 EDP_CORE_SHA_256_DATA_OUT_3_P Register (Offset = 405Ch) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_3_P is shown in [Figure 8-199](#) and described in [Table 8-408](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 4' dw

**Table 8-407. EDP_CORE_SHA_256_DATA_OUT_3_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 405Ch |

Figure 8-199. EDP_CORE_SHA_256_DATA_OUT_3_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-408. EDP_CORE_SHA_256_DATA_OUT_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-0 | SHA_256_DATA_OUT_3 | R | 0h | Holds the next significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.144 EDP_CORE_SHA_256_DATA_OUT_4_P Register (Offset = 4060h) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_4_P is shown in [Figure 8-200](#) and described in [Table 8-410](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 5' dw

Table 8-409. EDP_CORE_SHA_256_DATA_OUT_4_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4060h |

Figure 8-200. EDP_CORE_SHA_256_DATA_OUT_4_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-410. EDP_CORE_SHA_256_DATA_OUT_4_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-0 | SHA_256_DATA_OUT_4 | R | 0h | Holds the next significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.145 EDP_CORE_SHA_256_DATA_OUT_5_P Register (Offset = 4064h) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_5_P is shown in [Figure 8-201](#) and described in [Table 8-412](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 6' dw

**Table 8-411. EDP_CORE_SHA_256_DATA_OUT_5_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4064h |

Figure 8-201. EDP_CORE_SHA_256_DATA_OUT_5_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-412. EDP_CORE_SHA_256_DATA_OUT_5_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-0 | SHA_256_DATA_OUT_5 | R | 0h | Holds the next significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.146 EDP_CORE_SHA_256_DATA_OUT_6_P Register (Offset = 4068h) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_6_P is shown in [Figure 8-202](#) and described in [Table 8-414](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 7' dw

Table 8-413. EDP_CORE_SHA_256_DATA_OUT_6_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4068h |

Figure 8-202. EDP_CORE_SHA_256_DATA_OUT_6_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-414. EDP_CORE_SHA_256_DATA_OUT_6_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-0 | SHA_256_DATA_OUT_6 | R | 0h | Holds the next significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.147 EDP_CORE_SHA_256_DATA_OUT_7_P Register (Offset = 406Ch) [reset = 0h]

EDP_CORE_SHA_256_DATA_OUT_7_P is shown in [Figure 8-203](#) and described in [Table 8-416](#).

Return to [Summary Table](#).

Result of operation SHA-256 - 8' dw

**Table 8-415. EDP_CORE_SHA_256_DATA_OUT_7_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 406Ch |

Figure 8-203. EDP_CORE_SHA_256_DATA_OUT_7_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA_256_DATA_OUT_7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-416. EDP_CORE_SHA_256_DATA_OUT_7_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 31-0 | SHA_256_DATA_OUT_7 | R | 0h | Holds the most significant 32-bits word of the 256-bits output data word of the SHA-256 module. |

8.5.148 EDP_CORE_AES_32_KEY_0_P Register (Offset = 4070h) [reset = 0h]

EDP_CORE_AES_32_KEY_0_P is shown in [Figure 8-204](#) and described in [Table 8-418](#).

Return to [Summary Table](#).

Input key word of the AES-32 module - 1' dw

Table 8-417. EDP_CORE_AES_32_KEY_0_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4070h |

Figure 8-204. EDP_CORE_AES_32_KEY_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_KEY_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-418. EDP_CORE_AES_32_KEY_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-0 | AES_32_KEY_0 | R/W | 0h | Holds the least significant 32-bits word of the 128-bits input key word of the AES-32 module. |

8.5.149 EDP_CORE_AES_32_KEY_1_P Register (Offset = 4074h) [reset = 0h]

EDP_CORE_AES_32_KEY_1_P is shown in [Figure 8-205](#) and described in [Table 8-420](#).

Return to [Summary Table](#).

Input key word of the AES-32 module - 2' dw

**Table 8-419. EDP_CORE_AES_32_KEY_1_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4074h |

Figure 8-205. EDP_CORE_AES_32_KEY_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_KEY_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-420. EDP_CORE_AES_32_KEY_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-0 | AES_32_KEY_1 | R/W | 0h | Holds the next significant 32-bits word of the 128-bits input key word of the AES-32 module. |

8.5.150 EDP_CORE_AES_32_KEY_2_P Register (Offset = 4078h) [reset = 0h]

EDP_CORE_AES_32_KEY_2_P is shown in [Figure 8-206](#) and described in [Table 8-422](#).

Return to [Summary Table](#).

Input key word of the AES-32 module - 3' dw

**Table 8-421. EDP_CORE_AES_32_KEY_2_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4078h |

Figure 8-206. EDP_CORE_AES_32_KEY_2_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_KEY_2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-422. EDP_CORE_AES_32_KEY_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-0 | AES_32_KEY_2 | R/W | 0h | Holds the next significant 32-bits word of the 128-bits input key word of the AES-32 module. |

8.5.151 EDP_CORE_AES_32_KEY_3_P Register (Offset = 407Ch) [reset = 0h]

EDP_CORE_AES_32_KEY_3_P is shown in [Figure 8-207](#) and described in [Table 8-424](#).

Return to [Summary Table](#).

Input key word of the AES-32 module - 4' dw

**Table 8-423. EDP_CORE_AES_32_KEY_3_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 407Ch |

Figure 8-207. EDP_CORE_AES_32_KEY_3_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_KEY_3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-424. EDP_CORE_AES_32_KEY_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-0 | AES_32_KEY_3 | R/W | 0h | Holds the most significant 32-bits word of the 128-bits input key word of the AES-32 module. |

8.5.152 EDP_CORE_AES_32_DATA_IN_P Register (Offset = 4080h) [reset = 0h]

EDP_CORE_AES_32_DATA_IN_P is shown in [Figure 8-208](#) and described in [Table 8-426](#).

Return to [Summary Table](#).

Input data word to the AES-32 module

Table 8-425. EDP_CORE_AES_32_DATA_IN_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4080h |

Figure 8-208. EDP_CORE_AES_32_DATA_IN_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_DATA_IN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-426. EDP_CORE_AES_32_DATA_IN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-0 | AES_32_DATA_IN | R/W | 0h | Holds the input data word to the AES-32 module. |

8.5.153 EDP_CORE_AES_32_DATA_OUT_0_P Register (Offset = 4084h) [reset = 0h]

EDP_CORE_AES_32_DATA_OUT_0_P is shown in [Figure 8-209](#) and described in [Table 8-428](#).

Return to [Summary Table](#).

AES-32 module - 128-bits output data word - 1' dw

**Table 8-427. EDP_CORE_AES_32_DATA_OUT_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4084h |

Figure 8-209. EDP_CORE_AES_32_DATA_OUT_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_DATA_OUT_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-428. EDP_CORE_AES_32_DATA_OUT_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|---|
| 31-0 | AES_32_DATA_OUT_0 | R | 0h | Holds the least significant 32-bits word of the 128-bits output data word of the AES-32 module. |

8.5.154 EDP_CORE_AES_32_DATA_OUT_1_P Register (Offset = 4088h) [reset = 0h]

EDP_CORE_AES_32_DATA_OUT_1_P is shown in [Figure 8-210](#) and described in [Table 8-430](#).

Return to [Summary Table](#).

AES-32 module - 128-bits output data word - 2' dw

Table 8-429. EDP_CORE_AES_32_DATA_OUT_1_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4088h |

Figure 8-210. EDP_CORE_AES_32_DATA_OUT_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_DATA_OUT_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-430. EDP_CORE_AES_32_DATA_OUT_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-0 | AES_32_DATA_OUT_1 | R | 0h | Holds the next significant 32-bits word of the 128-bits output data word of the AES-32 module. |

8.5.155 EDP_CORE_AES_32_DATA_OUT_2_P Register (Offset = 408Ch) [reset = 0h]

EDP_CORE_AES_32_DATA_OUT_2_P is shown in [Figure 8-211](#) and described in [Table 8-432](#).

Return to [Summary Table](#).

AES-32 module - 128-bits output data word - 3' dw

**Table 8-431. EDP_CORE_AES_32_DATA_OUT_2_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 408Ch |

Figure 8-211. EDP_CORE_AES_32_DATA_OUT_2_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_DATA_OUT_2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-432. EDP_CORE_AES_32_DATA_OUT_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-0 | AES_32_DATA_OUT_2 | R | 0h | Holds the next significant 32-bits word of the 128-bits output data word of the AES-32 module. |

8.5.156 EDP_CORE_AES_32_DATA_OUT_3_P Register (Offset = 4090h) [reset = 0h]

EDP_CORE_AES_32_DATA_OUT_3_P is shown in [Figure 8-212](#) and described in [Table 8-434](#).

Return to [Summary Table](#).

AES-32 module - 128-bits output data word - 4' dw

Table 8-433. EDP_CORE_AES_32_DATA_OUT_3_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 4090h |

Figure 8-212. EDP_CORE_AES_32_DATA_OUT_3_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AES_32_DATA_OUT_3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-434. EDP_CORE_AES_32_DATA_OUT_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-0 | AES_32_DATA_OUT_3 | R | 0h | Holds the most significant 32-bits word of the 128-bits output data word of the AES-32 module. |

8.5.157 EDP_CORE_CRYPT014_CONFIG_P Register (Offset = 40A0h) [reset = 0h]

EDP_CORE_CRYPT014_CONFIG_P is shown in [Figure 8-213](#) and described in [Table 8-436](#).

Return to [Summary Table](#).

Contains global configuration information for the HDCP 1.4 Crypto module

Table 8-435. EDP_CORE_CRYPT014_CONFIG_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40A0h |

Figure 8-213. EDP_CORE_CRYPT014_CONFIG_P Register

| | | | | | | | |
|----------|--------------------|---------------|-------------|-----------------------|-----------------|---------|-----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | HDCP_AUTHENTICATED | HDCP_REPEATER | START_REKEY | CRYPTO_START_FREE_RUN | START_BLOCK_SEQ | GET_KSV | VALID_KSV |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-436. EDP_CORE_CRYPT014_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 6 | HDCP_AUTHENTICATED | R/W | 0h | Authenticated finished. |
| 5 | HDCP_REPEATER | R/W | 0h | Repeater bit : 0: for the receiver, 1: for the repeater |
| 4 | START_REKEY | R/W | 0h | Crypto 1.4 command to start hdcpRekeyCipher |
| 3 | CRYPTO_START_FREE_RUN | R/W | 0h | Crypto 1.4 command to start free running enable for operation hdcpRngCipher |
| 2 | START_BLOCK_SEQ | R/W | 0h | Crypto 1.4 command to start LFSR calculation |
| 1 | GET_KSV | R/W | 0h | Read it's own KSV enable bit.'0' reading not allowed'1' start reading. |
| 0 | VALID_KSV | R/W | 0h | Enable for Km calculation. When high, start calculating Km. Indicates a good moment for ri_out sampling. |

8.5.158 EDP_CORE_CRYPT014_STATUS_P Register (Offset = 40A4h) [reset = 0h]

EDP_CORE_CRYPT014_STATUS_P is shown in [Figure 8-214](#) and described in [Table 8-438](#).

Return to [Summary Table](#).

Contains global status information for the HDCP 1.4 Crypto module

Table 8-437. EDP_CORE_CRYPT014_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40A4h |

Figure 8-214. EDP_CORE_CRYPT014_STATUS_P Register

| | | | | | | | |
|----------|----|-----------|----------------|------------|------------------|-------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | CRYPTO14_STATE | | SHA1_V_READ Y | SHA1_NEXT_M SG | RESERVED |
| R-0h | | | R-0h | | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | SHA1_STATE | | | RESERVED |
| R-0h | | | | R-0h | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | DKS_STATE | | | PRNM_DONE | RESERVED | KM_DONE |
| R-0h | | R-0h | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-438. EDP_CORE_CRYPT014_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-21 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 20-19 | CRYPTO14_STATE | R | 0h | Crypto operation SM state: Possible values: 00- HDCP_RNG_CIPHER 01 - HDCP_BLOCK_CIPHER 10 - HDCP_STREAM_CIPHER 11 - HDCP_REKEY_CIPHER |
| 18 | SHA1_V_READY | R | 0h | Indication that V value from SHA-1 CRYPTO14_SHA1_V_VALUE_4 is ready. |
| 17 | SHA1_NEXT_MSG | R | 0h | Request for the next message block. When set high, CRYPTO14_SHA1_MSG_DATA_0-15 registers shall be written. |
| 16-12 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |

Table 8-438. EDP_CORE_CRYPT014_STATUS_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 11-9 | SHA1_STATE | R | 0h | Current state for Crypto 1.4 SHA-1 FSM. Used for debug purpose. Possible values: 000 - IDLE 001 - PREPARE 010 - CALCULATE 011 - RESULT 100 - BLOCK_WAIT |
| 8-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 5-3 | DKS_STATE | R | 0h | Crypto 1.4 DKS current state. Used for debug purpose. Possible values: 000 - HDCP_IDLE_KSV 010 - HDCP_IDLE 100 - HDCP_PRECALC 101 - HDCP_POSTCALC 110 - HDCP_CALC 111 - HDCP_READY |
| 2 | PRNM_DONE | R | 0h | LFSR and block output finished calculation. |
| 1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | KM_DONE | R | 0h | Done reading/calculating Km. Used as interrupt event. |

8.5.159 EDP_CORE_CRYPT014_PRNM_OUT_P Register (Offset = 40A8h) [reset = 0h]

EDP_CORE_CRYPT014_PRNM_OUT_P is shown in [Figure 8-215](#) and described in [Table 8-440](#).

Return to [Summary Table](#).

Contains 24-bit pseudo random data

Table 8-439. EDP_CORE_CRYPT014_PRNM_OUT_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40A8h |

Figure 8-215. EDP_CORE_CRYPT014_PRNM_OUT_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | PRNM_OUT | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-440. EDP_CORE_CRYPT014_PRNM_OUT_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 23-0 | PRNM_OUT | R | 0h | 24-bit pseudo-random data. |

8.5.160 EDP_CORE_CRYPT014_KM_0_P Register (Offset = 40ACh) [reset = 0h]

EDP_CORE_CRYPT014_KM_0_P is shown in [Figure 8-216](#) and described in [Table 8-442](#).

Return to [Summary Table](#).

Contains the first word of the Km value

**Table 8-441. EDP_CORE_CRYPT014_KM_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40ACh |

Figure 8-216. EDP_CORE_CRYPT014_KM_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_KM_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-442. EDP_CORE_CRYPT014_KM_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---------------------------------------|
| 31-0 | CRYPTO14_KM_0 | R | 0h | Holds the first word of the Km value. |

8.5.161 EDP_CORE_CRYPT014_KM_1_P Register (Offset = 40B0h) [reset = 0h]

EDP_CORE_CRYPT014_KM_1_P is shown in [Figure 8-217](#) and described in [Table 8-444](#).

Return to [Summary Table](#).

Contains the most significant 3 bytes of the Km value

Table 8-443. EDP_CORE_CRYPT014_KM_1_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40B0h |

Figure 8-217. EDP_CORE_CRYPT014_KM_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRYPTO14_KM_1 | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-444. EDP_CORE_CRYPT014_KM_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 23-0 | CRYPTO14_KM_1 | R | 0h | Holds the most significant 3 bytes of the Km value. |

8.5.162 EDP_CORE_CRYPT014_AN_0_P Register (Offset = 40B4h) [reset = 0h]

EDP_CORE_CRYPT014_AN_0_P is shown in [Figure 8-218](#) and described in [Table 8-446](#).

Return to [Summary Table](#).

First word of An value generated by hdcpRngCipher operation.

**Table 8-445. EDP_CORE_CRYPT014_AN_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40B4h |

Figure 8-218. EDP_CORE_CRYPT014_AN_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_AN_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-446. EDP_CORE_CRYPT014_AN_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-0 | CRYPTO14_AN_0 | R/W | 0h | Holds the first 4 bytes of the An value. |

8.5.163 EDP_CORE_CRYPT014_AN_1_P Register (Offset = 40B8h) [reset = 0h]

EDP_CORE_CRYPT014_AN_1_P is shown in [Figure 8-219](#) and described in [Table 8-448](#).

Return to [Summary Table](#).

Second word of An value generated by hdcpRngCipher operation

Table 8-447. EDP_CORE_CRYPT014_AN_1_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40B8h |

Figure 8-219. EDP_CORE_CRYPT014_AN_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_AN_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-448. EDP_CORE_CRYPT014_AN_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-0 | CRYPTO14_AN_1 | R/W | 0h | Holds the most significant 4 bytes of the An value. |

8.5.164 EDP_CORE_CRYPT014_YOUR_KSV_0_P Register (Offset = 40BCh) [reset = 0h]

EDP_CORE_CRYPT014_YOUR_KSV_0_P is shown in [Figure 8-220](#) and described in [Table 8-450](#).

Return to [Summary Table](#).

First 32 bits of the KSV from the other HDCP device

Table 8-449.
EDP_CORE_CRYPT014_YOUR_KSV_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40BCh |

Figure 8-220. EDP_CORE_CRYPT014_YOUR_KSV_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_YOUR_KSV_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-450. EDP_CORE_CRYPT014_YOUR_KSV_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-0 | CRYPTO14_YOUR_KSV_0 | R/W | 0h | Holds the first 32 bits of the KSV from the other HDCP device. |

8.5.165 EDP_CORE_CRYPT014_YOUR_KSV_1_P Register (Offset = 40C0h) [reset = 0h]

EDP_CORE_CRYPT014_YOUR_KSV_1_P is shown in [Figure 8-221](#) and described in [Table 8-452](#).

Return to [Summary Table](#).

Last byte of the KSV from other HDCP device

Table 8-451.
EDP_CORE_CRYPT014_YOUR_KSV_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40C0h |

Figure 8-221. EDP_CORE_CRYPT014_YOUR_KSV_1_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRYPTO14_YOUR_KSV_1 | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-452. EDP_CORE_CRYPT014_YOUR_KSV_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 7-0 | CRYPTO14_YOUR_KSV_1 | R/W | 0h | Holds the last byte of the KSV from other HDCP device |

8.5.166 EDP_CORE_CRYPT014_MI_0_P Register (Offset = 40C4h) [reset = 0h]

EDP_CORE_CRYPT014_MI_0_P is shown in [Figure 8-222](#) and described in [Table 8-454](#).

Return to [Summary Table](#).

Mi value - 1' dw

**Table 8-453. EDP_CORE_CRYPT014_MI_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40C4h |

Figure 8-222. EDP_CORE_CRYPT014_MI_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_MI_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-454. EDP_CORE_CRYPT014_MI_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | CRYPTO14_MI_0 | R | 0h | Mi value first 32 bits |

8.5.167 EDP_CORE_CRYPT014_MI_1_P Register (Offset = 40C8h) [reset = 0h]

EDP_CORE_CRYPT014_MI_1_P is shown in [Figure 8-223](#) and described in [Table 8-456](#).

Return to [Summary Table](#).

Mi value - 2' dw

Table 8-455. EDP_CORE_CRYPT014_MI_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40C8h |

Figure 8-223. EDP_CORE_CRYPT014_MI_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_MI_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-456. EDP_CORE_CRYPT014_MI_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------------------|
| 31-0 | CRYPTO14_MI_1 | R | 0h | Mi value second 32 bits |

8.5.168 EDP_CORE_CRYPT014_TI_0_P Register (Offset = 40CCh) [reset = 0h]

EDP_CORE_CRYPT014_TI_0_P is shown in [Figure 8-224](#) and described in [Table 8-458](#).

Return to [Summary Table](#).

Ti value

**Table 8-457. EDP_CORE_CRYPT014_TI_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40CCh |

Figure 8-224. EDP_CORE_CRYPT014_TI_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRYPTO14_TI_0 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-458. EDP_CORE_CRYPT014_TI_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | CRYPTO14_TI_0 | R | 0h | Ti value |

8.5.169 EDP_CORE_CRYPT014_KI_0_P Register (Offset = 40D0h) [reset = 0h]

EDP_CORE_CRYPT014_KI_0_P is shown in [Figure 8-225](#) and described in [Table 8-460](#).

Return to [Summary Table](#).

First 32 bits of the Ki frame key from this HDCP device

Table 8-459. EDP_CORE_CRYPT014_KI_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40D0h |

Figure 8-225. EDP_CORE_CRYPT014_KI_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRYPTO14_KI_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-460. EDP_CORE_CRYPT014_KI_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-0 | CRYPTO14_KI_0 | R | 0h | Holds the first 32 bits of the Ki frame key from this HDCP device. |

8.5.170 EDP_CORE_CRYPT014_KI_1_P Register (Offset = 40D4h) [reset = 0h]

EDP_CORE_CRYPT014_KI_1_P is shown in [Figure 8-226](#) and described in [Table 8-462](#).

Return to [Summary Table](#).

Last 3 bytes of the Ki frame key from this HDCP device.

Table 8-461. EDP_CORE_CRYPT014_KI_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40D4h |

Figure 8-226. EDP_CORE_CRYPT014_KI_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRYPTO14_KI_1 | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-462. EDP_CORE_CRYPT014_KI_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 23-0 | CRYPTO14_KI_1 | R | 0h | Holds the last 3 bytes of the Ki frame key from this HDCP device. |

8.5.171 EDP_CORE_CRYPT014_BLOCKS_NUM_P Register (Offset = 40D8h) [reset = 0h]

EDP_CORE_CRYPT014_BLOCKS_NUM_P is shown in [Figure 8-227](#) and described in [Table 8-464](#).

Return to [Summary Table](#).

This register defines number of iterations for SHA-1 calculations

Table 8-463.
EDP_CORE_CRYPT014_BLOCKS_NUM_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40D8h |

Figure 8-227. EDP_CORE_CRYPT014_BLOCKS_NUM_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BLOCKS_NUM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-464. EDP_CORE_CRYPT014_BLOCKS_NUM_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | BLOCKS_NUM | R/W | 0h | Number of iterations for SHA-1 calculation. |

8.5.172 EDP_CORE_CRYPT014_KEY_MEM_DATA_0_P Register (Offset = 40DCh) [reset = 0h]

EDP_CORE_CRYPT014_KEY_MEM_DATA_0_P is shown in [Figure 8-228](#) and described in [Table 8-466](#).

Return to [Summary Table](#).

Key memory control register. Writing data to this register transfers data to the key RAM. This is input for DKS block. First 32 bits

Table 8-465.
EDP_CORE_CRYPT014_KEY_MEM_DATA_0_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40DCh |

Figure 8-228. EDP_CORE_CRYPT014_KEY_MEM_DATA_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| KEY_MEM_DATA_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-466. EDP_CORE_CRYPT014_KEY_MEM_DATA_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-0 | KEY_MEM_DATA_0 | R/W | 0h | Output data from keys RAM. Input for DKS block. First 32 bits. |

8.5.173 EDP_CORE_CRYPT014_KEY_MEM_DATA_1_P Register (Offset = 40E0h) [reset = 0h]

EDP_CORE_CRYPT014_KEY_MEM_DATA_1_P is shown in [Figure 8-229](#) and described in [Table 8-468](#).

Return to [Summary Table](#).

Key memory control register. Writing data to this register transfers data to the key RAM. When data is written to this register, pulse key_mem_vld shall be also generated to the core_clk clock domain, as indication of new key_mem_data. This is input for DKS block. Last 3 bytes

Table 8-467.
EDP_CORE_CRYPT014_KEY_MEM_DATA_1_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40E0h |

Figure 8-229. EDP_CORE_CRYPT014_KEY_MEM_DATA_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | KEY_MEM_DATA_1 | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-468. EDP_CORE_CRYPT014_KEY_MEM_DATA_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 23-0 | KEY_MEM_DATA_1 | R/W | 0h | Output data from keys RAM. Input for DKS block. Last 3 bytes. |

8.5.174 EDP_CORE_CRYPT014_SHA1_MSG_DATA_P Register (Offset = 40E4h) [reset = 0h]

EDP_CORE_CRYPT014_SHA1_MSG_DATA_P is shown in [Figure 8-230](#) and described in [Table 8-470](#).

Return to [Summary Table](#).

SHA1 message control register. 32-bit word for SHA-1 message. Input for SHA-1 block. Writing data to this register transfers data to the SHA-1 block. Write to this register shall be repeated 16 times.

Table 8-469.
EDP_CORE_CRYPT014_SHA1_MSG_DATA_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40E4h |

Figure 8-230. EDP_CORE_CRYPT014_SHA1_MSG_DATA_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SHA1_MSG_DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-470. EDP_CORE_CRYPT014_SHA1_MSG_DATA_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-0 | SHA1_MSG_DATA | R/W | 0h | 32-bit word for SHA-1 message. Input for SHA-1 block. |

8.5.175 EDP_CORE_CRYPT014_SHA1_V_VALUE_0_P Register (Offset = 40E8h) [reset = 67452301h]

EDP_CORE_CRYPT014_SHA1_V_VALUE_0_P is shown in [Figure 8-231](#) and described in [Table 8-472](#).

Return to [Summary Table](#).

SHA1 message status register. First 32-bit word for SHA-1 calculation. Output from SHA-1 block

Table 8-471.
EDP_CORE_CRYPT014_SHA1_V_VALUE_0_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40E8h |

Figure 8-231. EDP_CORE_CRYPT014_SHA1_V_VALUE_0_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| V_VALUE_0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-67452301h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-472. EDP_CORE_CRYPT014_SHA1_V_VALUE_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-----------|--|
| 31-0 | V_VALUE_0 | R | 67452301h | First 32-bit word for SHA-1 calculation value. Output from SHA-1 block. |

8.5.176 EDP_CORE_CRYPT014_SHA1_V_VALUE_1_P Register (Offset = 40ECh) [reset = EFCDAB89h]

EDP_CORE_CRYPT014_SHA1_V_VALUE_1_P is shown in [Figure 8-232](#) and described in [Table 8-474](#).

Return to [Summary Table](#).

SHA1 message status register. Second 32-bit word for SHA-1 calculation. Output from SHA-1 block

Table 8-473.
EDP_CORE_CRYPT014_SHA1_V_VALUE_1_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40ECh |

Figure 8-232. EDP_CORE_CRYPT014_SHA1_V_VALUE_1_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| V_VALUE_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-EFCDAB89h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-474. EDP_CORE_CRYPT014_SHA1_V_VALUE_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-----------|---|
| 31-0 | V_VALUE_1 | R | EFCDAB89h | Second 32-bit word for SHA-1 calculation value. Output from SHA-1 block. |

8.5.177 EDP_CORE_CRYPT014_SHA1_V_VALUE_2_P Register (Offset = 40F0h) [reset = 98BADCFEh]

EDP_CORE_CRYPT014_SHA1_V_VALUE_2_P is shown in [Figure 8-233](#) and described in [Table 8-476](#).

Return to [Summary Table](#).

SHA1 message status register. Third 32-bit word for SHA-1 calculation. Output from SHA-1 block

Table 8-475.
EDP_CORE_CRYPT014_SHA1_V_VALUE_2_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40F0h |

Figure 8-233. EDP_CORE_CRYPT014_SHA1_V_VALUE_2_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| V_VALUE_2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-98BADCFEh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-476. EDP_CORE_CRYPT014_SHA1_V_VALUE_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|---------------|--|
| 31-0 | V_VALUE_2 | R | 98BADCFE h | Third 32-bit word for SHA-1 calculation value. Output from SHA-1 block. |

8.5.178 EDP_CORE_CRYPT014_SHA1_V_VALUE_3_P Register (Offset = 40F4h) [reset = 10325476h]

EDP_CORE_CRYPT014_SHA1_V_VALUE_3_P is shown in [Figure 8-234](#) and described in [Table 8-478](#).

Return to [Summary Table](#).

SHA1 message status register. Third 32-bit word for SHA-1 calculation. Output from SHA-1 block

Table 8-477.
EDP_CORE_CRYPT014_SHA1_V_VALUE_3_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40F4h |

Figure 8-234. EDP_CORE_CRYPT014_SHA1_V_VALUE_3_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| V_VALUE_3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-10325476h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-478. EDP_CORE_CRYPT014_SHA1_V_VALUE_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-----------|--|
| 31-0 | V_VALUE_3 | R | 10325476h | 4th 32-bit word for SHA-1 calculation value. Output from SHA-1 block. |

8.5.179 EDP_CORE_CRYPT014_SHA1_V_VALUE_4_P Register (Offset = 40F8h) [reset = C3D2E1F0h]

EDP_CORE_CRYPT014_SHA1_V_VALUE_4_P is shown in [Figure 8-235](#) and described in [Table 8-480](#).

Return to [Summary Table](#).

SHA1 message status register. 5th 32-bit word for SHA-1 calculation. Output from SHA-1 block

Table 8-479.
EDP_CORE_CRYPT014_SHA1_V_VALUE_4_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 40F8h |

Figure 8-235. EDP_CORE_CRYPT014_SHA1_V_VALUE_4_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| V_VALUE_4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-C3D2E1F0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-480. EDP_CORE_CRYPT014_SHA1_V_VALUE_4_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-----------|--|
| 31-0 | V_VALUE_4 | R | C3D2E1F0h | 5th 32-bit word for SHA-1 calculation value. Output from SHA-1 block. |

8.5.180 EDP_CORE_MSA_HORIZONTAL_0_P_j Register (Offset = 3000h + formula) [reset = 0h]

EDP_CORE_MSA_HORIZONTAL_0_P_j is shown in [Figure 8-236](#) and described in [Table 8-482](#).

Return to [Summary Table](#).

MSA horizontal parameters. This settings define MSA content (not used for input video stream parameters). This field must be set prior video is enabled and must not be changed when video transmission is active.

Offset = 3000h + (j * 80h); where j = 0h to 3h

Table 8-481. EDP_CORE_MSA_HORIZONTAL_0_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3000h + formula |

Figure 8-236. EDP_CORE_MSA_HORIZONTAL_0_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCK_STUFF_HSTART | | | | | | | | | | | | | | | | PCK_STUFF_HTOTAL | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-482. EDP_CORE_MSA_HORIZONTAL_0_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-16 | PCK_STUFF_HSTART | R/W | 0h | MSA Hstart value. Horizontal active start from leading edge of Hsync, measured in pixel count. |
| 15-0 | PCK_STUFF_HTOTAL | R/W | 0h | MSA HTotal value. Horizontal total of transmitted main video stream, measured in pixel count. |

8.5.181 EDP_CORE_MSA_HORIZONTAL_1_P_j Register (Offset = 3004h + formula) [reset = 0h]

EDP_CORE_MSA_HORIZONTAL_1_P_j is shown in [Figure 8-237](#) and described in [Table 8-484](#).

Return to [Summary Table](#).

MSA horizontal parameters. This settings define MSA content (not used for input video stream parameters). This field must be set prior video is enabled and must not be changed when video transmission is active.

Offset = 3004h + (j * 80h); where j = 0h to 3h

Table 8-483. EDP_CORE_MSA_HORIZONTAL_1_P_j Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3004h + formula |

Figure 8-237. EDP_CORE_MSA_HORIZONTAL_1_P_j Register

| | | | | | | | |
|---------------------------------|----------------------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PCK_STUFF_HWIDTH | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCK_STUFF_HWIDTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PCK_STUFF_H SYNCPOLARIT Y | PCK_STUFF_HSYNCWIDTH | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCK_STUFF_HSYNCWIDTH | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-484. EDP_CORE_MSA_HORIZONTAL_1_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | PCK_STUFF_HWIDTH | R/W | 0h | MSA Hwidth parameter. Active video width, measured in pixel count. |
| 15 | PCK_STUFF_HSYNCPOLARITY | R/W | 0h | MSA HSync Polarity. 0 - Active high pulse. Synchronization signal is high for the sync pulse width. 1 - Active low pulse. Synchronization signal is low for the sync pulse width. This value may be different than actual polarity of the stream received at the video input interface. |
| 14-0 | PCK_STUFF_HSYNCWIDTH | R/W | 0h | MSA HSyncWidth parameter. Hsync width, measured in pixel count. |

8.5.182 EDP_CORE_MSA_VERTICAL_0_P_j Register (Offset = 3008h + formula) [reset = 0h]

EDP_CORE_MSA_VERTICAL_0_P_j is shown in [Figure 8-238](#) and described in [Table 8-486](#).

Return to [Summary Table](#).

MSA vertical parameters. This settings define MSA content (not used for input video stream parameters). This field must be set prior video is enabled and must not be changed when video transmission is active.

Offset = 3008h + (j * 80h); where j = 0h to 3h

**Table 8-485. EDP_CORE_MSA_VERTICAL_0_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3008h + formula |

Figure 8-238. EDP_CORE_MSA_VERTICAL_0_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCK_STUFF_VSTART | | | | | | | | | | | | | | | | PCK_STUFF_VTOTAL | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-486. EDP_CORE_MSA_VERTICAL_0_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-16 | PCK_STUFF_VSTART | R/W | 0h | MSA Vstart parameter. Vertical active start from leading edge of Vsync, measured in line count. |
| 15-0 | PCK_STUFF_VTOTAL | R/W | 0h | MSA Vtotal parameter. Vertical total of transmitted main video stream, measured in line count. |

8.5.183 EDP_CORE_MSA_VERTICAL_1_P_j Register (Offset = 300Ch + formula) [reset = 0h]

EDP_CORE_MSA_VERTICAL_1_P_j is shown in [Figure 8-239](#) and described in [Table 8-488](#).

Return to [Summary Table](#).

MSA vertical parameters. This settings define MSA content (not used for input video stream parameters). This field must be set prior video is enabled and must not be changed when video transmission is active.

Offset = 300Ch + (j * 80h); where j = 0h to 3h

Table 8-487. EDP_CORE_MSA_VERTICAL_1_P_j Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 300Ch + formula |

Figure 8-239. EDP_CORE_MSA_VERTICAL_1_P_j Register

| | | | | | | | |
|---------------------------------|----------------------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PCK_STUFF_VHEIGHT | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCK_STUFF_VHEIGHT | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PCK_STUFF_V SYNCPOLARIT Y | PCK_STUFF_VSYNCWIDTH | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCK_STUFF_VSYNCWIDTH | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-488. EDP_CORE_MSA_VERTICAL_1_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-16 | PCK_STUFF_VHEIGHT | R/W | 0h | MSA VHeigh parameter. Active video height, measured in line count. |
| 15 | PCK_STUFF_VSYNCPOLARITY | R/W | 0h | MSA VSyncPolarity. 0 - Active high pulse. Synchronization signal is high for the sync pulse width. 1 - Active low pulse. Synchronization signal is low for the sync pulse width. This value may be different than actual polarity of the stream received at the video input interface. |
| 14-0 | PCK_STUFF_VSYNCWIDTH | R/W | 0h | MSA VSyncWidth parameter. Vsync width, measured in line count. |

8.5.184 EDP_CORE_MSA_MISC_P_J Register (Offset = 3010h + formula) [reset = 00020000h]

EDP_CORE_MSA_MISC_P_J is shown in [Figure 8-240](#) and described in [Table 8-490](#).

Return to [Summary Table](#).

MSA MISC0 and MISC1 control register. This field must be set prior video is enabled and must not be changed when video transmission is active.

Offset = 3010h + (j * 80h); where j = 0h to 3h

Table 8-489. EDP_CORE_MSA_MISC_P_J Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3010h + formula |

Figure 8-240. EDP_CORE_MSA_MISC_P_J Register

| | | | | | | | |
|-----------|----|----|----|----|----|---------------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | MSA_IN_MID_I NTERLACE_E N | MSA_MISC1_I NV |
| R-0h | | | | | | R/W-1h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MSA_MISC1 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSA_MISC0 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-490. EDP_CORE_MSA_MISC_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 17 | MSA_IN_MID_INTERLAC E_EN | R/W | 1h | MSA transmission control in interlaced mode. 0 - enable transmission of MSA on each field, 1 - MSA transmitted on Top only |
| 16 | MSA_MISC1_INV | R/W | 0h | L/R toggle for interlaced and field sequential video. 0 - left 1 - right |
| 15-8 | MSA_MISC1 | R/W | 0h | MAS Miscellaneous1 as described in DisplayPort specification. |
| 7-0 | MSA_MISC0 | R/W | 0h | MSA Miscellaneous0 as described in DisplayPort specification. |

8.5.185 EDP_CORE_STREAM_CONFIG_P_j Register (Offset = 3014h + formula) [reset = 2h]

EDP_CORE_STREAM_CONFIG_P_j is shown in [Figure 8-241](#) and described in [Table 8-492](#).

Return to [Summary Table](#).

Stream configuration register. Used only in MST mode.

Offset = 3014h + (j * 80h); where j = 0h to 3h

Table 8-491. EDP_CORE_STREAM_CONFIG_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3014h + formula |

Figure 8-241. EDP_CORE_STREAM_CONFIG_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|-----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | NO_VIDEO | STREAM_EN |
| R-0h | | | | | | R/W-1h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-492. EDP_CORE_STREAM_CONFIG_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 1 | NO_VIDEO | R/W | 1h | Stream no video mode. 0 - video mode 1 - no video mode |
| 0 | STREAM_EN | R/W | 0h | Stream enable. 0 - stream disabled 1 - stream enabled |

8.5.186 EDP_CORE_AUDIO_PACK_STATUS_P_j Register (Offset = 3018h + formula) [reset = 00120002h]

EDP_CORE_AUDIO_PACK_STATUS_P_j is shown in [Figure 8-242](#) and described in [Table 8-494](#).

Return to [Summary Table](#).

Status signals for the audio pack.

Offset = 3018h + (j * 80h); where j = 0h to 3h

Table 8-493.
EDP_CORE_AUDIO_PACK_STATUS_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3018h + formula |

Figure 8-242. EDP_CORE_AUDIO_PACK_STATUS_P_j Register

| | | | | | | | |
|------------------------|----|-----------------------------|-----------------------------|--------------------|------------------------|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | AUDIO_TS_VERSION | | | | | |
| R-0h | | R/W-12h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | AP_PARITY_FSM_CURRENT_STATE | | AP_FIFO_WR_FSM_CURR_ST | | |
| R-0h | | | R-0h | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AP_FIFO_RD_FSM_CURR_ST | | AP_SDP_TRANSFER_FSM_CURR_ST | | AP_AIF_FSM_CURR_ST | AP_FIFO_FULL | AP_FIFO_EMPTY | |
| R-0h | | R-0h | | R-0h | R-1h | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-494. EDP_CORE_AUDIO_PACK_STATUS_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|--|
| 31-22 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 21-16 | AUDIO_TS_VERSION | R/W | 12h | Audio timestamp version. This field is transmitted in HB3 [7:2] of a Audio_TimeStamp SDP Header. |
| 15-13 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 12-10 | AP_PARITY_FSM_CURR ENT_STATE | R | 0h | Audio pack parity calc fsm state. Used only for debug purposes. |
| 9-8 | AP_FIFO_WR_FSM_CUR R_ST | R | 0h | Audio pack FIFO write fsm state. Used only for debug purposes. |
| 7-6 | AP_FIFO_RD_FSM_CUR R_ST | R | 0h | Audio pack FIFO read fsm state. Used only for debug purposes. |
| 5-3 | AP_SDP_TRANSFER_FS M_CURR_ST | R | 0h | Audio pack sdp transfer fsm state. Used only for debug purposes. |

Table 8-494. EDP_CORE_AUDIO_PACK_STATUS_P_j Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 2 | AP_AIF_FSM_CURR_ST | R | 0h | Audio pack aif fsm state. Used only for debug purposes. |
| 1 | AP_FIFO_FULL | R | 1h | Audio Pack Sync FIFO full flag, active high. Used only for debug purposes. |
| 0 | AP_FIFO_EMPTY | R | 0h | Audio Pack Sync FIFO empty flag, active high. Used only for debug purposes. |

8.5.187 EDP_CORE_VIF_STATUS_P_j Register (Offset = 301Ch + formula) [reset = 5555h]

EDP_CORE_VIF_STATUS_P_j is shown in [Figure 8-243](#) and described in [Table 8-496](#).

Return to [Summary Table](#).

Status signals for the VIF module. Used only for debug purposes.

Offset = 301Ch + (j * 80h); where j = 0h to 3h

Table 8-495. EDP_CORE_VIF_STATUS_P_j Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 301Ch + formula |

Figure 8-243. EDP_CORE_VIF_STATUS_P_j Register

| | | | | | | | |
|-------------------|----|----|----|-------------------|----|---------------|----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | VIF_RD_CTRL_STATE | | | |
| R-0h | | | | R-55h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VIF_RD_CTRL_STATE | | | | | | | |
| R-55h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VIF_RD_CTRL_STATE | | | | | | | |
| R-55h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VIF_WR_CTRL_STATE | | | | | | VIF_FIFO_FULL | VIF_FIFO_EMPTY |
| R-15h | | | | | | R-0h | R-1h |

LEGEND: R = Read Only; -n = value after reset

Table 8-496. EDP_CORE_VIF_STATUS_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 27-8 | VIF_RD_CTRL_STATE | R | 55h | VIF rd fsm current state. |
| 7-2 | VIF_WR_CTRL_STATE | R | 15h | VIF wr fsm current state. |
| 1 | VIF_FIFO_FULL | R | 0h | VIF ASync FIFO full flag, active high. |
| 0 | VIF_FIFO_EMPTY | R | 1h | VIF ASync FIFO empty flag, active high. |

8.5.188 EDP_CORE_PCK_STUFF_STATUS_0_P_j Register (Offset = 3020h + formula) [reset = 01000101h]

EDP_CORE_PCK_STUFF_STATUS_0_P_j is shown in [Figure 8-244](#) and described in [Table 8-498](#).

Return to [Summary Table](#).

Status of the the video stuff module (0). Used only for debug purposes.

Offset = 3020h + (j * 80h); where j = 0h to 3h

Table 8-497.
EDP_CORE_PCK_STUFF_STATUS_0_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3020h + formula |

Figure 8-244. EDP_CORE_PCK_STUFF_STATUS_0_P_j Register

| | | | | | | | |
|----------|---------------------|----|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | MSA_GEN_STATE | | | | | | |
| R-0h | R-1h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | SST_VIDEO_GEN_STATE | | | | | | |
| R-0h | R-1h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | NO_VIDEO_GEN_STATE | | | |
| R-0h | | | | R-1h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-498. EDP_CORE_PCK_STUFF_STATUS_0_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 30-24 | MSA_GEN_STATE | R | 1h | Secondary Data generator FSM status. |
| 23-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 14-8 | SST_VIDEO_GEN_STATE | R | 1h | SST video generator FSM status. |
| 7-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 4-0 | NO_VIDEO_GEN_STATE | R | 1h | No video generator FSM status. |

8.5.189 EDP_CORE_PCK_STUFF_STATUS_1_P_j Register (Offset = 3024h + formula) [reset = 1h]

EDP_CORE_PCK_STUFF_STATUS_1_P_j is shown in [Figure 8-245](#) and described in [Table 8-500](#).

Return to [Summary Table](#).

Status of the the video stuff module (1). Used only for debug purposes.

Offset = 3024h + (j * 80h); where j = 0h to 3h

Table 8-499.
EDP_CORE_PCK_STUFF_STATUS_1_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3024h + formula |

Figure 8-245. EDP_CORE_PCK_STUFF_STATUS_1_P_j Register

| | | | | | | | |
|----------|----|----|----|------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | SST_SS_GEN_STATE | | | |
| R-0h | | | | R-1h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-500. EDP_CORE_PCK_STUFF_STATUS_1_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 7-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5-0 | SST_SS_GEN_STATE | R | 1h | MSA generator FSM status. |

8.5.190 EDP_CORE_INFO_PACK_STATUS_P_j Register (Offset = 3028h + formula) [reset = 2h]

EDP_CORE_INFO_PACK_STATUS_P_j is shown in [Figure 8-246](#) and described in [Table 8-502](#).

Return to [Summary Table](#).

Status signals for the info pack module, as well as final VB-ID value. Used only for debug purposes.

Offset = 3028h + (j * 80h); where j = 0h to 3h

**Table 8-501. EDP_CORE_INFO_PACK_STATUS_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3028h + formula |

Figure 8-246. EDP_CORE_INFO_PACK_STATUS_P_j Register

| | | | | | | | |
|--------------------------------|----|----|-----------------------------|------------------------------|----|----------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IN_VBID | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IP_SEND_DATA_FSM_CURRENT_STATE | | | | IP_FIFO_RD_FSM_CURRENT_STATE | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IP_FIFO_WR_FSM_CURRENT_STATE | | | IP_PARITY_FSM_CURRENT_STATE | | | INFO_PACK_FIFO_EMPTY | INFO_PACK_FIFO_FULL |
| R-0h | | | R-0h | | | R-1h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-502. EDP_CORE_INFO_PACK_STATUS_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|--|
| 31-24 | IN_VBID | R | 0h | Value of the sent VB-ID [vb_id_final]. |
| 23-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-12 | IP_SEND_DATA_FSM_C URRENT_STATE | R | 0h | State of the send_data FSM. |
| 11-8 | IP_FIFO_RD_FSM_CURR ENT_STATE | R | 0h | State of the fifo_rd FSM. |
| 7-5 | IP_FIFO_WR_FSM_CUR RENT_STATE | R | 0h | State of the fifo_wr FSM. |
| 4-2 | IP_PARITY_FSM_CURRE NT_STATE | R | 0h | State of the parity FSM. |
| 1 | INFO_PACK_FIFO_EMPTY | R | 1h | Info_pack fifo empty flag, active high. |
| 0 | INFO_PACK_FIFO_FULL | R | 0h | Info_pack fifo full flag, active high. |

8.5.191 EDP_CORE_STREAM_CONFIG_2_P_j Register (Offset = 302Ch + formula) [reset = 0h]

EDP_CORE_STREAM_CONFIG_2_P_j is shown in [Figure 8-247](#) and described in [Table 8-504](#).

Return to [Summary Table](#).

Additional video stream configuration. Used for debug purposes or for non-standard video formats.

Offset = 302Ch + (j * 80h); where j = 0h to 3h

Table 8-503. EDP_CORE_STREAM_CONFIG_2_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 302Ch + formula |

Figure 8-247. EDP_CORE_STREAM_CONFIG_2_P_j Register

| | | | | | | | |
|------------------------|--------------------|----|----|----|----|----------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | CFG_EN_HSY NC_DELAY |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CFG_HSYNC_DELAY | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MST_SF_EVAL_VAL_SYM | | | | | | CFG_TU_VS_DIFF | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MST_SF_EVAL _OVR_EN | MST_SF_EVAL_PERIOD | | | | | | |
| R/W-0h | R/W-0h | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-504. EDP_CORE_STREAM_CONFIG_2_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 24 | CFG_EN_HSYNC_DELAY | R/W | 0h | Unused. Kept RW for software backward compatibility. |
| 23-16 | CFG_HSYNC_DELAY | R/W | 0h | Unused. Kept RW for software backward compatibility. |
| 15-10 | MST_SF_EVAL_VAL_SYM | R/W | 0h | Number of valid symbols to output during stream fill evaluation period. This should be less than mst_sf_eval_period. |
| 9-8 | CFG_TU_VS_DIFF | R/W | 0h | Unused. Kept RW for software backward compatibility. |
| 7 | MST_SF_EVAL_OVR_EN | R/W | 0h | Enable override of mst_sf_eval_period, mst_sf_eval_val_sym and cfg_tu_vs_diff when in MST mode. |
| 6-0 | MST_SF_EVAL_PERIOD | R/W | 0h | Stream fill evaluation period when in MST mode and mst_sf_eval_ovr_en bit is set. |

8.5.192 EDP_CORE_DP_HORIZONTAL_P_j Register (Offset = 3030h + formula) [reset = 0h]

EDP_CORE_DP_HORIZONTAL_P_j is shown in [Figure 8-248](#) and described in [Table 8-506](#).

Return to [Summary Table](#).

Video Horizontal parameters. This register must be programmed prior enabling video and must not be changed while video is being transmitted.

In case of compressed stream transmission (DSC) and split panel mode values in this register must be divided by 2 since VIF interface operates at pixel clock divided by 2. This will ensure the same timing compared to uncompressed stream and.

Offset = 3030h + (j * 80h); where j = 0h to 3h

Table 8-505. EDP_CORE_DP_HORIZONTAL_P_j Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3030h + formula |

Figure 8-248. EDP_CORE_DP_HORIZONTAL_P_j Register

| | | | | | | | |
|------------|------------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HWIDTH | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HWIDTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | HSYNCWIDTH | | | | | | |
| R-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HSYNCWIDTH | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-506. EDP_CORE_DP_HORIZONTAL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | HWIDTH | R/W | 0h | Horizontal Active Video Width. Width of video active period [VACTIVE] expressed in number pixel clock cycles. It must be a multiply of 16. |
| 15 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 14-0 | HSYNCWIDTH | R/W | 0h | Horizontal Sync Width. Width of horizontal synchronization pulse [HSYNC] expressed in number pixel clock cycles. |

8.5.193 EDP_CORE_DP_VERTICAL_0_P_j Register (Offset = 3034h + formula) [reset = 0h]

EDP_CORE_DP_VERTICAL_0_P_j is shown in [Figure 8-249](#) and described in [Table 8-508](#).

Return to [Summary Table](#).

Video Vertical parameters. This register must be programmed prior enabling video and must not be changed while video is being transmitted.

Offset = 3034h + (j * 80h); where j = 0h to 3h

**Table 8-507. EDP_CORE_DP_VERTICAL_0_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3034h + formula |

Figure 8-249. EDP_CORE_DP_VERTICAL_0_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSTART | | | | | | | | | | | | | | | | VHEIGHT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-508. EDP_CORE_DP_VERTICAL_0_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------|------|-------|---|
| 31-16 | VSTART | R/W | 0h | Vertical Active Start [VSTART]. Index of the first active line in a video frame. |
| 15-0 | VHEIGHT | R/W | 0h | Vertical Active High [VACTIVE]. Number of active lines in a video frame. |

8.5.194 EDP_CORE_DP_VERTICAL_1_P_j Register (Offset = 3038h + formula) [reset = 0h]

EDP_CORE_DP_VERTICAL_1_P_j is shown in [Figure 8-250](#) and described in [Table 8-510](#).

Return to [Summary Table](#).

Video Vertical parameters. This register must be programmed prior enabling video and must not be changed while video is being transmitted.

Offset = 3038h + (j * 80h); where j = 0h to 3h

Table 8-509. EDP_CORE_DP_VERTICAL_1_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3038h + formula |

Figure 8-250. EDP_CORE_DP_VERTICAL_1_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | VTOTAL_EVEN |
| R-0h | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VTOTAL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VTOTAL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-510. EDP_CORE_DP_VERTICAL_1_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-17 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 16 | VTOTAL_EVEN | R/W | 0h | Indicate Vtotal is an even number as described in MISC1[0] in DisplayPort specification. Active high. |
| 15-0 | VTOTAL | R/W | 0h | Vertical Total Heigh [HTOTAL]. Total number of lines per frame. |

8.5.195 EDP_CORE_DP_BLOCK_SDP_P_j Register (Offset = 303Ch + formula) [reset = 0h]

EDP_CORE_DP_BLOCK_SDP_P_j is shown in [Figure 8-251](#) and described in [Table 8-512](#).

Return to [Summary Table](#).

SDP scheduling control register. Allows for tuning when SDP can be sent during blanking periods. This register must be programmed prior enabling video and must not be changed while video is being transmitted.

Offset = 303Ch + (j * 80h); where j = 0h to 3h

**Table 8-511. EDP_CORE_DP_BLOCK_SDP_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 303Ch + formula |

Figure 8-251. EDP_CORE_DP_BLOCK_SDP_P_j Register

| | | | | | | | |
|--------------------|--------------------|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BS_SDP_STOP_OVR_EN | BS_SDP_STOP_ACTIVE | | | | | | |
| R/W-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BS_SDP_STOP_ACTIVE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BS_SDP_STOP_BLANK | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BS_SDP_STOP_BLANK | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-512. EDP_CORE_DP_BLOCK_SDP_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31 | BS_SDP_STOP_OVR_EN | R/W | 0h | Enable override settings. If this bit is not set, the hardware will not automatically block SDP transmission during video lines, this may result in shifting of video timing. |
| 30-16 | BS_SDP_STOP_ACTIVE | R/W | 0h | Block SDP scheduling after specified cycles after BS during horizontal blank lines. Maximum is 32767. If set to 0, no SDPs will be transmitted during hblank. Only used when bs_sdp_stop_ovr_en is set to 1. |
| 15-0 | BS_SDP_STOP_BLANK | R/W | 0h | Block SDP scheduling after specified cycles after BS during vertical blank lines. Maximum is 65535. If set to 0, no SDPs will be transmitted during vblank. Only used when bs_sdp_stop_ovr_en is set to 1. |

8.5.196 EDP_CORE_DP_MST_SLOT_ALLOCATE_P_J Register (Offset = 3044h + formula) [reset = 0h]

EDP_CORE_DP_MST_SLOT_ALLOCATE_P_J is shown in [Figure 8-252](#) and described in [Table 8-514](#).

Return to [Summary Table](#).

Stream slots allocation in MST mode. This register defines slots in the MTP assigned to a given stream. All slots between start and end are assigned to the stream. Assignment of noncontiguous slots to a single stream is not supported.

Offset = 3044h + (j * 80h); where j = 0h to 3h

Table 8-513.
EDP_CORE_DP_MST_SLOT_ALLOCATE_P_J
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3044h + formula |

Figure 8-252. EDP_CORE_DP_MST_SLOT_ALLOCATE_P_J Register

| | | | | | | | |
|----------|----|----|----|-------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | STREAM_END_SLOT | | | |
| R-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | STREAM_START_SLOT | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-514. EDP_CORE_DP_MST_SLOT_ALLOCATE_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-14 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 13-8 | STREAM_END_SLOT | R/W | 0h | Stream end slot. This value determines last slot in MTP assigned to a given stream. Allowed values are stream_start_slot-63. |
| 7-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5-0 | STREAM_START_SLOT | R/W | 0h | Stream start slot. This value determines first slot in MTP assigned to a given stream. Allowed values are 1-63. |

8.5.197 EDP_CORE_RATE_GOVERNING_CTRL_P_j Register (Offset = 3048h + formula) [reset = 0h]

EDP_CORE_RATE_GOVERNING_CTRL_P_j is shown in [Figure 8-253](#) and described in [Table 8-516](#).

Return to [Summary Table](#).

Control rate governing for stream in MST mode.

Offset = 3048h + (j * 80h); where j = 0h to 3h

Table 8-515.
EDP_CORE_RATE_GOVERNING_CTRL_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3048h + formula |

Figure 8-253. EDP_CORE_RATE_GOVERNING_CTRL_P_j Register

| | | | | | | | |
|-----------------|----|----|----|-----------------|-----------------|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | RATE_GOV_E N | TARG_AV_SLOTS_X | |
| R-0h | | | | | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TARG_AV_SLOTS_X | | | | TARG_AV_SLOTS_Y | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-516. EDP_CORE_RATE_GOVERNING_CTRL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 10 | RATE_GOV_EN | R/W | 0h | Enable rate governing. When set to 0, this stream will only output VCPF |
| 9-4 | TARG_AV_SLOTS_X | R/W | 0h | Target average number of slots per MTP configuration |
| 3-0 | TARG_AV_SLOTS_Y | R/W | 0h | Target average number of slots per MTP configuration. Fractional component |

8.5.198 EDP_CORE_DP_FRAMER_PXL_REPR_P_j Register (Offset = 304Ch + formula) [reset = 102h]

EDP_CORE_DP_FRAMER_PXL_REPR_P_j is shown in [Figure 8-254](#) and described in [Table 8-518](#).

Return to [Summary Table](#).

Video pixel format configuration. This register must be programmed prior enabling video and must not be changed while video is being transmitted.

Offset = 304Ch + (j * 80h); where j = 0h to 3h

Table 8-517.
EDP_CORE_DP_FRAMER_PXL_REPR_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 304Ch + formula |

Figure 8-254. EDP_CORE_DP_FRAMER_PXL_REPR_P_j Register

| | | | | | | | |
|----------|--------|----|----|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | DIFF | | | | | | |
| R-0h | R/W-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | M | | | | | | |
| R-0h | R/W-0h | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | PXL_ENC_FORMAT | | | |
| R-0h | | | | R/W-1h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | COLOR_DEPTH | | | |
| R-0h | | | | R/W-2h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-518. EDP_CORE_DP_FRAMER_PXL_REPR_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 30-24 | DIFF | R/W | 0h | Difference between Denominator and Numerator of the ratio that describes valid symbols distribution. Example: If TU_VALID*=12.34 then DIFF= 100-34=66. TU_VALID calculated according to DisplayPort specification. This setting apply only when compressed [DSC] stream is being transmitted. |
| 23 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |

Table 8-518. EDP_CORE_DP_FRAMER_PXL_REPR_P_j Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 22-16 | M | R/W | 0h | Numerator of the ratio that describes valid symbols distribution. Example: If TU_VALID=12.34 then M=34. TU_VALID calculated according to DisplayPort specification. This setting apply only when compressed [DSC] stream is being transmitted. |
| 15-13 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 12-8 | PXL_ENC_FORMAT | R/W | 1h | Pixel encoding format: 1h - RGB 2h - YCbCr 4: 4:4 4h - YCbCr 4: 2:2 8h - Y CbCr 4: 2:0 10h - Y-only All other values - RESERVED |
| 7-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 4-0 | COLOR_DEPTH | R/W | 2h | Color depth: 1h - 6 bpc, 2h - 8 bpc, 4h - 10 bpc, 8h - 12 bpc, 10h - 16 bpc, All other values - RESERVED |

8.5.199 EDP_CORE_DP_FRAMER_SP_P_j Register (Offset = 3050h + formula) [reset = 0h]

EDP_CORE_DP_FRAMER_SP_P_j is shown in [Figure 8-255](#) and described in [Table 8-520](#).

Return to [Summary Table](#).

Synchronization signals polarity and 3D control. This register must be programmed prior enabling video and must not be changed while video is being transmitted.

Offset = 3050h + (j * 80h); where j = 0h to 3h

Table 8-519. EDP_CORE_DP_FRAMER_SP_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3050h + formula |

Figure 8-255. EDP_CORE_DP_FRAMER_SP_P_j Register

| | | | | | | | |
|----------|----|----|---------------|--------------|--------------|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | STACKED_3D_EN | FRAMER_3D_EN | INTERLACE_EN | HSP | VSP |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-520. EDP_CORE_DP_FRAMER_SP_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 4 | STACKED_3D_EN | R/W | 0h | Unused. Kept RW for software backward compatibility. |
| 3 | FRAMER_3D_EN | R/W | 0h | 3D video enable, active high. This bit must be set when 3D Field Sequential Stereo Format is enabled. Other 3D formats do not require setting this bit. |
| 2 | INTERLACE_EN | R/W | 0h | Interlaced video enable. Active high. |
| 1 | HSP | R/W | 0h | Video interface HSYNC polarity: 0 - active high, 1 - active low |
| 0 | VSP | R/W | 0h | Video interface VSYNC polarity: 0 - active high, 1 - active low |

8.5.200 EDP_CORE_AUDIO_PACK_CONTROL_P_j Register (Offset = 3054h + formula) [reset = 0h]

EDP_CORE_AUDIO_PACK_CONTROL_P_j is shown in [Figure 8-256](#) and described in [Table 8-522](#).

Return to [Summary Table](#).

Audio packet configuration.

Offset = 3054h + (j * 80h); where j = 0h to 3h

Table 8-521.
EDP_CORE_AUDIO_PACK_CONTROL_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3054h + formula |

Figure 8-256. EDP_CORE_AUDIO_PACK_CONTROL_P_j Register

| | | | | | | | |
|------------|----|----|----|----|----|--------|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | MONO | AUDIO_PACK_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MST_SDP_ID | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-522. EDP_CORE_AUDIO_PACK_CONTROL_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 31-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 9 | MONO | R/W | 0h | In case of 2-channel layout and one lane configuration SW decides whether it is a stereo or mono transfer. Relevant for SDP HB3 [2:0] - ChannelCount field |
| 8 | AUDIO_PACK_EN | R/W | 0h | Enables the Audio_Pack module, active high |
| 7-0 | MST_SDP_ID | R/W | 0h | Secondary-Data Packet ID. This field is transmitted in HB0 of the Audio SDP [Audio_TimeStamp and Audio_Stream]. |

8.5.201 EDP_CORE_LINE_THRESH_P_j Register (Offset = 3064h + formula) [reset = 20h]

EDP_CORE_LINE_THRESH_P_j is shown in [Figure 8-257](#) and described in [Table 8-524](#).

Return to [Summary Table](#).

Video FIFO latency threshold

Offset = 3064h + (j * 80h); where j = 0h to 3h

**Table 8-523. EDP_CORE_LINE_THRESH_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3064h + formula |

Figure 8-257. EDP_CORE_LINE_THRESH_P_j Register

| | | | | | | | |
|----------|----|-----------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CFG_ACTIVE_LINE_TRESH | | | | | |
| R-0h | | R/W-20h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-524. EDP_CORE_LINE_THRESH_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 5-0 | CFG_ACTIVE_LINE_TRESH | R/W | 20h | Video Fifo Latency threshold. Defines the number of FIFO rows before reading starts. This setting depends on the transmitted video format and link rate. |

8.5.202 EDP_CORE_DP_VB_ID_P_J Register (Offset = 3068h + formula) [reset = 9h]

EDP_CORE_DP_VB_ID_P_J is shown in [Figure 8-258](#) and described in [Table 8-526](#).

Return to [Summary Table](#).

Vertical blanking ID

Offset = 3068h + (j * 80h); where j = 0h to 3h

Table 8-525. EDP_CORE_DP_VB_ID_P_J Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3068h + formula |

Figure 8-258. EDP_CORE_DP_VB_ID_P_J Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | VB_ID | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | R/W-9h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-526. EDP_CORE_DP_VB_ID_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 7-0 | VB_ID | R/W | 9h | VB-ID as described in the DisplayPort specification. Bits that are timing dependent [VerticalBlanking_Flag, FieldID_Flag, HDCP SYNC DETECT, Compressed Stream_Flag] are overridden by hardware thus actual value written to the register is ignored. |

8.5.203 EDP_CORE_DP_FIELDSEQ_3D_P_j Register (Offset = 306Ch + formula) [reset = 0h]

EDP_CORE_DP_FIELDSEQ_3D_P_j is shown in [Figure 8-259](#) and described in [Table 8-528](#).

Return to [Summary Table](#).

Supporting configuration to switch from top/bottom on the input to field sequential on the output

Offset = 306Ch + (j * 80h); where j = 0h to 3h

**Table 8-527. EDP_CORE_DP_FIELDSEQ_3D_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 306Ch + formula |

Figure 8-259. EDP_CORE_DP_FIELDSEQ_3D_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIELD_SEQ_END | | | | | | | | | | | | | | | | FIELD_SEQ_START | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-528. EDP_CORE_DP_FIELDSEQ_3D_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-16 | FIELD_SEQ_END | R/W | 0h | Number of line in the frame where the Vblank part in the field sequential format ends |
| 15-0 | FIELD_SEQ_START | R/W | 0h | Number of line in the frame where the Vblank part in the field sequential format starts |

8.5.204 EDP_CORE_DP_FRONT_BACK_PORCH_P_j Register (Offset = 3078h + formula) [reset = 0010003Ch]

EDP_CORE_DP_FRONT_BACK_PORCH_P_j is shown in [Figure 8-260](#) and described in [Table 8-530](#).

Return to [Summary Table](#).

Front and Back Porch configuration register.

In case of compressed stream transmission (DSC) and split panel mode values in this register must be divided by 2 since VIF interface operates at pixel clock divided by 2. This will ensure the same timing compared to uncompressed stream and.

Offset = 3078h + (j * 80h); where j = 0h to 3h

Table 8-529.
EDP_CORE_DP_FRONT_BACK_PORCH_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 3078h + formula |

Figure 8-260. EDP_CORE_DP_FRONT_BACK_PORCH_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRONT_PORCH | | | | | | | | | | | | | | | | BACK_PORCH | | | | | | | | | | | | | | | |
| R/W-10h | | | | | | | | | | | | | | | | R/W-3Ch | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-530. EDP_CORE_DP_FRONT_BACK_PORCH_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--------------------------|
| 31-16 | FRONT_PORCH | R/W | 10h | Value of the front porch |
| 15-0 | BACK_PORCH | R/W | 3Ch | Value of the back porch |

8.5.205 EDP_CORE_DP_BYTE_COUNT_P_j Register (Offset = 307Ch + formula) [reset = 2A4h]

EDP_CORE_DP_BYTE_COUNT_P_j is shown in [Figure 8-261](#) and described in [Table 8-532](#).

Return to [Summary Table](#).

Number of bytes per lane/chunk parameters

Offset = 307Ch + (j * 80h); where j = 0h to 3h

Table 8-531. EDP_CORE_DP_BYTE_COUNT_P_j Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A00 307Ch + formula |

Figure 8-261. EDP_CORE_DP_BYTE_COUNT_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTES_IN_CHUNK | | | | | | | | | | | | | | | | BYTE_COUNT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-2A4h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-532. EDP_CORE_DP_BYTE_COUNT_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-16 | BYTES_IN_CHUNK | R/W | 0h | Number of bytes in chunk per lane, including additional EOC symbol. |
| 15-0 | BYTE_COUNT | R/W | 2A4h | Total number of bytes in a line in case of non-DSC video. When DSC is enabled should be total number of bytes in a line *per lane*, including the additional EOC symbol[s]. |

8.5.206 EDP_CORE_IRAM_REG_P_y Register (Offset = 00010000h + formula) [reset = 0h]

EDP_CORE_IRAM_REG_P_y is shown in [Figure 8-262](#) and described in [Table 8-534](#).

Return to [Summary Table](#).

Xtensa Instruction RAM address space. Accessed only during boot mode to load firmware.

Offset = 00010000h + (y * 4h); where y = 0h to 3FFFh

Table 8-533. EDP_CORE_IRAM_REG_P_y Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A01 0000h + formula |

Figure 8-262. EDP_CORE_IRAM_REG_P_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IRAM_DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-534. EDP_CORE_IRAM_REG_P_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|-------------|
| 31-0 | IRAM_DATA | R/W | 0h | IRAM data |

8.5.207 EDP_CORE_DRAM_REG_P_y Register (Offset = 00020000h + formula) [reset = 0h]

EDP_CORE_DRAM_REG_P_y is shown in [Figure 8-263](#) and described in [Table 8-536](#).

Return to [Summary Table](#).

Xtensa Data RAM address space. Accessed only during boot mode to load firmware.

Offset = 00020000h + (y * 4h); where y = 0h to 3FFFh

**Table 8-535. EDP_CORE_DRAM_REG_P_y
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A02 0000h + formula |

Figure 8-263. EDP_CORE_DRAM_REG_P_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DRAM_DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-536. EDP_CORE_DRAM_REG_P_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|-------------|
| 31-0 | DRAM_DATA | R/W | 0h | DRAM data |

8.5.208 EDP_CORE_AUX_CONFIG_P Register (Offset = 00030A00h) [reset = 0D0E0331h]

EDP_CORE_AUX_CONFIG_P is shown in [Figure 8-264](#) and described in [Table 8-538](#).

Return to [Summary Table](#).

AUX Configuration Register

Table 8-537. EDP_CORE_AUX_CONFIG_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A00h |

Figure 8-264. EDP_CORE_AUX_CONFIG_P Register

| | | | | | | | |
|----------|--------------|--------------------|------------------|--------------|---------------|----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | TERM_SEG_EN | | | |
| R-0h | | | | R/W-Dh | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | TX_CURR_CTRL | | | |
| R-0h | | | | R/W-Eh | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | TX_SLEW_RATE | | TX_REDUCED_SWING | RESERVED | RX_HYST_LVL | | |
| R-0h | R/W-0h | | R/W-0h | R-0h | R/W-3h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RX DEGLITCH_FILTER | | RESERVED | RX_OFFSET_DIS | BANDGAP_ADJUST | |
| R-0h | | R/W-3h | | R-0h | R/W-0h | R/W-1h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-538. EDP_CORE_AUX_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-29 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 28-24 | TERM_SEG_EN | R/W | Dh | Enables output resistor segments for termination impedance. |
| 23-21 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 20-16 | TX_CURR_CTRL | R/W | Eh | TX current for output diff pair. |
| 15 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 14-13 | TX_SLEW_RATE | R/W | 0h | TX slew rate adjust. |
| 12 | TX_REDUCED_SWING | R/W | 0h | Control for lowering AUX transmitter swing level. |
| 11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |

Table 8-538. EDP_CORE_AUX_CONFIG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---|
| 10-8 | RX_HYST_LVL | R/W | 3h | Hysteresis control for AUX receiver front end. |
| 7-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 5-4 | RX_DEGLITCH_FILTER | R/W | 3h | Suppresses high-frequency pulses on AUX receiver output. |
| 3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 2 | RX_OFFSET_DIS | R/W | 0h | Disables internal receiver cmn mode offset. |
| 1-0 | BANDGAP_ADJUST | R/W | 1h | Bandgap startup circuit adjust. |

8.5.209 EDP_CORE_AUX_CTRL_P Register (Offset = 00030A04h) [reset = 0h]

EDP_CORE_AUX_CTRL_P is shown in [Figure 8-265](#) and described in [Table 8-540](#).

[Return to Summary Table.](#)

AUX Control Register

Table 8-539. EDP_CORE_AUX_CTRL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A04h |

Figure 8-265. EDP_CORE_AUX_CTRL_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DECAP_EN | BANDGAP_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-540. EDP_CORE_AUX_CTRL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 1 | DECAP_EN | R/W | 0h | Decap enable. Active HIGH. Asserted as long as DPTX system is enabled. |
| 0 | BANDGAP_EN | R/W | 0h | Bandgap enable. Active HIGH. Asserted when AUX channel needs to be used for request/response traffic - can be disabled after response is received if channel will not be needed for more than 4.5 microseconds. |

8.5.210 EDP_CORE_AUX_ATBSEL_P Register (Offset = 00030A08h) [reset = 0h]

EDP_CORE_AUX_ATBSEL_P is shown in [Figure 8-266](#) and described in [Table 8-542](#).

Return to [Summary Table](#).

AUX_ATBSEL

Table 8-541. EDP_CORE_AUX_ATBSEL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A08h |

Figure 8-266. EDP_CORE_AUX_ATBSEL_P Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | AUXIP_ATBSEL_ONEHOT | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-542. EDP_CORE_AUX_ATBSEL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 7-0 | AUXIP_ATBSEL_ONEHOT | R/W | 0h | auxip_atbssel_onehot |

8.5.211 EDP_CORE_AUX_TESTMODE_CTL_P Register (Offset = 00030A0Ch) [reset = 0h]

EDP_CORE_AUX_TESTMODE_CTL_P is shown in [Figure 8-267](#) and described in [Table 8-544](#).

Return to [Summary Table](#).

AUX IP test control register.

**Table 8-543. EDP_CORE_AUX_TESTMODE_CTL_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A0Ch |

Figure 8-267. EDP_CORE_AUX_TESTMODE_CTL_P Register

| | | | | | | | |
|----------|----|----|------------------|-------------|------------|------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | DECAP_EN_DE L | AUX_DATA_IN | TX_EN_CTRL | RX_EN_CTRL | AUX_TESTMO DE_EN |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-544. EDP_CORE_AUX_TESTMODE_CTL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 4 | DECAP_EN_DEL | R/W | 0h | decap_en_del test value. Reflected at the decap_en_del output when aux_testmode_en=1 |
| 3 | AUX_DATA_IN | R/W | 0h | aux_data_in test value. Reflected at the aux_data_in output when aux_testmode_en=1 |
| 2 | TX_EN_CTRL | R/W | 0h | tx_en test value. Reflected at the tx_en output when aux_testmode_en=1 |
| 1 | RX_EN_CTRL | R/W | 0h | rx_en test value. Reflected at the rx_en output when aux_testmode_en=1 |
| 0 | AUX_TESTMODE_EN | R/W | 0h | AUX test enable. 0 - Test mode disabled 1 - test mode enabled, rx_en, tx_en, aux_data_in and decap_en_del are driven directly from the control registers |

8.5.212 EDP_CORE_AUX_TESTMODE_ST_P Register (Offset = 00030A10h) [reset = 0h]

EDP_CORE_AUX_TESTMODE_ST_P is shown in [Figure 8-268](#) and described in [Table 8-546](#).

Return to [Summary Table](#).

AUX IP interface status.

Table 8-545. EDP_CORE_AUX_TESTMODE_ST_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A10h |

Figure 8-268. EDP_CORE_AUX_TESTMODE_ST_P Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | AUX_DATA_OUT | HPD_DATA_OUT |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-546. EDP_CORE_AUX_TESTMODE_ST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 1 | AUX_DATA_OUT | R | 0h | Raw status of aux_data_out output from AUX IP |
| 0 | HPD_DATA_OUT | R | 0h | Raw status of HPD output from AUX IP |

8.5.213 EDP_CORE_PHY_RESET_P Register (Offset = 00030A20h) [reset = 0h]

EDP_CORE_PHY_RESET_P is shown in [Figure 8-269](#) and described in [Table 8-548](#).

Return to [Summary Table](#).

PHY Reset Control Register

Table 8-547. EDP_CORE_PHY_RESET_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A20h |

Figure 8-269. EDP_CORE_PHY_RESET_P Register

| | | | | | | | |
|-----------------------|-----------------------|-----------------------|-----------------------|------------------|------------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | PHY_RESET |
| R-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PMA_TX_ELEC_IDLE_LN_3 | PMA_TX_ELEC_IDLE_LN_2 | PMA_TX_ELEC_IDLE_LN_1 | PMA_TX_ELEC_IDLE_LN_0 | PHY_L03_RES_ET_N | PHY_L02_RES_ET_N | PHY_L01_RES_ET_N | PHY_L00_RES_ET_N |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-548. EDP_CORE_PHY_RESET_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-9 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 8 | PHY_RESET | R/W | 0h | 0 - reset all PHY logic for the entire PHY with the exception of the PHY APB registers, 1 - turn off reset. PHY reset is active LOW. |
| 7 | PMA_TX_ELEC_IDLE_LN_3 | R/W | 0h | PMA Tx electrical idle for line 3. 1 - Tx differential output placed into electrical idle, 0 - transmit data. |
| 6 | PMA_TX_ELEC_IDLE_LN_2 | R/W | 0h | PMA Tx electrical idle for line 2. 1 - Tx differential output placed into electrical idle, 0 - transmit data. |
| 5 | PMA_TX_ELEC_IDLE_LN_1 | R/W | 0h | PMA Tx electrical idle for line 1. 1 - Tx differential output placed into electrical idle, 0 - transmit data. |
| 4 | PMA_TX_ELEC_IDLE_LN_0 | R/W | 0h | PMA Tx electrical idle for line 0. 1 - Tx differential output placed into electrical idle, 0 - transmit data. |

Table 8-548. EDP_CORE_PHY_RESET_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 3 | PHY_L03_RESET_N | R/W | 0h | 0 - turn on PHY I03 reset with the exception of the PHY APB registers, 1 - turn off reset. PHY I03 reset is active LOW. |
| 2 | PHY_L02_RESET_N | R/W | 0h | 0 - turn on PHY I02 reset with the exception of the PHY APB registers, 1 - turn off reset. PHY I02 reset is active LOW. |
| 1 | PHY_L01_RESET_N | R/W | 0h | 0 - turn on PHY I01 reset with the exception of the PHY APB registers, 1 - turn off reset. PHY I01 reset is active LOW. |
| 0 | PHY_L00_RESET_N | R/W | 0h | 0 - turn on PHY I00 reset with the exception of the PHY APB registers, 1 - turn off reset. PHY I00 reset is active LOW. |

8.5.214 EDP_CORE_PMA_PLLCLK_EN_P Register (Offset = 00030A24h) [reset = 0h]

EDP_CORE_PMA_PLLCLK_EN_P is shown in [Figure 8-270](#) and described in [Table 8-550](#).

Return to [Summary Table](#).

PHY Link PLL Clock Enable Register

**Table 8-549. EDP_CORE_PMA_PLLCLK_EN_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A24h |

Figure 8-270. EDP_CORE_PMA_PLLCLK_EN_P Register

| | | | | | | | |
|----------|----|----|----|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | PMA_XCVR_P LLCLK_EN_LN _3 | PMA_XCVR_P LLCLK_EN_LN _2 | PMA_XCVR_P LLCLK_EN_LN _1 | PMA_XCVR_P LLCLK_EN_LN _0 |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-550. EDP_CORE_PMA_PLLCLK_EN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 3 | PMA_XCVR_PLLCLK_EN_LN_3 | R/W | 0h | Link PLL clock enable used to cleanly turn off the data rate clock in the PMA for line 3, 1 - enable Line 3 PLL clock. 0 - disable PLL clock. |
| 2 | PMA_XCVR_PLLCLK_EN_LN_2 | R/W | 0h | Link PLL clock enable used to cleanly turn off the data rate clock in the PMA for line 2, 1 - enable Line 2 PLL clock. 0 - disable PLL clock. |
| 1 | PMA_XCVR_PLLCLK_EN_LN_1 | R/W | 0h | Link PLL clock enable used to cleanly turn off the data rate clock in the PMA for line 1, 1 - enable Line 1 PLL clock. 0 - disable PLL clock. |

Table 8-550. EDP_CORE_PMA_PLLCLK_EN_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 0 | PMA_XCVR_PLLCLK_EN_LN_0 | R/W | 0h | Link PLL clock enable used to cleanly turn off the data rate clock in the PMA for line 0, 1 - enable Line 0 PLL clock. 0 - disable PLL clock. |

8.5.215 EDP_CORE_PMA_PLLCLK_EN_ACK_P Register (Offset = 00030A28h) [reset = 0h]

EDP_CORE_PMA_PLLCLK_EN_ACK_P is shown in [Figure 8-271](#) and described in [Table 8-552](#).

Return to [Summary Table](#).

PHY Link PLL Clock Status Register

Table 8-551. EDP_CORE_PMA_PLLCLK_EN_ACK_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A28h |

Figure 8-271. EDP_CORE_PMA_PLLCLK_EN_ACK_P Register

| | | | | | | | |
|----------|----|----|----|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | PMA_XCVR_P LLCLK_EN_AC K_LN_3 | PMA_XCVR_P LLCLK_EN_AC K_LN_2 | PMA_XCVR_P LLCLK_EN_AC K_LN_1 | PMA_XCVR_P LLCLK_EN_AC K_LN_0 |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-552. EDP_CORE_PMA_PLLCLK_EN_ACK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 3 | PMA_XCVR_PLLCLK_EN _ACK_LN_3 | R | 0h | Link PLL clock enable acknowledgement, indicates whether the data rate clock in the PMA for line 3 is running. Active HIGH. |
| 2 | PMA_XCVR_PLLCLK_EN _ACK_LN_2 | R | 0h | Link PLL clock enable acknowledgement, indicates whether the data rate clock in the PMA for line 2 is running. Active HIGH. |
| 1 | PMA_XCVR_PLLCLK_EN _ACK_LN_1 | R | 0h | Link PLL clock enable acknowledgement, indicates whether the data rate clock in the PMA for line 1 is running. Active HIGH. |
| 0 | PMA_XCVR_PLLCLK_EN _ACK_LN_0 | R | 0h | Link PLL clock enable acknowledgement, indicates whether the data rate clock in the PMA for line 0 is running. Active HIGH. |

8.5.216 EDP_CORE_PMA_POWER_STATE_REQ_P Register (Offset = 00030A2Ch) [reset = 0h]

EDP_CORE_PMA_POWER_STATE_REQ_P is shown in [Figure 8-272](#) and described in [Table 8-554](#).

Return to [Summary Table](#).

PHY Link Power State Request Register. Please refer to PHY Specification for detailed power state values

Table 8-553.
EDP_CORE_PMA_POWER_STATE_REQ_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A2Ch |

Figure 8-272. EDP_CORE_PMA_POWER_STATE_REQ_P Register

| | | | | | | | |
|----------|----|-------------------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | PMA_XCVR_POWER_STATE_REQ_LN_3 | | | | | |
| R-0h | | R/W-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | PMA_XCVR_POWER_STATE_REQ_LN_2 | | | | | |
| R-0h | | R/W-0h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | PMA_XCVR_POWER_STATE_REQ_LN_1 | | | | | |
| R-0h | | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | PMA_XCVR_POWER_STATE_REQ_LN_0 | | | | | |
| R-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-554. EDP_CORE_PMA_POWER_STATE_REQ_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 29-24 | PMA_XCVR_POWER_STATE_REQ_LN_3 | R/W | 0h | Change the link power state. When the link has completed the transition to the requested power state, the state will be reflected on pma_xcvr_power_state_ack_ln_3. |
| 23-22 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 21-16 | PMA_XCVR_POWER_STATE_REQ_LN_2 | R/W | 0h | Change the link power state. When the link has completed the transition to the requested power state, the state will be reflected on pma_xcvr_power_state_ack_ln_2. |
| 15-14 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |

Table 8-554. EDP_CORE_PMA_POWER_STATE_REQ_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|--|
| 13-8 | PMA_XCVR_POWER_STATE_REQ_LN_1 | R/W | 0h | Change the link power state. When the link has completed the transition to the requested power state, the state will be reflected on pma_xcvr_power_state_ack_ln_1. |
| 7-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 5-0 | PMA_XCVR_POWER_STATE_REQ_LN_0 | R/W | 0h | Change the link power state. When the link has completed the transition to the requested power state, the state will be reflected on pma_xcvr_power_state_ack_ln_0. |

8.5.217 EDP_CORE_PMA_POWER_STATE_ACK_P Register (Offset = 00030A30h) [reset = 0h]

EDP_CORE_PMA_POWER_STATE_ACK_P is shown in [Figure 8-273](#) and described in [Table 8-556](#).

Return to [Summary Table](#).

PHY Link Power State Status Register

Table 8-555.
EDP_CORE_PMA_POWER_STATE_ACK_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A30h |

Figure 8-273. EDP_CORE_PMA_POWER_STATE_ACK_P Register

| | | | | | | | |
|----------|----|----|----|-------------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | PMA_XCVR_POWER_STATE_ACK_LN_3 | | | |
| R-0h | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | PMA_XCVR_POWER_STATE_ACK_LN_2 | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | PMA_XCVR_POWER_STATE_ACK_LN_1 | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | PMA_XCVR_POWER_STATE_ACK_LN_0 | | | |
| R-0h | | | | R-0h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-556. EDP_CORE_PMA_POWER_STATE_ACK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 29-24 | PMA_XCVR_POWER_STATE_ACK_LN_3 | R | 0h | Link power state acknowledgement, this signal provides indication that a power state change request has completed. |
| 23-22 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 21-16 | PMA_XCVR_POWER_STATE_ACK_LN_2 | R | 0h | Link power state acknowledgement, this signal provides indication that a power state change request has completed. |
| 15-14 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 13-8 | PMA_XCVR_POWER_STATE_ACK_LN_1 | R | 0h | Link power state acknowledgement, this signal provides indication that a power state change request has completed. |

Table 8-556. EDP_CORE_PMA_POWER_STATE_ACK_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|------|-------|--|
| 7-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 5-0 | PMA_XCVR_POWER_STATE_ACK_LN_0 | R | 0h | Link power state acknowledgement, this signal provides indication that a power state change request has completed. |

8.5.218 EDP_CORE_PMA_CMN_READY_P Register (Offset = 00030A34h) [reset = 0h]

EDP_CORE_PMA_CMN_READY_P is shown in [Figure 8-274](#) and described in [Table 8-558](#).

Return to [Summary Table](#).

PMA Operation Status Register

Table 8-557. EDP_CORE_PMA_CMN_READY_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A34h |

Figure 8-274. EDP_CORE_PMA_CMN_READY_P Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PMA_CMN_READY |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-558. EDP_CORE_PMA_CMN_READY_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 0 | PMA_CMN_READY | R | 0h | PMA common ready, 1 = PMA common is ready for operation. Used as part of Raw SerDes startup sequence and power state changes. |

8.5.219 EDP_CORE_PMA_TX_VMARGIN_P Register (Offset = 00030A38h) [reset = 0h]

EDP_CORE_PMA_TX_VMARGIN_P is shown in [Figure 8-275](#) and described in [Table 8-560](#).

Return to [Summary Table](#).

PMA Tx Voltage Margin Control Register. Please refer to PHY Specification for Voltage Margin settings.

**Table 8-559. EDP_CORE_PMA_TX_VMARGIN_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A38h |

Figure 8-275. EDP_CORE_PMA_TX_VMARGIN_P Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | PMA_TX_VMARGIN_LN_3 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | PMA_TX_VMARGIN_LN_2 | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | PMA_TX_VMARGIN_LN_1 | |
| R-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | PMA_TX_VMARGIN_LN_0 | |
| R-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-560. EDP_CORE_PMA_TX_VMARGIN_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 25-24 | PMA_TX_VMARGIN_LN_3 | R/W | 0h | Drives PMA input tx_vmargin_ln_3 for the associated lane. Drive with desired initial transit margin upon de-assertion of phy_reset_n. |
| 23-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 17-16 | PMA_TX_VMARGIN_LN_2 | R/W | 0h | Drives PMA input tx_vmargin_ln_2 for the associated lane. Drive with desired initial transit margin upon de-assertion of phy_reset_n. |
| 15-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 9-8 | PMA_TX_VMARGIN_LN_1 | R/W | 0h | Drives PMA input tx_vmargin_ln_1 for the associated lane. Drive with desired initial transit margin upon de-assertion of phy_reset_n. |

Table 8-560. EDP_CORE_PMA_TX_VMARGIN_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 1-0 | PMA_TX_VMARGIN_LN_0 | R/W | 0h | Drives PMA input tx_vmargln_0 for the associated lane. Drive with desired initial transit margin upon de-assertion of phy_reset_n. |

8.5.220 EDP_CORE_PMA_TX_DEEMPH_P Register (Offset = 00030A3Ch) [reset = 0h]

EDP_CORE_PMA_TX_DEEMPH_P is shown in [Figure 8-276](#) and described in [Table 8-562](#).

Return to [Summary Table](#).

PMA Tx Deemphasis Level Control Register. Please refer to PHY Specification for Deemphasis Level settings.

Table 8-561. EDP_CORE_PMA_TX_DEEMPH_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A3Ch |

Figure 8-276. EDP_CORE_PMA_TX_DEEMPH_P Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | PMA_TX_DEEMPHASIS_LN_3 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | PMA_TX_DEEMPHASIS_LN_2 | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | PMA_TX_DEEMPHASIS_LN_1 | |
| R-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | PMA_TX_DEEMPHASIS_LN_0 | |
| R-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-562. EDP_CORE_PMA_TX_DEEMPH_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 25-24 | PMA_TX_DEEMPHASIS_LN_3 | R/W | 0h | Drives PMA input tx_deemphasis_in_3 for the associated lane. Drives with desired initial deemphasis setting upon de-assertion of phy_reset_n. |
| 23-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 17-16 | PMA_TX_DEEMPHASIS_LN_2 | R/W | 0h | Drives PMA input tx_deemphasis_in_2 for the associated lane. Drives with desired initial deemphasis setting upon de-assertion of phy_reset_n. |
| 15-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 9-8 | PMA_TX_DEEMPHASIS_LN_1 | R/W | 0h | Drives PMA input tx_deemphasis_in_1 for the associated lane. Drives with desired initial deemphasis setting upon de-assertion of phy_reset_n. |

Table 8-562. EDP_CORE_PMA_TX_DEEMPH_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|--|
| 7-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. ignored on write. |
| 1-0 | PMA_TX_DEEMPHASIS_LN_0 | R/W | 0h | Drives PMA input tx_deemphasis_ln_0 for the associated lane. Drives with desired initial deemphasis setting upon de-assertion of phy_reset_n. |

8.5.221 EDP_CORE_ASF_IPS_CTRL Register (Offset = 00030A60h) [reset = 1h]

EDP_CORE_ASF_IPS_CTRL is shown in [Figure 8-277](#) and described in [Table 8-564](#).

Return to [Summary Table](#).

ASF control register, implemented only when ASF support is enabled in IP configuration

Table 8-563. EDP_CORE_ASF_IPS_CTRL Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0A60h |

Figure 8-277. EDP_CORE_ASF_IPS_CTRL Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | IF_ADDR_PAR CHECK_EN |
| R-0h | | | | | | | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-564. EDP_CORE_ASF_IPS_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 0 | IF_ADDR_PARCHECK_EN | R/W | 1h | When set, enables parity check at APB/SAPB address bus. This bit should be enabled during normal operation but disabled in test mode when internal parity checkers are verified |

8.5.222 EDP_CORE_ASF_INT_STATUS Register (Offset = 00030B00h) [reset = 0h]

EDP_CORE_ASF_INT_STATUS is shown in [Figure 8-278](#) and described in [Table 8-566](#).

Return to [Summary Table](#).

ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_fatal or asf_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 8-565. EDP_CORE_ASF_INT_STATUS Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B00h |

Figure 8-278. EDP_CORE_ASF_INT_STATUS Register

| | | | | | | | |
|----------|-------------------|------------------|-----------------------------|-------------|-------------|----------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_TIMEOUT_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORRECTABLE_ERR | ASF_SRAM_CORRECTABLE_ERR |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-566. EDP_CORE_ASF_INT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | ASF_INTEGRITY_ERR | R/W | 0h | Integrity error interrupt, 1 is active, 0 is not active |
| 5 | ASF_PROTOCOL_ERR | R/W | 0h | Protocol error interrupt, 1 is active, 0 is not active |
| 4 | ASF_TRANSACTION_TIMEOUT_ERR | R/W | 0h | Transaction timeouts error interrupt, 1 is active, 0 is not active |
| 3 | ASF_CSR_ERR | R/W | 0h | Configuration and status registers error interrupt, 1 is active, 0 is not active |
| 2 | ASF_DAP_ERR | R/W | 0h | Data and address paths parity error interrupt, 1 is active, 0 is not active |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR | R/W | 0h | SRAM uncorrectable error interrupt, 1 is active, 0 is not active |
| 0 | ASF_SRAM_CORRECTABLE_ERR | R/W | 0h | SRAM correctable error interrupt, 1 is active, 0 is not active |

8.5.223 EDP_CORE_ASF_INT_RAW_STATUS Register (Offset = 00030B04h) [reset = 0h]

EDP_CORE_ASF_INT_RAW_STATUS is shown in [Figure 8-279](#) and described in [Table 8-568](#).

Return to [Summary Table](#).

ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 8-567. EDP_CORE_ASF_INT_RAW_STATUS Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B04h |

Figure 8-279. EDP_CORE_ASF_INT_RAW_STATUS Register

| | | | | | | | |
|----------|------------------|------------------|---------------------|-------------|-------------|---------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | SF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORR_ERR | ASF_SRAM_CORR_ERR |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-568. EDP_CORE_ASF_INT_RAW_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | SF_INTEGRITY_ERR | R/W | 0h | Integrity error interrupt, 1 is active, 0 is not active |
| 5 | ASF_PROTOCOL_ERR | R/W | 0h | Protocol error interrupt, 1 is active, 0 is not active |
| 4 | ASF_TRANSACTION_ERR | R/W | 0h | Transaction timeouts error interrupt, 1 is active, 0 is not active |
| 3 | ASF_CSR_ERR | R/W | 0h | Configuration and status registers error interrupt, 1 is active, 0 is not active |
| 2 | ASF_DAP_ERR | R/W | 0h | Data and address paths parity error interrupt, 1 is active, 0 is not active |
| 1 | ASF_SRAM_UNCORR_ERR | R/W | 0h | SRAM uncorrectable error interrupt, 1 is active, 0 is not active |
| 0 | ASF_SRAM_CORR_ERR | R/W | 0h | SRAM correctable error interrupt, 1 is active, 0 is not active |

8.5.224 EDP_CORE_ASF_INT_MASK Register (Offset = 00030B08h) [reset = 7Fh]

EDP_CORE_ASF_INT_MASK is shown in [Figure 8-280](#) and described in [Table 8-570](#).

Return to [Summary Table](#).

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt.

Table 8-569. EDP_CORE_ASF_INT_MASK Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B08h |

Figure 8-280. EDP_CORE_ASF_INT_MASK Register

| | | | | | | | |
|----------|------------------------|-----------------------|--------------------------|------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR_MASK | ASF_PROTOCOL_ERR_MASK | ASF_TRANSACTION_ERR_MASK | ASF_CSR_ERR_MASK | ASF_DAP_ERR_MASK | ASF_SRAM_UNCORR_ERR_MASK | ASF_SRAM_CORR_ERR_MASK |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-570. EDP_CORE_ASF_INT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | ASF_INTEGRITY_ERR_MASK | R/W | 1h | Mask bit for Integrity error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 5 | ASF_PROTOCOL_ERR_MASK | R/W | 1h | Mask bit for Protocol error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 4 | ASF_TRANSACTION_ERR_MASK | R/W | 1h | Mask bit for Transaction timeouts error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 3 | ASF_CSR_ERR_MASK | R/W | 1h | Mask bit for Configuration and status registers error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |

Table 8-570. EDP_CORE_ASF_INT_MASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|---|
| 2 | ASF_DAP_ERR_MASK | R/W | 1h | Mask bit for Data and address paths parity error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 1 | ASF_SRAM_UNCORR_ERR_MASK | R/W | 1h | Mask bit for SRAM uncorrectable error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 0 | ASF_SRAM_CORR_ERR_MASK | R/W | 1h | Mask bit for SRAM correctable error interrupt, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |

8.5.225 EDP_CORE_ASF_INT_TEST Register (Offset = 00030B0Ch) [reset = 0h]

EDP_CORE_ASF_INT_TEST is shown in [Figure 8-281](#) and described in [Table 8-572](#).

Return to [Summary Table](#).

The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrupt accordingly.

Table 8-571. EDP_CORE_ASF_INT_TEST Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B0Ch |

Figure 8-281. EDP_CORE_ASF_INT_TEST Register

| | | | | | | | |
|----------|----------------------------|---------------------------|---------------------------|----------------------|----------------------|----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRIT Y_ERR_TEST | ASF_PROTOC OL_ERR_TEST | ASF_TRANS_T O_ERR_TEST | ASF_CSR_ER R_TEST | ASF_DAP_ERR _TEST | ASF_SRAM_U NCORR_ERR_ TEST | ASF_SRAM_C ORR_ERR_TE ST |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-572. EDP_CORE_ASF_INT_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|------|-------|---|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | ASF_INTEGRITY_ERR_T EST | R/W | 0h | Test bit for Integrity error interrupt, 1 is active, 0 is not active |
| 5 | ASF_PROTOCOL_ERR_ TEST | R/W | 0h | Test bit for Protocol error interrupt, 1 is active, 0 is not active |
| 4 | ASF_TRANS_TO_ERR_T EST | R/W | 0h | Test bit for Transaction timeouts error interrupt, 1 is active, 0 is not active |
| 3 | ASF_CSR_ERR_TEST | R/W | 0h | Test bit for Configuration and status registers error interrupt, 1 is active, 0 is not active |
| 2 | ASF_DAP_ERR_TEST | R/W | 0h | Test bit for Data and address paths parity error interrupt, 1 is active, 0 is not active |
| 1 | ASF_SRAM_UNCORR_E RR_TEST | R/W | 0h | Test bit for SRAM uncorrectable error interrupt, 1 is active, 0 is not active |
| 0 | ASF_SRAM_CORR_ERR _TEST | R/W | 0h | Test bit for SRAM correctable error interrupt, 1 is active, 0 is not active |

8.5.226 EDP_CORE_ASF_FATAL_NONFATAL_SELECT Register (Offset = 00030B10h) [reset = 7Fh]

EDP_CORE_ASF_FATAL_NONFATAL_SELECT is shown in [Figure 8-282](#) and described in [Table 8-574](#).

Return to [Summary Table](#).

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered.

Table 8-573.
EDP_CORE_ASF_FATAL_NONFATAL_SELECT
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B10h |

Figure 8-282. EDP_CORE_ASF_FATAL_NONFATAL_SELECT Register

| | | | | | | | |
|----------|-----------------------|----------------------|----------------------|-----------------|-------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRIT Y_ERR | ASF_PROTOL OL_ERR | ASF_TRANS_T O_ERR | ASF_CSR_ER R | ASF_DAP_ERR | ASF_SRAM_U NCORR_ERR | ASF_SRAM_C ORR_ERR |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-574. EDP_CORE_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 6 | ASF_INTEGRITY_ERR | R/W | 1h | Enable Integrity error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |
| 5 | ASF_PROTOCOL_ERR | R/W | 1h | Enable Protocol error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |
| 4 | ASF_TRANS_TO_ERR | R/W | 1h | Enable Transaction timeouts error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |
| 3 | ASF_CSR_ERR | R/W | 1h | Enable Configuration and status registers error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |
| 2 | ASF_DAP_ERR | R/W | 1h | Enable Data and address paths parity error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |
| 1 | ASF_SRAM_UNCORR_ERR | R/W | 1h | Enable SRAM uncorrectable error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |

Table 8-574. EDP_CORE_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 0 | ASF_SRAM_CORR_ERR | R/W | 1h | Enable SRAM correctable error interrupt as fatal, 1 is fatal interrupt, 0 is non-fatal |

8.5.227 EDP_CORE_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 00030B20h) [reset = 0h]

EDP_CORE_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 8-283](#) and described in [Table 8-576](#).

Return to [Summary Table](#).

Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active.

Table 8-575.
EDP_CORE_ASF_SRAM_CORR_FAULT_STATUS
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B20h |

Figure 8-283. EDP_CORE_ASF_SRAM_CORR_FAULT_STATUS Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|--------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_CORR_FAULT_INST | | | | | | | | ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-576. EDP_CORE_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-24 | ASF_SRAM_CORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault |
| 23-0 | ASF_SRAM_CORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault |

8.5.228 EDP_CORE_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 00030B24h) [reset = 0h]

EDP_CORE_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 8-284](#) and described in [Table 8-578](#).

Return to [Summary Table](#).

Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active.

Table 8-577.
EDP_CORE_ASF_SRAM_UNCORR_FAULT_STATUS
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B24h |

Figure 8-284. EDP_CORE_ASF_SRAM_UNCORR_FAULT_STATUS Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_SRAM_UNCORR_FAULT_INST | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-578. EDP_CORE_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-24 | ASF_SRAM_UNCORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault |
| 23-0 | ASF_SRAM_UNCORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault |

8.5.229 EDP_CORE_ASF_SRAM_FAULT_STATUS Register (Offset = 00030B28h) [reset = 0h]

EDP_CORE_ASF_SRAM_FAULT_STATUS is shown in [Figure 8-285](#) and described in [Table 8-580](#).

Return to [Summary Table](#).

Statistics register for SRAM faults. Note that this register clears when software writes to any field.

Table 8-579.
EDP_CORE_ASF_SRAM_FAULT_STATUS Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B28h |

Figure 8-285. EDP_CORE_ASF_SRAM_FAULT_STATUS Register

| | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_FAULT_UNCORR_STATS | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_FAULT_CORR_STATS | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-580. EDP_CORE_ASF_SRAM_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-16 | ASF_SRAM_FAULT_UNCORR_STATS | R/W | 0h | Count of number of uncorrectable errors if implemented. Count value will saturate at 0xffff |
| 15-0 | ASF_SRAM_FAULT_CORR_STATS | R/W | 0h | Count of number of correctable errors if implemented. Count value will saturate at 0xffff |

8.5.230 EDP_CORE_ASF_TRANS_TO_CTRL Register (Offset = 00030B30h) [reset = 0h]

EDP_CORE_ASF_TRANS_TO_CTRL is shown in [Figure 8-286](#) and described in [Table 8-582](#).

Return to [Summary Table](#).

Control register to configure the ASF transaction timeout monitors.

Table 8-581. EDP_CORE_ASF_TRANS_TO_CTRL Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B30h |

Figure 8-286. EDP_CORE_ASF_TRANS_TO_CTRL Register

| | | | | | | | |
|---------------------|----------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_TRANS_T O_EN | RESERVED | | | | | | |
| R/W-0h | R-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-582. EDP_CORE_ASF_TRANS_TO_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31 | ASF_TRANS_TO_EN | R/W | 0h | Enable transaction timeout monitoring, 1 is active, 0 is not active |
| 30-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 15-0 | ASF_TRANS_TO_CTRL | R/W | 0h | Timer value to use for transaction timeout monitor |

8.5.231 EDP_CORE_ASF_TRANS_TO_FAULT_MASK Register (Offset = 00030B34h) [reset = 7h]

EDP_CORE_ASF_TRANS_TO_FAULT_MASK is shown in [Figure 8-287](#) and described in [Table 8-584](#).

Return to [Summary Table](#).

Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 8-583.
EDP_CORE_ASF_TRANS_TO_FAULT_MASK
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B34h |

Figure 8-287. EDP_CORE_ASF_TRANS_TO_FAULT_MASK Register

| | | | | | | | |
|----------|----|----|----|----|-----------------------------------|-----------------------------------|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | ASF_TRANS_T O_FAULT_2_M ASK | ASF_TRANS_T O_FAULT_1_M ASK | ASF_TRANS_T O_FAULT_0_M ASK |
| R-0h | | | | | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-584. EDP_CORE_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 2 | ASF_TRANS_TO_FAULT_2_MASK | R/W | 1h | Mask bit for SAPB interface for transaction timeout fault, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 1 | ASF_TRANS_TO_FAULT_1_MASK | R/W | 1h | Mask bit for APB interface for transaction timeout fault, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |
| 0 | ASF_TRANS_TO_FAULT_0_MASK | R/W | 1h | Mask bit for Xtensa watchdog error for transaction timeout fault, 0 is active, 1 is not active. Interrupt from source which mask is 0 is permitted, otherwise interrupt is not permitted |

8.5.232 EDP_CORE_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 00030B38h) [reset = 0h]

EDP_CORE_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 8-288](#) and described in [Table 8-586](#).

Return to [Summary Table](#).

Status register for transaction timeouts fault. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit.

Table 8-585.
EDP_CORE_ASF_TRANS_TO_FAULT_STATUS
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B38h |

Figure 8-288. EDP_CORE_ASF_TRANS_TO_FAULT_STATUS Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------------------|-------------------------------------|-------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | ASF_TRANS_T O_FAULT_2_S TATUS | ASF_TRANS_T O_FAULT_1_S TATUS | ASF_TRANS_T O_FAULT_0_S TATUS |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-586. EDP_CORE_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 2 | ASF_TRANS_TO_FAULT_2_STATUS | R/W | 0h | Status bits for SAPB interface for transaction timeout fault, 1 is active, 0 is not active |
| 1 | ASF_TRANS_TO_FAULT_1_STATUS | R/W | 0h | Status bits for APB interface for transaction timeout fault, 1 is active, 0 is not active |
| 0 | ASF_TRANS_TO_FAULT_0_STATUS | R/W | 0h | Status bits for Xtensa watchdog error for transaction timeout fault, 1 is active, 0 is not active |

8.5.233 EDP_CORE_ASF_PROTOCOL_FAULT_MASK Register (Offset = 00030B40h) [reset = Fh]

EDP_CORE_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 8-289](#) and described in [Table 8-588](#).

Return to [Summary Table](#).

Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 8-587.
EDP_CORE_ASF_PROTOCOL_FAULT_MASK
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B40h |

Figure 8-289. EDP_CORE_ASF_PROTOCOL_FAULT_MASK Register

| | | | | | | | |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ASF_PROTOL_FAULT_3_MASK | ASF_PROTOL_FAULT_2_MASK | ASF_PROTOL_FAULT_1_MASK | ASF_PROTOL_FAULT_0_MASK |
| R-0h | | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-588. EDP_CORE_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | ASF_PROTOCOL_FAULT_3_MASK | R/W | 1h | Mask bit for FEC FSM fault. When 0 interrupt is enabled. |
| 2 | ASF_PROTOCOL_FAULT_2_MASK | R/W | 1h | Mask bit for 8b10b Encoding fault from FEC module. When 0 interrupt is enabled. |
| 1 | ASF_PROTOCOL_FAULT_1_MASK | R/W | 1h | Mask bit for Parity Encoding fault from FEC module. When 0 interrupt is enabled. |
| 0 | ASF_PROTOCOL_FAULT_0_MASK | R/W | 1h | Mask bit for Parity Generation fault from FEC module. When 0 interrupt is enabled. |

8.5.234 EDP_CORE_ASF_PROTOCOL_FAULT_STATUS Register (Offset = 00030B44h) [reset = 0h]

EDP_CORE_ASF_PROTOCOL_FAULT_STATUS is shown in [Figure 8-290](#) and described in [Table 8-590](#).

Return to [Summary Table](#).

Status register for protocol faults. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit

Table 8-589.
EDP_CORE_ASF_PROTOCOL_FAULT_STATUS
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0B44h |

Figure 8-290. EDP_CORE_ASF_PROTOCOL_FAULT_STATUS Register

| | | | | | | | |
|----------|----|----|----|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ASF_PROTOCOL_FAULT_3_STATUS | ASF_PROTOCOL_FAULT_2_STATUS | ASF_PROTOCOL_FAULT_1_STATUS | ASF_PROTOCOL_FAULT_0_STATUS |
| R-0h | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-590. EDP_CORE_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read. |
| 3 | ASF_PROTOCOL_FAULT_3_STATUS | R/W | 0h | FEC symbol injection fault. Active HIGH. Asserted when FEC FSM is in unexpected state. |
| 2 | ASF_PROTOCOL_FAULT_2_STATUS | R/W | 0h | 8b10b Encoding fault in FEC module. Active HIGH. Asserted when fault in 8b10b encoding is detected. |
| 1 | ASF_PROTOCOL_FAULT_1_STATUS | R/W | 0h | Parity Encoding fault in FEC module. Active HIGH. Asserted when fault in RS parity encoding is detected. |
| 0 | ASF_PROTOCOL_FAULT_0_STATUS | R/W | 0h | Parity Generation fault in FEC module. Active HIGH. Asserted when fault in RS parity generation is detected. |

8.5.235 EDP_CORE_COM_MAIN_CONF_P Register (Offset = 00030C00h) [reset = 0h]

EDP_CORE_COM_MAIN_CONF_P is shown in [Figure 8-291](#) and described in [Table 8-592](#).

Return to [Summary Table](#).

Encoder common configuration values

Table 8-591. EDP_CORE_COM_MAIN_CONF_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0C00h |

Figure 8-291. EDP_CORE_COM_MAIN_CONF_P Register

| | | | | | | | |
|----------|---------------------|---------------------------|------------|-----------------------|------------------------|---------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | AUTO_REGS_DB_UPDATE | MULTIPLEX_MODE_EOC_ENABLE | INPUT_MODE | REGS_DE_RASTER_ENABLE | REGS_MULTIPLEX_SEL_OUT | REGS_MULTIPLEX_MODE | REGS_SPLIT_PANEL |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-592. EDP_CORE_COM_MAIN_CONF_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 6 | AUTO_REGS_DB_UPDATE | R/W | 0h | Active-High to enable auto update double buffer regs on vsync falling edge. Only available when input_mode=1 [DPI mode] |
| 5 | MULTIPLEX_MODE_EOC_ENABLE | R/W | 0h | When split_panel and multiplex_mode are set, indicates that multiplexer output separated chunks [inserts zeros on partial words at each end of chunk] and signal end of chunks. Active high |
| 4 | INPUT_MODE | R/W | 0h | Video input interface mode: 0: Native 1: DPI. Input mode set to DPI automatically enable the internal Auto Start Of Frame |
| 3 | REGS_DE_RASTER_ENABLE | R/W | 0h | Indicates if the De-Rasterization Buffer is used or bypassed: '1' Active '0' Bypassed |
| 2 | REGS_MULTIPLEX_SEL_OUT | R/W | 0h | When split_panel and multiplex_mode are set, indicates to which output the multiplexed stream is sent: '0': enc0_data_out '1': enc1_data_out |

Table 8-592. EDP_CORE_COM_MAIN_CONF_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 1 | REGS_MULTIPLEX_MODE | R/W | 0h | Active-High, indicates that both encoders are used to produce a multiplex stream on a single Transport link. When set, split_panel must also be set. |
| 0 | REGS_SPLIT_PANEL | R/W | 0h | Active-High, indicates that both encoders are used in parallel for one video stream [L and R split]. When set, the effective width of each encoder is halved [as each encoder is operating on half of the encx_picture_width]. In addition, the ICH is cleared at the end of each line. |

8.5.236 EDP_CORE_ENC0_MAIN_CONF_P Register (Offset = 00030D20h) [reset = 0F000004h]

EDP_CORE_ENC0_MAIN_CONF_P is shown in [Figure 8-292](#) and described in [Table 8-594](#).

Return to [Summary Table](#).

Encoder Main Configuration values

Table 8-593. EDP_CORE_ENC0_MAIN_CONF_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D20h |

Figure 8-292. EDP_CORE_ENC0_MAIN_CONF_P Register

| | | | | | | | |
|----------------|----|----|-------------|------------|-------------------|----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INITIAL_LINES | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | ICH_RST_EOL | VIDEO_MODE | BLOCK_PRED_ENABLE | BITS_PER_PIXEL | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BITS_PER_PIXEL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINEBUF_DEPTH | | | | ENABLE_422 | CONVERT_RGB | INPUT_BPC | |
| R/W-0h | | | | R/W-0h | R/W-1h | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-594. EDP_CORE_ENC0_MAIN_CONF_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31-24 | INITIAL_LINES | R/W | Fh | Number of lines to wait before initiating transport in Command Mode. |
| 23-21 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 20 | ICH_RST_EOL | R/W | 0h | Forces the ICH to reset at EOL [when not in split mode]. |
| 19 | VIDEO_MODE | R/W | 0h | MIPI Video/Command mode: '0' Command mode '1' Video mode |
| 18 | BLOCK_PRED_ENABLE | R/W | 0h | Active-High input Block Prediction Enable |
| 17-8 | BITS_PER_PIXEL | R/W | 0h | Target bits per pixel. The value is in 6.4 format [4 LSBs for fractional part, they should be 0000] |
| 7-4 | LINEBUF_DEPTH | R/W | 0h | Depth of the line buffer used by the decoder [i.e., the number of bits stored for each component of the pixels on the previous line] |
| 3 | ENABLE_422 | R/W | 0h | Active-High input to indicate the data_in pixels are 4:2:2 sub-sampled. This input is valid only when convert_rgb is low. NOT SUPPORTED, MUST BE SET TO '0' |
| 2 | CONVERT_RGB | R/W | 1h | Active-High input to indicate the data_in pixels are RGB. When set to low input, it is YUV and does not require conversion. |

Table 8-594. EDP_CORE_ENC0_MAIN_CONF_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 1-0 | INPUT_BPC | R/W | 0h | Indicates the current input pixel stream bits per component: 00: input is 8 bits/component 01: input is 10 bits/component |

8.5.237 EDP_CORE_ENC0_PICTURE_SIZE_P Register (Offset = 00030D24h) [reset = 0h]

EDP_CORE_ENC0_PICTURE_SIZE_P is shown in [Figure 8-293](#) and described in [Table 8-596](#).

Return to [Summary Table](#).

Encoder Picture configuration

**Table 8-595. EDP_CORE_ENC0_PICTURE_SIZE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D24h |

Figure 8-293. EDP_CORE_ENC0_PICTURE_SIZE_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PICTURE_HEIGHT | | | | | | | | | | | | | | | | PICTURE_WIDTH | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-596. EDP_CORE_ENC0_PICTURE_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|----------------|
| 31-16 | PICTURE_HEIGHT | R/W | 0h | Picture height |
| 15-0 | PICTURE_WIDTH | R/W | 0h | Picture width |

8.5.238 EDP_CORE_ENC0_SLICE_SIZE_P Register (Offset = 00030D28h) [reset = 0h]

EDP_CORE_ENC0_SLICE_SIZE_P is shown in [Figure 8-294](#) and described in [Table 8-598](#).

Return to [Summary Table](#).

Encoder Slice(s) configuration

Table 8-597. EDP_CORE_ENC0_SLICE_SIZE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D28h |

Figure 8-294. EDP_CORE_ENC0_SLICE_SIZE_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLICE_HEIGHT | | | | | | | | | | | | | | | | SLICE_WIDTH | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-598. EDP_CORE_ENC0_SLICE_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--------------|
| 31-16 | SLICE_HEIGHT | R/W | 0h | Slice height |
| 15-0 | SLICE_WIDTH | R/W | 0h | Slice width |

8.5.239 EDP_CORE_ENC0_MISC_SIZE_P Register (Offset = 00030D2Ch) [reset = FFFCh]

EDP_CORE_ENC0_MISC_SIZE_P is shown in [Figure 8-295](#) and described in [Table 8-600](#).

Return to [Summary Table](#).

Encoder Group, Output Buffer(s), and Transport Chunk Size

**Table 8-599. EDP_CORE_ENC0_MISC_SIZE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D2Ch |

Figure 8-295. EDP_CORE_ENC0_MISC_SIZE_P Register

| | | | | | | | |
|-------------|----|----|----|----|----|-----------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CHUNK_SIZE | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CHUNK_SIZE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OB_MAX_ADDR | | | | | | | |
| R/W-3FFFh | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OB_MAX_ADDR | | | | | | SLICE_LAST_GROUP_SIZE | |
| R/W-3FFFh | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-600. EDP_CORE_ENC0_MISC_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-16 | CHUNK_SIZE | R/W | 0h | Chunk size in bytes |
| 15-2 | OB_MAX_ADDR | R/W | 3FFFh | Output Buffer[s] max pointer address[es] |
| 1-0 | SLICE_LAST_GROUP_SIZE | R/W | 0h | Size of last group of the slice line [0-based]: 0 = 1 pixel, 1 = 2 pixels, 2 = 3 pixels [slice_width + 2] % 3 |

8.5.240 EDP_CORE_ENC0_HRD_DELAYS_P Register (Offset = 00030D30h) [reset = 0h]

EDP_CORE_ENC0_HRD_DELAYS_P is shown in [Figure 8-296](#) and described in [Table 8-602](#).

Return to [Summary Table](#).

Hypothetical Reference Decoder delays

Table 8-601. EDP_CORE_ENC0_HRD_DELAYS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D30h |

Figure 8-296. EDP_CORE_ENC0_HRD_DELAYS_P Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INITIAL_DEC_DELAY | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | INITIAL_XMIT_DELAY | | | | | | | | | |
| R-0h | | | | | | R/W-0h | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-602. EDP_CORE_ENC0_HRD_DELAYS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-16 | INITIAL_DEC_DELAY | R/W | 0h | Initial Decoder delay |
| 15-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 9-0 | INITIAL_XMIT_DELAY | R/W | 0h | Initial Decoder Transmit delay |

8.5.241 EDP_CORE_ENC0_RC_SCALE_P Register (Offset = 00030D34h) [reset = 0h]

EDP_CORE_ENC0_RC_SCALE_P is shown in [Figure 8-297](#) and described in [Table 8-604](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Scale value

**Table 8-603. EDP_CORE_ENC0_RC_SCALE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D34h |

Figure 8-297. EDP_CORE_ENC0_RC_SCALE_P Register

| | | | | | | | |
|----------|----|---------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | INITIAL_SCALE_VALUE | | | | | |
| R-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-604. EDP_CORE_ENC0_RC_SCALE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 5-0 | INITIAL_SCALE_VALUE | R/W | 0h | Three fractional bits |

8.5.242 EDP_CORE_ENC0_RC_SCALE_INC_DEC_P Register (Offset = 00030D38h) [reset = 0h]

EDP_CORE_ENC0_RC_SCALE_INC_DEC_P is shown in [Figure 8-298](#) and described in [Table 8-606](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Increment and Decrement Scale values

Table 8-605.
EDP_CORE_ENC0_RC_SCALE_INC_DEC_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D38h |

Figure 8-298. EDP_CORE_ENC0_RC_SCALE_INC_DEC_P Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|--------------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | SCALE_DECREMENT_INTERVAL | | | | | | | | | | | |
| R-0h | | | | R/W-0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCALE_INCREMENT_INTERVAL | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-606. EDP_CORE_ENC0_RC_SCALE_INC_DEC_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 27-16 | SCALE_DECREMENT_INTERVAL | R/W | 0h | RC scale decrement value |
| 15-0 | SCALE_INCREMENT_INTERVAL | R/W | 0h | RC scale increment value |

8.5.243 EDP_CORE_ENC0_RC_OFFSETS_1_P Register (Offset = 00030D3Ch) [reset = 0h]

EDP_CORE_ENC0_RC_OFFSETS_1_P is shown in [Figure 8-299](#) and described in [Table 8-608](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Various Offset control values 1

**Table 8-607. EDP_CORE_ENC0_RC_OFFSETS_1_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D3Ch |

Figure 8-299. EDP_CORE_ENC0_RC_OFFSETS_1_P Register

| | | | | | | | |
|----------|----|----|----|-----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | FIRST_LINE_BPG_OFFSET | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-608. EDP_CORE_ENC0_RC_OFFSETS_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|---|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 4-0 | FIRST_LINE_BPG_OFFSET | R/W | 0h | First Line |

8.5.244 EDP_CORE_ENC0_RC_OFFSETS_2_P Register (Offset = 00030D40h) [reset = 0h]

EDP_CORE_ENC0_RC_OFFSETS_2_P is shown in [Figure 8-300](#) and described in [Table 8-610](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Various Offset control values 2

Table 8-609. EDP_CORE_ENC0_RC_OFFSETS_2_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D40h |

Figure 8-300. EDP_CORE_ENC0_RC_OFFSETS_2_P Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| SLICE_BPG_OFFSET | | | | | | | | | | | | | | | | NFL_BPG_OFFSET | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-610. EDP_CORE_ENC0_RC_OFFSETS_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-16 | SLICE_BPG_OFFSET | R/W | 0h | Extra budget per group [11 fractional bits] |
| 15-0 | NFL_BPG_OFFSET | R/W | 0h | Non First Line [11 fractional bits] |

8.5.245 EDP_CORE_ENC0_RC_OFFSETS_3_P Register (Offset = 00030D44h) [reset = 0h]

EDP_CORE_ENC0_RC_OFFSETS_3_P is shown in [Figure 8-301](#) and described in [Table 8-612](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Various Offset control values 3

**Table 8-611. EDP_CORE_ENC0_RC_OFFSETS_3_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D44h |

Figure 8-301. EDP_CORE_ENC0_RC_OFFSETS_3_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FINAL_OFFSET | | | | | | | | | | | | | | | | INITIAL_OFFSET | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-612. EDP_CORE_ENC0_RC_OFFSETS_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|----------------|
| 31-16 | FINAL_OFFSET | R/W | 0h | Final Offset |
| 15-0 | INITIAL_OFFSET | R/W | 0h | Initial Offset |

8.5.246 EDP_CORE_ENC0_FLATNESS_DETECTION_P Register (Offset = 00030D48h) [reset = 0h]

EDP_CORE_ENC0_FLATNESS_DETECTION_P is shown in [Figure 8-302](#) and described in [Table 8-614](#).

Return to [Summary Table](#).

Flatness Signaling QP Override thresholds

Table 8-613.
EDP_CORE_ENC0_FLATNESS_DETECTION_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D48h |

Figure 8-302. EDP_CORE_ENC0_FLATNESS_DETECTION_P Register

| | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|-----------------|----|----|----|----|-----------------|----|-------------------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | FLATNESS_DE T_THRESH | | |
| R-0h | | | | | | | | | | | | | R/W-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FLATNESS_DET_THRESH | | | | | | FLATNESS_MAX_QP | | | | | FLATNESS_MIN_QP | | | | |
| R/W-0h | | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-614. EDP_CORE_ENC0_FLATNESS_DETECTION_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 17-10 | FLATNESS_DET_THRESH | R/W | 0h | Flatness Detection Threshold, as defined in PPS table of the DSC specification |
| 9-5 | FLATNESS_MAX_QP | R/W | 0h | Maximum threshold |
| 4-0 | FLATNESS_MIN_QP | R/W | 0h | Minimum threshold |

8.5.247 EDP_CORE_ENC0_RC_MODEL_SIZE_P Register (Offset = 00030D4Ch) [reset = 0h]

EDP_CORE_ENC0_RC_MODEL_SIZE_P is shown in [Figure 8-303](#) and described in [Table 8-616](#).

Return to [Summary Table](#).

RC Model Size

**Table 8-615. EDP_CORE_ENC0_RC_MODEL_SIZE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D4Ch |

Figure 8-303. EDP_CORE_ENC0_RC_MODEL_SIZE_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | RC_MODEL_SIZE | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-616. EDP_CORE_ENC0_RC_MODEL_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | RC_MODEL_SIZE | R/W | 0h | RC Model Size |

8.5.248 EDP_CORE_ENC0_RC_CONFIG_P Register (Offset = 00030D50h) [reset = 0h]

EDP_CORE_ENC0_RC_CONFIG_P is shown in [Figure 8-304](#) and described in [Table 8-618](#).

Return to [Summary Table](#).

RC Model Various Config

Table 8-617. EDP_CORE_ENC0_RC_CONFIG_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D50h |

Figure 8-304. EDP_CORE_ENC0_RC_CONFIG_P Register

| | | | | | | | |
|----------------------|----|----|----|----------------------|----|----------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RC_TGT_OFFSET_LO | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_TGT_OFFSET_HI | | | | RESERVED | | RC_QUANT_INCR_LIMIT1 | |
| R/W-0h | | | | R-0h | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RC_QUANT_INCR_LIMIT1 | | | | RC_QUANT_INCR_LIMIT0 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RC_EDGE_FACTOR | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-618. EDP_CORE_ENC0_RC_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 27-24 | RC_TGT_OFFSET_LO | R/W | 0h | RC Target offset low |
| 23-20 | RC_TGT_OFFSET_HI | R/W | 0h | RC Target offset high |
| 19-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 17-13 | RC_QUANT_INCR_LIMIT1 | R/W | 0h | RC quantization increment limit 1 |
| 12-8 | RC_QUANT_INCR_LIMIT0 | R/W | 0h | RC quantization increment limit 0 |
| 7-4 | RESERVED | R | 0h | RC Edge factor [1 fractional bit] |
| 3-0 | RC_EDGE_FACTOR | R/W | 0h | Reserved. Writes are ignored. 0x0 when read |

8.5.249 EDP_CORE_ENC0_RC_BUF_THRESH_0_P Register (Offset = 00030D54h) [reset = 0h]

EDP_CORE_ENC0_RC_BUF_THRESH_0_P is shown in [Figure 8-305](#) and described in [Table 8-620](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 0

Table 8-619.
EDP_CORE_ENC0_RC_BUF_THRESH_0_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D54h |

Figure 8-305. EDP_CORE_ENC0_RC_BUF_THRESH_0_P Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_BUF_THRESH_3 | | | | | | | | RC_BUF_THRESH_2 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_1 | | | | | | | | RC_BUF_THRESH_0 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-620. EDP_CORE_ENC0_RC_BUF_THRESH_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-24 | RC_BUF_THRESH_3 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 23-16 | RC_BUF_THRESH_2 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_1 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_0 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.250 EDP_CORE_ENC0_RC_BUF_THRESH_1_P Register (Offset = 00030D58h) [reset = 0h]

EDP_CORE_ENC0_RC_BUF_THRESH_1_P is shown in [Figure 8-306](#) and described in [Table 8-622](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 1

Table 8-621.
EDP_CORE_ENC0_RC_BUF_THRESH_1_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D58h |

Figure 8-306. EDP_CORE_ENC0_RC_BUF_THRESH_1_P Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_BUF_THRESH_7 | | | | | | | | RC_BUF_THRESH_6 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_5 | | | | | | | | RC_BUF_THRESH_4 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-622. EDP_CORE_ENC0_RC_BUF_THRESH_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-24 | RC_BUF_THRESH_7 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 23-16 | RC_BUF_THRESH_6 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_5 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_4 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.251 EDP_CORE_ENC0_RC_BUF_THRESH_2_P Register (Offset = 00030D5Ch) [reset = 0h]

EDP_CORE_ENC0_RC_BUF_THRESH_2_P is shown in [Figure 8-307](#) and described in [Table 8-624](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 2

Table 8-623.
EDP_CORE_ENC0_RC_BUF_THRESH_2_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D5Ch |

Figure 8-307. EDP_CORE_ENC0_RC_BUF_THRESH_2_P Register

| | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_BUF_THRESH_11 | | | | | | | | RC_BUF_THRESH_10 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_9 | | | | | | | | RC_BUF_THRESH_8 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-624. EDP_CORE_ENC0_RC_BUF_THRESH_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-24 | RC_BUF_THRESH_11 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 23-16 | RC_BUF_THRESH_10 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_9 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_8 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.252 EDP_CORE_ENC0_RC_BUF_THRESH_3_P Register (Offset = 00030D60h) [reset = 0h]

EDP_CORE_ENC0_RC_BUF_THRESH_3_P is shown in [Figure 8-308](#) and described in [Table 8-626](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 3

Table 8-625.
EDP_CORE_ENC0_RC_BUF_THRESH_3_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D60h |

Figure 8-308. EDP_CORE_ENC0_RC_BUF_THRESH_3_P Register

| | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_13 | | | | | | | | RC_BUF_THRESH_12 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-626. EDP_CORE_ENC0_RC_BUF_THRESH_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-8 | RC_BUF_THRESH_13 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_12 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.253 EDP_CORE_ENC0_RC_MIN_QP_0_P Register (Offset = 00030D64h) [reset = 0h]

EDP_CORE_ENC0_RC_MIN_QP_0_P is shown in [Figure 8-309](#) and described in [Table 8-628](#).

Return to [Summary Table](#).

RC Min QP 0

**Table 8-627. EDP_CORE_ENC0_RC_MIN_QP_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D64h |

Figure 8-309. EDP_CORE_ENC0_RC_MIN_QP_0_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|----|----|--------|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MIN_QP_4 | | | | RANGE_MIN_QP_3 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MIN_QP_3 | RANGE_MIN_QP_2 | | | | | RANGE_MIN_QP_1 | | | | | RANGE_MIN_QP_0 | | | | |
| R/W-0h | | | | R/W-0h | | | | R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-628. EDP_CORE_ENC0_RC_MIN_QP_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MIN_QP_4 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MIN_QP_3 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MIN_QP_2 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MIN_QP_1 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MIN_QP_0 | R/W | 0h | As per DSC specification |

8.5.254 EDP_CORE_ENC0_RC_MIN_QP_1_P Register (Offset = 00030D68h) [reset = 0h]

EDP_CORE_ENC0_RC_MIN_QP_1_P is shown in [Figure 8-310](#) and described in [Table 8-630](#).

Return to [Summary Table](#).

RC Min QP 1

Table 8-629. EDP_CORE_ENC0_RC_MIN_QP_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D68h |

Figure 8-310. EDP_CORE_ENC0_RC_MIN_QP_1_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|----|----|----|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MIN_QP_9 | | | | RANGE_MIN_QP_8 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MIN_QP_8 | RANGE_MIN_QP_7 | | | | | RANGE_MIN_QP_6 | | | | | RANGE_MIN_QP_5 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-630. EDP_CORE_ENC0_RC_MIN_QP_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MIN_QP_9 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MIN_QP_8 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MIN_QP_7 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MIN_QP_6 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MIN_QP_5 | R/W | 0h | As per DSC specification |

8.5.255 EDP_CORE_ENC0_RC_MIN_QP_2_P Register (Offset = 00030D6Ch) [reset = 0h]

EDP_CORE_ENC0_RC_MIN_QP_2_P is shown in [Figure 8-311](#) and described in [Table 8-632](#).

Return to [Summary Table](#).

RC Min QP 2

**Table 8-631. EDP_CORE_ENC0_RC_MIN_QP_2_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D6Ch |

Figure 8-311. EDP_CORE_ENC0_RC_MIN_QP_2_P Register

| | | | | | | | | | | | | | | | |
|------------------------------|-----------------|----|----|----|----|-----------------|-----------------|----|----|----|-----------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | RANGE_MIN_QP_14 | | | | | RANGE_MIN_QP_13 | | | |
| R-0h | | | | | | | R/W-0h | | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANG E_MIN _QP_1 _3 | RANGE_MIN_QP_12 | | | | | RANGE_MIN_QP_11 | | | | | RANGE_MIN_QP_10 | | | | |
| R/W-0h | | | | | | | R/W-0h | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-632. EDP_CORE_ENC0_RC_MIN_QP_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MIN_QP_14 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MIN_QP_13 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MIN_QP_12 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MIN_QP_11 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MIN_QP_10 | R/W | 0h | As per DSC specification |

8.5.256 EDP_CORE_ENC0_RC_MAX_QP_0_P Register (Offset = 00030D70h) [reset = 0h]

EDP_CORE_ENC0_RC_MAX_QP_0_P is shown in [Figure 8-312](#) and described in [Table 8-634](#).

Return to [Summary Table](#).

RC Max QP 0

Table 8-633. EDP_CORE_ENC0_RC_MAX_QP_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D70h |

Figure 8-312. EDP_CORE_ENC0_RC_MAX_QP_0_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|----|----|----|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MAX_QP_4 | | | | RANGE_MAX_QP_3 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MAX_QP_3 | RANGE_MAX_QP_2 | | | | | RANGE_MAX_QP_1 | | | | | RANGE_MAX_QP_0 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-634. EDP_CORE_ENC0_RC_MAX_QP_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MAX_QP_4 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MAX_QP_3 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MAX_QP_2 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MAX_QP_1 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MAX_QP_0 | R/W | 0h | As per DSC specification |

8.5.257 EDP_CORE_ENC0_RC_MAX_QP_1_P Register (Offset = 00030D74h) [reset = 0h]

EDP_CORE_ENC0_RC_MAX_QP_1_P is shown in [Figure 8-313](#) and described in [Table 8-636](#).

Return to [Summary Table](#).

RC Max QP 1

**Table 8-635. EDP_CORE_ENC0_RC_MAX_QP_1_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D74h |

Figure 8-313. EDP_CORE_ENC0_RC_MAX_QP_1_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|----|----|----|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MAX_QP_9 | | | | RANGE_MAX_QP_8 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MAX_QP_8 | RANGE_MAX_QP_7 | | | | | RANGE_MAX_QP_6 | | | | | RANGE_MAX_QP_5 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-636. EDP_CORE_ENC0_RC_MAX_QP_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MAX_QP_9 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MAX_QP_8 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MAX_QP_7 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MAX_QP_6 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MAX_QP_5 | R/W | 0h | As per DSC specification |

8.5.258 EDP_CORE_ENC0_RC_MAX_QP_2_P Register (Offset = 00030D78h) [reset = 0h]

EDP_CORE_ENC0_RC_MAX_QP_2_P is shown in [Figure 8-314](#) and described in [Table 8-638](#).

Return to [Summary Table](#).

RC Max QP 2

Table 8-637. EDP_CORE_ENC0_RC_MAX_QP_2_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D78h |

Figure 8-314. EDP_CORE_ENC0_RC_MAX_QP_2_P Register

| | | | | | | | | | | | | | | | |
|-----------------|-----------------|----|----|----|----|-----------------|----|-----------------|----|----|-----------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MAX_QP_14 | | | | RANGE_MAX_QP_13 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MAX_QP_13 | RANGE_MAX_QP_12 | | | | | RANGE_MAX_QP_11 | | | | | RANGE_MAX_QP_10 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-638. EDP_CORE_ENC0_RC_MAX_QP_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MAX_QP_14 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MAX_QP_13 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MAX_QP_12 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MAX_QP_11 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MAX_QP_10 | R/W | 0h | As per DSC specification |

8.5.259 EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_0_P Register (Offset = 00030D7Ch) [reset = 0h]

EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_0_P is shown in [Figure 8-315](#) and described in [Table 8-640](#).

Return to [Summary Table](#).

RC Range bpg Offsets 0

Table 8-639.
EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D7Ch |

Figure 8-315. EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_0_P Register

| | | | | | | | |
|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RANGE_BPG_OFFSET_4 | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RANGE_BPG_OFFSET_3 | | | | | | RANGE_BPG_OFFSET_2 | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RANGE_BPG_OFFSET_2 | | | | RANGE_BPG_OFFSET_1 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_BPG_OFFSET_1 | | RANGE_BPG_OFFSET_0 | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-640. EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 29-24 | RANGE_BPG_OFFSET_4 | R/W | 0h | As per DSC specification |
| 23-18 | RANGE_BPG_OFFSET_3 | R/W | 0h | As per DSC specification |
| 17-12 | RANGE_BPG_OFFSET_2 | R/W | 0h | As per DSC specification |
| 11-6 | RANGE_BPG_OFFSET_1 | R/W | 0h | As per DSC specification |
| 5-0 | RANGE_BPG_OFFSET_0 | R/W | 0h | As per DSC specification |

8.5.260 EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_1_P Register (Offset = 00030D80h) [reset = 0h]

EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_1_P is shown in [Figure 8-316](#) and described in [Table 8-642](#).

Return to [Summary Table](#).

RC Range bpg Offsets 1

Table 8-641.
EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D80h |

Figure 8-316. EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_1_P Register

| | | | | | | | |
|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RANGE_BPG_OFFSET_9 | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RANGE_BPG_OFFSET_8 | | | | | | RANGE_BPG_OFFSET_7 | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RANGE_BPG_OFFSET_7 | | | | RANGE_BPG_OFFSET_6 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_BPG_OFFSET_6 | | RANGE_BPG_OFFSET_5 | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-642. EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 29-24 | RANGE_BPG_OFFSET_9 | R/W | 0h | As per DSC specification |
| 23-18 | RANGE_BPG_OFFSET_8 | R/W | 0h | As per DSC specification |
| 17-12 | RANGE_BPG_OFFSET_7 | R/W | 0h | As per DSC specification |
| 11-6 | RANGE_BPG_OFFSET_6 | R/W | 0h | As per DSC specification |
| 5-0 | RANGE_BPG_OFFSET_5 | R/W | 0h | As per DSC specification |

8.5.261 EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_2_P Register (Offset = 00030D84h) [reset = 0h]

EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_2_P is shown in [Figure 8-317](#) and described in [Table 8-644](#).

Return to [Summary Table](#).

RC Range bpg Offsets 2

Table 8-643.
EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_2_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D84h |

Figure 8-317. EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_2_P Register

| | | | | | | | |
|---------------------|----|---------------------|----|---------------------|----|---------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RANGE_BPG_OFFSET_14 | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RANGE_BPG_OFFSET_13 | | | | | | RANGE_BPG_OFFSET_12 | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RANGE_BPG_OFFSET_12 | | | | RANGE_BPG_OFFSET_11 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_BPG_OFFSET_11 | | RANGE_BPG_OFFSET_10 | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-644. EDP_CORE_ENC0_RC_RANGE_BPG_OFFSETS_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 29-24 | RANGE_BPG_OFFSET_14 | R/W | 0h | As per DSC specification |
| 23-18 | RANGE_BPG_OFFSET_13 | R/W | 0h | As per DSC specification |
| 17-12 | RANGE_BPG_OFFSET_12 | R/W | 0h | As per DSC specification |
| 11-6 | RANGE_BPG_OFFSET_11 | R/W | 0h | As per DSC specification |
| 5-0 | RANGE_BPG_OFFSET_10 | R/W | 0h | As per DSC specification |

8.5.262 EDP_CORE_ENC0_DPI_CTRL_OUT_DELAY_P Register (Offset = 00030D88h) [reset = 0h]

EDP_CORE_ENC0_DPI_CTRL_OUT_DELAY_P is shown in [Figure 8-318](#) and described in [Table 8-646](#).

Return to [Summary Table](#).

Delay applied to DPI input control signals to generate DPI output control signals

Table 8-645.
EDP_CORE_ENC0_DPI_CTRL_OUT_DELAY_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0D88h |

Figure 8-318. EDP_CORE_ENC0_DPI_CTRL_OUT_DELAY_P Register

| | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPI_CTRL_OUT_DELAY | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-646. EDP_CORE_ENC0_DPI_CTRL_OUT_DELAY_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | DPI_CTRL_OUT_DELAY | R/W | 0h | Delay in number of encx clock cycles. The delay should equal to InitialLines x Htotal[clk] where Htotal is the upstream source timing controller total line time [in clock cycles, not in pixels] including the horizontal blanking [Htotal[clk] = Hactive[clk] + Hblank[clk]]When in split panel mode, the Hactive[clk] is expected to be picture_width divided by 2 |

8.5.263 EDP_CORE_ENC0_GENERAL_STATUS_P Register (Offset = 00030DC0h) [reset = 18h]

EDP_CORE_ENC0_GENERAL_STATUS_P is shown in [Figure 8-319](#) and described in [Table 8-648](#).

Return to [Summary Table](#).

General Encoder Status

Table 8-647.
EDP_CORE_ENC0_GENERAL_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DC0h |

Figure 8-319. EDP_CORE_ENC0_GENERAL_STATUS_P Register

| | | | | | | | |
|----------|-------------------------|-------------------------|--------------------------|--------------------------|------------|---------------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 | OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE |
| R-0h | R-0h | R-0h | R-1h | R-1h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-648. EDP_CORE_ENC0_GENERAL_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 6 | OUT_BUFF_FULL_CONTEXT_1 | R | 0h | Output buffer 1 [soft slice 1] is full.For Debug purposes only. |
| 5 | OUT_BUFF_FULL_CONTEXT_0 | R | 0h | Output buffer 0 [soft slice 0] is full.For Debug purposes only. |
| 4 | OUT_BUFF_EMPTY_CONTEXT_1 | R | 1h | Output buffer 1 [soft slice 1] is empty.For Debug purposes only. |
| 3 | OUT_BUFF_EMPTY_CONTEXT_0 | R | 1h | Output buffer 0 [soft slice 0] is empty.For Debug purposes only. |
| 2 | FRAME_DONE | R | 0h | Encoder finished a frame |
| 1 | FRAME_STARTED | R | 0h | Encoder is currently processing a frame |
| 0 | CE | R | 0h | Flow control internal clock enable status.For Debug purposes only. |

8.5.264 EDP_CORE_ENC0_HSLICE_STATUS_P Register (Offset = 00030DC4h) [reset = 0h]

EDP_CORE_ENC0_HSLICE_STATUS_P is shown in [Figure 8-320](#) and described in [Table 8-650](#).

[Return to Summary Table.](#)

Hard Slice Encoded Status

Table 8-649. EDP_CORE_ENC0_HSLICE_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DC4h |

Figure 8-320. EDP_CORE_ENC0_HSLICE_STATUS_P Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SLICE_COUNT_ENCODED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLICE_LINE_COUNT_ENCODED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-650. EDP_CORE_ENC0_HSLICE_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-16 | SLICE_COUNT_ENCODED | R | 0h | Actual slice number of current frame being processed at VLC encoder. Not re-synchronized in register clock domain. For Debug purposes only. |
| 15-0 | SLICE_LINE_COUNT_ENCODED | R | 0h | Actual line number of current slice being processed at VLC encoder. Not re-synchronized in register clock domain. For Debug purposes only. |

8.5.265 EDP_CORE_ENC0_OUT_STATUS_P Register (Offset = 00030DC8h) [reset = 0h]

EDP_CORE_ENC0_OUT_STATUS_P is shown in [Figure 8-321](#) and described in [Table 8-652](#).

Return to [Summary Table](#).

Outputted Slice Status

**Table 8-651. EDP_CORE_ENC0_OUT_STATUS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DC8h |

Figure 8-321. EDP_CORE_ENC0_OUT_STATUS_P Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SLICE_COUNT_OUT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLICE_LINE_COUNT_OUT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-652. EDP_CORE_ENC0_OUT_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-16 | SLICE_COUNT_OUT | R | 0h | Actual slice number of current frame being read at output interface. Not re-synchronized in register clock domain. For Debug purposes only. |
| 15-0 | SLICE_LINE_COUNT_OUT | R | 0h | Actual line number of current slice being read at output interface. Not re-synchronized in register clock domain. For Debug purposes only. |

8.5.266 EDP_CORE_ENC0_INT_STAT_P Register (Offset = 00030DCCh) [reset = 0h]

EDP_CORE_ENC0_INT_STAT_P is shown in [Figure 8-322](#) and described in [Table 8-654](#).

[Return to Summary Table.](#)

Encoder Interrupt Status

Table 8-653. EDP_CORE_ENC0_INT_STAT_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DCCh |

Figure 8-322. EDP_CORE_ENC0_INT_STAT_P Register

| | | | | | | | |
|--------------------------|------------|---------------|------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-654. EDP_CORE_ENC0_INT_STAT_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R | 0h | Output buffer 1 [soft slice 1] became full |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R | 0h | Output buffer 0 [soft slice 0] became full |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R | 0h | Output buffer 1 [soft slice 1] became empty |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R | 0h | Output buffer 0 [soft slice 0] became empty |
| 6 | FRAME_DONE | R | 0h | Encoder finished a frame |
| 5 | FRAME_STARTED | R | 0h | Encoder is started to process a frame |
| 4 | CE | R | 0h | Flow control internal clock enable becomes high |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R | 0h | rc_model_buffer 1 [soft slice 1] overflow |

Table 8-654. EDP_CORE_ENC0_INT_STAT_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|---|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R | 0h | rc_model_buffer 0 [soft slice 0] overflow |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R | 0h | output buffer 1 [soft slice 1] underflow |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R | 0h | output buffer 0 [soft slice 0] underflow |

8.5.267 EDP_CORE_ENC0_INT_CLR_P Register (Offset = 00030DD0h) [reset = 0h]

EDP_CORE_ENC0_INT_CLR_P is shown in [Figure 8-323](#) and described in [Table 8-656](#).

Return to [Summary Table](#).

Encoder Interrupt Clear. Setting any one of these bits, clears the corresponding ENC_INT_STAT bits. This register is self-clearing after 8 regs_pclk cycles.

Table 8-655. EDP_CORE_ENC0_INT_CLR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DD0h |

Figure 8-323. EDP_CORE_ENC0_INT_CLR_P Register

| | | | | | | | |
|--------------------------|------------|---------------|--------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-656. EDP_CORE_ENC0_INT_CLR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became full |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became full |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became empty |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became empty |
| 6 | FRAME_DONE | R/W | 0h | Encoder finished a frame |
| 5 | FRAME_STARTED | R/W | 0h | Encoder is started to process a frame |
| 4 | CE | R/W | 0h | Flow control internal clock enable |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R/W | 0h | rc model buffer 1 overflow |

Table 8-656. EDP_CORE_ENC0_INT_CLR_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|----------------------------|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R/W | 0h | rc model buffer 0 overflow |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R/W | 0h | output buffer 1 underflow |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R/W | 0h | output buffer 0 underflow |

8.5.268 EDP_CORE_ENC0_INT_MASK_P Register (Offset = 00030DD4h) [reset = 0h]

EDP_CORE_ENC0_INT_MASK_P is shown in [Figure 8-324](#) and described in [Table 8-658](#).

Return to [Summary Table](#).

Encoder Interrupt Mask. Any bit set to 1'b1 is enabled to report an interrupt on the corresponding bit position

Table 8-657. EDP_CORE_ENC0_INT_MASK_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DD4h |

Figure 8-324. EDP_CORE_ENC0_INT_MASK_P Register

| | | | | | | | |
|--------------------------|------------|---------------|--------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-658. EDP_CORE_ENC0_INT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became full |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became full |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became empty |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became empty |
| 6 | FRAME_DONE | R/W | 0h | Encoder finished a frame |
| 5 | FRAME_STARTED | R/W | 0h | Encoder is started to process a frame |
| 4 | CE | R/W | 0h | Flow control internal clock enable |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R/W | 0h | rc model buffer 1 overflow |

Table 8-658. EDP_CORE_ENC0_INT_MASK_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|----------------------------|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R/W | 0h | rc model buffer 0 overflow |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R/W | 0h | enc underflow 1 underflow |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R/W | 0h | enc underflow 0 underflow |

8.5.269 EDP_CORE_ENC0_INT_TEST_P Register (Offset = 00030DD8h) [reset = 0h]

EDP_CORE_ENC0_INT_TEST_P is shown in [Figure 8-325](#) and described in [Table 8-660](#).

Return to [Summary Table](#).

Encoder Interrupt Test. Setting any one of these bits to 0x0 and then to 0x1 simulate a hardware event and generate an interrupt if the corresponding ENCx_INT_MASK bit is set.

Table 8-659. EDP_CORE_ENC0_INT_TEST_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0DD8h |

Figure 8-325. EDP_CORE_ENC0_INT_TEST_P Register

| | | | | | | | |
|--------------------------|------------|---------------|--------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-660. EDP_CORE_ENC0_INT_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became full test |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became full test |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became empty test |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became empty test |
| 6 | FRAME_DONE | R/W | 0h | Encoder finished a frame test |
| 5 | FRAME_STARTED | R/W | 0h | Encoder is started to process a frame test |
| 4 | CE | R/W | 0h | Flow control internal clock enable test |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R/W | 0h | rc model buffer 1 overflow test |

Table 8-660. EDP_CORE_ENC0_INT_TEST_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|---------------------------------|
| 2 | RC_MODEL_BUFFER_F ULLNESS_OVERFLOW_ CONTEXT_0 | R/W | 0h | rc model buffer 0 overflow test |
| 1 | ENC_UNDERFLOW_CON TEXT_1 | R/W | 0h | enc underflow 1 underflow test |
| 0 | ENC_UNDERFLOW_CON TEXT_0 | R/W | 0h | enc underflow 0 underflow test |

8.5.270 EDP_CORE_ENC1_MAIN_CONF_P Register (Offset = 00030E20h) [reset = 0F000004h]

EDP_CORE_ENC1_MAIN_CONF_P is shown in [Figure 8-326](#) and described in [Table 8-662](#).

Return to [Summary Table](#).

Encoder Main Configuration values test

Table 8-661. EDP_CORE_ENC1_MAIN_CONF_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E20h |

Figure 8-326. EDP_CORE_ENC1_MAIN_CONF_P Register

| | | | | | | | |
|----------------|----|----|-------------|------------|-------------------|----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INITIAL_LINES | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | ICH_RST_EOL | VIDEO_MODE | BLOCK_PRED_ENABLE | BITS_PER_PIXEL | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BITS_PER_PIXEL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINEBUF_DEPTH | | | | ENABLE_422 | CONVERT_RGB | INPUT_BPC | |
| R/W-0h | | | | R/W-0h | R/W-1h | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-662. EDP_CORE_ENC1_MAIN_CONF_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31-24 | INITIAL_LINES | R/W | Fh | Number of lines to wait before initiating transport in Command Mode. |
| 23-21 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 20 | ICH_RST_EOL | R/W | 0h | Forces the ICH to reset at EOL [when not in split mode]. |
| 19 | VIDEO_MODE | R/W | 0h | MIPI Video/Command mode: '0' Command mode '1' Video mode |
| 18 | BLOCK_PRED_ENABLE | R/W | 0h | Active-High input Block Prediction Enable |
| 17-8 | BITS_PER_PIXEL | R/W | 0h | Target bits per pixel. The value is in 6.4 format [4 LSBs for fractional part, they should be 0000] |
| 7-4 | LINEBUF_DEPTH | R/W | 0h | Depth of the line buffer used by the decoder [i.e., the number of bits stored for each component of the pixels on the previous line] |
| 3 | ENABLE_422 | R/W | 0h | Active-High input to indicate the data_in pixels are 4:2:2 sub-sampled. This input is valid only when convert_rgb is low. NOT SUPPORTED, MUST BE SET TO '0' |
| 2 | CONVERT_RGB | R/W | 1h | Active-High input to indicate the data_in pixels are RGB. When set to low input, it is YUV and does not require conversion. |

Table 8-662. EDP_CORE_ENC1_MAIN_CONF_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 1-0 | INPUT_BPC | R/W | 0h | Indicates the current input pixel stream bits per component: 00: input is 8 bits/component 01: input is 10 bits/component |

8.5.271 EDP_CORE_ENC1_PICTURE_SIZE_P Register (Offset = 00030E24h) [reset = 0h]

EDP_CORE_ENC1_PICTURE_SIZE_P is shown in [Figure 8-327](#) and described in [Table 8-664](#).

Return to [Summary Table](#).

Encoder Picture configuration

Table 8-663. EDP_CORE_ENC1_PICTURE_SIZE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E24h |

Figure 8-327. EDP_CORE_ENC1_PICTURE_SIZE_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PICTURE_HEIGHT | | | | | | | | | | | | | | | | PICTURE_WIDTH | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-664. EDP_CORE_ENC1_PICTURE_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|----------------|
| 31-16 | PICTURE_HEIGHT | R/W | 0h | Picture height |
| 15-0 | PICTURE_WIDTH | R/W | 0h | Picture width |

8.5.272 EDP_CORE_ENC1_SLICE_SIZE_P Register (Offset = 00030E28h) [reset = 0h]

EDP_CORE_ENC1_SLICE_SIZE_P is shown in [Figure 8-328](#) and described in [Table 8-666](#).

Return to [Summary Table](#).

Encoder Slice(s) configuration

**Table 8-665. EDP_CORE_ENC1_SLICE_SIZE_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E28h |

Figure 8-328. EDP_CORE_ENC1_SLICE_SIZE_P Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| SLICE_HEIGHT | | | | | | | | | | | | | | | | SLICE_WIDTH | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-666. EDP_CORE_ENC1_SLICE_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--------------|
| 31-16 | SLICE_HEIGHT | R/W | 0h | Slice height |
| 15-0 | SLICE_WIDTH | R/W | 0h | Slice width |

8.5.273 EDP_CORE_ENC1_MISC_SIZE_P Register (Offset = 00030E2Ch) [reset = FFFCh]

EDP_CORE_ENC1_MISC_SIZE_P is shown in [Figure 8-329](#) and described in [Table 8-668](#).

Return to [Summary Table](#).

Encoder Group, Output Buffer(s), and Transport Chunk Size

Table 8-667. EDP_CORE_ENC1_MISC_SIZE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E2Ch |

Figure 8-329. EDP_CORE_ENC1_MISC_SIZE_P Register

| | | | | | | | |
|-------------|----|----|----|----|----|-----------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CHUNK_SIZE | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CHUNK_SIZE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OB_MAX_ADDR | | | | | | | |
| R/W-3FFFh | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OB_MAX_ADDR | | | | | | SLICE_LAST_GROUP_SIZE | |
| R/W-3FFFh | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-668. EDP_CORE_ENC1_MISC_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-16 | CHUNK_SIZE | R/W | 0h | Chunk size in bytes |
| 15-2 | OB_MAX_ADDR | R/W | 3FFFh | Output Buffer[s] max pointer address[es] |
| 1-0 | SLICE_LAST_GROUP_SIZE | R/W | 0h | Size of last group of the slice line [0-based]: 0 = 1 pixel, 1 = 2 pixels, 2 = 3 pixels [slice_width + 2] % 3 |

8.5.274 EDP_CORE_ENC1_HRD_DELAYS_P Register (Offset = 00030E30h) [reset = 0h]

EDP_CORE_ENC1_HRD_DELAYS_P is shown in [Figure 8-330](#) and described in [Table 8-670](#).

Return to [Summary Table](#).

Hypothetical Reference Decoder delays

**Table 8-669. EDP_CORE_ENC1_HRD_DELAYS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E30h |

Figure 8-330. EDP_CORE_ENC1_HRD_DELAYS_P Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INITIAL_DEC_DELAY | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | INITIAL_XMIT_DELAY | | | | | | | | | |
| R-0h | | | | | | R/W-0h | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-670. EDP_CORE_ENC1_HRD_DELAYS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-16 | INITIAL_DEC_DELAY | R/W | 0h | Initial Decoder delay |
| 15-10 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 9-0 | INITIAL_XMIT_DELAY | R/W | 0h | Initial Decoder Transmit delay |

8.5.275 EDP_CORE_ENC1_RC_SCALE_P Register (Offset = 00030E34h) [reset = 0h]

EDP_CORE_ENC1_RC_SCALE_P is shown in [Figure 8-331](#) and described in [Table 8-672](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Scale value

Table 8-671. EDP_CORE_ENC1_RC_SCALE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E34h |

Figure 8-331. EDP_CORE_ENC1_RC_SCALE_P Register

| | | | | | | | |
|----------|----|----|----|---------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | INITIAL_SCALE_VALUE | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-672. EDP_CORE_ENC1_RC_SCALE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-6 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 5-0 | INITIAL_SCALE_VALUE | R/W | 0h | Three fractional bits |

8.5.276 EDP_CORE_ENC1_RC_SCALE_INC_DEC_P Register (Offset = 00030E38h) [reset = 0h]

EDP_CORE_ENC1_RC_SCALE_INC_DEC_P is shown in [Figure 8-332](#) and described in [Table 8-674](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Increment and Decrement Scale values

Table 8-673.
EDP_CORE_ENC1_RC_SCALE_INC_DEC_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E38h |

Figure 8-332. EDP_CORE_ENC1_RC_SCALE_INC_DEC_P Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|--------------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | SCALE_DECREMENT_INTERVAL | | | | | | | | | | | |
| R-0h | | | | R/W-0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCALE_INCREMENT_INTERVAL | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-674. EDP_CORE_ENC1_RC_SCALE_INC_DEC_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 27-16 | SCALE_DECREMENT_INTERVAL | R/W | 0h | RC scale decrement value |
| 15-0 | SCALE_INCREMENT_INTERVAL | R/W | 0h | RC scale increment value |

8.5.277 EDP_CORE_ENC1_RC_OFFSETS_1_P Register (Offset = 00030E3Ch) [reset = 0h]

EDP_CORE_ENC1_RC_OFFSETS_1_P is shown in [Figure 8-333](#) and described in [Table 8-676](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Various Offset control values 1

Table 8-675. EDP_CORE_ENC1_RC_OFFSETS_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E3Ch |

Figure 8-333. EDP_CORE_ENC1_RC_OFFSETS_1_P Register

| | | | | | | | |
|----------|----|----|----|-----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | FIRST_LINE_BPG_OFFSET | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-676. EDP_CORE_ENC1_RC_OFFSETS_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|---|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 4-0 | FIRST_LINE_BPG_OFFSET | R/W | 0h | First Line |

8.5.278 EDP_CORE_ENC1_RC_OFFSETS_2_P Register (Offset = 00030E40h) [reset = 0h]

EDP_CORE_ENC1_RC_OFFSETS_2_P is shown in [Figure 8-334](#) and described in [Table 8-678](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Various Offset control values 2

**Table 8-677. EDP_CORE_ENC1_RC_OFFSETS_2_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E40h |

Figure 8-334. EDP_CORE_ENC1_RC_OFFSETS_2_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLICE_BPG_OFFSET | | | | | | | | | | | | | | | | NFL_BPG_OFFSET | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-678. EDP_CORE_ENC1_RC_OFFSETS_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-16 | SLICE_BPG_OFFSET | R/W | 0h | Extra budget per group [11 fractional bits] |
| 15-0 | NFL_BPG_OFFSET | R/W | 0h | Non First Line [11 fractional bits] |

8.5.279 EDP_CORE_ENC1_RC_OFFSETS_3_P Register (Offset = 00030E44h) [reset = 0h]

EDP_CORE_ENC1_RC_OFFSETS_3_P is shown in [Figure 8-335](#) and described in [Table 8-680](#).

Return to [Summary Table](#).

RC Calculate Buffer Fullness and Offset, Various Offset control values 3

Table 8-679. EDP_CORE_ENC1_RC_OFFSETS_3_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E44h |

Figure 8-335. EDP_CORE_ENC1_RC_OFFSETS_3_P Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| FINAL_OFFSET | | | | | | | | | | | | | | | | INITIAL_OFFSET | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-680. EDP_CORE_ENC1_RC_OFFSETS_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|----------------|
| 31-16 | FINAL_OFFSET | R/W | 0h | Final Offset |
| 15-0 | INITIAL_OFFSET | R/W | 0h | Initial Offset |

8.5.280 EDP_CORE_ENC1_FLATNESS_DETECTION_P Register (Offset = 00030E48h) [reset = 0h]

EDP_CORE_ENC1_FLATNESS_DETECTION_P is shown in [Figure 8-336](#) and described in [Table 8-682](#).

Return to [Summary Table](#).

Flatness Signaling QP Override thresholds

Table 8-681.
EDP_CORE_ENC1_FLATNESS_DETECTION_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E48h |

Figure 8-336. EDP_CORE_ENC1_FLATNESS_DETECTION_P Register

| | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|-----------------|----|----|----|----|----|-----------------|----|-------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | FLATNESS_DE T_THRESH | |
| R-0h | | | | | | | | | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FLATNESS_DET_THRESH | | | | | | FLATNESS_MAX_QP | | | | | | FLATNESS_MIN_QP | | | |
| R/W-0h | | | | | | R/W-0h | | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-682. EDP_CORE_ENC1_FLATNESS_DETECTION_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 17-10 | FLATNESS_DET_THRES H | R/W | 0h | Flatness Detection Threshold, as defined in PPS table of the DSC specification |
| 9-5 | FLATNESS_MAX_QP | R/W | 0h | Maximum threshold |
| 4-0 | FLATNESS_MIN_QP | R/W | 0h | Minimum threshold |

8.5.281 EDP_CORE_ENC1_RC_MODEL_SIZE_P Register (Offset = 00030E4Ch) [reset = 0h]

EDP_CORE_ENC1_RC_MODEL_SIZE_P is shown in [Figure 8-337](#) and described in [Table 8-684](#).

Return to [Summary Table](#).

RC Model Size

Table 8-683. EDP_CORE_ENC1_RC_MODEL_SIZE_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E4Ch |

Figure 8-337. EDP_CORE_ENC1_RC_MODEL_SIZE_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | RC_MODEL_SIZE | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-684. EDP_CORE_ENC1_RC_MODEL_SIZE_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | RC_MODEL_SIZE | R/W | 0h | RC Model Size |

8.5.282 EDP_CORE_ENC1_RC_CONFIG_P Register (Offset = 00030E50h) [reset = 0h]

EDP_CORE_ENC1_RC_CONFIG_P is shown in [Figure 8-338](#) and described in [Table 8-686](#).

Return to [Summary Table](#).

RC Model Various Config

**Table 8-685. EDP_CORE_ENC1_RC_CONFIG_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E50h |

Figure 8-338. EDP_CORE_ENC1_RC_CONFIG_P Register

| | | | | | | | |
|----------------------|----|----|----|----------------------|----|----------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RC_TGT_OFFSET_LO | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_TGT_OFFSET_HI | | | | RESERVED | | RC_QUANT_INCR_LIMIT1 | |
| R/W-0h | | | | R-0h | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RC_QUANT_INCR_LIMIT1 | | | | RC_QUANT_INCR_LIMIT0 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RC_EDGE_FACTOR | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-686. EDP_CORE_ENC1_RC_CONFIG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 27-24 | RC_TGT_OFFSET_LO | R/W | 0h | RC Target offset low |
| 23-20 | RC_TGT_OFFSET_HI | R/W | 0h | RC Target offset high |
| 19-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 17-13 | RC_QUANT_INCR_LIMIT1 | R/W | 0h | RC quantization increment limit 1 |
| 12-8 | RC_QUANT_INCR_LIMIT0 | R/W | 0h | RC quantization increment limit 0 |
| 7-4 | RESERVED | R | 0h | RC Edge factor [1 fractional bit] |
| 3-0 | RC_EDGE_FACTOR | R/W | 0h | Reserved. Writes are ignored. 0x0 when read |

8.5.283 EDP_CORE_ENC1_RC_BUF_THRESH_0_P Register (Offset = 00030E54h) [reset = 0h]

EDP_CORE_ENC1_RC_BUF_THRESH_0_P is shown in [Figure 8-339](#) and described in [Table 8-688](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 0

Table 8-687.
EDP_CORE_ENC1_RC_BUF_THRESH_0_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E54h |

Figure 8-339. EDP_CORE_ENC1_RC_BUF_THRESH_0_P Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_BUF_THRESH_3 | | | | | | | | RC_BUF_THRESH_2 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_1 | | | | | | | | RC_BUF_THRESH_0 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-688. EDP_CORE_ENC1_RC_BUF_THRESH_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-24 | RC_BUF_THRESH_3 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 23-16 | RC_BUF_THRESH_2 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_1 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_0 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.284 EDP_CORE_ENC1_RC_BUF_THRESH_1_P Register (Offset = 00030E58h) [reset = 0h]

EDP_CORE_ENC1_RC_BUF_THRESH_1_P is shown in [Figure 8-340](#) and described in [Table 8-690](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 1

Table 8-689.
EDP_CORE_ENC1_RC_BUF_THRESH_1_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E58h |

Figure 8-340. EDP_CORE_ENC1_RC_BUF_THRESH_1_P Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|-----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_BUF_THRESH_7 | | | | | | | | RC_BUF_THRESH_6 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_5 | | | | | | | | RC_BUF_THRESH_4 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-690. EDP_CORE_ENC1_RC_BUF_THRESH_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-24 | RC_BUF_THRESH_7 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 23-16 | RC_BUF_THRESH_6 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_5 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_4 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.285 EDP_CORE_ENC1_RC_BUF_THRESH_2_P Register (Offset = 00030E5Ch) [reset = 0h]

EDP_CORE_ENC1_RC_BUF_THRESH_2_P is shown in [Figure 8-341](#) and described in [Table 8-692](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 2

Table 8-691.
EDP_CORE_ENC1_RC_BUF_THRESH_2_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E5Ch |

Figure 8-341. EDP_CORE_ENC1_RC_BUF_THRESH_2_P Register

| | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RC_BUF_THRESH_11 | | | | | | | | RC_BUF_THRESH_10 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_9 | | | | | | | | RC_BUF_THRESH_8 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-692. EDP_CORE_ENC1_RC_BUF_THRESH_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-24 | RC_BUF_THRESH_11 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 23-16 | RC_BUF_THRESH_10 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_9 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_8 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.286 EDP_CORE_ENC1_RC_BUF_THRESH_3_P Register (Offset = 00030E60h) [reset = 0h]

EDP_CORE_ENC1_RC_BUF_THRESH_3_P is shown in [Figure 8-342](#) and described in [Table 8-694](#).

Return to [Summary Table](#).

RC Model Buffer Thresholds 3

Table 8-693.
EDP_CORE_ENC1_RC_BUF_THRESH_3_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E60h |

Figure 8-342. EDP_CORE_ENC1_RC_BUF_THRESH_3_P Register

| | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RC_BUF_THRESH_13 | | | | | | | | RC_BUF_THRESH_12 | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-694. EDP_CORE_ENC1_RC_BUF_THRESH_3_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 15-8 | RC_BUF_THRESH_13 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |
| 7-0 | RC_BUF_THRESH_12 | R/W | 0h | 8 MSBs of the value. Values in configuration files are 14 bits but 6 LSBs are always 0 |

8.5.287 EDP_CORE_ENC1_RC_MIN_QP_0_P Register (Offset = 00030E64h) [reset = 0h]

EDP_CORE_ENC1_RC_MIN_QP_0_P is shown in [Figure 8-343](#) and described in [Table 8-696](#).

Return to [Summary Table](#).

RC Min QP 0

Table 8-695. EDP_CORE_ENC1_RC_MIN_QP_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E64h |

Figure 8-343. EDP_CORE_ENC1_RC_MIN_QP_0_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|--------|----|----|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MIN_QP_4 | | | | RANGE_MIN_QP_3 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MIN_QP_3 | RANGE_MIN_QP_2 | | | | | RANGE_MIN_QP_1 | | | | | RANGE_MIN_QP_0 | | | | |
| R/W-0h | | R/W-0h | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-696. EDP_CORE_ENC1_RC_MIN_QP_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MIN_QP_4 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MIN_QP_3 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MIN_QP_2 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MIN_QP_1 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MIN_QP_0 | R/W | 0h | As per DSC specification |

8.5.288 EDP_CORE_ENC1_RC_MIN_QP_1_P Register (Offset = 00030E68h) [reset = 0h]

EDP_CORE_ENC1_RC_MIN_QP_1_P is shown in [Figure 8-344](#) and described in [Table 8-698](#).

Return to [Summary Table](#).

RC Min QP 1

**Table 8-697. EDP_CORE_ENC1_RC_MIN_QP_1_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E68h |

Figure 8-344. EDP_CORE_ENC1_RC_MIN_QP_1_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|----|----|--------|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MIN_QP_9 | | | | RANGE_MIN_QP_8 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MIN_QP_8 | RANGE_MIN_QP_7 | | | | | RANGE_MIN_QP_6 | | | | | RANGE_MIN_QP_5 | | | | |
| R/W-0h | | | | R/W-0h | | | | R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-698. EDP_CORE_ENC1_RC_MIN_QP_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MIN_QP_9 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MIN_QP_8 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MIN_QP_7 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MIN_QP_6 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MIN_QP_5 | R/W | 0h | As per DSC specification |

8.5.289 EDP_CORE_ENC1_RC_MIN_QP_2_P Register (Offset = 00030E6Ch) [reset = 0h]

EDP_CORE_ENC1_RC_MIN_QP_2_P is shown in [Figure 8-345](#) and described in [Table 8-700](#).

Return to [Summary Table](#).

RC Min QP 2

Table 8-699. EDP_CORE_ENC1_RC_MIN_QP_2_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E6Ch |

Figure 8-345. EDP_CORE_ENC1_RC_MIN_QP_2_P Register

| | | | | | | | | | | | | | | | |
|-----------------|-----------------|----|----|----|----|-----------------|-----------------|----|----|----|-----------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | RANGE_MIN_QP_14 | | | | | RANGE_MIN_QP_13 | | | |
| R-0h | | | | | | | R/W-0h | | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MIN_QP_13 | RANGE_MIN_QP_12 | | | | | RANGE_MIN_QP_11 | | | | | RANGE_MIN_QP_10 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-700. EDP_CORE_ENC1_RC_MIN_QP_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MIN_QP_14 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MIN_QP_13 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MIN_QP_12 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MIN_QP_11 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MIN_QP_10 | R/W | 0h | As per DSC specification |

8.5.290 EDP_CORE_ENC1_RC_MAX_QP_0_P Register (Offset = 00030E70h) [reset = 0h]

EDP_CORE_ENC1_RC_MAX_QP_0_P is shown in [Figure 8-346](#) and described in [Table 8-702](#).

Return to [Summary Table](#).

RC Max QP 0

**Table 8-701. EDP_CORE_ENC1_RC_MAX_QP_0_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E70h |

Figure 8-346. EDP_CORE_ENC1_RC_MAX_QP_0_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|--------|----|----|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MAX_QP_4 | | | | RANGE_MAX_QP_3 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MAX_QP_3 | RANGE_MAX_QP_2 | | | | | RANGE_MAX_QP_1 | | | | | RANGE_MAX_QP_0 | | | | |
| R/W-0h | | R/W-0h | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-702. EDP_CORE_ENC1_RC_MAX_QP_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MAX_QP_4 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MAX_QP_3 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MAX_QP_2 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MAX_QP_1 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MAX_QP_0 | R/W | 0h | As per DSC specification |

8.5.291 EDP_CORE_ENC1_RC_MAX_QP_1_P Register (Offset = 00030E74h) [reset = 0h]

EDP_CORE_ENC1_RC_MAX_QP_1_P is shown in [Figure 8-347](#) and described in [Table 8-704](#).

Return to [Summary Table](#).

RC Max QP 1

Table 8-703. EDP_CORE_ENC1_RC_MAX_QP_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E74h |

Figure 8-347. EDP_CORE_ENC1_RC_MAX_QP_1_P Register

| | | | | | | | | | | | | | | | |
|----------------|----------------|----|----|----|----|----------------|----|----------------|----|----|----------------|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | RANGE_MAX_QP_9 | | | | RANGE_MAX_QP_8 | | | |
| R-0h | | | | | | | | R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MAX_QP_8 | RANGE_MAX_QP_7 | | | | | RANGE_MAX_QP_6 | | | | | RANGE_MAX_QP_5 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-704. EDP_CORE_ENC1_RC_MAX_QP_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MAX_QP_9 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MAX_QP_8 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MAX_QP_7 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MAX_QP_6 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MAX_QP_5 | R/W | 0h | As per DSC specification |

8.5.292 EDP_CORE_ENC1_RC_MAX_QP_2_P Register (Offset = 00030E78h) [reset = 0h]

EDP_CORE_ENC1_RC_MAX_QP_2_P is shown in [Figure 8-348](#) and described in [Table 8-706](#).

Return to [Summary Table](#).

RC Max QP 2

**Table 8-705. EDP_CORE_ENC1_RC_MAX_QP_2_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E78h |

Figure 8-348. EDP_CORE_ENC1_RC_MAX_QP_2_P Register

| | | | | | | | | | | | | | | | |
|-----------------|-----------------|----|----|----|----|-----------------|-----------------|----|----|----|-----------------|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | RANGE_MAX_QP_14 | | | | RANGE_MAX_QP_13 | | | | |
| R-0h | | | | | | | R/W-0h | | | | R/W-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_MAX_QP_13 | RANGE_MAX_QP_12 | | | | | RANGE_MAX_QP_11 | | | | | RANGE_MAX_QP_10 | | | | |
| R/W-0h | R/W-0h | | | | | R/W-0h | | | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-706. EDP_CORE_ENC1_RC_MAX_QP_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-25 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 24-20 | RANGE_MAX_QP_14 | R/W | 0h | As per DSC specification |
| 19-15 | RANGE_MAX_QP_13 | R/W | 0h | As per DSC specification |
| 14-10 | RANGE_MAX_QP_12 | R/W | 0h | As per DSC specification |
| 9-5 | RANGE_MAX_QP_11 | R/W | 0h | As per DSC specification |
| 4-0 | RANGE_MAX_QP_10 | R/W | 0h | As per DSC specification |

8.5.293 EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_0_P Register (Offset = 00030E7Ch) [reset = 0h]

EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_0_P is shown in [Figure 8-349](#) and described in [Table 8-708](#).

Return to [Summary Table](#).

RC Range bpg Offsets 0

Table 8-707.
EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_0_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E7Ch |

Figure 8-349. EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_0_P Register

| | | | | | | | |
|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RANGE_BPG_OFFSET_4 | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RANGE_BPG_OFFSET_3 | | | | | | RANGE_BPG_OFFSET_2 | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RANGE_BPG_OFFSET_2 | | | | RANGE_BPG_OFFSET_1 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_BPG_OFFSET_1 | | RANGE_BPG_OFFSET_0 | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-708. EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_0_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 29-24 | RANGE_BPG_OFFSET_4 | R/W | 0h | As per DSC specification |
| 23-18 | RANGE_BPG_OFFSET_3 | R/W | 0h | As per DSC specification |
| 17-12 | RANGE_BPG_OFFSET_2 | R/W | 0h | As per DSC specification |
| 11-6 | RANGE_BPG_OFFSET_1 | R/W | 0h | As per DSC specification |
| 5-0 | RANGE_BPG_OFFSET_0 | R/W | 0h | As per DSC specification |

8.5.294 EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_1_P Register (Offset = 00030E80h) [reset = 0h]

EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_1_P is shown in [Figure 8-350](#) and described in [Table 8-710](#).

Return to [Summary Table](#).

RC Range bpg Offsets 1

Table 8-709.
EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_1_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E80h |

Figure 8-350. EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_1_P Register

| | | | | | | | |
|--------------------|----|--------------------|----|--------------------|----|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RANGE_BPG_OFFSET_9 | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RANGE_BPG_OFFSET_8 | | | | | | RANGE_BPG_OFFSET_7 | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RANGE_BPG_OFFSET_7 | | | | RANGE_BPG_OFFSET_6 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_BPG_OFFSET_6 | | RANGE_BPG_OFFSET_5 | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-710. EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_1_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 29-24 | RANGE_BPG_OFFSET_9 | R/W | 0h | As per DSC specification |
| 23-18 | RANGE_BPG_OFFSET_8 | R/W | 0h | As per DSC specification |
| 17-12 | RANGE_BPG_OFFSET_7 | R/W | 0h | As per DSC specification |
| 11-6 | RANGE_BPG_OFFSET_6 | R/W | 0h | As per DSC specification |
| 5-0 | RANGE_BPG_OFFSET_5 | R/W | 0h | As per DSC specification |

8.5.295 EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_2_P Register (Offset = 00030E84h) [reset = 0h]

EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_2_P is shown in [Figure 8-351](#) and described in [Table 8-712](#).

Return to [Summary Table](#).

RC Range bpg Offsets 2

Table 8-711.
EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_2_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E84h |

Figure 8-351. EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_2_P Register

| | | | | | | | |
|---------------------|----|---------------------|----|---------------------|----|---------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | RANGE_BPG_OFFSET_14 | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RANGE_BPG_OFFSET_13 | | | | | | RANGE_BPG_OFFSET_12 | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RANGE_BPG_OFFSET_12 | | | | RANGE_BPG_OFFSET_11 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RANGE_BPG_OFFSET_11 | | RANGE_BPG_OFFSET_10 | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-712. EDP_CORE_ENC1_RC_RANGE_BPG_OFFSETS_2_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-30 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 29-24 | RANGE_BPG_OFFSET_14 | R/W | 0h | As per DSC specification |
| 23-18 | RANGE_BPG_OFFSET_13 | R/W | 0h | As per DSC specification |
| 17-12 | RANGE_BPG_OFFSET_12 | R/W | 0h | As per DSC specification |
| 11-6 | RANGE_BPG_OFFSET_11 | R/W | 0h | As per DSC specification |
| 5-0 | RANGE_BPG_OFFSET_10 | R/W | 0h | As per DSC specification |

8.5.296 EDP_CORE_ENC1_DPI_CTRL_OUT_DELAY_P Register (Offset = 00030E88h) [reset = 0h]

EDP_CORE_ENC1_DPI_CTRL_OUT_DELAY_P is shown in [Figure 8-352](#) and described in [Table 8-714](#).

Return to [Summary Table](#).

Delay applied to DPI input control signals to generate DPI output control signals

Table 8-713.
EDP_CORE_ENC1_DPI_CTRL_OUT_DELAY_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0E88h |

Figure 8-352. EDP_CORE_ENC1_DPI_CTRL_OUT_DELAY_P Register

| | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DPI_CTRL_OUT_DELAY | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-714. EDP_CORE_ENC1_DPI_CTRL_OUT_DELAY_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | DPI_CTRL_OUT_DELAY | R/W | 0h | Delay in number of encx clock cycles. The delay should equal to InitialLines x Htotal[clk] where Htotal is the upstream source timing controller total line time [in clock cycles, not in pixels] including the horizontal blanking [Htotal[clk] = Hactive[clk] + Hblank[clk]]When in split panel mode, the Hactive[clk] is expected to be picture_width divided by 2 |

8.5.297 EDP_CORE_ENC1_GENERAL_STATUS_P Register (Offset = 00030EC0h) [reset = 18h]

EDP_CORE_ENC1_GENERAL_STATUS_P is shown in [Figure 8-353](#) and described in [Table 8-716](#).

Return to [Summary Table](#).

General Encoder Status

Table 8-715.
EDP_CORE_ENC1_GENERAL_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0EC0h |

Figure 8-353. EDP_CORE_ENC1_GENERAL_STATUS_P Register

| | | | | | | | |
|----------|-------------------------|-------------------------|--------------------------|--------------------------|------------|----------------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 | OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_START_ED | CE |
| R-0h | R-0h | R-0h | R-1h | R-1h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-716. EDP_CORE_ENC1_GENERAL_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 6 | OUT_BUFF_FULL_CONTEXT_1 | R | 0h | Output buffer 1 [soft slice 1] is full.For Debug purposes only. |
| 5 | OUT_BUFF_FULL_CONTEXT_0 | R | 0h | Output buffer 0 [soft slice 0] is full.For Debug purposes only. |
| 4 | OUT_BUFF_EMPTY_CONTEXT_1 | R | 1h | Output buffer 1 [soft slice 1] is empty.For Debug purposes only. |
| 3 | OUT_BUFF_EMPTY_CONTEXT_0 | R | 1h | Output buffer 0 [soft slice 0] is empty.For Debug purposes only. |
| 2 | FRAME_DONE | R | 0h | Encoder finished a frame |
| 1 | FRAME_STARTED | R | 0h | Encoder is currently processing a frame |
| 0 | CE | R | 0h | Flow control internal clock enable status.For Debug purposes only. |

8.5.298 EDP_CORE_ENC1_HSLICE_STATUS_P Register (Offset = 00030EC4h) [reset = 0h]

EDP_CORE_ENC1_HSLICE_STATUS_P is shown in [Figure 8-354](#) and described in [Table 8-718](#).

[Return to Summary Table.](#)

Hard Slice Encoded Status

**Table 8-717. EDP_CORE_ENC1_HSLICE_STATUS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0EC4h |

Figure 8-354. EDP_CORE_ENC1_HSLICE_STATUS_P Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SLICE_COUNT_ENCODED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLICE_LINE_COUNT_ENCODED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-718. EDP_CORE_ENC1_HSLICE_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-16 | SLICE_COUNT_ENCODED | R | 0h | Actual slice number of current frame being processed at VLC encoder. Not re-synchronized in register clock domain. For Debug purposes only. |
| 15-0 | SLICE_LINE_COUNT_ENCODED | R | 0h | Actual line number of current slice being processed at VLC encoder. Not re-synchronized in register clock domain. For Debug purposes only. |

8.5.299 EDP_CORE_ENC1_OUT_STATUS_P Register (Offset = 00030EC8h) [reset = 0h]

EDP_CORE_ENC1_OUT_STATUS_P is shown in [Figure 8-355](#) and described in [Table 8-720](#).

Return to [Summary Table](#).

Outputted Slice Status

Table 8-719. EDP_CORE_ENC1_OUT_STATUS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0EC8h |

Figure 8-355. EDP_CORE_ENC1_OUT_STATUS_P Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SLICE_COUNT_OUT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLICE_LINE_COUNT_OUT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-720. EDP_CORE_ENC1_OUT_STATUS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-16 | SLICE_COUNT_OUT | R | 0h | Actual slice number of current frame being read at output interface. Not re-synchronized in register clock domain. For Debug purposes only. |
| 15-0 | SLICE_LINE_COUNT_OUT | R | 0h | Actual line number of current slice being read at output interface. Not re-synchronized in register clock domain. For Debug purposes only. |

8.5.300 EDP_CORE_ENC1_INT_STAT_P Register (Offset = 00030ECCh) [reset = 0h]

EDP_CORE_ENC1_INT_STAT_P is shown in [Figure 8-356](#) and described in [Table 8-722](#).

Return to [Summary Table](#).

Encoder Interrupt Status

**Table 8-721. EDP_CORE_ENC1_INT_STAT_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0ECCh |

Figure 8-356. EDP_CORE_ENC1_INT_STAT_P Register

| | | | | | | | |
|--------------------------|------------|---------------|------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-722. EDP_CORE_ENC1_INT_STAT_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R | 0h | Output buffer 1 [soft slice 1] became full |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R | 0h | Output buffer 0 [soft slice 0] became full |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R | 0h | Output buffer 1 [soft slice 1] became empty |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R | 0h | Output buffer 0 [soft slice 0] became empty |
| 6 | FRAME_DONE | R | 0h | Encoder finished a frame |
| 5 | FRAME_STARTED | R | 0h | Encoder is started to process a frame |
| 4 | CE | R | 0h | Flow control internal clock enable becomes high |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R | 0h | output buffer 1 [soft slice 1] underflow |

Table 8-722. EDP_CORE_ENC1_INT_STAT_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|--|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R | 0h | output buffer 0 [soft slice 0] underflow |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R | 0h | output buffer 1 [soft slice 1] underflow |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R | 0h | output buffer 0 [soft slice 0] underflow |

8.5.301 EDP_CORE_ENC1_INT_CLR_P Register (Offset = 00030ED0h) [reset = 0h]

EDP_CORE_ENC1_INT_CLR_P is shown in [Figure 8-357](#) and described in [Table 8-724](#).

Return to [Summary Table](#).

Encoder Interrupt Clear. Setting any one of these bits, clears the corresponding ENC_INT_STAT bits. This register is self-clearing after 8 regs_pclk cycles.

**Table 8-723. EDP_CORE_ENC1_INT_CLR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0ED0h |

Figure 8-357. EDP_CORE_ENC1_INT_CLR_P Register

| | | | | | | | |
|--------------------------|------------|----------------|--------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_START_ED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-724. EDP_CORE_ENC1_INT_CLR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became full |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became full |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became empty |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became empty |
| 6 | FRAME_DONE | R/W | 0h | Encoder finished a frame |
| 5 | FRAME_STARTED | R/W | 0h | Encoder is started to process a frame |
| 4 | CE | R/W | 0h | Flow control internal clock enable |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R/W | 0h | rc model buffer 1 overflow |

Table 8-724. EDP_CORE_ENC1_INT_CLR_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|----------------------------|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R/W | 0h | rc model buffer 0 overflow |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R/W | 0h | output buffer 1 underflow |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R/W | 0h | output buffer 0 underflow |

8.5.302 EDP_CORE_ENC1_INT_MASK_P Register (Offset = 00030ED4h) [reset = 0h]

EDP_CORE_ENC1_INT_MASK_P is shown in [Figure 8-358](#) and described in [Table 8-726](#).

Return to [Summary Table](#).

Encoder Interrupt Mask. Any bit set to 1'b1 is enabled to report an interrupt on the corresponding bit position

**Table 8-725. EDP_CORE_ENC1_INT_MASK_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0ED4h |

Figure 8-358. EDP_CORE_ENC1_INT_MASK_P Register

| | | | | | | | |
|--------------------------|------------|---------------|--------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-726. EDP_CORE_ENC1_INT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became full |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became full |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became empty |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became empty |
| 6 | FRAME_DONE | R/W | 0h | Encoder finished a frame |
| 5 | FRAME_STARTED | R/W | 0h | Encoder is started to process a frame |
| 4 | CE | R/W | 0h | Flow control internal clock enable |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R/W | 0h | rc model buffer 1 overflow |

Table 8-726. EDP_CORE_ENC1_INT_MASK_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|----------------------------|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R/W | 0h | rc model buffer 0 overflow |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R/W | 0h | enc underflow 1 underflow |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R/W | 0h | enc underflow 0 underflow |

8.5.303 EDP_CORE_ENC1_INT_TEST_P Register (Offset = 00030ED8h) [reset = 0h]

EDP_CORE_ENC1_INT_TEST_P is shown in [Figure 8-359](#) and described in [Table 8-728](#).

Return to [Summary Table](#).

Encoder Interrupt Test. Setting any one of these bits to 0x0 and then to 0x1 simulate a hardware event and generate an interrupt if the corresponding ENC_x_INT_MASK bit is set.

**Table 8-727. EDP_CORE_ENC1_INT_TEST_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0ED8h |

Figure 8-359. EDP_CORE_ENC1_INT_TEST_P Register

| | | | | | | | |
|--------------------------|------------|---------------|--------|---|---|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | OUT_BUFF_FULL_CONTEXT_1 | OUT_BUFF_FULL_CONTEXT_0 | OUT_BUFF_EMPTY_CONTEXT_1 |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OUT_BUFF_EMPTY_CONTEXT_0 | FRAME_DONE | FRAME_STARTED | CE | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | ENC_UNDERFLOW_CONTEXT_1 | ENC_UNDERFLOW_CONTEXT_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-728. EDP_CORE_ENC1_INT_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | OUT_BUFF_FULL_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became full test |
| 9 | OUT_BUFF_FULL_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became full test |
| 8 | OUT_BUFF_EMPTY_CONTEXT_1 | R/W | 0h | Output buffer 1 [soft slice 1] became empty test |
| 7 | OUT_BUFF_EMPTY_CONTEXT_0 | R/W | 0h | Output buffer 0 [soft slice 0] became empty test |
| 6 | FRAME_DONE | R/W | 0h | Encoder finished a frame test |
| 5 | FRAME_STARTED | R/W | 0h | Encoder is started to process a frame test |
| 4 | CE | R/W | 0h | Flow control internal clock enable test |
| 3 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_1 | R/W | 0h | rc model buffer 1 overflow test |

Table 8-728. EDP_CORE_ENC1_INT_TEST_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|---------------------------------|
| 2 | RC_MODEL_BUFFER_FULLNESS_OVERFLOW_CONTEXT_0 | R/W | 0h | rc model buffer 0 overflow test |
| 1 | ENC_UNDERFLOW_CONTEXT_1 | R/W | 0h | enc underflow 1 underflow test |
| 0 | ENC_UNDERFLOW_CONTEXT_0 | R/W | 0h | enc underflow 0 underflow test |

8.5.304 EDP_CORE_ENC_ASF_INT_STAT_P Register (Offset = 00030F00h) [reset = 0h]

EDP_CORE_ENC_ASF_INT_STAT_P is shown in [Figure 8-360](#) and described in [Table 8-730](#).

Return to [Summary Table](#).

Encoder ASF Interrupt Status

**Table 8-729. EDP_CORE_ENC_ASF_INT_STAT_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F00h |

Figure 8-360. EDP_CORE_ENC_ASF_INT_STAT_P Register

| | | | | | | | |
|-----------------------|----------------------|----------------------------------|--------------------------------|-----------------------|----------------------|----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ASF_CSR_ER R |
| R-0h | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC1_SELF_C HK_ERR | ENC1_OUT_C HK_ERR | ENC1_ASF_SR AM_UNCORR_ ERR | ENC1_ASF_SR AM_CORR_ER R | ENC0_SELF_C HK_ERR | ENC0_OUT_C HK_ERR | ENC0_ASF_SR AM_UNCORR_ ERR | ENC0_ASF_SR AM_CORR_ER R |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-730. EDP_CORE_ENC_ASF_INT_STAT_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|---|
| 31-9 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 8 | ASF_CSR_ERR | R | 0h | Configuration and status registers uncorrectable error interrupt |
| 7 | ENC1_SELF_CHK_ERR | R | 0h | Hard Slice 1 Encoder self-check uncorrectable error interrupt |
| 6 | ENC1_OUT_CHK_ERR | R | 0h | Hard Slice 1 Encoder output checker uncorrectable error interrupt |
| 5 | ENC1_ASF_SRAM_UNCORR_ERR | R | 0h | Hard Slice 1 SRAM uncorrectable error interrupt |
| 4 | ENC1_ASF_SRAM_CORR_ERR | R | 0h | Hard Slice 1 SRAM correctable error interrupt |
| 3 | ENC0_SELF_CHK_ERR | R | 0h | Hard Slice 0 Encoder self-check uncorrectable error interrupt |
| 2 | ENC0_OUT_CHK_ERR | R | 0h | Hard Slice 0 Encoder output checker uncorrectable error interrupt |
| 1 | ENC0_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 0 SRAM uncorrectable error interrupt |
| 0 | ENC0_ASF_SRAM_CORR_ERR | R | 0h | Hard Slice 0 SRAM correctable error interrupt |

8.5.305 EDP_CORE_ENC_ASF_INT_MASK_P Register (Offset = 00030F04h) [reset = 0h]

EDP_CORE_ENC_ASF_INT_MASK_P is shown in [Figure 8-361](#) and described in [Table 8-732](#).

Return to [Summary Table](#).

Encoder ASF Interrupt Mask. Any bit set to 1'b1 is enabled to report an interrupt on the corresponding bit position

Table 8-731. EDP_CORE_ENC_ASF_INT_MASK_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F04h |

Figure 8-361. EDP_CORE_ENC_ASF_INT_MASK_P Register

| | | | | | | | |
|-------------------|------------------|--------------------------|------------------------|-------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ASF_CSR_ERR |
| R-0h | | | | | | | R |
| | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC1_SELF_CHK_ERR | ENC1_OUT_CHK_ERR | ENC1_ASF_SRAM_UNCORR_ERR | ENC1_ASF_SRAM_CORR_ERR | ENC0_SELF_CHK_ERR | ENC0_OUT_CHK_ERR | ENC0_ASF_SRAM_UNCORR_ERR | ENC0_ASF_SRAM_CORR_ERR |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-732. EDP_CORE_ENC_ASF_INT_MASK_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|---|
| 31-9 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 8 | ASF_CSR_ERR | R/W | 0h | Configuration and status registers uncorrectable error interrupt |
| 7 | ENC1_SELF_CHK_ERR | R/W | 0h | Hard Slice 1 Encoder self-check uncorrectable error interrupt |
| 6 | ENC1_OUT_CHK_ERR | R/W | 0h | Hard Slice 1 Encoder output checker uncorrectable error interrupt |
| 5 | ENC1_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 1 SRAM uncorrectable error interrupt |
| 4 | ENC1_ASF_SRAM_CORR_ERR | R/W | 0h | Hard Slice 1 SRAM correctable error interrupt |
| 3 | ENC0_SELF_CHK_ERR | R/W | 0h | Hard Slice 0 Encoder self-check uncorrectable error interrupt |
| 2 | ENC0_OUT_CHK_ERR | R/W | 0h | Hard Slice 0 Encoder output checker uncorrectable error interrupt |
| 1 | ENC0_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 0 SRAM uncorrectable error interrupt |
| 0 | ENC0_ASF_SRAM_CORR_ERR | R/W | 0h | Hard Slice 0 SRAM correctable error interrupt |

8.5.306 EDP_CORE_ENC_ASF_INT_CLR_P Register (Offset = 00030F08h) [reset = 0h]

EDP_CORE_ENC_ASF_INT_CLR_P is shown in [Figure 8-362](#) and described in [Table 8-734](#).

Return to [Summary Table](#).

Encoder ASF Interrupt Clear. Setting any one of these bits, clears the corresponding ENC_ASF_INT_STAT bits

**Table 8-733. EDP_CORE_ENC_ASF_INT_CLR_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F08h |

Figure 8-362. EDP_CORE_ENC_ASF_INT_CLR_P Register

| | | | | | | | |
|-------------------|------------------|--------------------------|------------------------|-------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ASF_CSR_ERR |
| R-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC1_SELF_CHK_ERR | ENC1_OUT_CHK_ERR | ENC1_ASF_SRAM_UNCORR_ERR | ENC1_ASF_SRAM_CORR_ERR | ENC0_SELF_CHK_ERR | ENC0_OUT_CHK_ERR | ENC0_ASF_SRAM_UNCORR_ERR | ENC0_ASF_SRAM_CORR_ERR |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-734. EDP_CORE_ENC_ASF_INT_CLR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|---|
| 31-9 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 8 | ASF_CSR_ERR | R/W | 0h | Configuration and status registers uncorrectable error interrupt |
| 7 | ENC1_SELF_CHK_ERR | R/W | 0h | Hard Slice 1 Encoder self-check uncorrectable error interrupt |
| 6 | ENC1_OUT_CHK_ERR | R/W | 0h | Hard Slice 1 Encoder output checker uncorrectable error interrupt |
| 5 | ENC1_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 1 SRAM uncorrectable error interrupt |
| 4 | ENC1_ASF_SRAM_CORR_ERR | R/W | 0h | Hard Slice 1 SRAM correctable error interrupt |
| 3 | ENC0_SELF_CHK_ERR | R/W | 0h | Hard Slice 0 Encoder self-check uncorrectable error interrupt |
| 2 | ENC0_OUT_CHK_ERR | R/W | 0h | Hard Slice 0 Encoder output checker uncorrectable error interrupt |
| 1 | ENC0_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 0 SRAM uncorrectable error interrupt |
| 0 | ENC0_ASF_SRAM_CORR_ERR | R/W | 0h | Hard Slice 0 SRAM correctable error interrupt |

8.5.307 EDP_CORE_ENC_ASF_INT_TEST_P Register (Offset = 00030F0Ch) [reset = 0h]

EDP_CORE_ENC_ASF_INT_TEST_P is shown in [Figure 8-363](#) and described in [Table 8-736](#).

Return to [Summary Table](#).

Encoder ASF Interrupt Test. Setting any one of these bits to 0x0 and then to 0x1 simulate a hardware event and generate an interrupt if the corresponding ENC_ASF_INT_MASK bit is set

Table 8-735. EDP_CORE_ENC_ASF_INT_TEST_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F0Ch |

Figure 8-363. EDP_CORE_ENC_ASF_INT_TEST_P Register

| | | | | | | | |
|-------------------|------------------|--------------------------|------------------------|-------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | ASF_CSR_ERR |
| R-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC1_SELF_CHK_ERR | ENC1_OUT_CHK_ERR | ENC1_ASF_SRAM_UNCORR_ERR | ENC1_ASF_SRAM_CORR_ERR | ENC0_SELF_CHK_ERR | ENC0_OUT_CHK_ERR | ENC0_ASF_SRAM_UNCORR_ERR | ENC0_ASF_SRAM_CORR_ERR |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-736. EDP_CORE_ENC_ASF_INT_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-9 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 8 | ASF_CSR_ERR | R/W | 0h | Configuration and status registers uncorrectable error interrupt test |
| 7 | ENC1_SELF_CHK_ERR | R/W | 0h | Hard Slice 1 Encoder self-check uncorrectable error interrupt test |
| 6 | ENC1_OUT_CHK_ERR | R/W | 0h | Hard Slice 1 Encoder output checker uncorrectable error interrupt test |
| 5 | ENC1_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 1 SRAM uncorrectable error interrupt test |
| 4 | ENC1_ASF_SRAM_CORR_ERR | R/W | 0h | Hard Slice 1 SRAM correctable error interrupt test |
| 3 | ENC0_SELF_CHK_ERR | R/W | 0h | Hard Slice 0 Encoder self-check uncorrectable error interrupt test |
| 2 | ENC0_OUT_CHK_ERR | R/W | 0h | Hard Slice 0 Encoder output checker uncorrectable error interrupt test |
| 1 | ENC0_ASF_SRAM_UNCORR_ERR | R/W | 0h | Hard Slice 0 SRAM uncorrectable error interrupt test |

Table 8-736. EDP_CORE_ENC_ASF_INT_TEST_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 0 | ENC0_ASF_SRAM_COR R_ERR | R/W | 0h | Hard Slice 0 SRAM correctable error interrupt test |

8.5.308 EDP_CORE_ENC0_ASF_SRAM_CORR_P Register (Offset = 00030F20h) [reset = 0h]

EDP_CORE_ENC0_ASF_SRAM_CORR_P is shown in [Figure 8-364](#) and described in [Table 8-738](#).

Return to [Summary Table](#).

Hard Slice 0 Status register for SRAM uncorrectable fault

Table 8-737.
EDP_CORE_ENC0_ASF_SRAM_CORR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F20h |

Figure 8-364. EDP_CORE_ENC0_ASF_SRAM_CORR_P Register

| | | | | | | | |
|--------------------------|----|----|----|----|----|--------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ASF_SRAM_CORR_FAULT_INST | |
| R-0h | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-738. EDP_CORE_ENC0_ASF_SRAM_CORR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | ASF_SRAM_CORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. In case of simultaneous faults, priority is given to the highest number below. 3: SSM_S 2: SSM_D 1: Output Buffer 0: Line Buffer |
| 23-0 | ASF_SRAM_CORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault |

8.5.309 EDP_CORE_ENC0_ASF_SRAM_UNCORR_P Register (Offset = 00030F24h) [reset = 0h]

EDP_CORE_ENC0_ASF_SRAM_UNCORR_P is shown in [Figure 8-365](#) and described in [Table 8-740](#).

Return to [Summary Table](#).

Hard Slice 0 Status register for SRAM uncorrectable fault

Table 8-739.
EDP_CORE_ENC0_ASF_SRAM_UNCORR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F24h |

Figure 8-365. EDP_CORE_ENC0_ASF_SRAM_UNCORR_P Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|--------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ASF_SRAM_UNCORR_FAULT_I NST | |
| R-0h | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-740. EDP_CORE_ENC0_ASF_SRAM_UNCORR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | ASF_SRAM_UNCORR_F AULT_INST | R | 0h | Last SRAM instance that generated fault. In case of simultaneous faults, priority is given to the highest number below. 3: SSM_S 2: SSM_D 1: Output Buffer 0: Line Buffer |
| 23-0 | ASF_SRAM_UNCORR_F AULT_ADDR | R | 0h | Last SRAM address that generated fault |

8.5.310 EDP_CORE_ENC1_ASF_SRAM_CORR_P Register (Offset = 00030F28h) [reset = 0h]

EDP_CORE_ENC1_ASF_SRAM_CORR_P is shown in [Figure 8-366](#) and described in [Table 8-742](#).

Return to [Summary Table](#).

Hard Slice 1 Status register for SRAM uncorrectable fault

Table 8-741.
EDP_CORE_ENC1_ASF_SRAM_CORR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F28h |

Figure 8-366. EDP_CORE_ENC1_ASF_SRAM_CORR_P Register

| | | | | | | | |
|--------------------------|----|----|----|----|----|--------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ASF_SRAM_CORR_FAULT_INST | |
| R-0h | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-742. EDP_CORE_ENC1_ASF_SRAM_CORR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | ASF_SRAM_CORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. In case of simultaneous faults, priority is given to the highest number below. 3: SSM_S 2: SSM_D 1: Output Buffer 0: Line Buffer |
| 23-0 | ASF_SRAM_CORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault |

8.5.311 EDP_CORE_ENC1_ASF_SRAM_UNCORR_P Register (Offset = 00030F2Ch) [reset = 0h]

EDP_CORE_ENC1_ASF_SRAM_UNCORR_P is shown in [Figure 8-367](#) and described in [Table 8-744](#).

Return to [Summary Table](#).

Hard Slice 1 Status register for SRAM uncorrectable fault

Table 8-743.
EDP_CORE_ENC1_ASF_SRAM_UNCORR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F2Ch |

Figure 8-367. EDP_CORE_ENC1_ASF_SRAM_UNCORR_P Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|--------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | ASF_SRAM_UNCORR_FAULT_I NST | |
| R-0h | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-744. EDP_CORE_ENC1_ASF_SRAM_UNCORR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | ASF_SRAM_UNCORR_F AULT_INST | R | 0h | Last SRAM instance that generated fault. In case of simultaneous faults, priority is given to the highest number below. 3: SSM_S 2: SSM_D 1: Output Buffer 0: Line Buffer |
| 23-0 | ASF_SRAM_UNCORR_F AULT_ADDR | R | 0h | Last SRAM address that generated fault |

8.5.312 EDP_CORE_ENC0_ASF_CSR_CHK_TEST_P Register (Offset = 00030F30h) [reset = 0h]

EDP_CORE_ENC0_ASF_CSR_CHK_TEST_P is shown in [Figure 8-368](#) and described in [Table 8-746](#).

Return to [Summary Table](#).

Hard Slice 0 Test for CSR protection expected CRC

Table 8-745.
EDP_CORE_ENC0_ASF_CSR_CHK_TEST_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F30h |

Figure 8-368. EDP_CORE_ENC0_ASF_CSR_CHK_TEST_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC0_ASF_CSR_CHK_TEST | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-746. EDP_CORE_ENC0_ASF_CSR_CHK_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | ENC0_ASF_CSR_CHK_T EST | R/W | 0h | Each bit of the expected CRC can be corrupted separately [one bit at a time] using this register. |

8.5.313 EDP_CORE_ENC1_ASF_CSR_CHK_TEST_P Register (Offset = 00030F34h) [reset = 0h]

EDP_CORE_ENC1_ASF_CSR_CHK_TEST_P is shown in [Figure 8-369](#) and described in [Table 8-748](#).

Return to [Summary Table](#).

Hard Slice 1 Test for CSR protection expected CRC

Table 8-747.
EDP_CORE_ENC1_ASF_CSR_CHK_TEST_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F34h |

Figure 8-369. EDP_CORE_ENC1_ASF_CSR_CHK_TEST_P Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC1_ASF_CSR_CHK_TEST | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-748. EDP_CORE_ENC1_ASF_CSR_CHK_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | ENC1_ASF_CSR_CHK_T EST | R/W | 0h | Each bit of the expected CRC can be corrupted separately [one bit at a time] using this register. |

8.5.314 EDP_CORE_ENC0_ASF_SELF_CHK_TEST_P Register (Offset = 00030F38h) [reset = 0h]

EDP_CORE_ENC0_ASF_SELF_CHK_TEST_P is shown in [Figure 8-370](#) and described in [Table 8-750](#).

Return to [Summary Table](#).

Hard Slice 0 Test for Self Check expected CRC

Table 8-749.
EDP_CORE_ENC0_ASF_SELF_CHK_TEST_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F38h |

Figure 8-370. EDP_CORE_ENC0_ASF_SELF_CHK_TEST_P Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC0_ASF_SELF_CHK_TEST | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-750. EDP_CORE_ENC0_ASF_SELF_CHK_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | ENC0_ASF_SELF_CHK_TEST | R/W | 0h | Each bit of the expected CRC can be corrupted separately [one bit at a time] using this register. |

8.5.315 EDP_CORE_ENC1_ASF_SELF_CHK_TEST_P Register (Offset = 00030F3Ch) [reset = 0h]

EDP_CORE_ENC1_ASF_SELF_CHK_TEST_P is shown in [Figure 8-371](#) and described in [Table 8-752](#).

Return to [Summary Table](#).

Hard Slice 1 Test for Self Check expected CRC

Table 8-751.
EDP_CORE_ENC1_ASF_SELF_CHK_TEST_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F3Ch |

Figure 8-371. EDP_CORE_ENC1_ASF_SELF_CHK_TEST_P Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENC1_ASF_SELF_CHK_TEST | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-752. EDP_CORE_ENC1_ASF_SELF_CHK_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-0 | ENC1_ASF_SELF_CHK_TEST | R/W | 0h | Each bit of the expected CRC can be corrupted separately [one bit at a time] using this register. |

8.5.316 EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P Register (Offset = 00030F40h) [reset = 0h]

EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P is shown in [Figure 8-372](#) and described in [Table 8-754](#).

Return to [Summary Table](#).

Hard Slice 0 Test for Output Checker. Each bit (one at a time) can be used to corrupt various input/parameter values of the module.

Table 8-753.
EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F40h |

Figure 8-372. EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P Register

| | | | | | | | |
|-------------------------|----------------------|----------------------|---------------------|------------------|---------------|--------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | END_FRAME_OUT_STUCK1_ERR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| END_LINE_OUT_STUCK1_ERR | END_CHUNK_STUCK1_ERR | VALID_OUT_STUCK1_ERR | DATA_OUT_STUCK1_ERR | VALID_STUCK0_ERR | NVB_VALUE_ERR | LINE_CNT_ERR | BYTE_CNT_ERR |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-754. EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-9 | RESERVED | R/W | 0h | Reserved but this field is a R/W field that returns the same value that was written to it. |
| 8 | END_FRAME_OUT_STUCK1_ERR | R/W | 0h | |
| 7 | END_LINE_OUT_STUCK1_ERR | R/W | 0h | |
| 6 | END_CHUNK_STUCK1_ERR | R/W | 0h | |
| 5 | VALID_OUT_STUCK1_ERR | R/W | 0h | |
| 4 | DATA_OUT_STUCK1_ERR | R/W | 0h | |
| 3 | VALID_STUCK0_ERR | R/W | 0h | |
| 2 | NVB_VALUE_ERR | R/W | 0h | |

Table 8-754. EDP_CORE_ENC0_ASF_OUT_CHK_TEST_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-------------|
| 1 | LINE_CNT_ERR | R/W | 0h | |
| 0 | BYTE_CNT_ERR | R/W | 0h | |

8.5.317 EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P Register (Offset = 00030F44h) [reset = 0h]

EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P is shown in [Figure 8-373](#) and described in [Table 8-756](#).

Return to [Summary Table](#).

Hard Slice 1 Test for Output Checker. Each bit (one at a time) can be used to corrupt various input/parameter values of the module.

Table 8-755.
EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0F44h |

Figure 8-373. EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P Register

| | | | | | | | |
|-------------------------|----------------------|----------------------|---------------------|------------------|---------------|--------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | END_FRAME_OUT_STUCK1_ERR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| END_LINE_OUT_STUCK1_ERR | END_CHUNK_STUCK1_ERR | VALID_OUT_STUCK1_ERR | DATA_OUT_STUCK1_ERR | VALID_STUCK0_ERR | NVB_VALUE_ERR | LINE_CNT_ERR | BYTE_CNT_ERR |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-756. EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-16 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 15-9 | RESERVED | R/W | 0h | Reserved but this field is a R/W field that returns the same value that was written to it. |
| 8 | END_FRAME_OUT_STUCK1_ERR | R/W | 0h | |
| 7 | END_LINE_OUT_STUCK1_ERR | R/W | 0h | |
| 6 | END_CHUNK_STUCK1_ERR | R/W | 0h | |
| 5 | VALID_OUT_STUCK1_ERR | R/W | 0h | |
| 4 | DATA_OUT_STUCK1_ERR | R/W | 0h | |
| 3 | VALID_STUCK0_ERR | R/W | 0h | |
| 2 | NVB_VALUE_ERR | R/W | 0h | |

Table 8-756. EDP_CORE_ENC1_ASF_OUT_CHK_TEST_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-------------|
| 1 | LINE_CNT_ERR | R/W | 0h | |
| 0 | BYTE_CNT_ERR | R/W | 0h | |

8.5.318 EDP_CORE_AUDIO_SRC_CNTL_P Register (Offset = 00030000h) [reset = 0h]

EDP_CORE_AUDIO_SRC_CNTL_P is shown in [Figure 8-374](#) and described in [Table 8-758](#).

Return to [Summary Table](#).

Audio source control

Table 8-757. EDP_CORE_AUDIO_SRC_CNTL_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0000h |

Figure 8-374. EDP_CORE_AUDIO_SRC_CNTL_P Register

| | | | | | | | |
|----------|-----------|------------------|-----------|-------------|-----------------------|---------------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | VALID_ALL | VALID_BITS_FORCE | I2S_TS_EN | SPDIF_TS_EN | I2S_BLOCK_START_FORCE | I2S_DEC_START | SW_RST |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-758. EDP_CORE_AUDIO_SRC_CNTL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 6 | VALID_ALL | R/W | 0h | valid bit for all samples |
| 5 | VALID_BITS_FORCE | R/W | 0h | Force valid bits of the channels |
| 4 | I2S_TS_EN | R/W | 0h | Enable I2S Time Stamp when decoders are disabled |
| 3 | SPDIF_TS_EN | R/W | 0h | Enable SPDIF Time Stamp when decoders are disabled |
| 2 | I2S_BLOCK_START_FORCE | R/W | 0h | Force a Block Start in the audio stream |
| 1 | I2S_DEC_START | R/W | 0h | When high Source Decoder starts. |
| 0 | SW_RST | R/W | 0h | Software reset. Active high. |

8.5.319 EDP_CORE_AUDIO_SRC_CNFG_P Register (Offset = 00030004h) [reset = 0h]

EDP_CORE_AUDIO_SRC_CNFG_P is shown in [Figure 8-375](#) and described in [Table 8-760](#).

Return to [Summary Table](#).

Audio source configuration

**Table 8-759. EDP_CORE_AUDIO_SRC_CNFG_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0004h |

Figure 8-375. EDP_CORE_AUDIO_SRC_CNFG_P Register

| | | | | | | | |
|-----------------------|--------------|----|------------------|----|--------------------|------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | I2S_DEC_PORT_EN | | | AUDIO_CHAN NEL_TYPE | |
| R-0h | | | R/W-0h | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| AUDIO_CHANNEL_TYPE | | | TRANS_SMPL_WIDTH | | AUDIO_SAMPLE_WIDTH | | AUDIO_SAMPL E_JUST |
| R/W-0h | | | R/W-0h | | R/W-0h | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUDIO_SAMPL E_JUST | AUDIO_CH_NUM | | | | WS_POLARITY | | LOW_INDEX_ MSB |
| R/W-0h | R/W-0h | | | | R/W-0h | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-760. EDP_CORE_AUDIO_SRC_CNFG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-21 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 20-17 | I2S_DEC_PORT_EN | R/W | 0h | Enables the I2S Decoder ports. Allowed values are: 0001 - I2S port 0 is enabled. 0011 - I2S ports 0,1 are enabled. 1111 - I2S ports 0,1,2,3 are enabled. No other values are allowed. |
| 16-13 | AUDIO_CHANNEL_TYPE | R/W | 0h | Set the transmission type. |
| 12-11 | TRANS_SMPL_WIDTH | R/W | 0h | Decoder Word Select width: 00-16 bit 01-24 bit 10-32 bit |
| 10-9 | AUDIO_SAMPLE_WIDTH | R/W | 0h | Decoder sample width: 00-16 bit 01-24 bit 10-32 bit |

Table 8-760. EDP_CORE_AUDIO_SRC_CNFG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 8-7 | AUDIO_SAMPLE_JUST | R/W | 0h | Data justification setting: 00 left-justified 01 right-justified |
| 6-2 | AUDIO_CH_NUM | R/W | 0h | Number of channels to decode |
| 1 | WS_POLARITY | R/W | 0h | Word Select Polarity. 0: No change 1: Inverted. |
| 0 | LOW_INDEX_MSB | R/W | 0h | When low MSB is transmitted first. When high LSB is transmitted first. |

8.5.320 EDP_CORE_COM_CH_STTS_BITS_P Register (Offset = 00030008h) [reset = 0h]

EDP_CORE_COM_CH_STTS_BITS_P is shown in [Figure 8-376](#) and described in [Table 8-762](#).

Return to [Summary Table](#).

Common channels configuration

**Table 8-761. EDP_CORE_COM_CH_STTS_BITS_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0008h |

Figure 8-376. EDP_CORE_COM_CH_STTS_BITS_P Register

| | | | | | | | |
|----------------|----|----|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | ORIGINAL_SAMP_FREQ | | | |
| R-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLOCK_ACCURACY | | | | SAMPLING_FREQ | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CATEGORY_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BYTE0 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-762. EDP_CORE_COM_CH_STTS_BITS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 27-24 | ORIGINAL_SAMP_FREQ | R/W | 0h | Original Sampling Freq. of transmitted channel. Same for all channels. |
| 23-20 | CLOCK_ACCURACY | R/W | 0h | Clock Accuracy of transmitted channel. Same for all channels. |
| 19-16 | SAMPLING_FREQ | R/W | 0h | Sampling Frequency of transmitted channel. Same for all channels. |
| 15-8 | CATEGORY_CODE | R/W | 0h | Category Code of transmitted channel. Same for all channels. |
| 7-0 | BYTE0 | R/W | 0h | Byte 0 of transmitted channel. Same for all channels. |

8.5.321 EDP_CORE_STTS_BIT_CH01_P Register (Offset = 0003000Ch) [reset = 0h]

EDP_CORE_STTS_BIT_CH01_P is shown in [Figure 8-377](#) and described in [Table 8-764](#).

Return to [Summary Table](#).

Channels 0,1 configuration

Table 8-763. EDP_CORE_STTS_BIT_CH01_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 000Ch |

Figure 8-377. EDP_CORE_STTS_BIT_CH01_P Register

| | | | | | | | |
|-----------------|----|----|----|-----------------|----|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS1_0 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH1 | | | | CHANNEL_NUM_CH1 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH1 | | | | WORD_LENGTH_CH0 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH0 | | | | SOURCE_NUM_CH0 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-764. EDP_CORE_STTS_BIT_CH01_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS1_0 | R/W | 0h | Valid Bits for channel 1 and 0 if force is enabled |
| 23-20 | WORD_LENGTH_CH1 | R/W | 0h | Channel 1 word length. |
| 19-16 | CHANNEL_NUM_CH1 | R/W | 0h | Channel 1 channel number. |
| 15-12 | SOURCE_NUM_CH1 | R/W | 0h | Channel 1 Source number. |
| 11-8 | WORD_LENGTH_CH0 | R/W | 0h | Channel 0 word length. |
| 7-4 | CHANNEL_NUM_CH0 | R/W | 0h | Channel 0 channel number. |
| 3-0 | SOURCE_NUM_CH0 | R/W | 0h | Channel 0 Source number. |

8.5.322 EDP_CORE_STTS_BIT_CH23_P Register (Offset = 00030010h) [reset = 0h]

EDP_CORE_STTS_BIT_CH23_P is shown in [Figure 8-378](#) and described in [Table 8-766](#).

Return to [Summary Table](#).

Channels 2,3 configuration

**Table 8-765. EDP_CORE_STTS_BIT_CH23_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0010h |

Figure 8-378. EDP_CORE_STTS_BIT_CH23_P Register

| | | | | | | | |
|-----------------|----|----|----|-----------------|----|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS3_2 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH3 | | | | CHANNEL_NUM_CH3 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH3 | | | | WORD_LENGTH_CH2 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH2 | | | | SOURCE_NUM_CH2 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-766. EDP_CORE_STTS_BIT_CH23_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS3_2 | R/W | 0h | Valid Bits for channel 3 and 2 if force is enabled |
| 23-20 | WORD_LENGTH_CH3 | R/W | 0h | Channel 3 word length. |
| 19-16 | CHANNEL_NUM_CH3 | R/W | 0h | Channel 3 channel number. |
| 15-12 | SOURCE_NUM_CH3 | R/W | 0h | Channel 3 Source number. |
| 11-8 | WORD_LENGTH_CH2 | R/W | 0h | Channel 2 word length. |
| 7-4 | CHANNEL_NUM_CH2 | R/W | 0h | Channel 2 channel number. |
| 3-0 | SOURCE_NUM_CH2 | R/W | 0h | Channel 2 Source number. |

8.5.323 EDP_CORE_STTS_BIT_CH45_P Register (Offset = 00030014h) [reset = 0h]

EDP_CORE_STTS_BIT_CH45_P is shown in [Figure 8-379](#) and described in [Table 8-768](#).

Return to [Summary Table](#).

Channels 4,5 configuration

Table 8-767. EDP_CORE_STTS_BIT_CH45_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0014h |

Figure 8-379. EDP_CORE_STTS_BIT_CH45_P Register

| | | | | | | | |
|-----------------|----|----|----|-----------------|----|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS5_4 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH5 | | | | CHANNEL_NUM_CH5 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH5 | | | | WORD_LENGTH_CH4 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH4 | | | | SOURCE_NUM_CH4 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-768. EDP_CORE_STTS_BIT_CH45_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS5_4 | R/W | 0h | Valid Bits for channel 5 and 4 if force is enabled |
| 23-20 | WORD_LENGTH_CH5 | R/W | 0h | Channel 5 word length. |
| 19-16 | CHANNEL_NUM_CH5 | R/W | 0h | Channel 5 channel number. |
| 15-12 | SOURCE_NUM_CH5 | R/W | 0h | Channel 5 Source number. |
| 11-8 | WORD_LENGTH_CH4 | R/W | 0h | Channel 4 word length. |
| 7-4 | CHANNEL_NUM_CH4 | R/W | 0h | Channel 4 channel number. |
| 3-0 | SOURCE_NUM_CH4 | R/W | 0h | Channel 4 Source number. |

8.5.324 EDP_CORE_STTS_BIT_CH67_P Register (Offset = 00030018h) [reset = 0h]

EDP_CORE_STTS_BIT_CH67_P is shown in [Figure 8-380](#) and described in [Table 8-770](#).

Return to [Summary Table](#).

Channels 6,7 configuration

**Table 8-769. EDP_CORE_STTS_BIT_CH67_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0018h |

Figure 8-380. EDP_CORE_STTS_BIT_CH67_P Register

| | | | | | | | |
|-----------------|----|----|----|-----------------|----|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS7_6 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH7 | | | | CHANNEL_NUM_CH7 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH7 | | | | WORD_LENGTH_CH6 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH6 | | | | SOURCE_NUM_CH6 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-770. EDP_CORE_STTS_BIT_CH67_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS7_6 | R/W | 0h | Valid Bits for channel 7 and 6 if force is enabled |
| 23-20 | WORD_LENGTH_CH7 | R/W | 0h | Channel 7 word length. |
| 19-16 | CHANNEL_NUM_CH7 | R/W | 0h | Channel 7 channel number. |
| 15-12 | SOURCE_NUM_CH7 | R/W | 0h | Channel 7 Source number. |
| 11-8 | WORD_LENGTH_CH6 | R/W | 0h | Channel 6 word length. |
| 7-4 | CHANNEL_NUM_CH6 | R/W | 0h | Channel 6 channel number. |
| 3-0 | SOURCE_NUM_CH6 | R/W | 0h | Channel 6 Source number. |

8.5.325 EDP_CORE_STTS_BIT_CH89_P Register (Offset = 0003001Ch) [reset = 0h]

EDP_CORE_STTS_BIT_CH89_P is shown in [Figure 8-381](#) and described in [Table 8-772](#).

Return to [Summary Table](#).

Channels 8,9 configuration

Table 8-771. EDP_CORE_STTS_BIT_CH89_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 001Ch |

Figure 8-381. EDP_CORE_STTS_BIT_CH89_P Register

| | | | | | | | |
|-----------------|----|----|----|-----------------|----|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS9_8 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH9 | | | | CHANNEL_NUM_CH9 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH9 | | | | WORD_LENGTH_CH8 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH8 | | | | SOURCE_NUM_CH8 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-772. EDP_CORE_STTS_BIT_CH89_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS9_8 | R/W | 0h | Valid Bits for channel 9 and 8 if force is enabled |
| 23-20 | WORD_LENGTH_CH9 | R/W | 0h | Channel 9 word length. |
| 19-16 | CHANNEL_NUM_CH9 | R/W | 0h | Channel 9 channel number. |
| 15-12 | SOURCE_NUM_CH9 | R/W | 0h | Channel 9 Source number. |
| 11-8 | WORD_LENGTH_CH8 | R/W | 0h | Channel 8 word length. |
| 7-4 | CHANNEL_NUM_CH8 | R/W | 0h | Channel 8 channel number. |
| 3-0 | SOURCE_NUM_CH8 | R/W | 0h | Channel 8 Source number. |

8.5.326 EDP_CORE_STTS_BIT_CH1011_P Register (Offset = 00030020h) [reset = 0h]

EDP_CORE_STTS_BIT_CH1011_P is shown in [Figure 8-382](#) and described in [Table 8-774](#).

Return to [Summary Table](#).

Channels 10,11 configuration

Table 8-773. EDP_CORE_STTS_BIT_CH1011_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0020h |

Figure 8-382. EDP_CORE_STTS_BIT_CH1011_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS11_10 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH11 | | | | CHANNEL_NUM_CH11 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH11 | | | | WORD_LENGTH_CH10 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH10 | | | | SOURCE_NUM_CH10 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-774. EDP_CORE_STTS_BIT_CH1011_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS11_10 | R/W | 0h | Valid Bits for channel 11 and 10 if force is enabled |
| 23-20 | WORD_LENGTH_CH11 | R/W | 0h | Channel 11 word length. |
| 19-16 | CHANNEL_NUM_CH11 | R/W | 0h | Channel 11 channel number. |
| 15-12 | SOURCE_NUM_CH11 | R/W | 0h | Channel 11 Source number. |
| 11-8 | WORD_LENGTH_CH10 | R/W | 0h | Channel 10 word length. |
| 7-4 | CHANNEL_NUM_CH10 | R/W | 0h | Channel 10 channel number. |
| 3-0 | SOURCE_NUM_CH10 | R/W | 0h | Channel 10 Source number. |

8.5.327 EDP_CORE_STTS_BIT_CH1213_P Register (Offset = 00030024h) [reset = 0h]

EDP_CORE_STTS_BIT_CH1213_P is shown in [Figure 8-383](#) and described in [Table 8-776](#).

Return to [Summary Table](#).

Channels 12,13 configuration

Table 8-775. EDP_CORE_STTS_BIT_CH1213_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0024h |

Figure 8-383. EDP_CORE_STTS_BIT_CH1213_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS13_12 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH13 | | | | CHANNEL_NUM_CH13 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH13 | | | | WORD_LENGTH_CH12 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH12 | | | | SOURCE_NUM_CH12 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-776. EDP_CORE_STTS_BIT_CH1213_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS13_12 | R/W | 0h | Valid Bits for channel 13 and 12 if force is enabled |
| 23-20 | WORD_LENGTH_CH13 | R/W | 0h | Channel 13 word length. |
| 19-16 | CHANNEL_NUM_CH13 | R/W | 0h | Channel 13 channel number. |
| 15-12 | SOURCE_NUM_CH13 | R/W | 0h | Channel 13 Source number. |
| 11-8 | WORD_LENGTH_CH12 | R/W | 0h | Channel 12 word length. |
| 7-4 | CHANNEL_NUM_CH12 | R/W | 0h | Channel 12 channel number. |
| 3-0 | SOURCE_NUM_CH12 | R/W | 0h | Channel 12 Source number. |

8.5.328 EDP_CORE_STTS_BIT_CH1415_P Register (Offset = 00030028h) [reset = 0h]

EDP_CORE_STTS_BIT_CH1415_P is shown in [Figure 8-384](#) and described in [Table 8-778](#).

Return to [Summary Table](#).

Channels 14,15 configuration

**Table 8-777. EDP_CORE_STTS_BIT_CH1415_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0028h |

Figure 8-384. EDP_CORE_STTS_BIT_CH1415_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS15_14 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH15 | | | | CHANNEL_NUM_CH15 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH15 | | | | WORD_LENGTH_CH14 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH14 | | | | SOURCE_NUM_CH14 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-778. EDP_CORE_STTS_BIT_CH1415_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS15_14 | R/W | 0h | Valid Bits for channel 15 and 14 if force is enabled |
| 23-20 | WORD_LENGTH_CH15 | R/W | 0h | Channel 15 word length. |
| 19-16 | CHANNEL_NUM_CH15 | R/W | 0h | Channel 15 channel number. |
| 15-12 | SOURCE_NUM_CH15 | R/W | 0h | Channel 15 Source number. |
| 11-8 | WORD_LENGTH_CH14 | R/W | 0h | Channel 14 word length. |
| 7-4 | CHANNEL_NUM_CH14 | R/W | 0h | Channel 14 channel number. |
| 3-0 | SOURCE_NUM_CH14 | R/W | 0h | Channel 14 Source number. |

8.5.329 EDP_CORE_STTS_BIT_CH1617_P Register (Offset = 0003002Ch) [reset = 0h]

EDP_CORE_STTS_BIT_CH1617_P is shown in [Figure 8-385](#) and described in [Table 8-780](#).

Return to [Summary Table](#).

Channels 16,17 configuration

Table 8-779. EDP_CORE_STTS_BIT_CH1617_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 002Ch |

Figure 8-385. EDP_CORE_STTS_BIT_CH1617_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS17_16 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH17 | | | | CHANNEL_NUM_CH17 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH17 | | | | WORD_LENGTH_CH16 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH16 | | | | SOURCE_NUM_CH16 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-780. EDP_CORE_STTS_BIT_CH1617_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS17_16 | R/W | 0h | Valid Bits for channel 17 and 16 if force is enabled |
| 23-20 | WORD_LENGTH_CH17 | R/W | 0h | Channel 17 word length. |
| 19-16 | CHANNEL_NUM_CH17 | R/W | 0h | Channel 17 channel number. |
| 15-12 | SOURCE_NUM_CH17 | R/W | 0h | Channel 17 Source number. |
| 11-8 | WORD_LENGTH_CH16 | R/W | 0h | Channel 16 word length. |
| 7-4 | CHANNEL_NUM_CH16 | R/W | 0h | Channel 16 channel number. |
| 3-0 | SOURCE_NUM_CH16 | R/W | 0h | Channel 16 Source number. |

8.5.330 EDP_CORE_STTS_BIT_CH1819_P Register (Offset = 00030030h) [reset = 0h]

EDP_CORE_STTS_BIT_CH1819_P is shown in [Figure 8-386](#) and described in [Table 8-782](#).

Return to [Summary Table](#).

Channels 18,19 configuration

**Table 8-781. EDP_CORE_STTS_BIT_CH1819_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0030h |

Figure 8-386. EDP_CORE_STTS_BIT_CH1819_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS19_18 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH19 | | | | CHANNEL_NUM_CH19 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH19 | | | | WORD_LENGTH_CH18 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH18 | | | | SOURCE_NUM_CH18 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-782. EDP_CORE_STTS_BIT_CH1819_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS19_18 | R/W | 0h | Valid Bits for channel 19 and 18 if force is enabled |
| 23-20 | WORD_LENGTH_CH19 | R/W | 0h | Channel 19 word length. |
| 19-16 | CHANNEL_NUM_CH19 | R/W | 0h | Channel 19 channel number. |
| 15-12 | SOURCE_NUM_CH19 | R/W | 0h | Channel 19 Source number. |
| 11-8 | WORD_LENGTH_CH18 | R/W | 0h | Channel 18 word length. |
| 7-4 | CHANNEL_NUM_CH18 | R/W | 0h | Channel 18 channel number. |
| 3-0 | SOURCE_NUM_CH18 | R/W | 0h | Channel 18 Source number. |

8.5.331 EDP_CORE_STTS_BIT_CH2021_P Register (Offset = 00030034h) [reset = 0h]

EDP_CORE_STTS_BIT_CH2021_P is shown in [Figure 8-387](#) and described in [Table 8-784](#).

Return to [Summary Table](#).

Channels 20,21 configuration

Table 8-783. EDP_CORE_STTS_BIT_CH2021_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0034h |

Figure 8-387. EDP_CORE_STTS_BIT_CH2021_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS21_20 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH21 | | | | CHANNEL_NUM_CH21 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH21 | | | | WORD_LENGTH_CH20 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH20 | | | | SOURCE_NUM_CH20 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-784. EDP_CORE_STTS_BIT_CH2021_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS21_20 | R/W | 0h | Valid Bits for channel 21 and 20 if force is enabled |
| 23-20 | WORD_LENGTH_CH21 | R/W | 0h | Channel 21 word length. |
| 19-16 | CHANNEL_NUM_CH21 | R/W | 0h | Channel 21 channel number. |
| 15-12 | SOURCE_NUM_CH21 | R/W | 0h | Channel 21 Source number. |
| 11-8 | WORD_LENGTH_CH20 | R/W | 0h | Channel 20 word length. |
| 7-4 | CHANNEL_NUM_CH20 | R/W | 0h | Channel 20 channel number. |
| 3-0 | SOURCE_NUM_CH20 | R/W | 0h | Channel 20 Source number. |

8.5.332 EDP_CORE_STTS_BIT_CH2223_P Register (Offset = 00030038h) [reset = 0h]

EDP_CORE_STTS_BIT_CH2223_P is shown in [Figure 8-388](#) and described in [Table 8-786](#).

Return to [Summary Table](#).

Channels 22,23 configuration

**Table 8-785. EDP_CORE_STTS_BIT_CH2223_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0038h |

Figure 8-388. EDP_CORE_STTS_BIT_CH2223_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS23_22 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH23 | | | | CHANNEL_NUM_CH23 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH23 | | | | WORD_LENGTH_CH22 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH22 | | | | SOURCE_NUM_CH22 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-786. EDP_CORE_STTS_BIT_CH2223_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS23_22 | R/W | 0h | Valid Bits for channel 23 and 22 if force is enabled |
| 23-20 | WORD_LENGTH_CH23 | R/W | 0h | Channel 23 word length. |
| 19-16 | CHANNEL_NUM_CH23 | R/W | 0h | Channel 23 channel number. |
| 15-12 | SOURCE_NUM_CH23 | R/W | 0h | Channel 23 Source number. |
| 11-8 | WORD_LENGTH_CH22 | R/W | 0h | Channel 22 word length. |
| 7-4 | CHANNEL_NUM_CH22 | R/W | 0h | Channel 22 channel number. |
| 3-0 | SOURCE_NUM_CH22 | R/W | 0h | Channel 22 Source number. |

8.5.333 EDP_CORE_STTS_BIT_CH2425_P Register (Offset = 0003003Ch) [reset = 0h]

EDP_CORE_STTS_BIT_CH2425_P is shown in [Figure 8-389](#) and described in [Table 8-788](#).

Return to [Summary Table](#).

Channels 24,25 configuration

Table 8-787. EDP_CORE_STTS_BIT_CH2425_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 003Ch |

Figure 8-389. EDP_CORE_STTS_BIT_CH2425_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS25_24 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH25 | | | | CHANNEL_NUM_CH25 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH25 | | | | WORD_LENGTH_CH24 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH24 | | | | SOURCE_NUM_CH24 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-788. EDP_CORE_STTS_BIT_CH2425_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS25_24 | R/W | 0h | Valid Bits for channel 25 and 24 if force is enabled |
| 23-20 | WORD_LENGTH_CH25 | R/W | 0h | Channel 25 word length. |
| 19-16 | CHANNEL_NUM_CH25 | R/W | 0h | Channel 25 channel number. |
| 15-12 | SOURCE_NUM_CH25 | R/W | 0h | Channel 25 Source number. |
| 11-8 | WORD_LENGTH_CH24 | R/W | 0h | Channel 24 word length. |
| 7-4 | CHANNEL_NUM_CH24 | R/W | 0h | Channel 24 channel number. |
| 3-0 | SOURCE_NUM_CH24 | R/W | 0h | Channel 24 Source number. |

8.5.334 EDP_CORE_STTS_BIT_CH2627_P Register (Offset = 00030040h) [reset = 0h]

EDP_CORE_STTS_BIT_CH2627_P is shown in [Figure 8-390](#) and described in [Table 8-790](#).

Return to [Summary Table](#).

Channels 26,27 configuration

**Table 8-789. EDP_CORE_STTS_BIT_CH2627_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0040h |

Figure 8-390. EDP_CORE_STTS_BIT_CH2627_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS27_26 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH27 | | | | CHANNEL_NUM_CH27 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH27 | | | | WORD_LENGTH_CH26 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH26 | | | | SOURCE_NUM_CH26 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-790. EDP_CORE_STTS_BIT_CH2627_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS27_26 | R/W | 0h | Valid Bits for channel 27 and 26 if force is enabled |
| 23-20 | WORD_LENGTH_CH27 | R/W | 0h | Channel 27 word length. |
| 19-16 | CHANNEL_NUM_CH27 | R/W | 0h | Channel 27 channel number. |
| 15-12 | SOURCE_NUM_CH27 | R/W | 0h | Channel 27 Source number. |
| 11-8 | WORD_LENGTH_CH26 | R/W | 0h | Channel 26 word length. |
| 7-4 | CHANNEL_NUM_CH26 | R/W | 0h | Channel 26 channel number. |
| 3-0 | SOURCE_NUM_CH26 | R/W | 0h | Channel 26 Source number. |

8.5.335 EDP_CORE_STTS_BIT_CH2829_P Register (Offset = 00030044h) [reset = 0h]

EDP_CORE_STTS_BIT_CH2829_P is shown in [Figure 8-391](#) and described in [Table 8-792](#).

Return to [Summary Table](#).

Channels 28,29 configuration

Table 8-791. EDP_CORE_STTS_BIT_CH2829_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0044h |

Figure 8-391. EDP_CORE_STTS_BIT_CH2829_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS29_28 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH29 | | | | CHANNEL_NUM_CH29 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH29 | | | | WORD_LENGTH_CH28 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH28 | | | | SOURCE_NUM_CH28 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-792. EDP_CORE_STTS_BIT_CH2829_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS29_28 | R/W | 0h | Valid Bits for channel 29 and 28 if force is enabled |
| 23-20 | WORD_LENGTH_CH29 | R/W | 0h | Channel 29 word length. |
| 19-16 | CHANNEL_NUM_CH29 | R/W | 0h | Channel 29 channel number. |
| 15-12 | SOURCE_NUM_CH29 | R/W | 0h | Channel 29 Source number. |
| 11-8 | WORD_LENGTH_CH28 | R/W | 0h | Channel 28 word length. |
| 7-4 | CHANNEL_NUM_CH28 | R/W | 0h | Channel 28 channel number. |
| 3-0 | SOURCE_NUM_CH28 | R/W | 0h | Channel 28 Source number. |

8.5.336 EDP_CORE_STTS_BIT_CH3031_P Register (Offset = 00030048h) [reset = 0h]

EDP_CORE_STTS_BIT_CH3031_P is shown in [Figure 8-392](#) and described in [Table 8-794](#).

Return to [Summary Table](#).

Channels 30,31 configuration

**Table 8-793. EDP_CORE_STTS_BIT_CH3031_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0048h |

Figure 8-392. EDP_CORE_STTS_BIT_CH3031_P Register

| | | | | | | | |
|------------------|----|----|----|------------------|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | VALID_BITS31_30 | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WORD_LENGTH_CH31 | | | | CHANNEL_NUM_CH31 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SOURCE_NUM_CH31 | | | | WORD_LENGTH_CH30 | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHANNEL_NUM_CH30 | | | | SOURCE_NUM_CH30 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-794. EDP_CORE_STTS_BIT_CH3031_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-24 | VALID_BITS31_30 | R/W | 0h | Valid Bits for channel 31 and 30 if force is enabled |
| 23-20 | WORD_LENGTH_CH31 | R/W | 0h | Channel 31 word length. |
| 19-16 | CHANNEL_NUM_CH31 | R/W | 0h | Channel 31 channel number. |
| 15-12 | SOURCE_NUM_CH31 | R/W | 0h | Channel 31 Source number. |
| 11-8 | WORD_LENGTH_CH30 | R/W | 0h | Channel 30 word length. |
| 7-4 | CHANNEL_NUM_CH30 | R/W | 0h | Channel 30 channel number. |
| 3-0 | SOURCE_NUM_CH30 | R/W | 0h | Channel 30 Source number. |

8.5.337 EDP_CORE_SPDIF_CTRL_ADDR_P Register (Offset = 0003004Ch) [reset = 0h]

EDP_CORE_SPDIF_CTRL_ADDR_P is shown in [Figure 8-393](#) and described in [Table 8-796](#).

Return to [Summary Table](#).

SPDIF control

Table 8-795. EDP_CORE_SPDIF_CTRL_ADDR_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 004Ch |

Figure 8-393. EDP_CORE_SPDIF_CTRL_ADDR_P Register

| | | | | | | | |
|----------------------|----|------------------|-------------------|-------------------------|----------------------|---------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | SPDIF_JITTER_STATUS | |
| R-0h | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SPDIF_JITTER_STATUS | | SPDIF_ENABL E | SPDIF_AVG_S EL | SPDIF_JITTER _BYPASS | SPDIF_FIFO_MID_RANGE | | |
| R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SPDIF_FIFO_MID_RANGE | | | | | SPDIF_JITTER_THRSH | | |
| R/W-0h | | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_JITTER_THRSH | | | | | SPDIF_JITTER_AVG_WIN | | |
| R/W-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-796. EDP_CORE_SPDIF_CTRL_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-26 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 25-22 | SPDIF_JITTER_STATUS | R | 0h | SPDIF Jitter Status |
| 21 | SPDIF_ENABLE | R/W | 0h | SPDIF Enable |
| 20 | SPDIF_AVG_SEL | R/W | 0h | SPDIF average Select |
| 19 | SPDIF_JITTER_BYPASS | R/W | 0h | SPDIF Jitter Bypass |
| 18-11 | SPDIF_FIFO_MID_RANG E | R/W | 0h | SPDIF fifo mid range |
| 10-3 | SPDIF_JITTER_THRSH | R/W | 0h | SPDIF Jitter threshold |
| 2-0 | SPDIF_JITTER_AVG_WI N | R/W | 0h | Spdif Jitter AVG Window |

8.5.338 EDP_CORE_SPDIF_CH1_CS_3100_ADDR_P Register (Offset = 00030050h) [reset = 0h]

EDP_CORE_SPDIF_CH1_CS_3100_ADDR_P is shown in [Figure 8-394](#) and described in [Table 8-798](#).

Return to [Summary Table](#).

SPDIF channel 1 status [31:00]

Table 8-797.
EDP_CORE_SPDIF_CH1_CS_3100_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0050h |

Figure 8-394. EDP_CORE_SPDIF_CH1_CS_3100_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH1_ST_STTS_BITS3100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-798. EDP_CORE_SPDIF_CH1_CS_3100_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|-----------------------------------|
| 31-0 | SPDIF_CH1_ST_STTS_BITS3100 | R | 0h | SPDIF Channel 1 Status bits[31:0] |

8.5.339 EDP_CORE_SPDIF_CH1_CS_6332_ADDR_P Register (Offset = 00030054h) [reset = 0h]

EDP_CORE_SPDIF_CH1_CS_6332_ADDR_P is shown in [Figure 8-395](#) and described in [Table 8-800](#).

Return to [Summary Table](#).

SPDIF channel 1 status [63:32]

Table 8-799.
EDP_CORE_SPDIF_CH1_CS_6332_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0054h |

Figure 8-395. EDP_CORE_SPDIF_CH1_CS_6332_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH1_ST_STTS_BITS6332 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-800. EDP_CORE_SPDIF_CH1_CS_6332_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|------------------------------------|
| 31-0 | SPDIF_CH1_ST_STTS_BITS6332 | R | 0h | SPDIF Channel 1 Status bits[63:32] |

8.5.340 EDP_CORE_SPDIF_CH1_CS_9564_ADDR_P Register (Offset = 00030058h) [reset = 0h]

EDP_CORE_SPDIF_CH1_CS_9564_ADDR_P is shown in [Figure 8-396](#) and described in [Table 8-802](#).

Return to [Summary Table](#).

SPDIF channel 1 status [95:64]

Table 8-801.
EDP_CORE_SPDIF_CH1_CS_9564_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0058h |

Figure 8-396. EDP_CORE_SPDIF_CH1_CS_9564_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH1_ST_STTS_BITS9564 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-802. EDP_CORE_SPDIF_CH1_CS_9564_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|------------------------------------|
| 31-0 | SPDIF_CH1_ST_STTS_BITS9564 | R | 0h | SPDIF Channel 1 Status bits[95:64] |

8.5.341 EDP_CORE_SPDIF_CH1_CS_12796_ADDR_P Register (Offset = 0003005Ch) [reset = 0h]

EDP_CORE_SPDIF_CH1_CS_12796_ADDR_P is shown in [Figure 8-397](#) and described in [Table 8-804](#).

Return to [Summary Table](#).

SPDIF channel 1 status [127:96]

Table 8-803.
EDP_CORE_SPDIF_CH1_CS_12796_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 005Ch |

Figure 8-397. EDP_CORE_SPDIF_CH1_CS_12796_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH1_ST_STTS_BITS12796 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-804. EDP_CORE_SPDIF_CH1_CS_12796_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|-------------------------------------|
| 31-0 | SPDIF_CH1_ST_STTS_BITS12796 | R | 0h | SPDIF Channel 1 Status bits[127:96] |

8.5.342 EDP_CORE_SPDIF_CH1_CS_159128_ADDR_P Register (Offset = 00030060h) [reset = 0h]

EDP_CORE_SPDIF_CH1_CS_159128_ADDR_P is shown in [Figure 8-398](#) and described in [Table 8-806](#).

Return to [Summary Table](#).

SPDIF channel 1 status [159:128]

Table 8-805.
EDP_CORE_SPDIF_CH1_CS_159128_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0060h |

Figure 8-398. EDP_CORE_SPDIF_CH1_CS_159128_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH1_ST_STTS_BITS159128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-806. EDP_CORE_SPDIF_CH1_CS_159128_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|------|-------|--------------------------------------|
| 31-0 | SPDIF_CH1_ST_STTS_B ITS159128 | R | 0h | SPDIF Channel 1 Status bits[159:128] |

8.5.343 EDP_CORE_SPDIF_CH1_CS_191160_ADDR_P Register (Offset = 00030064h) [reset = 0h]

EDP_CORE_SPDIF_CH1_CS_191160_ADDR_P is shown in [Figure 8-399](#) and described in [Table 8-808](#).

Return to [Summary Table](#).

SPDIF channel 1 status [191:160]

Table 8-807.
EDP_CORE_SPDIF_CH1_CS_191160_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0064h |

Figure 8-399. EDP_CORE_SPDIF_CH1_CS_191160_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH1_ST_STTS_BITS191160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-808. EDP_CORE_SPDIF_CH1_CS_191160_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|------|-------|--------------------------------------|
| 31-0 | SPDIF_CH1_ST_STTS_BITS191160 | R | 0h | SPDIF Channel 1 Status bits[191:160] |

8.5.344 EDP_CORE_SPDIF_CH2_CS_3100_ADDR_P Register (Offset = 00030068h) [reset = 0h]

EDP_CORE_SPDIF_CH2_CS_3100_ADDR_P is shown in [Figure 8-400](#) and described in [Table 8-810](#).

Return to [Summary Table](#).

SPDIF channel 2 status [31:00]

Table 8-809.
EDP_CORE_SPDIF_CH2_CS_3100_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0068h |

Figure 8-400. EDP_CORE_SPDIF_CH2_CS_3100_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH2_ST_STTS_BITS3100 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-810. EDP_CORE_SPDIF_CH2_CS_3100_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|-----------------------------------|
| 31-0 | SPDIF_CH2_ST_STTS_BITS3100 | R | 0h | SPDIF Channel 2 Status bits[31:0] |

8.5.345 EDP_CORE_SPDIF_CH2_CS_6332_ADDR_P Register (Offset = 0003006Ch) [reset = 0h]

EDP_CORE_SPDIF_CH2_CS_6332_ADDR_P is shown in [Figure 8-401](#) and described in [Table 8-812](#).

Return to [Summary Table](#).

SPDIF channel 2 status [63:32]

Table 8-811.
EDP_CORE_SPDIF_CH2_CS_6332_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 006Ch |

Figure 8-401. EDP_CORE_SPDIF_CH2_CS_6332_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH2_ST_STTS_BITS6332 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-812. EDP_CORE_SPDIF_CH2_CS_6332_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|------------------------------------|
| 31-0 | SPDIF_CH2_ST_STTS_BITS6332 | R | 0h | SPDIF Channel 2 Status bits[63:32] |

8.5.346 EDP_CORE_SPDIF_CH2_CS_9564_ADDR_P Register (Offset = 00030070h) [reset = 0h]

EDP_CORE_SPDIF_CH2_CS_9564_ADDR_P is shown in [Figure 8-402](#) and described in [Table 8-814](#).

Return to [Summary Table](#).

SPDIF channel 2 status [95:64]

Table 8-813.
EDP_CORE_SPDIF_CH2_CS_9564_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0070h |

Figure 8-402. EDP_CORE_SPDIF_CH2_CS_9564_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH2_ST_STTS_BITS9564 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-814. EDP_CORE_SPDIF_CH2_CS_9564_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|------------------------------------|
| 31-0 | SPDIF_CH2_ST_STTS_BITS9564 | R | 0h | SPDIF Channel 2 Status bits[95:64] |

8.5.347 EDP_CORE_SPDIF_CH2_CS_12796_ADDR_P Register (Offset = 00030074h) [reset = 0h]

EDP_CORE_SPDIF_CH2_CS_12796_ADDR_P is shown in [Figure 8-403](#) and described in [Table 8-816](#).

Return to [Summary Table](#).

SPDIF channel 2 status [127:96]

Table 8-815.
EDP_CORE_SPDIF_CH2_CS_12796_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0074h |

Figure 8-403. EDP_CORE_SPDIF_CH2_CS_12796_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH2_ST_STTS_BITS12796 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-816. EDP_CORE_SPDIF_CH2_CS_12796_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|-------------------------------------|
| 31-0 | SPDIF_CH2_ST_STTS_BITS12796 | R | 0h | SPDIF Channel 2 Status bits[127:96] |

8.5.348 EDP_CORE_SPDIF_CH2_CS_159128_ADDR_P Register (Offset = 00030078h) [reset = 0h]

EDP_CORE_SPDIF_CH2_CS_159128_ADDR_P is shown in [Figure 8-404](#) and described in [Table 8-818](#).

Return to [Summary Table](#).

SPDIF channel 2 status [159:128]

Table 8-817.
EDP_CORE_SPDIF_CH2_CS_159128_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0078h |

Figure 8-404. EDP_CORE_SPDIF_CH2_CS_159128_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH2_ST_STTS_BITS159128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-818. EDP_CORE_SPDIF_CH2_CS_159128_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|------|-------|--------------------------------------|
| 31-0 | SPDIF_CH2_ST_STTS_B ITS159128 | R | 0h | SPDIF Channel 2 Status bits[159:128] |

8.5.349 EDP_CORE_SPDIF_CH2_CS_191160_ADDR_P Register (Offset = 0003007Ch) [reset = 0h]

EDP_CORE_SPDIF_CH2_CS_191160_ADDR_P is shown in [Figure 8-405](#) and described in [Table 8-820](#).

Return to [Summary Table](#).

SPDIF channel 2 status [191:160]

Table 8-819.
EDP_CORE_SPDIF_CH2_CS_191160_ADDR_P
Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 007Ch |

Figure 8-405. EDP_CORE_SPDIF_CH2_CS_191160_ADDR_P Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPDIF_CH2_ST_STTS_BITS191160 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-820. EDP_CORE_SPDIF_CH2_CS_191160_ADDR_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|------|-------|--------------------------------------|
| 31-0 | SPDIF_CH2_ST_STTS_BITS191160 | R | 0h | SPDIF Channel 2 Status bits[191:160] |

8.5.350 EDP_CORE_SMPL2PKT_CNTL_P Register (Offset = 00030080h) [reset = 0h]

EDP_CORE_SMPL2PKT_CNTL_P is shown in [Figure 8-406](#) and described in [Table 8-822](#).

Return to [Summary Table](#).

Sample 2 Packets Control Register

**Table 8-821. EDP_CORE_SMPL2PKT_CNTL_P
Instances**

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0080h |

Figure 8-406. EDP_CORE_SMPL2PKT_CNTL_P Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | SMPL2PKT_EN | SW_RST |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-822. EDP_CORE_SMPL2PKT_CNTL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 1 | SMPL2PKT_EN | R/W | 0h | When high Sample to Packets Block starts. |
| 0 | SW_RST | R/W | 0h | Software reset. Active high. |

8.5.351 EDP_CORE_SMPL2PKT_CNFG_P Register (Offset = 00030084h) [reset = 800h]

EDP_CORE_SMPL2PKT_CNFG_P is shown in [Figure 8-407](#) and described in [Table 8-824](#).

Return to [Summary Table](#).

Sample 2 Packets Config Register

Table 8-823. EDP_CORE_SMPL2PKT_CNFG_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0084h |

Figure 8-407. EDP_CORE_SMPL2PKT_CNFG_P Register

| | | | | | | | |
|----------------------------------|----------------------------------|------------------|----------------------------------|--------------------|------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | CFG_SAMPLE _PRESENT_FO RCE | CFG_SAMPLE_PRESENT | | | |
| R-0h | | | R/W-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CFG_EN_AUT O_SUB_PCKT_ NUM | CFG_BLOCK_L PCM_FIRST_P KT | CFG_SUB_PCKT_NUM | | | AUDIO_TYPE | | |
| R/W-0h | R/W-0h | R/W-1h | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUDIO_TYPE | NUM_OF_I2S_PORTS | | MAX_NUM_CH | | | | |
| R/W-0h | R/W-0h | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-824. EDP_CORE_SMPL2PKT_CNFG_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-21 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 20 | CFG_SAMPLE_PRESEN T_FORCE | R/W | 0h | Force sample present bits |
| 19-16 | CFG_SAMPLE_PRESEN T | R/W | 0h | Sample present bits if force them is active |
| 15 | CFG_EN_AUTO_SUB_P CKT_NUM | R/W | 0h | Enable automatics sub packet number. When enabled number of sub-packets will be set according to MEM FIFO number of samples. |
| 14 | CFG_BLOCK_LPCM_FIR ST_PKT | R/W | 0h | 0 - All packets behave the same. 1- First lpcm audio packet is sent with 1 - SP. |

Table 8-824. EDP_CORE_SMPL2PKT_CNFG_P Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 13-11 | CFG_SUB_PCKT_NUM | R/W | 1h | Number of sub-packets in HDMI audio 2-ch packet. 00: 1-SP 01: 2-SP 10: 3-SP 11: 4-SP. 100- 111: NA. |
| 10-7 | AUDIO_TYPE | R/W | 0h | Audio Type setting. Packet is structured according to audio type. |
| 6-5 | NUM_OF_I2S_PORTS | R/W | 0h | Number of active I2S ports. 00- 1 port 01-2 ports 11- 4 ports 11 -NA. |
| 4-0 | MAX_NUM_CH | R/W | 0h | Number of channels to decode. 0: 1 channel 31: 32 channels |

8.5.352 EDP_CORE_FIFO_CNTL_P Register (Offset = 00030088h) [reset = 0h]

EDP_CORE_FIFO_CNTL_P is shown in [Figure 8-408](#) and described in [Table 8-826](#).

Return to [Summary Table](#).

FIFO control register

Table 8-825. EDP_CORE_FIFO_CNTL_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0088h |

Figure 8-408. EDP_CORE_FIFO_CNTL_P Register

| | | | | | | | |
|----------|----|----|-------------------|---------------------|----------|------------------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CFG_DIS_POR T3 | FIFO_EMPTY_ CALC | FIFO_DIR | SYNC_WR_TO _CH_ZERO | FIFO_SW_RST |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-826. EDP_CORE_FIFO_CNTL_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|--|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 4 | CFG_DIS_PORT3 | R/W | 0h | 0 - Normal Operation. 1 - I2S port 3 is disabled [user should ignore its outputs]. This allows for 24-ch, 12-ch, 6-ch transfer. |
| 3 | FIFO_EMPTY_CALC | R/W | 0h | 0 - Empty is a function of read address. 1 - Empty is a function of BASE read address. |
| 2 | FIFO_DIR | R/W | 0h | 0 - smpl2pkt [inc_step=number of I2S ports] 1 - pkt2smpl [inc_step=num_ch_per_port] |
| 1 | SYNC_WR_TO_CH_ZERO | R/W | 0h | When high the last channel index synchronizes the write addresses [to the next channel group] |
| 0 | FIFO_SW_RST | R/W | 0h | Resets Fifo's write and read pointers. When FIFO configuration bits change this signal should be high [due to synchronization issues]. |

8.5.353 EDP_CORE_FIFO_STTS_P Register (Offset = 0003008Ch) [reset = 0h]

EDP_CORE_FIFO_STTS_P is shown in [Figure 8-409](#) and described in [Table 8-828](#).

[Return to Summary Table.](#)

FIFO Status register

Table 8-827. EDP_CORE_FIFO_STTS_P Instances

| Instance | Physical Address |
|-----------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 008Ch |

Figure 8-409. EDP_CORE_FIFO_STTS_P Register

| | | | | | | | |
|----------|----|----|----|----------|---------|-------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | UNDERRUN | OVERRUN | EMPTY | WFULL |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-828. EDP_CORE_FIFO_STTS_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 3 | UNDERRUN | R | 0h | Indicates a FIFO underrun error has occurred - FIFO read when it was empty. For debug purposes, not synchronized. |
| 2 | OVERRUN | R | 0h | Indicates a FIFO overrun error has occurred - FIFO written to when it was full. For debug purposes, not synchronized. |
| 1 | EMPTY | R | 0h | Indicates FIFO Empty. For debug purposes, not synchronized. |
| 0 | WFULL | R | 0h | Indicates FIFO Full. For debug purposes, not synchronized. |

8.5.354 EDP_CORE_SUB_PCKT_THRSH_P Register (Offset = 00030090h) [reset = 00302010h]

EDP_CORE_SUB_PCKT_THRSH_P is shown in [Figure 8-410](#) and described in [Table 8-830](#).

Return to [Summary Table](#).

SUB Packet Threshold register

Table 8-829. EDP_CORE_SUB_PCKT_THRSH_P Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0090h |

Figure 8-410. EDP_CORE_SUB_PCKT_THRSH_P Register

| | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | CFG_MEM_FIFO_THRSH3 | | | | | | | |
| R-0h | | | | | | | | R/W-30h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CFG_MEM_FIFO_THRSH2 | | | | | | | | CFG_MEM_FIFO_THRSH1 | | | | | | | |
| R/W-20h | | | | | | | | R/W-10h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-830. EDP_CORE_SUB_PCKT_THRSH_P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-24 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 23-16 | CFG_MEM_FIFO_THRSH 3 | R/W | 30h | If number of samples in MEM FIFO is below Threshold 3: Each Packet will contain only 3 subpacket. |
| 15-8 | CFG_MEM_FIFO_THRSH 2 | R/W | 20h | If number of samples in MEM FIFO is below Threshold 2: Each Packet will contain only 2 subpacket. |
| 7-0 | CFG_MEM_FIFO_THRSH 1 | R/W | 10h | If number of samples in MEM FIFO is below Threshold 1: Each Packet will contain only 1 subpacket. |

8.5.355 EDP_CORE_SOURCE_PIF_WR_ADDR_P_j Register (Offset = 00030800h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_WR_ADDR_P_j is shown in [Figure 8-411](#) and described in [Table 8-832](#).

Return to [Summary Table](#).

4 MSB of the packet memory address in which the data is written.

Offset = 00030800h + (j * 40h); where j = 0h to 3h

Table 8-831.
EDP_CORE_SOURCE_PIF_WR_ADDR_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0800h + formula |

Figure 8-411. EDP_CORE_SOURCE_PIF_WR_ADDR_P_j Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | WR_ADDR | | | |
| R-0h | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-832. EDP_CORE_SOURCE_PIF_WR_ADDR_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 3-0 | WR_ADDR | R/W | 0h | 4 MSB of the packet memory address in which the data is written. |

8.5.356 EDP_CORE_SOURCE_PIF_WR_REQ_P_j Register (Offset = 00030804h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_WR_REQ_P_j is shown in [Figure 8-412](#) and described in [Table 8-834](#).

Return to [Summary Table](#).

Write request bit for the host write transaction.

Offset = 00030804h + (j * 40h); where j = 0h to 3h

Table 8-833.
EDP_CORE_SOURCE_PIF_WR_REQ_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0804h + formula |

Figure 8-412. EDP_CORE_SOURCE_PIF_WR_REQ_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | HOST_WR |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-834. EDP_CORE_SOURCE_PIF_WR_REQ_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | HOST_WR | R/W | 0h | Write request bit for the host write transaction, active high. Bit is automatically cleared when operation is completed. |

8.5.357 EDP_CORE_SOURCE_PIF_RD_ADDR_P_j Register (Offset = 00030808h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_RD_ADDR_P_j is shown in [Figure 8-413](#) and described in [Table 8-836](#).

Return to [Summary Table](#).

4 MSB of the packet memory address from which the data is read.

Offset = 00030808h + (j * 40h); where j = 0h to 3h

Table 8-835.
EDP_CORE_SOURCE_PIF_RD_ADDR_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0808h + formula |

Figure 8-413. EDP_CORE_SOURCE_PIF_RD_ADDR_P_j Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | RD_ADDR | | | |
| R-0h | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-836. EDP_CORE_SOURCE_PIF_RD_ADDR_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 3-0 | RD_ADDR | R/W | 0h | 4 MSB of the packet memory address from which the data is read. |

8.5.358 EDP_CORE_SOURCE_PIF_RD_REQ_P_j Register (Offset = 0003080Ch + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_RD_REQ_P_j is shown in [Figure 8-414](#) and described in [Table 8-838](#).

Return to [Summary Table](#).

Read request bit for the host read transaction.

Offset = 0003080Ch + (j * 40h); where j = 0h to 3h

Table 8-837.
EDP_CORE_SOURCE_PIF_RD_REQ_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 080Ch + formula |

Figure 8-414. EDP_CORE_SOURCE_PIF_RD_REQ_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | HOST_RD |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-838. EDP_CORE_SOURCE_PIF_RD_REQ_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | HOST_RD | R/W | 0h | Read request bit for the host read transaction, active high. Bit is automatically cleared when operation is completed. |

8.5.359 EDP_CORE_SOURCE_PIF_DATA_WR_P_j Register (Offset = 00030810h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_DATA_WR_P_j is shown in [Figure 8-415](#) and described in [Table 8-840](#).

Return to [Summary Table](#).

The 32 bits of the data to be written to the packet memory.

Offset = 00030810h + (j * 40h); where j = 0h to 3h

Table 8-839.
EDP_CORE_SOURCE_PIF_DATA_WR_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0810h + formula |

Figure 8-415. EDP_CORE_SOURCE_PIF_DATA_WR_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA_WR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-840. EDP_CORE_SOURCE_PIF_DATA_WR_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---|
| 31-0 | DATA_WR | R/W | 0h | The 32 bits of the data to be written to the packet memory. When written to this register fifo1_wr_enable will automatically be asserted and the data is stored in FIFO. |

8.5.360 EDP_CORE_SOURCE_PIF_DATA_RD_P_j Register (Offset = 00030814h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_DATA_RD_P_j is shown in [Figure 8-416](#) and described in [Table 8-842](#).

Return to [Summary Table](#).

The 32 bits of the data to be read from the packet memory.

Offset = 00030814h + (j * 40h); where j = 0h to 3h

Table 8-841.
EDP_CORE_SOURCE_PIF_DATA_RD_P_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0814h + formula |

Figure 8-416. EDP_CORE_SOURCE_PIF_DATA_RD_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIFO2_DATA_OUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-842. EDP_CORE_SOURCE_PIF_DATA_RD_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-0 | FIFO2_DATA_OUT | R | 0h | The 32 bits of the data to be read from the packet memory. When read from this register fifo2_rd_enable will automatically be asserted and the data is read from the FIFO. |

8.5.361 EDP_CORE_SOURCE_PIF_FIFO1_FLUSH_P_j Register (Offset = 00030818h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_FIFO1_FLUSH_P_j is shown in [Figure 8-417](#) and described in [Table 8-844](#).

Return to [Summary Table](#).

Fifo1 flush

Offset = 00030818h + (j * 40h); where j = 0h to 3h

Table 8-843.
EDP_CORE_SOURCE_PIF_FIFO1_FLUSH_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0818h + formula |

Figure 8-417. EDP_CORE_SOURCE_PIF_FIFO1_FLUSH_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | FIFO1_FLUSH |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-844. EDP_CORE_SOURCE_PIF_FIFO1_FLUSH_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | FIFO1_FLUSH | R/W | 0h | Fifo1 flush bit, active high. Bit is automatically cleared when operation is completed. |

8.5.362 EDP_CORE_SOURCE_PIF_FIFO2_FLUSH_P_j Register (Offset = 0003081Ch + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_FIFO2_FLUSH_P_j is shown in [Figure 8-418](#) and described in [Table 8-846](#).

Return to [Summary Table](#).

Fifo2 flush

Offset = 0003081Ch + (j * 40h); where j = 0h to 3h

Table 8-845.
EDP_CORE_SOURCE_PIF_FIFO2_FLUSH_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 081Ch + formula |

Figure 8-418. EDP_CORE_SOURCE_PIF_FIFO2_FLUSH_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | FIFO2_FLUSH |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-846. EDP_CORE_SOURCE_PIF_FIFO2_FLUSH_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | FIFO2_FLUSH | R/W | 0h | Fifo2 flush bit, active high. Bit is automatically cleared when operation is completed. |

8.5.363 EDP_CORE_SOURCE_PIF_STATUS_P_j Register (Offset = 00030820h + formula) [reset = 10h]

EDP_CORE_SOURCE_PIF_STATUS_P_j is shown in [Figure 8-419](#) and described in [Table 8-848](#).

Return to [Summary Table](#).

Status bits for the PIF module

Offset = 00030820h + (j * 40h); where j = 0h to 3h

**Table 8-847. EDP_CORE_SOURCE_PIF_STATUS_P_j
Instances**

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0820h + formula |

Figure 8-419. EDP_CORE_SOURCE_PIF_STATUS_P_j Register

| | | | | | | | |
|----------|----|----|-------------|------------|-------------------------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | FIFO2_EMPTY | FIFO1_FULL | SOURCE_PKT_MEM_CTRL_FSM_STATE | | |
| R-0h | | | R-1h | R-0h | R-0h | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-848. EDP_CORE_SOURCE_PIF_STATUS_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|---|
| 31-5 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 4 | FIFO2_EMPTY | R | 1h | Fifo2 empty indication, when high indicates that FIFO2 is empty |
| 3 | FIFO1_FULL | R | 0h | Fifo1 full indication, when high indicates that FIFO1 is full |
| 2-0 | SOURCE_PKT_MEM_CTRL_FSM_STATE | R | 0h | State of the FSM that controls packet memory transactions. |

8.5.364 EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P_J Register (Offset = 00030824h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P_J is shown in [Figure 8-420](#) and described in [Table 8-850](#).

Return to [Summary Table](#).

Interrupt sources of the PIF module, active high. Automatically cleared on read. If any of this interrupt is enabled and triggered bit apb_pif_intr_status in APB_INT_STATUS register is set.

Offset = 00030824h + (j * 40h); where j = 0h to 3h

Table 8-849.
EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P
_J Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0824h + formula |

Figure 8-420. EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P_J Register

| | | | | | | | |
|-----------------|----------------|----------------|---------------|----------|-------------------------------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | PPS_SENT | FIFO2_UNDERFLOW | FIFO2_OVERFLOW |
| R-0h | | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIFO1_UNDERFLOW | FIFO1_OVERFLOW | ALLOC_WR_ERROR | ALLOC_WR_DONE | RESERVED | NONVALID_TY PE_REQUEST ED_INT | HOST_RD_DONE_INT | HOST_WR_DONE_INT |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-850. EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-11 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 10 | PPS_SENT | R | 0h | PPS sent to framer indication. Active HIGH. Clear on read. |
| 9 | FIFO2_UNDERFLOW | R | 0h | Fifo2 underflow indication. Indicates incorrect programming sequence. Active HIGH. Clear on read. |
| 8 | FIFO2_OVERFLOW | R | 0h | Fifo2 overflow indication. Indicates incorrect programming sequence. Active HIGH. Clear on read. |

**Table 8-850. EDP_CORE_SOURCE_PIF_INTERRUPT_SOURCE_P_J Register Field Descriptions
(continued)**

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 7 | FIFO1_UNDERFLOW | R | 0h | Fifo1 underflow indication. Indicates incorrect programming sequence. Active HIGH. Clear on read. |
| 6 | FIFO1_OVERFLOW | R | 0h | Fifo1 overflow indication. Indicates incorrect programming sequence. Active HIGH. Clear on read. |
| 5 | ALLOC_WR_ERROR | R | 0h | Error happened, invalid write to the allocation table. Indicates incorrect programming sequence. Active HIGH. Clear on read. |
| 4 | ALLOC_WR_DONE | R | 0h | Successful write to the allocation table. Active HIGH. Clear on read. |
| 3 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 2 | NONVALID_TYPE_REQUESTED_INT | R | 0h | Indication that nonvalid type of packet is requested by the packet interface. Indicates incorrect programming sequence. Active HIGH. Clear on read. |
| 1 | HOST_RD_DONE_INT | R | 0h | Indication that the host read transaction finished. Active HIGH. Clear on read. |
| 0 | HOST_WR_DONE_INT | R | 0h | Indication that the host write transaction finished. Active HIGH. Clear on read. |

8.5.365 EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_J Register (Offset = 00030828h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_J is shown in [Figure 8-421](#) and described in [Table 8-852](#).

Return to [Summary Table](#).

Masks for the interrupt sources in the SOURCE_PIF_INTERRUPT_SOURCE register, when set high, these bits disable the corresponding interrupts

Offset = 00030828h + (j * 40h); where j = 0h to 3h

Table 8-851.
EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_J
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0828h + formula |

Figure 8-421. EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_J Register

| | | | | | | | |
|--------------------------|-------------------------|-------------------------|------------------------|----------|--|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | PPS_SENT_M ASK | FIFO2_UNDER FLOW_MASK | FIFO2_OVERF LOW_MASK |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FIFO1_UNDER FLOW_MASK | FIFO1_OVERF LOW_MASK | ALLOC_WR_E RROR_MASK | ALLOC_WR_D ONE_MASK | RESERVED | NONVALID_TY PE_REQUEST ED_INT_MASK | HOST_RD_DO NE_INT_MASK | HOST_WR_DO NE_INT_MASK |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-852. EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-11 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 10 | PPS_SENT_MASK | R/W | 0h | Masks the pps_sent interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 9 | FIFO2_UNDERFLOW_MA SK | R/W | 0h | Masks the fifo2_underflow interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |

Table 8-852. EDP_CORE_SOURCE_PIF_INTERRUPT_MASK_P_J Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|---|
| 8 | FIFO2_OVERFLOW_MASK | R/W | 0h | Masks the fifo2_overflow interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 7 | FIFO1_UNDERFLOW_MASK | R/W | 0h | Masks the fifo1_underflow interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 6 | FIFO1_OVERFLOW_MASK | R/W | 0h | Masks the fifo1_overflow interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 5 | ALLOC_WR_ERROR_MASK | R/W | 0h | Masks the alloc_wr_error interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 4 | ALLOC_WR_DONE_MASK | R/W | 0h | Masks the alloc_wr_done interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 3 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 2 | NONVALID_TYPE_REQUESTED_INT_MASK | R/W | 0h | Masks the nonvalid_type_requested_int interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 1 | HOST_RD_DONE_INT_MASK | R/W | 0h | Masks the host_rd_done_int interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 0 | HOST_WR_DONE_INT_MASK | R/W | 0h | Masks the host_wr_done_int interrupt. 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.5.366 EDP_CORE_SOURCE_PIF_PKT_ALLOC_REG_P_j Register (Offset = 0003082Ch + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_PKT_ALLOC_REG_P_j is shown in [Figure 8-422](#) and described in [Table 8-854](#).

Return to [Summary Table](#).

Packet configuration to be stored in the allocation table

Offset = 0003082Ch + (j * 40h); where j = 0h to 3h

Table 8-853.
EDP_CORE_SOURCE_PIF_PKT_ALLOC_REG_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 082Ch + formula |

Figure 8-422. EDP_CORE_SOURCE_PIF_PKT_ALLOC_REG_P_j Register

| | | | | | | | |
|-------------|----|----|----|-------------------|----|-------------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | ACTIVE_IDLE_ TYPE | TYPE_VALID |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PACKET_TYPE | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | PKT_ALLOC_ADDRESS | | | |
| R-0h | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-854. EDP_CORE_SOURCE_PIF_PKT_ALLOC_REG_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31-18 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 17 | ACTIVE_IDLE_TYPE | R/W | 0h | Indicates in which mode the SDP will be sent. 0- no_video mode, 1- video mode |
| 16 | TYPE_VALID | R/W | 0h | 1 for valid, 0 for nonvalid |
| 15-8 | PACKET_TYPE | R/W | 0h | 8-bit value of the packet type |
| 7-4 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 3-0 | PKT_ALLOC_ADDRESS | R/W | 0h | Address of the register in the source allocation table |

8.5.367 EDP_CORE_SOURCE_PIF_PKT_ALLOC_WR_EN_P_j Register (Offset = 00030830h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_PKT_ALLOC_WR_EN_P_j is shown in [Figure 8-423](#) and described in [Table 8-856](#).

Return to [Summary Table](#).

Enable bit for writing to the allocation table

Offset = 00030830h + (j * 40h); where j = 0h to 3h

Table 8-855.
EDP_CORE_SOURCE_PIF_PKT_ALLOC_WR_EN_P
_j Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0830h + formula |

Figure 8-423. EDP_CORE_SOURCE_PIF_PKT_ALLOC_WR_EN_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PKT_ALLOC_ |
| | | | | | | | WR_EN |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-856. EDP_CORE_SOURCE_PIF_PKT_ALLOC_WR_EN_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | PKT_ALLOC_WR_EN | R/W | 0h | Enable bit for writing to the allocation table, active high |

8.5.368 EDP_CORE_SOURCE_PIF_SW_RESET_P_j Register (Offset = 00030834h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_SW_RESET_P_j is shown in [Figure 8-424](#) and described in [Table 8-858](#).

Return to [Summary Table](#).

Software reset.

Offset = 00030834h + (j * 40h); where j = 0h to 3h

Table 8-857.
EDP_CORE_SOURCE_PIF_SW_RESET_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0834h + formula |

Figure 8-424. EDP_CORE_SOURCE_PIF_SW_RESET_P_j Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | SW_RST |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-858. EDP_CORE_SOURCE_PIF_SW_RESET_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | SW_RST | R/W | 0h | Software reset, active high. Bit is automatically cleared when operation is completed. |

8.5.369 EDP_CORE_SOURCE_PIF_PPS_HEADER_P_j Register (Offset = 00030838h + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_PPS_HEADER_P_j is shown in [Figure 8-425](#) and described in [Table 8-860](#).

Return to [Summary Table](#).

PPS header

Offset = 00030838h + (j * 40h); where j = 0h to 3h

Table 8-859.
EDP_CORE_SOURCE_PIF_PPS_HEADER_P_j
Instances

| Instance | Physical Address |
|-----------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 0838h + formula |

Figure 8-425. EDP_CORE_SOURCE_PIF_PPS_HEADER_P_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPS_HEADER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 8-860. EDP_CORE_SOURCE_PIF_PPS_HEADER_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---------------------------------------|
| 31-0 | PPS_HEADER | R/W | 0h | value of the PPS header as per DPv1.4 |

8.5.370 EDP_CORE_SOURCE_PIF_PPS_P_j Register (Offset = 0003083Ch + formula) [reset = 0h]

EDP_CORE_SOURCE_PIF_PPS_P_j is shown in [Figure 8-426](#) and described in [Table 8-862](#).

Return to [Summary Table](#).

PPS SDP indication

Offset = 0003083Ch + (j * 40h); where j = 0h to 3h

Table 8-861. EDP_CORE_SOURCE_PIF_PPS_P_j Instances

| Instance | Physical Address |
|--------------------------------|----------------------|
| DSS_EDP0_V2A_CORE_VP_REGS_A PB | 0A03 083Ch + formula |

Figure 8-426. EDP_CORE_SOURCE_PIF_PPS_P_j Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | PPS |
| R-0h | | | | | | | | | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-862. EDP_CORE_SOURCE_PIF_PPS_P_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved. Writes are ignored. 0x0 when read |
| 0 | PPS | R/W | 0h | PPS SDP indication, active high. When set, the SDP to be read/written from/to the memory by the host is in fact PPS. Bit is automatically cleared when operation is completed. |

8.6 EDP_CORE_SAPB Registers

Table 8-864 lists the memory-mapped registers for the EDP_CORE_SAPB. All register offset addresses not listed in Table 8-864 should be considered as reserved locations and the register contents should not be modified.

MMR registers for eDP Core SAPB domain

Table 8-863. EDP_CORE_SAPB Instances

| Instance | Base Address |
|----------------------------------|--------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8000h |

Table 8-864. EDP_CORE_SAPB Registers

| Offset | Acronym | Register Name | DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB Physical Address |
|--------|---|---------------|--|
| 0h | EDP_CORE_APB_CTRL_S | | 04F4 8000h |
| 4h | EDP_CORE_XT_INT_CTRL_S | | 04F4 8004h |
| 8h | EDP_CORE_MAILBOX_FULL_ADDR_S | | 04F4 8008h |
| Ch | EDP_CORE_MAILBOX_EMPTY_ADDR_S | | 04F4 800Ch |
| 10h | EDP_CORE_MAILBOX0_WR_DATA_S | | 04F4 8010h |
| 14h | EDP_CORE_MAILBOX0_RD_DATA_S | | 04F4 8014h |
| 18h | EDP_CORE_KEEP_ALIVE_S | | 04F4 8018h |
| 1Ch | EDP_CORE_VER_I_S | | 04F4 801Ch |
| 20h | EDP_CORE_VER_H_S | | 04F4 8020h |
| 24h | EDP_CORE_VER_LIB_L_ADDR_S | | 04F4 8024h |
| 28h | EDP_CORE_VER_LIB_H_ADDR_S | | 04F4 8028h |
| 2Ch | EDP_CORE_SW_DEBUG_I_S | | 04F4 802Ch |
| 30h | EDP_CORE_SW_DEBUG_H_S | | 04F4 8030h |
| 34h | EDP_CORE_MAILBOX_INT_MASK_S | | 04F4 8034h |
| 38h | EDP_CORE_MAILBOX_INT_STATUS_S | | 04F4 8038h |
| 3Ch | EDP_CORE_SW_CLK_I_S | | 04F4 803Ch |
| 40h | EDP_CORE_SW_CLK_H_S | | 04F4 8040h |
| 44h | EDP_CORE_SW_EVENTS0_S | | 04F4 8044h |
| 48h | EDP_CORE_SW_EVENTS1_S | | 04F4 8048h |
| 4Ch | EDP_CORE_SW_EVENTS2_S | | 04F4 804Ch |
| 50h | EDP_CORE_SW_EVENTS3_S | | 04F4 8050h |
| 60h | EDP_CORE_XT_OCD_CTRL_S | | 04F4 8060h |
| 64h | EDP_CORE_XT_OCD_CTRL_RO_S | | 04F4 8064h |
| 6Ch | EDP_CORE_APB_INT_MASK_S | | 04F4 806Ch |
| 70h | EDP_CORE_APB_STATUS_S | | 04F4 8070h |

8.6.1 EDP_CORE_APB_CTRL_S Register (Offset = 0h) [reset = Fh]

EDP_CORE_APB_CTRL_S is shown in [Figure 8-427](#) and described in [Table 8-866](#).

Return to [Summary Table](#).

APB control register (SAPB)

Table 8-865. EDP_CORE_APB_CTRL_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8000h |

Figure 8-427. EDP_CORE_APB_CTRL_S Register

| | | | | | | | |
|----------|----|----|----|---------------------|-------------------|-------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | APB_XT_RUNS TALL | APB_IRAM_PA TH | APB_DRAM_P ATH | APB_XT_RESE T |
| R-0h | | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-866. EDP_CORE_APB_CTRL_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-4 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 3 | APB_XT_RUNSTALL | R/W | 1h | Not used |
| 2 | APB_IRAM_PATH | R/W | 1h | Not used |
| 1 | APB_DRAM_PATH | R/W | 1h | Not used |
| 0 | APB_XT_RESET | R/W | 1h | Not used |

8.6.2 EDP_CORE_XT_INT_CTRL_S Register (Offset = 4h) [reset = 0h]

EDP_CORE_XT_INT_CTRL_S is shown in [Figure 8-428](#) and described in [Table 8-868](#).

Return to [Summary Table](#).

Internal CPU Interrupt Polarity Control Register.

Table 8-867. EDP_CORE_XT_INT_CTRL_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8004h |

Figure 8-428. EDP_CORE_XT_INT_CTRL_S Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | XT_INT_POLARITY | |
| R-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-868. EDP_CORE_XT_INT_CTRL_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1-0 | XT_INT_POLARITY | R/W | 0h | Not used |

8.6.3 EDP_CORE_MAILBOX_FULL_ADDR_S Register (Offset = 8h) [reset = 0h]

EDP_CORE_MAILBOX_FULL_ADDR_S is shown in [Figure 8-429](#) and described in [Table 8-870](#).

Return to [Summary Table](#).

Mailbox full indication status register. This register provides a status of the mailbox that is used to send messages from the Host processor to internal uCPU. Mailbox full flag can be a source of mailbox interrupt.

Table 8-869. EDP_CORE_MAILBOX_FULL_ADDR_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8008h |

Figure 8-429. EDP_CORE_MAILBOX_FULL_ADDR_S Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | MAILBOX_FULL |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-870. EDP_CORE_MAILBOX_FULL_ADDR_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-1 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 0 | MAILBOX_FULL | R | 0h | Mailbox full indication. 0x 1-mailbox full. No more messages can be sent to mailbox 0x 0-mailbox not-full. At least 1 write can be performed to mailbox |

8.6.4 EDP_CORE_MAILBOX_EMPTY_ADDR_S Register (Offset = Ch) [reset = 1h]

EDP_CORE_MAILBOX_EMPTY_ADDR_S is shown in [Figure 8-430](#) and described in [Table 8-872](#).

Return to [Summary Table](#).

Mailbox empty indication status register. This register provides a status of the mailbox that is used to send responses from the internal uCPU to host processor as a result of previously sent message. Mailbox empty flag can be a source of not-empty mailbox interrupt.

Table 8-871.
EDP_CORE_MAILBOX_EMPTY_ADDR_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 800Ch |

Figure 8-430. EDP_CORE_MAILBOX_EMPTY_ADDR_S Register

| | | | | | | | |
|----------|----|----|----|----|----|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | MAILBOX_EMPTY |
| R-0h | | | | | | | R-1h |

LEGEND: R = Read Only; -n = value after reset

Table 8-872. EDP_CORE_MAILBOX_EMPTY_ADDR_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 0 | MAILBOX_EMPTY | R | 1h | Mailbox Empty indication 0x 1-mailbox empty. No response available 0x 0-mailbox not-empty. There is at least 1 byte of a response in mailbox available to read by Host processor |

8.6.5 EDP_CORE_MAILBOX0_WR_DATA_S Register (Offset = 10h) [reset = 0h]

EDP_CORE_MAILBOX0_WR_DATA_S is shown in [Figure 8-431](#) and described in [Table 8-874](#).

Return to [Summary Table](#).

Mailbox write data register

Table 8-873. EDP_CORE_MAILBOX0_WR_DATA_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8010h |

Figure 8-431. EDP_CORE_MAILBOX0_WR_DATA_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | MAILBOX0_WR_DATA | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-874. EDP_CORE_MAILBOX0_WR_DATA_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | MAILBOX0_WR_DATA | R/W | 0h | Mailbox write Data. |

8.6.6 EDP_CORE_MAILBOX0_RD_DATA_S Register (Offset = 14h) [reset = 0h]

EDP_CORE_MAILBOX0_RD_DATA_S is shown in [Figure 8-432](#) and described in [Table 8-876](#).

Return to [Summary Table](#).

Mailbox Read data register

**Table 8-875. EDP_CORE_MAILBOX0_RD_DATA_S
Instances**

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8014h |

Figure 8-432. EDP_CORE_MAILBOX0_RD_DATA_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | MAILBOX0_RD_DATA | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-876. EDP_CORE_MAILBOX0_RD_DATA_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | MAILBOX0_RD_DATA | R | 0h | Mailbox Read data |

8.6.7 EDP_CORE_KEEP_ALIVE_S Register (Offset = 18h) [reset = 0h]

EDP_CORE_KEEP_ALIVE_S is shown in [Figure 8-433](#) and described in [Table 8-878](#).

Return to [Summary Table](#).

Software keep alive counter

Table 8-877. EDP_CORE_KEEP_ALIVE_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8018h |

Figure 8-433. EDP_CORE_KEEP_ALIVE_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | KEEP_ALIVE_CNT | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-878. EDP_CORE_KEEP_ALIVE_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | KEEP_ALIVE_CNT | R | 0h | Software keep alive counter. Counter is initialized to 0x0 after reset and incremented by 0x1 with every FW kernel loop. It can be used to determine if internal CPU started running correctly. |

8.6.8 EDP_CORE_VER_I_S Register (Offset = 1Ch) [reset = 0h]

EDP_CORE_VER_I_S is shown in [Figure 8-434](#) and described in [Table 8-880](#).

[Return to Summary Table.](#)

Software Version Register.

Table 8-879. EDP_CORE_VER_I_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 801Ch |

Figure 8-434. EDP_CORE_VER_I_S Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | VER_LSB | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-880. EDP_CORE_VER_I_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | VER_LSB | R | 0h | Software Version lower byte. Loaded by Firmware at the beginning of firmware operation. |

8.6.9 EDP_CORE_VER_H_S Register (Offset = 20h) [reset = 0h]

EDP_CORE_VER_H_S is shown in [Figure 8-435](#) and described in [Table 8-882](#).

Return to [Summary Table](#).

Software Version Register.

Table 8-881. EDP_CORE_VER_H_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8020h |

Figure 8-435. EDP_CORE_VER_H_S Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | VER_MSB | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-882. EDP_CORE_VER_H_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | VER_MSB | R | 0h | Software Version higher byte. Loaded by Firmware at the beginning of firmware operation. |

8.6.10 EDP_CORE_VER_LIB_L_ADDR_S Register (Offset = 24h) [reset = 0h]

EDP_CORE_VER_LIB_L_ADDR_S is shown in [Figure 8-436](#) and described in [Table 8-884](#).

Return to [Summary Table](#).

Software Library Version Register.

**Table 8-883. EDP_CORE_VER_LIB_L_ADDR_S
Instances**

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8024h |

Figure 8-436. EDP_CORE_VER_LIB_L_ADDR_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_LIB_VER_L | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-884. EDP_CORE_VER_LIB_L_ADDR_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_LIB_VER_L | R | 0h | Software Library Version lower byte. Loaded by Firmware at the beginning of firmware operation. |

8.6.11 EDP_CORE_VER_LIB_H_ADDR_S Register (Offset = 28h) [reset = 0h]

EDP_CORE_VER_LIB_H_ADDR_S is shown in [Figure 8-437](#) and described in [Table 8-886](#).

Return to [Summary Table](#).

Software Library Version Register.

Table 8-885. EDP_CORE_VER_LIB_H_ADDR_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8028h |

Figure 8-437. EDP_CORE_VER_LIB_H_ADDR_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_LIB_VER_H | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-886. EDP_CORE_VER_LIB_H_ADDR_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_LIB_VER_H | R | 0h | Software Library Version higher byte. Loaded by Firmware at the beginning of firmware operation. |

8.6.12 EDP_CORE_SW_DEBUG_I_S Register (Offset = 2Ch) [reset = 0h]

EDP_CORE_SW_DEBUG_I_S is shown in [Figure 8-438](#) and described in [Table 8-888](#).

Return to [Summary Table](#).

Software/Firmware Debug Register.

Table 8-887. EDP_CORE_SW_DEBUG_I_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 802Ch |

Figure 8-438. EDP_CORE_SW_DEBUG_I_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_DEBUG_7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-888. EDP_CORE_SW_DEBUG_I_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_DEBUG_7_0 | R | 0h | Register used for debug purposes [lower byte]. Can be written internally by firmware to allow Core Driver to read the internal status. Not used during normal operation since it requires a special version of firmware with a debug capabilities. |

8.6.13 EDP_CORE_SW_DEBUG_H_S Register (Offset = 30h) [reset = 0h]

EDP_CORE_SW_DEBUG_H_S is shown in [Figure 8-439](#) and described in [Table 8-890](#).

Return to [Summary Table](#).

Software/Firmware Debug Register.

**Table 8-889. EDP_CORE_SW_DEBUG_H_S
Instances**

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8030h |

Figure 8-439. EDP_CORE_SW_DEBUG_H_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_DEBUG_15_8 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-890. EDP_CORE_SW_DEBUG_H_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_DEBUG_15_8 | R | 0h | Register used for debug purposes [higher byte]. Can be written internally by firmware to allow Core Driver to read the internal status. Not used during normal operation since it requires a special version of firmware with a debug capabilities. |

8.6.14 EDP_CORE_MAILBOX_INT_MASK_S Register (Offset = 34h) [reset = 0h]

EDP_CORE_MAILBOX_INT_MASK_S is shown in [Figure 8-440](#) and described in [Table 8-892](#).

Return to [Summary Table](#).

Mailbox Interrupt mask register

**Table 8-891. EDP_CORE_MAILBOX_INT_MASK_S
Instances**

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8034h |

Figure 8-440. EDP_CORE_MAILBOX_INT_MASK_S Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | MAILBOX_FULL_INT_MASK | MAILBOX_EMPTY_INT_MASK |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-892. EDP_CORE_MAILBOX_INT_MASK_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | MAILBOX_FULL_INT_MASK | R/W | 0h | Mailbox Full Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |
| 0 | MAILBOX_EMPTY_INT_MASK | R/W | 0h | Mailbox Not-empty Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.6.15 EDP_CORE_MAILBOX_INT_STATUS_S Register (Offset = 38h) [reset = 0h]

EDP_CORE_MAILBOX_INT_STATUS_S is shown in [Figure 8-441](#) and described in [Table 8-894](#).

Return to [Summary Table](#).

Mailbox Interrupt Status register

Table 8-893. EDP_CORE_MAILBOX_INT_STATUS_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8038h |

Figure 8-441. EDP_CORE_MAILBOX_INT_STATUS_S Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | MAILBOX_FULL_INT_STATUS | MAILBOX_EMPTY_INT_STATUS |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-894. EDP_CORE_MAILBOX_INT_STATUS_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | MAILBOX_FULL_INT_STATUS | R | 0h | Mailbox full interrupt. Active HIGH. Cleared on read. This interrupt is set when mailbox becomes full which means there is no more space for messages sent from Host processor to internal uCPU and when this interrupt is enabled in MAILBOX_INT_MASK_p register. It is set when mailbox_full bit transitions from 0 to 1. |
| 0 | MAILBOX_EMPTY_INT_STATUS | R | 0h | Mailbox not-empty interrupt. Active HIGH. Cleared on read. This interrupt is set when mailbox becomes not-empty which means there is a response in the mailbox available to read by the Host processor and when interrupt is enabled in MAILBOX_INT_MASK_p register. It is set when mailbox_empty bit transitions from 1 to 0. |

8.6.16 EDP_CORE_SW_CLK_I_S Register (Offset = 3Ch) [reset = 0h]

EDP_CORE_SW_CLK_I_S is shown in [Figure 8-442](#) and described in [Table 8-896](#).

[Return to Summary Table.](#)

Core Clock frequency

Table 8-895. EDP_CORE_SW_CLK_I_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 803Ch |

Figure 8-442. EDP_CORE_SW_CLK_I_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_CLOCK_VAL_L | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-896. EDP_CORE_SW_CLK_I_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_CLOCK_VAL_L | R/W | 0h | Not used. |

8.6.17 EDP_CORE_SW_CLK_H_S Register (Offset = 40h) [reset = 64h]

EDP_CORE_SW_CLK_H_S is shown in [Figure 8-443](#) and described in [Table 8-898](#).

Return to [Summary Table](#).

Core Clock frequency

Table 8-897. EDP_CORE_SW_CLK_H_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8040h |

Figure 8-443. EDP_CORE_SW_CLK_H_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_CLOCK_VAL_H | | | | | | | |
| R-0h | | | | | | | | R/W-64h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-898. EDP_CORE_SW_CLK_H_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_CLOCK_VAL_H | R/W | 64h | Not used. |

8.6.18 EDP_CORE_SW_EVENTS0_S Register (Offset = 44h) [reset = 0h]

EDP_CORE_SW_EVENTS0_S is shown in [Figure 8-444](#) and described in [Table 8-900](#).

Return to [Summary Table](#).

Not used. 0x0 when read.

Table 8-899. EDP_CORE_SW_EVENTS0_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8044h |

Figure 8-444. EDP_CORE_SW_EVENTS0_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-900. EDP_CORE_SW_EVENTS0_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS7_0 | R | 0h | Not used. 0x0 when read. |

8.6.19 EDP_CORE_SW_EVENTS1_S Register (Offset = 48h) [reset = 0h]

EDP_CORE_SW_EVENTS1_S is shown in [Figure 8-445](#) and described in [Table 8-902](#).

Return to [Summary Table](#).

Not used. 0x0 when read.

Table 8-901. EDP_CORE_SW_EVENTS1_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8048h |

Figure 8-445. EDP_CORE_SW_EVENTS1_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS15_8 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-902. EDP_CORE_SW_EVENTS1_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS15_8 | R | 0h | Not used. 0x0 when read. |

8.6.20 EDP_CORE_SW_EVENTS2_S Register (Offset = 4Ch) [reset = 0h]

EDP_CORE_SW_EVENTS2_S is shown in [Figure 8-446](#) and described in [Table 8-904](#).

Return to [Summary Table](#).

Not used. 0x0 when read.

Table 8-903. EDP_CORE_SW_EVENTS2_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 804Ch |

Figure 8-446. EDP_CORE_SW_EVENTS2_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS23_16 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-904. EDP_CORE_SW_EVENTS2_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS23_16 | R | 0h | Not used. 0x0 when read. |

8.6.21 EDP_CORE_SW_EVENTS3_S Register (Offset = 50h) [reset = 0h]

EDP_CORE_SW_EVENTS3_S is shown in [Figure 8-447](#) and described in [Table 8-906](#).

Return to [Summary Table](#).

Not used. 0x0 when read.

Table 8-905. EDP_CORE_SW_EVENTS3_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8050h |

Figure 8-447. EDP_CORE_SW_EVENTS3_S Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | SW_EVENTS31_24 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 8-906. EDP_CORE_SW_EVENTS3_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-8 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 7-0 | SW_EVENTS31_24 | R | 0h | Not used. 0x0 when read. |

8.6.22 EDP_CORE_XT_OCD_CTRL_S Register (Offset = 60h) [reset = 3h]

EDP_CORE_XT_OCD_CTRL_S is shown in [Figure 8-448](#) and described in [Table 8-908](#).

Return to [Summary Table](#).

Internal CPU - On Chip Debug (OCD) Ctrl Register

**Table 8-907. EDP_CORE_XT_OCD_CTRL_S
Instances**

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8060h |

Figure 8-448. EDP_CORE_XT_OCD_CTRL_S Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|-----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | XT_OCDHALT ONRESET | XT_DRESET |
| R-0h | | | | | | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-908. EDP_CORE_XT_OCD_CTRL_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | XT_OCDHALTONRESET | R/W | 1h | Not used |
| 0 | XT_DRESET | R/W | 1h | Not used |

8.6.23 EDP_CORE_XT_OCD_CTRL_RO_S Register (Offset = 64h) [reset = 0h]

EDP_CORE_XT_OCD_CTRL_RO_S is shown in [Figure 8-449](#) and described in [Table 8-910](#).

Return to [Summary Table](#).

Internal CPU - OCD R0 mode configuration

Table 8-909. EDP_CORE_XT_OCD_CTRL_RO_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8064h |

Figure 8-449. EDP_CORE_XT_OCD_CTRL_RO_S Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | XT_XOCDMODE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-910. EDP_CORE_XT_OCD_CTRL_RO_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 0 | XT_XOCDMODE | R | 0h | Internal CPU - OCD mode configuration |

8.6.24 EDP_CORE_APB_INT_MASK_S Register (Offset = 6Ch) [reset = 3h]

EDP_CORE_APB_INT_MASK_S is shown in [Figure 8-450](#) and described in [Table 8-912](#).

Return to [Summary Table](#).

APB Interrupt Mask Register

**Table 8-911. EDP_CORE_APB_INT_MASK_S
Instances**

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 806Ch |

Figure 8-450. EDP_CORE_APB_INT_MASK_S Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | APB_SW_INTR_MASK | APB_MAILBOX_INTR_MASK |
| R-0h | | | | | | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 8-912. EDP_CORE_APB_INT_MASK_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | APB_SW_INTR_MASK | R/W | 1h | Not used. |
| 0 | APB_MAILBOX_INTR_MASK | R/W | 1h | Mailbox Interrupt mask 0x 0-interrupt enabled 0x 1-interrupt disabled |

8.6.25 EDP_CORE_APB_STATUS_S Register (Offset = 70h) [reset = 0h]

EDP_CORE_APB_STATUS_S is shown in [Figure 8-451](#) and described in [Table 8-914](#).

Return to [Summary Table](#).

APB interrupt status register

Table 8-913. EDP_CORE_APB_STATUS_S Instances

| Instance | Physical Address |
|----------------------------------|------------------|
| DSS_EDP0_V2A_S_CORE_VP_REGS_SAPB | 04F4 8070h |

Figure 8-451. EDP_CORE_APB_STATUS_S Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | APB_SW_INTR_STATUS | APB_MAILBOX_INTR_STATUS |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 8-914. EDP_CORE_APB_STATUS_S Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved field. 0x0 when read. Writes ignored. |
| 1 | APB_SW_INTR_STATUS | R | 0h | Not used. |
| 0 | APB_MAILBOX_INTR_STATUS | R | 0h | Mailbox Interrupt status. Active HIGH. If this bit is set further status should be read from MAILBOX_INT_STATUS register. This bit is cleared automatically on read from MAILBOX_INT_STATUS register. |

9 CSI_RX_IF Registers

Table 9-1 lists the the CSI_RX_IF memory map. For detailed description of each memory region, refer to the respective register subsection.

Table 9-1. CSI_RX_IF Memory Map

| Name | Start | End | Size |
|---|------------|------------|------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0000h | 02A3 03FFh | 1 KB |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1000h | 02A3 13FFh | 1 KB |
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0000h | 0450 0FFFh | 4 KB |
| CSI_RX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2RX | 0450 4000h | 0450 4FFFh | 4 KB |
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8000h | 0450 8FFFh | 4 KB |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0000h | 0451 0FFFh | 4 KB |
| CSI_RX_IF1_VBUS2APB_WRAP_VBUSP_APB_CSI2RX | 0451 4000h | 0451 4FFFh | 4 KB |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8000h | 0451 8FFFh | 4 KB |

9.1 CSI_RX_IF_ECC Registers

Table 9-3 lists the memory-mapped registers for the CSI_RX_IF_ECC registers. All register offset addresses not listed in Table 9-3 should be considered as reserved locations and the register contents should not be modified.

Table 9-2. CSI_RX_IF_ECC Instances

| Instance | Base Address |
|-------------------------|--------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0000h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1000h |

Table 9-3. CSI_RX_IF_ECC Registers

| Offset | Acronym | Register Name | CSI_RX_IF0_ECC_AGGR_CFG Physical Address | CSI_RX_IF1_ECC_AGGR_CFG Physical Address |
|---------------|---|---|--|--|
| 0h | CSI_RX_IF_ECC_REV | Aggregator Revision Register | 02A3 0000h | 02A3 1000h |
| 8h | CSI_RX_IF_ECC_VECTOR | ECC Vector Register | 02A3 0008h | 02A3 1008h |
| Ch | CSI_RX_IF_ECC_STAT | Misc Status | 02A3 000Ch | 02A3 100Ch |
| 10h + formula | CSI_RX_IF_ECC_RESERVED_SVBUS_y | Reserved Area for Serial VBUS Registers | 02A3 0010h + formula | 02A3 1010h + formula |
| 3Ch | CSI_RX_IF_ECC_SEC_EOI_REG | EOI Register | 02A3 003Ch | 02A3 103Ch |
| 40h | CSI_RX_IF_ECC_SEC_STATUS_REG0 | Interrupt Status Register 0 | 02A3 0040h | 02A3 1040h |
| 80h | CSI_RX_IF_ECC_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02A3 0080h | 02A3 1080h |
| C0h | CSI_RX_IF_ECC_SEC_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02A3 00C0h | 02A3 10C0h |
| 13Ch | CSI_RX_IF_ECC_DED_EOI_REG | EOI Register | 02A3 013Ch | 02A3 113Ch |
| 140h | CSI_RX_IF_ECC_DED_STATUS_REG0 | Interrupt Status Register 0 | 02A3 0140h | 02A3 1140h |
| 180h | CSI_RX_IF_ECC_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02A3 0180h | 02A3 1180h |
| 1C0h | CSI_RX_IF_ECC_DED_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02A3 01C0h | 02A3 11C0h |
| 200h | CSI_RX_IF_ECC_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 02A3 0200h | 02A3 1200h |
| 204h | CSI_RX_IF_ECC_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 02A3 0204h | 02A3 1204h |
| 208h | CSI_RX_IF_ECC_AGGR_STATUS_SET | AGGR interrupt status set Register | 02A3 0208h | 02A3 1208h |
| 20Ch | CSI_RX_IF_ECC_AGGR_STATUS_CLR | AGGR interrupt status clear Register | 02A3 020Ch | 02A3 120Ch |

9.2 CSI_RX_IF_ECC_REV Register (Offset = 0h) [reset = 66A0EA00h]

CSI_RX_IF_ECC_REV is shown in [Figure 9-1](#) and described in [Table 9-5](#).

Return to [Summary Table](#).

Revision parameters

Table 9-4. CSI_RX_IF_ECC_REV Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0000h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1000h |

Figure 9-1. CSI_RX_IF_ECC_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-5. CSI_RX_IF_ECC_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

9.3 CSI_RX_IF_ECC_VECTOR Register (Offset = 8h) [reset = X]

CSI_RX_IF_ECC_VECTOR is shown in [Figure 9-2](#) and described in [Table 9-7](#).

Return to [Summary Table](#).

ECC Vector Register

Table 9-6. CSI_RX_IF_ECC_VECTOR Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0008h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1008h |

Figure 9-2. CSI_RX_IF_ECC_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|----|------------|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_DONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | | ECC_VECTOR | |
| R/W1S-0h | R/W-X | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-7. CSI_RX_IF_ECC_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or status |

9.4 CSI_RX_IF_ECC_STAT Register (Offset = Ch) [reset = X]

CSI_RX_IF_ECC_STAT is shown in [Figure 9-3](#) and described in [Table 9-9](#).

Return to [Summary Table](#).

Misc Status

Table 9-8. CSI_RX_IF_ECC_STAT Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 000Ch |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 100Ch |

Figure 9-3. CSI_RX_IF_ECC_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | R-8h | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-9. CSI_RX_IF_ECC_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 8h | Indicates the number of RAMs serviced by the ECC aggregator |

9.5 CSI_RX_IF_ECC_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

CSI_RX_IF_ECC_RESERVED_SVBUS_y is shown in [Figure 9-4](#) and described in [Table 9-11](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 9-10. CSI_RX_IF_ECC_RESERVED_SVBUS_y Instances

| Instance | Physical Address |
|-------------------------|----------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0010h + formula |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1010h + formula |

Figure 9-4. CSI_RX_IF_ECC_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-11. CSI_RX_IF_ECC_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

9.6 CSI_RX_IF_ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

CSI_RX_IF_ECC_SEC_EOI_REG is shown in [Figure 9-5](#) and described in [Table 9-13](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 9-12. CSI_RX_IF_ECC_SEC_EOI_REG
Instances**

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 003Ch |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 103Ch |

Figure 9-5. CSI_RX_IF_ECC_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-13. CSI_RX_IF_ECC_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

9.7 CSI_RX_IF_ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

CSI_RX_IF_ECC_SEC_STATUS_REG0 is shown in [Figure 9-6](#) and described in [Table 9-15](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 9-14. CSI_RX_IF_ECC_SEC_STATUS_REG0 Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0040h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1040h |

Figure 9-6. CSI_RX_IF_ECC_SEC_STATUS_REG0 Register

| | | | | | | | |
|--------------------------|--------------------------|----------------------|----------------------|----------------------|----------------------|---------------------------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VP1_FIFO_RA MECC_PEND | VP0_FIFO_RA MECC_PEND | RAM_RAMECC 3_PEND | RAM_RAMECC 2_PEND | RAM_RAMECC 1_PEND | RAM_RAMECC 0_PEND | PSIL_FIFO_RA MECC_PEND | BUSECC_PEN D |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-15. CSI_RX_IF_ECC_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | VP1_FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for vp1_fifo_amecc_pending |
| 6 | VP0_FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for vp0_fifo_amecc_pending |
| 5 | RAM_RAMECC3_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc3_pending |
| 4 | RAM_RAMECC2_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc2_pending |
| 3 | RAM_RAMECC1_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc1_pending |
| 2 | RAM_RAMECC0_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc0_pending |
| 1 | PSIL_FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for psil_fifo_amecc_pending |
| 0 | BUSECC_PEND | R/W1S | 0h | Interrupt Pending Status for busecc_pending |

9.8 CSI_RX_IF_ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

CSI_RX_IF_ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 9-7](#) and described in [Table 9-17](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 9-16.
CSI_RX_IF_ECC_SEC_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0080h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1080h |

Figure 9-7. CSI_RX_IF_ECC_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|------------------------------------|------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-------------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VP1_FIFO_RA MECC_ENABL E_SET | VP0_FIFO_RA MECC_ENABL E_SET | RAM_RAMECC 3_ENABLE_SE T | RAM_RAMECC 2_ENABLE_SE T | RAM_RAMECC 1_ENABLE_SE T | RAM_RAMECC 0_ENABLE_SE T | PSIL_FIFO_RA MECC_ENABL E_SET | BUSECC_ENA BLE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-17. CSI_RX_IF_ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | |
| 7 | VP1_FIFO_RAMECC_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for vp1_fifo_ramecc_pend |
| 6 | VP0_FIFO_RAMECC_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for vp0_fifo_ramecc_pend |
| 5 | RAM_RAMECC3_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc3_pend |
| 4 | RAM_RAMECC2_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc2_pend |
| 3 | RAM_RAMECC1_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc1_pend |
| 2 | RAM_RAMECC0_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc0_pend |
| 1 | PSIL_FIFO_RAMECC_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for psil_fifo_ramecc_pend |
| 0 | BUSECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for busecc_pend |

9.9 CSI_RX_IF_ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

CSI_RX_IF_ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 9-8](#) and described in [Table 9-19](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 9-18.
CSI_RX_IF_ECC_SEC_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 00C0h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 10C0h |

Figure 9-8. CSI_RX_IF_ECC_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|------------------------------------|------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-------------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VP1_FIFO_RA MECC_ENABL E_CLR | VP0_FIFO_RA MECC_ENABL E_CLR | RAM_RAMECC 3_ENABLE_CL R | RAM_RAMECC 2_ENABLE_CL R | RAM_RAMECC 1_ENABLE_CL R | RAM_RAMECC 0_ENABLE_CL R | PSIL_FIFO_RA MECC_ENABL E_CLR | BUSECC_ENA BLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-19. CSI_RX_IF_ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | |
| 7 | VP1_FIFO_RAMECC_EN ABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for vp1_fifo_ramecc_pend |
| 6 | VP0_FIFO_RAMECC_EN ABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for vp0_fifo_ramecc_pend |
| 5 | RAM_RAMECC3_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc3_pend |
| 4 | RAM_RAMECC2_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc2_pend |
| 3 | RAM_RAMECC1_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc1_pend |
| 2 | RAM_RAMECC0_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc0_pend |
| 1 | PSIL_FIFO_RAMECC_EN ABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for psil_fifo_ramecc_pend |
| 0 | BUSECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for busecc_pend |

9.10 CSI_RX_IF_ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

CSI_RX_IF_ECC_DED_EOI_REG is shown in [Figure 9-9](#) and described in [Table 9-21](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 9-20. CSI_RX_IF_ECC_DED_EOI_REG
Instances**

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 013Ch |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 113Ch |

Figure 9-9. CSI_RX_IF_ECC_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-21. CSI_RX_IF_ECC_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

9.11 CSI_RX_IF_ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

CSI_RX_IF_ECC_DED_STATUS_REG0 is shown in [Figure 9-10](#) and described in [Table 9-23](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 9-22. CSI_RX_IF_ECC_DED_STATUS_REG0 Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0140h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1140h |

Figure 9-10. CSI_RX_IF_ECC_DED_STATUS_REG0 Register

| | | | | | | | |
|--------------------------|--------------------------|----------------------|----------------------|----------------------|----------------------|---------------------------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VP1_FIFO_RA MECC_PEND | VP0_FIFO_RA MECC_PEND | RAM_RAMECC 3_PEND | RAM_RAMECC 2_PEND | RAM_RAMECC 1_PEND | RAM_RAMECC 0_PEND | PSIL_FIFO_RA MECC_PEND | BUSECC_PEN D |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-23. CSI_RX_IF_ECC_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|-------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7 | VP1_FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for vp1_fifo_amecc_pending |
| 6 | VP0_FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for vp0_fifo_amecc_pending |
| 5 | RAM_RAMECC3_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc3_pending |
| 4 | RAM_RAMECC2_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc2_pending |
| 3 | RAM_RAMECC1_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc1_pending |
| 2 | RAM_RAMECC0_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc0_pending |
| 1 | PSIL_FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for psil_fifo_amecc_pending |
| 0 | BUSECC_PEND | R/W1S | 0h | Interrupt Pending Status for busecc_pending |

9.12 CSI_RX_IF_ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

CSI_RX_IF_ECC_DED_ENABLE_SET_REG0 is shown in [Figure 9-11](#) and described in [Table 9-25](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 9-24.
CSI_RX_IF_ECC_DED_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0180h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1180h |

Figure 9-11. CSI_RX_IF_ECC_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|------------------------------------|------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-------------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VP1_FIFO_RA MECC_ENABL E_SET | VP0_FIFO_RA MECC_ENABL E_SET | RAM_RAMECC 3_ENABLE_SE T | RAM_RAMECC 2_ENABLE_SE T | RAM_RAMECC 1_ENABLE_SE T | RAM_RAMECC 0_ENABLE_SE T | PSIL_FIFO_RA MECC_ENABL E_SET | BUSECC_ENA BLE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-25. CSI_RX_IF_ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | |
| 7 | VP1_FIFO_RAMECC_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for vp1_fifo_ramecc_pend |
| 6 | VP0_FIFO_RAMECC_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for vp0_fifo_ramecc_pend |
| 5 | RAM_RAMECC3_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc3_pend |
| 4 | RAM_RAMECC2_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc2_pend |
| 3 | RAM_RAMECC1_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc1_pend |
| 2 | RAM_RAMECC0_ENABL E_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_ramecc0_pend |
| 1 | PSIL_FIFO_RAMECC_EN ABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for psil_fifo_ramecc_pend |
| 0 | BUSECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for busecc_pend |

9.13 CSI_RX_IF_ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

CSI_RX_IF_ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 9-12](#) and described in [Table 9-27](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 9-26.
CSI_RX_IF_ECC_DED_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 01C0h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 11C0h |

Figure 9-12. CSI_RX_IF_ECC_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|------------------------------------|------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|-------------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VP1_FIFO_RA MECC_ENABL E_CLR | VP0_FIFO_RA MECC_ENABL E_CLR | RAM_RAMECC 3_ENABLE_CL R | RAM_RAMECC 2_ENABLE_CL R | RAM_RAMECC 1_ENABLE_CL R | RAM_RAMECC 0_ENABLE_CL R | PSIL_FIFO_RA MECC_ENABL E_CLR | BUSECC_ENA BLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-27. CSI_RX_IF_ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | |
| 7 | VP1_FIFO_RAMECC_EN ABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for vp1_fifo_ramecc_pend |
| 6 | VP0_FIFO_RAMECC_EN ABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for vp0_fifo_ramecc_pend |
| 5 | RAM_RAMECC3_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc3_pend |
| 4 | RAM_RAMECC2_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc2_pend |
| 3 | RAM_RAMECC1_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc1_pend |
| 2 | RAM_RAMECC0_ENABL E_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_ramecc0_pend |
| 1 | PSIL_FIFO_RAMECC_EN ABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for psil_fifo_ramecc_pend |
| 0 | BUSECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for busecc_pend |

9.14 CSI_RX_IF_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

CSI_RX_IF_ECC_AGGR_ENABLE_SET is shown in [Figure 9-13](#) and described in [Table 9-29](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 9-28. CSI_RX_IF_ECC_AGGR_ENABLE_SET Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0200h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1200h |

Figure 9-13. CSI_RX_IF_ECC_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-29. CSI_RX_IF_ECC_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

9.15 CSI_RX_IF_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

CSI_RX_IF_ECC_AGGR_ENABLE_CLR is shown in [Figure 9-14](#) and described in [Table 9-31](#).

[Return to Summary Table.](#)

AGGR interrupt enable clear Register

Table 9-30. CSI_RX_IF_ECC_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0204h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1204h |

Figure 9-14. CSI_RX_IF_ECC_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-31. CSI_RX_IF_ECC_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

9.16 CSI_RX_IF_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

CSI_RX_IF_ECC_AGGR_STATUS_SET is shown in [Figure 9-15](#) and described in [Table 9-33](#).

Return to [Summary Table](#).

AGGR interrupt status set Register

**Table 9-32. CSI_RX_IF_ECC_AGGR_STATUS_SET
Instances**

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 0208h |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 1208h |

Figure 9-15. CSI_RX_IF_ECC_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 9-33. CSI_RX_IF_ECC_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt status set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt status set for parity errors |

9.17 CSI_RX_IF_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

CSI_RX_IF_ECC_AGGR_STATUS_CLR is shown in [Figure 9-16](#) and described in [Table 9-35](#).

Return to [Summary Table](#).

AGGR interrupt status clear Register

Table 9-34. CSI_RX_IF_ECC_AGGR_STATUS_CLR Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_RX_IF0_ECC_AGGR_CFG | 02A3 020Ch |
| CSI_RX_IF1_ECC_AGGR_CFG | 02A3 120Ch |

Figure 9-16. CSI_RX_IF_ECC_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 9-35. CSI_RX_IF_ECC_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt status clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt status clear for parity errors |

9.18 CSI_RX_IF_SHIM Registers

Table 9-37 lists the memory-mapped registers for the CSI_RX_IF_SHIM registers. All register offset addresses not listed in Table 9-37 should be considered as reserved locations and the register contents should not be modified.

Table 9-36. CSI_RX_IF_SHIM Instances

| Instance | Base Address |
|---------------------------------------|--------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0000h |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0000h |

Table 9-37. CSI_RX_IF_SHIM Registers

| Offset | Acronym | Register Name | CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF Physical Address | CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF Physical Address |
|--------|---|---------------------------------------|--|--|
| 0h | CSI_RX_IF_SHIM_CSIRX_ID | nothing | 0450 0000h | 0451 0000h |
| 8h | CSI_RX_IF_SHIM_VP0 | Video Port 0 CSI_RX_IF_SHIM_CONFIG | 0450 0008h | 0451 0008h |
| Ch | CSI_RX_IF_SHIM_VP1 | Video Port 1 CSI_RX_IF_SHIM_CONFIG | 0450 000Ch | 0451 000Ch |
| 10h | CSI_RX_IF_SHIM_CNTL | control register for csi rx wrapper | 0450 0010h | 0451 0010h |
| 20h | CSI_RX_IF_SHIM_DMACNTX | DMA Channel Context | 0450 0020h | 0451 0020h |
| 24h | CSI_RX_IF_SHIM_PSI_CFG0 | psi configuration register0 | 0450 0024h | 0451 0024h |
| 28h | CSI_RX_IF_SHIM_PSI_CFG1 | psi configuration register1 | 0450 0028h | 0451 0028h |

9.19 CSI_RX_IF_SHIM_CSIRX_ID Register (Offset = 0h) [reset = 64706100h]

CSI_RX_IF_SHIM_CSIRX_ID is shown in [Figure 9-17](#) and described in [Table 9-39](#).

[Return to Summary Table.](#)

nothing

Table 9-38. CSI_RX_IF_SHIM_CSIRX_ID Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSEP_MMR_CSIRXIF | 0450 0000h |
| CSI_RX_IF1_RX_SHIM_VBUSEP_MMR_CSIRXIF | 0451 0000h |

Figure 9-17. CSI_RX_IF_SHIM_CSIRX_ID Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|------|--------|--------|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | | | BU | | FUNC | | | | | | | | | |
| R-1h | | | | R-2h | | R-470h | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTLVER | | | | | MAJREV | | | CUSTOM | | MINREV | | | | | |
| R-Ch | | | | | R-1h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-39. CSI_RX_IF_SHIM_CSIRX_ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|--------------------------------|
| 31-30 | SCHEME | R | 1h | scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | FUNC | R | 470h | function |
| 15-11 | RTLVER | R | Ch | rtl version |
| 10-8 | MAJREV | R | 1h | major CSI_RX_IF_SHIM_REVISION |
| 7-6 | CUSTOM | R | 0h | custom CSI_RX_IF_SHIM_REVISION |
| 5-0 | MINREV | R | 0h | min CSI_RX_IF_SHIM_REVISION |

9.20 CSI_RX_IF_SHIM_VP0 Register (Offset = 8h) [reset = X]

CSI_RX_IF_SHIM_VP0 is shown in [Figure 9-18](#) and described in [Table 9-41](#).

Return to [Summary Table](#).

Video Port 0 configuration

Table 9-40. CSI_RX_IF_SHIM_VP0 Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0008h |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0008h |

Figure 9-18. CSI_RX_IF_SHIM_VP0 Register

| | | | | | | | |
|----------|----------|----|--------|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EN_CFG | RESERVED | | | IH_CFG | | | |
| R/W-0h | R/W-X | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IH_CFG | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | IW_CFG | | | | |
| R/W-X | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IW_CFG | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-41. CSI_RX_IF_SHIM_VP0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31 | EN_CFG | R/W | 0h | Video Port enable. Disable: drops pixel data Enable: start on VS, captures and sends frame data. Will force ih and iw size by zero pad or trunc. When 1 prevents writing rest of fields in this register. |
| 30-29 | RESERVED | R/W | X | |
| 28-16 | IH_CFG | R/W | 0h | (U13) input height in units of lines. Only writable when vp0_en_cfg=0. writes blockes when vp0_en_cfg=1 |
| 15-13 | RESERVED | R/W | X | |
| 12-00 | IW_CFG | R/W | 0h | (U13) input width in units of RAW data samples. Max usable value determined by populated line buffer RAM size. Only writable when vp0_en_cfg=0. writes blockes when vp0_en_cfg=1. You should read this value first and if set to 0 then you should write the height/width values. |

9.21 CSI_RX_IF_SHIM_VP1 Register (Offset = Ch) [reset = X]

CSI_RX_IF_SHIM_VP1 is shown in [Figure 9-19](#) and described in [Table 9-43](#).

Return to [Summary Table](#).

Video Port 1 configuration

Table 9-42. CSI_RX_IF_SHIM_VP1 Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 000Ch |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 000Ch |

Figure 9-19. CSI_RX_IF_SHIM_VP1 Register

| | | | | | | | |
|----------|----------|----|--------|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EN_CFG | RESERVED | | | IH_CFG | | | |
| R/W-0h | R/W-X | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IH_CFG | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | IW_CFG | | | | |
| R/W-X | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IW_CFG | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-43. CSI_RX_IF_SHIM_VP1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31 | EN_CFG | R/W | 0h | Video Port enable. Disable: drops pixel data Enable: start on VS, captures and sends frame data. Will force ih and iw size by zero pad or trunc. When 1 prevents writing rest of fields in this register. |
| 30-29 | RESERVED | R/W | X | |
| 28-16 | IH_CFG | R/W | 0h | (U13) input height in units of lines. Only writable when vp0_en_cfg=0. writes blockes when vp1_en_cfg=1 |
| 15-13 | RESERVED | R/W | X | |
| 12-00 | IW_CFG | R/W | 0h | (U13) input width in units of RAW data samples. Max usable value determined by populated line buffer RAM size. Only writable when vp1_en_cfg=0. writes blockes when vp1_en_cfg=1. You should read this value first and if set to 0 then you should write the height/width values. |

9.22 CSI_RX_IF_SHIM_CNTL Register (Offset = 10h) [reset = X]

CSI_RX_IF_SHIM_CNTL is shown in [Figure 9-20](#) and described in [Table 9-45](#).

[Return to Summary Table.](#)

control register for csi rx wrapper

Table 9-44. CSI_RX_IF_SHIM_CNTL Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0010h |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0010h |

Figure 9-20. CSI_RX_IF_SHIM_CNTL Register

| | | | | | | | |
|----------|----|----|----|------------------|------------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | STREAM3_IDL E | STREAM2_IDL E | STREAM1_IDL E | STREAM0_IDL E |
| R/W-X | | | | R-1h | R-1h | R-1h | R-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PIXEL_RESET |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-45. CSI_RX_IF_SHIM_CNTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-12 | RESERVED | R/W | X | |
| 11 | STREAM3_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 10 | STREAM2_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 9 | STREAM1_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 8 | STREAM0_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 7-1 | RESERVED | R/W | X | |
| 0 | PIXEL_RESET | R/W | 0h | reset for the pixeal interface. 0-reset, 1 not in reset. this should be asserted till after you program the csi controller configuration registers |

9.23 CSI_RX_IF_SHIM_DMACNTX Register (Offset = 20h) [reset = X]

CSI_RX_IF_SHIM_DMACNTX is shown in [Figure 9-21](#) and described in [Table 9-47](#).

Return to [Summary Table](#).

DMA Channel Context. Configuration for each of 32 possible channel contexts. Illegal to program 2 chanCntx with same extraction values.

Table 9-46. CSI_RX_IF_SHIM_DMACNTX Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0020h |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0020h |

Figure 9-21. CSI_RX_IF_SHIM_DMACNTX Register

| | | | | | | | |
|------------|------------|------------|------------|-----------------|------------|--------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EN_CFG | RESERVED | RSV0 | RSV1 | YUV422_MODE_CFG | RSV2 | DUAL_PCK_CFG | |
| R/W-0h | R/W-X | R/W-0h | R/W-0h | R/W-3h | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | SIZE_CFG | RESERVED | PCK12_CFG | RESERVED | | | |
| R/W-X | R/W-0h | R/W-X | R/W-0h | R/W-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | VIRTCH_CFG | |
| R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VIRTCH_CFG | DATTYP_CFG | DATTYP_CFG | DATTYP_CFG | DATTYP_CFG | DATTYP_CFG | DATTYP_CFG | DATTYP_CFG |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-47. CSI_RX_IF_SHIM_DMACNTX Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31 | EN_CFG | R/W | 0h | DMA context is enabled. Will extract channel if input matches dataType and VirtualChan |
| 30 | RESERVED | R/W | X | |
| 29 | RSV0 | R/W | 0h | reserved |
| 28 | RSV1 | R/W | 0h | reserved |
| 27-26 | YUV422_MODE_CFG | R/W | 3h | yuv422 mode 00:UYVY, 01:VYUY, 10:YUYV, 11:YVYU |
| 25 | RSV2 | R/W | 0h | reserved |
| 24 | DUAL_PCK_CFG | R/W | 0h | dual packed format extraction for 8 bits or less |
| 23-22 | RESERVED | R/W | X | |
| 21-20 | SIZE_CFG | R/W | 0h | data size shift when unpacking, 00=8, 01=16, 10=32, 11=RSVD |
| 19 | RESERVED | R/W | X | |
| 18 | PCK12_CFG | R/W | 0h | 12-bit packing enable |
| 17-10 | RESERVED | R/W | X | |

Table 9-47. CSI_RX_IF_SHIM_DMACNTX Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 9-06 | VIRTCH_CFG | R/W | 0h | CSI virtual channel index. Supplied by MIPI CSI protocol to DPHY. For CSISver1.3 program 2MSb==0 |
| 5-00 | DATTYP_CFG | R/W | 0h | CSI data type index. Supplied by MIPI CSI protocol to DPHY |

9.24 CSI_RX_IF_SHIM_PSI_CFG0 Register (Offset = 24h) [reset = 0h]

CSI_RX_IF_SHIM_PSI_CFG0 is shown in [Figure 9-22](#) and described in [Table 9-49](#).

Return to [Summary Table](#).

psi configuration register0

Table 9-48. CSI_RX_IF_SHIM_PSI_CFG0 Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0024h |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0024h |

Figure 9-22. CSI_RX_IF_SHIM_PSI_CFG0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DST_TAG | | | | | | | | | | | | | | | | SRC_TAG | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-49. CSI_RX_IF_SHIM_PSI_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------|------|-------|----------------|
| 31-16 | DST_TAG | R/W | 0h | psi dst tag |
| 15-0 | SRC_TAG | R/W | 0h | psi source tag |

9.25 CSI_RX_IF_SHIM_PSI_CFG1 Register (Offset = 28h) [reset = X]

CSI_RX_IF_SHIM_PSI_CFG1 is shown in [Figure 9-23](#) and described in [Table 9-51](#).

Return to [Summary Table](#).

psi configuration register1

Table 9-50. CSI_RX_IF_SHIM_PSI_CFG1 Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_RX_IF0_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0450 0028h |
| CSI_RX_IF1_RX_SHIM_VBUSP_MMR_CSI2RXIF | 0451 0028h |

Figure 9-23. CSI_RX_IF_SHIM_PSI_CFG1 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----------|----|----|----|----------|----|----|----|----------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | PS_FLAGS | | | | RESERVED | | | | PKT_TYPE | | | |
| R/W-X | | | | R/W-0h | | | | R/W-X | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-51. CSI_RX_IF_SHIM_PSI_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-----------------|
| 31-12 | RESERVED | R/W | X | |
| 11-8 | PS_FLAGS | R/W | 0h | ps flags |
| 7-5 | RESERVED | R/W | X | |
| 4-0 | PKT_TYPE | R/W | 0h | psi packet type |

9.26 CSI_RX_IF_VBUS2APB Registers

Table 9-53 lists the memory-mapped registers for the CSI_RX_IF_VBUS2APB registers. All register offset addresses not listed in Table 9-53 should be considered as reserved locations and the register contents should not be modified.

Table 9-52. CSI_RX_IF_VBUS2APB Instances

| Instance | Base Address |
|---------------------|--------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4000h |
| CSI_RX_IF_VBUS2APB1 | 0451 4000h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|---|---|---|
| 0h | CSI_RX_IF_VBUS2APB_DEVICE_CONFIG | This register provides information related to the current configuration. This should be read by FW to determine the number of streams available and other associated parameters that will influence how the device should be controlled. | 0450 4000h | 0451 4000h |
| 4h | CSI_RX_IF_VBUS2APB_SOFT_RESET | CSI2 Slave Controller Individual Soft Reset for Front and Protocol blocks. Writing to these registers will cause a single cycle pulse to be applied to the soft reset signals. Soft reset must only be applied when the associated clocks are running. These are used to recover from error conditions and should not be required during normal operation. | 0450 4004h | 0451 4004h |
| 8h | CSI_RX_IF_VBUS2APB_STATIC_CFG | Configuration register to set the physical/logical DPHY lane mapping, the number of lanes being used, external DPHY selection and ECC support for CSI2RX v2.0. This register should be set prior to enabling the streams and must not be updated when the stream is running. | 0450 4008h | 0451 4008h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|---|---|---|
| 10h | CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG | Error detection event flag configuration. This allows various error conditions to be masked that would normally prevent data being applied to the pixel interface. This applies to ALL streams that are enabled. This register should only be modified while the datapath is disabled. In case this register is modified while the datapath is enabled, the behavior on the current frame is unpredictable. Hard reset value is 0x00000000, meaning all error masking is disabled. | 0450 4010h | 0451 4010h |
| 18h | CSI_RX_IF_VBUS2APB_MONITOR_IRQS | Information type Interrupt status (non-error conditions) | 0450 4018h | 0451 4018h |
| 1Ch | CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG | Monitor interrupt mask. Bit addressable mask register in order to independently enable each event to trigger the monitor_irq line. Only events whose corresponding bit is set to 1 can trigger the interruption line. Hard reset is 0x00000000, i.e. interrupt line disabled | 0450 401Ch | 0451 401Ch |
| 20h | CSI_RX_IF_VBUS2APB_INFO_IRQS | Information type Interrupt status (non-error conditions) | 0450 4020h | 0451 4020h |
| 24h | CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG | Information interrupt mask. Bit addressable mask register in order to independently enable each event to trigger the info_irq line. Only events whose corresponding bit is set to 1 can trigger the interruption line. Hard reset is 0x00000000, i.e. interrupt line disabled | 0450 4024h | 0451 4024h |
| 28h | CSI_RX_IF_VBUS2APB_ERROR_IRQS | Datapath error interrupt status. Provides information about data path errors. The host processor can read the interrupt status register to identify the root cause of the event, typically after that the csi2rx_err_irq interrupt line is raised | 0450 4028h | 0451 4028h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 2Ch | CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG | Datapath error interrupt enable Bits. This register is used to independently enable each event to trigger the err_irq interrupt line. Only events whose corresponding enable bit is set to 1 can trigger the interrupt line. Hard reset is 0x00000000, i.e. all interrupt lines are disabled | 0450 402Ch | 0451 402Ch |
| 40h | CSI_RX_IF_VBUS2APB_DPHY_LANE_CONTROL | DPHY lane control for data and clock lanes enables and resets | 0450 4040h | 0451 4040h |
| 48h | CSI_RX_IF_VBUS2APB_DPHY_STATUS | DPHY Clock and Data Lane mode status | 0450 4048h | 0451 4048h |
| 4Ch | CSI_RX_IF_VBUS2APB_DPHY_ERR_STATUS_IRQ | DPHY error interrupt status | 0450 404Ch | 0451 404Ch |
| 50h | CSI_RX_IF_VBUS2APB_DPHY_ERR_IRQ_MASK_CFG | DPHY error interrupt status | 0450 4050h | 0451 4050h |
| 60h | CSI_RX_IF_VBUS2APB_INTEGRATION_DEBUG | Used to observe the current data field, extracted by the protocol block from the last short packet data field and FSM state. FSM states are one-hot. It also indicates what data type and virtual channels were used for that short packet. This is primarily used during error condition debug. Since the data can come from asynchronous domains the data coherency cannot be relied upon. | 0450 4060h | 0451 4060h |
| 74h | CSI_RX_IF_VBUS2APB_ERROR_DEBUG | Error condition debug. After an error is detected by the CSI2RX, this register indicates which virtual channel, datatype and data field is impacted. | 0450 4074h | 0451 4074h |
| 80h | CSI_RX_IF_VBUS2APB_TEST_GENERIC | Generic test control and status register that controls and reads primary I/O. | 0450 4080h | 0451 4080h |
| 100h | CSI_RX_IF_VBUS2APB_STREAM0_CTRL | CSI2RX Stream Data output datapath control. Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started. | 0450 4100h | 0451 4100h |
| 104h | CSI_RX_IF_VBUS2APB_STREAM0_STATUS | CSI2 Slave Controller Status. Contains useful debug information such as FSM states. | 0450 4104h | 0451 4104h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 108h | CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG | Secondary CSI2 Slave Controller Data outputs configuration. This register is used to configure the data types and virtual channels are processed and output by this stream. | 0450 4108h | 0451 4108h |
| 10Ch | CSI_RX_IF_VBUS2APB_STREAM0_CFG | Primary CSI2 Slave Controller Data pixel outputs configuration. This register is used to configure the output mode. It is also used to set up some Stream FIFO related settings. | 0450 410Ch | 0451 410Ch |
| 110h | CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL | Stream Monitor configuration. This register is used to configure the CSI2RX Monitors: Programmable Frame monitor to trigger an event if a truncated frame is detected, Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end, Programmable line/byte counters to trigger an event at a specific byte in a line. This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event. This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled. In these cases, the behaviour is unpredictable. Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0. | 0450 4110h | 0451 4110h |
| 114h | CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_FRAME | Stream Monitor Frame. Used to observe the current frame number and packet size on monitored virtual channels. These values are extracted by the CSI2RX from the last frame start short packet data field. | 0450 4114h | 0451 4114h |
| 118h | CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_LB | Stream Monitor Line. Used to specify the byte and line numbers that will generate an interrupt. This register must only be modified when the corresponding line/byte enable is disabled. | 0450 4118h | 0451 4118h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 11Ch | CSI_RX_IF_VBUS2APB_STREAM0_TIMER | Stream Timer. Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end. This register must only be modified when the corresponding timer enable is disabled. | 0450 411Ch | 0451 411Ch |
| 120h | CSI_RX_IF_VBUS2APB_STREAM0_FCC_CFG | Stream Frame Capture Control configuration. Used to specify the frame count value when the CSI2RX must generate interrupts FCC_START and FCC_STOP. This register must only be modified when the corresponding frame count enable is disabled. | 0450 4120h | 0451 4120h |
| 124h | CSI_RX_IF_VBUS2APB_STREAM0_FCC_CTRL | Stream Frame Capture Counter control. Used to enable / disable the FCC and specify which virtual channel it should operate on. | 0450 4124h | 0451 4124h |
| 128h | CSI_RX_IF_VBUS2APB_STREAM0_FIFO_FILL_LVL | Stream FIFO fill level monitor. This can operate in 2 modes: 1 - Monitor peak fill level until the stream is stopped. 2 - Monitor peak fill level when the first FIFO read is made during a frame. | 0450 4128h | 0451 4128h |
| 200h | CSI_RX_IF_VBUS2APB_STREAM1_CTRL | CSI2RX Stream Data output datapath control. Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started. | 0450 4200h | 0451 4200h |
| 204h | CSI_RX_IF_VBUS2APB_STREAM1_STATUS | CSI2 Slave Controller Status. Contains useful debug information such as FSM states. | 0450 4204h | 0451 4204h |
| 208h | CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG | Secondary CSI2 Slave Controller Data outputs configuration. This register is used to configure the data types and virtual channels are processed and output by this stream. | 0450 4208h | 0451 4208h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 20Ch | CSI_RX_IF_VBUS2APB_STREAM1_CFG | Primary CSI2 Slave Controller Data pixel outputs configuration. This register is used to configure the output mode. It is also used to set up some Stream FIFO related settings. | 0450 420Ch | 0451 420Ch |
| 210h | CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL | Stream Monitor configuration. This register is used to configure the CSI2RX Monitors: Programmable Frame monitor to trigger an event if a truncated frame is detected, Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end, Programmable line/byte counters to trigger an event at a specific byte in a line. This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event. This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled. In these cases, the behaviour is unpredictable. Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0. | 0450 4210h | 0451 4210h |
| 214h | CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_FRAME | Stream Monitor Frame. Used to observe the current frame number and packet size on monitored virtual channels. These values are extracted by the CSI2RX from the last frame start short packet data field. | 0450 4214h | 0451 4214h |
| 218h | CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_LB | Stream Monitor Line. Used to specify the byte and line numbers that will generate an interrupt. This register must only be modified when the corresponding line/byte enable is disabled. | 0450 4218h | 0451 4218h |
| 21Ch | CSI_RX_IF_VBUS2APB_STREAM1_TIMER | Stream Timer. Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end. This register must only be modified when the corresponding timer enable is disabled. | 0450 421Ch | 0451 421Ch |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 220h | CSI_RX_IF_VBUS2APB_STREAM1_FCC_CFG | Stream Frame Capture Control configuration. Used to specify the frame count value when the CSI2RX must generate interrupts FCC_START and FCC_STOP. This register must only be modified when the corresponding frame count enable is disabled. | 0450 4220h | 0451 4220h |
| 224h | CSI_RX_IF_VBUS2APB_STREAM1_FCC_CTRL | Stream Frame Capture Counter control. Used to enable / disable the FCC and specify which virtual channel it should operate on. | 0450 4224h | 0451 4224h |
| 228h | CSI_RX_IF_VBUS2APB_STREAM1_FIFO_FILL_LVL | Stream FIFO fill level monitor. This can operate in 2 modes: 1 - Monitor peak fill level until the stream is stopped. 2 - Monitor peak fill level when the first FIFO read is made during a frame. | 0450 4228h | 0451 4228h |
| 300h | CSI_RX_IF_VBUS2APB_STREAM2_CTRL | CSI2RX Stream Data output datapath control. Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started. | 0450 4300h | 0451 4300h |
| 304h | CSI_RX_IF_VBUS2APB_STREAM2_STATUS | CSI2 Slave Controller Status. Contains useful debug information such as FSM states. | 0450 4304h | 0451 4304h |
| 308h | CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG | Secondary CSI2 Slave Controller Data outputs configuration. This register is used to configure the data types and virtual channels are processed and output by this stream. | 0450 4308h | 0451 4308h |
| 30Ch | CSI_RX_IF_VBUS2APB_STREAM2_CFG | Primary CSI2 Slave Controller Data pixel outputs configuration. This register is used to configure the output mode. It is also used to set up some Stream FIFO related settings. | 0450 430Ch | 0451 430Ch |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|---|---|---|
| 310h | CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL | Stream Monitor configuration. This register is used to configure the CSI2RX Monitors: Programmable Frame monitor to trigger an event if a truncated frame is detected, Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end, Programmable line/byte counters to trigger an event at a specific byte in a line. This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event. This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled. In these cases, the behaviour is unpredictable. Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0. | 0450 4310h | 0451 4310h |
| 314h | CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_FRAME | Stream Monitor Frame. Used to observe the current frame number and packet size on monitored virtual channels. These values are extracted by the CSI2RX from the last frame start short packet data field. | 0450 4314h | 0451 4314h |
| 318h | CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_LB | Stream Monitor Line. Used to specify the byte and line numbers that will generate an interrupt. This register must only be modified when the corresponding line/byte enable is disabled. | 0450 4318h | 0451 4318h |
| 31Ch | CSI_RX_IF_VBUS2APB_STREAM2_TIMER | Stream Timer. Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end. This register must only be modified when the corresponding timer enable is disabled. | 0450 431Ch | 0451 431Ch |
| 320h | CSI_RX_IF_VBUS2APB_STREAM2_FCC_CFG | Stream Frame Capture Control configuration. Used to specify the frame count value when the CSI2RX must generate interrupts FCC_START and FCC_STOP. This register must only be modified when the corresponding frame count enable is disabled. | 0450 4320h | 0451 4320h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 324h | CSI_RX_IF_VBUS2APB_STREAM2_FCC_CTRL | Stream Frame Capture Counter control. Used to enable / disable the FCC and specify which virtual channel it should operate on. | 0450 4324h | 0451 4324h |
| 328h | CSI_RX_IF_VBUS2APB_STREAM2_FIFO_FILL_LVL | Stream FIFO fill level monitor. This can operate in 2 modes: 1 - Monitor peak fill level until the stream is stopped. 2 - Monitor peak fill level when the first FIFO read is made during a frame. | 0450 4328h | 0451 4328h |
| 400h | CSI_RX_IF_VBUS2APB_STREAM3_CTRL | CSI2RX Stream Data output datapath control. Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started. | 0450 4400h | 0451 4400h |
| 404h | CSI_RX_IF_VBUS2APB_STREAM3_STATUS | CSI2 Slave Controller Status. Contains useful debug information such as FSM states. | 0450 4404h | 0451 4404h |
| 408h | CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG | Secondary CSI2 Slave Controller Data outputs configuration. This register is used to configure the data types and virtual channels are processed and output by this stream. | 0450 4408h | 0451 4408h |
| 40Ch | CSI_RX_IF_VBUS2APB_STREAM3_CFG | Primary CSI2 Slave Controller Data pixel outputs configuration. This register is used to configure the output mode. It is also used to set up some Stream FIFO related settings. | 0450 440Ch | 0451 440Ch |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|---|---|---|
| 410h | CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL | Stream Monitor configuration. This register is used to configure the CSI2RX Monitors: Programmable Frame monitor to trigger an event if a truncated frame is detected, Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end, Programmable line/byte counters to trigger an event at a specific byte in a line. This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event. This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled. In these cases, the behaviour is unpredictable. Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0. | 0450 4410h | 0451 4410h |
| 414h | CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_FRAME | Stream Monitor Frame. Used to observe the current frame number and packet size on monitored virtual channels. These values are extracted by the CSI2RX from the last frame start short packet data field. | 0450 4414h | 0451 4414h |
| 418h | CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_LB | Stream Monitor Line. Used to specify the byte and line numbers that will generate an interrupt. This register must only be modified when the corresponding line/byte enable is disabled. | 0450 4418h | 0451 4418h |
| 41Ch | CSI_RX_IF_VBUS2APB_STREAM3_TIMER | Stream Timer. Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end. This register must only be modified when the corresponding timer enable is disabled. | 0450 441Ch | 0451 441Ch |
| 420h | CSI_RX_IF_VBUS2APB_STREAM3_FCC_CFG | Stream Frame Capture Control configuration. Used to specify the frame count value when the CSI2RX must generate interrupts FCC_START and FCC_STOP. This register must only be modified when the corresponding frame count enable is disabled. | 0450 4420h | 0451 4420h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|--|---|---|
| 424h | CSI_RX_IF_VBUS2APB_STREAM3_FCC_CTRL | Stream Frame Capture Counter control. Used to enable / disable the FCC and specify which virtual channel it should operate on. | 0450 4424h | 0451 4424h |
| 428h | CSI_RX_IF_VBUS2APB_STREAM3_FIFO_FILL_LVL | Stream FIFO fill level monitor. This can operate in 2 modes: 1 - Monitor peak fill level until the stream is stopped. 2 - Monitor peak fill level when the first FIFO read is made during a frame. | 0450 4428h | 0451 4428h |
| 900h | CSI_RX_IF_VBUS2APB_ASF_INT_STATUS | ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_int_fatal or asf_int_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register. | 0450 4900h | 0451 4900h |
| 904h | CSI_RX_IF_VBUS2APB_ASF_INT_RAW_STATUS | ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register. | 0450 4904h | 0451 4904h |
| 908h | CSI_RX_IF_VBUS2APB_ASF_INT_MASK | The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt. | 0450 4908h | 0451 4908h |
| 90Ch | CSI_RX_IF_VBUS2APB_ASF_INT_TEST | The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrupt accordingly. | 0450 490Ch | 0451 490Ch |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|---|---|---|
| 910h | CSI_RX_IF_VBUS2APB_ASF_FATAL_NONFATAL_SELECT | The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered. | 0450 4910h | 0451 4910h |
| 920h | CSI_RX_IF_VBUS2APB_ASF_SRAM_CORR_FAULT_STATU S | Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active. | 0450 4920h | 0451 4920h |
| 924h | CSI_RX_IF_VBUS2APB_ASF_SRAM_UNCORR_FAULT_ST ATUS | Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active. | 0450 4924h | 0451 4924h |
| 928h | CSI_RX_IF_VBUS2APB_ASF_SRAM_FAULT_STATS | Statistics register for SRAM faults. Note that this register clears when software writes to any field. | 0450 4928h | 0451 4928h |
| 930h | CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_CTRL | Control register to configure the ASF transaction timeout monitors. | 0450 4930h | 0451 4930h |
| 934h | CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_MASK | Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific. | 0450 4934h | 0451 4934h |
| 938h | CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_STATUS | Status register for transaction timeouts fault. If a fault occurs the revelant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit. | 0450 4938h | 0451 4938h |
| 940h | CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK | Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific. | 0450 4940h | 0451 4940h |
| 944h | CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS | Status register for protocol faults. If a fault occurs the revelant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit | 0450 4944h | 0451 4944h |

Table 9-53. CSI_RX_IF_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | CSI_RX_IF_VBUS2APB 0 Physical Address | CSI_RX_IF_VBUS2APB 1 Physical Address |
|--------|--|---|---|---|
| FFCh | CSI_RX_IF_VBUS2APB_ID_PROD_VER | <p>This register is hard-coded in order to allow software to identify the product and its release version.</p> <p>The product ID will be fixed for all versions, while the version will be updated as new releases for the CSI2RX product are made.</p> | 0450 4FFCh | 0451 4FFCh |

9.27 CSI_RX_IF_VBUS2APB_DEVICE_CONFIG Register (Offset = 0h) [reset = X]

CSI_RX_IF_VBUS2APB_DEVICE_CONFIG is shown in [Figure 9-24](#) and described in [Table 9-55](#).

Return to [Summary Table](#).

This register provides information related to the current configuration.

This should be read by FW to determine the number of streams available and other associated parameters that will influence how the device should be controlled.

Table 9-54.
CSI_RX_IF_VBUS2APB_DEVICE_CONFIG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4000h |
| CSI_RX_IF_VBUS2APB1 | 0451 4000h |

Figure 9-24. CSI_RX_IF_VBUS2APB_DEVICE_CONFIG Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------------|--------------------|------------------------|--------------------|---------------|------------------------|--------------------|------------------------|
| STREAM3_MONITOR_PRESEN | STREAM3_NUM_PIXELS | | STREAM3_FIFO_MODE | | STREAM2_MONITOR_PRESEN | STREAM2_NUM_PIXELS | |
| R-1h | R-0h | | R-0h | | R-1h | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STREAM2_FIFO_MODE | | STREAM1_MONITOR_PRESEN | STREAM1_NUM_PIXELS | | STREAM1_FIFO_MODE | | STREAM0_MONITOR_PRESEN |
| R-0h | | R-1h | R-0h | | R-0h | | R-1h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| STREAM0_NUM_PIXELS | | STREAM0_FIFO_MODE | | RESERVED | ASF_CONFIG | VCX_CONFIG | DATAPATH_SIZE |
| R-0h | | R-0h | | R-X | R-1h | R-1h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATAPATH_SIZE | NUM_STREAMS | | | CDNS_PHY_PRES | MAX_LANE_NB | | |
| R-0h | R-4h | | | R-1h | R-4h | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-55. CSI_RX_IF_VBUS2APB_DEVICE_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31 | STREAM3_MONITOR_PRES | R | 1h | Pixel stream 3 Monitor present 1 = implemented |
| 30-29 | STREAM3_NUM_PIXELS | R | 0h | The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 28-27 | STREAM3_FIFO_MODE | R | 0h | Stream 3 FIFO Mode. |
| 26 | STREAM2_MONITOR_PRES | R | 1h | Pixel stream 2 Monitor present 1 = implemented |

Table 9-55. CSI_RX_IF_VBUS2APB_DEVICE_CONFIG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 25-24 | STREAM2_NUM_PIXELS | R | 0h | The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 23-22 | STREAM2_FIFO_MODE | R | 0h | Stream 2 FIFO Mode. |
| 21 | STREAM1_MONITOR_P RESENT | R | 1h | Pixel stream 1 Monitor present 1 = implemented |
| 20-19 | STREAM1_NUM_PIXELS | R | 0h | The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 18-17 | STREAM1_FIFO_MODE | R | 0h | Stream 1 FIFO Mode. |
| 16 | STREAM0_MONITOR_P RESENT | R | 1h | Pixel stream 0 Monitor present 1 = implemented |
| 15-14 | STREAM0_NUM_PIXELS | R | 0h | The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 13-12 | STREAM0_FIFO_MODE | R | 0h | Stream 0 FIFO Mode. |
| 11 | RESERVED | R | X | |
| 10 | ASF_CONFIG | R | 1h | Additional Features [ASF] Configuration: 0 = None 1 = Full ASF. |
| 9 | VCX_CONFIG | R | 1h | Extended Virtual Channel [VCX] Configuration: 0 = 4 VCs 1 = 16 VCs |
| 8-7 | DATAPATH_SIZE | R | 0h | Internal Datapath width 00 - 32 bit, 01 - 64bit, 10 - 16 bit, 11 - 8 Bits. |
| 6-4 | NUM_STREAMS | R | 4h | Number of Stream interfaces [1-4] |
| 3 | CDNS_PHY_PRESENT | R | 1h | DPDHY present 1 = Yes |

Table 9-55. CSI_RX_IF_VBUS2APB_DEVICE_CONFIG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|------------------------------|
| 2-0 | MAX_LANE_NB | R | 4h | Max Number of Lanes [1-4] |

9.28 CSI_RX_IF_VBUS2APB_SOFT_RESET Register (Offset = 4h) [reset = X]

CSI_RX_IF_VBUS2APB_SOFT_RESET is shown in [Figure 9-25](#) and described in [Table 9-57](#).

Return to [Summary Table](#).

CSI2 Slave Controller Individual Soft Reset for Front and Protocol blocks.

Writing to these registers will cause a single cycle pulse to be applied to the soft reset signals.

Soft reset must only be applied when the associated clocks are running.

These are used to recover from error conditions and should not be required during normal operation.

Table 9-56. CSI_RX_IF_VBUS2APB_SOFT_RESET Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4004h |
| CSI_RX_IF_VBUS2APB1 | 0451 4004h |

Figure 9-25. CSI_RX_IF_VBUS2APB_SOFT_RESET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | PROTOCOL | FRONT |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-57. CSI_RX_IF_VBUS2APB_SOFT_RESET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | PROTOCOL | R/W1C | 0h | writing 1'b1 will apply a synchronous soft reset to the protocol module |
| 0 | FRONT | R/W1C | 0h | writing 1'b1 will apply a synchronous soft reset to the Front module |

9.29 CSI_RX_IF_VBUS2APB_STATIC_CFG Register (Offset = 8h) [reset = X]

CSI_RX_IF_VBUS2APB_STATIC_CFG is shown in [Figure 9-26](#) and described in [Table 9-59](#).

Return to [Summary Table](#).

Configuration register to set the physical/logical DPHY lane mapping, the number of lanes being used, external DPHY selection and ECC support for CSI2RX v2.0. This register should be set prior to enabling the streams and must not be updated when the stream is running.

Table 9-58. CSI_RX_IF_VBUS2APB_STATIC_CFG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4008h |
| CSI_RX_IF_VBUS2APB1 | 0451 4008h |

Figure 9-26. CSI_RX_IF_VBUS2APB_STATIC_CFG Register

| | | | | | | | |
|----------|---------|--------|---------------------|----------|---------|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | DL3_MAP | | | RESERVED | DL2_MAP | | |
| R/W-X | | R/W-4h | | R/W-X | | R/W-3h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | DL1_MAP | | | RESERVED | DL0_MAP | | |
| R/W-X | | R/W-2h | | R/W-X | | R/W-1h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | LANE_NB | | |
| R/W-X | | | | | R/W-1h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | V2P0_SUPPORT_ENABLE | RESERVED | | SEL | |
| R/W-X | | | R/W-0h | | R/W-X | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-59. CSI_RX_IF_VBUS2APB_STATIC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31 | RESERVED | R/W | X | |
| 30-28 | DL3_MAP | R/W | 4h | physical mapping of logical data lane 3 |
| 27 | RESERVED | R/W | X | |
| 26-24 | DL2_MAP | R/W | 3h | physical mapping of logical data lane 2. |
| 23 | RESERVED | R/W | X | |
| 22-20 | DL1_MAP | R/W | 2h | physical mapping of logical data lane 1. |
| 19 | RESERVED | R/W | X | |
| 18-16 | DL0_MAP | R/W | 1h | physical mapping of logical data lane 0. |
| 15-11 | RESERVED | R/W | X | |
| 10-8 | LANE_NB | R/W | 1h | The number of lanes |
| 7-5 | RESERVED | R/W | X | |
| 4 | V2P0_SUPPORT_ENAB LE | R/W | 0h | Support extended VC, up to 16 virtual channels [4-bits] and RAW16/20. as per CSI2RX v2.0. Default is up to 4 virtual channels [3-bits] as per CSI2RX v1.3 |

Table 9-59. CSI_RX_IF_VBUS2APB_STATIC_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 3-2 | RESERVED | R/W | X | |
| 1-0 | SEL | R/W | 0h | selection of DPHY used as input of CSI2RX module |

9.30 CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG Register (Offset = 10h) [reset = X]

CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG is shown in [Figure 9-27](#) and described in [Table 9-61](#).

Return to [Summary Table](#).

Error detection event flag configuration.

This allows various error conditions to be masked that would normally prevent data being applied to the pixel interface.

This applies to ALL streams that are enabled.

This register should only be modified while the datapath is disabled.

In case this register is modified while the datapath is enabled, the behavior on the current frame is unpredictable.

Hard reset value is 0x00000000, meaning all error masking is disabled.

Table 9-60.
CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4010h |
| CSI_RX_IF_VBUS2APB1 | 0451 4010h |

Figure 9-27. CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG Register

| | | | | | | | |
|----------|----|----|----|----|---------|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | DATA_ID | ECC | CRC |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-61. CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-3 | RESERVED | R/W | X | |
| 2 | DATA_ID | R/W | 0h | Enables Data ID error bypass for stream outputs. When enabled, Data ID errors in packets are signalled as interrupt events, however the data is still passed to the pixel/packed data outputs. The system must decide to mask or use the pixel data. |
| 1 | ECC | R/W | 0h | Enables ECC error bypass for stream outputs. When enabled, CRC errors in packets are signalled as interrupt events, however the data is still passed to the pixel/packed data outputs. The system must decide to mask or use the pixel data. NOTE:Currently not fully supported. |

Table 9-61. CSI_RX_IF_VBUS2APB_ERROR_BYPASS_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 0 | CRC | R/W | 0h | <p>Enables CRC error bypass for stream outputs.</p> <p>When enabled, CRC errors in packets are signalled as interrupt events, however the data is still passed to the pixel/packed data outputs.</p> <p>The system must decide to mask or use the pixel data.</p> |

9.31 CSI_RX_IF_VBUS2APB_MONITOR_IRQS Register (Offset = 18h) [reset = 0h]

CSI_RX_IF_VBUS2APB_MONITOR_IRQS is shown in [Figure 9-28](#) and described in [Table 9-63](#).

Return to [Summary Table](#).

Information type Interrupt status (non-error conditions)

**Table 9-62. CSI_RX_IF_VBUS2APB_MONITOR_IRQS
Instances**

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4018h |
| CSI_RX_IF_VBUS2APB1 | 0451 4018h |

Figure 9-28. CSI_RX_IF_VBUS2APB_MONITOR_IRQS Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------|----------------------------|-------------------------------|----------------------|-----------------------|-------------------|-----------------------|-------------------|
| STREAM3_LINE_CNT_ERROR_IRQ | STREAM3_FRAME_MISMATCH_IRQ | STREAM3_FRAME_COUNT_ERROR_IRQ | STREAM3_FCC_STOP_IRQ | STREAM3_FCC_START_IRQ | STREAM3_FRAME_IRQ | STREAM3_LINE_BYTE_IRQ | STREAM3_TIMER_IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STREAM2_LINE_CNT_ERROR_IRQ | STREAM2_FRAME_MISMATCH_IRQ | STREAM2_FRAME_COUNT_ERROR_IRQ | STREAM2_FCC_STOP_IRQ | STREAM2_FCC_START_IRQ | STREAM2_FRAME_IRQ | STREAM2_LINE_BYTE_IRQ | STREAM2_TIMER_IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| STREAM1_LINE_CNT_ERROR_IRQ | STREAM1_FRAME_MISMATCH_IRQ | STREAM1_FRAME_COUNT_ERROR_IRQ | STREAM1_FCC_STOP_IRQ | STREAM1_FCC_START_IRQ | STREAM1_FRAME_IRQ | STREAM1_LINE_BYTE_IRQ | STREAM1_TIMER_IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM0_LINE_CNT_ERROR_IRQ | STREAM0_FRAME_MISMATCH_IRQ | STREAM0_FRAME_COUNT_ERROR_IRQ | STREAM0_FCC_STOP_IRQ | STREAM0_FCC_START_IRQ | STREAM0_FRAME_IRQ | STREAM0_LINE_BYTE_IRQ | STREAM0_TIMER_IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-63. CSI_RX_IF_VBUS2APB_MONITOR_IRQS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|-------|-------|---|
| 31 | STREAM3_LINE_CNT_ERROR_IRQ | R/W1C | 0h | Stream 3 Line count error interrupt |
| 30 | STREAM3_FRAME_MISMATCH_IRQ | R/W1C | 0h | Stream 3 Frame mismatch error interrupt |
| 29 | STREAM3_FRAME_COUNT_ERROR_IRQ | R/W1C | 0h | Stream 3 Frame count error interrupt |
| 28 | STREAM3_FCC_STOP_IRQ | R/W1C | 0h | Stream 3 FCC stop interrupt |
| 27 | STREAM3_FCC_START_IRQ | R/W1C | 0h | Stream 3 FCC start interrupt |
| 26 | STREAM3_FRAME_IRQ | R/W1C | 0h | Stream 3 Frame interrupt |
| 25 | STREAM3_LINE_BYTE_IRQ | R/W1C | 0h | Stream 3 Line/byte interrupt |
| 24 | STREAM3_TIMER_IRQ | R/W1C | 0h | Stream 3 Timer interrupt |
| 23 | STREAM2_LINE_CNT_ERROR_IRQ | R/W1C | 0h | Stream 2 Line count error interrupt |

Table 9-63. CSI_RX_IF_VBUS2APB_MONITOR_IRQS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|-------|-------|---|
| 22 | STREAM2_FRAME_MISMATCH_IRQ | R/W1C | 0h | Stream 2 Frame mismatch error interrupt |
| 21 | STREAM2_FRAME_COUNT_ERROR_IRQ | R/W1C | 0h | Stream 2 Frame count error interrupt |
| 20 | STREAM2_FCC_STOP_IRQ | R/W1C | 0h | Stream 2 FCC stop interrupt |
| 19 | STREAM2_FCC_START_IRQ | R/W1C | 0h | Stream 2 FCC start interrupt |
| 18 | STREAM2_FRAME_IRQ | R/W1C | 0h | Stream 2 Frame interrupt |
| 17 | STREAM2_LB_IRQ | R/W1C | 0h | Stream 2 Line/byte interrupt |
| 16 | STREAM2_TIMER_IRQ | R/W1C | 0h | Stream 2 Timer interrupt |
| 15 | STREAM1_LINE_COUNT_ERROR_IRQ | R/W1C | 0h | Stream 1 Line count error interrupt |
| 14 | STREAM1_FRAME_MISMATCH_IRQ | R/W1C | 0h | Stream 1 Frame mismatch error interrupt |
| 13 | STREAM1_FRAME_COUNT_ERROR_IRQ | R/W1C | 0h | Stream 1 Frame count error interrupt |
| 12 | STREAM1_FCC_STOP_IRQ | R/W1C | 0h | Stream 1 FCC stop interrupt |
| 11 | STREAM1_FCC_START_IRQ | R/W1C | 0h | Stream 1 FCC start interrupt |
| 10 | STREAM1_FRAME_IRQ | R/W1C | 0h | Stream 1 Frame interrupt |
| 9 | STREAM1_LB_IRQ | R/W1C | 0h | Stream 1 Line/byte interrupt |
| 8 | STREAM1_TIMER_IRQ | R/W1C | 0h | Stream 1 Timer interrupt |
| 7 | STREAM0_LINE_COUNT_ERROR_IRQ | R/W1C | 0h | Stream 0 Line count error interrupt |
| 6 | STREAM0_FRAME_MISMATCH_IRQ | R/W1C | 0h | Stream 0 Frame mismatch error interrupt |
| 5 | STREAM0_FRAME_COUNT_ERROR_IRQ | R/W1C | 0h | Stream 0 Frame count error interrupt |
| 4 | STREAM0_FCC_STOP_IRQ | R/W1C | 0h | Stream 0 FCC stop interrupt |
| 3 | STREAM0_FCC_START_IRQ | R/W1C | 0h | Stream 0 FCC start interrupt |
| 2 | STREAM0_FRAME_IRQ | R/W1C | 0h | Stream 0 Frame interrupt |
| 1 | STREAM0_LB_IRQ | R/W1C | 0h | Stream 0 Line/byte interrupt |
| 0 | STREAM0_TIMER_IRQ | R/W1C | 0h | Stream 0 Timer interrupt |

9.32 CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG Register (Offset = 1Ch) [reset = 0h]

CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG is shown in [Figure 9-29](#) and described in [Table 9-65](#).

Return to [Summary Table](#).

Monitor interrupt mask. Bit addressable mask register in order to independently enable each event to trigger the monitor_irq line. Only events whose corresponding bit is set to 1 can trigger the interruption line.

Hard reset is 0x00000000, i.e. interrupt line disabled

Table 9-64.
CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 401Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 401Ch |

Figure 9-29. CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|-----------------------------|--------------------------------|-----------------------|------------------------|--------------------|------------------------|--------------------|
| STREAM3_LINE_CNT_ERROR_IRQM | STREAM3_FRAME_MISMATCH_IRQM | STREAM3_FRAME_COUNT_ERROR_IRQM | STREAM3_FCC_STOP_IRQM | STREAM3_FCC_START_IRQM | STREAM3_FRAME_IRQM | STREAM3_LINE_BYTE_IRQM | STREAM3_TIMER_IRQM |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STREAM2_LINE_CNT_ERROR_IRQM | STREAM2_FRAME_MISMATCH_IRQM | STREAM2_FRAME_COUNT_ERROR_IRQM | STREAM2_FCC_STOP_IRQM | STREAM2_FCC_START_IRQM | STREAM2_FRAME_IRQM | STREAM2_LINE_BYTE_IRQM | STREAM2_TIMER_IRQM |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| STREAM1_LINE_CNT_ERROR_IRQM | STREAM1_FRAME_MISMATCH_IRQM | STREAM1_FRAME_COUNT_ERROR_IRQM | STREAM1_FCC_STOP_IRQM | STREAM1_FCC_START_IRQM | STREAM1_FRAME_IRQM | STREAM1_LINE_BYTE_IRQM | STREAM1_TIMER_IRQM |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM0_LINE_CNT_ERROR_IRQM | STREAM0_FRAME_MISMATCH_IRQM | STREAM0_FRAME_COUNT_ERROR_IRQM | STREAM0_FCC_STOP_IRQM | STREAM0_FCC_START_IRQM | STREAM0_FRAME_IRQM | STREAM0_LINE_BYTE_IRQM | STREAM0_TIMER_IRQM |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-65. CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------|------|-------|---|
| 31 | STREAM3_LINE_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 3 Line count error. |
| 30 | STREAM3_FRAME_MISMATCH_IRQM | R/W | 0h | Interrupt mask for stream 3 Frame mismatch error. |
| 29 | STREAM3_FRAME_COUNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 3 Frame count error. |
| 28 | STREAM3_FCC_STOP_IRQM | R/W | 0h | Interrupt mask for stream 3 FCC stop. |
| 27 | STREAM3_FCC_START_IRQM | R/W | 0h | Interrupt mask for stream 3 FCC start. |
| 26 | STREAM3_FRAME_IRQM | R/W | 0h | Interrupt mask for stream 3 Frame. |
| 25 | STREAM3_LINE_BYTE_IRQM | R/W | 0h | Interrupt mask for stream 3 Line/byte. |

Table 9-65. CSI_RX_IF_VBUS2APB_MONITOR_IRQS_MASK_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|---|
| 24 | STREAM3_TIMER_IRQM | R/W | 0h | Interrupt mask stream 3 Timer |
| 23 | STREAM2_LINE_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 2 Line count error. |
| 22 | STREAM2_FRAME_MISMATCH_IRQM | R/W | 0h | Interrupt mask for stream 2 Frame mismatch error. |
| 21 | STREAM2_FRAME_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 2 Frame count error. |
| 20 | STREAM2_FCC_STOP_IRQM | R/W | 0h | Interrupt mask for stream 2 FCC stop. |
| 19 | STREAM2_FCC_START_IRQM | R/W | 0h | Interrupt mask for stream 2 FCC start. |
| 18 | STREAM2_FRAME_IRQM | R/W | 0h | Interrupt mask for stream 2 Frame. |
| 17 | STREAM2_LB_IRQM | R/W | 0h | Interrupt mask for stream 2 Line/byte. |
| 16 | STREAM2_TIMER_IRQM | R/W | 0h | Interrupt mask stream 2 Timer |
| 15 | STREAM1_LINE_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 1 Line count error. |
| 14 | STREAM1_FRAME_MISMATCH_IRQM | R/W | 0h | Interrupt mask for stream 1 Frame mismatch error. |
| 13 | STREAM1_FRAME_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 1 Frame count error. |
| 12 | STREAM1_FCC_STOP_IRQM | R/W | 0h | Interrupt mask for stream 1 FCC stop. |
| 11 | STREAM1_FCC_START_IRQM | R/W | 0h | Interrupt mask for stream 1 FCC start. |
| 10 | STREAM1_FRAME_IRQM | R/W | 0h | Interrupt mask for stream 1 Frame. |
| 9 | STREAM1_LB_IRQM | R/W | 0h | Interrupt mask for stream 1 Line/byte. |
| 8 | STREAM1_TIMER_IRQM | R/W | 0h | Interrupt mask stream 1 Timer |
| 7 | STREAM0_LINE_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 0 Line count error. |
| 6 | STREAM0_FRAME_MISMATCH_IRQM | R/W | 0h | Interrupt mask for stream 0 Frame mismatch error. |
| 5 | STREAM0_FRAME_CNT_ERROR_IRQM | R/W | 0h | Interrupt mask for stream 0 Frame count error. |
| 4 | STREAM0_FCC_STOP_IRQM | R/W | 0h | Interrupt mask for stream 0 FCC stop. |
| 3 | STREAM0_FCC_START_IRQM | R/W | 0h | Interrupt mask for stream 0 FCC start. |
| 2 | STREAM0_FRAME_IRQM | R/W | 0h | Interrupt mask for stream 0 Frame. |
| 1 | STREAM0_LB_IRQM | R/W | 0h | Interrupt mask for stream 0 Line/byte. |
| 0 | STREAM0_TIMER_IRQM | R/W | 0h | Interrupt mask stream 0 Timer |

9.33 CSI_RX_IF_VBUS2APB_INFO_IRQS Register (Offset = 20h) [reset = X]

CSI_RX_IF_VBUS2APB_INFO_IRQS is shown in [Figure 9-30](#) and described in [Table 9-67](#).

Return to [Summary Table](#).

Information type Interrupt status (non-error conditions)

**Table 9-66. CSI_RX_IF_VBUS2APB_INFO_IRQS
Instances**

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4020h |
| CSI_RX_IF_VBUS2APB1 | 0451 4020h |

Figure 9-30. CSI_RX_IF_VBUS2APB_INFO_IRQS Register

| | | | | | | | |
|------------------|---------------------|------------------|------------------------|------------------|-------------------|------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | STREAM3_ABORT_IRQ | STREAM3_STOP_IRQ | STREAM2_ABORT_IRQ | STREAM2_STOP_IRQ | STREAM1_ABORT_IRQ | STREAM1_STOP_IRQ | STREAM0_ABORT_IRQ |
| R/W-X | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM0_STOP_IRQ | SP_GENERIC_RCVD_IRQ | DESKEW_ENTRY_IRQ | ECC_SPARES_NONZERO_IRQ | WAKEUP_IRQ | SLEEP_IRQ | LP_RCVD_IRQ | SP_RCVD_IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-67. CSI_RX_IF_VBUS2APB_INFO_IRQS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|-------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | STREAM3_ABORT_IRQ | R/W1C | 0h | Stream 3 Abort process complete. Apply a Soft reset before re-enabling the stream. |
| 13 | STREAM3_STOP_IRQ | R/W1C | 0h | Stream 3 Stop process complete. Apply a Soft reset before re-enabling the stream. |
| 12 | STREAM2_ABORT_IRQ | R/W1C | 0h | Stream 2 Abort process complete. Apply a Soft reset before re-enabling the stream. |
| 11 | STREAM2_STOP_IRQ | R/W1C | 0h | Stream 2 Stop process complete. Apply a Soft reset before re-enabling the stream. |
| 10 | STREAM1_ABORT_IRQ | R/W1C | 0h | Stream 1 Abort process complete. Apply a Soft reset before re-enabling the stream. |
| 9 | STREAM1_STOP_IRQ | R/W1C | 0h | Stream 1 Stop process complete. Apply a Soft reset before re-enabling the stream. |
| 8 | STREAM0_ABORT_IRQ | R/W1C | 0h | Stream 0 Abort process complete. Apply a Soft reset before re-enabling the stream. |
| 7 | STREAM0_STOP_IRQ | R/W1C | 0h | Stream 0 Stop process complete. Apply a Soft reset before re-enabling the stream. |

Table 9-67. CSI_RX_IF_VBUS2APB_INFO_IRQS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------|-------|-------|---|
| 6 | SP_GENERIC_RCVD_IRQ | R/W1C | 0h | A generic short packet has been received. |
| 5 | DESKEW_ENTRY_IRQ | R/W1C | 0h | Either clock or any datalane has entered deskew |
| 4 | ECC_SPARES_NONZERO_IRQ | R/W1C | 0h | Bits 7:6 of the ECC byte are non-zero. Indicates non compliance with the MIPI specification although the core will continue to operate as normal. |
| 3 | WAKEUP_IRQ | R/W1C | 0h | Wake-up interrupt. |
| 2 | SLEEP_IRQ | R/W1C | 0h | Sleep interrupt. |
| 1 | LP_RCVD_IRQ | R/W1C | 0h | Long Packet received by the protocol module |
| 0 | SP_RCVD_IRQ | R/W1C | 0h | Short Packet received by the protocol module |

9.34 CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG Register (Offset = 24h) [reset = X]

CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG is shown in [Figure 9-31](#) and described in [Table 9-69](#).

Return to [Summary Table](#).

Information interrupt mask. Bit addressable mask register in order to independently enable each event to trigger the info_irq line. Only events whose corresponding bit is set to 1 can trigger the interruption line.

Hard reset is 0x00000000, i.e. interrupt line disabled

Table 9-68.
CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4024h |
| CSI_RX_IF_VBUS2APB1 | 0451 4024h |

Figure 9-31. CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG Register

| | | | | | | | |
|-------------------|----------------------|-------------------|-------------------------|-------------------|--------------------|-------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | STREAM3_ABORT_IRQM | STREAM3_STOP_IRQM | STREAM2_ABORT_IRQM | STREAM2_STOP_IRQM | STREAM1_ABORT_IRQM | STREAM1_STOP_IRQM | STREAM0_ABORT_IRQM |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM0_STOP_IRQM | SP_GENERIC_RCVD_IRQM | DESKEW_ENTRY_IRQM | ECC_SPARES_NONZERO_IRQM | WAKEUP_IRQM | SLEEP_IRQM | LP_RCVD_IRQM | SP_RCVD_IRQM |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-69. CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-15 | RESERVED | R/W | X | |
| 14 | STREAM3_ABORT_IRQM | R/W | 0h | Interrupt mask for stream 3 Abort process. |
| 13 | STREAM3_STOP_IRQM | R/W | 0h | Interrupt mask for Stream 3 Stop process complete. |
| 12 | STREAM2_ABORT_IRQM | R/W | 0h | Interrupt mask for stream 2 Abort process. |
| 11 | STREAM2_STOP_IRQM | R/W | 0h | Interrupt mask for Stream 2 Stop process complete. |
| 10 | STREAM1_ABORT_IRQM | R/W | 0h | Interrupt mask for stream 1 Abort process. |
| 9 | STREAM1_STOP_IRQM | R/W | 0h | Interrupt mask for Stream 1 Stop process complete. |
| 8 | STREAM0_ABORT_IRQM | R/W | 0h | Interrupt mask for stream 0 Abort process. |
| 7 | STREAM0_STOP_IRQM | R/W | 0h | Interrupt mask for Stream 0 Stop process complete. |
| 6 | SP_GENERIC_RCVD_IRQM | R/W | 0h | Interrupt mask for Generic Short Packet received |
| 5 | DESKEW_ENTRY_IRQM | R/W | 0h | Interrupt mask for Deskew entry check |

Table 9-69. CSI_RX_IF_VBUS2APB_INFO_IRQS_MASK_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 4 | ECC_SPARES_NONZERO_IRQM | R/W | 0h | Interrupt mask for ECC spares check |
| 3 | WAKEUP_IRQM | R/W | 0h | Interrupt mask for Wake-up interrupt. |
| 2 | SLEEP_IRQM | R/W | 0h | Interrupt mask for Sleep interrupt. |
| 1 | LP_RCVD_IRQM | R/W | 0h | Interrupt mask for Long Packet received flag |
| 0 | SP_RCVD_IRQM | R/W | 0h | Interrupt mask for Short Packet received |

9.35 CSI_RX_IF_VBUS2APB_ERROR_IRQS Register (Offset = 28h) [reset = X]

CSI_RX_IF_VBUS2APB_ERROR_IRQS is shown in [Figure 9-32](#) and described in [Table 9-71](#).

Return to [Summary Table](#).

Datapath error interrupt status.

Provides information about data path errors.

The host processor can read the interrupt status register to identify the root cause of the event, typically after that the csi2rx_err_irq interrupt line is raised

**Table 9-70. CSI_RX_IF_VBUS2APB_ERROR_IRQS
Instances**

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4028h |
| CSI_RX_IF_VBUS2APB1 | 0451 4028h |

Figure 9-32. CSI_RX_IF_VBUS2APB_ERROR_IRQS Register

| | | | | | | | |
|-------------|--------------------------|----------------|---------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | STREAM3_FIFO_OVERFLOW_IRQ | STREAM2_FIFO_OVERFLOW_IRQ | STREAM1_FIFO_OVERFLOW_IRQ | STREAM0_FIFO_OVERFLOW_IRQ |
| R/W-X | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | FRONT_TRUNC_HDR_IRQ | PROT_TRUNCATED_PACKET_IRQ | FRONT_LP_NO_PAYLOAD_IRQ | SP_INVALID_R_CVD_IRQ | INVALID_ACCESS_IRQ |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA_ID_IRQ | HEADER_CORRECTED_ECC_IRQ | HEADER_ECC_IRQ | PAYLOAD_CRC_IRQ | RESERVED | | | FRONT_FIFO_OVERFLOW_IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W-X | | | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-71. CSI_RX_IF_VBUS2APB_ERROR_IRQS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|-------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19 | STREAM3_FIFO_OVERFLOW_IRQ | R/W1C | 0h | Overflow of the Stream FIFO detected: stream_fifo_overflow[19] -> Stream 3 overflow |
| 18 | STREAM2_FIFO_OVERFLOW_IRQ | R/W1C | 0h | Overflow of the Stream FIFO detected: stream_fifo_overflow[18] -> Stream 2 overflow |
| 17 | STREAM1_FIFO_OVERFLOW_IRQ | R/W1C | 0h | Overflow of the Stream FIFO detected: stream_fifo_overflow[17] -> Stream 1 overflow |
| 16 | STREAM0_FIFO_OVERFLOW_IRQ | R/W1C | 0h | Overflow of the Stream FIFO detected: stream_fifo_overflow[16] -> Stream 0 overflow |
| 15-13 | RESERVED | R/W | X | |
| 12 | FRONT_TRUNC_HDR_IRQ | R/W1C | 0h | A truncated header [short or Long] has been received |

Table 9-71. CSI_RX_IF_VBUS2APB_ERROR_IRQS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|-------|-------|--|
| 11 | PROT_TRUNCATED_PACKET_IRQ | R/W1C | 0h | A truncated Long packet has been received. Too few/many bytes |
| 10 | FRONT_LP_NO_PAYLOAD_IRQ | R/W1C | 0h | A truncated Long packet has been received. No payload |
| 9 | SP_INVALID_RCVD_IRQ | R/W1C | 0h | A reserved or invalid short packet has been received |
| 8 | INVALID_ACCESS_IRQ | R/W1C | 0h | Invalid access to the configuration register space. |
| 7 | DATA_ID_IRQ | R/W1C | 0h | Data ID error has been detected in the header packet |
| 6 | HEADER_CORRECTED_ECC_IRQ | R/W1C | 0h | ECC error has been detected and corrected. |
| 5 | HEADER_ECC_IRQ | R/W1C | 0h | Unrecoverable ECC error has been detected. |
| 4 | PAYLOAD_CRC_IRQ | R/W1C | 0h | CRC error has been detected. |
| 3-1 | RESERVED | R/W | X | |
| 0 | FRONT_FIFO_OVERFLOW_IRQ | R/W1C | 0h | Overflow detected in resynchronization FIFO between DPHY Lane Management and Protocol blocks. This will occur if sys_clk is not fast enough and should be increased since the byte clock frequency is fixed |

9.36 CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG Register (Offset = 2Ch) [reset = X]

CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG is shown in [Figure 9-33](#) and described in [Table 9-73](#).

Return to [Summary Table](#).

Datapath error interrupt enable Bits. This register is used to independently enable each event to trigger the err_irq interrupt line. Only events whose corresponding enable bit is set to 1 can trigger the interrupt line.

Hard reset is 0x0000000, i.e. all interrupt lines are disabled

Table 9-72.
CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 402Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 402Ch |

Figure 9-33. CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG Register

| | | | | | | | |
|--------------|---------------------------|-----------------|----------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | STREAM3_FIFO_OVERFLOW_IRQM | STREAM2_FIFO_OVERFLOW_IRQM | STREAM1_FIFO_OVERFLOW_IRQM | STREAM0_FIFO_OVERFLOW_IRQM |
| R/W-X | | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | FRONT_TRUNC_HDR_IRQM | PROT_TRUNCATED_PACKET_IRQM | FRONT_LP_N_O_PAYLOAD_IRQM | SP_INVALID_R_CVD_IRQM | INVALID_ACCESS_IRQM |
| R/W-X | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA_ID_IRQM | HEADER_CORRECTED_ECC_IRQM | HEADER_ECC_IRQM | PAYLOAD_CRC_IRQM | RESERVED | | | FRONT_FIFO_OVERFLOW_IRQM |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-73. CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-20 | RESERVED | R/W | X | |
| 19 | STREAM3_FIFO_OVERFLOW_IRQM | R/W | 0h | Interrupt enable bit for: stream_fifo_overflow[19] -> Stream 3 overflow |
| 18 | STREAM2_FIFO_OVERFLOW_IRQM | R/W | 0h | Interrupt enable bit for: stream_fifo_overflow[18] -> Stream 2 overflow |
| 17 | STREAM1_FIFO_OVERFLOW_IRQM | R/W | 0h | Interrupt enable bit for: stream_fifo_overflow[17] -> Stream 1 overflow |
| 16 | STREAM0_FIFO_OVERFLOW_IRQM | R/W | 0h | Interrupt enable bit for: stream_fifo_overflow[16] -> Stream 0 overflow |
| 15-13 | RESERVED | R/W | X | |
| 12 | FRONT_TRUNC_HDR_IRQM | R/W | 0h | Interrupt enable bit for truncated hdr. |

Table 9-73. CSI_RX_IF_VBUS2APB_ERROR_IRQS_MASK_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 11 | PROT_TRUNCATED_PACKET_IRQM | R/W | 0h | Interrupt enable bit for long packet payload with too many/few bytes |
| 10 | FRONT_LP_NO_PAYLOAD_IRQM | R/W | 0h | Interrupt enable bit for long packet header received with no payload |
| 9 | SP_INVALID_RCVD_IRQM | R/W | 0h | Interrupt enable bit for invalid short packet |
| 8 | INVALID_ACCESS_IRQM | R/W | 0h | Interrupt enable bit for error_irqs_invalid_access. |
| 7 | DATA_ID_IRQM | R/W | 0h | Interrupt enable bit for error_irqs_data_id |
| 6 | HEADER_CORRECTED_ECC_IRQM | R/W | 0h | Interrupt enable bit for error_irqs_header_corrected_ecc |
| 5 | HEADER_ECC_IRQM | R/W | 0h | Interrupt enable bit for error_irqs_header_ecc |
| 4 | PAYLOAD_CRC_IRQM | R/W | 0h | Interrupt enable bit for error_irqs_payload_crc |
| 3-1 | RESERVED | R/W | X | |
| 0 | FRONT_FIFO_OVERFLOW_IRQM | R/W | 0h | Interrupt enable bit for error_irqs_front_fifo_overflow |

9.37 CSI_RX_IF_VBUS2APB_DPHY_LANE_CONTROL Register (Offset = 40h) [reset = X]

CSI_RX_IF_VBUS2APB_DPHY_LANE_CONTROL is shown in [Figure 9-34](#) and described in [Table 9-75](#).

Return to [Summary Table](#).

DPHY lane control for data and clock lanes enables and resets

Table 9-74.
CSI_RX_IF_VBUS2APB_DPHY_LANE_CONTROL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4040h |
| CSI_RX_IF_VBUS2APB1 | 0451 4040h |

Figure 9-34. CSI_RX_IF_VBUS2APB_DPHY_LANE_CONTROL Register

| | | | | | | | |
|-----------|-----------|-----------|-----------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | CL_RESET |
| R/W-X | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_RESET | DL2_RESET | DL1_RESET | DL0_RESET | RESERVED | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CL_ENABLE | DL3_ENABLE | DL2_ENABLE | DL1_ENABLE | DL0_ENABLE |
| R/W-X | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-75. CSI_RX_IF_VBUS2APB_DPHY_LANE_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|-------------------------|
| 31-17 | RESERVED | R/W | X | |
| 16 | CL_RESET | R/W | 0h | DPHY Clock lane Reset |
| 15 | DL3_RESET | R/W | 0h | DPHY data lane 3 Reset |
| 14 | DL2_RESET | R/W | 0h | DPHY data lane 2 Reset |
| 13 | DL1_RESET | R/W | 0h | DPHY data lane 1 Reset |
| 12 | DL0_RESET | R/W | 0h | DPHY data lane 0 Reset |
| 11-5 | RESERVED | R/W | X | |
| 4 | CL_ENABLE | R/W | 0h | DPHY Clock lane Enable |
| 3 | DL3_ENABLE | R/W | 0h | DPHY data lane 3 Enable |
| 2 | DL2_ENABLE | R/W | 0h | DPHY data lane 2 Enable |
| 1 | DL1_ENABLE | R/W | 0h | DPHY data lane 1 Enable |
| 0 | DL0_ENABLE | R/W | 0h | DPHY data lane 0 Enable |

9.38 CSI_RX_IF_VBUS2APB_DPHY_STATUS Register (Offset = 48h) [reset = X]

CSI_RX_IF_VBUS2APB_DPHY_STATUS is shown in [Figure 9-35](#) and described in [Table 9-77](#).

Return to [Summary Table](#).

DPHY Clock and Data Lane mode status

Table 9-76. CSI_RX_IF_VBUS2APB_DPHY_STATUS Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4048h |
| CSI_RX_IF_VBUS2APB1 | 0451 4048h |

Figure 9-35. CSI_RX_IF_VBUS2APB_DPHY_STATUS Register

| | | | | | | | |
|----------|-------------------|-----------------------|-------------------|----------|---------------------|-----------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | DL3_RXULPSE SC | DL3_ULPSACT IVENOT | DL3_STOPSTA TE | RESERVED | DL2_RXULPSE SC | DL2_ULPSACT IVENOT | DL2_STOPSTA TE |
| R-X | R-0h | R-0h | R-0h | R-X | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | DL1_RXULPSE SC | DL1_ULPSACT IVENOT | DL1_STOPSTA TE | RESERVED | DL0_RXULPSE SC | DL0_ULPSACT IVENOT | DL0_STOPSTA TE |
| R-X | R-0h | R-0h | R-0h | R-X | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | CL_RXULPSC LKNOT | CL_ULPSACTI VENOT | CL_STOPSTAT E |
| R-X | | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 9-77. CSI_RX_IF_VBUS2APB_DPHY_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--------------------------------|
| 31-23 | RESERVED | R | X | |
| 22 | DL3_RXULPSESC | R | 0h | DPHY Data lane 3 ULPS Esc |
| 21 | DL3_ULPSACTIVENOT | R | 0h | DPHY Data lane 3 ULPSActiveNot |
| 20 | DL3_STOPSTATE | R | X | DPHY Data lane 3 Stop State |
| 19 | RESERVED | R | X | |
| 18 | DL2_RXULPSESC | R | 0h | DPHY Data lane 2 ULPS Esc |
| 17 | DL2_ULPSACTIVENOT | R | 0h | DPHY Data lane 2 ULPSActiveNot |
| 16 | DL2_STOPSTATE | R | X | DPHY Data lane 2 Stop State |
| 15 | RESERVED | R | X | |
| 14 | DL1_RXULPSESC | R | 0h | DPHY Data lane 1 ULPS Esc |
| 13 | DL1_ULPSACTIVENOT | R | 0h | DPHY Data lane 1 ULPSActiveNot |
| 12 | DL1_STOPSTATE | R | X | DPHY Data lane 1 Stop State |
| 11 | RESERVED | R | X | |
| 10 | DL0_RXULPSESC | R | 0h | DPHY Data lane 0 ULPS Esc |
| 9 | DL0_ULPSACTIVENOT | R | 0h | DPHY Data lane 0 ULPSActiveNot |
| 8 | DL0_STOPSTATE | R | X | DPHY Data lane 0 Stop State |

Table 9-77. CSI_RX_IF_VBUS2APB_DPHY_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|-------------------------------|
| 7-3 | RESERVED | R | X | |
| 2 | CL_RXULPSClkNOT | R | 0h | DPHY Clock lane RxULPSClkNot |
| 1 | CL_ULPSACTIVENOT | R | 0h | DPHY Clock lane ULPSActiveNot |
| 0 | CL_STOPSTATE | R | X | DPHY Clock lane Stop State |

9.39 CSI_RX_IF_VBUS2APB_DPHY_ERR_STATUS_IRQ Register (Offset = 4Ch) [reset = X]

CSI_RX_IF_VBUS2APB_DPHY_ERR_STATUS_IRQ is shown in [Figure 9-36](#) and described in [Table 9-79](#).

Return to [Summary Table](#).

DPHY error interrupt status

Table 9-78.
CSI_RX_IF_VBUS2APB_DPHY_ERR_STATUS_IRQ
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 404Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 404Ch |

Figure 9-36. CSI_RX_IF_VBUS2APB_DPHY_ERR_STATUS_IRQ Register

| | | | | | | | |
|----------|----|----|----------------------|----------|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | DL3_ERRSOT HS_IRQ | RESERVED | | | DL2_ERRSOT HS_IRQ |
| R/W-X | | | R/W1C-0h | R/W-X | | | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | DL1_ERRSOT HS_IRQ | RESERVED | | | DL0_ERRSOT HS_IRQ |
| R/W-X | | | R/W1C-0h | R/W-X | | | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-79. CSI_RX_IF_VBUS2APB_DPHY_ERR_STATUS_IRQ Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|---------------------------|
| 31-21 | RESERVED | R/W | X | |
| 20 | DL3_ERRSOTHS_IRQ | R/W1C | 0h | DPHY Data lane 3 ErrSotHS |
| 19-17 | RESERVED | R/W | X | |
| 16 | DL2_ERRSOTHS_IRQ | R/W1C | 0h | DPHY Data lane 2 ErrSotHS |
| 15-13 | RESERVED | R/W | X | |
| 12 | DL1_ERRSOTHS_IRQ | R/W1C | 0h | DPHY Data lane 1 ErrSotHS |
| 11-9 | RESERVED | R/W | X | |
| 8 | DL0_ERRSOTHS_IRQ | R/W1C | 0h | DPHY Data lane 0 ErrSotHS |
| 7-0 | RESERVED | R/W | X | |

9.40 CSI_RX_IF_VBUS2APB_DPHY_ERR_IRQ_MASK_CFG Register (Offset = 50h) [reset = X]

CSI_RX_IF_VBUS2APB_DPHY_ERR_IRQ_MASK_CFG is shown in [Figure 9-37](#) and described in [Table 9-81](#).

[Return to Summary Table.](#)

DPHY error interrupt status

Table 9-80.
CSI_RX_IF_VBUS2APB_DPHY_ERR_IRQ_MASK_CFG
G Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4050h |
| CSI_RX_IF_VBUS2APB1 | 0451 4050h |

Figure 9-37. CSI_RX_IF_VBUS2APB_DPHY_ERR_IRQ_MASK_CFG Register

| | | | | | | | |
|----------|----|----|-----------------------|----------|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | DL3_ERRSOT HS_IRQM | RESERVED | | | DL2_ERRSOT HS_IRQM |
| R/W-X | | | R/W-0h | R/W-X | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | DL1_ERRSOT HS_IRQM | RESERVED | | | DL0_ERRSOT HS_IRQM |
| R/W-X | | | R/W-0h | R/W-X | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-81. CSI_RX_IF_VBUS2APB_DPHY_ERR_IRQ_MASK_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--------------------------------|
| 31-21 | RESERVED | R/W | X | |
| 20 | DL3_ERRSOTHS_IRQM | R/W | 0h | DPHY Data lane 3 ErrSotHS mask |
| 19-17 | RESERVED | R/W | X | |
| 16 | DL2_ERRSOTHS_IRQM | R/W | 0h | DPHY Data lane 2 ErrSotHS mask |
| 15-13 | RESERVED | R/W | X | |
| 12 | DL1_ERRSOTHS_IRQM | R/W | 0h | DPHY Data lane 1 ErrSotHS mask |
| 11-9 | RESERVED | R/W | X | |
| 8 | DL0_ERRSOTHS_IRQM | R/W | 0h | DPHY Data lane 0 ErrSotHS mask |
| 7-0 | RESERVED | R/W | X | |

9.41 CSI_RX_IF_VBUS2APB_INTEGRATION_DEBUG Register (Offset = 60h) [reset = X]

CSI_RX_IF_VBUS2APB_INTEGRATION_DEBUG is shown in [Figure 9-38](#) and described in [Table 9-83](#).

Return to [Summary Table](#).

Used to observe the current data field, extracted by the protocol block from the last short packet data field and FSM state.

FSM states are one-hot.

It also indicates what data type and virtual channels were used for that short packet.

This is primarily used during error condition debug.

Since the data can come from asynchronous domains the data coherency cannot be relied upon.

Table 9-82.
CSI_RX_IF_VBUS2APB_INTEGRATION_DEBUG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4060h |
| CSI_RX_IF_VBUS2APB1 | 0451 4060h |

Figure 9-38. CSI_RX_IF_VBUS2APB_INTEGRATION_DEBUG Register

| | | | | | | | |
|-----------------|----|---------|----|----------|----|---------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PROT_FSM_STATE | | | | RESERVED | | PROT_VC | |
| R-0h | | | | R-X | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PROT_VC | | PROT_DT | | | | | |
| R-0h | | R-0h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PROT_WORD_COUNT | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PROT_WORD_COUNT | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-83. CSI_RX_IF_VBUS2APB_INTEGRATION_DEBUG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-28 | PROT_FSM_STATE | R | X | csi2rx_fsm_state 0x 1: WAIT_FOR_PACKET 0x 2: PAYLOAD_DATA 0x 4: PACKET_FOOTER_CHECK |
| 27-26 | RESERVED | R | X | |
| 25-22 | PROT_VC | R | 0h | Protocol Virtual Channel |
| 21-16 | PROT_DT | R | 0h | Protocol Datatype |
| 15-0 | PROT_WORD_COUNT | R | 0h | Protocol Word Count [Data Field] |

9.42 CSI_RX_IF_VBUS2APB_ERROR_DEBUG Register (Offset = 74h) [reset = X]

CSI_RX_IF_VBUS2APB_ERROR_DEBUG is shown in [Figure 9-39](#) and described in [Table 9-85](#).

Return to [Summary Table](#).

Error condition debug. After an error is detected by the CSI2RX, this register indicates which virtual channel, datatype and data field is impacted.

Table 9-84. CSI_RX_IF_VBUS2APB_ERROR_DEBUG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4074h |
| CSI_RX_IF_VBUS2APB1 | 0451 4074h |

Figure 9-39. CSI_RX_IF_VBUS2APB_ERROR_DEBUG Register

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|------|----|----|----|------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_FIELD | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | VC | | | | DT | | | | | |
| R-X | | | | | | R-0h | | | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-85. CSI_RX_IF_VBUS2APB_ERROR_DEBUG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | DATA_FIELD | R | 0h | Indicates the Data Field for an invalid CRC/ECC/Data ID |
| 15-10 | RESERVED | R | X | |
| 9-6 | VC | R | 0h | Indicates the Virtual Channel for a invalid CRC/ECC/Data ID |
| 5-0 | DT | R | 0h | Indicates the Data Type for a invalid CRC/ECC/Data ID |

9.43 CSI_RX_IF_VBUS2APB_TEST_GENERIC Register (Offset = 80h) [reset = 0h]

CSI_RX_IF_VBUS2APB_TEST_GENERIC is shown in [Figure 9-40](#) and described in [Table 9-87](#).

Return to [Summary Table](#).

Generic test control and status register that controls and reads primary I/O.

Table 9-86. CSI_RX_IF_VBUS2APB_TEST_GENERIC Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4080h |
| CSI_RX_IF_VBUS2APB1 | 0451 4080h |

Figure 9-40. CSI_RX_IF_VBUS2APB_TEST_GENERIC Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STATUS | | | | | | | | | | | | | | | | CTRL | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-87. CSI_RX_IF_VBUS2APB_TEST_GENERIC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 31-16 | STATUS | R | 0h | Test status - Directly reflects, after resynchronisation into the pclk domain, the state of 'test_generic_status' primary inputs. |
| 15-0 | CTRL | R/W | 0h | Test control - Directly controls primary outputs 'test_generic_ctrl' |

9.44 CSI_RX_IF_VBUS2APB_STREAM0_CTRL Register (Offset = 100h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_CTRL is shown in [Figure 9-41](#) and described in [Table 9-89](#).

Return to [Summary Table](#).

CSI2RX Stream Data output datapath control.

Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started.

Table 9-88.
CSI_RX_IF_VBUS2APB_STREAM0_CTRL Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4100h |
| CSI_RX_IF_VBUS2APB1 | 0451 4100h |

Figure 9-41. CSI_RX_IF_VBUS2APB_STREAM0_CTRL Register

| | | | | | | | |
|----------|----|----|----------|----------|-------|------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | SOFT_RST | RESERVED | ABORT | STOP | START |
| R/W-X | | | R/W1C-0h | R/W-X | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; W = Write Only; -n = value after reset

Table 9-89. CSI_RX_IF_VBUS2APB_STREAM0_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | SOFT_RST | R/W1C | 0h | Writing 1'b1 will apply a synchronous soft reset of this stream registers/FIFO |
| 3 | RESERVED | R/W | X | |
| 2 | ABORT | W | 0h | Writing 1 this register will cause the csi2rx to stop streaming on the corresponding output immediately. This may corrupt the output protocol. stream_abort_irq is generated on completion of the abort operation. |
| 1 | STOP | W | 0h | Writing 1 in this register will cause csi2rx to stop streaming on the corresponding output at the end of the current frame. If the command is issued during frame blanking, then the datapath will immediately stop streaming data on that output. stream_stop_irq is generated on completion of the stop operation. |

Table 9-89. CSI_RX_IF_VBUS2APB_STREAM0_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | START | W | 0h | Writing 1 in this register enables the corresponding datapath output. It will start streaming data at the start of the next frame that complies with the output configuration. stream_status[31] running indicates when data stream is enabled. |

9.45 CSI_RX_IF_VBUS2APB_STREAM0_STATUS Register (Offset = 104h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_STATUS is shown in [Figure 9-42](#) and described in [Table 9-91](#).

Return to [Summary Table](#).

CSI2 Slave Controller Status. Contains useful debug information such as FSM states.

Table 9-90.
CSI_RX_IF_VBUS2APB_STREAM0_STATUS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4104h |
| CSI_RX_IF_VBUS2APB1 | 0451 4104h |

Figure 9-42. CSI_RX_IF_VBUS2APB_STREAM0_STATUS Register

| | | | | | | | |
|------------|----------|----|----|----------|----|--------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RUNNING | RESERVED | | | | | | |
| R-0h | R-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | READY_STATE |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_FSM | | | | RESERVED | | PROTOCOL_FSM | |
| R-0h | | | | R-X | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 9-91. CSI_RX_IF_VBUS2APB_STREAM0_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 31 | RUNNING | R | 0h | The Stream is enabled |
| 30-9 | RESERVED | R | X | |
| 8 | READY_STATE | R | 0h | Indicates the state of the pushback signal pixel_ready_if for this stream |

Table 9-91. CSI_RX_IF_VBUS2APB_STREAM0_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-4 | STREAM_FSM | R | 0h | Output to Stream FSM states: 0x 0: STREAM_IDLE 0x 1: STREAM_WAIT_CTRL_DATA // Expecting control data next 0x 2: STREAM_CTRL // Check contents of Ctrl packet and extract header information 0x 3: STREAM_DATA // Pixel stream pixel data unpacking 0x 4: STREAM_CONV_PIX_NB // 1st cycle delay for byte2pixel conversion 0x 5: STREAM_CONV_PIX_NB_EXT // 2nd cycle delay for byte2pixel conversion 0x 6: STREAM_DATA_START // Assert Hsync 0x 7: STREAM_DATA_END // De-assert Hsync 0x 8: STREAM_FILL_WAIT // Elastic Buffer cfg - wait until fill level is reached 0x 9: STREAM_STOP // Stop at the end of Frame - used to set irq 0xA: STREAM_WAIT_CRC // Wait until CRC check has completed - Full Line cfg 0xB: STREAM_WAIT_PKT_DONE // Wait for CRC to complete before proceeding 0xC: STREAM_PKT_DONE // Packet complete - no error conditions after this point 0xD: STREAM_NULL // NULL pkt received 0xE: STREAM_FLUSH // Flush due to CRC error |
| 3-2 | RESERVED | R | X | |
| 1-0 | PROTOCOL_FSM | R | 0h | Input to Stream FSM states: 0x 0: PROT_IDLE 0x 1: PROT_WAIT_CTRL 0x 2: PROT_CTRL 0x 3: PROT_DATA |

9.46 CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG Register (Offset = 108h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG is shown in [Figure 9-43](#) and described in [Table 9-93](#).

Return to [Summary Table](#).

Secondary CSI2 Slave Controller Data outputs configuration.
This register is used to configure the data types and virtual channels
are processed and output by this stream.

Table 9-92.
CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4108h |
| CSI_RX_IF_VBUS2APB1 | 0451 4108h |

Figure 9-43. CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG Register

| | | | | | | | |
|------------|----------|------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ENABLE_DT1 | RESERVED | DATATYPE_SELECT1 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENABLE_DT0 | RESERVED | DATATYPE_SELECT0 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-93. CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | VC_SELECT | R/W | 0h | Selection of Virtual Channels to be processed: Default '0' -> All Virtual Channels are processed vc_select0[16] -> Virtual Channel Select 0 is processed vc_select1[17] -> Virtual Channel Select 1 is processed vc_select2[18] -> Virtual Channel Select 2 is processed vc_select3[19] -> Virtual Channel Select 3 is processed vc_select4[20] -> Virtual Channel Select 4 is processed vc_select5[21] -> Virtual Channel Select 5 is processed vc_select6[22] -> Virtual Channel Select 6 is processed vc_select7[23] -> Virtual Channel Select 7 is processed vc_select8[24] -> Virtual Channel Select 8 is processed vc_select9[25] -> Virtual Channel Select 9 is processed vc_select10[26] -> Virtual Channel Select 10 is processed vc_select11[27] -> Virtual Channel Select 11 is processed vc_select12[28] -> Virtual Channel Select 12 is processed vc_select13[29] -> Virtual Channel Select 13 is processed vc_select14[30] -> Virtual Channel Select 14 is processed vc_select15[31] -> Virtual Channel Select 15 is processed |
| 15 | ENABLE_DT1 | R/W | 0h | Enable processing of dt1 |

Table 9-93. CSI_RX_IF_VBUS2APB_STREAM0_DATA_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 14 | RESERVED | R/W | X | |
| 13-8 | DATATYPE_SELECT1 | R/W | 0h | Second data type format that this stream will process |
| 7 | ENABLE_DT0 | R/W | 0h | Enable processing of dt0 |
| 6 | RESERVED | R/W | X | |
| 5-0 | DATATYPE_SELECT0 | R/W | 0h | First data type format that this stream will process |

9.47 CSI_RX_IF_VBUS2APB_STREAM0_CFG Register (Offset = 10Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_CFG is shown in [Figure 9-44](#) and described in [Table 9-95](#).

Return to [Summary Table](#).

Primary CSI2 Slave Controller Data pixel outputs configuration.

This register is used to configure the output mode.

It is also used to set up some Stream FIFO related settings.

Table 9-94. CSI_RX_IF_VBUS2APB_STREAM0_CFG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 410Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 410Ch |

Figure 9-44. CSI_RX_IF_VBUS2APB_STREAM0_CFG Register

| | | | | | | | |
|-----------|------------|----|----|----------|------------|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | BPP_BYPASS | | | RESERVED | FIFO_MODE | | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | NUM_PIXELS | | | RESERVED | LS_LE_MODE | INTERFACE_M ODE | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-95. CSI_RX_IF_VBUS2APB_STREAM0_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | FIFO_FILL | R/W | 0h | Set the FIFO_FILL_LEVEL which is used to hold data in the FIFO until this level is reached before allow data to be pulled. This setting is only used when fifo_mode is set for Large Buffer operation |
| 15 | RESERVED | R/W | X | |
| 14-12 | BPP_BYPASS | R/W | 0h | Force unpacking of any Data type as selected RAW type. 0 - No bypass 1 - unpack as RAW6 2 - unpack as RAW7 3 - unpack as RAW8 4 - unpack as RAW10 5 - unpack as RAW12 6 - unpack as RAW14 7 - unpack as RAW16 |
| 11-10 | RESERVED | R/W | X | |

Table 9-95. CSI_RX_IF_VBUS2APB_STREAM0_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 9-8 | FIFO_MODE | R/W | 0h | Stream FIFO configuration, which must be set in accordance to FIFO sizing, flow control and the relationship between the link and pixel interface data rates. Refer to Use Case descriptions for further guidance on FIFO sizing and valid stream configuration options. 00: Full Line Buffer. Hold data in FIFO until CRC check completes. 01: Large Buffer [Fill Level Controlled]. Hold data in FIFO until FIFO_FILL_LEVEL is reached. 1x: Short Buffer. When pixel output data rate can match link data rate, a small buffer can be used to accommodate CDC, pixel data packing, and data rate matching |
| 7-6 | RESERVED | R/W | X | |
| 5-4 | NUM_PIXELS | R/W | 0h | Number of pixels to output from the stream. Valid values are 1, 2, 4 and 8. The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 3-2 | RESERVED | R/W | X | |
| 1 | LS_LE_MODE | R/W | 0h | Enable LS/LE control of HYSNC_VALID output. By default, LS and LE short packets are not required and HYSC_VALID will be generated from the start and end of payload data. |
| 0 | INTERFACE_MODE | R/W | 0h | Select the output configuration. Pixel = 0 [default] Packed = 1 |

9.48 CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL Register (Offset = 110h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL is shown in [Figure 9-45](#) and described in [Table 9-97](#).

Return to [Summary Table](#).

Stream Monitor configuration.

This register is used to configure the CSI2RX Monitors:

Programmable Frame monitor to trigger an event if a truncated frame is detected,

Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end,

Programmable line/byte counters to trigger an event at a specific byte in a line.

This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event.

This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled.

In these cases, the behaviour is unpredictable.

Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0.

Table 9-96.
CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4110h |
| CSI_RX_IF_VBUS2APB1 | 0451 4110h |

Figure 9-45. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL Register

| | | | | | | | |
|--------------|--------------|----|--------|--------|-----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FRAME_MON_EN | FRAME_MON_VC | | | | TIMER_EOF | TIMER_EN | TIMER_VC |
| R/W-0h | R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TIMER_VC | | | LB_EN | LB_VC | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-97. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-16 | FRAME_LENGTH | R/W | 0h | Indicates the frame length in lines to detect truncated frames. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. 0x0000 means truncated frame detection feature disabled |
| 15 | FRAME_MON_EN | R/W | 0h | Enables monitor. This bit must only be set high after the frame_mon_vc and frame_length have been set. |

Table 9-97. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 14-11 | FRAME_MON_VC | R/W | 0h | Indicates virtual channel for monitor. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. |
| 10 | TIMER_EOF | R/W | 0h | Select the starting point of the timer: 0x 0: Start of Frame event on selected virtual channel 0x 1: End of Frame event on selected virtual channel. This value must not change while timer_en is enabled |
| 9 | TIMER_EN | R/W | 0h | Enables timer based interrupt. This bit must only be set high after the timer_eof and timer_vc have been set. |
| 8-5 | TIMER_VC | R/W | 0h | Indicates which VC should be used to generate timer based interrupt. This value must not change while timer_en is enabled. |
| 4 | LB_EN | R/W | 0h | Enables line/byte counter. This bit must only be set high after the lb_vc, line_count and byte_count have been set. |
| 3-0 | LB_VC | R/W | 0h | Indicates which VC should be used to generate line/byte counter interrupt. This value must not change while lb_en is enabled |

9.49 CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_FRAME Register (Offset = 114h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_FRAME is shown in [Figure 9-46](#) and described in [Table 9-99](#).

Return to [Summary Table](#).

Stream Monitor Frame.

Used to observe the current frame number and packet size on monitored virtual channels.

These values are extracted by the CSI2RX from the last frame start short packet data field.

Table 9-98.
CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_FRA
ME Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4114h |
| CSI_RX_IF_VBUS2APB1 | 0451 4114h |

Figure 9-46. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_FRAME Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PACKET_SIZE | | | | | | | | | | | | | | | | NB | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-99. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_FRAME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|-------------------------------------|
| 31-16 | PACKET_SIZE | R | 0h | Size of the current payload |
| 15-0 | NB | R | 0h | Number of the last frame processed. |

9.50 CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_LB Register (Offset = 118h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_LB is shown in [Figure 9-47](#) and described in [Table 9-101](#).

Return to [Summary Table](#).

Stream Monitor Line.

Used to specify the byte and line numbers that will generate an interrupt.

This register must only be modified when the corresponding line/byte enable is disabled.

Table 9-100.
CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_LB
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4118h |
| CSI_RX_IF_VBUS2APB1 | 0451 4118h |

Figure 9-47. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_LB Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_COUNT | | | | | | | | | | | | | | | | BYTE_COUNT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-101. CSI_RX_IF_VBUS2APB_STREAM0_MONITOR_LB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | LINE_COUNT | R/W | 0h | Indicates the line number to generate an interrupt. [First line of a Frame is line number 0] |
| 15-0 | BYTE_COUNT | R/W | 0h | Indicates the byte number of the line to generate an interrupt. [First byte of a line is byte number 0] |

9.51 CSI_RX_IF_VBUS2APB_STREAM0_TIMER Register (Offset = 11Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_TIMER is shown in [Figure 9-48](#) and described in [Table 9-103](#).

Return to [Summary Table](#).

Stream Timer.

Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end.

This register must only be modified when the corresponding timer enable is disabled.

Table 9-102.
CSI_RX_IF_VBUS2APB_STREAM0_TIMER
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 411Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 411Ch |

Figure 9-48. CSI_RX_IF_VBUS2APB_STREAM0_TIMER Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | COUNT | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-103. CSI_RX_IF_VBUS2APB_STREAM0_TIMER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|------------------------|
| 31-25 | RESERVED | R/W | X | |
| 24-0 | COUNT | R/W | 0h | Number of clock cycles |

9.52 CSI_RX_IF_VBUS2APB_STREAM0_FCC_CFG Register (Offset = 120h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM0_FCC_CFG is shown in [Figure 9-49](#) and described in [Table 9-105](#).

Return to [Summary Table](#).

Stream Frame Capture Control configuration.

Used to specify the frame count value when the CSI2RX must generate interrupts

FCC_START and FCC_STOP.

This register must only be modified when the corresponding frame count enable is disabled.

Table 9-104.
CSI_RX_IF_VBUS2APB_STREAM0_FCC_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4120h |
| CSI_RX_IF_VBUS2APB1 | 0451 4120h |

Figure 9-49. CSI_RX_IF_VBUS2APB_STREAM0_FCC_CFG Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNT_STOP | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRAME_COUNT_START | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-105. CSI_RX_IF_VBUS2APB_STREAM0_FCC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-16 | FRAME_COUNT_STOP | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will stop outputting data on the pixel interface. [0x0000 will be continuous frames.] |
| 15-0 | FRAME_COUNT_START | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will start outputting data on the pixel interface. [0x0000 will be the current frame.] |

9.53 CSI_RX_IF_VBUS2APB_STREAM0_FCC_CTRL Register (Offset = 124h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_FCC_CTRL is shown in [Figure 9-50](#) and described in [Table 9-107](#).

Return to [Summary Table](#).

Stream Frame Capture Counter control.

Used to enable / disable the FCC and specify which virtual channel it should operate on.

Table 9-106.
CSI_RX_IF_VBUS2APB_STREAM0_FCC_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4124h |
| CSI_RX_IF_VBUS2APB1 | 0451 4124h |

Figure 9-50. CSI_RX_IF_VBUS2APB_STREAM0_FCC_CTRL Register

| | | | | | | | |
|---------------|----|----|--------|----|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | FCC_VC | | | FCC_EN | |
| R/W-X | | | R/W-0h | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-107. CSI_RX_IF_VBUS2APB_STREAM0_FCC_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 31-16 | FRAME_COUNTER | R | 0h | Current Frame number being processed |
| 15-5 | RESERVED | R/W | X | |
| 4-1 | FCC_VC | R/W | 0h | Indicates which VC should be used to generate FCC interrupts. This value must not change while fcc_en is enabled |
| 0 | FCC_EN | R/W | 0h | Frame Capture Counter enable. |

9.54 CSI_RX_IF_VBUS2APB_STREAM0_FIFO_FILL_LVL Register (Offset = 128h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM0_FIFO_FILL_LVL is shown in [Figure 9-51](#) and described in [Table 9-109](#).

Return to [Summary Table](#).

Stream FIFO fill level monitor. This can operate in 2 modes:

- 1 - Monitor peak fill level until the stream is stopped.
- 2 - Monitor peak fill level when the first FIFO read is made during a frame.

Table 9-108.
CSI_RX_IF_VBUS2APB_STREAM0_FIFO_FILL_LVL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4128h |
| CSI_RX_IF_VBUS2APB1 | 0451 4128h |

Figure 9-51. CSI_RX_IF_VBUS2APB_STREAM0_FIFO_FILL_LVL Register

| | | | | | | | |
|----------|----|--------|----|----------|----|-------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | MODE | | RESERVED | | COUNT | |
| R/W-X | | R/W-0h | | R/W-X | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNT | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-109. CSI_RX_IF_VBUS2APB_STREAM0_FIFO_FILL_LVL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-14 | RESERVED | R/W | X | |
| 13-12 | MODE | R/W | 0h | 00 -> Fill level detection disabled 01 -> Mode 1 10 -> Mode 2 11 -> Reserved |
| 11-10 | RESERVED | R/W | X | |
| 9-0 | COUNT | R | 0h | Peak fill level of FIFO. |

9.55 CSI_RX_IF_VBUS2APB_STREAM1_CTRL Register (Offset = 200h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_CTRL is shown in [Figure 9-52](#) and described in [Table 9-111](#).

Return to [Summary Table](#).

CSI2RX Stream Data output datapath control.

Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started.

Table 9-110.
CSI_RX_IF_VBUS2APB_STREAM1_CTRL Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4200h |
| CSI_RX_IF_VBUS2APB1 | 0451 4200h |

Figure 9-52. CSI_RX_IF_VBUS2APB_STREAM1_CTRL Register

| | | | | | | | |
|----------|----|----|----------|----------|-------|------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | SOFT_RST | RESERVED | ABORT | STOP | START |
| R/W-X | | | R/W1C-0h | R/W-X | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; W = Write Only; -n = value after reset

Table 9-111. CSI_RX_IF_VBUS2APB_STREAM1_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | SOFT_RST | R/W1C | 0h | Writing 1'b1 will apply a synchronous soft reset of this stream registers/FIFO |
| 3 | RESERVED | R/W | X | |
| 2 | ABORT | W | 0h | Writing 1 this register will cause the csi2rx to stop streaming on the corresponding output immediately. This may corrupt the output protocol. stream_abort_irq is generated on completion of the abort operation. |
| 1 | STOP | W | 0h | Writing 1 in this register will cause csi2rx to stop streaming on the corresponding output at the end of the current frame. If the command is issued during frame blanking, then the datapath will immediately stop streaming data on that output. stream_stop_irq is generated on completion of the stop operation. |

Table 9-111. CSI_RX_IF_VBUS2APB_STREAM1_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | START | W | 0h | Writing 1 in this register enables the corresponding datapath output. It will start streaming data at the start of the next frame that complies with the output configuration. stream_status[31] running indicates when data stream is enabled. |

9.56 CSI_RX_IF_VBUS2APB_STREAM1_STATUS Register (Offset = 204h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_STATUS is shown in [Figure 9-53](#) and described in [Table 9-113](#).

Return to [Summary Table](#).

CSI2 Slave Controller Status. Contains useful debug information such as FSM states.

Table 9-112.
CSI_RX_IF_VBUS2APB_STREAM1_STATUS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4204h |
| CSI_RX_IF_VBUS2APB1 | 0451 4204h |

Figure 9-53. CSI_RX_IF_VBUS2APB_STREAM1_STATUS Register

| | | | | | | | |
|------------|----------|----|----|----------|----|--------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RUNNING | RESERVED | | | | | | |
| R-0h | R-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | READY_STATE |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_FSM | | | | RESERVED | | PROTOCOL_FSM | |
| R-0h | | | | R-X | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 9-113. CSI_RX_IF_VBUS2APB_STREAM1_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 31 | RUNNING | R | 0h | The Stream is enabled |
| 30-9 | RESERVED | R | X | |
| 8 | READY_STATE | R | 0h | Indicates the state of the pushback signal pixel_ready_if for this stream |

Table 9-113. CSI_RX_IF_VBUS2APB_STREAM1_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-4 | STREAM_FSM | R | 0h | Output to Stream FSM states: 0x 0: STREAM_IDLE 0x 1: STREAM_WAIT_CTRL_DATA // Expecting control data next 0x 2: STREAM_CTRL // Check contents of Ctrl packet and extract header information 0x 3: STREAM_DATA // Pixel stream pixel data unpacking 0x 4: STREAM_CONV_PIX_NB // 1st cycle delay for byte2pixel conversion 0x 5: STREAM_CONV_PIX_NB_EXT // 2nd cycle delay for byte2pixel conversion 0x 6: STREAM_DATA_START // Assert Hsync 0x 7: STREAM_DATA_END // De-assert Hsync 0x 8: STREAM_FILL_WAIT // Elastic Buffer cfg - wait until fill level is reached 0x 9: STREAM_STOP // Stop at the end of Frame - used to set irq 0xA: STREAM_WAIT_CRC // Wait until CRC check has completed - Full Line cfg 0xB: STREAM_WAIT_PKT_DONE // Wait for CRC to complete before proceeding 0xC: STREAM_PKT_DONE // Packet complete - no error conditions after this point 0xD: STREAM_NULL // NULL pkt received 0xE: STREAM_FLUSH // Flush due to CRC error |
| 3-2 | RESERVED | R | X | |
| 1-0 | PROTOCOL_FSM | R | 0h | Input to Stream FSM states: 0x 0: PROT_IDLE 0x 1: PROT_WAIT_CTRL 0x 2: PROT_CTRL 0x 3: PROT_DATA |

9.57 CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG Register (Offset = 208h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG is shown in [Figure 9-54](#) and described in [Table 9-115](#).

Return to [Summary Table](#).

Secondary CSI2 Slave Controller Data outputs configuration.

This register is used to configure the data types and virtual channels are processed and output by this stream.

Table 9-114.
CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4208h |
| CSI_RX_IF_VBUS2APB1 | 0451 4208h |

Figure 9-54. CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG Register

| | | | | | | | |
|------------|----------|------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ENABLE_DT1 | RESERVED | DATATYPE_SELECT1 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENABLE_DT0 | RESERVED | DATATYPE_SELECT0 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-115. CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | VC_SELECT | R/W | 0h | Selection of Virtual Channels to be processed: Default '0' -> All Virtual Channels are processed vc_select0[16] -> Virtual Channel Select 0 is processed vc_select1[17] -> Virtual Channel Select 1 is processed vc_select2[18] -> Virtual Channel Select 2 is processed vc_select3[19] -> Virtual Channel Select 3 is processed vc_select4[20] -> Virtual Channel Select 4 is processed vc_select5[21] -> Virtual Channel Select 5 is processed vc_select6[22] -> Virtual Channel Select 6 is processed vc_select7[23] -> Virtual Channel Select 7 is processed vc_select8[24] -> Virtual Channel Select 8 is processed vc_select9[25] -> Virtual Channel Select 9 is processed vc_select10[26] -> Virtual Channel Select 10 is processed vc_select11[27] -> Virtual Channel Select 11 is processed vc_select12[28] -> Virtual Channel Select 12 is processed vc_select13[29] -> Virtual Channel Select 13 is processed vc_select14[30] -> Virtual Channel Select 14 is processed vc_select15[31] -> Virtual Channel Select 15 is processed |
| 15 | ENABLE_DT1 | R/W | 0h | Enable processing of dt1 |

Table 9-115. CSI_RX_IF_VBUS2APB_STREAM1_DATA_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 14 | RESERVED | R/W | X | |
| 13-8 | DATATYPE_SELECT1 | R/W | 0h | Second data type format that this stream will process |
| 7 | ENABLE_DT0 | R/W | 0h | Enable processing of dt0 |
| 6 | RESERVED | R/W | X | |
| 5-0 | DATATYPE_SELECT0 | R/W | 0h | First data type format that this stream will process |

9.58 CSI_RX_IF_VBUS2APB_STREAM1_CFG Register (Offset = 20Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_CFG is shown in [Figure 9-55](#) and described in [Table 9-117](#).

Return to [Summary Table](#).

Primary CSI2 Slave Controller Data pixel outputs configuration.

This register is used to configure the output mode.

It is also used to set up some Stream FIFO related settings.

Table 9-116.
CSI_RX_IF_VBUS2APB_STREAM1_CFG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 420Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 420Ch |

Figure 9-55. CSI_RX_IF_VBUS2APB_STREAM1_CFG Register

| | | | | | | | |
|-----------|------------|----|----|----------|------------|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | BPP_BYPASS | | | RESERVED | FIFO_MODE | | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | NUM_PIXELS | | | RESERVED | LS_LE_MODE | INTERFACE_M ODE | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-117. CSI_RX_IF_VBUS2APB_STREAM1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | FIFO_FILL | R/W | 0h | Set the FIFO_FILL_LEVEL which is used to hold data in the FIFO until this level is reached before allow data to be pulled. This setting is only used when fifo_mode is set for Large Buffer operation |
| 15 | RESERVED | R/W | X | |
| 14-12 | BPP_BYPASS | R/W | 0h | Force unpacking of any Data type as selected RAW type. 0 - No bypass 1 - unpack as RAW6 2 - unpack as RAW7 3 - unpack as RAW8 4 - unpack as RAW10 5 - unpack as RAW12 6 - unpack as RAW14 7 - unpack as RAW16 |
| 11-10 | RESERVED | R/W | X | |

Table 9-117. CSI_RX_IF_VBUS2APB_STREAM1_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 9-8 | FIFO_MODE | R/W | 0h | Stream FIFO configuration, which must be set in accordance to FIFO sizing, flow control and the relationship between the link and pixel interface data rates. Refer to Use Case descriptions for further guidance on FIFO sizing and valid stream configuration options. 00: Full Line Buffer. Hold data in FIFO until CRC check completes. 01: Large Buffer [Fill Level Controlled]. Hold data in FIFO until FIFO_FILL_LEVEL is reached. 1x: Short Buffer. When pixel output data rate can match link data rate, a small buffer can be used to accommodate CDC, pixel data packing, and data rate matching |
| 7-6 | RESERVED | R/W | X | |
| 5-4 | NUM_PIXELS | R/W | 0h | Number of pixels to output from the stream. Valid values are 1, 2, 4 and 8. The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 3-2 | RESERVED | R/W | X | |
| 1 | LS_LE_MODE | R/W | 0h | Enable LS/LE control of HYSNC_VALID output. By default, LS and LE short packets are not required and HYSC_VALID will be generated from the start and end of payload data. |
| 0 | INTERFACE_MODE | R/W | 0h | Select the output configuration. Pixel = 0 [default] Packed = 1 |

9.59 CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL Register (Offset = 210h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL is shown in [Figure 9-56](#) and described in [Table 9-119](#).

Return to [Summary Table](#).

Stream Monitor configuration.

This register is used to configure the CSI2RX Monitors:

Programmable Frame monitor to trigger an event if a truncated frame is detected,

Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end,

Programmable line/byte counters to trigger an event at a specific byte in a line.

This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event.

This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled.

In these cases, the behaviour is unpredictable.

Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0.

Table 9-118.
CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4210h |
| CSI_RX_IF_VBUS2APB1 | 0451 4210h |

Figure 9-56. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL Register

| | | | | | | | |
|--------------|--------------|----|--------|--------|-----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FRAME_MON_EN | FRAME_MON_VC | | | | TIMER_EOF | TIMER_EN | TIMER_VC |
| R/W-0h | R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TIMER_VC | | | LB_EN | LB_VC | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-119. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-16 | FRAME_LENGTH | R/W | 0h | Indicates the frame length in lines to detect truncated frames. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. 0x0000 means truncated frame detection feature disabled |
| 15 | FRAME_MON_EN | R/W | 0h | Enables monitor. This bit must only be set high after the frame_mon_vc and frame_length have been set. |

Table 9-119. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 14-11 | FRAME_MON_VC | R/W | 0h | Indicates virtual channel for monitor. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. |
| 10 | TIMER_EOF | R/W | 0h | Select the starting point of the timer: 0x 0: Start of Frame event on selected virtual channel 0x 1: End of Frame event on selected virtual channel. This value must not change while timer_en is enabled |
| 9 | TIMER_EN | R/W | 0h | Enables timer based interrupt. This bit must only be set high after the timer_eof and timer_vc have been set. |
| 8-5 | TIMER_VC | R/W | 0h | Indicates which VC should be used to generate timer based interrupt. This value must not change while timer_en is enabled. |
| 4 | LB_EN | R/W | 0h | Enables line/byte counter. This bit must only be set high after the lb_vc, line_count and byte_count have been set. |
| 3-0 | LB_VC | R/W | 0h | Indicates which VC should be used to generate line/byte counter interrupt. This value must not change while lb_en is enabled |

9.60 CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_FRAME Register (Offset = 214h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_FRAME is shown in [Figure 9-57](#) and described in [Table 9-121](#).

Return to [Summary Table](#).

Stream Monitor Frame.

Used to observe the current frame number and packet size on monitored virtual channels.

These values are extracted by the CSI2RX from the last frame start short packet data field.

Table 9-120.
CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_FRA
ME Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4214h |
| CSI_RX_IF_VBUS2APB1 | 0451 4214h |

Figure 9-57. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_FRAME Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PACKET_SIZE | | | | | | | | | | | | | | | | NB | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-121. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_FRAME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|-------------------------------------|
| 31-16 | PACKET_SIZE | R | 0h | Size of the current payload |
| 15-0 | NB | R | 0h | Number of the last frame processed. |

9.61 CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_LB Register (Offset = 218h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_LB is shown in [Figure 9-58](#) and described in [Table 9-123](#).

Return to [Summary Table](#).

Stream Monitor Line.

Used to specify the byte and line numbers that will generate an interrupt.

This register must only be modified when the corresponding line/byte enable is disabled.

Table 9-122.
CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_LB
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4218h |
| CSI_RX_IF_VBUS2APB1 | 0451 4218h |

Figure 9-58. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_LB Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_COUNT | | | | | | | | | | | | | | | | BYTE_COUNT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-123. CSI_RX_IF_VBUS2APB_STREAM1_MONITOR_LB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | LINE_COUNT | R/W | 0h | Indicates the line number to generate an interrupt. [First line of a Frame is line number 0] |
| 15-0 | BYTE_COUNT | R/W | 0h | Indicates the byte number of the line to generate an interrupt. [First byte of a line is byte number 0] |

9.62 CSI_RX_IF_VBUS2APB_STREAM1_TIMER Register (Offset = 21Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_TIMER is shown in [Figure 9-59](#) and described in [Table 9-125](#).

Return to [Summary Table](#).

Stream Timer.

Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end.

This register must only be modified when the corresponding timer enable is disabled.

Table 9-124.
CSI_RX_IF_VBUS2APB_STREAM1_TIMER
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 421Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 421Ch |

Figure 9-59. CSI_RX_IF_VBUS2APB_STREAM1_TIMER Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | COUNT | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-125. CSI_RX_IF_VBUS2APB_STREAM1_TIMER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|------------------------|
| 31-25 | RESERVED | R/W | X | |
| 24-0 | COUNT | R/W | 0h | Number of clock cycles |

9.63 CSI_RX_IF_VBUS2APB_STREAM1_FCC_CFG Register (Offset = 220h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM1_FCC_CFG is shown in [Figure 9-60](#) and described in [Table 9-127](#).

Return to [Summary Table](#).

Stream Frame Capture Control configuration.

Used to specify the frame count value when the CSI2RX must generate interrupts

FCC_START and FCC_STOP.

This register must only be modified when the corresponding frame count enable is disabled.

Table 9-126.
CSI_RX_IF_VBUS2APB_STREAM1_FCC_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4220h |
| CSI_RX_IF_VBUS2APB1 | 0451 4220h |

Figure 9-60. CSI_RX_IF_VBUS2APB_STREAM1_FCC_CFG Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNT_STOP | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRAME_COUNT_START | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-127. CSI_RX_IF_VBUS2APB_STREAM1_FCC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-16 | FRAME_COUNT_STOP | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will stop outputting data on the pixel interface. [0x0000 will be continuous frames.] |
| 15-0 | FRAME_COUNT_START | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will start outputting data on the pixel interface. [0x0000 will be the current frame.] |

9.64 CSI_RX_IF_VBUS2APB_STREAM1_FCC_CTRL Register (Offset = 224h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_FCC_CTRL is shown in [Figure 9-61](#) and described in [Table 9-129](#).

Return to [Summary Table](#).

Stream Frame Capture Counter control.

Used to enable / disable the FCC and specify which virtual channel it should operate on.

Table 9-128.
CSI_RX_IF_VBUS2APB_STREAM1_FCC_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4224h |
| CSI_RX_IF_VBUS2APB1 | 0451 4224h |

Figure 9-61. CSI_RX_IF_VBUS2APB_STREAM1_FCC_CTRL Register

| | | | | | | | |
|---------------|----|----|--------|----|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | FCC_VC | | | FCC_EN | |
| R/W-X | | | R/W-0h | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-129. CSI_RX_IF_VBUS2APB_STREAM1_FCC_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 31-16 | FRAME_COUNTER | R | 0h | Current Frame number being processed |
| 15-5 | RESERVED | R/W | X | |
| 4-1 | FCC_VC | R/W | 0h | Indicates which VC should be used to generate FCC interrupts. This value must not change while fcc_en is enabled |
| 0 | FCC_EN | R/W | 0h | Frame Capture Counter enable. |

9.65 CSI_RX_IF_VBUS2APB_STREAM1_FIFO_FILL_LVL Register (Offset = 228h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM1_FIFO_FILL_LVL is shown in [Figure 9-62](#) and described in [Table 9-131](#).

Return to [Summary Table](#).

Stream FIFO fill level monitor. This can operate in 2 modes:

- 1 - Monitor peak fill level until the stream is stopped.
- 2 - Monitor peak fill level when the first FIFO read is made during a frame.

Table 9-130.
CSI_RX_IF_VBUS2APB_STREAM1_FIFO_FILL_LVL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4228h |
| CSI_RX_IF_VBUS2APB1 | 0451 4228h |

Figure 9-62. CSI_RX_IF_VBUS2APB_STREAM1_FIFO_FILL_LVL Register

| | | | | | | | |
|----------|----|--------|----|----------|----|-------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | MODE | | RESERVED | | COUNT | |
| R/W-X | | R/W-0h | | R/W-X | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNT | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-131. CSI_RX_IF_VBUS2APB_STREAM1_FIFO_FILL_LVL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-14 | RESERVED | R/W | X | |
| 13-12 | MODE | R/W | 0h | 00 -> Fill level detection disabled 01 -> Mode 1 10 -> Mode 2 11 -> Reserved |
| 11-10 | RESERVED | R/W | X | |
| 9-0 | COUNT | R | 0h | Peak fill level of FIFO. |

9.66 CSI_RX_IF_VBUS2APB_STREAM2_CTRL Register (Offset = 300h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_CTRL is shown in [Figure 9-63](#) and described in [Table 9-133](#).

Return to [Summary Table](#).

CSI2RX Stream Data output datapath control.

Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started.

Table 9-132.
CSI_RX_IF_VBUS2APB_STREAM2_CTRL Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4300h |
| CSI_RX_IF_VBUS2APB1 | 0451 4300h |

Figure 9-63. CSI_RX_IF_VBUS2APB_STREAM2_CTRL Register

| | | | | | | | |
|----------|----|----|----------|----------|-------|------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | SOFT_RST | RESERVED | ABORT | STOP | START |
| R/W-X | | | R/W1C-0h | R/W-X | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; W = Write Only; -n = value after reset

Table 9-133. CSI_RX_IF_VBUS2APB_STREAM2_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | SOFT_RST | R/W1C | 0h | Writing 1'b1 will apply a synchronous soft reset of this stream registers/FIFO |
| 3 | RESERVED | R/W | X | |
| 2 | ABORT | W | 0h | Writing 1 this register will cause the csi2rx to stop streaming on the corresponding output immediately. This may corrupt the output protocol. stream_abort_irq is generated on completion of the abort operation. |
| 1 | STOP | W | 0h | Writing 1 in this register will cause csi2rx to stop streaming on the corresponding output at the end of the current frame. If the command is issued during frame blanking, then the datapath will immediately stop streaming data on that output. stream_stop_irq is generated on completion of the stop operation. |

Table 9-133. CSI_RX_IF_VBUS2APB_STREAM2_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | START | W | 0h | Writing 1 in this register enables the corresponding datapath output. It will start streaming data at the start of the next frame that complies with the output configuration. stream_status[31] running indicates when data stream is enabled. |

9.67 CSI_RX_IF_VBUS2APB_STREAM2_STATUS Register (Offset = 304h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_STATUS is shown in [Figure 9-64](#) and described in [Table 9-135](#).

Return to [Summary Table](#).

CSI2 Slave Controller Status. Contains useful debug information such as FSM states.

Table 9-134.
CSI_RX_IF_VBUS2APB_STREAM2_STATUS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4304h |
| CSI_RX_IF_VBUS2APB1 | 0451 4304h |

Figure 9-64. CSI_RX_IF_VBUS2APB_STREAM2_STATUS Register

| | | | | | | | |
|------------|----------|----|----|----------|----|--------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RUNNING | RESERVED | | | | | | |
| R-0h | R-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | READY_STATE |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_FSM | | | | RESERVED | | PROTOCOL_FSM | |
| R-0h | | | | R-X | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 9-135. CSI_RX_IF_VBUS2APB_STREAM2_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 31 | RUNNING | R | 0h | The Stream is enabled |
| 30-9 | RESERVED | R | X | |
| 8 | READY_STATE | R | 0h | Indicates the state of the pushback signal pixel_ready_if for this stream |

Table 9-135. CSI_RX_IF_VBUS2APB_STREAM2_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-4 | STREAM_FSM | R | 0h | Output to Stream FSM states: 0x 0: STREAM_IDLE 0x 1: STREAM_WAIT_CTRL_DATA // Expecting control data next 0x 2: STREAM_CTRL // Check contents of Ctrl packet and extract header information 0x 3: STREAM_DATA // Pixel stream pixel data unpacking 0x 4: STREAM_CONV_PIX_NB // 1st cycle delay for byte2pixel conversion 0x 5: STREAM_CONV_PIX_NB_EXT // 2nd cycle delay for byte2pixel conversion 0x 6: STREAM_DATA_START // Assert Hsync 0x 7: STREAM_DATA_END // De-assert Hsync 0x 8: STREAM_FILL_WAIT // Elastic Buffer cfg - wait until fill level is reached 0x 9: STREAM_STOP // Stop at the end of Frame - used to set irq 0xA: STREAM_WAIT_CRC // Wait until CRC check has completed - Full Line cfg 0xB: STREAM_WAIT_PKT_DONE // Wait for CRC to complete before proceeding 0xC: STREAM_PKT_DONE // Packet complete - no error conditions after this point 0xD: STREAM_NULL // NULL pkt received 0xE: STREAM_FLUSH // Flush due to CRC error |
| 3-2 | RESERVED | R | X | |
| 1-0 | PROTOCOL_FSM | R | 0h | Input to Stream FSM states: 0x 0: PROT_IDLE 0x 1: PROT_WAIT_CTRL 0x 2: PROT_CTRL 0x 3: PROT_DATA |

9.68 CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG Register (Offset = 308h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG is shown in [Figure 9-65](#) and described in [Table 9-137](#).

Return to [Summary Table](#).

Secondary CSI2 Slave Controller Data outputs configuration.

This register is used to configure the data types and virtual channels are processed and output by this stream.

Table 9-136.
CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4308h |
| CSI_RX_IF_VBUS2APB1 | 0451 4308h |

Figure 9-65. CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG Register

| | | | | | | | |
|------------|----------|------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ENABLE_DT1 | RESERVED | DATATYPE_SELECT1 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENABLE_DT0 | RESERVED | DATATYPE_SELECT0 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-137. CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | VC_SELECT | R/W | 0h | Selection of Virtual Channels to be processed: Default '0' -> All Virtual Channels are processed vc_select0[16] -> Virtual Channel Select 0 is processed vc_select1[17] -> Virtual Channel Select 1 is processed vc_select2[18] -> Virtual Channel Select 2 is processed vc_select3[19] -> Virtual Channel Select 3 is processed vc_select4[20] -> Virtual Channel Select 4 is processed vc_select5[21] -> Virtual Channel Select 5 is processed vc_select6[22] -> Virtual Channel Select 6 is processed vc_select7[23] -> Virtual Channel Select 7 is processed vc_select8[24] -> Virtual Channel Select 8 is processed vc_select9[25] -> Virtual Channel Select 9 is processed vc_select10[26] -> Virtual Channel Select 10 is processed vc_select11[27] -> Virtual Channel Select 11 is processed vc_select12[28] -> Virtual Channel Select 12 is processed vc_select13[29] -> Virtual Channel Select 13 is processed vc_select14[30] -> Virtual Channel Select 14 is processed vc_select15[31] -> Virtual Channel Select 15 is processed |
| 15 | ENABLE_DT1 | R/W | 0h | Enable processing of dt1 |

Table 9-137. CSI_RX_IF_VBUS2APB_STREAM2_DATA_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 14 | RESERVED | R/W | X | |
| 13-8 | DATATYPE_SELECT1 | R/W | 0h | Second data type format that this stream will process |
| 7 | ENABLE_DT0 | R/W | 0h | Enable processing of dt0 |
| 6 | RESERVED | R/W | X | |
| 5-0 | DATATYPE_SELECT0 | R/W | 0h | First data type format that this stream will process |

9.69 CSI_RX_IF_VBUS2APB_STREAM2_CFG Register (Offset = 30Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_CFG is shown in [Figure 9-66](#) and described in [Table 9-139](#).

Return to [Summary Table](#).

Primary CSI2 Slave Controller Data pixel outputs configuration.

This register is used to configure the output mode.

It is also used to set up some Stream FIFO related settings.

Table 9-138.
CSI_RX_IF_VBUS2APB_STREAM2_CFG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 430Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 430Ch |

Figure 9-66. CSI_RX_IF_VBUS2APB_STREAM2_CFG Register

| | | | | | | | |
|-----------|------------|----|----|----------|------------|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | BPP_BYPASS | | | RESERVED | FIFO_MODE | | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | NUM_PIXELS | | | RESERVED | LS_LE_MODE | INTERFACE_M ODE | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-139. CSI_RX_IF_VBUS2APB_STREAM2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | FIFO_FILL | R/W | 0h | Set the FIFO_FILL_LEVEL which is used to hold data in the FIFO until this level is reached before allow data to be pulled. This setting is only used when fifo_mode is set for Large Buffer operation |
| 15 | RESERVED | R/W | X | |
| 14-12 | BPP_BYPASS | R/W | 0h | Force unpacking of any Data type as selected RAW type. 0 - No bypass 1 - unpack as RAW6 2 - unpack as RAW7 3 - unpack as RAW8 4 - unpack as RAW10 5 - unpack as RAW12 6 - unpack as RAW14 7 - unpack as RAW16 |
| 11-10 | RESERVED | R/W | X | |

Table 9-139. CSI_RX_IF_VBUS2APB_STREAM2_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 9-8 | FIFO_MODE | R/W | 0h | Stream FIFO configuration, which must be set in accordance to FIFO sizing, flow control and the relationship between the link and pixel interface data rates. Refer to Use Case descriptions for further guidance on FIFO sizing and valid stream configuration options. 00: Full Line Buffer. Hold data in FIFO until CRC check completes. 01: Large Buffer [Fill Level Controlled]. Hold data in FIFO until FIFO_FILL_LEVEL is reached. 1x: Short Buffer. When pixel output data rate can match link data rate, a small buffer can be used to accommodate CDC, pixel data packing, and data rate matching |
| 7-6 | RESERVED | R/W | X | |
| 5-4 | NUM_PIXELS | R/W | 0h | Number of pixels to output from the stream. Valid values are 1, 2, 4 and 8. The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 3-2 | RESERVED | R/W | X | |
| 1 | LS_LE_MODE | R/W | 0h | Enable LS/LE control of HYSNC_VALID output. By default, LS and LE short packets are not required and HYSC_VALID will be generated from the start and end of payload data. |
| 0 | INTERFACE_MODE | R/W | 0h | Select the output configuration. Pixel = 0 [default] Packed = 1 |

9.70 CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL Register (Offset = 310h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL is shown in [Figure 9-67](#) and described in [Table 9-141](#).

Return to [Summary Table](#).

Stream Monitor configuration.

This register is used to configure the CSI2RX Monitors:

Programmable Frame monitor to trigger an event if a truncated frame is detected,

Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end,

Programmable line/byte counters to trigger an event at a specific byte in a line.

This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event.

This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled.

In these cases, the behaviour is unpredictable.

Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0.

Table 9-140.
CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4310h |
| CSI_RX_IF_VBUS2APB1 | 0451 4310h |

Figure 9-67. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL Register

| | | | | | | | |
|--------------|--------------|----|--------|--------|-----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FRAME_MON_EN | FRAME_MON_VC | | | | TIMER_EOF | TIMER_EN | TIMER_VC |
| R/W-0h | R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TIMER_VC | | | LB_EN | LB_VC | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-141. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-16 | FRAME_LENGTH | R/W | 0h | Indicates the frame length in lines to detect truncated frames. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. 0x0000 means truncated frame detection feature disabled |
| 15 | FRAME_MON_EN | R/W | 0h | Enables monitor. This bit must only be set high after the frame_mon_vc and frame_length have been set. |

Table 9-141. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 14-11 | FRAME_MON_VC | R/W | 0h | Indicates virtual channel for monitor. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. |
| 10 | TIMER_EOF | R/W | 0h | Select the starting point of the timer: 0x 0: Start of Frame event on selected virtual channel 0x 1: End of Frame event on selected virtual channel. This value must not change while timer_en is enabled |
| 9 | TIMER_EN | R/W | 0h | Enables timer based interrupt. This bit must only be set high after the timer_eof and timer_vc have been set. |
| 8-5 | TIMER_VC | R/W | 0h | Indicates which VC should be used to generate timer based interrupt. This value must not change while timer_en is enabled. |
| 4 | LB_EN | R/W | 0h | Enables line/byte counter. This bit must only be set high after the lb_vc, line_count and byte_count have been set. |
| 3-0 | LB_VC | R/W | 0h | Indicates which VC should be used to generate line/byte counter interrupt. This value must not change while lb_en is enabled |

9.71 CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_FRAME Register (Offset = 314h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_FRAME is shown in [Figure 9-68](#) and described in [Table 9-143](#).

Return to [Summary Table](#).

Stream Monitor Frame.

Used to observe the current frame number and packet size on monitored virtual channels.

These values are extracted by the CSI2RX from the last frame start short packet data field.

Table 9-142.
CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_FRA
ME Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4314h |
| CSI_RX_IF_VBUS2APB1 | 0451 4314h |

Figure 9-68. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_FRAME Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PACKET_SIZE | | | | | | | | | | | | | | | | NB | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-143. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_FRAME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|-------------------------------------|
| 31-16 | PACKET_SIZE | R | 0h | Size of the current payload |
| 15-0 | NB | R | 0h | Number of the last frame processed. |

9.72 CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_LB Register (Offset = 318h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_LB is shown in [Figure 9-69](#) and described in [Table 9-145](#).

Return to [Summary Table](#).

Stream Monitor Line.

Used to specify the byte and line numbers that will generate an interrupt.

This register must only be modified when the corresponding line/byte enable is disabled.

Table 9-144.
CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_LB
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4318h |
| CSI_RX_IF_VBUS2APB1 | 0451 4318h |

Figure 9-69. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_LB Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_COUNT | | | | | | | | | | | | | | | | BYTE_COUNT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-145. CSI_RX_IF_VBUS2APB_STREAM2_MONITOR_LB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | LINE_COUNT | R/W | 0h | Indicates the line number to generate an interrupt. [First line of a Frame is line number 0] |
| 15-0 | BYTE_COUNT | R/W | 0h | Indicates the byte number of the line to generate an interrupt. [First byte of a line is byte number 0] |

9.73 CSI_RX_IF_VBUS2APB_STREAM2_TIMER Register (Offset = 31Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_TIMER is shown in [Figure 9-70](#) and described in [Table 9-147](#).

Return to [Summary Table](#).

Stream Timer.

Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end.

This register must only be modified when the corresponding timer enable is disabled.

Table 9-146.
CSI_RX_IF_VBUS2APB_STREAM2_TIMER
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 431Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 431Ch |

Figure 9-70. CSI_RX_IF_VBUS2APB_STREAM2_TIMER Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COUNT | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-147. CSI_RX_IF_VBUS2APB_STREAM2_TIMER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|------------------------|
| 31-25 | RESERVED | R/W | X | |
| 24-0 | COUNT | R/W | 0h | Number of clock cycles |

9.74 CSI_RX_IF_VBUS2APB_STREAM2_FCC_CFG Register (Offset = 320h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM2_FCC_CFG is shown in [Figure 9-71](#) and described in [Table 9-149](#).

Return to [Summary Table](#).

Stream Frame Capture Control configuration.

Used to specify the frame count value when the CSI2RX must generate interrupts

FCC_START and FCC_STOP.

This register must only be modified when the corresponding frame count enable is disabled.

Table 9-148.
CSI_RX_IF_VBUS2APB_STREAM2_FCC_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4320h |
| CSI_RX_IF_VBUS2APB1 | 0451 4320h |

Figure 9-71. CSI_RX_IF_VBUS2APB_STREAM2_FCC_CFG Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNT_STOP | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRAME_COUNT_START | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-149. CSI_RX_IF_VBUS2APB_STREAM2_FCC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-16 | FRAME_COUNT_STOP | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will stop outputting data on the pixel interface. [0x0000 will be continuous frames.] |
| 15-0 | FRAME_COUNT_START | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will start outputting data on the pixel interface. [0x0000 will be the current frame.] |

9.75 CSI_RX_IF_VBUS2APB_STREAM2_FCC_CTRL Register (Offset = 324h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_FCC_CTRL is shown in [Figure 9-72](#) and described in [Table 9-151](#).

Return to [Summary Table](#).

Stream Frame Capture Counter control.

Used to enable / disable the FCC and specify which virtual channel it should operate on.

Table 9-150.
CSI_RX_IF_VBUS2APB_STREAM2_FCC_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4324h |
| CSI_RX_IF_VBUS2APB1 | 0451 4324h |

Figure 9-72. CSI_RX_IF_VBUS2APB_STREAM2_FCC_CTRL Register

| | | | | | | | |
|---------------|----|----|--------|----|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | FCC_VC | | | FCC_EN | |
| R/W-X | | | R/W-0h | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-151. CSI_RX_IF_VBUS2APB_STREAM2_FCC_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-16 | FRAME_COUNTER | R | 0h | Current Frame number being processed |
| 15-5 | RESERVED | R/W | X | |
| 4-1 | FCC_VC | R/W | 0h | Indicates which VC should be used to generate FCC interrupts. This value must not change while fcc_en is enabled |
| 0 | FCC_EN | R/W | 0h | Frame Capture Counter enable. |

9.76 CSI_RX_IF_VBUS2APB_STREAM2_FIFO_FILL_LVL Register (Offset = 328h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM2_FIFO_FILL_LVL is shown in [Figure 9-73](#) and described in [Table 9-153](#).

Return to [Summary Table](#).

Stream FIFO fill level monitor. This can operate in 2 modes:

- 1 - Monitor peak fill level until the stream is stopped.
- 2 - Monitor peak fill level when the first FIFO read is made during a frame.

Table 9-152.
CSI_RX_IF_VBUS2APB_STREAM2_FIFO_FILL_LVL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4328h |
| CSI_RX_IF_VBUS2APB1 | 0451 4328h |

Figure 9-73. CSI_RX_IF_VBUS2APB_STREAM2_FIFO_FILL_LVL Register

| | | | | | | | |
|----------|----|--------|----|----------|----|-------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | MODE | | RESERVED | | COUNT | |
| R/W-X | | R/W-0h | | R/W-X | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNT | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-153. CSI_RX_IF_VBUS2APB_STREAM2_FIFO_FILL_LVL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-14 | RESERVED | R/W | X | |
| 13-12 | MODE | R/W | 0h | 00 -> Fill level detection disabled 01 -> Mode 1 10 -> Mode 2 11 -> Reserved |
| 11-10 | RESERVED | R/W | X | |
| 9-0 | COUNT | R | 0h | Peak fill level of FIFO. |

9.77 CSI_RX_IF_VBUS2APB_STREAM3_CTRL Register (Offset = 400h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_CTRL is shown in [Figure 9-74](#) and described in [Table 9-155](#).

Return to [Summary Table](#).

CSI2RX Stream Data output datapath control.

Start and Stop commands are independent for each output with the exception of pixel outputs that can never be enabled together. If a pixel output is started while the other is already running, the start command will be ignored. If both pixel outputs are enabled in a single register access, then both start commands are ignored and no pixel output is started.

Table 9-154.
CSI_RX_IF_VBUS2APB_STREAM3_CTRL Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4400h |
| CSI_RX_IF_VBUS2APB1 | 0451 4400h |

Figure 9-74. CSI_RX_IF_VBUS2APB_STREAM3_CTRL Register

| | | | | | | | |
|----------|----|----|----------|----------|-------|------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | SOFT_RST | RESERVED | ABORT | STOP | START |
| R/W-X | | | R/W1C-0h | R/W-X | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; W = Write Only; -n = value after reset

Table 9-155. CSI_RX_IF_VBUS2APB_STREAM3_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | SOFT_RST | R/W1C | 0h | Writing 1'b1 will apply a synchronous soft reset of this stream registers/FIFO |
| 3 | RESERVED | R/W | X | |
| 2 | ABORT | W | 0h | Writing 1 this register will cause the csi2rx to stop streaming on the corresponding output immediately. This may corrupt the output protocol. stream_abort_irq is generated on completion of the abort operation. |
| 1 | STOP | W | 0h | Writing 1 in this register will cause csi2rx to stop streaming on the corresponding output at the end of the current frame. If the command is issued during frame blanking, then the datapath will immediately stop streaming data on that output. stream_stop_irq is generated on completion of the stop operation. |

Table 9-155. CSI_RX_IF_VBUS2APB_STREAM3_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 0 | START | W | 0h | Writing 1 in this register enables the corresponding datapath output. It will start streaming data at the start of the next frame that complies with the output configuration. stream_status[31] running indicates when data stream is enabled. |

9.78 CSI_RX_IF_VBUS2APB_STREAM3_STATUS Register (Offset = 404h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_STATUS is shown in [Figure 9-75](#) and described in [Table 9-157](#).

Return to [Summary Table](#).

CSI2 Slave Controller Status. Contains useful debug information such as FSM states.

Table 9-156.
CSI_RX_IF_VBUS2APB_STREAM3_STATUS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4404h |
| CSI_RX_IF_VBUS2APB1 | 0451 4404h |

Figure 9-75. CSI_RX_IF_VBUS2APB_STREAM3_STATUS Register

| | | | | | | | |
|------------|----------|----|----|----------|----|--------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RUNNING | RESERVED | | | | | | |
| R-0h | R-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | READY_STATE |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_FSM | | | | RESERVED | | PROTOCOL_FSM | |
| R-0h | | | | R-X | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 9-157. CSI_RX_IF_VBUS2APB_STREAM3_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 31 | RUNNING | R | 0h | The Stream is enabled |
| 30-9 | RESERVED | R | X | |
| 8 | READY_STATE | R | 0h | Indicates the state of the pushback signal pixel_ready_if for this stream |

Table 9-157. CSI_RX_IF_VBUS2APB_STREAM3_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-4 | STREAM_FSM | R | 0h | Output to Stream FSM states: 0x 0: STREAM_IDLE 0x 1: STREAM_WAIT_CTRL_DATA // Expecting control data next 0x 2: STREAM_CTRL // Check contents of Ctrl packet and extract header information 0x 3: STREAM_DATA // Pixel stream pixel data unpacking 0x 4: STREAM_CONV_PIX_NB // 1st cycle delay for byte2pixel conversion 0x 5: STREAM_CONV_PIX_NB_EXT // 2nd cycle delay for byte2pixel conversion 0x 6: STREAM_DATA_START // Assert Hsync 0x 7: STREAM_DATA_END // De-assert Hsync 0x 8: STREAM_FILL_WAIT // Elastic Buffer cfg - wait until fill level is reached 0x 9: STREAM_STOP // Stop at the end of Frame - used to set irq 0xA: STREAM_WAIT_CRC // Wait until CRC check has completed - Full Line cfg 0xB: STREAM_WAIT_PKT_DONE // Wait for CRC to complete before proceeding 0xC: STREAM_PKT_DONE // Packet complete - no error conditions after this point 0xD: STREAM_NULL // NULL pkt received 0xE: STREAM_FLUSH // Flush due to CRC error |
| 3-2 | RESERVED | R | X | |
| 1-0 | PROTOCOL_FSM | R | 0h | Input to Stream FSM states: 0x 0: PROT_IDLE 0x 1: PROT_WAIT_CTRL 0x 2: PROT_CTRL 0x 3: PROT_DATA |

9.79 CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG Register (Offset = 408h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG is shown in [Figure 9-76](#) and described in [Table 9-159](#).

Return to [Summary Table](#).

Secondary CSI2 Slave Controller Data outputs configuration.
This register is used to configure the data types and virtual channels
are processed and output by this stream.

Table 9-158.
CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4408h |
| CSI_RX_IF_VBUS2APB1 | 0451 4408h |

Figure 9-76. CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG Register

| | | | | | | | |
|------------|----------|------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_SELECT | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ENABLE_DT1 | RESERVED | DATATYPE_SELECT1 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENABLE_DT0 | RESERVED | DATATYPE_SELECT0 | | | | | |
| R/W-0h | R/W-X | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-159. CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | VC_SELECT | R/W | 0h | Selection of Virtual Channels to be processed: Default '0' -> All Virtual Channels are processed vc_select0[16] -> Virtual Channel Select 0 is processed vc_select1[17] -> Virtual Channel Select 1 is processed vc_select2[18] -> Virtual Channel Select 2 is processed vc_select3[19] -> Virtual Channel Select 3 is processed vc_select4[20] -> Virtual Channel Select 4 is processed vc_select5[21] -> Virtual Channel Select 5 is processed vc_select6[22] -> Virtual Channel Select 6 is processed vc_select7[23] -> Virtual Channel Select 7 is processed vc_select8[24] -> Virtual Channel Select 8 is processed vc_select9[25] -> Virtual Channel Select 9 is processed vc_select10[26] -> Virtual Channel Select 10 is processed vc_select11[27] -> Virtual Channel Select 11 is processed vc_select12[28] -> Virtual Channel Select 12 is processed vc_select13[29] -> Virtual Channel Select 13 is processed vc_select14[30] -> Virtual Channel Select 14 is processed vc_select15[31] -> Virtual Channel Select 15 is processed |
| 15 | ENABLE_DT1 | R/W | 0h | Enable processing of dt1 |

Table 9-159. CSI_RX_IF_VBUS2APB_STREAM3_DATA_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 14 | RESERVED | R/W | X | |
| 13-8 | DATATYPE_SELECT1 | R/W | 0h | Second data type format that this stream will process |
| 7 | ENABLE_DT0 | R/W | 0h | Enable processing of dt0 |
| 6 | RESERVED | R/W | X | |
| 5-0 | DATATYPE_SELECT0 | R/W | 0h | First data type format that this stream will process |

9.80 CSI_RX_IF_VBUS2APB_STREAM3_CFG Register (Offset = 40Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_CFG is shown in [Figure 9-77](#) and described in [Table 9-161](#).

Return to [Summary Table](#).

Primary CSI2 Slave Controller Data pixel outputs configuration.

This register is used to configure the output mode.

It is also used to set up some Stream FIFO related settings.

Table 9-160.
CSI_RX_IF_VBUS2APB_STREAM3_CFG Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 440Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 440Ch |

Figure 9-77. CSI_RX_IF_VBUS2APB_STREAM3_CFG Register

| | | | | | | | |
|-----------|------------|----|----|----------|------------|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FIFO_FILL | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | BPP_BYPASS | | | RESERVED | FIFO_MODE | | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | NUM_PIXELS | | | RESERVED | LS_LE_MODE | INTERFACE_M ODE | |
| R/W-X | R/W-0h | | | R/W-X | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-161. CSI_RX_IF_VBUS2APB_STREAM3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | FIFO_FILL | R/W | 0h | Set the FIFO_FILL_LEVEL which is used to hold data in the FIFO until this level is reached before allow data to be pulled. This setting is only used when fifo_mode is set for Large Buffer operation |
| 15 | RESERVED | R/W | X | |
| 14-12 | BPP_BYPASS | R/W | 0h | Force unpacking of any Data type as selected RAW type. 0 - No bypass 1 - unpack as RAW6 2 - unpack as RAW7 3 - unpack as RAW8 4 - unpack as RAW10 5 - unpack as RAW12 6 - unpack as RAW14 7 - unpack as RAW16 |
| 11-10 | RESERVED | R/W | X | |

Table 9-161. CSI_RX_IF_VBUS2APB_STREAM3_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 9-8 | FIFO_MODE | R/W | 0h | Stream FIFO configuration, which must be set in accordance to FIFO sizing, flow control and the relationship between the link and pixel interface data rates. Refer to Use Case descriptions for further guidance on FIFO sizing and valid stream configuration options. 00: Full Line Buffer. Hold data in FIFO until CRC check completes. 01: Large Buffer [Fill Level Controlled]. Hold data in FIFO until FIFO_FILL_LEVEL is reached. 1x: Short Buffer. When pixel output data rate can match link data rate, a small buffer can be used to accommodate CDC, pixel data packing, and data rate matching |
| 7-6 | RESERVED | R/W | X | |
| 5-4 | NUM_PIXELS | R/W | 0h | Number of pixels to output from the stream. Valid values are 1, 2, 4 and 8. The width of the pixel interface and the bits per pixel for the selected datatype will determine how many pixels can be output in a single cycle. Default will be 1 pixel per clock. 00 -> 1 pixel per clock 01 -> 2 pixels per clock 10 -> 4 pixels per clock 11 -> 8 pixels per clock [Reserved] |
| 3-2 | RESERVED | R/W | X | |
| 1 | LS_LE_MODE | R/W | 0h | Enable LS/LE control of HYSNC_VALID output. By default, LS and LE short packets are not required and HYSC_VALID will be generated from the start and end of payload data. |
| 0 | INTERFACE_MODE | R/W | 0h | Select the output configuration. Pixel = 0 [default] Packed = 1 |

9.81 CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL Register (Offset = 410h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL is shown in [Figure 9-78](#) and described in [Table 9-163](#).

Return to [Summary Table](#).

Stream Monitor configuration.

This register is used to configure the CSI2RX Monitors:

Programmable Frame monitor to trigger an event if a truncated frame is detected,

Programmable Timer to trigger an event based on a clock cycle counter after a frame start or frame end,

Programmable line/byte counters to trigger an event at a specific byte in a line.

This register is used to enable/disable CSI2RX programmable interrupt, select the virtual channel for each programmable IT and select the point which will trigger the event.

This register should not be modified while the data path is enabled, nor should any of settings be changed when the respective monitor/counter/timer is enabled.

In these cases, the behaviour is unpredictable.

Hard reset value is 0x00000000, all interrupt generators disabled on Virtual Channel 0.

Table 9-162.
CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4410h |
| CSI_RX_IF_VBUS2APB1 | 0451 4410h |

Figure 9-78. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL Register

| | | | | | | | |
|--------------|--------------|----|--------|--------|-----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_LENGTH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FRAME_MON_EN | FRAME_MON_VC | | | | TIMER_EOF | TIMER_EN | TIMER_VC |
| R/W-0h | R/W-0h | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TIMER_VC | | | LB_EN | LB_VC | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-163. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-16 | FRAME_LENGTH | R/W | 0h | Indicates the frame length in lines to detect truncated frames. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. 0x0000 means truncated frame detection feature disabled |
| 15 | FRAME_MON_EN | R/W | 0h | Enables monitor. This bit must only be set high after the frame_mon_vc and frame_length have been set. |

Table 9-163. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 14-11 | FRAME_MON_VC | R/W | 0h | Indicates virtual channel for monitor. This value must not change while monitor is enabled, i.e. it must only be changed when the frame_mon_en bit is low. |
| 10 | TIMER_EOF | R/W | 0h | Select the starting point of the timer: 0x 0: Start of Frame event on selected virtual channel 0x 1: End of Frame event on selected virtual channel. This value must not change while timer_en is enabled |
| 9 | TIMER_EN | R/W | 0h | Enables timer based interrupt. This bit must only be set high after the timer_eof and timer_vc have been set. |
| 8-5 | TIMER_VC | R/W | 0h | Indicates which VC should be used to generate timer based interrupt. This value must not change while timer_en is enabled. |
| 4 | LB_EN | R/W | 0h | Enables line/byte counter. This bit must only be set high after the lb_vc, line_count and byte_count have been set. |
| 3-0 | LB_VC | R/W | 0h | Indicates which VC should be used to generate line/byte counter interrupt. This value must not change while lb_en is enabled |

9.82 CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_FRAME Register (Offset = 414h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_FRAME is shown in [Figure 9-79](#) and described in [Table 9-165](#).

Return to [Summary Table](#).

Stream Monitor Frame.

Used to observe the current frame number and packet size on monitored virtual channels.

These values are extracted by the CSI2RX from the last frame start short packet data field.

Table 9-164.
CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_FRA
ME Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4414h |
| CSI_RX_IF_VBUS2APB1 | 0451 4414h |

Figure 9-79. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_FRAME Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PACKET_SIZE | | | | | | | | | | | | | | | | NB | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-165. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_FRAME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|-------------------------------------|
| 31-16 | PACKET_SIZE | R | 0h | Size of the current payload |
| 15-0 | NB | R | 0h | Number of the last frame processed. |

9.83 CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_LB Register (Offset = 418h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_LB is shown in [Figure 9-80](#) and described in [Table 9-167](#).

Return to [Summary Table](#).

Stream Monitor Line.

Used to specify the byte and line numbers that will generate an interrupt.

This register must only be modified when the corresponding line/byte enable is disabled.

Table 9-166.
CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_LB
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4418h |
| CSI_RX_IF_VBUS2APB1 | 0451 4418h |

Figure 9-80. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_LB Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_COUNT | | | | | | | | | | | | | | | | BYTE_COUNT | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-167. CSI_RX_IF_VBUS2APB_STREAM3_MONITOR_LB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-16 | LINE_COUNT | R/W | 0h | Indicates the line number to generate an interrupt. [First line of a Frame is line number 0] |
| 15-0 | BYTE_COUNT | R/W | 0h | Indicates the byte number of the line to generate an interrupt. [First byte of a line is byte number 0] |

9.84 CSI_RX_IF_VBUS2APB_STREAM3_TIMER Register (Offset = 41Ch) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_TIMER is shown in [Figure 9-81](#) and described in [Table 9-169](#).

Return to [Summary Table](#).

Stream Timer.

Used to specify the number of clock cycles until the interrupt is triggered after frame start or frame end.

This register must only be modified when the corresponding timer enable is disabled.

Table 9-168.
CSI_RX_IF_VBUS2APB_STREAM3_TIMER
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 441Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 441Ch |

Figure 9-81. CSI_RX_IF_VBUS2APB_STREAM3_TIMER Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COUNT | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-169. CSI_RX_IF_VBUS2APB_STREAM3_TIMER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|------------------------|
| 31-25 | RESERVED | R/W | X | |
| 24-0 | COUNT | R/W | 0h | Number of clock cycles |

9.85 CSI_RX_IF_VBUS2APB_STREAM3_FCC_CFG Register (Offset = 420h) [reset = 0h]

CSI_RX_IF_VBUS2APB_STREAM3_FCC_CFG is shown in [Figure 9-82](#) and described in [Table 9-171](#).

Return to [Summary Table](#).

Stream Frame Capture Control configuration.

Used to specify the frame count value when the CSI2RX must generate interrupts

FCC_START and FCC_STOP.

This register must only be modified when the corresponding frame count enable is disabled.

Table 9-170.
CSI_RX_IF_VBUS2APB_STREAM3_FCC_CFG
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4420h |
| CSI_RX_IF_VBUS2APB1 | 0451 4420h |

Figure 9-82. CSI_RX_IF_VBUS2APB_STREAM3_FCC_CFG Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNT_STOP | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRAME_COUNT_START | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-171. CSI_RX_IF_VBUS2APB_STREAM3_FCC_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-16 | FRAME_COUNT_STOP | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will stop outputting data on the pixel interface. [0x0000 will be continuous frames.] |
| 15-0 | FRAME_COUNT_START | R/W | 0h | Indicates the frame number on which the interrupt should be generated and the stream will start outputting data on the pixel interface. [0x0000 will be the current frame.] |

9.86 CSI_RX_IF_VBUS2APB_STREAM3_FCC_CTRL Register (Offset = 424h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_FCC_CTRL is shown in [Figure 9-83](#) and described in [Table 9-173](#).

Return to [Summary Table](#).

Stream Frame Capture Counter control.

Used to enable / disable the FCC and specify which virtual channel it should operate on.

Table 9-172.
CSI_RX_IF_VBUS2APB_STREAM3_FCC_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4424h |
| CSI_RX_IF_VBUS2APB1 | 0451 4424h |

Figure 9-83. CSI_RX_IF_VBUS2APB_STREAM3_FCC_CTRL Register

| | | | | | | | |
|---------------|----|----|--------|----|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_COUNTER | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | FCC_VC | | | FCC_EN | |
| R/W-X | | | R/W-0h | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-173. CSI_RX_IF_VBUS2APB_STREAM3_FCC_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 31-16 | FRAME_COUNTER | R | 0h | Current Frame number being processed |
| 15-5 | RESERVED | R/W | X | |
| 4-1 | FCC_VC | R/W | 0h | Indicates which VC should be used to generate FCC interrupts. This value must not change while fcc_en is enabled |
| 0 | FCC_EN | R/W | 0h | Frame Capture Counter enable. |

9.87 CSI_RX_IF_VBUS2APB_STREAM3_FIFO_FILL_LVL Register (Offset = 428h) [reset = X]

CSI_RX_IF_VBUS2APB_STREAM3_FIFO_FILL_LVL is shown in [Figure 9-84](#) and described in [Table 9-175](#).

Return to [Summary Table](#).

Stream FIFO fill level monitor. This can operate in 2 modes:

- 1 - Monitor peak fill level until the stream is stopped.
- 2 - Monitor peak fill level when the first FIFO read is made during a frame.

Table 9-174.
CSI_RX_IF_VBUS2APB_STREAM3_FIFO_FILL_LVL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4428h |
| CSI_RX_IF_VBUS2APB1 | 0451 4428h |

Figure 9-84. CSI_RX_IF_VBUS2APB_STREAM3_FIFO_FILL_LVL Register

| | | | | | | | |
|----------|----|--------|----|----------|----|-------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | MODE | | RESERVED | | COUNT | |
| R/W-X | | R/W-0h | | R/W-X | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNT | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-175. CSI_RX_IF_VBUS2APB_STREAM3_FIFO_FILL_LVL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-14 | RESERVED | R/W | X | |
| 13-12 | MODE | R/W | 0h | 00 -> Fill level detection disabled 01 -> Mode 1 10 -> Mode 2 11 -> Reserved |
| 11-10 | RESERVED | R/W | X | |
| 9-0 | COUNT | R | 0h | Peak fill level of FIFO. |

9.88 CSI_RX_IF_VBUS2APB_ASF_INT_STATUS Register (Offset = 900h) [reset = 0h]

CSI_RX_IF_VBUS2APB_ASF_INT_STATUS is shown in [Figure 9-85](#) and described in [Table 9-177](#).

Return to [Summary Table](#).

ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_int_fatal or asf_int_nonfatal signal will be asserted. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 9-176.
CSI_RX_IF_VBUS2APB_ASF_INT_STATUS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4900h |
| CSI_RX_IF_VBUS2APB1 | 0451 4900h |

Figure 9-85. CSI_RX_IF_VBUS2APB_ASF_INT_STATUS Register

| | | | | | | | |
|----------|-------------------|------------------|---------------------|-------------|-------------|---------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORR_ERR | ASF_SRAM_CORR_ERR |
| R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-177. CSI_RX_IF_VBUS2APB_ASF_INT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|-------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W1C | 0h | Integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR | R/W1C | 0h | Protocol error interrupt |
| 4 | ASF_TRANSACTION_ERR | R/W1C | 0h | Transaction timeouts error interrupt |
| 3 | ASF_CSR_ERR | R/W1C | 0h | Configuration and status registers error interrupt |
| 2 | ASF_DAP_ERR | R/W1C | 0h | Data and address paths parity error interrupt |
| 1 | ASF_SRAM_UNCORR_ERR | R/W1C | 0h | SRAM uncorrectable error interrupt |
| 0 | ASF_SRAM_CORR_ERR | R/W1C | 0h | SRAM correctable error interrupt |

9.89 CSI_RX_IF_VBUS2APB_ASF_INT_RAW_STATUS Register (Offset = 904h) [reset = 0h]

CSI_RX_IF_VBUS2APB_ASF_INT_RAW_STATUS is shown in [Figure 9-86](#) and described in [Table 9-179](#).

Return to [Summary Table](#).

ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked status registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt status test register.

Table 9-178.
CSI_RX_IF_VBUS2APB_ASF_INT_RAW_STATUS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4904h |
| CSI_RX_IF_VBUS2APB1 | 0451 4904h |

Figure 9-86. CSI_RX_IF_VBUS2APB_ASF_INT_RAW_STATUS Register

| | | | | | | | |
|----------|-------------------|------------------|---------------------|-------------|-------------|---------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORR_ERR | ASF_SRAM_CORR_ERR |
| R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-179. CSI_RX_IF_VBUS2APB_ASF_INT_RAW_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|-------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W1C | 0h | Integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR | R/W1C | 0h | Protocol error interrupt |
| 4 | ASF_TRANSACTION_ERR | R/W1C | 0h | Transaction timeouts error interrupt |
| 3 | ASF_CSR_ERR | R/W1C | 0h | Configuration and status registers error interrupt |
| 2 | ASF_DAP_ERR | R/W1C | 0h | Data and address paths parity error interrupt |
| 1 | ASF_SRAM_UNCORR_ERR | R/W1C | 0h | SRAM uncorrectable error interrupt |
| 0 | ASF_SRAM_CORR_ERR | R/W1C | 0h | SRAM correctable error interrupt |

9.90 CSI_RX_IF_VBUS2APB_ASF_INT_MASK Register (Offset = 908h) [reset = 7Fh]

CSI_RX_IF_VBUS2APB_ASF_INT_MASK is shown in [Figure 9-87](#) and described in [Table 9-181](#).

Return to [Summary Table](#).

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt status register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt.

Table 9-180.
CSI_RX_IF_VBUS2APB_ASF_INT_MASK Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4908h |
| CSI_RX_IF_VBUS2APB1 | 0451 4908h |

Figure 9-87. CSI_RX_IF_VBUS2APB_ASF_INT_MASK Register

| | | | | | | | |
|----------|------------------------|-----------------------|--------------------------|------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR_MASK | ASF_PROTOCOL_ERR_MASK | ASF_TRANSACTION_ERR_MASK | ASF_CSR_ERR_MASK | ASF_DAP_ERR_MASK | ASF_SRAM_UNCORR_ERR_MASK | ASF_SRAM_CORR_ERR_MASK |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-181. CSI_RX_IF_VBUS2APB_ASF_INT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR_MASK | R/W | 1h | Mask bit for integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR_MASK | R/W | 1h | Mask bit for protocol error interrupt. |
| 4 | ASF_TRANSACTION_ERR_MASK | R/W | 1h | Mask bit for transaction timeouts error interrupt. |
| 3 | ASF_CSR_ERR_MASK | R/W | 1h | Mask bit for configuration and status registers error interrupt. |
| 2 | ASF_DAP_ERR_MASK | R/W | 1h | Mask bit for data and address paths parity error interrupt. |
| 1 | ASF_SRAM_UNCORR_ERR_MASK | R/W | 1h | Mask bit for SRAM uncorrectable error interrupt. |
| 0 | ASF_SRAM_CORR_ERR_MASK | R/W | 1h | Mask bit for SRAM correctable error interrupt. |

9.91 CSI_RX_IF_VBUS2APB_ASF_INT_TEST Register (Offset = 90Ch) [reset = 0h]

CSI_RX_IF_VBUS2APB_ASF_INT_TEST is shown in [Figure 9-88](#) and described in [Table 9-183](#).

Return to [Summary Table](#).

The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) status registers according to mask and will generate interrupt accordingly.

Table 9-182. CSI_RX_IF_VBUS2APB_ASF_INT_TEST Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 490Ch |
| CSI_RX_IF_VBUS2APB1 | 0451 490Ch |

Figure 9-88. CSI_RX_IF_VBUS2APB_ASF_INT_TEST Register

| | | | | | | | |
|----------|------------------------|-----------------------|--------------------------|------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR_TEST | ASF_PROTOCOL_ERR_TEST | ASF_TRANSACTION_ERR_TEST | ASF_CSR_ERR_TEST | ASF_DAP_ERR_TEST | ASF_SRAM_UNCORR_ERR_TEST | ASF_SRAM_CORR_ERR_TEST |
| R-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 9-183. CSI_RX_IF_VBUS2APB_ASF_INT_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR_TEST | W | 0h | Test bit for integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR_TEST | W | 0h | Test bit for protocol error interrupt. |
| 4 | ASF_TRANSACTION_ERR_TEST | W | 0h | Test bit for transaction timeouts error interrupt. |
| 3 | ASF_CSR_ERR_TEST | W | 0h | Test bit for configuration and status registers error interrupt. |
| 2 | ASF_DAP_ERR_TEST | W | 0h | Test bit for data and address paths parity error interrupt. |
| 1 | ASF_SRAM_UNCORR_ERR_TEST | W | 0h | Test bit for SRAM uncorrectable error interrupt. |
| 0 | ASF_SRAM_CORR_ERR_TEST | W | 0h | Test bit for SRAM correctable error interrupt. |

9.92 CSI_RX_IF_VBUS2APB_ASF_FATAL_NONFATAL_SELECT Register (Offset = 910h) [reset = 7Fh]

CSI_RX_IF_VBUS2APB_ASF_FATAL_NONFATAL_SELECT is shown in [Figure 9-89](#) and described in [Table 9-185](#).

Return to [Summary Table](#).

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered.

Table 9-184.
CSI_RX_IF_VBUS2APB_ASF_FATAL_NONFATAL_SELECT Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4910h |
| CSI_RX_IF_VBUS2APB1 | 0451 4910h |

Figure 9-89. CSI_RX_IF_VBUS2APB_ASF_FATAL_NONFATAL_SELECT Register

| | | | | | | | |
|----------|-------------------|------------------|---------------------|-------------|-------------|---------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR | ASF_PROTOCOL_ERR | ASF_TRANSACTION_ERR | ASF_CSR_ERR | ASF_DAP_ERR | ASF_SRAM_UNCORR_ERR | ASF_SRAM_CORR_ERR |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 9-185. CSI_RX_IF_VBUS2APB_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W | 1h | Enable integrity error interrupt as fatal |
| 5 | ASF_PROTOCOL_ERR | R/W | 1h | Enable protocol error interrupt as fatal. |
| 4 | ASF_TRANSACTION_ERR | R/W | 1h | Enable transaction timeouts error interrupt as fatal. |
| 3 | ASF_CSR_ERR | R/W | 1h | Enable configuration and status registers error interrupt as fatal. |
| 2 | ASF_DAP_ERR | R/W | 1h | Enable data and address paths parity error interrupt as fatal. |
| 1 | ASF_SRAM_UNCORR_ERR | R/W | 1h | Enable SRAM uncorrectable error interrupt as fatal. |
| 0 | ASF_SRAM_CORR_ERR | R/W | 1h | Enable SRAM correctable error interrupt as fatal. |

9.93 CSI_RX_IF_VBUS2APB_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 920h) [reset = 0h]

CSI_RX_IF_VBUS2APB_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 9-90](#) and described in [Table 9-187](#).

Return to [Summary Table](#).

Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active.

Table 9-186.
CSI_RX_IF_VBUS2APB_ASF_SRAM_CORR_FAULT_
STATUS Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4920h |
| CSI_RX_IF_VBUS2APB1 | 0451 4920h |

Figure 9-90. CSI_RX_IF_VBUS2APB_ASF_SRAM_CORR_FAULT_STATUS Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|--------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_CORR_FAULT_INST | | | | | | | | ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-187. CSI_RX_IF_VBUS2APB_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-24 | ASF_SRAM_CORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. |
| 23-0 | ASF_SRAM_CORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault. |

9.94 CSI_RX_IF_VBUS2APB_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 924h) [reset = 0h]

CSI_RX_IF_VBUS2APB_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 9-91](#) and described in [Table 9-189](#).

Return to [Summary Table](#).

Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active.

Table 9-188.
CSI_RX_IF_VBUS2APB_ASF_SRAM_UNCORR_FAULT_STATUS Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4924h |
| CSI_RX_IF_VBUS2APB1 | 0451 4924h |

Figure 9-91. CSI_RX_IF_VBUS2APB_ASF_SRAM_UNCORR_FAULT_STATUS Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_SRAM_UNCORR_FAULT_INST | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-189. CSI_RX_IF_VBUS2APB_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-24 | ASF_SRAM_UNCORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. |
| 23-0 | ASF_SRAM_UNCORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault. |

9.95 CSI_RX_IF_VBUS2APB_ASF_SRAM_FAULT_STATS Register (Offset = 928h) [reset = 0h]

CSI_RX_IF_VBUS2APB_ASF_SRAM_FAULT_STATS is shown in [Figure 9-92](#) and described in [Table 9-191](#).

Return to [Summary Table](#).

Statistics register for SRAM faults. Note that this register clears when software writes to any field.

Table 9-190.
CSI_RX_IF_VBUS2APB_ASF_SRAM_FAULT_STATS
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4928h |
| CSI_RX_IF_VBUS2APB1 | 0451 4928h |

Figure 9-92. CSI_RX_IF_VBUS2APB_ASF_SRAM_FAULT_STATS Register

| | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_FAULT_CORR_STATS | | | | | | | | | | | | | | | |
| R/W1C-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-191. CSI_RX_IF_VBUS2APB_ASF_SRAM_FAULT_STATS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|-------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 15-0 | ASF_SRAM_FAULT_CORR_STATS | R/W1C | 0h | Count of number of correctable errors if implemented. Count value will saturate at 0xffff. |

9.96 CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_CTRL Register (Offset = 930h) [reset = X]

CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_CTRL is shown in [Figure 9-93](#) and described in [Table 9-193](#).

Return to [Summary Table](#).

Control register to configure the ASF transaction timeout monitors.

Table 9-192.
CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_CTRL
Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4930h |
| CSI_RX_IF_VBUS2APB1 | 0451 4930h |

Figure 9-93. CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_CTRL Register

| | | | | | | | |
|-------------------|----------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_TRANS_TO_EN | RESERVED | | | | | | |
| R/W-0h | R/W-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-193. CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31 | ASF_TRANS_TO_EN | R/W | 0h | Enable transaction timeout monitoring. |
| 30-16 | RESERVED | R/W | X | |
| 15-0 | ASF_TRANS_TO_CTRL | R/W | 0h | Timer value to use for transaction timeout monitor. |

9.97 CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_MASK Register (Offset = 934h) [reset = X]

CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_MASK is shown in [Figure 9-94](#) and described in [Table 9-195](#).

Return to [Summary Table](#).

Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 9-194.
CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_M
ASK Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4934h |
| CSI_RX_IF_VBUS2APB1 | 0451 4934h |

Figure 9-94. CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_MASK Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ASF_TRANS_T O_FAULT_0_M ASK |
| R/W-X | | | | | | | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-195. CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | ASF_TRANS_TO_FAULT_0_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |

9.98 CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 938h) [reset = X]

CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 9-95](#) and described in [Table 9-197](#).

Return to [Summary Table](#).

Status register for transaction timeouts fault. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit.

Table 9-196.
CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_STATUS Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4938h |
| CSI_RX_IF_VBUS2APB1 | 0451 4938h |

Figure 9-95. CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_STATUS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ASF_TRANS_TO_FAULT_0_STATUS |
| R/W-X | | | | | | | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-197. CSI_RX_IF_VBUS2APB_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | ASF_TRANS_TO_FAULT_0_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |

9.99 CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK Register (Offset = 940h) [reset = X]

CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 9-96](#) and described in [Table 9-199](#).

Return to [Summary Table](#).

Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 9-198.
CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4940h |
| CSI_RX_IF_VBUS2APB1 | 0451 4940h |

Figure 9-96. CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK Register

| | | | | | | | |
|---------------------------|---------------------------|----------------------------|----------------------------|----------------------------|----------------------------|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | ASF_PROTOCOL_FAULT_13_MASK | ASF_PROTOCOL_FAULT_12_MASK | ASF_PROTOCOL_FAULT_11_MASK | ASF_PROTOCOL_FAULT_10_MASK | ASF_PROTOCOL_FAULT_9_MASK | ASF_PROTOCOL_FAULT_8_MASK |
| R/W-X | | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_PROTOCOL_FAULT_7_MASK | ASF_PROTOCOL_FAULT_6_MASK | ASF_PROTOCOL_FAULT_5_MASK | ASF_PROTOCOL_FAULT_4_MASK | ASF_PROTOCOL_FAULT_3_MASK | ASF_PROTOCOL_FAULT_2_MASK | ASF_PROTOCOL_FAULT_1_MASK | ASF_PROTOCOL_FAULT_0_MASK |
| R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-199. CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-14 | RESERVED | R/W | X | |
| 13 | ASF_PROTOCOL_FAULT_13_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 12 | ASF_PROTOCOL_FAULT_12_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 11 | ASF_PROTOCOL_FAULT_11_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 10 | ASF_PROTOCOL_FAULT_10_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 9 | ASF_PROTOCOL_FAULT_9_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 8 | ASF_PROTOCOL_FAULT_8_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 7 | ASF_PROTOCOL_FAULT_7_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |

**Table 9-199. CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions
(continued)**

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|---|
| 6 | ASF_PROTOCOL_FAULT_6_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 5 | ASF_PROTOCOL_FAULT_5_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 4 | ASF_PROTOCOL_FAULT_4_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 3 | ASF_PROTOCOL_FAULT_3_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 2 | ASF_PROTOCOL_FAULT_2_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 1 | ASF_PROTOCOL_FAULT_1_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 0 | ASF_PROTOCOL_FAULT_0_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |

9.100 CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS Register (Offset = 944h) [reset = X]

CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS is shown in [Figure 9-97](#) and described in [Table 9-201](#).

Return to [Summary Table](#).

Status register for protocol faults. If a fault occurs the relevant status bit will be set to 1. Each bit can be cleared by software writing 1 to each bit

Table 9-200.
CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4944h |
| CSI_RX_IF_VBUS2APB1 | 0451 4944h |

Figure 9-97. CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS Register

| | | | | | | | |
|-----------------------------|-----------------------------|------------------------------|------------------------------|------------------------------|------------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | ASF_PROTOCOL_FAULT_13_STATUS | ASF_PROTOCOL_FAULT_12_STATUS | ASF_PROTOCOL_FAULT_11_STATUS | ASF_PROTOCOL_FAULT_10_STATUS | ASF_PROTOCOL_FAULT_9_STATUS | ASF_PROTOCOL_FAULT_8_STATUS |
| R/W-X | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_PROTOCOL_FAULT_7_STATUS | ASF_PROTOCOL_FAULT_6_STATUS | ASF_PROTOCOL_FAULT_5_STATUS | ASF_PROTOCOL_FAULT_4_STATUS | ASF_PROTOCOL_FAULT_3_STATUS | ASF_PROTOCOL_FAULT_2_STATUS | ASF_PROTOCOL_FAULT_1_STATUS | ASF_PROTOCOL_FAULT_0_STATUS |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-201. CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|-------|-------|----------------------------------|
| 31-14 | RESERVED | R/W | X | |
| 13 | ASF_PROTOCOL_FAULT_13_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 12 | ASF_PROTOCOL_FAULT_12_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 11 | ASF_PROTOCOL_FAULT_11_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 10 | ASF_PROTOCOL_FAULT_10_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 9 | ASF_PROTOCOL_FAULT_9_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 8 | ASF_PROTOCOL_FAULT_8_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 7 | ASF_PROTOCOL_FAULT_7_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 6 | ASF_PROTOCOL_FAULT_6_STATUS | R/W1C | 0h | Status bits for protocol faults. |

**Table 9-201. CSI_RX_IF_VBUS2APB_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions
(continued)**

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|-------|-------|----------------------------------|
| 5 | ASF_PROTOCOL_FAULT_5_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 4 | ASF_PROTOCOL_FAULT_4_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 3 | ASF_PROTOCOL_FAULT_3_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 2 | ASF_PROTOCOL_FAULT_2_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 1 | ASF_PROTOCOL_FAULT_1_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 0 | ASF_PROTOCOL_FAULT_0_STATUS | R/W1C | 0h | Status bits for protocol faults. |

9.101 CSI_RX_IF_VBUS2APB_ID_PROD_VER Register (Offset = FFCh) [reset = 50220200h]

CSI_RX_IF_VBUS2APB_ID_PROD_VER is shown in [Figure 9-98](#) and described in [Table 9-203](#).

Return to [Summary Table](#).

This register is hard-coded in order to allow software to identify the product and its release version. The product ID will be fixed for all versions, while the version will be updated as new releases for the CSI2RX product are made.

Table 9-202. CSI_RX_IF_VBUS2APB_ID_PROD_VER Instances

| Instance | Physical Address |
|---------------------|------------------|
| CSI_RX_IF_VBUS2APB0 | 0450 4FFCh |
| CSI_RX_IF_VBUS2APB1 | 0451 4FFCh |

Figure 9-98. CSI_RX_IF_VBUS2APB_ID_PROD_VER Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PRODUCT_ID | | | | | | | | | | | | | | | | VERSION_ID | | | | | | | | | | | | | | | |
| R-5022h | | | | | | | | | | | | | | | | R-200h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-203. CSI_RX_IF_VBUS2APB_ID_PROD_VER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | PRODUCT_ID | R | 5022h | Product Identification Number [IP5022/IP5022A]. |
| 15-0 | VERSION_ID | R | 200h | Product Version Number [R200]. |

9.102 CSI_RX_IF_CP_INTD Registers

Table 9-205 lists the memory-mapped registers for the CSI_RX_IF_CP_INTD registers. All register offset addresses not listed in Table 9-205 should be considered as reserved locations and the register contents should not be modified.

Table 9-204. CSI_RX_IF_CP_INTD Instances

| Instance | Base Address |
|---------------------------------|--------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8000h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8000h |

Table 9-205. CSI_RX_IF_CP_INTD Registers

| Offset | Acronym | Register Name | CSI_RX_IF0_C P_INTD_CFG_I NTD_CFG Physical Address | CSI_RX_IF1_C P_INTD_CFG_I NTD_CFG Physical Address |
|--------|--|----------------------------|--|--|
| 0h | CSI_RX_IF_CP_INTD_REVISION | Revision Register | 0450 8000h | 0451 8000h |
| 10h | CSI_RX_IF_CP_INTD_EOI_REG | End of Interrupt Register | 0450 8010h | 0451 8010h |
| 14h | CSI_RX_IF_CP_INTD_INTR_VECTOR_REG | Interrupt Vector Register | 0450 8014h | 0451 8014h |
| 100h | CSI_RX_IF_CP_INTD_ENABLE_REG_LEVEL_0 | Enable Register 0 | 0450 8100h | 0451 8100h |
| 104h | CSI_RX_IF_CP_INTD_ENABLE_REG_PULSE_0 | Enable Register 1 | 0450 8104h | 0451 8104h |
| 300h | CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_LEVEL_0 | Enable Clear Register 0 | 0450 8300h | 0451 8300h |
| 304h | CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_PULSE_0 | Enable Clear Register 1 | 0450 8304h | 0451 8304h |
| 500h | CSI_RX_IF_CP_INTD_STATUS_REG_LEVEL_0 | Status Register 0 | 0450 8500h | 0451 8500h |
| 504h | CSI_RX_IF_CP_INTD_STATUS_REG_PULSE_0 | Status Register 1 | 0450 8504h | 0451 8504h |
| 700h | CSI_RX_IF_CP_INTD_STATUS_CLR_REG_LEVEL_0 | Status Clear Register 0 | 0450 8700h | 0451 8700h |
| 704h | CSI_RX_IF_CP_INTD_STATUS_CLR_REG_PULSE_0 | Status Clear Register 1 | 0450 8704h | 0451 8704h |
| A80h | CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_LEVEL | Interrupt Vector for level | 0450 8A80h | 0451 8A80h |
| A84h | CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_PULSE | Interrupt Vector for pulse | 0450 8A84h | 0451 8A84h |

9.103 CSI_RX_IF_CP_INTD_REVISION Register (Offset = 0h) [reset = 6690A200h]

CSI_RX_IF_CP_INTD_REVISION is shown in [Figure 9-99](#) and described in [Table 9-207](#).

Return to [Summary Table](#).

Revision Register

Table 9-206. CSI_RX_IF_CP_INTD_REVISION Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8000h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8000h |

Figure 9-99. CSI_RX_IF_CP_INTD_REVISION Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|------|--------|----------|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | | | BU | | FUNCTION | | | | | | | | | |
| R-1h | | | | R-2h | | R-690h | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTLVER | | | | | MAJREV | | | CUSTOM | | MINREV | | | | | |
| R-14h | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-207. CSI_RX_IF_CP_INTD_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-----------------------------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | BU |
| 27-16 | FUNCTION | R | 690h | Module ID |
| 15-11 | RTLVER | R | 14h | RTL revisions |
| 10-8 | MAJREV | R | 2h | Major CSI_RX_IF_CP_INTD_REVISION |
| 7-6 | CUSTOM | R | 0h | Custom CSI_RX_IF_CP_INTD_REVISION |
| 5-0 | MINREV | R | 0h | Minor CSI_RX_IF_CP_INTD_REVISION |

9.104 CSI_RX_IF_CP_INTD_EOI_REG Register (Offset = 10h) [reset = X]

CSI_RX_IF_CP_INTD_EOI_REG is shown in [Figure 9-100](#) and described in [Table 9-209](#).

Return to [Summary Table](#).

End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 9-208. CSI_RX_IF_CP_INTD_EOI_REG
Instances**

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8010h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8010h |

Figure 9-100. CSI_RX_IF_CP_INTD_EOI_REG Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | EOI_VECTOR | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 9-209. CSI_RX_IF_CP_INTD_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|-------------------------|
| 31-8 | RESERVED | R/W | X | |
| 7-0 | EOI_VECTOR | R/W | 0h | End of Interrupt Vector |

9.105 CSI_RX_IF_CP_INTD_INTR_VECTOR_REG Register (Offset = 14h) [reset = 0h]

CSI_RX_IF_CP_INTD_INTR_VECTOR_REG is shown in [Figure 9-101](#) and described in [Table 9-211](#).

Return to [Summary Table](#).

Interrupt Vector Register

Table 9-210.
CSI_RX_IF_CP_INTD_INTR_VECTOR_REG
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8014h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8014h |

Figure 9-101. CSI_RX_IF_CP_INTD_INTR_VECTOR_REG Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTR_VECTOR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-211. CSI_RX_IF_CP_INTD_INTR_VECTOR_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---------------------------|
| 31-0 | INTR_VECTOR | R | 0h | Interrupt Vector Register |

9.106 CSI_RX_IF_CP_INTD_ENABLE_REG_LEVEL_0 Register (Offset = 100h) [reset = X]

CSI_RX_IF_CP_INTD_ENABLE_REG_LEVEL_0 is shown in [Figure 9-102](#) and described in [Table 9-213](#).

Return to [Summary Table](#).

Enable Register 0

Table 9-212.
CSI_RX_IF_CP_INTD_ENABLE_REG_LEVEL_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8100h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8100h |

Figure 9-102. CSI_RX_IF_CP_INTD_ENABLE_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|-------------------------------------|------------------------------------|-------------------------------------|------------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ENABLE_LEVEL_EN_INT_VP1_ERROVERFLOW | ENABLE_LEVEL_EN_INT_VP1_ERRINLNFRM | ENABLE_LEVEL_EN_INT_VP0_ERROVERFLOW | ENABLE_LEVEL_EN_INT_VP0_ERRINLNFRM | ENABLE_LEVEL_EN_FIFO_OVERFLOW |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-213. CSI_RX_IF_CP_INTD_ENABLE_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | ENABLE_LEVEL_EN_INT_VP1_ERROVERFLOW | R/W1S | 0h | Enable Set for level_en_int_vp1_erroverflow |
| 3 | ENABLE_LEVEL_EN_INT_VP1_ERRINLNFRM | R/W1S | 0h | Enable Set for level_en_int_vp1_errInLnFrm |
| 2 | ENABLE_LEVEL_EN_INT_VP0_ERROVERFLOW | R/W1S | 0h | Enable Set for level_en_int_vp0_erroverflow |
| 1 | ENABLE_LEVEL_EN_INT_VP0_ERRINLNFRM | R/W1S | 0h | Enable Set for level_en_int_vp0_errInLnFrm |
| 0 | ENABLE_LEVEL_EN_FIFO_OVERFLOW | R/W1S | 0h | Enable Set for level_en_fifo_overflow |

9.107 CSI_RX_IF_CP_INTD_ENABLE_REG_PULSE_0 Register (Offset = 104h) [reset = X]

CSI_RX_IF_CP_INTD_ENABLE_REG_PULSE_0 is shown in [Figure 9-103](#) and described in [Table 9-215](#).

Return to [Summary Table](#).

Enable Register 1

Table 9-214.
CSI_RX_IF_CP_INTD_ENABLE_REG_PULSE_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8104h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8104h |

Figure 9-103. CSI_RX_IF_CP_INTD_ENABLE_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|-------------------------------------|------------------------------------|-------------------------------------|------------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ENABLE_PULSE_EN_INT_VP1_ERROVERFLOW | ENABLE_PULSE_EN_INT_VP1_ERRINLNFRM | ENABLE_PULSE_EN_INT_VP0_ERROVERFLOW | ENABLE_PULSE_EN_INT_VP0_ERRINLNFRM | ENABLE_PULSE_EN_FIFO_OVERFLOW |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-215. CSI_RX_IF_CP_INTD_ENABLE_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | ENABLE_PULSE_EN_INT_VP1_ERROVERFLOW | R/W1S | 0h | Enable Set for pulse_en_int_vp1_erroverflow |
| 3 | ENABLE_PULSE_EN_INT_VP1_ERRINLNFRM | R/W1S | 0h | Enable Set for pulse_en_int_vp1_errlnLnFrm |
| 2 | ENABLE_PULSE_EN_INT_VP0_ERROVERFLOW | R/W1S | 0h | Enable Set for pulse_en_int_vp0_erroverflow |
| 1 | ENABLE_PULSE_EN_INT_VP0_ERRINLNFRM | R/W1S | 0h | Enable Set for pulse_en_int_vp0_errlnLnFrm |
| 0 | ENABLE_PULSE_EN_FIFO_OVERFLOW | R/W1S | 0h | Enable Set for pulse_en_fifo_overflow |

9.108 CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_LEVEL_0 Register (Offset = 300h) [reset = X]

CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_LEVEL_0 is shown in [Figure 9-104](#) and described in [Table 9-217](#).

Return to [Summary Table](#).

Enable Clear Register 0

Table 9-216.
CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_LEVEL_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8300h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8300h |

Figure 9-104. CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|---|--|---|--|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ENABLE_LEVEL_EN_INT_VP1_ERROVERFLOW_CLR | ENABLE_LEVEL_EN_INT_VP1_ERRINLNFRM_CLR | ENABLE_LEVEL_EN_INT_VP0_ERROVERFLOW_CLR | ENABLE_LEVEL_EN_INT_VP0_ERRINLNFRM_CLR | ENABLE_LEVEL_EN_FIFO_OVERFLOW_CLR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-217. CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | ENABLE_LEVEL_EN_INT_VP1_ERROVERFLOW_CLR | R/W1C | 0h | Enable Clear for level_en_int_vp1_erroroverflow |
| 3 | ENABLE_LEVEL_EN_INT_VP1_ERRINLNFRM_CLR | R/W1C | 0h | Enable Clear for level_en_int_vp1_errInLnFrm |
| 2 | ENABLE_LEVEL_EN_INT_VP0_ERROVERFLOW_CLR | R/W1C | 0h | Enable Clear for level_en_int_vp0_erroroverflow |
| 1 | ENABLE_LEVEL_EN_INT_VP0_ERRINLNFRM_CLR | R/W1C | 0h | Enable Clear for level_en_int_vp0_errInLnFrm |
| 0 | ENABLE_LEVEL_EN_FIFO_OVERFLOW_CLR | R/W1C | 0h | Enable Clear for level_en_fifo_overflow |

9.109 CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_PULSE_0 Register (Offset = 304h) [reset = X]

CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_PULSE_0 is shown in [Figure 9-105](#) and described in [Table 9-219](#).

Return to [Summary Table](#).

Enable Clear Register 1

Table 9-218.
CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_PULSE_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8304h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8304h |

Figure 9-105. CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|---|--|---|--|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ENABLE_PULSE_EN_INT_VP1_ERROVERFLOW_CLR | ENABLE_PULSE_EN_INT_VP1_ERRINLNFRM_CLR | ENABLE_PULSE_EN_INT_VP0_ERROVERFLOW_CLR | ENABLE_PULSE_EN_INT_VP0_ERRINLNFRM_CLR | ENABLE_PULSE_EN_FIFO_OVERFLOW_CLR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-219. CSI_RX_IF_CP_INTD_ENABLE_CLR_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | ENABLE_PULSE_EN_INT_VP1_ERROVERFLOW_CLR | R/W1C | 0h | Enable Clear for pulse_en_int_vp1_erroroverflow |
| 3 | ENABLE_PULSE_EN_INT_VP1_ERRINLNFRM_CLR | R/W1C | 0h | Enable Clear for pulse_en_int_vp1_errInLnFrm |
| 2 | ENABLE_PULSE_EN_INT_VP0_ERROVERFLOW_CLR | R/W1C | 0h | Enable Clear for pulse_en_int_vp0_erroroverflow |
| 1 | ENABLE_PULSE_EN_INT_VP0_ERRINLNFRM_CLR | R/W1C | 0h | Enable Clear for pulse_en_int_vp0_errInLnFrm |
| 0 | ENABLE_PULSE_EN_FIFO_OVERFLOW_CLR | R/W1C | 0h | Enable Clear for pulse_en_fifo_overflow |

9.110 CSI_RX_IF_CP_INTD_STATUS_REG_LEVEL_0 Register (Offset = 500h) [reset = X]

CSI_RX_IF_CP_INTD_STATUS_REG_LEVEL_0 is shown in [Figure 9-106](#) and described in [Table 9-221](#).

Return to [Summary Table](#).

Status Register 0

Table 9-220.
CSI_RX_IF_CP_INTD_STATUS_REG_LEVEL_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8500h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8500h |

Figure 9-106. CSI_RX_IF_CP_INTD_STATUS_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|----------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | STATUS_LEVEL_INT_VP1_ERROVERFLOW | STATUS_LEVEL_INT_VP1_ERRINLNFRM | STATUS_LEVEL_INT_VP0_ERROVERFLOW | STATUS_LEVEL_INT_VP0_ERRINLNFRM | STATUS_LEVEL_FIFO_OVERFLOW |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-221. CSI_RX_IF_CP_INTD_STATUS_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | STATUS_LEVEL_INT_VP1_ERROVERFLOW | R/W1S | 0h | Status ,write 1 to set, for level_en_int_vp1_erroverflow |
| 3 | STATUS_LEVEL_INT_VP1_ERRINLNFRM | R/W1S | 0h | Status ,write 1 to set, for level_en_int_vp1_errlnLnFrm |
| 2 | STATUS_LEVEL_INT_VP0_ERROVERFLOW | R/W1S | 0h | Status ,write 1 to set, for level_en_int_vp0_erroverflow |
| 1 | STATUS_LEVEL_INT_VP0_ERRINLNFRM | R/W1S | 0h | Status ,write 1 to set, for level_en_int_vp0_errlnLnFrm |
| 0 | STATUS_LEVEL_FIFO_OVERFLOW | R/W1S | 0h | Status ,write 1 to set, for level_en_fifo_overflow |

9.111 CSI_RX_IF_CP_INTD_STATUS_REG_PULSE_0 Register (Offset = 504h) [reset = X]

CSI_RX_IF_CP_INTD_STATUS_REG_PULSE_0 is shown in [Figure 9-107](#) and described in [Table 9-223](#).

Return to [Summary Table](#).

Status Register 1

Table 9-222.
CSI_RX_IF_CP_INTD_STATUS_REG_PULSE_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8504h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8504h |

Figure 9-107. CSI_RX_IF_CP_INTD_STATUS_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|----------------------------------|---------------------------------|----------------------------------|---------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | STATUS_PULSE_INT_VP1_ERROVERFLOW | STATUS_PULSE_INT_VP1_ERRINLNFRM | STATUS_PULSE_INT_VP0_ERROVERFLOW | STATUS_PULSE_INT_VP0_ERRINLNFRM | STATUS_PULSE_FIFO_OVERFLOW |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 9-223. CSI_RX_IF_CP_INTD_STATUS_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------------|-------|-------|---|
| 31-5 | RESERVED | R/W | X | |
| 4 | STATUS_PULSE_INT_VP1_ERROVERFLOW | R/W1S | 0h | Status ,write 1 to set, for pulse_en_int_vp1_eroverflow |
| 3 | STATUS_PULSE_INT_VP1_ERRINLNFRM | R/W1S | 0h | Status ,write 1 to set, for pulse_en_int_vp1_errlnLnFrm |
| 2 | STATUS_PULSE_INT_VP0_ERROVERFLOW | R/W1S | 0h | Status ,write 1 to set, for pulse_en_int_vp0_eroverflow |
| 1 | STATUS_PULSE_INT_VP0_ERRINLNFRM | R/W1S | 0h | Status ,write 1 to set, for pulse_en_int_vp0_errlnLnFrm |
| 0 | STATUS_PULSE_FIFO_OVERFLOW | R/W1S | 0h | Status ,write 1 to set, for pulse_en_fifo_overflow |

9.112 CSI_RX_IF_CP_INTD_STATUS_CLR_REG_LEVEL_0 Register (Offset = 700h) [reset = X]

CSI_RX_IF_CP_INTD_STATUS_CLR_REG_LEVEL_0 is shown in [Figure 9-108](#) and described in [Table 9-225](#).

Return to [Summary Table](#).

Status Clear Register 0

Table 9-224.
CSI_RX_IF_CP_INTD_STATUS_CLR_REG_LEVEL_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8700h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8700h |

Figure 9-108. CSI_RX_IF_CP_INTD_STATUS_CLR_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|--------------------------------------|-------------------------------------|--------------------------------------|-------------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | STATUS_LEVEL_INT_VP1_ERROVERFLOW_CLR | STATUS_LEVEL_INT_VP1_ERRINLNFRM_CLR | STATUS_LEVEL_INT_VP0_ERROVERFLOW_CLR | STATUS_LEVEL_INT_VP0_ERRINLNFRM_CLR | STATUS_LEVEL_FIFO_OVERFLOW_CLR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-225. CSI_RX_IF_CP_INTD_STATUS_CLR_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | STATUS_LEVEL_INT_VP1_ERROVERFLOW_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_int_vp1_erroverflow |
| 3 | STATUS_LEVEL_INT_VP1_ERRINLNFRM_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_int_vp1_errlnLnFrm |
| 2 | STATUS_LEVEL_INT_VP0_ERROVERFLOW_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_int_vp0_erroverflow |
| 1 | STATUS_LEVEL_INT_VP0_ERRINLNFRM_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_int_vp0_errlnLnFrm |
| 0 | STATUS_LEVEL_FIFO_OVERFLOW_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_fifo_overflow |

9.113 CSI_RX_IF_CP_INTD_STATUS_CLR_REG_PULSE_0 Register (Offset = 704h) [reset = X]

CSI_RX_IF_CP_INTD_STATUS_CLR_REG_PULSE_0 is shown in [Figure 9-109](#) and described in [Table 9-227](#).

Return to [Summary Table](#).

Status Clear Register 1

Table 9-226.
CSI_RX_IF_CP_INTD_STATUS_CLR_REG_PULSE_0
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8704h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8704h |

Figure 9-109. CSI_RX_IF_CP_INTD_STATUS_CLR_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|--------------------------------------|-------------------------------------|--------------------------------------|-------------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | STATUS_PULSE_INT_VP1_ERROVERFLOW_CLR | STATUS_PULSE_INT_VP1_ERRINLNFRM_CLR | STATUS_PULSE_INT_VP0_ERROVERFLOW_CLR | STATUS_PULSE_INT_VP0_ERRINLNFRM_CLR | STATUS_PULSE_FIFO_OVERFLOW_CLR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 9-227. CSI_RX_IF_CP_INTD_STATUS_CLR_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | STATUS_PULSE_INT_VP1_ERROVERFLOW_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_int_vp1_erroverflow |
| 3 | STATUS_PULSE_INT_VP1_ERRINLNFRM_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_int_vp1_errlnLnFrm |
| 2 | STATUS_PULSE_INT_VP0_ERROVERFLOW_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_int_vp0_erroverflow |
| 1 | STATUS_PULSE_INT_VP0_ERRINLNFRM_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_int_vp0_errlnLnFrm |
| 0 | STATUS_PULSE_FIFO_OVERFLOW_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_fifo_overflow |

9.114 CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_LEVEL Register (Offset = A80h) [reset = 0h]

CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_LEVEL is shown in [Figure 9-110](#) and described in [Table 9-229](#).

Return to [Summary Table](#).

Interrupt Vector for level

Table 9-228.
CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_LEVEL
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8A80h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8A80h |

Figure 9-110. CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_LEVEL Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTR_VECTOR_LEVEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-229. CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_LEVEL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|------------------|
| 31-0 | INTR_VECTOR_LEVEL | R | 0h | Interrupt Vector |

9.115 CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_PULSE Register (Offset = A84h) [reset = 0h]

CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_PULSE is shown in [Figure 9-111](#) and described in [Table 9-231](#).

Return to [Summary Table](#).

Interrupt Vector for pulse

Table 9-230.
CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_PULSE
Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_RX_IF0_CP_INTD_CFG_INTD_CFG | 0450 8A84h |
| CSI_RX_IF1_CP_INTD_CFG_INTD_CFG | 0451 8A84h |

Figure 9-111. CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_PULSE Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTR_VECTOR_PULSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 9-231. CSI_RX_IF_CP_INTD_INTR_VECTOR_REG_PULSE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|------------------|
| 31-0 | INTR_VECTOR_PULSE | R | 0h | Interrupt Vector |

10 CSI_TX_IF Registers

Table 10-1 lists the the CSI_TX_IF memory map. For detailed description of each memory region, refer to the respective register subsection.

Table 10-1. CSI_TX_IF Memory Map

| Name | Start | End | Size |
|---|------------|------------|------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8000h | 02A3 83FFh | 1 KB |
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8400h | 02A3 87FFh | 1 KB |
| CSI_TX_IF0_TX_SHIM_VBUSEP_MMR_CSI2TXIF | 0440 0000h | 0440 0FFFh | 4 KB |
| CSI_TX_IF0_VBUS2APB_WRAP_VBUSEP_APB_CS_I2TX | 0440 4000h | 0440 4FFFh | 4 KB |
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8000h | 0440 8FFFh | 4 KB |

10.1 CSI_TX_IF0_ECC_AGGR_CFG Registers

Table 10-3 lists the memory-mapped registers for the CSI_TX_IF0_ECC_AGGR_CFG registers. All register offset addresses not listed in Table 10-3 should be considered as reserved locations and the register contents should not be modified.

Table 10-2. CSI_TX_IF0_ECC_AGGR_CFG Instances

| Instance | Base Address |
|-------------------------|--------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8000h |

Table 10-3. CSI_TX_IF0_ECC_AGGR_CFG Registers

| Offset | Acronym | Register Name | CSI_TX_IF0_ECC_AGGR_CFG Physical Address |
|---------------|--|---|--|
| 0h | CSI_TX_IF_ECC_AGGR_REV | Aggregator Revision Register | 02A3 8000h |
| 8h | CSI_TX_IF_ECC_AGGR_VECTOR | ECC Vector Register | 02A3 8008h |
| Ch | CSI_TX_IF_ECC_AGGR_STAT | Misc Status | 02A3 800Ch |
| 10h + formula | CSI_TX_IF_ECC_AGGR_RESERVED_SVBUS_y | Reserved Area for Serial VBUS Registers | 02A3 8010h + formula |
| 3Ch | CSI_TX_IF_ECC_AGGR_SEC_EOI_REG | EOI Register | 02A3 803Ch |
| 40h | CSI_TX_IF_ECC_AGGR_SEC_STATUS_REG0 | Interrupt Status Register 0 | 02A3 8040h |
| 80h | CSI_TX_IF_ECC_AGGR_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02A3 8080h |
| C0h | CSI_TX_IF_ECC_AGGR_SEC_ENABLE_CLEAR_REG0 | Interrupt Enable Clear Register 0 | 02A3 80C0h |
| 13Ch | CSI_TX_IF_ECC_AGGR_DED_EOI_REG | EOI Register | 02A3 813Ch |
| 140h | CSI_TX_IF_ECC_AGGR_DED_STATUS_REG0 | Interrupt Status Register 0 | 02A3 8140h |
| 180h | CSI_TX_IF_ECC_AGGR_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02A3 8180h |
| 1C0h | CSI_TX_IF_ECC_AGGR_DED_ENABLE_CLEAR_REG0 | Interrupt Enable Clear Register 0 | 02A3 81C0h |
| 200h | CSI_TX_IF_ECC_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 02A3 8200h |
| 204h | CSI_TX_IF_ECC_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 02A3 8204h |
| 208h | CSI_TX_IF_ECC_AGGR_STATUS_SET | AGGR interrupt CSI_TX_IF_ECC_AGGR_STATUS set Register | 02A3 8208h |
| 20Ch | CSI_TX_IF_ECC_AGGR_STATUS_CLR | AGGR interrupt CSI_TX_IF_ECC_AGGR_STATUS clear Register | 02A3 820Ch |

10.2 CSI_TX_IF_ECC_AGGR_REV Register (Offset = 0h) [reset = 66A0EA00h]

CSI_TX_IF_ECC_AGGR_REV is shown in [Figure 10-1](#) and described in [Table 10-5](#).

Return to [Summary Table](#).

Revision parameters

Table 10-4. CSI_TX_IF_ECC_AGGR_REV Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8000h |

Figure 10-1. CSI_TX_IF_ECC_AGGR_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-5. CSI_TX_IF_ECC_AGGR_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

10.3 CSI_TX_IF_ECC_AGGR_VECTOR Register (Offset = 8h) [reset = X]

CSI_TX_IF_ECC_AGGR_VECTOR is shown in [Figure 10-2](#) and described in [Table 10-7](#).

Return to [Summary Table](#).

ECC Vector Register

Table 10-6. CSI_TX_IF_ECC_AGGR_VECTOR Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8008h |

Figure 10-2. CSI_TX_IF_ECC_AGGR_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_DONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R/W-X | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-7. CSI_TX_IF_ECC_AGGR_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or CSI_TX_IF_ECC_AGGR_STATUS |

10.4 CSI_TX_IF_ECC_AGGR_STAT Register (Offset = Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_STAT is shown in [Figure 10-3](#) and described in [Table 10-9](#).

Return to [Summary Table](#).

Misc Status

Table 10-8. CSI_TX_IF_ECC_AGGR_STAT Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 800Ch |

Figure 10-3. CSI_TX_IF_ECC_AGGR_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | R-3h | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-9. CSI_TX_IF_ECC_AGGR_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 3h | Indicates the number of RAMs serviced by the ECC aggregator |

10.5 CSI_TX_IF_ECC_AGGR_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

CSI_TX_IF_ECC_AGGR_RESERVED_SVBUS_y is shown in [Figure 10-4](#) and described in [Table 10-11](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 10-10.
CSI_TX_IF_ECC_AGGR_RESERVED_SVBUS_y
Instances

| Instance | Physical Address |
|-------------------------|----------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8010h + formula |

Figure 10-4. CSI_TX_IF_ECC_AGGR_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-11. CSI_TX_IF_ECC_AGGR_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

10.6 CSI_TX_IF_ECC_AGGR_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_SEC_EOI_REG is shown in [Figure 10-5](#) and described in [Table 10-13](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 10-12. CSI_TX_IF_ECC_AGGR_SEC_EOI_REG
Instances**

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 803Ch |

Figure 10-5. CSI_TX_IF_ECC_AGGR_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-13. CSI_TX_IF_ECC_AGGR_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

10.7 CSI_TX_IF_ECC_AGGR_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

CSI_TX_IF_ECC_AGGR_SEC_STATUS_REG0 is shown in [Figure 10-6](#) and described in [Table 10-15](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 10-14.
CSI_TX_IF_ECC_AGGR_SEC_STATUS_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8040h |

Figure 10-6. CSI_TX_IF_ECC_AGGR_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------|------------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | FDRAM_RAMECC_PEND | FIFO_RAMECC_PEND | BUSECC_PEND |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-15. CSI_TX_IF_ECC_AGGR_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|-------|-------|---|
| 31-3 | RESERVED | R/W | X | |
| 2 | FDRAM_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for fdram_amecc_pend |
| 1 | FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for fifo_amecc_pend |
| 0 | BUSECC_PEND | R/W1S | 0h | Interrupt Pending Status for busecc_pend |

10.8 CSI_TX_IF_ECC_AGGR_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

CSI_TX_IF_ECC_AGGR_SEC_ENABLE_SET_REG0 is shown in [Figure 10-7](#) and described in [Table 10-17](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 10-16.
CSI_TX_IF_ECC_AGGR_SEC_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8080h |

Figure 10-7. CSI_TX_IF_ECC_AGGR_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | FDRAM_RAMECC_ENABLE_SET | FIFO_RAMECC_ENABLE_SET | BUSECC_ENABLE_SET |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-17. CSI_TX_IF_ECC_AGGR_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | FDRAM_RAMECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for fdram_amecc_pend |
| 1 | FIFO_RAMECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for fifo_amecc_pend |
| 0 | BUSECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for busecc_pend |

10.9 CSI_TX_IF_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

CSI_TX_IF_ECC_AGGR_SEC_ENABLE_CLR_REG0 is shown in [Figure 10-8](#) and described in [Table 10-19](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 10-18.
CSI_TX_IF_ECC_AGGR_SEC_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 80C0h |

Figure 10-8. CSI_TX_IF_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | FDRAM_RAMECC_ENABLE_CLR | FIFO_RAMECC_ENABLE_CLR | BUSECC_ENABLE_CLR |
| R/W-X | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-19. CSI_TX_IF_ECC_AGGR_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | FDRAM_RAMECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for fdram_amecc_pend |
| 1 | FIFO_RAMECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for fifo_amecc_pend |
| 0 | BUSECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for busecc_pend |

10.10 CSI_TX_IF_ECC_AGGR_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_DED_EOI_REG is shown in [Figure 10-9](#) and described in [Table 10-21](#).

[Return to Summary Table.](#)

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

**Table 10-20. CSI_TX_IF_ECC_AGGR_DED_EOI_REG
Instances**

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 813Ch |

Figure 10-9. CSI_TX_IF_ECC_AGGR_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-21. CSI_TX_IF_ECC_AGGR_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

10.11 CSI_TX_IF_ECC_AGGR_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

CSI_TX_IF_ECC_AGGR_DED_STATUS_REG0 is shown in [Figure 10-10](#) and described in [Table 10-23](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 10-22.
CSI_TX_IF_ECC_AGGR_DED_STATUS_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8140h |

Figure 10-10. CSI_TX_IF_ECC_AGGR_DED_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------|------------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | FDRAM_RAMECC_PEND | FIFO_RAMECC_PEND | BUSECC_PEND |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-23. CSI_TX_IF_ECC_AGGR_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|-------|-------|---|
| 31-3 | RESERVED | R/W | X | |
| 2 | FDRAM_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for fdram_amecc_pend |
| 1 | FIFO_RAMECC_PEND | R/W1S | 0h | Interrupt Pending Status for fifo_amecc_pend |
| 0 | BUSECC_PEND | R/W1S | 0h | Interrupt Pending Status for busecc_pend |

10.12 CSI_TX_IF_ECC_AGGR_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

CSI_TX_IF_ECC_AGGR_DED_ENABLE_SET_REG0 is shown in [Figure 10-11](#) and described in [Table 10-25](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 10-24.
CSI_TX_IF_ECC_AGGR_DED_ENABLE_SET_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8180h |

Figure 10-11. CSI_TX_IF_ECC_AGGR_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | FDRAM_RAMECC_ENABLE_SET | FIFO_RAMECC_ENABLE_SET | BUSECC_ENABLE_SET |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-25. CSI_TX_IF_ECC_AGGR_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | FDRAM_RAMECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for fdram_amecc_pend |
| 1 | FIFO_RAMECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for fifo_amecc_pend |
| 0 | BUSECC_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for busecc_pend |

10.13 CSI_TX_IF_ECC_AGGR_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

CSI_TX_IF_ECC_AGGR_DED_ENABLE_CLR_REG0 is shown in [Figure 10-12](#) and described in [Table 10-27](#).

Return to [Summary Table](#).

Interrupt Enable Clear Register 0

Table 10-26.
CSI_TX_IF_ECC_AGGR_DED_ENABLE_CLR_REG0
Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 81C0h |

Figure 10-12. CSI_TX_IF_ECC_AGGR_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|----|-------------------------|------------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | FDRAM_RAMECC_ENABLE_CLR | FIFO_RAMECC_ENABLE_CLR | BUSECC_ENABLE_CLR |
| R/W-X | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-27. CSI_TX_IF_ECC_AGGR_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | FDRAM_RAMECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for fdram_amecc_pend |
| 1 | FIFO_RAMECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for fifo_amecc_pend |
| 0 | BUSECC_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for busecc_pend |

10.14 CSI_TX_IF_ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

CSI_TX_IF_ECC_AGGR_ENABLE_SET is shown in [Figure 10-13](#) and described in [Table 10-29](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 10-28. CSI_TX_IF_ECC_AGGR_ENABLE_SET Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8200h |

Figure 10-13. CSI_TX_IF_ECC_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-29. CSI_TX_IF_ECC_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

10.15 CSI_TX_IF_ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

CSI_TX_IF_ECC_AGGR_ENABLE_CLR is shown in [Figure 10-14](#) and described in [Table 10-31](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 10-30. CSI_TX_IF_ECC_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8204h |

Figure 10-14. CSI_TX_IF_ECC_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-31. CSI_TX_IF_ECC_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

10.16 CSI_TX_IF_ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

CSI_TX_IF_ECC_AGGR_STATUS_SET is shown in [Figure 10-15](#) and described in [Table 10-33](#).

Return to [Summary Table](#).

AGGR interrupt CSI_TX_IF_ECC_AGGR_STATUS set Register

Table 10-32. CSI_TX_IF_ECC_AGGR_STATUS_SET Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 8208h |

Figure 10-15. CSI_TX_IF_ECC_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 10-33. CSI_TX_IF_ECC_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt CSI_TX_IF_ECC_AGGR_STATUS set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt CSI_TX_IF_ECC_AGGR_STATUS set for parity errors |

10.17 CSI_TX_IF_ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_STATUS_CLR is shown in [Figure 10-16](#) and described in [Table 10-35](#).

Return to [Summary Table](#).

AGGR interrupt CSI_TX_IF_ECC_AGGR_STATUS clear Register

Table 10-34. CSI_TX_IF_ECC_AGGR_STATUS_CLR Instances

| Instance | Physical Address |
|-------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_CFG | 02A3 820Ch |

Figure 10-16. CSI_TX_IF_ECC_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 10-35. CSI_TX_IF_ECC_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt CSI_TX_IF_ECC_AGGR_STATUS clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt CSI_TX_IF_ECC_AGGR_STATUS clear for parity errors |

10.18 CSI_TX_IF0_ECC_AGGR_BYTE_CFG Registers

Table 10-37 lists the memory-mapped registers for the CSI_TX_IF0_ECC_AGGR_BYTE_CFG registers. All register offset addresses not listed in Table 10-37 should be considered as reserved locations and the register contents should not be modified.

Table 10-36. CSI_TX_IF0_ECC_AGGR_BYTE_CFG Instances

| Instance | Base Address |
|------------------------------|--------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8400h |

Table 10-37. CSI_TX_IF0_ECC_AGGR_BYTE_CFG Registers

| Offset | Acronym | Register Name | CSI_TX_IF0_ECC_AGGR_BYTE_CFG Physical Address |
|---------------|---|--|---|
| 0h | CSI_TX_IF_ECC_AGGR_BYTE_REV | Aggregator Revision Register | 02A3 8400h |
| 8h | CSI_TX_IF_ECC_AGGR_BYTE_VECTOR | ECC Vector Register | 02A3 8408h |
| Ch | CSI_TX_IF_ECC_AGGR_BYTE_STAT | Misc Status | 02A3 840Ch |
| 10h + formula | CSI_TX_IF_ECC_AGGR_BYTE_RESERVE_D_SVBUS_y | Reserved Area for Serial VBUS Registers | 02A3 8410h + formula |
| 3Ch | CSI_TX_IF_ECC_AGGR_BYTE_SEC_EOI_REG | EOI Register | 02A3 843Ch |
| 40h | CSI_TX_IF_ECC_AGGR_BYTE_SEC_STAT_US_REG0 | Interrupt Status Register 0 | 02A3 8440h |
| 80h | CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02A3 8480h |
| C0h | CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02A3 84C0h |
| 13Ch | CSI_TX_IF_ECC_AGGR_BYTE_DED_EOI_REG | EOI Register | 02A3 853Ch |
| 140h | CSI_TX_IF_ECC_AGGR_BYTE_DED_STAT_US_REG0 | Interrupt Status Register 0 | 02A3 8540h |
| 180h | CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_SET_REG0 | Interrupt Enable Set Register 0 | 02A3 8580h |
| 1C0h | CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_CLR_REG0 | Interrupt Enable Clear Register 0 | 02A3 85C0h |
| 200h | CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_SET | AGGR interrupt enable set Register | 02A3 8600h |
| 204h | CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_CLR | AGGR interrupt enable clear Register | 02A3 8604h |
| 208h | CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_SET | AGGR interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS set Register | 02A3 8608h |
| 20Ch | CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_CLR | AGGR interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS clear Register | 02A3 860Ch |

10.19 CSI_TX_IF_ECC_AGGR_BYTE_REV Register (Offset = 0h) [reset = 66A0EA00h]

CSI_TX_IF_ECC_AGGR_BYTE_REV is shown in [Figure 10-17](#) and described in [Table 10-39](#).

[Return to Summary Table.](#)

Revision parameters

Table 10-38. CSI_TX_IF_ECC_AGGR_BYTE_REV Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8400h |

Figure 10-17. CSI_TX_IF_ECC_AGGR_BYTE_REV Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|-----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | MODULE_ID | | | | | | | | | | | |
| R-1h | | R-2h | | R-6A0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REVRTL | | | | | REVMAJ | | | CUSTOM | | REVMIN | | | | | |
| R-1Dh | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-39. CSI_TX_IF_ECC_AGGR_BYTE_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | MODULE_ID | R | 6A0h | Module ID |
| 15-11 | REVRTL | R | 1Dh | RTL version |
| 10-8 | REVMAJ | R | 2h | Major version |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | REVMIN | R | 0h | Minor version |

10.20 CSI_TX_IF_ECC_AGGR_BYTE_VECTOR Register (Offset = 8h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_VECTOR is shown in [Figure 10-18](#) and described in [Table 10-41](#).

Return to [Summary Table](#).

ECC Vector Register

Table 10-40.
CSI_TX_IF_ECC_AGGR_BYTE_VECTOR Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8408h |

Figure 10-18. CSI_TX_IF_ECC_AGGR_BYTE_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_DONE |
| R/W-X | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R/W-X | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-41. CSI_TX_IF_ECC_AGGR_BYTE_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|---|
| 31-25 | RESERVED | R/W | X | |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read address |
| 15 | RD_SVBUS | R/W1S | 0h | Write 1 to trigger a read on the serial VBUS |
| 14-11 | RESERVED | R/W | X | |
| 10-0 | ECC_VECTOR | R/W | 0h | Value written to select the corresponding ECC RAM for control or CSI_TX_IF_ECC_AGGR_BYTE_STATUS |

10.21 CSI_TX_IF_ECC_AGGR_BYTE_STAT Register (Offset = Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_STAT is shown in [Figure 10-19](#) and described in [Table 10-43](#).

Return to [Summary Table](#).

Misc Status

Table 10-42. CSI_TX_IF_ECC_AGGR_BYTE_STAT Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 840Ch |

Figure 10-19. CSI_TX_IF_ECC_AGGR_BYTE_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | NUM_RAMs | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | | | | R-4h | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-43. CSI_TX_IF_ECC_AGGR_BYTE_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | X | |
| 10-0 | NUM_RAMs | R | 4h | Indicates the number of RAMs serviced by the ECC aggregator |

10.22 CSI_TX_IF_ECC_AGGR_BYTE_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

CSI_TX_IF_ECC_AGGR_BYTE_RESERVED_SVBUS_y is shown in [Figure 10-20](#) and described in [Table 10-45](#).

Return to [Summary Table](#).

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 10-44.
CSI_TX_IF_ECC_AGGR_BYTE_RESERVED_SVBUS
_y Instances

| Instance | Physical Address |
|------------------------------|----------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8410h + formula |

Figure 10-20. CSI_TX_IF_ECC_AGGR_BYTE_RESERVED_SVBUS_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-45. CSI_TX_IF_ECC_AGGR_BYTE_RESERVED_SVBUS_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---------------------------|
| 31-0 | DATA | R/W | 0h | Serial VBUS register data |

10.23 CSI_TX_IF_ECC_AGGR_BYTE_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_SEC_EOI_REG is shown in [Figure 10-21](#) and described in [Table 10-47](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 10-46.
CSI_TX_IF_ECC_AGGR_BYTE_SEC_EOI_REG
Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 843Ch |

Figure 10-21. CSI_TX_IF_ECC_AGGR_BYTE_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-47. CSI_TX_IF_ECC_AGGR_BYTE_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

10.24 CSI_TX_IF_ECC_AGGR_BYTE_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_SEC_STATUS_REG0 is shown in [Figure 10-22](#) and described in [Table 10-49](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 10-48.
CSI_TX_IF_ECC_AGGR_BYTE_SEC_STATUS_REG0
Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8440h |

Figure 10-22. CSI_TX_IF_ECC_AGGR_BYTE_SEC_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|------------------|------------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RAM_RAMECC3_PEND | RAM_RAMECC2_PEND | RAM_RAMECC1_PEND | RAM_RAMECC0_PEND |
| R/W-X | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-49. CSI_TX_IF_ECC_AGGR_BYTE_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3 | RAM_RAMECC3_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc3_pend |
| 2 | RAM_RAMECC2_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc2_pend |
| 1 | RAM_RAMECC1_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc1_pend |
| 0 | RAM_RAMECC0_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc0_pend |

10.25 CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_SET_REG0 is shown in [Figure 10-23](#) and described in [Table 10-51](#).

Return to [Summary Table](#).

Interrupt Enable Set Register 0

Table 10-50.
CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_SET_
REG0 Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8480h |

Figure 10-23. CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RAM_RAMECC3_ENABLE_SET | RAM_RAMECC2_ENABLE_SET | RAM_RAMECC1_ENABLE_SET | RAM_RAMECC0_ENABLE_SET |
| R/W-X | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-51. CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3 | RAM_RAMECC3_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc3_pend |
| 2 | RAM_RAMECC2_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc2_pend |
| 1 | RAM_RAMECC1_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc1_pend |
| 0 | RAM_RAMECC0_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc0_pend |

10.26 CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_CLR_REG0 is shown in [Figure 10-24](#) and described in [Table 10-53](#).

[Return to Summary Table.](#)

Interrupt Enable Clear Register 0

Table 10-52.
CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_CLR_
REG0 Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 84C0h |

Figure 10-24. CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RAM_RAMECC3_ENABLE_CLR | RAM_RAMECC2_ENABLE_CLR | RAM_RAMECC1_ENABLE_CLR | RAM_RAMECC0_ENABLE_CLR |
| R/W-X | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-53. CSI_TX_IF_ECC_AGGR_BYTE_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3 | RAM_RAMECC3_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc3_pend |
| 2 | RAM_RAMECC2_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc2_pend |
| 1 | RAM_RAMECC1_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc1_pend |
| 0 | RAM_RAMECC0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc0_pend |

10.27 CSI_TX_IF_ECC_AGGR_BYTE_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_DED_EOI_REG is shown in [Figure 10-25](#) and described in [Table 10-55](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 10-54.
CSI_TX_IF_ECC_AGGR_BYTE_DED_EOI_REG
Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 853Ch |

Figure 10-25. CSI_TX_IF_ECC_AGGR_BYTE_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-55. CSI_TX_IF_ECC_AGGR_BYTE_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--------------|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI_WR | R/W1S | 0h | EOI Register |

10.28 CSI_TX_IF_ECC_AGGR_BYTE_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_DED_STATUS_REG0 is shown in [Figure 10-26](#) and described in [Table 10-57](#).

Return to [Summary Table](#).

Interrupt Status Register 0

Table 10-56.
CSI_TX_IF_ECC_AGGR_BYTE_DED_STATUS_REG0
Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8540h |

Figure 10-26. CSI_TX_IF_ECC_AGGR_BYTE_DED_STATUS_REG0 Register

| | | | | | | | |
|----------|----|----|----|------------------|------------------|------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RAM_RAMECC3_PEND | RAM_RAMECC2_PEND | RAM_RAMECC1_PEND | RAM_RAMECC0_PEND |
| R/W-X | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-57. CSI_TX_IF_ECC_AGGR_BYTE_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|-------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3 | RAM_RAMECC3_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc3_pend |
| 2 | RAM_RAMECC2_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc2_pend |
| 1 | RAM_RAMECC1_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc1_pend |
| 0 | RAM_RAMECC0_PEND | R/W1S | 0h | Interrupt Pending Status for ram_amecc0_pend |

10.29 CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_SET_REG0 is shown in [Figure 10-27](#) and described in [Table 10-59](#).

[Return to Summary Table.](#)

Interrupt Enable Set Register 0

Table 10-58.
CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_SET_
REG0 Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8580h |

Figure 10-27. CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_SET_REG0 Register

| | | | | | | | |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RAM_RAMECC3_ENABLE_SET | RAM_RAMECC2_ENABLE_SET | RAM_RAMECC1_ENABLE_SET | RAM_RAMECC0_ENABLE_SET |
| R/W-X | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-59. CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3 | RAM_RAMECC3_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc3_pend |
| 2 | RAM_RAMECC2_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc2_pend |
| 1 | RAM_RAMECC1_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc1_pend |
| 0 | RAM_RAMECC0_ENABLE_SET | R/W1S | 0h | Interrupt Enable Set Register for ram_amecc0_pend |

10.30 CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_CLR_REG0 is shown in [Figure 10-28](#) and described in [Table 10-61](#).

[Return to Summary Table.](#)

Interrupt Enable Clear Register 0

Table 10-60.
CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_CLR_
REG0 Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 85C0h |

Figure 10-28. CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_CLR_REG0 Register

| | | | | | | | |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | RAM_RAMECC3_ENABLE_CLR | RAM_RAMECC2_ENABLE_CLR | RAM_RAMECC1_ENABLE_CLR | RAM_RAMECC0_ENABLE_CLR |
| R/W-X | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-61. CSI_TX_IF_ECC_AGGR_BYTE_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|-------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3 | RAM_RAMECC3_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc3_pend |
| 2 | RAM_RAMECC2_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc2_pend |
| 1 | RAM_RAMECC1_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc1_pend |
| 0 | RAM_RAMECC0_ENABLE_CLR | R/W1C | 0h | Interrupt Enable Clear Register for ram_amecc0_pend |

10.31 CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_SET is shown in [Figure 10-29](#) and described in [Table 10-63](#).

Return to [Summary Table](#).

AGGR interrupt enable set Register

Table 10-62.
CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_SET Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8600h |

Figure 10-29. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-63. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1S | 0h | interrupt enable set for svbus timeout errors |
| 0 | PARITY | R/W1S | 0h | interrupt enable set for parity errors |

10.32 CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_CLR is shown in [Figure 10-30](#) and described in [Table 10-65](#).

Return to [Summary Table](#).

AGGR interrupt enable clear Register

Table 10-64.
CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_CLR Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8604h |

Figure 10-30. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-65. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | TIMEOUT | R/W1C | 0h | interrupt enable clear for svbus timeout errors |
| 0 | PARITY | R/W1C | 0h | interrupt enable clear for parity errors |

10.33 CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_SET is shown in [Figure 10-31](#) and described in [Table 10-67](#).

Return to [Summary Table](#).

AGGR interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS set Register

Table 10-66.
CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_SET
Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 8608h |

Figure 10-31. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wincr-0h | | R/Wincr-0h | |

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -n = value after reset

Table 10-67. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wincr | 0h | interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS set for svbus timeout errors |
| 1-0 | PARITY | R/Wincr | 0h | interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS set for parity errors |

10.34 CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_CLR is shown in [Figure 10-32](#) and described in [Table 10-69](#).

Return to [Summary Table](#).

AGGR interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS clear Register

Table 10-68.
CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_CLR Instances

| Instance | Physical Address |
|------------------------------|------------------|
| CSI_TX_IF0_ECC_AGGR_BYTE_CFG | 02A3 860Ch |

Figure 10-32. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|------------|----|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R/W-X | | | | R/Wdecr-0h | | R/Wdecr-0h | |

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; -n = value after reset

Table 10-69. CSI_TX_IF_ECC_AGGR_BYTE_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|---------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3-2 | TIMEOUT | R/Wdecr | 0h | interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS clear for svbus timeout errors |
| 1-0 | PARITY | R/Wdecr | 0h | interrupt CSI_TX_IF_ECC_AGGR_BYTE_STATUS clear for parity errors |

10.35 CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF Registers

Table 10-71 lists the memory-mapped registers for the CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF registers. All register offset addresses not listed in Table 10-71 should be considered as reserved locations and the register contents should not be modified.

Table 10-70.
CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF
Instances

| Instance | Base Address |
|---------------------------------------|--------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0000h |

Table 10-71. CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF Registers

| Offset | Acronym | Register Name | CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF Physical Address |
|----------------|---|--|--|
| 0h | CSI_TX_IF_CSITX_ID | PID | 0440 0000h |
| 4h | CSI_TX_IF_COLOR_CNTL | color bar control register | 0440 0004h |
| 8h | CSI_TX_IF_COLOR_PARAM | color bar frame parameters | 0440 0008h |
| Ch | CSI_TX_IF_COLOR_START_DELAY | delay from starting first line after enabling | 0440 000Ch |
| 20h | CSI_TX_IF_COLOR_LINE_DELAY | last line start to next line start delay | 0440 0020h |
| 24h | CSI_TX_IF_COLOR_FRAME_DELAY | line start to next frame start delay | 0440 0024h |
| 28h | CSI_TX_IF_RETRANS_CNTL | retransmit control register | 0440 0028h |
| 2Ch | CSI_TX_IF_CONTROL1 | control register for csi tx wrapper | 0440 002Ch |
| 40h + formula | CSI_TX_IF_F2F_DELAY_y | delay in number of main clock cycles from start of last frame line to start of next frame first line | 0440 0040h + formula |
| 100h + formula | CSI_TX_IF_DMACNTX_j | DMA Channel Context | 0440 0100h + formula |
| 104h + formula | CSI_TX_IF_L2L_DELAY_j | delay in main clock cycles from start of one line to start of another line | 0440 0104h + formula |

10.36 CSI_TX_IF_CSITX_ID Register (Offset = 0h) [reset = 64784900h]

CSI_TX_IF_CSITX_ID is shown in [Figure 10-33](#) and described in [Table 10-73](#).

Return to [Summary Table](#).

PID

Table 10-72. CSI_TX_IF_CSITX_ID Instances

| Instance | Physical Address |
|--------------------------------------|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSITXIF | 0440 0000h |

Figure 10-33. CSI_TX_IF_CSITX_ID Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|------|--------|--------|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | | | BU | | FUNC | | | | | | | | | |
| R-1h | | | | R-2h | | R-478h | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTLVER | | | | | MAJREV | | | CUSTOM | | MINREV | | | | | |
| R-9h | | | | | R-1h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-73. CSI_TX_IF_CSITX_ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---------------------------|
| 31-30 | SCHEME | R | 1h | scheme |
| 29-28 | BU | R | 2h | bu |
| 27-16 | FUNC | R | 478h | function |
| 15-11 | RTLVER | R | 9h | rtl version |
| 10-8 | MAJREV | R | 1h | major CSI_TX_IF_REVISION |
| 7-6 | CUSTOM | R | 0h | custom CSI_TX_IF_REVISION |
| 5-0 | MINREV | R | 0h | min CSI_TX_IF_REVISION |

10.37 CSI_TX_IF_COLOR_CNTL Register (Offset = 4h) [reset = X]

CSI_TX_IF_COLOR_CNTL is shown in [Figure 10-34](#) and described in [Table 10-75](#).

[Return to Summary Table.](#)

color bar control register

Table 10-74. CSI_TX_IF_COLOR_CNTL Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0004h |

Figure 10-34. CSI_TX_IF_COLOR_CNTL Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|--------|----|----|----------|----|----|----|--------|--------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | VCHNL | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | DTYPE | | | RESERVED | | | | | EN | | |
| R/W-X | | | | | R/W-0h | | | R/W-X | | | | | R/W-0h | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-75. CSI_TX_IF_COLOR_CNTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------------------------|
| 31-20 | RESERVED | R/W | X | |
| 19-16 | VCHNL | R/W | 0h | color bar virtual channel |
| 15-11 | RESERVED | R/W | X | |
| 10-08 | DTYPE | R/W | 0h | color bar data type, data sel |
| 7-1 | RESERVED | R/W | X | |
| 0 | EN | R/W | 0h | 1: enable |

10.38 CSI_TX_IF_COLOR_PARAM Register (Offset = 8h) [reset = X]

CSI_TX_IF_COLOR_PARAM is shown in [Figure 10-35](#) and described in [Table 10-77](#).

Return to [Summary Table](#).

color bar frame parameters

Table 10-76. CSI_TX_IF_COLOR_PARAM Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0008h |

Figure 10-35. CSI_TX_IF_COLOR_PARAM Register

| | | | | | | | |
|----------|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | IH_CFG | | | |
| R/W-X | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IH_CFG | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | IW_CFG | | | |
| R/W-X | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IW_CFG | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-77. CSI_TX_IF_COLOR_PARAM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-29 | RESERVED | R/W | X | |
| 28-16 | IH_CFG | R/W | 0h | input height in units of pixels minus 1. |
| 15-13 | RESERVED | R/W | X | |
| 12-00 | IW_CFG | R/W | 0h | input width in units of pixels minus 1. |

10.39 CSI_TX_IF_COLOR_START_DELAY Register (Offset = Ch) [reset = 0h]

CSI_TX_IF_COLOR_START_DELAY is shown in [Figure 10-36](#) and described in [Table 10-79](#).

Return to [Summary Table](#).

delay from starting first line after enabling

Table 10-78. CSI_TX_IF_COLOR_START_DELAY Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 000Ch |

Figure 10-36. CSI_TX_IF_COLOR_START_DELAY Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_DELAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-79. CSI_TX_IF_COLOR_START_DELAY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | LINE_DELAY | R/W | 0h | delay in terms of main clock cycles before sending first line after enabling. |

10.40 CSI_TX_IF_COLOR_LINE_DELAY Register (Offset = 20h) [reset = 0h]

CSI_TX_IF_COLOR_LINE_DELAY is shown in [Figure 10-37](#) and described in [Table 10-81](#).

Return to [Summary Table](#).

last line start to next line start delay

**Table 10-80. CSI_TX_IF_COLOR_LINE_DELAY
Instances**

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_ CSI2TXIF | 0440 0020h |

Figure 10-37. CSI_TX_IF_COLOR_LINE_DELAY Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_DELAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-81. CSI_TX_IF_COLOR_LINE_DELAY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 31-0 | LINE_DELAY | R/W | 0h | delay in terms of main clock cycles from line start to next line start |

10.41 CSI_TX_IF_COLOR_FRAME_DELAY Register (Offset = 24h) [reset = 0h]

CSI_TX_IF_COLOR_FRAME_DELAY is shown in [Figure 10-38](#) and described in [Table 10-83](#).

Return to [Summary Table](#).

line start to next frame start delay

Table 10-82. CSI_TX_IF_COLOR_FRAME_DELAY Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0024h |

Figure 10-38. CSI_TX_IF_COLOR_FRAME_DELAY Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRAME_DELAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-83. CSI_TX_IF_COLOR_FRAME_DELAY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---|
| 31-0 | FRAME_DELAY | R/W | 0h | delay in terms of main clock cycles from last line start to start of next frame |

10.42 CSI_TX_IF_RETRANS_CNTL Register (Offset = 28h) [reset = X]

CSI_TX_IF_RETRANS_CNTL is shown in [Figure 10-39](#) and described in [Table 10-85](#).

[Return to Summary Table.](#)

retransmit control register

Table 10-84. CSI_TX_IF_RETRANS_CNTL Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_ CSI2TXIF | 0440 0028h |

Figure 10-39. CSI_TX_IF_RETRANS_CNTL Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|--------|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | VC1 | | | | RESERVED | | | | | | | | | | | | VC0 | | | |
| R/W-X | | | | | | | | | | | | R/W-1h | | | | R/W-X | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-85. CSI_TX_IF_RETRANS_CNTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-20 | RESERVED | R/W | X | |
| 19-16 | VC1 | R/W | 1h | virtual channel of csi tx to send out stream4 interface |
| 15-4 | RESERVED | R/W | X | |
| 3-0 | VC0 | R/W | 0h | virtual channel of csi tx to send out stream3 interface |

10.43 CSI_TX_IF_CONTROL1 Register (Offset = 2Ch) [reset = X]

CSI_TX_IF_CONTROL1 is shown in [Figure 10-40](#) and described in [Table 10-87](#).

[Return to Summary Table.](#)

control register for csi tx wrapper

Table 10-86. CSI_TX_IF_CONTROL1 Instances

| Instance | Physical Address |
|---------------------------------------|------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 002Ch |

Figure 10-40. CSI_TX_IF_CONTROL1 Register

| | | | | | | | |
|----------|----|----|----|--------------|--------------|--------------|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | STREAM3_IDLE | STREAM2_IDLE | STREAM1_IDLE | STREAM0_IDLE |
| R/W-X | | | | R-1h | R-1h | R-1h | R-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PIXEL_RESET |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-87. CSI_TX_IF_CONTROL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-12 | RESERVED | R/W | X | |
| 11 | STREAM3_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 10 | STREAM2_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 9 | STREAM1_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 8 | STREAM0_IDLE | R | 1h | indicates if stream interface is idle(1) or not(0) |
| 7-1 | RESERVED | R/W | X | |
| 0 | PIXEL_RESET | R/W | 0h | reset for the pixeal interface. 0=reset, 1 not in reset. this should be asserted till after you program the csi controller configuration registers |

10.44 CSI_TX_IF_F2F_DELAY_y Register (Offset = 40h + formula) [reset = 0h]

CSI_TX_IF_F2F_DELAY_y is shown in [Figure 10-41](#) and described in [Table 10-89](#).

Return to [Summary Table](#).

last line start to next frame start. Configuration for each of 16 virtual channels.

Offset = 40h + (y * 4h); where y = 0h to Fh

Table 10-88. CSI_TX_IF_F2F_DELAY_y Instances

| Instance | Physical Address |
|---------------------------------------|----------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0040h + formula |

Figure 10-41. CSI_TX_IF_F2F_DELAY_y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DELAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-89. CSI_TX_IF_F2F_DELAY_y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|---|
| 31-00 | DELAY | R/W | 0h | counter value delay of last line start of frame to first line of next frame |

10.45 CSI_TX_IF_DMANTX_j Register (Offset = 100h + formula) [reset = X]

dmaCntx_j is shown in [Figure 10-42](#) and described in [Table 10-91](#).

Return to [Summary Table](#).

DMA Channel Context. Configuration for each of 32 possible threads. Illegal to program 2 threads with same virtual channel and data type values

Offset = 100h + (j * 20h); where j = 0h to 1Fh

Table 10-90. CSI_TX_IF_DMANTX_j Instances

| Instance | Physical Address |
|---------------------------------------|----------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0100h + formula |

Figure 10-42. CSI_TX_IF_DMANTX_j Register

| | | | | | | | |
|------------|----------|------------|------------|-----------------|------------|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | YUV420_CFG | YUV422_MODE_CFG | YUV422_CFG | RESERVED | |
| R/W-X | | | R/W-0h | R/W-3h | R/W-0h | R/W-X | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PACK12_CFG | RESERVED | SIZE_CFG | | RESERVED | | | |
| R/W-0h | R/W-X | R/W-2h | | R/W-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | VIRTCH_CFG | |
| R/W-X | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VIRTCH_CFG | | DATSEL_CFG | | | | | |
| R/W-0h | | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-91. CSI_TX_IF_DMANTX_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|---|
| 31-29 | RESERVED | R/W | X | |
| 28 | YUV420_CFG | R/W | 0h | yuv422 format enable 0: not yuv420 /n 1: yuv420 |
| 27-26 | YUV422_MODE_CFG | R/W | 3h | yuv422 mode 00:UYVY, 01:VYUY, 10:YUYV, 11:YVYU |
| 25 | YUV422_CFG | R/W | 0h | yuv422 format enable 0: not yuv422 /n 1: yuv422 |
| 24 | RESERVED | R/W | X | |
| 23 | PACK12_CFG | R/W | 0h | pack12 format enable 0. used in conjunction with size for proper packing: not pack12 /n 1: pack12 |
| 22 | RESERVED | R/W | X | |

Table 10-91. CSI_TX_IF_DMACNTX_j Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 21-20 | SIZE_CFG | R/W | 2h | data size shift when unpacking, 00=8, 01=16, 10=32, 11=RSVD |
| 19-10 | RESERVED | R/W | X | |
| 9-06 | VIRTCH_CFG | R/W | 0h | CSI virtual channel index. Supplied by MIPI CSI protocol to DPHY. For CSilver1.3 program 2MSb==0 |
| 5-00 | DATSEL_CFG | R/W | 0h | CSI data type index. Supplied by MIPI CSI protocol to DPHY |

10.46 CSI_TX_IF_L2L_DELAY_j Register (Offset = 104h + formula) [reset = 0h]

CSI_TX_IF_L2L_DELAY_j is shown in [Figure 10-43](#) and described in [Table 10-93](#).

Return to [Summary Table](#).

line to line delay. Configuration for each of 32 possible channel contexts.

Offset = 104h + (j * 20h); where j = 0h to 1Fh

Table 10-92. CSI_TX_IF_L2L_DELAY_j Instances

| Instance | Physical Address |
|---------------------------------------|----------------------|
| CSI_TX_IF0_TX_SHIM_VBUSP_MMR_CSI2TXIF | 0440 0104h + formula |

Figure 10-43. CSI_TX_IF_L2L_DELAY_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DELAY | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-93. CSI_TX_IF_L2L_DELAY_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|--|
| 31-00 | DELAY | R/W | 0h | counter value delay line start to next line start within a frame |

10.47 CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Registers

Table 10-95 lists the memory-mapped registers for the CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX registers. All register offset addresses not listed in Table 10-95 should be considered as reserved locations and the register contents should not be modified.

Table 10-94. CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Instances

| Instance | Base Address |
|---|--------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX | 0440 4000h |

Table 10-95. CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Registers

| Offset | Acronym | Register Name | CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Physical Address |
|--------|--|--|--|
| 0h | CSI_TX_IF_DEVICE_CONFIG | CSI2 Transmitter Device Configuration Register | 0440 4000h |
| 4h | CSI_TX_IF_STATUS | CSI2 Transmitter Status Register | 0440 4004h |
| 8h | CSI_TX_IF_IRQ | CSI2 Transmitter Interrupt Register. Write '1' to clear | 0440 4008h |
| Ch | CSI_TX_IF_IRQ_MASK | CSI2 Transmitter Interrupt Mask Set Register | 0440 400Ch |
| 10h | CSI_TX_IF_DPHY_IRQ | DPHY Transmitter Interrupt Status. Level sensitive interrupt bits driven by DPHY signal pins. Write 1 to clear | 0440 4010h |
| 14h | CSI_TX_IF_DPHY_IRQ_MASK | DPHY Transmitter Interrupt Mask. Writing '1' to any bit enables interrupt generation when signal CSI_TX_IF_IRQ is set and interrupts are enabled. | 0440 4014h |
| 20h | CSI_TX_IF_TX_CONF | CSI2 Transmitter Configuration Register | 0440 4020h |
| 24h | CSI_TX_IF_WAIT_BURST_TIME | CSI2 Transmitter DPHY Wait Time configuration Register | 0440 4024h |
| 28h | CSI_TX_IF_DPHY_CFG | CSI2 Transmitter DPHY Lane Enable configuration Register | 0440 4028h |
| 2Ch | CSI_TX_IF_DPHY_CLK_WAKEUP | CSI2 Transmitter DPHY Clock Lane wakeup time configuration Register | 0440 402Ch |
| 30h | CSI_TX_IF_DPHY_ULPS_WAKEUP | CSI2 Transmitter DPHY Data Lane wakeup time configuration Register | 0440 4030h |
| 40h | CSI_TX_IF_VC0_CFG | CSI2 Transmitter Virtual Channel 0 Configuration Register | 0440 4040h |
| 44h | CSI_TX_IF_VC1_CFG | CSI2 Transmitter Virtual Channel 1 Configuration Register | 0440 4044h |
| 48h | CSI_TX_IF_VC2_CFG | CSI2 Transmitter Virtual Channel 2 Configuration Register | 0440 4048h |
| 4Ch | CSI_TX_IF_VC3_CFG | CSI2 Transmitter Virtual Channel 3 Configuration Register | 0440 404Ch |
| 50h | CSI_TX_IF_VC4_CFG | CSI2 Transmitter Virtual Channel 4 Configuration Register | 0440 4050h |
| 54h | CSI_TX_IF_VC5_CFG | CSI2 Transmitter Virtual Channel 5 Configuration Register | 0440 4054h |
| 58h | CSI_TX_IF_VC6_CFG | CSI2 Transmitter Virtual Channel 6 Configuration Register | 0440 4058h |
| 5Ch | CSI_TX_IF_VC7_CFG | CSI2 Transmitter Virtual Channel 7 Configuration Register | 0440 405Ch |
| 60h | CSI_TX_IF_VC8_CFG | CSI2 Transmitter Virtual Channel 8 Configuration Register | 0440 4060h |
| 64h | CSI_TX_IF_VC9_CFG | CSI2 Transmitter Virtual Channel 9 Configuration Register | 0440 4064h |
| 68h | CSI_TX_IF_VC10_CFG | CSI2 Transmitter Virtual Channel 10 Configuration Register | 0440 4068h |
| 6Ch | CSI_TX_IF_VC11_CFG | CSI2 Transmitter Virtual Channel 11 Configuration Register | 0440 406Ch |
| 70h | CSI_TX_IF_VC12_CFG | CSI2 Transmitter Virtual Channel 12 Configuration Register | 0440 4070h |
| 74h | CSI_TX_IF_VC13_CFG | CSI2 Transmitter Virtual Channel 13 Configuration Register | 0440 4074h |
| 78h | CSI_TX_IF_VC14_CFG | CSI2 Transmitter Virtual Channel 14 Configuration Register | 0440 4078h |
| 7Ch | CSI_TX_IF_VC15_CFG | CSI2 Transmitter Virtual Channel 15 Configuration Register | 0440 407Ch |
| 80h | CSI_TX_IF_DT0_CFG | CSI2 Transmitter Data Type 0 Configuration Register with pixel_dt_sel[:] = 0 | 0440 4080h |
| 84h | CSI_TX_IF_DT0_FORMAT | CSI2 Transmitter Data Type 0 Format Register | 0440 4084h |

Table 10-95. CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Registers (continued)

| Offset | Acronym | Register Name | CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Physical Address |
|--------|---|---|--|
| 88h | CSI_TX_IF_DT1_CFG | CSI2 Transmitter Data Type 1 Configuration Register with pixel_dt_sel[:] = 1 | 0440 4088h |
| 8Ch | CSI_TX_IF_DT1_FORMAT | CSI2 Transmitter Data Type 1 Format Register | 0440 408Ch |
| 90h | CSI_TX_IF_DT2_CFG | CSI2 Transmitter Data Type 2 Configuration Register with pixel_dt_sel[:] = 2 | 0440 4090h |
| 94h | CSI_TX_IF_DT2_FORMAT | CSI2 Transmitter Data Type 2 Format Register | 0440 4094h |
| 98h | CSI_TX_IF_DT3_CFG | CSI2 Transmitter Data Type 3 Configuration Register with pixel_dt_sel[:] = 3 | 0440 4098h |
| 9Ch | CSI_TX_IF_DT3_FORMAT | CSI2 Transmitter Data Type 3 Format Register | 0440 409Ch |
| A0h | CSI_TX_IF_DT4_CFG | CSI2 Transmitter Data Type 4 Configuration Register with pixel_dt_sel[:] = 4 | 0440 40A0h |
| A4h | CSI_TX_IF_DT4_FORMAT | CSI2 Transmitter Data Type 4 Format Register | 0440 40A4h |
| A8h | CSI_TX_IF_DT5_CFG | CSI2 Transmitter Data Type 5 Configuration Register with pixel_dt_sel[:] = 5 | 0440 40A8h |
| ACh | CSI_TX_IF_DT5_FORMAT | CSI2 Transmitter Data Type 5 Format Register | 0440 40ACh |
| B0h | CSI_TX_IF_DT6_CFG | CSI2 Transmitter Data Type 6 Configuration Register with pixel_dt_sel[:] = 6 | 0440 40B0h |
| B4h | CSI_TX_IF_DT6_FORMAT | CSI2 Transmitter Data Type 6 Format Register | 0440 40B4h |
| B8h | CSI_TX_IF_DT7_CFG | CSI2 Transmitter Data Type 7 Configuration Register with pixel_dt_sel[:] = 7 | 0440 40B8h |
| BCh | CSI_TX_IF_DT7_FORMAT | CSI2 Transmitter Data Type 7 Format Register | 0440 40BCh |
| 100h | CSI_TX_IF_STREAM_IF_0_CFG | CSI2 Stream 0 Configuration Register | 0440 4100h |
| 104h | CSI_TX_IF_STREAM_IF_1_CFG | CSI2 Stream 1 Configuration Register | 0440 4104h |
| 108h | CSI_TX_IF_STREAM_IF_2_CFG | CSI2 Stream 2 Configuration Register | 0440 4108h |
| 10Ch | CSI_TX_IF_STREAM_IF_3_CFG | CSI2 Stream 3 Configuration Register | 0440 410Ch |
| 110h | CSI_TX_IF_DEBUG_CFG | CSI2 Transmitter Debug Enable Register | 0440 4110h |
| 114h | CSI_TX_IF_DEBUG_LN_FSM | Debug Register for Lane FSM. | 0440 4114h |
| 118h | CSI_TX_IF_DEBUG_CLK_LN_FSM | Debug Register for Clock Lane FSM | 0440 4118h |
| 11Ch | CSI_TX_IF_DEBUG_DATA_LN_FSM | Debug Register for Data Lane FSM. | 0440 411Ch |
| 120h | CSI_TX_IF_DEBUG_PROT0_FSM | Debug Register for Pixel IF0 Protocol FSM. | 0440 4120h |
| 124h | CSI_TX_IF_DEBUG_PROT1_FSM | Debug Register for Pixel IF1 Protocol FSM. (Optional: Available when PIXEL_IF2 or 4) | 0440 4124h |
| 128h | CSI_TX_IF_DEBUG_PROT2_FSM | Debug Register for Pixel IF2 Protocol FSM. (Optional: Available when PIXEL_IF4) | 0440 4128h |
| 12Ch | CSI_TX_IF_DEBUG_PROT3_FSM | Debug Register for Pixel IF3 Protocol FSM. (Optional: Available when PIXEL_IF4) | 0440 412Ch |
| 130h | CSI_TX_IF_DPHY_STATUS | DPHY Transmitter Status. | 0440 4130h |
| 134h | CSI_TX_IF_DPHY_CFG1 | DPHY Transmitter Configuration. | 0440 4134h |
| 13Ch | CSI_TX_IF_GENERIC | CSI2 Transmitter Test Register. | 0440 413Ch |
| 200h | CSI_TX_IF_ASF_INT_STATUS | ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_int_fatal or asf_int_nonfatal signal will be asserted. Writing to either raw or masked CSI_TX_IF_STATUS registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt CSI_TX_IF_STATUS test register. | 0440 4200h |

Table 10-95. CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Registers (continued)

| Offset | Acronym | Register Name | CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Physical Address |
|--------|--|--|--|
| 204h | CSI_TX_IF_ASF_INT_RAW_STATUS | ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked CSI_TX_IF_STATUS registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt CSI_TX_IF_STATUS test register. | 0440 4204h |
| 208h | CSI_TX_IF_ASF_INT_MASK | The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt CSI_TX_IF_STATUS register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt. | 0440 4208h |
| 20Ch | CSI_TX_IF_ASF_INT_TEST | The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) CSI_TX_IF_STATUS registers according to mask and will generate interrupt accordingly. | 0440 420Ch |
| 210h | CSI_TX_IF_ASF_FATAL_NONFATAL_SELECT | The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered. | 0440 4210h |
| 220h | CSI_TX_IF_ASF_SRAM_CORR_FAULT_STATUS | Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active. | 0440 4220h |
| 224h | CSI_TX_IF_ASF_SRAM_UNCORR_FAULT_STATUS | Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active. | 0440 4224h |
| 228h | CSI_TX_IF_ASF_SRAM_FAULT_STATS | Statistics register for SRAM faults. Note that this register clears when software writes to any field. | 0440 4228h |
| 230h | CSI_TX_IF_ASF_TRANS_TO_CTRL | Control register to configure the ASF transaction timeout monitors. | 0440 4230h |
| 234h | CSI_TX_IF_ASF_TRANS_TO_FAULT_MASK | Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific. | 0440 4234h |
| 238h | CSI_TX_IF_ASF_TRANS_TO_FAULT_STATUS | Status register for transaction timeouts fault. If a fault occurs the relevant CSI_TX_IF_STATUS bit will be set to 1. Each bit can be cleared by software writing 1 to each bit. | 0440 4238h |
| 240h | CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK | Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific. | 0440 4240h |
| 244h | CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS | Status register for protocol faults. If a fault occurs the relevant CSI_TX_IF_STATUS bit will be set to 1. Each bit can be cleared by software writing 1 to each bit | 0440 4244h |

Table 10-95. CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Registers (continued)

| Offset | Acronym | Register Name | CSI_TX_IF0_VBUS2APB_WRAP_VBUSP_APB_CSI2TX Physical Address |
|--------|---------------------------------------|---|--|
| FFCh | CSI_TX_IF_ID_PROD_VER | CSI2 Transmitter Product ID and Version Register. This register is hard-coded in order to allow software to identify the product and its release version. The product ID will be fixed for all versions, while the version will be updated as new releases for the same product are made. | 0440 4FFCh |

10.48 CSI_TX_IF_DEVICE_CONFIG Register (Offset = 0h) [reset = X]

CSI_TX_IF_DEVICE_CONFIG is shown in [Figure 10-44](#) and described in [Table 10-97](#).

Return to [Summary Table](#).

CSI2 Transmitter Device Configuration Register

Table 10-96. CSI_TX_IF_DEVICE_CONFIG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4000h |

Figure 10-44. CSI_TX_IF_DEVICE_CONFIG Register

| | | | | | | | |
|---------------|-------------|---------|----|------------------|-------------|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | ASF_PRESENT | NUM_DTS | | |
| R-X | | | | R-1h | R-8h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| NUM_DTS | | NUM_VCS | | | | | DATAPATH_SIZE |
| R-8h | | R-10h | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATAPATH_SIZE | NUM_STREAMS | | | CDNS_PHY_PRESENT | MAX_LANE_NB | | |
| R-0h | R-4h | | | R-1h | R-4h | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-97. CSI_TX_IF_DEVICE_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-20 | RESERVED | R | X | |
| 19 | ASF_PRESENT | R | 1h | Active Internal Diagnostic Features: 1=implemented |
| 18-14 | NUM_DTS | R | 8h | Number of Datatypes DT_NUMBER=8 |
| 13-9 | NUM_VCS | R | 10h | Number of Virtual Channels VC_NUMBER=16 |
| 8-7 | DATAPATH_SIZE | R | 0h | Internal Datapath width 00 - 32 bit, 01 - 64bit, 10 - 16 bit, 11 - 8 Bits. |
| 6-4 | NUM_STREAMS | R | 4h | Number of Stream interfaces [1-4] STREAM_IF_4 |
| 3 | CDNS_PHY_PRESENT | R | 1h | DPHY present 1 = Yes |
| 2-0 | MAX_LANE_NB | R | 4h | Max Number of Lanes [1-4] |

10.49 CSI_TX_IF_STATUS Register (Offset = 4h) [reset = 4h]

CSI_TX_IF_STATUS is shown in [Figure 10-45](#) and described in [Table 10-99](#).

Return to [Summary Table](#).

CSI2 Transmitter Status Register

Table 10-98. CSI_TX_IF_STATUS Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4004h |

Figure 10-45. CSI_TX_IF_STATUS Register

| | | | | | | | |
|--------|-----------------|----------------|---------------------------|----------|----------------------|-------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | ULP_MODE_ACTIVE | HS_MODE_ACTIVE | FRAME_TRANSMISSION_ACTIVE | RESERVED | CONFIGURATION_ACTIVE | SOFT_RESET_ACTIVE | BYPASS_MODE_ACTIVE |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-1h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 10-99. CSI_TX_IF_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-7 | UNUSED | R | 0h | Reserved |
| 6 | ULP_MODE_ACTIVE | R | 0h | Ultra Low Power Mode Active Flag When HIGH this bit indicates that ultra low power mode is active. |
| 5 | HS_MODE_ACTIVE | R | 0h | High Speed Mode Active Flag When HIGH this bit indicates that high speed mode is active. |
| 4 | FRAME_TRANSMISSION_ACTIVE | R | 0h | Frame Transmission Active Flag When HIGH this bit indicates that frame transmission is active. |
| 3 | RESERVED | R | 0h | Unused bits |
| 2 | CONFIGURATION_ACTIVE | R | 1h | Configuration Mode Active Flag When HIGH this bit indicates that the CSI2TX module is in the configuration mode. |
| 1 | SOFT_RESET_ACTIVE | R | 0h | Soft Reset Active Flag When HIGH this bit indicates that soft reset is active. |
| 0 | BYPASS_MODE_ACTIVE | R | 0h | Bypass Mode Active Flag When HIGH this bit indicates that bypass mode is active. |

10.50 CSI_TX_IF_IRQ Register (Offset = 8h) [reset = 0h]

CSI_TX_IF_IRQ is shown in [Figure 10-46](#) and described in [Table 10-101](#).

Return to [Summary Table](#).

CSI2 Transmitter Interrupt Register. Write '1' to clear

Table 10-100. CSI_TX_IF_IRQ Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4008h |

Figure 10-46. CSI_TX_IF_IRQ Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------|------------------------------|------------------------|-------------------------|-------------------|---------------------|--------------------|----------------------|
| LINE_NUMBER_ERROR3 | BYTE_COUNT_MISMATCH_I RQ3 | DATA_FLOW_E RR_IRQ3 | FIFO_UNDERF LOW_IRQ3 | LINE_END_IRQ 3 | LINE_START_I RQ3 | FRAME_END_I RQ3 | FRAME_START _IRQ3 |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LINE_NUMBER_ERROR2 | BYTE_COUNT_MISMATCH_I RQ2 | DATA_FLOW_E RR_IRQ2 | FIFO_UNDERF LOW_IRQ2 | LINE_END_IRQ 2 | LINE_START_I RQ2 | FRAME_END_I RQ2 | FRAME_START _IRQ2 |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| LINE_NUMBER_ERROR1 | BYTE_COUNT_MISMATCH_I RQ1 | DATA_FLOW_E RR_IRQ1 | FIFO_UNDERF LOW_IRQ1 | LINE_END_IRQ 1 | LINE_START_I RQ1 | FRAME_END_I RQ1 | FRAME_START _IRQ1 |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LINE_NUMBER_ERROR0 | BYTE_COUNT_MISMATCH_I RQ0 | DATA_FLOW_E RR_IRQ0 | FIFO_UNDERF LOW_IRQ0 | LINE_END_IRQ 0 | LINE_START_I RQ0 | FRAME_END_I RQ0 | FRAME_START _IRQ0 |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-101. CSI_TX_IF_IRQ Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------------|-------|-------|---|
| 31 | LINE_NUMBER_ERROR3 | R/W1C | 0h | Pixel IF 3 Line Number Error Flag - When HIGH this bit indicates that a line number error occurred. |
| 30 | BYTE_COUNT_MISMATCH_I H_IRQ3 | R/W1C | 0h | Pixel IF 3 Byte Count Mismatch Flag - When HIGH this bit indicates that a byte count mismatch occurred. |
| 29 | DATA_FLOW_ERR_IRQ3 | R/W1C | 0h | Pixel IF 3 Data Flow Error Flag - When HIGH this bit indicates that data flow error has occurred, caused by the Frame/Line valid being asserted when the DPhy is not ready. |
| 28 | FIFO_UNDERFLOW_IRQ 3 | R/W1C | 0h | Pixel IF 3 FIFO Underflow Flag - When HIGH this bit indicates that at least one internal FIFO underflow occurred. |
| 27 | LINE_END_IRQ3 | R/W1C | 0h | Pixel IF 3 Line End Flag - When HIGH this bit indicates that a line end occurred. |
| 26 | LINE_START_IRQ3 | R/W1C | 0h | Pixel IF 3 Line Start Flag - When HIGH this bit indicates that a line start occurred. |
| 25 | FRAME_END_IRQ3 | R/W1C | 0h | Pixel IF 3 Frame End Flag - When HIGH this bit indicates that a frame end occurred. |

Table 10-101. CSI_TX_IF_IRQ Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|-------|-------|---|
| 24 | FRAME_START_IRQ3 | R/W1C | 0h | Pixel IF 3 Frame Start Flag - When HIGH this bit indicates that a frame start occurred. |
| 23 | LINE_NUMBER_ERROR2 | R/W1C | 0h | Pixel IF 2 Line Number Error Flag - When HIGH this bit indicates that a line number error occurred. |
| 22 | BYTE_COUNT_MISMATCH_IRQ2 | R/W1C | 0h | Pixel IF 2 Byte Count Mismatch Flag - When HIGH this bit indicates that a byte count mismatch occurred. |
| 21 | DATA_FLOW_ERR_IRQ2 | R/W1C | 0h | Pixel IF 2 Data Flow Error Flag - When HIGH this bit indicates that data flow error has occurred, caused by the Frame/Line valid being asserted when the DPhy is not ready. |
| 20 | FIFO_UNDERFLOW_IRQ2 | R/W1C | 0h | Pixel IF 2 FIFO Underflow Flag - When HIGH this bit indicates that at least one internal FIFO underflow occurred. |
| 19 | LINE_END_IRQ2 | R/W1C | 0h | Pixel IF 2 Line End Flag - When HIGH this bit indicates that a line end occurred. |
| 18 | LINE_START_IRQ2 | R/W1C | 0h | Pixel IF 2 Line Start Flag - When HIGH this bit indicates that a line start occurred. |
| 17 | FRAME_END_IRQ2 | R/W1C | 0h | Pixel IF 2 Frame End Flag - When HIGH this bit indicates that a frame end occurred. |
| 16 | FRAME_START_IRQ2 | R/W1C | 0h | Pixel IF 2 Frame Start Flag - When HIGH this bit indicates that a frame start occurred. |
| 15 | LINE_NUMBER_ERROR1 | R/W1C | 0h | Pixel IF 1 Line Number Error Flag - When HIGH this bit indicates that a line number error occurred. |
| 14 | BYTE_COUNT_MISMATCH_IRQ1 | R/W1C | 0h | Pixel IF 1 Byte Count Mismatch Flag - When HIGH this bit indicates that a byte count mismatch occurred. |
| 13 | DATA_FLOW_ERR_IRQ1 | R/W1C | 0h | Pixel IF 1 Data Flow Error Flag - When HIGH this bit indicates that data flow error has occurred, caused by the Frame/Line valid being asserted when the DPhy is not ready. |
| 12 | FIFO_UNDERFLOW_IRQ1 | R/W1C | 0h | Pixel IF 1 FIFO Underflow Flag - When HIGH this bit indicates that at least one internal FIFO underflow occurred. |
| 11 | LINE_END_IRQ1 | R/W1C | 0h | Pixel IF 1 Line End Flag - When HIGH this bit indicates that a line end occurred. |
| 10 | LINE_START_IRQ1 | R/W1C | 0h | Pixel IF 1 Line Start Flag - When HIGH this bit indicates that a line start occurred. |
| 9 | FRAME_END_IRQ1 | R/W1C | 0h | Pixel IF 1 Frame End Flag - When HIGH this bit indicates that a frame end occurred. |
| 8 | FRAME_START_IRQ1 | R/W1C | 0h | Pixel IF 1 Frame Start Flag - When HIGH this bit indicates that a frame start occurred. |
| 7 | LINE_NUMBER_ERROR0 | R/W1C | 0h | Pixel IF 0 Line Number Error Flag - When HIGH this bit indicates that a line number error occurred. |
| 6 | BYTE_COUNT_MISMATCH_IRQ0 | R/W1C | 0h | Pixel IF 0 Byte Count Mismatch Flag - When HIGH this bit indicates that a byte count mismatch occurred. |
| 5 | DATA_FLOW_ERR_IRQ0 | R/W1C | 0h | Pixel IF 0 Data Flow Error Flag - When HIGH this bit indicates that data flow error has occurred, caused by the Frame/Line valid being asserted when the DPhy is not ready. |
| 4 | FIFO_UNDERFLOW_IRQ0 | R/W1C | 0h | Pixel IF 0 FIFO Underflow Flag - When HIGH this bit indicates that at least one internal FIFO underflow occurred. |

Table 10-101. CSI_TX_IF_IRQ Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 3 | LINE_END_IRQ0 | R/W1C | 0h | Pixel IF 0 Line End Flag - When HIGH this bit indicates that a line end occurred. |
| 2 | LINE_START_IRQ0 | R/W1C | 0h | Pixel IF 0 Line Start Flag - When HIGH this bit indicates that a line start occurred. |
| 1 | FRAME_END_IRQ0 | R/W1C | 0h | Pixel IF 0 Frame End Flag - When HIGH this bit indicates that a frame end occurred. |
| 0 | FRAME_START_IRQ0 | R/W1C | 0h | Pixel IF 0 Frame Start Flag - When HIGH this bit indicates that a frame start occurred. |

10.51 CSI_TX_IF_IRQ_MASK Register (Offset = Ch) [reset = 0h]

CSI_TX_IF_IRQ_MASK is shown in [Figure 10-47](#) and described in [Table 10-103](#).

Return to [Summary Table](#).

CSI2 Transmitter Interrupt Mask Set Register

Table 10-102. CSI_TX_IF_IRQ_MASK Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 400Ch |

Figure 10-47. CSI_TX_IF_IRQ_MASK Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------|-------------------------------|---------------------------|--------------------------|--------------------|----------------------|---------------------|-----------------------|
| MASK_LINE_NUMBER_ERROR3 | MASK_BYTE_COUNT_MISMATCH_IRQ3 | MASK_DATA_FLOW_ERROR_IRQ3 | MASK_FIFO_UNDERFLOW_IRQ3 | MASK_LINE_END_IRQ3 | MASK_LINE_START_IRQ3 | MASK_FRAME_END_IRQ3 | MASK_FRAME_START_IRQ3 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK_LINE_NUMBER_ERROR2 | MASK_BYTE_COUNT_MISMATCH_IRQ2 | MASK_DATA_FLOW_ERROR_IRQ2 | MASK_FIFO_UNDERFLOW_IRQ2 | MASK_LINE_END_IRQ2 | MASK_LINE_START_IRQ2 | MASK_FRAME_END_IRQ2 | MASK_FRAME_START_IRQ2 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MASK_LINE_NUMBER_ERROR1 | MASK_BYTE_COUNT_MISMATCH_IRQ1 | MASK_DATA_FLOW_ERROR_IRQ1 | MASK_FIFO_UNDERFLOW_IRQ1 | MASK_LINE_END_IRQ1 | MASK_LINE_START_IRQ1 | MASK_FRAME_END_IRQ1 | MASK_FRAME_START_IRQ1 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASK_LINE_NUMBER_ERROR0 | MASK_BYTE_COUNT_MISMATCH_IRQ0 | MASK_DATA_FLOW_ERROR_IRQ0 | MASK_FIFO_UNDERFLOW_IRQ0 | MASK_LINE_END_IRQ0 | MASK_LINE_START_IRQ0 | MASK_FRAME_END_IRQ0 | MASK_FRAME_START_IRQ0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-103. CSI_TX_IF_IRQ_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|------|-------|--|
| 31 | MASK_LINE_NUMBER_ERROR3 | R/W | 0h | Pixel IF 3 Line Number Error Mask - Writing 1 to this bit enables interrupt generation from the line_number_error_irq bit. |
| 30 | MASK_BYTE_COUNT_MISMATCH_IRQ3 | R/W | 0h | Pixel IF 3 Byte Count Mismatch Mask - Writing 1 to this bit enables interrupt generation from the byte_count_mismatch_irq bit. |
| 29 | MASK_DATA_FLOW_ERROR_IRQ3 | R/W | 0h | Pixel IF 3 FIFO Overflow Mask - Writing 1 to this bit enables interrupt generation from the data_flow_err_irq bit. |
| 28 | MASK_FIFO_UNDERFLOW_IRQ3 | R/W | 0h | Pixel IF 3 FIFO Underflow Mask - Writing 1 to this bit enables interrupt generation from the fifo_underflow_irq bit. |
| 27 | MASK_LINE_END_IRQ3 | R/W | 0h | Pixel IF 3 Line End Mask - Writing 1 to this bit enables interrupt generation from the line_en_irq bit. |
| 26 | MASK_LINE_START_IRQ3 | R/W | 0h | Pixel IF 3 Line Start Mask - Writing 1 to this bit enables interrupt generation from the line_start_irq bit. |
| 25 | MASK_FRAME_END_IRQ3 | R/W | 0h | Pixel IF 3 Frame End Mask - Writing 1 to this bit enables interrupt generation from the frame_end_irq bit. |

Table 10-103. CSI_TX_IF_IRQ_MASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|------|-------|--|
| 24 | MASK_FRAME_START_IRQ3 | R/W | 0h | Pixel IF 3 Frame Start Mask - Writing 1 to this bit enables interrupt generation from the frame_start_irq bit. |
| 23 | MASK_LINE_NUMBER_ERROR2 | R/W | 0h | Pixel IF 2 Line Number Error Mask - Writing 1 to this bit enables interrupt generation from the line_number_error_irq bit. |
| 22 | MASK_BYTE_COUNT_MISMATCH_IRQ2 | R/W | 0h | Pixel IF 2 Byte Count Mismatch Mask - Writing 1 to this bit enables interrupt generation from the byte_count_mismatch_irq bit. |
| 21 | MASK_DATA_FLOW_ERROR_IRQ2 | R/W | 0h | Pixel IF 2 FIFO Overflow Mask - Writing 1 to this bit enables interrupt generation from the data_flow_err_irq bit. |
| 20 | MASK_FIFO_UNDERFLOW_IRQ2 | R/W | 0h | Pixel IF 2 FIFO Underflow Mask - Writing 1 to this bit enables interrupt generation from the fifo_underflow_irq bit. |
| 19 | MASK_LINE_END_IRQ2 | R/W | 0h | Pixel IF 2 Line End Mask - Writing 1 to this bit enables interrupt generation from the line_en_irq bit. |
| 18 | MASK_LINE_START_IRQ2 | R/W | 0h | Pixel IF 2 Line Start Mask - Writing 1 to this bit enables interrupt generation from the line_start_irq bit. |
| 17 | MASK_FRAME_END_IRQ2 | R/W | 0h | Pixel IF 2 Frame End Mask - Writing 1 to this bit enables interrupt generation from the frame_end_irq bit. |
| 16 | MASK_FRAME_START_IRQ2 | R/W | 0h | Pixel IF 2 Frame Start Mask - Writing 1 to this bit enables interrupt generation from the frame_start_irq bit. |
| 15 | MASK_LINE_NUMBER_ERROR1 | R/W | 0h | Pixel IF 1 Line Number Error Mask - Writing 1 to this bit enables interrupt generation from the line_number_error_irq bit. |
| 14 | MASK_BYTE_COUNT_MISMATCH_IRQ1 | R/W | 0h | Pixel IF 1 Byte Count Mismatch Mask - Writing 1 to this bit enables interrupt generation from the byte_count_mismatch_irq bit. |
| 13 | MASK_DATA_FLOW_ERROR_IRQ1 | R/W | 0h | Pixel IF 1 FIFO Overflow Mask - Writing 1 to this bit enables interrupt generation from the data_flow_err_irq bit. |
| 12 | MASK_FIFO_UNDERFLOW_IRQ1 | R/W | 0h | Pixel IF 1 FIFO Underflow Mask - Writing 1 to this bit enables interrupt generation from the fifo_underflow_irq bit. |
| 11 | MASK_LINE_END_IRQ1 | R/W | 0h | Pixel IF 1 Line End Mask - Writing 1 to this bit enables interrupt generation from the line_en_irq bit. |
| 10 | MASK_LINE_START_IRQ1 | R/W | 0h | Pixel IF 1 Line Start Mask - Writing 1 to this bit enables interrupt generation from the line_start_irq bit. |
| 9 | MASK_FRAME_END_IRQ1 | R/W | 0h | Pixel IF 1 Frame End Mask - Writing 1 to this bit enables interrupt generation from the frame_end_irq bit. |
| 8 | MASK_FRAME_START_IRQ1 | R/W | 0h | Pixel IF 1 Frame Start Mask - Writing 1 to this bit enables interrupt generation from the frame_start_irq bit. |
| 7 | MASK_LINE_NUMBER_ERROR0 | R/W | 0h | Pixel IF 0 Line Number Error Mask - Writing 1 to this bit enables interrupt generation from the line_number_error_irq bit. |
| 6 | MASK_BYTE_COUNT_MISMATCH_IRQ0 | R/W | 0h | Pixel IF 0 Byte Count Mismatch Mask - Writing 1 to this bit enables interrupt generation from the byte_count_mismatch_irq bit. |
| 5 | MASK_DATA_FLOW_ERROR_IRQ0 | R/W | 0h | Pixel IF 0 FIFO Overflow Mask - Writing 1 to this bit enables interrupt generation from the data_flow_err_irq bit. |
| 4 | MASK_FIFO_UNDERFLOW_IRQ0 | R/W | 0h | Pixel IF 0 FIFO Underflow Mask - Writing 1 to this bit enables interrupt generation from the fifo_underflow_irq bit. |
| 3 | MASK_LINE_END_IRQ0 | R/W | 0h | Pixel IF 0 Line End Mask - Writing 1 to this bit enables interrupt generation from the line_en_irq bit. |
| 2 | MASK_LINE_START_IRQ0 | R/W | 0h | Pixel IF 0 Line Start Mask - Writing 1 to this bit enables interrupt generation from the line_start_irq bit. |

Table 10-103. CSI_TX_IF_IRQ_MASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 1 | MASK_FRAME_END_IRQ0 | R/W | 0h | Pixel IF 0 Frame End Mask - Writing 1 to this bit enables interrupt generation from the frame_end_irq bit. |
| 0 | MASK_FRAME_START_IRQ0 | R/W | 0h | Pixel IF 0 Frame Start Mask - Writing 1 to this bit enables interrupt generation from the frame_start_irq bit. |

10.52 CSI_TX_IF_DPHY_IRQ Register (Offset = 10h) [reset = X]

CSI_TX_IF_DPHY_IRQ is shown in [Figure 10-48](#) and described in [Table 10-105](#).

Return to [Summary Table](#).

DPHY Transmitter Interrupt Status. Level sensitive interrupt bits driven by DPHY signal pins. Write 1 to clear

Table 10-104. CSI_TX_IF_DPHY_IRQ Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4010h |

Figure 10-48. CSI_TX_IF_DPHY_IRQ Register

| | | | | | | | |
|----------------------|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ERR_CTRL_TX 3_IRQ | ERR_CTRL_TX 2_IRQ | ERR_CTRL_TX 1_IRQ | ERR_CTRL_TX 0_IRQ | ERR_ESC_TX3 _IRQ | ERR_ESC_TX2 _IRQ | ERR_ESC_TX1 _IRQ | ERR_ESC_TX0 _IRQ |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_SYNC_T X3_IRQ | ERR_SYNC_T X2_IRQ | ERR_SYNC_T X1_IRQ | ERR_SYNC_T X0_IRQ | RESERVED | | | |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W-X | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-105. CSI_TX_IF_DPHY_IRQ Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15 | ERR_CTRL_TX3_IRQ | R/W1C | 0h | DPHY Transmitter Lane 3 ERR_CONTROL_IRQ |
| 14 | ERR_CTRL_TX2_IRQ | R/W1C | 0h | DPHY Transmitter Lane 2 ERR_CONTROL_IRQ |
| 13 | ERR_CTRL_TX1_IRQ | R/W1C | 0h | DPHY Transmitter Lane 1 ERR_CONTROL_IRQ |
| 12 | ERR_CTRL_TX0_IRQ | R/W1C | 0h | DPHY Transmitter Lane 0 ERR_CONTROL_IRQ |
| 11 | ERR_ESC_TX3_IRQ | R/W1C | 0h | DPHY Transmitter Lane 3 ERR_ESC_IRQ |
| 10 | ERR_ESC_TX2_IRQ | R/W1C | 0h | DPHY Transmitter Lane 2 ERR_ESC_IRQ |
| 9 | ERR_ESC_TX1_IRQ | R/W1C | 0h | DPHY Transmitter Lane 1 ERR_ESC_IRQ |
| 8 | ERR_ESC_TX0_IRQ | R/W1C | 0h | DPHY Transmitter Lane 0 ERR_ESC_IRQ |
| 7 | ERR_SYNC_TX3_IRQ | R/W1C | 0h | DPHY Transmitter Lane 3 ERR_SYNC_ESC_IRQ |
| 6 | ERR_SYNC_TX2_IRQ | R/W1C | 0h | DPHY Transmitter Lane 2 ERR_SYNC_ESC_IRQ |
| 5 | ERR_SYNC_TX1_IRQ | R/W1C | 0h | DPHY Transmitter Lane 1 ERR_SYNC_ESC_IRQ |
| 4 | ERR_SYNC_TX0_IRQ | R/W1C | 0h | DPHY Transmitter Lane 0 ERR_SYNC_ESC_IRQ |
| 3-0 | RESERVED | R/W | X | |

10.53 CSI_TX_IF_DPHY_IRQ_MASK Register (Offset = 14h) [reset = X]

CSI_TX_IF_DPHY_IRQ_MASK is shown in [Figure 10-49](#) and described in [Table 10-107](#).

Return to [Summary Table](#).

DPHY Transmitter Interrupt Mask. Writing '1' to any bit enables interrupt generation when signal CSI_TX_IF_IRQ is set and interrupts are enabled.

Table 10-106. CSI_TX_IF_DPHY_IRQ_MASK Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4014h |

Figure 10-49. CSI_TX_IF_DPHY_IRQ_MASK Register

| | | | | | | | |
|---------------------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| MASK_ERR_C TRL_TX3_IRQ | MASK_ERR_C TRL_TX2_IRQ | MASK_ERR_C TRL_TX1_IRQ | MASK_ERR_C TRL_TX0_IRQ | MASK_ERR_E SC_TX3_IRQ | MASK_ERR_E SC_TX2_IRQ | MASK_ERR_E SC_TX1_IRQ | MASK_ERR_E SC_TX0_IRQ |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MASK_ERR_S YNC_TX3_IRQ | MASK_ERR_S YNC_TX2_IRQ | MASK_ERR_S YNC_TX1_IRQ | MASK_ERR_S YNC_TX0_IRQ | RESERVED | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-107. CSI_TX_IF_DPHY_IRQ_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15 | MASK_ERR_CTRL_TX3_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 3 ERR_CONTROL_IRQ |
| 14 | MASK_ERR_CTRL_TX2_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 2 ERR_CONTROL_IRQ |
| 13 | MASK_ERR_CTRL_TX1_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 1 ERR_CONTROL_IRQ |
| 12 | MASK_ERR_CTRL_TX0_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 0 ERR_CONTROL_IRQ |
| 11 | MASK_ERR_ESC_TX3_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 3 ERR_ESC_IRQ |
| 10 | MASK_ERR_ESC_TX2_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 2 ERR_ESC_IRQ |
| 9 | MASK_ERR_ESC_TX1_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 1 ERR_ESC_IRQ |
| 8 | MASK_ERR_ESC_TX0_I RQ | R/W | 0h | DPHY Transmitter Mask Lane 0 ERR_ESC_IRQ |
| 7 | MASK_ERR_SYNC_TX3_ IRQ | R/W | 0h | DPHY Transmitter Mask Lane 3 ERR_SYNC_ESC_IRQ |
| 6 | MASK_ERR_SYNC_TX2_ IRQ | R/W | 0h | DPHY Transmitter Mask Lane 2 ERR_SYNC_ESC_IRQ |

Table 10-107. CSI_TX_IF_DPHY_IRQ_MASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 5 | MASK_ERR_SYNC_TX1_IRQ | R/W | 0h | DPHY Transmitter Mask Lane 1 ERR_SYNC_ESC_IRQ |
| 4 | MASK_ERR_SYNC_TX0_IRQ | R/W | 0h | DPHY Transmitter Mask Lane 0 ERR_SYNC_ESC_IRQ |
| 3-0 | RESERVED | R/W | X | |

10.54 CSI_TX_IF_TX_CONF Register (Offset = 20h) [reset = X]

CSI_TX_IF_TX_CONF is shown in [Figure 10-50](#) and described in [Table 10-109](#).

Return to [Summary Table](#).

CSI2 Transmitter Configuration Register

Table 10-108. CSI_TX_IF_TX_CONF Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4020h |

Figure 10-50. CSI_TX_IF_TX_CONF Register

| | | | | | | | |
|------------|----------|----|----|----|---------------------------|------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IRQ_ENABLE | RESERVED | | | | | | |
| R/W-0h | R/W-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | CONFIGURATI ON_REQUEST | SOFT_RESET_ REQUEST | BYPASS_MOD E_ENABLE |
| R/W-X | | | | | R/W-1h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-109. CSI_TX_IF_TX_CONF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|---|
| 31 | IRQ_ENABLE | R/W | 0h | Interrupt Enable - Writing 1 to this bit enables interrupts. |
| 30-3 | RESERVED | R/W | X | |
| 2 | CONFIGURATION_REQU EST | R/W | 1h | Configuration Request - Writing 1 to this bit enables configuration mode. |
| 1 | SOFT_RESET_REQUES T | R/W | 0h | Soft Reset Request - Writing 1 to this bit enables soft reset. |
| 0 | BYPASS_MODE_ENABL E | R/W | 0h | Bypass Mode - Enable Writing 1 to this bit enables bypass mode. |

10.55 CSI_TX_IF_WAIT_BURST_TIME Register (Offset = 24h) [reset = X]

SI_TX_IF_WAIT_BURST_TIME is shown in [Figure 10-51](#) and described in [Table 10-111](#).

Return to [Summary Table](#).

CSI2 Transmitter DPHY Wait Time configuration Register

**Table 10-110. CSI_TX_IF_WAIT_BURST_TIME
Instances**

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4024h |

Figure 10-51. CSI_TX_IF_WAIT_BURST_TIME Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | TX_CLOCK_EXIT_TIME | | | | | | | |
| R/W-X | | | | | | | | R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | WAIT_BURST_TIME_CNT | | | | | | | |
| R/W-X | | | | | | | | R/W-5h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-111. CSI_TX_IF_WAIT_BURST_TIME Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-16 | TX_CLOCK_EXIT_TIME | R/W | 5h | Tx clock exit time - Number of tx_byte_clk cycles corresponding to the HS clock exit time. |
| 15-8 | RESERVED | R/W | X | |
| 7-0 | WAIT_BURST_TIME_CNT | R/W | 5h | Wait Burst Time - Number of tx_byte_clk cycles corresponding to the inter HS burst gap. |

10.56 CSI_TX_IF_DPHY_CFG Register (Offset = 28h) [reset = X]

CSI_TX_IF_DPHY_CFG is shown in [Figure 10-52](#) and described in [Table 10-113](#).

Return to [Summary Table](#).

CSI2 Transmitter DPHY Lane Enable configuration Register

Table 10-112. CSI_TX_IF_DPHY_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4028h |

Figure 10-52. CSI_TX_IF_DPHY_CFG Register

| | | | | | | | |
|---------------------|---------------------|---------------------|---------------------|----------------------|----------------------|----------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | DPHY_CLK_RE SET |
| R/W-X | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DPHY_LN_3_R ESET | DPHY_LN_2_R ESET | DPHY_LN_1_R ESET | DPHY_LN_0_R ESET | DPHY_CAL_EN ABLE | DPHY_CLOCK _MODE | DPHY_MODE | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-2h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | DPHY_CLK_EN ABLE | DPHY_LN_3_E NABLE | DPHY_LN_2_E NABLE | DPHY_LN_1_E NABLE | DPHY_LN_0_E NABLE |
| R/W-X | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-113. CSI_TX_IF_DPHY_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|---|
| 31-17 | RESERVED | R/W | X | |
| 16 | DPHY_CLK_RESET | R/W | 0h | DPHY Clock Lane Reset - Active low reset for DPHY clock lane. |
| 15 | DPHY_LN_3_RESET | R/W | 0h | DPHY Line 0 Reset - Active low reset for DPHY data lane 3. |
| 14 | DPHY_LN_2_RESET | R/W | 0h | DPHY Line 0 Reset - Active low reset for DPHY data lane 2. |
| 13 | DPHY_LN_1_RESET | R/W | 0h | DPHY Line 0 Reset - Active low reset for DPHY data lane 1. |
| 12 | DPHY_LN_0_RESET | R/W | 0h | DPHY Line 0 Reset - Active low reset for DPHY data lane 0. |
| 11 | DPHY_CAL_ENABLE | R/W | 0h | DPHY Calibration Enable. Enables calibration for DPHY speeds over 1.5G. |
| 10 | DPHY_CLOCK_MODE | R/W | 0h | DPHY Clock Mode. Select the DPHY Clock Lane mode as Continuous [0], Non Continuous [1]. |
| 9-8 | DPHY_MODE | R/W | 2h | DPHY Mode. Select the DPHY clock mode during Non Continuous operation ultra low power [00], high speed [01] or low power stop state [10]. |
| 7-5 | RESERVED | R/W | X | |
| 4 | DPHY_CLK_ENABLE | R/W | 0h | DPHY Clock Lane - Active high enable for DPHY clock lane. |
| 3 | DPHY_LN_3_ENABLE | R/W | 0h | DPHY Lane 3 Enable - Active high enable for DPHY data lane 0. |
| 2 | DPHY_LN_2_ENABLE | R/W | 0h | DPHY Lane 2 Enable - Active high enable for DPHY data lane 0. |

Table 10-113. CSI_TX_IF_DPHY_CFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 1 | DPHY_LN_1_ENABLE | R/W | 0h | DPHY Lane 1 Enable - Active high enable for DPHY data lane 0. |
| 0 | DPHY_LN_0_ENABLE | R/W | 0h | DPHY Lane 0 Enable - Active high enable for DPHY data lane 0. |

10.57 CSI_TX_IF_DPHY_CLK_WAKEUP Register (Offset = 2Ch) [reset = X]

CSI_TX_IF_DPHY_CLK_WAKEUP is shown in [Figure 10-53](#) and described in [Table 10-115](#).

[Return to Summary Table.](#)

CSI2 Transmitter DPHY Clock Lane wakeup time configuration Register

Table 10-114. CSI_TX_IF_DPHY_CLK_WAKEUP Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 402Ch |

Figure 10-53. CSI_TX_IF_DPHY_CLK_WAKEUP Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ULPS_CLK_LANE_WAKEUP | | | | | | | | | | | | | | | |
| R/W-4E20h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-115. CSI_TX_IF_DPHY_CLK_WAKEUP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | ULPS_CLK_LANE_WAKEUP | R/W | 4E20h | DPHY clock lane wakeup time in esc_clk cycles. |

10.58 CSI_TX_IF_DPHY_ULPS_WAKEUP Register (Offset = 30h) [reset = X]

CSI_TX_IF_DPHY_ULPS_WAKEUP is shown in [Figure 10-54](#) and described in [Table 10-117](#).

Return to [Summary Table](#).

CSI2 Transmitter DPHY Data Lane wakeup time configuration Register

**Table 10-116. CSI_TX_IF_DPHY_ULPS_WAKEUP
Instances**

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4030h |

Figure 10-54. CSI_TX_IF_DPHY_ULPS_WAKEUP Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ULPS_DATA_LANE_WAKEUP | | | | | | | | | | | | | | | |
| R/W-4E20h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-117. CSI_TX_IF_DPHY_ULPS_WAKEUP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | ULPS_DATA_LANE_WAKEUP | R/W | 4E20h | DPHY data lane wakeup time in in esc_clk cycles. |

10.59 CSI_TX_IF_VC0_CFG Register (Offset = 40h) [reset = X]

CSI_TX_IF_VC0_CFG is shown in [Figure 10-55](#) and described in [Table 10-119](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 0 Configuration Register

Table 10-118. CSI_TX_IF_VC0_CFG Instances

| Instance | Physical Address |
|--|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUS2APB_CSI2TX | 0440 4040h |

Figure 10-55. CSI_TX_IF_VC0_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_0_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_0_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_0_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-119. CSI_TX_IF_VC0_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_0_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 0. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_0_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 0. |

10.60 CSI_TX_IF_VC1_CFG Register (Offset = 44h) [reset = X]

CSI_TX_IF_VC1_CFG is shown in [Figure 10-56](#) and described in [Table 10-121](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 1 Configuration Register

Table 10-120. CSI_TX_IF_VC1_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4044h |

Figure 10-56. CSI_TX_IF_VC1_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_1_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_1_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_1_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-121. CSI_TX_IF_VC1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_1_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 1. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_1_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 1. |

10.61 CSI_TX_IF_VC2_CFG Register (Offset = 48h) [reset = X]

CSI_TX_IF_VC2_CFG is shown in [Figure 10-57](#) and described in [Table 10-123](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 2 Configuration Register

Table 10-122. CSI_TX_IF_VC2_CFG Instances

| Instance | Physical Address |
|--|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUS2APB_CSI2TX | 0440 4048h |

Figure 10-57. CSI_TX_IF_VC2_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_2_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_2_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_2_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-123. CSI_TX_IF_VC2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|--|
| 31-16 | VC_2_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 2. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_2_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 2. |

10.62 CSI_TX_IF_VC3_CFG Register (Offset = 4Ch) [reset = X]

CSI_TX_IF_VC3_CFG is shown in [Figure 10-58](#) and described in [Table 10-125](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 3 Configuration Register

Table 10-124. CSI_TX_IF_VC3_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 404Ch |

Figure 10-58. CSI_TX_IF_VC3_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_3_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_3_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_3_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-125. CSI_TX_IF_VC3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_3_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 3. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_3_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 3. |

10.63 CSI_TX_IF_VC4_CFG Register (Offset = 50h) [reset = X]

CSI_TX_IF_VC4_CFG is shown in [Figure 10-59](#) and described in [Table 10-127](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 4 Configuration Register

Table 10-126. CSI_TX_IF_VC4_CFG Instances

| Instance | Physical Address |
|--|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUS2APB_CSI2TX | 0440 4050h |

Figure 10-59. CSI_TX_IF_VC4_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_4_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_4_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_4_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-127. CSI_TX_IF_VC4_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_4_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 4. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_4_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 4. |

10.64 CSI_TX_IF_VC5_CFG Register (Offset = 54h) [reset = X]

CSI_TX_IF_VC5_CFG is shown in [Figure 10-60](#) and described in [Table 10-129](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 5 Configuration Register

Table 10-128. CSI_TX_IF_VC5_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4054h |

Figure 10-60. CSI_TX_IF_VC5_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_5_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_5_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_5_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-129. CSI_TX_IF_VC5_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_5_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 5. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_5_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 5. |

10.65 CSI_TX_IF_VC6_CFG Register (Offset = 58h) [reset = X]

CSI_TX_IF_VC6_CFG is shown in [Figure 10-61](#) and described in [Table 10-131](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 6 Configuration Register

Table 10-130. CSI_TX_IF_VC6_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4058h |

Figure 10-61. CSI_TX_IF_VC6_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_6_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_6_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_6_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-131. CSI_TX_IF_VC6_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_6_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 6. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_6_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 6. |

10.66 CSI_TX_IF_VC7_CFG Register (Offset = 5Ch) [reset = X]

CSI_TX_IF_VC7_CFG is shown in [Figure 10-62](#) and described in [Table 10-133](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 7 Configuration Register

Table 10-132. CSI_TX_IF_VC7_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 405Ch |

Figure 10-62. CSI_TX_IF_VC7_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_7_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_7_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_7_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-133. CSI_TX_IF_VC7_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_7_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 7. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_7_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 7. |

10.67 CSI_TX_IF_VC8_CFG Register (Offset = 60h) [reset = X]

CSI_TX_IF_VC8_CFG is shown in [Figure 10-63](#) and described in [Table 10-135](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 8 Configuration Register

Table 10-134. CSI_TX_IF_VC8_CFG Instances

| Instance | Physical Address |
|--|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUS2APB_CSI2TX | 0440 4060h |

Figure 10-63. CSI_TX_IF_VC8_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_8_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_8_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_8_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-135. CSI_TX_IF_VC8_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_8_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 8. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_8_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 8. |

10.68 CSI_TX_IF_VC9_CFG Register (Offset = 64h) [reset = X]

CSI_TX_IF_VC9_CFG is shown in [Figure 10-64](#) and described in [Table 10-137](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 9 Configuration Register

Table 10-136. CSI_TX_IF_VC9_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4064h |

Figure 10-64. CSI_TX_IF_VC9_CFG Register

| | | | | | | | |
|-----------------------|----|----|----|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_9_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_9_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_9_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-137. CSI_TX_IF_VC9_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-16 | VC_9_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 9. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_9_FRAME_COUNT_ENABLE | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 9. |

10.69 CSI_TX_IF_VC10_CFG Register (Offset = 68h) [reset = X]

CSI_TX_IF_VC10_CFG is shown in [Figure 10-65](#) and described in [Table 10-139](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 10 Configuration Register

Table 10-138. CSI_TX_IF_VC10_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4068h |

Figure 10-65. CSI_TX_IF_VC10_CFG Register

| | | | | | | | |
|------------------------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_10_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_10_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_10_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-139. CSI_TX_IF_VC10_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | VC_10_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 10. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_10_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 10. |

10.70 CSI_TX_IF_VC11_CFG Register (Offset = 6Ch) [reset = X]

CSI_TX_IF_VC11_CFG is shown in [Figure 10-66](#) and described in [Table 10-141](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 11 Configuration Register

Table 10-140. CSI_TX_IF_VC11_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 406Ch |

Figure 10-66. CSI_TX_IF_VC11_CFG Register

| | | | | | | | |
|------------------------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_11_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_11_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_11_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-141. CSI_TX_IF_VC11_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | VC_11_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 11. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_11_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 11. |

10.71 CSI_TX_IF_VC12_CFG Register (Offset = 70h) [reset = X]

CSI_TX_IF_VC12_CFG is shown in [Figure 10-67](#) and described in [Table 10-143](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 12 Configuration Register

Table 10-142. CSI_TX_IF_VC12_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4070h |

Figure 10-67. CSI_TX_IF_VC12_CFG Register

| | | | | | | | |
|------------------------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_12_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_12_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_12_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-143. CSI_TX_IF_VC12_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | VC_12_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 12. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_12_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 12. |

10.72 CSI_TX_IF_VC13_CFG Register (Offset = 74h) [reset = X]

CSI_TX_IF_VC13_CFG is shown in [Figure 10-68](#) and described in [Table 10-145](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 13 Configuration Register

Table 10-144. CSI_TX_IF_VC13_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4074h |

Figure 10-68. CSI_TX_IF_VC13_CFG Register

| | | | | | | | |
|------------------------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_13_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_13_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_13_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-145. CSI_TX_IF_VC13_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | VC_13_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 13. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_13_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 13. |

10.73 CSI_TX_IF_VC14_CFG Register (Offset = 78h) [reset = X]

CSI_TX_IF_VC14_CFG is shown in [Figure 10-69](#) and described in [Table 10-147](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 14 Configuration Register

Table 10-146. CSI_TX_IF_VC14_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4078h |

Figure 10-69. CSI_TX_IF_VC14_CFG Register

| | | | | | | | |
|------------------------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_14_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_14_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_14_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-147. CSI_TX_IF_VC14_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | VC_14_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 14. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_14_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 14. |

10.74 CSI_TX_IF_VC15_CFG Register (Offset = 7Ch) [reset = X]

CSI_TX_IF_VC15_CFG is shown in [Figure 10-70](#) and described in [Table 10-149](#).

Return to [Summary Table](#).

CSI2 Transmitter Virtual Channel 15 Configuration Register

Table 10-148. CSI_TX_IF_VC15_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 407Ch |

Figure 10-70. CSI_TX_IF_VC15_CFG Register

| | | | | | | | |
|------------------------|----|----|----|----|----|----|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VC_15_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VC_15_MAX_FRAME_NUMBER | | | | | | | |
| R/W-1h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | VC_15_FRAME_COUNT_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-149. CSI_TX_IF_VC15_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-16 | VC_15_MAX_FRAME_NUMBER | R/W | 1h | Max Frame Number - Maximum number of frames on Virtual Channel 15. |
| 15-1 | RESERVED | R/W | X | |
| 0 | VC_15_FRAME_COUNT_EN | R/W | 0h | Frame Count Enable - Writing 1 to this bit enables frame count on Virtual Channel 15. |

10.75 CSI_TX_IF_DT0_CFG Register (Offset = 80h) [reset = X]

CSI_TX_IF_DT0_CFG is shown in [Figure 10-71](#) and described in [Table 10-151](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 0 Configuration Register with pixel_dt_sel[:] = 0

Table 10-150. CSI_TX_IF_DT0_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4080h |

Figure 10-71. CSI_TX_IF_DT0_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_0_PACKED_ENABLE | DT_0_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_0_DATA_TYPE | | | | | | DT_0_LSLE_GENERATION_EN | DT_0_LINE_COUNT_EN |
| R/W-12h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-151. CSI_TX_IF_DT0_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_0_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 0 with pixel_dt_sel[:] = 0. |
| 8 | DT_0_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 0 with pixel_dt_sel[:] = 0. |
| 7-2 | DT_0_DATA_TYPE | R/W | 12h | Data Type - Type of data on Data Type 0 with pixel_dt_sel[:] = 0. Default ED [0x12] |
| 1 | DT_0_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 0. |
| 0 | DT_0_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 0. |

10.76 CSI_TX_IF_DT0_FORMAT Register (Offset = 84h) [reset = 00640001h]

CSI_TX_IF_DT0_FORMAT is shown in [Figure 10-72](#) and described in [Table 10-153](#).

[Return to Summary Table.](#)

CSI2 Transmitter Data Type 0 Format Register

Table 10-152. CSI_TX_IF_DT0_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4084h |

Figure 10-72. CSI_TX_IF_DT0_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_0_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_0_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-1h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-153. CSI_TX_IF_DT0_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_0_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 0 with pixel_dt_sel[:] = 0. |
| 15-0 | DT_0_MAX_LINE_NUMBER | R/W | 1h | Max Line Number - Maximum number of lines on Data Type 0 with pixel_dt_sel[:] = 0. |

10.77 CSI_TX_IF_DT1_CFG Register (Offset = 88h) [reset = X]

CSI_TX_IF_DT1_CFG is shown in [Figure 10-73](#) and described in [Table 10-155](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 1 Configuration Register with pixel_dt_sel[:] = 1

Table 10-154. CSI_TX_IF_DT1_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4088h |

Figure 10-73. CSI_TX_IF_DT1_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_1_PACKED_ENABLE | DT_1_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_1_DATA_TYPE | | | | | | DT_1_LSLE_GENERATION_EN | DT_1_LINE_COUNT_EN |
| R/W-1Eh | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-155. CSI_TX_IF_DT1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_1_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 1 with pixel_dt_sel[:] = 1. |
| 8 | DT_1_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 1 with pixel_dt_sel[:] = 1. |
| 7-2 | DT_1_DATA_TYPE | R/W | 1Eh | Data Type - Type of data on Data Type 1 with pixel_dt_sel[:] = 1. Default YUV422 8bit [0x1E] |
| 1 | DT_1_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 1. |
| 0 | DT_1_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 1. |

10.78 CSI_TX_IF_DT1_FORMAT Register (Offset = 8Ch) [reset = 00640000h]

CSI_TX_IF_DT1_FORMAT is shown in [Figure 10-74](#) and described in [Table 10-157](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 1 Format Register

Table 10-156. CSI_TX_IF_DT1_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 408Ch |

Figure 10-74. CSI_TX_IF_DT1_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_1_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_1_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-157. CSI_TX_IF_DT1_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_1_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 1 with pixel_dt_sel[:] = 1. |
| 15-0 | DT_1_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 1 with pixel_dt_sel[:] = 1. |

10.79 CSI_TX_IF_DT2_CFG Register (Offset = 90h) [reset = X]

CSI_TX_IF_DT2_CFG is shown in [Figure 10-75](#) and described in [Table 10-159](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 2 Configuration Register with pixel_dt_sel[:] = 2

Table 10-158. CSI_TX_IF_DT2_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4090h |

Figure 10-75. CSI_TX_IF_DT2_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_2_PACKED_ENABLE | DT_2_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_2_DATA_TYPE | | | | | | DT_2_LSLE_GENERATION_EN | DT_2_LINE_COUNT_EN |
| R/W-2Ah | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-159. CSI_TX_IF_DT2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_2_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 2 with pixel_dt_sel[:] = 2. |
| 8 | DT_2_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 2 with pixel_dt_sel[:] = 2. |
| 7-2 | DT_2_DATA_TYPE | R/W | 2Ah | Data Type - Type of data on Data Type 2 with pixel_dt_sel[:] = 2. Default RAW8 [0x2A] |
| 1 | DT_2_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 2. |
| 0 | DT_2_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 2. |

10.80 CSI_TX_IF_DT2_FORMAT Register (Offset = 94h) [reset = 00640000h]

CSI_TX_IF_DT2_FORMAT is shown in [Figure 10-76](#) and described in [Table 10-161](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 2 Format Register

Table 10-160. CSI_TX_IF_DT2_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4094h |

Figure 10-76. CSI_TX_IF_DT2_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_2_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_2_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-161. CSI_TX_IF_DT2_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_2_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 2 with pixel_dt_sel[:] = 2. |
| 15-0 | DT_2_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 2 with pixel_dt_sel[:] = 2. |

10.81 CSI_TX_IF_DT3_CFG Register (Offset = 98h) [reset = X]

CSI_TX_IF_DT3_CFG is shown in [Figure 10-77](#) and described in [Table 10-163](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 3 Configuration Register with pixel_dt_sel[:] = 3

Table 10-162. CSI_TX_IF_DT3_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4098h |

Figure 10-77. CSI_TX_IF_DT3_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_3_PACKED_ENABLE | DT_3_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_3_DATA_TYPE | | | | | | DT_3_LSLE_GENERATION_EN | DT_3_LINE_COUNT_EN |
| R/W-24h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-163. CSI_TX_IF_DT3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_3_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 3 with pixel_dt_sel[:] = 3. |
| 8 | DT_3_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 3 with pixel_dt_sel[:] = 3. |
| 7-2 | DT_3_DATA_TYPE | R/W | 24h | Data Type - Type of data on Data Type 3 with pixel_dt_sel[:] = 3. Default RGB8 [0x24] |
| 1 | DT_3_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 3. |
| 0 | DT_3_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 3. |

10.82 CSI_TX_IF_DT3_FORMAT Register (Offset = 9Ch) [reset = 00640000h]

CSI_TX_IF_DT3_FORMAT is shown in [Figure 10-78](#) and described in [Table 10-165](#).

[Return to Summary Table.](#)

CSI2 Transmitter Data Type 3 Format Register

Table 10-164. CSI_TX_IF_DT3_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 409Ch |

Figure 10-78. CSI_TX_IF_DT3_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_3_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_3_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-165. CSI_TX_IF_DT3_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_3_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 3 with pixel_dt_sel[:] = 3. |
| 15-0 | DT_3_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 3 with pixel_dt_sel[:] = 3. |

10.83 CSI_TX_IF_DT4_CFG Register (Offset = A0h) [reset = X]

CSI_TX_IF_DT4_CFG is shown in [Figure 10-79](#) and described in [Table 10-167](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 4 Configuration Register with pixel_dt_sel[:] = 4

Table 10-166. CSI_TX_IF_DT4_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40A0h |

Figure 10-79. CSI_TX_IF_DT4_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_4_PACKED_ENABLE | DT_4_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_4_DATA_TYPE | | | | | | DT_4_LSLE_GENERATION_EN | DT_4_LINE_COUNT_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-167. CSI_TX_IF_DT4_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_4_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 4 with pixel_dt_sel[:] = 4. |
| 8 | DT_4_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 4 with pixel_dt_sel[:] = 4. |
| 7-2 | DT_4_DATA_TYPE | R/W | 0h | |
| 1 | DT_4_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 4. |
| 0 | DT_4_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 4. |

10.84 CSI_TX_IF_DT4_FORMAT Register (Offset = A4h) [reset = 00640000h]

CSI_TX_IF_DT4_FORMAT is shown in [Figure 10-80](#) and described in [Table 10-169](#).

[Return to Summary Table.](#)

CSI2 Transmitter Data Type 4 Format Register

Table 10-168. CSI_TX_IF_DT4_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40A4h |

Figure 10-80. CSI_TX_IF_DT4_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_4_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_4_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-169. CSI_TX_IF_DT4_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_4_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 4 with pixel_dt_sel[:] = 4. |
| 15-0 | DT_4_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 4 with pixel_dt_sel[:] = 4. |

10.85 CSI_TX_IF_DT5_CFG Register (Offset = A8h) [reset = X]

CSI_TX_IF_DT5_CFG is shown in [Figure 10-81](#) and described in [Table 10-171](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 5 Configuration Register with pixel_dt_sel[:] = 5

Table 10-170. CSI_TX_IF_DT5_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40A8h |

Figure 10-81. CSI_TX_IF_DT5_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_5_PACKED_ENABLE | DT_5_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_5_DATA_TYPE | | | | | | DT_5_LSLE_GENERATION_EN | DT_5_LINE_COUNT_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-171. CSI_TX_IF_DT5_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_5_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 5 with pixel_dt_sel[:] = 5. |
| 8 | DT_5_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 5 with pixel_dt_sel[:] = 5. |
| 7-2 | DT_5_DATA_TYPE | R/W | 0h | |
| 1 | DT_5_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 5. |
| 0 | DT_5_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 5. |

10.86 CSI_TX_IF_DT5_FORMAT Register (Offset = ACh) [reset = 00640000h]

CSI_TX_IF_DT5_FORMAT is shown in [Figure 10-82](#) and described in [Table 10-173](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 5 Format Register

Table 10-172. CSI_TX_IF_DT5_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40ACh |

Figure 10-82. CSI_TX_IF_DT5_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_5_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_5_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-173. CSI_TX_IF_DT5_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_5_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 5 with pixel_dt_sel[:] = 5. |
| 15-0 | DT_5_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 5 with pixel_dt_sel[:] = 5. |

10.87 CSI_TX_IF_DT6_CFG Register (Offset = B0h) [reset = X]

CSI_TX_IF_DT6_CFG is shown in [Figure 10-83](#) and described in [Table 10-175](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 6 Configuration Register with pixel_dt_sel[:] = 6

Table 10-174. CSI_TX_IF_DT6_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40B0h |

Figure 10-83. CSI_TX_IF_DT6_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_6_PACKED_ENABLE | DT_6_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_6_DATA_TYPE | | | | | | DT_6_LSLE_GENERATION_EN | DT_6_LINE_COUNT_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-175. CSI_TX_IF_DT6_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_6_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 6 with pixel_dt_sel[:] = 6. |
| 8 | DT_6_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 6 with pixel_dt_sel[:] = 6. |
| 7-2 | DT_6_DATA_TYPE | R/W | 0h | |
| 1 | DT_6_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 6. |
| 0 | DT_6_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 6. |

10.88 CSI_TX_IF_DT6_FORMAT Register (Offset = B4h) [reset = 00640000h]

CSI_TX_IF_DT6_FORMAT is shown in [Figure 10-84](#) and described in [Table 10-177](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 6 Format Register

Table 10-176. CSI_TX_IF_DT6_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40B4h |

Figure 10-84. CSI_TX_IF_DT6_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_6_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_6_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-177. CSI_TX_IF_DT6_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_6_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 6 with pixel_dt_sel[:] = 6. |
| 15-0 | DT_6_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 6 with pixel_dt_sel[:] = 6. |

10.89 CSI_TX_IF_DT7_CFG Register (Offset = B8h) [reset = X]

CSI_TX_IF_DT7_CFG is shown in [Figure 10-85](#) and described in [Table 10-179](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 7 Configuration Register with pixel_dt_sel[:] = 7

Table 10-178. CSI_TX_IF_DT7_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40B8h |

Figure 10-85. CSI_TX_IF_DT7_CFG Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | DT_7_PACKED_ENABLE | DT_7_EXTD_DATA_TYPE |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_7_DATA_TYPE | | | | | | DT_7_LSLE_GENERATION_EN | DT_7_LINE_COUNT_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-179. CSI_TX_IF_DT7_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9 | DT_7_PACKED_ENABLE | R/W | 0h | Packed Enable - data stream is prepended in to 32bit words on the pixel interface, the data is sent with the defined Data Type 7 with pixel_dt_sel[:] = 7. |
| 8 | DT_7_EXTD_DATA_TYPE | R/W | 0h | Extended Data Type - Type of data on Data Type 7 with pixel_dt_sel[:] = 7. |
| 7-2 | DT_7_DATA_TYPE | R/W | 0h | |
| 1 | DT_7_LSLE_GENERATION_EN | R/W | 0h | Line Start And Line End Short Packet Generation Enable - Writing 1 to this bit enables Line Start and Line End generation on Data Type 7. |
| 0 | DT_7_LINE_COUNT_EN | R/W | 0h | Line Count Enable - Writing 1 to this bit enables line count on Data Type 7. |

10.90 CSI_TX_IF_DT7_FORMAT Register (Offset = BCh) [reset = 00640000h]

CSI_TX_IF_DT7_FORMAT is shown in [Figure 10-86](#) and described in [Table 10-181](#).

Return to [Summary Table](#).

CSI2 Transmitter Data Type 7 Format Register

Table 10-180. CSI_TX_IF_DT7_FORMAT Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 40BCh |

Figure 10-86. CSI_TX_IF_DT7_FORMAT Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DT_7_BYTES_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-64h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DT_7_MAX_LINE_NUMBER | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-181. CSI_TX_IF_DT7_FORMAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | DT_7_BYTES_LINE_NUMBER | R/W | 64h | Bytes Per Line - Bytes per line on Data Type 7 with pixel_dt_sel[:] = 7. |
| 15-0 | DT_7_MAX_LINE_NUMBER | R/W | 0h | Max Line Number - Maximum number of lines on Data Type 7 with pixel_dt_sel[:] = 7. |

10.91 CSI_TX_IF_STREAM_IF_0_CFG Register (Offset = 100h) [reset = X]

CSI_TX_IF_STREAM_IF_0_CFG is shown in [Figure 10-87](#) and described in [Table 10-183](#).

Return to [Summary Table](#).

CSI2 Stream 0 Configuration Register

Table 10-182. CSI_TX_IF_STREAM_IF_0_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4100h |

Figure 10-87. CSI_TX_IF_STREAM_IF_0_CFG Register

| | | | | | | | | | | | | | | | |
|------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_IF_0_FILL_LEVEL | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-183. CSI_TX_IF_STREAM_IF_0_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | STREAM_IF_0_FILL_LEVEL | R/W | 0h | Fill Level - Minimum number of packed 32 words loaded into the stream fifo before Tx will start for Stream if 0. |

10.92 CSI_TX_IF_STREAM_IF_1_CFG Register (Offset = 104h) [reset = X]

CSI_TX_IF_STREAM_IF_1_CFG is shown in [Figure 10-88](#) and described in [Table 10-185](#).

Return to [Summary Table](#).

CSI2 Stream 1 Configuration Register

Table 10-184. CSI_TX_IF_STREAM_IF_1_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4104h |

Figure 10-88. CSI_TX_IF_STREAM_IF_1_CFG Register

| | | | | | | | |
|--------------------------------|----------|----|----|-------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STREAM_IF_1 _SLAVE_MOD E | RESERVED | | | | | | |
| R/W-0h | | | | R/W-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| STREAM_IF_1_FILL_LEVEL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_IF_1_FILL_LEVEL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-185. CSI_TX_IF_STREAM_IF_1_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23 | STREAM_IF_1_SLAVE_M ODE | R/W | 0h | Stream Slave Mode suppresses frame start/end packets in stream 1. To be used when DT interleaving is required in the same VC. NOTE: the stream must then be paired with stream 0 as the master on the StreamIF |
| 22-16 | RESERVED | R/W | X | |
| 15-0 | STREAM_IF_1_FILL_LEV EL | R/W | 0h | Fill Level - Minimum number of packed 32 words loaded into the stream fifo before Tx will start for Stream if 1. |

10.93 CSI_TX_IF_STREAM_IF_2_CFG Register (Offset = 108h) [reset = X]

CSI_TX_IF_STREAM_IF_2_CFG is shown in [Figure 10-89](#) and described in [Table 10-187](#).

Return to [Summary Table](#).

CSI2 Stream 2 Configuration Register

Table 10-186. CSI_TX_IF_STREAM_IF_2_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4108h |

Figure 10-89. CSI_TX_IF_STREAM_IF_2_CFG Register

| | | | | | | | |
|--------------------------------|----------|----|----|-------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STREAM_IF_2 _SLAVE_MOD E | RESERVED | | | | | | |
| R/W-0h | | | | R/W-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| STREAM_IF_2_FILL_LEVEL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_IF_2_FILL_LEVEL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-187. CSI_TX_IF_STREAM_IF_2_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23 | STREAM_IF_2_SLAVE_MODE | R/W | 0h | Stream Slave Mode suppresses frame start/end packets in stream 2. To be used when DT interleaving is required in the same VC. NOTE: the stream must then be paired with stream 0 as the master on the StreamIF |
| 22-16 | RESERVED | R/W | X | |
| 15-0 | STREAM_IF_2_FILL_LEVEL | R/W | 0h | Fill Level - Minimum number of packed 32 words loaded into the stream fifo before Tx will start for Stream if 2. |

10.94 CSI_TX_IF_STREAM_IF_3_CFG Register (Offset = 10Ch) [reset = X]

CSI_TX_IF_STREAM_IF_3_CFG is shown in [Figure 10-90](#) and described in [Table 10-189](#).

Return to [Summary Table](#).

CSI2 Stream 3 Configuration Register

Table 10-188. CSI_TX_IF_STREAM_IF_3_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 410Ch |

Figure 10-90. CSI_TX_IF_STREAM_IF_3_CFG Register

| | | | | | | | |
|--------------------------------|----------|----|----|-------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STREAM_IF_3 _SLAVE_MOD E | RESERVED | | | | | | |
| R/W-0h | | | | R/W-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| STREAM_IF_3_FILL_LEVEL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STREAM_IF_3_FILL_LEVEL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-189. CSI_TX_IF_STREAM_IF_3_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23 | STREAM_IF_3_SLAVE_MODE | R/W | 0h | Stream Slave Mode suppresses frame start/end packets in stream 3. To be used when DT interleaving is required in the same VC. NOTE: the stream must then be paired with stream 0 as the master on the StreamIF |
| 22-16 | RESERVED | R/W | X | |
| 15-0 | STREAM_IF_3_FILL_LEVEL | R/W | 0h | Fill Level - Minimum number of packed 32 words loaded into the stream fifo before Tx will start for Stream if 3. |

10.95 CSI_TX_IF_DEBUG_CFG Register (Offset = 110h) [reset = X]

CSI_TX_IF_DEBUG_CFG is shown in [Figure 10-91](#) and described in [Table 10-191](#).

Return to [Summary Table](#).

CSI2 Transmitter Debug Enable Register

Table 10-190. CSI_TX_IF_DEBUG_CFG Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4110h |

Figure 10-91. CSI_TX_IF_DEBUG_CFG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | DBG_EN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-191. CSI_TX_IF_DEBUG_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | DBG_EN | R/W | 0h | Debug Enable. This bit enables debug when high. If low then other DEBUG registers read 0. |

10.96 CSI_TX_IF_DEBUG_LN_FSM Register (Offset = 114h) [reset = X]

CSI_TX_IF_DEBUG_LN_FSM is shown in [Figure 10-92](#) and described in [Table 10-193](#).

Return to [Summary Table](#).

Debug Register for Lane FSM.

**Table 10-192. CSI_TX_IF_DEBUG_LN_FSM
Instances**

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4114h |

Figure 10-92. CSI_TX_IF_DEBUG_LN_FSM Register

| | | | | | | | |
|-----------------|--------------|--------------|----------------|----------|-----------------|-------------------|----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | NEW_BURST_ALLOWED | PACKET_VALID_R |
| R-X | | | | | | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PACKET_VALID_IN | END_OF_BURST | TRANS_ACTIVE | START_HS_TRANS | RESERVED | LANE_MGR_FSM_ST | | |
| R-0h | R-0h | R-0h | R-0h | R-X | R-0h | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-193. CSI_TX_IF_DEBUG_LN_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31-10 | RESERVED | R | X | |
| 9 | NEW_BURST_ALLOWED | R | 0h | Lane Management FSM. New burst allowed - CSI_TX_IF_WAIT_BURST_TIME expired |
| 8 | PACKET_VALID_R | R | 0h | Lane Management FSM. Valid packet in packet register |
| 7 | PACKET_VALID_IN | R | 0h | Lane Management FSM. Valid packet at input |
| 6 | END_OF_BURST | R | 0h | Lane Management FSM. End of High speed burst |
| 5 | TRANS_ACTIVE | R | 0h | Lane Management FSM. HS transmission active |
| 4 | START_HS_TRANS | R | 0h | Lane Management FSM. HS transmission ready |
| 3 | RESERVED | R | X | |
| 2-0 | LANE_MGR_FSM_ST | R | 0h | Lane Management FSM. State of Lane Management FSM |

10.97 CSI_TX_IF_DEBUG_CLK_LN_FSM Register (Offset = 118h) [reset = X]

CSI_TX_IF_DEBUG_CLK_LN_FSM is shown in [Figure 10-93](#) and described in [Table 10-195](#).

Return to [Summary Table](#).

Debug Register for Clock Lane FSM

Table 10-194. CSI_TX_IF_DEBUG_CLK_LN_FSM Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4118h |

Figure 10-93. CSI_TX_IF_DEBUG_CLK_LN_FSM Register

| | | | | | | | |
|--------------|---------------------------|------------------|------------------|-------------------|----------------------|--------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | ULPS_ACTIVE_CLK | ULPS_MODE_ACTIVE | ULPS_EXIT_CLK_PPI | ULPS_REQUEST_CLK_PPI | HS_MODE_ACTIVE_CLK | REQUEST_HS_CLK_PPI |
| R-X | | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| READY_HS_CLK | ULPS_WAKEUP_COUNT_DONE_CL | ULPS_REQUEST_CLK | HS_MODE_REQ_Q | ULPS_CLK_FSM | | HS_CLK_FSM | |
| R-0h | R-0h | R-0h | R-0h | R-0h | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 10-195. CSI_TX_IF_DEBUG_CLK_LN_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-14 | RESERVED | R | X | |
| 13 | ULPS_ACTIVE_CLK | R | 0h | Clock Lane FSM. ULPS active from DPHY |
| 12 | ULPS_MODE_ACTIVE | R | 0h | Clock Lane FSM. ULPS mode active |
| 11 | ULPS_EXIT_CLK_PPI | R | 0h | Clock Lane FSM. ULPS EXIT Request to DPHY |
| 10 | ULPS_REQUEST_CLK_PPI | R | 0h | Clock Lane FSM. ULPS request to DPHY |
| 9 | HS_MODE_ACTIVE_CLK | R | 0h | Clock Lane FSM. High speed mode active |
| 8 | REQUEST_HS_CLK_PPI | R | 0h | Clock Lane FSM. High speed clock request |
| 7 | READY_HS_CLK | R | 0h | Clock Lane FSM. High speed clock active from DPHY |
| 6 | ULPS_WAKEUP_COUNT_DONE_CL | R | 0h | Clock Lane FSM. Clock lane ULPS wakeup counter expired |

Table 10-195. CSI_TX_IF_DEBUG_CLK_LN_FSM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 5 | ULPS_REQUEST_CLK | R | 0h | Clock Lane FSM. Request ULPS mode |
| 4 | HS_MODE_REQ | R | 0h | Clock Lane FSM. Request High Speed mode |
| 3-2 | ULPS_CLK_FSM | R | 0h | Clock Lane FSM. State of ULPS control FSM. |
| 1-0 | HS_CLK_FSM | R | 0h | Clock Lane FSM. State of High Speed Clock FSM. |

10.98 CSI_TX_IF_DEBUG_DATA_LN_FSM Register (Offset = 11Ch) [reset = X]

CSI_TX_IF_DEBUG_DATA_LN_FSM is shown in [Figure 10-94](#) and described in [Table 10-197](#).

Return to [Summary Table](#).

Debug Register for Data Lane FSM.

Table 10-196. CSI_TX_IF_DEBUG_DATA_LN_FSM Instances

| Instance | Physical Address |
|--|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUS2APB_CSI2TX | 0440 411Ch |

Figure 10-94. CSI_TX_IF_DEBUG_DATA_LN_FSM Register

| | | | | | | | |
|------------------|------------------|------------------|----------------|----------|---------------------------|--------------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | ULPS_ACTIVE |
| R-X | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA_ULPS_ACTIVE | TX_ULPS_EXIT_ESC | TX_ULPS_ESC | TX_REQUEST_ESC | RESERVED | ULPS_WAKEUP_COUNT_DONE_DL | ULPS_ACTIVE_N | |
| R-0h | R-0h | R-0h | R-0h | R-X | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ULPS_ACTIVE_N | | HS_MODE_REQ_SYNC | ULPS_REQ_SYNC | RESERVED | | ULPS_DATA_LANE_FSM | |
| R-0h | | R-0h | R-0h | R-X | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 10-197. CSI_TX_IF_DEBUG_DATA_LN_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|--|
| 31-17 | RESERVED | R | X | |
| 16 | ULPS_ACTIVE | R | 0h | Data Lane FSM. Clock and data lane ULPS active |
| 15 | DATA_ULPS_ACTIVE | R | 0h | Debug Register for Data Lane FSM. Data lane ULPS active |
| 14 | TX_ULPS_EXIT_ESC | R | 0h | Data Lane FSM. Exit escape mode to DPHY |
| 13 | TX_ULPS_ESC | R | 0h | Data Lane FSM. ULPS escape mode to DPHY |
| 12 | TX_REQUEST_ESC | R | 0h | Data Lane FSM. Request escape mode to DPHY |
| 11 | RESERVED | R | X | |
| 10 | ULPS_WAKEUP_COUNT_DONE_DL | R | 0h | Data Lane FSM. Data Lane ULPS wakeup counter expired |
| 9-6 | ULPS_ACTIVE_N | R | 0h | Data Lane FSM. Data Lane ULPS active from DPHY |
| 5 | HS_MODE_REQ_SYNC | R | 0h | Data Lane FSM. HS Mode request |

Table 10-197. CSI_TX_IF_DEBUG_DATA_LN_FSM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|--|
| 4 | ULPS_REQ_SYNC | R | 0h | Data Lane FSM. ULPS Request |
| 3-2 | RESERVED | R | X | |
| 1-0 | ULPS_DATA_LANE_FSM | R | 0h | Data Lane FSM. State of Data Lane FSM FSM |

10.99 CSI_TX_IF_DEBUG_PROT0_FSM Register (Offset = 120h) [reset = X]

CSI_TX_IF_DEBUG_PROT0_FSM is shown in [Figure 10-95](#) and described in [Table 10-199](#).

Return to [Summary Table](#).

Debug Register for Pixel IF0 Protocol FSM.

Table 10-198. CSI_TX_IF_DEBUG_PROT0_FSM Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4120h |

Figure 10-95. CSI_TX_IF_DEBUG_PROT0_FSM Register

| | | | | | | | |
|------------------------|---------------|----|----|---------------------|----------------|----------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | VIRTUAL_CHANNEL_IF0 | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VIRTUAL_CHANNEL_IF0 | DATA_TYPE_IF0 | | | FRAME_VALID_IF0 | LINE_VALID_IF0 | RESERVED | LAST_PAYLOAD_DATA_IF0 |
| R-0h | R-0h | | | R-0h | R-0h | R-X | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAYLOAD_FIFO_EMPTY_IF0 | PROT_FSM_IF0 | | | | | | |
| R-0h | R-0h | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-199. CSI_TX_IF_DEBUG_PROT0_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-19 | RESERVED | R | X | |
| 18-15 | VIRTUAL_CHANNEL_IF0 | R | 0h | Pixel IF0 Protocol FSM. State of the top level Virtual Channel select signals State of the Virtual Channel [3:2] select signals when VCX enabled, otherwise '00' and state of the Virtual Channel [1:0] |
| 14-12 | DATA_TYPE_IF0 | R | 0h | Pixel IF0 Protocol FSM. State of the Data Type select signals |
| 11 | FRAME_VALID_IF0 | R | 0h | Pixel IF0 Protocol FSM. State of the Frame Valid signal |
| 10 | LINE_VALID_IF0 | R | 0h | Pixel IF0 Protocol FSM. State of the Line Valid signal |
| 9 | RESERVED | R | X | |
| 8 | LAST_PAYLOAD_DATA_IF0 | R | 0h | Pixel IF0 Protocol FSM. Last payload data in long packet |
| 7 | PAYLOAD_FIFO_EMPTY_IF0 | R | 0h | Pixel IF0 Protocol FSM. Payload FIFO empty |

Table 10-199. CSI_TX_IF_DEBUG_PROT0_FSM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 6-0 | PROT_FSM_IF0 | R | 0h | Pixel IF0 Protocol FSM. State of Protocol Control FSM |

10.100 CSI_TX_IF_DEBUG_PROT1_FSM Register (Offset = 124h) [reset = X]

CSI_TX_IF_DEBUG_PROT1_FSM is shown in [Figure 10-96](#) and described in [Table 10-201](#).

Return to [Summary Table](#).

Debug Register for Pixel IF1 Protocol FSM. (Optional: Available when PIXEL_IF2 or 4)

Table 10-200. CSI_TX_IF_DEBUG_PROT1_FSM Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4124h |

Figure 10-96. CSI_TX_IF_DEBUG_PROT1_FSM Register

| | | | | | | | |
|------------------------|---------------|----|----|---------------------|----------------|----------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | VIRTUAL_CHANNEL_IF1 | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VIRTUAL_CHANNEL_IF1 | DATA_TYPE_IF1 | | | FRAME_VALID_IF1 | LINE_VALID_IF1 | RESERVED | LAST_PAYLOAD_DATA_IF1 |
| R-0h | R-0h | | | R-0h | R-0h | R-X | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAYLOAD_FIFO_EMPTY_IF1 | PROT_FSM_IF1 | | | | | | |
| R-0h | R-0h | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-201. CSI_TX_IF_DEBUG_PROT1_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-19 | RESERVED | R | X | |
| 18-15 | VIRTUAL_CHANNEL_IF1 | R | 0h | Pixel IF1 Protocol FSM. State of the top level Virtual Channel select signals State of the Virtual Channel [3:2] select signals when VCX enabled, otherwise '00' and state of the Virtual Channel [1:0] |
| 14-12 | DATA_TYPE_IF1 | R | 0h | Pixel IF1 Protocol FSM. State of the Data Type select signals |
| 11 | FRAME_VALID_IF1 | R | 0h | Pixel IF1 Protocol FSM. State of the Frame Valid signal |
| 10 | LINE_VALID_IF1 | R | 0h | Pixel IF1 Protocol FSM. State of the Line Valid signal |
| 9 | RESERVED | R | X | |
| 8 | LAST_PAYLOAD_DATA_IF1 | R | 0h | Pixel IF1 Protocol FSM. Last payload data in long packet |
| 7 | PAYLOAD_FIFO_EMPTY_IF1 | R | 0h | Pixel IF1 Protocol FSM. Payload FIFO empty |

Table 10-201. CSI_TX_IF_DEBUG_PROT1_FSM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 6-0 | PROT_FSM_IF1 | R | 0h | Pixel IF1 Protocol FSM. State of Protocol Control FSM |

10.101 CSI_TX_IF_DEBUG_PROT2_FSM Register (Offset = 128h) [reset = X]

CSI_TX_IF_DEBUG_PROT2_FSM is shown in [Figure 10-97](#) and described in [Table 10-203](#).

Return to [Summary Table](#).

Debug Register for Pixel IF2 Protocol FSM. (Optional: Available when PIXEL_IF4)

Table 10-202. CSI_TX_IF_DEBUG_PROT2_FSM Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4128h |

Figure 10-97. CSI_TX_IF_DEBUG_PROT2_FSM Register

| | | | | | | | |
|------------------------|---------------|----|----|---------------------|----------------|----------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | VIRTUAL_CHANNEL_IF2 | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VIRTUAL_CHANNEL_IF2 | DATA_TYPE_IF2 | | | FRAME_VALID_IF2 | LINE_VALID_IF2 | RESERVED | LAST_PAYLOAD_DATA_IF2 |
| R-0h | R-0h | | | R-0h | R-0h | R-X | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAYLOAD_FIFO_EMPTY_IF2 | PROT_FSM_IF2 | | | | | | |
| R-0h | R-0h | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-203. CSI_TX_IF_DEBUG_PROT2_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-19 | RESERVED | R | X | |
| 18-15 | VIRTUAL_CHANNEL_IF2 | R | 0h | Pixel IF2 Protocol FSM. State of the top level Virtual Channel select signals State of the Virtual Channel [3:2] select signals when VCX enabled, otherwise '00' and state of the Virtual Channel [1:0] |
| 14-12 | DATA_TYPE_IF2 | R | 0h | Pixel IF2 Protocol FSM. State of the Data Type select signals |
| 11 | FRAME_VALID_IF2 | R | 0h | Pixel IF2 Protocol FSM. State of the Frame Valid signal |
| 10 | LINE_VALID_IF2 | R | 0h | Pixel IF2 Protocol FSM. State of the Line Valid signal |
| 9 | RESERVED | R | X | |
| 8 | LAST_PAYLOAD_DATA_IF2 | R | 0h | Pixel IF2 Protocol FSM. Last payload data in long packet |
| 7 | PAYLOAD_FIFO_EMPTY_IF2 | R | 0h | Pixel IF2 Protocol FSM. Payload FIFO empty |

Table 10-203. CSI_TX_IF_DEBUG_PROT2_FSM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 6-0 | PROT_FSM_IF2 | R | 0h | Pixel IF2 Protocol FSM. State of Protocol Control FSM |

10.102 CSI_TX_IF_DEBUG_PROT3_FSM Register (Offset = 12Ch) [reset = X]

CSI_TX_IF_DEBUG_PROT3_FSM is shown in [Figure 10-98](#) and described in [Table 10-205](#).

Return to [Summary Table](#).

Debug Register for Pixel IF3 Protocol FSM. (Optional: Available when PIXEL_IF4)

Table 10-204. CSI_TX_IF_DEBUG_PROT3_FSM Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 412Ch |

Figure 10-98. CSI_TX_IF_DEBUG_PROT3_FSM Register

| | | | | | | | |
|----------------------------|---------------|----|----|----------------------|---------------------|----------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | VIRTUAL_CHANNEL_IF3 | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VIRTUAL_CHAN- NEL_IF3 | DATA_TYPE_IF3 | | | FRAME_VALID- _IF3 | LINE_VALID_IF- 3 | RESERVED | LAST_PAYLOAD- DATA_IF3 |
| R-0h | R-0h | | | R-0h | R-0h | R-X | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAYLOAD_FIFO- EMPTY_IF3 | PROT_FSM_IF3 | | | | | | |
| R-0h | R-0h | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-205. CSI_TX_IF_DEBUG_PROT3_FSM Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-19 | RESERVED | R | X | |
| 18-15 | VIRTUAL_CHANNEL_IF3 | R | 0h | Pixel IF3 Protocol FSM. State of the top level Virtual Channel select signals State of the Virtual Channel [3:2] select signals when VCX enabled, otherwise '00' and state of the Virtual Channel [1:0] |
| 14-12 | DATA_TYPE_IF3 | R | 0h | Pixel IF3 Protocol FSM. State of the Data Type select signals |
| 11 | FRAME_VALID_IF3 | R | 0h | Pixel IF3 Protocol FSM. State of the Frame Valid signal |
| 10 | LINE_VALID_IF3 | R | 0h | Pixel IF3 Protocol FSM. State of the Line Valid signal |
| 9 | RESERVED | R | X | |
| 8 | LAST_PAYLOAD_DATA_I- F3 | R | 0h | Pixel IF3 Protocol FSM. Last payload data in long packet |
| 7 | PAYLOAD_FIFO_EMPTY- _IF3 | R | 0h | Pixel IF3 Protocol FSM. Payload FIFO empty |

Table 10-205. CSI_TX_IF_DEBUG_PROT3_FSM Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 6-0 | PROT_FSM_IF3 | R | 0h | Pixel IF3 Protocol FSM. State of Protocol Control FSM |

10.103 CSI_TX_IF_DPHY_STATUS Register (Offset = 130h) [reset = X]

CSI_TX_IF_DPHY_STATUS is shown in [Figure 10-99](#) and described in [Table 10-207](#).

Return to [Summary Table](#).

DPHY Transmitter Status.

Table 10-206. CSI_TX_IF_DPHY_STATUS Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4130h |

Figure 10-99. CSI_TX_IF_DPHY_STATUS Register

| | | | | | | | |
|----------|----|----|----------------------------|-----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | DPHY_ULPS_A CTIVE_N_CLK | DPHY_ULPS_ACTIVE_N_DL | | | |
| R-X | | | R-1h | R-Fh | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | DPHY_STOPS TATE_CLK | DPHY_STOPSTATE_DL | | | |
| R-X | | | R-1h | R-Fh | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-207. CSI_TX_IF_DPHY_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-13 | RESERVED | R | X | |
| 12 | DPHY_ULPS_ACTIVE_N _CLK | R | 1h | DPHY Transmitter ULPS_ACTIVE_N Clock Lane Status. |
| 11-8 | DPHY_ULPS_ACTIVE_N _DL | R | Fh | DPHY Transmitter ULPS_ACTIVE_N Data Lane [3:0] Status. |
| 7-5 | RESERVED | R | X | |
| 4 | DPHY_STOPSTATE_CLK | R | 1h | DPHY Transmitter STOP_STATE Clock Lane Status. |
| 3-0 | DPHY_STOPSTATE_DL | R | Fh | DPHY Transmitter STOP_STATE Data Lane [3:0] Status. |

10.104 CSI_TX_IF_DPHY_CFG1 Register (Offset = 134h) [reset = X]

CSI_TX_IF_DPHY_CFG1 is shown in [Figure 10-100](#) and described in [Table 10-209](#).

Return to [Summary Table](#).

DPHY Transmitter Configuration.

Table 10-208. CSI_TX_IF_DPHY_CFG1 Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4134h |

Figure 10-100. CSI_TX_IF_DPHY_CFG1 Register

| | | | | | | | |
|----------------|----|----|----|---------------------|----|----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | GEN_POWERDOWN | | C_POWERDOWN | |
| R/W-X | | | | R/W-0h | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| D_POWERDOWN | | | | RESERVED | | | |
| R/W-0h | | | | R/W-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | SWAP_DP_DN_CTX | |
| R/W-X | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SWAP_DP_DN_TX0 | | | | FORCE_STOP_MODE_TX0 | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-209. CSI_TX_IF_DPHY_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-28 | RESERVED | R/W | X | |
| 27-25 | GEN_POWERDOWN | R/W | 0h | DPHY Transmitter Power Down Common Module |
| 24 | C_POWERDOWN | R/W | 0h | DPHY Transmitter Power Down TX Clock |
| 23-20 | D_POWERDOWN | R/W | 0h | DPHY Transmitter Power Down TX Data Lanes |
| 19-9 | RESERVED | R/W | X | |
| 8 | SWAP_DP_DN_CTX | R/W | 0h | DPHY Transmitter Swap DP_DN on Clock Lane |
| 7-4 | SWAP_DP_DN_TX0 | R/W | 0h | DPHY Transmitter Swap DP_DN on TX Data Lanes |
| 3-0 | FORCE_STOP_MODE_TX0 | R/W | 0h | DPHY Transmitter FORCE_STOP_MODE TX Data Lanes |

10.105 CSI_TX_IF_GENERIC Register (Offset = 13Ch) [reset = 0h]

CSI_TX_IF_GENERIC is shown in [Figure 10-101](#) and described in [Table 10-211](#).

Return to [Summary Table](#).

CSI2 Transmitter Test Register.

Table 10-210. CSI_TX_IF_GENERIC Instances

| Instance | Physical Address |
|--|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBUS SP_APB_CSI2TX | 0440 413Ch |

Figure 10-101. CSI_TX_IF_GENERIC Register

| | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_GENERIC_STATUS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEST_GENERIC_CTRL | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-211. CSI_TX_IF_GENERIC Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-16 | TEST_GENERIC_STATUS | R | 0h | CSI2 Transmitter Test Generic Status signals. |
| 15-0 | TEST_GENERIC_CTRL | R/W | 0h | CSI2 Transmitter Test Generic Control signals. |

10.106 CSI_TX_IF_ASF_INT_STATUS Register (Offset = 200h) [reset = 0h]

CSI_TX_IF_ASF_INT_STATUS is shown in [Figure 10-102](#) and described in [Table 10-213](#).

Return to [Summary Table](#).

ASF Interrupt Status Register. This register indicates the source of ASF interrupts. The corresponding bit in the mask register must be clear for a bit to be set. If any bit is set in this register the asf_int_fatal or asf_int_nonfatal signal will be asserted. Writing to either raw or masked CSI_TX_IF_STATUS registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt CSI_TX_IF_STATUS test register.

**Table 10-212. CSI_TX_IF_ASF_INT_STATUS
Instances**

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4200h |

Figure 10-102. CSI_TX_IF_ASF_INT_STATUS Register

| | | | | | | | |
|----------|-----------------------|----------------------|----------------------|-----------------|-------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRIT Y_ERR | ASF_PROTOL OL_ERR | ASF_TRANS_T O_ERR | ASF_CSR_ER R | ASF_DAP_ERR | ASF_SRAM_U NCORR_ERR | ASF_SRAM_C ORR_ERR |
| R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-213. CSI_TX_IF_ASF_INT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W1C | 0h | Integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR | R/W1C | 0h | Protocol error interrupt |
| 4 | ASF_TRANSACTION_TIMEOUT_ERR | R/W1C | 0h | Transaction timeouts error interrupt |
| 3 | ASF_CSR_ERR | R/W1C | 0h | Configuration and CSI_TX_IF_STATUS registers error interrupt |
| 2 | ASF_DAP_ERR | R/W1C | 0h | Data and address paths parity error interrupt |
| 1 | ASF_SRAM_UNCORRECTABLE_ERR | R/W1C | 0h | SRAM uncorrectable error interrupt |
| 0 | ASF_SRAM_CORRECTABLE_ERR | R/W1C | 0h | SRAM correctable error interrupt |

10.107 CSI_TX_IF_ASF_INT_RAW_STATUS Register (Offset = 204h) [reset = 0h]

CSI_TX_IF_ASF_INT_RAW_STATUS is shown in [Figure 10-103](#) and described in [Table 10-215](#).

Return to [Summary Table](#).

ASF Interrupt Raw Status Register. A bit set in this raw register indicates a source of ASF fault in the corresponding feature. Writing to either raw or masked CSI_TX_IF_STATUS registers, clear both registers. For test purposes, trigger signal interrupt event by writing to the ASF interrupt CSI_TX_IF_STATUS test register.

Table 10-214. CSI_TX_IF_ASF_INT_RAW_STATUS Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4204h |

Figure 10-103. CSI_TX_IF_ASF_INT_RAW_STATUS Register

| | | | | | | | |
|----------|-----------------------|----------------------|----------------------|-----------------|-------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRIT Y_ERR | ASF_PROTOL OL_ERR | ASF_TRANS_T O_ERR | ASF_CSR_ER R | ASF_DAP_ERR | ASF_SRAM_U NCORR_ERR | ASF_SRAM_C ORR_ERR |
| R-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-215. CSI_TX_IF_ASF_INT_RAW_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|-------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W1C | 0h | Integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR | R/W1C | 0h | Protocol error interrupt |
| 4 | ASF_TRANS_TO_ERR | R/W1C | 0h | Transaction timeouts error interrupt |
| 3 | ASF_CSR_ERR | R/W1C | 0h | Configuration and CSI_TX_IF_STATUS registers error interrupt |
| 2 | ASF_DAP_ERR | R/W1C | 0h | Data and address paths parity error interrupt |
| 1 | ASF_SRAM_UNCORR_ERR | R/W1C | 0h | SRAM uncorrectable error interrupt |
| 0 | ASF_SRAM_CORR_ERR | R/W1C | 0h | SRAM correctable error interrupt |

10.108 CSI_TX_IF_ASF_INT_MASK Register (Offset = 208h) [reset = 7Fh]

CSI_TX_IF_ASF_INT_MASK is shown in [Figure 10-104](#) and described in [Table 10-217](#).

Return to [Summary Table](#).

The ASF interrupt mask register indicating which interrupt bits in the ASF interrupt CSI_TX_IF_STATUS register are masked. All bits are set at reset. Clear the individual bit to enable the corresponding interrupt.

Table 10-216. CSI_TX_IF_ASF_INT_MASK Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4208h |

Figure 10-104. CSI_TX_IF_ASF_INT_MASK Register

| | | | | | | | |
|----------|------------------------|-----------------------|--------------------------|------------------|------------------|--------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRITY_ERR_MASK | ASF_PROTOCOL_ERR_MASK | ASF_TRANSACTION_ERR_MASK | ASF_CSR_ERR_MASK | ASF_DAP_ERR_MASK | ASF_SRAM_UNCORR_ERR_MASK | ASF_SRAM_CORR_ERR_MASK |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-217. CSI_TX_IF_ASF_INT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR_MASK | R/W | 1h | Mask bit for integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR_MASK | R/W | 1h | Mask bit for protocol error interrupt. |
| 4 | ASF_TRANSACTION_ERR_MASK | R/W | 1h | Mask bit for transaction timeouts error interrupt. |
| 3 | ASF_CSR_ERR_MASK | R/W | 1h | Mask bit for configuration and CSI_TX_IF_STATUS registers error interrupt. |
| 2 | ASF_DAP_ERR_MASK | R/W | 1h | Mask bit for data and address paths parity error interrupt. |
| 1 | ASF_SRAM_UNCORR_ERR_MASK | R/W | 1h | Mask bit for SRAM uncorrectable error interrupt. |
| 0 | ASF_SRAM_CORR_ERR_MASK | R/W | 1h | Mask bit for SRAM correctable error interrupt. |

10.109 CSI_TX_IF_ASF_INT_TEST Register (Offset = 20Ch) [reset = 0h]

CSI_TX_IF_ASF_INT_TEST is shown in [Figure 10-105](#) and described in [Table 10-219](#).

Return to [Summary Table](#).

The ASF interrupt test register emulate hardware even. Write one to individual bit to trigger single event in (masked and raw) CSI_TX_IF_STATUS registers according to mask and will generate interrupt accordingly.

Table 10-218. CSI_TX_IF_ASF_INT_TEST Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 420Ch |

Figure 10-105. CSI_TX_IF_ASF_INT_TEST Register

| | | | | | | | |
|----------|----------------------------|---------------------------|---------------------------|----------------------|----------------------|----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRIT Y_ERR_TEST | ASF_PROTOC OL_ERR_TEST | ASF_TRANS_T O_ERR_TEST | ASF_CSR_ER R_TEST | ASF_DAP_ERR _TEST | ASF_SRAM_U NCORR_ERR_ TEST | ASF_SRAM_C ORR_ERR_TE ST |
| R-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R = Read Only; W = Write Only; -n = value after reset

Table 10-219. CSI_TX_IF_ASF_INT_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|------|-------|--|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR_TEST | W | 0h | Test bit for integrity error interrupt |
| 5 | ASF_PROTOCOL_ERR_TEST | W | 0h | Test bit for protocol error interrupt. |
| 4 | ASF_TRANS_TO_ERR_TEST | W | 0h | Test bit for transaction timeouts error interrupt. |
| 3 | ASF_CSR_ERR_TEST | W | 0h | Test bit for configuration and CSI_TX_IF_STATUS registers error interrupt. |
| 2 | ASF_DAP_ERR_TEST | W | 0h | Test bit for data and address paths parity error interrupt. |
| 1 | ASF_SRAM_UNCORR_ERR_TEST | W | 0h | Test bit for SRAM uncorrectable error interrupt. |
| 0 | ASF_SRAM_CORR_ERR_TEST | W | 0h | Test bit for SRAM correctable error interrupt. |

10.110 CSI_TX_IF_ASF_FATAL_NONFATAL_SELECT Register (Offset = 210h) [reset = 7Fh]

CSI_TX_IF_ASF_FATAL_NONFATAL_SELECT is shown in [Figure 10-106](#) and described in [Table 10-221](#).

Return to [Summary Table](#).

The fatal or non-fatal interrupt register selects whether a fatal (asf_int_fatal) or non-fatal (asf_int_nonfatal) interrupt is triggered. If the bit of the event will be set to one then fatal interrupt (asf_int_fatal) will be triggered. Otherwise the non-fatal interrupt (asf_int_nonfatal) will be triggered.

Table 10-220.
CSI_TX_IF_ASF_FATAL_NONFATAL_SELECT
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4210h |

Figure 10-106. CSI_TX_IF_ASF_FATAL_NONFATAL_SELECT Register

| | | | | | | | |
|----------|-----------------------|------------------------|----------------------|-----------------|-------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | ASF_INTEGRIT Y_ERR | ASF_PROTOCOL OL_ERR | ASF_TRANS_T O_ERR | ASF_CSR_ER R | ASF_DAP_ERR | ASF_SRAM_U NCORR_ERR | ASF_SRAM_C ORR_ERR |
| R-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 10-221. CSI_TX_IF_ASF_FATAL_NONFATAL_SELECT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-7 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 6 | ASF_INTEGRITY_ERR | R/W | 1h | Enable integrity error interrupt as fatal |
| 5 | ASF_PROTOCOL_ERR | R/W | 1h | Enable protocol error interrupt as fatal. |
| 4 | ASF_TRANS_TO_ERR | R/W | 1h | Enable transaction timeouts error interrupt as fatal. |
| 3 | ASF_CSR_ERR | R/W | 1h | Enable configuration and CSI_TX_IF_STATUS registers error interrupt as fatal. |
| 2 | ASF_DAP_ERR | R/W | 1h | Enable data and address paths parity error interrupt as fatal. |
| 1 | ASF_SRAM_UNCORR_ERR | R/W | 1h | Enable SRAM uncorrectable error interrupt as fatal. |
| 0 | ASF_SRAM_CORR_ERR | R/W | 1h | Enable SRAM correctable error interrupt as fatal. |

10.111 CSI_TX_IF_ASF_SRAM_CORR_FAULT_STATUS Register (Offset = 220h) [reset = 0h]

CSI_TX_IF_ASF_SRAM_CORR_FAULT_STATUS is shown in [Figure 10-107](#) and described in [Table 10-223](#).

Return to [Summary Table](#).

Status register for SRAM correctable fault. These fields are updated whenever asf_sram_corr_fault input is active.

Table 10-222.
CSI_TX_IF_ASF_SRAM_CORR_FAULT_STATUS
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4220h |

Figure 10-107. CSI_TX_IF_ASF_SRAM_CORR_FAULT_STATUS Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|----|----|----|----|--------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_CORR_FAULT_INST | | | | | | | | ASF_SRAM_CORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_CORR_FAULT_ADDR | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-223. CSI_TX_IF_ASF_SRAM_CORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-24 | ASF_SRAM_CORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. |
| 23-0 | ASF_SRAM_CORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault. |

10.112 CSI_TX_IF_ASF_SRAM_UNCORR_FAULT_STATUS Register (Offset = 224h) [reset = 0h]

CSI_TX_IF_ASF_SRAM_UNCORR_FAULT_STATUS is shown in [Figure 10-108](#) and described in [Table 10-225](#).

Return to [Summary Table](#).

Status register for SRAM uncorrectable fault. These fields are updated whenever asf_sram_uncorr_fault input is active.

Table 10-224.
CSI_TX_IF_ASF_SRAM_UNCORR_FAULT_STATUS
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4224h |

Figure 10-108. CSI_TX_IF_ASF_SRAM_UNCORR_FAULT_STATUS Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_SRAM_UNCORR_FAULT_INST | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_UNCORR_FAULT_ADDR | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-225. CSI_TX_IF_ASF_SRAM_UNCORR_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-24 | ASF_SRAM_UNCORR_FAULT_INST | R | 0h | Last SRAM instance that generated fault. |
| 23-0 | ASF_SRAM_UNCORR_FAULT_ADDR | R | 0h | Last SRAM address that generated fault. |

10.113 CSI_TX_IF_ASF_SRAM_FAULT_STATS Register (Offset = 228h) [reset = 0h]

CSI_TX_IF_ASF_SRAM_FAULT_STATS is shown in [Figure 10-109](#) and described in [Table 10-227](#).

Return to [Summary Table](#).

Statistics register for SRAM faults. Note that this register clears when software writes to any field.

Table 10-226. CSI_TX_IF_ASF_SRAM_FAULT_STATS Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4228h |

Figure 10-109. CSI_TX_IF_ASF_SRAM_FAULT_STATS Register

| | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_SRAM_FAULT_CORR_STATS | | | | | | | | | | | | | | | |
| R/W1C-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-227. CSI_TX_IF_ASF_SRAM_FAULT_STATS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|-------|-------|---|
| 31-16 | RESERVED | R | 0h | Reserved, read as 0, ignored on write. |
| 15-0 | ASF_SRAM_FAULT_CORR_STATS | R/W1C | 0h | Count of number of correctable errors if implemented. Count value will saturate at 0xffff. |

10.114 CSI_TX_IF_ASF_TRANS_TO_CTRL Register (Offset = 230h) [reset = X]

CSI_TX_IF_ASF_TRANS_TO_CTRL is shown in [Figure 10-110](#) and described in [Table 10-229](#).

Return to [Summary Table](#).

Control register to configure the ASF transaction timeout monitors.

Table 10-228. CSI_TX_IF_ASF_TRANS_TO_CTRL Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4230h |

Figure 10-110. CSI_TX_IF_ASF_TRANS_TO_CTRL Register

| | | | | | | | |
|---------------------|----------|----|----|-------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ASF_TRANS_T O_EN | RESERVED | | | | | | |
| R/W-0h | | | | R/W-X | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_TRANS_TO_CTRL | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-229. CSI_TX_IF_ASF_TRANS_TO_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---|
| 31 | ASF_TRANS_TO_EN | R/W | 0h | Enable transaction timeout monitoring. |
| 30-16 | RESERVED | R/W | X | |
| 15-0 | ASF_TRANS_TO_CTRL | R/W | 0h | Timer value to use for transaction timeout monitor. |

10.115 CSI_TX_IF_ASF_TRANS_TO_FAULT_MASK Register (Offset = 234h) [reset = X]

CSI_TX_IF_ASF_TRANS_TO_FAULT_MASK is shown in [Figure 10-111](#) and described in [Table 10-231](#).

Return to [Summary Table](#).

Control register to mask out ASF transaction timeout faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 10-230.
CSI_TX_IF_ASF_TRANS_TO_FAULT_MASK
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4234h |

Figure 10-111. CSI_TX_IF_ASF_TRANS_TO_FAULT_MASK Register

| | | | | | | | |
|----------|----|----|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ASF_TRANS_T O_FAULT_4_M ASK | ASF_TRANS_T O_FAULT_3_M ASK | ASF_TRANS_T O_FAULT_2_M ASK | ASF_TRANS_T O_FAULT_1_M ASK | ASF_TRANS_T O_FAULT_0_M ASK |
| R/W-X | | | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-231. CSI_TX_IF_ASF_TRANS_TO_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | ASF_TRANS_TO_FAULT_4_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 3 | ASF_TRANS_TO_FAULT_3_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 2 | ASF_TRANS_TO_FAULT_2_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 1 | ASF_TRANS_TO_FAULT_1_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |
| 0 | ASF_TRANS_TO_FAULT_0_MASK | R/W | 1h | Mask register for each ASF transaction timeout fault source. |

10.116 CSI_TX_IF_ASF_TRANS_TO_FAULT_STATUS Register (Offset = 238h) [reset = X]

CSI_TX_IF_ASF_TRANS_TO_FAULT_STATUS is shown in [Figure 10-112](#) and described in [Table 10-233](#).

Return to [Summary Table](#).

Status register for transaction timeouts fault. If a fault occurs the relevant CSI_TX_IF_STATUS bit will be set to 1. Each bit can be cleared by software writing 1 to each bit.

Table 10-232.
CSI_TX_IF_ASF_TRANS_TO_FAULT_STATUS
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4238h |

Figure 10-112. CSI_TX_IF_ASF_TRANS_TO_FAULT_STATUS Register

| | | | | | | | |
|----------|----|----|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | ASF_TRANS_T O_FAULT_4_S TATUS | ASF_TRANS_T O_FAULT_3_S TATUS | ASF_TRANS_T O_FAULT_2_S TATUS | ASF_TRANS_T O_FAULT_1_S TATUS | ASF_TRANS_T O_FAULT_0_S TATUS |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-233. CSI_TX_IF_ASF_TRANS_TO_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|-------|-------|--|
| 31-5 | RESERVED | R/W | X | |
| 4 | ASF_TRANS_TO_FAULT_4_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 3 | ASF_TRANS_TO_FAULT_3_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 2 | ASF_TRANS_TO_FAULT_2_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 1 | ASF_TRANS_TO_FAULT_1_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |
| 0 | ASF_TRANS_TO_FAULT_0_STATUS | R/W1C | 0h | Status bits for transaction timeouts faults. |

10.117 CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK Register (Offset = 240h) [reset = X]

CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK is shown in [Figure 10-113](#) and described in [Table 10-235](#).

Return to [Summary Table](#).

Control register to mask out ASF Protocol faults from triggering interrupts. On reset, all bits are set to mask out all sources. Clear the corresponding bit to enable the interrupt source. The width of this field is parameterisable and the bit definitions are implementation specific.

Table 10-234.
CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4240h |

Figure 10-113. CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK Register

| | | | | | | | |
|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|-------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | ASF_PROTOL_FAULT_16_MASK |
| R/W-X | | | | | | | R/W-1h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_PROTOL_FAULT_15_MASK | ASF_PROTOL_FAULT_14_MASK | ASF_PROTOL_FAULT_13_MASK | ASF_PROTOL_FAULT_12_MASK | ASF_PROTOL_FAULT_11_MASK | ASF_PROTOL_FAULT_10_MASK | ASF_PROTOL_FAULT_9_MASK | ASF_PROTOL_FAULT_8_MASK |
| R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_PROTOL_FAULT_7_MASK | ASF_PROTOL_FAULT_6_MASK | ASF_PROTOL_FAULT_5_MASK | ASF_PROTOL_FAULT_4_MASK | ASF_PROTOL_FAULT_3_MASK | ASF_PROTOL_FAULT_2_MASK | ASF_PROTOL_FAULT_1_MASK | ASF_PROTOL_FAULT_0_MASK |
| R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-235. CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-17 | RESERVED | R/W | X | |
| 16 | ASF_PROTOCOL_FAULT_16_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 15 | ASF_PROTOCOL_FAULT_15_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 14 | ASF_PROTOCOL_FAULT_14_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 13 | ASF_PROTOCOL_FAULT_13_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 12 | ASF_PROTOCOL_FAULT_12_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 11 | ASF_PROTOCOL_FAULT_11_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 10 | ASF_PROTOCOL_FAULT_10_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |

Table 10-235. CSI_TX_IF_ASF_PROTOCOL_FAULT_MASK Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|---|
| 9 | ASF_PROTOCOL_FAULT_9_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 8 | ASF_PROTOCOL_FAULT_8_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 7 | ASF_PROTOCOL_FAULT_7_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 6 | ASF_PROTOCOL_FAULT_6_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 5 | ASF_PROTOCOL_FAULT_5_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 4 | ASF_PROTOCOL_FAULT_4_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 3 | ASF_PROTOCOL_FAULT_3_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 2 | ASF_PROTOCOL_FAULT_2_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 1 | ASF_PROTOCOL_FAULT_1_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |
| 0 | ASF_PROTOCOL_FAULT_0_MASK | R/W | 1h | Mask register for each ASF protocol fault source. |

10.118 CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS Register (Offset = 244h) [reset = X]

CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS is shown in [Figure 10-114](#) and described in [Table 10-237](#).

Return to [Summary Table](#).

Status register for protocol faults. If a fault occurs the relevant CSI_TX_IF_STATUS bit will be set to 1. Each bit can be cleared by software writing 1 to each bit

Table 10-236.
CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS
Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4244h |

Figure 10-114. CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS Register

| | | | | | | | |
|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|---------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | ASF_PROTOL_FAULT_16_STATUS |
| R/W-X | | | | | | | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ASF_PROTOL_FAULT_15_STATUS | ASF_PROTOL_FAULT_14_STATUS | ASF_PROTOL_FAULT_13_STATUS | ASF_PROTOL_FAULT_12_STATUS | ASF_PROTOL_FAULT_11_STATUS | ASF_PROTOL_FAULT_10_STATUS | ASF_PROTOL_FAULT_9_STATUS | ASF_PROTOL_FAULT_8_STATUS |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ASF_PROTOL_FAULT_7_STATUS | ASF_PROTOL_FAULT_6_STATUS | ASF_PROTOL_FAULT_5_STATUS | ASF_PROTOL_FAULT_4_STATUS | ASF_PROTOL_FAULT_3_STATUS | ASF_PROTOL_FAULT_2_STATUS | ASF_PROTOL_FAULT_1_STATUS | ASF_PROTOL_FAULT_0_STATUS |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-237. CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|-------|-------|----------------------------------|
| 31-17 | RESERVED | R/W | X | |
| 16 | ASF_PROTOCOL_FAULT_16_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 15 | ASF_PROTOCOL_FAULT_15_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 14 | ASF_PROTOCOL_FAULT_14_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 13 | ASF_PROTOCOL_FAULT_13_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 12 | ASF_PROTOCOL_FAULT_12_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 11 | ASF_PROTOCOL_FAULT_11_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 10 | ASF_PROTOCOL_FAULT_10_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 9 | ASF_PROTOCOL_FAULT_9_STATUS | R/W1C | 0h | Status bits for protocol faults. |

Table 10-237. CSI_TX_IF_ASF_PROTOCOL_FAULT_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|-------|-------|----------------------------------|
| 8 | ASF_PROTOCOL_FAULT_8_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 7 | ASF_PROTOCOL_FAULT_7_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 6 | ASF_PROTOCOL_FAULT_6_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 5 | ASF_PROTOCOL_FAULT_5_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 4 | ASF_PROTOCOL_FAULT_4_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 3 | ASF_PROTOCOL_FAULT_3_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 2 | ASF_PROTOCOL_FAULT_2_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 1 | ASF_PROTOCOL_FAULT_1_STATUS | R/W1C | 0h | Status bits for protocol faults. |
| 0 | ASF_PROTOCOL_FAULT_0_STATUS | R/W1C | 0h | Status bits for protocol faults. |

10.119 CSI_TX_IF_ID_PROD_VER Register (Offset = FFCh) [reset = 50230200h]

CSI_TX_IF_ID_PROD_VER is shown in [Figure 10-115](#) and described in [Table 10-239](#).

Return to [Summary Table](#).

CSI2 Transmitter Product ID and Version Register.

This register is hard-coded in order to allow software to identify the product and its release version. The product ID will be fixed for all versions, while the version will be updated as new releases for the same product are made.

Table 10-238. CSI_TX_IF_ID_PROD_VER Instances

| Instance | Physical Address |
|---|------------------|
| CSI_TX_IF0_VBUS2APB_WRAP_VBU SP_APB_CSI2TX | 0440 4FFCh |

Figure 10-115. CSI_TX_IF_ID_PROD_VER Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| PRODUCT_ID | | | | | | | | | | | | | | | | VERSION_ID | | | | | | | | | | | | | | | |
| R-5023h | | | | | | | | | | | | | | | | R-200h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-239. CSI_TX_IF_ID_PROD_VER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | PRODUCT_ID | R | 5023h | CSI2 Transmitter Product Identification Number. |
| 15-0 | VERSION_ID | R | 200h | CSI2 Transmitter Product Version Number. |

10.120 CSI_TX_IF0_CP_INTD_CFG_INTD_CFG Registers

Table 10-241 lists the memory-mapped registers for the CSI_TX_IF0_CP_INTD_CFG_INTD_CFG registers. All register offset addresses not listed in Table 10-241 should be considered as reserved locations and the register contents should not be modified.

Table 10-240.
CSI_TX_IF0_CP_INTD_CFG_INTD_CFG Instances

| Instance | Base Address |
|---------------------------------|--------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8000h |

Table 10-241. CSI_TX_IF0_CP_INTD_CFG_INTD_CFG Registers

| Offset | Acronym | Register Name | CSI_TX_IF0_CP_INTD_CFG_INTD_CFG Physical Address |
|--------|--|----------------------------|--|
| 0h | CSI_TX_IF_REVISION | Revision Register | 0440 8000h |
| 10h | CSI_TX_IF_EOI_REG | End of Interrupt Register | 0440 8010h |
| 14h | CSI_TX_IF_INTR_VECTOR_REG | Interrupt Vector Register | 0440 8014h |
| 100h | CSI_TX_IF_ENABLE_REG_LEVEL_0 | Enable Register 0 | 0440 8100h |
| 104h | CSI_TX_IF_ENABLE_REG_PULSE_0 | Enable Register 1 | 0440 8104h |
| 300h | CSI_TX_IF_ENABLE_CLR_REG_LEVEL_0 | Enable Clear Register 0 | 0440 8300h |
| 304h | CSI_TX_IF_ENABLE_CLR_REG_PULSE_0 | Enable Clear Register 1 | 0440 8304h |
| 500h | CSI_TX_IF_STATUS_REG_LEVEL_0 | Status Register 0 | 0440 8500h |
| 504h | CSI_TX_IF_STATUS_REG_PULSE_0 | Status Register 1 | 0440 8504h |
| 700h | CSI_TX_IF_STATUS_CLR_REG_LEVEL_0 | Status Clear Register 0 | 0440 8700h |
| 704h | CSI_TX_IF_STATUS_CLR_REG_PULSE_0 | Status Clear Register 1 | 0440 8704h |
| A80h | CSI_TX_IF_INTR_VECTOR_REG_LEVEL | Interrupt Vector for level | 0440 8A80h |
| A84h | CSI_TX_IF_INTR_VECTOR_REG_PULSE | Interrupt Vector for pulse | 0440 8A84h |

10.121 CSI_TX_IF_REVISION Register (Offset = 0h) [reset = 6690A200h]

CSI_TX_IF_REVISION is shown in [Figure 10-116](#) and described in [Table 10-243](#).

[Return to Summary Table.](#)

Revision Register

Table 10-242. CSI_TX_IF_REVISION Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8000h |

Figure 10-116. CSI_TX_IF_REVISION Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|----------|--------|----|----|--------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | FUNCTION | | | | | | | | | | | |
| R-1h | | R-2h | | R-690h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTLVER | | | | | MAJREV | | | CUSTOM | | MINREV | | | | | |
| R-14h | | | | | R-2h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-243. CSI_TX_IF_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---------------------------|
| 31-30 | SCHEME | R | 1h | Scheme |
| 29-28 | BU | R | 2h | BU |
| 27-16 | FUNCTION | R | 690h | Module ID |
| 15-11 | RTLVER | R | 14h | RTL revisions |
| 10-8 | MAJREV | R | 2h | Major CSI_TX_IF_REVISION |
| 7-6 | CUSTOM | R | 0h | Custom CSI_TX_IF_REVISION |
| 5-0 | MINREV | R | 0h | Minor CSI_TX_IF_REVISION |

10.122 CSI_TX_IF_EOI_REG Register (Offset = 10h) [reset = X]

CSI_TX_IF_EOI_REG is shown in [Figure 10-117](#) and described in [Table 10-245](#).

Return to [Summary Table](#).

End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 10-244. CSI_TX_IF_EOI_REG Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8010h |

Figure 10-117. CSI_TX_IF_EOI_REG Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | EOI_VECTOR | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 10-245. CSI_TX_IF_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|-------------------------|
| 31-8 | RESERVED | R/W | X | |
| 7-0 | EOI_VECTOR | R/W | 0h | End of Interrupt Vector |

10.123 CSI_TX_IF_INTR_VECTOR_REG Register (Offset = 14h) [reset = 0h]

CSI_TX_IF_INTR_VECTOR_REG is shown in [Figure 10-118](#) and described in [Table 10-247](#).

Return to [Summary Table](#).

Interrupt Vector Register

Table 10-246. CSI_TX_IF_INTR_VECTOR_REG Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8014h |

Figure 10-118. CSI_TX_IF_INTR_VECTOR_REG Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTR_VECTOR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-247. CSI_TX_IF_INTR_VECTOR_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|---------------------------|
| 31-0 | INTR_VECTOR | R | 0h | Interrupt Vector Register |

10.124 CSI_TX_IF_ENABLE_REG_LEVEL_0 Register (Offset = 100h) [reset = X]

CSI_TX_IF_ENABLE_REG_LEVEL_0 is shown in [Figure 10-119](#) and described in [Table 10-249](#).

Return to [Summary Table](#).

Enable Register 0

**Table 10-248. CSI_TX_IF_ENABLE_REG_LEVEL_0
Instances**

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8100h |

Figure 10-119. CSI_TX_IF_ENABLE_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | ENABLE_LEVEL_EN_RETRANS3 | ENABLE_LEVEL_EN_RETRANS2 |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-249. CSI_TX_IF_ENABLE_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|-------|-------|----------------------------------|
| 31-2 | RESERVED | R/W | X | |
| 1 | ENABLE_LEVEL_EN_RETRANS3 | R/W1S | 0h | Enable Set for level_en_retrans3 |
| 0 | ENABLE_LEVEL_EN_RETRANS2 | R/W1S | 0h | Enable Set for level_en_retrans2 |

10.125 CSI_TX_IF_ENABLE_REG_PULSE_0 Register (Offset = 104h) [reset = X]

CSI_TX_IF_ENABLE_REG_PULSE_0 is shown in [Figure 10-120](#) and described in [Table 10-251](#).

Return to [Summary Table](#).

Enable Register 1

Table 10-250. CSI_TX_IF_ENABLE_REG_PULSE_0 Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8104h |

Figure 10-120. CSI_TX_IF_ENABLE_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | ENABLE_PULSE_EN_RETRANS3 | ENABLE_PULSE_EN_RETRANS2 |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-251. CSI_TX_IF_ENABLE_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------|-------|-------|----------------------------------|
| 31-2 | RESERVED | R/W | X | |
| 1 | ENABLE_PULSE_EN_RETRANS3 | R/W1S | 0h | Enable Set for pulse_en_retrans3 |
| 0 | ENABLE_PULSE_EN_RETRANS2 | R/W1S | 0h | Enable Set for pulse_en_retrans2 |

10.126 CSI_TX_IF_ENABLE_CLR_REG_LEVEL_0 Register (Offset = 300h) [reset = X]

CSI_TX_IF_ENABLE_CLR_REG_LEVEL_0 is shown in [Figure 10-121](#) and described in [Table 10-253](#).

Return to [Summary Table](#).

Enable Clear Register 0

Table 10-252.
CSI_TX_IF_ENABLE_CLR_REG_LEVEL_0 Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8300h |

Figure 10-121. CSI_TX_IF_ENABLE_CLR_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | ENABLE_LEVEL_EN_RETRANS3_CLR | ENABLE_LEVEL_EN_RETRANS2_CLR |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-253. CSI_TX_IF_ENABLE_CLR_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|-------|-------|------------------------------------|
| 31-2 | RESERVED | R/W | X | |
| 1 | ENABLE_LEVEL_EN_RETRANS3_CLR | R/W1C | 0h | Enable Clear for level_en_retrans3 |
| 0 | ENABLE_LEVEL_EN_RETRANS2_CLR | R/W1C | 0h | Enable Clear for level_en_retrans2 |

10.127 CSI_TX_IF_ENABLE_CLR_REG_PULSE_0 Register (Offset = 304h) [reset = X]

CSI_TX_IF_ENABLE_CLR_REG_PULSE_0 is shown in [Figure 10-122](#) and described in [Table 10-255](#).

Return to [Summary Table](#).

Enable Clear Register 1

Table 10-254.
CSI_TX_IF_ENABLE_CLR_REG_PULSE_0 Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8304h |

Figure 10-122. CSI_TX_IF_ENABLE_CLR_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | ENABLE_PULSE_EN_RETRANS3_CLR | ENABLE_PULSE_EN_RETRANS2_CLR |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-255. CSI_TX_IF_ENABLE_CLR_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|-------|-------|------------------------------------|
| 31-2 | RESERVED | R/W | X | |
| 1 | ENABLE_PULSE_EN_RETRANS3_CLR | R/W1C | 0h | Enable Clear for pulse_en_retrans3 |
| 0 | ENABLE_PULSE_EN_RETRANS2_CLR | R/W1C | 0h | Enable Clear for pulse_en_retrans2 |

10.128 CSI_TX_IF_STATUS_REG_LEVEL_0 Register (Offset = 500h) [reset = X]

CSI_TX_IF_STATUS_REG_LEVEL_0 is shown in [Figure 10-123](#) and described in [Table 10-257](#).

Return to [Summary Table](#).

Status Register 0

**Table 10-256. CSI_TX_IF_STATUS_REG_LEVEL_0
Instances**

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8500h |

Figure 10-123. CSI_TX_IF_STATUS_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | STATUS_LEVEL_RETRANS3 | STATUS_LEVEL_RETRANS2 |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-257. CSI_TX_IF_STATUS_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | STATUS_LEVEL_RETRANS3 | R/W1S | 0h | Status ,write 1 to set, for level_en_retrans3 |
| 0 | STATUS_LEVEL_RETRANS2 | R/W1S | 0h | Status ,write 1 to set, for level_en_retrans2 |

10.129 CSI_TX_IF_STATUS_REG_PULSE_0 Register (Offset = 504h) [reset = X]

CSI_TX_IF_STATUS_REG_PULSE_0 is shown in [Figure 10-124](#) and described in [Table 10-259](#).

Return to [Summary Table](#).

Status Register 1

**Table 10-258. CSI_TX_IF_STATUS_REG_PULSE_0
Instances**

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8504h |

Figure 10-124. CSI_TX_IF_STATUS_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | STATUS_PULSE_RETRANS3 | STATUS_PULSE_RETRANS2 |
| R/W-X | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 10-259. CSI_TX_IF_STATUS_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | STATUS_PULSE_RETRANS3 | R/W1S | 0h | Status ,write 1 to set, for pulse_en_retrans3 |
| 0 | STATUS_PULSE_RETRANS2 | R/W1S | 0h | Status ,write 1 to set, for pulse_en_retrans2 |

10.130 CSI_TX_IF_STATUS_CLR_REG_LEVEL_0 Register (Offset = 700h) [reset = X]

CSI_TX_IF_STATUS_CLR_REG_LEVEL_0 is shown in [Figure 10-125](#) and described in [Table 10-261](#).

Return to [Summary Table](#).

Status Clear Register 0

Table 10-260.
CSI_TX_IF_STATUS_CLR_REG_LEVEL_0 Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8700h |

Figure 10-125. CSI_TX_IF_STATUS_CLR_REG_LEVEL_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | STATUS_LEVEL_RETRANS3_CLR | STATUS_LEVEL_RETRANS2_CLR |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-261. CSI_TX_IF_STATUS_CLR_REG_LEVEL_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | STATUS_LEVEL_RETRANS3_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_retrans3 |
| 0 | STATUS_LEVEL_RETRANS2_CLR | R/W1C | 0h | Status ,write 1 to clear, for level_en_retrans2 |

10.131 CSI_TX_IF_STATUS_CLR_REG_PULSE_0 Register (Offset = 704h) [reset = X]

CSI_TX_IF_STATUS_CLR_REG_PULSE_0 is shown in [Figure 10-126](#) and described in [Table 10-263](#).

Return to [Summary Table](#).

Status Clear Register 1

Table 10-262.
CSI_TX_IF_STATUS_CLR_REG_PULSE_0 Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8704h |

Figure 10-126. CSI_TX_IF_STATUS_CLR_REG_PULSE_0 Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | STATUS_PULSE_RETRANS3_CLR | STATUS_PULSE_RETRANS2_CLR |
| R/W-X | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 10-263. CSI_TX_IF_STATUS_CLR_REG_PULSE_0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|-------|-------|---|
| 31-2 | RESERVED | R/W | X | |
| 1 | STATUS_PULSE_RETRANS3_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_retrans3 |
| 0 | STATUS_PULSE_RETRANS2_CLR | R/W1C | 0h | Status ,write 1 to clear, for pulse_en_retrans2 |

10.132 CSI_TX_IF_INTR_VECTOR_REG_LEVEL Register (Offset = A80h) [reset = 0h]

CSI_TX_IF_INTR_VECTOR_REG_LEVEL is shown in [Figure 10-127](#) and described in [Table 10-265](#).

Return to [Summary Table](#).

Interrupt Vector for level

Table 10-264.
CSI_TX_IF_INTR_VECTOR_REG_LEVEL Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8A80h |

Figure 10-127. CSI_TX_IF_INTR_VECTOR_REG_LEVEL Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTR_VECTOR_LEVEL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-265. CSI_TX_IF_INTR_VECTOR_REG_LEVEL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|------------------|
| 31-0 | INTR_VECTOR_LEVEL | R | 0h | Interrupt Vector |

10.133 CSI_TX_IF_INTR_VECTOR_REG_PULSE Register (Offset = A84h) [reset = 0h]

CSI_TX_IF_INTR_VECTOR_REG_PULSE is shown in [Figure 10-128](#) and described in [Table 10-267](#).

Return to [Summary Table](#).

Interrupt Vector for pulse

Table 10-266.
CSI_TX_IF_INTR_VECTOR_REG_PULSE Instances

| Instance | Physical Address |
|---------------------------------|------------------|
| CSI_TX_IF0_CP_INTD_CFG_INTD_CFG | 0440 8A84h |

Figure 10-128. CSI_TX_IF_INTR_VECTOR_REG_PULSE Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTR_VECTOR_PULSE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 10-267. CSI_TX_IF_INTR_VECTOR_REG_PULSE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|------------------|
| 31-0 | INTR_VECTOR_PULSE | R | 0h | Interrupt Vector |

11 DPHY_RX Registers

[Table 11-1](#) lists the the DPHY_RX memory map. For detailed description of each memory region, refer to the respective register subsection.

Table 11-1. DPHY_RX Memory Map

| Name | Start | End | Size |
|---|------------|------------|-------|
| DPHY_RX0_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX | 0458 0000h | 0458 0FFFh | 4 KB |
| DPHY_RX0_MMR_SLV_K3_DPHY_WRAP | 0458 1000h | 0458 10FFh | 256 B |
| DPHY_RX1_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX | 0459 0000h | 0459 0FFFh | 4 KB |
| DPHY_RX1_MMR_SLV_K3_DPHY_WRAP | 0459 1000h | 0459 10FFh | 256 B |

11.1 DPHY_RX_VBUS2APB Registers

Table 11-3 lists the memory-mapped registers for the DPHY_RX_VBUS2APB registers. All register offset addresses not listed in Table 11-3 should be considered as reserved locations and the register contents should not be modified.

Table 11-2. DPHY_RX_VBUS2APB Instances

| Instance | Base Address |
|---|--------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0000h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0000h |

Table 11-3. DPHY_RX_VBUS2APB Registers

| Offset | Acronym | Register Name | DPHY_RX0_VBUS 2APB_WRAP_VB USP_K3_DPHY_R X Physical Address | DPHY_RX1_VBU S2APB_WRAP_V BUSP_K3_DPHY _RX Physical Address |
|--------|--|------------------|---|---|
| 0h | DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT0 | CMN_ANA_TBIT0 | 0458 0000h | 0459 0000h |
| 4h | DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT1 | CMN_ANA_TBIT1 | 0458 0004h | 0459 0004h |
| 8h | DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT2 | CMN_ANA_TBIT2 | 0458 0008h | 0459 0008h |
| Ch | DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT3 | CMN_ANA_TBIT3 | 0458 000Ch | 0459 000Ch |
| 10h | DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT4 | CMN_ANA_TBIT4 | 0458 0010h | 0459 0010h |
| 14h | DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT5 | CMN_ANA_TBIT5 | 0458 0014h | 0459 0014h |
| 18h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0 | CMN_DIG_TBIT0 | 0458 0018h | 0459 0018h |
| 1Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1 | CMN_DIG_TBIT1 | 0458 001Ch | 0459 001Ch |
| 20h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2 | CMN_DIG_TBIT2 | 0458 0020h | 0459 0020h |
| 24h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT3 | CMN_DIG_TBIT3 | 0458 0024h | 0459 0024h |
| 28h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT4 | CMN_DIG_TBIT4 | 0458 0028h | 0459 0028h |
| 2Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT5 | | 0458 002Ch | 0459 002Ch |
| 30h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT6 | CMN_DIG_TBIT6 | 0458 0030h | 0459 0030h |
| 34h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT7 | CMN_DIG_TBIT7 | 0458 0034h | 0459 0034h |
| 38h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT8 | CMN_DIG_TBIT8 | 0458 0038h | 0459 0038h |
| 3Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT9 | CMN_DIG_TBIT9 | 0458 003Ch | 0459 003Ch |
| 40h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT10 | CMN_DIG_TBIT10 | 0458 0040h | 0459 0040h |
| 44h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11 | CMN_DIG_TBIT11 | 0458 0044h | 0459 0044h |
| 48h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12 | CMN_DIG_TBIT12 | 0458 0048h | 0459 0048h |
| 4Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT13 | CMN_DIG_TBIT13 | 0458 004Ch | 0459 004Ch |
| 50h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT14 | CMN_DIG_TBIT14 | 0458 0050h | 0459 0050h |
| 68h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT20 | CMN_DIG_TBIT20 | 0458 0068h | 0459 0068h |
| 6Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT21 | CMN_DIG_TBIT21 | 0458 006Ch | 0459 006Ch |
| 70h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT22 | BIST_CONFIG_REG1 | 0458 0070h | 0459 0070h |
| 74h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT23 | BIST_CONFIG_REG2 | 0458 0074h | 0459 0074h |
| 78h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT24 | BIST_CONFIG_REG3 | 0458 0078h | 0459 0078h |
| 7Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT25 | BIST_CONFIG_REG4 | 0458 007Ch | 0459 007Ch |
| 80h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT26 | BIST_CONFIG_REG5 | 0458 0080h | 0459 0080h |
| 84h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT27 | BIST_CONFIG_REG6 | 0458 0084h | 0459 0084h |
| 88h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28 | BIST_CONFIG_REG7 | 0458 0088h | 0459 0088h |
| 94h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT31 | CMN_DIG_TBIT31 | 0458 0094h | 0459 0094h |
| 98h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT32 | CMN_DIG_TBIT32 | 0458 0098h | 0459 0098h |
| 9Ch | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT33 | CMN_DIG_TBIT33 | 0458 009Ch | 0459 009Ch |
| A0h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT34 | CMN_DIG_TBIT34 | 0458 00A0h | 0459 00A0h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS 2APB_WRAP_VB USP_K3_DPHY_R X Physical Address | DPHY_RX1_VBU S2APB_WRAP_V BUSP_K3_DPHY _RX Physical Address |
|--------|--|--------------------------------|---|---|
| A4h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT35 | CMN_DIG_TBIT35 | 0458 00A4h | 0459 00A4h |
| A8h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT36 | CMN_DIG_TBIT36 | 0458 00A8h | 0459 00A8h |
| ACH | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37 | | 0458 00ACH | 0459 00ACH |
| B0h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT38 | CMN_DIG_TBIT38 | 0458 00B0h | 0459 00B0h |
| B4h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT39 | CMN_DIG_TBIT39 | 0458 00B4h | 0459 00B4h |
| D8h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT50 | BIST_STATUS_REG1 | 0458 00D8h | 0459 00D8h |
| E4h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT53 | CMN_DIG_TBIT53 | 0458 00E4h | 0459 00E4h |
| E8h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT54 | CMN_DIG_TBIT54 | 0458 00E8h | 0459 00E8h |
| F0h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT56 | CMN_DIG_TBIT56 | 0458 00F0h | 0459 00F0h |
| F8h | DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT58 | CMN_DIG_TBIT58 | 0458 00F8h | 0459 00F8h |
| 100h | DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT0 | Analog Test Bit Reg0 | 0458 0100h | 0459 0100h |
| 104h | DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT1 | Analog Test Bit Reg1 | 0458 0104h | 0459 0104h |
| 108h | DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT2 | Analog Test Bit Reg2 | 0458 0108h | 0459 0108h |
| 10Ch | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT0 | Digital Test Bit Reg0 | 0458 010Ch | 0459 010Ch |
| 110h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT1 | Digital Extra Test Bit Reg0 | 0458 0110h | 0459 0110h |
| 114h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2 | Test Mux Register | 0458 0114h | 0459 0114h |
| 118h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT3 | Digital Extra Test Bit Reg1 | 0458 0118h | 0459 0118h |
| 11Ch | DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT3 | Analog Read Test Bit Reg3 | 0458 011Ch | 0459 011Ch |
| 120h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT4 | Digital Read Test Reg0 | 0458 0120h | 0459 0120h |
| 124h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT5 | Digital Read Test Bit Reg0 | 0458 0124h | 0459 0124h |
| 128h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT6 | BIST Status Reg0 | 0458 0128h | 0459 0128h |
| 12Ch | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT7 | Bist Extra Status Read Reg0 | 0458 012Ch | 0459 012Ch |
| 130h | DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT8 | Digital Extra Read Reg0 | 0458 0130h | 0459 0130h |
| 200h | DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT0 | ANA_TBIT0 | 0458 0200h | 0459 0200h |
| 204h | DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT1 | ANA_EXTRA_TBIT0 | 0458 0204h | 0459 0204h |
| 208h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0 | DIG_TBIT0 | 0458 0208h | 0459 0208h |
| 20Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT1 | DIG_TBIT1 | 0458 020Ch | 0459 020Ch |
| 210h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT2 | DIGITAL_EXTRA_TES T_REG0 | 0458 0210h | 0459 0210h |
| 214h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT3 | preamp_cal_ctrl_reg1 | 0458 0214h | 0459 0214h |
| 218h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4 | preamp_cal_ctrl_reg2 | 0458 0218h | 0459 0218h |
| 21Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT5 | dcc_comp_cal_ctrl_reg 1 | 0458 021Ch | 0459 021Ch |
| 220h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6 | dcc_comp_cal_ctrl_reg 2 | 0458 0220h | 0459 0220h |
| 224h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT7 | mix_comp_cal_ctrl_reg 1 | 0458 0224h | 0459 0224h |
| 228h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8 | mix_comp_cal_ctrl_reg 2 | 0458 0228h | 0459 0228h |
| 22Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT9 | pos_samp_cal_ctrl_reg 1 | 0458 022Ch | 0459 022Ch |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address | DPHY_RX1_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address |
|--------|--|---------------------------------------|--|--|
| 230h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10 | pos_samp_cal_ctrl_reg2 | 0458 0230h | 0459 0230h |
| 234h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT11 | pos_samp_cal_ctrl_reg3 | 0458 0234h | 0459 0234h |
| 238h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT12 | neg_samp_cal_ctrl_reg1 | 0458 0238h | 0459 0238h |
| 23Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13 | neg_samp_cal_ctrl_reg2 | 0458 023Ch | 0459 023Ch |
| 240h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT14 | neg_samp_cal_ctrl_reg3 | 0458 0240h | 0459 0240h |
| 244h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT15 | skew_cal_fsm_reg1 | 0458 0244h | 0459 0244h |
| 248h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT16 | skew_cal_fsm_reg2 | 0458 0248h | 0459 0248h |
| 24Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT17 | skew_cal_fsm_reg3 | 0458 024Ch | 0459 024Ch |
| 250h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT18 | ducy_corr_ctrl_reg1 | 0458 0250h | 0459 0250h |
| 254h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT19 | ducy_corr_ctrl_reg2 | 0458 0254h | 0459 0254h |
| 258h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20 | skew_cal_avg_reg1 | 0458 0258h | 0459 0258h |
| 25Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT21 | skew_cal_avg_reg2 | 0458 025Ch | 0459 025Ch |
| 260h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT22 | skew_cal_avg_reg3 | 0458 0260h | 0459 0260h |
| 264h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT23 | skew_cal_avg_reg4 | 0458 0264h | 0459 0264h |
| 268h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT24 | skew_cal_avg_reg5 | 0458 0268h | 0459 0268h |
| 26Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT25 | DIGITAL_EXTRA_CALI_B_REG0 | 0458 026Ch | 0459 026Ch |
| 270h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT26 | DIGITAL_EXTRA_CALI_B_REG1 | 0458 0270h | 0459 0270h |
| 274h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT27 | bist_config_reg1 | 0458 0274h | 0459 0274h |
| 278h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT28 | bist_config_reg2 | 0458 0278h | 0459 0278h |
| 27Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT29 | bist_config_reg3 | 0458 027Ch | 0459 027Ch |
| 280h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT30 | bist_config_reg4 | 0458 0280h | 0459 0280h |
| 284h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT31 | DIGITAL_EXTRA_TES_T_REG1 | 0458 0284h | 0459 0284h |
| 288h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT32 | DIGITAL_EXTRA_TES_T_REG2 | 0458 0288h | 0459 0288h |
| 28Ch | DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT2 | ANA_TBIT0 | 0458 028Ch | 0459 028Ch |
| 290h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT33 | deserialiser_fsm_status | 0458 0290h | 0459 0290h |
| 294h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT34 | lp_status | 0458 0294h | 0459 0294h |
| 298h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT35 | DIGITAL_EXTRA_REA_D_REG0 | 0458 0298h | 0459 0298h |
| 29Ch | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36 | dcc_mixer_comparator_calibration_stat | 0458 029Ch | 0459 029Ch |
| 2A0h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37 | preamp_cal_status_reg1 | 0458 02A0h | 0459 02A0h |
| 2A4h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38 | pos_samp_cal_status_reg1 | 0458 02A4h | 0459 02A4h |
| 2A8h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT39 | pos_samp_cal_status_reg2 | 0458 02A8h | 0459 02A8h |
| 2ACh | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40 | neg_samp_cal_status_reg1 | 0458 02ACh | 0459 02ACh |
| 2B0h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT41 | neg_samp_cal_status_reg2 | 0458 02B0h | 0459 02B0h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS 2APB_WRAP_VB USP_K3_DPHY_R X Physical Address | DPHY_RX1_VBU S2APB_WRAP_V BUSP_K3_DPHY _RX Physical Address |
|--------|--|-----------------------------------|---|---|
| 2B4h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42 | skew_cal_fsm_status_reg1 | 0458 02B4h | 0459 02B4h |
| 2B8h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT43 | skew_cal_avg_status_reg1 | 0458 02B8h | 0459 02B8h |
| 2BCh | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT44 | skew_cal_avg_status_reg2 | 0458 02BCh | 0459 02BCh |
| 2C0h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT45 | DIGITAL_CALIB_EXTR A_READ_REG0 | 0458 02C0h | 0459 02C0h |
| 2C4h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT46 | DIGITAL_CALIB_EXTR A_READ_REG1 | 0458 02C4h | 0459 02C4h |
| 2C8h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT47 | bist_status_reg1 | 0458 02C8h | 0459 02C8h |
| 2CCh | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT48 | bist_status_reg2 | 0458 02CCh | 0459 02CCh |
| 2D0h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT49 | DIG_BIST_EXTRA_READ_REG0 | 0458 02D0h | 0459 02D0h |
| 2D4h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT50 | DIG_EXTRA_READ_REG1 | 0458 02D4h | 0459 02D4h |
| 2D8h | DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT51 | DIG_EXTRA_READ_REG2 | 0458 02D8h | 0459 02D8h |
| 300h | DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT0 | ANA_TBIT0 | 0458 0300h | 0459 0300h |
| 304h | DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT1 | ANA_EXTRA_TBIT0 | 0458 0304h | 0459 0304h |
| 308h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0 | DIG_TBIT0 | 0458 0308h | 0459 0308h |
| 30Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT1 | DIG_TBIT1 | 0458 030Ch | 0459 030Ch |
| 310h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT2 | DIGITAL_EXTRA_TEST_REG0 | 0458 0310h | 0459 0310h |
| 314h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT3 | preamp_cal_ctrl_reg1 | 0458 0314h | 0459 0314h |
| 318h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4 | preamp_cal_ctrl_reg2 | 0458 0318h | 0459 0318h |
| 31Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT5 | dcc_comp_cal_ctrl_reg1 | 0458 031Ch | 0459 031Ch |
| 320h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6 | dcc_comp_cal_ctrl_reg2 | 0458 0320h | 0459 0320h |
| 324h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT7 | mix_comp_cal_ctrl_reg1 | 0458 0324h | 0459 0324h |
| 328h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8 | mix_comp_cal_ctrl_reg2 | 0458 0328h | 0459 0328h |
| 32Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT9 | pos_samp_cal_ctrl_reg1 | 0458 032Ch | 0459 032Ch |
| 330h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10 | pos_samp_cal_ctrl_reg2 | 0458 0330h | 0459 0330h |
| 334h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT11 | pos_samp_cal_ctrl_reg3 | 0458 0334h | 0459 0334h |
| 338h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT12 | neg_samp_cal_ctrl_reg1 | 0458 0338h | 0459 0338h |
| 33Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13 | neg_samp_cal_ctrl_reg2 | 0458 033Ch | 0459 033Ch |
| 340h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT14 | neg_samp_cal_ctrl_reg3 | 0458 0340h | 0459 0340h |
| 344h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT15 | skew_cal_fsm_reg1 | 0458 0344h | 0459 0344h |
| 348h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT16 | skew_cal_fsm_reg2 | 0458 0348h | 0459 0348h |
| 34Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT17 | skew_cal_fsm_reg3 | 0458 034Ch | 0459 034Ch |
| 350h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT18 | ducy_corr_ctrl_reg1 | 0458 0350h | 0459 0350h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS 2APB_WRAP_VB USP_K3_DPHY_R X Physical Address | DPHY_RX1_VBU S2APB_WRAP_V BUSP_K3_DPHY _RX Physical Address |
|--------|--|---|---|---|
| 354h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT19 | ducy_corr_ctrl_reg2 | 0458 0354h | 0459 0354h |
| 358h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20 | skew_cal_avg_reg1 | 0458 0358h | 0459 0358h |
| 35Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT21 | skew_cal_avg_reg2 | 0458 035Ch | 0459 035Ch |
| 360h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT22 | skew_cal_avg_reg3 | 0458 0360h | 0459 0360h |
| 364h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT23 | skew_cal_avg_reg4 | 0458 0364h | 0459 0364h |
| 368h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT24 | skew_cal_avg_reg5 | 0458 0368h | 0459 0368h |
| 36Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT25 | DIGITAL_EXTRA_CALI B_REG0 | 0458 036Ch | 0459 036Ch |
| 370h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT26 | DIGITAL_EXTRA_CALI B_REG1 | 0458 0370h | 0459 0370h |
| 374h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT27 | bist_config_reg1 | 0458 0374h | 0459 0374h |
| 378h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT28 | bist_config_reg2 | 0458 0378h | 0459 0378h |
| 37Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT29 | bist_config_reg3 | 0458 037Ch | 0459 037Ch |
| 380h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT30 | bist_config_reg4 | 0458 0380h | 0459 0380h |
| 384h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT31 | DIGITAL_EXTRA_TES T_REG1 | 0458 0384h | 0459 0384h |
| 388h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT32 | DIGITAL_EXTRA_TES T_REG2 | 0458 0388h | 0459 0388h |
| 38Ch | DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT2 | ANA_TBIT0 | 0458 038Ch | 0459 038Ch |
| 390h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT33 | deserialiser_fsm_status | 0458 0390h | 0459 0390h |
| 394h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT34 | lp_status | 0458 0394h | 0459 0394h |
| 398h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT35 | DIGITAL_EXTRA_REA D_REG0 | 0458 0398h | 0459 0398h |
| 39Ch | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36 | dcc_mixer_comparator _calibration_stat | 0458 039Ch | 0459 039Ch |
| 3A0h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37 | preamp_cal_status_reg 1 | 0458 03A0h | 0459 03A0h |
| 3A4h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38 | pos_samp_cal_status_ reg1 | 0458 03A4h | 0459 03A4h |
| 3A8h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT39 | pos_samp_cal_status_ reg2 | 0458 03A8h | 0459 03A8h |
| 3ACh | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40 | neg_samp_cal_status_ reg1 | 0458 03ACh | 0459 03ACh |
| 3B0h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT41 | neg_samp_cal_status_ reg2 | 0458 03B0h | 0459 03B0h |
| 3B4h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42 | skew_cal_fsm_status_r eg1 | 0458 03B4h | 0459 03B4h |
| 3B8h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT43 | skew_cal_avg_status_r eg1 | 0458 03B8h | 0459 03B8h |
| 3BCh | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT44 | skew_cal_avg_status_r eg2 | 0458 03BCh | 0459 03BCh |
| 3C0h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT45 | DIGITAL_CALIB_EXTR A_READ_REG0 | 0458 03C0h | 0459 03C0h |
| 3C4h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT46 | DIGITAL_CALIB_EXTR A_READ_REG1 | 0458 03C4h | 0459 03C4h |
| 3C8h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT47 | bist_status_reg1 | 0458 03C8h | 0459 03C8h |
| 3CCh | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT48 | bist_status_reg2 | 0458 03CCh | 0459 03CCh |
| 3D0h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT49 | DIG_BIST_EXTRA_RE AD_REG0 | 0458 03D0h | 0459 03D0h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address | DPHY_RX1_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address |
|--------|--|--------------------------|--|--|
| 3D4h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT50 | DIG_EXTRA_READ_R EG1 | 0458 03D4h | 0459 03D4h |
| 3D8h | DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT51 | DIG_EXTRA_READ_R EG2 | 0458 03D8h | 0459 03D8h |
| 400h | DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT0 | ANA_TBIT0 | 0458 0400h | 0459 0400h |
| 404h | DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT1 | ANA_EXTRA_TBIT0 | 0458 0404h | 0459 0404h |
| 408h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0 | DIG_TBIT0 | 0458 0408h | 0459 0408h |
| 40Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT1 | DIG_TBIT1 | 0458 040Ch | 0459 040Ch |
| 410h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT2 | DIGITAL_EXTRA_TEST_REG0 | 0458 0410h | 0459 0410h |
| 414h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT3 | preamp_cal_ctrl_reg1 | 0458 0414h | 0459 0414h |
| 418h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4 | preamp_cal_ctrl_reg2 | 0458 0418h | 0459 0418h |
| 41Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT5 | dcc_comp_cal_ctrl_reg1 | 0458 041Ch | 0459 041Ch |
| 420h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6 | dcc_comp_cal_ctrl_reg2 | 0458 0420h | 0459 0420h |
| 424h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT7 | mix_comp_cal_ctrl_reg1 | 0458 0424h | 0459 0424h |
| 428h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8 | mix_comp_cal_ctrl_reg2 | 0458 0428h | 0459 0428h |
| 42Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT9 | pos_samp_cal_ctrl_reg1 | 0458 042Ch | 0459 042Ch |
| 430h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10 | pos_samp_cal_ctrl_reg2 | 0458 0430h | 0459 0430h |
| 434h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT11 | pos_samp_cal_ctrl_reg3 | 0458 0434h | 0459 0434h |
| 438h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT12 | neg_samp_cal_ctrl_reg1 | 0458 0438h | 0459 0438h |
| 43Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13 | neg_samp_cal_ctrl_reg2 | 0458 043Ch | 0459 043Ch |
| 440h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT14 | neg_samp_cal_ctrl_reg3 | 0458 0440h | 0459 0440h |
| 444h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT15 | skew_cal_fsm_reg1 | 0458 0444h | 0459 0444h |
| 448h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT16 | skew_cal_fsm_reg2 | 0458 0448h | 0459 0448h |
| 44Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT17 | skew_cal_fsm_reg3 | 0458 044Ch | 0459 044Ch |
| 450h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT18 | ducy_corr_ctrl_reg1 | 0458 0450h | 0459 0450h |
| 454h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT19 | ducy_corr_ctrl_reg2 | 0458 0454h | 0459 0454h |
| 458h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20 | skew_cal_avg_reg1 | 0458 0458h | 0459 0458h |
| 45Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT21 | skew_cal_avg_reg2 | 0458 045Ch | 0459 045Ch |
| 460h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT22 | skew_cal_avg_reg3 | 0458 0460h | 0459 0460h |
| 464h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT23 | skew_cal_avg_reg4 | 0458 0464h | 0459 0464h |
| 468h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT24 | skew_cal_avg_reg5 | 0458 0468h | 0459 0468h |
| 46Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT25 | DIGITAL_EXTRA_CALIB_REG0 | 0458 046Ch | 0459 046Ch |
| 470h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT26 | DIGITAL_EXTRA_CALIB_REG1 | 0458 0470h | 0459 0470h |
| 474h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT27 | bist_config_reg1 | 0458 0474h | 0459 0474h |
| 478h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT28 | bist_config_reg2 | 0458 0478h | 0459 0478h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address | DPHY_RX1_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address |
|--------|--|---------------------------------------|--|--|
| 47Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT29 | bist_config_reg3 | 0458 047Ch | 0459 047Ch |
| 480h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT30 | bist_config_reg4 | 0458 0480h | 0459 0480h |
| 484h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT31 | DIGITAL_EXTRA_TEST_REG1 | 0458 0484h | 0459 0484h |
| 488h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT32 | DIGITAL_EXTRA_TEST_REG2 | 0458 0488h | 0459 0488h |
| 48Ch | DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT2 | ANA_TBIT0 | 0458 048Ch | 0459 048Ch |
| 490h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT33 | deserialiser_fsm_status | 0458 0490h | 0459 0490h |
| 494h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT34 | lp_status | 0458 0494h | 0459 0494h |
| 498h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT35 | DIGITAL_EXTRA_READ_REG0 | 0458 0498h | 0459 0498h |
| 49Ch | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36 | dcc_mixer_comparator_calibration_stat | 0458 049Ch | 0459 049Ch |
| 4A0h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37 | preamp_cal_status_reg1 | 0458 04A0h | 0459 04A0h |
| 4A4h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38 | pos_samp_cal_status_reg1 | 0458 04A4h | 0459 04A4h |
| 4A8h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT39 | pos_samp_cal_status_reg2 | 0458 04A8h | 0459 04A8h |
| 4ACh | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40 | neg_samp_cal_status_reg1 | 0458 04ACh | 0459 04ACh |
| 4B0h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT41 | neg_samp_cal_status_reg2 | 0458 04B0h | 0459 04B0h |
| 4B4h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42 | skew_cal_fsm_status_reg1 | 0458 04B4h | 0459 04B4h |
| 4B8h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT43 | skew_cal_avg_status_reg1 | 0458 04B8h | 0459 04B8h |
| 4BCh | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT44 | skew_cal_avg_status_reg2 | 0458 04BCh | 0459 04BCh |
| 4C0h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT45 | DIGITAL_CALIB_EXTRACT_READ_REG0 | 0458 04C0h | 0459 04C0h |
| 4C4h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT46 | DIGITAL_CALIB_EXTRACT_READ_REG1 | 0458 04C4h | 0459 04C4h |
| 4C8h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT47 | bist_status_reg1 | 0458 04C8h | 0459 04C8h |
| 4CCh | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT48 | bist_status_reg2 | 0458 04CCh | 0459 04CCh |
| 4D0h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT49 | DIG_BIST_EXTRA_READ_REG0 | 0458 04D0h | 0459 04D0h |
| 4D4h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT50 | DIG_EXTRA_READ_REG1 | 0458 04D4h | 0459 04D4h |
| 4D8h | DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT51 | DIG_EXTRA_READ_REG2 | 0458 04D8h | 0459 04D8h |
| 500h | DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT0 | ANA_TBIT0 | 0458 0500h | 0459 0500h |
| 504h | DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT1 | ANA_EXTRA_TBIT0 | 0458 0504h | 0459 0504h |
| 508h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0 | DIG_TBIT0 | 0458 0508h | 0459 0508h |
| 50Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT1 | DIG_TBIT1 | 0458 050Ch | 0459 050Ch |
| 510h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT2 | DIGITAL_EXTRA_TEST_REG0 | 0458 0510h | 0459 0510h |
| 514h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT3 | preamp_cal_ctrl_reg1 | 0458 0514h | 0459 0514h |
| 518h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4 | preamp_cal_ctrl_reg2 | 0458 0518h | 0459 0518h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS 2APB_WRAP_VB USP_K3_DPHY_R X Physical Address | DPHY_RX1_VBU S2APB_WRAP_V BUSP_K3_DPHY _RX Physical Address |
|--------|--|---|---|---|
| 51Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT5 | dcc_comp_cal_ctrl_reg 1 | 0458 051Ch | 0459 051Ch |
| 520h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6 | dcc_comp_cal_ctrl_reg 2 | 0458 0520h | 0459 0520h |
| 524h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT7 | mix_comp_cal_ctrl_reg 1 | 0458 0524h | 0459 0524h |
| 528h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8 | mix_comp_cal_ctrl_reg 2 | 0458 0528h | 0459 0528h |
| 52Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT9 | pos_samp_cal_ctrl_reg 1 | 0458 052Ch | 0459 052Ch |
| 530h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10 | pos_samp_cal_ctrl_reg 2 | 0458 0530h | 0459 0530h |
| 534h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT11 | pos_samp_cal_ctrl_reg 3 | 0458 0534h | 0459 0534h |
| 538h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT12 | neg_samp_cal_ctrl_reg 1 | 0458 0538h | 0459 0538h |
| 53Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13 | neg_samp_cal_ctrl_reg 2 | 0458 053Ch | 0459 053Ch |
| 540h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT14 | neg_samp_cal_ctrl_reg 3 | 0458 0540h | 0459 0540h |
| 544h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT15 | skew_cal_fsm_reg1 | 0458 0544h | 0459 0544h |
| 548h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT16 | skew_cal_fsm_reg2 | 0458 0548h | 0459 0548h |
| 54Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT17 | skew_cal_fsm_reg3 | 0458 054Ch | 0459 054Ch |
| 550h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT18 | ducy_corr_ctrl_reg1 | 0458 0550h | 0459 0550h |
| 554h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT19 | ducy_corr_ctrl_reg2 | 0458 0554h | 0459 0554h |
| 558h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20 | skew_cal_avg_reg1 | 0458 0558h | 0459 0558h |
| 55Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT21 | skew_cal_avg_reg2 | 0458 055Ch | 0459 055Ch |
| 560h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT22 | skew_cal_avg_reg3 | 0458 0560h | 0459 0560h |
| 564h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT23 | skew_cal_avg_reg4 | 0458 0564h | 0459 0564h |
| 568h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT24 | skew_cal_avg_reg5 | 0458 0568h | 0459 0568h |
| 56Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT25 | DIGITAL_EXTRA_CALI B_REG0 | 0458 056Ch | 0459 056Ch |
| 570h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT26 | DIGITAL_EXTRA_CALI B_REG1 | 0458 0570h | 0459 0570h |
| 574h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT27 | bist_config_reg1 | 0458 0574h | 0459 0574h |
| 578h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT28 | bist_config_reg2 | 0458 0578h | 0459 0578h |
| 57Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT29 | bist_config_reg3 | 0458 057Ch | 0459 057Ch |
| 580h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT30 | bist_config_reg4 | 0458 0580h | 0459 0580h |
| 584h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT31 | DIGITAL_EXTRA_TES T_REG1 | 0458 0584h | 0459 0584h |
| 588h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT32 | DIGITAL_EXTRA_TES T_REG2 | 0458 0588h | 0459 0588h |
| 58Ch | DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT2 | ANA_TBIT0 | 0458 058Ch | 0459 058Ch |
| 590h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT33 | deserialiser_fsm_status | 0458 0590h | 0459 0590h |
| 594h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT34 | lp_status | 0458 0594h | 0459 0594h |
| 598h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT35 | DIGITAL_EXTRA_REA D_REG0 | 0458 0598h | 0459 0598h |
| 59Ch | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36 | dcc_mixer_comparator _calibration_stat | 0458 059Ch | 0459 059Ch |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address | DPHY_RX1_VBUS2APB_WRAP_VBUSP_K3_DPHY_RX Physical Address |
|--------|---|---------------------------------|--|--|
| 5A0h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37 | preamp_cal_status_reg1 | 0458 05A0h | 0459 05A0h |
| 5A4h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38 | pos_samp_cal_status_reg1 | 0458 05A4h | 0459 05A4h |
| 5A8h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT39 | pos_samp_cal_status_reg2 | 0458 05A8h | 0459 05A8h |
| 5ACh | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40 | neg_samp_cal_status_reg1 | 0458 05ACh | 0459 05ACh |
| 5B0h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT41 | neg_samp_cal_status_reg2 | 0458 05B0h | 0459 05B0h |
| 5B4h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42 | skew_cal_fsm_status_reg1 | 0458 05B4h | 0459 05B4h |
| 5B8h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT43 | skew_cal_avg_status_reg1 | 0458 05B8h | 0459 05B8h |
| 5BCh | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT44 | skew_cal_avg_status_reg2 | 0458 05BCh | 0459 05BCh |
| 5C0h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT45 | DIGITAL_CALIB_EXTRACT_READ_REG0 | 0458 05C0h | 0459 05C0h |
| 5C4h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT46 | DIGITAL_CALIB_EXTRACT_READ_REG1 | 0458 05C4h | 0459 05C4h |
| 5C8h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT47 | bist_status_reg1 | 0458 05C8h | 0459 05C8h |
| 5CCh | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT48 | bist_status_reg2 | 0458 05CCh | 0459 05CCh |
| 5D0h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT49 | DIG_BIST_EXTRA_READ_REG0 | 0458 05D0h | 0459 05D0h |
| 5D4h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT50 | DIG_EXTRA_READ_REG1 | 0458 05D4h | 0459 05D4h |
| 5D8h | DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT51 | DIG_EXTRA_READ_REG2 | 0458 05D8h | 0459 05D8h |
| B00h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0 | PHY_BAND_CONTROL | 0458 0B00h | 0459 0B00h |
| B04h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1 | PHY_PSM_CONFIG | 0458 0B04h | 0459 0B04h |
| B08h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2 | PHY_PI_PH2_DL_CONFIG | 0458 0B08h | 0459 0B08h |
| B0Ch | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3 | PHY_PI_PH2_CL_CONFIG | 0458 0B0Ch | 0459 0B0Ch |
| B10h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT4 | PHY_PI_PH1_DL_CONFIG | 0458 0B10h | 0459 0B10h |
| B14h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT5 | PHY_PI_PH1_CL_CONFIG | 0458 0B14h | 0459 0B14h |
| B18h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT6 | PHY_DL_SPARE_LEFT | 0458 0B18h | 0459 0B18h |
| B1Ch | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT7 | PHY_DL_SPARE_RIGHT | 0458 0B1Ch | 0459 0B1Ch |
| B20h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT8 | PHY_CL_CMN_SPARE | 0458 0B20h | 0459 0B20h |
| B24h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT9 | PHY_PI_CONFIG | 0458 0B24h | 0459 0B24h |
| B28h | DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT10 | DIG_TBIT10 | 0458 0B28h | 0459 0B28h |
| C00h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_CNTRL | PHY_ISO_CNTRL | 0458 0C00h | 0459 0C00h |
| C04h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_RESET | PHY_ISO_RESET | 0458 0C04h | 0459 0C04h |
| C08h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_ENABLE | PHY_ISO_ENABLE | 0458 0C08h | 0459 0C08h |

Table 11-3. DPHY_RX_VBUS2APB Registers (continued)

| Offset | Acronym | Register Name | DPHY_RX0_VBUS 2APB_WRAP_VB USP_K3_DPHY_R X Physical Address | DPHY_RX1_VBU S2APB_WRAP_V BUSP_K3_DPHY _RX Physical Address |
|--------|---|----------------------|---|---|
| C0Ch | DPHY_RX_VBUS2APB_ISO_PHY_ISO_CMN_CTRL | PHY_ISO_CMN_CTRL | 0458 0C0Ch | 0459 0C0Ch |
| C10h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_CL_CNTRL_L | PHY_ISO_CL_CNTRL_L | 0458 0C10h | 0459 0C10h |
| C14h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L0 | PHY_ISO_DL_CTRL_L0 | 0458 0C14h | 0459 0C14h |
| C18h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L0 | PHY_ISO_DL_HS_L0 | 0458 0C18h | 0459 0C18h |
| C1Ch | DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L0 | PHY_ISO_DL_RX_ESC_L0 | 0458 0C1Ch | 0459 0C1Ch |
| C20h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L1 | PHY_ISO_DL_CTRL_L1 | 0458 0C20h | 0459 0C20h |
| C24h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L1 | PHY_ISO_DL_HS_L1 | 0458 0C24h | 0459 0C24h |
| C28h | DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L1 | PHY_ISO_DL_RX_ESC_L1 | 0458 0C28h | 0459 0C28h |
| C2Ch | DPHY_RX_VBUS2APB_ISO_PHY_ISO_SPARE_1 | PHY_ISO_SPARE_1 | 0458 0C2Ch | 0459 0C2Ch |
| C30h | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L2 | PHY_ISO_DL_CTRL_L2 | 0458 0C30h | 0459 0C30h |
| C34h | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L2 | PHY_ISO_DL_HS_L2 | 0458 0C34h | 0459 0C34h |
| C38h | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 | PHY_ISO_DL_RX_ESC_L2 | 0458 0C38h | 0459 0C38h |
| C3Ch | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L3 | PHY_ISO_DL_CTRL_L3 | 0458 0C3Ch | 0459 0C3Ch |
| C40h | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L3 | PHY_ISO_DL_HS_L3 | 0458 0C40h | 0459 0C40h |
| C44h | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 | PHY_ISO_DL_RX_ESC_L3 | 0458 0C44h | 0459 0C44h |
| C48h | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_1 | PHY_ISO_RX_SPARE_1 | 0458 0C48h | 0459 0C48h |
| C4Ch | DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_2 | PHY_ISO_RX_SPARE_2 | 0458 0C4Ch | 0459 0C4Ch |

11.2 DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT0 Register (Offset = 0h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT0 is shown in [Figure 11-1](#) and described in [Table 11-5](#).

Return to [Summary Table](#).

CMN_ANA_TBIT0

Table 11-4.
DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0000h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0000h |

Figure 11-1. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-5. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

11.3 DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT1 Register (Offset = 4h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT1 is shown in [Figure 11-2](#) and described in [Table 11-7](#).

Return to [Summary Table](#).

CMN_ANA_TBIT1

Table 11-6.
DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0004h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0004h |

Figure 11-2. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-7. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

11.4 DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT2 Register (Offset = 8h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT2 is shown in [Figure 11-3](#) and described in [Table 11-9](#).

Return to [Summary Table](#).

CMN_ANA_TBIT2

Table 11-8.
DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0008h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0008h |

Figure 11-3. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-9. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

11.5 DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT3 Register (Offset = Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT3 is shown in [Figure 11-4](#) and described in [Table 11-11](#).

Return to [Summary Table](#).

CMN_ANA_TBIT3

Table 11-10.
DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 000Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 000Ch |

Figure 11-4. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-11. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|-------------|
| 31-0 | ANA_TBIT3 | R | 0h | RESERVED |

11.6 DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT4 Register (Offset = 10h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT4 is shown in [Figure 11-5](#) and described in [Table 11-13](#).

Return to [Summary Table](#).

CMN_ANA_TBIT4

Table 11-12.
DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT4
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0010h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0010h |

Figure 11-5. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-13. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

11.7 DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT5 Register (Offset = 14h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT5 is shown in [Figure 11-6](#) and described in [Table 11-15](#).

Return to [Summary Table](#).

CMN_ANA_TBIT5

Table 11-14.
DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0014h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0014h |

Figure 11-6. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | | | ANA_TBIT5 | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-15. DPHY_RX_VBUS2APB_CMN0_CMN_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-8 | UNUSED | R | 0h | RESERVED |
| 7-0 | ANA_TBIT5 | R/W | 0h | Analog Test register 5 |

11.8 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0 Register (Offset = 18h) [reset = 1140h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0 is shown in [Figure 11-7](#) and described in [Table 11-17](#).

Return to [Summary Table](#).

CMN_DIG_TBIT0

Table 11-16.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0018h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0018h |

Figure 11-7. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------------------|-------------------------------------|------------------------------|------------------------------------|------------------------------|-----------------------------------|---------------------------------|----|
| UNUSED | | | O_RES_CAL_S TART_TM | O_RES_CAL_S TART_TM_SEL | O_RES_COMP _OUT_POL_IN V_TM | O_RES_TX_OFFSET_TEST_LO W_TM | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_RES_TX_OFFSET_TEST_LO W_TM | O_RES_TX_OF FSET_LOW_D EC_TM | | O_RES_TX_OF FSET_LOW_T M_SEL | O_RES_TX_OFFSET_TEST_HIGH_TM | | | |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_RES_TX_OF FSET_HIGH_D EC_TM | O_RES_TX_OF FSET_HIGH_T M_SEL | O_RES_CALIB_DECISION_WAIT_TM | | | | O_RES_CALIB_INIT_WAIT_TM | |
| R/W-0h | R/W-0h | R/W-4h | | | | R/W-5h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RES_CALIB_INIT_WAIT_TM | O_RES_CALIB _RSTB_TM | | O_RES_CALIB _RSTB_TM_SE L | UNUSED2 | | | |
| R/W-5h | | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-17. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | O_RES_CAL_START_TM | R/W | 0h | res_cal_start in test mode |
| 27 | O_RES_CAL_START_TM _SEL | R/W | 0h | res_cal_start select from test_mode |
| 26 | O_RES_COMP_OUT_PO L_INV_TM | R/W | 0h | Invert polarity for resistor calib comparator output |
| 25-22 | O_RES_TX_OFFSET_TE ST_LOW_TM | R/W | 0h | o_res_tx_offset_test_low_TM - Res calib manipulation code for res calib code low |
| 21 | O_RES_TX_OFFSET_LO W_DEC_TM | R/W | 0h | o_res_tx_offset_low_dec_TM asserted - Perform increment manipulation on res calib code if o_res_tx_offset_low_TM_sel is asserted |

Table 11-17. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--|
| 20 | O_RES_TX_OFFSET_LO W_TM_SEL | R/W | 0h | o_res_tx_offset_low_TM_sel asserted - Enable offset manipulation for res calib code low |
| 19-16 | O_RES_TX_OFFSET_TE ST_HIGH_TM | R/W | 0h | o_res_tx_offset_test_high_TM - Res calib manipulation code for res calib code high |
| 15 | O_RES_TX_OFFSET_HI GH_DEC_TM | R/W | 0h | o_res_tx_offset_high_dec_TM asserted - Perform increment manipulation on res calib code if o_res_tx_offset_high_TM_sel is asserted |
| 14 | O_RES_TX_OFFSET_HI GH_TM_SEL | R/W | 0h | o_res_tx_offset_high_TM_sel asserted - Enable offset manipulation for res calib code high |
| 13-10 | O_RES_CALIB_DECISIO N_WAIT_TM | R/W | 4h | res_calib decision wait time |
| 9-6 | O_RES_CALIB_INIT_WAI T_TM | R/W | 5h | res_calib initial wait time |
| 5 | O_RES_CALIB_RSTB_T M | R/W | 0h | w_res_calib_rstb value in testmode |
| 4 | O_RES_CALIB_RSTB_T M_SEL | R/W | 0h | w_res_calib_rstb select from test_mode |
| 3-0 | UNUSED2 | R | 0h | RESERVED |

11.9 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1 Register (Offset = 1Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1 is shown in [Figure 11-8](#) and described in [Table 11-19](#).

Return to [Summary Table](#).

CMN_DIG_TBIT1

Table 11-18.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 001Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 001Ch |

Figure 11-8. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|-------------------------|----|----|--------------------|------------------------|-------------------------------------|
| O_ATB_EN | O_ATB_SRC | BF_29_17 | | | | | |
| R/W-0h | R/W-0h | R/W-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_29_17 | | | | | | | O_ANA_PLL_A TB_CP_CUR_S EL |
| R/W-0h | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_ANA_PLL_A TBH_GM_CUR _SEL | UNUSED | | | | O_ANA_BG_P D_TM | O_ANA_BG_P D_TM_SEL | |
| R/W-0h | R-0h | | | | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_RES_ CALIB_PD_TM | O_ANA_RES_ CALIB_PD_TM _SEL | O_ANA_RES_CALIB_CODE_TM | | | | | O_ANA_RES_ CALIB_CODE_ TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-19. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31 | O_ATB_EN | R/W | 0h | ATB probing enabled |
| 30 | O_ATB_SRC | R/W | 0h | Select IO for atb probing |
| 29-17 | BF_29_17 | R/W | 0h | |
| 16 | O_ANA_PLL_ATB_CP_C UR_SEL | R/W | 0h | o_ana_pll_atb_cp_cur_sel |
| 15 | O_ANA_PLL_ATBH_GM_ CUR_SEL | R/W | 0h | o_ana_pll_atbh_gm_cur_sel |
| 14-10 | UNUSED | R | 0h | RESERVED |
| 9 | O_ANA_BG_PD_TM | R/W | 0h | o_ana_bg_pd value in testmode |
| 8 | O_ANA_BG_PD_TM_SEL | R/W | 0h | o_ana_bg_pd select from test_mode |
| 7 | O_ANA_RES_CALIB_PD_ TM | R/W | 0h | o_ana_res_calib_pd value in testmode |
| 6 | O_ANA_RES_CALIB_PD_ TM_SEL | R/W | 0h | o_ana_res_calib_pd select from test_mode |

Table 11-19. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|--|
| 5-1 | O_ANA_RES_CALIB_CODE_TM | R/W | 0h | o_ana_res_calib_code value in test_mode |
| 0 | O_ANA_RES_CALIB_CODE_TM_SEL | R/W | 0h | o_ana_res_calib_code select from test_mode |

11.10 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2 Register (Offset = 20h) [reset = 28h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2 is shown in [Figure 11-9](#) and described in [Table 11-21](#).

Return to [Summary Table](#).

CMN_DIG_TBIT2

Table 11-20.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0020h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0020h |

Figure 11-9. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2 Register

| | | | | | | | |
|---------------------|----|----|----|----|----------------------|----------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | O_CMN_RX_M ODE_EN | O_CMN_TX_M ODE_EN | O_SSM_WAIT_ BGCAL_EN |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-14h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_SSM_WAIT_BGCAL_EN | | | | | | O_CMN_SSM_ EN | |
| R/W-14h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-21. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-11 | UNUSED | R | 0h | RESERVED |
| 10 | O_CMN_RX_MODE_EN | R/W | 0h | Enable CMN RX related StateMachines |
| 9 | O_CMN_TX_MODE_EN | R/W | 0h | Enable CMN TX related StateMachines |
| 8-1 | O_SSM_WAIT_BGCAL_EN | R/W | 14h | Wait time for Calibrations enable after bandgap is enabled [in us] |
| 0 | O_CMN_SSM_EN | R/W | 0h | Enable CMN startup state machine |

11.11 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT3 Register (Offset = 24h) [reset = 05030101h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT3 is shown in [Figure 11-10](#) and described in [Table 11-23](#).

Return to [Summary Table](#).

CMN_DIG_TBIT3

Table 11-22.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0024h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0024h |

Figure 11-10. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT3 Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_PLL_WAIT_PLL_ACCINV | | | | | | | | O_PLL_WAIT_PLL_BIAS | | | | | | | |
| R/W-5h | | | | | | | | R/W-3h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_PLL_WAIT_PLL_EN_DEL | | | | | | | | O_PLL_WAIT_PLL_EN | | | | | | | |
| R/W-1h | | | | | | | | R/W-1h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-23. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---------------------------------|
| 31-24 | O_PLL_WAIT_PLL_ACCINV | R/W | 5h | Wait time in pll_accinv [in us] |
| 23-16 | O_PLL_WAIT_PLL_BIAS | R/W | 3h | Wait time in pll_bias [in us] |
| 15-8 | O_PLL_WAIT_PLL_EN_DEL | R/W | 1h | Wait time in pll_en_del [in us] |
| 7-0 | O_PLL_WAIT_PLL_EN | R/W | 1h | Wait time in PLL en [in us] |

11.12 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT4 Register (Offset = 28h) [reset = 0032011Eh]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT4 is shown in [Figure 11-11](#) and described in [Table 11-25](#).

Return to [Summary Table](#).

CMN_DIG_TBIT4

Table 11-24.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT4
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0028h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0028h |

Figure 11-11. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT4 Register

| | | | | | | | |
|-------------------------------|----|----|----|------------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | O_PLL_WAIT_PLL_LOCK_DET_WAIT | | | |
| R-0h | | | | R/W-32h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_PLL_WAIT_PLL_LOCK_DET_WAIT | | | | | | | |
| R/W-32h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_PLL_WAIT_PLL_RST_DEASSERT_2 | | | | | | | |
| R/W-1h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_PLL_WAIT_PLL_RST_DEASSERT | | | | | | | |
| R/W-1Eh | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-25. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-28 | UNUSED | R | 0h | RESERVED |
| 27-16 | O_PLL_WAIT_PLL_LOCK_DET_WAIT | R/W | 32h | Wait time in pll_lock_det_wait [in us] |
| 15-8 | O_PLL_WAIT_PLL_RST_DEASSERT_2 | R/W | 1h | Wait time in pll_rst_deassert_2ndset [in us] |
| 7-0 | O_PLL_WAIT_PLL_RST_DEASSERT | R/W | 1Eh | Wait time in pll_rst_deassert [in us] |

11.13 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT5 Register (Offset = 2Ch) [reset = 400h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT5 is shown in [Figure 11-12](#) and described in [Table 11-27](#).

Return to [Summary Table](#).

Table 11-26.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 002Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 002Ch |

Figure 11-12. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT5 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|----|---------------------------------|-----------------|---------------------|----------------------|-----------------------------|--------|
| O_CMN_TX_READY_TM_SEL | | O_PLL_PROCEED_WITH_LOCK_FAIL_TM | O_PLL_LOCKED_TM | O_PLL_LOCKED_TM_SEL | O_PLL_LOCK_DET_EN_TM | O_PLL_LOCK_DET_EN_TM_SEL | UNUSED |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | O_PLL_WAIT_PLL_LOCK_TIMEOUT | |
| R-0h | | | | | | R/W-400h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_PLL_WAIT_PLL_LOCK_TIMEOUT | | | | | | | |
| R/W-400h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_PLL_WAIT_PLL_LOCK_TIMEOUT | | | | | | | |
| R/W-400h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-27. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|--|
| 31-30 | O_CMN_TX_READY_TM_SEL | R/W | 0h | ATB probing enabled |
| 29 | O_PLL_PROCEED_WITH_LOCK_FAIL_TM | R/W | 0h | o_ana_pll_atb_cp_cur_sel |
| 28 | O_PLL_LOCKED_TM | R/W | 0h | Forced value of pll_locked going to fsm = 1 |
| 27 | O_PLL_LOCKED_TM_SEL | R/W | 0h | pll_locked going to fsm forced from test registers |
| 26 | O_PLL_LOCK_DET_EN_TM | R/W | 0h | Forced value of pll_lock_det_en = 1 |
| 25 | O_PLL_LOCK_DET_EN_TM_SEL | R/W | 0h | pll_lock_det_en forced from test registers |
| 24-18 | UNUSED | R | 0h | RESERVED |
| 17-0 | O_PLL_WAIT_PLL_LOCK_TIMEOUT | R/W | 400h | Wait time for pll_lock_timeout [in us] |

11.14 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT6 Register (Offset = 30h) [reset = 000400C8h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT6 is shown in [Figure 11-13](#) and described in [Table 11-29](#).

Return to [Summary Table](#).

CMN_DIG_TBIT6

Table 11-28.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0030h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0030h |

Figure 11-13. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_LOCKDET_REFCNT_IDLE_VALUE | | | | | | | | | | | | | | | |
| R/W-4h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_LOCKDET_REFCNT_START_VALUE | | | | | | | | | | | | | | | |
| R/W-C8h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-29. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-16 | O_LOCKDET_REFCNT_IDLE_VALUE | R/W | 4h | refcnt idle value for PLL lock detect module |
| 15-0 | O_LOCKDET_REFCNT_START_VALUE | R/W | C8h | refcnt start value for PLL lock detect module |

11.15 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT7 Register (Offset = 34h) [reset = 000300C8h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT7 is shown in [Figure 11-14](#) and described in [Table 11-31](#).

Return to [Summary Table](#).

CMN_DIG_TBIT7

Table 11-30.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0034h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0034h |

Figure 11-14. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | |
|---------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_LOCKDET_PLLCNT_LOCK_THR_VALUE | | | | | | | | | | | | | | | |
| R/W-3h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_LOCKDET_PLLCNT_START_VALUE | | | | | | | | | | | | | | | |
| R/W-C8h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-31. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|--|
| 31-16 | O_LOCKDET_PLLCNT_LOCK_THR_VALUE | R/W | 3h | pllcnt lock threshold value for PLL lock detect module |
| 15-0 | O_LOCKDET_PLLCNT_START_VALUE | R/W | C8h | pllcnt start value for PLL lock detect module |

11.16 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT8 Register (Offset = 38h) [reset = 00080103h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT8 is shown in [Figure 11-15](#) and described in [Table 11-33](#).

Return to [Summary Table](#).

CMN_DIG_TBIT8

Table 11-32.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0038h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0038h |

Figure 11-15. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT8 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| O_ANA_PLL_VRESET_VCTRL_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_ANA_PLL_VRESET_VCO_BIAS_TUNE | | | | | | | |
| R/W-8h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_ANA_PLL_GM_TUNE | | | | | | | |
| R/W-1h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_PLL_CP_TUNE | | | | | | | |
| R/W-3h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-33. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31-24 | O_ANA_PLL_VRESET_VCTRL_TUNE | R/W | 0h | unconnected, intended for vreset_vctrl[CP output] programmability |
| 23-16 | O_ANA_PLL_VRESET_VCO_BIAS_TUNE | R/W | 8h | Programmability for vco bias[gmbyc] initial voltage |
| 15-8 | O_ANA_PLL_GM_TUNE | R/W | 1h | gm tune value for PLL |
| 7-0 | O_ANA_PLL_CP_TUNE | R/W | 3h | Charge Pump Tune value for PLL |

11.17 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT9 Register (Offset = 3Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT9 is shown in [Figure 11-16](#) and described in [Table 11-35](#).

Return to [Summary Table](#).

CMN_DIG_TBIT9

Table 11-34.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT9
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 003Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 003Ch |

Figure 11-16. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT9 Register

| | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| O_ANA_PLL_VREF_VCO_BIAS_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_ANA_PLL_VCO_BIAS_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_ANA_PLL_GMBYC_CAP_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_PLL_LOOP_FILTER_TUNE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-35. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-24 | O_ANA_PLL_VREF_VCO_BIAS_TUNE | R/W | 0h | Tuning Control for reference vco bias in PLL |
| 23-16 | O_ANA_PLL_VCO_BIAS_TUNE | R/W | 0h | Tuning Control for PLL vco bias |
| 15-8 | O_ANA_PLL_GMBYC_CAP_TUNE | R/W | 0h | gmbyc tune value for PLL |
| 7-0 | O_ANA_PLL_LOOP_FILTER_TUNE | R/W | 0h | Tuning Control for loop filter |

11.18 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT10 Register (Offset = 40h) [reset = 00800000h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT10 is shown in [Figure 11-17](#) and described in [Table 11-37](#).

Return to [Summary Table](#).

CMN_DIG_TBIT10

Table 11-36.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT10
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0040h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0040h |

Figure 11-17. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT10 Register

| | | | | | | | | | | | | | | | |
|--------------------------|----|----|----|-----------------------|----|---------------------------|----|----|----|----|----|------------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | O_ANA_PLL_BYTECLK_DIV | | | | | | | | O_ANA_PLL_GM_PWM_DIV_LO W | | | |
| R-0h | | | | R/W-8h | | | | | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_PLL_GM_PWM_DIV_LOW | | | | | | O_ANA_PLL_GM_PWM_DIV_HIGH | | | | | | | | | |
| R/W-0h | | | | | | R/W-0h | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-37. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|--|
| 31-28 | UNUSED | R | 0h | RESERVED |
| 27-20 | O_ANA_PLL_BYTECLK_DIV | R/W | 8h | Byteclk divider value |
| 19-10 | O_ANA_PLL_GM_PWM_DIV_LOW | R/W | 0h | Low division value setting for the gm PWM control divider |
| 9-0 | O_ANA_PLL_GM_PWM_DIV_HIGH | R/W | 0h | High division value setting for the gm PWM control divider |

11.19 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11 Register (Offset = 44h) [reset = 15h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11 is shown in [Figure 11-18](#) and described in [Table 11-39](#).

Return to [Summary Table](#).

CMN_DIG_TBIT11

Table 11-38.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0044h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0044h |

Figure 11-18. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11 Register

| | | | | | | | |
|----------------------|-------------------------------------|--------------------------|------------------------------------|---------------------------------------|------------------------------------|------------------------------------|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| O_ANA_PLL_CYA | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_ANA_PLL_CYA | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | O_ANA_PLL_PFD_EN_1U_DE L_TM_SEL | O_ANA_PLL_V RESET_VCO_ BIAS_SEL | O_ANA_PLL_V RESET_VCTRL _SEL | O_ANA_PLL_S EL_FBCLK_GM _PWM | O_ANA_PLL_O P_BY2_BYPAS S |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_PLL_B YPASS | O_ANA_PLL_F BDIV_CLKINBY 2_EN | O_ANA_PLL_D SM_CLK_EN | O_ANA_PLL_G M_PWM_EN | O_ANA_PLL_O P_DIV_CLK_E N | O_ANA_PLL_IP _DIV_CLK_EN | O_ANA_PLL_R EF_CLK_EN | O_ANA_PLL_F B_DIV_CLK_E N |
| R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-0h | R/W-1h | R/W-0h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-39. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-16 | O_ANA_PLL_CYA | R/W | 0h | Drives pllda_cya going to ANA |
| 15-13 | UNUSED | R | 0h | RESERVED |
| 12 | O_ANA_PLL_PFD_EN_1 U_DEL_TM_SEL | R/W | 0h | Testmode signal for selecting 1us delayed for pll_pfd_reset_n |
| 11 | O_ANA_PLL_VRESET_V CO_BIAS_SEL | R/W | 0h | vreset_vctrl_gmbyc is set inside the pll_vreset_gen |
| 10 | O_ANA_PLL_VRESET_V CTRL_SEL | R/W | 0h | vreset_vctrl is set to ground inside the pll_vreset_gen |
| 9 | O_ANA_PLL_SEL_FBCL K_GM_PWM | R/W | 0h | Enable mode to use feedback clock as the PWM control input for the gm stage |
| 8 | O_ANA_PLL_OP_BY2_B YPASS | R/W | 0h | Mode to bypass the divide by 2 in the PLL output which generates clk_bit and clk_bitb |
| 7 | O_ANA_PLL_BYPASS | R/W | 0h | Bypass PLL and pass refclk as output |
| 6 | O_ANA_PLL_FBDIV_CLK INBY2_EN | R/W | 0h | Enable division by 2 on the feedback divider input clock |

Table 11-39. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT11 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|---|
| 5 | O_ANA_PLL_DSM_CLK_EN | R/W | 0h | Enable for dsm clock output to digital |
| 4 | O_ANA_PLL_GM_PWM_EN | R/W | 1h | Enable PWM control of the gm, else it will operate in the continuous mode |
| 3 | O_ANA_PLL_OP_DIV_CLK_EN | R/W | 0h | Enable for op divider clock output to digital |
| 2 | O_ANA_PLL_IP_DIV_CLK_EN | R/W | 1h | Enable for ip divider output to digital |
| 1 | O_ANA_PLL_REF_CLK_EN | R/W | 0h | enables refclk to PLL |
| 0 | O_ANA_PLL_FB_DIV_CLK_EN | R/W | 1h | Enable for feedback clock output to digital |

11.20 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12 Register (Offset = 48h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12 is shown in [Figure 11-19](#) and described in [Table 11-41](#).

Return to [Summary Table](#).

CMN_DIG_TBIT12

Table 11-40.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0048h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0048h |

Figure 11-19. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--|--|---------------------------------|-------------------------------------|--|--|--------------------------------------|--|
| O_ANA_PLL_V RESET_GEN_ EN_TM | O_ANA_PLL_V RESET_GEN_ EN_TM_SEL | O_ANA_PLL_P FD_EN_TM | O_ANA_PLL_P FD_EN_TM_SE L | O_ANA_PLL_L OOP_FILTER_ RESET_N_TM | O_ANA_PLL_L OOP_FILTER_ RESET_N_TM_ SEL | O_ANA_PLL_G M_RESET_N_T M | O_ANA_PLL_G M_RESET_N_T M_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_ANA_PLL_G M_BYCAP_R RESET_N_TM | O_ANA_PLL_G M_BYCAP_R RESET_N_TM_S EL | O_ANA_PLL_C P_RESET_N_T M | O_ANA_PLL_C P_RESET_N_T M_SEL | O_ANA_PLL_A CCINV_EN_TM | O_ANA_PLL_A CCINV_EN_TM_ SEL | O_ANA_PLL_BI AS_EN_TM | O_ANA_PLL_BI AS_EN_TM_SE L |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_ANA_PLLDA EN_DEL_TM | O_ANA_PLLDA EN_DEL_TM_ SEL | O_ANA_PLLDA EN_TM | O_ANA_PLLDA EN_TM_SEL | O_ANA_OP_B Y2_DIV_RESE T_N_TM | O_ANA_OP_B Y2_DIV_RESE T_N_TM_SEL | O_ANA_OP_DI V_RESET_N_T M | O_ANA_OP_DI V_RESET_N_T M_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_IP_DIV RESET_N_TM | O_ANA_IP_DIV RESET_N_TM_ SEL | O_ANA_FB_DI V_RESET_N_T M | O_ANA_FB_DI V_RESET_N_T M_SEL | O_ANA_GM_P WM_DIV_RES ET_N_TM | O_ANA_GM_P WM_DIV_RES ET_N_TM_SEL | O_ANA_BYTE CLK_DIV_RES ET_N_TM | O_ANA_BYTE CLK_DIV_RES ET_N_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-41. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--|------|-------|---|
| 31 | O_ANA_PLL_VRESET_G EN_EN_TM | R/W | 0h | Forced value of pll_vreset_gen_en = 1 |
| 30 | O_ANA_PLL_VRESET_G EN_EN_TM_SEL | R/W | 0h | pll_vreset_gen_en forced from test registers |
| 29 | O_ANA_PLL_PFD_EN_T M | R/W | 0h | Forced value of pllda_pfd_en = 1 |
| 28 | O_ANA_PLL_PFD_EN_T M_SEL | R/W | 0h | pllda_pfd_en forced from test registers |
| 27 | O_ANA_PLL_LOOP_FILT ER_RESET_N_TM | R/W | 0h | Forced value of pll_loop_filter_reset_n = 1 |
| 26 | O_ANA_PLL_LOOP_FILT ER_RESET_N_TM_SEL | R/W | 0h | pll_loop_filter_reset_n is drivne from test registers |

Table 11-41. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT12 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------------|------|-------|--|
| 25 | O_ANA_PLL_GM_RESET_N_TM | R/W | 0h | Forced value of pll_gm_reset_n = 1 |
| 24 | O_ANA_PLL_GM_RESET_N_TM_SEL | R/W | 0h | pll_gm_reset_n is drivne from test registers |
| 23 | O_ANA_PLL_GMBYC_CAP_RESET_N_TM | R/W | 0h | Forced value of pll_gmbyc_cap_reset_n = 1 |
| 22 | O_ANA_PLL_GMBYC_CAP_RESET_N_TM_SEL | R/W | 0h | pll_gmbyc_cap_reset_n is drivne from test registers |
| 21 | O_ANA_PLL_CP_RESET_N_TM | R/W | 0h | Forced value of pll_cp_reset_n = 1 |
| 20 | O_ANA_PLL_CP_RESET_N_TM_SEL | R/W | 0h | pll_cp_reset_n is drivne from test registers |
| 19 | O_ANA_PLL_ACCINV_EN_TM | R/W | 0h | Forced value of pllda_accinv = 1 |
| 18 | O_ANA_PLL_ACCINV_EN_TM_SEL | R/W | 0h | pllda_accinv forced from test registers |
| 17 | O_ANA_PLL_BIAS_EN_TM | R/W | 0h | Forced value of pllda_bias_en = 1 |
| 16 | O_ANA_PLL_BIAS_EN_TM_SEL | R/W | 0h | pllda_bias_en forced from test registers |
| 15 | O_ANA_PL LDA_EN_DEL_TM | R/W | 0h | Forced value of pllda_en_del = 1 |
| 14 | O_ANA_PL LDA_EN_DEL_TM_SEL | R/W | 0h | pllda_en_del forced from test registers |
| 13 | O_ANA_PL LDA_EN_TM | R/W | 0h | Forced value of pllda_en_del = 1 |
| 12 | O_ANA_PL LDA_EN_TM_SEL | R/W | 0h | pllda_en_del forced from test registers |
| 11 | O_ANA_OP_BY2_DIV_RESET_N_TM | R/W | 0h | Forced valu of pllda_op_by2_div_reset_n = 1 |
| 10 | O_ANA_OP_BY2_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_op_by2_div_reset_n forced from test registers |
| 9 | O_ANA_OP_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_op_div_reset_n = 1 |
| 8 | O_ANA_OP_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_op_div_reset_n forced from test registers |
| 7 | O_ANA_IP_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_ip_div_reset_n = 1 |
| 6 | O_ANA_IP_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_ip_div_reset_n forced from test registers |
| 5 | O_ANA_FB_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_fb_div_reset_n = 1 |
| 4 | O_ANA_FB_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_fb_div_reset_n forced from test registers |
| 3 | O_ANA_GM_PWM_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_gm_pwm_div_reset_n = 1 |
| 2 | O_ANA_GM_PWM_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_gm_pwm_div_reset_n forced from test registers |
| 1 | O_ANA_BYTECLK_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_byteclk_div_reset_n = 1 |
| 0 | O_ANA_BYTECLK_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_byteclk_div_reset_n forced from test registers |

11.21 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT13 Register (Offset = 4Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT13 is shown in [Figure 11-20](#) and described in [Table 11-43](#).

Return to [Summary Table](#).

CMN_DIG_TBIT13

Table 11-42.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT13
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 004Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 004Ch |

Figure 11-20. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT13 Register

| | | | | | | | |
|--------------------------|----|-------------------------------------|--------------------------|----|--------------------------------------|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| O_ANA_PLL_FB_DIV_LOW_TM | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_ANA_PLL_FB_DIV_LOW_TM | | O_ANA_PLL_F B_DIV_LOW_T M_SEL | O_ANA_PLL_FB_DIV_HIGH_TM | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_ANA_PLL_FB_DIV_HIGH_TM | | | | | O_ANA_PLL_F B_DIV_HIGH_T M_SEL | UNUSED | |
| R/W-0h | | | | | R/W-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-43. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--|
| 31-22 | O_ANA_PLL_FB_DIV_LO W_TM | R/W | 0h | forced value for pll_fb_div_clk_low |
| 21 | O_ANA_PLL_FB_DIV_LO W_TM_SEL | R/W | 0h | pll_fb_div_clk_low forced from test registers |
| 20-11 | O_ANA_PLL_FB_DIV_HI GH_TM | R/W | 0h | forced value for pll_fb_div_clk_high |
| 10 | O_ANA_PLL_FB_DIV_HI GH_TM_SEL | R/W | 0h | pll_fb_div_clk_high forced from test registers |
| 9-0 | UNUSED | R | 0h | RESERVED |

11.22 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT14 Register (Offset = 50h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT14 is shown in [Figure 11-21](#) and described in [Table 11-45](#).

Return to [Summary Table](#).

CMN_DIG_TBIT14

Table 11-44.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT14
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0050h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0050h |

Figure 11-21. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT14 Register

| | | | | | | | |
|-------------------------|---------------------------------|---------------------|----|---------------------|----|----|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | O_ANA_PLL_OP_DIV_TM | | | |
| R-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_ANA_PLL_O P_DIV_TM | O_ANA_PLL_O P_DIV_TM_SE L | O_ANA_PLL_IP_DIV_TM | | | | | O_ANA_PLL_IP _DIV_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-45. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|-----------------------------------|
| 31-13 | UNUSED | R | 0h | RESERVED |
| 12-7 | O_ANA_PLL_OP_DIV_T M | R/W | 0h | forced value for op_div |
| 6 | O_ANA_PLL_OP_DIV_T M_SEL | R/W | 0h | op_div forced from test registers |
| 5-1 | O_ANA_PLL_IP_DIV_TM | R/W | 0h | forced value for ip_div |
| 0 | O_ANA_PLL_IP_DIV_TM _SEL | R/W | 0h | ip_div forced from test registers |

11.23 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT20 Register (Offset = 68h) [reset = 140h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT20 is shown in [Figure 11-22](#) and described in [Table 11-47](#).

Return to [Summary Table](#).

CMN_DIG_TBIT20

Table 11-46.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT20
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0068h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0068h |

Figure 11-22. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT20 Register

| | | | | | | | |
|---------------------------|----|----|----|---------------------------|----|-------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | O_CMSMT_REF_CLK_TMR_VALUE | | | |
| R-0h | | | | R/W-14h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_CMSMT_REF_CLK_TMR_VALUE | | | | | | | |
| R/W-14h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_CMSMT_REF_CLK_TMR_VALUE | | | | BF_3_1 | | O_CMSMT_MEASUREMENT_RUN | |
| R/W-14h | | | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-47. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|--|
| 31-20 | UNUSED | R | 0h | RESERVED |
| 19-4 | O_CMSMT_REF_CLK_TMR_VALUE | R/W | 14h | Number of refclk cycles required for clock measurement |
| 3-1 | BF_3_1 | R/W | 0h | |
| 0 | O_CMSMT_MEASUREMENT_RUN | R/W | 0h | Enables clock measurement |

11.24 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT21 Register (Offset = 6Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT21 is shown in [Figure 11-23](#) and described in [Table 11-49](#).

Return to [Summary Table](#).

CMN_DIG_TBIT21

Table 11-48.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT21
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 006Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 006Ch |

Figure 11-23. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT21 Register

| | | | | | | | |
|--------|---|--|----------------------------------|--------------------------------------|--------------------------|----------------------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | O_CMNDA_HS RX_BIST_CLK_ SERSYNTH_S WAPDPDN | O_CMNDA_HS RX_BIST_DATA_ SERSYNTH_S WAPDPDN | O_CMNDA_RX BIST_EN_DEL_ TM | O_CMNDA_RX BIST_EN_DEL_ TM_SEL | O_CMNDA_RX BIST_EN_TM | O_CMNDA_RX BIST_EN_TM_ SEL | O_RX_DIG_BIS T_EN |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-49. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--|------|-------|---|
| 31-7 | UNUSED | R | 0h | RESERVED |
| 6 | O_CMNDA_HSRX_BIST_ CLK_SERSYNTH_SWAP DPDN | R/W | 0h | Enables swapping DP-DN lines for clock bist |
| 5 | O_CMNDA_HSRX_BIST_ DATA_SERSYNTH_SWA PDPDN | R/W | 0h | Enables swapping DP-DN lines for data bist |
| 4 | O_CMNDA_RX_BIST_EN_ DEL_TM | R/W | 0h | forced value of cmnda_rx_bist_en_del = 1 |
| 3 | O_CMNDA_RX_BIST_EN_ DEL_TM_SEL | R/W | 0h | cmnda_rx_bist_en_del driven from test registers |
| 2 | O_CMNDA_RX_BIST_EN_ TM | R/W | 0h | forced value of cmnda_rx_bist_en = 1 |
| 1 | O_CMNDA_RX_BIST_EN_ TM_SEL | R/W | 0h | cmnda_rx_bist_en driven from test registers |
| 0 | O_RX_DIG_BIST_EN | R/W | 0h | BIST enable for digital |

11.25 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT22 Register (Offset = 70h) [reset = 694h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT22 is shown in [Figure 11-24](#) and described in [Table 11-51](#).

Return to [Summary Table](#).

BIST_CONFIG_REG1

Table 11-50.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT22
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0070h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0070h |

Figure 11-24. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT22 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------------|----------------------|-----------------------|---------------------------|----|----|--------------------|----|
| TM_SKEW_CAL_SYNC_PKT_SEL | TM_SKEW_CAL_SYNC_PKT | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_SYNC_PKT | TM_HS_SYNC_PKT_SEL | TM_HS_SYNC_PKT | | | | | |
| R/W-0h | R/W-0h | R/W-0h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_HS_SYNC_PKT | | BIST_LENGTH_OF_DESKEW | | | | | |
| R/W-0h | | R/W-Dh | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BIST_LENGTH_OF_DESKEW | BIST_SEND_CONFIG | | BIST_MODE_ENTRY_WAIT_TIME | | | BIST_CONTROLLER_EN | |
| R/W-Dh | R/W-0h | | R/W-Ah | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-51. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31 | TM_SKEW_CAL_SYNC_PKT_SEL | R/W | 0h | To send 'FF as Skew calibration sync packet |
| 30-23 | TM_SKEW_CAL_SYNC_PKT | R/W | 0h | desired skew calibration test sync packet |
| 22 | TM_HS_SYNC_PKT_SEL | R/W | 0h | To send 'B8 as HS sync packet |
| 21-14 | TM_HS_SYNC_PKT | R/W | 0h | desired HS test sync packet |
| 13-7 | BIST_LENGTH_OF_DESKEW | R/W | Dh | Length of deskew sequence In terms of us By default 13us of deskew sequence will be transmitted |
| 6-5 | BIST_SEND_CONFIG | R/W | 0h | Option of configuring what to send in BIST mose To send both deskew and HS data |
| 4-1 | BIST_MODE_ENTRY_WAIT_TIME | R/W | Ah | Once after giving bist_en signal to pattern generator, after these many number of BYTE clcok cycles pattern generation will start |
| 0 | BIST_CONTROLLER_EN | R/W | 0h | Enable BIST controller |

11.26 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT23 Register (Offset = 74h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT23 is shown in [Figure 11-25](#) and described in [Table 11-53](#).

Return to [Summary Table](#).

BIST_CONFIG_REG2

Table 11-52.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT23
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0074h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0074h |

Figure 11-25. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT23 Register

| | | | | | | | |
|-----------------------|---------------------------|-------------------|----|----|----|----|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_TX_DATA_ HS_SEL | TM_TX_DATA_HS | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_TX_DATA_ HS | BIST_TM_BAND_ CTRL_SEL | BIST_TM_BAND_CTRL | | | | | TM_SKEW_CAL_ PATTERN_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_PATTERN | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-53. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|---|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23 | TM_TX_DATA_HS_SEL | R/W | 0h | sends single test byte to sersynth, which is in < 22:15> |
| 22-15 | TM_TX_DATA_HS | R/W | 0h | Desired clock patetrn that can be sent using clk_sersynth |
| 14 | BIST_TM_BAND_CTRL_SEL | R/W | 0h | To take the default band control settigns by the design |
| 13-9 | BIST_TM_BAND_CTRL | R/W | 0h | Test mode band control setting to be done for BIST |
| 8 | TM_SKEW_CAL_PATTER_N_SEL | R/W | 0h | To send 'AA as skew calibration pattern |
| 7-0 | TM_SKEW_CAL_PATTER_N | R/W | 0h | desired skew calibration test sequence |

11.27 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT24 Register (Offset = 78h) [reset = 0F0501B0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT24 is shown in [Figure 11-26](#) and described in [Table 11-55](#).

Return to [Summary Table](#).

BIST_CONFIG_REG3

Table 11-54.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT24
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0078h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0078h |

Figure 11-26. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT24 Register

| | | | | | | | |
|--------------------|--------------|-----------|----|----------------|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BIST_FRM_IDLE_TIME | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BIST_PKT_NUM | | | | | | | |
| R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BIST_INF_MODE | BIST_FRM_NUM | | | | | | |
| R/W-0h | R/W-3h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BIST_FRM_NUM | BIST_CLEAR | BIST_PRBS | | BIST_TEST_MODE | | UNUSED_0 | |
| R/W-3h | R/W-0h | R/W-3h | | R/W-0h | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-55. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-24 | BIST_FRM_IDLE_TIME | R/W | Fh | BIST_FRM_IDLE time is time between the frames |
| 23-16 | BIST_PKT_NUM | R/W | 5h | BIST_PAK_NUM is number of packets that are to be transmitted per frame |
| 15 | BIST_INF_MODE | R/W | 0h | run infinite BIST mode |
| 14-7 | BIST_FRM_NUM | R/W | 3h | BIST_FRM_NUM is number of frames to be transmitted |
| 6 | BIST_CLEAR | R/W | 0h | clear the bist |
| 5-4 | BIST_PRBS | R/W | 3h | BIST PRBS MODE 9 |
| 3-1 | BIST_TEST_MODE | R/W | 0h | PRBS mode |
| 0 | UNUSED_0 | R | 0h | RESERVED |

11.28 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT25 Register (Offset = 7Ch) [reset = 28h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT25 is shown in [Figure 11-27](#) and described in [Table 11-57](#).

Return to [Summary Table](#).

BIST_CONFIG_REG4

Table 11-56.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT25
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 007Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 007Ch |

Figure 11-27. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|-----------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | BIST_RUN_LENGTH | | | | | | | | | | | |
| R-0h | | | | R/W-28h | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-57. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|-----------------|
| 31-12 | UNUSED | R | 0h | RESERVED |
| 11-0 | BIST_RUN_LENGTH | R/W | 28h | BIST_RUN_LENGTH |

11.29 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT26 Register (Offset = 80h) [reset = Ah]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT26 is shown in [Figure 11-28](#) and described in [Table 11-59](#).

Return to [Summary Table](#).

BIST_CONFIG_REG5

Table 11-58.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT26
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0080h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0080h |

Figure 11-28. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED_31_8 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED_31_8 | | | | | | | | BIST_IDLE_TIME | | | | | | | |
| R-0h | | | | | | | | R/W-Ah | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-59. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|----------------|
| 31-8 | UNUSED_31_8 | R | 0h | RESERVED |
| 7-0 | BIST_IDLE_TIME | R/W | Ah | BIST_IDLE_TIME |

11.30 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT27 Register (Offset = 84h) [reset = DECDBCABh]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT27 is shown in [Figure 11-29](#) and described in [Table 11-61](#).

Return to [Summary Table](#).

BIST_CONFIG_REG6

Table 11-60.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT27
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0084h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0084h |

Figure 11-29. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT27 Register

| | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|-----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BIST_PKT4 | | | | | | | | BIST_PKT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BIST_PKT2 | | | | | | | | BIST_PKT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-61. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|----------------|
| 31-24 | BIST_PKT4 | R/W | DEh | BIST_TEST_PAT4 |
| 23-16 | BIST_PKT3 | R/W | CDh | BIST_TEST_PAT3 |
| 15-8 | BIST_PKT2 | R/W | BCh | BIST_TEST_PAT2 |
| 7-0 | BIST_PKT1 | R/W | ABh | BIST_TEST_PAT1 |

11.31 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28 Register (Offset = 88h) [reset = 28h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28 is shown in [Figure 11-30](#) and described in [Table 11-63](#).

Return to [Summary Table](#).

BIST_CONFIG_REG7

Table 11-62.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0088h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0088h |

Figure 11-30. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28 Register

| | | | | | | | |
|---------------------------------|---------------------------------|---------------------------------|---------------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BIST_TM_CLO CK_LP_DP_SE L | BIST_TM_CLO CK_LP_DP_VA L | BIST_TM_CLO CK_LP_DN_SE L | BIST_TM_CLO CK_LP_DN_VA L | BIST_TM_DAT A_LP_DP_SEL | BIST_TM_DAT A_LP_DP_VAL | BIST_TM_DAT A_LP_DN_SEL | BIST_TM_DAT A_LP_DN_VAL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED_INT | | BIST_LFSR_FR EEZE | BIST_ERR_INJ_POINT | | | | |
| R-0h | | R/W-0h | R/W-14h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BIST_ERR_INJ_POINT | | | | | | | BIST_ERR_INJ _EN |
| R/W-14h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-63. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23 | BIST_TM_CLOCK_LP_D P_SEL | R/W | 0h | Test mode selection bit to force clcok LP DP buffer to value from design |
| 22 | BIST_TM_CLOCK_LP_D P_VAL | R/W | 0h | Test mode clock LP DP buffer value is 0 |
| 21 | BIST_TM_CLOCK_LP_D N_SEL | R/W | 0h | Test mode selection bit to force clcok LP DN buffer to value from design |
| 20 | BIST_TM_CLOCK_LP_D N_VAL | R/W | 0h | Test mode clock LP DN buffer value is 0 |
| 19 | BIST_TM_DATA_LP_DP_ SEL | R/W | 0h | Test mode selection bit to force data LP DP buffer to value from design |
| 18 | BIST_TM_DATA_LP_DP_ VAL | R/W | 0h | Test mode data LP DP buffer value is 0 |
| 17 | BIST_TM_DATA_LP_DN_ SEL | R/W | 0h | Test mode selection bit to force data LP DN buffer to value from design |

Table 11-63. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT28 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 16 | BIST_TM_DATA_LP_DN_VAL | R/W | 0h | Test mode data LP DN buffer value is 0 |
| 15-14 | UNUSED_INT | R | 0h | RESERVED |
| 13 | BIST_LFSR_FREEZE | R/W | 0h | Reset LFSR contents after every packet or frame |
| 12-1 | BIST_ERR_INJ_POINT | R/W | 14h | BIST_ERR_INJECT_POINT is where to inject the error in the packet |
| 0 | BIST_ERR_INJ_EN | R/W | 0h | Inject error in the BIST during the packet |

11.32 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT31 Register (Offset = 94h) [reset = 00040400h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT31 is shown in [Figure 11-31](#) and described in [Table 11-65](#).

Return to [Summary Table](#).

CMN_DIG_TBIT31

Table 11-64.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT31
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0094h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0094h |

Figure 11-31. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | |
|-------------------------|----|----|----|----|----|----|----|-------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | O_RX_SSM_LDO_EN_REF_TMR | | | | | | | |
| R-0h | | | | | | | | R/W-4h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RX_SSM_LDO_EN_DEL_TMR | | | | | | | | O_RX_SSM_LDO_EN_TMR | | | | | | | |
| R/W-4h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-65. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-16 | O_RX_SSM_LDO_EN_REF_TMR | R/W | 4h | Wait time before enabling oscialltor calibration |
| 15-8 | O_RX_SSM_LDO_EN_DEL_TMR | R/W | 4h | wait time before enabling ldo_en_ref |
| 7-0 | O_RX_SSM_LDO_EN_TMR | R/W | 0h | Wait time between ldo_en and ldo_en_del |

11.33 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT32 Register (Offset = 98h) [reset = 201h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT32 is shown in [Figure 11-32](#) and described in [Table 11-67](#).

Return to [Summary Table](#).

CMN_DIG_TBIT32

Table 11-66.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT32
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0098h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0098h |

Figure 11-32. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT32 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_RX_SSM_ANA_BIST_ISO_DIS_TMR | | | | | | | |
| R/W-2h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RX_SSM_ANA_BIST_EN_DEL_TMR | | | | | | | |
| R/W-1h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-67. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-16 | UNUSED | R | 0h | RESERVED |
| 15-8 | O_RX_SSM_ANA_BIST_I SO_DIS_TMR | R/W | 2h | Wait time between Bist_en_del and disabling isolation |
| 7-0 | O_RX_SSM_ANA_BIST_ EN_DEL_TMR | R/W | 1h | Wait time between Bist_en and bist_en_Del |

11.34 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT33 Register (Offset = 9Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT33 is shown in [Figure 11-33](#) and described in [Table 11-69](#).

Return to [Summary Table](#).

CMN_DIG_TBIT33

Table 11-68.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT33
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 009Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 009Ch |

Figure 11-33. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT33 Register

| | | | | | | | |
|-------------------------------------|----|---|---------------------------------|----|----|---|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| O_RX_OSC_CAL_TIMER_SCALE_SEL | | | UNUSED | | | O_RX_REFCLK_TIMER_ITER_V ALUE_TM | |
| R/W-0h | | | R-0h | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_RX_REFCLK_TIMER_ITER_VALUE_TM | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_RX_REFCLK_TIMER_ITER_V ALUE_TM | | O_RX_REFCLK TIMER_ITER VALUE_TM_SE L | O_RX_REFCLK_TIMER_INIT_VALUE_TM | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RX_REFCLK_TIMER_INIT_VALUE_TM | | | | | | O_RX_REFCLK TIMER_INIT VALUE_TM_SE L | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-69. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-29 | O_RX_OSC_CAL_TIMER_SCALE_SEL | R/W | 0h | Timer scale value for vco_count_window |
| 28-26 | UNUSED | R | 0h | RESERVED |
| 25-14 | O_RX_REFCLK_TIMER_I TER_VALUE_TM | R/W | 0h | Wait time required before enabling vco count window during iteration in test mode |
| 13 | O_RX_REFCLK_TIMER_I TER_VALUE_TM_SEL | R/W | 0h | refclk_timer_iter value driven from test register |
| 12-1 | O_RX_REFCLK_TIMER_I NIT_VALUE_TM | R/W | 0h | Wait time required before enabling vco count window in initial phase in test mode |
| 0 | O_RX_REFCLK_TIMER_I NIT_VALUE_TM_SEL | R/W | 0h | refclk_timer_init value driven from test register |

11.35 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT34 Register (Offset = A0h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT34 is shown in [Figure 11-34](#) and described in [Table 11-71](#).

Return to [Summary Table](#).

CMN_DIG_TBIT34

Table 11-70.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT34
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00A0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00A0h |

Figure 11-34. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT34 Register

| | | | | | | | |
|----------------------------------|----|--|----------------------------------|----|----|--|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | O_RX_OSC_EN_DEL_TMR_VAL UE_TM | |
| R-0h | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| O_RX_OSC_EN_DEL_TMR_VALUE_TM | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_RX_OSC_EN_DEL_TMR_VAL UE_TM | | O_RX_OSC_E N_DEL_TMR_V ALUE_TM_SEL | O_RX_REFCLK_TIMER_START_VALUE_TM | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RX_REFCLK_TIMER_START_VALUE_TM | | | | | | O_RX_REFCLK TIMER STAR T_VALUE_TM SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-71. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-26 | UNUSED | R | 0h | RESERVED |
| 25-14 | O_RX_OSC_EN_DEL_TM R_VALUE_TM | R/W | 0h | Wait time between osc_en and osc_en_del in Test mode |
| 13 | O_RX_OSC_EN_DEL_TM R_VALUE_TM_SEL | R/W | 0h | osc_en_del_tmr driven from test register |
| 12-1 | O_RX_REFCLK_TIMER_ START_VALUE_TM | R/W | 0h | No of refclk cycles required for single vco count window in test mode |
| 0 | O_RX_REFCLK_TIMER_ START_VALUE_TM_SEL | R/W | 0h | refclk_timer_start_value driven from test mode |

11.36 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT35 Register (Offset = A4h) [reset = 001380BBh]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT35 is shown in [Figure 11-35](#) and described in [Table 11-73](#).

Return to [Summary Table](#).

CMN_DIG_TBIT35

Table 11-72.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT35
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00A4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00A4h |

Figure 11-35. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | |
|---------------------------------|----|----|----|---------------------------------|----|----|----|---------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | O_RX_PLLCNT_COUNT_START_VALUE_2 | | | | | | | |
| R-0h | | | | | | | | R/W-138h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RX_PLLCNT_COUNT_START_VALUE_2 | | | | O_RX_PLLCNT_COUNT_START_VALUE_1 | | | | | | | | | | | |
| R/W-138h | | | | | | | | R/W-BBh | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-73. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-12 | O_RX_PLLCNT_COUNT_START_VALUE_2 | R/W | 138h | No of PLL clock cycles expected in 25G mode |
| 11-0 | O_RX_PLLCNT_COUNT_START_VALUE_1 | R/W | BBh | No of PLL clock cycles expected in 15G mode |

11.37 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT36 Register (Offset = A8h) [reset = EE8h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT36 is shown in [Figure 11-36](#) and described in [Table 11-75](#).

Return to [Summary Table](#).

CMN_DIG_TBIT36

Table 11-74.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT36
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00A8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00A8h |

Figure 11-36. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT36 Register

| | | | | | | | |
|---------------------------|----|----|---------------------------------|---------------------------|---------------------------|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | O_RX_TM_VCOCAL_OVRD_VALUE | | | |
| R-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| O_RX_TM_VCOCAL_OVRD_VALUE | | | O_RX_TM_VC O_CAL_OVERRIDE_EN | O_RX_OSC_CAL_CODE_START | | | |
| R/W-0h | | | R/W-0h | R/W-77h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_RX_OSC_CAL_CODE_START | | | O_RX_OSC_CAL_CODE_INIT_STEP | | O_RX_TM_SEL _1P5G_MODE | O_RX_TM_OSC_CAL_EN | |
| R/W-77h | | | R/W-2h | | R/W-0h | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-75. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-20 | UNUSED | R | 0h | RESERVED |
| 19-13 | O_RX_TM_VCOCAL_OVRD_VALUE | R/W | 0h | Vco calcode Test mode value |
| 12 | O_RX_TM_VCO_CAL_OVERRIDE_EN | R/W | 0h | Enables test mode overwrite for vco cal code |
| 11-5 | O_RX_OSC_CAL_CODE_START | R/W | 77h | Starting code for vco calibration |
| 4-2 | O_RX_OSC_CAL_CODE_INIT_STEP | R/W | 2h | Step size for incrementing vco cal code |
| 1 | O_RX_TM_SEL_1P5G_MODE | R/W | 0h | Select 1p5g mode oscillator clock |
| 0 | O_RX_TM_OSC_CAL_EN | R/W | 0h | Test mode overwrite for crude osc calibration enable |

11.38 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37 Register (Offset = ACh) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37 is shown in [Figure 11-37](#) and described in [Table 11-77](#).

Return to [Summary Table](#).

Table 11-76.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 00ACh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 00ACh |

Figure 11-37. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37 Register

| | | | | | | | |
|--------------------------|--------------------------------|------------------------------------|-------------------------------|-----------------------------------|------------------------------|------------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | O_CMNDA_HS_RX_OSC_CALIB_SEL_TM | O_CMNDA_HS_RX_OSC_CALIB_SEL_TM_SEL | O_CMNDA_RX_OSC_DIV_RESET_N_TM | O_CMNDA_RX_OSC_DIV_RESET_N_TM_SEL | O_CMNDA_RX_OSC_EN_DEL_TM | O_CMNDA_RX_OSC_EN_DEL_TM_SEL | O_CMNDA_RX_OSC_EN_TM |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_CMNDA_RX_OSC_EN_TM_SEL | O_CMNDA_RX_LDO_BYPASS_TM | O_CMNDA_RX_LDO_REF_EN_TM | O_CMNDA_RX_LDO_REF_EN_TM_SEL | O_CMNDA_RX_LDO_EN_DEL_TM | O_CMNDA_RX_LDO_EN_DEL_TM_SEL | O_CMNDA_RX_LDO_EN_TM | O_CMNDA_RX_LDO_EN_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-77. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-15 | UNUSED | R | 0h | RESERVED |
| 14 | O_CMNDA_HSRX_OSC_CALIB_SEL_TM | R/W | 0h | forced value of hsrx_osc_calib_sel = 1 |
| 13 | O_CMNDA_HSRX_OSC_CALIB_SEL_TM_SEL | R/W | 0h | hsrx_osc_calib_sel driven from test registers |
| 12 | O_CMNDA_RX_OSC_DIV_RESET_N_TM | R/W | 0h | forced value of rx_osc_div_reset_n = 1 |
| 11 | O_CMNDA_RX_OSC_DIV_RESET_N_TM_SEL | R/W | 0h | rx_osc_div_reset_n driven from test registers |
| 10 | O_CMNDA_RX_OSC_EN_DEL_TM | R/W | 0h | forced value of rx_osc_en_del = 1 |
| 9 | O_CMNDA_RX_OSC_EN_DEL_TM_SEL | R/W | 0h | rx_osc_en_del driven from test registers |
| 8 | O_CMNDA_RX_OSC_EN_TM | R/W | 0h | forced value of rx_osc_en = 1 |
| 7 | O_CMNDA_RX_OSC_EN_TM_SEL | R/W | 0h | rx_osc_en driven from test registers |

Table 11-77. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT37 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|--|
| 6 | O_CMNDA_RX_LDO_BY_PASS_TM | R/W | 0h | Bypass LDO in test mode |
| 5 | O_CMNDA_RX_LDO_REF_EN_TM | R/W | 0h | forced value of rx_ldo_ref_en = 1 |
| 4 | O_CMNDA_RX_LDO_REF_EN_TM_SEL | R/W | 0h | rx_ldo_ref_en driven from test registers |
| 3 | O_CMNDA_RX_LDO_EN_DEL_TM | R/W | 0h | forced value of rx_ldo_en_del = 1 |
| 2 | O_CMNDA_RX_LDO_EN_DEL_TM_SEL | R/W | 0h | rx_ldo_en_del driven from test registers |
| 1 | O_CMNDA_RX_LDO_EN_TM | R/W | 0h | forced value of rx_ldo_en = 1 |
| 0 | O_CMNDA_RX_LDO_EN_TM_SEL | R/W | 0h | rx_ldo_en driven from test registers |

11.39 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT38 Register (Offset = B0h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT38 is shown in [Figure 11-38](#) and described in [Table 11-79](#).

Return to [Summary Table](#).

CMN_DIG_TBIT38

Table 11-78.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT38
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00B0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00B0h |

Figure 11-38. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT38 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-79. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT38 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31-0 | UNUSED | R | 0h | RESERVED |

11.40 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT39 Register (Offset = B4h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT39 is shown in [Figure 11-39](#) and described in [Table 11-81](#).

Return to [Summary Table](#).

CMN_DIG_TBIT39

Table 11-80.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT39
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00B4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00B4h |

Figure 11-39. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT39 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPARE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-81. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-------------|
| 31-0 | SPARE | R/W | 0h | spare |

11.41 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT50 Register (Offset = D8h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT50 is shown in [Figure 11-40](#) and described in [Table 11-83](#).

Return to [Summary Table](#).

BIST_STATUS_REG1

Table 11-82.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT50
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00D8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00D8h |

Figure 11-40. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT50 Register

| | | | | | | | |
|--------|----|----|----|----|----|-------------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | BIST_COMPLE TE | BIST_EN_ACK |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-83. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT50 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|----------------------------|
| 31-2 | UNUSED | R | 0h | RESERVED |
| 1 | BIST_COMPLETE | R | 0h | BIST is completed |
| 0 | BIST_EN_ACK | R | 0h | BIST Controller is enabled |

11.42 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT53 Register (Offset = E4h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT53 is shown in [Figure 11-41](#) and described in [Table 11-85](#).

Return to [Summary Table](#).

CMN_DIG_TBIT53

Table 11-84.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT53
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00E4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00E4h |

Figure 11-41. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT53 Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|----------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | I_CMSMT_TEST_CLK_CNT_VALUE | |
| R-0h | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| I_CMSMT_TEST_CLK_CNT_VALUE | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I_CMSMT_TEST_CLK_CNT_VALUE | | | | | | I_CMSMT_MEASUREMENT_DONE | |
| R-0h | | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-85. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT53 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-17 | UNUSED | R | 0h | RESERVED |
| 16-1 | I_CMSMT_TEST_CLK_CNT_VALUE | R | 0h | Gives clocks cycles count for test clock during measurement |
| 0 | I_CMSMT_MEASUREMENT_DONE | R | 0h | Indicates clock measurement is done |

11.43 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT54 Register (Offset = E8h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT54 is shown in [Figure 11-42](#) and described in [Table 11-87](#).

Return to [Summary Table](#).

CMN_DIG_TBIT54

Table 11-86.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT54
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00E8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00E8h |

Figure 11-42. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT54 Register

| | | | | | | | |
|---------------------|----|----|--------------|------------------|--------------|--------------------|----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| I_CMN_PLL_SSM_STATE | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| I_CMN_PLL_SSM_STATE | | | | UNUSED | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | I_DIG_PG_ACK | I_PLL_NOT_LOCKED | I_PLL_LOCKED | I_ANA_RES_COMP_OUT | I_CMN_TX_READY |
| R-0h | | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-87. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT54 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-20 | I_CMN_PLL_SSM_STATE | R | 0h | Gives CMN PLL ssm state |
| 19-5 | UNUSED | R | 0h | RESERVED |
| 4 | I_DIG_PG_ACK | R | 0h | PSM power good acknowledgement |
| 3 | I_PLL_NOT_LOCKED | R | 0h | Indicates PLL is not locked before timeout |
| 2 | I_PLL_LOCKED | R | 0h | Indicates PLL is locked |
| 1 | I_ANA_RES_COMP_OUT | R | 0h | read value of comaprator output |
| 0 | I_CMN_TX_READY | R | 0h | Indiacates cmn is ready for TX IP |

11.44 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT56 Register (Offset = F0h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT56 is shown in [Figure 11-43](#) and described in [Table 11-89](#).

Return to [Summary Table](#).

CMN_DIG_TBIT56

Table 11-88.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT56
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00F0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00F0h |

Figure 11-43. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT56 Register

| | | | | | | | |
|------------------------|----|----|----|------------------------|------------------------|------------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | I_CMNDA_RX_OSC_CALCODE | | | |
| R-0h | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| I_CMNDA_RX_OSC_CALCODE | | | | I_CMN_RX_SSM_STATE | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| I_CMN_RX_SSM_STATE | | | | | I_RX_OSC_CAL_FSM_STATE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I_RX_OSC_CAL_FSM_STATE | | | | | | I_ANA_RES_C OMP_OUT | I_CMN_RX_RE ADY |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-89. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT56 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-28 | UNUSED | R | 0h | RESERVED |
| 27-21 | I_CMNDA_RX_OSC_CAL CODE | R | 0h | Reads out calib code applied to oscillator |
| 20-11 | I_CMN_RX_SSM_STATE | R | 0h | Gives CMN Rx ssm state |
| 10-2 | I_RX_OSC_CAL_FSM_S TATE | R | 0h | Gives Rx osc calib FSM state |
| 1 | I_ANA_RES_COMP_OUT | R | 0h | read value of comaprator output |
| 0 | I_CMN_RX_READY | R | 0h | Indicates cmn is ready for RX IP |

11.45 DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT58 Register (Offset = F8h) [reset = 0h]

DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT58 is shown in [Figure 11-44](#) and described in [Table 11-91](#).

Return to [Summary Table](#).

CMN_DIG_TBIT58

Table 11-90.
DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT58
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 00F8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 00F8h |

Figure 11-44. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT58 Register

| | | | | | | | |
|--------|----|------------------|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | I_RES_CALIB_CODE | | | | | I_RES_CALIB_DONE |
| R-0h | | R-0h | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-91. DPHY_RX_VBUS2APB_CMN0_CMN_DIG_TBIT58 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-6 | UNUSED | R | 0h | RESERVED |
| 5-1 | I_RES_CALIB_CODE | R | 0h | Gives out calibrated resistor calibration code |
| 0 | I_RES_CALIB_DONE | R | 0h | Indicates resistor calibration is done |

11.46 DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT0 Register (Offset = 100h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT0 is shown in [Figure 11-45](#) and described in [Table 11-93](#).

Return to [Summary Table](#).

Analog Test Bit Reg0

Table 11-92.
DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0100h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0100h |

Figure 11-45. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-93. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT0 | R/W | 0h | Analog Test Register 0 |

11.47 DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT1 Register (Offset = 104h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT1 is shown in [Figure 11-46](#) and described in [Table 11-95](#).

Return to [Summary Table](#).

Analog Test Bit Reg1

Table 11-94.
DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0104h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0104h |

Figure 11-46. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-95. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT1 | R/W | 0h | Analog Test Register 1 |

11.48 DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT2 Register (Offset = 108h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT2 is shown in [Figure 11-47](#) and described in [Table 11-97](#).

Return to [Summary Table](#).

Analog Test Bit Reg2

Table 11-96.
DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0108h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0108h |

Figure 11-47. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-97. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|-------------|
| 31-0 | ANA_TBIT2 | R | 0h | RESERVED |

11.49 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT0 Register (Offset = 10Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT0 is shown in [Figure 11-48](#) and described in [Table 11-99](#).

[Return to Summary Table.](#)

Digital Test Bit Reg0

Table 11-98.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 010Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 010Ch |

Figure 11-48. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT0 Register

| | | | | | | | |
|--------|----|----|---------|--------|------------------------|--------------------|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | TD_RSTN | TD_EN | TM_ULPS_ACTIVE_NOT_SEL | TM_ULPS_ACTIVE_NOT | FORCE_RX_HS_MODE |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-99. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|---|
| 31-5 | UNUSED | R | 0h | RESERVED |
| 4 | TD_RSTN | R/W | 0h | TD is reset - Active low reset control to "transition_detector_logic" |
| 3 | TD_EN | R/W | 0h | TD is ENABLED - Active high control to enable "transition_detector_logic" |
| 2 | TM_ULPS_ACTIVE_NOT_SEL | R/W | 0h | Power suspend request in ULPS mode through a test register bypassed with a test value via bit-1 here |
| 1 | TM_ULPS_ACTIVE_NOT | R/W | 0h | When want to control the ULPS mode power suspend request by test register, what should be the value - 0 - "1" |
| 0 | FORCE_RX_HS_MODE | R/W | 0h | Set this bit to force the CRX into HS mode |

11.50 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT1 Register (Offset = 110h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT1 is shown in [Figure 11-49](#) and described in [Table 11-101](#).

Return to [Summary Table](#).

Digital Extra Test Bit Reg0

Table 11-100.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0110h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0110h |

Figure 11-49. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-101. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------------------------|
| 31-0 | DIG_EXTRA_TBIT0 | R/W | 0h | Digital Extra Test Register 0 |

11.51 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2 Register (Offset = 114h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2 is shown in [Figure 11-50](#) and described in [Table 11-103](#).

Return to [Summary Table](#).

Test Mux Register

Table 11-102.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0114h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0114h |

Figure 11-50. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------------|--------------------------------|--------------------------|----------------------|--------------------------------|---------------------|---------------------------------|-------------------------|
| UNUSED | | | | | | | RXDA_LPRX_B IST_EN |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RXDA_ASYNC CLK_EN_SEL | RXDA_ASYNC CLK_EN | RXDA_HSRX BIST_EN_SEL | RXDA_HSRX BIST_EN | RXDA_FREQ BAND_SEL1_S EL | RXDA_FREQ_BAND_SEL1 | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RXDA_FREQ BAND_SEL1 | RXDA_FREQ BAND_SEL2_S EL | RXDA_FREQ_BAND_SEL2 | | | | RXDA_HS_STA RT_PULSE_SE L | RXDA_HS_STA RT_PULSE |
| R/W-0h | R/W-0h | R/W-0h | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RXDA_HS_STB Y_EN_SEL | RXDA_HS_STB Y_EN | RXDA_LPRXC D_EN_SEL | RXDA_LPRXC D_EN | RXDA_RX_TE RM_EN_SEL | RXDA_RX_TE RM_EN | RXDA_ULPS_E N_SEL | RXDA_ULPS_E N |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-103. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | RXDA_LPRX_BIST_EN | R/W | 0h | LP BIST ENABLED |
| 23 | RXDA_ASYNC_CLK_EN_SEL | R/W | 0h | rxda_async_clk_en_sel - Controls the selection on clock "Gate-en" for allowing HS-DDR clock onto Analog Interface with options being the functional mode or from Register-bit |
| 22 | RXDA_ASYNC_CLK_EN | R/W | 0h | rxda_async_clk_en - "Gate_en" value to be considered when chosen to take the value through software way when [23] here is set |
| 21 | RXDA_HSRX_BIST_EN_SEL | R/W | 0h | rxda_hsrx_bist_en_sel - Select signal to choose between functional "bist_en" from top-level [or] from software register |
| 20 | RXDA_HSRX_BIST_EN | R/W | 0h | rxda_hsrx_bist_en - value to be considered when chosen to take the value through software way |

Table 11-103. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 19 | RXDA_FREQ_BAND_SEL1_SEL | R/W | 0h | rxda_freq_band_sel1_sel - Select signal to choose between functional "freq_band" from top-level [or] from software register |
| 18-15 | RXDA_FREQ_BAND_SEL1 | R/W | 0h | rxda_freq_band_sel1 - "freq_band" value considered when selected to have it via software way |
| 14 | RXDA_FREQ_BAND_SEL2_SEL | R/W | 0h | rxda_freq_band_sel2_sel - Select signal to choose between functional "freq_band" from top-level [or] from software register |
| 13-10 | RXDA_FREQ_BAND_SEL2 | R/W | 0h | rxda_freq_band_sel2 - "freq_band" value considered when selected to have it via software way |
| 9 | RXDA_HS_START_PULSE_SEL | R/W | 0h | rxda_hs_start_pulse_sel - Select signal to choose between functional "start_pulse" [or] from software register |
| 8 | RXDA_HS_START_PULSE | R/W | 0h | rxda_hs_start_pulse - "start_pulse" value considered when selected to have it via software way |
| 7 | RXDA_HS_STBY_EN_SEL | R/W | 0h | rxda_hs_stby_en_sel - Select signal to choose between functional "stby_en" [or] from software register |
| 6 | RXDA_HS_STBY_EN | R/W | 0h | rxda_hs_stby_en - "stby_en" value considered when selected to have it via software way |
| 5 | RXDA_LPRXCD_EN_SEL | R/W | 0h | rxda_lprxcd_en_sel - Select signal to choose between functional "lprxcd_en" [or] from software register |
| 4 | RXDA_LPRXCD_EN | R/W | 0h | rxda_lprxcd_en - "lprxcd_en" value considered when selected to have it via software way |
| 3 | RXDA_RX_TERM_EN_SEL | R/W | 0h | rxda_rx_term_en_sel - Select signal to choose between functional "term_en" [or] from software register |
| 2 | RXDA_RX_TERM_EN | R/W | 0h | rxda_rx_term_en - "term_en" value considered when selected to have it via software way |
| 1 | RXDA_ULPS_EN_SEL | R/W | 0h | rxda_ulps_en_sel - Select signal to choose between functional "ulps_en" [or] from software register |
| 0 | RXDA_ULPS_EN | R/W | 0h | rxda_ulps_en - "ulps_en" value considered when selected to have it via software way |

11.52 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT3 Register (Offset = 118h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT3 is shown in [Figure 11-51](#) and described in [Table 11-105](#).

Return to [Summary Table](#).

Digital Extra Test Bit Reg1

Table 11-104.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0118h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0118h |

Figure 11-51. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-105. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_TBIT1 | R | 0h | RESERVED |

11.53 DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT3 Register (Offset = 11Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT3 is shown in [Figure 11-52](#) and described in [Table 11-107](#).

Return to [Summary Table](#).

Analog Read Test Bit Reg3

Table 11-106.
DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 011Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 011Ch |

Figure 11-52. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_READ_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-107. DPHY_RX_VBUS2APB_CLK0_RX_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | ANA_READ_TBIT3 | R | 0h | Analog read register 3 |

11.54 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT4 Register (Offset = 120h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT4 is shown in [Figure 11-53](#) and described in [Table 11-109](#).

Return to [Summary Table](#).

Digital Read Test Reg0

Table 11-108.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT4
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0120h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0120h |

Figure 11-53. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT4 Register

| | | | | | | | | | | | | | | | |
|--------|----|-----------|----|----|----|----|----|-----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | LP_STATUS | | | | | | TD_STATUS | | | | | | | |
| R-0h | | R-0h | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-109. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|--|
| 31-14 | UNUSED | R | 0h | RESERVED |
| 13-8 | LP_STATUS | R | 0h | Status of DP,DN pins of LPRX, LPCD, ULPRX respectively |
| 7-0 | TD_STATUS | R | 0h | Posedge and Negedge transition detect status of LPRX_DP, LPRX_DN, LPCD_DP, LPCD_DN |

11.55 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT5 Register (Offset = 124h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT5 is shown in [Figure 11-54](#) and described in [Table 11-111](#).

Return to [Summary Table](#).

Digital Read Test Bit Reg0

Table 11-110.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0124h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0124h |

Figure 11-54. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_READ_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-111. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_READ_EXTRA_TBIT0 | R | 0h | RESERVED |

11.56 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT6 Register (Offset = 128h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT6 is shown in [Figure 11-55](#) and described in [Table 11-113](#).

Return to [Summary Table](#).

BIST Status Reg0

Table 11-112.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0128h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0128h |

Figure 11-55. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-113. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31-0 | UNUSED | R | 0h | RESERVED |

11.57 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT7 Register (Offset = 12Ch) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT7 is shown in [Figure 11-56](#) and described in [Table 11-115](#).

Return to [Summary Table](#).

Bist Extra Status Read Reg0

Table 11-114.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 012Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 012Ch |

Figure 11-56. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_BIST_READ_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-115. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31-0 | DIG_BIST_READ_EXTRA_TBIT0 | R | 0h | RESERVED |

11.58 DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT8 Register (Offset = 130h) [reset = 0h]

DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT8 is shown in [Figure 11-57](#) and described in [Table 11-117](#).

Return to [Summary Table](#).

Digital Extra Read Reg0

Table 11-116.
DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0130h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0130h |

Figure 11-57. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-117. DPHY_RX_VBUS2APB_CLK0_RX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DIG_READ_TBIT1 | R | 0h | RESERVED |

11.59 DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT0 Register (Offset = 200h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT0 is shown in [Figure 11-58](#) and described in [Table 11-119](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-118.
DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0200h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0200h |

Figure 11-58. DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-119. DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

11.60 DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT1 Register (Offset = 204h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT1 is shown in [Figure 11-59](#) and described in [Table 11-121](#).

Return to [Summary Table](#).

ANA_EXTRA_TBIT0

Table 11-120.
DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0204h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0204h |

Figure 11-59. DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-121. DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | ANA_EXTRA_TBIT0 | R | 0h | RESERVED |

11.61 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0 Register (Offset = 208h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0 is shown in [Figure 11-60](#) and described in [Table 11-123](#).

Return to [Summary Table](#).

DIG_TBIT0

Table 11-122.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0208h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0208h |

Figure 11-60. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0 Register

| | | | | | | | |
|--------------------------|---------------------------|--------------------------|-------------------------------------|-------------------|------------|--------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_1P5TO2P5 G_MODE_SEL | TM_1P5TO2P5 G_MODE_EN | TM_STD_BY | TM_STD_BY_S EL | TM_TERM_EN | TM_TERM_EN _SEL | TM_SETTLE_C OUNT_SEL |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SETTLE_COUNT | | | | | | | SETTLE_COU NT_OFFSET_C ORR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SETTLE_COUNT_OFFSET_CORR | | | TM_DISABLE_ BCLK_PHASE_ ALIGN | UNUSED_3_0 | | | |
| R/W-0h | | | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-123. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_1P5TO2P5G_MODE_ SEL | R/W | 0h | w_tm_1p5to2p5g_mode_sel - Select signal to choose "mode_en" based on top-level "bandctrl" input provided [or] from software register |
| 21 | TM_1P5TO2P5G_MODE_ EN | R/W | 0h | w_tm_1p5to2p5g_mode_en - "mode_en" value considered when selected to have it via software way |
| 20 | TM_STD_BY | R/W | 0h | w_tm_std_by - "tm_std_by" value to be considered when selected to have it via software way Part of control logic to initiate movement of "calib_ctrl" FSM |
| 19 | TM_STD_BY_SEL | R/W | 0h | w_tm_std_by_sel - Select signal to choose between functional "tm_std_by" [or] from software register |
| 18 | TM_TERM_EN | R/W | 0h | w_tm_term_en - "tm_term_en" value to be considered when selected to have it via software way Value provided here converges onto "rxda_rx_term_en" pin on alalog interface |

Table 11-123. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|--|
| 17 | TM_TERM_EN_SEL | R/W | 0h | w_tm_term_en_sel - Select signal to choose between functional "term_en_sel" [or] from software register |
| 16 | TM_SETTLE_COUNT_SE L | R/W | 0h | Test mode settle count selection = 0 - Select signal to choose between functional "settle_count" [or] from software register Value obtained in functional mode depends on the "BandCtl" and "Settle_count_offset" [ie, bits [8:5] here] |
| 15-9 | TM_SETTLE_COUNT | R/W | 0h | Test mode settle count, if bit <16> is set - "settle_count" value to be considered when selected to have it via software way |
| 8-5 | SETTLE_COUNT_OFFSE T_CORR | R/W | 0h | Settle count offset correction value that adds up to the internal predefined settle count based on "BandCtl" which helps in deciding the final "settle_count" to be observed for |
| 4 | TM_DISABLE_BCLK_PH ASE_ALIGN | R/W | 0h | test mode to disable byte clock phase alignment 0-enable 1-disable |
| 3-0 | UNUSED_3_0 | R | 0h | RESERVED |

11.62 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT1 Register (Offset = 20Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT1 is shown in [Figure 11-61](#) and described in [Table 11-125](#).

Return to [Summary Table](#).

DIG_TBIT1

Table 11-124.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 020Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 020Ch |

Figure 11-61. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT1 Register

| | | | | | | | |
|---------------|-----------|---------------|----|----|----|----------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_ULP_RCV_SEL | TM_ULP_RCV |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_LPRXCD_SEL | TM_LPRXCD | TM_UNUSED_5_1 | | | | | TM_FORCE_TX_STOP_STATE |
| R/W-0h | R/W-0h | R-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-125. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_ULP_RCV_SEL | R/W | 0h | w_tm_ulp_rcv_sel - Select signal to choose between functional "ulp_rcv_en" or a value from software register The effective value converges onto port "i_ana_ulps_rcv_en" of "lane_always_on" block at DPHY_RX_VBUS2APB_LANE-level |
| 8 | TM_ULP_RCV | R/W | 0h | w_tm_ulp_rcv_en - "ulp_rcv_en" value considered when selected to have it via software way |
| 7 | TM_LPRXCD_SEL | R/W | 0h | w_tm_lprxcd_sel - Select signal to choose the lprxcd's block enable value to analog between the one from "lane_always_on" or from the software way onto the port "rxda_lprxcd_en" on Analog interface |
| 6 | TM_LPRXCD | R/W | 0h | w_tm_lprxcd_en - "lprxcd_en" value considered when selected to have it via software way |
| 5-1 | TM_UNUSED_5_1 | R | 0h | RESERVED |
| 0 | TM_FORCE_TX_STOP_STATE | R/W | 0h | 0' - No force on escape mode logic - Check polarity |

11.63 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT2 Register (Offset = 210h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT2 is shown in [Figure 11-62](#) and described in [Table 11-127](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG0

Table 11-126.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0210h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0210h |

Figure 11-62. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_TEST_REG0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-127. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-0 | DIG_EXTRA_TEST_REG0 | R/W | 0h | Digital Extra Functional Test Register 0 |

11.64 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT3 Register (Offset = 214h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT3 is shown in [Figure 11-63](#) and described in [Table 11-129](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg1

Table 11-128.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0214h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0214h |

Figure 11-63. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------------------|-----------------|----|----|----|----|---------------------------------|---------------------------------|
| TM_DIAG_CAL_CLOCK_GATE_EN | TM_UNUSED_30_18 | | | | | | |
| R/W-0h | R-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_30_18 | | | | | | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | TM_PREAMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_ITER_WAIT_TIME | | | | | | | TM_PREAMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-129. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31 | TM_DIAG_CAL_CLOCK_GATE_EN | R/W | 0h | While running diagnostic calibrations, this acts as calibration's clock gate enable Enable = 1 |
| 30-18 | TM_UNUSED_30_18 | R | 0h | RESERVED |
| 17 | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode wait time between two codes selection |
| 16-9 | TM_PREAMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode wait time between two codes |
| 8 | TM_PREAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode initial wait time selection - Select signal to choose between the one from software way or the functional one Functional value gets decided internally based on the "psm_clock_freq" input to Data-Lane |
| 7-0 | TM_PREAMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode initial wait time - "init_value" considered when selected to choose it via software way |

11.65 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4 Register (Offset = 218h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4 is shown in [Figure 11-64](#) and described in [Table 11-131](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg2

Table 11-130.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0218h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0218h |

Figure 11-64. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|-----------------------------|-----------------------|-------------------|---------------|--------------------------|-------------------------|-----------------|
| UNUSED | | | | | TM_PREAMP_ANA_CAL_EN_SEL | TM_PREAMP_ANA_CAL_EN | TM_UNUSED_24_18 |
| R-0h | | | | | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_24_18 | | | | | | TM_PREAMP_CAL_CODE_TUNE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_CODE_TUNE | TM_PREAMP_CAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_OVERRIDE_CODE | TM_PREAMP_CAL_OVERRIDE_EN | TM_PREAMP_CAL_RUN_SEL | TM_PREAMP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-131. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26 | TM_PREAMP_ANA_CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 25 | TM_PREAMP_ANA_CAL_EN | R/W | 0h | test mode analog calibration enable |
| 24-18 | TM_UNUSED_24_18 | R | 0h | RESERVED |
| 17-15 | TM_PREAMP_CAL_CODE_TUNE | R/W | 0h | final preamp cal code tune value |
| 14-7 | TM_PREAMP_CAL_OVERRIDE_CODE | R/W | 0h | preamp calibration override code |
| 6 | TM_PREAMP_CAL_OVERRIDE_EN | R/W | 0h | preamp calibration code override enable |
| 5 | TM_PREAMP_CAL_RUN_SEL | R/W | 0h | test mode calibration run selection |

Table 11-131. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---------------------------|
| 4 | TM_PREAMP_CAL_RUN | R/W | 0h | test mode calibration run |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.66 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT5 Register (Offset = 21Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT5 is shown in [Figure 11-65](#) and described in [Table 11-133](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg1

Table 11-132.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 021Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 021Ch |

Figure 11-65. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT5 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | TM_DCC_COMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-133. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration iteration time enable |
| 16-9 | TM_DCC_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode dcc comp calibration iteration time |
| 8 | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration initial wait time enable |
| 7-0 | TM_DCC_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode dcc comp calibration initial wait time |

11.67 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6 Register (Offset = 220h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6 is shown in [Figure 11-66](#) and described in [Table 11-135](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg2

Table 11-134.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0220h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0220h |

Figure 11-66. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6 Register

| | | | | | | | |
|---------------------------------------|-------------------------------------|---------------------------------|------------------------------------|--------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_DCC_COM P_ANA_CAL_E N_SEL | TM_DCC_COM P_ANA_CAL_E N | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_CODE_TUNE | | | TM_DCC_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_OVER RIDE_CODE | TM_DCC_COM P_CAL_OVER RIDE_EN | TM_DCC_COM P_CAL_RUN_S EL | TM_DCC_COM P_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-135. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_DCC_COMP_ANA_C AL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_DCC_COMP_ANA_C AL_EN | R/W | 0h | test mode dcc comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_DCC_COMP_CAL_C ODE_TUNE | R/W | 0h | test mode dcc comp calibration code tune value |
| 12-7 | TM_DCC_COMP_CAL_O VERRIDE_CODE | R/W | 0h | test mode dcc comp calibration code overirde |
| 6 | TM_DCC_COMP_CAL_O VERRIDE_EN | R/W | 0h | test mode dcc comp calibration override code enable |
| 5 | TM_DCC_COMP_CAL_R UN_SEL | R/W | 0h | dcc comp calibration run selection |
| 4 | TM_DCC_COMP_CAL_R UN | R/W | 0h | dcc comp calibration test mode run |

Table 11-135. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.68 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT7 Register (Offset = 224h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT7 is shown in [Figure 11-67](#) and described in [Table 11-137](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg1

Table 11-136.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0224h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0224h |

Figure 11-67. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT7 Register

| | | | | | | | |
|----------------------------------|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME_E N | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_MIXER_CO MP_CAL_INIT _WAIT_TIME_E N |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-137. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration itertaion time enable |
| 16-9 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode mixer comp calibration iteration time |
| 8 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration initial wait time enable |
| 7-0 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode mixer comp calibration initial wait time |

11.69 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8 Register (Offset = 228h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8 is shown in [Figure 11-68](#) and described in [Table 11-139](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg2

Table 11-138.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0228h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0228h |

Figure 11-68. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8 Register

| | | | | | | | |
|---|---------------------------------------|-----------------------------------|--------------------------------------|----------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_MIXER_CO MP_ANA_CAL_ EN_SEL | TM_MIXER_CO MP_ANA_CAL_ EN | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_CODE_TUNE | | | TM_MIXER_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_CO MP_CAL_OVE RRIDE_CODE | TM_MIXER_CO MP_CAL_OVE RRIDE_EN | TM_MIXER_CO MP_CAL_RUN _SEL | TM_MIXER_CO MP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-139. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_MIXER_COMP_ANA_ CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_MIXER_COMP_ANA_ CAL_EN | R/W | 0h | test mode mixer comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_MIXER_COMP_CAL_ CODE_TUNE | R/W | 0h | test mode mixer comp calibration code tune value |
| 12-7 | TM_MIXER_COMP_CAL_ OVERRIDE_CODE | R/W | 0h | test mode mixer comp calibration code override |
| 6 | TM_MIXER_COMP_CAL_ OVERRIDE_EN | R/W | 0h | test mode mixer comp calibration override code enable |
| 5 | TM_MIXER_COMP_CAL_ RUN_SEL | R/W | 0h | mixer comp calibration run selection |
| 4 | TM_MIXER_COMP_CAL_ RUN | R/W | 0h | mixer comp calibration test mode run |

Table 11-139. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT8 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.70 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT9 Register (Offset = 22Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT9 is shown in [Figure 11-69](#) and described in [Table 11-141](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg1

Table 11-140.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT9
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 022Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 022Ch |

Figure 11-69. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT9 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-141. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_POS_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | posedge sampler calibration iteration time between codes |
| 7-0 | TM_POS_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | posedge sampler calibration initial wait time |

11.71 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10 Register (Offset = 230h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10 is shown in [Figure 11-70](#) and described in [Table 11-143](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg2

Table 11-142.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0230h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0230h |

Figure 11-70. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_MCAL_OVERRIDE_EN | TM_POS_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_PCAL_OVERRIDE_CODE | TM_POS_SAMP_PCAL_OVERRIDE_EN | TM_POS_SAMP_CAL_RUN | TM_POS_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-143. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode iteration wait time enable |
| 30 | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_POS_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override mcal_code |
| 15 | TM_POS_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration mcal_code override en |
| 14-7 | TM_POS_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override pcal_code |
| 6 | TM_POS_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration pcal_code override en |
| 5 | TM_POS_SAMP_CAL_RUN | R/W | 0h | posedge sampler calibration test mode run |

Table 11-143. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT10 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_POS_SAMP_CAL_R UN_SEL | R/W | 0h | posedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.72 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT11 Register (Offset = 234h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT11 is shown in [Figure 11-71](#) and described in [Table 11-145](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg3

Table 11-144.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT11
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0234h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0234h |

Figure 11-71. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT11 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_POS_SAMP_ANA_CAL_EN_SEL | TM_POS_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_POS_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-145. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_POS_SAMP_ANA_CAL_EN_SEL | R/W | 0h | posedge sampler calibration analog calib enable selection |
| 8 | TM_POS_SAMP_ANA_CAL_EN | R/W | 0h | posedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_POS_SAMP_CAL_CODE_TUNE | R/W | 0h | posedge sampler calibration tune code |

11.73 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT12 Register (Offset = 238h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT12 is shown in [Figure 11-72](#) and described in [Table 11-147](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg1

Table 11-146.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT12
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0238h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0238h |

Figure 11-72. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT12 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-147. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | negedge sampler calibration iteration time between codes |
| 7-0 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | negedge sampler calibration initial wait time |

11.74 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13 Register (Offset = 23Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13 is shown in [Figure 11-73](#) and described in [Table 11-149](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg2

Table 11-148.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 023Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 023Ch |

Figure 11-73. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_MCAL_OVERRIDE_EN | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_PCAL_OVERRIDE_CODE | TM_NEG_SAMP_PCAL_OVERRIDE_EN | TM_NEG_SAMP_CAL_RUN | TM_NEG_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-149. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode iteration wait time enable |
| 30 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_NEG_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override mcal_code |
| 15 | TM_NEG_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration mcal_code override en |
| 14-7 | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override pcal_code |
| 6 | TM_NEG_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration pcal_code override en |
| 5 | TM_NEG_SAMP_CAL_RUN | R/W | 0h | negedge sampler calibration test mode run |

Table 11-149. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT13 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_NEG_SAMP_CAL_R UN_SEL | R/W | 0h | negedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.75 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT14 Register (Offset = 240h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT14 is shown in [Figure 11-74](#) and described in [Table 11-151](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg3

Table 11-150.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT14
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0240h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0240h |

Figure 11-74. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT14 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_NEG_SAMP_ANA_CAL_EN_SEL | TM_NEG_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_NEG_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-151. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_NEG_SAMP_ANA_CAL_EN_SEL | R/W | 0h | negedge sampler calibration analog calib enable selection |
| 8 | TM_NEG_SAMP_ANA_CAL_EN | R/W | 0h | negedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_NEG_SAMP_CAL_CODE_TUNE | R/W | 0h | negedge sampler calibration tune code |

11.76 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT15 Register (Offset = 244h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT15 is shown in [Figure 11-75](#) and described in [Table 11-153](#).

Return to [Summary Table](#).

skew_cal_fsm_reg1

Table 11-152.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT15
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0244h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0244h |

Figure 11-75. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT15 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|----|----|--------------------------------|------------------------------------|-----------------------------------|------------------------------|------------------------------|
| UNUSED | | | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | | | | | TM_SKEW_CAL_FPHASE_WAIT_TIME | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_FPHASE_WAIT_TIME | | | | | | | TM_SKEW_CAL_TIMER_INIT_COUNT |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-153. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | R/W | 0h | skew calibration analog max saturation test mode enable |
| 27 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | R/W | 0h | skew calibration analog max saturation selection |
| 26-18 | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | R/W | 0h | skew calibration fast phase long wait time |
| 17-9 | TM_SKEW_CAL_FPHASE_WAIT_TIME | R/W | 0h | skew calibration fast phase wait time |
| 8-0 | TM_SKEW_CAL_TIMER_INIT_COUNT | R/W | 0h | skew calibration initial wait time |

11.77 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT16 Register (Offset = 248h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT16 is shown in [Figure 11-76](#) and described in [Table 11-155](#).

Return to [Summary Table](#).

skew_cal_fsm_reg2

Table 11-154.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT16
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0248h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0248h |

Figure 11-76. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT16 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|------------------------------------|------------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | |
| R-0h | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_ACC_CODE_MIN_VALUE | | | | | | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | TM_SKEW_CAL_SPHASE_WAIT_TIME |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_SPHASE_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-155. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26-19 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | R/W | 0h | skew calibration delay code test mode max value |
| 18 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | R/W | 0h | skew calibration max code test reg selection |
| 17-10 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | R/W | 0h | skew calibration delay code test mode min value |
| 9 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | R/W | 0h | skew calibration min code test reg selection |
| 8-0 | TM_SKEW_CAL_SPHASE_WAIT_TIME | R/W | 0h | skew calibration slow phase wait time |

11.78 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT17 Register (Offset = 24Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT17 is shown in [Figure 11-77](#) and described in [Table 11-157](#).

Return to [Summary Table](#).

skew_cal_fsm_reg3

Table 11-156.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT17
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 024Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 024Ch |

Figure 11-77. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT17 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_DESKEW_START_CODE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-157. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|-------------------------------------|
| 31-8 | UNUSED | R | 0h | RESERVED |
| 7-0 | TM_SKEW_CAL_DESKEW_START_CODE | R/W | 0h | skew calibration initial start code |

11.79 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT18 Register (Offset = 250h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT18 is shown in [Figure 11-78](#) and described in [Table 11-159](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg1

Table 11-158.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT18
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0250h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0250h |

Figure 11-78. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT18 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_TIMER_ITER_COUNT | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_TIMER_ITER_COUNT | | | | | | | TM_DUCY_CORR_TIMER_INIT_COUNT |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CORR_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-159. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-9 | TM_DUCY_CORR_TIME_R_ITER_COUNT | R/W | 0h | duty cycle correction iteration wait time specified in this register will be considered when a non-zero value is specified here |
| 8-0 | TM_DUCY_CORR_TIME_R_INIT_COUNT | R/W | 0h | duty cycle correction initial wait time specified in this register will be considered when a non-zero value is specified here |

11.80 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT19 Register (Offset = 254h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT19 is shown in [Figure 11-79](#) and described in [Table 11-161](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg2

Table 11-160.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT19
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0254h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0254h |

Figure 11-79. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT19 Register

| | | | | | | | |
|---|---|-----------------------------|---|---------------------------------|----|-------------------------------------|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_ACC_CODE_ MAX_VALUE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_ACC_CODE_MAX_VALUE | | | TM_DUCY_CO RR_ACC_COD E_MAX_VALUE _SEL | TM_DUCY_CORR_ACC_CODE_MIN_VALUE | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CO RR_ACC_COD E_MIN_VALUE | TM_DUCY_CO RR_ACC_COD E_MIN_VALUE _SEL | TM_DUCY_CORR_ACC_START_CODE | | | | | TM_DUCY_CO RR_ACC_STA RT_CODE_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-161. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-13 | TM_DUCY_CORR_ACC_ CODE_MAX_VALUE | R/W | 0h | duty cycle correction test mode max value |
| 12 | TM_DUCY_CORR_ACC_ CODE_MAX_VALUE_SEL | R/W | 0h | duty cycle correction test mode max value selection |
| 11-7 | TM_DUCY_CORR_ACC_ CODE_MIN_VALUE | R/W | 0h | duty cycle correction test mode min value |
| 6 | TM_DUCY_CORR_ACC_ CODE_MIN_VALUE_SEL | R/W | 0h | duty cycle correction test mode min value selection |
| 5-1 | TM_DUCY_CORR_ACC_ START_CODE | R/W | 0h | duty cycle correction test mode start code |
| 0 | TM_DUCY_CORR_ACC_ START_CODE_SEL | R/W | 0h | duty cycle correction test mode start code selection |

11.81 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20 Register (Offset = 258h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20 is shown in [Figure 11-80](#) and described in [Table 11-163](#).

Return to [Summary Table](#).

skew_cal_avg_reg1

Table 11-162.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0258h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0258h |

Figure 11-80. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------------|----------------------------------|---------------------|----|----|---------------------------------|----------------------|------------------------------------|
| TM_ANA_DES KEW_DCC_EN | TM_ANA_DES KEW_DCC_EN _SEL | TM_DCC_CODE_TUNE | | | TM_DCC_COD E_OVERRIDE_ EN | TM_DCC_CODE_OVERRIDE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DCC_CODE_OVERRIDE | | TM_DESKEW_CODE_TUNE | | | | | TM_DESKEW_ CODE_OVERR IDE_EN |
| R/W-0h | | R/W-0h | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_CODE_OVERRIDE | | | | | | | TM_PROC_TIM ER_LOAD_VAL |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PROC_TIMER_LOAD_VAL | | | | | | | TM_PROC_TIM ER_LOAD_VAL _SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-163. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31 | TM_ANA_DESKEW_DCC_EN | R/W | 0h | test mode analog deskew enable |
| 30 | TM_ANA_DESKEW_DCC_EN_SEL | R/W | 0h | test mode deskew analog enable selection |
| 29-27 | TM_DCC_CODE_TUNE | R/W | 0h | duty cycle correction code tune |
| 26 | TM_DCC_CODE_OVERRIDE_EN | R/W | 0h | duty cycle correction code override enable |
| 25-22 | TM_DCC_CODE_OVERRIDE | R/W | 0h | duty cycle correction override code |
| 21-17 | TM_DESKEW_CODE_TUNE | R/W | 0h | skew calibration delay line code tune |
| 16 | TM_DESKEW_CODE_OVERRIDE_EN | R/W | 0h | skew calibration delay code override enable |
| 15-9 | TM_DESKEW_CODE_OVERRIDE | R/W | 0h | skew calibration delay line override code |

Table 11-163. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 8-1 | TM_PROC_TIMER_LOAD_VAL | R/W | 0h | skew calibration process time test mode value |
| 0 | TM_PROC_TIMER_LOAD_VAL_SEL | R/W | 0h | skew calibration process time test mode value selection |

11.82 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT21 Register (Offset = 25Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT21 is shown in [Figure 11-81](#) and described in [Table 11-165](#).

Return to [Summary Table](#).

skew_cal_avg_reg2

Table 11-164.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT21
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 025Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 025Ch |

Figure 11-81. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT21 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|------------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG LENG_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG LENG_TIMER_LOAD_VAL | | | | | | TM_AVG2AVG LENG_TIMER_LOAD_VAL_SEL | TM_DCC_ACC LENG_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC LENG_TIMER_LOAD_VAL | | | | | | TM_DCC_ACC LENG_TIMER_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-165. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG LENG_TIMER_LOAD_VAL | R/W | 0h | delay line code averaging to dcc code averaging wait time |
| 9 | TM_AVG2AVG LENG_TIMER_LOAD_VAL_SEL | R/W | 0h | delay line code averaging to dcc code averaging wait time selection |
| 8-1 | TM_DCC_ACC LENG_TIMER_LOAD_VAL | R/W | 0h | total number of dcc codes to be taken for averaging in test mode |
| 0 | TM_DCC_ACC LENG_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection value for test mode number of dcc codes under averaging |

11.83 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT22 Register (Offset = 260h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT22 is shown in [Figure 11-82](#) and described in [Table 11-167](#).

Return to [Summary Table](#).

skew_cal_avg_reg3

Table 11-166.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT22
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0260h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0260h |

Figure 11-82. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT22 Register

| | | | | | | | |
|--|----|----|----|----|----|--|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ DONE_LEN TIMER_LOAD_ VAL_SEL | TM_DESKEW_ ACC_LEN TIMER_LOAD_ VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ ACC_LEN TIMER_LOAD_ VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-167. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | R/W | 0h | after skew calibration is done, length of wait timer |
| 9 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | test mode selection value for length of wait time after deskew |
| 8-1 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | R/W | 0h | number of deskew dealy codes to be taken for averaging |
| 0 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | tets mode selction for test mode number of delay line codes for averaging |

11.84 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT23 Register (Offset = 264h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT23 is shown in [Figure 11-83](#) and described in [Table 11-169](#).

Return to [Summary Table](#).

skew_cal_avg_reg4

Table 11-168.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT23
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0264h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0264h |

Figure 11-83. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT23 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-----------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG_RES_TIMER_LOAD_VAL | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | TM_DCC_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC_RES_TIMER_LOAD_VAL | | | | | | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-169. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging to deskew averaging wait time in test mode |
| 9 | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging to deskew averaging wait time |
| 8-1 | TM_DCC_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging wait time in test mode |
| 0 | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging wait time |

11.85 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT24 Register (Offset = 268h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT24 is shown in [Figure 11-84](#) and described in [Table 11-171](#).

Return to [Summary Table](#).

skew_cal_avg_reg5

Table 11-170.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT24
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0268h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0268h |

Figure 11-84. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT24 Register

| | | | | | | | |
|-----------------------------------|----|----|----|----|----|---------------------------------------|--------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | | | | | | | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-171. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew done wait time in test mode |
| 9 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selction of resolution time of deskew done wait time in test mode |
| 8-1 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew averaging wait time in test mode |
| 0 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | tets mode selection of resolution time of deskew averaging wait time in test mode |

11.86 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT25 Register (Offset = 26Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT25 is shown in [Figure 11-85](#) and described in [Table 11-173](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG0

Table 11-172.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT25
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 026Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 026Ch |

Figure 11-85. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-173. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT0 | R | 0h | RESERVED |

11.87 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT26 Register (Offset = 270h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT26 is shown in [Figure 11-86](#) and described in [Table 11-175](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG1

Table 11-174.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT26
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0270h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0270h |

Figure 11-86. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-175. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT1 | R | 0h | RESERVED |

11.88 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT27 Register (Offset = 274h) [reset = 0A000018h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT27 is shown in [Figure 11-87](#) and described in [Table 11-177](#).

Return to [Summary Table](#).

bist_config_reg1

Table 11-176.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT27
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0274h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0274h |

Figure 11-87. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT27 Register

| | | | | | | | |
|---------------------|----|----|--------------|----|-------------|-----------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_IDLE_TIME_LENGTH | | | | | | | |
| R/W-Ah | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_MODE | | | TM_PRBS_MODE | | TM_UNUSED_2 | TM_FREEZE | TM_BIST_EN |
| R/W-0h | | | R/W-3h | | R-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-177. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-24 | TM_IDLE_TIME_LENGTH | R/W | Ah | BIST_IDLE_TIME |
| 23-8 | TM_UNUSED_23_8 | R | 0h | RESERVED |
| 7-5 | TM_TEST_MODE | R/W | 0h | PRBS mode - when set to '1' PRBS mode is selected |
| 4-3 | TM_PRBS_MODE | R/W | 3h | BIST PRBS MODE 9 when 0x0 |
| 2 | TM_UNUSED_2 | R | 0h | RESERVED |
| 1 | TM_FREEZE | R/W | 0h | Freeze the LFSR contents after every packet or frame |
| 0 | TM_BIST_EN | R/W | 0h | Enable signal for pattern checker |

11.89 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT28 Register (Offset = 278h) [reset = DECDBCABh]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT28 is shown in [Figure 11-88](#) and described in [Table 11-179](#).

Return to [Summary Table](#).

bist_config_reg2

Table 11-178.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT28
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0278h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0278h |

Figure 11-88. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_TEST_PAT4 | | | | | | | | TM_TEST_PAT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_PAT2 | | | | | | | | TM_TEST_PAT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-179. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-24 | TM_TEST_PAT4 | R/W | DEh | User registers to specify the BIST data4 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 23-16 | TM_TEST_PAT3 | R/W | CDh | User registers to specify the BIST data3 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 15-8 | TM_TEST_PAT2 | R/W | BCh | User registers to specify the BIST data2 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 7-0 | TM_TEST_PAT1 | R/W | ABh | User registers to specify the BIST data1 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |

11.90 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT29 Register (Offset = 27Ch) [reset = 28h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT29 is shown in [Figure 11-89](#) and described in [Table 11-181](#).

Return to [Summary Table](#).

bist_config_reg3

Table 11-180.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT29
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 027Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 027Ch |

Figure 11-89. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT29 Register

| | | | | | | | |
|-----------------|----|----|---------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_CLEAR_BIST | TM_UNUSED_27_12 | | | |
| R-0h | | | R/W-0h | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_27_12 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_27_12 | | | | TM_PKT_LENGTH | | | |
| R-0h | | | | R/W-28h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PKT_LENGTH | | | | | | | |
| R/W-28h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-181. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_CLEAR_BIST | R/W | 0h | Setting this will clear all the BIST related flags and counters |
| 27-12 | TM_UNUSED_27_12 | R | 0h | RESERVED |
| 11-0 | TM_PKT_LENGTH | R/W | 28h | Based on the default_mode design will consider the run-length from design or the programmed value specified here |

11.91 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT30 Register (Offset = 280h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT30 is shown in [Figure 11-90](#) and described in [Table 11-183](#).

Return to [Summary Table](#).

bist_config_reg4

Table 11-182.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT30
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0280h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0280h |

Figure 11-90. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT30 Register

| | | | | | | | |
|--------|----|----|----|----|----|---------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | TM_LPRX_BIS T_EN | TM_HSRX_BIS T_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-183. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-2 | UNUSED | R | 0h | RESERVED |
| 1 | TM_LPRX_BIST_EN | R/W | 0h | LPRX BIST is enabled - rxda_lprx_bist_en - When '1', LP BIST is enabled |
| 0 | TM_HSRX_BIST_EN | R/W | 0h | HSRX BIST is enabled - rxda_hsrx_bist_en - when '1', HS BIST is enabled |

11.92 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT31 Register (Offset = 284h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT31 is shown in [Figure 11-91](#) and described in [Table 11-185](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG1

Table 11-184.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT31
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0284h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0284h |

Figure 11-91. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-185. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT1 | R | 0h | RESERVED |

11.93 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT32 Register (Offset = 288h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT32 is shown in [Figure 11-92](#) and described in [Table 11-187](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG2

Table 11-186.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT32
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0288h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0288h |

Figure 11-92. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-187. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT2 | R | 0h | RESERVED |

11.94 DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT2 Register (Offset = 28Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT2 is shown in [Figure 11-93](#) and described in [Table 11-189](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-188.
DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 028Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 028Ch |

Figure 11-93. DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-189. DPHY_RX_VBUS2APB_DL0_RX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | ANA_READ_TBIT0 | R | 0h | Analog read register 0 |

11.95 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT33 Register (Offset = 290h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT33 is shown in [Figure 11-94](#) and described in [Table 11-191](#).

Return to [Summary Table](#).

deserialiser_fsm_status

Table 11-190.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT33
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0290h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0290h |

Figure 11-94. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|------------------|----|-------------|----|----|----|-------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_PPI_CUR_STATE | | | | | | TM_CTRL_CUR_STATE | | | |
| R-0h | | | | | | R-0h | | | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_CTRL_CUR_STATE | | | | | | | | TM_SYNC_PKT | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-191. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-26 | UNUSED | R | 0h | RESERVED |
| 25-18 | TM_PPI_CUR_STATE | R | 0h | Current State of the SYNC detection FSM during the HS data receive mode or skew calibration mode |
| 17-8 | TM_CTRL_CUR_STATE | R | 0h | current state status of HS receive FSM |
| 7-0 | TM_SYNC_PKT | R | 0h | Status of received SYNC packet |

11.96 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT34 Register (Offset = 294h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT34 is shown in [Figure 11-95](#) and described in [Table 11-193](#).

Return to [Summary Table](#).

lp_status

Table 11-192.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT34
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0294h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0294h |

Figure 11-95. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT34 Register

| | | | | | | | |
|--------------------|----|--------------|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | TM_LP_RX_CUR_STATE | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_LP_RX_CUR_STATE | | TM_LP_STATUS | | | | | |
| R-0h | | R-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-193. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-19 | UNUSED | R | 0h | RESERVED |
| 18-14 | TM_LP_RX_CUR_STATE | R | 0h | Current state of LP receiver FSM |
| 13-8 | TM_LP_STATUS | R | 0h | Status of DP,DN pins of LPRX, LPCD, ULPRX respectively |
| 7-0 | UNUSED_7_0 | R | 0h | RESERVED |

11.97 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT35 Register (Offset = 298h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT35 is shown in [Figure 11-96](#) and described in [Table 11-195](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_READ_REG0

Table 11-194.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT35
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0298h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0298h |

Figure 11-96. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-195. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.98 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36 Register (Offset = 29Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36 is shown in [Figure 11-97](#) and described in [Table 11-197](#).

Return to [Summary Table](#).

dcc_mixer_comparator_calibration_stat

Table 11-196.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 029Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 029Ch |

Figure 11-97. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36 Register

| | | | | | | | |
|--------------------------|--------------------------|---------------------|----|----|----|---------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_MIX_COM P_ANA_RESP | TM_MIX_COMP_CALCODE | | | | TM_MIX_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIX_COM P_CAL_DONE | TM_DCC_COM P_ANA_RESP | TM_DCC_COMP_CALCODE | | | | TM_DCC_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_DONE | TM_CALIB_CTRL_CUR_STATE | | | | | TM_CUR_DRX _CAL_DONE | |
| R-0h | R-0h | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-197. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_MIX_COMP_ANA_RESP | R | 0h | Mixer comparator analog response |
| 21-17 | TM_MIX_COMP_CALCODE | R | 0h | Mixer comparator calibration code |
| 16 | TM_MIX_COMP_CAL_NO_RESP | R | 0h | Mixer comparator calibration has no response from analog |
| 15 | TM_MIX_COMP_CAL_DONE | R | 0h | Mixer comparator calibration is done properly |
| 14 | TM_DCC_COMP_ANA_RESP | R | 0h | Duty Cycle Comparator analog response |
| 13-9 | TM_DCC_COMP_CALCODE | R | 0h | Duty cycle corrector comparator calibration code |
| 8 | TM_DCC_COMP_CAL_NO_RESP | R | 0h | Duty cycle corrector comparator calibration has no response from analog |

Table 11-197. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT36 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7 | TM_DCC_COMP_CAL_DONE | R | 0h | Duty cycle corrector comparator calibration is done properly |
| 6-1 | TM_CALIB_CTRL_CUR_STATE | R | 0h | If struck, indicates calibration FSM current state |
| 0 | TM_CUR_DRX_CAL_DONE | R | 0h | Current DRX DPHY_RX_VBUS2APB_LANE calibrations are done |

11.99 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37 Register (Offset = 2A0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37 is shown in [Figure 11-98](#) and described in [Table 11-199](#).

Return to [Summary Table](#).

preamp_cal_status_reg1

Table 11-198.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 02A0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 02A0h |

Figure 11-98. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------|----|-----------------------------|--------------------------|---------------------------------|-------------------------|-----------------------------------|
| TM_ANA_RES_P_STAT | TM_PREAMP_STAT_ANA_CAL_CODE | | | | | | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE |
| R-0h | R-0h | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | | | | | | | TM_PREAMP_STAT_NCAL_PREAMP_CODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_STAT_NCAL_PREAMP_CODE | | | | | TM_PREAMP_STAT_PCAL_PREAMP_CODE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_STAT_PCAL_PREAMP_CODE | TM_PREAMP_STAT_NCAL_NO_RESP | | TM_PREAMP_STAT_PCAL_NO_RESP | TM_PREAMP_STAT_NCAL_DONE | TM_PREAMP_STAT_PCAL_DONE | TM_PREAMP_STAT_CAL_DONE | |
| R-0h | R-0h | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-199. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31 | TM_ANA_RESP_STAT | R | 0h | current analog or test mode response for which calibration is happening |
| 30-25 | TM_PREAMP_STAT_ANA_CAL_CODE | R | 0h | code going to analog |
| 24-17 | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | R | 0h | code decided to send to analog before tune |
| 16-11 | TM_PREAMP_STAT_NCAL_PREAMP_CODE | R | 0h | calib code in posedge_data run |
| 10-5 | TM_PREAMP_STAT_PCAL_PREAMP_CODE | R | 0h | calib code in negedge_data run |
| 4 | TM_PREAMP_STAT_NCAL_NO_RESP | R | 0h | negedge_data run has no response |
| 3 | TM_PREAMP_STAT_PCAL_NO_RESP | R | 0h | posedge_data run has no response |
| 2 | TM_PREAMP_STAT_NCAL_DONE | R | 0h | negedge_data cal run is done |

Table 11-199. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT37 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|------------------------------|
| 1 | TM_PREAMP_STAT_PCA L_DONE | R | 0h | posedge_data cal run is done |
| 0 | TM_PREAMP_STAT_CAL _DONE | R | 0h | preamp calibration is done |

11.100 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38 Register (Offset = 2A4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38 is shown in [Figure 11-99](#) and described in [Table 11-201](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg1

Table 11-200.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02A4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02A4h |

Figure 11-99. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38 Register

| | | | | | | | |
|---------------------------------|----|----|---|---------------------------------|----------------------------|---------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_POS_SAMP_STAT_SAMP LTM_POS_SAMP_STAT_CAL_DONE | TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_POS_SAMP_STAT_CODE_TYPE | TM_POS_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_UP_CAL_CODE | | | | | | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | TM_POS_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-201. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_POS_SAMP_STAT_SAMP LTM_POS_SAMP_STAT_CAL_DONE | R | 0h | posedge sampler calibration is done |
| 19-11 | TM_POS_SAMP_STAT_FINAL_CAL_CODE | R | 0h | posedge sampler calibration final code |
| 10 | TM_POS_SAMP_STAT_CODE_TYPE | R | 0h | code type that is changing for posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-201. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT38 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_POS_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.101 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT39 Register (Offset = 2A8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT39 is shown in [Figure 11-100](#) and described in [Table 11-203](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg2

Table 11-202.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT39
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02A8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02A8h |

Figure 11-100. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT39 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|--|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_POS_SAMP P_ANA_CAL_R ESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_POS_SAMP P_STAT_ANA_ CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_POS_SAMP_STAT_DOWN_ CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_POS_SAMP P_STAT_NO_D OWN_CAL_RE SP | TM_POS_SAMP P_STAT_DOW N_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-203. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_POS_SAMP_ANA_CAL_RESP | R | 0h | test mode status of posedge sampler |
| 23-17 | TM_POS_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to posedge sampler |
| 16-10 | TM_POS_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_POS_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.102 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40 Register (Offset = 2ACh) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40 is shown in [Figure 11-101](#) and described in [Table 11-205](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg1

Table 11-204.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02ACh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02ACh |

Figure 11-101. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40 Register

| | | | | | | | |
|---------------------------------|----|----|---|---------------------------------|----------------------------|---------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_NEG_SAMP_STAT_CODE_TYPE | TM_NEG_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_UP_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_UP_CAL_RESP | TM_NEG_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-205. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | R | 0h | negedge sampler calibration is done |
| 19-11 | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | R | 0h | negedge sampler calibration final code |
| 10 | TM_NEG_SAMP_STAT_CODE_TYPE | R | 0h | code type that is changing for negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-205. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT40 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_NEG_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.103 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT41 Register (Offset = 2B0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT41 is shown in [Figure 11-102](#) and described in [Table 11-207](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg2

Table 11-206.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT41
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02B0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02B0h |

Figure 11-102. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT41 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_NEG_SAMP_ANA_CAL_RESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_NEG_SAMP_STAT_ANA_CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | TM_NEG_SAMP_STAT_DOWN_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-207. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT41 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_NEG_SAMP_ANA_CAL_RESP | R | 0h | test mode status of negedge sampler |
| 23-17 | TM_NEG_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to negedge sampler |
| 16-10 | TM_NEG_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_NEG_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.104 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42 Register (Offset = 2B4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42 is shown in [Figure 11-103](#) and described in [Table 11-209](#).

[Return to Summary Table.](#)

skew_cal_fsm_status_reg1

Table 11-208.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 02B4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 02B4h |

Figure 11-103. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42 Register

| | | | | | | | |
|------------------------------------|----|-------------------------------------|-------------------------|----|-----------------------------------|-----------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_DESKEW_DCC_CUR_STATE | | | | |
| R-0h | | | R-0h | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_CUR_STATE | | TM_DESKEW_DCC_INIT_MIXER_VALUE | TM_SP_FIRST_TRIP_CODE | | | | |
| R-0h | | R-0h | R-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SP_FIRST_TRIP_CODE | | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | | | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | |
| R-0h | | R-0h | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | | | | | | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | |
| R-0h | | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-209. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28-22 | TM_DESKEW_DCC_CUR_STATE | R | 0h | Duty cycle correction logic current state |
| 21 | TM_DESKEW_DCC_INIT_MIXER_VALUE | R | 0h | Duty cycle correction initial comparator value |
| 20-14 | TM_SP_FIRST_TRIP_CODE | R | 0h | slow phase first trip code |
| 13-10 | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | R | 0h | current state of the deskew FSM |
| 9 | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | R | 0h | if asserted, deskew FSM has gone into max saturation second time |
| 8 | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | R | 0h | if asserted, deskew FSM has got saturated once |

Table 11-209. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT42 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------------|------|-------|--------------------------------------|
| 7-1 | TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | R | 0h | deskew FSM fast phase trip code |
| 0 | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | R | 0h | deskew algorithm mixer initial value |

11.105 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT43 Register (Offset = 2B8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT43 is shown in [Figure 11-104](#) and described in [Table 11-211](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg1

Table 11-210.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT43
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02B8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02B8h |

Figure 11-104. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT43 Register

| | | | | | | | |
|-------------------------------------|----------------------------------|----|----|-------------------------------------|-------------------------------|----------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | | | | | | | TM_DESKEW_DCC_AVG_ANA_DCC_CODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DCC_AVG_ANA_DCC_CODE | | | | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | | | | TM_DESKEW_DCC_AVG_DONE_DESKEW | TM_DESKEW_DCC_AVG_DONE_DCC | |
| R-0h | R-0h | | | | R-0h | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-211. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT43 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-17 | TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | R | 0h | final code going to delay line |
| 16-13 | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | R | 0h | final code going to duty cycle corrector |
| 12-6 | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | R | 0h | delay line code before tuning |
| 5-2 | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | R | 0h | duty code before tuning |
| 1 | TM_DESKEW_DCC_AVG_DONE_DESKEW | R | 0h | skew calibration is done |
| 0 | TM_DESKEW_DCC_AVG_DONE_DCC | R | 0h | duty cycle correction is done |

11.106 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT44 Register (Offset = 2BCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT44 is shown in [Figure 11-105](#) and described in [Table 11-213](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg2

Table 11-212.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT44
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02BCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02BCh |

Figure 11-105. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT44 Register

| | | | | | | | | | | | | | | | |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | TM_D ESKE W_DC C_AVG _CUT M_DE SKEW _DCC_ AVG_S TATE | |
| R-0h | | | | | | | | | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-213. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT44 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-17 | UNUSED | R | 0h | RESERVED |
| 16-0 | TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | R | 0h | current state of deskew_dcc_averaging FSM |

11.107 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT45 Register (Offset = 2C0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT45 is shown in [Figure 11-106](#) and described in [Table 11-215](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG0

Table 11-214.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT45
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02C0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02C0h |

Figure 11-106. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT45 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-215. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT45 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT0 | R | 0h | RESERVED |

11.108 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT46 Register (Offset = 2C4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT46 is shown in [Figure 11-107](#) and described in [Table 11-217](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG1

Table 11-216.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT46
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02C4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02C4h |

Figure 11-107. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT46 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-217. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT46 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT1 | R | 0h | RESERVED |

11.109 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT47 Register (Offset = 2C8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT47 is shown in [Figure 11-108](#) and described in [Table 11-219](#).

Return to [Summary Table](#).

bist_status_reg1

Table 11-218.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT47
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02C8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02C8h |

Figure 11-108. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT47 Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| W_PAT_CHE_ERROR_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W_PAT_CHE_PKT_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-219. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT47 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-16 | W_PAT_CHE_ERROR_COUNT | R | 0h | BIST Pattern checker error count's live status can be obtained by poling this field |
| 15-0 | W_PAT_CHE_PKT_COUNT | R | 0h | BIST packet count's live status can be obtained by poling this field |

11.110 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT48 Register (Offset = 2CCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT48 is shown in [Figure 11-109](#) and described in [Table 11-221](#).

Return to [Summary Table](#).

bist_status_reg2

Table 11-220.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT48
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02CCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02CCh |

Figure 11-109. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT48 Register

| | | | | | | | |
|--------|----|----|----|----|------------------|--------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | W_BIST_ERRO R | R_PAT_CHE_S YNC | W_DRX_BIST_ PASS |
| R-0h | | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-221. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT48 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-3 | UNUSED | R | 0h | RESERVED |
| 2 | W_BIST_ERROR | R | 0h | Status of HS data path comparison outcome, '0' means pass |
| 1 | R_PAT_CHE_SYNC | R | 0h | Informs BIST Pattern checker is not in sync with pattern generator - Check polarity |
| 0 | W_DRX_BIST_PASS | R | 0h | Entire DRX has passed BIST when this bit's status is set |

11.111 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT49 Register (Offset = 2D0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT49 is shown in [Figure 11-110](#) and described in [Table 11-223](#).

Return to [Summary Table](#).

DIG_BIST_EXTRA_READ_REG0

Table 11-222.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT49
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02D0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02D0h |

Figure 11-110. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT49 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_BIST_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-223. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT49 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31-0 | DIG_BIST_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.112 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT50 Register (Offset = 2D4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT50 is shown in [Figure 11-111](#) and described in [Table 11-225](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG1

Table 11-224.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT50
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02D4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02D4h |

Figure 11-111. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT50 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-225. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT50 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT1 | R | 0h | RESERVED |

11.113 DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT51 Register (Offset = 2D8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT51 is shown in [Figure 11-112](#) and described in [Table 11-227](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG2

Table 11-226.
DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT51
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 02D8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 02D8h |

Figure 11-112. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT51 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-227. DPHY_RX_VBUS2APB_DL0_RX_DIG_TBIT51 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT2 | R | 0h | RESERVED |

11.114 DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT0 Register (Offset = 300h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT0 is shown in [Figure 11-113](#) and described in [Table 11-229](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-228.
DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0300h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0300h |

Figure 11-113. DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-229. DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

11.115 DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT1 Register (Offset = 304h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT1 is shown in [Figure 11-114](#) and described in [Table 11-231](#).

Return to [Summary Table](#).

ANA_EXTRA_TBIT0

Table 11-230.
DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0304h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0304h |

Figure 11-114. DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-231. DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | ANA_EXTRA_TBIT0 | R | 0h | RESERVED |

11.116 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0 Register (Offset = 308h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0 is shown in [Figure 11-115](#) and described in [Table 11-233](#).

Return to [Summary Table](#).

DIG_TBIT0

Table 11-232.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0308h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0308h |

Figure 11-115. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0 Register

| | | | | | | | |
|--------------------------|---------------------------|--------------------------|-------------------------------------|-------------------|------------|--------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_1P5TO2P5 G_MODE_SEL | TM_1P5TO2P5 G_MODE_EN | TM_STD_BY | TM_STD_BY_S EL | TM_TERM_EN | TM_TERM_EN _SEL | TM_SETTLE_C OUNT_SEL |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SETTLE_COUNT | | | | | | | SETTLE_COU NT_OFFSET_C ORR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SETTLE_COUNT_OFFSET_CORR | | | TM_DISABLE_ BCLK_PHASE_ ALIGN | UNUSED_3_0 | | | |
| R/W-0h | | | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-233. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_1P5TO2P5G_MODE_ SEL | R/W | 0h | w_tm_1p5to2p5g_mode_sel - Select signal to choose "mode_en" based on top-level "bandctrl" input provided [or] from software register |
| 21 | TM_1P5TO2P5G_MODE_ EN | R/W | 0h | w_tm_1p5to2p5g_mode_en - "mode_en" value considered when selected to have it via software way |
| 20 | TM_STD_BY | R/W | 0h | w_tm_std_by - "tm_std_by" value to be considered when selected to have it via software way Part of control logic to initiate movement of "calib_ctrl" FSM |
| 19 | TM_STD_BY_SEL | R/W | 0h | w_tm_std_by_sel - Select signal to choose between functional "tm_std_by" [or] from software register |
| 18 | TM_TERM_EN | R/W | 0h | w_tm_term_en - "tm_term_en" value to be considered when selected to have it via software way Value provided here converges onto "rxda_rx_term_en" pin on alalog interface |

Table 11-233. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|---------------------------------|------|-------|--|
| 17 | TM_TERM_EN_SEL | R/W | 0h | w_tm_term_en_sel - Select signal to choose between functional "term_en_sel" [or] from software register |
| 16 | TM_SETTLE_COUNT_SE L | R/W | 0h | Test mode settle count selection = 0 - Select signal to choose between functional "settle_count" [or] from software register Value obtained in functional mode depends on the "BandCtl" and "Settle_count_offset" [ie, bits [8:5] here] |
| 15-9 | TM_SETTLE_COUNT | R/W | 0h | Test mode settle count, if bit <16> is set - "settle_count" value to be considered when selected to have it via software way |
| 8-5 | SETTLE_COUNT_OFFSE T_CORR | R/W | 0h | Settle count offset correction value that adds up to the internal predefined settle count based on "BandCtl" which helps in deciding the final "settle_count" to be observed for |
| 4 | TM_DISABLE_BCLK_PH ASE_ALIGN | R/W | 0h | test mode to disable byte clock phase alignment 0-enable 1-disable |
| 3-0 | UNUSED_3_0 | R | 0h | RESERVED |

11.117 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT1 Register (Offset = 30Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT1 is shown in [Figure 11-116](#) and described in [Table 11-235](#).

Return to [Summary Table](#).

DIG_TBIT1

Table 11-234.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 030Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 030Ch |

Figure 11-116. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT1 Register

| | | | | | | | |
|---------------|-----------|---------------|----|----|----|----------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_ULP_RCV_SEL | TM_ULP_RCV |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_LPRXCD_SEL | TM_LPRXCD | TM_UNUSED_5_1 | | | | | TM_FORCE_TX_STOP_STATE |
| R/W-0h | R/W-0h | R-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-235. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_ULP_RCV_SEL | R/W | 0h | w_tm_ulp_rcv_sel - Select signal to choose between functional "ulp_rcv_en" or a value from software register. The effective value converges onto port "i_ana_ulps_rcv_en" of "lane_always_on" block at DPHY_RX_VBUS2APB_LANE-level |
| 8 | TM_ULP_RCV | R/W | 0h | w_tm_ulp_rcv_en - "ulp_rcv_en" value considered when selected to have it via software way |
| 7 | TM_LPRXCD_SEL | R/W | 0h | w_tm_lprxcd_sel - Select signal to choose the lprxcd's block enable value to analog between the one from "lane_always_on" or from the software way onto the port "rxda_lprxcd_en" on Analog interface |
| 6 | TM_LPRXCD | R/W | 0h | w_tm_lprxcd_en - "lprxcd_en" value considered when selected to have it via software way |
| 5-1 | TM_UNUSED_5_1 | R | 0h | RESERVED |
| 0 | TM_FORCE_TX_STOP_STATE | R/W | 0h | 0' - No force on escape mode logic - Check polarity |

11.118 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT2 Register (Offset = 310h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT2 is shown in [Figure 11-117](#) and described in [Table 11-237](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG0

Table 11-236.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0310h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0310h |

Figure 11-117. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_TEST_REG0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-237. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-0 | DIG_EXTRA_TEST_REG0 | R/W | 0h | Digital Extra Functional Test Register 0 |

11.119 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT3 Register (Offset = 314h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT3 is shown in [Figure 11-118](#) and described in [Table 11-239](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg1

Table 11-238.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0314h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0314h |

Figure 11-118. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT3 Register

| | | | | | | | |
|------------------------------|-----------------|----|----|----|----|---------------------------------|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_DIAG_CAL_CLOCK_GATE_EN | TM_UNUSED_30_18 | | | | | | |
| R/W-0h | R-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_30_18 | | | | | | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | TM_PREAMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_ITER_WAIT_TIME | | | | | | | TM_PREAMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-239. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31 | TM_DIAG_CAL_CLOCK_GATE_EN | R/W | 0h | While running diagnostic calibrations, this acts as calibration's clock gate enable Enable = 1 |
| 30-18 | TM_UNUSED_30_18 | R | 0h | RESERVED |
| 17 | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode wait time between two codes selection |
| 16-9 | TM_PREAMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode wait time between two codes |
| 8 | TM_PREAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode initial wait time selection - Select signal to choose between the one from software way or the functional one Functional value gets decided internally based on the "psm_clock_freq" input to Data-Lane |
| 7-0 | TM_PREAMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode initial wait time - "init_value" considered when selected to choose it via software way |

11.120 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4 Register (Offset = 318h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4 is shown in [Figure 11-119](#) and described in [Table 11-241](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg2

Table 11-240.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0318h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0318h |

Figure 11-119. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|-----------------------------|-----------------------|-------------------|---------------|--------------------------|-------------------------|-----------------|
| UNUSED | | | | | TM_PREAMP_ANA_CAL_EN_SEL | TM_PREAMP_ANA_CAL_EN | TM_UNUSED_24_18 |
| R-0h | | | | | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_24_18 | | | | | | TM_PREAMP_CAL_CODE_TUNE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_CODE_TUNE | TM_PREAMP_CAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_OVERRIDE_CODE | TM_PREAMP_CAL_OVERRIDE_EN | TM_PREAMP_CAL_RUN_SEL | TM_PREAMP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-241. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26 | TM_PREAMP_ANA_CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 25 | TM_PREAMP_ANA_CAL_EN | R/W | 0h | test mode analog calibration enable |
| 24-18 | TM_UNUSED_24_18 | R | 0h | RESERVED |
| 17-15 | TM_PREAMP_CAL_CODE_TUNE | R/W | 0h | final preamp cal code tune value |
| 14-7 | TM_PREAMP_CAL_OVERRIDE_CODE | R/W | 0h | preamp calibration override code |
| 6 | TM_PREAMP_CAL_OVERRIDE_EN | R/W | 0h | preamp calibration code override enable |
| 5 | TM_PREAMP_CAL_RUN_SEL | R/W | 0h | test mode calibration run selection |

Table 11-241. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---------------------------|
| 4 | TM_PREAMP_CAL_RUN | R/W | 0h | test mode calibration run |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.121 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT5 Register (Offset = 31Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT5 is shown in [Figure 11-120](#) and described in [Table 11-243](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg1

Table 11-242.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 031Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 031Ch |

Figure 11-120. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT5 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_DCC_COM P_CAL_ITER_ WAIT_TIME_E N | TM_DCC_COM P_CAL_ITER_ WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_DCC_COM P_CAL_INIT_W AIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-243. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration iteration time enable |
| 16-9 | TM_DCC_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode dcc comp calibration iteration time |
| 8 | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration initial wait time enable |
| 7-0 | TM_DCC_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode dcc comp calibration initial wait time |

11.122 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6 Register (Offset = 320h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6 is shown in [Figure 11-121](#) and described in [Table 11-245](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg2

Table 11-244.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0320h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0320h |

Figure 11-121. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6 Register

| | | | | | | | |
|---------------------------------------|-------------------------------------|---------------------------------|------------------------------------|--------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_DCC_COM P_ANA_CAL_E N_SEL | TM_DCC_COM P_ANA_CAL_E N | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_CODE_TUNE | | | TM_DCC_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_OVER RIDE_CODE | TM_DCC_COM P_CAL_OVER RIDE_EN | TM_DCC_COM P_CAL_RUN_S EL | TM_DCC_COM P_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-245. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_DCC_COMP_ANA_C AL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_DCC_COMP_ANA_C AL_EN | R/W | 0h | test mode dcc comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_DCC_COMP_CAL_C ODE_TUNE | R/W | 0h | test mode dcc comp calibration code tune value |
| 12-7 | TM_DCC_COMP_CAL_O VERRIDE_CODE | R/W | 0h | test mode dcc comp calibration code overirde |
| 6 | TM_DCC_COMP_CAL_O VERRIDE_EN | R/W | 0h | test mode dcc comp calibration override code enable |
| 5 | TM_DCC_COMP_CAL_R UN_SEL | R/W | 0h | dcc comp calibration run selection |
| 4 | TM_DCC_COMP_CAL_R UN | R/W | 0h | dcc comp calibration test mode run |

Table 11-245. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.123 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT7 Register (Offset = 324h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT7 is shown in [Figure 11-122](#) and described in [Table 11-247](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg1

Table 11-246.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0324h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0324h |

Figure 11-122. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT7 Register

| | | | | | | | |
|----------------------------------|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME_E N | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_MIXER_CO MP_CAL_INIT _WAIT_TIME_E N |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-247. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration iteration time enable |
| 16-9 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode mixer comp calibration iteration time |
| 8 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration initial wait time enable |
| 7-0 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode mixer comp calibration initial wait time |

11.124 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8 Register (Offset = 328h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8 is shown in [Figure 11-123](#) and described in [Table 11-249](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg2

Table 11-248.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0328h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0328h |

Figure 11-123. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8 Register

| | | | | | | | |
|---|---------------------------------------|-----------------------------------|--------------------------------------|----------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_MIXER_CO MP_ANA_CAL_ EN_SEL | TM_MIXER_CO MP_ANA_CAL_ EN | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_CODE_TUNE | | | TM_MIXER_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_CO MP_CAL_OVE RRIDE_CODE | TM_MIXER_CO MP_CAL_OVE RRIDE_EN | TM_MIXER_CO MP_CAL_RUN _SEL | TM_MIXER_CO MP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-249. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_MIXER_COMP_ANA_ CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_MIXER_COMP_ANA_ CAL_EN | R/W | 0h | test mode mixer comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_MIXER_COMP_CAL_ CODE_TUNE | R/W | 0h | test mode mixer comp calibration code tune value |
| 12-7 | TM_MIXER_COMP_CAL_ OVERRIDE_CODE | R/W | 0h | test mode mixer comp calibration code override |
| 6 | TM_MIXER_COMP_CAL_ OVERRIDE_EN | R/W | 0h | test mode mixer comp calibration override code enable |
| 5 | TM_MIXER_COMP_CAL_ RUN_SEL | R/W | 0h | mixer comp calibration run selection |
| 4 | TM_MIXER_COMP_CAL_ RUN | R/W | 0h | mixer comp calibration test mode run |

Table 11-249. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT8 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.125 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT9 Register (Offset = 32Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT9 is shown in [Figure 11-124](#) and described in [Table 11-251](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg1

Table 11-250.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT9
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 032Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 032Ch |

Figure 11-124. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT9 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-251. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_POS_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | posedge sampler calibration iteration time between codes |
| 7-0 | TM_POS_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | posedge sampler calibration initial wait time |

11.126 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10 Register (Offset = 330h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10 is shown in [Figure 11-125](#) and described in [Table 11-253](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg2

Table 11-252.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0330h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0330h |

Figure 11-125. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_MCAL_OVERRIDE_EN | TM_POS_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_PCAL_OVERRIDE_CODE | TM_POS_SAMP_PCAL_OVERRIDE_EN | TM_POS_SAMP_CAL_RUN | TM_POS_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-253. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode iteration wait time enable |
| 30 | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_POS_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override mcal_code |
| 15 | TM_POS_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration mcal_code override en |
| 14-7 | TM_POS_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override pcal_code |
| 6 | TM_POS_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration pcal_code override en |
| 5 | TM_POS_SAMP_CAL_RUN | R/W | 0h | posedge sampler calibration test mode run |

Table 11-253. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT10 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_POS_SAMP_CAL_R UN_SEL | R/W | 0h | posedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.127 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT11 Register (Offset = 334h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT11 is shown in [Figure 11-126](#) and described in [Table 11-255](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg3

Table 11-254.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT11
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0334h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0334h |

Figure 11-126. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT11 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_POS_SAMP_ANA_CAL_EN_SEL | TM_POS_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_POS_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-255. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_POS_SAMP_ANA_CAL_EN_SEL | R/W | 0h | posedge sampler calibration analog calib enable selection |
| 8 | TM_POS_SAMP_ANA_CAL_EN | R/W | 0h | posedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_POS_SAMP_CAL_CODE_TUNE | R/W | 0h | posedge sampler calibration tune code |

11.128 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT12 Register (Offset = 338h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT12 is shown in [Figure 11-127](#) and described in [Table 11-257](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg1

Table 11-256.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT12
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0338h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0338h |

Figure 11-127. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT12 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-257. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | negedge sampler calibration iteration time between codes |
| 7-0 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | negedge sampler calibration initial wait time |

11.129 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13 Register (Offset = 33Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13 is shown in [Figure 11-128](#) and described in [Table 11-259](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg2

Table 11-258.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 033Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 033Ch |

Figure 11-128. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_MCAL_OVERRIDE_EN | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_PCAL_OVERRIDE_CODE | TM_NEG_SAMP_PCAL_OVERRIDE_EN | TM_NEG_SAMP_CAL_RUN | TM_NEG_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-259. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode iteration wait time enable |
| 30 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_NEG_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override mcal_code |
| 15 | TM_NEG_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration mcal_code override en |
| 14-7 | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override pcal_code |
| 6 | TM_NEG_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration pcal_code override en |
| 5 | TM_NEG_SAMP_CAL_RUN | R/W | 0h | negedge sampler calibration test mode run |

Table 11-259. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT13 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_NEG_SAMP_CAL_R UN_SEL | R/W | 0h | negedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.130 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT14 Register (Offset = 340h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT14 is shown in [Figure 11-129](#) and described in [Table 11-261](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg3

Table 11-260.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT14
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0340h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0340h |

Figure 11-129. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT14 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_NEG_SAMP_ANA_CAL_EN_SEL | TM_NEG_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_NEG_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-261. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_NEG_SAMP_ANA_CAL_EN_SEL | R/W | 0h | negedge sampler calibration analog calib enable selection |
| 8 | TM_NEG_SAMP_ANA_CAL_EN | R/W | 0h | negedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_NEG_SAMP_CAL_CODE_TUNE | R/W | 0h | negedge sampler calibration tune code |

11.131 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT15 Register (Offset = 344h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT15 is shown in [Figure 11-130](#) and described in [Table 11-263](#).

Return to [Summary Table](#).

skew_cal_fsm_reg1

Table 11-262.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT15
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0344h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0344h |

Figure 11-130. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT15 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|----|----|--------------------------------|------------------------------------|-----------------------------------|------------------------------|------------------------------|
| UNUSED | | | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | | | | | TM_SKEW_CAL_FPHASE_WAIT_TIME | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_FPHASE_WAIT_TIME | | | | | | | TM_SKEW_CAL_TIMER_INIT_COUNT |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-263. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | R/W | 0h | skew calibration analog max saturation test mode enable |
| 27 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | R/W | 0h | skew calibration analog max saturation selection |
| 26-18 | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | R/W | 0h | skew calibration fast phase long wait time |
| 17-9 | TM_SKEW_CAL_FPHASE_WAIT_TIME | R/W | 0h | skew calibration fast phase wait time |
| 8-0 | TM_SKEW_CAL_TIMER_INIT_COUNT | R/W | 0h | skew calibration initial wait time |

11.132 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT16 Register (Offset = 348h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT16 is shown in [Figure 11-131](#) and described in [Table 11-265](#).

Return to [Summary Table](#).

skew_cal_fsm_reg2

Table 11-264.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT16
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0348h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0348h |

Figure 11-131. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT16 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|------------------------------------|------------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | |
| R-0h | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_ACC_CODE_MIN_VALUE | | | | | | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | TM_SKEW_CAL_SPHASE_WAIT_TIME |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_SPHASE_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-265. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26-19 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | R/W | 0h | skew calibration delay code test mode max value |
| 18 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | R/W | 0h | skew calibration max code test reg selection |
| 17-10 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | R/W | 0h | skew calibration delay code test mode min value |
| 9 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | R/W | 0h | skew calibration min code test reg selection |
| 8-0 | TM_SKEW_CAL_SPHASE_WAIT_TIME | R/W | 0h | skew calibration slow phase wait time |

11.133 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT17 Register (Offset = 34Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT17 is shown in [Figure 11-132](#) and described in [Table 11-267](#).

Return to [Summary Table](#).

skew_cal_fsm_reg3

Table 11-266.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT17
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 034Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 034Ch |

Figure 11-132. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT17 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_DESKEW_START_CODE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-267. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|-------------------------------------|
| 31-8 | UNUSED | R | 0h | RESERVED |
| 7-0 | TM_SKEW_CAL_DESKEW_START_CODE | R/W | 0h | skew calibration initial start code |

11.134 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT18 Register (Offset = 350h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT18 is shown in [Figure 11-133](#) and described in [Table 11-269](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg1

Table 11-268.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT18
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0350h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0350h |

Figure 11-133. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT18 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_TIMER_ITER_COUNT | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_TIMER_ITER_COUNT | | | | | | TM_DUCY_CORR_TIMER_INIT_COUNT | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CORR_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-269. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-9 | TM_DUCY_CORR_TIMER_ITER_COUNT | R/W | 0h | duty cycle correction iteration wait time specified in this register will be considered when a non-zero value is specified here |
| 8-0 | TM_DUCY_CORR_TIMER_INIT_COUNT | R/W | 0h | duty cycle correction initial wait time specified in this register will be considered when a non-zero value is specified here |

11.135 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT19 Register (Offset = 354h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT19 is shown in [Figure 11-134](#) and described in [Table 11-271](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg2

Table 11-270.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT19
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0354h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0354h |

Figure 11-134. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT19 Register

| | | | | | | | |
|---------------------------------|-------------------------------------|-----------------------------|-------------------------------------|---------------------------------|----|---------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_ACC_CODE_MAX_VALUE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_ACC_CODE_MAX_VALUE | | | TM_DUCY_CORR_ACC_CODE_MAX_VALUE_SEL | TM_DUCY_CORR_ACC_CODE_MIN_VALUE | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CORR_ACC_CODE_MIN_VALUE | TM_DUCY_CORR_ACC_CODE_MIN_VALUE_SEL | TM_DUCY_CORR_ACC_START_CODE | | | | TM_DUCY_CORR_ACC_START_CODE_SEL | |
| R/W-0h | R/W-0h | R/W-0h | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-271. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-13 | TM_DUCY_CORR_ACC_CODE_MAX_VALUE | R/W | 0h | duty cycle correction test mode max value |
| 12 | TM_DUCY_CORR_ACC_CODE_MAX_VALUE_SEL | R/W | 0h | duty cycle correction test mode max value selection |
| 11-7 | TM_DUCY_CORR_ACC_CODE_MIN_VALUE | R/W | 0h | duty cycle correction test mode min value |
| 6 | TM_DUCY_CORR_ACC_CODE_MIN_VALUE_SEL | R/W | 0h | duty cycle correction test mode min value selection |
| 5-1 | TM_DUCY_CORR_ACC_START_CODE | R/W | 0h | duty cycle correction test mode start code |
| 0 | TM_DUCY_CORR_ACC_START_CODE_SEL | R/W | 0h | duty cycle correction test mode start code selection |

11.136 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20 Register (Offset = 358h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20 is shown in [Figure 11-135](#) and described in [Table 11-273](#).

Return to [Summary Table](#).

skew_cal_avg_reg1

Table 11-272.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0358h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0358h |

Figure 11-135. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------------|----------------------------------|---------------------|----|----|---------------------------------|------------------------------------|------------------------------------|
| TM_ANA_DES KEW_DCC_EN | TM_ANA_DES KEW_DCC_EN _SEL | TM_DCC_CODE_TUNE | | | TM_DCC_COD E_OVERRIDE_ EN | TM_DCC_CODE_OVERRIDE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DCC_CODE_OVERRIDE | | TM_DESKEW_CODE_TUNE | | | | | TM_DESKEW_ CODE_OVERR IDE_EN |
| R/W-0h | | R/W-0h | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_CODE_OVERRIDE | | | | | | TM_PROC_TIM ER_LOAD_VAL | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PROC_TIMER_LOAD_VAL | | | | | | TM_PROC_TIM ER_LOAD_VAL _SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-273. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31 | TM_ANA_DESKEW_DCC_EN | R/W | 0h | test mode analog deskew enable |
| 30 | TM_ANA_DESKEW_DCC_EN_SEL | R/W | 0h | test mode deskew analog enable selection |
| 29-27 | TM_DCC_CODE_TUNE | R/W | 0h | duty cycle correction code tune |
| 26 | TM_DCC_CODE_OVERRIDE_EN | R/W | 0h | duty cycle correction code override enable |
| 25-22 | TM_DCC_CODE_OVERRIDE | R/W | 0h | duty cycle correction override code |
| 21-17 | TM_DESKEW_CODE_TUNE | R/W | 0h | skew calibration delay line code tune |
| 16 | TM_DESKEW_CODE_OVERRIDE_EN | R/W | 0h | skew calibration delay code override enable |
| 15-9 | TM_DESKEW_CODE_OVERRIDE | R/W | 0h | skew calibration delay line override code |

Table 11-273. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 8-1 | TM_PROC_TIMER_LOAD_VAL | R/W | 0h | skew calibration process time test mode value |
| 0 | TM_PROC_TIMER_LOAD_VAL_SEL | R/W | 0h | skew calibration process time test mode value selection |

11.137 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT21 Register (Offset = 35Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT21 is shown in [Figure 11-136](#) and described in [Table 11-275](#).

[Return to Summary Table.](#)

skew_cal_avg_reg2

Table 11-274.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT21
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 035Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 035Ch |

Figure 11-136. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT21 Register

| | | | | | | | |
|-----------------------------|----|----|----|----|----|---------------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG_LEN_TMR_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG_LEN_TMR_LOAD_VAL | | | | | | TM_AVG2AVG_LEN_TMR_LOAD_VAL_SEL | TM_DCC_ACC_LEN_TMR_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC_LEN_TMR_LOAD_VAL | | | | | | TM_DCC_ACC_LEN_TMR_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-275. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG_LEN_TMR_LOAD_VAL | R/W | 0h | delay line code averaging to dcc code averaging wait time |
| 9 | TM_AVG2AVG_LEN_TMR_LOAD_VAL_SEL | R/W | 0h | delay line code averaging to dcc code averaging wait time selection |
| 8-1 | TM_DCC_ACC_LEN_TMR_LOAD_VAL | R/W | 0h | total number of dcc codes to be taken for averaging in test mode |
| 0 | TM_DCC_ACC_LEN_TMR_LOAD_VAL_SEL | R/W | 0h | test mode selection value for test mode number of dcc codes under averaging |

11.138 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT22 Register (Offset = 360h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT22 is shown in [Figure 11-137](#) and described in [Table 11-277](#).

Return to [Summary Table](#).

skew_cal_avg_reg3

Table 11-276.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT22
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0360h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0360h |

Figure 11-137. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT22 Register

| | | | | | | | |
|--|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ DONE_LEN TIMER_LOAD_ VAL_SEL | TM_DESKEW_ ACC_LEN G_TIMER_LOAD_ VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ ACC_LEN G_TIMER_LOAD_ VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-277. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | R/W | 0h | after skew calibration is done, length of wait timer |
| 9 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | test mode selection value for length of wait time after deskew |
| 8-1 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | R/W | 0h | number of deskew dealy codes to be taken for averaging |
| 0 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | tets mode selction for test mode number of delay line codes for averaging |

11.139 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT23 Register (Offset = 364h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT23 is shown in [Figure 11-138](#) and described in [Table 11-279](#).

Return to [Summary Table](#).

skew_cal_avg_reg4

Table 11-278.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT23
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0364h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0364h |

Figure 11-138. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT23 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-----------------------------------|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG_RES_TIMER_LOAD_VAL | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | TM_DCC_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC_RES_TIMER_LOAD_VAL | | | | | | | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-279. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging to deskew averaging wait time in test mode |
| 9 | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging to deskew averaging wait time |
| 8-1 | TM_DCC_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging wait time in test mode |
| 0 | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging wait time |

11.140 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT24 Register (Offset = 368h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT24 is shown in [Figure 11-139](#) and described in [Table 11-281](#).

Return to [Summary Table](#).

skew_cal_avg_reg5

Table 11-280.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT24
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0368h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0368h |

Figure 11-139. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT24 Register

| | | | | | | | |
|-----------------------------------|----|----|----|----|----|---------------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-281. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew done wait time in test mode |
| 9 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selction of resolution time of deskew done wait time in test mode |
| 8-1 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew averaging wait time in test mode |
| 0 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | tets mode selection of resolution time of deskew averaging wait time in test mode |

11.141 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT25 Register (Offset = 36Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT25 is shown in [Figure 11-140](#) and described in [Table 11-283](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG0

Table 11-282.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT25
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 036Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 036Ch |

Figure 11-140. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-283. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT0 | R | 0h | RESERVED |

11.142 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT26 Register (Offset = 370h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT26 is shown in [Figure 11-141](#) and described in [Table 11-285](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG1

Table 11-284.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT26
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0370h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0370h |

Figure 11-141. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-285. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT1 | R | 0h | RESERVED |

11.143 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT27 Register (Offset = 374h) [reset = 0A000018h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT27 is shown in [Figure 11-142](#) and described in [Table 11-287](#).

Return to [Summary Table](#).

bist_config_reg1

Table 11-286.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT27
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0374h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0374h |

Figure 11-142. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT27 Register

| | | | | | | | |
|---------------------|----|----|--------------|----|-------------|-----------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_IDLE_TIME_LENGTH | | | | | | | |
| R/W-Ah | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_MODE | | | TM_PRBS_MODE | | TM_UNUSED_2 | TM_FREEZE | TM_BIST_EN |
| R/W-0h | | | R/W-3h | | R-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-287. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-24 | TM_IDLE_TIME_LENGTH | R/W | Ah | BIST_IDLE_TIME |
| 23-8 | TM_UNUSED_23_8 | R | 0h | RESERVED |
| 7-5 | TM_TEST_MODE | R/W | 0h | PRBS mode - when set to '1' PRBS mode is selected |
| 4-3 | TM_PRBS_MODE | R/W | 3h | BIST PRBS MODE 9 when 0x0 |
| 2 | TM_UNUSED_2 | R | 0h | RESERVED |
| 1 | TM_FREEZE | R/W | 0h | Freeze the LFSR contents after every packet or frame |
| 0 | TM_BIST_EN | R/W | 0h | Enable signal for pattern checker |

11.144 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT28 Register (Offset = 378h) [reset = DECDBCABh]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT28 is shown in [Figure 11-143](#) and described in [Table 11-289](#).

Return to [Summary Table](#).

bist_config_reg2

Table 11-288.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT28
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0378h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0378h |

Figure 11-143. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_TEST_PAT4 | | | | | | | | TM_TEST_PAT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_PAT2 | | | | | | | | TM_TEST_PAT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-289. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-24 | TM_TEST_PAT4 | R/W | DEh | User registers to specify the BIST data4 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 23-16 | TM_TEST_PAT3 | R/W | CDh | User registers to specify the BIST data3 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 15-8 | TM_TEST_PAT2 | R/W | BCh | User registers to specify the BIST data2 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 7-0 | TM_TEST_PAT1 | R/W | ABh | User registers to specify the BIST data1 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |

11.145 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT29 Register (Offset = 37Ch) [reset = 28h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT29 is shown in [Figure 11-144](#) and described in [Table 11-291](#).

Return to [Summary Table](#).

bist_config_reg3

Table 11-290.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT29
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 037Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 037Ch |

Figure 11-144. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT29 Register

| | | | | | | | |
|-----------------|----|----|---------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_CLEAR_BIST | TM_UNUSED_27_12 | | | |
| R-0h | | | R/W-0h | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_27_12 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_27_12 | | | | TM_PKT_LENGTH | | | |
| R-0h | | | | R/W-28h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PKT_LENGTH | | | | | | | |
| R/W-28h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-291. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_CLEAR_BIST | R/W | 0h | Setting this will clear all the BIST related flags and counters |
| 27-12 | TM_UNUSED_27_12 | R | 0h | RESERVED |
| 11-0 | TM_PKT_LENGTH | R/W | 28h | Based on the default_mode design will consider the run-length from design or the programmed value specified here |

11.146 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT30 Register (Offset = 380h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT30 is shown in [Figure 11-145](#) and described in [Table 11-293](#).

Return to [Summary Table](#).

bist_config_reg4

Table 11-292.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT30
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0380h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0380h |

Figure 11-145. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT30 Register

| | | | | | | | |
|--------|----|----|----|----|----|---------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | TM_LPRX_BIS T_EN | TM_HSRX_BIS T_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-293. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-2 | UNUSED | R | 0h | RESERVED |
| 1 | TM_LPRX_BIST_EN | R/W | 0h | LPRX BIST is enabled - rxda_lprx_bist_en - When '1', LP BIST is enabled |
| 0 | TM_HSRX_BIST_EN | R/W | 0h | HSRX BIST is enabled - rxda_hsrx_bist_en - when '1', HS BIST is enabled |

11.147 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT31 Register (Offset = 384h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT31 is shown in [Figure 11-146](#) and described in [Table 11-295](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG1

Table 11-294.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT31
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0384h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0384h |

Figure 11-146. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-295. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT1 | R | 0h | RESERVED |

11.148 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT32 Register (Offset = 388h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT32 is shown in [Figure 11-147](#) and described in [Table 11-297](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG2

Table 11-296.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT32
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0388h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0388h |

Figure 11-147. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-297. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT2 | R | 0h | RESERVED |

11.149 DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT2 Register (Offset = 38Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT2 is shown in [Figure 11-148](#) and described in [Table 11-299](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-298.
DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 038Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 038Ch |

Figure 11-148. DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-299. DPHY_RX_VBUS2APB_DL1_RX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | ANA_READ_TBIT0 | R | 0h | Analog read register 0 |

11.150 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT33 Register (Offset = 390h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT33 is shown in [Figure 11-149](#) and described in [Table 11-301](#).

Return to [Summary Table](#).

deserialiser_fsm_status

Table 11-300.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT33
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0390h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0390h |

Figure 11-149. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|------------------|----|-------------|----|----|----|-------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_PPI_CUR_STATE | | | | | | TM_CTRL_CUR_STATE | | | |
| R-0h | | | | | | R-0h | | | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_CTRL_CUR_STATE | | | | | | | | TM_SYNC_PKT | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-301. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-26 | UNUSED | R | 0h | RESERVED |
| 25-18 | TM_PPI_CUR_STATE | R | 0h | Current State of the SYNC detection FSM during the HS data receive mode or skew calibration mode |
| 17-8 | TM_CTRL_CUR_STATE | R | 0h | current state status of HS receive FSM |
| 7-0 | TM_SYNC_PKT | R | 0h | Status of received SYNC packet |

11.151 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT34 Register (Offset = 394h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT34 is shown in [Figure 11-150](#) and described in [Table 11-303](#).

Return to [Summary Table](#).

lp_status

Table 11-302.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT34
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0394h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0394h |

Figure 11-150. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT34 Register

| | | | | | | | |
|--------------------|----|--------------|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | TM_LP_RX_CUR_STATE | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_LP_RX_CUR_STATE | | TM_LP_STATUS | | | | | |
| R-0h | | R-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-303. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-19 | UNUSED | R | 0h | RESERVED |
| 18-14 | TM_LP_RX_CUR_STATE | R | 0h | Current state of LP receiver FSM |
| 13-8 | TM_LP_STATUS | R | 0h | Status of DP,DN pins of LPRX, LPCD, ULPRX respectively |
| 7-0 | UNUSED_7_0 | R | 0h | RESERVED |

11.152 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT35 Register (Offset = 398h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT35 is shown in [Figure 11-151](#) and described in [Table 11-305](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_READ_REG0

Table 11-304.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT35
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0398h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0398h |

Figure 11-151. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-305. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.153 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36 Register (Offset = 39Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36 is shown in [Figure 11-152](#) and described in [Table 11-307](#).

Return to [Summary Table](#).

dcc_mixer_comparator_calibration_stat

Table 11-306.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 039Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 039Ch |

Figure 11-152. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36 Register

| | | | | | | | |
|--------------------------|--------------------------|---------------------|----|----|----|---------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_MIX_COM P_ANA_RESP | TM_MIX_COMP_CALCODE | | | | TM_MIX_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIX_COM P_CAL_DONE | TM_DCC_COM P_ANA_RESP | TM_DCC_COMP_CALCODE | | | | TM_DCC_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_DONE | TM_CALIB_CTRL_CUR_STATE | | | | | TM_CUR_DRX _CAL_DONE | |
| R-0h | R-0h | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-307. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_MIX_COMP_ANA_RESP | R | 0h | Mixer comparator analog response |
| 21-17 | TM_MIX_COMP_CALCODE | R | 0h | Mixer comparator calibration code |
| 16 | TM_MIX_COMP_CAL_NO_RESP | R | 0h | Mixer comparator calibration has no response from analog |
| 15 | TM_MIX_COMP_CAL_DONE | R | 0h | Mixer comparator calibration is done properly |
| 14 | TM_DCC_COMP_ANA_RESP | R | 0h | Duty Cycle Comparator analog response |
| 13-9 | TM_DCC_COMP_CALCODE | R | 0h | Duty cycle corrector comparator calibration code |
| 8 | TM_DCC_COMP_CAL_NO_RESP | R | 0h | Duty cycle corrector comparator calibration has no response from analog |

Table 11-307. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT36 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7 | TM_DCC_COMP_CAL_DONE | R | 0h | Duty cycle corrector comparator calibration is done properly |
| 6-1 | TM_CALIB_CTRL_CUR_STATE | R | 0h | If struck, indicates calibration FSM current state |
| 0 | TM_CUR_DRX_CAL_DONE | R | 0h | Current DRX DPHY_RX_VBUS2APB_LANE calibrations are done |

11.154 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37 Register (Offset = 3A0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37 is shown in [Figure 11-153](#) and described in [Table 11-309](#).

Return to [Summary Table](#).

preamp_cal_status_reg1

Table 11-308.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 03A0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 03A0h |

Figure 11-153. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------|----|-----------------------------|-----------------------------|---------------------------------|--------------------------|-----------------------------------|
| TM_ANA_RESP_STAT | TM_PREAMP_STAT_ANA_CAL_CODE | | | | | | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE |
| R-0h | R-0h | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | | | | | | | TM_PREAMP_STAT_NCAL_PREAMP_CODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_STAT_NCAL_PREAMP_CODE | | | | | TM_PREAMP_STAT_PCAL_PREAMP_CODE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_STAT_PCAL_PREAMP_CODE | | | TM_PREAMP_STAT_NCAL_NO_RESP | TM_PREAMP_STAT_PCAL_NO_RESP | TM_PREAMP_STAT_NCAL_DONE | TM_PREAMP_STAT_PCAL_DONE | TM_PREAMP_STAT_CAL_DONE |
| R-0h | | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-309. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31 | TM_ANA_RESP_STAT | R | 0h | current analog or test mode response for which calibration is happening |
| 30-25 | TM_PREAMP_STAT_ANA_CAL_CODE | R | 0h | code going to analog |
| 24-17 | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | R | 0h | code decided to send to analog before tune |
| 16-11 | TM_PREAMP_STAT_NCAL_PREAMP_CODE | R | 0h | calib code in posedge_data run |
| 10-5 | TM_PREAMP_STAT_PCAL_PREAMP_CODE | R | 0h | calib code in negedge_data run |
| 4 | TM_PREAMP_STAT_NCAL_NO_RESP | R | 0h | negedge_data run has no response |
| 3 | TM_PREAMP_STAT_PCAL_NO_RESP | R | 0h | posedge_data run has no response |
| 2 | TM_PREAMP_STAT_NCAL_DONE | R | 0h | negedge_data cal run is done |

Table 11-309. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT37 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|------------------------------|
| 1 | TM_PREAMP_STAT_PCA L_DONE | R | 0h | posedge_data cal run is done |
| 0 | TM_PREAMP_STAT_CAL _DONE | R | 0h | preamp calibration is done |

11.155 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38 Register (Offset = 3A4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38 is shown in [Figure 11-154](#) and described in [Table 11-311](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg1

Table 11-310.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03A4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03A4h |

Figure 11-154. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38 Register

| | | | | | | | |
|---------------------------------|----|----|---------------------------|---------------------------------|------------------------------|---------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_POS_SAMP_STAT_CAL_DONE | TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_POS_SAMP_STAT_UP_CAL_CODE | TM_POS_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_UP_CAL_CODE | | | | | | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | TM_POS_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-311. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_POS_SAMP_STAT_SAMP_STAT_CAL_DONE | R | 0h | posedge sampler calibration is done |
| 19-11 | TM_POS_SAMP_STAT_FINAL_CAL_CODE | R | 0h | posedge sampler calibration final code |
| 10 | TM_POS_SAMP_STAT_CODE_TYPE | R | 0h | code type that is changing for posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-311. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT38 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_POS_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.156 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT39 Register (Offset = 3A8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT39 is shown in [Figure 11-155](#) and described in [Table 11-313](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg2

Table 11-312.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT39
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03A8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03A8h |

Figure 11-155. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT39 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|--|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_POS_SAMP P_ANA_CAL_R ESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_POS_SAMP P_STAT_ANA_ CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_POS_SAMP_STAT_DOWN_ CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_POS_SAMP P_STAT_NO_D OWN_CAL_RE SP | TM_POS_SAMP P_STAT_DOW N_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-313. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_POS_SAMP_ANA_CAL_RESP | R | 0h | test mode status of posedge sampler |
| 23-17 | TM_POS_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to posedge sampler |
| 16-10 | TM_POS_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_POS_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.157 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40 Register (Offset = 3ACh) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40 is shown in [Figure 11-156](#) and described in [Table 11-315](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg1

Table 11-314.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03ACh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03ACh |

Figure 11-156. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40 Register

| | | | | | | | |
|---------------------------------|----|----|---|---------------------------------|--------------------------------|------------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_NEG_SAMP_STAT_CODE _TYPE | TM_NEG_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_UP_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_UP CAL_RESP | TM_NEG_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-315. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | R | 0h | negedge sampler calibration is done |
| 19-11 | TM_NEG_SAMP_STAT_FINAL CAL_CODE | R | 0h | negedge sampler calibration final code |
| 10 | TM_NEG_SAMP_STAT_CODE _TYPE | R | 0h | code type that is changing for negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_UP CAL_CODE | R | 0h | up check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_UP CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-315. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT40 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_NEG_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.158 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT41 Register (Offset = 3B0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT41 is shown in [Figure 11-157](#) and described in [Table 11-317](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg2

Table 11-316.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT41
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 03B0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 03B0h |

Figure 11-157. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT41 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_NEG_SAMP_ANA_CAL_RESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_NEG_SAMP_STAT_ANA_CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | TM_NEG_SAMP_STAT_DOWN_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-317. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT41 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_NEG_SAMP_ANA_CAL_RESP | R | 0h | test mode status of negedge sampler |
| 23-17 | TM_NEG_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to negedge sampler |
| 16-10 | TM_NEG_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_NEG_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.159 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42 Register (Offset = 3B4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42 is shown in [Figure 11-158](#) and described in [Table 11-319](#).

Return to [Summary Table](#).

skew_cal_fsm_status_reg1

Table 11-318.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03B4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03B4h |

Figure 11-158. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42 Register

| | | | | | | | |
|------------------------------------|----|-------------------------------------|-------------------------|----|-----------------------------------|-----------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_DESKEW_DCC_CUR_STATE | | | | |
| R-0h | | | R-0h | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_CUR_STATE | | TM_DESKEW_DCC_INIT_MIXER_VALUE | TM_SP_FIRST_TRIP_CODE | | | | |
| R-0h | | R-0h | R-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SP_FIRST_TRIP_CODE | | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | | | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | |
| R-0h | | R-0h | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | | | | | | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | |
| R-0h | | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-319. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28-22 | TM_DESKEW_DCC_CUR_STATE | R | 0h | Duty cycle correction logic current state |
| 21 | TM_DESKEW_DCC_INIT_MIXER_VALUE | R | 0h | Duty cycle correction initial comparator value |
| 20-14 | TM_SP_FIRST_TRIP_CODE | R | 0h | slow phase first trip code |
| 13-10 | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | R | 0h | current state of the deskew FSM |
| 9 | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | R | 0h | if asserted, deskew FSM has gone into max saturation second time |
| 8 | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | R | 0h | if asserted, deskew FSM has got saturated once |

Table 11-319. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT42 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------------|------|-------|--------------------------------------|
| 7-1 | TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | R | 0h | deskew FSM fast phase trip code |
| 0 | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | R | 0h | deskew algorithm mixer initial value |

11.160 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT43 Register (Offset = 3B8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT43 is shown in [Figure 11-159](#) and described in [Table 11-321](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg1

Table 11-320.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT43
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03B8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03B8h |

Figure 11-159. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT43 Register

| | | | | | | | |
|-------------------------------------|----|----------------------------------|-------------------------------------|----|-------------------------------|--------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | | | | | | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | |
| R-0h | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DCC_AVG_ANA_DCC_CODE | | | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | | | |
| R-0h | | | R-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | | | TM_DESKEW_DCC_AVG_DONE_DESKEW | | TM_DESKEW_DCC_AVG_DONE_DCC |
| R-0h | | R-0h | | | R-0h | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-321. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT43 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-17 | TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | R | 0h | final code going to delay line |
| 16-13 | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | R | 0h | final code going to duty cycle corrector |
| 12-6 | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | R | 0h | delay line code before tuning |
| 5-2 | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | R | 0h | duty code before tuning |
| 1 | TM_DESKEW_DCC_AVG_DONE_DESKEW | R | 0h | skew calibration is done |
| 0 | TM_DESKEW_DCC_AVG_DONE_DCC | R | 0h | duty cycle correction is done |

11.161 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT44 Register (Offset = 3BCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT44 is shown in [Figure 11-160](#) and described in [Table 11-323](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg2

Table 11-322.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT44
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03BCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03BCh |

Figure 11-160. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT44 Register

| | | | | | | | | | | | | | | | |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | |
| R-0h | | | | | | | | | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-323. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT44 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-17 | UNUSED | R | 0h | RESERVED |
| 16-0 | TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | R | 0h | current state of deskew_dcc_averaging FSM |

11.162 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT45 Register (Offset = 3C0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT45 is shown in [Figure 11-161](#) and described in [Table 11-325](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG0

Table 11-324.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT45
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03C0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03C0h |

Figure 11-161. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT45 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-325. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT45 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT0 | R | 0h | RESERVED |

11.163 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT46 Register (Offset = 3C4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT46 is shown in [Figure 11-162](#) and described in [Table 11-327](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG1

Table 11-326.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT46
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03C4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03C4h |

Figure 11-162. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT46 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-327. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT46 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT1 | R | 0h | RESERVED |

11.164 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT47 Register (Offset = 3C8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT47 is shown in [Figure 11-163](#) and described in [Table 11-329](#).

Return to [Summary Table](#).

bist_status_reg1

Table 11-328.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT47
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03C8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03C8h |

Figure 11-163. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT47 Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| W_PAT_CHE_ERROR_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W_PAT_CHE_PKT_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-329. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT47 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-16 | W_PAT_CHE_ERROR_COUNT | R | 0h | BIST Pattern checker error count's live status can be obtained by poling this field |
| 15-0 | W_PAT_CHE_PKT_COUNT | R | 0h | BIST packet count's live status can be obtained by poling this field |

11.165 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT48 Register (Offset = 3CCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT48 is shown in [Figure 11-164](#) and described in [Table 11-331](#).

Return to [Summary Table](#).

bist_status_reg2

Table 11-330.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT48
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03CCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03CCh |

Figure 11-164. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT48 Register

| | | | | | | | |
|--------|----|----|----|----|------------------|--------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | W_BIST_ERRO R | R_PAT_CHE_S YNC | W_DRX_BIST_ PASS |
| R-0h | | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-331. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT48 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-3 | UNUSED | R | 0h | RESERVED |
| 2 | W_BIST_ERROR | R | 0h | Status of HS data path comparision outcome, '0' means pass |
| 1 | R_PAT_CHE_SYNC | R | 0h | Informs BIST Pattern checker is not in sync with pattern generator - Check polarity |
| 0 | W_DRX_BIST_PASS | R | 0h | Entire DRX has passed BIST when this bit's status is set |

11.166 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT49 Register (Offset = 3D0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT49 is shown in [Figure 11-165](#) and described in [Table 11-333](#).

Return to [Summary Table](#).

DIG_BIST_EXTRA_READ_REG0

Table 11-332.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT49
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03D0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03D0h |

Figure 11-165. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT49 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_BIST_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-333. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT49 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31-0 | DIG_BIST_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.167 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT50 Register (Offset = 3D4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT50 is shown in [Figure 11-166](#) and described in [Table 11-335](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG1

Table 11-334.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT50
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03D4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03D4h |

Figure 11-166. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT50 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-335. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT50 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT1 | R | 0h | RESERVED |

11.168 DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT51 Register (Offset = 3D8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT51 is shown in [Figure 11-167](#) and described in [Table 11-337](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG2

Table 11-336.
DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT51
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 03D8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 03D8h |

Figure 11-167. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT51 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-337. DPHY_RX_VBUS2APB_DL1_RX_DIG_TBIT51 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT2 | R | 0h | RESERVED |

11.169 DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT0 Register (Offset = 400h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT0 is shown in [Figure 11-168](#) and described in [Table 11-339](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-338.
DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0400h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0400h |

Figure 11-168. DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-339. DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

11.170 DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT1 Register (Offset = 404h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT1 is shown in [Figure 11-169](#) and described in [Table 11-341](#).

Return to [Summary Table](#).

ANA_EXTRA_TBIT0

Table 11-340.
DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0404h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0404h |

Figure 11-169. DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-341. DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | ANA_EXTRA_TBIT0 | R | 0h | RESERVED |

11.171 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0 Register (Offset = 408h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0 is shown in [Figure 11-170](#) and described in [Table 11-343](#).

Return to [Summary Table](#).

DIG_TBIT0

Table 11-342.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0408h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0408h |

Figure 11-170. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0 Register

| | | | | | | | |
|--------------------------|---------------------------|--------------------------|-------------------------------------|-------------------|------------|--------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_1P5TO2P5 G_MODE_SEL | TM_1P5TO2P5 G_MODE_EN | TM_STD_BY | TM_STD_BY_S EL | TM_TERM_EN | TM_TERM_EN _SEL | TM_SETTLE_C OUNT_SEL |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SETTLE_COUNT | | | | | | | SETTLE_COU NT_OFFSET_C ORR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SETTLE_COUNT_OFFSET_CORR | | | TM_DISABLE_ BCLK_PHASE_ ALIGN | UNUSED_3_0 | | | |
| R/W-0h | | | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-343. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_1P5TO2P5G_MODE_ SEL | R/W | 0h | w_tm_1p5to2p5g_mode_sel - Select signal to choose "mode_en" based on top-level "bandctrl" input provided [or] from software register |
| 21 | TM_1P5TO2P5G_MODE_ EN | R/W | 0h | w_tm_1p5to2p5g_mode_en - "mode_en" value considered when selected to have it via software way |
| 20 | TM_STD_BY | R/W | 0h | w_tm_std_by - "tm_std_by" value to be considered when selected to have it via software way Part of control logic to initiate movement of "calib_ctrl" FSM |
| 19 | TM_STD_BY_SEL | R/W | 0h | w_tm_std_by_sel - Select signal to choose between functional "tm_std_by" [or] from software register |
| 18 | TM_TERM_EN | R/W | 0h | w_tm_term_en - "tm_term_en" value to be considered when selected to have it via software way Value provided here converges onto "rxda_rx_term_en" pin on alalog interface |

Table 11-343. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|--|
| 17 | TM_TERM_EN_SEL | R/W | 0h | w_tm_term_en_sel - Select signal to choose between functional "term_en_sel" [or] from software register |
| 16 | TM_SETTLE_COUNT_SEL | R/W | 0h | Test mode settle count selection = 0 - Select signal to choose between functional "settle_count" [or] from software register Value obtained in functional mode depends on the "BandCtl" and "Settle_count_offset" [ie, bits [8:5] here] |
| 15-9 | TM_SETTLE_COUNT | R/W | 0h | Test mode settle count, if bit <16> is set - "settle_count" value to be considered when selected to have it via software way |
| 8-5 | SETTLE_COUNT_OFFSET_CORR | R/W | 0h | Settle count offset correction value that adds up to the internal predefined settle count based on "BandCtl" which helps in deciding the final "settle_count" to be observed for |
| 4 | TM_DISABLE_BCLK_PHASE_ALIGN | R/W | 0h | test mode to disable byte clock phase alignment 0-enable 1-disable |
| 3-0 | UNUSED_3_0 | R | 0h | RESERVED |

11.172 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT1 Register (Offset = 40Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT1 is shown in [Figure 11-171](#) and described in [Table 11-345](#).

Return to [Summary Table](#).

DIG_TBIT1

Table 11-344.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 040Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 040Ch |

Figure 11-171. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT1 Register

| | | | | | | | |
|---------------|-----------|---------------|----|----|----|----------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_ULP_RCV_SEL | TM_ULP_RCV |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_LPRXCD_SEL | TM_LPRXCD | TM_UNUSED_5_1 | | | | | TM_FORCE_TX_STOP_STATE |
| R/W-0h | R/W-0h | R-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-345. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_ULP_RCV_SEL | R/W | 0h | w_tm_ulp_rcv_sel - Select signal to choose between functional "ulp_rcv_en" or a value from software register. The effective value converges onto port "i_ana_ulps_rcv_en" of "lane_always_on" block at DPHY_RX_VBUS2APB_LANE-level. |
| 8 | TM_ULP_RCV | R/W | 0h | w_tm_ulp_rcv_en - "ulp_rcv_en" value considered when selected to have it via software way. |
| 7 | TM_LPRXCD_SEL | R/W | 0h | w_tm_lprxcd_sel - Select signal to choose the lprxcd's block enable value to analog between the one from "lane_always_on" or from the software way onto the port "rxda_lprxcd_en" on Analog interface. |
| 6 | TM_LPRXCD | R/W | 0h | w_tm_lprxcd_en - "lprxcd_en" value considered when selected to have it via software way. |
| 5-1 | TM_UNUSED_5_1 | R | 0h | RESERVED |
| 0 | TM_FORCE_TX_STOP_STATE | R/W | 0h | 0' - No force on escape mode logic - Check polarity. |

11.173 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT2 Register (Offset = 410h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT2 is shown in [Figure 11-172](#) and described in [Table 11-347](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG0

Table 11-346.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0410h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0410h |

Figure 11-172. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_TEST_REG0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-347. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-0 | DIG_EXTRA_TEST_REG0 | R/W | 0h | Digital Extra Functional Test Register 0 |

11.174 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT3 Register (Offset = 414h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT3 is shown in [Figure 11-173](#) and described in [Table 11-349](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg1

Table 11-348.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0414h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0414h |

Figure 11-173. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------------------|-----------------|----|----|----|----|---------------------------------|---------------------------------|
| TM_DIAG_CAL_CLOCK_GATE_EN | TM_UNUSED_30_18 | | | | | | |
| R/W-0h | R-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_30_18 | | | | | | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | TM_PREAMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_ITER_WAIT_TIME | | | | | | | TM_PREAMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-349. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31 | TM_DIAG_CAL_CLOCK_GATE_EN | R/W | 0h | While running diagnostic calibrations, this acts as calibration's clock gate enable Enable = 1 |
| 30-18 | TM_UNUSED_30_18 | R | 0h | RESERVED |
| 17 | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode wait time between two codes selection |
| 16-9 | TM_PREAMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode wait time between two codes |
| 8 | TM_PREAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode initial wait time selection - Select signal to choose between the one from software way or the functional one Functional value gets decided internally based on the "psm_clock_freq" input to Data-Lane |
| 7-0 | TM_PREAMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode initial wait time - "init_value" considered when selected to choose it via software way |

11.175 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4 Register (Offset = 418h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4 is shown in [Figure 11-174](#) and described in [Table 11-351](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg2

Table 11-350.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0418h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0418h |

Figure 11-174. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|-----------------------------|-----------------------|-------------------|---------------|--------------------------|-------------------------|-----------------|
| UNUSED | | | | | TM_PREAMP_ANA_CAL_EN_SEL | TM_PREAMP_ANA_CAL_EN | TM_UNUSED_24_18 |
| R-0h | | | | | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_24_18 | | | | | | TM_PREAMP_CAL_CODE_TUNE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_CODE_TUNE | TM_PREAMP_CAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_OVERRIDE_CODE | TM_PREAMP_CAL_OVERRIDE_EN | TM_PREAMP_CAL_RUN_SEL | TM_PREAMP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-351. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26 | TM_PREAMP_ANA_CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 25 | TM_PREAMP_ANA_CAL_EN | R/W | 0h | test mode analog calibration enable |
| 24-18 | TM_UNUSED_24_18 | R | 0h | RESERVED |
| 17-15 | TM_PREAMP_CAL_CODE_TUNE | R/W | 0h | final preamp cal code tune value |
| 14-7 | TM_PREAMP_CAL_OVERRIDE_CODE | R/W | 0h | preamp calibration override code |
| 6 | TM_PREAMP_CAL_OVERRIDE_EN | R/W | 0h | preamp calibration code override enable |
| 5 | TM_PREAMP_CAL_RUN_SEL | R/W | 0h | test mode calibration run selection |

Table 11-351. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---------------------------|
| 4 | TM_PREAMP_CAL_RUN | R/W | 0h | test mode calibration run |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.176 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT5 Register (Offset = 41Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT5 is shown in [Figure 11-175](#) and described in [Table 11-353](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg1

Table 11-352.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 041Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 041Ch |

Figure 11-175. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT5 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | TM_DCC_COMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-353. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration iteration time enable |
| 16-9 | TM_DCC_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode dcc comp calibration iteration time |
| 8 | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration initial wait time enable |
| 7-0 | TM_DCC_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode dcc comp calibration initial wait time |

11.177 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6 Register (Offset = 420h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6 is shown in [Figure 11-176](#) and described in [Table 11-355](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg2

Table 11-354.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0420h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0420h |

Figure 11-176. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6 Register

| | | | | | | | |
|---------------------------------------|-------------------------------------|---------------------------------|------------------------------------|--------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_DCC_COM P_ANA_CAL_E N_SEL | TM_DCC_COM P_ANA_CAL_E N | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_CODE_TUNE | | | TM_DCC_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_OVER RIDE_CODE | TM_DCC_COM P_CAL_OVER RIDE_EN | TM_DCC_COM P_CAL_RUN_S EL | TM_DCC_COM P_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-355. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_DCC_COMP_ANA_C AL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_DCC_COMP_ANA_C AL_EN | R/W | 0h | test mode dcc comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_DCC_COMP_CAL_C ODE_TUNE | R/W | 0h | test mode dcc comp calibration code tune value |
| 12-7 | TM_DCC_COMP_CAL_O VERRIDE_CODE | R/W | 0h | test mode dcc comp calibration code overirde |
| 6 | TM_DCC_COMP_CAL_O VERRIDE_EN | R/W | 0h | test mode dcc comp calibration override code enable |
| 5 | TM_DCC_COMP_CAL_R UN_SEL | R/W | 0h | dcc comp calibration run selection |
| 4 | TM_DCC_COMP_CAL_R UN | R/W | 0h | dcc comp calibration test mode run |

Table 11-355. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.178 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT7 Register (Offset = 424h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT7 is shown in [Figure 11-177](#) and described in [Table 11-357](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg1

Table 11-356.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0424h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0424h |

Figure 11-177. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT7 Register

| | | | | | | | |
|----------------------------------|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME_E N | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_MIXER_CO MP_CAL_INIT _WAIT_TIME_E N |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-357. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration iteration time enable |
| 16-9 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode mixer comp calibration iteration time |
| 8 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration initial wait time enable |
| 7-0 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode mixer comp calibration initial wait time |

11.179 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8 Register (Offset = 428h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8 is shown in [Figure 11-178](#) and described in [Table 11-359](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg2

Table 11-358.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0428h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0428h |

Figure 11-178. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8 Register

| | | | | | | | |
|---|---------------------------------------|-----------------------------------|--------------------------------------|----------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_MIXER_CO MP_ANA_CAL_ EN_SEL | TM_MIXER_CO MP_ANA_CAL_ EN | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_CODE_TUNE | | | TM_MIXER_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_CO MP_CAL_OVE RRIDE_CODE | TM_MIXER_CO MP_CAL_OVE RRIDE_EN | TM_MIXER_CO MP_CAL_RUN _SEL | TM_MIXER_CO MP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-359. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_MIXER_COMP_ANA_ CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_MIXER_COMP_ANA_ CAL_EN | R/W | 0h | test mode mixer comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_MIXER_COMP_CAL_ CODE_TUNE | R/W | 0h | test mode mixer comp calibration code tune value |
| 12-7 | TM_MIXER_COMP_CAL_ OVERRIDE_CODE | R/W | 0h | test mode mixer comp calibration code override |
| 6 | TM_MIXER_COMP_CAL_ OVERRIDE_EN | R/W | 0h | test mode mixer comp calibration override code enable |
| 5 | TM_MIXER_COMP_CAL_ RUN_SEL | R/W | 0h | mixer comp calibration run selection |
| 4 | TM_MIXER_COMP_CAL_ RUN | R/W | 0h | mixer comp calibration test mode run |

Table 11-359. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT8 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.180 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT9 Register (Offset = 42Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT9 is shown in [Figure 11-179](#) and described in [Table 11-361](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg1

Table 11-360.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT9
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 042Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 042Ch |

Figure 11-179. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT9 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-361. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_POS_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | posedge sampler calibration iteration time between codes |
| 7-0 | TM_POS_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | posedge sampler calibration initial wait time |

11.181 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10 Register (Offset = 430h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10 is shown in [Figure 11-180](#) and described in [Table 11-363](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg2

Table 11-362.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0430h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0430h |

Figure 11-180. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_MCAL_OVERRIDE_EN | TM_POS_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_PCAL_OVERRIDE_CODE | TM_POS_SAMP_PCAL_OVERRIDE_EN | TM_POS_SAMP_CAL_RUN | TM_POS_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-363. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode iteration wait time enable |
| 30 | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_POS_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override mcal_code |
| 15 | TM_POS_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration mcal_code override en |
| 14-7 | TM_POS_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override pcal_code |
| 6 | TM_POS_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration pcal_code override en |
| 5 | TM_POS_SAMP_CAL_RUN | R/W | 0h | posedge sampler calibration test mode run |

Table 11-363. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT10 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_POS_SAMP_CAL_R UN_SEL | R/W | 0h | posedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.182 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT11 Register (Offset = 434h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT11 is shown in [Figure 11-181](#) and described in [Table 11-365](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg3

Table 11-364.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT11
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0434h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0434h |

Figure 11-181. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT11 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_POS_SAMP_ANA_CAL_EN_SEL | TM_POS_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_POS_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-365. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_POS_SAMP_ANA_CAL_EN_SEL | R/W | 0h | posedge sampler calibration analog calib enable selection |
| 8 | TM_POS_SAMP_ANA_CAL_EN | R/W | 0h | posedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_POS_SAMP_CAL_CODE_TUNE | R/W | 0h | posedge sampler calibration tune code |

11.183 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT12 Register (Offset = 438h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT12 is shown in [Figure 11-182](#) and described in [Table 11-367](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg1

Table 11-366.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT12
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0438h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0438h |

Figure 11-182. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT12 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-367. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | negedge sampler calibration iteration time between codes |
| 7-0 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | negedge sampler calibration initial wait time |

11.184 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13 Register (Offset = 43Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13 is shown in [Figure 11-183](#) and described in [Table 11-369](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg2

Table 11-368.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 043Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 043Ch |

Figure 11-183. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_MCAL_OVERRIDE_EN | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_PCAL_OVERRIDE_CODE | TM_NEG_SAMP_PCAL_OVERRIDE_EN | TM_NEG_SAMP_CAL_RUN | TM_NEG_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-369. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode iteration wait time enable |
| 30 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_NEG_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override mcal_code |
| 15 | TM_NEG_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration mcal_code override en |
| 14-7 | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override pcal_code |
| 6 | TM_NEG_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration pcal_code override en |
| 5 | TM_NEG_SAMP_CAL_RUN | R/W | 0h | negedge sampler calibration test mode run |

Table 11-369. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT13 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_NEG_SAMP_CAL_R UN_SEL | R/W | 0h | negedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.185 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT14 Register (Offset = 440h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT14 is shown in [Figure 11-184](#) and described in [Table 11-371](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg3

Table 11-370.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT14
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0440h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0440h |

Figure 11-184. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT14 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_NEG_SAMP_ANA_CAL_EN_SEL | TM_NEG_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_NEG_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-371. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_NEG_SAMP_ANA_CAL_EN_SEL | R/W | 0h | negedge sampler calibration analog calib enable selection |
| 8 | TM_NEG_SAMP_ANA_CAL_EN | R/W | 0h | negedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_NEG_SAMP_CAL_CODE_TUNE | R/W | 0h | negedge sampler calibration tune code |

11.186 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT15 Register (Offset = 444h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT15 is shown in [Figure 11-185](#) and described in [Table 11-373](#).

Return to [Summary Table](#).

skew_cal_fsm_reg1

Table 11-372.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT15
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0444h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0444h |

Figure 11-185. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT15 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|----|----|--------------------------------|------------------------------------|-----------------------------------|------------------------------|------------------------------|
| UNUSED | | | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | | | | | TM_SKEW_CAL_FPHASE_WAIT_TIME | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_FPHASE_WAIT_TIME | | | | | | | TM_SKEW_CAL_TIMER_INIT_COUNT |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-373. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | R/W | 0h | skew calibration analog max saturation test mode enable |
| 27 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | R/W | 0h | skew calibration analog max saturation selection |
| 26-18 | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | R/W | 0h | skew calibration fast phase long wait time |
| 17-9 | TM_SKEW_CAL_FPHASE_WAIT_TIME | R/W | 0h | skew calibration fast phase wait time |
| 8-0 | TM_SKEW_CAL_TIMER_INIT_COUNT | R/W | 0h | skew calibration initial wait time |

11.187 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT16 Register (Offset = 448h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT16 is shown in [Figure 11-186](#) and described in [Table 11-375](#).

Return to [Summary Table](#).

skew_cal_fsm_reg2

Table 11-374.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT16
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0448h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0448h |

Figure 11-186. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT16 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|------------------------------------|------------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | |
| R-0h | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_ACC_CODE_MIN_VALUE | | | | | | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | TM_SKEW_CAL_SPHASE_WAIT_TIME |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_SPHASE_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-375. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26-19 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | R/W | 0h | skew calibration delay code test mode max value |
| 18 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | R/W | 0h | skew calibration max code test reg selection |
| 17-10 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | R/W | 0h | skew calibration delay code test mode min value |
| 9 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | R/W | 0h | skew calibration min code test reg selection |
| 8-0 | TM_SKEW_CAL_SPHASE_WAIT_TIME | R/W | 0h | skew calibration slow phase wait time |

11.188 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT17 Register (Offset = 44Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT17 is shown in [Figure 11-187](#) and described in [Table 11-377](#).

Return to [Summary Table](#).

skew_cal_fsm_reg3

Table 11-376.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT17
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 044Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 044Ch |

Figure 11-187. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT17 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_DESKEW_START_CODE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-377. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|-------------------------------------|
| 31-8 | UNUSED | R | 0h | RESERVED |
| 7-0 | TM_SKEW_CAL_DESKEW_START_CODE | R/W | 0h | skew calibration initial start code |

11.189 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT18 Register (Offset = 450h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT18 is shown in [Figure 11-188](#) and described in [Table 11-379](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg1

Table 11-378.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT18
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0450h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0450h |

Figure 11-188. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT18 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_TIMER_ITER_COUNT | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_TIMER_ITER_COUNT | | | | | | TM_DUCY_CORR_TIMER_INIT_COUNT | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CORR_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-379. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-9 | TM_DUCY_CORR_TIMER_ITER_COUNT | R/W | 0h | duty cycle correction iteration wait time specified in this register will be considered when a non-zero value is specified here |
| 8-0 | TM_DUCY_CORR_TIMER_INIT_COUNT | R/W | 0h | duty cycle correction initial wait time specified in this register will be considered when a non-zero value is specified here |

11.190 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT19 Register (Offset = 454h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT19 is shown in [Figure 11-189](#) and described in [Table 11-381](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg2

Table 11-380.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT19
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0454h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0454h |

Figure 11-189. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT19 Register

| | | | | | | | |
|---|---|-----------------------------|---|---------------------------------|----|-------------------------------------|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_ACC_CODE_ MAX_VALUE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_ACC_CODE_MAX_VALUE | | | TM_DUCY_CO RR_ACC_COD E_MAX_VALUE _SEL | TM_DUCY_CORR_ACC_CODE_MIN_VALUE | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CO RR_ACC_COD E_MIN_VALUE | TM_DUCY_CO RR_ACC_COD E_MIN_VALUE _SEL | TM_DUCY_CORR_ACC_START_CODE | | | | | TM_DUCY_CO RR_ACC_STA RT_CODE_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-381. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-13 | TM_DUCY_CORR_ACC_ CODE_MAX_VALUE | R/W | 0h | duty cycle correction test mode max value |
| 12 | TM_DUCY_CORR_ACC_ CODE_MAX_VALUE_SEL | R/W | 0h | duty cycle correction test mode max value selection |
| 11-7 | TM_DUCY_CORR_ACC_ CODE_MIN_VALUE | R/W | 0h | duty cycle correction test mode min value |
| 6 | TM_DUCY_CORR_ACC_ CODE_MIN_VALUE_SEL | R/W | 0h | duty cycle correction test mode min value selection |
| 5-1 | TM_DUCY_CORR_ACC_ START_CODE | R/W | 0h | duty cycle correction test mode start code |
| 0 | TM_DUCY_CORR_ACC_ START_CODE_SEL | R/W | 0h | duty cycle correction test mode start code selection |

11.191 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20 Register (Offset = 458h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20 is shown in [Figure 11-190](#) and described in [Table 11-383](#).

Return to [Summary Table](#).

skew_cal_avg_reg1

Table 11-382.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0458h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0458h |

Figure 11-190. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------|--------------------------|---------------------|----|----|-------------------------|----------------------|----------------------------|
| TM_ANA_DESKEW_DCC_EN | TM_ANA_DESKEW_DCC_EN_SEL | TM_DCC_CODE_TUNE | | | TM_DCC_CODE_OVERRIDE_EN | TM_DCC_CODE_OVERRIDE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DCC_CODE_OVERRIDE | | TM_DESKEW_CODE_TUNE | | | | | TM_DESKEW_CODE_OVERRIDE_EN |
| R/W-0h | | R/W-0h | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_CODE_OVERRIDE | | | | | | | TM_PROC_TIMER_LOAD_VAL |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PROC_TIMER_LOAD_VAL | | | | | | | TM_PROC_TIMER_LOAD_VAL_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-383. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31 | TM_ANA_DESKEW_DCC_EN | R/W | 0h | test mode analog deskew enable |
| 30 | TM_ANA_DESKEW_DCC_EN_SEL | R/W | 0h | test mode deskew analog enable selection |
| 29-27 | TM_DCC_CODE_TUNE | R/W | 0h | duty cycle correction code tune |
| 26 | TM_DCC_CODE_OVERRIDE_EN | R/W | 0h | duty cycle correction code override enable |
| 25-22 | TM_DCC_CODE_OVERRIDE | R/W | 0h | duty cycle correction override code |
| 21-17 | TM_DESKEW_CODE_TUNE | R/W | 0h | skew calibration delay line code tune |
| 16 | TM_DESKEW_CODE_OVERRIDE_EN | R/W | 0h | skew calibration delay code override enable |
| 15-9 | TM_DESKEW_CODE_OVERRIDE | R/W | 0h | skew calibration delay line override code |

Table 11-383. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 8-1 | TM_PROC_TIMER_LOAD_VAL | R/W | 0h | skew calibration process time test mode value |
| 0 | TM_PROC_TIMER_LOAD_VAL_SEL | R/W | 0h | skew calibration process time test mode value selection |

11.192 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT21 Register (Offset = 45Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT21 is shown in [Figure 11-191](#) and described in [Table 11-385](#).

Return to [Summary Table](#).

skew_cal_avg_reg2

Table 11-384.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT21
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 045Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 045Ch |

Figure 11-191. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT21 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|------------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG LENG_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG LENG_TIMER_LOAD_VAL | | | | | | TM_AVG2AVG LENG_TIMER_LOAD_VAL_SEL | TM_DCC_ACC LENG_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC LENG_TIMER_LOAD_VAL | | | | | | TM_DCC_ACC LENG_TIMER_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-385. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG LENG_TIMER_LOAD_VAL | R/W | 0h | delay line code averaging to dcc code averaging wait time |
| 9 | TM_AVG2AVG LENG_TIMER_LOAD_VAL_SEL | R/W | 0h | delay line code averaging to dcc code averaging wait time selection |
| 8-1 | TM_DCC_ACC LENG_TIMER_LOAD_VAL | R/W | 0h | total number of dcc codes to be taken for averaging in test mode |
| 0 | TM_DCC_ACC LENG_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection value for test mode number of dcc codes under averaging |

11.193 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT22 Register (Offset = 460h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT22 is shown in [Figure 11-192](#) and described in [Table 11-387](#).

[Return to Summary Table.](#)

skew_cal_avg_reg3

Table 11-386.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT22
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0460h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0460h |

Figure 11-192. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT22 Register

| | | | | | | | |
|--|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ DONE_LEN TIMER_LOAD_ VAL_SEL | TM_DESKEW_ ACC_LEN G_TIMER_LOAD_ VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ ACC_LEN G_TIMER_LOAD_ VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-387. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | R/W | 0h | after skew calibration is done, length of wait timer |
| 9 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | test mode selection value for length of wait time after deskew |
| 8-1 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | R/W | 0h | number of deskew dealy codes to be taken for averaging |
| 0 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | tets mode selction for test mode number of delay line codes for averaging |

11.194 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT23 Register (Offset = 464h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT23 is shown in [Figure 11-193](#) and described in [Table 11-389](#).

Return to [Summary Table](#).

skew_cal_avg_reg4

Table 11-388.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT23
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0464h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0464h |

Figure 11-193. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT23 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-----------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG_RES_TIMER_LOAD_VAL | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | TM_DCC_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC_RES_TIMER_LOAD_VAL | | | | | | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-389. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging to deskew averaging wait time in test mode |
| 9 | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging to deskew averaging wait time |
| 8-1 | TM_DCC_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging wait time in test mode |
| 0 | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging wait time |

11.195 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT24 Register (Offset = 468h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT24 is shown in [Figure 11-194](#) and described in [Table 11-391](#).

Return to [Summary Table](#).

skew_cal_avg_reg5

Table 11-390.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT24
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0468h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0468h |

Figure 11-194. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT24 Register

| | | | | | | | |
|-----------------------------------|----|----|----|----|----|---------------------------------------|--------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | | | | | | | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-391. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew done wait time in test mode |
| 9 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selction of resolution time of deskew done wait time in test mode |
| 8-1 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew averaging wait time in test mode |
| 0 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | tets mode selection of resolution time of deskew averaging wait time in test mode |

11.196 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT25 Register (Offset = 46Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT25 is shown in [Figure 11-195](#) and described in [Table 11-393](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG0

Table 11-392.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT25
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 046Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 046Ch |

Figure 11-195. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-393. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT0 | R | 0h | RESERVED |

11.197 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT26 Register (Offset = 470h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT26 is shown in [Figure 11-196](#) and described in [Table 11-395](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG1

Table 11-394.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT26
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0470h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0470h |

Figure 11-196. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-395. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT1 | R | 0h | RESERVED |

11.198 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT27 Register (Offset = 474h) [reset = 0A000018h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT27 is shown in [Figure 11-197](#) and described in [Table 11-397](#).

Return to [Summary Table](#).

bist_config_reg1

Table 11-396.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT27
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0474h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0474h |

Figure 11-197. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT27 Register

| | | | | | | | |
|---------------------|----|----|--------------|----|-------------|-----------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_IDLE_TIME_LENGTH | | | | | | | |
| R/W-Ah | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_MODE | | | TM_PRBS_MODE | | TM_UNUSED_2 | TM_FREEZE | TM_BIST_EN |
| R/W-0h | | | R/W-3h | | R-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-397. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-24 | TM_IDLE_TIME_LENGTH | R/W | Ah | BIST_IDLE_TIME |
| 23-8 | TM_UNUSED_23_8 | R | 0h | RESERVED |
| 7-5 | TM_TEST_MODE | R/W | 0h | PRBS mode - when set to '1' PRBS mode is selected |
| 4-3 | TM_PRBS_MODE | R/W | 3h | BIST PRBS MODE 9 when 0x0 |
| 2 | TM_UNUSED_2 | R | 0h | RESERVED |
| 1 | TM_FREEZE | R/W | 0h | Freeze the LFSR contents after every packet or frame |
| 0 | TM_BIST_EN | R/W | 0h | Enable signal for pattern checker |

11.199 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT28 Register (Offset = 478h) [reset = DECDBCABh]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT28 is shown in [Figure 11-198](#) and described in [Table 11-399](#).

Return to [Summary Table](#).

bist_config_reg2

Table 11-398.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT28
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0478h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0478h |

Figure 11-198. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_TEST_PAT4 | | | | | | | | TM_TEST_PAT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_PAT2 | | | | | | | | TM_TEST_PAT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-399. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-24 | TM_TEST_PAT4 | R/W | DEh | User registers to specify the BIST data4 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 23-16 | TM_TEST_PAT3 | R/W | CDh | User registers to specify the BIST data3 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 15-8 | TM_TEST_PAT2 | R/W | BCh | User registers to specify the BIST data2 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 7-0 | TM_TEST_PAT1 | R/W | ABh | User registers to specify the BIST data1 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |

11.200 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT29 Register (Offset = 47Ch) [reset = 28h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT29 is shown in [Figure 11-199](#) and described in [Table 11-401](#).

Return to [Summary Table](#).

bist_config_reg3

Table 11-400.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT29
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 047Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 047Ch |

Figure 11-199. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT29 Register

| | | | | | | | |
|-----------------|----|----|---------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_CLEAR_BIST | TM_UNUSED_27_12 | | | |
| R-0h | | | R/W-0h | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_27_12 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_27_12 | | | | TM_PKT_LENGTH | | | |
| R-0h | | | | R/W-28h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PKT_LENGTH | | | | | | | |
| R/W-28h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-401. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_CLEAR_BIST | R/W | 0h | Setting this will clear all the BIST related flags and counters |
| 27-12 | TM_UNUSED_27_12 | R | 0h | RESERVED |
| 11-0 | TM_PKT_LENGTH | R/W | 28h | Based on the default_mode design will consider the run-length from design or the programmed value specified here |

11.201 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT30 Register (Offset = 480h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT30 is shown in [Figure 11-200](#) and described in [Table 11-403](#).

Return to [Summary Table](#).

bist_config_reg4

Table 11-402.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT30
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0480h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0480h |

Figure 11-200. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT30 Register

| | | | | | | | |
|--------|----|----|----|----|----|---------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | TM_LPRX_BIS T_EN | TM_HSRX_BIS T_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-403. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-2 | UNUSED | R | 0h | RESERVED |
| 1 | TM_LPRX_BIST_EN | R/W | 0h | LPRX BIST is enabled - rxda_lprx_bist_en - When '1', LP BIST is enabled |
| 0 | TM_HSRX_BIST_EN | R/W | 0h | HSRX BIST is enabled - rxda_hsrx_bist_en - when '1', HS BIST is enabled |

11.202 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT31 Register (Offset = 484h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT31 is shown in [Figure 11-201](#) and described in [Table 11-405](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG1

Table 11-404.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT31
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0484h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0484h |

Figure 11-201. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-405. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT1 | R | 0h | RESERVED |

11.203 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT32 Register (Offset = 488h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT32 is shown in [Figure 11-202](#) and described in [Table 11-407](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG2

Table 11-406.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT32
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0488h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0488h |

Figure 11-202. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-407. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT2 | R | 0h | RESERVED |

11.204 DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT2 Register (Offset = 48Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT2 is shown in [Figure 11-203](#) and described in [Table 11-409](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-408.
DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 048Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 048Ch |

Figure 11-203. DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-409. DPHY_RX_VBUS2APB_DL2_RX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | ANA_READ_TBIT0 | R | 0h | Analog read register 0 |

11.205 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT33 Register (Offset = 490h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT33 is shown in [Figure 11-204](#) and described in [Table 11-411](#).

Return to [Summary Table](#).

deserialiser_fsm_status

Table 11-410.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT33
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0490h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0490h |

Figure 11-204. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|------------------|----|-------------|----|----|----|-------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_PPI_CUR_STATE | | | | | | TM_CTRL_CUR_STATE | | | |
| R-0h | | | | | | R-0h | | | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_CTRL_CUR_STATE | | | | | | | | TM_SYNC_PKT | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-411. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-26 | UNUSED | R | 0h | RESERVED |
| 25-18 | TM_PPI_CUR_STATE | R | 0h | Current State of the SYNC detection FSM during the HS data receive mode or skew calibration mode |
| 17-8 | TM_CTRL_CUR_STATE | R | 0h | current state status of HS receive FSM |
| 7-0 | TM_SYNC_PKT | R | 0h | Status of received SYNC packet |

11.206 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT34 Register (Offset = 494h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT34 is shown in [Figure 11-205](#) and described in [Table 11-413](#).

Return to [Summary Table](#).

lp_status

Table 11-412.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT34
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0494h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0494h |

Figure 11-205. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT34 Register

| | | | | | | | |
|--------------------|----|--------------|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | TM_LP_RX_CUR_STATE | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_LP_RX_CUR_STATE | | TM_LP_STATUS | | | | | |
| R-0h | | R-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-413. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|---|
| 31-19 | UNUSED | R | 0h | RESERVED |
| 18-14 | TM_LP_RX_CUR_STATE | R | 0h | Current state of LP receiver FSM |
| 13-8 | TM_LP_STATUS | R | 0h | Status of DP, DN pins of LPRX, LPCD, ULPRX respectively |
| 7-0 | UNUSED_7_0 | R | 0h | RESERVED |

11.207 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT35 Register (Offset = 498h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT35 is shown in [Figure 11-206](#) and described in [Table 11-415](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_READ_REG0

Table 11-414.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT35
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0498h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0498h |

Figure 11-206. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-415. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.208 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36 Register (Offset = 49Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36 is shown in [Figure 11-207](#) and described in [Table 11-417](#).

Return to [Summary Table](#).

dcc_mixer_comparator_calibration_stat

Table 11-416.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 049Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 049Ch |

Figure 11-207. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36 Register

| | | | | | | | |
|--------------------------|--------------------------|---------------------|----|----|----|---------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_MIX_COM P_ANA_RESP | TM_MIX_COMP_CALCODE | | | | TM_MIX_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIX_COM P_CAL_DONE | TM_DCC_COM P_ANA_RESP | TM_DCC_COMP_CALCODE | | | | TM_DCC_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_DONE | TM_CALIB_CTRL_CUR_STATE | | | | | TM_CUR_DRX _CAL_DONE | |
| R-0h | R-0h | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-417. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_MIX_COMP_ANA_RESP | R | 0h | Mixer comparator analog response |
| 21-17 | TM_MIX_COMP_CALCODE | R | 0h | Mixer comparator calibration code |
| 16 | TM_MIX_COMP_CAL_NO_RESP | R | 0h | Mixer comparator calibration has no response from analog |
| 15 | TM_MIX_COMP_CAL_DONE | R | 0h | Mixer comparator calibration is done properly |
| 14 | TM_DCC_COMP_ANA_RESP | R | 0h | Duty Cycle Comparator analog response |
| 13-9 | TM_DCC_COMP_CALCODE | R | 0h | Duty cycle corrector comparator calibration code |
| 8 | TM_DCC_COMP_CAL_NO_RESP | R | 0h | Duty cycle corrector comparator calibration has no response from analog |

Table 11-417. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT36 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7 | TM_DCC_COMP_CAL_DONE | R | 0h | Duty cycle corrector comparator calibration is done properly |
| 6-1 | TM_CALIB_CTRL_CUR_STATE | R | 0h | If struck, indicates calibration FSM current state |
| 0 | TM_CUR_DRX_CAL_DONE | R | 0h | Current DRX DPHY_RX_VBUS2APB_LANE calibrations are done |

11.209 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37 Register (Offset = 4A0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37 is shown in [Figure 11-208](#) and described in [Table 11-419](#).

Return to [Summary Table](#).

preamp_cal_status_reg1

Table 11-418.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 04A0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 04A0h |

Figure 11-208. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------|----|-----------------------------|-----------------------------|---------------------------------|--------------------------|-----------------------------------|
| TM_ANA_RES_P_STAT | TM_PREAMP_STAT_ANA_CAL_CODE | | | | | | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE |
| R-0h | R-0h | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | | | | | | | TM_PREAMP_STAT_NCAL_PREAMP_CODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_STAT_NCAL_PREAMP_CODE | | | | | TM_PREAMP_STAT_PCAL_PREAMP_CODE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_STAT_PCAL_PREAMP_CODE | | | TM_PREAMP_STAT_NCAL_NO_RESP | TM_PREAMP_STAT_PCAL_NO_RESP | TM_PREAMP_STAT_NCAL_DONE | TM_PREAMP_STAT_PCAL_DONE | TM_PREAMP_STAT_CAL_DONE |
| R-0h | | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-419. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31 | TM_ANA_RESP_STAT | R | 0h | current analog or test mode response for which calibration is happening |
| 30-25 | TM_PREAMP_STAT_ANA_CAL_CODE | R | 0h | code going to analog |
| 24-17 | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | R | 0h | code decided to send to analog before tune |
| 16-11 | TM_PREAMP_STAT_NCAL_PREAMP_CODE | R | 0h | calib code in posedge_data run |
| 10-5 | TM_PREAMP_STAT_PCAL_PREAMP_CODE | R | 0h | calib code in negedge_data run |
| 4 | TM_PREAMP_STAT_NCAL_NO_RESP | R | 0h | negedge_data run has no response |
| 3 | TM_PREAMP_STAT_PCAL_NO_RESP | R | 0h | posedge_data run has no response |
| 2 | TM_PREAMP_STAT_NCAL_DONE | R | 0h | negedge_data cal run is done |

Table 11-419. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT37 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|------------------------------|
| 1 | TM_PREAMP_STAT_PCA L_DONE | R | 0h | posedge_data cal run is done |
| 0 | TM_PREAMP_STAT_CAL _DONE | R | 0h | preamp calibration is done |

11.210 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38 Register (Offset = 4A4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38 is shown in [Figure 11-209](#) and described in [Table 11-421](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg1

Table 11-420.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04A4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04A4h |

Figure 11-209. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38 Register

| | | | | | | | |
|---------------------------------|----|----|---|---------------------------------|----------------------------|---------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_POS_SAMP_STAT_SAMP LTM_POS_SAMP_STAT_CAL_DONE | TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_POS_SAMP_STAT_CODE_TYPE | TM_POS_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_UP_CAL_CODE | | | | | | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | TM_POS_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-421. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_POS_SAMP_STAT_SAMP LTM_POS_SAMP_STAT_CAL_DONE | R | 0h | posedge sampler calibration is done |
| 19-11 | TM_POS_SAMP_STAT_FINAL_CAL_CODE | R | 0h | posedge sampler calibration final code |
| 10 | TM_POS_SAMP_STAT_CODE_TYPE | R | 0h | code type that is changing for posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-421. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT38 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_POS_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.211 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT39 Register (Offset = 4A8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT39 is shown in [Figure 11-210](#) and described in [Table 11-423](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg2

Table 11-422.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT39
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04A8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04A8h |

Figure 11-210. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT39 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|--|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_POS_SAMP P_ANA_CAL_R ESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_POS_SAMP P_STAT_ANA_ CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_POS_SAMP_STAT_DOWN_ CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_POS_SAMP P_STAT_NO_D OWN_CAL_RE SP | TM_POS_SAMP P_STAT_DOW N_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-423. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_POS_SAMP_ANA_CAL_RESP | R | 0h | test mode status of posedge sampler |
| 23-17 | TM_POS_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to posedge sampler |
| 16-10 | TM_POS_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_POS_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.212 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40 Register (Offset = 4ACh) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40 is shown in [Figure 11-211](#) and described in [Table 11-425](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg1

Table 11-424.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04ACh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04ACh |

Figure 11-211. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40 Register

| | | | | | | | |
|---------------------------------|----|----|---|---------------------------------|----------------------------|---------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_NEG_SAMP_STAT_CODE_TYPE | TM_NEG_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_UP_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_UP_CAL_RESP | TM_NEG_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-425. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | R | 0h | negedge sampler calibration is done |
| 19-11 | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | R | 0h | negedge sampler calibration final code |
| 10 | TM_NEG_SAMP_STAT_CODE_TYPE | R | 0h | code type that is changing for negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-425. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT40 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_NEG_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.213 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT41 Register (Offset = 4B0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT41 is shown in [Figure 11-212](#) and described in [Table 11-427](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg2

Table 11-426.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT41
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04B0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04B0h |

Figure 11-212. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT41 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_NEG_SAMP_ANA_CAL_RESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_NEG_SAMP_STAT_ANA_CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | TM_NEG_SAMP_STAT_DOWN_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-427. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT41 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_NEG_SAMP_ANA_CAL_RESP | R | 0h | test mode status of negedge sampler |
| 23-17 | TM_NEG_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to negedge sampler |
| 16-10 | TM_NEG_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_NEG_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.214 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42 Register (Offset = 4B4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42 is shown in [Figure 11-213](#) and described in [Table 11-429](#).

Return to [Summary Table](#).

skew_cal_fsm_status_reg1

Table 11-428.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 04B4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 04B4h |

Figure 11-213. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42 Register

| | | | | | | | |
|------------------------------------|----|-------------------------------------|-------------------------|----|-----------------------------------|-----------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_DESKEW_DCC_CUR_STATE | | | | |
| R-0h | | | R-0h | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_CUR_STATE | | TM_DESKEW_DCC_INIT_MIXER_VALUE | TM_SP_FIRST_TRIP_CODE | | | | |
| R-0h | | R-0h | R-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SP_FIRST_TRIP_CODE | | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | | | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | |
| R-0h | | R-0h | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | | | | | | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | |
| R-0h | | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-429. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28-22 | TM_DESKEW_DCC_CUR_STATE | R | 0h | Duty cycle correction logic current state |
| 21 | TM_DESKEW_DCC_INIT_MIXER_VALUE | R | 0h | Duty cycle correction initial comparator value |
| 20-14 | TM_SP_FIRST_TRIP_CODE | R | 0h | slow phase first trip code |
| 13-10 | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | R | 0h | current state of the deskew FSM |
| 9 | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | R | 0h | if asserted, deskew FSM has gone into max saturation second time |
| 8 | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | R | 0h | if asserted, deskew FSM has got saturated once |

Table 11-429. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT42 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------------|------|-------|--------------------------------------|
| 7-1 | TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | R | 0h | deskew FSM fast phase trip code |
| 0 | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | R | 0h | deskew algorithm mixer initial value |

11.215 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT43 Register (Offset = 4B8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT43 is shown in [Figure 11-214](#) and described in [Table 11-431](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg1

Table 11-430.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT43
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04B8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04B8h |

Figure 11-214. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT43 Register

| | | | | | | | |
|-------------------------------------|----|----------------------------------|-------------------------------------|----|-------------------------------|--------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | | | | | | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | |
| R-0h | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DCC_AVG_ANA_DCC_CODE | | | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | | | |
| R-0h | | | R-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | | | TM_DESKEW_DCC_AVG_DONE_DESKEW | | TM_DESKEW_DCC_AVG_DONE_DCC |
| R-0h | | R-0h | | | R-0h | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-431. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT43 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-17 | TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | R | 0h | final code going to delay line |
| 16-13 | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | R | 0h | final code going to duty cycle corrector |
| 12-6 | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | R | 0h | delay line code before tuning |
| 5-2 | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | R | 0h | duty code before tuning |
| 1 | TM_DESKEW_DCC_AVG_DONE_DESKEW | R | 0h | skew calibration is done |
| 0 | TM_DESKEW_DCC_AVG_DONE_DCC | R | 0h | duty cycle correction is done |

11.216 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT44 Register (Offset = 4BCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT44 is shown in [Figure 11-215](#) and described in [Table 11-433](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg2

Table 11-432.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT44
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04BCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04BCh |

Figure 11-215. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT44 Register

| | | | | | | | | | | | | | | | |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | TM_D ESKE W_DC C_AVG _CUT M_DE SKEW _DCC_ AVG_S TATE | |
| R-0h | | | | | | | | | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-433. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT44 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-17 | UNUSED | R | 0h | RESERVED |
| 16-0 | TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | R | 0h | current state of deskew_dcc_averaging FSM |

11.217 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT45 Register (Offset = 4C0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT45 is shown in [Figure 11-216](#) and described in [Table 11-435](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG0

Table 11-434.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT45
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04C0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04C0h |

Figure 11-216. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT45 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-435. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT45 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT0 | R | 0h | RESERVED |

11.218 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT46 Register (Offset = 4C4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT46 is shown in [Figure 11-217](#) and described in [Table 11-437](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG1

Table 11-436.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT46
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04C4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04C4h |

Figure 11-217. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT46 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-437. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT46 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT1 | R | 0h | RESERVED |

11.219 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT47 Register (Offset = 4C8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT47 is shown in [Figure 11-218](#) and described in [Table 11-439](#).

Return to [Summary Table](#).

bist_status_reg1

Table 11-438.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT47
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04C8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04C8h |

Figure 11-218. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT47 Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| W_PAT_CHE_ERROR_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W_PAT_CHE_PKT_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-439. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT47 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-16 | W_PAT_CHE_ERROR_COUNT | R | 0h | BIST Pattern checker error count's live status can be obtained by poling this field |
| 15-0 | W_PAT_CHE_PKT_COUNT | R | 0h | BIST packet count's live status can be obtained by poling this field |

11.220 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT48 Register (Offset = 4CCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT48 is shown in [Figure 11-219](#) and described in [Table 11-441](#).

Return to [Summary Table](#).

bist_status_reg2

Table 11-440.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT48
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04CCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04CCh |

Figure 11-219. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT48 Register

| | | | | | | | |
|--------|----|----|----|----|------------------|--------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | W_BIST_ERRO R | R_PAT_CHE_S YNC | W_DRX_BIST_ PASS |
| R-0h | | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-441. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT48 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-3 | UNUSED | R | 0h | RESERVED |
| 2 | W_BIST_ERROR | R | 0h | Status of HS data path comparision outcome, '0' means pass |
| 1 | R_PAT_CHE_SYNC | R | 0h | Informs BIST Pattern checker is not in sync with pattern generator - Check polarity |
| 0 | W_DRX_BIST_PASS | R | 0h | Entire DRX has passed BIST when this bit's status is set |

11.221 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT49 Register (Offset = 4D0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT49 is shown in [Figure 11-220](#) and described in [Table 11-443](#).

Return to [Summary Table](#).

DIG_BIST_EXTRA_READ_REG0

Table 11-442.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT49
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04D0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04D0h |

Figure 11-220. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT49 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_BIST_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-443. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT49 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31-0 | DIG_BIST_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.222 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT50 Register (Offset = 4D4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT50 is shown in [Figure 11-221](#) and described in [Table 11-445](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG1

Table 11-444.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT50
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04D4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04D4h |

Figure 11-221. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT50 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-445. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT50 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT1 | R | 0h | RESERVED |

11.223 DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT51 Register (Offset = 4D8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT51 is shown in [Figure 11-222](#) and described in [Table 11-447](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG2

Table 11-446.
DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT51
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 04D8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 04D8h |

Figure 11-222. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT51 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-447. DPHY_RX_VBUS2APB_DL2_RX_DIG_TBIT51 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT2 | R | 0h | RESERVED |

11.224 DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT0 Register (Offset = 500h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT0 is shown in [Figure 11-223](#) and described in [Table 11-449](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-448.
DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0500h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0500h |

Figure 11-223. DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-449. DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|------------------------|
| 31-0 | ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

11.225 DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT1 Register (Offset = 504h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT1 is shown in [Figure 11-224](#) and described in [Table 11-451](#).

Return to [Summary Table](#).

ANA_EXTRA_TBIT0

Table 11-450.
DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0504h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0504h |

Figure 11-224. DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-451. DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | ANA_EXTRA_TBIT0 | R | 0h | RESERVED |

11.226 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0 Register (Offset = 508h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0 is shown in [Figure 11-225](#) and described in [Table 11-453](#).

Return to [Summary Table](#).

DIG_TBIT0

Table 11-452.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0508h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0508h |

Figure 11-225. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0 Register

| | | | | | | | |
|--------------------------|-----------------------|----------------------|-----------------------------|---------------|------------|----------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_1P5TO2P5G_MODE_SEL | TM_1P5TO2P5G_MODE_EN | TM_STD_BY | TM_STD_BY_SEL | TM_TERM_EN | TM_TERM_EN_SEL | TM_SETTLE_COUNT_SEL |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SETTLE_COUNT | | | | | | | SETTLE_COUNT_OFFSET_CORR |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SETTLE_COUNT_OFFSET_CORR | | | TM_DISABLE_BCLK_PHASE_ALIGN | UNUSED_3_0 | | | |
| R/W-0h | | | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-453. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_1P5TO2P5G_MODE_SEL | R/W | 0h | w_tm_1p5to2p5g_mode_sel - Select signal to choose "mode_en" based on top-level "bandctrl" input provided [or] from software register |
| 21 | TM_1P5TO2P5G_MODE_EN | R/W | 0h | w_tm_1p5to2p5g_mode_en - "mode_en" value considered when selected to have it via software way |
| 20 | TM_STD_BY | R/W | 0h | w_tm_std_by - "tm_std_by" value to be considered when selected to have it via software way Part of control logic to initiate movement of "calib_ctrl" FSM |
| 19 | TM_STD_BY_SEL | R/W | 0h | w_tm_std_by_sel - Select signal to choose between functional "tm_std_by" [or] from software register |
| 18 | TM_TERM_EN | R/W | 0h | w_tm_term_en - "tm_term_en" value to be considered when selected to have it via software way Value provided here converges onto "rxda_rx_term_en" pin on alalog interface |

Table 11-453. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-----------------------------|------|-------|--|
| 17 | TM_TERM_EN_SEL | R/W | 0h | w_tm_term_en_sel - Select signal to choose between functional "term_en_sel" [or] from software register |
| 16 | TM_SETTLE_COUNT_SEL | R/W | 0h | Test mode settle count selection = 0 - Select signal to choose between functional "settle_count" [or] from software register Value obtained in functional mode depends on the "BandCtl" and "Settle_count_offset" [ie, bits [8:5] here] |
| 15-9 | TM_SETTLE_COUNT | R/W | 0h | Test mode settle count, if bit <16> is set - "settle_count" value to be considered when selected to have it via software way |
| 8-5 | SETTLE_COUNT_OFFSET_CORR | R/W | 0h | Settle count offset correction value that adds up to the internal predefined settle count based on "BandCtl" which helps in deciding the final "settle_count" to be observed for |
| 4 | TM_DISABLE_BCLK_PHASE_ALIGN | R/W | 0h | test mode to disable byte clock phase alignment 0-enable 1-disable |
| 3-0 | UNUSED_3_0 | R | 0h | RESERVED |

11.227 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT1 Register (Offset = 50Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT1 is shown in [Figure 11-226](#) and described in [Table 11-455](#).

Return to [Summary Table](#).

DIG_TBIT1

Table 11-454.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 050Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 050Ch |

Figure 11-226. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT1 Register

| | | | | | | | |
|---------------|-----------|---------------|----|----|----|----------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_ULP_RCV_SEL | TM_ULP_RCV |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_LPRXCD_SEL | TM_LPRXCD | TM_UNUSED_5_1 | | | | | TM_FORCE_TX_STOP_STATE |
| R/W-0h | R/W-0h | R-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-455. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_ULP_RCV_SEL | R/W | 0h | w_tm_ulp_rcv_sel - Select signal to choose between functional "ulp_rcv_en" or a value from software register. The effective value converges onto port "i_ana_ulps_rcv_en" of "lane_always_on" block at DPHY_RX_VBUS2APB_LANE-level |
| 8 | TM_ULP_RCV | R/W | 0h | w_tm_ulp_rcv_en - "ulp_rcv_en" value considered when selected to have it via software way |
| 7 | TM_LPRXCD_SEL | R/W | 0h | w_tm_lprxcd_sel - Select signal to choose the lprxcd's block enable value to analog between the one from "lane_always_on" or from the software way onto the port "rxda_lprxcd_en" on Analog interface |
| 6 | TM_LPRXCD | R/W | 0h | w_tm_lprxcd_en - "lprxcd_en" value considered when selected to have it via software way |
| 5-1 | TM_UNUSED_5_1 | R | 0h | RESERVED |
| 0 | TM_FORCE_TX_STOP_STATE | R/W | 0h | 0' - No force on escape mode logic - Check polarity |

11.228 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT2 Register (Offset = 510h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT2 is shown in [Figure 11-227](#) and described in [Table 11-457](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG0

Table 11-456.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0510h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0510h |

Figure 11-227. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_TEST_REG0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-457. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|--|
| 31-0 | DIG_EXTRA_TEST_REG0 | R/W | 0h | Digital Extra Functional Test Register 0 |

11.229 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT3 Register (Offset = 514h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT3 is shown in [Figure 11-228](#) and described in [Table 11-459](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg1

Table 11-458.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0514h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0514h |

Figure 11-228. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------------------|-----------------|----|----|----|----|---------------------------------|---------------------------------|
| TM_DIAG_CAL_CLOCK_GATE_EN | TM_UNUSED_30_18 | | | | | | |
| R/W-0h | R-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_30_18 | | | | | | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | TM_PREAMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_ITER_WAIT_TIME | | | | | | | TM_PREAMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-459. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31 | TM_DIAG_CAL_CLOCK_GATE_EN | R/W | 0h | While running diagnostic calibrations, this acts as calibration's clock gate enable Enable = 1 |
| 30-18 | TM_UNUSED_30_18 | R | 0h | RESERVED |
| 17 | TM_PREAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode wait time between two codes selection |
| 16-9 | TM_PREAMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode wait time between two codes |
| 8 | TM_PREAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode initial wait time selection - Select signal to choose between the one from software way or the functional one Functional value gets decided internally based on the "psm_clock_freq" input to Data-Lane |
| 7-0 | TM_PREAMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode initial wait time - "init_value" considered when selected to choose it via software way |

11.230 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4 Register (Offset = 518h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4 is shown in [Figure 11-229](#) and described in [Table 11-461](#).

Return to [Summary Table](#).

preamp_cal_ctrl_reg2

Table 11-460.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0518h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0518h |

Figure 11-229. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|-----------------------------|-----------------------|-------------------|---------------|--------------------------|-------------------------|-----------------|
| UNUSED | | | | | TM_PREAMP_ANA_CAL_EN_SEL | TM_PREAMP_ANA_CAL_EN | TM_UNUSED_24_18 |
| R-0h | | | | | R/W-0h | R/W-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_24_18 | | | | | | TM_PREAMP_CAL_CODE_TUNE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_CAL_CODE_TUNE | TM_PREAMP_CAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_CAL_OVERRIDE_CODE | TM_PREAMP_CAL_OVERRIDE_EN | TM_PREAMP_CAL_RUN_SEL | TM_PREAMP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-461. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26 | TM_PREAMP_ANA_CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 25 | TM_PREAMP_ANA_CAL_EN | R/W | 0h | test mode analog calibration enable |
| 24-18 | TM_UNUSED_24_18 | R | 0h | RESERVED |
| 17-15 | TM_PREAMP_CAL_CODE_TUNE | R/W | 0h | final preamp cal code tune value |
| 14-7 | TM_PREAMP_CAL_OVERRIDE_CODE | R/W | 0h | preamp calibration override code |
| 6 | TM_PREAMP_CAL_OVERRIDE_EN | R/W | 0h | preamp calibration code override enable |
| 5 | TM_PREAMP_CAL_RUN_SEL | R/W | 0h | test mode calibration run selection |

Table 11-461. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---------------------------|
| 4 | TM_PREAMP_CAL_RUN | R/W | 0h | test mode calibration run |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.231 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT5 Register (Offset = 51Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT5 is shown in [Figure 11-230](#) and described in [Table 11-463](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg1

Table 11-462.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT5
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 051Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 051Ch |

Figure 11-230. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT5 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|-----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | TM_DCC_COMP_CAL_ITER_WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-463. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_DCC_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration iteration time enable |
| 16-9 | TM_DCC_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode dcc comp calibration iteration time |
| 8 | TM_DCC_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode dcc comp calibration initial wait time enable |
| 7-0 | TM_DCC_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode dcc comp calibration initial wait time |

11.232 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6 Register (Offset = 520h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6 is shown in [Figure 11-231](#) and described in [Table 11-465](#).

Return to [Summary Table](#).

dcc_comp_cal_ctrl_reg2

Table 11-464.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0520h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0520h |

Figure 11-231. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6 Register

| | | | | | | | |
|---------------------------------------|-------------------------------------|---------------------------------|------------------------------------|--------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_DCC_COM P_ANA_CAL_E N_SEL | TM_DCC_COM P_ANA_CAL_E N | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DCC_COMP_CAL_CODE_TUNE | | | TM_DCC_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_OVER RIDE_CODE | TM_DCC_COM P_CAL_OVER RIDE_EN | TM_DCC_COM P_CAL_RUN_S EL | TM_DCC_COM P_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-465. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_DCC_COMP_ANA_C AL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_DCC_COMP_ANA_C AL_EN | R/W | 0h | test mode dcc comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_DCC_COMP_CAL_C ODE_TUNE | R/W | 0h | test mode dcc comp calibration code tune value |
| 12-7 | TM_DCC_COMP_CAL_O VERRIDE_CODE | R/W | 0h | test mode dcc comp calibration code overirde |
| 6 | TM_DCC_COMP_CAL_O VERRIDE_EN | R/W | 0h | test mode dcc comp calibration override code enable |
| 5 | TM_DCC_COMP_CAL_R UN_SEL | R/W | 0h | dcc comp calibration run selection |
| 4 | TM_DCC_COMP_CAL_R UN | R/W | 0h | dcc comp calibration test mode run |

Table 11-465. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.233 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT7 Register (Offset = 524h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT7 is shown in [Figure 11-232](#) and described in [Table 11-467](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg1

Table 11-466.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0524h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0524h |

Figure 11-232. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT7 Register

| | | | | | | | |
|----------------------------------|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_18 | | | | | | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME_E N | TM_MIXER_CO MP_CAL_ITER _WAIT_TIME |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_ITER_WAIT_TIME | | | | | | | TM_MIXER_CO MP_CAL_INIT _WAIT_TIME_E N |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_COMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-467. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-18 | TM_UNUSED_31_18 | R | 0h | RESERVED |
| 17 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration iteration time enable |
| 16-9 | TM_MIXER_COMP_CAL_ITER_WAIT_TIME | R/W | 0h | test mode mixer comp calibration iteration time |
| 8 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | test mode mixer comp calibration initial wait time enable |
| 7-0 | TM_MIXER_COMP_CAL_INIT_WAIT_TIME | R/W | 0h | test mode mixer comp calibration initial wait time |

11.234 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8 Register (Offset = 528h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8 is shown in [Figure 11-233](#) and described in [Table 11-469](#).

Return to [Summary Table](#).

mix_comp_cal_ctrl_reg2

Table 11-468.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0528h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0528h |

Figure 11-233. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8 Register

| | | | | | | | |
|---|---------------------------------------|-----------------------------------|--------------------------------------|----------------------------------|-----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_MIXER_CO MP_ANA_CAL_ EN_SEL | TM_MIXER_CO MP_ANA_CAL_ EN | TM_UNUSED_18_16 | | |
| R-0h | | | R/W-0h | R/W-0h | R-0h | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIXER_COMP_CAL_CODE_TUNE | | | TM_MIXER_COMP_CAL_OVERRIDE_CODE | | | | |
| R/W-0h | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_MIXER_CO MP_CAL_OVE RRIDE_CODE | TM_MIXER_CO MP_CAL_OVE RRIDE_EN | TM_MIXER_CO MP_CAL_RUN _SEL | TM_MIXER_CO MP_CAL_RUN | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-469. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_MIXER_COMP_ANA_ CAL_EN_SEL | R/W | 0h | take analog calib en from logic or test reg |
| 19 | TM_MIXER_COMP_ANA_ CAL_EN | R/W | 0h | test mode mixer comp cal analog enable |
| 18-16 | TM_UNUSED_18_16 | R | 0h | RESERVED |
| 15-13 | TM_MIXER_COMP_CAL_ CODE_TUNE | R/W | 0h | test mode mixer comp calibration code tune value |
| 12-7 | TM_MIXER_COMP_CAL_ OVERRIDE_CODE | R/W | 0h | test mode mixer comp calibration code override |
| 6 | TM_MIXER_COMP_CAL_ OVERRIDE_EN | R/W | 0h | test mode mixer comp calibration override code enable |
| 5 | TM_MIXER_COMP_CAL_ RUN_SEL | R/W | 0h | mixer comp calibration run selection |
| 4 | TM_MIXER_COMP_CAL_ RUN | R/W | 0h | mixer comp calibration test mode run |

Table 11-469. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT8 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|-------------|
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.235 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT9 Register (Offset = 52Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT9 is shown in [Figure 11-234](#) and described in [Table 11-471](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg1

Table 11-470.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT9
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 052Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 052Ch |

Figure 11-234. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT9 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-471. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_POS_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | posedge sampler calibration iteration time between codes |
| 7-0 | TM_POS_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | posedge sampler calibration initial wait time |

11.236 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10 Register (Offset = 530h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10 is shown in [Figure 11-235](#) and described in [Table 11-473](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg2

Table 11-472.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0530h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0530h |

Figure 11-235. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_MCAL_OVERRIDE_EN | TM_POS_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_PCAL_OVERRIDE_CODE | TM_POS_SAMP_PCAL_OVERRIDE_EN | TM_POS_SAMP_CAL_RUN | TM_POS_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-473. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_POS_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode iteration wait time enable |
| 30 | TM_POS_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | posedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_POS_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override mcal_code |
| 15 | TM_POS_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration mcal_code override en |
| 14-7 | TM_POS_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | posedge sampler calibration override pcal_code |
| 6 | TM_POS_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | posedge sampler calibration pcal_code override en |
| 5 | TM_POS_SAMP_CAL_RUN | R/W | 0h | posedge sampler calibration test mode run |

Table 11-473. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT10 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_POS_SAMP_CAL_R UN_SEL | R/W | 0h | posedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.237 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT11 Register (Offset = 534h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT11 is shown in [Figure 11-236](#) and described in [Table 11-475](#).

Return to [Summary Table](#).

pos_samp_cal_ctrl_reg3

Table 11-474.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT11
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0534h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0534h |

Figure 11-236. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT11 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_POS_SAMP_ANA_CAL_EN_SEL | TM_POS_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_POS_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-475. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_POS_SAMP_ANA_CAL_EN_SEL | R/W | 0h | posedge sampler calibration analog calib enable selection |
| 8 | TM_POS_SAMP_ANA_CAL_EN | R/W | 0h | posedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_POS_SAMP_CAL_CODE_TUNE | R/W | 0h | posedge sampler calibration tune code |

11.238 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT12 Register (Offset = 538h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT12 is shown in [Figure 11-237](#) and described in [Table 11-477](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg1

Table 11-476.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT12
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0538h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0538h |

Figure 11-237. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT12 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_CAL_INIT_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-477. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-16 | TM_UNUSED_31_16 | R | 0h | RESERVED |
| 15-8 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME | R/W | 0h | negedge sampler calibration iteration time between codes |
| 7-0 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME | R/W | 0h | negedge sampler calibration initial wait time |

11.239 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13 Register (Offset = 53Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13 is shown in [Figure 11-238](#) and described in [Table 11-479](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg2

Table 11-478.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 053Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 053Ch |

Figure 11-238. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------------|---------------------|-------------------------|---------------|----|----|----|
| TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | TM_UNUSED_29_24 | | | | | |
| R/W-0h | R/W-0h | R-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_MCAL_OVERRIDE_CODE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_MCAL_OVERRIDE_EN | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_PCAL_OVERRIDE_CODE | TM_NEG_SAMP_PCAL_OVERRIDE_EN | TM_NEG_SAMP_CAL_RUN | TM_NEG_SAMP_CAL_RUN_SEL | TM_UNUSED_3_0 | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-479. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31 | TM_NEG_SAMP_CAL_ITER_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode iteration wait time enable |
| 30 | TM_NEG_SAMP_CAL_INIT_WAIT_TIME_EN | R/W | 0h | negedge sampler calibration test mode initial wait time enable |
| 29-24 | TM_UNUSED_29_24 | R | 0h | RESERVED |
| 23-16 | TM_NEG_SAMP_MCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override mcal_code |
| 15 | TM_NEG_SAMP_MCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration mcal_code override en |
| 14-7 | TM_NEG_SAMP_PCAL_OVERRIDE_CODE | R/W | 0h | negedge sampler calibration override pcal_code |
| 6 | TM_NEG_SAMP_PCAL_OVERRIDE_EN | R/W | 0h | negedge sampler calibration pcal_code override en |
| 5 | TM_NEG_SAMP_CAL_RUN | R/W | 0h | negedge sampler calibration test mode run |

Table 11-479. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT13 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------------|------|-------|---|
| 4 | TM_NEG_SAMP_CAL_R UN_SEL | R/W | 0h | negedge sampler calibration test mode selection |
| 3-0 | TM_UNUSED_3_0 | R | 0h | RESERVED |

11.240 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT14 Register (Offset = 540h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT14 is shown in [Figure 11-239](#) and described in [Table 11-481](#).

Return to [Summary Table](#).

neg_samp_cal_ctrl_reg3

Table 11-480.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT14
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0540h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0540h |

Figure 11-239. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT14 Register

| | | | | | | | |
|---------------|----|----|----|----|---------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | TM_NEG_SAMP_ANA_CAL_EN_SEL | TM_NEG_SAMP_ANA_CAL_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_UNUSED_7_3 | | | | | TM_NEG_SAMP_CAL_CODE_TUNE | | |
| R-0h | | | | | R/W-0h | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-481. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9 | TM_NEG_SAMP_ANA_CAL_EN_SEL | R/W | 0h | negedge sampler calibration analog calib enable selection |
| 8 | TM_NEG_SAMP_ANA_CAL_EN | R/W | 0h | negedge sampler calibration analog calibration enable |
| 7-3 | TM_UNUSED_7_3 | R | 0h | RESERVED |
| 2-0 | TM_NEG_SAMP_CAL_CODE_TUNE | R/W | 0h | negedge sampler calibration tune code |

11.241 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT15 Register (Offset = 544h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT15 is shown in [Figure 11-240](#) and described in [Table 11-483](#).

Return to [Summary Table](#).

skew_cal_fsm_reg1

Table 11-482.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT15
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0544h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0544h |

Figure 11-240. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT15 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|----|----|--------------------------------|------------------------------------|-----------------------------------|------------------------------|------------------------------|
| UNUSED | | | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | |
| R-0h | | | R/W-0h | R/W-0h | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | | | | | | TM_SKEW_CAL_FPHASE_WAIT_TIME | |
| R/W-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_FPHASE_WAIT_TIME | | | | | | | TM_SKEW_CAL_TIMER_INIT_COUNT |
| R/W-0h | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-483. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT | R/W | 0h | skew calibration analog max saturation test mode enable |
| 27 | TM_SKEW_CAL_ANA_DESKEW_MAX_SAT_SEL | R/W | 0h | skew calibration analog max saturation selection |
| 26-18 | TM_SKEW_CAL_FPHASE_LONG_WAIT_TIME | R/W | 0h | skew calibration fast phase long wait time |
| 17-9 | TM_SKEW_CAL_FPHASE_WAIT_TIME | R/W | 0h | skew calibration fast phase wait time |
| 8-0 | TM_SKEW_CAL_TIMER_INIT_COUNT | R/W | 0h | skew calibration initial wait time |

11.242 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT16 Register (Offset = 548h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT16 is shown in [Figure 11-241](#) and described in [Table 11-485](#).

Return to [Summary Table](#).

skew_cal_fsm_reg2

Table 11-484.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT16
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0548h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0548h |

Figure 11-241. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT16 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|------------------------------------|------------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | |
| R-0h | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_SKEW_CAL_ACC_CODE_MAX_VALUE | | | | | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SKEW_CAL_ACC_CODE_MIN_VALUE | | | | | | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | TM_SKEW_CAL_SPHASE_WAIT_TIME |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_SPHASE_WAIT_TIME | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-485. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-27 | UNUSED | R | 0h | RESERVED |
| 26-19 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE | R/W | 0h | skew calibration delay code test mode max value |
| 18 | TM_SKEW_CAL_ACC_CODE_MAX_VALUE_SEL | R/W | 0h | skew calibration max code test reg selection |
| 17-10 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE | R/W | 0h | skew calibration delay code test mode min value |
| 9 | TM_SKEW_CAL_ACC_CODE_MIN_VALUE_SEL | R/W | 0h | skew calibration min code test reg selection |
| 8-0 | TM_SKEW_CAL_SPHASE_WAIT_TIME | R/W | 0h | skew calibration slow phase wait time |

11.243 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT17 Register (Offset = 54Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT17 is shown in [Figure 11-242](#) and described in [Table 11-487](#).

Return to [Summary Table](#).

skew_cal_fsm_reg3

Table 11-486.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT17
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 054Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 054Ch |

Figure 11-242. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT17 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_SKEW_CAL_DESKEW_START_CODE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-487. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------------|------|-------|-------------------------------------|
| 31-8 | UNUSED | R | 0h | RESERVED |
| 7-0 | TM_SKEW_CAL_DESKEW_START_CODE | R/W | 0h | skew calibration initial start code |

11.244 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT18 Register (Offset = 550h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT18 is shown in [Figure 11-243](#) and described in [Table 11-489](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg1

Table 11-488.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT18
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0550h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0550h |

Figure 11-243. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT18 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_TIMER_ITER_COUNT | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_TIMER_ITER_COUNT | | | | | | TM_DUCY_CORR_TIMER_INIT_COUNT | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CORR_TIMER_INIT_COUNT | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-489. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-9 | TM_DUCY_CORR_TIME_R_ITER_COUNT | R/W | 0h | duty cycle correction iteration wait time specified in this register will be considered when a non-zero value is specified here |
| 8-0 | TM_DUCY_CORR_TIME_R_INIT_COUNT | R/W | 0h | duty cycle correction initial wait time specified in this register will be considered when a non-zero value is specified here |

11.245 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT19 Register (Offset = 554h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT19 is shown in [Figure 11-244](#) and described in [Table 11-491](#).

Return to [Summary Table](#).

ducy_corr_ctrl_reg2

Table 11-490.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT19
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0554h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0554h |

Figure 11-244. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT19 Register

| | | | | | | | |
|---------------------------------|-------------------------------------|-----------------------------|-------------------------------------|---------------------------------|----|---------------------------------|---------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DUCY_CORR_ACC_CODE_MAX_VALUE | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DUCY_CORR_ACC_CODE_MAX_VALUE | | | TM_DUCY_CORR_ACC_CODE_MAX_VALUE_SEL | TM_DUCY_CORR_ACC_CODE_MIN_VALUE | | | |
| R/W-0h | | | R/W-0h | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DUCY_CORR_ACC_CODE_MIN_VALUE | TM_DUCY_CORR_ACC_CODE_MIN_VALUE_SEL | TM_DUCY_CORR_ACC_START_CODE | | | | | TM_DUCY_CORR_ACC_START_CODE_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-491. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-13 | TM_DUCY_CORR_ACC_CODE_MAX_VALUE | R/W | 0h | duty cycle correction test mode max value |
| 12 | TM_DUCY_CORR_ACC_CODE_MAX_VALUE_SEL | R/W | 0h | duty cycle correction test mode max value selection |
| 11-7 | TM_DUCY_CORR_ACC_CODE_MIN_VALUE | R/W | 0h | duty cycle correction test mode min value |
| 6 | TM_DUCY_CORR_ACC_CODE_MIN_VALUE_SEL | R/W | 0h | duty cycle correction test mode min value selection |
| 5-1 | TM_DUCY_CORR_ACC_START_CODE | R/W | 0h | duty cycle correction test mode start code |
| 0 | TM_DUCY_CORR_ACC_START_CODE_SEL | R/W | 0h | duty cycle correction test mode start code selection |

11.246 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20 Register (Offset = 558h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20 is shown in [Figure 11-245](#) and described in [Table 11-493](#).

Return to [Summary Table](#).

skew_cal_avg_reg1

Table 11-492.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0558h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0558h |

Figure 11-245. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|--------------------------|----------------------------------|---------------------|----|----|---------------------------------|------------------------------------|------------------------------------|
| TM_ANA_DES KEW_DCC_EN | TM_ANA_DES KEW_DCC_EN _SEL | TM_DCC_CODE_TUNE | | | TM_DCC_COD E_OVERRIDE_ EN | TM_DCC_CODE_OVERRIDE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DCC_CODE_OVERRIDE | | TM_DESKEW_CODE_TUNE | | | | | TM_DESKEW_ CODE_OVERR IDE_EN |
| R/W-0h | | R/W-0h | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_CODE_OVERRIDE | | | | | | TM_PROC_TIM ER_LOAD_VAL | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PROC_TIMER_LOAD_VAL | | | | | | TM_PROC_TIM ER_LOAD_VAL _SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-493. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---|
| 31 | TM_ANA_DESKEW_DCC_EN | R/W | 0h | test mode analog deskew enable |
| 30 | TM_ANA_DESKEW_DCC_EN_SEL | R/W | 0h | test mode deskew analog enable selection |
| 29-27 | TM_DCC_CODE_TUNE | R/W | 0h | duty cycle correction code tune |
| 26 | TM_DCC_CODE_OVERRIDE_EN | R/W | 0h | duty cycle correction code override enable |
| 25-22 | TM_DCC_CODE_OVERRIDE | R/W | 0h | duty cycle correction override code |
| 21-17 | TM_DESKEW_CODE_TUNE | R/W | 0h | skew calibration delay line code tune |
| 16 | TM_DESKEW_CODE_OVERRIDE_EN | R/W | 0h | skew calibration delay code override enable |
| 15-9 | TM_DESKEW_CODE_OVERRIDE | R/W | 0h | skew calibration delay line override code |

Table 11-493. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|---|
| 8-1 | TM_PROC_TIMER_LOAD_VAL | R/W | 0h | skew calibration process time test mode value |
| 0 | TM_PROC_TIMER_LOAD_VAL_SEL | R/W | 0h | skew calibration process time test mode value selection |

11.247 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT21 Register (Offset = 55Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT21 is shown in [Figure 11-246](#) and described in [Table 11-495](#).

[Return to Summary Table.](#)

skew_cal_avg_reg2

Table 11-494.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT21
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 055Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 055Ch |

Figure 11-246. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT21 Register

| | | | | | | | |
|-----------------------------|----|----|----|----|----|---------------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG_LEN_TMR_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG_LEN_TMR_LOAD_VAL | | | | | | TM_AVG2AVG_LEN_TMR_LOAD_VAL_SEL | TM_DCC_ACC_LEN_TMR_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC_LEN_TMR_LOAD_VAL | | | | | | TM_DCC_ACC_LEN_TMR_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-495. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG_LEN_TMR_LOAD_VAL | R/W | 0h | delay line code averaging to dcc code averaging wait time |
| 9 | TM_AVG2AVG_LEN_TMR_LOAD_VAL_SEL | R/W | 0h | delay line code averaging to dcc code averaging wait time selection |
| 8-1 | TM_DCC_ACC_LEN_TMR_LOAD_VAL | R/W | 0h | total number of dcc codes to be taken for averaging in test mode |
| 0 | TM_DCC_ACC_LEN_TMR_LOAD_VAL_SEL | R/W | 0h | test mode selection value for test mode number of dcc codes under averaging |

11.248 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT22 Register (Offset = 560h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT22 is shown in [Figure 11-247](#) and described in [Table 11-497](#).

Return to [Summary Table](#).

skew_cal_avg_reg3

Table 11-496.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT22
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0560h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0560h |

Figure 11-247. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT22 Register

| | | | | | | | |
|--|----|----|----|----|----|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ DONE_LEN TIMER_LOAD_ VAL_SEL | TM_DESKEW_ ACC_LEN G_TIMER_LOAD_ VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | | | | | | TM_DESKEW_ ACC_LEN G_TIMER_LOAD_ VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-497. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL | R/W | 0h | after skew calibration is done, length of wait timer |
| 9 | TM_DESKEW_DONE_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | test mode selection value for length of wait time after deskew |
| 8-1 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL | R/W | 0h | number of deskew dealy codes to be taken for averaging |
| 0 | TM_DESKEW_ACC_LEN G_TIMER_LOAD_VAL_ SEL | R/W | 0h | tets mode selction for test mode number of delay line codes for averaging |

11.249 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT23 Register (Offset = 564h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT23 is shown in [Figure 11-248](#) and described in [Table 11-499](#).

Return to [Summary Table](#).

skew_cal_avg_reg4

Table 11-498.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT23
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0564h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0564h |

Figure 11-248. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT23 Register

| | | | | | | | |
|-------------------------------|----|----|----|----|----|-----------------------------------|-------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_AVG2AVG_RES_TIMER_LOAD_VAL | | | | | | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | TM_DCC_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_ACC_RES_TIMER_LOAD_VAL | | | | | | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-499. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_AVG2AVG_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging to deskew averaging wait time in test mode |
| 9 | TM_AVG2AVG_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging to deskew averaging wait time |
| 8-1 | TM_DCC_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of dcc averaging wait time in test mode |
| 0 | TM_DCC_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selection of resolution time of dcc averaging wait time |

11.250 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT24 Register (Offset = 568h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT24 is shown in [Figure 11-249](#) and described in [Table 11-501](#).

Return to [Summary Table](#).

skew_cal_avg_reg5

Table 11-500.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT24
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0568h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0568h |

Figure 11-249. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT24 Register

| | | | | | | | |
|-----------------------------------|----|----|----|----|----|---------------------------------------|--------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | |
| R-0h | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | | | | | | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | | | | | | | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-501. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------------|------|-------|---|
| 31-18 | UNUSED | R | 0h | RESERVED |
| 17-10 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew done wait time in test mode |
| 9 | TM_DESKEW_DONE_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | test mode selction of resolution time of deskew done wait time in test mode |
| 8-1 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL | R/W | 0h | resolution time of deskew averaging wait time in test mode |
| 0 | TM_DESKEW_ACC_RES_TIMER_LOAD_VAL_SEL | R/W | 0h | tets mode selection of resolution time of deskew averaging wait time in test mode |

11.251 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT25 Register (Offset = 56Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT25 is shown in [Figure 11-250](#) and described in [Table 11-503](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG0

Table 11-502.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT25
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 056Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 056Ch |

Figure 11-250. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-503. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT0 | R | 0h | RESERVED |

11.252 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT26 Register (Offset = 570h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT26 is shown in [Figure 11-251](#) and described in [Table 11-505](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_CALIB_REG1

Table 11-504.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT26
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0570h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0570h |

Figure 11-251. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIB_EXTRA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-505. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------|
| 31-0 | DIG_CALIB_EXTRA_TBIT1 | R | 0h | RESERVED |

11.253 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT27 Register (Offset = 574h) [reset = 0A000018h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT27 is shown in [Figure 11-252](#) and described in [Table 11-507](#).

Return to [Summary Table](#).

bist_config_reg1

Table 11-506.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT27
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0574h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0574h |

Figure 11-252. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT27 Register

| | | | | | | | |
|---------------------|----|----|--------------|----|-------------|-----------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TM_IDLE_TIME_LENGTH | | | | | | | |
| R/W-Ah | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_23_8 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_MODE | | | TM_PRBS_MODE | | TM_UNUSED_2 | TM_FREEZE | TM_BIST_EN |
| R/W-0h | | | R/W-3h | | R-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-507. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|--|
| 31-24 | TM_IDLE_TIME_LENGTH | R/W | Ah | BIST_IDLE_TIME |
| 23-8 | TM_UNUSED_23_8 | R | 0h | RESERVED |
| 7-5 | TM_TEST_MODE | R/W | 0h | PRBS mode - when set to '1' PRBS mode is selected |
| 4-3 | TM_PRBS_MODE | R/W | 3h | BIST PRBS MODE 9 when 0x0 |
| 2 | TM_UNUSED_2 | R | 0h | RESERVED |
| 1 | TM_FREEZE | R/W | 0h | Freeze the LFSR contents after every packet or frame |
| 0 | TM_BIST_EN | R/W | 0h | Enable signal for pattern checker |

11.254 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT28 Register (Offset = 578h) [reset = DECDBCABh]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT28 is shown in [Figure 11-253](#) and described in [Table 11-509](#).

Return to [Summary Table](#).

bist_config_reg2

Table 11-508.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT28
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0578h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0578h |

Figure 11-253. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|--------------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_TEST_PAT4 | | | | | | | | TM_TEST_PAT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_TEST_PAT2 | | | | | | | | TM_TEST_PAT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-509. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-24 | TM_TEST_PAT4 | R/W | DEh | User registers to specify the BIST data4 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 23-16 | TM_TEST_PAT3 | R/W | CDh | User registers to specify the BIST data3 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 15-8 | TM_TEST_PAT2 | R/W | BCh | User registers to specify the BIST data2 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |
| 7-0 | TM_TEST_PAT1 | R/W | ABh | User registers to specify the BIST data1 Based on the default_mode setting design will consider either of the hard-value from RTL [or] the soft-value provided here |

11.255 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT29 Register (Offset = 57Ch) [reset = 28h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT29 is shown in [Figure 11-254](#) and described in [Table 11-511](#).

Return to [Summary Table](#).

bist_config_reg3

Table 11-510.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT29
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 057Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 057Ch |

Figure 11-254. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT29 Register

| | | | | | | | |
|-----------------|----|----|---------------|-----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | TM_CLEAR_BIST | TM_UNUSED_27_12 | | | |
| R-0h | | | R/W-0h | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_UNUSED_27_12 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_UNUSED_27_12 | | | | TM_PKT_LENGTH | | | |
| R-0h | | | | R/W-28h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PKT_LENGTH | | | | | | | |
| R/W-28h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-511. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28 | TM_CLEAR_BIST | R/W | 0h | Setting this will clear all the BIST related flags and counters |
| 27-12 | TM_UNUSED_27_12 | R | 0h | RESERVED |
| 11-0 | TM_PKT_LENGTH | R/W | 28h | Based on the default_mode design will consider the run-length from design or the programmed value specified here |

11.256 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT30 Register (Offset = 580h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT30 is shown in [Figure 11-255](#) and described in [Table 11-513](#).

Return to [Summary Table](#).

bist_config_reg4

Table 11-512.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT30
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0580h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0580h |

Figure 11-255. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT30 Register

| | | | | | | | |
|--------|----|----|----|----|----|---------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | TM_LPRX_BIS T_EN | TM_HSRX_BIS T_EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-513. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-2 | UNUSED | R | 0h | RESERVED |
| 1 | TM_LPRX_BIST_EN | R/W | 0h | LPRX BIST is enbaled - rxda_lprx_bist_en - When '1', LP BIST is enabled |
| 0 | TM_HSRX_BIST_EN | R/W | 0h | HSRX BIST is enbaled - rxda_hsrx_bist_en - when '1', HS BIST is enabled |

11.257 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT31 Register (Offset = 584h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT31 is shown in [Figure 11-256](#) and described in [Table 11-515](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG1

Table 11-514.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT31
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0584h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0584h |

Figure 11-256. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-515. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT1 | R | 0h | RESERVED |

11.258 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT32 Register (Offset = 588h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT32 is shown in [Figure 11-257](#) and described in [Table 11-517](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_TEST_REG2

Table 11-516.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT32
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0588h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0588h |

Figure 11-257. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_FUNC_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-517. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_FUNC_TBIT2 | R | 0h | RESERVED |

11.259 DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT2 Register (Offset = 58Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT2 is shown in [Figure 11-258](#) and described in [Table 11-519](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 11-518.
DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 058Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 058Ch |

Figure 11-258. DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ANA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-519. DPHY_RX_VBUS2APB_DL3_RX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | ANA_READ_TBIT0 | R | 0h | Analog read register 0 |

11.260 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT33 Register (Offset = 590h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT33 is shown in [Figure 11-259](#) and described in [Table 11-521](#).

Return to [Summary Table](#).

deserialiser_fsm_status

Table 11-520.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT33
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0590h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0590h |

Figure 11-259. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|------------------|----|-------------|----|----|----|-------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | TM_PPI_CUR_STATE | | | | | | TM_CTRL_CUR_STATE | | | |
| R-0h | | | | | | R-0h | | | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_CTRL_CUR_STATE | | | | | | | | TM_SYNC_PKT | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-521. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-26 | UNUSED | R | 0h | RESERVED |
| 25-18 | TM_PPI_CUR_STATE | R | 0h | Current State of the SYNC detection FSM during the HS data receive mode or skew calibration mode |
| 17-8 | TM_CTRL_CUR_STATE | R | 0h | current state status of HS receive FSM |
| 7-0 | TM_SYNC_PKT | R | 0h | Status of received SYNC packet |

11.261 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT34 Register (Offset = 594h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT34 is shown in [Figure 11-260](#) and described in [Table 11-523](#).

Return to [Summary Table](#).

lp_status

Table 11-522.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT34
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0594h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0594h |

Figure 11-260. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT34 Register

| | | | | | | | |
|--------------------|----|--------------|----|--------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | TM_LP_RX_CUR_STATE | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_LP_RX_CUR_STATE | | TM_LP_STATUS | | | | | |
| R-0h | | R-0h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-523. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|--|
| 31-19 | UNUSED | R | 0h | RESERVED |
| 18-14 | TM_LP_RX_CUR_STATE | R | 0h | Current state of LP receiver FSM |
| 13-8 | TM_LP_STATUS | R | 0h | Status of DP,DN pins of LPRX, LPCD, ULPRX respectively |
| 7-0 | UNUSED_7_0 | R | 0h | RESERVED |

11.262 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT35 Register (Offset = 598h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT35 is shown in [Figure 11-261](#) and described in [Table 11-525](#).

Return to [Summary Table](#).

DIGITAL_EXTRA_READ_REG0

Table 11-524.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT35
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0598h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0598h |

Figure 11-261. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-525. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.263 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36 Register (Offset = 59Ch) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36 is shown in [Figure 11-262](#) and described in [Table 11-527](#).

Return to [Summary Table](#).

dcc_mixer_comparator_calibration_stat

Table 11-526.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 059Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 059Ch |

Figure 11-262. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36 Register

| | | | | | | | |
|--------------------------|--------------------------|---------------------|----|----|----|---------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | TM_MIX_COM P_ANA_RESP | TM_MIX_COMP_CALCODE | | | | TM_MIX_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_MIX_COM P_CAL_DONE | TM_DCC_COM P_ANA_RESP | TM_DCC_COMP_CALCODE | | | | TM_DCC_COM P_CAL_NO_RE SP | |
| R-0h | R-0h | R-0h | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DCC_COM P_CAL_DONE | TM_CALIB_CTRL_CUR_STATE | | | | | TM_CUR_DRX _CAL_DONE | |
| R-0h | R-0h | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-527. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-23 | UNUSED | R | 0h | RESERVED |
| 22 | TM_MIX_COMP_ANA_RESP | R | 0h | Mixer comparator analog response |
| 21-17 | TM_MIX_COMP_CALCODE | R | 0h | Mixer comparator calibration code |
| 16 | TM_MIX_COMP_CAL_NO_RESP | R | 0h | Mixer comparator calibration has no response from analog |
| 15 | TM_MIX_COMP_CAL_DONE | R | 0h | Mixer comparator calibration is done properly |
| 14 | TM_DCC_COMP_ANA_RESP | R | 0h | Duty Cycle Comparator analog response |
| 13-9 | TM_DCC_COMP_CALCODE | R | 0h | Duty cycle corrector comparator calibration code |
| 8 | TM_DCC_COMP_CAL_NO_RESP | R | 0h | Duty cycle corrector comparator calibration has no response from analog |

Table 11-527. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT36 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7 | TM_DCC_COMP_CAL_DONE | R | 0h | Duty cycle corrector comparator calibration is done properly |
| 6-1 | TM_CALIB_CTRL_CUR_STATE | R | 0h | If struck, indicates calibration FSM current state |
| 0 | TM_CUR_DRX_CAL_DONE | R | 0h | Current DRX DPHY_RX_VBUS2APB_LANE calibrations are done |

11.264 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37 Register (Offset = 5A0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37 is shown in [Figure 11-263](#) and described in [Table 11-529](#).

Return to [Summary Table](#).

preamp_cal_status_reg1

Table 11-528.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 05A0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 05A0h |

Figure 11-263. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------|-----------------------------|----|-----------------------------|--------------------------|---------------------------------|-------------------------|-----------------------------------|
| TM_ANA_RES_P_STAT | TM_PREAMP_STAT_ANA_CAL_CODE | | | | | | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE |
| R-0h | R-0h | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | | | | | | | TM_PREAMP_STAT_NCAL_PREAMP_CODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_PREAMP_STAT_NCAL_PREAMP_CODE | | | | | TM_PREAMP_STAT_PCAL_PREAMP_CODE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_PREAMP_STAT_PCAL_PREAMP_CODE | TM_PREAMP_STAT_NCAL_NO_RESP | | TM_PREAMP_STAT_PCAL_NO_RESP | TM_PREAMP_STAT_NCAL_DONE | TM_PREAMP_STAT_PCAL_DONE | TM_PREAMP_STAT_CAL_DONE | |
| R-0h | R-0h | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-529. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31 | TM_ANA_RESP_STAT | R | 0h | current analog or test mode response for which calibration is happening |
| 30-25 | TM_PREAMP_STAT_ANA_CAL_CODE | R | 0h | code going to analog |
| 24-17 | TM_PREAMP_STAT_ANA_FINAL_CAL_CODE | R | 0h | code decided to send to analog before tune |
| 16-11 | TM_PREAMP_STAT_NCAL_PREAMP_CODE | R | 0h | calib code in posedge_data run |
| 10-5 | TM_PREAMP_STAT_PCAL_PREAMP_CODE | R | 0h | calib code in negedge_data run |
| 4 | TM_PREAMP_STAT_NCAL_NO_RESP | R | 0h | negedge_data run has no response |
| 3 | TM_PREAMP_STAT_PCAL_NO_RESP | R | 0h | posedge_data run has no response |
| 2 | TM_PREAMP_STAT_NCAL_DONE | R | 0h | negedge_data cal run is done |

Table 11-529. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT37 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|------------------------------|
| 1 | TM_PREAMP_STAT_PCA L_DONE | R | 0h | posedge_data cal run is done |
| 0 | TM_PREAMP_STAT_CAL _DONE | R | 0h | preamp calibration is done |

11.265 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38 Register (Offset = 5A4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38 is shown in [Figure 11-264](#) and described in [Table 11-531](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg1

Table 11-530.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05A4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05A4h |

Figure 11-264. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38 Register

| | | | | | | | |
|---------------------------------|----|----|----------------------------|---------------------------------|---------------------------------|------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_POS_SAMP_STAT_SAMP_DONE | TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_POS_SAMP_STAT_UP_CAL_CODE | TM_POS_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_UP_CAL_CODE | | | | | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | TM_POS_SAMP_STAT_UP_CAL_DONE | |
| R-0h | | | | | R-0h | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-531. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_POS_SAMP_STAT_SAMP_DONE | R | 0h | posedge sampler calibration is done |
| 19-11 | TM_POS_SAMP_STAT_FINAL_CAL_CODE | R | 0h | posedge sampler calibration final code |
| 10 | TM_POS_SAMP_STAT_UP_CAL_CODE_TYPE | R | 0h | code type that is changing for posedged sampler |
| 9-2 | TM_POS_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for posedged sampler |
| 1 | TM_POS_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-531. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT38 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_POS_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.266 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT39 Register (Offset = 5A8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT39 is shown in [Figure 11-265](#) and described in [Table 11-533](#).

Return to [Summary Table](#).

pos_samp_cal_status_reg2

Table 11-532.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT39
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05A8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05A8h |

Figure 11-265. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT39 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|--|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_POS_SAMP P_ANA_CAL_R ESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_POS_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_POS_SAMP P_STAT_ANA_ CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_POS_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_POS_SAMP_STAT_DOWN_ CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_POS_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_POS_SAMP P_STAT_NO_D OWN_CAL_RE SP | TM_POS_SAMP P_STAT_DOW N_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-533. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_POS_SAMP_ANA_CAL_RESP | R | 0h | test mode status of posedge sampler |
| 23-17 | TM_POS_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to posedge sampler |
| 16-10 | TM_POS_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to posedge sampler |
| 9-2 | TM_POS_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for posedge sampler |
| 1 | TM_POS_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_POS_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.267 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40 Register (Offset = 5ACh) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40 is shown in [Figure 11-266](#) and described in [Table 11-535](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg1

Table 11-534.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05ACh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05ACh |

Figure 11-266. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40 Register

| | | | | | | | |
|---------------------------------|----|----|---|---------------------------------|----------------------------|---------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | |
| R-0h | | | R-0h | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_FINAL_CAL_CODE | | | | | TM_NEG_SAMP_STAT_CODE_TYPE | TM_NEG_SAMP_STAT_UP_CAL_CODE | |
| R-0h | | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_UP_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_UP_CAL_RESP | TM_NEG_SAMP_STAT_UP_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-535. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|--|
| 31-21 | UNUSED | R | 0h | RESERVED |
| 20 | TM_NEG_SAMP_STAT_SAMP LTM_NEG_SAMP_STAT_CAL_DONE | R | 0h | negedge sampler calibration is done |
| 19-11 | TM_NEG_SAMP_STAT_FINAL_CAL_CODE | R | 0h | negedge sampler calibration final code |
| 10 | TM_NEG_SAMP_STAT_CODE_TYPE | R | 0h | code type that is changing for negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_UP_CAL_CODE | R | 0h | up check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_UP_CAL_RESP | R | 0h | up check calib run code has no analog response |

Table 11-535. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT40 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------------------|------|-------|------------------------------|
| 0 | TM_NEG_SAMP_STAT_U P_CAL_DONE | R | 0h | up check calibration is done |

11.268 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT41 Register (Offset = 5B0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT41 is shown in [Figure 11-267](#) and described in [Table 11-537](#).

Return to [Summary Table](#).

neg_samp_cal_status_reg2

Table 11-536.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT41
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05B0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05B0h |

Figure 11-267. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT41 Register

| | | | | | | | |
|--------------------------------|----|----|----|----|----|-----------------------------------|--------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | TM_NEG_SAMP_ANA_CAL_RESP |
| R-0h | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_NEG_SAMP_STAT_ANA_CAL_MCODE | | | | | | | TM_NEG_SAMP_STAT_ANA_CAL_PCODE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_NEG_SAMP_STAT_ANA_CAL_PCODE | | | | | | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | |
| R-0h | | | | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_NEG_SAMP_STAT_DOWN_CAL_CODE | | | | | | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | TM_NEG_SAMP_STAT_DOWN_CAL_DONE |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-537. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT41 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-25 | UNUSED | R | 0h | RESERVED |
| 24 | TM_NEG_SAMP_ANA_CAL_RESP | R | 0h | test mode status of negedge sampler |
| 23-17 | TM_NEG_SAMP_STAT_ANA_CAL_MCODE | R | 0h | final m code going to negedge sampler |
| 16-10 | TM_NEG_SAMP_STAT_ANA_CAL_PCODE | R | 0h | final p code going to negedge sampler |
| 9-2 | TM_NEG_SAMP_STAT_DOWN_CAL_CODE | R | 0h | down check calib run code for negedge sampler |
| 1 | TM_NEG_SAMP_STAT_NO_DOWN_CAL_RESP | R | 0h | down check calib run code has no analog response |
| 0 | TM_NEG_SAMP_STAT_DOWN_CAL_DONE | R | 0h | down check calibration is done |

11.269 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42 Register (Offset = 5B4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42 is shown in [Figure 11-268](#) and described in [Table 11-539](#).

[Return to Summary Table.](#)

skew_cal_fsm_status_reg1

Table 11-538.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 05B4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 05B4h |

Figure 11-268. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------------------------|-------------------------------------|----|-------------------------|----|-----------------------------------|-----------------------------------|----|
| UNUSED | | | TM_DESKEW_DCC_CUR_STATE | | | | |
| R-0h | | | R-0h | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_CUR_STATE | TM_DESKEW_DCC_INIT_MIXER_VALUE | | TM_SP_FIRST_TRIP_CODE | | | | |
| R-0h | R-0h | | R-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_SP_FIRST_TRIP_CODE | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | | | | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | |
| R-0h | R-0h | | | | R-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | | | | | | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | |
| R-0h | | | | | | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 11-539. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-29 | UNUSED | R | 0h | RESERVED |
| 28-22 | TM_DESKEW_DCC_CUR_STATE | R | 0h | Duty cycle correction logic current state |
| 21 | TM_DESKEW_DCC_INIT_MIXER_VALUE | R | 0h | Duty cycle correction initial comparator value |
| 20-14 | TM_SP_FIRST_TRIP_CODE | R | 0h | slow phase first trip code |
| 13-10 | TM_DESKEW_DCC_CUTM_DESKEW_DCC_STATE | R | 0h | current state of the deskew FSM |
| 9 | TM_DESKEW_DCC_MAX_SAT_SECOND_TIME | R | 0h | if asserted, deskew FSM has gone into max saturation second time |
| 8 | TM_DESKEW_DCC_MAX_SAT_FIRST_TIME | R | 0h | if asserted, deskew FSM has got saturated once |

Table 11-539. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT42 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------------|------|-------|--------------------------------------|
| 7-1 | TM_DESKEW_DCC_FAST_PHASE_TRIP_CODE | R | 0h | deskew FSM fast phase trip code |
| 0 | TM_DESKEW_DCC_MIX_COMP_INIT_VALUE | R | 0h | deskew algorithm mixer initial value |

11.270 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT43 Register (Offset = 5B8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT43 is shown in [Figure 11-269](#) and described in [Table 11-541](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg1

Table 11-540.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT43
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05B8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05B8h |

Figure 11-269. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT43 Register

| | | | | | | | |
|-------------------------------------|----|----------------------------------|-------------------------------------|----|-------------------------------|--------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | | | | | | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | |
| R-0h | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TM_DESKEW_DCC_AVG_ANA_DCC_CODE | | | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | | | |
| R-0h | | | R-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | | | TM_DESKEW_DCC_AVG_DONE_DESKEW | | TM_DESKEW_DCC_AVG_DONE_DCC |
| R-0h | | R-0h | | | R-0h | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-541. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT43 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|--|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-17 | TM_DESKEW_DCC_AVG_ANA_SKEW_CAL_CODE | R | 0h | final code going to delay line |
| 16-13 | TM_DESKEW_DCC_AVG_ANA_DCC_CODE | R | 0h | final code going to duty cycle corrector |
| 12-6 | TM_DESKEW_DCC_AVG_DESKEW_FINAL_CODE | R | 0h | delay line code before tuning |
| 5-2 | TM_DESKEW_DCC_AVG_DCC_FINAL_CODE | R | 0h | duty code before tuning |
| 1 | TM_DESKEW_DCC_AVG_DONE_DESKEW | R | 0h | skew calibration is done |
| 0 | TM_DESKEW_DCC_AVG_DONE_DCC | R | 0h | duty cycle correction is done |

11.271 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT44 Register (Offset = 5BCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT44 is shown in [Figure 11-270](#) and described in [Table 11-543](#).

Return to [Summary Table](#).

skew_cal_avg_status_reg2

Table 11-542.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT44
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05BCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05BCh |

Figure 11-270. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT44 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----|
| UNUSED | | | | | | | | | | | | | | TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | |
| R-0h | | | | | | | | | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-543. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT44 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-17 | UNUSED | R | 0h | RESERVED |
| 16-0 | TM_DESKEW_DCC_AVG_CUTM_DESKEW_DCC_AVG_STATE | R | 0h | current state of deskew_dcc_averaging FSM |

11.272 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT45 Register (Offset = 5C0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT45 is shown in [Figure 11-271](#) and described in [Table 11-545](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG0

Table 11-544.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT45
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05C0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05C0h |

Figure 11-271. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT45 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-545. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT45 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT0 | R | 0h | RESERVED |

11.273 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT46 Register (Offset = 5C4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT46 is shown in [Figure 11-272](#) and described in [Table 11-547](#).

Return to [Summary Table](#).

DIGITAL_CALIB_EXTRA_READ_REG1

Table 11-546.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT46
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05C4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05C4h |

Figure 11-272. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT46 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_CALIBRATION_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-547. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT46 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------------------------|------|-------|-------------|
| 31-0 | DIG_CALIBRATION_EXT RA_READ_TBIT1 | R | 0h | RESERVED |

11.274 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT47 Register (Offset = 5C8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT47 is shown in [Figure 11-273](#) and described in [Table 11-549](#).

Return to [Summary Table](#).

bist_status_reg1

Table 11-548.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT47
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05C8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05C8h |

Figure 11-273. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT47 Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| W_PAT_CHE_ERROR_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W_PAT_CHE_PKT_COUNT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-549. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT47 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-16 | W_PAT_CHE_ERROR_COUNT | R | 0h | BIST Pattern checker error count's live status can be obtained by poling this field |
| 15-0 | W_PAT_CHE_PKT_COUNT | R | 0h | BIST packet count's live status can be obtained by poling this field |

11.275 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT48 Register (Offset = 5CCh) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT48 is shown in [Figure 11-274](#) and described in [Table 11-551](#).

[Return to Summary Table.](#)

bist_status_reg2

Table 11-550.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT48
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05CCh |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05CCh |

Figure 11-274. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT48 Register

| | | | | | | | |
|--------|----|----|----|----|------------------|--------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | W_BIST_ERRO R | R_PAT_CHE_S YNC | W_DRX_BIST_ PASS |
| R-0h | | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 11-551. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT48 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-3 | UNUSED | R | 0h | RESERVED |
| 2 | W_BIST_ERROR | R | 0h | Status of HS data path comparison outcome, '0' means pass |
| 1 | R_PAT_CHE_SYNC | R | 0h | Informs BIST Pattern checker is not in sync with pattern generator - Check polarity |
| 0 | W_DRX_BIST_PASS | R | 0h | Entire DRX has passed BIST when this bit's status is set |

11.276 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT49 Register (Offset = 5D0h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT49 is shown in [Figure 11-275](#) and described in [Table 11-553](#).

Return to [Summary Table](#).

DIG_BIST_EXTRA_READ_REG0

Table 11-552.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT49
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05D0h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05D0h |

Figure 11-275. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT49 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_BIST_EXTRA_READ_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-553. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT49 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31-0 | DIG_BIST_EXTRA_READ_TBIT0 | R | 0h | RESERVED |

11.277 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT50 Register (Offset = 5D4h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT50 is shown in [Figure 11-276](#) and described in [Table 11-555](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG1

Table 11-554.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT50
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05D4h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05D4h |

Figure 11-276. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT50 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-555. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT50 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT1 | R | 0h | RESERVED |

11.278 DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT51 Register (Offset = 5D8h) [reset = 0h]

DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT51 is shown in [Figure 11-277](#) and described in [Table 11-557](#).

Return to [Summary Table](#).

DIG_EXTRA_READ_REG2

Table 11-556.
DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT51
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 05D8h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 05D8h |

Figure 11-277. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT51 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_EXTRA_READ_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-557. DPHY_RX_VBUS2APB_DL3_RX_DIG_TBIT51 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31-0 | DIG_EXTRA_READ_TBIT2 | R | 0h | RESERVED |

11.279 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0 Register (Offset = B00h) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0 is shown in [Figure 11-278](#) and described in [Table 11-559](#).

Return to [Summary Table](#).

PHY_BAND_CONTROL

Table 11-558.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B00h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B00h |

Figure 11-278. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0 Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----------------|----|----|----|----|----|----------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | BAND_CTL_REG_R | | | | | | BAND_CTL_REG_L | | | |
| R-0h | | | | | | R/W-0h | | | | | | R/W-0h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-559. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-10 | UNUSED | R | 0h | RESERVED |
| 9-5 | BAND_CTL_REG_R | R/W | 0h | Band control value for right lanes: Program this field using the encoding similar to the left lane. |

Table 11-559. DPHY_RX_VBUS2APB_PCS_TX_DIG_TB1T0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 4-0 | BAND_CTL_REG_L | R/W | 0h | <p>Band control value for left lanes: The range of data rates supported by this PMA are divided into multiple data rate bands. This signal specifies the values associated with each band. The encoding of the values for each band is as follows.</p> <ul style="list-style-type: none"> • 5'b00000: 80 Mbps - <100 Mbps • 5'b00001: 100 Mbps - <120 Mbps • 5'b00010: 120 Mbps - <160 Mbps • 5'b00011: 160 Mbps - <200 Mbps • 5'b00100: 200 Mbps - <240 Mbps • 5'b00101: 240 Mbps - <280 Mbps • 5'b00110: 280 Mbps - <320 Mbps • 5'b00111: 320 Mbps - <360 Mbps • 5'b01000: 360 Mbps - <400 Mbps • 5'b01001: 400 Mbps - <480 Mbps • 5'b01010: 480 Mbps - <560 Mbps • 5'b01011: 560 Mbps - <640 Mbps • 5'b01100: 640 Mbps - <720 Mbps • 5'b01101: 720 Mbps - <800 Mbps • 5'b01110: 800 Mbps - <880 Mbps • 5'b01111: 880 Mbps - <1040 Mbps • 5'b10000: 1040 Mbps - <1200 Mbps • 5'b10001: 1200 Mbps - <1350 Mbps • 5'b10010: 1350 Mbps - <=1500 Mbps • 5'b10011: >1500 Mbps - <1750 Mbps • 5'b10100: 1750 Mbps - <2000 Mbps • 5'b10101: 2000 Mbps - <2250 Mbps • 5'b10110: 2250 Mbps - <2500 Mbps • 5'b10111 - 5'b11111: Reserved |

11.280 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1 Register (Offset = B04h) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1 is shown in [Figure 11-279](#) and described in [Table 11-561](#).

Return to [Summary Table](#).

PHY_PSM_CONFIG

Table 11-560.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B04h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B04h |

Figure 11-279. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1 Register

| | | | | | | | |
|----------------|----|----|----|----|----|-------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | PSM_CLOCK_FREQ | |
| R-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSM_CLOCK_FREQ | | | | | | PSM_CLOCK_FREQ_EN | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-561. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|-------------------------------|
| 31-9 | UNUSED | R | 0h | RESERVED |
| 8-1 | PSM_CLOCK_FREQ | R/W | 0h | psm_clock_freq value |
| 0 | PSM_CLOCK_FREQ_EN | R/W | 0h | take psm_clock_freq from tbit |

11.281 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2 Register (Offset = B08h) [reset = 2222222h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2 is shown in [Figure 11-280](#) and described in [Table 11-563](#).

Return to [Summary Table](#).

PHY_PI_PH2_DL_CONFIG

Table 11-562.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B08h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B08h |

Figure 11-280. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2 Register

| | | | | | | | |
|------------------------|----|----|----|------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| POWER_SW_2_TIME_DL_R_3 | | | | POWER_SW_2_TIME_DL_R_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| POWER_SW_2_TIME_DL_R_1 | | | | POWER_SW_2_TIME_DL_R_0 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| POWER_SW_2_TIME_DL_L_3 | | | | POWER_SW_2_TIME_DL_L_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POWER_SW_2_TIME_DL_L_1 | | | | POWER_SW_2_TIME_DL_L_0 | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-563. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|------------------------|
| 31-28 | POWER_SW_2_TIME_DL_R_3 | R/W | 2h | power_sw_2_time_dl_r_3 |
| 27-24 | POWER_SW_2_TIME_DL_R_2 | R/W | 2h | power_sw_2_time_dl_r_2 |
| 23-20 | POWER_SW_2_TIME_DL_R_1 | R/W | 2h | power_sw_2_time_dl_r_1 |
| 19-16 | POWER_SW_2_TIME_DL_R_0 | R/W | 2h | power_sw_2_time_dl_r_0 |
| 15-12 | POWER_SW_2_TIME_DL_L_3 | R/W | 2h | power_sw_2_time_dl_l_3 |
| 11-8 | POWER_SW_2_TIME_DL_L_2 | R/W | 2h | power_sw_2_time_dl_l_2 |
| 7-4 | POWER_SW_2_TIME_DL_L_1 | R/W | 2h | power_sw_2_time_dl_l_1 |
| 3-0 | POWER_SW_2_TIME_DL_L_0 | R/W | 2h | power_sw_2_time_dl_l_0 |

11.282 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3 Register (Offset = B0Ch) [reset = 222h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3 is shown in [Figure 11-281](#) and described in [Table 11-565](#).

Return to [Summary Table](#).

PHY_PI_PH2_CL_CMN_CONFIG

Table 11-564.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B0Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B0Ch |

Figure 11-281. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3 Register

| | | | | | | | |
|----------------------|----|----|----|----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | POWER_SW_2_TIME_CMN | | | |
| R-0h | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POWER_SW_2_TIME_CL_R | | | | POWER_SW_2_TIME_CL_L | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-565. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|----------------------|
| 31-12 | UNUSED | R | 0h | RESERVED |
| 11-8 | POWER_SW_2_TIME_CMN | R/W | 2h | power_sw_2_time_cmn |
| 7-4 | POWER_SW_2_TIME_CL_R | R/W | 2h | power_sw_2_time_cl_r |
| 3-0 | POWER_SW_2_TIME_CL_L | R/W | 2h | power_sw_2_time_cl_l |

11.283 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT4 Register (Offset = B10h) [reset = 2222222h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT4 is shown in [Figure 11-282](#) and described in [Table 11-567](#).

Return to [Summary Table](#).

PHY_PI_PH1_DL_CONFIG

Table 11-566.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT4
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B10h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B10h |

Figure 11-282. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT4 Register

| | | | | | | | |
|------------------------|----|----|----|------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| POWER_SW_1_TIME_DL_R_3 | | | | POWER_SW_1_TIME_DL_R_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| POWER_SW_1_TIME_DL_R_1 | | | | POWER_SW_1_TIME_DL_R_0 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| POWER_SW_1_TIME_DL_L_3 | | | | POWER_SW_1_TIME_DL_L_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POWER_SW_1_TIME_DL_L_1 | | | | POWER_SW_1_TIME_DL_L_0 | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-567. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|------------------------|
| 31-28 | POWER_SW_1_TIME_DL_R_3 | R/W | 2h | power_sw_1_time_dl_r_3 |
| 27-24 | POWER_SW_1_TIME_DL_R_2 | R/W | 2h | power_sw_1_time_dl_r_2 |
| 23-20 | POWER_SW_1_TIME_DL_R_1 | R/W | 2h | power_sw_1_time_dl_r_1 |
| 19-16 | POWER_SW_1_TIME_DL_R_0 | R/W | 2h | power_sw_1_time_dl_r_0 |
| 15-12 | POWER_SW_1_TIME_DL_L_3 | R/W | 2h | power_sw_1_time_dl_l_3 |
| 11-8 | POWER_SW_1_TIME_DL_L_2 | R/W | 2h | power_sw_1_time_dl_l_2 |
| 7-4 | POWER_SW_1_TIME_DL_L_1 | R/W | 2h | power_sw_1_time_dl_l_1 |
| 3-0 | POWER_SW_1_TIME_DL_L_0 | R/W | 2h | power_sw_1_time_dl_l_0 |

11.284 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT5 Register (Offset = B14h) [reset = 222h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT5 is shown in [Figure 11-283](#) and described in [Table 11-569](#).

Return to [Summary Table](#).

PHY_PI_PH1_CL_CMN_CONFIG

Table 11-568.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT5
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0B14h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0B14h |

Figure 11-283. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT5 Register

| | | | | | | | |
|----------------------|----|----|----|----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | POWER_SW_1_TIME_CMN | | | |
| R-0h | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POWER_SW_1_TIME_CL_R | | | | POWER_SW_1_TIME_CL_L | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-569. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|----------------------|
| 31-12 | UNUSED | R | 0h | RESERVED |
| 11-8 | POWER_SW_1_TIME_CMN | R/W | 2h | power_sw_1_time_cmn |
| 7-4 | POWER_SW_1_TIME_CL_R | R/W | 2h | power_sw_1_time_cl_r |
| 3-0 | POWER_SW_1_TIME_CL_L | R/W | 2h | power_sw_1_time_cl_l |

11.285 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT6 Register (Offset = B18h) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT6 is shown in [Figure 11-284](#) and described in [Table 11-571](#).

Return to [Summary Table](#).

PHY_DL_SPARE_LEFT

Table 11-570.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT6
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B18h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B18h |

Figure 11-284. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DTX_L_3_SPARE | | | | | | | | DTX_L_2_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DTX_L_1_SPARE | | | | | | | | DTX_L_0_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-571. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--------------------|
| 31-24 | DTX_L_3_SPARE | R/W | 0h | dtx_l_3 spare port |
| 23-16 | DTX_L_2_SPARE | R/W | 0h | dtx_l_2 spare port |
| 15-8 | DTX_L_1_SPARE | R/W | 0h | dtx_l_1 spare port |
| 7-0 | DTX_L_0_SPARE | R/W | 0h | dtx_l_0 spare port |

11.286 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT7 Register (Offset = B1Ch) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT7 is shown in [Figure 11-285](#) and described in [Table 11-573](#).

Return to [Summary Table](#).

PHY_DL_SPARE_RIGHT

Table 11-572.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT7
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B1Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B1Ch |

Figure 11-285. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DTX_R_3_SPARE | | | | | | | | DTX_R_2_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DTX_R_1_SPARE | | | | | | | | DTX_R_0_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-573. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--------------------|
| 31-24 | DTX_R_3_SPARE | R/W | 0h | dtx_r_3 spare port |
| 23-16 | DTX_R_2_SPARE | R/W | 0h | dtx_r_2 spare port |
| 15-8 | DTX_R_1_SPARE | R/W | 0h | dtx_r_1 spare port |
| 7-0 | DTX_R_0_SPARE | R/W | 0h | dtx_r_0 spare port |

11.287 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT8 Register (Offset = B20h) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT8 is shown in [Figure 11-286](#) and described in [Table 11-575](#).

Return to [Summary Table](#).

PHY_CL_CMN_SPARE

Table 11-574.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT8
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B20h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B20h |

Figure 11-286. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | | CMN_SPARE | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CL_R_SPARE | | | | | | | | CL_L_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-575. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|-----------------|
| 31-24 | UNUSED | R | 0h | RESERVED |
| 23-16 | CMN_SPARE | R/W | 0h | cmn spare port |
| 15-8 | CL_R_SPARE | R/W | 0h | cl_r spare port |
| 7-0 | CL_L_SPARE | R/W | 0h | cl_l spare port |

11.288 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT9 Register (Offset = B24h) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT9 is shown in [Figure 11-287](#) and described in [Table 11-577](#).

Return to [Summary Table](#).

PHY_PI_CONFIG

Table 11-576.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT9
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B24h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B24h |

Figure 11-287. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT9 Register

| | | | | | | | |
|--------|----|----|----|----|----|-----------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UNUSED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UNUSED | | | | | | PSO_DISABLE _VALUE | PSO_DISABLE _EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-577. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------|------|-------|---------------------------|
| 31-2 | UNUSED | R | 0h | RESERVED |
| 1 | PSO_DISABLE_VALUE | R/W | 0h | pso_disbale value |
| 0 | PSO_DISABLE_EN | R/W | 0h | take pso_diable from tbit |

11.289 DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT10 Register (Offset = B28h) [reset = 0h]

DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT10 is shown in [Figure 11-288](#) and described in [Table 11-579](#).

Return to [Summary Table](#).

DIG_TBIT10

Table 11-578.
DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT10
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0B28h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0B28h |

Figure 11-288. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT10 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIG_TBIT10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 11-579. DPHY_RX_VBUS2APB_PCS_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|-------------------------------|
| 31-0 | DIG_TBIT10 | R/W | 0h | Digital Test Register Extra 4 |

11.290 DPHY_RX_VBUS2APB_ISO_PHY_ISO_CNTRL Register (Offset = C00h) [reset = 50Fh]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_CNTRL is shown in [Figure 11-289](#) and described in [Table 11-581](#).

Return to [Summary Table](#).

PHY_ISO_CNTRL

Table 11-580.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_CNTRL
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C00h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C00h |

Figure 11-289. DPHY_RX_VBUS2APB_ISO_PHY_ISO_CNTRL Register

| | | | | | | | |
|------------|----|----|----|-------------------|-------------|------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_12 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_12 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_12 | | | | PHY_ISOLATIO N | PHY_ISO_CMN | PHY_ISO_CL | |
| R-0h | | | | R/W-0h | R/W-1h | R/W-1h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY_ISO_DL | | | | | | | |
| R/W-Fh | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-581. DPHY_RX_VBUS2APB_ISO_PHY_ISO_CNTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 31-12 | BF_31_12 | R | 0h | |
| 11 | PHY_ISOLATION | R/W | 0h | when set enables phy_isolation |
| 10 | PHY_ISO_CMN | R/W | 1h | This bit enables the Isolation on Common Lane |
| 9-8 | PHY_ISO_CL | R/W | 1h | Bit 1: Setting a value 1 isolates the Right Clock Lane |
| 7-0 | PHY_ISO_DL | R/W | Fh | Bit 7: Setting a value 1 isolates the Data Lane 3 on Right Link |

11.291 DPHY_RX_VBUS2APB_ISO_PHY_ISO_RESET Register (Offset = C04h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_RESET is shown in [Figure 11-290](#) and described in [Table 11-583](#).

Return to [Summary Table](#).

PHY_ISO_RESET

Table 11-582.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_RESET
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C04h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C04h |

Figure 11-290. DPHY_RX_VBUS2APB_ISO_PHY_ISO_RESET Register

| | | | | | | | |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_11 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_11 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_11 | | | | | LANE_RSTB_C MN | LANE_RSTB_C L_R | LANE_RSTB_C L_L |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LANE_RSTB_D L_R_3 | LANE_RSTB_D L_R_2 | LANE_RSTB_D L_R_1 | LANE_RSTB_D L_R_0 | LANE_RSTB_D L_L_3 | LANE_RSTB_D L_L_2 | LANE_RSTB_D L_L_1 | LANE_RSTB_D L_L_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-583. DPHY_RX_VBUS2APB_ISO_PHY_ISO_RESET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-11 | BF_31_11 | R | 0h | |
| 10 | LANE_RSTB_CMN | R/W | 0h | Drives the Lane Reset for Common lane_rstb_cm_n |
| 9 | LANE_RSTB_CL_R | R/W | 0h | Drives the Right Clock Lane Reset lane_rstb_cl_l |
| 8 | LANE_RSTB_CL_L | R/W | 0h | Drives the Left Clock Lane Reset lane_rstb_cl_l |
| 7 | LANE_RSTB_DL_R_3 | R/W | 0h | Drives the Data Lane 3 Right Link Reset lane_rstb_dl_7 |
| 6 | LANE_RSTB_DL_R_2 | R/W | 0h | Drives the Data Lane 2 Right Link Reset lane_rstb_dl_6 |
| 5 | LANE_RSTB_DL_R_1 | R/W | 0h | Drives the Data Lane 1 Right Link Reset lane_rstb_dl_5 |
| 4 | LANE_RSTB_DL_R_0 | R/W | 0h | Drives the Data Lane 0 Right Link Reset lane_rstb_dl_4 |
| 3 | LANE_RSTB_DL_L_3 | R/W | 0h | Drives the Data Lane 3 Left Link Reset lane_rstb_dl_3 |
| 2 | LANE_RSTB_DL_L_2 | R/W | 0h | Drives the Data Lane 2 Left Link Reset lane_rstb_dl_2 |
| 1 | LANE_RSTB_DL_L_1 | R/W | 0h | Drives the Data Lane 1 Left Link Reset lane_rstb_dl_1 |
| 0 | LANE_RSTB_DL_L_0 | R/W | 0h | Drives the Data Lane 0 Left Link Reset lane_rstb_dl_0 |

11.292 DPHY_RX_VBUS2APB_ISO_PHY_ISO_ENABLE Register (Offset = C08h) [reset = 10Fh]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_ENABLE is shown in [Figure 11-291](#) and described in [Table 11-585](#).

Return to [Summary Table](#).

PHY_ISO_ENABLE

Table 11-584.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_ENABLE
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C08h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C08h |

Figure 11-291. DPHY_RX_VBUS2APB_ISO_PHY_ISO_ENABLE Register

| | | | | | | | |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_10 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_10 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_10 | | | | | | RXENABLECLK_CLK_R | RXENABLECLK_CLK_L |
| R-0h | | | | | | R/W-0h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S_ENABLE_DL_R_3 | S_ENABLE_DL_R_2 | S_ENABLE_DL_R_1 | S_ENABLE_DL_R_0 | S_ENABLE_DL_L_3 | S_ENABLE_DL_L_2 | S_ENABLE_DL_L_1 | S_ENABLE_DL_L_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-585. DPHY_RX_VBUS2APB_ISO_PHY_ISO_ENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-10 | BF_31_10 | R | 0h | |
| 9 | RXENABLECLK_CLK_R | R/W | 0h | Drives to enable the right clock DPHY_RX_VBUS2APB_LANE TxEnableClk_clk_r |
| 8 | RXENABLECLK_CLK_L | R/W | 1h | Drives to enable the left clock DPHY_RX_VBUS2APB_LANE TxEnableClk_clk_l |
| 7 | S_ENABLE_DL_R_3 | R/W | 0h | Enables the Data Lane 3 Right Link M_Enable_dl_7 |
| 6 | S_ENABLE_DL_R_2 | R/W | 0h | Enables the Data Lane 2 Right Link M_Enable_dl_6 |
| 5 | S_ENABLE_DL_R_1 | R/W | 0h | Enables the Data Lane 1 Right Link M_Enable_dl_5 |
| 4 | S_ENABLE_DL_R_0 | R/W | 0h | Enables the Data Lane 0 Right Link M_Enable_dl_4 |
| 3 | S_ENABLE_DL_L_3 | R/W | 1h | Enables the Data Lane 3 Left Link M_Enable_dl_3 |
| 2 | S_ENABLE_DL_L_2 | R/W | 1h | Enables the Data Lane 2 Left Link M_Enable_dl_2 |
| 1 | S_ENABLE_DL_L_1 | R/W | 1h | Enables the Data Lane 1 Left Link M_Enable_dl_1 |
| 0 | S_ENABLE_DL_L_0 | R/W | 1h | Enables the Data Lane 0 Left Link M_Enable_dl_0 |

11.293 DPHY_RX_VBUS2APB_ISO_PHY_ISO_CMN_CTRL Register (Offset = C0Ch) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_CMN_CTRL is shown in [Figure 11-292](#) and described in [Table 11-587](#).

Return to [Summary Table](#).

PHY_ISO_CMN_CTRL

Table 11-586.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_CMN_CTRL
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C0Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C0Ch |

Figure 11-292. DPHY_RX_VBUS2APB_ISO_PHY_ISO_CMN_CTRL Register

| | | | | | | | |
|----------------|------------------|-------------|---------------|----|----|---------|----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_9 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_9 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_9 | | | | | | | LANE_READY_CMN |
| R-0h | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| O_SUPPLY_IO_PG | O_SUPPLY_CORE_PG | O_CMN_READY | IP_CONFIG_CMN | | | PSO_CMN | PSO_DISABLE |
| R-0h | R-0h | R-0h | R/W-0h | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-587. DPHY_RX_VBUS2APB_ISO_PHY_ISO_CMN_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-9 | BF_31_9 | R | 0h | |
| 8 | LANE_READY_CMN | R | 0h | Drives lane_ready_cmn |
| 7 | O_SUPPLY_IO_PG | R | 0h | I/O supply power is good o_supply_io_pg |
| 6 | O_SUPPLY_CORE_PG | R | 0h | Core Supply Power is good o_supply_core_pg |
| 5 | O_CMN_READY | R | 0h | Common ready Indicator o_cmn_ready |
| 4-2 | IP_CONFIG_CMN | R/W | 0h | Drives the IP configuration to decide which clock DPHY_RX_VBUS2APB_LANE acts as the master DPHY_RX_VBUS2APB_LANE to all clock lanes ip_config_cmn |
| 1 | PSO_CMN | R/W | 0h | Drives the power shut off for the Common pso_cmn |
| 0 | PSO_DISABLE | R/W | 0h | Disable power shut off pso_disable |

11.294 DPHY_RX_VBUS2APB_ISO_PHY_ISO_CL_CNTRL_L Register (Offset = C10h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_CL_CNTRL_L is shown in [Figure 11-293](#) and described in [Table 11-589](#).

Return to [Summary Table](#).

PHY_ISO_CL_CNTRL_L

Table 11-588.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_CL_CNTRL_L
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C10h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C10h |

Figure 11-293. DPHY_RX_VBUS2APB_ISO_PHY_ISO_CL_CNTRL_L Register

| | | | | | | | |
|---------|---------------------|--------------------|---------------------|-------------------------|------------------------|--------------------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BF_31_7 | S_CLK_SWAPDPDN_CL_L | RXULPSCCLKNOT_CL_L | RXSTOPSTATECLK_CL_L | RXULPSACTIVENOTCLK_CL_L | RXCLKACTIVEHSCCLK_CL_L | RXENABLECLK_K_CL_L | LANE_READY_CL_L |
| R-0h | R/W-0h | R-0h | R-0h | R-0h | R-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-589. DPHY_RX_VBUS2APB_ISO_PHY_ISO_CL_CNTRL_L Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|---|
| 31-7 | BF_31_7 | R | 0h | |
| 6 | S_CLK_SWAPDPDN_CL_L | R/W | 0h | Drives the value to enable the Swap of DP and DN signals inside the clock DPHY_RX_VBUS2APB_LANE S_Clk_SwapDpDn_cl_I |
| 5 | RXULPSCCLKNOT_CL_L | R | 0h | Receives ULPS power state status RxULPSClkNot_cl_I |
| 4 | RXSTOPSTATECLK_CL_L | R | 0h | Receives DPHY_RX_VBUS2APB_LANE state status RxStopStateClk_cl_I |
| 3 | RXULPSACTIVENOTCLK_CL_L | R | 0h | Receives DPHY_RX_VBUS2APB_LANE ULPS active state status RxULPSActiveNotClk_cl_I |
| 2 | RXCLKACTIVEHSCCLK_CL_L | R | 0h | Stores Receiver high speed active RxClkActiveHSClk_cl_I |
| 1 | RXENABLECLK_CL_L | R/W | 0h | Enable the Clock Lane RxEnableClk_cl_I |
| 0 | LANE_READY_CL_L | R | 0h | High speed clock transmission ready lane_ready_cl_I |

11.295 DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L0 Register (Offset = C14h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L0 is shown in [Figure 11-294](#) and described in [Table 11-591](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L0

Table 11-590.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C14h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C14h |

Figure 11-294. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L0 Register

| | | | | | | | |
|---------|---------------------------|------------------------|----------------------------|------------------------|----------------------------|---------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BF_31_7 | S_CLK_SWAP DPDN_DL_L_0 | FORCERXMOD E_DL_L_0 | S_DATA_SWAP DPDN_DL_L_0 | S_STOPSTATE _DL_L_0 | S_ULPSACTIV ENOT_DL_L_0 | S_ENABLE_DL _L_0 | LANE_READY_ DL_L_0 |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-591. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-7 | BF_31_7 | R | 0h | |
| 6 | S_CLK_SWAPDPDN_DL_L_0 | R/W | 0h | Drives S_Clk_SwapDpDn_dl_I_0 |
| 5 | FORCERXMODE_DL_L_0 | R/W | 0h | Forces the DPHY_RX_VBUS2APB_LANE in Receiver mode ForceRxMode_dl_I_0 |
| 4 | S_DATA_SWAPDPDN_DL_L_0 | R/W | 0h | Swaps the tx_p and tx_m differential pins S_Data_SwapDpDn_dl_I_0 |
| 3 | S_STOPSTATE_DL_L_0 | R | 0h | Receives Lane Stop state status S_StopState_dl_I_0 |
| 2 | S_ULPSACTIVENOT_DL_L_0 | R | 0h | Receives the Turnaround request S_ULPSActiveNot_dl_I_0 |
| 1 | S_ENABLE_DL_L_0 | R/W | 0h | Enables the data DPHY_RX_VBUS2APB_LANE S_Enable_dl_I_0 |
| 0 | LANE_READY_DL_L_0 | R | 0h | High Speed data DPHY_RX_VBUS2APB_LANE ready lane_ready_dl_I_0 |

11.296 DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L0 Register (Offset = C18h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L0 is shown in [Figure 11-295](#) and described in [Table 11-593](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L0

Table 11-592.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L0
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C18h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C18h |

Figure 11-295. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L0 Register

| | | | | | | | |
|-----------------|---------------------|-----------------|-----------------|------------------|--------------------|-------------------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_14 | ERRSOTSYNCHS_DL_L_0 | ERRSOTHS_DL_L_0 | RXSYNCHS_DL_L_0 | RXVALIDHS_DL_L_0 | RXSKEWCALHS_DL_L_0 | RXACTIVEHS_DL_L_0 | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RXDATAHS_DL_L_0 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-593. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-14 | BF_31_14 | R | 0h | |
| 13 | ERRSOTSYNCHS_DL_L_0 | R | 0h | Start of transmission error ErrSoTSyncHS_dl_I_0 |
| 12 | ERRSOTHS_DL_L_0 | R | 0h | Start of transmission error ErrSoTHS_dl_I_0 |
| 11 | RXSYNCHS_DL_L_0 | R | 0h | Stores the high speed receive synchronization RxSyncHS_dl_I_0 |
| 10 | RXVALIDHS_DL_L_0 | R | 0h | High speed data receive data valid RxValidHS_dl_I_0 |
| 9 | RXSKEWCALHS_DL_L_0 | R | 0h | High speed data receive dksew calibration RxSkewCalHS_dl_I_0 |
| 8 | RXACTIVEHS_DL_L_0 | R | 0h | Stores the high speed data reception active RxActiveHS_dl_I_0 |
| 7-0 | RXDATAHS_DL_L_0 | R | 0h | High speed receive data RxDataHS_dl_I_0 [7:0] |

11.297 DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L0 Register (Offset = C1Ch) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L0 is shown in [Figure 11-296](#) and described in [Table 11-595](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L0

Table 11-594.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L0 Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C1Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C1Ch |

Figure 11-296. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L0 Register

| | | | | | | | |
|--------------------|-----------------------|----|----|----|---------------------|----------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_18 | | | | | | S_ERRSYNC_DL_L_0 | S_ERRCONTR_OL_DL_L_0 |
| R-0h | | | | | | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| S_ERRESC_DL_L_0 | S_RXTRIGGERESC_DL_L_0 | | | | S_RXULPSES_C_DL_L_0 | S_RXVALIDES_C_DL_L_0 | S_RXLPDTEESC_DL_L_0 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S_RXDATAESC_DL_L_0 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-595. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-18 | BF_31_18 | R | 0h | |
| 17 | S_ERRSYNC_DL_L_0 | R | 0h | Control error S_ErrControl_dl_l_0 |
| 16 | S_ERRCONTROL_DL_L_0 | R | 0h | Control error S_ErrControl_dl_l_0 |
| 15 | S_ERRESC_DL_L_0 | R | 0h | Escape entry error S_ErrEsc_dl_l_0 |
| 14-11 | S_RXTRIGGERESC_DL_L_0 | R | 0h | Receive escape mode lower power trigger state S_RxTriggerEsc_dl_l_0 [3:0] |
| 10 | S_RXULPSESC_DL_L_0 | R | 0h | Receive escape mode ultra low power state S_RxULPSEsc_dl_l_0 |
| 9 | S_RXVALIDESC_DL_L_0 | R | 0h | Receive escape mode data present S_RxValidEsc_dl_l_0 |
| 8 | S_RXLPDTEESC_DL_L_0 | R | 0h | Receive escape mode low power data indicator S_RxLPDTEsc_dl_l_0 |
| 7-0 | S_RXDATAESC_DL_L_0 | R | 0h | Receive escape mode low power receive data S_RxDataEsc_dl_l_0 [7:0] |

11.298 DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L1 Register (Offset = C20h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L1 is shown in [Figure 11-297](#) and described in [Table 11-597](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L1

Table 11-596.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L1
Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C20h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C20h |

Figure 11-297. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L1 Register

| | | | | | | | |
|---------|---------------------------|------------------------|----------------------------|------------------------|----------------------------|---------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BF_31_7 | S_CLK_SWAP DPDN_DL_L_1 | FORCERXMOD E_DL_L_1 | S_DATA_SWAP DPDN_DL_L_1 | S_STOPSTATE _DL_L_1 | S_ULPSACTIV ENOT_DL_L_1 | S_ENABLE_DL _L_1 | LANE_READY_ DL_L_1 |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-597. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_CTRL_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-7 | BF_31_7 | R | 0h | |
| 6 | S_CLK_SWAPDPDN_DL_L_1 | R/W | 0h | Drives S_Clk_SwapDpDn_dl_I_1 |
| 5 | FORCERXMODE_DL_L_1 | R/W | 0h | Forces the DPHY_RX_VBUS2APB_LANE in Receiver mode ForceRxMode_dl_I_1 |
| 4 | S_DATA_SWAPDPDN_DL_L_1 | R/W | 0h | Swaps the tx_p and tx_m differential pins S_Data_SwapDpDn_dl_I_1 |
| 3 | S_STOPSTATE_DL_L_1 | R | 0h | Receives Lane Stop state status S_StopState_dl_I_1 |
| 2 | S_ULPSACTIVENOT_DL_L_1 | R | 0h | Receives the Turnaround request S_ULPSActiveNot_dl_I_1 |
| 1 | S_ENABLE_DL_L_1 | R/W | 0h | Enables the data DPHY_RX_VBUS2APB_LANE S_Enable_dl_I_1 |
| 0 | LANE_READY_DL_L_1 | R | 0h | High Speed data DPHY_RX_VBUS2APB_LANE ready lane_ready_dl_I_1 |

11.299 DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L1 Register (Offset = C24h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L1 is shown in [Figure 11-298](#) and described in [Table 11-599](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L1

Table 11-598.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C24h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C24h |

Figure 11-298. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L1 Register

| | | | | | | | |
|-----------------|---------------------|-----------------|-----------------|------------------|--------------------|-------------------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_14 | ERRSOTSYNCHS_DL_L_1 | ERRSOTHS_DL_L_1 | RXSYNCHS_DL_L_1 | RXVALIDHS_DL_L_1 | RXSKEWCALHS_DL_L_1 | RXACTIVEHS_DL_L_1 | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RXDATAHS_DL_L_1 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-599. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_HS_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-14 | BF_31_14 | R | 0h | |
| 13 | ERRSOTSYNCHS_DL_L_1 | R | 0h | Start of transmission error ErrSoTSyncHS_dl_I_1 |
| 12 | ERRSOTHS_DL_L_1 | R | 0h | Start of transmission error ErrSoTHS_dl_I_1 |
| 11 | RXSYNCHS_DL_L_1 | R | 0h | Stores the high speed receive synchronization RxSyncHS_dl_I_1 |
| 10 | RXVALIDHS_DL_L_1 | R | 0h | High speed data receive data valid RxValidHS_dl_I_1 |
| 9 | RXSKEWCALHS_DL_L_1 | R | 0h | High speed data receive dksew calibration RxSkewCalHS_dl_I_1 |
| 8 | RXACTIVEHS_DL_L_1 | R | 0h | Stores the high speed data reception active RxActiveHS_dl_I_1 |
| 7-0 | RXDATAHS_DL_L_1 | R | 0h | High speed receive data RxDataHS_dl_I_1 [7:0] |

11.300 DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L1 Register (Offset = C28h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L1 is shown in [Figure 11-299](#) and described in [Table 11-601](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L1

Table 11-600.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L1 Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C28h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C28h |

Figure 11-299. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L1 Register

| | | | | | | | |
|--------------------|-----------------------|----|----|----|---------------------|----------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_18 | | | | | | S_ERRSYNC_DL_L_1 | S_ERRCONTR_OL_DL_L_1 |
| R-0h | | | | | | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| S_ERRESC_DL_L_1 | S_RXTRIGGERESC_DL_L_1 | | | | S_RXULPSES_C_DL_L_1 | S_RXVALIDES_C_DL_L_1 | S_RXLPDTEESC_DL_L_1 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S_RXDATAESC_DL_L_1 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-601. DPHY_RX_VBUS2APB_ISO_PHY_ISO_DL_RX_ESC_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-18 | BF_31_18 | R | 0h | |
| 17 | S_ERRSYNC_DL_L_1 | R | 0h | Control error S_ErrControl_dl_l_1 |
| 16 | S_ERRCONTROL_DL_L_1 | R | 0h | Control error S_ErrControl_dl_l_1 |
| 15 | S_ERRESC_DL_L_1 | R | 0h | Escape entry error S_ErrEsc_dl_l_1 |
| 14-11 | S_RXTRIGGERESC_DL_L_1 | R | 0h | Receive escape mode lower power trigger state S_RxTriggerEsc_dl_l_1 [3:0] |
| 10 | S_RXULPSESC_DL_L_1 | R | 0h | Receive escape mode ultra low power state S_RxULPSEsc_dl_l_1 |
| 9 | S_RXVALIDESC_DL_L_1 | R | 0h | Receive escape mode data present S_RxValidEsc_dl_l_1 |
| 8 | S_RXLPDTEESC_DL_L_1 | R | 0h | Receive escape mode low power data indicator S_RxLPDTEsc_dl_l_1 |
| 7-0 | S_RXDATAESC_DL_L_1 | R | 0h | Receive escape mode low power receive data S_RxDataEsc_dl_l_1 [7:0] |

11.301 DPHY_RX_VBUS2APB_ISO_PHY_ISO_SPARE_1 Register (Offset = C2Ch) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_PHY_ISO_SPARE_1 is shown in [Figure 11-300](#) and described in [Table 11-603](#).

Return to [Summary Table](#).

PHY_ISO_SPARE_1

Table 11-602.
DPHY_RX_VBUS2APB_ISO_PHY_ISO_SPARE_1
Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C2Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C2Ch |

Figure 11-300. DPHY_RX_VBUS2APB_ISO_PHY_ISO_SPARE_1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY_ISO_SPARE_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-603. DPHY_RX_VBUS2APB_ISO_PHY_ISO_SPARE_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|----------------|
| 31-0 | PHY_ISO_SPARE_1 | R | 0h | spare register |

11.302 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L2 Register (Offset = C30h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L2 is shown in [Figure 11-301](#) and described in [Table 11-605](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L2

Table 11-604.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L2 Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C30h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C30h |

Figure 11-301. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L2 Register

| | | | | | | | |
|---------|-----------------------|--------------------|------------------------|--------------------|------------------------|-----------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BF_31_7 | S_CLK_SWAPDPDN_DL_L_2 | FORCERXMODE_DL_L_2 | S_DATA_SWAPDPDN_DL_L_2 | S_STOPSTATE_DL_L_2 | S_ULPSACTIVENOT_DL_L_2 | S_ENABLE_DL_L_2 | LANE_READY_DL_L_2 |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-605. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-7 | BF_31_7 | R | 0h | |
| 6 | S_CLK_SWAPDPDN_DL_L_2 | R/W | 0h | Drives S_Clk_SwapDpDn_dl_I_2 |
| 5 | FORCERXMODE_DL_L_2 | R/W | 0h | Forces the DPHY_RX_VBUS2APB_LANE in Receiver mode ForceRxMode_dl_I_2 |
| 4 | S_DATA_SWAPDPDN_DL_L_2 | R/W | 0h | Swaps the tx_p and tx_m differential pins S_Data_SwapDpDn_dl_I_2 |
| 3 | S_STOPSTATE_DL_L_2 | R | 0h | Receives Lane Stop state status S_StopState_dl_I_2 |
| 2 | S_ULPSACTIVENOT_DL_L_2 | R | 0h | Receives the Turnaround request S_ULPSActiveNot_dl_I_2 |
| 1 | S_ENABLE_DL_L_2 | R/W | 0h | Enables the data DPHY_RX_VBUS2APB_LANE S_Enable_dl_I_2 |
| 0 | LANE_READY_DL_L_2 | R | 0h | High Speed data DPHY_RX_VBUS2APB_LANE ready lane_ready_dl_I_2 |

11.303 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L2 Register (Offset = C34h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L2 is shown in [Figure 11-302](#) and described in [Table 11-607](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L2

Table 11-606.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_
L2 Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C34h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C34h |

Figure 11-302. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L2 Register

| | | | | | | | |
|-----------------|---------------------|-----------------|-----------------|------------------|--------------------|-------------------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_14 | ERRSOTSYNCHS_DL_L_2 | ERRSOTHS_DL_L_2 | RXSYNCHS_DL_L_2 | RXVALIDHS_DL_L_2 | RXSKEWCALHS_DL_L_2 | RXACTIVEHS_DL_L_2 | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RXDATAHS_DL_L_2 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-607. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-14 | BF_31_14 | R | 0h | |
| 13 | ERRSOTSYNCHS_DL_L_2 | R | 0h | Start of transmission error ErrSoTSyncHS_dl_l_2 |
| 12 | ERRSOTHS_DL_L_2 | R | 0h | Start of transmission error ErrSoTHS_dl_l_2 |
| 11 | RXSYNCHS_DL_L_2 | R | 0h | Stores the high speed receive synchronization RxSyncHS_dl_l_2 |
| 10 | RXVALIDHS_DL_L_2 | R | 0h | High speed data receive data valid RxValidHS_dl_l_2 |
| 9 | RXSKEWCALHS_DL_L_2 | R | 0h | High speed data receive dksew calibration RxSkewCalHS_dl_l_2 |
| 8 | RXACTIVEHS_DL_L_2 | R | 0h | Stores the high speed data reception active RxActiveHS_dl_l_2 |
| 7-0 | RXDATAHS_DL_L_2 | R | 0h | High speed receive data RxDataHS_dl_l_2 [7:0] |

11.304 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 Register (Offset = C38h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 is shown in [Figure 11-303](#) and described in [Table 11-609](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L2

Table 11-608.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_
ESC_L2 Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C38h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C38h |

Figure 11-303. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 Register

| | | | | | | | |
|---------------------|-----------------------|----|----|----|------------------------|-------------------------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_18 | | | | | | S_ERRSYNC_ DL_L_2 | S_ERRCONTR OL_DL_L_2 |
| R-0h | | | | | | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| S_ERRESC_DL _L_2 | S_RXTRIGGERESC_DL_L_2 | | | | S_RXULPSES C_DL_L_2 | S_RXVALIDES C_DL_L_2 | S_RXLPDTEESC _DL_L_2 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S_RXDATAESC_DL_L_2 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-609. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-18 | BF_31_18 | R | 0h | |
| 17 | S_ERRSYNC_DL_L_2 | R | 0h | Control error S_ErrControl_dl_r_2 |
| 16 | S_ERRCONTROL_DL_L_2 | R | 0h | Control error S_ErrControl_dl_l_2 |
| 15 | S_ERRESC_DL_L_2 | R | 0h | Escape entry error S_ErrEsc_dl_l_2 |
| 14-11 | S_RXTRIGGERESC_DL_L_2 | R | 0h | Receive escape mode lower power trigger state S_RxTriggerEsc_dl_l_2 [3:0] |
| 10 | S_RXULPSESC_DL_L_2 | R | 0h | Receive escape mode ultra low power state S_RxULPSEsc_dl_l_2 |
| 9 | S_RXVALIDESC_DL_L_2 | R | 0h | Receive escape mode data present S_RxValidEsc_dl_l_2 |
| 8 | S_RXLPDTEESC_DL_L_2 | R | 0h | Receive escape mode low power data indicator S_RxLPDTEsc_dl_l_2 |
| 7-0 | S_RXDATAESC_DL_L_2 | R | 0h | Receive escape mode low power receive data S_RxDataEsc_dl_l_2 [7:0] |

11.305 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L3 Register (Offset = C3Ch) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L3 is shown in [Figure 11-304](#) and described in [Table 11-611](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L3

Table 11-610.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CT
RL_L3 Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C3Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C3Ch |

Figure 11-304. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L3 Register

| | | | | | | | |
|---------|---------------------------|------------------------|----------------------------|------------------------|----------------------------|---------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_7 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BF_31_7 | S_CLK_SWAP DPDN_DL_L_3 | FORCERXMOD E_DL_L_3 | S_DATA_SWAP DPDN_DL_L_3 | S_STOPSTATE _DL_L_3 | S_ULPSACTIV ENOT_DL_L_3 | S_ENABLE_DL _L_3 | LANE_READY_ DL_L_3 |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R-0h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-611. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_CTRL_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-7 | BF_31_7 | R | 0h | |
| 6 | S_CLK_SWAPDPDN_DL_L_3 | R/W | 0h | Drives S_Clk_SwapDpDn_dl_I_0 |
| 5 | FORCERXMODE_DL_L_3 | R/W | 0h | Forces the DPHY_RX_VBUS2APB_LANE in Receiver mode ForceRxMode_dl_I_3 |
| 4 | S_DATA_SWAPDPDN_DL_L_3 | R/W | 0h | Swaps the tx_p and tx_m differential pins S_Data_SwapDpDn_dl_I_3 |
| 3 | S_STOPSTATE_DL_L_3 | R | 0h | Receives Lane Stop state status S_StopState_dl_I_3 |
| 2 | S_ULPSACTIVENOT_DL_L_3 | R | 0h | Receives the Turnaround request S_ULPSActiveNot_dl_I_3 |
| 1 | S_ENABLE_DL_L_3 | R/W | 0h | Enables the data DPHY_RX_VBUS2APB_LANE S_Enable_dl_I_3 |
| 0 | LANE_READY_DL_L_3 | R | 0h | High Speed data DPHY_RX_VBUS2APB_LANE ready lane_ready_dl_I_3 |

11.306 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L3 Register (Offset = C40h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L3 is shown in [Figure 11-305](#) and described in [Table 11-613](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L3

Table 11-612.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_
L3 Instances

| Instance | Physical Address |
|---|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0458 0C40h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS P_K3_DPHY_RX | 0459 0C40h |

Figure 11-305. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L3 Register

| | | | | | | | |
|-----------------|---------------------|-----------------|-----------------|------------------|--------------------|-------------------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_14 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BF_31_14 | ERRSOTSYNCHS_DL_L_3 | ERRSOTHS_DL_L_3 | RXSYNCHS_DL_L_3 | RXVALIDHS_DL_L_3 | RXSKEWCALHS_DL_L_3 | RXACTIVEHS_DL_L_3 | |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RXDATAHS_DL_L_3 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-613. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_HS_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-14 | BF_31_14 | R | 0h | |
| 13 | ERRSOTSYNCHS_DL_L_3 | R | 0h | Start of transmission error ErrSoTSyncHS_dl_I_3 |
| 12 | ERRSOTHS_DL_L_3 | R | 0h | Start of transmission error ErrSoTHS_dl_I_3 |
| 11 | RXSYNCHS_DL_L_3 | R | 0h | Stores the high speed receive synchronization RxSyncHS_dl_I_3 |
| 10 | RXVALIDHS_DL_L_3 | R | 0h | High speed data receive data valid RxValidHS_dl_I_3 |
| 9 | RXSKEWCALHS_DL_L_3 | R | 0h | High speed data receive dksew calibration RxSkewCalHS_dl_I_3 |
| 8 | RXACTIVEHS_DL_L_3 | R | 0h | Stores the high speed data reception active RxActiveHS_dl_I_3 |
| 7-0 | RXDATAHS_DL_L_3 | R | 0h | High speed receive data RxDataHS_dl_I_3 [7:0] |

11.307 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 Register (Offset = C44h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 is shown in [Figure 11-306](#) and described in [Table 11-615](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L3

Table 11-614.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_
ESC_L3 Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C44h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C44h |

Figure 11-306. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 Register

| | | | | | | | |
|--------------------|-----------------------|----|----|----|---------------------|----------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BF_31_18 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BF_31_18 | | | | | | S_ERRSYNC_DL_L_3 | S_ERRCONTR_OL_DL_L_3 |
| R-0h | | | | | | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| S_ERRESC_DL_L_3 | S_RXTRIGGERESC_DL_L_3 | | | | S_RXULPSES_C_DL_L_3 | S_RXVALIDES_C_DL_L_3 | S_RXLPDTEESC_DL_L_3 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S_RXDATAESC_DL_L_3 | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-615. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|---|
| 31-18 | BF_31_18 | R | 0h | |
| 17 | S_ERRSYNC_DL_L_3 | R | 0h | Control error S_ErrSync_dl_l_3 |
| 16 | S_ERRCONTROL_DL_L_3 | R | 0h | Control error S_ErrControl_dl_l_3 |
| 15 | S_ERRESC_DL_L_3 | R | 0h | Escape entry error S_ErrEsc_dl_l_3 |
| 14-11 | S_RXTRIGGERESC_DL_L_3 | R | 0h | Receive escape mode lower power trigger state S_RxTriggerEsc_dl_l_3 [3:0] |
| 10 | S_RXULPSESC_DL_L_3 | R | 0h | Receive escape mode ultra low power state S_RxULPSEsc_dl_l_3 |
| 9 | S_RXVALIDESC_DL_L_3 | R | 0h | Receive escape mode data present S_RxValidEsc_dl_l_3 |
| 8 | S_RXLPDTEESC_DL_L_3 | R | 0h | Receive escape mode low power data indicator S_RxLPDTEsc_dl_l_3 |
| 7-0 | S_RXDATAESC_DL_L_3 | R | 0h | Receive escape mode low power receive data S_RxDataEsc_dl_l_3 [7:0] |

11.308 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_1 Register (Offset = C48h) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_1 is shown in [Figure 11-307](#) and described in [Table 11-617](#).

Return to [Summary Table](#).

PHY_ISO_RX_SPARE_1

Table 11-616.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_1 Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C48h |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C48h |

Figure 11-307. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY_ISO_RX_SPARE_1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-617. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------|
| 31-0 | PHY_ISO_RX_SPARE_1 | R | 0h | spare register |

11.309 DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_2 Register (Offset = C4Ch) [reset = 0h]

DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_2 is shown in [Figure 11-308](#) and described in [Table 11-619](#).

Return to [Summary Table](#).

PHY_ISO_RX_SPARE_2

Table 11-618.
DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_2 Instances

| Instance | Physical Address |
|--|------------------|
| DPHY_RX0_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0458 0C4Ch |
| DPHY_RX1_VBUS2APB_WRAP_VBUS_P_K3_DPHY_RX | 0459 0C4Ch |

Figure 11-308. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PHY_ISO_RX_SPARE_2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 11-619. DPHY_RX_VBUS2APB_ISO_LDD_PHY_ISO_RX_SPARE_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------|
| 31-0 | PHY_ISO_RX_SPARE_2 | R | 0h | spare register |

11.310 DPHY_RX_MMR_SLV Registers

Table 11-621 lists the memory-mapped registers for the DPHY_RX_MMR_SLV registers. All register offset addresses not listed in Table 11-621 should be considered as reserved locations and the register contents should not be modified.

Table 11-620. DPHY_RX_MMR_SLV Instances

| Instance | Base Address |
|-------------------------------|--------------|
| DPHY_RX0_MMR_SLV_K3_DPHY_WRAP | 0458 0000h |
| DPHY_RX1_MMR_SLV_K3_DPHY_WRAP | 0459 0000h |

Table 11-621. DPHY_RX_MMR_SLV Registers

| Offset | Acronym | Register Name | DPHY_RX0_MMR_SLV_K3_DPHY_WRAP Physical Address | DPHY_RX1_MMR_SLV_K3_DPHY_WRAP Physical Address |
|--------|----------------------|---|--|--|
| 1000h | DPHY_RX_MMR_SLV_LANE | DPHY_RX_MMR_SLV_LANE control and status | 0458 1000h | 0459 1000h |

11.311 DPHY_RX_MMR_SLV_LANE Register (Offset = 1000h) [reset = X]

DPHY_RX_MMR_SLV_LANE is shown in [Figure 11-309](#) and described in [Table 11-623](#).

Return to [Summary Table](#).

DPHY_RX_MMR_SLV_LANE control and status

Table 11-622. DPHY_RX_MMR_SLV_LANE Instances

| Instance | Physical Address |
|--------------------------------|------------------|
| DPHY_RX0_MMR_SLV_K3_DPHY_WR AP | 0458 1000h |
| DPHY_RX1_MMR_SLV_K3_DPHY_WR AP | 0459 1000h |

Figure 11-309. DPHY_RX_MMR_SLV_LANE Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------|--------------------------|--------------------------|-------------------------|-------------------------|--------------------------|--------------------------|-------------------------|
| RXCLKACTIVE HSCLK | CMN_READY | RESERVED | | | | PSO_DISABLE | PSO_CMN |
| R-0h | R-0h | R/W-X | | | | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LANE_RSTB_C MN | PSM_CLOCK_FREQ | | | | | | |
| R/W-0h | R/W-0h | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | IPCONFIG_CMN | | | CLK_SWAPDP DN_DL_L_3 |
| R/W-X | | | | R/W-0h | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK_SWAPDP DN_DL_L_2 | DATA_SWAPD PDN_DL_L_3 | DATA_SWAPD PDN_DL_L_2 | CLK_SWAPDP DN_DL_L_1 | CLK_SWAPDP DN_DL_L_0 | DATA_SWAPD PDN_DL_L_1 | DATA_SWAPD PDN_DL_L_0 | CLK_SWAPDP DN_CL_L |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 11-623. DPHY_RX_MMR_SLV_LANE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 31 | RXCLKACTIVEHSCLK | R | 0h | Receiver high speed clock active: Driven active when the receiver high speed clock is active. 1'b 0: Receiver high speed clock not active, 1'b 1: Receiver high speed clock active |
| 30 | CMN_READY | R | 0h | Common ready indication: Indicates the completion of the startup process of the common module. Once this signal is driven active, the PMA lanes may be released from reset. 1'b 0 : Indicates that the startup process for the common components is not complete. This will be the case for both the power on reset sequence, and when the common is transitioning into and out of the low power modes. 1'b 1: Indicates that the startup process for the common components is complete and the common is ready. Note that this is a function of the PLL being enabled and locked. |

Table 11-623. DPHY_RX_MMR_SLV_LANE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 29-27 | RESERVED | R/W | X | |
| 26 | PSO_DISABLE | R/W | 0h | <p>Disable power shut off: Disables the ability to switch off the analog switched power islands in the DPHY_RX_MMR_SLV_LANE when in the ultra low power state.</p> <p>1'b</p> <p>0: Power islands are switched off and on under the normal control of the escape mode process.</p> <p>1'b</p> <p>1: Power island shutoff functions disabled, and switched power islands forced to the enabled state.</p> |
| 25 | RESERVED | R/W | X | |
| 24 | PSO_CMN | R/W | 0h | <p>Disable power shut off: Power Shutoff signal for CMN</p> <p>1 : CMN is power OFF</p> <p>0 : CMN is power ON</p> |
| 23 | LANE_RSTB_CMN | R/W | 0h | <p>[Only on SR1.1+] SW reset for CMN.</p> <p>0: asserted</p> <p>1: released</p> |
| 22-16 | PSM_CLOCK_FREQ | R/W | 0h | <p>PMA state machine clock frequency divider control: This signal specifies a divider value used to create an internal divided clock that is a function of the psm_clock clock.</p> <p>This signal must be driven with a value such that the frequency of the divided clock is 1 MHz.</p> <p>In the case where it is not possible for the divided clock to be exactly 1 MHz, a value should be selected that results in the clock frequency being the closest to 1 MHz.</p> <p>The following specifies the divider settings that the values of this signal correspond to.</p> <p># 8'h</p> <p>00 : Reserved # 8'h</p> <p>01 : Div 1 # 8'h</p> <p>02 : Div 2 # 8'h</p> <p>03 : Div 3 # 8'h</p> <p>04 : Div 4 ...</p> <p># 8'hFF : Div 255 Note: PSM clock has a maximum frequency of 100 MHz.</p> <p>values beyond 100 should not be programmed</p> |
| 15-12 | RESERVED | R/W | X | |
| 11-9 | IPCONFIG_CMN | R/W | 0h | <p>This signal decides which clock DPHY_RX_MMR_SLV_LANE acts as master clock DPHY_RX_MMR_SLV_LANE to all data lanes.</p> <p>Needed only for RX IP.</p> <p>Bit[2]: Reserved CASE {Bit[1],Bit[0]}:</p> <p>00: Left RX clk DPHY_RX_MMR_SLV_LANE provides clock to all left and right data lanes.</p> <p>01: Left RX clk DPHY_RX_MMR_SLV_LANE provides clock to all right data lanes, Right RX clk DPHY_RX_MMR_SLV_LANE provides clock to all left data lanes.</p> <p>10: Right RX clk DPHY_RX_MMR_SLV_LANE provides clock to all right data lanes, Left RX clk DPHY_RX_MMR_SLV_LANE provides clock to all left data lanes.</p> <p>11: Right RX clk DPHY_RX_MMR_SLV_LANE provides clock to all left and right data lanes.</p> |

Table 11-623. DPHY_RX_MMR_SLV_LANE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 8 | CLK_SWAPDPDN_DL_L_3 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 7 | CLK_SWAPDPDN_DL_L_2 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 6 | DATA_SWAPDPDN_DL_L_3 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 5 | DATA_SWAPDPDN_DL_L_2 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 4 | CLK_SWAPDPDN_DL_L_1 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 3 | CLK_SWAPDPDN_DL_L_0 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 2 | DATA_SWAPDPDN_DL_L_1 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 1 | DATA_SWAPDPDN_DL_L_0 | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |
| 0 | CLK_SWAPDPDN_CL_L | R/W | 0h | Swap DP and DN: When enabled, the rx_p and rx_m differential pins will be swapped. 1'b 0: Not swapped 1'b 1: Swapped |

12 DPHY_TX Registers

Table 12-2 lists the memory-mapped registers for the DPHY_TX registers. All register offset addresses not listed in Table 12-2 should be considered as reserved locations and the register contents should not be modified.

This is the MMR register region for the DPHY_TX component

Table 12-1. DPHY_TX Instances

| Instance | Base Address |
|----------|--------------|
| DPHY_TX0 | 0448 0000h |

Table 12-2. DPHY_TX Registers

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|-----------------------------|---------------|---------------------------------|
| 0h | DPHY_TX_CMN0_CMN_ANA_TBIT0 | | 0448 0000h |
| 4h | DPHY_TX_CMN0_CMN_ANA_TBIT1 | | 0448 0004h |
| 8h | DPHY_TX_CMN0_CMN_ANA_TBIT2 | | 0448 0008h |
| Ch | DPHY_TX_CMN0_CMN_ANA_TBIT3 | | 0448 000Ch |
| 10h | DPHY_TX_CMN0_CMN_ANA_TBIT4 | | 0448 0010h |
| 14h | DPHY_TX_CMN0_CMN_ANA_TBIT5 | | 0448 0014h |
| 18h | DPHY_TX_CMN0_CMN_DIG_TBIT0 | | 0448 0018h |
| 1Ch | DPHY_TX_CMN0_CMN_DIG_TBIT1 | | 0448 001Ch |
| 20h | DPHY_TX_CMN0_CMN_DIG_TBIT2 | | 0448 0020h |
| 24h | DPHY_TX_CMN0_CMN_DIG_TBIT3 | | 0448 0024h |
| 28h | DPHY_TX_CMN0_CMN_DIG_TBIT4 | | 0448 0028h |
| 2Ch | DPHY_TX_CMN0_CMN_DIG_TBIT5 | | 0448 002Ch |
| 30h | DPHY_TX_CMN0_CMN_DIG_TBIT6 | | 0448 0030h |
| 34h | DPHY_TX_CMN0_CMN_DIG_TBIT7 | | 0448 0034h |
| 38h | DPHY_TX_CMN0_CMN_DIG_TBIT8 | | 0448 0038h |
| 3Ch | DPHY_TX_CMN0_CMN_DIG_TBIT9 | | 0448 003Ch |
| 40h | DPHY_TX_CMN0_CMN_DIG_TBIT10 | | 0448 0040h |
| 44h | DPHY_TX_CMN0_CMN_DIG_TBIT11 | | 0448 0044h |
| 48h | DPHY_TX_CMN0_CMN_DIG_TBIT12 | | 0448 0048h |
| 4Ch | DPHY_TX_CMN0_CMN_DIG_TBIT13 | | 0448 004Ch |
| 50h | DPHY_TX_CMN0_CMN_DIG_TBIT14 | | 0448 0050h |
| 68h | DPHY_TX_CMN0_CMN_DIG_TBIT20 | | 0448 0068h |
| 6Ch | DPHY_TX_CMN0_CMN_DIG_TBIT21 | | 0448 006Ch |
| 70h | DPHY_TX_CMN0_CMN_DIG_TBIT22 | | 0448 0070h |
| 74h | DPHY_TX_CMN0_CMN_DIG_TBIT23 | | 0448 0074h |
| 78h | DPHY_TX_CMN0_CMN_DIG_TBIT24 | | 0448 0078h |
| 7Ch | DPHY_TX_CMN0_CMN_DIG_TBIT25 | | 0448 007Ch |
| 80h | DPHY_TX_CMN0_CMN_DIG_TBIT26 | | 0448 0080h |
| 84h | DPHY_TX_CMN0_CMN_DIG_TBIT27 | | 0448 0084h |
| 88h | DPHY_TX_CMN0_CMN_DIG_TBIT28 | | 0448 0088h |
| 94h | DPHY_TX_CMN0_CMN_DIG_TBIT31 | | 0448 0094h |
| 98h | DPHY_TX_CMN0_CMN_DIG_TBIT32 | | 0448 0098h |
| 9Ch | DPHY_TX_CMN0_CMN_DIG_TBIT33 | | 0448 009Ch |
| A0h | DPHY_TX_CMN0_CMN_DIG_TBIT34 | | 0448 00A0h |
| A4h | DPHY_TX_CMN0_CMN_DIG_TBIT35 | | 0448 00A4h |
| A8h | DPHY_TX_CMN0_CMN_DIG_TBIT36 | | 0448 00A8h |
| ACh | DPHY_TX_CMN0_CMN_DIG_TBIT37 | | 0448 00ACh |

Table 12-2. DPHY_TX Registers (continued)

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|---|---------------|---------------------------------|
| B4h | DPHY_TX_CMN0_CMN_DIG_TBIT39 | | 0448 00B4h |
| D8h | DPHY_TX_CMN0_CMN_DIG_TBIT50 | | 0448 00D8h |
| E4h | DPHY_TX_CMN0_CMN_DIG_TBIT53 | | 0448 00E4h |
| E8h | DPHY_TX_CMN0_CMN_DIG_TBIT54 | | 0448 00E8h |
| F0h | DPHY_TX_CMN0_CMN_DIG_TBIT56 | | 0448 00F0h |
| F8h | DPHY_TX_CMN0_CMN_DIG_TBIT58 | | 0448 00F8h |
| 100h | DPHY_TX_CLK0_TX_ANA_TBIT0 | | 0448 0100h |
| 104h | DPHY_TX_CLK0_TX_ANA_TBIT1 | | 0448 0104h |
| 108h | DPHY_TX_CLK0_TX_ANA_TBIT2 | | 0448 0108h |
| 10Ch | DPHY_TX_CLK0_TX_ANA_TBIT3 | | 0448 010Ch |
| 110h | DPHY_TX_CLK0_TX_ANA_TBIT4 | | 0448 0110h |
| 11Ch | DPHY_TX_CLK0_TX_DIG_TBIT0 | | 0448 011Ch |
| 120h | DPHY_TX_CLK0_TX_DIG_TBIT1 | | 0448 0120h |
| 124h | DPHY_TX_CLK0_TX_DIG_TBIT2 | | 0448 0124h |
| 13Ch | DPHY_TX_CLK0_TX_DIG_TBIT8 | | 0448 013Ch |
| 140h | DPHY_TX_CLK0_TX_DIG_TBIT9 | | 0448 0140h |
| 144h | DPHY_TX_CLK0_TX_DIG_TBIT10 | | 0448 0144h |
| 154h | DPHY_TX_CLK0_TX_DIG_TBIT14 | | 0448 0154h |
| 158h | DPHY_TX_CLK0_TX_DIG_TBIT15 | | 0448 0158h |
| 15Ch | DPHY_TX_CLK0_TX_DIG_TBIT16 | | 0448 015Ch |
| 160h | DPHY_TX_CLK0_TX_DIG_TBIT17 | | 0448 0160h |
| 164h | DPHY_TX_CLK0_TX_DIG_TBIT18 | | 0448 0164h |
| 168h | DPHY_TX_CLK0_TX_DIG_TBIT19 | | 0448 0168h |
| 16Ch | DPHY_TX_CLK0_TX_DIG_TBIT20 | | 0448 016Ch |
| 170h | DPHY_TX_CLK0_TX_ANA_TBIT5 | | 0448 0170h |
| 17Ch | DPHY_TX_CLK0_TX_DIG_TBIT21 | | 0448 017Ch |
| 180h | DPHY_TX_CLK0_TX_DIG_TBIT22 | | 0448 0180h |
| 188h | DPHY_TX_CLK0_TX_DIG_TBIT24 | | 0448 0188h |
| 18Ch | DPHY_TX_CLK0_TX_DIG_TBIT25 | | 0448 018Ch |
| 190h | DPHY_TX_CLK0_TX_DIG_TBIT26 | | 0448 0190h |
| 194h | DPHY_TX_CLK0_TX_DIG_TBIT27 | | 0448 0194h |
| 198h | DPHY_TX_CLK0_TX_DIG_TBIT28 | | 0448 0198h |
| 19Ch | DPHY_TX_CLK0_TX_DIG_TBIT29 | | 0448 019Ch |
| 200h | DPHY_TX_DL0_TX_ANA_TBIT0 | | 0448 0200h |
| 204h | DPHY_TX_DL0_TX_ANA_TBIT1 | | 0448 0204h |
| 208h | DPHY_TX_DL0_TX_ANA_TBIT2 | | 0448 0208h |
| 20Ch | DPHY_TX_DL0_TX_ANA_TBIT3 | | 0448 020Ch |
| 210h | DPHY_TX_DL0_TX_ANA_TBIT4 | | 0448 0210h |
| 21Ch | DPHY_TX_DL0_TX_DIG_TBIT0 | | 0448 021Ch |
| 220h | DPHY_TX_DL0_TX_DIG_TBIT1 | | 0448 0220h |
| 224h | DPHY_TX_DL0_TX_DIG_TBIT2 | | 0448 0224h |
| 228h | DPHY_TX_DL0_TX_DIG_TBIT3 | | 0448 0228h |
| 22Ch | DPHY_TX_DL0_TX_DIG_TBIT4 | | 0448 022Ch |
| 230h | DPHY_TX_DL0_TX_DIG_TBIT5 | | 0448 0230h |
| 234h | DPHY_TX_DL0_TX_DIG_TBIT6 | | 0448 0234h |

Table 12-2. DPHY_TX Registers (continued)

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|---|---------------|---------------------------------|
| 238h | DPHY_TX_DL0_TX_DIG_TBIT7 | | 0448 0238h |
| 23Ch | DPHY_TX_DL0_TX_DIG_TBIT8 | | 0448 023Ch |
| 240h | DPHY_TX_DL0_TX_DIG_TBIT9 | | 0448 0240h |
| 244h | DPHY_TX_DL0_TX_DIG_TBIT10 | | 0448 0244h |
| 248h | DPHY_TX_DL0_TX_DIG_TBIT11 | | 0448 0248h |
| 24Ch | DPHY_TX_DL0_TX_DIG_TBIT12 | | 0448 024Ch |
| 250h | DPHY_TX_DL0_TX_DIG_TBIT13 | | 0448 0250h |
| 254h | DPHY_TX_DL0_TX_DIG_TBIT14 | | 0448 0254h |
| 258h | DPHY_TX_DL0_TX_DIG_TBIT15 | | 0448 0258h |
| 25Ch | DPHY_TX_DL0_TX_DIG_TBIT16 | | 0448 025Ch |
| 260h | DPHY_TX_DL0_TX_DIG_TBIT17 | | 0448 0260h |
| 264h | DPHY_TX_DL0_TX_DIG_TBIT18 | | 0448 0264h |
| 268h | DPHY_TX_DL0_TX_DIG_TBIT19 | | 0448 0268h |
| 26Ch | DPHY_TX_DL0_TX_DIG_TBIT20 | | 0448 026Ch |
| 270h | DPHY_TX_DL0_TX_DIG_TBIT21 | | 0448 0270h |
| 274h | DPHY_TX_DL0_TX_DIG_TBIT22 | | 0448 0274h |
| 278h | DPHY_TX_DL0_TX_DIG_TBIT23 | | 0448 0278h |
| 27Ch | DPHY_TX_DL0_TX_DIG_TBIT24 | | 0448 027Ch |
| 280h | DPHY_TX_DL0_TX_ANA_TBIT5 | | 0448 0280h |
| 28Ch | DPHY_TX_DL0_TX_DIG_TBIT25 | | 0448 028Ch |
| 290h | DPHY_TX_DL0_TX_DIG_TBIT26 | | 0448 0290h |
| 298h | DPHY_TX_DL0_TX_DIG_TBIT28 | | 0448 0298h |
| 29Ch | DPHY_TX_DL0_TX_DIG_TBIT29 | | 0448 029Ch |
| 2A0h | DPHY_TX_DL0_TX_DIG_TBIT30 | | 0448 02A0h |
| 2A4h | DPHY_TX_DL0_TX_DIG_TBIT31 | | 0448 02A4h |
| 2A8h | DPHY_TX_DL0_TX_DIG_TBIT32 | | 0448 02A8h |
| 2ACh | DPHY_TX_DL0_TX_DIG_TBIT33 | | 0448 02ACh |
| 2B0h | DPHY_TX_DL0_TX_DIG_TBIT34 | | 0448 02B0h |
| 2B4h | DPHY_TX_DL0_TX_DIG_TBIT35 | | 0448 02B4h |
| 2B8h | DPHY_TX_DL0_TX_DIG_TBIT36 | | 0448 02B8h |
| 300h | DPHY_TX_DL1_TX_ANA_TBIT0 | | 0448 0300h |
| 304h | DPHY_TX_DL1_TX_ANA_TBIT1 | | 0448 0304h |
| 308h | DPHY_TX_DL1_TX_ANA_TBIT2 | | 0448 0308h |
| 30Ch | DPHY_TX_DL1_TX_ANA_TBIT3 | | 0448 030Ch |
| 310h | DPHY_TX_DL1_TX_ANA_TBIT4 | | 0448 0310h |
| 31Ch | DPHY_TX_DL1_TX_DIG_TBIT0 | | 0448 031Ch |
| 320h | DPHY_TX_DL1_TX_DIG_TBIT1 | | 0448 0320h |
| 324h | DPHY_TX_DL1_TX_DIG_TBIT2 | | 0448 0324h |
| 328h | DPHY_TX_DL1_TX_DIG_TBIT3 | | 0448 0328h |
| 32Ch | DPHY_TX_DL1_TX_DIG_TBIT4 | | 0448 032Ch |
| 330h | DPHY_TX_DL1_TX_DIG_TBIT5 | | 0448 0330h |
| 334h | DPHY_TX_DL1_TX_DIG_TBIT6 | | 0448 0334h |
| 338h | DPHY_TX_DL1_TX_DIG_TBIT7 | | 0448 0338h |
| 33Ch | DPHY_TX_DL1_TX_DIG_TBIT8 | | 0448 033Ch |
| 340h | DPHY_TX_DL1_TX_DIG_TBIT9 | | 0448 0340h |

Table 12-2. DPHY_TX Registers (continued)

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|---------------------------|---------------|---------------------------------|
| 344h | DPHY_TX_DL1_TX_DIG_TBIT10 | | 0448 0344h |
| 348h | DPHY_TX_DL1_TX_DIG_TBIT11 | | 0448 0348h |
| 34Ch | DPHY_TX_DL1_TX_DIG_TBIT12 | | 0448 034Ch |
| 350h | DPHY_TX_DL1_TX_DIG_TBIT13 | | 0448 0350h |
| 354h | DPHY_TX_DL1_TX_DIG_TBIT14 | | 0448 0354h |
| 358h | DPHY_TX_DL1_TX_DIG_TBIT15 | | 0448 0358h |
| 35Ch | DPHY_TX_DL1_TX_DIG_TBIT16 | | 0448 035Ch |
| 360h | DPHY_TX_DL1_TX_DIG_TBIT17 | | 0448 0360h |
| 364h | DPHY_TX_DL1_TX_DIG_TBIT18 | | 0448 0364h |
| 368h | DPHY_TX_DL1_TX_DIG_TBIT19 | | 0448 0368h |
| 36Ch | DPHY_TX_DL1_TX_DIG_TBIT20 | | 0448 036Ch |
| 370h | DPHY_TX_DL1_TX_DIG_TBIT21 | | 0448 0370h |
| 374h | DPHY_TX_DL1_TX_DIG_TBIT22 | | 0448 0374h |
| 378h | DPHY_TX_DL1_TX_DIG_TBIT23 | | 0448 0378h |
| 37Ch | DPHY_TX_DL1_TX_DIG_TBIT24 | | 0448 037Ch |
| 380h | DPHY_TX_DL1_TX_ANA_TBIT5 | | 0448 0380h |
| 38Ch | DPHY_TX_DL1_TX_DIG_TBIT25 | | 0448 038Ch |
| 390h | DPHY_TX_DL1_TX_DIG_TBIT26 | | 0448 0390h |
| 398h | DPHY_TX_DL1_TX_DIG_TBIT28 | | 0448 0398h |
| 39Ch | DPHY_TX_DL1_TX_DIG_TBIT29 | | 0448 039Ch |
| 3A0h | DPHY_TX_DL1_TX_DIG_TBIT30 | | 0448 03A0h |
| 3A4h | DPHY_TX_DL1_TX_DIG_TBIT31 | | 0448 03A4h |
| 3A8h | DPHY_TX_DL1_TX_DIG_TBIT32 | | 0448 03A8h |
| 3ACh | DPHY_TX_DL1_TX_DIG_TBIT33 | | 0448 03ACh |
| 3B0h | DPHY_TX_DL1_TX_DIG_TBIT34 | | 0448 03B0h |
| 3B4h | DPHY_TX_DL1_TX_DIG_TBIT35 | | 0448 03B4h |
| 3B8h | DPHY_TX_DL1_TX_DIG_TBIT36 | | 0448 03B8h |
| 400h | DPHY_TX_DL2_TX_ANA_TBIT0 | | 0448 0400h |
| 404h | DPHY_TX_DL2_TX_ANA_TBIT1 | | 0448 0404h |
| 408h | DPHY_TX_DL2_TX_ANA_TBIT2 | | 0448 0408h |
| 40Ch | DPHY_TX_DL2_TX_ANA_TBIT3 | | 0448 040Ch |
| 410h | DPHY_TX_DL2_TX_ANA_TBIT4 | | 0448 0410h |
| 41Ch | DPHY_TX_DL2_TX_DIG_TBIT0 | | 0448 041Ch |
| 420h | DPHY_TX_DL2_TX_DIG_TBIT1 | | 0448 0420h |
| 424h | DPHY_TX_DL2_TX_DIG_TBIT2 | | 0448 0424h |
| 428h | DPHY_TX_DL2_TX_DIG_TBIT3 | | 0448 0428h |
| 42Ch | DPHY_TX_DL2_TX_DIG_TBIT4 | | 0448 042Ch |
| 430h | DPHY_TX_DL2_TX_DIG_TBIT5 | | 0448 0430h |
| 434h | DPHY_TX_DL2_TX_DIG_TBIT6 | | 0448 0434h |
| 438h | DPHY_TX_DL2_TX_DIG_TBIT7 | | 0448 0438h |
| 43Ch | DPHY_TX_DL2_TX_DIG_TBIT8 | | 0448 043Ch |
| 440h | DPHY_TX_DL2_TX_DIG_TBIT9 | | 0448 0440h |
| 444h | DPHY_TX_DL2_TX_DIG_TBIT10 | | 0448 0444h |
| 448h | DPHY_TX_DL2_TX_DIG_TBIT11 | | 0448 0448h |
| 44Ch | DPHY_TX_DL2_TX_DIG_TBIT12 | | 0448 044Ch |

Table 12-2. DPHY_TX Registers (continued)

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|---------------------------|---------------|---------------------------------|
| 450h | DPHY_TX_DL2_TX_DIG_TBIT13 | | 0448 0450h |
| 454h | DPHY_TX_DL2_TX_DIG_TBIT14 | | 0448 0454h |
| 458h | DPHY_TX_DL2_TX_DIG_TBIT15 | | 0448 0458h |
| 45Ch | DPHY_TX_DL2_TX_DIG_TBIT16 | | 0448 045Ch |
| 460h | DPHY_TX_DL2_TX_DIG_TBIT17 | | 0448 0460h |
| 464h | DPHY_TX_DL2_TX_DIG_TBIT18 | | 0448 0464h |
| 468h | DPHY_TX_DL2_TX_DIG_TBIT19 | | 0448 0468h |
| 46Ch | DPHY_TX_DL2_TX_DIG_TBIT20 | | 0448 046Ch |
| 470h | DPHY_TX_DL2_TX_DIG_TBIT21 | | 0448 0470h |
| 474h | DPHY_TX_DL2_TX_DIG_TBIT22 | | 0448 0474h |
| 478h | DPHY_TX_DL2_TX_DIG_TBIT23 | | 0448 0478h |
| 47Ch | DPHY_TX_DL2_TX_DIG_TBIT24 | | 0448 047Ch |
| 480h | DPHY_TX_DL2_TX_ANA_TBIT5 | | 0448 0480h |
| 48Ch | DPHY_TX_DL2_TX_DIG_TBIT25 | | 0448 048Ch |
| 490h | DPHY_TX_DL2_TX_DIG_TBIT26 | | 0448 0490h |
| 498h | DPHY_TX_DL2_TX_DIG_TBIT28 | | 0448 0498h |
| 49Ch | DPHY_TX_DL2_TX_DIG_TBIT29 | | 0448 049Ch |
| 4A0h | DPHY_TX_DL2_TX_DIG_TBIT30 | | 0448 04A0h |
| 4A4h | DPHY_TX_DL2_TX_DIG_TBIT31 | | 0448 04A4h |
| 4A8h | DPHY_TX_DL2_TX_DIG_TBIT32 | | 0448 04A8h |
| 4ACh | DPHY_TX_DL2_TX_DIG_TBIT33 | | 0448 04ACh |
| 4B0h | DPHY_TX_DL2_TX_DIG_TBIT34 | | 0448 04B0h |
| 4B4h | DPHY_TX_DL2_TX_DIG_TBIT35 | | 0448 04B4h |
| 4B8h | DPHY_TX_DL2_TX_DIG_TBIT36 | | 0448 04B8h |
| 500h | DPHY_TX_DL3_TX_ANA_TBIT0 | | 0448 0500h |
| 504h | DPHY_TX_DL3_TX_ANA_TBIT1 | | 0448 0504h |
| 508h | DPHY_TX_DL3_TX_ANA_TBIT2 | | 0448 0508h |
| 50Ch | DPHY_TX_DL3_TX_ANA_TBIT3 | | 0448 050Ch |
| 510h | DPHY_TX_DL3_TX_ANA_TBIT4 | | 0448 0510h |
| 51Ch | DPHY_TX_DL3_TX_DIG_TBIT0 | | 0448 051Ch |
| 520h | DPHY_TX_DL3_TX_DIG_TBIT1 | | 0448 0520h |
| 524h | DPHY_TX_DL3_TX_DIG_TBIT2 | | 0448 0524h |
| 528h | DPHY_TX_DL3_TX_DIG_TBIT3 | | 0448 0528h |
| 52Ch | DPHY_TX_DL3_TX_DIG_TBIT4 | | 0448 052Ch |
| 530h | DPHY_TX_DL3_TX_DIG_TBIT5 | | 0448 0530h |
| 534h | DPHY_TX_DL3_TX_DIG_TBIT6 | | 0448 0534h |
| 538h | DPHY_TX_DL3_TX_DIG_TBIT7 | | 0448 0538h |
| 53Ch | DPHY_TX_DL3_TX_DIG_TBIT8 | | 0448 053Ch |
| 540h | DPHY_TX_DL3_TX_DIG_TBIT9 | | 0448 0540h |
| 544h | DPHY_TX_DL3_TX_DIG_TBIT10 | | 0448 0544h |
| 548h | DPHY_TX_DL3_TX_DIG_TBIT11 | | 0448 0548h |
| 54Ch | DPHY_TX_DL3_TX_DIG_TBIT12 | | 0448 054Ch |
| 550h | DPHY_TX_DL3_TX_DIG_TBIT13 | | 0448 0550h |
| 554h | DPHY_TX_DL3_TX_DIG_TBIT14 | | 0448 0554h |
| 558h | DPHY_TX_DL3_TX_DIG_TBIT15 | | 0448 0558h |

Table 12-2. DPHY_TX Registers (continued)

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|--|---------------|---------------------------------|
| 55Ch | DPHY_TX_DL3_TX_DIG_TBIT16 | | 0448 055Ch |
| 560h | DPHY_TX_DL3_TX_DIG_TBIT17 | | 0448 0560h |
| 564h | DPHY_TX_DL3_TX_DIG_TBIT18 | | 0448 0564h |
| 568h | DPHY_TX_DL3_TX_DIG_TBIT19 | | 0448 0568h |
| 56Ch | DPHY_TX_DL3_TX_DIG_TBIT20 | | 0448 056Ch |
| 570h | DPHY_TX_DL3_TX_DIG_TBIT21 | | 0448 0570h |
| 574h | DPHY_TX_DL3_TX_DIG_TBIT22 | | 0448 0574h |
| 578h | DPHY_TX_DL3_TX_DIG_TBIT23 | | 0448 0578h |
| 57Ch | DPHY_TX_DL3_TX_DIG_TBIT24 | | 0448 057Ch |
| 580h | DPHY_TX_DL3_TX_ANA_TBIT5 | | 0448 0580h |
| 58Ch | DPHY_TX_DL3_TX_DIG_TBIT25 | | 0448 058Ch |
| 590h | DPHY_TX_DL3_TX_DIG_TBIT26 | | 0448 0590h |
| 598h | DPHY_TX_DL3_TX_DIG_TBIT28 | | 0448 0598h |
| 59Ch | DPHY_TX_DL3_TX_DIG_TBIT29 | | 0448 059Ch |
| 5A0h | DPHY_TX_DL3_TX_DIG_TBIT30 | | 0448 05A0h |
| 5A4h | DPHY_TX_DL3_TX_DIG_TBIT31 | | 0448 05A4h |
| 5A8h | DPHY_TX_DL3_TX_DIG_TBIT32 | | 0448 05A8h |
| 5ACh | DPHY_TX_DL3_TX_DIG_TBIT33 | | 0448 05ACh |
| 5B0h | DPHY_TX_DL3_TX_DIG_TBIT34 | | 0448 05B0h |
| 5B4h | DPHY_TX_DL3_TX_DIG_TBIT35 | | 0448 05B4h |
| 5B8h | DPHY_TX_DL3_TX_DIG_TBIT36 | | 0448 05B8h |
| B00h | DPHY_TX_PCS_TX_DIG_TBIT0 | | 0448 0B00h |
| B04h | DPHY_TX_PCS_TX_DIG_TBIT1 | | 0448 0B04h |
| B08h | DPHY_TX_PCS_TX_DIG_TBIT2 | | 0448 0B08h |
| B0Ch | DPHY_TX_PCS_TX_DIG_TBIT3 | | 0448 0B0Ch |
| B10h | DPHY_TX_PCS_TX_DIG_TBIT4 | | 0448 0B10h |
| B14h | DPHY_TX_PCS_TX_DIG_TBIT5 | | 0448 0B14h |
| B18h | DPHY_TX_PCS_TX_DIG_TBIT6 | | 0448 0B18h |
| B1Ch | DPHY_TX_PCS_TX_DIG_TBIT7 | | 0448 0B1Ch |
| B20h | DPHY_TX_PCS_TX_DIG_TBIT8 | | 0448 0B20h |
| B24h | DPHY_TX_PCS_TX_DIG_TBIT9 | | 0448 0B24h |
| B28h | DPHY_TX_PCS_TX_DIG_TBIT10 | | 0448 0B28h |
| C00h | DPHY_TX_ISO_PHY_ISO_CNTRL | | 0448 0C00h |
| C04h | DPHY_TX_ISO_PHY_ISO_RESET | | 0448 0C04h |
| C08h | DPHY_TX_ISO_PHY_ISO_ENABLE | | 0448 0C08h |
| C0Ch | DPHY_TX_ISO_PHY_ISO_CMN_CTRL | | 0448 0C0Ch |
| C10h | DPHY_TX_ISO_PHY_ISO_CMN_PLL | | 0448 0C10h |
| C14h | DPHY_TX_ISO_PHY_ISO_CL_CNTRL_L | | 0448 0C14h |
| C18h | DPHY_TX_ISO_PHY_ISO_DL_CTRL_L0 | | 0448 0C18h |
| C1Ch | DPHY_TX_ISO_PHY_ISO_DL_HS_L0 | | 0448 0C1Ch |
| C20h | DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 | | 0448 0C20h |
| C24h | DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L0 | | 0448 0C24h |
| C28h | DPHY_TX_ISO_PHY_ISO_DL_CTRL_L1 | | 0448 0C28h |
| C2Ch | DPHY_TX_ISO_PHY_ISO_DL_HS_L1 | | 0448 0C2Ch |
| C30h | DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 | | 0448 0C30h |

Table 12-2. DPHY_TX Registers (continued)

| Offset | Acronym | Register Name | DPHY_TX0 Physical Address |
|--------|--------------------------------------|--------------------------|---------------------------------|
| C34h | DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L1 | | 0448 0C34h |
| C38h | DPHY_TX_ISO_PHY_ISO_SPARE_1 | | 0448 0C38h |
| C3Ch | DPHY_TX_ISO_PHY_ISO_SPARE_2 | | 0448 0C3Ch |
| C40h | DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L2 | | 0448 0C40h |
| C44h | DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L2 | | 0448 0C44h |
| C48h | DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2 | | 0448 0C48h |
| C4Ch | DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 | | 0448 0C4Ch |
| C50h | DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L3 | | 0448 0C50h |
| C54h | DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L3 | | 0448 0C54h |
| C58h | DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3 | | 0448 0C58h |
| C5Ch | DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 | | 0448 0C5Ch |
| F00h | DPHY_TX_MOD_VER | Module and Version | 0448 0F00h |
| F04h | DPHY_TX_PLL_CTRL | PLL Control | 0448 0F04h |
| F08h | DPHY_TX_STATUS | Status Register | 0448 0F08h |
| F0Ch | DPHY_TX_RST_CTRL | RST Control | 0448 0F0Ch |
| F10h | DPHY_TX_PSM_FREQ | PSM Frequency | 0448 0F10h |
| F14h | DPHY_TX_IPCONFIG | IP Config | 0448 0F14h |
| FF8h | DPHY_TX_PLLRES | PLL Reserved | 0448 0FF8h |
| FFCh | DPHY_TX_DIAG_TEST | Diagnostic Test Register | 0448 0FFCh |

12.1 DPHY_TX_CMN0_CMN_ANA_TBIT0 Register (Offset = 0h) [reset = 0h]

DPHY_TX_CMN0_CMN_ANA_TBIT0 is shown in [Figure 12-1](#) and described in [Table 12-4](#).

Return to [Summary Table](#).

CMN_ANA_TBIT0

**Table 12-3. DPHY_TX_CMN0_CMN_ANA_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0000h |

Figure 12-1. DPHY_TX_CMN0_CMN_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-4. DPHY_TX_CMN0_CMN_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CMN0_ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

12.2 DPHY_TX_CMN0_CMN_ANA_TBIT1 Register (Offset = 4h) [reset = 0h]

DPHY_TX_CMN0_CMN_ANA_TBIT1 is shown in [Figure 12-2](#) and described in [Table 12-6](#).

Return to [Summary Table](#).

CMN_ANA_TBIT1

Table 12-5. DPHY_TX_CMN0_CMN_ANA_TBIT1 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0004h |

Figure 12-2. DPHY_TX_CMN0_CMN_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-6. DPHY_TX_CMN0_CMN_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CMN0_ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

12.3 DPHY_TX_CMN0_CMN_ANA_TBIT2 Register (Offset = 8h) [reset = 0h]

DPHY_TX_CMN0_CMN_ANA_TBIT2 is shown in [Figure 12-3](#) and described in [Table 12-8](#).

Return to [Summary Table](#).

CMN_ANA_TBIT2

**Table 12-7. DPHY_TX_CMN0_CMN_ANA_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0008h |

Figure 12-3. DPHY_TX_CMN0_CMN_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-8. DPHY_TX_CMN0_CMN_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CMN0_ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

12.4 DPHY_TX_CMN0_CMN_ANA_TBIT3 Register (Offset = Ch) [reset = 0h]

DPHY_TX_CMN0_CMN_ANA_TBIT3 is shown in [Figure 12-4](#) and described in [Table 12-10](#).

Return to [Summary Table](#).

CMN_ANA_TBIT3

Table 12-9. DPHY_TX_CMN0_CMN_ANA_TBIT3 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 000Ch |

Figure 12-4. DPHY_TX_CMN0_CMN_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-10. DPHY_TX_CMN0_CMN_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | CMN0_ANA_TBIT3 | R | 0h | RESERVED |

12.5 DPHY_TX_CMN0_CMN_ANA_TBIT4 Register (Offset = 10h) [reset = 0h]

DPHY_TX_CMN0_CMN_ANA_TBIT4 is shown in [Figure 12-5](#) and described in [Table 12-12](#).

Return to [Summary Table](#).

CMN_ANA_TBIT4

**Table 12-11. DPHY_TX_CMN0_CMN_ANA_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0010h |

Figure 12-5. DPHY_TX_CMN0_CMN_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-12. DPHY_TX_CMN0_CMN_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CMN0_ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

12.6 DPHY_TX_CMN0_CMN_ANA_TBIT5 Register (Offset = 14h) [reset = X]

DPHY_TX_CMN0_CMN_ANA_TBIT5 is shown in [Figure 12-6](#) and described in [Table 12-14](#).

Return to [Summary Table](#).

CMN_ANA_TBIT5

Table 12-13. DPHY_TX_CMN0_CMN_ANA_TBIT5 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0014h |

Figure 12-6. DPHY_TX_CMN0_CMN_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CMN0_ANA_TBIT5 | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-14. DPHY_TX_CMN0_CMN_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-8 | RESERVED | R/W | X | |
| 7-0 | CMN0_ANA_TBIT5 | R/W | 0h | Analog Test register 5 |

12.7 DPHY_TX_CMN0_CMN_DIG_TBIT0 Register (Offset = 18h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT0 is shown in [Figure 12-7](#) and described in [Table 12-16](#).

Return to [Summary Table](#).

CMN_DIG_TBIT0

Table 12-15. DPHY_TX_CMN0_CMN_DIG_TBIT0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0018h |

Figure 12-7. DPHY_TX_CMN0_CMN_DIG_TBIT0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------------|----------------------------------|-----------------------------------|-----------------------------------|-----------------------------|--------------------------------|----------------------------------|----|
| RESERVED | | | CMN0_O_RES_CAL_START_TM | CMN0_O_RES_CAL_START_TM_SEL | CMN0_O_RES_COMP_OUT_POL_INV_TM | CMN0_O_RES_TX_OFFSET_TEST_LOW_TM | |
| R/W-X | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_RES_TX_OFFSET_TEST_LOW_TM | CMN0_O_RES_TX_OFFSET_LOW_DEC_TM | CMN0_O_RES_TX_OFFSET_LOW_TM_SEL | CMN0_O_RES_TX_OFFSET_TEST_HIGH_TM | | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_RES_TX_OFFSET_HIGH_DEC_TM | CMN0_O_RES_TX_OFFSET_HIGH_TM_SEL | CMN0_O_RES_CALIB_DECISION_WAIT_TM | | | | CMN0_O_RES_CALIB_INIT_WAIT_TM | |
| R/W-0h | R/W-0h | R/W-4h | | | | R/W-5h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RES_CALIB_INIT_WAIT_TM | CMN0_O_RES_CALIB_RSTB_TM | CMN0_O_RES_CALIB_RSTB_TM_SEL | RESERVED | | | | |
| R/W-5h | R/W-0h | R/W-0h | R/W-X | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-16. DPHY_TX_CMN0_CMN_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------------|------|-------|--|
| 31-29 | RESERVED | R/W | X | |
| 28 | CMN0_O_RES_CAL_STA RT_TM | R/W | 0h | res_cal_start in test mode |
| 27 | CMN0_O_RES_CAL_STA RT_TM_SEL | R/W | 0h | res_cal_start select from test_mode |
| 26 | CMN0_O_RES_COMP_O UT_POL_INV_TM | R/W | 0h | Invert polarity for resistor calib comparator output |
| 25-22 | CMN0_O_RES_TX_OFFS ET_TEST_LOW_TM | R/W | 0h | o_res_tx_offset_test_low_TM - Res calib manipulation code for res calib code low |
| 21 | CMN0_O_RES_TX_OFFS ET_LOW_DEC_TM | R/W | 0h | o_res_tx_offset_low_dec_TM asserted - Perform increment manipulation on res calib code if o_res_tx_offset_low_TM_sel is asserted |
| 20 | CMN0_O_RES_TX_OFFS ET_LOW_TM_SEL | R/W | 0h | o_res_tx_offset_low_TM_sel asserted - Enable offset manipulation for res calib code low |
| 19-16 | CMN0_O_RES_TX_OFFS ET_TEST_HIGH_TM | R/W | 0h | o_res_tx_offset_test_high_TM - Res calib manipulation code for res calib code high |

Table 12-16. DPHY_TX_CMN0_CMN_DIG_TBIT0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 15 | CMN0_O_RES_TX_OFFSET_HIGH_DEC_TM | R/W | 0h | o_res_tx_offset_high_dec_TM asserted - Perform increment manipulation on res_calib code if o_res_tx_offset_high_TM_sel is asserted |
| 14 | CMN0_O_RES_TX_OFFSET_HIGH_TM_SEL | R/W | 0h | o_res_tx_offset_high_TM_sel asserted - Enable offset manipulation for res_calib code high |
| 13-10 | CMN0_O_RES_CALIB_DECISION_WAIT_TM | R/W | 4h | res_calib decision wait time |
| 9-6 | CMN0_O_RES_CALIB_INIT_WAIT_TM | R/W | 5h | res_calib initial wait time |
| 5 | CMN0_O_RES_CALIB_RSTB_TM | R/W | 0h | w_res_calib_rstb value in testmode |
| 4 | CMN0_O_RES_CALIB_RSTB_TM_SEL | R/W | 0h | w_res_calib_rstb select from test_mode |
| 3-0 | RESERVED | R/W | X | |

12.8 DPHY_TX_CMN0_CMN_DIG_TBIT1 Register (Offset = 1Ch) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT1 is shown in [Figure 12-8](#) and described in [Table 12-18](#).

Return to [Summary Table](#).

CMN_DIG_TBIT1

**Table 12-17. DPHY_TX_CMN0_CMN_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 001Ch |

Figure 12-8. DPHY_TX_CMN0_CMN_DIG_TBIT1 Register

| | | | | | | | |
|--------------------------------|--------------------------------|------------------------------|----|----|----|---------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_ATB_EN | CMN0_O_ATB_SRC | CMN0_BF_29_17 | | | | | |
| R/W-0h | R/W-0h | R/W-0h | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_BF_29_17 | | | | | | | CMN0_O_ANA_PLL_ATB_CP_CUR_SEL |
| R/W-0h | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_ANA_PLL_ATBH_GM_CUR_SEL | RESERVED | | | | | CMN0_O_ANA_BG_PD_TM | CMN0_O_ANA_BG_PD_TM_SEL |
| R/W-0h | R/W-X | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_RES_CALIB_PD_TM | CMN0_O_ANA_RES_CALIB_PD_TM_SEL | CMN0_O_ANA_RES_CALIB_CODE_TM | | | | | CMN0_O_ANA_RES_CALIB_CODE_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-18. DPHY_TX_CMN0_CMN_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31 | CMN0_O_ATB_EN | R/W | 0h | ATB probing enabled |
| 30 | CMN0_O_ATB_SRC | R/W | 0h | Select IO for atb probing |
| 29-17 | CMN0_BF_29_17 | R/W | 0h | atb sel |
| 16 | CMN0_O_ANA_PLL_ATB_CP_CUR_SEL | R/W | 0h | o_ana_pll_atb_cp_cur_sel |
| 15 | CMN0_O_ANA_PLL_ATBH_GM_CUR_SEL | R/W | 0h | o_ana_pll_atbh_gm_cur_sel |
| 14-10 | RESERVED | R/W | X | |
| 9 | CMN0_O_ANA_BG_PD_TM | R/W | 0h | o_ana_bg_pd value in testmode |
| 8 | CMN0_O_ANA_BG_PD_TM_SEL | R/W | 0h | o_ana_bg_pd select from test_mode |
| 7 | CMN0_O_ANA_RES_CALIB_PD_TM | R/W | 0h | o_ana_res_calib_pd value in testmode |
| 6 | CMN0_O_ANA_RES_CALIB_PD_TM_SEL | R/W | 0h | o_ana_res_calib_pd select from test_mode |

Table 12-18. DPHY_TX_CMN0_CMN_DIG_TBIT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------------------------|------|-------|--|
| 5-1 | CMN0_O_ANA_RES_CAL IB_CODE_TM | R/W | 0h | o_ana_res_calib_code value in test_mode |
| 0 | CMN0_O_ANA_RES_CAL IB_CODE_TM_SEL | R/W | 0h | o_ana_res_calib_code select from test_mode |

12.9 DPHY_TX_CMN0_CMN_DIG_TBIT2 Register (Offset = 20h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT2 is shown in [Figure 12-9](#) and described in [Table 12-20](#).

Return to [Summary Table](#).

CMN_DIG_TBIT2

**Table 12-19. DPHY_TX_CMN0_CMN_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0020h |

Figure 12-9. DPHY_TX_CMN0_CMN_DIG_TBIT2 Register

| | | | | | | | |
|--------------------------|----|----|----|----|-----------------------|-----------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | CMN0_O_CMN_RX_MODE_EN | CMN0_O_CMN_TX_MODE_EN | CMN0_O_SSM_WAIT_BGCAL_EN |
| R/W-X | | | | | R/W-0h | R/W-0h | R/W-14h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_SSM_WAIT_BGCAL_EN | | | | | | CMN0_O_CMN_SSM_EN | |
| R/W-14h | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-20. DPHY_TX_CMN0_CMN_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-11 | RESERVED | R/W | X | |
| 10 | CMN0_O_CMN_RX_MODE_EN | R/W | 0h | Enable CMN RX related StateMachines |
| 9 | CMN0_O_CMN_TX_MODE_EN | R/W | 0h | Enable CMN TX related StateMachines |
| 8-1 | CMN0_O_SSM_WAIT_BGCAL_EN | R/W | 14h | Wait time for Calibrations enable after bandgap is enabled (in us) |
| 0 | CMN0_O_CMN_SSM_EN | R/W | 0h | Enable CMN startup state machine |

12.10 DPHY_TX_CMN0_CMN_DIG_TBIT3 Register (Offset = 24h) [reset = 05030101h]

DPHY_TX_CMN0_CMN_DIG_TBIT3 is shown in [Figure 12-10](#) and described in [Table 12-22](#).

Return to [Summary Table](#).

CMN_DIG_TBIT3

Table 12-21. DPHY_TX_CMN0_CMN_DIG_TBIT3 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0024h |

Figure 12-10. DPHY_TX_CMN0_CMN_DIG_TBIT3 Register

| | | | | | | | |
|----------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_PLL_WAIT_PLL_ACCINV | | | | | | | |
| R/W-5h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_PLL_WAIT_PLL_BIAS | | | | | | | |
| R/W-3h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_PLL_WAIT_PLL_EN_DEL | | | | | | | |
| R/W-1h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_PLL_WAIT_PLL_EN | | | | | | | |
| R/W-1h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-22. DPHY_TX_CMN0_CMN_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|---------------------------------|
| 31-24 | CMN0_O_PLL_WAIT_PLL_ACCINV | R/W | 5h | Wait time in pll_accinv (in us) |
| 23-16 | CMN0_O_PLL_WAIT_PLL_BIAS | R/W | 3h | Wait time in pll_bias (in us) |
| 15-8 | CMN0_O_PLL_WAIT_PLL_EN_DEL | R/W | 1h | Wait time in pll_en_del (in us) |
| 7-0 | CMN0_O_PLL_WAIT_PLL_EN | R/W | 1h | Wait time in PLL en (in us) |

12.11 DPHY_TX_CMN0_CMN_DIG_TBIT4 Register (Offset = 28h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT4 is shown in [Figure 12-11](#) and described in [Table 12-24](#).

Return to [Summary Table](#).

CMN_DIG_TBIT4

**Table 12-23. DPHY_TX_CMN0_CMN_DIG_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0028h |

Figure 12-11. DPHY_TX_CMN0_CMN_DIG_TBIT4 Register

| | | | | | | | |
|------------------------------------|----|----|----|-----------------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | CMN0_O_PLL_WAIT_PLL_LOCK_DET_WAIT | | | |
| R/W-X | | | | R/W-32h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_PLL_WAIT_PLL_LOCK_DET_WAIT | | | | | | | |
| R/W-32h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_PLL_WAIT_PLL_RST_DEASSERT_2 | | | | | | | |
| R/W-1h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_PLL_WAIT_PLL_RST_DEASSERT | | | | | | | |
| R/W-1Eh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-24. DPHY_TX_CMN0_CMN_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|--|
| 31-28 | RESERVED | R/W | X | |
| 27-16 | CMN0_O_PLL_WAIT_PLL_LOCK_DET_WAIT | R/W | 32h | Wait time in pll_lock_det_wait (in us) |
| 15-8 | CMN0_O_PLL_WAIT_PLL_RST_DEASSERT_2 | R/W | 1h | Wait time in pll_rst_deassert_2ndset (in us) |
| 7-0 | CMN0_O_PLL_WAIT_PLL_RST_DEASSERT | R/W | 1Eh | Wait time in pll_rst_deassert (in us) |

12.12 DPHY_TX_CMN0_CMN_DIG_TBIT5 Register (Offset = 2Ch) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT5 is shown in [Figure 12-12](#) and described in [Table 12-26](#).

Return to [Summary Table](#).

CMN_DIG_TBIT5

Table 12-25. DPHY_TX_CMN0_CMN_DIG_TBIT5 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 002Ch |

Figure 12-12. DPHY_TX_CMN0_CMN_DIG_TBIT5 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------------|----|--------------------------------------|----------------------|--------------------------|---------------------------|----------------------------------|----------|
| CMN0_O_CMN_TX_READY_TM_SEL | | CMN0_O_PLL_PROCEED_WITH_LOCK_FAIL_TM | CMN0_O_PLL_LOCKED_TM | CMN0_O_PLL_LOCKED_TM_SEL | CMN0_O_PLL_LOCK_DET_EN_TM | CMN0_O_PLL_LOCK_DET_EN_TM_SEL | RESERVED |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | CMN0_O_PLL_WAIT_PLL_LOCK_TIMEOUT | |
| R/W-X | | | | | | R/W-400h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_PLL_WAIT_PLL_LOCK_TIMEOUT | | | | | | | |
| R/W-400h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_PLL_WAIT_PLL_LOCK_TIMEOUT | | | | | | | |
| R/W-400h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-26. DPHY_TX_CMN0_CMN_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------------|------|-------|--|
| 31-30 | CMN0_O_CMN_TX_READY_TM_SEL | R/W | 0h | ATB probing enabled |
| 29 | CMN0_O_PLL_PROCEED_WITH_LOCK_FAIL_TM | R/W | 0h | o_ana_pll_atb_cp_cur_sel |
| 28 | CMN0_O_PLL_LOCKED_TM | R/W | 0h | Forced value of pll_locked going to fsm = 1 |
| 27 | CMN0_O_PLL_LOCKED_TM_SEL | R/W | 0h | pll_locked going to fsm forced from test registers |
| 26 | CMN0_O_PLL_LOCK_DET_EN_TM | R/W | 0h | Forced value of pll_lock_det_en = 1 |
| 25 | CMN0_O_PLL_LOCK_DET_EN_TM_SEL | R/W | 0h | pll_lock_det_en forced from test registers |
| 24-18 | RESERVED | R/W | X | |
| 17-0 | CMN0_O_PLL_WAIT_PLL_LOCK_TIMEOUT | R/W | 400h | Wait time for pll_lock_timeout (in us) |

12.13 DPHY_TX_CMN0_CMN_DIG_TBIT6 Register (Offset = 30h) [reset = 000400C8h]

DPHY_TX_CMN0_CMN_DIG_TBIT6 is shown in [Figure 12-13](#) and described in [Table 12-28](#).

Return to [Summary Table](#).

CMN_DIG_TBIT6

**Table 12-27. DPHY_TX_CMN0_CMN_DIG_TBIT6
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0030h |

Figure 12-13. DPHY_TX_CMN0_CMN_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | |
|-----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_LOCKDET_REFCNT_IDLE_VALUE | | | | | | | | | | | | | | | |
| R/W-4h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_LOCKDET_REFCNT_START_VALUE | | | | | | | | | | | | | | | |
| R/W-C8h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-28. DPHY_TX_CMN0_CMN_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|---|
| 31-16 | CMN0_O_LOCKDET_REFCNT_IDLE_VALUE | R/W | 4h | refcnt idle value for PLL lock detect module |
| 15-0 | CMN0_O_LOCKDET_REFCNT_START_VALUE | R/W | C8h | refcnt start value for PLL lock detect module |

12.14 DPHY_TX_CMN0_CMN_DIG_TBIT7 Register (Offset = 34h) [reset = 000300C8h]

DPHY_TX_CMN0_CMN_DIG_TBIT7 is shown in [Figure 12-14](#) and described in [Table 12-30](#).

Return to [Summary Table](#).

CMN_DIG_TBIT7

Table 12-29. DPHY_TX_CMN0_CMN_DIG_TBIT7 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0034h |

Figure 12-14. DPHY_TX_CMN0_CMN_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | |
|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_LOCKDET_PLLCNT_LOCK_THR_VALUE | | | | | | | | | | | | | | | |
| R/W-3h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_LOCKDET_PLLCNT_START_VALUE | | | | | | | | | | | | | | | |
| R/W-C8h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-30. DPHY_TX_CMN0_CMN_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------------|------|-------|--|
| 31-16 | CMN0_O_LOCKDET_PLLCNT_LOCK_THR_VALUE | R/W | 3h | pllcnt lock threshold value for PLL lock detect module |
| 15-0 | CMN0_O_LOCKDET_PLLCNT_START_VALUE | R/W | C8h | pllcnt start value for PLL lock detect module |

12.15 DPHY_TX_CMN0_CMN_DIG_TBIT8 Register (Offset = 38h) [reset = 00080103h]

DPHY_TX_CMN0_CMN_DIG_TBIT8 is shown in [Figure 12-15](#) and described in [Table 12-32](#).

Return to [Summary Table](#).

CMN_DIG_TBIT8

**Table 12-31. DPHY_TX_CMN0_CMN_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0038h |

Figure 12-15. DPHY_TX_CMN0_CMN_DIG_TBIT8 Register

| | | | | | | | |
|-------------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_ANA_PLL_VRESET_VCTRL_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_ANA_PLL_VRESET_VCO_BIAS_TUNE | | | | | | | |
| R/W-8h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_ANA_PLL_GM_TUNE | | | | | | | |
| R/W-1h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_PLL_CP_TUNE | | | | | | | |
| R/W-3h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-32. DPHY_TX_CMN0_CMN_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-24 | CMN0_O_ANA_PLL_VRESET_VCTRL_TUNE | R/W | 0h | unconnected, intended for vreset_vctrl(CP output) programmability |
| 23-16 | CMN0_O_ANA_PLL_VRESET_VCO_BIAS_TUNE | R/W | 8h | Programmability for vco bias(gmbyc) initial voltage |
| 15-8 | CMN0_O_ANA_PLL_GM_TUNE | R/W | 1h | gm tune value for PLL |
| 7-0 | CMN0_O_ANA_PLL_CP_TUNE | R/W | 3h | Charge Pump Tune value for PLL |

12.16 DPHY_TX_CMN0_CMN_DIG_TBIT9 Register (Offset = 3Ch) [reset = 0h]

DPHY_TX_CMN0_CMN_DIG_TBIT9 is shown in [Figure 12-16](#) and described in [Table 12-34](#).

Return to [Summary Table](#).

CMN_DIG_TBIT9

Table 12-33. DPHY_TX_CMN0_CMN_DIG_TBIT9 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 003Ch |

Figure 12-16. DPHY_TX_CMN0_CMN_DIG_TBIT9 Register

| | | | | | | | |
|-----------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_ANA_PLL_VREF_VCO_BIAS_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_ANA_PLL_VCO_BIAS_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_ANA_PLL_GMBYC_CAP_TUNE | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_PLL_LOOP_FILTER_TUNE | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-34. DPHY_TX_CMN0_CMN_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-24 | CMN0_O_ANA_PLL_VREF_VCO_BIAS_TUNE | R/W | 0h | Tuning Control for reference vco bias in PLL |
| 23-16 | CMN0_O_ANA_PLL_VCO_BIAS_TUNE | R/W | 0h | Tuning Control for PLL vco bias |
| 15-8 | CMN0_O_ANA_PLL_GMBYC_CAP_TUNE | R/W | 0h | gmbyc tune value for PLL |
| 7-0 | CMN0_O_ANA_PLL_LOOP_FILTER_TUNE | R/W | 0h | Tuning Control for loop filter |

12.17 DPHY_TX_CMN0_CMN_DIG_TBIT10 Register (Offset = 40h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT10 is shown in [Figure 12-17](#) and described in [Table 12-36](#).

Return to [Summary Table](#).

CMN_DIG_TBIT10

**Table 12-35. DPHY_TX_CMN0_CMN_DIG_TBIT10
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0040h |

Figure 12-17. DPHY_TX_CMN0_CMN_DIG_TBIT10 Register

| | | | | | | | |
|--------------------------------|----|----|----|-------------------------------|----|--------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | CMN0_O_ANA_PLL_BYTECLK_DIV | | | |
| R/W-X | | | | R/W-8h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_ANA_PLL_BYTECLK_DIV | | | | CMN0_O_ANA_PLL_GM_PWM_DIV_LOW | | | |
| R/W-8h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_ANA_PLL_GM_PWM_DIV_LOW | | | | | | CMN0_O_ANA_PLL_GM_PWM_DIV_HIGH | |
| R/W-0h | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_PLL_GM_PWM_DIV_HIGH | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-36. DPHY_TX_CMN0_CMN_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-28 | RESERVED | R/W | X | |
| 27-20 | CMN0_O_ANA_PLL_BYTECLK_DIV | R/W | 8h | Byteclk divider value |
| 19-10 | CMN0_O_ANA_PLL_GM_PWM_DIV_LOW | R/W | 0h | Low division value setting for the gm PWM control divider |
| 9-0 | CMN0_O_ANA_PLL_GM_PWM_DIV_HIGH | R/W | 0h | High division value setting for the gm PWM control divider |

12.18 DPHY_TX_CMN0_CMN_DIG_TBIT11 Register (Offset = 44h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT11 is shown in [Figure 12-18](#) and described in [Table 12-38](#).

Return to [Summary Table](#).

CMN_DIG_TBIT11

Table 12-37. DPHY_TX_CMN0_CMN_DIG_TBIT11 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0044h |

Figure 12-18. DPHY_TX_CMN0_CMN_DIG_TBIT11 Register

| | | | | | | | |
|-----------------------|----------------------------------|---------------------------|-------------------------------------|------------------------------------|---------------------------------|----------------------------------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_ANA_PLL_CYA | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_ANA_PLL_CYA | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | CMN0_O_ANA_PLL_PFD_EN_1U_DEL_TM_SEL | CMN0_O_ANA_PLL_VRESET_VCO_BIAS_SEL | CMN0_O_ANA_PLL_VRESET_VCTRL_SEL | CMN0_O_ANA_PLL_SEL_FB_CLK_GM_PWM | CMN0_O_ANA_PLL_OP_BY2_BYPASS |
| R/W-X | | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_PLL_BYPASS | CMN0_O_ANA_PLL_FBDIV_CLKINBY2_EN | CMN0_O_ANA_PLL_DSM_CLK_EN | CMN0_O_ANA_PLL_GM_PWM_EN | CMN0_O_ANA_PLL_OP_DIV_CLK_EN | CMN0_O_ANA_PLL_IP_DIV_CLK_EN | CMN0_O_ANA_PLL_REF_CLK_EN | CMN0_O_ANA_PLL_FB_DIV_CLK_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-0h | R/W-1h | R/W-0h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-38. DPHY_TX_CMN0_CMN_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------------|------|-------|---|
| 31-16 | CMN0_O_ANA_PLL_CYA | R/W | 0h | Drives pllda_cya going to ANA |
| 15-13 | RESERVED | R/W | X | |
| 12 | CMN0_O_ANA_PLL_PFD_EN_1U_DEL_TM_SEL | R/W | 0h | Testmode signal for selecting 1us delayed for pll_pfd_reset_n |
| 11 | CMN0_O_ANA_PLL_VRESET_VCO_BIAS_SEL | R/W | 0h | vreset_vctrl_gmbyc is set inside the pll_vreset_gen |
| 10 | CMN0_O_ANA_PLL_VRESET_VCTRL_SEL | R/W | 0h | vreset_vctrl is set to ground inside the pll_vreset_gen |
| 9 | CMN0_O_ANA_PLL_SEL_FBCLK_GM_PWM | R/W | 0h | Enable mode to use feedback clock as the PWM control input for the gm stage |
| 8 | CMN0_O_ANA_PLL_OP_BY2_BYPASS | R/W | 0h | Mode to bypass the divide by 2 in the PLL output which generates clk_bit and clk_bitb |
| 7 | CMN0_O_ANA_PLL_BYPASS | R/W | 0h | Bypass PLL and pass refclk as output |
| 6 | CMN0_O_ANA_PLL_FBDIV_CLKINBY2_EN | R/W | 0h | Enable division by 2 on the feedback divider input clock |
| 5 | CMN0_O_ANA_PLL_DSM_CLK_EN | R/W | 0h | Enable for dsm clock output to digital |
| 4 | CMN0_O_ANA_PLL_GM_PWM_EN | R/W | 1h | Enable PWM control of the gm, else it will operate in the continuous mode |

Table 12-38. DPHY_TX_CMN0_CMN_DIG_TBIT11 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------------|------|-------|---|
| 3 | CMN0_O_ANA_PLL_OP_DIV_CLK_EN | R/W | 0h | Enable for op divider clock output to digital |
| 2 | CMN0_O_ANA_PLL_IP_DIV_CLK_EN | R/W | 1h | Enable for ip divider output to digital |
| 1 | CMN0_O_ANA_PLL_REF_CLK_EN | R/W | 0h | enables refclk to PLL |
| 0 | CMN0_O_ANA_PLL_FB_DIV_CLK_EN | R/W | 1h | Enable for feedback clock output to digital |

12.19 DPHY_TX_CMN0_CMN_DIG_TBIT12 Register (Offset = 48h) [reset = 0h]

DPHY_TX_CMN0_CMN_DIG_TBIT12 is shown in [Figure 12-19](#) and described in [Table 12-40](#).

Return to [Summary Table](#).

CMN_DIG_TBIT12

Table 12-39. DPHY_TX_CMN0_CMN_DIG_TBIT12 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0048h |

Figure 12-19. DPHY_TX_CMN0_CMN_DIG_TBIT12 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------------------|---|-------------------------------|-----------------------------------|---------------------------------------|---|-----------------------------------|---------------------------------------|
| CMN0_O_ANA_PLL_VRESET_GEN_EN_TM | CMN0_O_ANA_PLL_VRESET_GEN_EN_TM_SEL | CMN0_O_ANA_PLL_PFD_EN_TM | CMN0_O_ANA_PLL_PFD_EN_TM_SEL | CMN0_O_ANA_PLL_LOOP_FILTER_RESET_N_TM | CMN0_O_ANA_PLL_LOOP_FILTER_RESET_N_TM_SEL | CMN0_O_ANA_PLL_GM_RESET_N_TM | CMN0_O_ANA_PLL_GM_RESET_N_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_ANA_PLL_GMBYC_CAP_RESET_N_TM | CMN0_O_ANA_PLL_GMBYC_CAP_RESET_N_TM_SEL | CMN0_O_ANA_PLL_CP_RES_ET_N_TM | CMN0_O_ANA_PLL_CP_RES_ET_N_TM_SEL | CMN0_O_ANA_PLL_ACCINV_EN_TM | CMN0_O_ANA_PLL_ACCINV_EN_TM_SEL | CMN0_O_ANA_PLL_BIAS_EN_TM | CMN0_O_ANA_PLL_BIAS_EN_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_ANA_PLLDA_EN_DEL_TM | CMN0_O_ANA_PLLDA_EN_DEL_TM_SEL | CMN0_O_ANA_PLLDA_EN_TM | CMN0_O_ANA_PLLDA_EN_TM_SEL | CMN0_O_ANA_OP_BY2_DIV_RESET_N_TM | CMN0_O_ANA_OP_BY2_DIV_RESET_N_TM_SEL | CMN0_O_ANA_OP_DIV_RESET_N_TM | CMN0_O_ANA_OP_DIV_RESET_N_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_IP_DIV_RESET_N_TM | CMN0_O_ANA_IP_DIV_RESET_N_TM_SEL | CMN0_O_ANA_FB_DIV_RESET_N_TM | CMN0_O_ANA_FB_DIV_RESET_N_TM_SEL | CMN0_O_ANA_GM_PWM_DIV_RESET_N_TM | CMN0_O_ANA_GM_PWM_DIV_RESET_N_TM_SEL | CMN0_O_ANA_BYTECLK_DIV_RESET_N_TM | CMN0_O_ANA_BYTECLK_DIV_RESET_N_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-40. DPHY_TX_CMN0_CMN_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---|------|-------|---|
| 31 | CMN0_O_ANA_PLL_VRESET_GEN_EN_TM | R/W | 0h | Forced value of pll_vreset_gen_en = 1 |
| 30 | CMN0_O_ANA_PLL_VRESET_GEN_EN_TM_SEL | R/W | 0h | pll_vreset_gen_en forced from test registers |
| 29 | CMN0_O_ANA_PLL_PFD_EN_TM | R/W | 0h | Forced value of pllda_pfd_en = 1 |
| 28 | CMN0_O_ANA_PLL_PFD_EN_TM_SEL | R/W | 0h | pllda_pfd_en forced from test registers |
| 27 | CMN0_O_ANA_PLL_LOOP_FILTER_RESET_N_TM | R/W | 0h | Forced value of pll_loop_filter_reset_n = 1 |
| 26 | CMN0_O_ANA_PLL_LOOP_FILTER_RESET_N_TM_SEL | R/W | 0h | pll_loop_filter_reset_n is drivne from test registers |
| 25 | CMN0_O_ANA_PLL_GM_RESET_N_TM | R/W | 0h | Forced value of pll_gm_reset_n = 1 |

Table 12-40. DPHY_TX_CMN0_CMN_DIG_TBIT12 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--|------|-------|--|
| 24 | CMN0_O_ANA_PLL_GM_RESET_N_TM_SEL | R/W | 0h | pll_gm_reset_n is drivne from test registers |
| 23 | CMN0_O_ANA_PLL_GM_BYC_CAP_RESET_N_TM | R/W | 0h | Forced value of pll_gmbyc_cap_reset_n = 1 |
| 22 | CMN0_O_ANA_PLL_GM_BYC_CAP_RESET_N_TM_SEL | R/W | 0h | pll_gmbyc_cap_reset_n is drivne from test registers |
| 21 | CMN0_O_ANA_PLL_CP_RESET_N_TM | R/W | 0h | Forced value of pll_cp_reset_n = 1 |
| 20 | CMN0_O_ANA_PLL_CP_RESET_N_TM_SEL | R/W | 0h | pll_cp_reset_n is drivne from test registers |
| 19 | CMN0_O_ANA_PLL_ACC_INV_EN_TM | R/W | 0h | Forced value of pllda_accinv = 1 |
| 18 | CMN0_O_ANA_PLL_ACC_INV_EN_TM_SEL | R/W | 0h | pllda_accinv forced from test registers |
| 17 | CMN0_O_ANA_PLL_BIAS_EN_TM | R/W | 0h | Forced value of pllda_bias_en = 1 |
| 16 | CMN0_O_ANA_PLL_BIAS_EN_TM_SEL | R/W | 0h | pllda_bias_en forced from test registers |
| 15 | CMN0_O_ANA_PLLDA_EN_DEL_TM | R/W | 0h | Forced value of pllda_en_del = 1 |
| 14 | CMN0_O_ANA_PLLDA_EN_DEL_TM_SEL | R/W | 0h | pllda_en_del forced from test registers |
| 13 | CMN0_O_ANA_PLLDA_EN_TM | R/W | 0h | Forced value of pllda_en_del = 1 |
| 12 | CMN0_O_ANA_PLLDA_EN_TM_SEL | R/W | 0h | pllda_en_del forced from test registers |
| 11 | CMN0_O_ANA_OP_BY2_DIV_RESET_N_TM | R/W | 0h | Forced valu of pllda_op_by2_div_reset_n = 1 |
| 10 | CMN0_O_ANA_OP_BY2_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_op_by2_div_reset_n forced from test registers |
| 9 | CMN0_O_ANA_OP_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_op_div_reset_n = 1 |
| 8 | CMN0_O_ANA_OP_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_op_div_reset_n forced from test registers |
| 7 | CMN0_O_ANA_IP_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_ip_div_reset_n = 1 |
| 6 | CMN0_O_ANA_IP_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_ip_div_reset_n forced from test registers |
| 5 | CMN0_O_ANA_FB_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_fb_div_reset_n = 1 |
| 4 | CMN0_O_ANA_FB_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_fb_div_reset_n forced from test registers |
| 3 | CMN0_O_ANA_GM_PWM_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_gm_pwm_div_reset_n = 1 |
| 2 | CMN0_O_ANA_GM_PWM_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_gm_pwm_div_reset_n forced from test registers |
| 1 | CMN0_O_ANA_BYTECLK_DIV_RESET_N_TM | R/W | 0h | Forced value of pllda_byteclk_div_reset_n = 1 |
| 0 | CMN0_O_ANA_BYTECLK_DIV_RESET_N_TM_SEL | R/W | 0h | pllda_byteclk_div_reset_n forced from test registers |

12.20 DPHY_TX_CMN0_CMN_DIG_TBIT13 Register (Offset = 4Ch) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT13 is shown in [Figure 12-20](#) and described in [Table 12-42](#).

Return to [Summary Table](#).

CMN_DIG_TBIT13

Table 12-41. DPHY_TX_CMN0_CMN_DIG_TBIT13 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 004Ch |

Figure 12-20. DPHY_TX_CMN0_CMN_DIG_TBIT13 Register

| | | | | | | | |
|-------------------------------|----|----------------------------------|-------------------------------|----|-----------------------------------|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_ANA_PLL_FB_DIV_LOW_TM | | | | | | | |
| R/W-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_ANA_PLL_FB_DIV_LOW_TM | | CMN0_O_ANA_PLL_FB_DIV_LOW_TM_SEL | CMN0_O_ANA_PLL_FB_DIV_HIGH_TM | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_ANA_PLL_FB_DIV_HIGH_TM | | | | | CMN0_O_ANA_PLL_FB_DIV_HIGH_TM_SEL | RESERVED | |
| R/W-0h | | | | | R/W-0h | R/W-X | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-42. DPHY_TX_CMN0_CMN_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------------|------|-------|--|
| 31-22 | CMN0_O_ANA_PLL_FB_DIV_LOW_TM | R/W | 0h | forced value for pll_fb_div_clk_low |
| 21 | CMN0_O_ANA_PLL_FB_DIV_LOW_TM_SEL | R/W | 0h | pll_fb_div_clk_low forced from test registers |
| 20-11 | CMN0_O_ANA_PLL_FB_DIV_HIGH_TM | R/W | 0h | forced value for pll_fb_div_clk_high |
| 10 | CMN0_O_ANA_PLL_FB_DIV_HIGH_TM_SEL | R/W | 0h | pll_fb_div_clk_high forced from test registers |
| 9-0 | RESERVED | R/W | X | |

12.21 DPHY_TX_CMN0_CMN_DIG_TBIT14 Register (Offset = 50h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT14 is shown in [Figure 12-21](#) and described in [Table 12-44](#).

Return to [Summary Table](#).

CMN_DIG_TBIT14

**Table 12-43. DPHY_TX_CMN0_CMN_DIG_TBIT14
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0050h |

Figure 12-21. DPHY_TX_CMN0_CMN_DIG_TBIT14 Register

| | | | | | | | |
|--------------------------|------------------------------|--------------------------|--------------------------|----|----|----|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | CMN0_O_ANA_PLL_OP_DIV_TM | | | | |
| R/W-X | | | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_ANA_PLL_OP_DIV_TM | CMN0_O_ANA_PLL_OP_DIV_TM_SEL | CMN0_O_ANA_PLL_IP_DIV_TM | | | | | CMN0_O_ANA_PLL_IP_DIV_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-44. DPHY_TX_CMN0_CMN_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|-----------------------------------|
| 31-13 | RESERVED | R/W | X | |
| 12-7 | CMN0_O_ANA_PLL_OP_DIV_TM | R/W | 0h | forced value for op_div |
| 6 | CMN0_O_ANA_PLL_OP_DIV_TM_SEL | R/W | 0h | op_div forced from test registers |
| 5-1 | CMN0_O_ANA_PLL_IP_DIV_TM | R/W | 0h | forced value for ip_div |
| 0 | CMN0_O_ANA_PLL_IP_DIV_TM_SEL | R/W | 0h | ip_div forced from test registers |

12.22 DPHY_TX_CMN0_CMN_DIG_TBIT20 Register (Offset = 68h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT20 is shown in [Figure 12-22](#) and described in [Table 12-46](#).

Return to [Summary Table](#).

CMN_DIG_TBIT20

Table 12-45. DPHY_TX_CMN0_CMN_DIG_TBIT20 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0068h |

Figure 12-22. DPHY_TX_CMN0_CMN_DIG_TBIT20 Register

| | | | | | | | |
|--------------------------------|----|----|----|--------------------------------|----|------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | CMN0_O_CMSMT_REF_CLK_TMR_VALUE | | | |
| R/W-X | | | | R/W-14h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_CMSMT_REF_CLK_TMR_VALUE | | | | | | | |
| R/W-14h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_CMSMT_REF_CLK_TMR_VALUE | | | | CMN0_BF_3_1 | | CMN0_O_CMSMT_MEASUREMENT_RUN | |
| R/W-14h | | | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-46. DPHY_TX_CMN0_CMN_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19-4 | CMN0_O_CMSMT_REF_CLK_TMR_VALUE | R/W | 14h | Number of refclk cycles required for clock measurement |
| 3-1 | CMN0_BF_3_1 | R/W | 0h | test clock |
| 0 | CMN0_O_CMSMT_MEASUREMENT_RUN | R/W | 0h | Enables clock measurement |

12.23 DPHY_TX_CMN0_CMN_DIG_TBIT21 Register (Offset = 6Ch) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT21 is shown in [Figure 12-23](#) and described in [Table 12-48](#).

Return to [Summary Table](#).

CMN_DIG_TBIT21

**Table 12-47. DPHY_TX_CMN0_CMN_DIG_TBIT21
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 006Ch |

Figure 12-23. DPHY_TX_CMN0_CMN_DIG_TBIT21 Register

| | | | | | | | |
|----------|--|---|--------------------------------|------------------------------------|----------------------------|--------------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | CMN0_O_CMNDA_HSRX_BIST_CLK_SERSYNTH_SWAPDPDN | CMN0_O_CMNDA_HSRX_BIST_DATA_SERSYNTH_SWAPDPDN | CMN0_O_CMNDA_RX_BIST_EN_DEL_TM | CMN0_O_CMNDA_RX_BIST_EN_DEL_TM_SEL | CMN0_O_CMNDA_RX_BIST_EN_TM | CMN0_O_CMNDA_RX_BIST_EN_TM_SEL | CMN0_O_RX_DIG_BIST_EN |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-48. DPHY_TX_CMN0_CMN_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---|------|-------|---|
| 31-7 | RESERVED | R/W | X | |
| 6 | CMN0_O_CMNDA_HSRX_BIST_CLK_SERSYNTH_SWAPDPDN | R/W | 0h | Enables swapping DP-DN lines for clock bist |
| 5 | CMN0_O_CMNDA_HSRX_BIST_DATA_SERSYNTH_SWAPDPDN | R/W | 0h | Enables swapping DP-DN lines for data bist |
| 4 | CMN0_O_CMNDA_RX_BIST_EN_DEL_TM | R/W | 0h | forced value of cmnda_rx_bist_en_del = 1 |
| 3 | CMN0_O_CMNDA_RX_BIST_EN_DEL_TM_SEL | R/W | 0h | cmnda_rx_bist_en_del driven from test registers |
| 2 | CMN0_O_CMNDA_RX_BIST_EN_TM | R/W | 0h | forced value of cmnda_rx_bist_en = 1 |
| 1 | CMN0_O_CMNDA_RX_BIST_EN_TM_SEL | R/W | 0h | cmnda_rx_bist_en driven from test registers |
| 0 | CMN0_O_RX_DIG_BIST_EN | R/W | 0h | BIST enable for digital |

12.24 DPHY_TX_CMN0_CMN_DIG_TBIT22 Register (Offset = 70h) [reset = 694h]

DPHY_TX_CMN0_CMN_DIG_TBIT22 is shown in [Figure 12-24](#) and described in [Table 12-50](#).

Return to [Summary Table](#).

BIST_CONFIG_REG1

Table 12-49. DPHY_TX_CMN0_CMN_DIG_TBIT22 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0070h |

Figure 12-24. DPHY_TX_CMN0_CMN_DIG_TBIT22 Register

| | | | | | | | |
|-------------------------------|---------------------------|----------------------------|--------------------------------|--------|----|-------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_TM_SKEW_CAL_SYNC_PKT_SEL | CMN0_TM_SKEW_CAL_SYNC_PKT | | | | | | |
| R/W-0h | | | | R/W-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_TM_SKEW_CAL_SYNC_PKT | CMN0_TM_HS_SYNC_PKT_SEL | CMN0_TM_HS_SYNC_PKT | | | | | |
| R/W-0h | | R/W-0h | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_TM_HS_SYNC_PKT | | CMN0_BIST_LENGTH_OF_DESKEW | | | | | |
| R/W-0h | | | | R/W-Dh | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_BIST_LENGTH_OF_DESKEW | CMN0_BIST_SEND_CONFIG | | CMN0_BIST_MODE_ENTRY_WAIT_TIME | | | CMN0_BIST_CONTROLLER_EN | |
| R/W-Dh | | R/W-0h | | R/W-Ah | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-50. DPHY_TX_CMN0_CMN_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31 | CMN0_TM_SKEW_CAL_SYNC_PKT_SEL | R/W | 0h | To send 'FF as Skew calibration sync packet |
| 30-23 | CMN0_TM_SKEW_CAL_SYNC_PKT | R/W | 0h | desired skew calibration test sync packet |
| 22 | CMN0_TM_HS_SYNC_PKT_SEL | R/W | 0h | To send 'B8 as HS sync packet |
| 21-14 | CMN0_TM_HS_SYNC_PKT | R/W | 0h | desired HS test sync packet |
| 13-7 | CMN0_BIST_LENGTH_OF_DESKEW | R/W | Dh | Length of deskew sequence In terms of us. By default 13us of deskew sequence will be transmitted |
| 6-5 | CMN0_BIST_SEND_CONFIG | R/W | 0h | Option of configuring what to send in BIST mose. To send both deskew and HS data |
| 4-1 | CMN0_BIST_MODE_ENTRY_WAIT_TIME | R/W | Ah | Once after giving bist_en signal to pattern generator, after these many number of BYTE clcok cycles pattern generation will start |
| 0 | CMN0_BIST_CONTROLLER_EN | R/W | 0h | Enable BIST controller |

12.25 DPHY_TX_CMN0_CMN_DIG_TBIT23 Register (Offset = 74h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT23 is shown in [Figure 12-25](#) and described in [Table 12-52](#).

Return to [Summary Table](#).

BIST_CONFIG_REG2

**Table 12-51. DPHY_TX_CMN0_CMN_DIG_TBIT23
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0074h |

Figure 12-25. DPHY_TX_CMN0_CMN_DIG_TBIT23 Register

| | | | | | | | |
|--------------------------|----------------------------|------------------------|----|--------|----|--------|------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_TM_TX_DATA_HS_SEL | CMN0_TM_TX_DATA_HS | | | | | | |
| R/W-0h | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_TM_TX_DATA_HS | CMN0_BIST_TM_BAND_CTRL_SEL | CMN0_BIST_TM_BAND_CTRL | | | | | CMN0_TM_SKEW_CAL_PATTERN_SEL |
| R/W-0h | R/W-0h | R/W-0h | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_TM_SKEW_CAL_PATTERN | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-52. DPHY_TX_CMN0_CMN_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23 | CMN0_TM_TX_DATA_HS_SEL | R/W | 0h | sends single test byte to sersynth, which is in < 22:15> |
| 22-15 | CMN0_TM_TX_DATA_HS | R/W | 0h | Desired clock patetrn that can be sent using clk_sersynth |
| 14 | CMN0_BIST_TM_BAND_CTRL_SEL | R/W | 0h | To take the default band control settigns by the design |
| 13-9 | CMN0_BIST_TM_BAND_CTRL | R/W | 0h | Test mode band control setting to be done for BIST |
| 8 | CMN0_TM_SKEW_CAL_PATTERN_SEL | R/W | 0h | To send 'AA as skew calibration pattern |
| 7-0 | CMN0_TM_SKEW_CAL_PATTERN | R/W | 0h | desired skew calibration test sequence |

12.26 DPHY_TX_CMN0_CMN_DIG_TBIT24 Register (Offset = 78h) [reset = 0F0501B0h]

DPHY_TX_CMN0_CMN_DIG_TBIT24 is shown in [Figure 12-26](#) and described in [Table 12-54](#).

Return to [Summary Table](#).

BIST_CONFIG_REG3

Table 12-53. DPHY_TX_CMN0_CMN_DIG_TBIT24 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0078h |

Figure 12-26. DPHY_TX_CMN0_CMN_DIG_TBIT24 Register

| | | | | | | | |
|-------------------------|-------------------|----------------|----|---------------------|----|---------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_BIST_FRM_IDLE_TIME | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_BIST_PKT_NUM | | | | | | | |
| R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_BIST_INF_MODE | CMN0_BIST_FRM_NUM | | | | | | |
| R/W-0h | R/W-3h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_BIST_FRM_NUM | CMN0_BIST_CLEAR | CMN0_BIST_PRBS | | CMN0_BIST_TEST_MODE | | CMN0_UNUSED_0 | |
| R/W-3h | R/W-0h | R/W-3h | | R/W-0h | | R-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-54. DPHY_TX_CMN0_CMN_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|--|
| 31-24 | CMN0_BIST_FRM_IDLE_TIME | R/W | Fh | BIST_FRM_IDLE time is time between the frames |
| 23-16 | CMN0_BIST_PKT_NUM | R/W | 5h | BIST_PAK_NUM is number of packets that are to be transmitted per frame |
| 15 | CMN0_BIST_INF_MODE | R/W | 0h | run infinite BIST mode |
| 14-7 | CMN0_BIST_FRM_NUM | R/W | 3h | BIST_FRM_NUM is number of frames to be transmitted |
| 6 | CMN0_BIST_CLEAR | R/W | 0h | clear the bist |
| 5-4 | CMN0_BIST_PRBS | R/W | 3h | BIST PRBS MODE 9 |
| 3-1 | CMN0_BIST_TEST_MODE | R/W | 0h | PRBS mode |
| 0 | CMN0_UNUSED_0 | R | 0h | RESERVED |

12.27 DPHY_TX_CMN0_CMN_DIG_TBIT25 Register (Offset = 7Ch) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT25 is shown in [Figure 12-27](#) and described in [Table 12-56](#).

Return to [Summary Table](#).

BIST_CONFIG_REG4

**Table 12-55. DPHY_TX_CMN0_CMN_DIG_TBIT25
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 007Ch |

Figure 12-27. DPHY_TX_CMN0_CMN_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | CMN0_BIST_RUN_LENGTH | | | | | | | | | | | |
| R/W-X | | | | R/W-28h | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-56. DPHY_TX_CMN0_CMN_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|-----------------|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | CMN0_BIST_RUN_LENGTH | R/W | 28h | BIST_RUN_LENGTH |

12.28 DPHY_TX_CMN0_CMN_DIG_TBIT26 Register (Offset = 80h) [reset = Ah]

DPHY_TX_CMN0_CMN_DIG_TBIT26 is shown in [Figure 12-28](#) and described in [Table 12-58](#).

Return to [Summary Table](#).

BIST_CONFIG_REG5

Table 12-57. DPHY_TX_CMN0_CMN_DIG_TBIT26 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0080h |

Figure 12-28. DPHY_TX_CMN0_CMN_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|---------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_UNUSED_31_8 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_UNUSED_31_8 | | | | | | | | CMN0_BIST_IDLE_TIME | | | | | | | |
| R-0h | | | | | | | | R/W-Ah | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-58. DPHY_TX_CMN0_CMN_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|----------------|
| 31-8 | CMN0_UNUSED_31_8 | R | 0h | RESERVED |
| 7-0 | CMN0_BIST_IDLE_TIME | R/W | Ah | BIST_IDLE_TIME |

12.29 DPHY_TX_CMN0_CMN_DIG_TBIT27 Register (Offset = 84h) [reset = DECDBCABh]

DPHY_TX_CMN0_CMN_DIG_TBIT27 is shown in [Figure 12-29](#) and described in [Table 12-60](#).

Return to [Summary Table](#).

BIST_CONFIG_REG6

**Table 12-59. DPHY_TX_CMN0_CMN_DIG_TBIT27
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0084h |

Figure 12-29. DPHY_TX_CMN0_CMN_DIG_TBIT27 Register

| | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_BIST_PKT4 | | | | | | | | CMN0_BIST_PKT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_BIST_PKT2 | | | | | | | | CMN0_BIST_PKT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-60. DPHY_TX_CMN0_CMN_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|----------------|
| 31-24 | CMN0_BIST_PKT4 | R/W | DEh | BIST_TEST_PAT4 |
| 23-16 | CMN0_BIST_PKT3 | R/W | CDh | BIST_TEST_PAT3 |
| 15-8 | CMN0_BIST_PKT2 | R/W | BCh | BIST_TEST_PAT2 |
| 7-0 | CMN0_BIST_PKT1 | R/W | ABh | BIST_TEST_PAT1 |

12.30 DPHY_TX_CMN0_CMN_DIG_TBIT28 Register (Offset = 88h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT28 is shown in [Figure 12-30](#) and described in [Table 12-62](#).

Return to [Summary Table](#).

BIST_CONFIG_REG7

Table 12-61. DPHY_TX_CMN0_CMN_DIG_TBIT28 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0088h |

Figure 12-30. DPHY_TX_CMN0_CMN_DIG_TBIT28 Register

| | | | | | | | |
|------------------------------|------------------------------|------------------------------|------------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_BIST_TM_CLOCK_LP_DP_SEL | CMN0_BIST_TM_CLOCK_LP_DP_VAL | CMN0_BIST_TM_CLOCK_LP_DN_SEL | CMN0_BIST_TM_CLOCK_LP_DN_VAL | CMN0_BIST_TM_DATA_LP_DP_SEL | CMN0_BIST_TM_DATA_LP_DP_VAL | CMN0_BIST_TM_DATA_LP_DN_SEL | CMN0_BIST_TM_DATA_LP_DN_VAL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_UNUSED_INT | | CMN0_BIST_LFSR_FREEZE | CMN0_BIST_ERR_INJ_POINT | | | | |
| R-0h | | R/W-0h | R/W-14h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_BIST_ERR_INJ_POINT | | | | | | | CMN0_BIST_ERR_INJ_EN |
| R/W-14h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-62. DPHY_TX_CMN0_CMN_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23 | CMN0_BIST_TM_CLOCK_LP_DP_SEL | R/W | 0h | Test mode selection bit to force clock LP DP buffer to value from design |
| 22 | CMN0_BIST_TM_CLOCK_LP_DP_VAL | R/W | 0h | Test mode clock LP DP buffer value is 0 |
| 21 | CMN0_BIST_TM_CLOCK_LP_DN_SEL | R/W | 0h | Test mode selection bit to force clock LP DN buffer to value from design |
| 20 | CMN0_BIST_TM_CLOCK_LP_DN_VAL | R/W | 0h | Test mode clock LP DN buffer value is 0 |
| 19 | CMN0_BIST_TM_DATA_LP_DP_SEL | R/W | 0h | Test mode selection bit to force data LP DP buffer to value from design |
| 18 | CMN0_BIST_TM_DATA_LP_DP_VAL | R/W | 0h | Test mode data LP DP buffer value is 0 |
| 17 | CMN0_BIST_TM_DATA_LP_DN_SEL | R/W | 0h | Test mode selection bit to force data LP DN buffer to value from design |
| 16 | CMN0_BIST_TM_DATA_LP_DN_VAL | R/W | 0h | Test mode data LP DN buffer value is 0 |
| 15-14 | CMN0_UNUSED_INT | R | 0h | RESERVED |
| 13 | CMN0_BIST_LFSR_FREEZE | R/W | 0h | Reset LFSR contents after every packet or frame |

Table 12-62. DPHY_TX_CMN0_CMN_DIG_TBIT28 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-------------------------|------|-------|--|
| 12-1 | CMN0_BIST_ERR_INJ_POINT | R/W | 14h | BIST_ERR_INJECT_POINT is where to inject the error in the packet |
| 0 | CMN0_BIST_ERR_INJ_EN | R/W | 0h | Inject error in the BIST during the packet |

12.31 DPHY_TX_CMN0_CMN_DIG_TBIT31 Register (Offset = 94h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT31 is shown in [Figure 12-31](#) and described in [Table 12-64](#).

Return to [Summary Table](#).

CMN_DIG_TBIT31

Table 12-63. DPHY_TX_CMN0_CMN_DIG_TBIT31 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0094h |

Figure 12-31. DPHY_TX_CMN0_CMN_DIG_TBIT31 Register

| | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_RX_SSM_LDO_EN_REF_TMR | | | | | | | |
| R/W-4h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_RX_SSM_LDO_EN_DEL_TMR | | | | | | | |
| R/W-4h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RX_SSM_LDO_EN_TMR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-64. DPHY_TX_CMN0_CMN_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-16 | CMN0_O_RX_SSM_LDO_EN_REF_TMR | R/W | 4h | Wait time before enabling oscialltor calibration |
| 15-8 | CMN0_O_RX_SSM_LDO_EN_DEL_TMR | R/W | 4h | wait time before enabling ldo_en_ref |
| 7-0 | CMN0_O_RX_SSM_LDO_EN_TMR | R/W | 0h | Wait time between ldo_en and ldo_en_del |

12.32 DPHY_TX_CMN0_CMN_DIG_TBIT32 Register (Offset = 98h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT32 is shown in [Figure 12-32](#) and described in [Table 12-66](#).

Return to [Summary Table](#).

CMN_DIG_TBIT32

**Table 12-65. DPHY_TX_CMN0_CMN_DIG_TBIT32
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0098h |

Figure 12-32. DPHY_TX_CMN0_CMN_DIG_TBIT32 Register

| | | | | | | | |
|------------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_RX_SSM_ANA_BIST_ISO_DIS_TMR | | | | | | | |
| R/W-2h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RX_SSM_ANA_BIST_EN_DEL_TMR | | | | | | | |
| R/W-1h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-66. DPHY_TX_CMN0_CMN_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15-8 | CMN0_O_RX_SSM_ANA_BIST_ISO_DIS_TMR | R/W | 2h | Wait time between Bist_en_del and disabling isolation |
| 7-0 | CMN0_O_RX_SSM_ANA_BIST_EN_DEL_TMR | R/W | 1h | Wait time between Bist_en and bist_en_Del |

12.33 DPHY_TX_CMN0_CMN_DIG_TBIT33 Register (Offset = 9Ch) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT33 is shown in [Figure 12-33](#) and described in [Table 12-68](#).

Return to [Summary Table](#).

CMN_DIG_TBIT33

Table 12-67. DPHY_TX_CMN0_CMN_DIG_TBIT33 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 009Ch |

Figure 12-33. DPHY_TX_CMN0_CMN_DIG_TBIT33 Register

| | | | | | | | |
|--------------------------------------|----|--|--------------------------------------|----|----|--|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_O_RX_OSC_CAL_TIMER_SCALE_SEL | | | RESERVED | | | CMN0_O_RX_REFCLK_TIMER_ITER_VALUE_TM | |
| R/W-0h | | | R/W-X | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_RX_REFCLK_TIMER_ITER_VALUE_TM | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_RX_REFCLK_TIMER_ITER_VALUE_TM | | CMN0_O_RX_REFCLK_TIMER_ITER_VALUE_TM_SEL | CMN0_O_RX_REFCLK_TIMER_INIT_VALUE_TM | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RX_REFCLK_TIMER_INIT_VALUE_TM | | | | | | CMN0_O_RX_REFCLK_TIMER_INIT_VALUE_TM_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-68. DPHY_TX_CMN0_CMN_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-29 | CMN0_O_RX_OSC_CAL_TIMER_SCALE_SEL | R/W | 0h | Timer scale value for vco_count_window |
| 28-26 | RESERVED | R/W | X | |
| 25-14 | CMN0_O_RX_REFCLK_TIMER_ITER_VALUE_TM | R/W | 0h | Wait time required before enabling vco count window during iteration in test mode |
| 13 | CMN0_O_RX_REFCLK_TIMER_ITER_VALUE_TM_SEL | R/W | 0h | refclk_timer_iter value driven from test register |
| 12-1 | CMN0_O_RX_REFCLK_TIMER_INIT_VALUE_TM | R/W | 0h | Wait time required before enabling vco count window in initial phase in test mode |
| 0 | CMN0_O_RX_REFCLK_TIMER_INIT_VALUE_TM_SEL | R/W | 0h | refclk_timer_init value driven from test register |

12.34 DPHY_TX_CMN0_CMN_DIG_TBIT34 Register (Offset = A0h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT34 is shown in [Figure 12-34](#) and described in [Table 12-70](#).

Return to [Summary Table](#).

CMN_DIG_TBIT34

**Table 12-69. DPHY_TX_CMN0_CMN_DIG_TBIT34
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00A0h |

Figure 12-34. DPHY_TX_CMN0_CMN_DIG_TBIT34 Register

| | | | | | | | |
|---------------------------------------|----|---------------------------------------|---------------------------------------|----|----|---|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | CMN0_O_RX_OSC_EN_DEL_TMR_VALUE_TM | |
| R/W-X | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_O_RX_OSC_EN_DEL_TMR_VALUE_TM | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_RX_OSC_EN_DEL_TMR_VALUE_TM | | CMN0_O_RX_OSC_EN_DEL_TMR_VALUE_TM_SEL | CMN0_O_RX_REFCLK_TIMER_START_VALUE_TM | | | | |
| R/W-0h | | R/W-0h | R/W-0h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RX_REFCLK_TIMER_START_VALUE_TM | | | | | | CMN0_O_RX_REFCLK_TIMER_START_VALUE_TM_SEL | |
| R/W-0h | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-70. DPHY_TX_CMN0_CMN_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---|------|-------|---|
| 31-26 | RESERVED | R/W | X | |
| 25-14 | CMN0_O_RX_OSC_EN_DEL_TMR_VALUE_TM | R/W | 0h | Wait time between osc_en and osc_en_del in Test mode |
| 13 | CMN0_O_RX_OSC_EN_DEL_TMR_VALUE_TM_SEL | R/W | 0h | osc_en_del_tmr driven from test register |
| 12-1 | CMN0_O_RX_REFCLK_TIMER_START_VALUE_TM | R/W | 0h | No of refclk cycles required for single vco count window in test mode |
| 0 | CMN0_O_RX_REFCLK_TIMER_START_VALUE_TM_SEL | R/W | 0h | refclk_timer_start_value driven from test mode |

12.35 DPHY_TX_CMN0_CMN_DIG_TBIT35 Register (Offset = A4h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT35 is shown in [Figure 12-35](#) and described in [Table 12-72](#).

Return to [Summary Table](#).

CMN_DIG_TBIT35

Table 12-71. DPHY_TX_CMN0_CMN_DIG_TBIT35 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00A4h |

Figure 12-35. DPHY_TX_CMN0_CMN_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|--------------------------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | CMN0_O_RX_PLLCNT_COUNT_START_VALUE_2 | | | | | | | |
| R/W-X | | | | | | | | R/W-138h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RX_PLLCNT_COUNT_START_VALUE_2 | | | | CMN0_O_RX_PLLCNT_COUNT_START_VALUE_1 | | | | | | | | | | | |
| R/W-138h | | | | | | | | R/W-BBh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-72. DPHY_TX_CMN0_CMN_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-12 | CMN0_O_RX_PLLCNT_COUNT_START_VALUE_2 | R/W | 138h | No of PLL clock cycles expected in 2.5G mode |
| 11-0 | CMN0_O_RX_PLLCNT_COUNT_START_VALUE_1 | R/W | BBh | No of PLL clock cycles expected in 1.5G mode |

12.36 DPHY_TX_CMN0_CMN_DIG_TBIT36 Register (Offset = A8h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT36 is shown in [Figure 12-36](#) and described in [Table 12-74](#).

Return to [Summary Table](#).

CMN_DIG_TBIT36

**Table 12-73. DPHY_TX_CMN0_CMN_DIG_TBIT36
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00A8h |

Figure 12-36. DPHY_TX_CMN0_CMN_DIG_TBIT36 Register

| | | | | | | | |
|--------------------------------|----|----|----------------------------------|--------------------------------|----------------------------|-------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | CMN0_O_RX_TM_VCOCAL_OVRD_VALUE | | | |
| R/W-X | | | | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_O_RX_TM_VCOCAL_OVRD_VALUE | | | CMN0_O_RX_TM_VCO_CAL_OVERRIDE_EN | CMN0_O_RX_OSC_CAL_CODE_START | | | |
| R/W-0h | | | R/W-0h | R/W-77h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_RX_OSC_CAL_CODE_START | | | CMN0_O_RX_OSC_CAL_CODE_INIT_STEP | | CMN0_O_RX_TM_SEL_1P5G_MODE | CMN0_O_RX_TM_OSC_CAL_EN | |
| R/W-77h | | | R/W-2h | | R/W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-74. DPHY_TX_CMN0_CMN_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19-13 | CMN0_O_RX_TM_VCOCAL_OVRD_VALUE | R/W | 0h | Vco calcode Test mode value |
| 12 | CMN0_O_RX_TM_VCO_CAL_OVERRIDE_EN | R/W | 0h | Enables test mode overwrite for vco cal code |
| 11-5 | CMN0_O_RX_OSC_CAL_CODE_START | R/W | 77h | Starting code for vco calibration |
| 4-2 | CMN0_O_RX_OSC_CAL_CODE_INIT_STEP | R/W | 2h | Step size for incrmenting vco cal code |
| 1 | CMN0_O_RX_TM_SEL_1P5G_MODE | R/W | 0h | Select 1p5g mode oscillator clock |
| 0 | CMN0_O_RX_TM_OSC_CAL_EN | R/W | 0h | Test mode overwrite for crude osc calibration enable |

12.37 DPHY_TX_CMN0_CMN_DIG_TBIT37 Register (Offset = ACh) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT37 is shown in [Figure 12-37](#) and described in [Table 12-76](#).

Return to [Summary Table](#).

CMN_DIG_TBIT37

Table 12-75. DPHY_TX_CMN0_CMN_DIG_TBIT37 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00ACh |

Figure 12-37. DPHY_TX_CMN0_CMN_DIG_TBIT37 Register

| | | | | | | | |
|---------------------------------------|--|--|--|--|---|---|---------------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | CMN0_O_CMN DA_HSRX_OS C_CALIB_SEL_ TM | CMN0_O_CMN DA_HSRX_OS C_CALIB_SEL_ TM_SEL | CMN0_O_CMN DA_RX_OSC_ DIV_RESET_N_ TM | CMN0_O_CMN DA_RX_OSC_ DIV_RESET_N_ TM_SEL | CMN0_O_CMN DA_RX_OSC_ EN_DEL_TM | CMN0_O_CMN DA_RX_OSC_ EN_DEL_TM_S EL | CMN0_O_CMN DA_RX_OSC_ EN_TM |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_O_CMN DA_RX_OSC_ EN_TM_SEL | CMN0_O_CMN DA_RX_LDO_B YPASS_TM | CMN0_O_CMN DA_RX_LDO_R EF_EN_TM | CMN0_O_CMN DA_RX_LDO_R EF_EN_TM_SE L | CMN0_O_CMN DA_RX_LDO_E N_DEL_TM | CMN0_O_CMN DA_RX_LDO_E N_DEL_TM_SE L | CMN0_O_CMN DA_RX_LDO_E N_TM | CMN0_O_CMN DA_RX_LDO_E N_TM_SEL |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-76. DPHY_TX_CMN0_CMN_DIG_TBIT37 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | CMN0_O_CMNDA_HSRX_OSC_CALIB_SEL_TM | R/W | 0h | forced value of hsrx_osc_calib_sel = 1 |
| 13 | CMN0_O_CMNDA_HSRX_OSC_CALIB_SEL_TM_SEL | R/W | 0h | hsrx_osc_calib_sel driven from test registers |
| 12 | CMN0_O_CMNDA_RX_OSC_DIV_RESET_N_TM | R/W | 0h | forced value of rx_osc_div_reset_n = 1 |
| 11 | CMN0_O_CMNDA_RX_OSC_DIV_RESET_N_TM_SEL | R/W | 0h | rx_osc_div_reset_n driven from test registers |
| 10 | CMN0_O_CMNDA_RX_OSC_EN_DEL_TM | R/W | 0h | forced value of rx_osc_en_del = 1 |
| 9 | CMN0_O_CMNDA_RX_OSC_EN_DEL_TM_SEL | R/W | 0h | rx_osc_en_del driven from test registers |
| 8 | CMN0_O_CMNDA_RX_OSC_EN_TM | R/W | 0h | forced value of rx_osc_en = 1 |
| 7 | CMN0_O_CMNDA_RX_OSC_EN_TM_SEL | R/W | 0h | rx_osc_en driven from test registers |

Table 12-76. DPHY_TX_CMN0_CMN_DIG_TBIT37 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------------------------|------|-------|--|
| 6 | CMN0_O_CMNDA_RX_L DO_BYPASS_TM | R/W | 0h | Bypass LDO in test mode |
| 5 | CMN0_O_CMNDA_RX_L DO_REF_EN_TM | R/W | 0h | forced value of rx_ldo_ref_en = 1 |
| 4 | CMN0_O_CMNDA_RX_L DO_REF_EN_TM_SEL | R/W | 0h | rx_ldo_ref_en driven from test registers |
| 3 | CMN0_O_CMNDA_RX_L DO_EN_DEL_TM | R/W | 0h | forced value of rx_ldo_en_del = 1 |
| 2 | CMN0_O_CMNDA_RX_L DO_EN_DEL_TM_SEL | R/W | 0h | rx_ldo_en_del driven from test registers |
| 1 | CMN0_O_CMNDA_RX_L DO_EN_TM | R/W | 0h | forced value of rx_ldo_en = 1 |
| 0 | CMN0_O_CMNDA_RX_L DO_EN_TM_SEL | R/W | 0h | rx_ldo_en driven from test registers |

12.38 DPHY_TX_CMN0_CMN_DIG_TBIT39 Register (Offset = B4h) [reset = 0h]

DPHY_TX_CMN0_CMN_DIG_TBIT39 is shown in [Figure 12-38](#) and described in [Table 12-78](#).

Return to [Summary Table](#).

CMN_DIG_TBIT39

Table 12-77. DPHY_TX_CMN0_CMN_DIG_TBIT39 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00B4h |

Figure 12-38. DPHY_TX_CMN0_CMN_DIG_TBIT39 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_SPARE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-78. DPHY_TX_CMN0_CMN_DIG_TBIT39 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31-0 | CMN0_SPARE | R/W | 0h | spare |

12.39 DPHY_TX_CMN0_CMN_DIG_TBIT50 Register (Offset = D8h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT50 is shown in [Figure 12-39](#) and described in [Table 12-80](#).

Return to [Summary Table](#).

BIST_STATUS_REG1

**Table 12-79. DPHY_TX_CMN0_CMN_DIG_TBIT50
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00D8h |

Figure 12-39. DPHY_TX_CMN0_CMN_DIG_TBIT50 Register

| | | | | | | | |
|----------|----|----|----|----|----|-------------------------|----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CMN0_BIST_C COMPLETE | CMN0_BIST_E N_ACK |
| R-X | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-80. DPHY_TX_CMN0_CMN_DIG_TBIT50 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------------------|
| 31-2 | RESERVED | R | X | |
| 1 | CMN0_BIST_COMPLETE | R | 0h | BIST is completed |
| 0 | CMN0_BIST_EN_ACK | R | 0h | BIST Controller is enabled |

12.40 DPHY_TX_CMN0_CMN_DIG_TBIT53 Register (Offset = E4h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT53 is shown in [Figure 12-40](#) and described in [Table 12-82](#).

Return to [Summary Table](#).

CMN_DIG_TBIT53

Table 12-81. DPHY_TX_CMN0_CMN_DIG_TBIT53 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00E4h |

Figure 12-40. DPHY_TX_CMN0_CMN_DIG_TBIT53 Register

| | | | | | | | |
|---------------------------------|----|----|----|----|----|----|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | CMN0_I_CMS MT_TEST_CLK _CNT_VALUE |
| R-X | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_I_CMSMT_TEST_CLK_CNT_VALUE | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_I_CMSMT_TEST_CLK_CNT_VALUE | | | | | | | CMN0_I_CMS MT_MEASURE MENT_DONE |
| R-0h | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-82. DPHY_TX_CMN0_CMN_DIG_TBIT53 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-17 | RESERVED | R | X | |
| 16-1 | CMN0_I_CMSMT_TEST_CLK_CNT_VALUE | R | 0h | Gives clocks cycles count for test clock during measurement |
| 0 | CMN0_I_CMSMT_MEASUREMENT_DONE | R | 0h | Indicates clock measurement is done |

12.41 DPHY_TX_CMN0_CMN_DIG_TBIT54 Register (Offset = E8h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT54 is shown in [Figure 12-41](#) and described in [Table 12-84](#).

Return to [Summary Table](#).

CMN_DIG_TBIT54

**Table 12-83. DPHY_TX_CMN0_CMN_DIG_TBIT54
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00E8h |

Figure 12-41. DPHY_TX_CMN0_CMN_DIG_TBIT54 Register

| | | | | | | | |
|--------------------------|----|----|-------------------|-----------------------|-------------------|-------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMN0_I_CMN_PLL_SSM_STATE | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_I_CMN_PLL_SSM_STATE | | | | RESERVED | | | |
| R-0h | | | | R-X | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CMN0_I_DIG_PG_ACK | CMN0_I_PLL_NOT_LOCKED | CMN0_I_PLL_LOCKED | CMN0_I_ANA_RES_COMP_OUT | CMN0_I_CMN_TX_READY |
| R-X | | | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-84. DPHY_TX_CMN0_CMN_DIG_TBIT54 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-20 | CMN0_I_CMN_PLL_SSM_STATE | R | 0h | Gives CMN PLL ssm state |
| 19-5 | RESERVED | R | X | |
| 4 | CMN0_I_DIG_PG_ACK | R | 0h | PSM power good acknowledgement |
| 3 | CMN0_I_PLL_NOT_LOCKED | R | 0h | Indicates PLL is not locked before timeout |
| 2 | CMN0_I_PLL_LOCKED | R | 0h | Indicates PLL is locked |
| 1 | CMN0_I_ANA_RES_COMP_OUT | R | 0h | read value of comaprator output |
| 0 | CMN0_I_CMN_TX_READY | R | 0h | Indiacates cmn is ready for TX IP |

12.42 DPHY_TX_CMN0_CMN_DIG_TBIT56 Register (Offset = F0h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT56 is shown in [Figure 12-42](#) and described in [Table 12-86](#).

Return to [Summary Table](#).

CMN_DIG_TBIT56

Table 12-85. DPHY_TX_CMN0_CMN_DIG_TBIT56 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00F0h |

Figure 12-42. DPHY_TX_CMN0_CMN_DIG_TBIT56 Register

| | | | | | | | |
|-----------------------------|----|----|----|-----------------------------|-----------------------------|---------------------------|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | CMN0_I_CMNDA_RX_OSC_CALCODE | | | |
| R-X | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMN0_I_CMNDA_RX_OSC_CALCODE | | | | CMN0_I_CMN_RX_SSM_STATE | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMN0_I_CMN_RX_SSM_STATE | | | | | CMN0_I_RX_OSC_CAL_FSM_STATE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CMN0_I_RX_OSC_CAL_FSM_STATE | | | | | | CMN0_I_ANA_RES_COMP_OUT_X | CMN0_I_CMN_RX_READY |
| R-0h | | | | | | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-86. DPHY_TX_CMN0_CMN_DIG_TBIT56 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------------|------|-------|--|
| 31-28 | RESERVED | R | X | |
| 27-21 | CMN0_I_CMNDA_RX_OSC_CALCODE | R | 0h | Reads out calib code applied to oscillator |
| 20-11 | CMN0_I_CMN_RX_SSM_STATE | R | 0h | Gives CMN Rx ssm state |
| 10-2 | CMN0_I_RX_OSC_CAL_FSM_STATE | R | 0h | Gives Rx osc calib FSM state |
| 1 | CMN0_I_ANA_RES_COMP_OUT_X | R | 0h | read value of comparator output |
| 0 | CMN0_I_CMN_RX_READY | R | 0h | Indicates cmn is ready for RX IP |

12.43 DPHY_TX_CMN0_CMN_DIG_TBIT58 Register (Offset = F8h) [reset = X]

DPHY_TX_CMN0_CMN_DIG_TBIT58 is shown in [Figure 12-43](#) and described in [Table 12-88](#).

Return to [Summary Table](#).

CMN_DIG_TBIT58

**Table 12-87. DPHY_TX_CMN0_CMN_DIG_TBIT58
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 00F8h |

Figure 12-43. DPHY_TX_CMN0_CMN_DIG_TBIT58 Register

| | | | | | | | |
|----------|----|-----------------------|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CMN0_I_RES_CALIB_CODE | | | | | CMN0_I_RES_CALIB_DONE |
| R-X | | R-0h | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-88. DPHY_TX_CMN0_CMN_DIG_TBIT58 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-6 | RESERVED | R | X | |
| 5-1 | CMN0_I_RES_CALIB_CODE | R | 0h | Gives out calibrated resistor calibration code |
| 0 | CMN0_I_RES_CALIB_DONE | R | 0h | Indicates resistor calibration is done |

12.44 DPHY_TX_CLK0_TX_ANA_TBIT0 Register (Offset = 100h) [reset = 0h]

DPHY_TX_CLK0_TX_ANA_TBIT0 is shown in [Figure 12-44](#) and described in [Table 12-90](#).

Return to [Summary Table](#).

ANA_TBIT0

Table 12-89. DPHY_TX_CLK0_TX_ANA_TBIT0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0100h |

Figure 12-44. DPHY_TX_CLK0_TX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-90. DPHY_TX_CLK0_TX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CLK0_ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

12.45 DPHY_TX_CLK0_TX_ANA_TBIT1 Register (Offset = 104h) [reset = 0h]

DPHY_TX_CLK0_TX_ANA_TBIT1 is shown in [Figure 12-45](#) and described in [Table 12-92](#).

Return to [Summary Table](#).

ANA_TBIT1

**Table 12-91. DPHY_TX_CLK0_TX_ANA_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0104h |

Figure 12-45. DPHY_TX_CLK0_TX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-92. DPHY_TX_CLK0_TX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CLK0_ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

12.46 DPHY_TX_CLK0_TX_ANA_TBIT2 Register (Offset = 108h) [reset = 0h]

DPHY_TX_CLK0_TX_ANA_TBIT2 is shown in [Figure 12-46](#) and described in [Table 12-94](#).

Return to [Summary Table](#).

ANA_TBIT2

**Table 12-93. DPHY_TX_CLK0_TX_ANA_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0108h |

Figure 12-46. DPHY_TX_CLK0_TX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-94. DPHY_TX_CLK0_TX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CLK0_ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

12.47 DPHY_TX_CLK0_TX_ANA_TBIT3 Register (Offset = 10Ch) [reset = 0h]

DPHY_TX_CLK0_TX_ANA_TBIT3 is shown in [Figure 12-47](#) and described in [Table 12-96](#).

Return to [Summary Table](#).

ANA_TBIT3

**Table 12-95. DPHY_TX_CLK0_TX_ANA_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 010Ch |

Figure 12-47. DPHY_TX_CLK0_TX_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-96. DPHY_TX_CLK0_TX_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CLK0_ANA_TBIT3 | R/W | 0h | Analog Test register 3 |

12.48 DPHY_TX_CLK0_TX_ANA_TBIT4 Register (Offset = 110h) [reset = 0h]

DPHY_TX_CLK0_TX_ANA_TBIT4 is shown in [Figure 12-48](#) and described in [Table 12-98](#).

Return to [Summary Table](#).

ANA_TBIT4

**Table 12-97. DPHY_TX_CLK0_TX_ANA_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0110h |

Figure 12-48. DPHY_TX_CLK0_TX_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-98. DPHY_TX_CLK0_TX_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CLK0_ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

12.49 DPHY_TX_CLK0_TX_DIG_TBIT0 Register (Offset = 11Ch) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT0 is shown in [Figure 12-49](#) and described in [Table 12-100](#).

Return to [Summary Table](#).

ana_ctrl_counter_values

**Table 12-99. DPHY_TX_CLK0_TX_DIG_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 011Ch |

Figure 12-49. DPHY_TX_CLK0_TX_DIG_TBIT0 Register

| | | | | | | | |
|-----------------|----|----|----|----------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | CLK0_ULPS_PULLDN_CNT | | | |
| R/W-X | | | | R/W-6h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_UNUSED_7_5 | | | | CLK0_LDO_EN_CNT | | | |
| R-0h | | | | R/W-6h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-100. DPHY_TX_CLK0_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-13 | RESERVED | R/W | X | |
| 12-8 | CLK0_ULPS_PULLDN_CNT | R/W | 6h | After enabling LDO, ulps_pulldn will go to 0 after these many uS |
| 7-5 | CLK0_UNUSED_7_5 | R | 0h | RESERVED |
| 4-0 | CLK0_LDO_EN_CNT | R/W | 6h | Once the analog's power down signal is de asserted, LDO will be enabled after these many uS |

12.50 DPHY_TX_CLK0_TX_DIG_TBIT1 Register (Offset = 120h) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT1 is shown in [Figure 12-50](#) and described in [Table 12-102](#).

Return to [Summary Table](#).

unused

**Table 12-101. DPHY_TX_CLK0_TX_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0120h |

Figure 12-50. DPHY_TX_CLK0_TX_DIG_TBIT1 Register

| | | | | | | | |
|-----------------------|----|----|----|----------------------|----|-----------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | CLK0_HS_PRE P_HALF_CYC_ SEL | CLK0_HS_PRE P_HALF_CYC_ EN |
| R/W-X | | | | | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLK0_CLK_TRAIL_OFFSET | | | | CLK0_CLK_ZERO_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_CLK_PREP_OFFSET | | | | CLK0_TLPX_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-102. DPHY_TX_CLK0_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|---|
| 31-18 | RESERVED | R/W | X | |
| 17 | CLK0_HS_PREP_HALF_ CYC_SEL | R/W | 0h | HS Prepare extra half cycle offset is controlled by digital logic |
| 16 | CLK0_HS_PREP_HALF_ CYC_EN | R/W | 0h | If bit 17 == 1, Sets HS Prepare extra offset to 0 half cycle |
| 15-12 | CLK0_CLK_TRAIL_OFFS ET | R/W | 0h | Sets CLK-TRAIL Offset to 0 |
| 11-8 | CLK0_CLK_ZERO_OFFS ET | R/W | 0h | Sets CLK-ZERO offset to 0 |
| 7-4 | CLK0_CLK_PREP_OFFS ET | R/W | 0h | Sets CLK-PREPARE offset to 0 |
| 3-0 | CLK0_TLPX_OFFSET | R/W | 0h | Sets TLPX Offset to 0 |

12.51 DPHY_TX_CLK0_TX_DIG_TBIT2 Register (Offset = 124h) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT2 is shown in [Figure 12-51](#) and described in [Table 12-104](#).

Return to [Summary Table](#).

sersynth control signals

**Table 12-103. DPHY_TX_CLK0_TX_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0124h |

Figure 12-51. DPHY_TX_CLK0_TX_DIG_TBIT2 Register

| | | | | | | | |
|----------|----|--------------------------------|----------------------|----|----|-----------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CLK0_SERSYN TH_LOOPBAC K | CLK0_BAL_FORCE_STATE | | | CLK0_BAL_FO RCE_EN | RESERVED |
| R/W-X | | R/W-0h | R/W-0h | | | R/W-0h | R/W-X |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-104. DPHY_TX_CLK0_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | CLK0_SERSYNTH_LOOPBACK | R/W | 0h | De-serialiser will take input from sampler |
| 4-2 | CLK0_BAL_FORCE_STATE | R/W | 0h | Force the SYNC packet detection logic into below states if <1> is '1', SYNC_DONE state |
| 1 | CLK0_BAL_FORCE_EN | R/W | 0h | SYNC packet detection FSM in serialiser in BIST mode will work as per logic |
| 0 | RESERVED | R/W | X | |

12.52 DPHY_TX_CLK0_TX_DIG_TBIT8 Register (Offset = 13Ch) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT8 is shown in [Figure 12-52](#) and described in [Table 12-106](#).

Return to [Summary Table](#).

BIST configuration register 1

**Table 12-105. DPHY_TX_CLK0_TX_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 013Ch |

Figure 12-52. DPHY_TX_CLK0_TX_DIG_TBIT8 Register

| | | | | | | | |
|------------------------|----|----|----------------|----|----|------------------------|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | CLK0_WAIT_TIME | | | CLK0_ULPTX_TEST_TIME | |
| R/W-X | | | R/W-4h | | | R/W-40h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLK0_ULPTX_TEST_TIME | | | | | | CLK0_HS_CLK_CHECK_TIME | |
| R/W-40h | | | | | | R/W-64h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLK0_HS_CLK_CHECK_TIME | | | | | | | |
| R/W-64h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_HS_CLK_CHECK_TIME | | | | | | CLK0_LOOPBACK_MODE | CLK0_BIST_EN |
| R/W-64h | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-106. DPHY_TX_CLK0_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-30 | RESERVED | R/W | X | |
| 29-26 | CLK0_WAIT_TIME | R/W | 4h | Wait time between posedge run and negedge run of sampler clock |
| 25-18 | CLK0_ULPTX_TEST_TIME | R/W | 40h | While testing ULPTX, LP00 will be maintained on DPDN for this many number of byte clock cycles |
| 17-2 | CLK0_HS_CLK_CHECK_TIME | R/W | 64h | For how much time clock pattern will be checked for transitions. This value will be counted on byte clock |
| 1 | CLK0_LOOPBACK_MODE | R/W | 0h | Internal Loopback mode |
| 0 | CLK0_BIST_EN | R/W | 0h | BIST Disabled |

12.53 DPHY_TX_CLK0_TX_DIG_TBIT9 Register (Offset = 140h) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT9 is shown in [Figure 12-53](#) and described in [Table 12-108](#).

Return to [Summary Table](#).

BIST configuration register 2

**Table 12-107. DPHY_TX_CLK0_TX_DIG_TBIT9
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0140h |

Figure 12-53. DPHY_TX_CLK0_TX_DIG_TBIT9 Register

| | | | | | | | |
|-----------------|----|----|------------------------------|----|-------------------------------|-----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | CLK0_BIST_DIG_TO_DIG_LOOPBACK | CLK0_UNUSED_9_5 | |
| R/W-X | | | | | R/W-0h | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_UNUSED_9_5 | | | CLK0_HS_CLK_CHECK_EXTRA_TIME | | | | |
| R-0h | | | R/W-Ah | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-108. DPHY_TX_CLK0_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-11 | RESERVED | R/W | X | |
| 10 | CLK0_BIST_DIG_TO_DIG_LOOPBACK | R/W | 0h | main digital to pattern checker loopback enabled |
| 9-5 | CLK0_UNUSED_9_5 | R | 0h | RESERVED |
| 4-0 | CLK0_HS_CLK_CHECK_EXTRA_TIME | R/W | Ah | After the clock has been transmitted for programmed number of byte clock cycles, if we need clock to be sent for some more time, set this value as per requirement |

12.54 DPHY_TX_CLK0_TX_DIG_TBIT10 Register (Offset = 144h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT10 is shown in [Figure 12-54](#) and described in [Table 12-110](#).

Return to [Summary Table](#).

spare

Table 12-109. DPHY_TX_CLK0_TX_DIG_TBIT10 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0144h |

Figure 12-54. DPHY_TX_CLK0_TX_DIG_TBIT10 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_SPARE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-110. DPHY_TX_CLK0_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31-0 | CLK0_SPARE | R/W | 0h | spare |

12.55 DPHY_TX_CLK0_TX_DIG_TBIT14 Register (Offset = 154h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT14 is shown in [Figure 12-55](#) and described in [Table 12-112](#).

Return to [Summary Table](#).

digital to analog signals test muxing

**Table 12-111. DPHY_TX_CLK0_TX_DIG_TBIT14
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0154h |

Figure 12-55. DPHY_TX_CLK0_TX_DIG_TBIT14 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------|-------------------------|------------------------|--------------------|---------------------------------|-----------------------------|------------------------|-------------------|
| CLK0_TM_ISO_EN | CLK0_TM_LOAD_DPDN_SEL | CLK0_TM_LOAD_DPDN | | | CLK0_TM_HSTX_DATA_RATE_SEL | CLK0_TM_HSTX_DATA_RATE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLK0_TM_BIST_ULP_RCV_EN_SEL | CLK0_TM_BIST_ULP_RCV_EN | CLK0_TM_ULPS_PULDN_SEL | CLK0_TM_ULPS_PULDN | CLK0_TM_BIST_SMPLR_CLK_EDGE_SEL | CLK0_TM_BIST_SMPLR_CLK_EDGE | CLK0_TM_BIST_EN_SEL | CLK0_TM_BIST_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLK0_TM_LPTX_TRST_SEL | CLK0_TM_LPTX_TRST | CLK0_TM_LPTX_RST_SEL | CLK0_TM_LPTX_RST | CLK0_TM_LPTX_DP_SEL | CLK0_TM_LPTX_DP | CLK0_TM_LPTX_DN_SEL | CLK0_TM_LPTX_DN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_TM_LDO_REF_EN_SEL | CLK0_TM_LDO_REF_EN | CLK0_TM_HSTX_TRST_SEL | CLK0_TM_HSTX_TRST | CLK0_TM_HSTX_RQST_SEL | CLK0_TM_HSTX_RQST | CLK0_TM_GLOBAL_PD_SEL | CLK0_TM_GLOBAL_PD |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-112. DPHY_TX_CLK0_TX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31 | CLK0_TM_ISO_EN | R/W | 0h | Enable isolation in test mode |
| 30 | CLK0_TM_LOAD_DPDN_SEL | R/W | 0h | Take ana_dpdn_load from dig logic |
| 29-27 | CLK0_TM_LOAD_DPDN | R/W | 0h | set ana_dpdn_load as per requirement in test mode |
| 26 | CLK0_TM_HSTX_DATA_RATE_SEL | R/W | 0h | Take ana_hstx_datarate from dig logic |
| 25-24 | CLK0_TM_HSTX_DATA_RATE | R/W | 0h | set ana_hstx_datarate as per requirement in test mode |
| 23 | CLK0_TM_BIST_ULP_RCV_EN_SEL | R/W | 0h | Take ana_bist_ulps_rcv_en from dig logic |
| 22 | CLK0_TM_BIST_ULP_RCV_EN | R/W | 0h | set ana_bist_ulps_rcv_en to 0 |
| 21 | CLK0_TM_ULPS_PULDN_SEL | R/W | 0h | Take ana_ulps_puldn from dig logic |
| 20 | CLK0_TM_ULPS_PULDN | R/W | 0h | set ana_ulps_puldn to 0 |
| 19 | CLK0_TM_BIST_SMPLR_CLK_EDGE_SEL | R/W | 0h | Take ana_bist_smplr_clkedge from dig logic |
| 18 | CLK0_TM_BIST_SMPLR_CLK_EDGE | R/W | 0h | set ana_bist_smplr_clkedge to posedge |

Table 12-112. DPHY_TX_CLK0_TX_DIG_TBIT14 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------------|------|-------|--|
| 17 | CLK0_TM_BIST_EN_SEL | R/W | 0h | Take ana_bist_en from dig logic |
| 16 | CLK0_TM_BIST_EN | R/W | 0h | set ana_bist_en to 0 |
| 15 | CLK0_TM_LPTX_TRST_SEL | R/W | 0h | Take ana_lptx_trst from dig logic |
| 14 | CLK0_TM_LPTX_TRST | R/W | 0h | set ana_lptx_trst to 0 |
| 13 | CLK0_TM_LPTX_RST_SEL | R/W | 0h | Take ana_lptx_rst from dig logic |
| 12 | CLK0_TM_LPTX_RST | R/W | 0h | set ana_lptx_rst to 0 |
| 11 | CLK0_TM_LPTX_DP_SEL | R/W | 0h | give output for LPTX DP from dig logic |
| 10 | CLK0_TM_LPTX_DP | R/W | 0h | send 0 to LP TX Dp |
| 9 | CLK0_TM_LPTX_DN_SEL | R/W | 0h | give output for LPTX DN from dig logic |
| 8 | CLK0_TM_LPTX_DN | R/W | 0h | send 0 to LP TX Dn |
| 7 | CLK0_TM_LDO_REF_EN_SEL | R/W | 0h | Take ana_ldo_ref_en from dig logic |
| 6 | CLK0_TM_LDO_REF_EN | R/W | 0h | set ana_ldo_ref_en to 0 |
| 5 | CLK0_TM_HSTX_TRST_SEL | R/W | 0h | Take ana_hstx_trst from dig logic |
| 4 | CLK0_TM_HSTX_TRST | R/W | 0h | set ana_hstx_trst to 0 |
| 3 | CLK0_TM_HSTX_RQST_SEL | R/W | 0h | Take ana_hstx_rqst from dig logic |
| 2 | CLK0_TM_HSTX_RQST | R/W | 0h | set ana_hstx_rqst to 0 |
| 1 | CLK0_TM_GLOBAL_PD_SEL | R/W | 0h | Take ana_global_pd from dig logic |
| 0 | CLK0_TM_GLOBAL_PD | R/W | 0h | set ana_global_pd to 0 (powered up) |

12.56 DPHY_TX_CLK0_TX_DIG_TBIT15 Register (Offset = 158h) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT15 is shown in [Figure 12-56](#) and described in [Table 12-114](#).

Return to [Summary Table](#).

digital to analog signals test muxing

**Table 12-113. DPHY_TX_CLK0_TX_DIG_TBIT15
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0158h |

Figure 12-56. DPHY_TX_CLK0_TX_DIG_TBIT15 Register

| | | | | | | | |
|--------------------|------------------------------------|----------------------------|---------------------------|--------------------------|---------------------------------|-------------------------|---------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | CLK0_TM_SER SYNTH_RST_N _SEL | CLK0_TM_SER SYNTH_RST_N | CLK0_TM_SW AP_DPDN_SEL | CLK0_TM_SW AP_DPDN_EN | CLK0_TM_SER SYNTH_EN_SE L | CLK0_TM_SER SYNTH_EN | CLK0_TM_TX DATA_HS_SEL |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_TM_TX_DATA_HS | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-114. DPHY_TX_CLK0_TX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | CLK0_TM_SERSYNTH_R ST_N_SEL | R/W | 0h | Take sersynth_rst_n from dig logic |
| 13 | CLK0_TM_SERSYNTH_R ST_N | R/W | 0h | Set sersynth_rst_n to 1 |
| 12 | CLK0_TM_SWAP_DPDN_ SEL | R/W | 0h | Take swapdp_dn from dig logic |
| 11 | CLK0_TM_SWAP_DPDN_ EN | R/W | 0h | Set swap_dpdn to 1 |
| 10 | CLK0_TM_SERSYNTH_E N_SEL | R/W | 0h | Take sersynth_en from dig logic |
| 9 | CLK0_TM_SERSYNTH_E N | R/W | 0h | set sersynth_en to 1 |
| 8 | CLK0_TM_TX_DATA_HS_ SEL | R/W | 0h | sends single test byte to sersynth, which is in <7:0> |
| 7-0 | CLK0_TM_TX_DATA_HS | R/W | 0h | Test byte that can be sent constantly to sersynth. This is validated by bit <8> of this reg |

12.57 DPHY_TX_CLK0_TX_DIG_TBIT16 Register (Offset = 15Ch) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT16 is shown in [Figure 12-57](#) and described in [Table 12-116](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT16

Table 12-115. DPHY_TX_CLK0_TX_DIG_TBIT16 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 015Ch |

Figure 12-57. DPHY_TX_CLK0_TX_DIG_TBIT16 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-116. DPHY_TX_CLK0_TX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT16 | R | 0h | RESERVED |

12.58 DPHY_TX_CLK0_TX_DIG_TBIT17 Register (Offset = 160h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT17 is shown in [Figure 12-58](#) and described in [Table 12-118](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT17

**Table 12-117. DPHY_TX_CLK0_TX_DIG_TBIT17
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0160h |

Figure 12-58. DPHY_TX_CLK0_TX_DIG_TBIT17 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-118. DPHY_TX_CLK0_TX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT17 | R | 0h | RESERVED |

12.59 DPHY_TX_CLK0_TX_DIG_TBIT18 Register (Offset = 164h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT18 is shown in [Figure 12-59](#) and described in [Table 12-120](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT18

Table 12-119. DPHY_TX_CLK0_TX_DIG_TBIT18 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0164h |

Figure 12-59. DPHY_TX_CLK0_TX_DIG_TBIT18 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-120. DPHY_TX_CLK0_TX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT18 | R | 0h | RESERVED |

12.60 DPHY_TX_CLK0_TX_DIG_TBIT19 Register (Offset = 168h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT19 is shown in [Figure 12-60](#) and described in [Table 12-122](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT19

**Table 12-121. DPHY_TX_CLK0_TX_DIG_TBIT19
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0168h |

Figure 12-60. DPHY_TX_CLK0_TX_DIG_TBIT19 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-122. DPHY_TX_CLK0_TX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT19 | R | 0h | RESERVED |

12.61 DPHY_TX_CLK0_TX_DIG_TBIT20 Register (Offset = 16Ch) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT20 is shown in [Figure 12-61](#) and described in [Table 12-124](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT20

Table 12-123. DPHY_TX_CLK0_TX_DIG_TBIT20 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 016Ch |

Figure 12-61. DPHY_TX_CLK0_TX_DIG_TBIT20 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT20 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-124. DPHY_TX_CLK0_TX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT20 | R | 0h | RESERVED |

12.62 DPHY_TX_CLK0_TX_ANA_TBIT5 Register (Offset = 170h) [reset = 0h]

DPHY_TX_CLK0_TX_ANA_TBIT5 is shown in [Figure 12-62](#) and described in [Table 12-126](#).

Return to [Summary Table](#).

additional analog test registers

**Table 12-125. DPHY_TX_CLK0_TX_ANA_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0170h |

Figure 12-62. DPHY_TX_CLK0_TX_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_ANA_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-126. DPHY_TX_CLK0_TX_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|------------------------|
| 31-0 | CLK0_ANA_TBIT5 | R | 0h | Analog Test register 5 |

12.63 DPHY_TX_CLK0_TX_DIG_TBIT21 Register (Offset = 17Ch) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT21 is shown in [Figure 12-63](#) and described in [Table 12-128](#).

Return to [Summary Table](#).

bal and ana_ctrl [DPHY_TX_STATUS](#)

Table 12-127. DPHY_TX_CLK0_TX_DIG_TBIT21 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 017Ch |

Figure 12-63. DPHY_TX_CLK0_TX_DIG_TBIT21 Register

| | | | | | | | |
|----------------------|----|----|----|-------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | CLK0_ANA_CTRL_FSM_STATE | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLK0_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-128. DPHY_TX_CLK0_TX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|------|-------|---|
| 31-21 | RESERVED | R | X | |
| 20-16 | CLK0_ANA_CTRL_FSM_STATE | R | 0h | FSM state readout for ana_ctrl |
| 15-0 | CLK0_BIST_BAL_STATUS | R | 0h | BAL logic DPHY_TX_STATUS read |

12.64 DPHY_TX_CLK0_TX_DIG_TBIT22 Register (Offset = 180h) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT22 is shown in [Figure 12-64](#) and described in [Table 12-130](#).

Return to [Summary Table](#).

all FSM states in the design1

**Table 12-129. DPHY_TX_CLK0_TX_DIG_TBIT22
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0180h |

Figure 12-64. DPHY_TX_CLK0_TX_DIG_TBIT22 Register

| | | | | | | | | | | | | | | | |
|-----------------------|----|----|----|----|----------------------|----|----|----|----|-----------------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | CLK0_TM_ESC_FSM_STATE | | | | | |
| R-X | | | | | | | | | | R-0h | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_TM_ESC_FSM_STATE | | | | | CLK0_TM_HS_FSM_STATE | | | | | | | | | | |
| R-0h | | | | | R-0h | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-130. DPHY_TX_CLK0_TX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|------|-------|-----------------------------------|
| 31-22 | RESERVED | R | X | |
| 21-12 | CLK0_TM_ESC_FSM_STATE | R | 0h | FSM state readout for escape path |
| 11-0 | CLK0_TM_HS_FSM_STATE | R | 0h | FSM state readout for hs path |

12.65 DPHY_TX_CLK0_TX_DIG_TBIT24 Register (Offset = 188h) [reset = X]

DPHY_TX_CLK0_TX_DIG_TBIT24 is shown in [Figure 12-65](#) and described in [Table 12-132](#).

Return to [Summary Table](#).

BIST Status register

Table 12-131. DPHY_TX_CLK0_TX_DIG_TBIT24 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0188h |

Figure 12-65. DPHY_TX_CLK0_TX_DIG_TBIT24 Register

| | | | | | | | |
|----------------------|--------------------------|----------------------|-------------------------|----------------------|----------------------|----------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | CLK0_BIST_UL_P_DP | CLK0_BIST_UL_P_DN |
| R-X | | | | | | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLK0_BAL_FAIL | CLK0_ULPTX_CHE_FSM_STATE | | CLK0_LPTX_CHE_FSM_STATE | | | CLK0_CTRLR_FSM_STATE | |
| R-0h | R-0h | | R-0h | | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_CTRLR_FSM_STATE | CLK0_BIST_PASS | CLK0_ULPTX_BIST_PASS | CLK0_LPTX_BIST_PASS | CLK0_HS_BIST_ERR_POS | CLK0_HS_BIST_ERR_NEG | CLK0_BIST_CMPLT | CLK0_BIST_ENABLED |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-132. DPHY_TX_CLK0_TX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|--|
| 31-18 | RESERVED | R | X | |
| 17 | CLK0_BIST_ULP_DP | R | 0h | Status of BIST ULPRX DP |
| 16 | CLK0_BIST_ULP_DN | R | 0h | Status of BIST ULPRX DN |
| 15 | CLK0_BAL_FAIL | R | 0h | byte alignment logic failed to give valid signal |
| 14-13 | CLK0_ULPTX_CHE_FSM_STATE | R | 0h | FSM state in which ULPTX checker is in |
| 12-10 | CLK0_LPTX_CHE_FSM_STATE | R | 0h | FSM state in which LPTX checker is in |
| 9-7 | CLK0_CTRLR_FSM_STATE | R | 0h | FSM state in which controller is currently |
| 6 | CLK0_BIST_PASS | R | 0h | Clock lane has passed BIST completely |
| 5 | CLK0_ULPTX_BIST_PASS | R | 0h | ULPTX Bist passed |
| 4 | CLK0_LPTX_BIST_PASS | R | 0h | LPTX Bist passed |
| 3 | CLK0_HS_BIST_ERR_POS | R | 0h | HS Bist error detected with posedge of sampler clock |
| 2 | CLK0_HS_BIST_ERR_NEG | R | 0h | HS Bist error detected with negedge of sampler clock |
| 1 | CLK0_BIST_CMPLT | R | 0h | BIST is completed |
| 0 | CLK0_BIST_ENABLED | R | 0h | BIST controller is enabled |

12.66 DPHY_TX_CLK0_TX_DIG_TBIT25 Register (Offset = 18Ch) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT25 is shown in [Figure 12-66](#) and described in [Table 12-134](#).

Return to [Summary Table](#).

additional digital read only registers

**Table 12-133. DPHY_TX_CLK0_TX_DIG_TBIT25
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 018Ch |

Figure 12-66. DPHY_TX_CLK0_TX_DIG_TBIT25 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-134. DPHY_TX_CLK0_TX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT25 | R | 0h | RESERVED |

12.67 DPHY_TX_CLK0_TX_DIG_TBIT26 Register (Offset = 190h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT26 is shown in [Figure 12-67](#) and described in [Table 12-136](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT26

Table 12-135. DPHY_TX_CLK0_TX_DIG_TBIT26 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0190h |

Figure 12-67. DPHY_TX_CLK0_TX_DIG_TBIT26 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT26 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-136. DPHY_TX_CLK0_TX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT26 | R | 0h | RESERVED |

12.68 DPHY_TX_CLK0_TX_DIG_TBIT27 Register (Offset = 194h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT27 is shown in [Figure 12-68](#) and described in [Table 12-138](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT27

**Table 12-137. DPHY_TX_CLK0_TX_DIG_TBIT27
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0194h |

Figure 12-68. DPHY_TX_CLK0_TX_DIG_TBIT27 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT27 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-138. DPHY_TX_CLK0_TX_DIG_TBIT27 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT27 | R | 0h | RESERVED |

12.69 DPHY_TX_CLK0_TX_DIG_TBIT28 Register (Offset = 198h) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT28 is shown in [Figure 12-69](#) and described in [Table 12-140](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT28

Table 12-139. DPHY_TX_CLK0_TX_DIG_TBIT28 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0198h |

Figure 12-69. DPHY_TX_CLK0_TX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-140. DPHY_TX_CLK0_TX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT28 | R | 0h | RESERVED |

12.70 DPHY_TX_CLK0_TX_DIG_TBIT29 Register (Offset = 19Ch) [reset = 0h]

DPHY_TX_CLK0_TX_DIG_TBIT29 is shown in [Figure 12-70](#) and described in [Table 12-142](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT29

**Table 12-141. DPHY_TX_CLK0_TX_DIG_TBIT29
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 019Ch |

Figure 12-70. DPHY_TX_CLK0_TX_DIG_TBIT29 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CLK0_DIG_TBIT29 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-142. DPHY_TX_CLK0_TX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31-0 | CLK0_DIG_TBIT29 | R | 0h | RESERVED |

12.71 DPHY_TX_DL0_TX_ANA_TBIT0 Register (Offset = 200h) [reset = 0h]

DPHY_TX_DL0_TX_ANA_TBIT0 is shown in [Figure 12-71](#) and described in [Table 12-144](#).

Return to [Summary Table](#).

TX_ANA_TBIT0

**Table 12-143. DPHY_TX_DL0_TX_ANA_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0200h |

Figure 12-71. DPHY_TX_DL0_TX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-144. DPHY_TX_DL0_TX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL0_ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

12.72 DPHY_TX_DL0_TX_ANA_TBIT1 Register (Offset = 204h) [reset = 0h]

DPHY_TX_DL0_TX_ANA_TBIT1 is shown in [Figure 12-72](#) and described in [Table 12-146](#).

Return to [Summary Table](#).

TX_ANA_TBIT1

**Table 12-145. DPHY_TX_DL0_TX_ANA_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0204h |

Figure 12-72. DPHY_TX_DL0_TX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-146. DPHY_TX_DL0_TX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL0_ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

12.73 DPHY_TX_DL0_TX_ANA_TBIT2 Register (Offset = 208h) [reset = 0h]

DPHY_TX_DL0_TX_ANA_TBIT2 is shown in [Figure 12-73](#) and described in [Table 12-148](#).

Return to [Summary Table](#).

TX_ANA_TBIT2

**Table 12-147. DPHY_TX_DL0_TX_ANA_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0208h |

Figure 12-73. DPHY_TX_DL0_TX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-148. DPHY_TX_DL0_TX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL0_ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

12.74 DPHY_TX_DL0_TX_ANA_TBIT3 Register (Offset = 20Ch) [reset = 0h]

DPHY_TX_DL0_TX_ANA_TBIT3 is shown in [Figure 12-74](#) and described in [Table 12-150](#).

Return to [Summary Table](#).

TX_ANA_TBIT3

**Table 12-149. DPHY_TX_DL0_TX_ANA_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 020Ch |

Figure 12-74. DPHY_TX_DL0_TX_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-150. DPHY_TX_DL0_TX_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL0_ANA_TBIT3 | R/W | 0h | Analog Test register 3 |

12.75 DPHY_TX_DL0_TX_ANA_TBIT4 Register (Offset = 210h) [reset = 0h]

DPHY_TX_DL0_TX_ANA_TBIT4 is shown in [Figure 12-75](#) and described in [Table 12-152](#).

Return to [Summary Table](#).

TX_ANA_TBIT4

Table 12-151. DPHY_TX_DL0_TX_ANA_TBIT4 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0210h |

Figure 12-75. DPHY_TX_DL0_TX_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-152. DPHY_TX_DL0_TX_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL0_ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

12.76 DPHY_TX_DL0_TX_DIG_TBIT0 Register (Offset = 21Ch) [reset = 606h]

DPHY_TX_DL0_TX_DIG_TBIT0 is shown in [Figure 12-76](#) and described in [Table 12-154](#).

Return to [Summary Table](#).

ana_ctrl_counter_values

**Table 12-153. DPHY_TX_DL0_TX_DIG_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 021Ch |

Figure 12-76. DPHY_TX_DL0_TX_DIG_TBIT0 Register

| | | | | | | | |
|------------------|----|----|----|---------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL0_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_UNUSED_31_13 | | | | DL0_ULPS_PULLDN_CNT | | | |
| R-0h | | | | R/W-6h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_UNUSED_7_5 | | | | DL0_LDO_EN_CNT | | | |
| R-0h | | | | R/W-6h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-154. DPHY_TX_DL0_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-13 | DL0_UNUSED_31_13 | R | 0h | RESERVED |
| 12-8 | DL0_ULPS_PULLDN_CNT | R/W | 6h | After enabling LDO, ulps_pulldn will go to 0 after these many uS |
| 7-5 | DL0_UNUSED_7_5 | R | 0h | RESERVED |
| 4-0 | DL0_LDO_EN_CNT | R/W | 6h | Once the analog's power down signal is de asserted, LDO will be enabled after these many uS |

12.77 DPHY_TX_DL0_TX_DIG_TBIT1 Register (Offset = 220h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT1 is shown in [Figure 12-77](#) and described in [Table 12-156](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT1

**Table 12-155. DPHY_TX_DL0_TX_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0220h |

Figure 12-77. DPHY_TX_DL0_TX_DIG_TBIT1 Register

| | | | | | | | |
|---------------------|----|----------------------|----------------------|----------------------|---------------------------|--|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | DL0_TEST_LP TX_DP | DL0_TEST_LP TX_DN | DL0_TEST_LP TX_EN | DL0_TM_READ Y_SKEW_CAL | DL0_TM_HS_P REP_HAFCYC _OVERRIDE | DL0_TM_HS_P REP_HSF CYC |
| R/W-X | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_HS_TRAIL_OFFSET | | | | DL0_HS_ZERO_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_HS_PREP_OFFSET | | | | DL0_HS_TLPX_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-156. DPHY_TX_DL0_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-22 | RESERVED | R/W | X | |
| 21 | DL0_TEST_LPTX_DP | R/W | 0h | send 0 to LP TX Dn in HS mode |
| 20 | DL0_TEST_LPTX_DN | R/W | 0h | send 0 to LP TX Dp in HS mode |
| 19 | DL0_TEST_LPTX_EN | R/W | 0h | give output for LPTX from dig logic for HS entry LP sequence |
| 18 | DL0_TM_READY_SKEW_CAL | R/W | 0h | Assert o_TxReadyHS during skew calibration pattern transmission. |
| 17 | DL0_TM_HS_PREP_HAF CYC_OVERRIDE | R/W | 0h | HS Prepare extra half cycle offset is controlled by digital logic |
| 16 | DL0_TM_HS_PREP_HSF CYC | R/W | 0h | If bit 17 == 1 Sets HS Prepare extra offset to 0 half cycle |
| 15-12 | DL0_HS_TRAIL_OFFSET | R/W | 0h | Sets HS-TRAIL Offset to 0 |
| 11-8 | DL0_HS_ZERO_OFFSET | R/W | 0h | Sets HS-ZERO offset to 0 |
| 7-4 | DL0_HS_PREP_OFFSET | R/W | 0h | Sets HS-PREPARE offset to 0 |
| 3-0 | DL0_HS_TLPX_OFFSET | R/W | 0h | Sets TLPX Offset to 0 |

12.78 DPHY_TX_DL0_TX_DIG_TBIT2 Register (Offset = 224h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT2 is shown in [Figure 12-78](#) and described in [Table 12-158](#).

Return to [Summary Table](#).

test modes for during hs mode

**Table 12-157. DPHY_TX_DL0_TX_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0224h |

Figure 12-78. DPHY_TX_DL0_TX_DIG_TBIT2 Register

| | | | | | | | |
|--------------------------|----|----|----|----|-------------------------|------------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | DL0_TM_SKEW_CAL_SEQ | | |
| R/W-X | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_TM_SKEW_CAL_SEQ | | | | | DL0_TM_SKEW_CAL_SEQ_SEL | DL0_TM_SKEW_CAL_SYNC_PKT | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_TM_SKEW_CAL_SYNC_PKT | | | | | | DL0_TM_SKEW_CAL_SYNC_PKT_SEL | DL0_TM_HS_SYNC_PKT |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_TM_HS_SYNC_PKT | | | | | | | DL0_TM_HS_SYNC_PKT_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-158. DPHY_TX_DL0_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-27 | RESERVED | R/W | X | |
| 26-19 | DL0_TM_SKEW_CAL_SEQ | R/W | 0h | desired skew calibration test sequence |
| 18 | DL0_TM_SKEW_CAL_SEQ_SEL | R/W | 0h | To send 'AA as skew calibration pattern |
| 17-10 | DL0_TM_SKEW_CAL_SYNC_PKT | R/W | 0h | desired skew calibration test sync packet |
| 9 | DL0_TM_SKEW_CAL_SYNC_PKT_SEL | R/W | 0h | To send 'FF as Skew calibration sync packet |
| 8-1 | DL0_TM_HS_SYNC_PKT | R/W | 0h | desired HS test sync packet |
| 0 | DL0_TM_HS_SYNC_PKT_SEL | R/W | 0h | To send 'B8 as HS sync packet |

12.79 DPHY_TX_DL0_TX_DIG_TBIT3 Register (Offset = 228h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT3 is shown in [Figure 12-79](#) and described in [Table 12-160](#).

Return to [Summary Table](#).

tm_sersynth

**Table 12-159. DPHY_TX_DL0_TX_DIG_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0228h |

Figure 12-79. DPHY_TX_DL0_TX_DIG_TBIT3 Register

| | | | | | | | |
|----------|----|-----------------------|---------------------|----|----|------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | DL0_SERSYNTH_LOOPBACK | DL0_BAL_FORCE_STATE | | | DL0_BAL_FORCE_EN | RESERVED |
| R/W-X | | R/W-0h | R/W-0h | | | R/W-0h | R/W-X |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-160. DPHY_TX_DL0_TX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | DL0_SERSYNTH_LOOPBACK | R/W | 0h | De-serialiser will take input from sampler |
| 4-2 | DL0_BAL_FORCE_STATE | R/W | 0h | Force the SYNC packet detection logic into below states if <1> is '1', SYNC_DONE state |
| 1 | DL0_BAL_FORCE_EN | R/W | 0h | SYNC packet detection FSM in serialiser in BIST mode will work as per logic |
| 0 | RESERVED | R/W | X | |

12.80 DPHY_TX_DL0_TX_DIG_TBIT4 Register (Offset = 22Ch) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT4 is shown in [Figure 12-80](#) and described in [Table 12-162](#).

Return to [Summary Table](#).

lp test logic

**Table 12-161. DPHY_TX_DL0_TX_DIG_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 022Ch |

Figure 12-80. DPHY_TX_DL0_TX_DIG_TBIT4 Register

| | | | | | | | |
|--------------------|------------------|----|-------------------|---------------------------|---------------------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_CONTENTION_EN | DL0_UNUSED_14_13 | | DL0_FORCE_RX_MODE | DL0_TEST_DATA_LPTX_DP_SEL | DL0_TEST_DATA_LPTX_DN_SEL | DL0_TEST_DATA_LPTX | |
| R/W-0h | R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_TEST_DATA_LPTX | | | | | | DL0_TEST_DATA_LPTX_RSTN | DL0_TEST_DATA_LPTX_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-162. DPHY_TX_DL0_TX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---------------------------------------|
| 31-16 | RESERVED | R/W | X | |
| 15 | DL0_CONTENTION_EN | R/W | 0h | Contention detector logic is enabled |
| 14-13 | DL0_UNUSED_14_13 | R | 0h | RESERVED |
| 12 | DL0_FORCE_RX_MODE | R/W | 0h | Force LPRX into RX mode |
| 11 | DL0_TEST_DATA_LPTX_DP_SEL | R/W | 0h | Normal_ LPTX DP_B from logic for LPDT |
| 10 | DL0_TEST_DATA_LPTX_DN_SEL | R/W | 0h | Normal_ LPTX DN_B from logic for LPDT |
| 9-2 | DL0_TEST_DATA_LPTX | R/W | 0h | LPTX test data |
| 1 | DL0_TEST_DATA_LPTX_RSTN | R/W | 0h | LP test data logic is RESET |
| 0 | DL0_TEST_DATA_LPTX_EN | R/W | 0h | LP test data logic DISABLED |

12.81 DPHY_TX_DL0_TX_DIG_TBIT5 Register (Offset = 230h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT5 is shown in [Figure 12-81](#) and described in [Table 12-164](#).

Return to [Summary Table](#).

TX_DIG_TBIT5

**Table 12-163. DPHY_TX_DL0_TX_DIG_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0230h |

Figure 12-81. DPHY_TX_DL0_TX_DIG_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-164. DPHY_TX_DL0_TX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT5 | R | 0h | RESERVED |

12.82 DPHY_TX_DL0_TX_DIG_TBIT6 Register (Offset = 234h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT6 is shown in [Figure 12-82](#) and described in [Table 12-166](#).

Return to [Summary Table](#).

TX_DIG_TBIT6

**Table 12-165. DPHY_TX_DL0_TX_DIG_TBIT6
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0234h |

Figure 12-82. DPHY_TX_DL0_TX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-166. DPHY_TX_DL0_TX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT6 | R | 0h | RESERVED |

12.83 DPHY_TX_DL0_TX_DIG_TBIT7 Register (Offset = 238h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT7 is shown in [Figure 12-83](#) and described in [Table 12-168](#).

Return to [Summary Table](#).

TX_DIG_TBIT7

**Table 12-167. DPHY_TX_DL0_TX_DIG_TBIT7
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0238h |

Figure 12-83. DPHY_TX_DL0_TX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-168. DPHY_TX_DL0_TX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT7 | R | 0h | RESERVED |

12.84 DPHY_TX_DL0_TX_DIG_TBIT8 Register (Offset = 23Ch) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT8 is shown in [Figure 12-84](#) and described in [Table 12-170](#).

Return to [Summary Table](#).

TX_DIG_TBIT8

**Table 12-169. DPHY_TX_DL0_TX_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 023Ch |

Figure 12-84. DPHY_TX_DL0_TX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-170. DPHY_TX_DL0_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT8 | R | 0h | RESERVED |

12.85 DPHY_TX_DL0_TX_DIG_TBIT9 Register (Offset = 240h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT9 is shown in [Figure 12-85](#) and described in [Table 12-172](#).

Return to [Summary Table](#).

TX_DIG_TBIT9

**Table 12-171. DPHY_TX_DL0_TX_DIG_TBIT9
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0240h |

Figure 12-85. DPHY_TX_DL0_TX_DIG_TBIT9 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-172. DPHY_TX_DL0_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT9 | R | 0h | RESERVED |

12.86 DPHY_TX_DL0_TX_DIG_TBIT10 Register (Offset = 244h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT10 is shown in [Figure 12-86](#) and described in [Table 12-174](#).

Return to [Summary Table](#).

bist_reg1

**Table 12-173. DPHY_TX_DL0_TX_DIG_TBIT10
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0244h |

Figure 12-86. DPHY_TX_DL0_TX_DIG_TBIT10 Register

| | | | | | | | |
|---------------------------|----|----|----|--------------------------|----|----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | DL0_BIST_WAIT_TIME |
| R/W-X | | | | | | | R/W-4h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_BIST_WAIT_TIME | | | | DL0_BIST_ULPTX_TEST_TIME | | | |
| R/W-4h | | | | R/W-40h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_BIST_ULPTX_TEST_TIME | | | | DL0_BIST_SEND_CONFIG | | DL0_BIST_DIG_TO_DIG_LOOPBK | DL0_BIST_RUN_NEGEDGE_FIRST |
| R/W-40h | | | | R/W-0h | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_LENGTH_OF_DESKEW | | | | | | DL0_BIST_LOOPBK_MODE | DL0_BIST_EN |
| R/W-Bh | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-174. DPHY_TX_DL0_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24-21 | DL0_BIST_WAIT_TIME | R/W | 4h | BIST wait time between posedge run and negedge run of sampler clock |
| 20-13 | DL0_BIST_ULPTX_TEST_TIME | R/W | 40h | While testing ULPTX, LP00 will be maintained on DPDN for this many number of byte clock cycles |
| 12-11 | DL0_BIST_SEND_CONFIG | R/W | 0h | Option of configuring what to send in BIST mose. To send both deskew and HS data |
| 10 | DL0_BIST_DIG_TO_DIG_LOOPBK | R/W | 0h | main digital to pattern checker loopback enabled |
| 9 | DL0_BIST_RUN_NEGEDGE_FIRST | R/W | 0h | BIST will run with posedge of sampler clock first |
| 8-2 | DL0_BIST_LENGTH_OF_DESKEW | R/W | Bh | Length of deskew sequence In terms of us. By default 13us of deskew sequence will be transmitted |
| 1 | DL0_BIST_LOOPBK_MODE | R/W | 0h | loopback_mode bit, EXTERNAL_LOOPBACK |
| 0 | DL0_BIST_EN | R/W | 0h | BIST Disabled |

12.87 DPHY_TX_DL0_TX_DIG_TBIT11 Register (Offset = 248h) [reset = 0F0501B0h]

DPHY_TX_DL0_TX_DIG_TBIT11 is shown in [Figure 12-87](#) and described in [Table 12-176](#).

Return to [Summary Table](#).

bist_reg2

Table 12-175. DPHY_TX_DL0_TX_DIG_TBIT11 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0248h |

Figure 12-87. DPHY_TX_DL0_TX_DIG_TBIT11 Register

| | | | | | | | |
|------------------------|------------------|---------------|----|--------------------|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL0_BIST_FRM_IDLE_TIME | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_BIST_PKT_NUM | | | | | | | |
| R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_BIST_INF_MODE | DL0_BIST_FRM_NUM | | | | | | |
| R/W-0h | R/W-3h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_FRM_NUM | DL0_BIST_CLEAR | DL0_BIST_PRBS | | DL0_BIST_TEST_MODE | | | DL0_UNUSED_0 |
| R/W-3h | R/W-0h | R/W-3h | | R/W-0h | | | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-176. DPHY_TX_DL0_TX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-24 | DL0_BIST_FRM_IDLE_TIME | R/W | Fh | BIST_FRM_IDLE time is time between the frames |
| 23-16 | DL0_BIST_PKT_NUM | R/W | 5h | BIST_PAK_NUM is number of packets that are to be transmitted per frame |
| 15 | DL0_BIST_INF_MODE | R/W | 0h | run infinite BIST mode |
| 14-7 | DL0_BIST_FRM_NUM | R/W | 3h | BIST_FRM_NUM is number of frames to be transmitted |
| 6 | DL0_BIST_CLEAR | R/W | 0h | clear the bist |
| 5-4 | DL0_BIST_PRBS | R/W | 3h | BIST PRBS MODE 9 |
| 3-1 | DL0_BIST_TEST_MODE | R/W | 0h | PRBS mode |
| 0 | DL0_UNUSED_0 | R | 0h | RESERVED |

12.88 DPHY_TX_DL0_TX_DIG_TBIT12 Register (Offset = 24Ch) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT12 is shown in [Figure 12-88](#) and described in [Table 12-178](#).

Return to [Summary Table](#).

bist_reg3

**Table 12-177. DPHY_TX_DL0_TX_DIG_TBIT12
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 024Ch |

Figure 12-88. DPHY_TX_DL0_TX_DIG_TBIT12 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|---------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | DL0_BIST_RUN_LENGTH | | | | | | | | | | | |
| R/W-X | | | | R/W-28h | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-178. DPHY_TX_DL0_TX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|-----------------|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | DL0_BIST_RUN_LENGTH | R/W | 28h | BIST_RUN_LENGTH |

12.89 DPHY_TX_DL0_TX_DIG_TBIT13 Register (Offset = 250h) [reset = Ah]

DPHY_TX_DL0_TX_DIG_TBIT13 is shown in [Figure 12-89](#) and described in [Table 12-180](#).

Return to [Summary Table](#).

bist_reg4

**Table 12-179. DPHY_TX_DL0_TX_DIG_TBIT13
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0250h |

Figure 12-89. DPHY_TX_DL0_TX_DIG_TBIT13 Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_UNUSED_31_8 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_UNUSED_31_8 | | | | | | | | DL0_BIST_IDLE_TIME | | | | | | | |
| R-0h | | | | | | | | R/W-Ah | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-180. DPHY_TX_DL0_TX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------|
| 31-8 | DL0_UNUSED_31_8 | R | 0h | RESERVED |
| 7-0 | DL0_BIST_IDLE_TIME | R/W | Ah | BIST_IDLE_TIME |

12.90 DPHY_TX_DL0_TX_DIG_TBIT14 Register (Offset = 254h) [reset = DECDBCABh]

DPHY_TX_DL0_TX_DIG_TBIT14 is shown in [Figure 12-90](#) and described in [Table 12-182](#).

Return to [Summary Table](#).

bist_reg5

**Table 12-181. DPHY_TX_DL0_TX_DIG_TBIT14
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0254h |

Figure 12-90. DPHY_TX_DL0_TX_DIG_TBIT14 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_BIST_PKT4 | | | | | | | | DL0_BIST_PKT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_PKT2 | | | | | | | | DL0_BIST_PKT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-182. DPHY_TX_DL0_TX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|----------------|
| 31-24 | DL0_BIST_PKT4 | R/W | DEh | BIST_TEST_PAT4 |
| 23-16 | DL0_BIST_PKT3 | R/W | CDh | BIST_TEST_PAT3 |
| 15-8 | DL0_BIST_PKT2 | R/W | BCh | BIST_TEST_PAT2 |
| 7-0 | DL0_BIST_PKT1 | R/W | ABh | BIST_TEST_PAT1 |

12.91 DPHY_TX_DL0_TX_DIG_TBIT15 Register (Offset = 258h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT15 is shown in [Figure 12-91](#) and described in [Table 12-184](#).

Return to [Summary Table](#).

bist_reg6

Table 12-183. DPHY_TX_DL0_TX_DIG_TBIT15 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0258h |

Figure 12-91. DPHY_TX_DL0_TX_DIG_TBIT15 Register

| | | | | | | | |
|------------------------|----|----------------------|------------------------|----|----|---------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | DL0_BIST_LFSR_FREEZE | DL0_BIST_ERR_INJ_POINT | | | | |
| R/W-X | | R/W-0h | R/W-14h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_ERR_INJ_POINT | | | | | | DL0_BIST_ERR_INJ_EN | |
| R/W-14h | | | | | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-184. DPHY_TX_DL0_TX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-14 | RESERVED | R/W | X | |
| 13 | DL0_BIST_LFSR_FREEZE | R/W | 0h | Reset LFSR contents after every packet or frame |
| 12-1 | DL0_BIST_ERR_INJ_POINT | R/W | 14h | BIST_ERR_INJECT_POINT is where to inject the error in the packet |
| 0 | DL0_BIST_ERR_INJ_EN | R/W | 0h | Inject error in the BIST during the packet |

12.92 DPHY_TX_DL0_TX_DIG_TBIT16 Register (Offset = 25Ch) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT16 is shown in [Figure 12-92](#) and described in [Table 12-186](#).

Return to [Summary Table](#).

TX_DIG_TBIT16

**Table 12-185. DPHY_TX_DL0_TX_DIG_TBIT16
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 025Ch |

Figure 12-92. DPHY_TX_DL0_TX_DIG_TBIT16 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-186. DPHY_TX_DL0_TX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT16 | R | 0h | RESERVED |

12.93 DPHY_TX_DL0_TX_DIG_TBIT17 Register (Offset = 260h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT17 is shown in [Figure 12-93](#) and described in [Table 12-188](#).

Return to [Summary Table](#).

TX_DIG_TBIT17

**Table 12-187. DPHY_TX_DL0_TX_DIG_TBIT17
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0260h |

Figure 12-93. DPHY_TX_DL0_TX_DIG_TBIT17 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-188. DPHY_TX_DL0_TX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT17 | R | 0h | RESERVED |

12.94 DPHY_TX_DL0_TX_DIG_TBIT18 Register (Offset = 264h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT18 is shown in [Figure 12-94](#) and described in [Table 12-190](#).

Return to [Summary Table](#).

TX_DIG_TBIT18

**Table 12-189. DPHY_TX_DL0_TX_DIG_TBIT18
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0264h |

Figure 12-94. DPHY_TX_DL0_TX_DIG_TBIT18 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-190. DPHY_TX_DL0_TX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT18 | R | 0h | RESERVED |

12.95 DPHY_TX_DL0_TX_DIG_TBIT19 Register (Offset = 268h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT19 is shown in [Figure 12-95](#) and described in [Table 12-192](#).

Return to [Summary Table](#).

TX_DIG_TBIT19

Table 12-191. DPHY_TX_DL0_TX_DIG_TBIT19 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0268h |

Figure 12-95. DPHY_TX_DL0_TX_DIG_TBIT19 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-192. DPHY_TX_DL0_TX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT19 | R | 0h | RESERVED |

12.96 DPHY_TX_DL0_TX_DIG_TBIT20 Register (Offset = 26Ch) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT20 is shown in [Figure 12-96](#) and described in [Table 12-194](#).

Return to [Summary Table](#).

digital to analog signal muxing

**Table 12-193. DPHY_TX_DL0_TX_DIG_TBIT20
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 026Ch |

Figure 12-96. DPHY_TX_DL0_TX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------|------------------------|-----------------------|-------------------|---------------------------------|-----------------------------|-----------------------|-------------------|
| DL0_TM_ISO_EN | DL0_TM_LOAD_DPDN_SEL | DL0_TM_LOAD_DPDN | | | DL0_TM_HSTX_DATA_RATE_SEL | DL0_TM_HSTX_DATA_RATE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_TM_BIST_ULP_RCV_EN_SEL | DL0_TM_BIST_ULP_RCV_EN | DL0_TM_ULPS_PULDN_SEL | DL0_TM_ULPS_PULDN | DL0_TM_BIST_SMPLR_CLK_E_DGE_SEL | DL0_TM_BIST_SMPLR_CLK_E_DGE | DL0_TM_BIST_EN_SEL | DL0_TM_BIST_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_TM_LPTX_TRST_SEL | DL0_TM_LPTX_TRST | DL0_TM_LPTX_RST_SEL | DL0_TM_LPTX_RST | DL0_TM_LPTX_DP_SEL | DL0_TM_LPTX_DP | DL0_TM_LPTX_DN_SEL | DL0_TM_LPTX_DN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_TM_LDO_REF_EN_SEL | DL0_TM_LDO_REF_EN | DL0_TM_HSTX_TRST_SEL | DL0_TM_HSTX_TRST | DL0_TM_HSTX_RQST_SEL | DL0_TM_HSTX_RQST | DL0_TM_GLOB_AL_PD_SEL | DL0_TM_GLOB_AL_PD |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-194. DPHY_TX_DL0_TX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31 | DL0_TM_ISO_EN | R/W | 0h | Enable isolation in test mode |
| 30 | DL0_TM_LOAD_DPDN_SEL | R/W | 0h | Take ana_dpdn_load from dig logic |
| 29-27 | DL0_TM_LOAD_DPDN | R/W | 0h | set ana_dpdn_load as per requirement in test mode |
| 26 | DL0_TM_HSTX_DATA_RATE_SEL | R/W | 0h | Take ana_hstx_datarate from dig logic |
| 25-24 | DL0_TM_HSTX_DATA_RATE | R/W | 0h | set ana_hstx_datarate as per requirement in test mode |
| 23 | DL0_TM_BIST_ULP_RCV_EN_SEL | R/W | 0h | Take ana_bist_ulps_rcv_en from dig logic |
| 22 | DL0_TM_BIST_ULP_RCV_EN | R/W | 0h | set ana_bist_ulps_rcv_en to 0 |
| 21 | DL0_TM_ULPS_PULDN_SEL | R/W | 0h | Take ana_ulps_puldn from dig logic |
| 20 | DL0_TM_ULPS_PULDN | R/W | 0h | set ana_ulps_puldn to 0 |
| 19 | DL0_TM_BIST_SMPLR_CLK_EDGE_SEL | R/W | 0h | Take ana_bist_smplr_clkedge from dig logic |
| 18 | DL0_TM_BIST_SMPLR_CLK_EDGE | R/W | 0h | set ana_bist_smplr_clkedge to posedge |

Table 12-194. DPHY_TX_DL0_TX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 17 | DL0_TM_BIST_EN_SEL | R/W | 0h | Take ana_bist_en from dig logic |
| 16 | DL0_TM_BIST_EN | R/W | 0h | set ana_bist_en to 0 |
| 15 | DL0_TM_LPTX_TRST_SEL | R/W | 0h | Take ana_lptx_trst from dig logic |
| 14 | DL0_TM_LPTX_TRST | R/W | 0h | set ana_lptx_trst to 0 |
| 13 | DL0_TM_LPTX_RST_SEL | R/W | 0h | Take ana_lptx_rst from dig logic |
| 12 | DL0_TM_LPTX_RST | R/W | 0h | set ana_lptx_rst to 0 |
| 11 | DL0_TM_LPTX_DP_SEL | R/W | 0h | give output for LPTX DP from dig logic |
| 10 | DL0_TM_LPTX_DP | R/W | 0h | send 0 to LP TX Dp |
| 9 | DL0_TM_LPTX_DN_SEL | R/W | 0h | give output for LPTX DN from dig logic |
| 8 | DL0_TM_LPTX_DN | R/W | 0h | send 0 to LP TX Dn |
| 7 | DL0_TM_LDO_REF_EN_SEL | R/W | 0h | Take ana_ldo_ref_en from dig logic |
| 6 | DL0_TM_LDO_REF_EN | R/W | 0h | set ana_ldo_ref_en to 0 |
| 5 | DL0_TM_HSTX_TRST_SEL | R/W | 0h | Take ana_hstx_trst from dig logic |
| 4 | DL0_TM_HSTX_TRST | R/W | 0h | set ana_hstx_trst to 0 |
| 3 | DL0_TM_HSTX_RQST_SEL | R/W | 0h | Take ana_hstx_rqst from dig logic |
| 2 | DL0_TM_HSTX_RQST | R/W | 0h | set ana_hstx_rqst to 0 |
| 1 | DL0_TM_GLOBAL_PD_SEL | R/W | 0h | Take ana_global_pd from dig logic |
| 0 | DL0_TM_GLOBAL_PD | R/W | 0h | set ana_global_pd to 0 (powered up) |

12.97 DPHY_TX_DL0_TX_DIG_TBIT21 Register (Offset = 270h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT21 is shown in [Figure 12-97](#) and described in [Table 12-196](#).

Return to [Summary Table](#).

digital to analog signals test muxing

**Table 12-195. DPHY_TX_DL0_TX_DIG_TBIT21
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0270h |

Figure 12-97. DPHY_TX_DL0_TX_DIG_TBIT21 Register

| | | | | | | | |
|-------------------|---------------------------|-----------------------|----------------------|---------------------|------------------------|--------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | DL0_TM_SERSYNTH_RST_N_SEL | DL0_TM_SERSYNTH_RST_N | DL0_TM_SWAP_DPDN_SEL | DL0_TM_SWAP_DPDN_EN | DL0_TM_SERSYNTH_EN_SEL | DL0_TM_SERSYNTH_EN | DL0_TM_TX_DATA_HS_SEL |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_TM_TX_DATA_HS | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-196. DPHY_TX_DL0_TX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | DL0_TM_SERSYNTH_RST_N_SEL | R/W | 0h | Take sersynth_rst_n from dig logic |
| 13 | DL0_TM_SERSYNTH_RST_N | R/W | 0h | Set sersynth_rst_n to 1 |
| 12 | DL0_TM_SWAP_DPDN_SEL | R/W | 0h | Take swapdp_dn from dig logic |
| 11 | DL0_TM_SWAP_DPDN_EN | R/W | 0h | Set swap_dpdn to 1 |
| 10 | DL0_TM_SERSYNTH_EN_SEL | R/W | 0h | Take sersynth_en from dig logic |
| 9 | DL0_TM_SERSYNTH_EN | R/W | 0h | set sersynth_en to 1 |
| 8 | DL0_TM_TX_DATA_HS_SEL | R/W | 0h | sends single test byte to sersynth, which is in <7:0> |
| 7-0 | DL0_TM_TX_DATA_HS | R/W | 0h | Test byte that can be sent constantly to sersynth. This is validated by bit <8> of this reg |

12.98 DPHY_TX_DL0_TX_DIG_TBIT22 Register (Offset = 274h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT22 is shown in [Figure 12-98](#) and described in [Table 12-198](#).

Return to [Summary Table](#).

TX_DIG_TBIT22

Table 12-197. DPHY_TX_DL0_TX_DIG_TBIT22 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0274h |

Figure 12-98. DPHY_TX_DL0_TX_DIG_TBIT22 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-198. DPHY_TX_DL0_TX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT22 | R/W | 0h | spare |

12.99 DPHY_TX_DL0_TX_DIG_TBIT23 Register (Offset = 278h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT23 is shown in [Figure 12-99](#) and described in [Table 12-200](#).

Return to [Summary Table](#).

TX_DIG_TBIT23

**Table 12-199. DPHY_TX_DL0_TX_DIG_TBIT23
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0278h |

Figure 12-99. DPHY_TX_DL0_TX_DIG_TBIT23 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-200. DPHY_TX_DL0_TX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT23 | R | 0h | RESERVED |

12.100 DPHY_TX_DL0_TX_DIG_TBIT24 Register (Offset = 27Ch) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT24 is shown in [Figure 12-100](#) and described in [Table 12-202](#).

Return to [Summary Table](#).

TX_DIG_TBIT24

Table 12-201. DPHY_TX_DL0_TX_DIG_TBIT24 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 027Ch |

Figure 12-100. DPHY_TX_DL0_TX_DIG_TBIT24 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-202. DPHY_TX_DL0_TX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT24 | R | 0h | RESERVED |

12.101 DPHY_TX_DL0_TX_ANA_TBIT5 Register (Offset = 280h) [reset = 0h]

DPHY_TX_DL0_TX_ANA_TBIT5 is shown in [Figure 12-101](#) and described in [Table 12-204](#).

Return to [Summary Table](#).

TX_ANA_TBIT5

**Table 12-203. DPHY_TX_DL0_TX_ANA_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0280h |

Figure 12-101. DPHY_TX_DL0_TX_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_ANA_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-204. DPHY_TX_DL0_TX_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL0_ANA_TBIT5 | R | 0h | Analog Test register 5 |

12.102 DPHY_TX_DL0_TX_DIG_TBIT25 Register (Offset = 28Ch) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT25 is shown in [Figure 12-102](#) and described in [Table 12-206](#).

Return to [Summary Table](#).

bal and ana_ctrl [DPHY_TX_STATUS](#)

Table 12-205. DPHY_TX_DL0_TX_DIG_TBIT25 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 028Ch |

Figure 12-102. DPHY_TX_DL0_TX_DIG_TBIT25 Register

| | | | | | | | |
|---------------------|----|----|----|------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | DL0_ANA_CTRL_FSM_STATE | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-206. DPHY_TX_DL0_TX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|---|
| 31-21 | RESERVED | R | X | |
| 20-16 | DL0_ANA_CTRL_FSM_STATE | R | 0h | FSM state readout for ana_ctrl |
| 15-0 | DL0_BIST_BAL_STATUS | R | 0h | BAL logic DPHY_TX_STATUS read |

12.103 DPHY_TX_DL0_TX_DIG_TBIT26 Register (Offset = 290h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT26 is shown in [Figure 12-103](#) and described in [Table 12-208](#).

Return to [Summary Table](#).

fsm states in the design1

**Table 12-207. DPHY_TX_DL0_TX_DIG_TBIT26
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0290h |

Figure 12-103. DPHY_TX_DL0_TX_DIG_TBIT26 Register

| | | | | | | | |
|----------------------------------|----|----|----|----|----------------------------------|----|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL0_TM_DATA_ESC_RX_FSM_STATE | | | | | DL0_TM_DATA_ESCTX_CTRL_FSM_STATE | | |
| R-0h | | | | | R-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_TM_DATA_ESCTX_CTRL_FSM_STATE | | | | | | | DL0_TM_DATA_ESCTX_DATA_FSM_STATE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_TM_DATA_ESCTX_DATA_FSM_STATE | | | | | DL0_TM_HS_PATH_FSM_STATE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_TM_HS_PATH_FSM_STATE | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-208. DPHY_TX_DL0_TX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--------------------------------------|
| 31-27 | DL0_TM_DATA_ESC_RX_FSM_STATE | R | 0h | FSM state readout for esc rx path |
| 26-17 | DL0_TM_DATA_ESCTX_CTRL_FSM_STATE | R | 0h | fsm state for escape tx control path |
| 16-12 | DL0_TM_DATA_ESCTX_DATA_FSM_STATE | R | 0h | fsm state for escape tx data path |
| 11-0 | DL0_TM_HS_PATH_FSM_STATE | R | 0h | FSM state readout for hs path fsm |

12.104 DPHY_TX_DL0_TX_DIG_TBIT28 Register (Offset = 298h) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT28 is shown in [Figure 12-104](#) and described in [Table 12-210](#).

Return to [Summary Table](#).

lp component DPHY_TX_STATUS

Table 12-209. DPHY_TX_DL0_TX_DIG_TBIT28 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0298h |

Figure 12-104. DPHY_TX_DL0_TX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_TM_ANA_COMP_OUTS | | | | | | | | DL0_UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-210. DPHY_TX_DL0_TX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---------------------------|
| 31-16 | RESERVED | R | X | |
| 15-8 | DL0_TM_ANA_COMP_OUTS | R | 0h | Analog components outputs |
| 7-0 | DL0_UNUSED_7_0 | R | 0h | RESERVED |

12.105 DPHY_TX_DL0_TX_DIG_TBIT29 Register (Offset = 29Ch) [reset = X]

DPHY_TX_DL0_TX_DIG_TBIT29 is shown in [Figure 12-105](#) and described in [Table 12-212](#).

Return to [Summary Table](#).

bist DPHY_TX_STATUS reg1

**Table 12-211. DPHY_TX_DL0_TX_DIG_TBIT29
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 029Ch |

Figure 12-105. DPHY_TX_DL0_TX_DIG_TBIT29 Register

| | | | | | | | |
|----------------------------|------------------------|---------------------|---------------------------|-------------------|-------------------------|----------------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | DL0_TM_CUR_STATE_ULPTX_CHE | |
| R-X | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_TM_CUR_STATE_ULPRX_CHE | | | DL0_TM_CUR_STATE_LPCD_CHE | | | DL0_TM_CUR_STATE_LPRX_CHE | |
| R-0h | | | R-0h | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL0_TM_CUR_STATE_LPRX_CHE | DL0_TM_CUR_STATE_CTRLR | | | | DL0_BIST_DATA_LANE_PASS | DL0_BIST_LPRX_PASS | DL0_BIST_LPCD_PASS |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_ULPRX_PASS | DL0_BIST_ULPTX_PASS | DL0_BIST_HS_NEG_ERR | DL0_BIST_HS_POS_ERR | DL0_BIST_POS_SYNC | DL0_BIST_NEG_SYNC | DL0_BIST_CM_PLT | DL0_BIST_EN_STATUS |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-212. DPHY_TX_DL0_TX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-26 | RESERVED | R | X | |
| 25-24 | DL0_TM_CUR_STATE_ULPTX_CHE | R | 0h | Current state of the ULPTX checker FSM |
| 23-21 | DL0_TM_CUR_STATE_ULPRX_CHE | R | 0h | Current state of the ULPRX checker FSM |
| 20-18 | DL0_TM_CUR_STATE_LPCD_CHE | R | 0h | Current state of the LPCD checker FSM |
| 17-15 | DL0_TM_CUR_STATE_LPRX_CHE | R | 0h | Current state of the LPRX checker FSM |
| 14-11 | DL0_TM_CUR_STATE_CTRLR | R | 0h | Current state of the Control FSM |
| 10 | DL0_BIST_DATA_LANE_PASS | R | 0h | Data lane has passed BIST completely |
| 9 | DL0_BIST_LPRX_PASS | R | 0h | LPRX BIST pass |
| 8 | DL0_BIST_LPCD_PASS | R | 0h | LPCD BIST Passed |
| 7 | DL0_BIST_ULPRX_PASS | R | 0h | ULPRX BIST passed |
| 6 | DL0_BIST_ULPTX_PASS | R | 0h | ULPTX BIST passed |
| 5 | DL0_BIST_HS_NEG_ERR | R | 0h | HS Bist error detected with negedge of sampler clock |
| 4 | DL0_BIST_HS_POS_ERR | R | 0h | HS Bist error detected with posedge of sampler clock |

Table 12-212. DPHY_TX_DL0_TX_DIG_TBIT29 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 3 | DL0_BIST_POS_SYNC | R | 0h | Pattern checker in negedge run have synced with pattern generator |
| 2 | DL0_BIST_NEG_SYNC | R | 0h | Pattern checker in posedge run have synced with pattern generator |
| 1 | DL0_BIST_CMPLT | R | 0h | BIST is completed |
| 0 | DL0_BIST_EN_STATUS | R | 0h | BIST Controller is enabled |

12.106 DPHY_TX_DL0_TX_DIG_TBIT30 Register (Offset = 2A0h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT30 is shown in [Figure 12-106](#) and described in [Table 12-214](#).

[Return to Summary Table.](#)

bist pkt count values

**Table 12-213. DPHY_TX_DL0_TX_DIG_TBIT30
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02A0h |

Figure 12-106. DPHY_TX_DL0_TX_DIG_TBIT30 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_BIST_PAT_CHE_PKT_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_PAT_CHE_PKT_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-214. DPHY_TX_DL0_TX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-16 | DL0_BIST_PAT_CHE_PKT_CNT_NEG | R | 0h | pattern checker packet count with negedge run of sampler clock |
| 15-0 | DL0_BIST_PAT_CHE_PKT_CNT_POS | R | 0h | pattern checker packet count with posedge run of sampler clock |

12.107 DPHY_TX_DL0_TX_DIG_TBIT31 Register (Offset = 2A4h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT31 is shown in [Figure 12-107](#) and described in [Table 12-216](#).

Return to [Summary Table](#).

bist err count values

Table 12-215. DPHY_TX_DL0_TX_DIG_TBIT31 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02A4h |

Figure 12-107. DPHY_TX_DL0_TX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL0_BIST_PAT_CHE_ERR_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_BIST_PAT_CHE_ERR_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-216. DPHY_TX_DL0_TX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-16 | DL0_BIST_PAT_CHE_ERR_CNT_NEG | R | 0h | pattern checker error count with negedge run of sampler clock |
| 15-0 | DL0_BIST_PAT_CHE_ERR_CNT_POS | R | 0h | pattern checker error count with posedge run of sampler clock |

12.108 DPHY_TX_DL0_TX_DIG_TBIT32 Register (Offset = 2A8h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT32 is shown in [Figure 12-108](#) and described in [Table 12-218](#).

Return to [Summary Table](#).

TX_DIG_TBIT32

**Table 12-217. DPHY_TX_DL0_TX_DIG_TBIT32
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02A8h |

Figure 12-108. DPHY_TX_DL0_TX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-218. DPHY_TX_DL0_TX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT32 | R | 0h | RESERVED |

12.109 DPHY_TX_DL0_TX_DIG_TBIT33 Register (Offset = 2ACh) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT33 is shown in [Figure 12-109](#) and described in [Table 12-220](#).

Return to [Summary Table](#).

TX_DIG_TBIT33

**Table 12-219. DPHY_TX_DL0_TX_DIG_TBIT33
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02ACh |

Figure 12-109. DPHY_TX_DL0_TX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT33 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-220. DPHY_TX_DL0_TX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT33 | R | 0h | RESERVED |

12.110 DPHY_TX_DL0_TX_DIG_TBIT34 Register (Offset = 2B0h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT34 is shown in [Figure 12-110](#) and described in [Table 12-222](#).

Return to [Summary Table](#).

TX_DIG_TBIT34

**Table 12-221. DPHY_TX_DL0_TX_DIG_TBIT34
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02B0h |

Figure 12-110. DPHY_TX_DL0_TX_DIG_TBIT34 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| DL0_DIG_TBIT34 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-222. DPHY_TX_DL0_TX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT34 | R | 0h | RESERVED |

12.111 DPHY_TX_DL0_TX_DIG_TBIT35 Register (Offset = 2B4h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT35 is shown in [Figure 12-111](#) and described in [Table 12-224](#).

Return to [Summary Table](#).

TX_DIG_TBIT35

Table 12-223. DPHY_TX_DL0_TX_DIG_TBIT35 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02B4h |

Figure 12-111. DPHY_TX_DL0_TX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT35 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-224. DPHY_TX_DL0_TX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT35 | R | 0h | RESERVED |

12.112 DPHY_TX_DL0_TX_DIG_TBIT36 Register (Offset = 2B8h) [reset = 0h]

DPHY_TX_DL0_TX_DIG_TBIT36 is shown in [Figure 12-112](#) and described in [Table 12-226](#).

Return to [Summary Table](#).

TX_DIG_TBIT36

**Table 12-225. DPHY_TX_DL0_TX_DIG_TBIT36
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 02B8h |

Figure 12-112. DPHY_TX_DL0_TX_DIG_TBIT36 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL0_DIG_TBIT36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-226. DPHY_TX_DL0_TX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL0_DIG_TBIT36 | R | 0h | RESERVED |

12.113 DPHY_TX_DL1_TX_ANA_TBIT0 Register (Offset = 300h) [reset = 0h]

DPHY_TX_DL1_TX_ANA_TBIT0 is shown in [Figure 12-113](#) and described in [Table 12-228](#).

Return to [Summary Table](#).

TX_ANA_TBIT0

**Table 12-227. DPHY_TX_DL1_TX_ANA_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0300h |

Figure 12-113. DPHY_TX_DL1_TX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-228. DPHY_TX_DL1_TX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL1_ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

12.114 DPHY_TX_DL1_TX_ANA_TBIT1 Register (Offset = 304h) [reset = 0h]

DPHY_TX_DL1_TX_ANA_TBIT1 is shown in [Figure 12-114](#) and described in [Table 12-230](#).

Return to [Summary Table](#).

TX_ANA_TBIT1

**Table 12-229. DPHY_TX_DL1_TX_ANA_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0304h |

Figure 12-114. DPHY_TX_DL1_TX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-230. DPHY_TX_DL1_TX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL1_ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

12.115 DPHY_TX_DL1_TX_ANA_TBIT2 Register (Offset = 308h) [reset = 0h]

DPHY_TX_DL1_TX_ANA_TBIT2 is shown in [Figure 12-115](#) and described in [Table 12-232](#).

Return to [Summary Table](#).

TX_ANA_TBIT2

**Table 12-231. DPHY_TX_DL1_TX_ANA_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0308h |

Figure 12-115. DPHY_TX_DL1_TX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-232. DPHY_TX_DL1_TX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL1_ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

12.116 DPHY_TX_DL1_TX_ANA_TBIT3 Register (Offset = 30Ch) [reset = 0h]

DPHY_TX_DL1_TX_ANA_TBIT3 is shown in [Figure 12-116](#) and described in [Table 12-234](#).

Return to [Summary Table](#).

TX_ANA_TBIT3

**Table 12-233. DPHY_TX_DL1_TX_ANA_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 030Ch |

Figure 12-116. DPHY_TX_DL1_TX_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-234. DPHY_TX_DL1_TX_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL1_ANA_TBIT3 | R/W | 0h | Analog Test register 3 |

12.117 DPHY_TX_DL1_TX_ANA_TBIT4 Register (Offset = 310h) [reset = 0h]

DPHY_TX_DL1_TX_ANA_TBIT4 is shown in [Figure 12-117](#) and described in [Table 12-236](#).

Return to [Summary Table](#).

TX_ANA_TBIT4

**Table 12-235. DPHY_TX_DL1_TX_ANA_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0310h |

Figure 12-117. DPHY_TX_DL1_TX_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-236. DPHY_TX_DL1_TX_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL1_ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

12.118 DPHY_TX_DL1_TX_DIG_TBIT0 Register (Offset = 31Ch) [reset = 606h]

DPHY_TX_DL1_TX_DIG_TBIT0 is shown in [Figure 12-118](#) and described in [Table 12-238](#).

Return to [Summary Table](#).

ana_ctrl_counter_values

**Table 12-237. DPHY_TX_DL1_TX_DIG_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 031Ch |

Figure 12-118. DPHY_TX_DL1_TX_DIG_TBIT0 Register

| | | | | | | | |
|------------------|----|----|----|---------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL1_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_UNUSED_31_13 | | | | DL1_ULPS_PULLDN_CNT | | | |
| R-0h | | | | R/W-6h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_UNUSED_7_5 | | | | DL1_LDO_EN_CNT | | | |
| R-0h | | | | R/W-6h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-238. DPHY_TX_DL1_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-13 | DL1_UNUSED_31_13 | R | 0h | RESERVED |
| 12-8 | DL1_ULPS_PULLDN_CNT | R/W | 6h | After enabling LDO, ulps_pulldn will go to 0 after these many uS |
| 7-5 | DL1_UNUSED_7_5 | R | 0h | RESERVED |
| 4-0 | DL1_LDO_EN_CNT | R/W | 6h | Once the analog's power down signal is de asserted, LDO will be enabled after these many uS |

12.119 DPHY_TX_DL1_TX_DIG_TBIT1 Register (Offset = 320h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT1 is shown in [Figure 12-119](#) and described in [Table 12-240](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT1

**Table 12-239. DPHY_TX_DL1_TX_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0320h |

Figure 12-119. DPHY_TX_DL1_TX_DIG_TBIT1 Register

| | | | | | | | |
|---------------------|----|-------------------|-------------------|--------------------|------------------------|---------------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | DL1_TEST_LP_TX_DP | DL1_TEST_LP_TX_DN | DL1_TEST_LP_TX_EN | DL1_TM_READ_Y_SKEW_CAL | DL1_TM_HS_PREP_HAF_CYC_OVERRIDE | DL1_TM_HS_PREP_HSF_CYC |
| R/W-X | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_HS_TRAIL_OFFSET | | | | DL1_HS_ZERO_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_HS_PREP_OFFSET | | | | DL1_HS_TLPX_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-240. DPHY_TX_DL1_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-22 | RESERVED | R/W | X | |
| 21 | DL1_TEST_LPTX_DP | R/W | 0h | send 0 to LP TX Dn in HS mode |
| 20 | DL1_TEST_LPTX_DN | R/W | 0h | send 0 to LP TX Dp in HS mode |
| 19 | DL1_TEST_LPTX_EN | R/W | 0h | give output for LPTX from dig logic for HS entry LP sequence |
| 18 | DL1_TM_READY_SKEW_CAL | R/W | 0h | Assert o_TxReadyHS during skew calibration pattern transmission. |
| 17 | DL1_TM_HS_PREP_HAF_CYC_OVERRIDE | R/W | 0h | HS Prepare extra half cycle offset is controlled by digital logic |
| 16 | DL1_TM_HS_PREP_HSF_CYC | R/W | 0h | If bit 17 == 1 Sets HS Prepare extra offset to 0 half cycle |
| 15-12 | DL1_HS_TRAIL_OFFSET | R/W | 0h | Sets HS-TRAIL Offset to 0 |
| 11-8 | DL1_HS_ZERO_OFFSET | R/W | 0h | Sets HS-ZERO offset to 0 |
| 7-4 | DL1_HS_PREP_OFFSET | R/W | 0h | Sets HS-PREPARE offset to 0 |
| 3-0 | DL1_HS_TLPX_OFFSET | R/W | 0h | Sets TLPX Offset to 0 |

12.120 DPHY_TX_DL1_TX_DIG_TBIT2 Register (Offset = 324h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT2 is shown in [Figure 12-120](#) and described in [Table 12-242](#).

Return to [Summary Table](#).

test modes for during hs mode

**Table 12-241. DPHY_TX_DL1_TX_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0324h |

Figure 12-120. DPHY_TX_DL1_TX_DIG_TBIT2 Register

| | | | | | | | |
|--------------------------|----|----|----|----|-------------------------|------------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | DL1_TM_SKEW_CAL_SEQ | | |
| R/W-X | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_TM_SKEW_CAL_SEQ | | | | | DL1_TM_SKEW_CAL_SEQ_SEL | DL1_TM_SKEW_CAL_SYNC_PKT | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_TM_SKEW_CAL_SYNC_PKT | | | | | | DL1_TM_SKEW_CAL_SYNC_PKT_SEL | DL1_TM_HS_SYNC_PKT |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_TM_HS_SYNC_PKT | | | | | | | DL1_TM_HS_SYNC_PKT_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-242. DPHY_TX_DL1_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-27 | RESERVED | R/W | X | |
| 26-19 | DL1_TM_SKEW_CAL_SEQ | R/W | 0h | desired skew calibration test sequence |
| 18 | DL1_TM_SKEW_CAL_SEQ_SEL | R/W | 0h | To send 'AA as skew calibration pattern |
| 17-10 | DL1_TM_SKEW_CAL_SYNC_PKT | R/W | 0h | desired skew calibration test sync packet |
| 9 | DL1_TM_SKEW_CAL_SYNC_PKT_SEL | R/W | 0h | To send 'FF as Skew calibration sync packet |
| 8-1 | DL1_TM_HS_SYNC_PKT | R/W | 0h | desired HS test sync packet |
| 0 | DL1_TM_HS_SYNC_PKT_SEL | R/W | 0h | To send 'B8 as HS sync packet |

12.121 DPHY_TX_DL1_TX_DIG_TBIT3 Register (Offset = 328h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT3 is shown in [Figure 12-121](#) and described in [Table 12-244](#).

Return to [Summary Table](#).

tm_sersynth

**Table 12-243. DPHY_TX_DL1_TX_DIG_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0328h |

Figure 12-121. DPHY_TX_DL1_TX_DIG_TBIT3 Register

| | | | | | | | |
|----------|----|-----------------------|---------------------|----|----|------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | DL1_SERSYNTH_LOOPBACK | DL1_BAL_FORCE_STATE | | | DL1_BAL_FORCE_EN | RESERVED |
| R/W-X | | R/W-0h | R/W-0h | | | R/W-0h | R/W-X |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-244. DPHY_TX_DL1_TX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | DL1_SERSYNTH_LOOPBACK | R/W | 0h | De-serialiser will take input from sampler |
| 4-2 | DL1_BAL_FORCE_STATE | R/W | 0h | Force the SYNC packet detection logic into below states if <1> is '1', SYNC_DONE state |
| 1 | DL1_BAL_FORCE_EN | R/W | 0h | SYNC packet detection FSM in serialiser in BIST mode will work as per logic |
| 0 | RESERVED | R/W | X | |

12.122 DPHY_TX_DL1_TX_DIG_TBIT4 Register (Offset = 32Ch) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT4 is shown in [Figure 12-122](#) and described in [Table 12-246](#).

Return to [Summary Table](#).

lp test logic

**Table 12-245. DPHY_TX_DL1_TX_DIG_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 032Ch |

Figure 12-122. DPHY_TX_DL1_TX_DIG_TBIT4 Register

| | | | | | | | |
|--------------------|------------------|----|-------------------|---------------------------|---------------------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_CONTENTION_EN | DL1_UNUSED_14_13 | | DL1_FORCE_RX_MODE | DL1_TEST_DATA_LPTX_DP_SEL | DL1_TEST_DATA_LPTX_DN_SEL | DL1_TEST_DATA_LPTX | |
| R/W-0h | R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_TEST_DATA_LPTX | | | | | | DL1_TEST_DATA_LPTX_RSTN | DL1_TEST_DATA_LPTX_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-246. DPHY_TX_DL1_TX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---------------------------------------|
| 31-16 | RESERVED | R/W | X | |
| 15 | DL1_CONTENTION_EN | R/W | 0h | Contention detector logic is enabled |
| 14-13 | DL1_UNUSED_14_13 | R | 0h | RESERVED |
| 12 | DL1_FORCE_RX_MODE | R/W | 0h | Force LPRX into RX mode |
| 11 | DL1_TEST_DATA_LPTX_DP_SEL | R/W | 0h | Normal_ LPTX DP_B from logic for LPDT |
| 10 | DL1_TEST_DATA_LPTX_DN_SEL | R/W | 0h | Normal_ LPTX DN_B from logic for LPDT |
| 9-2 | DL1_TEST_DATA_LPTX | R/W | 0h | LPTX test data |
| 1 | DL1_TEST_DATA_LPTX_RSTN | R/W | 0h | LP test data logic is RESET |
| 0 | DL1_TEST_DATA_LPTX_EN | R/W | 0h | LP test data logic DISABLED |

12.123 DPHY_TX_DL1_TX_DIG_TBIT5 Register (Offset = 330h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT5 is shown in [Figure 12-123](#) and described in [Table 12-248](#).

Return to [Summary Table](#).

TX_DIG_TBIT5

**Table 12-247. DPHY_TX_DL1_TX_DIG_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0330h |

Figure 12-123. DPHY_TX_DL1_TX_DIG_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-248. DPHY_TX_DL1_TX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT5 | R | 0h | RESERVED |

12.124 DPHY_TX_DL1_TX_DIG_TBIT6 Register (Offset = 334h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT6 is shown in [Figure 12-124](#) and described in [Table 12-250](#).

Return to [Summary Table](#).

TX_DIG_TBIT6

**Table 12-249. DPHY_TX_DL1_TX_DIG_TBIT6
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0334h |

Figure 12-124. DPHY_TX_DL1_TX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-250. DPHY_TX_DL1_TX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT6 | R | 0h | RESERVED |

12.125 DPHY_TX_DL1_TX_DIG_TBIT7 Register (Offset = 338h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT7 is shown in [Figure 12-125](#) and described in [Table 12-252](#).

Return to [Summary Table](#).

TX_DIG_TBIT7

**Table 12-251. DPHY_TX_DL1_TX_DIG_TBIT7
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0338h |

Figure 12-125. DPHY_TX_DL1_TX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-252. DPHY_TX_DL1_TX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT7 | R | 0h | RESERVED |

12.126 DPHY_TX_DL1_TX_DIG_TBIT8 Register (Offset = 33Ch) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT8 is shown in [Figure 12-126](#) and described in [Table 12-254](#).

Return to [Summary Table](#).

TX_DIG_TBIT8

**Table 12-253. DPHY_TX_DL1_TX_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 033Ch |

Figure 12-126. DPHY_TX_DL1_TX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-254. DPHY_TX_DL1_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT8 | R | 0h | RESERVED |

12.127 DPHY_TX_DL1_TX_DIG_TBIT9 Register (Offset = 340h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT9 is shown in [Figure 12-127](#) and described in [Table 12-256](#).

Return to [Summary Table](#).

TX_DIG_TBIT9

**Table 12-255. DPHY_TX_DL1_TX_DIG_TBIT9
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0340h |

Figure 12-127. DPHY_TX_DL1_TX_DIG_TBIT9 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-256. DPHY_TX_DL1_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT9 | R | 0h | RESERVED |

12.128 DPHY_TX_DL1_TX_DIG_TBIT10 Register (Offset = 344h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT10 is shown in [Figure 12-128](#) and described in [Table 12-258](#).

Return to [Summary Table](#).

bist_reg1

**Table 12-257. DPHY_TX_DL1_TX_DIG_TBIT10
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0344h |

Figure 12-128. DPHY_TX_DL1_TX_DIG_TBIT10 Register

| | | | | | | | |
|---------------------------|----|----|----|--------------------------|----|----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | DL1_BIST_WAIT_TIME |
| R/W-X | | | | | | | R/W-4h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_BIST_WAIT_TIME | | | | DL1_BIST_ULPTX_TEST_TIME | | | |
| R/W-4h | | | | R/W-40h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_BIST_ULPTX_TEST_TIME | | | | DL1_BIST_SEND_CONFIG | | DL1_BIST_DIG_TO_DIG_LOOPBK | DL1_BIST_RUN_NEGEDGE_FIRST |
| R/W-40h | | | | R/W-0h | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_LENGTH_OF_DESKEW | | | | | | DL1_BIST_LOOPBK_MODE | DL1_BIST_EN |
| R/W-Bh | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-258. DPHY_TX_DL1_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24-21 | DL1_BIST_WAIT_TIME | R/W | 4h | BIST wait time between posedge run and negedge run of sampler clock |
| 20-13 | DL1_BIST_ULPTX_TEST_TIME | R/W | 40h | While testing ULPTX, LP00 will be maintained on DPDN for this many number of byte clock cycles |
| 12-11 | DL1_BIST_SEND_CONFIG | R/W | 0h | Option of configuring what to send in BIST mose. To send both deskew and HS data |
| 10 | DL1_BIST_DIG_TO_DIG_LOOPBK | R/W | 0h | main digital to pattern checker loopback enabled |
| 9 | DL1_BIST_RUN_NEGEDGE_FIRST | R/W | 0h | BIST will run with posedge of sampler clock first |
| 8-2 | DL1_BIST_LENGTH_OF_DESKEW | R/W | Bh | Length of deskew sequence In terms of us. By default 13us of deskew sequence will be transmitted |
| 1 | DL1_BIST_LOOPBK_MODE | R/W | 0h | loopback_mode bit, EXTERNAL_LOOPBACK |
| 0 | DL1_BIST_EN | R/W | 0h | BIST Disabled |

12.129 DPHY_TX_DL1_TX_DIG_TBIT11 Register (Offset = 348h) [reset = 0F0501B0h]

DPHY_TX_DL1_TX_DIG_TBIT11 is shown in [Figure 12-129](#) and described in [Table 12-260](#).

Return to [Summary Table](#).

bist_reg2

Table 12-259. DPHY_TX_DL1_TX_DIG_TBIT11 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0348h |

Figure 12-129. DPHY_TX_DL1_TX_DIG_TBIT11 Register

| | | | | | | | |
|------------------------|------------------|---------------|----|--------------------|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL1_BIST_FRM_IDLE_TIME | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_BIST_PKT_NUM | | | | | | | |
| R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_BIST_INF_MODE | DL1_BIST_FRM_NUM | | | | | | |
| R/W-0h | R/W-3h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_FRM_NUM | DL1_BIST_CLEAR | DL1_BIST_PRBS | | DL1_BIST_TEST_MODE | | | DL1_UNUSED_0 |
| R/W-3h | R/W-0h | R/W-3h | | R/W-0h | | | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-260. DPHY_TX_DL1_TX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-24 | DL1_BIST_FRM_IDLE_TIME | R/W | Fh | BIST_FRM_IDLE time is time between the frames |
| 23-16 | DL1_BIST_PKT_NUM | R/W | 5h | BIST_PAK_NUM is number of packets that are to be transmitted per frame |
| 15 | DL1_BIST_INF_MODE | R/W | 0h | run infinite BIST mode |
| 14-7 | DL1_BIST_FRM_NUM | R/W | 3h | BIST_FRM_NUM is number of frames to be transmitted |
| 6 | DL1_BIST_CLEAR | R/W | 0h | clear the bist |
| 5-4 | DL1_BIST_PRBS | R/W | 3h | BIST PRBS MODE 9 |
| 3-1 | DL1_BIST_TEST_MODE | R/W | 0h | PRBS mode |
| 0 | DL1_UNUSED_0 | R | 0h | RESERVED |

12.130 DPHY_TX_DL1_TX_DIG_TBIT12 Register (Offset = 34Ch) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT12 is shown in [Figure 12-130](#) and described in [Table 12-262](#).

Return to [Summary Table](#).

bist_reg3

**Table 12-261. DPHY_TX_DL1_TX_DIG_TBIT12
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 034Ch |

Figure 12-130. DPHY_TX_DL1_TX_DIG_TBIT12 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|---------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | DL1_BIST_RUN_LENGTH | | | | | | | | | | | |
| R/W-X | | | | R/W-28h | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-262. DPHY_TX_DL1_TX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|-----------------|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | DL1_BIST_RUN_LENGTH | R/W | 28h | BIST_RUN_LENGTH |

12.131 DPHY_TX_DL1_TX_DIG_TBIT13 Register (Offset = 350h) [reset = Ah]

DPHY_TX_DL1_TX_DIG_TBIT13 is shown in [Figure 12-131](#) and described in [Table 12-264](#).

Return to [Summary Table](#).

bist_reg4

**Table 12-263. DPHY_TX_DL1_TX_DIG_TBIT13
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0350h |

Figure 12-131. DPHY_TX_DL1_TX_DIG_TBIT13 Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_UNUSED_31_8 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_UNUSED_31_8 | | | | | | | | DL1_BIST_IDLE_TIME | | | | | | | |
| R-0h | | | | | | | | R/W-Ah | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-264. DPHY_TX_DL1_TX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------|
| 31-8 | DL1_UNUSED_31_8 | R | 0h | RESERVED |
| 7-0 | DL1_BIST_IDLE_TIME | R/W | Ah | BIST_IDLE_TIME |

12.132 DPHY_TX_DL1_TX_DIG_TBIT14 Register (Offset = 354h) [reset = DECDBCABh]

DPHY_TX_DL1_TX_DIG_TBIT14 is shown in [Figure 12-132](#) and described in [Table 12-266](#).

Return to [Summary Table](#).

bist_reg5

**Table 12-265. DPHY_TX_DL1_TX_DIG_TBIT14
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0354h |

Figure 12-132. DPHY_TX_DL1_TX_DIG_TBIT14 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_BIST_PKT4 | | | | | | | | DL1_BIST_PKT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_PKT2 | | | | | | | | DL1_BIST_PKT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-266. DPHY_TX_DL1_TX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|----------------|
| 31-24 | DL1_BIST_PKT4 | R/W | DEh | BIST_TEST_PAT4 |
| 23-16 | DL1_BIST_PKT3 | R/W | CDh | BIST_TEST_PAT3 |
| 15-8 | DL1_BIST_PKT2 | R/W | BCh | BIST_TEST_PAT2 |
| 7-0 | DL1_BIST_PKT1 | R/W | ABh | BIST_TEST_PAT1 |

12.133 DPHY_TX_DL1_TX_DIG_TBIT15 Register (Offset = 358h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT15 is shown in [Figure 12-133](#) and described in [Table 12-268](#).

Return to [Summary Table](#).

bist_reg6

**Table 12-267. DPHY_TX_DL1_TX_DIG_TBIT15
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0358h |

Figure 12-133. DPHY_TX_DL1_TX_DIG_TBIT15 Register

| | | | | | | | |
|------------------------|----|----------------------|------------------------|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | DL1_BIST_LFSR_FREEZE | DL1_BIST_ERR_INJ_POINT | | | | |
| R/W-X | | R/W-0h | R/W-14h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_ERR_INJ_POINT | | | | | | | DL1_BIST_ERR_INJ_EN |
| R/W-14h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-268. DPHY_TX_DL1_TX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-14 | RESERVED | R/W | X | |
| 13 | DL1_BIST_LFSR_FREEZE | R/W | 0h | Reset LFSR contents after every packet or frame |
| 12-1 | DL1_BIST_ERR_INJ_POINT | R/W | 14h | BIST_ERR_INJECT_POINT is where to inject the error in the packet |
| 0 | DL1_BIST_ERR_INJ_EN | R/W | 0h | Inject error in the BIST during the packet |

12.134 DPHY_TX_DL1_TX_DIG_TBIT16 Register (Offset = 35Ch) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT16 is shown in [Figure 12-134](#) and described in [Table 12-270](#).

Return to [Summary Table](#).

TX_DIG_TBIT16

**Table 12-269. DPHY_TX_DL1_TX_DIG_TBIT16
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 035Ch |

Figure 12-134. DPHY_TX_DL1_TX_DIG_TBIT16 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-270. DPHY_TX_DL1_TX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT16 | R | 0h | RESERVED |

12.135 DPHY_TX_DL1_TX_DIG_TBIT17 Register (Offset = 360h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT17 is shown in [Figure 12-135](#) and described in [Table 12-272](#).

Return to [Summary Table](#).

TX_DIG_TBIT17

Table 12-271. DPHY_TX_DL1_TX_DIG_TBIT17 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0360h |

Figure 12-135. DPHY_TX_DL1_TX_DIG_TBIT17 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-272. DPHY_TX_DL1_TX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT17 | R | 0h | RESERVED |

12.136 DPHY_TX_DL1_TX_DIG_TBIT18 Register (Offset = 364h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT18 is shown in [Figure 12-136](#) and described in [Table 12-274](#).

Return to [Summary Table](#).

TX_DIG_TBIT18

**Table 12-273. DPHY_TX_DL1_TX_DIG_TBIT18
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0364h |

Figure 12-136. DPHY_TX_DL1_TX_DIG_TBIT18 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-274. DPHY_TX_DL1_TX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT18 | R | 0h | RESERVED |

12.137 DPHY_TX_DL1_TX_DIG_TBIT19 Register (Offset = 368h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT19 is shown in [Figure 12-137](#) and described in [Table 12-276](#).

Return to [Summary Table](#).

TX_DIG_TBIT19

Table 12-275. DPHY_TX_DL1_TX_DIG_TBIT19 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0368h |

Figure 12-137. DPHY_TX_DL1_TX_DIG_TBIT19 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-276. DPHY_TX_DL1_TX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT19 | R | 0h | RESERVED |

12.138 DPHY_TX_DL1_TX_DIG_TBIT20 Register (Offset = 36Ch) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT20 is shown in [Figure 12-138](#) and described in [Table 12-278](#).

Return to [Summary Table](#).

digital to analog signal muxing

**Table 12-277. DPHY_TX_DL1_TX_DIG_TBIT20
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 036Ch |

Figure 12-138. DPHY_TX_DL1_TX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------|------------------------|-----------------------|-------------------|---------------------------------|-----------------------------|-----------------------|-------------------|
| DL1_TM_ISO_EN | DL1_TM_LOAD_DPDN_SEL | DL1_TM_LOAD_DPDN | | | DL1_TM_HSTX_DATA_RATE_SEL | DL1_TM_HSTX_DATE_RATE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_TM_BIST_ULP_RCV_EN_SEL | DL1_TM_BIST_ULP_RCV_EN | DL1_TM_ULPS_PULDN_SEL | DL1_TM_ULPS_PULDN | DL1_TM_BIST_SMPLR_CLK_E_DGE_SEL | DL1_TM_BIST_SMPLR_CLK_E_DGE | DL1_TM_BIST_EN_SEL | DL1_TM_BIST_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_TM_LPTX_TRST_SEL | DL1_TM_LPTX_TRST | DL1_TM_LPTX_RST_SEL | DL1_TM_LPTX_RST | DL1_TM_LPTX_DP_SEL | DL1_TM_LPTX_DP | DL1_TM_LPTX_DN_SEL | DL1_TM_LPTX_DN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_TM_LDO_REF_EN_SEL | DL1_TM_LDO_REF_EN | DL1_TM_HSTX_TRST_SEL | DL1_TM_HSTX_TRST | DL1_TM_HSTX_RQST_SEL | DL1_TM_HSTX_RQST | DL1_TM_GLOB_AL_PD_SEL | DL1_TM_GLOB_AL_PD |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-278. DPHY_TX_DL1_TX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31 | DL1_TM_ISO_EN | R/W | 0h | Enable isolation in test mode |
| 30 | DL1_TM_LOAD_DPDN_SEL | R/W | 0h | Take ana_dpdn_load from dig logic |
| 29-27 | DL1_TM_LOAD_DPDN | R/W | 0h | set ana_dpdn_load as per requirement in test mode |
| 26 | DL1_TM_HSTX_DATA_RATE_SEL | R/W | 0h | Take ana_hstx_datarate from dig logic |
| 25-24 | DL1_TM_HSTX_DATE_RATE | R/W | 0h | set ana_hstx_datarate as per requirement in test mode |
| 23 | DL1_TM_BIST_ULP_RCV_EN_SEL | R/W | 0h | Take ana_bist_ulps_rcv_en from dig logic |
| 22 | DL1_TM_BIST_ULP_RCV_EN | R/W | 0h | set ana_bist_ulps_rcv_en to 0 |
| 21 | DL1_TM_ULPS_PULDN_SEL | R/W | 0h | Take ana_ulps_puldn from dig logic |
| 20 | DL1_TM_ULPS_PULDN | R/W | 0h | set ana_ulps_puldn to 0 |
| 19 | DL1_TM_BIST_SMPLR_CLK_EDGE_SEL | R/W | 0h | Take ana_bist_smplr_clkedge from dig logic |
| 18 | DL1_TM_BIST_SMPLR_CLK_EDGE | R/W | 0h | set ana_bist_smplr_clkedge to posedge |

Table 12-278. DPHY_TX_DL1_TX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 17 | DL1_TM_BIST_EN_SEL | R/W | 0h | Take ana_bist_en from dig logic |
| 16 | DL1_TM_BIST_EN | R/W | 0h | set ana_bist_en to 0 |
| 15 | DL1_TM_LPTX_TRST_SEL | R/W | 0h | Take ana_lptx_trst from dig logic |
| 14 | DL1_TM_LPTX_TRST | R/W | 0h | set ana_lptx_trst to 0 |
| 13 | DL1_TM_LPTX_RST_SEL | R/W | 0h | Take ana_lptx_rst from dig logic |
| 12 | DL1_TM_LPTX_RST | R/W | 0h | set ana_lptx_rst to 0 |
| 11 | DL1_TM_LPTX_DP_SEL | R/W | 0h | give output for LPTX DP from dig logic |
| 10 | DL1_TM_LPTX_DP | R/W | 0h | send 0 to LP TX Dp |
| 9 | DL1_TM_LPTX_DN_SEL | R/W | 0h | give output for LPTX DN from dig logic |
| 8 | DL1_TM_LPTX_DN | R/W | 0h | send 0 to LP TX Dn |
| 7 | DL1_TM_LDO_REF_EN_SEL | R/W | 0h | Take ana_ldo_ref_en from dig logic |
| 6 | DL1_TM_LDO_REF_EN | R/W | 0h | set ana_ldo_ref_en to 0 |
| 5 | DL1_TM_HSTX_TRST_SEL | R/W | 0h | Take ana_hstx_trst from dig logic |
| 4 | DL1_TM_HSTX_TRST | R/W | 0h | set ana_hstx_trst to 0 |
| 3 | DL1_TM_HSTX_RQST_SEL | R/W | 0h | Take ana_hstx_rqst from dig logic |
| 2 | DL1_TM_HSTX_RQST | R/W | 0h | set ana_hstx_rqst to 0 |
| 1 | DL1_TM_GLOBAL_PD_SEL | R/W | 0h | Take ana_global_pd from dig logic |
| 0 | DL1_TM_GLOBAL_PD | R/W | 0h | set ana_global_pd to 0 (powered up) |

12.139 DPHY_TX_DL1_TX_DIG_TBIT21 Register (Offset = 370h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT21 is shown in [Figure 12-139](#) and described in [Table 12-280](#).

Return to [Summary Table](#).

digital to analog signals test muxing

**Table 12-279. DPHY_TX_DL1_TX_DIG_TBIT21
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0370h |

Figure 12-139. DPHY_TX_DL1_TX_DIG_TBIT21 Register

| | | | | | | | |
|-------------------|---------------------------|-----------------------|----------------------|---------------------|------------------------|--------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | DL1_TM_SERSYNTH_RST_N_SEL | DL1_TM_SERSYNTH_RST_N | DL1_TM_SWAP_DPDN_SEL | DL1_TM_SWAP_DPDN_EN | DL1_TM_SERSYNTH_EN_SEL | DL1_TM_SERSYNTH_EN | DL1_TM_TX_DATA_HS_SEL |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_TM_TX_DATA_HS | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-280. DPHY_TX_DL1_TX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | DL1_TM_SERSYNTH_RST_N_SEL | R/W | 0h | Take sersynth_rst_n from dig logic |
| 13 | DL1_TM_SERSYNTH_RST_N | R/W | 0h | Set sersynth_rst_n to 1 |
| 12 | DL1_TM_SWAP_DPDN_SEL | R/W | 0h | Take swapdp_dn from dig logic |
| 11 | DL1_TM_SWAP_DPDN_EN | R/W | 0h | Set swap_dpdn to 1 |
| 10 | DL1_TM_SERSYNTH_EN_SEL | R/W | 0h | Take sersynth_en from dig logic |
| 9 | DL1_TM_SERSYNTH_EN | R/W | 0h | set sersynth_en to 1 |
| 8 | DL1_TM_TX_DATA_HS_SEL | R/W | 0h | sends single test byte to sersynth, which is in <7:0> |
| 7-0 | DL1_TM_TX_DATA_HS | R/W | 0h | Test byte that can be sent constantly to sersynth. This is validated by bit <8> of this reg |

12.140 DPHY_TX_DL1_TX_DIG_TBIT22 Register (Offset = 374h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT22 is shown in [Figure 12-140](#) and described in [Table 12-282](#).

Return to [Summary Table](#).

TX_DIG_TBIT22

**Table 12-281. DPHY_TX_DL1_TX_DIG_TBIT22
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0374h |

Figure 12-140. DPHY_TX_DL1_TX_DIG_TBIT22 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-282. DPHY_TX_DL1_TX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT22 | R/W | 0h | spare |

12.141 DPHY_TX_DL1_TX_DIG_TBIT23 Register (Offset = 378h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT23 is shown in [Figure 12-141](#) and described in [Table 12-284](#).

Return to [Summary Table](#).

TX_DIG_TBIT23

**Table 12-283. DPHY_TX_DL1_TX_DIG_TBIT23
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0378h |

Figure 12-141. DPHY_TX_DL1_TX_DIG_TBIT23 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-284. DPHY_TX_DL1_TX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT23 | R | 0h | RESERVED |

12.142 DPHY_TX_DL1_TX_DIG_TBIT24 Register (Offset = 37Ch) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT24 is shown in [Figure 12-142](#) and described in [Table 12-286](#).

Return to [Summary Table](#).

TX_DIG_TBIT24

Table 12-285. DPHY_TX_DL1_TX_DIG_TBIT24 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 037Ch |

Figure 12-142. DPHY_TX_DL1_TX_DIG_TBIT24 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-286. DPHY_TX_DL1_TX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT24 | R | 0h | RESERVED |

12.143 DPHY_TX_DL1_TX_ANA_TBIT5 Register (Offset = 380h) [reset = 0h]

DPHY_TX_DL1_TX_ANA_TBIT5 is shown in [Figure 12-143](#) and described in [Table 12-288](#).

Return to [Summary Table](#).

TX_ANA_TBIT5

**Table 12-287. DPHY_TX_DL1_TX_ANA_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0380h |

Figure 12-143. DPHY_TX_DL1_TX_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_ANA_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-288. DPHY_TX_DL1_TX_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL1_ANA_TBIT5 | R | 0h | Analog Test register 5 |

12.144 DPHY_TX_DL1_TX_DIG_TBIT25 Register (Offset = 38Ch) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT25 is shown in [Figure 12-144](#) and described in [Table 12-290](#).

Return to [Summary Table](#).

bal and ana_ctrl DPHY_TX_STATUS

Table 12-289. DPHY_TX_DL1_TX_DIG_TBIT25 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 038Ch |

Figure 12-144. DPHY_TX_DL1_TX_DIG_TBIT25 Register

| | | | | | | | |
|---------------------|----|----|----|------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | DL1_ANA_CTRL_FSM_STATE | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-290. DPHY_TX_DL1_TX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--------------------------------|
| 31-21 | RESERVED | R | X | |
| 20-16 | DL1_ANA_CTRL_FSM_STATE | R | 0h | FSM state readout for ana_ctrl |
| 15-0 | DL1_BIST_BAL_STATUS | R | 0h | BAL logic DPHY_TX_STATUS read |

12.145 DPHY_TX_DL1_TX_DIG_TBIT26 Register (Offset = 390h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT26 is shown in [Figure 12-145](#) and described in [Table 12-292](#).

Return to [Summary Table](#).

fsm states in the design1

**Table 12-291. DPHY_TX_DL1_TX_DIG_TBIT26
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0390h |

Figure 12-145. DPHY_TX_DL1_TX_DIG_TBIT26 Register

| | | | | | | | |
|----------------------------------|----|----|----|----------------------------------|----|----------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL1_TM_DATA_ESC_RX_FSM_STATE | | | | DL1_TM_DATA_ESCTX_CTRL_FSM_STATE | | | |
| R-0h | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_TM_DATA_ESCTX_CTRL_FSM_STATE | | | | | | DL1_TM_DATA_ESCTX_DATA_FSM_STATE | |
| R-0h | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_TM_DATA_ESCTX_DATA_FSM_STATE | | | | DL1_TM_HS_PATH_FSM_STATE | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_TM_HS_PATH_FSM_STATE | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-292. DPHY_TX_DL1_TX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--------------------------------------|
| 31-27 | DL1_TM_DATA_ESC_RX_FSM_STATE | R | 0h | FSM state readout for esc rx path |
| 26-17 | DL1_TM_DATA_ESCTX_CTRL_FSM_STATE | R | 0h | fsm state for escape tx control path |
| 16-12 | DL1_TM_DATA_ESCTX_DATA_FSM_STATE | R | 0h | fsm state for escape tx data path |
| 11-0 | DL1_TM_HS_PATH_FSM_STATE | R | 0h | FSM state readout for hs path fsm |

12.146 DPHY_TX_DL1_TX_DIG_TBIT28 Register (Offset = 398h) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT28 is shown in [Figure 12-146](#) and described in [Table 12-294](#).

Return to [Summary Table](#).

lp component DPHY_TX_STATUS

Table 12-293. DPHY_TX_DL1_TX_DIG_TBIT28 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0398h |

Figure 12-146. DPHY_TX_DL1_TX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_TM_ANA_COMP_OUTS | | | | | | | | DL1_UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-294. DPHY_TX_DL1_TX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---------------------------|
| 31-16 | RESERVED | R | X | |
| 15-8 | DL1_TM_ANA_COMP_OUTS | R | 0h | Analog components outputs |
| 7-0 | DL1_UNUSED_7_0 | R | 0h | RESERVED |

12.147 DPHY_TX_DL1_TX_DIG_TBIT29 Register (Offset = 39Ch) [reset = X]

DPHY_TX_DL1_TX_DIG_TBIT29 is shown in [Figure 12-147](#) and described in [Table 12-296](#).

Return to [Summary Table](#).

bist DPHY_TX_STATUS reg1

**Table 12-295. DPHY_TX_DL1_TX_DIG_TBIT29
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 039Ch |

Figure 12-147. DPHY_TX_DL1_TX_DIG_TBIT29 Register

| | | | | | | | |
|----------------------------|------------------------|---------------------|---------------------------|-------------------|-------------------------|----------------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | DL1_TM_CUR_STATE_ULPTX_CHE | |
| R-X | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_TM_CUR_STATE_ULPRX_CHE | | | DL1_TM_CUR_STATE_LPCD_CHE | | | DL1_TM_CUR_STATE_LPRX_CHE | |
| R-0h | | | R-0h | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL1_TM_CUR_STATE_LPRX_CHE | DL1_TM_CUR_STATE_CTRLR | | | | DL1_BIST_DATA_LANE_PASS | DL1_BIST_LPRX_PASS | DL1_BIST_LPCD_PASS |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_ULPRX_PASS | DL1_BIST_ULPTX_PASS | DL1_BIST_HS_NEG_ERR | DL1_BIST_HS_POS_ERR | DL1_BIST_POS_SYNC | DL1_BIST_NEG_SYNC | DL1_BIST_CM_PLT | DL1_BIST_EN_STATUS |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-296. DPHY_TX_DL1_TX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-26 | RESERVED | R | X | |
| 25-24 | DL1_TM_CUR_STATE_ULPTX_CHE | R | 0h | Current state of the ULPTX checker FSM |
| 23-21 | DL1_TM_CUR_STATE_ULPRX_CHE | R | 0h | Current state of the ULPRX checker FSM |
| 20-18 | DL1_TM_CUR_STATE_LPCD_CHE | R | 0h | Current state of the LPCD checker FSM |
| 17-15 | DL1_TM_CUR_STATE_LPRX_CHE | R | 0h | Current state of the LPRX checker FSM |
| 14-11 | DL1_TM_CUR_STATE_CTRLR | R | 0h | Current state of the Control FSM |
| 10 | DL1_BIST_DATA_LANE_PASS | R | 0h | Data lane has passed BIST completely |
| 9 | DL1_BIST_LPRX_PASS | R | 0h | LPRX BIST pass |
| 8 | DL1_BIST_LPCD_PASS | R | 0h | LPCD BIST Passed |
| 7 | DL1_BIST_ULPRX_PASS | R | 0h | ULPRX BIST passed |
| 6 | DL1_BIST_ULPTX_PASS | R | 0h | ULPTX BIST passed |
| 5 | DL1_BIST_HS_NEG_ERR | R | 0h | HS Bist error detected with negedge of sampler clock |
| 4 | DL1_BIST_HS_POS_ERR | R | 0h | HS Bist error detected with posedge of sampler clock |

Table 12-296. DPHY_TX_DL1_TX_DIG_TBIT29 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 3 | DL1_BIST_POS_SYNC | R | 0h | Pattern checker in negedge run have synced with pattern generator |
| 2 | DL1_BIST_NEG_SYNC | R | 0h | Pattern checker in posedge run have synced with pattern generator |
| 1 | DL1_BIST_CMPLT | R | 0h | BIST is completed |
| 0 | DL1_BIST_EN_STATUS | R | 0h | BIST Controller is enabled |

12.148 DPHY_TX_DL1_TX_DIG_TBIT30 Register (Offset = 3A0h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT30 is shown in [Figure 12-148](#) and described in [Table 12-298](#).

[Return to Summary Table.](#)

bist pkt count values

**Table 12-297. DPHY_TX_DL1_TX_DIG_TBIT30
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03A0h |

Figure 12-148. DPHY_TX_DL1_TX_DIG_TBIT30 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_BIST_PAT_CHE_PKT_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_PAT_CHE_PKT_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-298. DPHY_TX_DL1_TX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-16 | DL1_BIST_PAT_CHE_PKT_CNT_NEG | R | 0h | pattern checker packet count with negedge run of sampler clock |
| 15-0 | DL1_BIST_PAT_CHE_PKT_CNT_POS | R | 0h | pattern checker packet count with posedge run of sampler clock |

12.149 DPHY_TX_DL1_TX_DIG_TBIT31 Register (Offset = 3A4h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT31 is shown in [Figure 12-149](#) and described in [Table 12-300](#).

Return to [Summary Table](#).

bist err count values

Table 12-299. DPHY_TX_DL1_TX_DIG_TBIT31 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03A4h |

Figure 12-149. DPHY_TX_DL1_TX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL1_BIST_PAT_CHE_ERR_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_BIST_PAT_CHE_ERR_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-300. DPHY_TX_DL1_TX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-16 | DL1_BIST_PAT_CHE_ERR_CNT_NEG | R | 0h | pattern checker error count with negedge run of sampler clock |
| 15-0 | DL1_BIST_PAT_CHE_ERR_CNT_POS | R | 0h | pattern checker error count with posedge run of sampler clock |

12.150 DPHY_TX_DL1_TX_DIG_TBIT32 Register (Offset = 3A8h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT32 is shown in [Figure 12-150](#) and described in [Table 12-302](#).

Return to [Summary Table](#).

TX_DIG_TBIT32

**Table 12-301. DPHY_TX_DL1_TX_DIG_TBIT32
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03A8h |

Figure 12-150. DPHY_TX_DL1_TX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-302. DPHY_TX_DL1_TX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT32 | R | 0h | RESERVED |

12.151 DPHY_TX_DL1_TX_DIG_TBIT33 Register (Offset = 3ACh) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT33 is shown in [Figure 12-151](#) and described in [Table 12-304](#).

Return to [Summary Table](#).

TX_DIG_TBIT33

**Table 12-303. DPHY_TX_DL1_TX_DIG_TBIT33
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03ACh |

Figure 12-151. DPHY_TX_DL1_TX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT33 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-304. DPHY_TX_DL1_TX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT33 | R | 0h | RESERVED |

12.152 DPHY_TX_DL1_TX_DIG_TBIT34 Register (Offset = 3B0h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT34 is shown in [Figure 12-152](#) and described in [Table 12-306](#).

Return to [Summary Table](#).

TX_DIG_TBIT34

**Table 12-305. DPHY_TX_DL1_TX_DIG_TBIT34
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03B0h |

Figure 12-152. DPHY_TX_DL1_TX_DIG_TBIT34 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT34 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-306. DPHY_TX_DL1_TX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT34 | R | 0h | RESERVED |

12.153 DPHY_TX_DL1_TX_DIG_TBIT35 Register (Offset = 3B4h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT35 is shown in [Figure 12-153](#) and described in [Table 12-308](#).

Return to [Summary Table](#).

TX_DIG_TBIT35

**Table 12-307. DPHY_TX_DL1_TX_DIG_TBIT35
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03B4h |

Figure 12-153. DPHY_TX_DL1_TX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT35 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-308. DPHY_TX_DL1_TX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT35 | R | 0h | RESERVED |

12.154 DPHY_TX_DL1_TX_DIG_TBIT36 Register (Offset = 3B8h) [reset = 0h]

DPHY_TX_DL1_TX_DIG_TBIT36 is shown in [Figure 12-154](#) and described in [Table 12-310](#).

Return to [Summary Table](#).

TX_DIG_TBIT36

**Table 12-309. DPHY_TX_DL1_TX_DIG_TBIT36
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 03B8h |

Figure 12-154. DPHY_TX_DL1_TX_DIG_TBIT36 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL1_DIG_TBIT36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-310. DPHY_TX_DL1_TX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL1_DIG_TBIT36 | R | 0h | RESERVED |

12.155 DPHY_TX_DL2_TX_ANA_TBIT0 Register (Offset = 400h) [reset = 0h]

DPHY_TX_DL2_TX_ANA_TBIT0 is shown in [Figure 12-155](#) and described in [Table 12-312](#).

Return to [Summary Table](#).

TX_ANA_TBIT0

**Table 12-311. DPHY_TX_DL2_TX_ANA_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0400h |

Figure 12-155. DPHY_TX_DL2_TX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-312. DPHY_TX_DL2_TX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL2_ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

12.156 DPHY_TX_DL2_TX_ANA_TBIT1 Register (Offset = 404h) [reset = 0h]

DPHY_TX_DL2_TX_ANA_TBIT1 is shown in [Figure 12-156](#) and described in [Table 12-314](#).

Return to [Summary Table](#).

TX_ANA_TBIT1

**Table 12-313. DPHY_TX_DL2_TX_ANA_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0404h |

Figure 12-156. DPHY_TX_DL2_TX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-314. DPHY_TX_DL2_TX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL2_ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

12.157 DPHY_TX_DL2_TX_ANA_TBIT2 Register (Offset = 408h) [reset = 0h]

DPHY_TX_DL2_TX_ANA_TBIT2 is shown in [Figure 12-157](#) and described in [Table 12-316](#).

Return to [Summary Table](#).

TX_ANA_TBIT2

**Table 12-315. DPHY_TX_DL2_TX_ANA_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0408h |

Figure 12-157. DPHY_TX_DL2_TX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-316. DPHY_TX_DL2_TX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL2_ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

12.158 DPHY_TX_DL2_TX_ANA_TBIT3 Register (Offset = 40Ch) [reset = 0h]

DPHY_TX_DL2_TX_ANA_TBIT3 is shown in [Figure 12-158](#) and described in [Table 12-318](#).

Return to [Summary Table](#).

TX_ANA_TBIT3

**Table 12-317. DPHY_TX_DL2_TX_ANA_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 040Ch |

Figure 12-158. DPHY_TX_DL2_TX_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-318. DPHY_TX_DL2_TX_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL2_ANA_TBIT3 | R/W | 0h | Analog Test register 3 |

12.159 DPHY_TX_DL2_TX_ANA_TBIT4 Register (Offset = 410h) [reset = 0h]

DPHY_TX_DL2_TX_ANA_TBIT4 is shown in [Figure 12-159](#) and described in [Table 12-320](#).

Return to [Summary Table](#).

TX_ANA_TBIT4

Table 12-319. DPHY_TX_DL2_TX_ANA_TBIT4 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0410h |

Figure 12-159. DPHY_TX_DL2_TX_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-320. DPHY_TX_DL2_TX_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL2_ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

12.160 DPHY_TX_DL2_TX_DIG_TBIT0 Register (Offset = 41Ch) [reset = 606h]

DPHY_TX_DL2_TX_DIG_TBIT0 is shown in [Figure 12-160](#) and described in [Table 12-322](#).

Return to [Summary Table](#).

ana_ctrl_counter_values

**Table 12-321. DPHY_TX_DL2_TX_DIG_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 041Ch |

Figure 12-160. DPHY_TX_DL2_TX_DIG_TBIT0 Register

| | | | | | | | |
|------------------|----|----|----|---------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL2_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_UNUSED_31_13 | | | | DL2_ULPS_PULLDN_CNT | | | |
| R-0h | | | | R/W-6h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_UNUSED_7_5 | | | | DL2_LDO_EN_CNT | | | |
| R-0h | | | | R/W-6h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-322. DPHY_TX_DL2_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-13 | DL2_UNUSED_31_13 | R | 0h | RESERVED |
| 12-8 | DL2_ULPS_PULLDN_CNT | R/W | 6h | After enabling LDO, ulps_pulldn will go to 0 after these many uS |
| 7-5 | DL2_UNUSED_7_5 | R | 0h | RESERVED |
| 4-0 | DL2_LDO_EN_CNT | R/W | 6h | Once the analog's power down signal is de asserted, LDO will be enabled after these many uS |

12.161 DPHY_TX_DL2_TX_DIG_TBIT1 Register (Offset = 420h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT1 is shown in [Figure 12-161](#) and described in [Table 12-324](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT1

**Table 12-323. DPHY_TX_DL2_TX_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0420h |

Figure 12-161. DPHY_TX_DL2_TX_DIG_TBIT1 Register

| | | | | | | | |
|---------------------|----|----------------------|----------------------|----------------------|---------------------------|--|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | DL2_TEST_LP TX_DP | DL2_TEST_LP TX_DN | DL2_TEST_LP TX_EN | DL2_TM_READ Y_SKEW_CAL | DL2_TM_HS_P REP_HAFCYC _OVERRIDE | DL2_TM_HS_P REP_HSF CYC |
| R/W-X | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_HS_TRAIL_OFFSET | | | | DL2_HS_ZERO_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_HS_PREP_OFFSET | | | | DL2_HS_TLPX_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-324. DPHY_TX_DL2_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------------|------|-------|---|
| 31-22 | RESERVED | R/W | X | |
| 21 | DL2_TEST_LPTX_DP | R/W | 0h | send 0 to LP TX Dn in HS mode |
| 20 | DL2_TEST_LPTX_DN | R/W | 0h | send 0 to LP TX Dp in HS mode |
| 19 | DL2_TEST_LPTX_EN | R/W | 0h | give output for LPTX from dig logic for HS entry LP sequence |
| 18 | DL2_TM_READY_SKEW_CAL | R/W | 0h | Assert o_TxReadyHS during skew calibration pattern transmission. |
| 17 | DL2_TM_HS_PREP_HAF CYC_OVERRIDE | R/W | 0h | HS Prepare extra half cycle offset is controlled by digital logic |
| 16 | DL2_TM_HS_PREP_HSF CYC | R/W | 0h | If bit 17 == 1 Sets HS Prepare extra offset to 0 half cycle |
| 15-12 | DL2_HS_TRAIL_OFFSET | R/W | 0h | Sets HS-TRAIL Offset to 0 |
| 11-8 | DL2_HS_ZERO_OFFSET | R/W | 0h | Sets HS-ZERO offset to 0 |
| 7-4 | DL2_HS_PREP_OFFSET | R/W | 0h | Sets HS-PREPARE offset to 0 |
| 3-0 | DL2_HS_TLPX_OFFSET | R/W | 0h | Sets TLPX Offset to 0 |

12.162 DPHY_TX_DL2_TX_DIG_TBIT2 Register (Offset = 424h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT2 is shown in [Figure 12-162](#) and described in [Table 12-326](#).

Return to [Summary Table](#).

test modes for during hs mode

**Table 12-325. DPHY_TX_DL2_TX_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0424h |

Figure 12-162. DPHY_TX_DL2_TX_DIG_TBIT2 Register

| | | | | | | | |
|--------------------------|----|----|----|----|-------------------------|------------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | DL2_TM_SKEW_CAL_SEQ | | |
| R/W-X | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_TM_SKEW_CAL_SEQ | | | | | DL2_TM_SKEW_CAL_SEQ_SEL | DL2_TM_SKEW_CAL_SYNC_PKT | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_TM_SKEW_CAL_SYNC_PKT | | | | | | DL2_TM_SKEW_CAL_SYNC_PKT_SEL | DL2_TM_HS_SYNC_PKT |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_TM_HS_SYNC_PKT | | | | | | | DL2_TM_HS_SYNC_PKT_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-326. DPHY_TX_DL2_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-27 | RESERVED | R/W | X | |
| 26-19 | DL2_TM_SKEW_CAL_SEQ | R/W | 0h | desired skew calibration test sequence |
| 18 | DL2_TM_SKEW_CAL_SEQ_SEL | R/W | 0h | To send 'AA as skew calibration pattern |
| 17-10 | DL2_TM_SKEW_CAL_SYNC_PKT | R/W | 0h | desired skew calibration test sync packet |
| 9 | DL2_TM_SKEW_CAL_SYNC_PKT_SEL | R/W | 0h | To send 'FF as Skew calibration sync packet |
| 8-1 | DL2_TM_HS_SYNC_PKT | R/W | 0h | desired HS test sync packet |
| 0 | DL2_TM_HS_SYNC_PKT_SEL | R/W | 0h | To send 'B8 as HS sync packet |

12.163 DPHY_TX_DL2_TX_DIG_TBIT3 Register (Offset = 428h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT3 is shown in [Figure 12-163](#) and described in [Table 12-328](#).

Return to [Summary Table](#).

tm_sersynth

**Table 12-327. DPHY_TX_DL2_TX_DIG_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0428h |

Figure 12-163. DPHY_TX_DL2_TX_DIG_TBIT3 Register

| | | | | | | | |
|----------|----|-----------------------|---------------------|----|----|------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | DL2_SERSYNTH_LOOPBACK | DL2_BAL_FORCE_STATE | | | DL2_BAL_FORCE_EN | RESERVED |
| R/W-X | | R/W-0h | R/W-0h | | | R/W-0h | R/W-X |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-328. DPHY_TX_DL2_TX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | DL2_SERSYNTH_LOOPBACK | R/W | 0h | De-serialiser will take input from sampler |
| 4-2 | DL2_BAL_FORCE_STATE | R/W | 0h | Force the SYNC packet detection logic into below states if <1> is '1', SYNC_DONE state |
| 1 | DL2_BAL_FORCE_EN | R/W | 0h | SYNC packet detection FSM in serialiser in BIST mode will work as per logic |
| 0 | RESERVED | R/W | X | |

12.164 DPHY_TX_DL2_TX_DIG_TBIT4 Register (Offset = 42Ch) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT4 is shown in [Figure 12-164](#) and described in [Table 12-330](#).

Return to [Summary Table](#).

lp test logic

**Table 12-329. DPHY_TX_DL2_TX_DIG_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 042Ch |

Figure 12-164. DPHY_TX_DL2_TX_DIG_TBIT4 Register

| | | | | | | | |
|--------------------|------------------|----|-------------------|---------------------------|---------------------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_CONTENTION_EN | DL2_UNUSED_14_13 | | DL2_FORCE_RX_MODE | DL2_TEST_DATA_LPTX_DP_SEL | DL2_TEST_DATA_LPTX_DN_SEL | DL2_TEST_DATA_LPTX | |
| R/W-0h | R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_TEST_DATA_LPTX | | | | | | DL2_TEST_DATA_LPTX_RSTN | DL2_TEST_DATA_LPTX_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-330. DPHY_TX_DL2_TX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---------------------------------------|
| 31-16 | RESERVED | R/W | X | |
| 15 | DL2_CONTENTION_EN | R/W | 0h | Contention detector logic is enabled |
| 14-13 | DL2_UNUSED_14_13 | R | 0h | RESERVED |
| 12 | DL2_FORCE_RX_MODE | R/W | 0h | Force LPRX into RX mode |
| 11 | DL2_TEST_DATA_LPTX_DP_SEL | R/W | 0h | Normal_ LPTX DP_B from logic for LPDT |
| 10 | DL2_TEST_DATA_LPTX_DN_SEL | R/W | 0h | Normal_ LPTX DN_B from logic for LPDT |
| 9-2 | DL2_TEST_DATA_LPTX | R/W | 0h | LPTX test data |
| 1 | DL2_TEST_DATA_LPTX_RSTN | R/W | 0h | LP test data logic is RESET |
| 0 | DL2_TEST_DATA_LPTX_EN | R/W | 0h | LP test data logic DISABLED |

12.165 DPHY_TX_DL2_TX_DIG_TBIT5 Register (Offset = 430h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT5 is shown in [Figure 12-165](#) and described in [Table 12-332](#).

Return to [Summary Table](#).

TX_DIG_TBIT5

**Table 12-331. DPHY_TX_DL2_TX_DIG_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0430h |

Figure 12-165. DPHY_TX_DL2_TX_DIG_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-332. DPHY_TX_DL2_TX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT5 | R | 0h | RESERVED |

12.166 DPHY_TX_DL2_TX_DIG_TBIT6 Register (Offset = 434h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT6 is shown in [Figure 12-166](#) and described in [Table 12-334](#).

Return to [Summary Table](#).

TX_DIG_TBIT6

**Table 12-333. DPHY_TX_DL2_TX_DIG_TBIT6
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0434h |

Figure 12-166. DPHY_TX_DL2_TX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-334. DPHY_TX_DL2_TX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT6 | R | 0h | RESERVED |

12.167 DPHY_TX_DL2_TX_DIG_TBIT7 Register (Offset = 438h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT7 is shown in [Figure 12-167](#) and described in [Table 12-336](#).

Return to [Summary Table](#).

TX_DIG_TBIT7

**Table 12-335. DPHY_TX_DL2_TX_DIG_TBIT7
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0438h |

Figure 12-167. DPHY_TX_DL2_TX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-336. DPHY_TX_DL2_TX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT7 | R | 0h | RESERVED |

12.168 DPHY_TX_DL2_TX_DIG_TBIT8 Register (Offset = 43Ch) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT8 is shown in [Figure 12-168](#) and described in [Table 12-338](#).

Return to [Summary Table](#).

TX_DIG_TBIT8

**Table 12-337. DPHY_TX_DL2_TX_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 043Ch |

Figure 12-168. DPHY_TX_DL2_TX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-338. DPHY_TX_DL2_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT8 | R | 0h | RESERVED |

12.169 DPHY_TX_DL2_TX_DIG_TBIT9 Register (Offset = 440h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT9 is shown in [Figure 12-169](#) and described in [Table 12-340](#).

Return to [Summary Table](#).

TX_DIG_TBIT9

**Table 12-339. DPHY_TX_DL2_TX_DIG_TBIT9
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0440h |

Figure 12-169. DPHY_TX_DL2_TX_DIG_TBIT9 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-340. DPHY_TX_DL2_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT9 | R | 0h | RESERVED |

12.170 DPHY_TX_DL2_TX_DIG_TBIT10 Register (Offset = 444h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT10 is shown in [Figure 12-170](#) and described in [Table 12-342](#).

Return to [Summary Table](#).

bist_reg1

**Table 12-341. DPHY_TX_DL2_TX_DIG_TBIT10
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0444h |

Figure 12-170. DPHY_TX_DL2_TX_DIG_TBIT10 Register

| | | | | | | | |
|---------------------------|----|----|----|--------------------------|----|----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | DL2_BIST_WAIT_TIME |
| R/W-X | | | | | | | R/W-4h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_BIST_WAIT_TIME | | | | DL2_BIST_ULPTX_TEST_TIME | | | |
| R/W-4h | | | | R/W-40h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_BIST_ULPTX_TEST_TIME | | | | DL2_BIST_SEND_CONFIG | | DL2_BIST_DIG_TO_DIG_LOOPBK | DL2_BIST_RUN_NEGEDGE_FIRST |
| R/W-40h | | | | R/W-0h | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_LENGTH_OF_DESKEW | | | | | | DL2_BIST_LOOPBK_MODE | DL2_BIST_EN |
| R/W-Bh | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-342. DPHY_TX_DL2_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24-21 | DL2_BIST_WAIT_TIME | R/W | 4h | BIST wait time between posedge run and negedge run of sampler clock |
| 20-13 | DL2_BIST_ULPTX_TEST_TIME | R/W | 40h | While testing ULPTX, LP00 will be maintained on DPDN for this many number of byte clock cycles |
| 12-11 | DL2_BIST_SEND_CONFIG | R/W | 0h | Option of configuring what to send in BIST mose. To send both deskew and HS data |
| 10 | DL2_BIST_DIG_TO_DIG_LOOPBK | R/W | 0h | main digital to pattern checker loopback enabled |
| 9 | DL2_BIST_RUN_NEGEDGE_FIRST | R/W | 0h | BIST will run with posedge of sampler clock first |
| 8-2 | DL2_BIST_LENGTH_OF_DESKEW | R/W | Bh | Length of deskew sequence In terms of us. By default 13us of deskew sequence will be transmitted |
| 1 | DL2_BIST_LOOPBK_MODE | R/W | 0h | loopback_mode bit, EXTERNAL_LOOPBACK |
| 0 | DL2_BIST_EN | R/W | 0h | BIST Disabled |

12.171 DPHY_TX_DL2_TX_DIG_TBIT11 Register (Offset = 448h) [reset = 0F0501B0h]

DPHY_TX_DL2_TX_DIG_TBIT11 is shown in [Figure 12-171](#) and described in [Table 12-344](#).

Return to [Summary Table](#).

bist_reg2

Table 12-343. DPHY_TX_DL2_TX_DIG_TBIT11 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0448h |

Figure 12-171. DPHY_TX_DL2_TX_DIG_TBIT11 Register

| | | | | | | | |
|------------------------|------------------|---------------|----|--------------------|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL2_BIST_FRM_IDLE_TIME | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_BIST_PKT_NUM | | | | | | | |
| R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_BIST_INF_MODE | DL2_BIST_FRM_NUM | | | | | | |
| R/W-0h | R/W-3h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_FRM_NUM | DL2_BIST_CLEAR | DL2_BIST_PRBS | | DL2_BIST_TEST_MODE | | | DL2_UNUSED_0 |
| R/W-3h | R/W-0h | R/W-3h | | R/W-0h | | | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-344. DPHY_TX_DL2_TX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-24 | DL2_BIST_FRM_IDLE_TIME | R/W | Fh | BIST_FRM_IDLE time is time between the frames |
| 23-16 | DL2_BIST_PKT_NUM | R/W | 5h | BIST_PAK_NUM is number of packets that are to be transmitted per frame |
| 15 | DL2_BIST_INF_MODE | R/W | 0h | run infinite BIST mode |
| 14-7 | DL2_BIST_FRM_NUM | R/W | 3h | BIST_FRM_NUM is number of frames to be transmitted |
| 6 | DL2_BIST_CLEAR | R/W | 0h | clear the bist |
| 5-4 | DL2_BIST_PRBS | R/W | 3h | BIST PRBS MODE 9 |
| 3-1 | DL2_BIST_TEST_MODE | R/W | 0h | PRBS mode |
| 0 | DL2_UNUSED_0 | R | 0h | RESERVED |

12.172 DPHY_TX_DL2_TX_DIG_TBIT12 Register (Offset = 44Ch) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT12 is shown in [Figure 12-172](#) and described in [Table 12-346](#).

Return to [Summary Table](#).

bist_reg3

**Table 12-345. DPHY_TX_DL2_TX_DIG_TBIT12
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 044Ch |

Figure 12-172. DPHY_TX_DL2_TX_DIG_TBIT12 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|---------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | DL2_BIST_RUN_LENGTH | | | | | | | | | | | |
| R/W-X | | | | R/W-28h | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-346. DPHY_TX_DL2_TX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|-----------------|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | DL2_BIST_RUN_LENGTH | R/W | 28h | BIST_RUN_LENGTH |

12.173 DPHY_TX_DL2_TX_DIG_TBIT13 Register (Offset = 450h) [reset = Ah]

DPHY_TX_DL2_TX_DIG_TBIT13 is shown in [Figure 12-173](#) and described in [Table 12-348](#).

Return to [Summary Table](#).

bist_reg4

**Table 12-347. DPHY_TX_DL2_TX_DIG_TBIT13
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0450h |

Figure 12-173. DPHY_TX_DL2_TX_DIG_TBIT13 Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_UNUSED_31_8 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_UNUSED_31_8 | | | | | | | | DL2_BIST_IDLE_TIME | | | | | | | |
| R-0h | | | | | | | | R/W-Ah | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-348. DPHY_TX_DL2_TX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------|
| 31-8 | DL2_UNUSED_31_8 | R | 0h | RESERVED |
| 7-0 | DL2_BIST_IDLE_TIME | R/W | Ah | BIST_IDLE_TIME |

12.174 DPHY_TX_DL2_TX_DIG_TBIT14 Register (Offset = 454h) [reset = DECDBCABh]

DPHY_TX_DL2_TX_DIG_TBIT14 is shown in [Figure 12-174](#) and described in [Table 12-350](#).

Return to [Summary Table](#).

bist_reg5

**Table 12-349. DPHY_TX_DL2_TX_DIG_TBIT14
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0454h |

Figure 12-174. DPHY_TX_DL2_TX_DIG_TBIT14 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_BIST_PKT4 | | | | | | | | DL2_BIST_PKT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_PKT2 | | | | | | | | DL2_BIST_PKT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-350. DPHY_TX_DL2_TX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|----------------|
| 31-24 | DL2_BIST_PKT4 | R/W | DEh | BIST_TEST_PAT4 |
| 23-16 | DL2_BIST_PKT3 | R/W | CDh | BIST_TEST_PAT3 |
| 15-8 | DL2_BIST_PKT2 | R/W | BCh | BIST_TEST_PAT2 |
| 7-0 | DL2_BIST_PKT1 | R/W | ABh | BIST_TEST_PAT1 |

12.175 DPHY_TX_DL2_TX_DIG_TBIT15 Register (Offset = 458h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT15 is shown in [Figure 12-175](#) and described in [Table 12-352](#).

Return to [Summary Table](#).

bist_reg6

**Table 12-351. DPHY_TX_DL2_TX_DIG_TBIT15
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0458h |

Figure 12-175. DPHY_TX_DL2_TX_DIG_TBIT15 Register

| | | | | | | | |
|------------------------|----|----------------------|------------------------|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | DL2_BIST_LFSR_FREEZE | DL2_BIST_ERR_INJ_POINT | | | | |
| R/W-X | | R/W-0h | R/W-14h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_ERR_INJ_POINT | | | | | | | DL2_BIST_ERR_INJ_EN |
| R/W-14h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-352. DPHY_TX_DL2_TX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-14 | RESERVED | R/W | X | |
| 13 | DL2_BIST_LFSR_FREEZE | R/W | 0h | Reset LFSR contents after every packet or frame |
| 12-1 | DL2_BIST_ERR_INJ_POINT | R/W | 14h | BIST_ERR_INJECT_POINT is where to inject the error in the packet |
| 0 | DL2_BIST_ERR_INJ_EN | R/W | 0h | Inject error in the BIST during the packet |

12.176 DPHY_TX_DL2_TX_DIG_TBIT16 Register (Offset = 45Ch) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT16 is shown in [Figure 12-176](#) and described in [Table 12-354](#).

Return to [Summary Table](#).

TX_DIG_TBIT16

**Table 12-353. DPHY_TX_DL2_TX_DIG_TBIT16
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 045Ch |

Figure 12-176. DPHY_TX_DL2_TX_DIG_TBIT16 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-354. DPHY_TX_DL2_TX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT16 | R | 0h | RESERVED |

12.177 DPHY_TX_DL2_TX_DIG_TBIT17 Register (Offset = 460h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT17 is shown in [Figure 12-177](#) and described in [Table 12-356](#).

Return to [Summary Table](#).

TX_DIG_TBIT17

Table 12-355. DPHY_TX_DL2_TX_DIG_TBIT17 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0460h |

Figure 12-177. DPHY_TX_DL2_TX_DIG_TBIT17 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-356. DPHY_TX_DL2_TX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT17 | R | 0h | RESERVED |

12.178 DPHY_TX_DL2_TX_DIG_TBIT18 Register (Offset = 464h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT18 is shown in [Figure 12-178](#) and described in [Table 12-358](#).

Return to [Summary Table](#).

TX_DIG_TBIT18

**Table 12-357. DPHY_TX_DL2_TX_DIG_TBIT18
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0464h |

Figure 12-178. DPHY_TX_DL2_TX_DIG_TBIT18 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-358. DPHY_TX_DL2_TX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT18 | R | 0h | RESERVED |

12.179 DPHY_TX_DL2_TX_DIG_TBIT19 Register (Offset = 468h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT19 is shown in [Figure 12-179](#) and described in [Table 12-360](#).

Return to [Summary Table](#).

TX_DIG_TBIT19

**Table 12-359. DPHY_TX_DL2_TX_DIG_TBIT19
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0468h |

Figure 12-179. DPHY_TX_DL2_TX_DIG_TBIT19 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-360. DPHY_TX_DL2_TX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT19 | R | 0h | RESERVED |

12.180 DPHY_TX_DL2_TX_DIG_TBIT20 Register (Offset = 46Ch) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT20 is shown in [Figure 12-180](#) and described in [Table 12-362](#).

Return to [Summary Table](#).

digital to analog signal muxing

**Table 12-361. DPHY_TX_DL2_TX_DIG_TBIT20
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 046Ch |

Figure 12-180. DPHY_TX_DL2_TX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------|------------------------|-----------------------|-------------------|---------------------------------|-----------------------------|-----------------------|-------------------|
| DL2_TM_ISO_EN | DL2_TM_LOAD_DPDN_SEL | DL2_TM_LOAD_DPDN | | | DL2_TM_HSTX_DATA_RATE_SEL | DL2_TM_HSTX_DATE_RATE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_TM_BIST_ULP_RCV_EN_SEL | DL2_TM_BIST_ULP_RCV_EN | DL2_TM_ULPS_PULDN_SEL | DL2_TM_ULPS_PULDN | DL2_TM_BIST_SMPLR_CLK_E_DGE_SEL | DL2_TM_BIST_SMPLR_CLK_E_DGE | DL2_TM_BIST_EN_SEL | DL2_TM_BIST_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_TM_LPTX_TRST_SEL | DL2_TM_LPTX_TRST | DL2_TM_LPTX_RST_SEL | DL2_TM_LPTX_RST | DL2_TM_LPTX_DP_SEL | DL2_TM_LPTX_DP | DL2_TM_LPTX_DN_SEL | DL2_TM_LPTX_DN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_TM_LDO_REF_EN_SEL | DL2_TM_LDO_REF_EN | DL2_TM_HSTX_TRST_SEL | DL2_TM_HSTX_TRST | DL2_TM_HSTX_RQST_SEL | DL2_TM_HSTX_RQST | DL2_TM_GLOB_AL_PD_SEL | DL2_TM_GLOB_AL_PD |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-362. DPHY_TX_DL2_TX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31 | DL2_TM_ISO_EN | R/W | 0h | Enable isolation in test mode |
| 30 | DL2_TM_LOAD_DPDN_SEL | R/W | 0h | Take ana_dpdn_load from dig logic |
| 29-27 | DL2_TM_LOAD_DPDN | R/W | 0h | set ana_dpdn_load as per requirement in test mode |
| 26 | DL2_TM_HSTX_DATA_RATE_SEL | R/W | 0h | Take ana_hstx_datarate from dig logic |
| 25-24 | DL2_TM_HSTX_DATE_RATE | R/W | 0h | set ana_hstx_datarate as per requirement in test mode |
| 23 | DL2_TM_BIST_ULP_RCV_EN_SEL | R/W | 0h | Take ana_bist_ulps_rcv_en from dig logic |
| 22 | DL2_TM_BIST_ULP_RCV_EN | R/W | 0h | set ana_bist_ulps_rcv_en to 0 |
| 21 | DL2_TM_ULPS_PULDN_SEL | R/W | 0h | Take ana_ulps_puldn from dig logic |
| 20 | DL2_TM_ULPS_PULDN | R/W | 0h | set ana_ulps_puldn to 0 |
| 19 | DL2_TM_BIST_SMPLR_CLK_EDGE_SEL | R/W | 0h | Take ana_bist_smplr_clkedge from dig logic |
| 18 | DL2_TM_BIST_SMPLR_CLK_EDGE | R/W | 0h | set ana_bist_smplr_clkedge to posedge |

Table 12-362. DPHY_TX_DL2_TX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 17 | DL2_TM_BIST_EN_SEL | R/W | 0h | Take ana_bist_en from dig logic |
| 16 | DL2_TM_BIST_EN | R/W | 0h | set ana_bist_en to 0 |
| 15 | DL2_TM_LPTX_TRST_SEL | R/W | 0h | Take ana_lptx_trst from dig logic |
| 14 | DL2_TM_LPTX_TRST | R/W | 0h | set ana_lptx_trst to 0 |
| 13 | DL2_TM_LPTX_RST_SEL | R/W | 0h | Take ana_lptx_rst from dig logic |
| 12 | DL2_TM_LPTX_RST | R/W | 0h | set ana_lptx_rst to 0 |
| 11 | DL2_TM_LPTX_DP_SEL | R/W | 0h | give output for LPTX DP from dig logic |
| 10 | DL2_TM_LPTX_DP | R/W | 0h | send 0 to LP TX Dp |
| 9 | DL2_TM_LPTX_DN_SEL | R/W | 0h | give output for LPTX DN from dig logic |
| 8 | DL2_TM_LPTX_DN | R/W | 0h | send 0 to LP TX Dn |
| 7 | DL2_TM_LDO_REF_EN_SEL | R/W | 0h | Take ana_ldo_ref_en from dig logic |
| 6 | DL2_TM_LDO_REF_EN | R/W | 0h | set ana_ldo_ref_en to 0 |
| 5 | DL2_TM_HSTX_TRST_SEL | R/W | 0h | Take ana_hstx_trst from dig logic |
| 4 | DL2_TM_HSTX_TRST | R/W | 0h | set ana_hstx_trst to 0 |
| 3 | DL2_TM_HSTX_RQST_SEL | R/W | 0h | Take ana_hstx_rqst from dig logic |
| 2 | DL2_TM_HSTX_RQST | R/W | 0h | set ana_hstx_rqst to 0 |
| 1 | DL2_TM_GLOBAL_PD_SEL | R/W | 0h | Take ana_global_pd from dig logic |
| 0 | DL2_TM_GLOBAL_PD | R/W | 0h | set ana_global_pd to 0 (powered up) |

12.181 DPHY_TX_DL2_TX_DIG_TBIT21 Register (Offset = 470h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT21 is shown in [Figure 12-181](#) and described in [Table 12-364](#).

Return to [Summary Table](#).

digital to analog signals test muxing

**Table 12-363. DPHY_TX_DL2_TX_DIG_TBIT21
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0470h |

Figure 12-181. DPHY_TX_DL2_TX_DIG_TBIT21 Register

| | | | | | | | |
|-------------------|---------------------------|-----------------------|----------------------|---------------------|------------------------|--------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | DL2_TM_SERSYNTH_RST_N_SEL | DL2_TM_SERSYNTH_RST_N | DL2_TM_SWAP_DPDN_SEL | DL2_TM_SWAP_DPDN_EN | DL2_TM_SERSYNTH_EN_SEL | DL2_TM_SERSYNTH_EN | DL2_TM_TX_DATA_HS_SEL |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_TM_TX_DATA_HS | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-364. DPHY_TX_DL2_TX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | DL2_TM_SERSYNTH_RST_N_SEL | R/W | 0h | Take sersynth_rst_n from dig logic |
| 13 | DL2_TM_SERSYNTH_RST_N | R/W | 0h | Set sersynth_rst_n to 1 |
| 12 | DL2_TM_SWAP_DPDN_SEL | R/W | 0h | Take swapdp_dn from dig logic |
| 11 | DL2_TM_SWAP_DPDN_EN | R/W | 0h | Set swap_dpdn to 1 |
| 10 | DL2_TM_SERSYNTH_EN_SEL | R/W | 0h | Take sersynth_en from dig logic |
| 9 | DL2_TM_SERSYNTH_EN | R/W | 0h | set sersynth_en to 1 |
| 8 | DL2_TM_TX_DATA_HS_SEL | R/W | 0h | sends single test byte to sersynth, which is in <7:0> |
| 7-0 | DL2_TM_TX_DATA_HS | R/W | 0h | Test byte that can be sent constantly to sersynth. This is validated by bit <8> of this reg |

12.182 DPHY_TX_DL2_TX_DIG_TBIT22 Register (Offset = 474h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT22 is shown in [Figure 12-182](#) and described in [Table 12-366](#).

Return to [Summary Table](#).

TX_DIG_TBIT22

**Table 12-365. DPHY_TX_DL2_TX_DIG_TBIT22
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0474h |

Figure 12-182. DPHY_TX_DL2_TX_DIG_TBIT22 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-366. DPHY_TX_DL2_TX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT22 | R/W | 0h | spare |

12.183 DPHY_TX_DL2_TX_DIG_TBIT23 Register (Offset = 478h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT23 is shown in [Figure 12-183](#) and described in [Table 12-368](#).

Return to [Summary Table](#).

TX_DIG_TBIT23

**Table 12-367. DPHY_TX_DL2_TX_DIG_TBIT23
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0478h |

Figure 12-183. DPHY_TX_DL2_TX_DIG_TBIT23 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-368. DPHY_TX_DL2_TX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT23 | R | 0h | RESERVED |

12.184 DPHY_TX_DL2_TX_DIG_TBIT24 Register (Offset = 47Ch) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT24 is shown in [Figure 12-184](#) and described in [Table 12-370](#).

Return to [Summary Table](#).

TX_DIG_TBIT24

**Table 12-369. DPHY_TX_DL2_TX_DIG_TBIT24
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 047Ch |

Figure 12-184. DPHY_TX_DL2_TX_DIG_TBIT24 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-370. DPHY_TX_DL2_TX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT24 | R | 0h | RESERVED |

12.185 DPHY_TX_DL2_TX_ANA_TBIT5 Register (Offset = 480h) [reset = 0h]

DPHY_TX_DL2_TX_ANA_TBIT5 is shown in [Figure 12-185](#) and described in [Table 12-372](#).

Return to [Summary Table](#).

TX_ANA_TBIT5

**Table 12-371. DPHY_TX_DL2_TX_ANA_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0480h |

Figure 12-185. DPHY_TX_DL2_TX_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_ANA_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-372. DPHY_TX_DL2_TX_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL2_ANA_TBIT5 | R | 0h | Analog Test register 5 |

12.186 DPHY_TX_DL2_TX_DIG_TBIT25 Register (Offset = 48Ch) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT25 is shown in [Figure 12-186](#) and described in [Table 12-374](#).

Return to [Summary Table](#).

bal and ana_ctrl [DPHY_TX_STATUS](#)

Table 12-373. DPHY_TX_DL2_TX_DIG_TBIT25 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 048Ch |

Figure 12-186. DPHY_TX_DL2_TX_DIG_TBIT25 Register

| | | | | | | | |
|---------------------|----|----|----|------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | DL2_ANA_CTRL_FSM_STATE | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-374. DPHY_TX_DL2_TX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--------------------------------|
| 31-21 | RESERVED | R | X | |
| 20-16 | DL2_ANA_CTRL_FSM_STATE | R | 0h | FSM state readout for ana_ctrl |
| 15-0 | DL2_BIST_BAL_STATUS | R | 0h | BAL logic DPHY_TX_STATUS read |

12.187 DPHY_TX_DL2_TX_DIG_TBIT26 Register (Offset = 490h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT26 is shown in [Figure 12-187](#) and described in [Table 12-376](#).

Return to [Summary Table](#).

fsm states in the design1

**Table 12-375. DPHY_TX_DL2_TX_DIG_TBIT26
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0490h |

Figure 12-187. DPHY_TX_DL2_TX_DIG_TBIT26 Register

| | | | | | | | |
|----------------------------------|----|----|----|----------------------------------|----|----------------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL2_TM_DATA_ESC_RX_FSM_STATE | | | | DL2_TM_DATA_ESCTX_CTRL_FSM_STATE | | | |
| R-0h | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_TM_DATA_ESCTX_CTRL_FSM_STATE | | | | | | DL2_TM_DATA_ESCTX_DATA_FSM_STATE | |
| R-0h | | | | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_TM_DATA_ESCTX_DATA_FSM_STATE | | | | DL2_TM_HS_PATH_FSM_STATE | | | |
| R-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_TM_HS_PATH_FSM_STATE | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-376. DPHY_TX_DL2_TX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--------------------------------------|
| 31-27 | DL2_TM_DATA_ESC_RX_FSM_STATE | R | 0h | FSM state readout for esc rx path |
| 26-17 | DL2_TM_DATA_ESCTX_CTRL_FSM_STATE | R | 0h | fsm state for escape tx control path |
| 16-12 | DL2_TM_DATA_ESCTX_DATA_FSM_STATE | R | 0h | fsm state for escape tx data path |
| 11-0 | DL2_TM_HS_PATH_FSM_STATE | R | 0h | FSM state readout for hs path fsm |

12.188 DPHY_TX_DL2_TX_DIG_TBIT28 Register (Offset = 498h) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT28 is shown in [Figure 12-188](#) and described in [Table 12-378](#).

Return to [Summary Table](#).

lp component DPHY_TX_STATUS

**Table 12-377. DPHY_TX_DL2_TX_DIG_TBIT28
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0498h |

Figure 12-188. DPHY_TX_DL2_TX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_TM_ANA_COMP_OUTS | | | | | | | | DL2_UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-378. DPHY_TX_DL2_TX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---------------------------|
| 31-16 | RESERVED | R | X | |
| 15-8 | DL2_TM_ANA_COMP_OUTS | R | 0h | Analog components outputs |
| 7-0 | DL2_UNUSED_7_0 | R | 0h | RESERVED |

12.189 DPHY_TX_DL2_TX_DIG_TBIT29 Register (Offset = 49Ch) [reset = X]

DPHY_TX_DL2_TX_DIG_TBIT29 is shown in [Figure 12-189](#) and described in [Table 12-380](#).

Return to [Summary Table](#).

bist DPHY_TX_STATUS reg1

**Table 12-379. DPHY_TX_DL2_TX_DIG_TBIT29
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 049Ch |

Figure 12-189. DPHY_TX_DL2_TX_DIG_TBIT29 Register

| | | | | | | | |
|----------------------------|------------------------|---------------------|---------------------------|-------------------|-------------------------|----------------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | DL2_TM_CUR_STATE_ULPTX_CHE | |
| R-X | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_TM_CUR_STATE_ULPRX_CHE | | | DL2_TM_CUR_STATE_LPCD_CHE | | | DL2_TM_CUR_STATE_LPRX_CHE | |
| R-0h | | | R-0h | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL2_TM_CUR_STATE_LPRX_CHE | DL2_TM_CUR_STATE_CTRLR | | | | DL2_BIST_DATA_LANE_PASS | DL2_BIST_LPRX_PASS | DL2_BIST_LPCD_PASS |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_ULPRX_PASS | DL2_BIST_ULPTX_PASS | DL2_BIST_HS_NEG_ERR | DL2_BIST_HS_POS_ERR | DL2_BIST_POS_SYNC | DL2_BIST_NEG_SYNC | DL2_BIST_CM_PLT | DL2_BIST_EN_STATUS |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-380. DPHY_TX_DL2_TX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-26 | RESERVED | R | X | |
| 25-24 | DL2_TM_CUR_STATE_ULPTX_CHE | R | 0h | Current state of the ULPTX checker FSM |
| 23-21 | DL2_TM_CUR_STATE_ULPRX_CHE | R | 0h | Current state of the ULPRX checker FSM |
| 20-18 | DL2_TM_CUR_STATE_LPCD_CHE | R | 0h | Current state of the LPCD checker FSM |
| 17-15 | DL2_TM_CUR_STATE_LPRX_CHE | R | 0h | Current state of the LPRX checker FSM |
| 14-11 | DL2_TM_CUR_STATE_CTRLR | R | 0h | Current state of the Control FSM |
| 10 | DL2_BIST_DATA_LANE_PASS | R | 0h | Data lane has passed BIST completely |
| 9 | DL2_BIST_LPRX_PASS | R | 0h | LPRX BIST pass |
| 8 | DL2_BIST_LPCD_PASS | R | 0h | LPCD BIST Passed |
| 7 | DL2_BIST_ULPRX_PASS | R | 0h | ULPRX BIST passed |
| 6 | DL2_BIST_ULPTX_PASS | R | 0h | ULPTX BIST passed |
| 5 | DL2_BIST_HS_NEG_ERR | R | 0h | HS Bist error detected with negedge of sampler clock |
| 4 | DL2_BIST_HS_POS_ERR | R | 0h | HS Bist error detected with posedge of sampler clock |

Table 12-380. DPHY_TX_DL2_TX_DIG_TBIT29 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 3 | DL2_BIST_POS_SYNC | R | 0h | Pattern checker in negedge run have synced with pattern generator |
| 2 | DL2_BIST_NEG_SYNC | R | 0h | Pattern checker in posedge run have synced with pattern generator |
| 1 | DL2_BIST_CMPLT | R | 0h | BIST is completed |
| 0 | DL2_BIST_EN_STATUS | R | 0h | BIST Controller is enabled |

12.190 DPHY_TX_DL2_TX_DIG_TBIT30 Register (Offset = 4A0h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT30 is shown in [Figure 12-190](#) and described in [Table 12-382](#).

[Return to Summary Table.](#)

bist pkt count values

**Table 12-381. DPHY_TX_DL2_TX_DIG_TBIT30
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04A0h |

Figure 12-190. DPHY_TX_DL2_TX_DIG_TBIT30 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_BIST_PAT_CHE_PKT_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_PAT_CHE_PKT_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-382. DPHY_TX_DL2_TX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-16 | DL2_BIST_PAT_CHE_PKT_CNT_NEG | R | 0h | pattern checker packet count with negedge run of sampler clock |
| 15-0 | DL2_BIST_PAT_CHE_PKT_CNT_POS | R | 0h | pattern checker packet count with posedge run of sampler clock |

12.191 DPHY_TX_DL2_TX_DIG_TBIT31 Register (Offset = 4A4h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT31 is shown in [Figure 12-191](#) and described in [Table 12-384](#).

Return to [Summary Table](#).

bist err count values

Table 12-383. DPHY_TX_DL2_TX_DIG_TBIT31 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04A4h |

Figure 12-191. DPHY_TX_DL2_TX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL2_BIST_PAT_CHE_ERR_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_BIST_PAT_CHE_ERR_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-384. DPHY_TX_DL2_TX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-16 | DL2_BIST_PAT_CHE_ERR_CNT_NEG | R | 0h | pattern checker error count with negedge run of sampler clock |
| 15-0 | DL2_BIST_PAT_CHE_ERR_CNT_POS | R | 0h | pattern checker error count with posedge run of sampler clock |

12.192 DPHY_TX_DL2_TX_DIG_TBIT32 Register (Offset = 4A8h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT32 is shown in [Figure 12-192](#) and described in [Table 12-386](#).

Return to [Summary Table](#).

TX_DIG_TBIT32

**Table 12-385. DPHY_TX_DL2_TX_DIG_TBIT32
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04A8h |

Figure 12-192. DPHY_TX_DL2_TX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-386. DPHY_TX_DL2_TX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT32 | R | 0h | RESERVED |

12.193 DPHY_TX_DL2_TX_DIG_TBIT33 Register (Offset = 4ACh) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT33 is shown in [Figure 12-193](#) and described in [Table 12-388](#).

Return to [Summary Table](#).

TX_DIG_TBIT33

**Table 12-387. DPHY_TX_DL2_TX_DIG_TBIT33
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04ACh |

Figure 12-193. DPHY_TX_DL2_TX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT33 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-388. DPHY_TX_DL2_TX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT33 | R | 0h | RESERVED |

12.194 DPHY_TX_DL2_TX_DIG_TBIT34 Register (Offset = 4B0h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT34 is shown in [Figure 12-194](#) and described in [Table 12-390](#).

Return to [Summary Table](#).

TX_DIG_TBIT34

**Table 12-389. DPHY_TX_DL2_TX_DIG_TBIT34
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04B0h |

Figure 12-194. DPHY_TX_DL2_TX_DIG_TBIT34 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT34 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-390. DPHY_TX_DL2_TX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT34 | R | 0h | RESERVED |

12.195 DPHY_TX_DL2_TX_DIG_TBIT35 Register (Offset = 4B4h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT35 is shown in [Figure 12-195](#) and described in [Table 12-392](#).

Return to [Summary Table](#).

TX_DIG_TBIT35

**Table 12-391. DPHY_TX_DL2_TX_DIG_TBIT35
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04B4h |

Figure 12-195. DPHY_TX_DL2_TX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT35 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-392. DPHY_TX_DL2_TX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT35 | R | 0h | RESERVED |

12.196 DPHY_TX_DL2_TX_DIG_TBIT36 Register (Offset = 4B8h) [reset = 0h]

DPHY_TX_DL2_TX_DIG_TBIT36 is shown in [Figure 12-196](#) and described in [Table 12-394](#).

Return to [Summary Table](#).

TX_DIG_TBIT36

**Table 12-393. DPHY_TX_DL2_TX_DIG_TBIT36
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 04B8h |

Figure 12-196. DPHY_TX_DL2_TX_DIG_TBIT36 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL2_DIG_TBIT36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-394. DPHY_TX_DL2_TX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL2_DIG_TBIT36 | R | 0h | RESERVED |

12.197 DPHY_TX_DL3_TX_ANA_TBIT0 Register (Offset = 500h) [reset = 0h]

DPHY_TX_DL3_TX_ANA_TBIT0 is shown in [Figure 12-197](#) and described in [Table 12-396](#).

Return to [Summary Table](#).

TX_ANA_TBIT0

Table 12-395. DPHY_TX_DL3_TX_ANA_TBIT0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0500h |

Figure 12-197. DPHY_TX_DL3_TX_ANA_TBIT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_ANA_TBIT0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-396. DPHY_TX_DL3_TX_ANA_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL3_ANA_TBIT0 | R/W | 0h | Analog Test register 0 |

12.198 DPHY_TX_DL3_TX_ANA_TBIT1 Register (Offset = 504h) [reset = 0h]

DPHY_TX_DL3_TX_ANA_TBIT1 is shown in [Figure 12-198](#) and described in [Table 12-398](#).

Return to [Summary Table](#).

TX_ANA_TBIT1

**Table 12-397. DPHY_TX_DL3_TX_ANA_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0504h |

Figure 12-198. DPHY_TX_DL3_TX_ANA_TBIT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_ANA_TBIT1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-398. DPHY_TX_DL3_TX_ANA_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL3_ANA_TBIT1 | R/W | 0h | Analog Test register 1 |

12.199 DPHY_TX_DL3_TX_ANA_TBIT2 Register (Offset = 508h) [reset = 0h]

DPHY_TX_DL3_TX_ANA_TBIT2 is shown in [Figure 12-199](#) and described in [Table 12-400](#).

Return to [Summary Table](#).

TX_ANA_TBIT2

**Table 12-399. DPHY_TX_DL3_TX_ANA_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0508h |

Figure 12-199. DPHY_TX_DL3_TX_ANA_TBIT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_ANA_TBIT2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-400. DPHY_TX_DL3_TX_ANA_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL3_ANA_TBIT2 | R/W | 0h | Analog Test register 2 |

12.200 DPHY_TX_DL3_TX_ANA_TBIT3 Register (Offset = 50Ch) [reset = 0h]

DPHY_TX_DL3_TX_ANA_TBIT3 is shown in [Figure 12-200](#) and described in [Table 12-402](#).

Return to [Summary Table](#).

TX_ANA_TBIT3

**Table 12-401. DPHY_TX_DL3_TX_ANA_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 050Ch |

Figure 12-200. DPHY_TX_DL3_TX_ANA_TBIT3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_ANA_TBIT3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-402. DPHY_TX_DL3_TX_ANA_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL3_ANA_TBIT3 | R/W | 0h | Analog Test register 3 |

12.201 DPHY_TX_DL3_TX_ANA_TBIT4 Register (Offset = 510h) [reset = 0h]

DPHY_TX_DL3_TX_ANA_TBIT4 is shown in [Figure 12-201](#) and described in [Table 12-404](#).

Return to [Summary Table](#).

TX_ANA_TBIT4

**Table 12-403. DPHY_TX_DL3_TX_ANA_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0510h |

Figure 12-201. DPHY_TX_DL3_TX_ANA_TBIT4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_ANA_TBIT4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-404. DPHY_TX_DL3_TX_ANA_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL3_ANA_TBIT4 | R/W | 0h | Analog Test register 4 |

12.202 DPHY_TX_DL3_TX_DIG_TBIT0 Register (Offset = 51Ch) [reset = 606h]

DPHY_TX_DL3_TX_DIG_TBIT0 is shown in [Figure 12-202](#) and described in [Table 12-406](#).

Return to [Summary Table](#).

ana_ctrl_counter_values

**Table 12-405. DPHY_TX_DL3_TX_DIG_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 051Ch |

Figure 12-202. DPHY_TX_DL3_TX_DIG_TBIT0 Register

| | | | | | | | |
|------------------|----|----|----|---------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL3_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_UNUSED_31_13 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_UNUSED_31_13 | | | | DL3_ULPS_PULLDN_CNT | | | |
| R-0h | | | | R/W-6h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_UNUSED_7_5 | | | | DL3_LDO_EN_CNT | | | |
| R-0h | | | | R/W-6h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-406. DPHY_TX_DL3_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|---|
| 31-13 | DL3_UNUSED_31_13 | R | 0h | RESERVED |
| 12-8 | DL3_ULPS_PULLDN_CNT | R/W | 6h | After enabling LDO, ulps_pulldn will go to 0 after these many uS |
| 7-5 | DL3_UNUSED_7_5 | R | 0h | RESERVED |
| 4-0 | DL3_LDO_EN_CNT | R/W | 6h | Once the analog's power down signal is de asserted, LDO will be enabled after these many uS |

12.203 DPHY_TX_DL3_TX_DIG_TBIT1 Register (Offset = 520h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT1 is shown in [Figure 12-203](#) and described in [Table 12-408](#).

Return to [Summary Table](#).

Register TX_DIG_TBIT1

**Table 12-407. DPHY_TX_DL3_TX_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0520h |

Figure 12-203. DPHY_TX_DL3_TX_DIG_TBIT1 Register

| | | | | | | | |
|---------------------|----|-------------------|-------------------|--------------------|------------------------|---------------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | DL3_TEST_LP_TX_DP | DL3_TEST_LP_TX_DN | DL3_TEST_LP_TX_EN | DL3_TM_READ_Y_SKEW_CAL | DL3_TM_HS_PREP_HAF_CYC_OVERRIDE | DL3_TM_HS_PREP_HSF_CYC |
| R/W-X | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_HS_TRAIL_OFFSET | | | | DL3_HS_ZERO_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_HS_PREP_OFFSET | | | | DL3_HS_TLPX_OFFSET | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-408. DPHY_TX_DL3_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------------|------|-------|---|
| 31-22 | RESERVED | R/W | X | |
| 21 | DL3_TEST_LPTX_DP | R/W | 0h | send 0 to LP TX Dn in HS mode |
| 20 | DL3_TEST_LPTX_DN | R/W | 0h | send 0 to LP TX Dp in HS mode |
| 19 | DL3_TEST_LPTX_EN | R/W | 0h | give output for LPTX from dig logic for HS entry LP sequence |
| 18 | DL3_TM_READY_SKEW_CAL | R/W | 0h | Assert o_TxReadyHS during skew calibration pattern transmission. |
| 17 | DL3_TM_HS_PREP_HAF_CYC_OVERRIDE | R/W | 0h | HS Prepare extra half cycle offset is controlled by digital logic |
| 16 | DL3_TM_HS_PREP_HSF_CYC | R/W | 0h | If bit 17 == 1 Sets HS Prepare extra offset to 0 half cycle |
| 15-12 | DL3_HS_TRAIL_OFFSET | R/W | 0h | Sets HS-TRAIL Offset to 0 |
| 11-8 | DL3_HS_ZERO_OFFSET | R/W | 0h | Sets HS-ZERO offset to 0 |
| 7-4 | DL3_HS_PREP_OFFSET | R/W | 0h | Sets HS-PREPARE offset to 0 |
| 3-0 | DL3_HS_TLPX_OFFSET | R/W | 0h | Sets TLPX Offset to 0 |

12.204 DPHY_TX_DL3_TX_DIG_TBIT2 Register (Offset = 524h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT2 is shown in [Figure 12-204](#) and described in [Table 12-410](#).

Return to [Summary Table](#).

test modes for during hs mode

**Table 12-409. DPHY_TX_DL3_TX_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0524h |

Figure 12-204. DPHY_TX_DL3_TX_DIG_TBIT2 Register

| | | | | | | | |
|--------------------------|----|----|----|----|-------------------------|------------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | DL3_TM_SKEW_CAL_SEQ | | |
| R/W-X | | | | | R/W-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_TM_SKEW_CAL_SEQ | | | | | DL3_TM_SKEW_CAL_SEQ_SEL | DL3_TM_SKEW_CAL_SYNC_PKT | |
| R/W-0h | | | | | R/W-0h | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_TM_SKEW_CAL_SYNC_PKT | | | | | | DL3_TM_SKEW_CAL_SYNC_PKT_SEL | DL3_TM_HS_SYNC_PKT |
| R/W-0h | | | | | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_TM_HS_SYNC_PKT | | | | | | | DL3_TM_HS_SYNC_PKT_SEL |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-410. DPHY_TX_DL3_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-27 | RESERVED | R/W | X | |
| 26-19 | DL3_TM_SKEW_CAL_SEQ | R/W | 0h | desired skew calibration test sequence |
| 18 | DL3_TM_SKEW_CAL_SEQ_SEL | R/W | 0h | To send 'AA as skew calibration pattern |
| 17-10 | DL3_TM_SKEW_CAL_SYNC_PKT | R/W | 0h | desired skew calibration test sync packet |
| 9 | DL3_TM_SKEW_CAL_SYNC_PKT_SEL | R/W | 0h | To send 'FF as Skew calibration sync packet |
| 8-1 | DL3_TM_HS_SYNC_PKT | R/W | 0h | desired HS test sync packet |
| 0 | DL3_TM_HS_SYNC_PKT_SEL | R/W | 0h | To send 'B8 as HS sync packet |

12.205 DPHY_TX_DL3_TX_DIG_TBIT3 Register (Offset = 528h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT3 is shown in [Figure 12-205](#) and described in [Table 12-412](#).

Return to [Summary Table](#).

tm_sersynth

Table 12-411. DPHY_TX_DL3_TX_DIG_TBIT3 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0528h |

Figure 12-205. DPHY_TX_DL3_TX_DIG_TBIT3 Register

| | | | | | | | |
|----------|----|-----------------------|---------------------|----|----|------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | DL3_SERSYNTH_LOOPBACK | DL3_BAL_FORCE_STATE | | | DL3_BAL_FORCE_EN | RESERVED |
| R/W-X | | R/W-0h | R/W-0h | | | R/W-0h | R/W-X |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-412. DPHY_TX_DL3_TX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5 | DL3_SERSYNTH_LOOPBACK | R/W | 0h | De-serialiser will take input from sampler |
| 4-2 | DL3_BAL_FORCE_STATE | R/W | 0h | Force the SYNC packet detection logic into below states if <1> is '1', SYNC_DONE state |
| 1 | DL3_BAL_FORCE_EN | R/W | 0h | SYNC packet detection FSM in serialiser in BIST mode will work as per logic |
| 0 | RESERVED | R/W | X | |

12.206 DPHY_TX_DL3_TX_DIG_TBIT4 Register (Offset = 52Ch) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT4 is shown in [Figure 12-206](#) and described in [Table 12-414](#).

Return to [Summary Table](#).

lp test logic

**Table 12-413. DPHY_TX_DL3_TX_DIG_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 052Ch |

Figure 12-206. DPHY_TX_DL3_TX_DIG_TBIT4 Register

| | | | | | | | |
|--------------------|------------------|----|-------------------|---------------------------|---------------------------|-------------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_CONTENTION_EN | DL3_UNUSED_14_13 | | DL3_FORCE_RX_MODE | DL3_TEST_DATA_LPTX_DP_SEL | DL3_TEST_DATA_LPTX_DN_SEL | DL3_TEST_DATA_LPTX | |
| R/W-0h | R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_TEST_DATA_LPTX | | | | | | DL3_TEST_DATA_LPTX_RSTN | DL3_TEST_DATA_LPTX_EN |
| R/W-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-414. DPHY_TX_DL3_TX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---------------------------------------|
| 31-16 | RESERVED | R/W | X | |
| 15 | DL3_CONTENTION_EN | R/W | 0h | Contention detector logic is enabled |
| 14-13 | DL3_UNUSED_14_13 | R | 0h | RESERVED |
| 12 | DL3_FORCE_RX_MODE | R/W | 0h | Force LPRX into RX mode |
| 11 | DL3_TEST_DATA_LPTX_DP_SEL | R/W | 0h | Normal_ LPTX DP_B from logic for LPDT |
| 10 | DL3_TEST_DATA_LPTX_DN_SEL | R/W | 0h | Normal_ LPTX DN_B from logic for LPDT |
| 9-2 | DL3_TEST_DATA_LPTX | R/W | 0h | LPTX test data |
| 1 | DL3_TEST_DATA_LPTX_RSTN | R/W | 0h | LP test data logic is RESET |
| 0 | DL3_TEST_DATA_LPTX_EN | R/W | 0h | LP test data logic DISABLED |

12.207 DPHY_TX_DL3_TX_DIG_TBIT5 Register (Offset = 530h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT5 is shown in [Figure 12-207](#) and described in [Table 12-416](#).

Return to [Summary Table](#).

TX_DIG_TBIT5

**Table 12-415. DPHY_TX_DL3_TX_DIG_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0530h |

Figure 12-207. DPHY_TX_DL3_TX_DIG_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-416. DPHY_TX_DL3_TX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT5 | R | 0h | RESERVED |

12.208 DPHY_TX_DL3_TX_DIG_TBIT6 Register (Offset = 534h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT6 is shown in [Figure 12-208](#) and described in [Table 12-418](#).

Return to [Summary Table](#).

TX_DIG_TBIT6

**Table 12-417. DPHY_TX_DL3_TX_DIG_TBIT6
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0534h |

Figure 12-208. DPHY_TX_DL3_TX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-418. DPHY_TX_DL3_TX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT6 | R | 0h | RESERVED |

12.209 DPHY_TX_DL3_TX_DIG_TBIT7 Register (Offset = 538h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT7 is shown in [Figure 12-209](#) and described in [Table 12-420](#).

Return to [Summary Table](#).

TX_DIG_TBIT7

**Table 12-419. DPHY_TX_DL3_TX_DIG_TBIT7
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0538h |

Figure 12-209. DPHY_TX_DL3_TX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-420. DPHY_TX_DL3_TX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT7 | R | 0h | RESERVED |

12.210 DPHY_TX_DL3_TX_DIG_TBIT8 Register (Offset = 53Ch) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT8 is shown in [Figure 12-210](#) and described in [Table 12-422](#).

Return to [Summary Table](#).

TX_DIG_TBIT8

**Table 12-421. DPHY_TX_DL3_TX_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 053Ch |

Figure 12-210. DPHY_TX_DL3_TX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-422. DPHY_TX_DL3_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT8 | R | 0h | RESERVED |

12.211 DPHY_TX_DL3_TX_DIG_TBIT9 Register (Offset = 540h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT9 is shown in [Figure 12-211](#) and described in [Table 12-424](#).

Return to [Summary Table](#).

TX_DIG_TBIT9

**Table 12-423. DPHY_TX_DL3_TX_DIG_TBIT9
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0540h |

Figure 12-211. DPHY_TX_DL3_TX_DIG_TBIT9 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-424. DPHY_TX_DL3_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT9 | R | 0h | RESERVED |

12.212 DPHY_TX_DL3_TX_DIG_TBIT10 Register (Offset = 544h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT10 is shown in [Figure 12-212](#) and described in [Table 12-426](#).

Return to [Summary Table](#).

bist_reg1

**Table 12-425. DPHY_TX_DL3_TX_DIG_TBIT10
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0544h |

Figure 12-212. DPHY_TX_DL3_TX_DIG_TBIT10 Register

| | | | | | | | |
|---------------------------|----|----|----|--------------------------|----|----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | DL3_BIST_WAIT_TIME |
| R/W-X | | | | | | | R/W-4h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_BIST_WAIT_TIME | | | | DL3_BIST_ULPTX_TEST_TIME | | | |
| R/W-4h | | | | R/W-40h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_BIST_ULPTX_TEST_TIME | | | | DL3_BIST_SEND_CONFIG | | DL3_BIST_DIG_TO_DIG_LOOPBK | DL3_BIST_RUN_NEGEDGE_FIRST |
| R/W-40h | | | | R/W-0h | | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_LENGTH_OF_DESKEW | | | | | | DL3_BIST_LOOPBK_MODE | DL3_BIST_EN |
| R/W-Bh | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-426. DPHY_TX_DL3_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24-21 | DL3_BIST_WAIT_TIME | R/W | 4h | BIST wait time between posedge run and negedge run of sampler clock |
| 20-13 | DL3_BIST_ULPTX_TEST_TIME | R/W | 40h | While testing ULPTX, LP00 will be maintained on DPDN for this many number of byte clock cycles |
| 12-11 | DL3_BIST_SEND_CONFIG | R/W | 0h | Option of configuring what to send in BIST mose. To send both deskew and HS data |
| 10 | DL3_BIST_DIG_TO_DIG_LOOPBK | R/W | 0h | main digital to pattern checker loopback enabled |
| 9 | DL3_BIST_RUN_NEGEDGE_FIRST | R/W | 0h | BIST will run with posedge of sampler clock first |
| 8-2 | DL3_BIST_LENGTH_OF_DESKEW | R/W | Bh | Length of deskew sequence In terms of us. By default 13us of deskew sequence will be transmitted |
| 1 | DL3_BIST_LOOPBK_MODE | R/W | 0h | loopback_mode bit, EXTERNAL_LOOPBACK |
| 0 | DL3_BIST_EN | R/W | 0h | BIST Disabled |

12.213 DPHY_TX_DL3_TX_DIG_TBIT11 Register (Offset = 548h) [reset = 0F0501B0h]

DPHY_TX_DL3_TX_DIG_TBIT11 is shown in [Figure 12-213](#) and described in [Table 12-428](#).

Return to [Summary Table](#).

bist_reg2

Table 12-427. DPHY_TX_DL3_TX_DIG_TBIT11 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0548h |

Figure 12-213. DPHY_TX_DL3_TX_DIG_TBIT11 Register

| | | | | | | | |
|------------------------|------------------|---------------|----|--------------------|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL3_BIST_FRM_IDLE_TIME | | | | | | | |
| R/W-Fh | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_BIST_PKT_NUM | | | | | | | |
| R/W-5h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_BIST_INF_MODE | DL3_BIST_FRM_NUM | | | | | | |
| R/W-0h | R/W-3h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_FRM_NUM | DL3_BIST_CLEAR | DL3_BIST_PRBS | | DL3_BIST_TEST_MODE | | | DL3_UNUSED_0 |
| R/W-3h | R/W-0h | R/W-3h | | R/W-0h | | | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-428. DPHY_TX_DL3_TX_DIG_TBIT11 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-24 | DL3_BIST_FRM_IDLE_TIME | R/W | Fh | BIST_FRM_IDLE time is time between the frames |
| 23-16 | DL3_BIST_PKT_NUM | R/W | 5h | BIST_PAK_NUM is number of packets that are to be transmitted per frame |
| 15 | DL3_BIST_INF_MODE | R/W | 0h | run infinite BIST mode |
| 14-7 | DL3_BIST_FRM_NUM | R/W | 3h | BIST_FRM_NUM is number of frames to be transmitted |
| 6 | DL3_BIST_CLEAR | R/W | 0h | clear the bist |
| 5-4 | DL3_BIST_PRBS | R/W | 3h | BIST PRBS MODE 9 |
| 3-1 | DL3_BIST_TEST_MODE | R/W | 0h | PRBS mode |
| 0 | DL3_UNUSED_0 | R | 0h | RESERVED |

12.214 DPHY_TX_DL3_TX_DIG_TBIT12 Register (Offset = 54Ch) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT12 is shown in [Figure 12-214](#) and described in [Table 12-430](#).

Return to [Summary Table](#).

bist_reg3

**Table 12-429. DPHY_TX_DL3_TX_DIG_TBIT12
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 054Ch |

Figure 12-214. DPHY_TX_DL3_TX_DIG_TBIT12 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|---------------------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | DL3_BIST_RUN_LENGTH | | | | | | | | | | | |
| R/W-X | | | | R/W-28h | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-430. DPHY_TX_DL3_TX_DIG_TBIT12 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------|------|-------|-----------------|
| 31-12 | RESERVED | R/W | X | |
| 11-0 | DL3_BIST_RUN_LENGTH | R/W | 28h | BIST_RUN_LENGTH |

12.215 DPHY_TX_DL3_TX_DIG_TBIT13 Register (Offset = 550h) [reset = Ah]

DPHY_TX_DL3_TX_DIG_TBIT13 is shown in [Figure 12-215](#) and described in [Table 12-432](#).

Return to [Summary Table](#).

bist_reg4

**Table 12-431. DPHY_TX_DL3_TX_DIG_TBIT13
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0550h |

Figure 12-215. DPHY_TX_DL3_TX_DIG_TBIT13 Register

| | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_UNUSED_31_8 | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_UNUSED_31_8 | | | | | | | | DL3_BIST_IDLE_TIME | | | | | | | |
| R-0h | | | | | | | | R/W-Ah | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-432. DPHY_TX_DL3_TX_DIG_TBIT13 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|----------------|
| 31-8 | DL3_UNUSED_31_8 | R | 0h | RESERVED |
| 7-0 | DL3_BIST_IDLE_TIME | R/W | Ah | BIST_IDLE_TIME |

12.216 DPHY_TX_DL3_TX_DIG_TBIT14 Register (Offset = 554h) [reset = DECDBCABh]

DPHY_TX_DL3_TX_DIG_TBIT14 is shown in [Figure 12-216](#) and described in [Table 12-434](#).

[Return to Summary Table.](#)

bist_reg5

**Table 12-433. DPHY_TX_DL3_TX_DIG_TBIT14
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0554h |

Figure 12-216. DPHY_TX_DL3_TX_DIG_TBIT14 Register

| | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_BIST_PKT4 | | | | | | | | DL3_BIST_PKT3 | | | | | | | |
| R/W-DEh | | | | | | | | R/W-CDh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_PKT2 | | | | | | | | DL3_BIST_PKT1 | | | | | | | |
| R/W-BCh | | | | | | | | R/W-ABh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-434. DPHY_TX_DL3_TX_DIG_TBIT14 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|----------------|
| 31-24 | DL3_BIST_PKT4 | R/W | DEh | BIST_TEST_PAT4 |
| 23-16 | DL3_BIST_PKT3 | R/W | CDh | BIST_TEST_PAT3 |
| 15-8 | DL3_BIST_PKT2 | R/W | BCh | BIST_TEST_PAT2 |
| 7-0 | DL3_BIST_PKT1 | R/W | ABh | BIST_TEST_PAT1 |

12.217 DPHY_TX_DL3_TX_DIG_TBIT15 Register (Offset = 558h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT15 is shown in [Figure 12-217](#) and described in [Table 12-436](#).

Return to [Summary Table](#).

bist_reg6

**Table 12-435. DPHY_TX_DL3_TX_DIG_TBIT15
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0558h |

Figure 12-217. DPHY_TX_DL3_TX_DIG_TBIT15 Register

| | | | | | | | |
|------------------------|----|----------------------|------------------------|----|----|----|---------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | DL3_BIST_LFSR_FREEZE | DL3_BIST_ERR_INJ_POINT | | | | |
| R/W-X | | R/W-0h | R/W-14h | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_ERR_INJ_POINT | | | | | | | DL3_BIST_ERR_INJ_EN |
| R/W-14h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-436. DPHY_TX_DL3_TX_DIG_TBIT15 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| 31-14 | RESERVED | R/W | X | |
| 13 | DL3_BIST_LFSR_FREEZE | R/W | 0h | Reset LFSR contents after every packet or frame |
| 12-1 | DL3_BIST_ERR_INJ_POINT | R/W | 14h | BIST_ERR_INJECT_POINT is where to inject the error in the packet |
| 0 | DL3_BIST_ERR_INJ_EN | R/W | 0h | Inject error in the BIST during the packet |

12.218 DPHY_TX_DL3_TX_DIG_TBIT16 Register (Offset = 55Ch) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT16 is shown in [Figure 12-218](#) and described in [Table 12-438](#).

Return to [Summary Table](#).

TX_DIG_TBIT16

**Table 12-437. DPHY_TX_DL3_TX_DIG_TBIT16
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 055Ch |

Figure 12-218. DPHY_TX_DL3_TX_DIG_TBIT16 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-438. DPHY_TX_DL3_TX_DIG_TBIT16 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT16 | R | 0h | RESERVED |

12.219 DPHY_TX_DL3_TX_DIG_TBIT17 Register (Offset = 560h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT17 is shown in [Figure 12-219](#) and described in [Table 12-440](#).

Return to [Summary Table](#).

TX_DIG_TBIT17

**Table 12-439. DPHY_TX_DL3_TX_DIG_TBIT17
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0560h |

Figure 12-219. DPHY_TX_DL3_TX_DIG_TBIT17 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT17 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-440. DPHY_TX_DL3_TX_DIG_TBIT17 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT17 | R | 0h | RESERVED |

12.220 DPHY_TX_DL3_TX_DIG_TBIT18 Register (Offset = 564h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT18 is shown in [Figure 12-220](#) and described in [Table 12-442](#).

Return to [Summary Table](#).

TX_DIG_TBIT18

**Table 12-441. DPHY_TX_DL3_TX_DIG_TBIT18
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0564h |

Figure 12-220. DPHY_TX_DL3_TX_DIG_TBIT18 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT18 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-442. DPHY_TX_DL3_TX_DIG_TBIT18 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT18 | R | 0h | RESERVED |

12.221 DPHY_TX_DL3_TX_DIG_TBIT19 Register (Offset = 568h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT19 is shown in [Figure 12-221](#) and described in [Table 12-444](#).

Return to [Summary Table](#).

TX_DIG_TBIT19

**Table 12-443. DPHY_TX_DL3_TX_DIG_TBIT19
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0568h |

Figure 12-221. DPHY_TX_DL3_TX_DIG_TBIT19 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT19 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-444. DPHY_TX_DL3_TX_DIG_TBIT19 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT19 | R | 0h | RESERVED |

12.222 DPHY_TX_DL3_TX_DIG_TBIT20 Register (Offset = 56Ch) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT20 is shown in [Figure 12-222](#) and described in [Table 12-446](#).

Return to [Summary Table](#).

digital to analog signal muxing

**Table 12-445. DPHY_TX_DL3_TX_DIG_TBIT20
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 056Ch |

Figure 12-222. DPHY_TX_DL3_TX_DIG_TBIT20 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------|------------------------|-----------------------|-------------------|---------------------------------|-----------------------------|-----------------------|-------------------|
| DL3_TM_ISO_EN | DL3_TM_LOAD_DPDN_SEL | DL3_TM_LOAD_DPDN | | | DL3_TM_HSTX_DATA_RATE_SEL | DL3_TM_HSTX_DATE_RATE | |
| R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_TM_BIST_ULP_RCV_EN_SEL | DL3_TM_BIST_ULP_RCV_EN | DL3_TM_ULPS_PULDN_SEL | DL3_TM_ULPS_PULDN | DL3_TM_BIST_SMPLR_CLK_E_DGE_SEL | DL3_TM_BIST_SMPLR_CLK_E_DGE | DL3_TM_BIST_EN_SEL | DL3_TM_BIST_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_TM_LPTX_TRST_SEL | DL3_TM_LPTX_TRST | DL3_TM_LPTX_RST_SEL | DL3_TM_LPTX_RST | DL3_TM_LPTX_DP_SEL | DL3_TM_LPTX_DP | DL3_TM_LPTX_DN_SEL | DL3_TM_LPTX_DN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_TM_LDO_REF_EN_SEL | DL3_TM_LDO_REF_EN | DL3_TM_HSTX_TRST_SEL | DL3_TM_HSTX_TRST | DL3_TM_HSTX_RQST_SEL | DL3_TM_HSTX_RQST | DL3_TM_GLOB_AL_PD_SEL | DL3_TM_GLOB_AL_PD |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-446. DPHY_TX_DL3_TX_DIG_TBIT20 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------------|------|-------|---|
| 31 | DL3_TM_ISO_EN | R/W | 0h | Enable isolation in test mode |
| 30 | DL3_TM_LOAD_DPDN_SEL | R/W | 0h | Take ana_dpdn_load from dig logic |
| 29-27 | DL3_TM_LOAD_DPDN | R/W | 0h | set ana_dpdn_load as per requirement in test mode |
| 26 | DL3_TM_HSTX_DATA_RATE_SEL | R/W | 0h | Take ana_hstx_datarate from dig logic |
| 25-24 | DL3_TM_HSTX_DATE_RATE | R/W | 0h | set ana_hstx_datarate as per requirement in test mode |
| 23 | DL3_TM_BIST_ULP_RCV_EN_SEL | R/W | 0h | Take ana_bist_ulps_rcv_en from dig logic |
| 22 | DL3_TM_BIST_ULP_RCV_EN | R/W | 0h | set ana_bist_ulps_rcv_en to 0 |
| 21 | DL3_TM_ULPS_PULDN_SEL | R/W | 0h | Take ana_ulps_puldn from dig logic |
| 20 | DL3_TM_ULPS_PULDN | R/W | 0h | set ana_ulps_puldn to 0 |
| 19 | DL3_TM_BIST_SMPLR_CLK_EDGE_SEL | R/W | 0h | Take ana_bist_smplr_clkedge from dig logic |
| 18 | DL3_TM_BIST_SMPLR_CLK_EDGE | R/W | 0h | set ana_bist_smplr_clkedge to posedge |

Table 12-446. DPHY_TX_DL3_TX_DIG_TBIT20 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|--|
| 17 | DL3_TM_BIST_EN_SEL | R/W | 0h | Take ana_bist_en from dig logic |
| 16 | DL3_TM_BIST_EN | R/W | 0h | set ana_bist_en to 0 |
| 15 | DL3_TM_LPTX_TRST_SEL | R/W | 0h | Take ana_lptx_trst from dig logic |
| 14 | DL3_TM_LPTX_TRST | R/W | 0h | set ana_lptx_trst to 0 |
| 13 | DL3_TM_LPTX_RST_SEL | R/W | 0h | Take ana_lptx_rst from dig logic |
| 12 | DL3_TM_LPTX_RST | R/W | 0h | set ana_lptx_rst to 0 |
| 11 | DL3_TM_LPTX_DP_SEL | R/W | 0h | give output for LPTX DP from dig logic |
| 10 | DL3_TM_LPTX_DP | R/W | 0h | send 0 to LP TX Dp |
| 9 | DL3_TM_LPTX_DN_SEL | R/W | 0h | give output for LPTX DN from dig logic |
| 8 | DL3_TM_LPTX_DN | R/W | 0h | send 0 to LP TX Dn |
| 7 | DL3_TM_LDO_REF_EN_SEL | R/W | 0h | Take ana_ldo_ref_en from dig logic |
| 6 | DL3_TM_LDO_REF_EN | R/W | 0h | set ana_ldo_ref_en to 0 |
| 5 | DL3_TM_HSTX_TRST_SEL | R/W | 0h | Take ana_hstx_trst from dig logic |
| 4 | DL3_TM_HSTX_TRST | R/W | 0h | set ana_hstx_trst to 0 |
| 3 | DL3_TM_HSTX_RQST_SEL | R/W | 0h | Take ana_hstx_rqst from dig logic |
| 2 | DL3_TM_HSTX_RQST | R/W | 0h | set ana_hstx_rqst to 0 |
| 1 | DL3_TM_GLOBAL_PD_SEL | R/W | 0h | Take ana_global_pd from dig logic |
| 0 | DL3_TM_GLOBAL_PD | R/W | 0h | set ana_global_pd to 0 (powered up) |

12.223 DPHY_TX_DL3_TX_DIG_TBIT21 Register (Offset = 570h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT21 is shown in [Figure 12-223](#) and described in [Table 12-448](#).

[Return to Summary Table.](#)

digital to analog signals test muxing

**Table 12-447. DPHY_TX_DL3_TX_DIG_TBIT21
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0570h |

Figure 12-223. DPHY_TX_DL3_TX_DIG_TBIT21 Register

| | | | | | | | |
|-------------------|---------------------------|-----------------------|----------------------|---------------------|------------------------|--------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | DL3_TM_SERSYNTH_RST_N_SEL | DL3_TM_SERSYNTH_RST_N | DL3_TM_SWAP_DPDN_SEL | DL3_TM_SWAP_DPDN_EN | DL3_TM_SERSYNTH_EN_SEL | DL3_TM_SERSYNTH_EN | DL3_TM_TX_DATA_HS_SEL |
| R/W-X | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_TM_TX_DATA_HS | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-448. DPHY_TX_DL3_TX_DIG_TBIT21 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | DL3_TM_SERSYNTH_RST_N_SEL | R/W | 0h | Take sersynth_rst_n from dig logic |
| 13 | DL3_TM_SERSYNTH_RST_N | R/W | 0h | Set sersynth_rst_n to 1 |
| 12 | DL3_TM_SWAP_DPDN_SEL | R/W | 0h | Take swapdp_dn from dig logic |
| 11 | DL3_TM_SWAP_DPDN_EN | R/W | 0h | Set swap_dpdn to 1 |
| 10 | DL3_TM_SERSYNTH_EN_SEL | R/W | 0h | Take sersynth_en from dig logic |
| 9 | DL3_TM_SERSYNTH_EN | R/W | 0h | set sersynth_en to 1 |
| 8 | DL3_TM_TX_DATA_HS_SEL | R/W | 0h | sends single test byte to sersynth, which is in <7:0> |
| 7-0 | DL3_TM_TX_DATA_HS | R/W | 0h | Test byte that can be sent constantly to sersynth. This is validated by bit <8> of this reg |

12.224 DPHY_TX_DL3_TX_DIG_TBIT22 Register (Offset = 574h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT22 is shown in [Figure 12-224](#) and described in [Table 12-450](#).

Return to [Summary Table](#).

TX_DIG_TBIT22

Table 12-449. DPHY_TX_DL3_TX_DIG_TBIT22 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0574h |

Figure 12-224. DPHY_TX_DL3_TX_DIG_TBIT22 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT22 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-450. DPHY_TX_DL3_TX_DIG_TBIT22 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT22 | R/W | 0h | spare |

12.225 DPHY_TX_DL3_TX_DIG_TBIT23 Register (Offset = 578h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT23 is shown in [Figure 12-225](#) and described in [Table 12-452](#).

Return to [Summary Table](#).

TX_DIG_TBIT23

**Table 12-451. DPHY_TX_DL3_TX_DIG_TBIT23
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0578h |

Figure 12-225. DPHY_TX_DL3_TX_DIG_TBIT23 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT23 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-452. DPHY_TX_DL3_TX_DIG_TBIT23 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT23 | R | 0h | RESERVED |

12.226 DPHY_TX_DL3_TX_DIG_TBIT24 Register (Offset = 57Ch) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT24 is shown in [Figure 12-226](#) and described in [Table 12-454](#).

Return to [Summary Table](#).

TX_DIG_TBIT24

Table 12-453. DPHY_TX_DL3_TX_DIG_TBIT24 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 057Ch |

Figure 12-226. DPHY_TX_DL3_TX_DIG_TBIT24 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT24 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-454. DPHY_TX_DL3_TX_DIG_TBIT24 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT24 | R | 0h | RESERVED |

12.227 DPHY_TX_DL3_TX_ANA_TBIT5 Register (Offset = 580h) [reset = 0h]

DPHY_TX_DL3_TX_ANA_TBIT5 is shown in [Figure 12-227](#) and described in [Table 12-456](#).

Return to [Summary Table](#).

TX_ANA_TBIT5

**Table 12-455. DPHY_TX_DL3_TX_ANA_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0580h |

Figure 12-227. DPHY_TX_DL3_TX_ANA_TBIT5 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_ANA_TBIT5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-456. DPHY_TX_DL3_TX_ANA_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | DL3_ANA_TBIT5 | R | 0h | Analog Test register 5 |

12.228 DPHY_TX_DL3_TX_DIG_TBIT25 Register (Offset = 58Ch) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT25 is shown in [Figure 12-228](#) and described in [Table 12-458](#).

Return to [Summary Table](#).

bal and ana_ctrl DPHY_TX_STATUS

Table 12-457. DPHY_TX_DL3_TX_DIG_TBIT25 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 058Ch |

Figure 12-228. DPHY_TX_DL3_TX_DIG_TBIT25 Register

| | | | | | | | |
|---------------------|----|----|----|------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | DL3_ANA_CTRL_FSM_STATE | | | |
| R-X | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_BAL_STATUS | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-458. DPHY_TX_DL3_TX_DIG_TBIT25 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--------------------------------|
| 31-21 | RESERVED | R | X | |
| 20-16 | DL3_ANA_CTRL_FSM_STATE | R | 0h | FSM state readout for ana_ctrl |
| 15-0 | DL3_BIST_BAL_STATUS | R | 0h | BAL logic DPHY_TX_STATUS read |

12.229 DPHY_TX_DL3_TX_DIG_TBIT26 Register (Offset = 590h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT26 is shown in [Figure 12-229](#) and described in [Table 12-460](#).

Return to [Summary Table](#).

fsm states in the design1

**Table 12-459. DPHY_TX_DL3_TX_DIG_TBIT26
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0590h |

Figure 12-229. DPHY_TX_DL3_TX_DIG_TBIT26 Register

| | | | | | | | |
|----------------------------------|----|----|----|----|----------------------------------|----|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DL3_TM_DATA_ESC_RX_FSM_STATE | | | | | DL3_TM_DATA_ESCTX_CTRL_FSM_STATE | | |
| R-0h | | | | | R-0h | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_TM_DATA_ESCTX_CTRL_FSM_STATE | | | | | | | DL3_TM_DATA_ESCTX_DATA_FSM_STATE |
| R-0h | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_TM_DATA_ESCTX_DATA_FSM_STATE | | | | | DL3_TM_HS_PATH_FSM_STATE | | |
| R-0h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_TM_HS_PATH_FSM_STATE | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-460. DPHY_TX_DL3_TX_DIG_TBIT26 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------------|------|-------|--------------------------------------|
| 31-27 | DL3_TM_DATA_ESC_RX_FSM_STATE | R | 0h | FSM state readout for esc rx path |
| 26-17 | DL3_TM_DATA_ESCTX_CTRL_FSM_STATE | R | 0h | fsm state for escape tx control path |
| 16-12 | DL3_TM_DATA_ESCTX_DATA_FSM_STATE | R | 0h | fsm state for escape tx data path |
| 11-0 | DL3_TM_HS_PATH_FSM_STATE | R | 0h | FSM state readout for hs path fsm |

12.230 DPHY_TX_DL3_TX_DIG_TBIT28 Register (Offset = 598h) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT28 is shown in [Figure 12-230](#) and described in [Table 12-462](#).

Return to [Summary Table](#).

lp component DPHY_TX_STATUS

**Table 12-461. DPHY_TX_DL3_TX_DIG_TBIT28
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0598h |

Figure 12-230. DPHY_TX_DL3_TX_DIG_TBIT28 Register

| | | | | | | | | | | | | | | | |
|----------------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_TM_ANA_COMP_OUTS | | | | | | | | DL3_UNUSED_7_0 | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-462. DPHY_TX_DL3_TX_DIG_TBIT28 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---------------------------|
| 31-16 | RESERVED | R | X | |
| 15-8 | DL3_TM_ANA_COMP_OUTS | R | 0h | Analog components outputs |
| 7-0 | DL3_UNUSED_7_0 | R | 0h | RESERVED |

12.231 DPHY_TX_DL3_TX_DIG_TBIT29 Register (Offset = 59Ch) [reset = X]

DPHY_TX_DL3_TX_DIG_TBIT29 is shown in [Figure 12-231](#) and described in [Table 12-464](#).

Return to [Summary Table](#).

bist DPHY_TX_STATUS reg1

**Table 12-463. DPHY_TX_DL3_TX_DIG_TBIT29
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 059Ch |

Figure 12-231. DPHY_TX_DL3_TX_DIG_TBIT29 Register

| | | | | | | | |
|----------------------------|------------------------|---------------------|---------------------------|-------------------|-------------------------|----------------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | DL3_TM_CUR_STATE_ULPTX_CHE | |
| R-X | | | | | | R-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_TM_CUR_STATE_ULPRX_CHE | | | DL3_TM_CUR_STATE_LPCD_CHE | | | DL3_TM_CUR_STATE_LPRX_CHE | |
| R-0h | | | R-0h | | | R-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DL3_TM_CUR_STATE_LPRX_CHE | DL3_TM_CUR_STATE_CTRLR | | | | DL3_BIST_DATA_LANE_PASS | DL3_BIST_LPRX_PASS | DL3_BIST_LPCD_PASS |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_ULPRX_PASS | DL3_BIST_ULPTX_PASS | DL3_BIST_HS_NEG_ERR | DL3_BIST_HS_POS_ERR | DL3_BIST_POS_SYNC | DL3_BIST_NEG_SYNC | DL3_BIST_CM_PLT | DL3_BIST_EN_STATUS |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-464. DPHY_TX_DL3_TX_DIG_TBIT29 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-26 | RESERVED | R | X | |
| 25-24 | DL3_TM_CUR_STATE_ULPTX_CHE | R | 0h | Current state of the ULPTX checker FSM |
| 23-21 | DL3_TM_CUR_STATE_ULPRX_CHE | R | 0h | Current state of the ULPRX checker FSM |
| 20-18 | DL3_TM_CUR_STATE_LPCD_CHE | R | 0h | Current state of the LPCD checker FSM |
| 17-15 | DL3_TM_CUR_STATE_LPRX_CHE | R | 0h | Current state of the LPRX checker FSM |
| 14-11 | DL3_TM_CUR_STATE_CTRLR | R | 0h | Current state of the Control FSM |
| 10 | DL3_BIST_DATA_LANE_PASS | R | 0h | Data lane has passed BIST completely |
| 9 | DL3_BIST_LPRX_PASS | R | 0h | LPRX BIST pass |
| 8 | DL3_BIST_LPCD_PASS | R | 0h | LPCD BIST Passed |
| 7 | DL3_BIST_ULPRX_PASS | R | 0h | ULPRX BIST passed |
| 6 | DL3_BIST_ULPTX_PASS | R | 0h | ULPTX BIST passed |
| 5 | DL3_BIST_HS_NEG_ERR | R | 0h | HS Bist error detected with negedge of sampler clock |
| 4 | DL3_BIST_HS_POS_ERR | R | 0h | HS Bist error detected with posedge of sampler clock |

Table 12-464. DPHY_TX_DL3_TX_DIG_TBIT29 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 3 | DL3_BIST_POS_SYNC | R | 0h | Pattern checker in negedge run have synced with pattern generator |
| 2 | DL3_BIST_NEG_SYNC | R | 0h | Pattern checker in posedge run have synced with pattern generator |
| 1 | DL3_BIST_CMPLT | R | 0h | BIST is completed |
| 0 | DL3_BIST_EN_STATUS | R | 0h | BIST Controller is enabled |

12.232 DPHY_TX_DL3_TX_DIG_TBIT30 Register (Offset = 5A0h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT30 is shown in [Figure 12-232](#) and described in [Table 12-466](#).

Return to [Summary Table](#).

bist pkt count values

**Table 12-465. DPHY_TX_DL3_TX_DIG_TBIT30
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05A0h |

Figure 12-232. DPHY_TX_DL3_TX_DIG_TBIT30 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_BIST_PAT_CHE_PKT_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_PAT_CHE_PKT_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-466. DPHY_TX_DL3_TX_DIG_TBIT30 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|--|
| 31-16 | DL3_BIST_PAT_CHE_PKT_CNT_NEG | R | 0h | pattern checker packet count with negedge run of sampler clock |
| 15-0 | DL3_BIST_PAT_CHE_PKT_CNT_POS | R | 0h | pattern checker packet count with posedge run of sampler clock |

12.233 DPHY_TX_DL3_TX_DIG_TBIT31 Register (Offset = 5A4h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT31 is shown in [Figure 12-233](#) and described in [Table 12-468](#).

Return to [Summary Table](#).

bist err count values

Table 12-467. DPHY_TX_DL3_TX_DIG_TBIT31 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05A4h |

Figure 12-233. DPHY_TX_DL3_TX_DIG_TBIT31 Register

| | | | | | | | | | | | | | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DL3_BIST_PAT_CHE_ERR_CNT_NEG | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_BIST_PAT_CHE_ERR_CNT_POS | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-468. DPHY_TX_DL3_TX_DIG_TBIT31 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------------------|------|-------|---|
| 31-16 | DL3_BIST_PAT_CHE_ERR_CNT_NEG | R | 0h | pattern checker error count with negedge run of sampler clock |
| 15-0 | DL3_BIST_PAT_CHE_ERR_CNT_POS | R | 0h | pattern checker error count with posedge run of sampler clock |

12.234 DPHY_TX_DL3_TX_DIG_TBIT32 Register (Offset = 5A8h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT32 is shown in [Figure 12-234](#) and described in [Table 12-470](#).

Return to [Summary Table](#).

TX_DIG_TBIT32

**Table 12-469. DPHY_TX_DL3_TX_DIG_TBIT32
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05A8h |

Figure 12-234. DPHY_TX_DL3_TX_DIG_TBIT32 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-470. DPHY_TX_DL3_TX_DIG_TBIT32 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT32 | R | 0h | RESERVED |

12.235 DPHY_TX_DL3_TX_DIG_TBIT33 Register (Offset = 5ACh) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT33 is shown in [Figure 12-235](#) and described in [Table 12-472](#).

Return to [Summary Table](#).

TX_DIG_TBIT33

**Table 12-471. DPHY_TX_DL3_TX_DIG_TBIT33
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05ACh |

Figure 12-235. DPHY_TX_DL3_TX_DIG_TBIT33 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT33 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-472. DPHY_TX_DL3_TX_DIG_TBIT33 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT33 | R | 0h | RESERVED |

12.236 DPHY_TX_DL3_TX_DIG_TBIT34 Register (Offset = 5B0h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT34 is shown in [Figure 12-236](#) and described in [Table 12-474](#).

Return to [Summary Table](#).

TX_DIG_TBIT34

**Table 12-473. DPHY_TX_DL3_TX_DIG_TBIT34
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05B0h |

Figure 12-236. DPHY_TX_DL3_TX_DIG_TBIT34 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT34 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-474. DPHY_TX_DL3_TX_DIG_TBIT34 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT34 | R | 0h | RESERVED |

12.237 DPHY_TX_DL3_TX_DIG_TBIT35 Register (Offset = 5B4h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT35 is shown in [Figure 12-237](#) and described in [Table 12-476](#).

Return to [Summary Table](#).

TX_DIG_TBIT35

**Table 12-475. DPHY_TX_DL3_TX_DIG_TBIT35
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05B4h |

Figure 12-237. DPHY_TX_DL3_TX_DIG_TBIT35 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT35 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-476. DPHY_TX_DL3_TX_DIG_TBIT35 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT35 | R | 0h | RESERVED |

12.238 DPHY_TX_DL3_TX_DIG_TBIT36 Register (Offset = 5B8h) [reset = 0h]

DPHY_TX_DL3_TX_DIG_TBIT36 is shown in [Figure 12-238](#) and described in [Table 12-478](#).

Return to [Summary Table](#).

TX_DIG_TBIT36

**Table 12-477. DPHY_TX_DL3_TX_DIG_TBIT36
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 05B8h |

Figure 12-238. DPHY_TX_DL3_TX_DIG_TBIT36 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DL3_DIG_TBIT36 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-478. DPHY_TX_DL3_TX_DIG_TBIT36 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31-0 | DL3_DIG_TBIT36 | R | 0h | RESERVED |

12.239 DPHY_TX_PCS_TX_DIG_TBIT0 Register (Offset = B00h) [reset = X]

DPHY_TX_PCS_TX_DIG_TBIT0 is shown in [Figure 12-239](#) and described in [Table 12-480](#).

Return to [Summary Table](#).

PHY_BAND_CONTROL

**Table 12-479. DPHY_TX_PCS_TX_DIG_TBIT0
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B00h |

Figure 12-239. DPHY_TX_PCS_TX_DIG_TBIT0 Register

| | | | | | | | |
|--------------------|----|----|----|--------------------|----|--------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | PCS_BAND_CTL_REG_R | |
| R/W-X | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_BAND_CTL_REG_R | | | | PCS_BAND_CTL_REG_L | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-480. DPHY_TX_PCS_TX_DIG_TBIT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|----------------------|
| 31-10 | RESERVED | R/W | X | |
| 9-5 | PCS_BAND_CTL_REG_R | R/W | 0h | Data Rate 80_100 MHz |
| 4-0 | PCS_BAND_CTL_REG_L | R/W | 0h | Data Rate 80_100 MHz |

12.240 DPHY_TX_PCS_TX_DIG_TBIT1 Register (Offset = B04h) [reset = X]

DPHY_TX_PCS_TX_DIG_TBIT1 is shown in [Figure 12-240](#) and described in [Table 12-482](#).

Return to [Summary Table](#).

PHY_PSM_CONFIG

**Table 12-481. DPHY_TX_PCS_TX_DIG_TBIT1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B04h |

Figure 12-240. DPHY_TX_PCS_TX_DIG_TBIT1 Register

| | | | | | | | |
|--------------------|----|----|----|----|----|----|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | PCS_PSM_CLOCK_FREQ |
| R/W-X | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_PSM_CLOCK_FREQ | | | | | | | PCS_PSM_CLOCK_FREQ_EN |
| R/W-0h | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-482. DPHY_TX_PCS_TX_DIG_TBIT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|-------------------------------|
| 31-9 | RESERVED | R/W | X | |
| 8-1 | PCS_PSM_CLOCK_FREQ | R/W | 0h | psm_clock freq value |
| 0 | PCS_PSM_CLOCK_FREQ_EN | R/W | 0h | take psm_clock_freq from tbit |

12.241 DPHY_TX_PCS_TX_DIG_TBIT2 Register (Offset = B08h) [reset = 22222222h]

DPHY_TX_PCS_TX_DIG_TBIT2 is shown in [Figure 12-241](#) and described in [Table 12-484](#).

Return to [Summary Table](#).

PHY_PI_PH2_DL_CONFIG

**Table 12-483. DPHY_TX_PCS_TX_DIG_TBIT2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B08h |

Figure 12-241. DPHY_TX_PCS_TX_DIG_TBIT2 Register

| | | | | | | | |
|----------------------------|----|----|----|----------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PCS_POWER_SW_2_TIME_DL_R_3 | | | | PCS_POWER_SW_2_TIME_DL_R_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCS_POWER_SW_2_TIME_DL_R_1 | | | | PCS_POWER_SW_2_TIME_DL_R_0 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PCS_POWER_SW_2_TIME_DL_L_3 | | | | PCS_POWER_SW_2_TIME_DL_L_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_POWER_SW_2_TIME_DL_L_1 | | | | PCS_POWER_SW_2_TIME_DL_L_0 | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-484. DPHY_TX_PCS_TX_DIG_TBIT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|------------------------|
| 31-28 | PCS_POWER_SW_2_TIME_DL_R_3 | R/W | 2h | power_sw_2_time_dl_r_3 |
| 27-24 | PCS_POWER_SW_2_TIME_DL_R_2 | R/W | 2h | power_sw_2_time_dl_r_2 |
| 23-20 | PCS_POWER_SW_2_TIME_DL_R_1 | R/W | 2h | power_sw_2_time_dl_r_1 |
| 19-16 | PCS_POWER_SW_2_TIME_DL_R_0 | R/W | 2h | power_sw_2_time_dl_r_0 |
| 15-12 | PCS_POWER_SW_2_TIME_DL_L_3 | R/W | 2h | power_sw_2_time_dl_l_3 |
| 11-8 | PCS_POWER_SW_2_TIME_DL_L_2 | R/W | 2h | power_sw_2_time_dl_l_2 |
| 7-4 | PCS_POWER_SW_2_TIME_DL_L_1 | R/W | 2h | power_sw_2_time_dl_l_1 |
| 3-0 | PCS_POWER_SW_2_TIME_DL_L_0 | R/W | 2h | power_sw_2_time_dl_l_0 |

12.242 DPHY_TX_PCS_TX_DIG_TBIT3 Register (Offset = B0Ch) [reset = X]

DPHY_TX_PCS_TX_DIG_TBIT3 is shown in [Figure 12-242](#) and described in [Table 12-486](#).

Return to [Summary Table](#).

PHY_PI_PH2_CL_CMN_CONFIG

**Table 12-485. DPHY_TX_PCS_TX_DIG_TBIT3
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B0Ch |

Figure 12-242. DPHY_TX_PCS_TX_DIG_TBIT3 Register

| | | | | | | | |
|--------------------------|----|----|----|--------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | PCS_POWER_SW_2_TIME_CMN | | | |
| R/W-X | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_POWER_SW_2_TIME_CL_R | | | | PCS_POWER_SW_2_TIME_CL_L | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-486. DPHY_TX_PCS_TX_DIG_TBIT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|----------------------|
| 31-12 | RESERVED | R/W | X | |
| 11-8 | PCS_POWER_SW_2_TIME_CMN | R/W | 2h | power_sw_2_time_cmn |
| 7-4 | PCS_POWER_SW_2_TIME_CL_R | R/W | 2h | power_sw_2_time_cl_r |
| 3-0 | PCS_POWER_SW_2_TIME_CL_L | R/W | 2h | power_sw_2_time_cl_l |

12.243 DPHY_TX_PCS_TX_DIG_TBIT4 Register (Offset = B10h) [reset = 2222222h]

DPHY_TX_PCS_TX_DIG_TBIT4 is shown in [Figure 12-243](#) and described in [Table 12-488](#).

Return to [Summary Table](#).

PHY_PI_PH1_DL_CONFIG

**Table 12-487. DPHY_TX_PCS_TX_DIG_TBIT4
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B10h |

Figure 12-243. DPHY_TX_PCS_TX_DIG_TBIT4 Register

| | | | | | | | |
|----------------------------|----|----|----|----------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PCS_POWER_SW_1_TIME_DL_R_3 | | | | PCS_POWER_SW_1_TIME_DL_R_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCS_POWER_SW_1_TIME_DL_R_1 | | | | PCS_POWER_SW_1_TIME_DL_R_0 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PCS_POWER_SW_1_TIME_DL_L_3 | | | | PCS_POWER_SW_1_TIME_DL_L_2 | | | |
| R/W-2h | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_POWER_SW_1_TIME_DL_L_1 | | | | PCS_POWER_SW_1_TIME_DL_L_0 | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-488. DPHY_TX_PCS_TX_DIG_TBIT4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|------------------------|
| 31-28 | PCS_POWER_SW_1_TIME_DL_R_3 | R/W | 2h | power_sw_1_time_dl_r_3 |
| 27-24 | PCS_POWER_SW_1_TIME_DL_R_2 | R/W | 2h | power_sw_1_time_dl_r_2 |
| 23-20 | PCS_POWER_SW_1_TIME_DL_R_1 | R/W | 2h | power_sw_1_time_dl_r_1 |
| 19-16 | PCS_POWER_SW_1_TIME_DL_R_0 | R/W | 2h | power_sw_1_time_dl_r_0 |
| 15-12 | PCS_POWER_SW_1_TIME_DL_L_3 | R/W | 2h | power_sw_1_time_dl_l_3 |
| 11-8 | PCS_POWER_SW_1_TIME_DL_L_2 | R/W | 2h | power_sw_1_time_dl_l_2 |
| 7-4 | PCS_POWER_SW_1_TIME_DL_L_1 | R/W | 2h | power_sw_1_time_dl_l_1 |
| 3-0 | PCS_POWER_SW_1_TIME_DL_L_0 | R/W | 2h | power_sw_1_time_dl_l_0 |

12.244 DPHY_TX_PCS_TX_DIG_TBIT5 Register (Offset = B14h) [reset = X]

DPHY_TX_PCS_TX_DIG_TBIT5 is shown in [Figure 12-244](#) and described in [Table 12-490](#).

Return to [Summary Table](#).

PHY_PI_PH1_CL_CMN_CONFIG

**Table 12-489. DPHY_TX_PCS_TX_DIG_TBIT5
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B14h |

Figure 12-244. DPHY_TX_PCS_TX_DIG_TBIT5 Register

| | | | | | | | |
|--------------------------|----|----|----|--------------------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | PCS_POWER_SW_1_TIME_CMN | | | |
| R/W-X | | | | R/W-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_POWER_SW_1_TIME_CL_R | | | | PCS_POWER_SW_1_TIME_CL_L | | | |
| R/W-2h | | | | R/W-2h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-490. DPHY_TX_PCS_TX_DIG_TBIT5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------------|------|-------|----------------------|
| 31-12 | RESERVED | R/W | X | |
| 11-8 | PCS_POWER_SW_1_TIME_CMN | R/W | 2h | power_sw_1_time_cmn |
| 7-4 | PCS_POWER_SW_1_TIME_CL_R | R/W | 2h | power_sw_1_time_cl_r |
| 3-0 | PCS_POWER_SW_1_TIME_CL_L | R/W | 2h | power_sw_1_time_cl_l |

12.245 DPHY_TX_PCS_TX_DIG_TBIT6 Register (Offset = B18h) [reset = 0h]

DPHY_TX_PCS_TX_DIG_TBIT6 is shown in [Figure 12-245](#) and described in [Table 12-492](#).

Return to [Summary Table](#).

PHY_DL_SPARE_LEFT

**Table 12-491. DPHY_TX_PCS_TX_DIG_TBIT6
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B18h |

Figure 12-245. DPHY_TX_PCS_TX_DIG_TBIT6 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCS_DTX_L_3_SPARE | | | | | | | | PCS_DTX_L_2_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_DTX_L_1_SPARE | | | | | | | | PCS_DTX_L_0_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-492. DPHY_TX_PCS_TX_DIG_TBIT6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--------------------|
| 31-24 | PCS_DTX_L_3_SPARE | R/W | 0h | dtx_l_3 spare port |
| 23-16 | PCS_DTX_L_2_SPARE | R/W | 0h | dtx_l_2 spare port |
| 15-8 | PCS_DTX_L_1_SPARE | R/W | 0h | dtx_l_1 spare port |
| 7-0 | PCS_DTX_L_0_SPARE | R/W | 0h | dtx_l_0 spare port |

12.246 DPHY_TX_PCS_TX_DIG_TBIT7 Register (Offset = B1Ch) [reset = 0h]

DPHY_TX_PCS_TX_DIG_TBIT7 is shown in [Figure 12-246](#) and described in [Table 12-494](#).

Return to [Summary Table](#).

PHY_DL_SPARE_RIGHT

**Table 12-493. DPHY_TX_PCS_TX_DIG_TBIT7
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B1Ch |

Figure 12-246. DPHY_TX_PCS_TX_DIG_TBIT7 Register

| | | | | | | | | | | | | | | | |
|-------------------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PCS_DTX_R_3_SPARE | | | | | | | | PCS_DTX_R_2_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_DTX_R_1_SPARE | | | | | | | | PCS_DTX_R_0_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-494. DPHY_TX_PCS_TX_DIG_TBIT7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--------------------|
| 31-24 | PCS_DTX_R_3_SPARE | R/W | 0h | dtx_r_3 spare port |
| 23-16 | PCS_DTX_R_2_SPARE | R/W | 0h | dtx_r_2 spare port |
| 15-8 | PCS_DTX_R_1_SPARE | R/W | 0h | dtx_r_1 spare port |
| 7-0 | PCS_DTX_R_0_SPARE | R/W | 0h | dtx_r_0 spare port |

12.247 DPHY_TX_PCS_TX_DIG_TBIT8 Register (Offset = B20h) [reset = X]

DPHY_TX_PCS_TX_DIG_TBIT8 is shown in [Figure 12-247](#) and described in [Table 12-496](#).

Return to [Summary Table](#).

PHY_CL_CMN_SPARE

**Table 12-495. DPHY_TX_PCS_TX_DIG_TBIT8
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B20h |

Figure 12-247. DPHY_TX_PCS_TX_DIG_TBIT8 Register

| | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | PCS_CMN_SPARE | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PCS_CL_R_SPARE | | | | | | | | PCS_CL_L_SPARE | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-496. DPHY_TX_PCS_TX_DIG_TBIT8 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|-----------------|
| 31-24 | RESERVED | R/W | X | |
| 23-16 | PCS_CMN_SPARE | R/W | 0h | cmn spare port |
| 15-8 | PCS_CL_R_SPARE | R/W | 0h | cl_r spare port |
| 7-0 | PCS_CL_L_SPARE | R/W | 0h | cl_l spare port |

12.248 DPHY_TX_PCS_TX_DIG_TBIT9 Register (Offset = B24h) [reset = X]

DPHY_TX_PCS_TX_DIG_TBIT9 is shown in [Figure 12-248](#) and described in [Table 12-498](#).

Return to [Summary Table](#).

PHY_PI_CONFIG

**Table 12-497. DPHY_TX_PCS_TX_DIG_TBIT9
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B24h |

Figure 12-248. DPHY_TX_PCS_TX_DIG_TBIT9 Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------------|--------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | PCS_PSO_DISABLE_VALUE | PCS_PSO_DISABLE_EN |
| R/W-X | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-498. DPHY_TX_PCS_TX_DIG_TBIT9 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------------|------|-------|----------------------------|
| 31-2 | RESERVED | R/W | X | |
| 1 | PCS_PSO_DISABLE_VALUE | R/W | 0h | pso_disbale value |
| 0 | PCS_PSO_DISABLE_EN | R/W | 0h | take pso_diabale from tbit |

12.249 DPHY_TX_PCS_TX_DIG_TBIT10 Register (Offset = B28h) [reset = 0h]

DPHY_TX_PCS_TX_DIG_TBIT10 is shown in [Figure 12-249](#) and described in [Table 12-500](#).

Return to [Summary Table](#).

DIG_TBIT10

Table 12-499. DPHY_TX_PCS_TX_DIG_TBIT10 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0B28h |

Figure 12-249. DPHY_TX_PCS_TX_DIG_TBIT10 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| PCS_DIG_TBIT10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-500. DPHY_TX_PCS_TX_DIG_TBIT10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|-------------------------------|
| 31-0 | PCS_DIG_TBIT10 | R/W | 0h | Digital Test Register Extra 4 |

12.250 DPHY_TX_ISO_PHY_ISO_CNTRL Register (Offset = C00h) [reset = 50Fh]

DPHY_TX_ISO_PHY_ISO_CNTRL is shown in [Figure 12-250](#) and described in [Table 12-502](#).

Return to [Summary Table](#).

PHY_ISO_CNTRL

**Table 12-501. DPHY_TX_ISO_PHY_ISO_CNTRL
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C00h |

Figure 12-250. DPHY_TX_ISO_PHY_ISO_CNTRL Register

| | | | | | | | |
|----------------|----|----|----|-----------------------|---------------------|----------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_12 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_12 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_12 | | | | ISO_PHY_ISOL ATION | ISO_PHY_ISO_ CMN | ISO_PHY_ISO_CL | |
| R-0h | | | | R/W-0h | R/W-1h | R/W-1h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_PHY_ISO_DL | | | | | | | |
| R/W-Fh | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-502. DPHY_TX_ISO_PHY_ISO_CNTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|--|
| 31-12 | ISO_BF_31_12 | R | 0h | Reserved |
| 11 | ISO_PHY_ISOLATION | R/W | 0h | when set enables phy_isolation |
| 10 | ISO_PHY_ISO_CMN | R/W | 1h | This bit enables the Isolation on Common Lane |
| 9-8 | ISO_PHY_ISO_CL | R/W | 1h | Bit 1: Setting a value 1 isolates the Right Clock Lane |
| 7-0 | ISO_PHY_ISO_DL | R/W | Fh | Bit 7: Setting a value 1 isolates the Data Lane 3 on Right Link |

12.251 DPHY_TX_ISO_PHY_ISO_RESET Register (Offset = C04h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_RESET is shown in [Figure 12-251](#) and described in [Table 12-504](#).

Return to [Summary Table](#).

PHY_ISO_RESET

Table 12-503. DPHY_TX_ISO_PHY_ISO_RESET Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C04h |

Figure 12-251. DPHY_TX_ISO_PHY_ISO_RESET Register

| | | | | | | | |
|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_11 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_11 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_11 | | | | | ISO_LANE_RS TB_CMN | ISO_LANE_RS TB_CL_R | ISO_LANE_RS TB_CL_L |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_LANE_RS TB_DL_R_3 | ISO_LANE_RS TB_DL_R_2 | ISO_LANE_RS TB_DL_R_1 | ISO_LANE_RS TB_DL_R_0 | ISO_LANE_RS TB_DL_L_3 | ISO_LANE_RS TB_DL_L_2 | ISO_LANE_RS TB_DL_L_1 | ISO_LANE_RS TB_DL_L_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-504. DPHY_TX_ISO_PHY_ISO_RESET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|--|
| 31-11 | ISO_BF_31_11 | R | 0h | Reserved |
| 10 | ISO_LANE_RSTB_CMN | R/W | 0h | Drives the Lane Reset for Common lane_rstb_cm_n |
| 9 | ISO_LANE_RSTB_CL_R | R/W | 0h | Drives the Right Clock Lane Reset lane_rstb_cl_l |
| 8 | ISO_LANE_RSTB_CL_L | R/W | 0h | Drives the Left Clock Lane Reset lane_rstb_cl_l |
| 7 | ISO_LANE_RSTB_DL_R_3 | R/W | 0h | Drives the Data Lane 3 Right Link Reset lane_rstb_dl_7 |
| 6 | ISO_LANE_RSTB_DL_R_2 | R/W | 0h | Drives the Data Lane 2 Right Link Reset lane_rstb_dl_6 |
| 5 | ISO_LANE_RSTB_DL_R_1 | R/W | 0h | Drives the Data Lane 1 Right Link Reset lane_rstb_dl_5 |
| 4 | ISO_LANE_RSTB_DL_R_0 | R/W | 0h | Drives the Data Lane 0 Right Link Reset lane_rstb_dl_4 |
| 3 | ISO_LANE_RSTB_DL_L_3 | R/W | 0h | Drives the Data Lane 3 Left Link Reset lane_rstb_dl_3 |
| 2 | ISO_LANE_RSTB_DL_L_2 | R/W | 0h | Drives the Data Lane 2 Left Link Reset lane_rstb_dl_2 |
| 1 | ISO_LANE_RSTB_DL_L_1 | R/W | 0h | Drives the Data Lane 1 Left Link Reset lane_rstb_dl_1 |
| 0 | ISO_LANE_RSTB_DL_L_0 | R/W | 0h | Drives the Data Lane 0 Left Link Reset lane_rstb_dl_0 |

12.252 DPHY_TX_ISO_PHY_ISO_ENABLE Register (Offset = C08h) [reset = 10Fh]

DPHY_TX_ISO_PHY_ISO_ENABLE is shown in [Figure 12-252](#) and described in [Table 12-506](#).

Return to [Summary Table](#).

PHY_ISO_ENABLE

Table 12-505. DPHY_TX_ISO_PHY_ISO_ENABLE Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C08h |

Figure 12-252. DPHY_TX_ISO_PHY_ISO_ENABLE Register

| | | | | | | | |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|--------------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_10 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_10 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_10 | | | | | | ISO_TXENABL ECLK_CL_R | ISO_TXENABL ECLK_CL_L |
| R-0h | | | | | | R/W-0h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_M_ENABL E_DL_R_3 | ISO_M_ENABL E_DL_R_2 | ISO_M_ENABL E_DL_R_1 | ISO_M_ENABL E_DL_R_0 | ISO_M_ENABL E_DL_L_3 | ISO_M_ENABL E_DL_L_2 | ISO_M_ENABL E_DL_L_1 | ISO_M_ENABL E_DL_L_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-506. DPHY_TX_ISO_PHY_ISO_ENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------|------|-------|---|
| 31-10 | ISO_BF_31_10 | R | 0h | Reserved |
| 9 | ISO_TXENABLECLK_CL_R | R/W | 0h | Drives to enable the right clock lane TxEnableClk_clk_r |
| 8 | ISO_TXENABLECLK_CL_L | R/W | 1h | Drives to enable the left clock lane TxEnableClk_clk_l |
| 7 | ISO_M_ENABLE_DL_R_3 | R/W | 0h | Enables the Data Lane 3 Right Link M_Enable_dl_7 |
| 6 | ISO_M_ENABLE_DL_R_2 | R/W | 0h | Enables the Data Lane 2 Right Link M_Enable_dl_6 |
| 5 | ISO_M_ENABLE_DL_R_1 | R/W | 0h | Enables the Data Lane 1 Right Link M_Enable_dl_5 |
| 4 | ISO_M_ENABLE_DL_R_0 | R/W | 0h | Enables the Data Lane 0 Right Link M_Enable_dl_4 |
| 3 | ISO_M_ENABLE_DL_L_3 | R/W | 1h | Enables the Data Lane 3 Left Link M_Enable_dl_3 |
| 2 | ISO_M_ENABLE_DL_L_2 | R/W | 1h | Enables the Data Lane 2 Left Link M_Enable_dl_2 |
| 1 | ISO_M_ENABLE_DL_L_1 | R/W | 1h | Enables the Data Lane 1 Left Link M_Enable_dl_1 |
| 0 | ISO_M_ENABLE_DL_L_0 | R/W | 1h | Enables the Data Lane 0 Left Link M_Enable_dl_0 |

12.253 DPHY_TX_ISO_PHY_ISO_CMN_CTRL Register (Offset = C0Ch) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_CMN_CTRL is shown in [Figure 12-253](#) and described in [Table 12-508](#).

Return to [Summary Table](#).

PHY_ISO_CMN_CTRL

Table 12-507. DPHY_TX_ISO_PHY_ISO_CMN_CTRL Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C0Ch |

Figure 12-253. DPHY_TX_ISO_PHY_ISO_CMN_CTRL Register

| | | | | | | | |
|-----------------|--------------------|----------------------|-----------------|-------------------|----|-------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_8 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_8 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_8 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_PSO_DISABLE | ISO_O_SUPPLY_IO_PG | ISO_O_SUPPLY_CORE_PG | ISO_O_CMN_READY | ISO_IP_CONFIG_CMN | | ISO_PSO_CMN | |
| R/W-0h | R-0h | R-0h | R-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-508. DPHY_TX_ISO_PHY_ISO_CMN_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------|------|-------|---|
| 31-8 | ISO_BF_31_8 | R | 0h | Reserved |
| 7 | ISO_PSO_DISABLE | R/W | 0h | Drives pso_disable |
| 6 | ISO_O_SUPPLY_IO_PG | R | 0h | I/O supply power is good o_supply_io_pg |
| 5 | ISO_O_SUPPLY_CORE_PG | R | 0h | Core Supply Power is good o_supply_core_pg |
| 4 | ISO_O_CMN_READY | R | 0h | Common ready Indicator o_cmn_ready |
| 3-1 | ISO_IP_CONFIG_CMN | R/W | 0h | Drives the IP configuration to decide which clock lane acts as the master lane to all clock lanes ip_config_cmn |
| 0 | ISO_PSO_CMN | R/W | 0h | Drives the power shut off for the Common pso_cmn |

12.254 DPHY_TX_ISO_PHY_ISO_CMN_PLL Register (Offset = C10h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_CMN_PLL is shown in [Figure 12-254](#) and described in [Table 12-510](#).

Return to [Summary Table](#).

PHY_ISO_CMN_PLL

Table 12-509. DPHY_TX_ISO_PHY_ISO_CMN_PLL Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C10h |

Figure 12-254. DPHY_TX_ISO_PHY_ISO_CMN_PLL Register

| | | | | | | | |
|---------------|-------------|------------|---------------|----|---------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_24 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_PLL_LOCK | ISO_PLL_PSO | ISO_PLL_PD | ISO_PLL_FBDIV | | | | |
| R-0h | R/W-0h | R/W-0h | R/W-0h | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_PLL_FBDIV | | | | | ISO_PLL_OPDIV | | |
| R/W-0h | | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_PLL_OPDIV | | | ISO_PLL_IPDIV | | | | |
| R/W-0h | | | R/W-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-510. DPHY_TX_ISO_PHY_ISO_CMN_PLL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|---|
| 31-24 | ISO_BF_31_24 | R | 0h | Reserved |
| 23 | ISO_PLL_LOCK | R | 0h | A value 1 indicates the PLL clock is locked to the reference clock (pll_lock) |
| 22 | ISO_PLL_PSO | R/W | 0h | Connected to pll_pso which are Reserved and reserved for future use |
| 21 | ISO_PLL_PD | R/W | 0h | Connected to pll_pd which are Reserved and reserved for future use |
| 20-11 | ISO_PLL_FBDIV | R/W | 0h | Drives the PLL feedback divider value {pll_fbdiv [9:0]} |
| 10-5 | ISO_PLL_OPDIV | R/W | 0h | Drives the PLL output divider value {pll_opdiv [5:0]} [On APB clock domain] |
| 4-0 | ISO_PLL_IPDIV | R/W | 0h | Drives the PLL input divider value {pll_ipdiv [4:0]} |

12.255 DPHY_TX_ISO_PHY_ISO_CL_CNTRL_L Register (Offset = C14h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_CL_CNTRL_L is shown in [Figure 12-255](#) and described in [Table 12-512](#).

Return to [Summary Table](#).

PHY_ISO_CL_CNTRL_L

Table 12-511.
DPHY_TX_ISO_PHY_ISO_CL_CNTRL_L Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C14h |

Figure 12-255. DPHY_TX_ISO_PHY_ISO_CL_CNTRL_L Register

| | | | | | | | |
|---------------------|-------------------------|------------------------------|------------------------|-------------------------|------------------------|---------------------|--------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_8_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_8_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_8_X | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_LANE_READY_CL_L | ISO_TXSTOPSTATECLK_CL_L | ISO_TXULPSACTIVE_NOTCLK_CL_L | ISO_TXREADYHSCCLK_CL_L | ISO_M_CLK_SWAPDPDN_CL_L | ISO_TXULPSEXITCLK_CL_L | ISO_TXULPSCCLK_CL_L | ISO_TXREQUESTHSCCLK_CL_L |
| R-0h | R-0h | R-0h | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-512. DPHY_TX_ISO_PHY_ISO_CL_CNTRL_L Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------------------|------|-------|---|
| 31-8 | ISO_BF_31_8_X | R | 0h | Reserved |
| 7 | ISO_LANE_READY_CL_L | R | 0h | clock lane ready |
| 6 | ISO_TXSTOPSTATECLK_CL_L | R | 0h | Driven high when the clock lane is in stop state TxStopStateClk_cl_l |
| 5 | ISO_TXULPSACTIVE_NOTCLK_CL_L | R | 0h | Driven high when the clock lane is in ULPS active state TxULPSActiveNotClk_clk_l |
| 4 | ISO_TXREADYHSCCLK_CL_L | R | 0h | Stores the High Speed Clock Transmission Ready TxReadyHSClk_clk_l |
| 3 | ISO_M_CLK_SWAPDPDN_CL_L | R/W | 0h | Drives the value to enable the Swap of DP and DN signals inside the clock lane M_Clk_SwapDpDn_clk_l |
| 2 | ISO_TXULPSEXITCLK_CL_L | R/W | 0h | Drives to initiate exit of ULPS TxULPSExitClk_clk_l |
| 1 | ISO_TXULPSCCLK_CL_L | R/W | 0h | Drives to initiate entry to ULPS TxULPSClk_clk_l |
| 0 | ISO_TXREQUESTHSCCLK_CL_L | R/W | 0h | Drives the High Speed Clock Transmission Request TxRequestHSClk_clk_l |

12.256 DPHY_TX_ISO_PHY_ISO_DL_CTRL_L0 Register (Offset = C18h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_DL_CTRL_L0 is shown in [Figure 12-256](#) and described in [Table 12-514](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L0

Table 12-513.
DPHY_TX_ISO_PHY_ISO_DL_CTRL_L0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C18h |

Figure 12-256. DPHY_TX_ISO_PHY_ISO_DL_CTRL_L0 Register

| | | | | | | | |
|-------------|----|----|----|---------------------------|-----------------------------------|------------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_4 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_4 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_4 | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_BF_31_4 | | | | ISO_LANE_RE ADY_DL_L_0 | ISO_M_DATA SWAPDPDN_D L_L_0 | ISO_FORCETX STOPMODE_D L_L_0 | ISO_M_TURNR EQUEST_DL_L _0 |
| R-0h | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-514. DPHY_TX_ISO_PHY_ISO_DL_CTRL_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|---|
| 31-4 | ISO_BF_31_4 | R | 0h | Reserved |
| 3 | ISO_LANE_READY_DL_L_0 | R | 0h | High Speed data lane ready lane_ready_dl_l_0 |
| 2 | ISO_M_DATA_SWAPDPDN_DL_L_0 | R/W | 0h | Swaps the tx_p and tx_m differential pins M_Data_SwapDpDn_dl_l_0 |
| 1 | ISO_FORCETXSTOPMODE_DL_L_0 | R/W | 0h | Drives the lane forcing into stop state ForceTxStopMode_dl_l_0 |
| 0 | ISO_M_TURNREQUEST_DL_L_0 | R/W | 0h | Drives the Turnaround request M_TurnRequest_dl_l_0 |

12.257 DPHY_TX_ISO_PHY_ISO_DL_HS_L0 Register (Offset = C1Ch) [reset = X]

DPHY_TX_ISO_PHY_ISO_DL_HS_L0 is shown in [Figure 12-257](#) and described in [Table 12-516](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L0

Table 12-515. DPHY_TX_ISO_PHY_ISO_DL_HS_L0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C1Ch |

Figure 12-257. DPHY_TX_ISO_PHY_ISO_DL_HS_L0 Register

| | | | | | | | |
|---------------------|----|----|----|----------------------|------------------------|----------------------------|------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_16 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_TXDATAHS_DL_L_0 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ISO_TXREADYHS_DL_L_0 | ISO_TXSKEWCALHS_DL_L_0 | ISO_TXSKEWCALHSINIT_DL_L_0 | ISO_TXREQUESTHS_DL_L_0 |
| R/W-X | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-516. DPHY_TX_ISO_PHY_ISO_DL_HS_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-16 | ISO_BF_31_16 | R | 0h | Reserved |
| 15-8 | ISO_TXDATAHS_DL_L_0 | R/W | 0h | Drives the high speed transmission data TxDataHS_dl_l_0 [7:0] |
| 7-4 | RESERVED | R/W | X | |
| 3 | ISO_TXREADYHS_DL_L_0 | R | 0h | Stores the high speed data transmission ready TxReadyHS_dl_l_0 |
| 2 | ISO_TXSKEWCALHS_DL_L_0 | R/W | 0h | Drives transmission skew calibration periodic TxSkewCalHS_dl_l_0 |
| 1 | ISO_TXSKEWCALHSINIT_DL_L_0 | R/W | 0h | Drives to run the initial skew calibration TxSkewCalHSInit_dl_l_0 |
| 0 | ISO_TXREQUESTHS_DL_L_0 | R/W | 0h | Drives the High Speed Data Transmission Request TxRequestHS_dl_l_0 |

12.258 DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 Register (Offset = C20h) [reset = X]

DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 is shown in [Figure 12-258](#) and described in [Table 12-518](#).

Return to [Summary Table](#).

PHY_ISO_DL_TX_ESC_L0

Table 12-517.
DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C20h |

Figure 12-258. DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------------|-------------------------|-------------------------|----------------------------|----------------------------|--------------------------|-------------------------|-------------------------------|
| ISO_BF_31_28 | | | | ISO_M_ULPSACTIVENOT_DL_L_0 | ISO_M_DIRECTION_DL_L_0 | ISO_M_STOPSTATE_DL_L_0 | ISO_M_ERRCONTENTIONLP1_DL_L_0 |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_M_ERRCONTENTIONLP0_DL_L_0 | ISO_M_ERRSYNCESC_DL_L_0 | ISO_M_ERRCONTROL_DL_L_0 | ISO_M_ERRESC_DL_L_0 | ISO_M_TXTRIGGERESC_DL_L_0 | | | |
| R-0h | R-0h | R-0h | R-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_M_TXDATAESC_DL_L_0 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ISO_M_TXREADYESC_DL_L_0 | ISO_M_TXULPSEXITESC_DL_L_0 | ISO_M_TXULPSESC_DL_L_0 | ISO_M_TXVALIDDESC_DL_L_0 | ISO_M_TXLPDTEESC_DL_L_0 | ISO_M_TXREQUESTESC_DL_L_0 |
| R/W-X | | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-518. DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-28 | ISO_BF_31_28 | R | 0h | Reserved |
| 27 | ISO_M_ULPSACTIVENOT_DL_L_0 | R | 0h | Lane ULPS Active state M_ULPSActiveNot_dl_l_0 |
| 26 | ISO_M_DIRECTION_DL_L_0 | R | 0h | Lane transmit / receive direction M_Direction_dl_l_0 |
| 25 | ISO_M_STOPSTATE_DL_L_0 | R | 0h | Lane Stop State M_StopState_dl_l_0 |
| 24 | ISO_M_ERRCONTENTIONLP1_DL_L_0 | R | 0h | LP1 contention Error M_ErrContentionLP1_dl_l_0 |
| 23 | ISO_M_ERRCONTENTIONLP0_DL_L_0 | R | 0h | LP1 contention Error M_ErrContentionLP0_dl_l_0 |
| 22 | ISO_M_ERRSYNCESC_DL_L_0 | R | 0h | Low power data transmission sync error M_ErrSyncEsc_dl_l_0 |
| 21 | ISO_M_ERRCONTROL_DL_L_0 | R | 0h | Control Error M_ErrControl_dl_l_0 |
| 20 | ISO_M_ERRESC_DL_L_0 | R | 0h | Escape Entry Error M_ErrEsc_dl_l_0 |
| 19-16 | ISO_M_TXTRIGGERESC_DL_L_0 | R/W | 0h | Transmit escape mode trigger M_TxTriggerEsc_dl_l_0 [3:0] |

Table 12-518. DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 15-8 | ISO_M_TXDATAESC_DL_L_0 | R/W | 0h | Transmit escape mode low power transmit data M_TxDataEsc_dl_l_0 [7:0] |
| 7-6 | RESERVED | R/W | X | |
| 5 | ISO_M_TXREADYESC_DL_L_0 | R | 0h | Transmit escape mode low power transmit data ready M_TxReadyEsc_dl_l_0 |
| 4 | ISO_M_TXULPSEXITESC_DL_L_0 | R/W | 0h | Initiate exit of ULPS M_TxULPSExitEsc_dl_l_0 |
| 3 | ISO_M_TXULPSESC_DL_L_0 | R/W | 0h | Transmit escape mode ultra low power state M_TxULPSEsc_dl_l_0 |
| 2 | ISO_M_TXVALIDESC_DL_L_0 | R/W | 0h | Transmit escape mode low power transmit data valid M_TxValidEsc_dl_l_0 |
| 1 | ISO_M_TXLPDTEESC_DL_L_0 | R/W | 0h | Transmit escape mode low power data M_TxLPDTEsc_dl_l_0 |
| 0 | ISO_M_TXREQUESTESC_DL_L_0 | R/W | 0h | Transmit escape mode request M_TxRequestEsc_dl_l_0 |

12.259 DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L0 Register (Offset = C24h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L0 is shown in [Figure 12-259](#) and described in [Table 12-520](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L0

Table 12-519.
DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L0 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C24h |

Figure 12-259. DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L0 Register

| | | | | | | | |
|----------------------------|---------------------------|----|----|----|----------------------------|-----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_15 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_15 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_15 | ISO_M_RXDATAESC_DL_L_0 | | | | | | |
| R-0h | R-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_M_RXDAT AESC_DL_L_0 | ISO_M_RXTRIGGERESC_DL_L_0 | | | | ISO_M_RXULP SESC_DL_L_0 | ISO_M_RXVALI DESC_DL_L_0 | ISO_M_RXLPD TESC_DL_L_0 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-520. DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | ISO_BF_31_15 | R | 0h | Reserved |
| 14-7 | ISO_M_RXDATAESC_DL_L_0 | R | 0h | Receive escape mode low power receive data M_RxDataEsc_dl_l_0 [7:0] |
| 6-3 | ISO_M_RXTRIGGERESC_DL_L_0 | R | 0h | Receive escape mode low power trigger state M_RxTriggerEsc_dl_l_0 [3:0] |
| 2 | ISO_M_RXULPSESC_DL_L_0 | R | 0h | Receive escape mode low power ultra low power state M_RxULPSEsc_dl_l_0 |
| 1 | ISO_M_RXVALIDESC_DL_L_0 | R | 0h | Receive escape mode low power receive data M_RxValidEsc_dl_l_0 |
| 0 | ISO_M_RXLPDTEESC_DL_L_0 | R | 0h | Receive escape mode low power data M_RxLPDTEsc_dl_l_0 |

12.260 DPHY_TX_ISO_PHY_ISO_DL_CTRL_L1 Register (Offset = C28h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_DL_CTRL_L1 is shown in [Figure 12-260](#) and described in [Table 12-522](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L1

Table 12-521.
DPHY_TX_ISO_PHY_ISO_DL_CTRL_L1 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C28h |

Figure 12-260. DPHY_TX_ISO_PHY_ISO_DL_CTRL_L1 Register

| | | | | | | | |
|---------------|----|----|----|---------------------------|------------------------------------|------------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_4_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_4_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_4_X | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_BF_31_4_X | | | | ISO_LANE_RE ADY_DL_L_1 | ISO_M_DATA_ SWAPDPDN_D L_L_1 | ISO_FORCETX STOPMODE_D L_L_1 | ISO_M_TURNR EQUEST_DL_L _1 |
| R-0h | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-522. DPHY_TX_ISO_PHY_ISO_DL_CTRL_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 31-4 | ISO_BF_31_4_X | R | 0h | Reserved |
| 3 | ISO_LANE_READY_DL_L_1 | R | 0h | High Speed data lane ready lane_ready_dl_l_1 |
| 2 | ISO_M_DATA_SWAPDPDN_DL_L_1 | R/W | 0h | Swaps the tx_p and tx_m differential pins M_Data_SwapDpDn_dl_l_1 |
| 1 | ISO_FORCETXSTOPMODE_DL_L_1 | R/W | 0h | Drives the lane forcing into stop state ForceTxStopMode_dl_l_1 |
| 0 | ISO_M_TURNREQUEST_DL_L_1 | R/W | 0h | Drives the Turnaround request M_TurnRequest_dl_l_1 |

12.261 DPHY_TX_ISO_PHY_ISO_DL_HS_L1 Register (Offset = C2Ch) [reset = X]

DPHY_TX_ISO_PHY_ISO_DL_HS_L1 is shown in [Figure 12-261](#) and described in [Table 12-524](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L1

**Table 12-523. DPHY_TX_ISO_PHY_ISO_DL_HS_L1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C2Ch |

Figure 12-261. DPHY_TX_ISO_PHY_ISO_DL_HS_L1 Register

| | | | | | | | |
|---------------------|----|----|----|--------------------------|----------------------------|------------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_16_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_16_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_TXDATAHS_DL_L_1 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ISO_TXREADY HS_DL_L_1 | ISO_TXSKEWC ALHS_DL_L_1 | ISO_TXSKEWC ALHSINIT_DL_ L_1 | ISO_TXREQUE STHS_DL_L_1 |
| R/W-X | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-524. DPHY_TX_ISO_PHY_ISO_DL_HS_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-16 | ISO_BF_31_16_X | R | 0h | Reserved |
| 15-8 | ISO_TXDATAHS_DL_L_1 | R/W | 0h | Drives the high speed transmission data TxDataHS_dl_l_1 [7:0] |
| 7-4 | RESERVED | R/W | X | |
| 3 | ISO_TXREADYHS_DL_L_1 | R | 0h | Stores the high speed data transmission ready TxReadyHS_dl_l_1 |
| 2 | ISO_TXSKEWCALHS_DL_L_1 | R/W | 0h | Drives transmission skew calibration periodic TxSkewCalHS_dl_l_1 |
| 1 | ISO_TXSKEWCALHSINIT_DL_L_1 | R/W | 0h | Drives to run the initial skew calibration TxSkewCalHSInit_dl_l_1 |
| 0 | ISO_TXREQUESTHS_DL_L_1 | R/W | 0h | Drives the High Speed Data Transmission Request TxRequestHS_dl_l_1 |

12.262 DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 Register (Offset = C30h) [reset = X]

DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 is shown in [Figure 12-262](#) and described in [Table 12-526](#).

Return to [Summary Table](#).

PHY_ISO_DL_TX_ESC_L1

Table 12-525.
DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C30h |

Figure 12-262. DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------------|-------------------------|-------------------------|----------------------------|----------------------------|--------------------------|-------------------------|-------------------------------|
| ISO_BF_31_28_X | | | | ISO_M_ULPSACTIVENOT_DL_L_1 | ISO_M_DIRECTION_DL_L_1 | ISO_M_STOPSTATE_DL_L_1 | ISO_M_ERRCONTENTIONLP1_DL_L_1 |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_M_ERRCONTENTIONLP0_DL_L_1 | ISO_M_ERRSYNCESC_DL_L_1 | ISO_M_ERRCONTROL_DL_L_1 | ISO_M_ERRESC_DL_L_1 | ISO_M_TXTRIGGERESC_DL_L_1 | | | |
| R-0h | R-0h | R-0h | R-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_M_TXDATAESC_DL_L_1 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ISO_M_TXREADYESC_DL_L_1 | ISO_M_TXULPSEXITESC_DL_L_1 | ISO_M_TXULPSESC_DL_L_1 | ISO_M_TXVALIDDESC_DL_L_1 | ISO_M_TXLPDTEESC_DL_L_1 | ISO_M_TXREQUESTESC_DL_L_1 |
| R/W-X | | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-526. DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-28 | ISO_BF_31_28_X | R | 0h | Reserved |
| 27 | ISO_M_ULPSACTIVENOT_DL_L_1 | R | 0h | Lane ULPS Active state M_ULPSActiveNot_dl_l_1 |
| 26 | ISO_M_DIRECTION_DL_L_1 | R | 0h | Lane transmit / receive direction M_Direction_dl_l_1 |
| 25 | ISO_M_STOPSTATE_DL_L_1 | R | 0h | Lane Stop State M_StopState_dl_l_1 |
| 24 | ISO_M_ERRCONTENTIONLP1_DL_L_1 | R | 0h | LP1 contention Error M_ErrContentionLP1_dl_l_1 |
| 23 | ISO_M_ERRCONTENTIONLP0_DL_L_1 | R | 0h | LP1 contention Error M_ErrContentionLP0_dl_l_1 |
| 22 | ISO_M_ERRSYNCESC_DL_L_1 | R | 0h | Low power data transmission sync error M_ErrSyncEsc_dl_l_1 |
| 21 | ISO_M_ERRCONTROL_DL_L_1 | R | 0h | Control Error M_ErrControl_dl_l_1 |
| 20 | ISO_M_ERRESC_DL_L_1 | R | 0h | Escape Entry Error M_ErrEsc_dl_l_1 |
| 19-16 | ISO_M_TXTRIGGERESC_DL_L_1 | R/W | 0h | Transmit escape mode trigger M_TxTriggerEsc_dl_l_1 [3:0] |

Table 12-526. DPHY_TX_ISO_PHY_ISO_DL_TX_ESC_L1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 15-8 | ISO_M_TXDATAESC_DL_L_1 | R/W | 0h | Transmit escape mode low power transmit data M_TxDataEsc_dl_l_1 [7:0] |
| 7-6 | RESERVED | R/W | X | |
| 5 | ISO_M_TXREADYESC_DL_L_1 | R | 0h | Transmit escape mode low power transmit data ready M_TxReadyEsc_dl_l_1 |
| 4 | ISO_M_TXULPSEXITESC_DL_L_1 | R/W | 0h | Initiate exit of ULPS M_TxULPSExitEsc_dl_l_1 |
| 3 | ISO_M_TXULPSESC_DL_L_1 | R/W | 0h | Transmit escape mode ultra low power state M_TxULPSEsc_dl_l_1 |
| 2 | ISO_M_TXVALIDESC_DL_L_1 | R/W | 0h | Transmit escape mode low power transmit data valid M_TxValidEsc_dl_l_1 |
| 1 | ISO_M_TXLPDTEESC_DL_L_1 | R/W | 0h | Transmit escape mode low power data M_TxLPDTEsc_dl_l_1 |
| 0 | ISO_M_TXREQUESTESC_DL_L_1 | R/W | 0h | Transmit escape mode request M_TxRequestEsc_dl_l_1 |

12.263 DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L1 Register (Offset = C34h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L1 is shown in [Figure 12-263](#) and described in [Table 12-528](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L1

Table 12-527.
DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L1 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C34h |

Figure 12-263. DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L1 Register

| | | | | | | | |
|----------------------------|---------------------------|----|----|----|----------------------------|-----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_15_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_15_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_15_X | ISO_M_RXDATAESC_DL_L_1 | | | | | | |
| R-0h | R-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_M_RXDAT AESC_DL_L_1 | ISO_M_RXTRIGGERESC_DL_L_1 | | | | ISO_M_RXULP SESC_DL_L_1 | ISO_M_RXVALI DESC_DL_L_1 | ISO_M_RXLPD TESC_DL_L_1 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-528. DPHY_TX_ISO_PHY_ISO_DL_RX_ESC_L1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | ISO_BF_31_15_X | R | 0h | Reserved |
| 14-7 | ISO_M_RXDATAESC_DL_L_1 | R | 0h | Receive escape mode low power receive data M_RxDataEsc_dl_l_1 [7:0] |
| 6-3 | ISO_M_RXTRIGGERESC_DL_L_1 | R | 0h | Receive escape mode low power trigger state M_RxTriggerEsc_dl_l_1 [3:0] |
| 2 | ISO_M_RXULPSESC_DL_L_1 | R | 0h | Receive escape mode low power ultra low power state M_RxULPSEsc_dl_l_1 |
| 1 | ISO_M_RXVALIDESC_DL_L_1 | R | 0h | Receive escape mode low power receive data M_RxValidEsc_dl_l_1 |
| 0 | ISO_M_RXLPDTEDESC_DL_L_1 | R | 0h | Receive escape mode low power data M_RxLPDTEsc_dl_l_1 |

12.264 DPHY_TX_ISO_PHY_ISO_SPARE_1 Register (Offset = C38h) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_SPARE_1 is shown in [Figure 12-264](#) and described in [Table 12-530](#).

Return to [Summary Table](#).

PHY_ISO_SPARE_1

**Table 12-529. DPHY_TX_ISO_PHY_ISO_SPARE_1
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C38h |

Figure 12-264. DPHY_TX_ISO_PHY_ISO_SPARE_1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ISO_SPARE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-530. DPHY_TX_ISO_PHY_ISO_SPARE_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|----------------|
| 31-0 | ISO_SPARE | R | 0h | Spare register |

12.265 DPHY_TX_ISO_PHY_ISO_SPARE_2 Register (Offset = C3Ch) [reset = 0h]

DPHY_TX_ISO_PHY_ISO_SPARE_2 is shown in [Figure 12-265](#) and described in [Table 12-532](#).

Return to [Summary Table](#).

PHY_ISO_SPARE_2

**Table 12-531. DPHY_TX_ISO_PHY_ISO_SPARE_2
Instances**

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C3Ch |

Figure 12-265. DPHY_TX_ISO_PHY_ISO_SPARE_2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ISO_SPARE_X | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-532. DPHY_TX_ISO_PHY_ISO_SPARE_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|----------------|
| 31-0 | ISO_SPARE_X | R | 0h | Spare register |

12.266 DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L2 Register (Offset = C40h) [reset = 0h]

DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L2 is shown in [Figure 12-266](#) and described in [Table 12-534](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L2

Table 12-533.
DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L2
Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C40h |

Figure 12-266. DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L2 Register

| | | | | | | | |
|-----------------|----|----|----|---------------------------|------------------------------------|------------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_4_X_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_4_X_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_4_X_X | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_BF_31_4_X_X | | | | ISO_LANE_RE ADY_DL_L_2 | ISO_M_DATA_ SWAPDPDN_D L_L_2 | ISO_FORCETX STOPMODE_D L_L_2 | ISO_M_TURNR EQUEST_DL_L _2 |
| R-0h | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-534. DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|---|
| 31-4 | ISO_BF_31_4_X_X | R | 0h | Reserved |
| 3 | ISO_LANE_READY_DL_L_2 | R | 0h | High Speed data lane ready lane_ready_dl_l_2 |
| 2 | ISO_M_DATA_SWAPDPDN_DL_L_2 | R/W | 0h | Swaps the tx_p and tx_m differential pins M_Data_SwapDpDn_dl_l_2 |
| 1 | ISO_FORCETXSTOPMODE_DL_L_2 | R/W | 0h | Drives the lane forcing into stop state ForceTxStopMode_dl_l_2 |
| 0 | ISO_M_TURNREQUEST_DL_L_2 | R/W | 0h | Drives the Turnaround request M_TurnRequest_dl_l_2 |

12.267 DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L2 Register (Offset = C44h) [reset = X]

DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L2 is shown in [Figure 12-267](#) and described in [Table 12-536](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L2

Table 12-535.
DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L2 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C44h |

Figure 12-267. DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L2 Register

| | | | | | | | |
|---------------------|----|----|----|--------------------------|----------------------------|------------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_16_X_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_16_X_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_TXDATAHS_DL_L_2 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ISO_TXREADY HS_DL_L_2 | ISO_TXSKEWC ALHS_DL_L_2 | ISO_TXSKEWC ALHSINIT_DL_ L_2 | ISO_TXREQUE STHS_DL_L_2 |
| R/W-X | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-536. DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-16 | ISO_BF_31_16_X_X | R | 0h | Reserved |
| 15-8 | ISO_TXDATAHS_DL_L_2 | R/W | 0h | Drives the high speed transmission data TxDataHS_dl_l_2 [7:0] |
| 7-4 | RESERVED | R/W | X | |
| 3 | ISO_TXREADYHS_DL_L_2 | R | 0h | Stores the high speed data transmission ready TxReadyHS_dl_l_2 |
| 2 | ISO_TXSKEWCALHS_DL_L_2 | R/W | 0h | Drives transmission skew calibration periodic TxSkewCalHS_dl_l_2 |
| 1 | ISO_TXSKEWCALHSINIT_DL_L_2 | R/W | 0h | Drives to run the initial skew calibration TxSkewCalHSInit_dl_l_2 |
| 0 | ISO_TXREQUESTHS_DL_L_2 | R/W | 0h | Drives the High Speed Data Transmission Request TxRequestHS_dl_l_2 |

12.268 DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2 Register (Offset = C48h) [reset = X]

DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2 is shown in [Figure 12-268](#) and described in [Table 12-538](#).

Return to [Summary Table](#).

PHY_ISO_DL_TX_ESC_L2

Table 12-537.
DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2
Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C48h |

Figure 12-268. DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------------|-------------------------|-------------------------|----------------------------|----------------------------|--------------------------|------------------------|-------------------------------|
| ISO_BF_31_28_X_X | | | | ISO_M_ULPSACTIVENOT_DL_L_2 | ISO_M_DIRECTION_DL_L_2 | ISO_M_STOPSTATE_DL_L_2 | ISO_M_ERRCONTENTIONLP1_DL_L_2 |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_M_ERRCONTENTIONLP0_DL_L_2 | ISO_M_ERRSYNCESC_DL_L_2 | ISO_M_ERRCONTROL_DL_L_2 | ISO_M_ERRESC_DL_L_2 | ISO_M_TXTRIGGERESC_DL_L_2 | | | |
| R-0h | R-0h | R-0h | R-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_M_TXDATAESC_DL_L_2 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ISO_M_TXREADYESC_DL_L_2 | ISO_M_TXULPSEXITESC_DL_L_2 | ISO_M_TXULPSESC_DL_L_2 | ISO_M_TXVALIDDESC_DL_L_2 | ISO_M_TXLPDTESC_DL_L_2 | ISO_M_TXREQUESTESC_DL_L_2 |
| R/W-X | | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-538. DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-28 | ISO_BF_31_28_X_X | R | 0h | Reserved |
| 27 | ISO_M_ULPSACTIVENOT_DL_L_2 | R | 0h | Lane ULPS Active state M_ULPSActiveNot_dl_l_2 |
| 26 | ISO_M_DIRECTION_DL_L_2 | R | 0h | Lane transmit / receive direction M_Direction_dl_l_2 |
| 25 | ISO_M_STOPSTATE_DL_L_2 | R | 0h | Lane Stop State M_StopState_dl_l_2 |
| 24 | ISO_M_ERRCONTENTIONLP1_DL_L_2 | R | 0h | LP1 contention Error M_ErrContentionLP1_dl_l_2 |
| 23 | ISO_M_ERRCONTENTIONLP0_DL_L_2 | R | 0h | LP1 contention Error M_ErrContentionLP0_dl_l_2 |
| 22 | ISO_M_ERRSYNCESC_DL_L_2 | R | 0h | Low power data transmission sync error M_ErrSyncEsc_dl_l_2 |
| 21 | ISO_M_ERRCONTROL_DL_L_2 | R | 0h | Control Error M_ErrControl_dl_l_2 |
| 20 | ISO_M_ERRESC_DL_L_2 | R | 0h | Escape Entry Error M_ErrEsc_dl_l_2 |
| 19-16 | ISO_M_TXTRIGGERESC_DL_L_2 | R/W | 0h | Transmit escape mode trigger M_TxTriggerEsc_dl_l_2 [3:0] |

Table 12-538. DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 15-8 | ISO_M_TXDATAESC_DL_L_2 | R/W | 0h | Transmit escape mode low power transmit data M_TxDataEsc_dl_l_2 [7:0] |
| 7-6 | RESERVED | R/W | X | |
| 5 | ISO_M_TXREADYESC_DL_L_2 | R | 0h | Transmit escape mode low power transmit data ready M_TxReadyEsc_dl_l_2 |
| 4 | ISO_M_TXULPSEXITESC_DL_L_2 | R/W | 0h | Initiate exit of ULPS M_TxULPSExitEsc_dl_l_2 |
| 3 | ISO_M_TXULPSESC_DL_L_2 | R/W | 0h | Transmit escape mode ultra low power state M_TxULPSEsc_dl_l_2 |
| 2 | ISO_M_TXVALIDESC_DL_L_2 | R/W | 0h | Transmit escape mode low power transmit data valid M_TxValidEsc_dl_l_2 |
| 1 | ISO_M_TXLPDTEESC_DL_L_2 | R/W | 0h | Transmit escape mode low power data M_TxLPDTEsc_dl_l_2 |
| 0 | ISO_M_TXREQUESTESC_DL_L_2 | R/W | 0h | Transmit escape mode request M_TxRequestEsc_dl_l_2 |

12.269 DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 Register (Offset = C4Ch) [reset = 0h]

DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 is shown in [Figure 12-269](#) and described in [Table 12-540](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L2

Table 12-539.
DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L2
Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C4Ch |

Figure 12-269. DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 Register

| | | | | | | | |
|------------------------|---------------------------|----|----|----|----------------------------|-----------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_15_X_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_15_X_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_15_X_X | ISO_M_RXDATAESC_DL_L_2 | | | | | | |
| R-0h | R-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_M_RXDATAESC_DL_L_2 | ISO_M_RXTRIGGERESC_DL_L_2 | | | | ISO_M_RXULP SESC_DL_L_2 | ISO_M_RXVALI DESC_DL_L_2 | ISO_M_RXLPD TESC_DL_L_2 |
| R-0h | R-0h | | | | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 12-540. DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | ISO_BF_31_15_X_X | R | 0h | Reserved |
| 14-7 | ISO_M_RXDATAESC_DL_L_2 | R | 0h | Receive escape mode low power receive data M_RxDataEsc_dl_l_2 [7:0] |
| 6-3 | ISO_M_RXTRIGGERESC_DL_L_2 | R | 0h | Receive escape mode low power trigger state M_RxTriggerEsc_dl_l_2 [3:0] |
| 2 | ISO_M_RXULPSESC_DL_L_2 | R | 0h | Receive escape mode low power ultra low power state M_RxULPSEsc_dl_l_2 |
| 1 | ISO_M_RXVALIDESC_DL_L_2 | R | 0h | Receive escape mode low power receive data M_RxValidEsc_dl_l_2 |
| 0 | ISO_M_RXLPDTEESC_DL_L_2 | R | 0h | Receive escape mode low power data M_RxLPDTEsc_dl_l_2 |

12.270 DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L3 Register (Offset = C50h) [reset = 0h]

DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L3 is shown in [Figure 12-270](#) and described in [Table 12-542](#).

Return to [Summary Table](#).

PHY_ISO_DL_CTRL_L3

Table 12-541.
DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L3
Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C50h |

Figure 12-270. DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L3 Register

| | | | | | | | |
|-------------------|----|----|----|---------------------------|------------------------------------|------------------------------------|----------------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_4_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_4_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_4_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_BF_31_4_X_X_X | | | | ISO_LANE_RE ADY_DL_L_3 | ISO_M_DATA_ SWAPDPDN_D L_L_3 | ISO_FORCETX STOPMODE_D L_L_3 | ISO_M_TURNR EQUEST_DL_L _3 |
| R-0h | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-542. DPHY_TX_ISO_LDD_PHY_ISO_DL_CTRL_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|---|
| 31-4 | ISO_BF_31_4_X_X_X | R | 0h | Reserved |
| 3 | ISO_LANE_READY_DL_L_3 | R | 0h | High Speed data lane ready lane_ready_dl_l_3 |
| 2 | ISO_M_DATA_SWAPDPDN_DL_L_3 | R/W | 0h | Swaps the tx_p and tx_m differential pins M_Data_SwapDpDn_dl_l_3 |
| 1 | ISO_FORCETXSTOPMODE_DL_L_3 | R/W | 0h | Drives the lane forcing into stop state ForceTxStopMode_dl_l_3 |
| 0 | ISO_M_TURNREQUEST_DL_L_3 | R/W | 0h | Drives the Turnaround request M_TurnRequest_dl_l_3 |

12.271 DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L3 Register (Offset = C54h) [reset = X]

DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L3 is shown in [Figure 12-271](#) and described in [Table 12-544](#).

Return to [Summary Table](#).

PHY_ISO_DL_HS_L3

Table 12-543.
DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L3 Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C54h |

Figure 12-271. DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L3 Register

| | | | | | | | |
|---------------------|----|----|----|--------------------------|----------------------------|------------------------------------|----------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_16_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_16_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_TXDATAHS_DL_L_3 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | ISO_TXREADY HS_DL_L_3 | ISO_TXSKEWC ALHS_DL_L_3 | ISO_TXSKEWC ALHSINIT_DL_ L_3 | ISO_TXREQUE STHS_DL_L_3 |
| R/W-X | | | | R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-544. DPHY_TX_ISO_LDD_PHY_ISO_DL_HS_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------------------|------|-------|--|
| 31-16 | ISO_BF_31_16_X_X_X | R | 0h | Reserved |
| 15-8 | ISO_TXDATAHS_DL_L_3 | R/W | 0h | Drives the high speed transmission data TxDataHS_dl_l_3 [7:0] |
| 7-4 | RESERVED | R/W | X | |
| 3 | ISO_TXREADYHS_DL_L_3 | R | 0h | Stores the high speed data transmission ready TxReadyHS_dl_l_3 |
| 2 | ISO_TXSKEWCALHS_DL_L_3 | R/W | 0h | Drives transmission skew calibration periodic TxSkewCalHS_dl_l_3 |
| 1 | ISO_TXSKEWCALHSINIT_DL_L_3 | R/W | 0h | Drives to run the initial skew calibration TxSkewCalHSInit_dl_l_3 |
| 0 | ISO_TXREQUESTHS_DL_L_3 | R/W | 0h | Drives the High Speed Data Transmission Request TxRequestHS_dl_l_3 |

12.272 DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3 Register (Offset = C58h) [reset = X]

DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3 is shown in [Figure 12-272](#) and described in [Table 12-546](#).

Return to [Summary Table](#).

PHY_ISO_DL_TX_ESC_L3

Table 12-545.
DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3
Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C58h |

Figure 12-272. DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------------------|-------------------------|-------------------------|----------------------------|----------------------------|--------------------------|------------------------|-------------------------------|
| ISO_BF_31_28_X_X_X | | | | ISO_M_ULPSACTIVENOT_DL_L_3 | ISO_M_DIRECTION_DL_L_3 | ISO_M_STOPSTATE_DL_L_3 | ISO_M_ERRCONTENTIONLP1_DL_L_3 |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_M_ERRCONTENTIONLP0_DL_L_3 | ISO_M_ERRSYNCESC_DL_L_3 | ISO_M_ERRCONTROL_DL_L_3 | ISO_M_ERRESC_DL_L_3 | ISO_M_TXTRIGGERESC_DL_L_3 | | | |
| R-0h | R-0h | R-0h | R-0h | R/W-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_M_TXDATAESC_DL_L_3 | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | ISO_M_TXREADYESC_DL_L_3 | ISO_M_TXULPSEXITESC_DL_L_3 | ISO_M_TXULPSESC_DL_L_3 | ISO_M_TXVALIDDESC_DL_L_3 | ISO_M_TXLPDTESC_DL_L_3 | ISO_M_TXREQUESTESC_DL_L_3 |
| R/W-X | | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-546. DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------------------|------|-------|--|
| 31-28 | ISO_BF_31_28_X_X_X | R | 0h | Reserved |
| 27 | ISO_M_ULPSACTIVENOT_DL_L_3 | R | 0h | Lane ULPS Active state M_ULPSActiveNot_dl_l_3 |
| 26 | ISO_M_DIRECTION_DL_L_3 | R | 0h | Lane transmit / receive direction M_Direction_dl_l_3 |
| 25 | ISO_M_STOPSTATE_DL_L_3 | R | 0h | Lane Stop State M_StopState_dl_l_3 |
| 24 | ISO_M_ERRCONTENTIONLP1_DL_L_3 | R | 0h | LP1 contention Error M_ErrContentionLP1_dl_l_3 |
| 23 | ISO_M_ERRCONTENTIONLP0_DL_L_3 | R | 0h | LP1 contention Error M_ErrContentionLP0_dl_l_3 |
| 22 | ISO_M_ERRSYNCESC_DL_L_3 | R | 0h | Low power data transmission sync error M_ErrSyncEsc_dl_l_3 |
| 21 | ISO_M_ERRCONTROL_DL_L_3 | R | 0h | Control Error M_ErrControl_dl_l_3 |
| 20 | ISO_M_ERRESC_DL_L_3 | R | 0h | Escape Entry Error M_ErrEsc_dl_l_3 |
| 19-16 | ISO_M_TXTRIGGERESC_DL_L_3 | R/W | 0h | Transmit escape mode trigger M_TxTriggerEsc_dl_l_3 [3:0] |

Table 12-546. DPHY_TX_ISO_LDD_PHY_ISO_DL_TX_ESC_L3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------------------------|------|-------|--|
| 15-8 | ISO_M_TXDATAESC_DL_L_3 | R/W | 0h | Transmit escape mode low power transmit data M_TxDataEsc_dl_l_3 [7:0] |
| 7-6 | RESERVED | R/W | X | |
| 5 | ISO_M_TXREADYESC_DL_L_3 | R | 0h | Transmit escape mode low power transmit data ready M_TxReadyEsc_dl_l_3 |
| 4 | ISO_M_TXULPSEXITESC_DL_L_3 | R/W | 0h | Initiate exit of ULPS M_TxULPSExitEsc_dl_l_3 |
| 3 | ISO_M_TXULPSESC_DL_L_3 | R/W | 0h | Transmit escape mode ultra low power state M_TxULPSEsc_dl_l_3 |
| 2 | ISO_M_TXVALIDESC_DL_L_3 | R/W | 0h | Transmit escape mode low power transmit data valid M_TxValidEsc_dl_l_3 |
| 1 | ISO_M_TXLPDTEESC_DL_L_3 | R/W | 0h | Transmit escape mode low power data M_TxLPDTEsc_dl_l_3 |
| 0 | ISO_M_TXREQUESTESC_DL_L_3 | R/W | 0h | Transmit escape mode request M_TxRequestEsc_dl_l_3 |

12.273 DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 Register (Offset = C5Ch) [reset = 0h]

DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 is shown in [Figure 12-273](#) and described in [Table 12-548](#).

Return to [Summary Table](#).

PHY_ISO_DL_RX_ESC_L3

Table 12-547.
DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L3
Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0C5Ch |

Figure 12-273. DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 Register

| | | | | | | | |
|----------------------------|---------------------------|----|----|----------------------------|-----------------------------|----------------------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ISO_BF_31_15_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ISO_BF_31_15_X_X_X | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ISO_BF_31_15_X_X_X | ISO_M_RXDATAESC_DL_L_3 | | | | | | |
| R-0h | R-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISO_M_RXDAT AESC_DL_L_3 | ISO_M_RXTRIGGERESC_DL_L_3 | | | ISO_M_RXULP SESC_DL_L_3 | ISO_M_RXVALI DESC_DL_L_3 | ISO_M_RXLPD TESC_DL_L_3 | |
| R-0h | R-0h | | | R-0h | R-0h | R-0h | |

LEGEND: R = Read Only; -n = value after reset

Table 12-548. DPHY_TX_ISO_LDD_PHY_ISO_DL_RX_ESC_L3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------------------|------|-------|---|
| 31-15 | ISO_BF_31_15_X_X_X | R | 0h | Reserved |
| 14-7 | ISO_M_RXDATAESC_DL_L_3 | R | 0h | Receive escape mode low power receive data M_RxDataEsc_dl_l_3 [7:0] |
| 6-3 | ISO_M_RXTRIGGERESC_DL_L_3 | R | 0h | Receive escape mode low power trigger state M_RxTriggerEsc_dl_l_3 [3:0] |
| 2 | ISO_M_RXULPSESC_DL_L_3 | R | 0h | Receive escape mode low power ultra low power state M_RxULPSEsc_dl_l_3 |
| 1 | ISO_M_RXVALIDESC_DL_L_3 | R | 0h | Receive escape mode low power receive data M_RxValidEsc_dl_l_3 |
| 0 | ISO_M_RXLPDTEESC_DL_L_3 | R | 0h | Receive escape mode low power data M_RxLPDTEsc_dl_l_3 |

12.274 DPHY_TX_MOD_VER Register (Offset = F00h) [reset = 69923801h]

DPHY_TX_MOD_VER is shown in [Figure 12-274](#) and described in [Table 12-550](#).

Return to [Summary Table](#).

The Module and Version Register identifies the module identifier and revision of the WIZ16B8M4CDT module.

Table 12-549. DPHY_TX_MOD_VER Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0F00h |

Figure 12-274. DPHY_TX_MOD_VER Register

| | | | | | | | |
|-----------------|----|----------------|----|-----------|----------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SCHEME | | BU | | MODULE_ID | | | |
| R-1h | | R-2h | | R-992h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MODULE_ID | | | | | | | |
| R-992h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RTL_VERSION | | | | | MAJOR_REVISION | | |
| R-7h | | | | | R-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM_REVISION | | MINOR_REVISION | | | | | |
| R-0h | | R-1h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 12-550. DPHY_TX_MOD_VER Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------|------|-------|-------------------------|
| 31-30 | SCHEME | R | 1h | Module Scheme |
| 29-28 | BU | R | 2h | Module Business Unit |
| 27-16 | MODULE_ID | R | 992h | WIZ16B8M4CDT module ID. |
| 15-11 | RTL_VERSION | R | 7h | RTL Version. |
| 10-8 | MAJOR_REVISION | R | 0h | Major Revision. |
| 7-6 | CUSTOM_REVISION | R | 0h | Custom Revision. |
| 5-0 | MINOR_REVISION | R | 1h | Minor Revision. |

12.275 DPHY_TX_PLL_CTRL Register (Offset = F04h) [reset = X]

DPHY_TX_PLL_CTRL is shown in [Figure 12-275](#) and described in [Table 12-552](#).

Return to [Summary Table](#).

Sets the PLL info.

Table 12-551. DPHY_TX_PLL_CTRL Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0F04h |

Figure 12-275. DPHY_TX_PLL_CTRL Register

| | | | | | | | |
|-----------|-------------|-----------|-----------|----------|----|-----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PLL_LOCK | PSO_DISABLE | PLL_PSO | PLL_PD | RESERVED | | PLL_FBDIV | |
| R-0h | R/W-0h | R/W-0h | R/W-1h | R/W-X | | R/W-FFh | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PLL_FBDIV | | | | | | | |
| R/W-FFh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | PLL_OPDIV | | | | | |
| R/W-X | | R/W-1h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | PLL_IPDIV | | | | |
| R/W-X | | | R/W-1h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 12-552. DPHY_TX_PLL_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31 | PLL_LOCK | R | 0h | Signal to indicate that PLL has got locked. 1: PLL locked to required frequency 0: PLL not yet locked |
| 30 | PSO_DISABLE | R/W | 0h | Disables the ability to switch off the analog switched power islands in the lane when in the ultra-low power state |
| 29 | PLL_PSO | R/W | 0h | Power Shut Off signal for PLL 1: PLL shutoff 0: PLL power ON |
| 28 | PLL_PD | R/W | 1h | Power down signal for PLL (Does not switch off the PLL supply) 1: PLL is powered down 0: PLL is active |
| 27-26 | RESERVED | R/W | X | |
| 25-16 | PLL_FBDIV | R/W | FFh | DPHY TX PLL VCO Feedback Divider ratio. Feedback divider value = ROUND ((Data Rate * 2 * pll_opdiv * pll_ipdiv) / PLL reference clock frequency) |
| 15-14 | RESERVED | R/W | X | |
| 13-8 | PLL_OPDIV | R/W | 1h | DPHY TX PLL OUTCLK Divider ratio. 6'h 01: Div by 1, 2.5 Gbps - 1.25 Gbps 6'h 02: Div by 2, 1.24 Gbps - 630 Mbps 6'h 04: Div by 4, 620 Mbps - 320 Mbps 6'h 08: Div by 8, 310 Mbps - 160 Mbps 6'h 10: Div by 16, 150 Mbps - 80 Mbps |
| 7-5 | RESERVED | R/W | X | |

Table 12-552. DPHY_TX_PLL_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 4-0 | PLL_IPDIV | R/W | 1h | DPHY TX PLL REFCLK Input Divider ratio. 5'h 01: Div by 1, 9.6 MHz - <19.2 MHz 5'h 02: Div by 2, 19.2 MHz - <38.4 MHz 5'h 04: Div by 4, 38.4 MHz - < 76.8 MHz 5'h 08: Div by 8, 76.8 MHz - < 150 MHz |

12.276 DPHY_TX_STATUS Register (Offset = F08h) [reset = X]

DPHY_TX_STATUS is shown in [Figure 12-276](#) and described in [Table 12-554](#).

Return to [Summary Table](#).

The DPHY_TX_STATUS register reports DPHY_TX_STATUS of the DPHYTS sub module.

Table 12-553. DPHY_TX_STATUS Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0F08h |

Figure 12-276. DPHY_TX_STATUS Register

| | | | | | | | |
|-------------|----------|----|----|----|------------------|----------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| O_CMN_READY | RESERVED | | | | | | |
| R-0h | R-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | O_SUPPLY_CORE_PG | O_SUPPLY_IO_PG | RESERVED |
| R-X | | | | | R-0h | R-0h | R-X |

LEGEND: R = Read Only; -n = value after reset

Table 12-554. DPHY_TX_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31 | O_CMN_READY | R | 0h | System Should check this during Power up Initialisation |
| 30-3 | RESERVED | R | X | |
| 2 | O_SUPPLY_CORE_PG | R | 0h | The indicates the core supply is good. |
| 1 | O_SUPPLY_IO_PG | R | 0h | The indicates the IO supply is good. |
| 0 | RESERVED | R | X | |

12.277 DPHY_TX_RST_CTRL Register (Offset = F0Ch) [reset = X]

DPHY_TX_RST_CTRL is shown in [Figure 12-277](#) and described in [Table 12-556](#).

Return to [Summary Table](#).

Sets the RST info.

Table 12-555. DPHY_TX_RST_CTRL Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0F0Ch |

Figure 12-277. DPHY_TX_RST_CTRL Register

| | | | | | | | |
|---------------|----------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LANE_RSTB_CMN | RESERVED | | | | | | |
| R/W-0h | R/W-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-556. DPHY_TX_RST_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31 | LANE_RSTB_CMN | R/W | 0h | DPHY System Reset for Common Module - required to be released after APB register programming See DPHY PMA specification for details of DPHY power up sequence |
| 30-0 | RESERVED | R/W | X | |

12.278 DPHY_TX_PSM_FREQ Register (Offset = F10h) [reset = X]

DPHY_TX_PSM_FREQ is shown in [Figure 12-278](#) and described in [Table 12-558](#).

Return to [Summary Table](#).

The PSM Frequency register configures the so that it knows hoe fast the PSM clock is.

Table 12-557. DPHY_TX_PSM_FREQ Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0F10h |

Figure 12-278. DPHY_TX_PSM_FREQ Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | PSM_CLOCK_FREQ | | | | | | | |
| R/W-X | | | | | | | | R/W-1h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-558. DPHY_TX_PSM_FREQ Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7-0 | PSM_CLOCK_FREQ | R/W | 1h | Static value based on System PSM clock frequency. The signal must be driven with a value such that the internal psm frequency of the divided psm clock is 1 MHz |

12.279 DPHY_TX_IPCONFIG Register (Offset = F14h) [reset = X]

DPHY_TX_IPCONFIG is shown in [Figure 12-279](#) and described in [Table 12-560](#).

Return to [Summary Table](#).

IP Config

Table 12-559. DPHY_TX_IPCONFIG Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0F14h |

Figure 12-279. DPHY_TX_IPCONFIG Register

| | | | | | | | |
|----------|----------|----|----|----|--------------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSO_CMN | RESERVED | | | | | | |
| R/W-0h | R/W-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | IPCONFIG_CMN | | |
| R/W-X | | | | | R/W-1h | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-560. DPHY_TX_IPCONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31 | PSO_CMN | R/W | 0h | Power Shutoff signal for CMN 1: CMN is power OFF 0: CMN is power ON |
| 30-3 | RESERVED | R/W | X | |
| 2-0 | IPCONFIG_CMN | R/W | 1h | This signal decides which clock lane acts as master clock lane to all data lanes. Needed only for RXIP. Bit[2]: Reserved CASE {Bit[1],Bit[0]}: 00: Left RX clk lane provides clock to all left and right data lanes. 01: Left RX clk lane provides clock to all right data lanes, Right RX clk lane provides clock to all left data lanes. 10: Right RX clk lane provides clock to all right data lanes, Left RX clk lane provides clock to all left data lanes. 11: Right RX clk lane provides clock to all left and right data lanes. |

12.280 DPHY_TX_PLLRES Register (Offset = FF8h) [reset = X]

DPHY_TX_PLLRES is shown in [Figure 12-280](#) and described in [Table 12-562](#).

Return to [Summary Table](#).

The PLL Reserved register is not being used currently

Table 12-561. DPHY_TX_PLLRES Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0FF8h |

Figure 12-280. DPHY_TX_PLLRES Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|---------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | PLLREFSEL_CMN | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-562. DPHY_TX_PLLRES Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|--|
| 31-8 | RESERVED | R/W | X | |
| 7-0 | PLLREFSEL_CMN | R/W | 0h | PLL frequency range. This signal is not being used currently. Should be 8'd0 |

12.281 DPHY_TX_DIAG_TEST Register (Offset = FFCh) [reset = 0h]

DPHY_TX_DIAG_TEST is shown in [Figure 12-281](#) and described in [Table 12-564](#).

Return to [Summary Table](#).

The Diagnostic Test Register allows the system to validate the read and write of all data bits.

Table 12-563. DPHY_TX_DIAG_TEST Instances

| Instance | Physical Address |
|----------|------------------|
| DPHY_TX0 | 0448 0FFCh |

Figure 12-281. DPHY_TX_DIAG_TEST Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DIAG_REG | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 12-564. DPHY_TX_DIAG_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|----------------------|
| 31-0 | DIAG_REG | R/W | 0h | Diagnostic register. |

13 VPFE Registers

This section describes VPFE Configuration registers and VPFE RAT module registers.

13.1 VPFE Configuration Registers

Table 13-2 lists the memory-mapped registers for the VPFE Configuration registers. All register offset addresses not listed in Table 13-2 should be considered as reserved locations and the register contents should not be modified.

VPFE Registers

Table 13-1. VPFE Instances

| Instance | Base Address |
|------------|--------------|
| VPFE0_VPFE | 02F0 8000h |

Table 13-2. VPFE Registers

| Offset | Acronym | Register Name | VPFE0_VPFE Physical Address |
|--------|-------------------------------------|---------------|-----------------------------|
| 0h | VPFE_REVISION | | 02F0 8000h |
| 4h | VPFE_PCR | | 02F0 8004h |
| 8h | VPFE_SYNMODE | | 02F0 8008h |
| Ch | VPFE_HD_VD_WID | | 02F0 800Ch |
| 10h | VPFE_PIX_LINES | | 02F0 8010h |
| 14h | VPFE_HORZ_INFO | | 02F0 8014h |
| 18h | VPFE_VERT_START | | 02F0 8018h |
| 1Ch | VPFE_VERT_LINES | | 02F0 801Ch |
| 20h | VPFE_CULLING | | 02F0 8020h |
| 24h | VPFE_HSIZE_OFF | | 02F0 8024h |
| 28h | VPFE_SDOFST | | 02F0 8028h |
| 2Ch | VPFE_SDR_ADDR | | 02F0 802Ch |
| 30h | VPFE_CLAMP | | 02F0 8030h |
| 34h | VPFE_DCSUB | | 02F0 8034h |
| 38h | VPFE_COLPTN | | 02F0 8038h |
| 3Ch | VPFE_BLKCMP | | 02F0 803Ch |
| 48h | VPFE_VDINT | | 02F0 8048h |
| 4Ch | VPFE_ALAW | | 02F0 804Ch |
| 50h | VPFE_REC656IF | | 02F0 8050h |
| 54h | VPFE_CCDCFG | | 02F0 8054h |
| 98h | VPFE_DMA_CNTL | | 02F0 8098h |
| 104h | VPFE_SYSCONFIG | | 02F0 8104h |
| 108h | VPFE_CONFIG | | 02F0 8108h |
| 110h | VPFE_IRQ_EOI | | 02F0 8110h |
| 114h | VPFE_IRQ_STATUS_RAW | | 02F0 8114h |
| 118h | VPFE_IRQ_STATUS | | 02F0 8118h |
| 11Ch | VPFE_IRQ_ENABLE_SET | | 02F0 811Ch |
| 120h | VPFE_IRQ_ENABLE_CLR | | 02F0 8120h |

13.2 VPFE_REVISION Register (Offset = 0h) [reset = X]

VPFE_REVISION is shown in [Figure 13-1](#) and described in [Table 13-4](#).

Return to [Summary Table](#).

IP Revision Identifier (X.Y.R) Used by software to track features, bugs, and compatibility

Table 13-3. VPFE_REVISION Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8000h |

Figure 13-1. VPFE_REVISION Register

| | | | | | | | |
|--------|----|----------|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SCHEME | | RESERVED | | FUNC | | | |
| R-1h | | R-X | | R-D00h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FUNC | | | | | | | |
| R-D00h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| R_RTL | | | | X_MAJOR | | | |
| R-2h | | | | R-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM | | Y_MINOR | | | | | |
| R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-4. VPFE_REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-30 | SCHEME | R | 1h | Used to distinguish between old scheme and current |
| 29-28 | RESERVED | R | X | |
| 27-16 | FUNC | R | D00h | Function value |
| 15-11 | R_RTL | R | 2h | RTL Version [R], maintained by IP design owner |
| 10-8 | X_MAJOR | R | 2h | Major Revision [X], maintained by IP specification owner |
| 7-6 | CUSTOM | R | 0h | Custom version |
| 5-0 | Y_MINOR | R | 0h | Minor Revision [Y], maintained by IP specification owner |

13.3 VPFE_PCR Register (Offset = 4h) [reset = X]

VPFE_PCR is shown in [Figure 13-2](#) and described in [Table 13-6](#).

Return to [Summary Table](#).

Peripheral Control Register

Table 13-5. VPFE_PCR Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8004h |

Figure 13-2. VPFE_PCR Register

| | | | | | | | |
|----------|----|----|----|---------|--------|------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | EXPG_EN | PG_EN | BUSY | ENABLE |
| R/W-X | | | | R/W-0h | R/W-0h | R-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-6. VPFE_PCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | |
| 3 | EXPG_EN | R/W | 0h | External pattern generator enable |
| 2 | PG_EN | R/W | 0h | Pattern generator enable |
| 1 | BUSY | R | 0h | VPFE busy bit 0h = Not busy 1h = Busy |
| 0 | ENABLE | R/W | 0h | This bit is latched by VD [start of frame] 0h = Disable 1h = Enable |

13.4 VPFE_SYNMODE Register (Offset = 8h) [reset = X]

VPFE_SYNMODE is shown in [Figure 13-3](#) and described in [Table 13-8](#).

Return to [Summary Table](#).

SYNC and Mode Set Register

Table 13-7. VPFE_SYNMODE Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8008h |

Figure 13-3. VPFE_SYNMODE Register

| | | | | | | | |
|----------|---------|--------|--------|----------|--------|--------|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | RESERVED | | WEN | VDHDEN |
| R/W-X | | | | R/W-0h | | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FLDSTAT | LPF | INPMOD | | PACK8 | DATSIZ | | |
| R-0h | R/W-0h | R/W-0h | | R/W-0h | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FLDMODE | DATAPOL | EXWEN | FLDPOL | HDPOL | VDPOL | FLDOUT | VDHDOUT |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-8. VPFE_SYNMODE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19-18 | RESERVED | R/W | 0h | |
| 17 | WEN | R/W | 0h | Data write enable Controls whether or not input raw data is written to external memory This bit is latched by VD 0h = Disable 1h = Enable |
| 16 | VDHDEN | R/W | 0h | VD/HD enable Activates internal timing generator to synchronize with external VD/HD signals This bit should be set to 1 when HD and VD signals are used at any time 0h = Disable 1h = Enable |
| 15 | FLDSTAT | R | 0h | Field status Indicates the status of the current field when in interlaced mode 0h = Odd field 1h = Even field |
| 14 | LPF | R/W | 0h | 3-tap low-pass [anti-aliasing] filter This bit is latched by VD 0h = Off 1h = On |
| 13-12 | INPMOD | R/W | 0h | Setting data input mode 0h = Raw Data 1h = YCbCr 16 bit 2h = YCbCr 8 bit 3h = Reserved |
| 11 | PACK8 | R/W | 0h | Pack to 8-bit/pixel [into external memory] 0h = Normal 16bits/pixel 1h = 8 bits/pixel |
| 10-8 | DATSIZ | R/W | 0h | CCD data width is only valid when INPMOD is set to 0 0h = 16 bits 1h = 15 bits 2h = 14 bits 3h = 13 bits 4h = 12 bits 5h = 11 bits 6h = 10 bits 7h = 8 bits |
| 7 | FLDMODE | R/W | 0h | Sensor field mode 0h = Non-interlaced 1h = interlaced |
| 6 | DATAPOL | R/W | 0h | Input data polarity 0h = Normal 1h = Ones complement |
| 5 | EXWEN | R/W | 0h | External WEN selection When set to 1 and when VDHDEN is set to 1, the WEN signal is used as the external memory write enable [to external memory] The data is stored to memory only when the external sync [HD and VD] signals are active 0h = Do not use external WEN 1h = Use external WEN |

Table 13-8. VPFE_SYNMODE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 4 | FLDPOL | R/W | 0h | Field indicator polarity 0h = Positive 1h = Negative |
| 3 | HDPOL | R/W | 0h | HD sync polarity 0h = Positive 1h = Negative |
| 2 | VDPOL | R/W | 0h | VD sync polarity 0h = Positive 1h = Negative |
| 1 | FLDOUT | R/W | 0h | Field ID Direction 0h = Input 1h = Output |
| 0 | VDHDOUT | R/W | 0h | VD/HD Sync Direction 0h = Input 1h = Output |

13.5 VPFE_HD_VD_WID Register (Offset = Ch) [reset = X]

VPFE_HD_VD_WID is shown in [Figure 13-4](#) and described in [Table 13-10](#).

Return to [Summary Table](#).

Table 13-9. VPFE_HD_VD_WID Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 800Ch |

Figure 13-4. VPFE_HD_VD_WID Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|--------|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | HDW | | | | | | | | | | | |
| R/W-X | | | | R/W-0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | VDW | | | | | | | | | | | |
| R/W-X | | | | R/W-0h | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-10. VPFE_HD_VD_WID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-28 | RESERVED | R/W | X | |
| 27-16 | HDW | R/W | 0h | Width of HD sync pulse if output HDW+1 pixel clocks HDWIDTH is not used when HD is input, ie when VDHDOUT in SYN_MODE register is cleared to '0' *This bit field is latched by VD |
| 15-12 | RESERVED | R/W | X | |
| 11-0 | VDW | R/W | 0h | Width of VD sync pulse if output VDW+1 lines VDWIDTH is not used when VD is input, ie when VDHDOUT in SYN_MODE register is cleared to '0' *This bit field is latched by VD |

13.6 VPFE_PIX_LINES Register (Offset = 10h) [reset = 0h]

VPFE_PIX_LINES is shown in [Figure 13-5](#) and described in [Table 13-12](#).

Return to [Summary Table](#).

Number of pixels in a horizontal line and number of lines in a frame

Table 13-11. VPFE_PIX_LINES Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8010h |

Figure 13-5. VPFE_PIX_LINES Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PPLN | | | | | | | | | | | | | | | | HLPFR | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-12. VPFE_PIX_LINES Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|--|
| 31-16 | PPLN | R/W | 0h | Pixels per line - number of pixel clock periods in one line HD period = PPLN+1 pixel clocks PPLN is not used when HD and VD are inputs, ie when VDHDOUT in SYN_MODE register is cleared to '0' *This bit field is latched by VD |
| 15-0 | HLPFR | R/W | 0h | Half lines per field or frame - sets number of half lines per frame or field VD period = [HLPFR+1]/2 lines HLPFR is not used when HD and VD are inputs, ie when VDHDOUT in SYN_MODE register is cleared to '0' This tells the internal timing generator to generate the sufficient number of HD pulses in between two VD pulses If the sensor is an interlaced sensor, say for example, with a total of 525 [or 526] lines, then this field should be set to 525 [or 526] This means that 525 [or 526] half lines are written for each field If the sensor is progressive, then this register should be set to be twice the number of lines to be written For example, if sensor outputs 1024 lines, this field should be set to 2048 Therefore, for interlaced sensors, this field should be set to the total number of lines For progressive sensors, this field should be set to twice the total number of lines *This bit field is latched by VD |

13.7 VPFE_HORZ_INFO Register (Offset = 14h) [reset = X]

VPFE_HORZ_INFO is shown in [Figure 13-6](#) and described in [Table 13-14](#).

Return to [Summary Table](#).

Horizontal Pixel Information Register

Table 13-13. VPFE_HORZ_INFO Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8014h |

Figure 13-6. VPFE_HORZ_INFO Register

| | | | | | | | |
|----------|--------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | SPH | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SPH | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | NPH | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NPH | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-14. VPFE_HORZ_INFO Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31 | RESERVED | R/W | X | |
| 30-16 | SPH | R/W | 0h | Start pixel, horizontal The SPH sets the pixel clock position at which data output to external memory begins, measured from the start of HD This bit field is latched by VD |
| 15 | RESERVED | R/W | X | |
| 14-0 | NPH | R/W | 0h | Number of pixels, horizontal NPH sets the number of horizontal pixels that is output to external memory = [NPH + 1] and 0xFFFF0 [ie, the number of horizontal output pixels truncates to multiples of 16] This bit field is latched by VD |

13.8 VPFE_VERT_START Register (Offset = 18h) [reset = X]

VPFE_VERT_START is shown in [Figure 13-7](#) and described in [Table 13-16](#).

Return to [Summary Table](#).

Vertical Line - Settings for the Starting Pixel Register

Table 13-15. VPFE_VERT_START Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8018h |

Figure 13-7. VPFE_VERT_START Register

| | | | | | | | |
|----------|--------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | SLV0 | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SLV0 | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | SLV1 | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SLV1 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-16. VPFE_VERT_START Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31 | RESERVED | R/W | X | |
| 30-16 | SLV0 | R/W | 0h | Start line, vertical [field 0] SLV0 sets line at which data output to external memory will begin, measured from the start of VD This bit field is latched by VD |
| 15 | RESERVED | R/W | X | |
| 14-0 | SLV1 | R/W | 0h | Start line, vertical [field 1] SLV1 sets line at which data output to external memory will begin, measured from the start of VD For a progressive sensor this field is ignored This bit field is latched by VD |

13.9 VPFE_VERT_LINES Register (Offset = 1Ch) [reset = X]

VPFE_VERT_LINES is shown in [Figure 13-8](#) and described in [Table 13-18](#).

Return to [Summary Table](#).

Number of Vertical Lines Register

Table 13-17. VPFE_VERT_LINES Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 801Ch |

Figure 13-8. VPFE_VERT_LINES Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | NLV | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-18. VPFE_VERT_LINES Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-15 | RESERVED | R/W | X | |
| 14-0 | NLV | R/W | 0h | Number of lines, vertical NLV sets the number of vertical lines that will be output to external memory The number of lines output to external memory = [NLV + 1] This bit field is latched by VD |

13.10 VPFE_CULLING Register (Offset = 20h) [reset = X]

VPFE_CULLING is shown in [Figure 13-9](#) and described in [Table 13-20](#).

Return to [Summary Table](#).

Culling Information in Horizontal and Vertical Directions Register

Table 13-19. VPFE_CULLING Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8020h |

Figure 13-9. VPFE_CULLING Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|---------|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| CULHEVN | | | | | | | | CULHODD | | | | | | | | RESERVED | | | | | | | | CULV | | | | | | | |
| R/W-FFh | | | | | | | | R/W-FFh | | | | | | | | R/W-X | | | | | | | | R/W-FFh | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-20. VPFE_CULLING Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-24 | CULHEVN | R/W | FFh | Horizontal Culling Pattern for Even Line, 8-bit mask LSB is first pixel, MSB is 8th pixel, then pattern repeats This bit field is latched by VD 0h = Culling(Deletion) 1h = Retain(to be saved in the memory) |
| 23-16 | CULHODD | R/W | FFh | Horizontal Culling Pattern for Odd Line, 8-bit mask LSB is first pixel, MSB is 8th pixel, then pattern repeats This bit field is latched by VD 0h = Culling(Deletion) 1h = Retain(to be saved in the memory) |
| 15-8 | RESERVED | R/W | X | |
| 7-0 | CULV | R/W | FFh | Vertical Culling Pattern, 8-bit mask LSB is first line, MSB is 8th line, then pattern repeats This bit field is latched by VD 0h = Culling(Deletion) 1h = Retain(to be saved in the memory) |

13.11 VPFE_HSIZE_OFF Register (Offset = 24h) [reset = X]

VPFE_HSIZE_OFF is shown in [Figure 13-10](#) and described in [Table 13-22](#).

Return to [Summary Table](#).

Horizontal Size Register

Table 13-21. VPFE_HSIZE_OFF Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8024h |

Figure 13-10. VPFE_HSIZE_OFF Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | LNOFST | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-22. VPFE_HSIZE_OFF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | LNOFST | R/W | 0h | Address offset for each line LNOFST Sets offset for each output line in external memory Either 16 or 32 pixels depending on setting of PACK8 the offset will be on a 32-byte boundary For optimal performance in the system, the address offset should be on a 256-byte boundary This bit field is latched by VD |

13.12 VPFE_SDOFST Register (Offset = 28h) [reset = X]

VPFE_SDOFST is shown in [Figure 13-11](#) and described in [Table 13-24](#).

Return to [Summary Table](#).

External Memory Line Offset Register

Table 13-23. VPFE_SDOFST Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8028h |

Figure 13-11. VPFE_SDOFST Register

| | | | | | | | |
|----------|--------|--------|----|--------|--------|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | FIINV | FOFST | | LOFST0 | | LOFST1 | |
| R/W-X | R/W-0h | R/W-0h | | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOFST1 | | LOFST2 | | | LOFST3 | | |
| R/W-0h | | R/W-0h | | | R/W-0h | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-24. VPFE_SDOFST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-15 | RESERVED | R/W | X | |
| 14 | FIINV | R/W | 0h | Field identification signal inverse This field is latched by VD 0h = Non-inverse 1h = Inverse |
| 13-12 | FOFST | R/W | 0h | Line offset value of field ID = 1 This field is latched by VD 0h = +1 line 1h = +2 lines 2h = +3 lines 3h = +4 lines |
| 11-9 | LOFST0 | R/W | 0h | Line offset values of even line and even field ID = 0 This field is latched by VD 0h = +1 line 1h = +2 lines 2h = +3 lines 3h = +4 lines 4h = -1 line 5h = -2 lines 6h = -3 lines 7h = -4 lines |
| 8-6 | LOFST1 | R/W | 0h | Line offset values of odd line and even field ID = 0 This field is latched by VD 0h = +1 line 1h = +2 lines 2h = +3 lines 3h = +4 lines 4h = -1 line 5h = -2 lines 6h = -3 lines 7h = -4 lines |
| 5-3 | LOFST2 | R/W | 0h | Line offset values of even line and odd field ID = 1 This field is latched by VD 0h = +1 line 1h = +2 lines 2h = +3 lines 3h = +4 lines 4h = -1 line 5h = -2 lines 6h = -3 lines 7h = -4 lines |
| 2-0 | LOFST3 | R/W | 0h | Line offset values of odd line and odd field ID = 1 This field is latched by VD 0h = +1 line 1h = +2 lines 2h = +3 lines 3h = +4 lines 4h = -1 line 5h = -2 lines 6h = -3 lines 7h = -4 lines |

13.13 VPFE_SDR_ADDR Register (Offset = 2Ch) [reset = 0h]

VPFE_SDR_ADDR is shown in [Figure 13-12](#) and described in [Table 13-26](#).

[Return to Summary Table.](#)

External Memory Address Register

Table 13-25. VPFE_SDR_ADDR Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 802Ch |

Figure 13-12. VPFE_SDR_ADDR Register

| | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADR_MSB | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADR_MSB | | | | | | | | | | | ADR_LSB | | | | |
| R/W-0h | | | | | | | | | | | R-0h | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-26. VPFE_SDR_ADDR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---|
| 31-5 | ADR_MSB | R/W | 0h | 32-bit external memory starting address for VPFE output This bit field is latched by VD The address should be aligned on a 32-byte boundary Therefore, the 5 LSB's are ignored Furthermore, reading this register will always show the 5 LSB's as 0 For optimal performance in the system, the address should be on a 256-byte boundary |
| 4-0 | ADR_LSB | R | 0h | 32-bit external memory starting address for VPFE output This bit field is latched by VD The address should be aligned on a 32-byte boundary Therefore, the 5 LSB's are ignored Furthermore, reading this register will always show the 5 LSB's as 0 For optimal performance in the system, the address should be on a 256-byte boundary |

13.14 VPFE_CLAMP Register (Offset = 30h) [reset = X]

VPFE_CLAMP is shown in [Figure 13-13](#) and described in [Table 13-28](#).

Return to [Summary Table](#).

Optical Black Clamping Setting Register

Table 13-27. VPFE_CLAMP Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8030h |

Figure 13-13. VPFE_CLAMP Register

| | | | | | | | |
|---------|----|--------|----|----|--------|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLAMPEN | | OBSLEN | | | OBSLN | | OBST |
| R/W-0h | | R/W-0h | | | R/W-0h | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | | | | OBST |
| | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | | | | OBST |
| | | | | | | | RESERVED |
| | | | | | | | R/W-X |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | OBGAIN |
| | | | | | | | R/W-10h |
| | | | | | | | RESERVED |
| | | | | | | | R/W-X |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-28. VPFE_CLAMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31 | CLAMPEN | R/W | 0h | Clamp enable Enable or disable clamping of CCD data based on the calculated average of optical black samples This bit is latched by VD 0h = Disable 1h = Enable |
| 30-28 | OBSLEN | R/W | 0h | Optical black sample length Number of Optical Black Sample pixels per line to include in the average calculation 0h = 1 pixels 1h = 2 pixels 2h = 4 pixels 3h = 8 pixels 4h = 16 pixels 5h = Reserved 6h = Reserved 7h = Reserved |
| 27-25 | OBSLN | R/W | 0h | Optical black sample lines Number of Optical Black Sample lines to include in the average calculation 0h = 1 lines 1h = 2 lines 2h = 4 lines 3h = 8 lines 4h = 16 lines 5h = Reserved 6h = Reserved 7h = Reserved |
| 24-10 | OBST | R/W | 0h | Start pixel of optical black samples The start pixel position of optical black samples, specified from the start of HD in pixel clocks |
| 9-5 | RESERVED | R/W | X | |
| 4-0 | OBGAIN | R/W | 10h | Gain to apply to the optical black average Multiply the optical black average with the specified gain 1Fh = 1 + 15/16 1Eh = 1 + 14/16 .. = .. 10h = 1 + 0/16 0Fh = 0 + 15/16 0Eh = 0 + 14/16 0Dh = 0 + 13/16 .. = .. 02h = 0 + 2/16 01h = 0 + 1/16 00h = 0 + 0/16 |

13.15 VPFE_DCSUB Register (Offset = 34h) [reset = X]

VPFE_DCSUB is shown in [Figure 13-14](#) and described in [Table 13-30](#).

Return to [Summary Table](#).

DC Clamp Register

Table 13-29. VPFE_DCSUB Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8034h |

Figure 13-14. VPFE_DCSUB Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | DCSUB | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-30. VPFE_DCSUB Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-14 | RESERVED | R/W | X | |
| 13-0 | DCSUB | R/W | 0h | DC level to subtract from CCD data The DC value set here is subtracted from the CCD data when OBS clamping is disabled - CLAMPCLAMPEN |

13.16 VPFE_COLPTN Register (Offset = 38h) [reset = 0h]

VPFE_COLPTN is shown in [Figure 13-15](#) and described in [Table 13-32](#).

Return to [Summary Table](#).

CCD Color Pattern Register

Table 13-31. VPFE_COLPTN Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8038h |

Figure 13-15. VPFE_COLPTN Register

| | | | | | | | |
|---------|----|---------|----|---------|----|---------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CP3LPC3 | | CP3LPC2 | | CP3LPC1 | | CP3LPC0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CP2LPC3 | | CP2LPC2 | | CP2LPC1 | | CP2LPC0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CP1LPC3 | | CP1LPC2 | | CP1LPC1 | | CP1LPC0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CP0LPC3 | | CP0LPC2 | | CP0LPC1 | | CP0LPC0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-32. VPFE_COLPTN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------|------|-------|--|
| 31-30 | CP3LPC3 | R/W | 0h | Color Pattern for 3rd Line, Pixel counter = 3 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 29-28 | CP3LPC2 | R/W | 0h | Color Pattern for 3rd Line, Pixel counter = 2 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 27-26 | CP3LPC1 | R/W | 0h | Color Pattern for 3rd Line, Pixel counter = 1 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 25-24 | CP3LPC0 | R/W | 0h | Color Pattern for 3rd Line, Pixel counter = 0 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 23-22 | CP2LPC3 | R/W | 0h | Color Pattern for 2nd Line, Pixel counter = 3 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 21-20 | CP2LPC2 | R/W | 0h | Color Pattern for 2nd Line, Pixel counter = 2 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 19-18 | CP2LPC1 | R/W | 0h | Color Pattern for 2nd Line, Pixel counter = 1 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 17-16 | CP2LPC0 | R/W | 0h | Color Pattern for 2nd Line, Pixel counter = 0 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 15-14 | CP1LPC3 | R/W | 0h | Color Pattern for 1st Line, Pixel counter = 3 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 13-12 | CP1LPC2 | R/W | 0h | Color Pattern for 1st Line, Pixel counter = 2 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 11-10 | CP1LPC1 | R/W | 0h | Color Pattern for 1st Line, Pixel counter = 1 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 9-8 | CP1LPC0 | R/W | 0h | Color Pattern for 1st Line, Pixel counter = 0 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 7-6 | CP0LPC3 | R/W | 0h | Color Pattern for 0th Line, Pixel counter = 3 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |

Table 13-32. VPFE_COLPTN Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 5-4 | CP0LPC2 | R/W | 0h | Color Pattern for 0th Line, Pixel counter = 2 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 3-2 | CP0LPC1 | R/W | 0h | Color Pattern for 0th Line, Pixel counter = 1 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |
| 1-0 | CP0LPC0 | R/W | 0h | Color Pattern for 0th Line, Pixel counter = 0 0h = R/Ye 1h = Gr/Cy 2h = Gb/G 3h = B/Mg |

13.17 VPFE_BLKCOMP Register (Offset = 3Ch) [reset = 0h]

VPFE_BLKCOMP is shown in [Figure 13-16](#) and described in [Table 13-34](#).

Return to [Summary Table](#).

Black Compensation Register

Table 13-33. VPFE_BLKCOMP Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 803Ch |

Figure 13-16. VPFE_BLKCOMP Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|--------|---|---|---|---|---|---|---|
| RYE | | | | | | | | GRCY | | | | | | | | GBG | | | | | | | | BMG | | | | | | | |
| R/W-0h | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-34. VPFE_BLKCOMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|---|
| 31-24 | RYE | R/W | 0h | Black level compensation for R/Ye pixels [-128:+127] 2's complement, MSB is sign bit |
| 23-16 | GRCY | R/W | 0h | Black level compensation for Gr/Cy pixels [-128:+127] 2's complement, MSB is sign bit |
| 15-8 | GBG | R/W | 0h | Black level compensation for Gb/G pixels [-128:+127] 2's complement, MSB is sign bit |
| 7-0 | BMG | R/W | 0h | Black level compensation for B/Mg pixels [-128:+127] 2's complement, MSB is sign bit |

13.18 VPFE_VDINT Register (Offset = 48h) [reset = X]

VPFE_VDINT is shown in [Figure 13-17](#) and described in [Table 13-36](#).

Return to [Summary Table](#).

VPFE Interrupt Control Register

Table 13-35. VPFE_VDINT Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8048h |

Figure 13-17. VPFE_VDINT Register

| | | | | | | | |
|----------|--------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | VDINT0 | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VDINT0 | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | VDINT1 | | | | | | |
| R/W-X | R/W-0h | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VDINT1 | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-36. VPFE_VDINT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31 | RESERVED | R/W | X | |
| 30-16 | VDINT0 | R/W | 0h | CCDC_VD0_INT interrupt timing Specify VDINT0 in units of horizontal lines from the start of VD pulse Resulting value is VDINT0+1 Note that if the rising edge [or falling edge if programmed] of the HD lines up with the rising edge [or falling edge if programmed] of VD, the 1st HD is not counted |
| 15 | RESERVED | R/W | X | |
| 14-0 | VDINT1 | R/W | 0h | CCDC_VD1_INT interrupt timing Specify VDINT1 in units of horizontal lines from the start of VD pulse Resulting value is VDINT1+1 Note that if the rising edge [or falling edge if programmed] of the HD lines up with the rising edge [or falling edge if programmed] of VD, the 1st HD is not counted |

13.19 VPFE_ALAW Register (Offset = 4Ch) [reset = X]

VPFE_ALAW is shown in [Figure 13-18](#) and described in [Table 13-38](#).

Return to [Summary Table](#).

VPFE_ALAW Configuration Register

Table 13-37. VPFE_ALAW Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 804Ch |

Figure 13-18. VPFE_ALAW Register

| | | | | | | | |
|----------|----|----|----|--------|--------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | CCDTBL | GWDI | | |
| R/W-X | | | | R/W-0h | R/W-4h | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-38. VPFE_ALAW Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R/W | X | |
| 3 | CCDTBL | R/W | 0h | Apply Gamma [A-LAW] to VPFE data saved to external memory 0h = Disable 1h = Enable |
| 2-0 | GWDI | R/W | 4h | A-law Width Input [A-LAW table] 0h = Bits 15-6 1h = Bits 14-5 2h = Bits 13-4 3h = Bits 12-3 4h = Bits 11-2 5h = Bits 10-1 6h = Bits 9-0 |

13.20 VPFE_REC656IF Register (Offset = 50h) [reset = X]

VPFE_REC656IF is shown in [Figure 13-19](#) and described in [Table 13-40](#).

Return to [Summary Table](#).

VPFE_REC656IF Configuration Register

Table 13-39. VPFE_REC656IF Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8050h |

Figure 13-19. VPFE_REC656IF Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | ECCFVH | R656ON |
| R/W-X | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-40. VPFE_REC656IF Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-2 | RESERVED | R/W | X | |
| 1 | ECCFVH | R/W | 0h | FVH error correction enable 0h = Disable 1h = Enable |
| 0 | R656ON | R/W | 0h | REC656 interface enable 0h = Disable 1h = Enable |

13.21 VPFE_CCDCFG Register (Offset = 54h) [reset = X]

VPFE_CCDCFG is shown in [Figure 13-20](#) and described in [Table 13-42](#).

Return to [Summary Table](#).

CCD Configuration Register

Table 13-41. VPFE_CCDCFG Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8054h |

Figure 13-20. VPFE_CCDCFG Register

| | | | | | | | |
|----------|---------|---------|---------|----------|----------|----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VDLC | MSBINVO | MSBINVI | BSWD | Y8POS | RESERVED | | WENLOG |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | BW656 | YCINSWP | RESERVED | YCOUTSWP | RESERVED | |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-X | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-42. VPFE_CCDCFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15 | VDLC | R/W | 0h | Enable latching function registers on internal VSYNC If this bit is set, all the register fields that are VSYNC latched will take on new value immediately Care should be taken not to alter fields that can cause undesired behavior to the output data 0h = Latched on VSYNC 1h = Not latched on VSYNC |
| 14 | MSBINVO | R/W | 0h | MSB of Chroma signal output inverted 0h = Normal 1h = MSB inverted |
| 13 | MSBINVI | R/W | 0h | MSB of Chroma input signal stored to SDRAM inverted 0h = Normal 1h = MSB inverted |
| 12 | BSWD | R/W | 0h | Byte Swap Data stored to SDRAM 0h = Normal 1h = Swap bytes |
| 11 | Y8POS | R/W | 0h | Location of Y signal when YCbCr 8bit data is input 0h = Even pixel 1h = Odd pixel |
| 10-9 | RESERVED | R/W | X | |
| 8 | WENLOG | R/W | 0h | Specifies CCD valid area 0h = Internal valid signal WEN signal is ANDed logically and 1h = Internal valid signal and WEN signal is ORed logically |
| 7-6 | RESERVED | R/W | 0h | |
| 5 | BW656 | R/W | 0h | The data width in CCIR656 input mode 0h = 8 bits 1h = 10 bits |
| 4 | YCINSWP | R/W | 0h | Y input [YIN [7:0]] and C input [CIN [7:0]] are swapped |
| 3 | RESERVED | R/W | 0h | |
| 2 | YCOUTSWP | R/W | 0h | Y output [YOUT [7:0]] and C output [COUT [7:0]] are swapped |

Table 13-42. VPFE_CCDCFG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 1-0 | RESERVED | R/W | X | |

13.22 VPFE_DMA_CNTL Register (Offset = 98h) [reset = X]

VPFE_DMA_CNTL is shown in [Figure 13-21](#) and described in [Table 13-44](#).

Return to [Summary Table](#).

DMA Status and Control

Table 13-43. VPFE_DMA_CNTL Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8098h |

Figure 13-21. VPFE_DMA_CNTL Register

| | | | | | | | |
|----------|----------|----|----|----|----------|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OVERFLOW | RESERVED | | | | | | |
| R/W1C-0h | R/W-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | RESERVED | | |
| R/W-X | | | | | R/W-0h | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-44. VPFE_DMA_CNTL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31 | OVERFLOW | R/W1C | 0h | DMA Overflow Flag Flag bit that is set when data is dropped due to a delay in writing data out the DMA interface This bit remains set until a 1 is written by software 0h = No overflow has occurred 1h = Overflow has occurred |
| 30-3 | RESERVED | R/W | X | |
| 2-0 | RESERVED | R/W | 0h | |

13.23 VPFE_SYSCONFIG Register (Offset = 104h) [reset = X]

VPFE_SYSCONFIG is shown in [Figure 13-22](#) and described in [Table 13-46](#).

Return to [Summary Table](#).

Clock management configuration

Table 13-45. VPFE_SYSCONFIG Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8104h |

Figure 13-22. VPFE_SYSCONFIG Register

| | | | | | | | |
|----------|----|-------------|----|----------|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | STANDBYMODE | | IDLEMODE | | RESERVED | |
| R/W-X | | R/W-2h | | R/W-2h | | R/W-X | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-46. VPFE_SYSCONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-6 | RESERVED | R/W | X | |
| 5-4 | STANDBYMODE | R/W | 2h | Configuration of the local initiator state management mode By definition, initiator may generate read/write transaction as long as it is out of STANDBY state 0h = Force Standby mode, local initiator is unconditionally placed in standby state. Backup mode, for debug only 1h = No Standby mode, local initiator is unconditionally placed out of standby state. Backup mode, for debug only 2h = Smart Standby mode, local initiator standby status depends on local conditions. IP module shall not generate wakeup events 3h = Smart Standby wakeup capable mode, local initiator standby status depends on local conditions. IP module may generate wakeup events when in standby state. Mode is only relevant if the appropriate IP module mwakeup output is implemented |

Table 13-46. VPFE_SYSCONFIG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 3-2 | IDLEMODE | R/W | 2h | <p>Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state. 0h = Force Idle mode, local targets idle state follows the systems idle requests unconditionally, regardless of the IP modules internal requirements.</p> <p>Backup mode, for debug only 1h = No idle mode, local target never enters idle state.</p> <p>Backup mode, for debug only 2h = Smart Idle mode, local targets idle eventually follows the systems idle requests, depends on the IP modules internal requirements.</p> <p>IP module shall not generate wakeup events 3h = Smart idle wakeup capable mode, local targets idle state eventually follows the systems idle requests, depending on the IP modules internal requirements.</p> <p>IP module may generate wakeup events when in idle state.</p> <p>Mode is only relevant if the appropriate IP module mwakeup output is implemented</p> |
| 1-0 | RESERVED | R/W | X | |

13.24 VPFE_CONFIG Register (Offset = 108h) [reset = X]

VPFE_CONFIG is shown in [Figure 13-23](#) and described in [Table 13-48](#).

Return to [Summary Table](#).

Module configuration register

Table 13-47. VPFE_CONFIG Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8108h |

Figure 13-23. VPFE_CONFIG Register

| | | | | | | | |
|----------|----|----|----|----|---------|---------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | VPFE_ST | VPFE_EN | PCLK_INV |
| R/W-X | | | | | R-1h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 13-48. VPFE_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | VPFE_ST | R | 1h | VPFE Master OCP interface Status 0h = OCP master interface is active 1h = OCP master interface is in standby mode |
| 1 | VPFE_EN | R/W | 0h | VPFE Master OCP interface enable Software can use this bit to enable/disable the VPFE master OCP interface. When the master OCP interface is disabled, it is placed in Standby mode. Standby mode can also be entered by using the right setting on the STANDBYMODE field in the VPFE_SYSCONFIG register. 0h = Disable VPFE master OCP interface 1h = Enable VPFE master OCP interface |
| 0 | PCLK_INV | R/W | 0h | Pixel clock inversion enable 0h = Pixel clock is not inverted, data is sampled on the rising edge of the clock 1h = pixel clock is inverted, data is sampled on the falling edge of the clock |

13.25 VPFE_IRQ_EOI Register (Offset = 110h) [reset = X]

VPFE_IRQ_EOI is shown in [Figure 13-24](#) and described in [Table 13-50](#).

Return to [Summary Table](#).

Module EOI register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 13-49. VPFE_IRQ_EOI Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8110h |

Figure 13-24. VPFE_IRQ_EOI Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | EOI |
| R/W-X | | | | | | | | | | | | | | | R/ W1C-0 h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-50. VPFE_IRQ_EOI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | EOI | R/W1C | 0h | EOI for VPFE This register allows software to acknowledge the completion of an interrupt When this register is written, an eoi_write signal is generated internal to the module and another interrupt will be triggered if the interrupt sources are still present The register will clear itself one cycle after it is written |

13.26 VPFE_IRQ_STATUS_RAW Register (Offset = 114h) [reset = X]

VPFE_IRQ_STATUS_RAW is shown in [Figure 13-25](#) and described in [Table 13-52](#).

[Return to Summary Table.](#)

Interrupt raw status register

Table 13-51. VPFE_IRQ_STATUS_RAW Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8114h |

Figure 13-25. VPFE_IRQ_STATUS_RAW Register

| | | | | | | | |
|----------|----|----|----|----|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | VD2_INT_RAW | VD1_INT_RAW | VD0_INT_RAW |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-52. VPFE_IRQ_STATUS_RAW Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | VD2_INT_RAW | R/W1S | 0h | CCDC VD2 interrupt status raw value - A read value of 1 from this register indicates that the VD2 interrupt status is 1 - When the read value is 0, software can write the value to 1 to set the interrupt - Writing a 0 to this bit has no effect |
| 1 | VD1_INT_RAW | R/W1S | 0h | CCDC VD1 interrupt status raw value - A read value of 1 from this register indicates that the VD1 interrupt status is 1 - When the read value is 0, software can write the value to 1 to set the interrupt - Writing a 0 to this bit has no effect |
| 0 | VD0_INT_RAW | R/W1S | 0h | CCDC VD0 interrupt status raw value - A read value of 1 from this register indicates that the VD0 interrupt status is 1 - When the read value is 0, software can write the value to 1 to set the interrupt - Writing a 0 to this bit has no effect |

13.27 VPFE_IRQ_STATUS Register (Offset = 118h) [reset = X]

VPFE_IRQ_STATUS is shown in [Figure 13-26](#) and described in [Table 13-54](#).

Return to [Summary Table](#).

Interrupt status register

Table 13-53. VPFE_IRQ_STATUS Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8118h |

Figure 13-26. VPFE_IRQ_STATUS Register

| | | | | | | | |
|----------|----|----|----|----|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | VD2_INT | VD1_INT | VD0_INT |
| R/W-X | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-54. VPFE_IRQ_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-3 | RESERVED | R/W | X | |
| 2 | VD2_INT | R/W1C | 0h | CCDC VD2 interrupt status value - A read value of 1 from this register indicates that the VD2 interrupt status is 1, if it is enabled - When the read value is 1, software can write a 1 to clear the interrupt - Writing a 0 to this bit has no effect |
| 1 | VD1_INT | R/W1C | 0h | CCDC VD1 interrupt status value - A read value of 1 from this register indicates that the VD2 interrupt status is 1, if it is enabled - When the read value is 1, software can write a 1 to clear the interrupt - Writing a 0 to this bit has no effect |
| 0 | VD0_INT | R/W1C | 0h | CCDC VD0 interrupt status value - A read value of 1 from this register indicates that the VD2 interrupt status is 1, if it is enabled - When the read value is 1, software can write a 1 to clear the interrupt - Writing a 0 to this bit has no effect |

13.28 VPFE_IRQ_ENABLE_SET Register (Offset = 11Ch) [reset = X]

VPFE_IRQ_ENABLE_SET is shown in [Figure 13-27](#) and described in [Table 13-56](#).

Return to [Summary Table](#).

Interrupt enable set

Table 13-55. VPFE_IRQ_ENABLE_SET Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 811Ch |

Figure 13-27. VPFE_IRQ_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | VD2_INT_EN | VD1_INT_EN | VD0_INT_EN |
| R/W-X | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-56. VPFE_IRQ_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | VD2_INT_EN | R/W1S | 0h | CCDC VD2 interrupt enable - Write 1 to enable this interrupt - Write 0 has no effect - Read 1 indicates interrupt is enabled - Read 0 indicates interrupt is not enabled |
| 1 | VD1_INT_EN | R/W1S | 0h | CCDC VD1 interrupt enable - Write 1 to enable this interrupt - Write 0 has no effect - Read 1 indicates interrupt is enabled - Read 0 indicates interrupt is not enabled |
| 0 | VD0_INT_EN | R/W1S | 0h | CCDC VD0 interrupt enable - Write 1 to enable this interrupt - Write 0 has no effect - Read 1 indicates interrupt is enabled - Read 0 indicates interrupt is not enabled |

13.29 VPFE_IRQ_ENABLE_CLR Register (Offset = 120h) [reset = X]

VPFE_IRQ_ENABLE_CLR is shown in [Figure 13-28](#) and described in [Table 13-58](#).

Return to [Summary Table](#).

Interrupt enable clear

Table 13-57. VPFE_IRQ_ENABLE_CLR Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_VPFE | 02F0 8120h |

Figure 13-28. VPFE_IRQ_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | VD2_INT_DIS | VD1_INT_DIS | VD0_INT_DIS |
| R/W-X | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-58. VPFE_IRQ_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|-------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | VD2_INT_DIS | R/W1C | 0h | CCDC VD2 interrupt disable - Write 1 to disable this interrupt - Write 0 has no effect - Read 1 indicates interrupt is enabled - Read 0 indicates interrupt is not enabled |
| 1 | VD1_INT_DIS | R/W1C | 0h | CCDC VD1 interrupt disable - Write 1 to disable this interrupt - Write 0 has no effect - Read 1 indicates interrupt is enabled - Read 0 indicates interrupt is not enabled |
| 0 | VD0_INT_DIS | R/W1C | 0h | CCDC VD0 interrupt disable - Write 1 to disable this interrupt - Write 0 has no effect - Read 1 indicates interrupt is enabled - Read 0 indicates interrupt is not enabled |

13.30 VPFE RAT Registers

Table 13-60 lists the memory-mapped registers for the VPFE RAT registers. All register offset addresses not listed in Table 13-60 should be considered as reserved locations and the register contents should not be modified.

KSBUS Region-Based Address Translation Region

Table 13-59. mmrs Instances

| Instance | Base Address |
|------------|--------------|
| VPFE0_MMRS | 02F0 0000h |

Table 13-60. MMRS Registers

| Offset | Acronym | Register Name | VPFE0_MMRS Physical Address | Section |
|--------|--|--|-----------------------------|-------------------------------|
| 0h | VPFE_PID | Revision Register | 02F0 0000h | Section 13.31 |
| 4h | VPFE_CONFIG | Config Register | 02F0 0004h | Section 13.32 |
| 20h | VPFE_CTRL_J | Region Control Register | 02F0 0020h | Section 13.33 |
| 24h | VPFE_BASE_J | Region Base Register | 02F0 0024h | Section 13.34 |
| 28h | VPFE_TRANS_L_J | Region Translated Lower Address | 02F0 0028h | Section 13.35 |
| 2Ch | VPFE_TRANS_U_J | Region Translated Upper Address | 02F0 002Ch | Section 13.36 |
| 804h | VPFE_DESTINATION_ID | Destination ID Register | 02F0 0804h | Section 13.37 |
| 820h | VPFE_EXCEPTION_LOGGING_CONTROL | Exception Logging Control Register | 02F0 0820h | Section 13.38 |
| 824h | VPFE_EXCEPTION_LOGGING_HEADER0 | Exception Logging Header 0 Register | 02F0 0824h | Section 13.39 |
| 828h | VPFE_EXCEPTION_LOGGING_HEADER1 | Exception Logging Header 1 Register | 02F0 0828h | Section 13.40 |
| 82Ch | VPFE_EXCEPTION_LOGGING_DATA0 | Exception Logging Data 0 Register | 02F0 082Ch | Section 13.41 |
| 830h | VPFE_EXCEPTION_LOGGING_DATA1 | Exception Logging Data 1 Register | 02F0 0830h | Section 13.42 |
| 834h | VPFE_EXCEPTION_LOGGING_DATA2 | Exception Logging Data 2 Register | 02F0 0834h | Section 13.43 |
| 838h | VPFE_EXCEPTION_LOGGING_DATA3 | Exception Logging Data 3 Register | 02F0 0838h | Section 13.44 |
| 840h | VPFE_EXCEPTION_PEND_SET | Exception Logging Interrupt Pending Set Register | 02F0 0840h | Section 13.45 |
| 844h | VPFE_EXCEPTION_PEND_CLEAR | Exception Logging Interrupt Pending Clear Register | 02F0 0844h | Section 13.46 |
| 848h | VPFE_EXCEPTION_ENABLE_SET | Exception Logging Interrupt Enable Set Register | 02F0 0848h | Section 13.47 |
| 84Ch | VPFE_EXCEPTION_ENABLE_CLEAR | Exception Logging Interrupt Enable Clear Register | 02F0 084Ch | Section 13.48 |
| 850h | VPFE_EOI_REG | EOI Register | 02F0 0850h | Section 13.49 |

13.31 VPFE_PID Register (Offset = 0h) [reset = 66803100h]

VPFE_PID is shown in [Figure 13-29](#) and described in [Table 13-62](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 13-61. VPFE_PID Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0000h |

Figure 13-29. VPFE_PID Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|--------|-------|----|----|--------|----|-------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | FUNC | | | | | | | | | | | |
| R-1h | | R-2h | | R-680h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTL | | | | | MAJOR | | | CUSTOM | | MINOR | | | | | |
| R-6h | | | | | R-1h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-62. VPFE_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 31-30 | SCHEME | R | 1h | VPFE_PID register scheme |
| 29-28 | BU | R | 2h | Business Unit: 10 = Processors |
| 27-16 | FUNC | R | 680h | Module ID |
| 15-11 | RTL | R | 6h | RTL VPFE_REVISION. Will vary depending on release. |
| 10-8 | MAJOR | R | 1h | Major VPFE_REVISION |
| 7-6 | CUSTOM | R | 0h | Custom |
| 5-0 | MINOR | R | 0h | Minor VPFE_REVISION |

13.32 VPFE_CONFIG Register (Offset = 4h) [reset = X]

VPFE_CONFIG is shown in [Figure 13-30](#) and described in [Table 13-64](#).

Return to [Summary Table](#).

The Config Register contains the configuration values for the module.

Table 13-63. VPFE_CONFIG Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0004h |

Figure 13-30. VPFE_CONFIG Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | ADDR_WIDTH | | | | | | | |
| R-X | | | | | | | | R-30h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADDRS | | | | | | | | REGIONS | | | | | | | |
| R-1h | | | | | | | | R-10h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-64. VPFE_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|------------------------|
| 31-24 | RESERVED | R | X | |
| 23-16 | ADDR_WIDTH | R | 30h | Number of address bits |
| 15-8 | ADDRS | R | 1h | Number of addresses |
| 7-0 | REGIONS | R | 10h | Number of regions |

13.33 VPFE_CTRL_j Register (Offset = 20h) [reset = X]

VPFE_CTRL_j is shown in [Figure 13-31](#) and described in [Table 13-66](#).

Return to [Summary Table](#).

The Control for Region a

Table 13-65. VPFE_CTRL_j Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0020h |

Figure 13-31. VPFE_CTRL_j Register

| | | | | | | | | | | | | | | | |
|----------|----------|----|----|----|----|----|----|-------|----|--------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EN | RESERVED | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | SIZE | | | | | |
| R/W-X | | | | | | | | | | R/W-0h | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-66. VPFE_CTRL_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31 | EN | R/W | 0h | Enable for the Region |
| 30-6 | RESERVED | R/W | X | |
| 5-0 | SIZE | R/W | 0h | Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB. |

13.34 VPFE_BASE_j Register (Offset = 24h) [reset = 0h]

VPFE_BASE_j is shown in [Figure 13-32](#) and described in [Table 13-68](#).

Return to [Summary Table](#).

The Base Address for Region a. This is the source address for matching to a region.

Table 13-67. VPFE_BASE_j Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0024h |

Figure 13-32. VPFE_BASE_j Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| BASE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-68. VPFE_BASE_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | BASE | R/W | 0h | Base Address for the Region. It must be aligned to the programmed size. |

13.35 VPFE_TRANS_I_J Register (Offset = 28h) [reset = 0h]

VPFE_TRANS_I_J is shown in [Figure 13-33](#) and described in [Table 13-70](#).

Return to [Summary Table](#).

The Translated Lower Address Bits for Region a

Table 13-69. VPFE_TRANS_I_J Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0028h |

Figure 13-33. VPFE_TRANS_I_J Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-70. VPFE_TRANS_I_J Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | LOWER | R/W | 0h | Translated Lower Address Bits for the Region. It must be aligned to the programmed size. |

13.36 VPFE_TRANS_U_j Register (Offset = 2Ch) [reset = X]

VPFE_TRANS_U_j is shown in [Figure 13-34](#) and described in [Table 13-72](#).

Return to [Summary Table](#).

The Translated Upper Address Bits for Region a

Table 13-71. VPFE_TRANS_U_j Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 002Ch |

Figure 13-34. VPFE_TRANS_U_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | UPPER | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-72. VPFE_TRANS_U_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | UPPER | R/W | 0h | Translated Upper Address Bits for the Region |

13.37 VPFE_DESTINATION_ID Register (Offset = 804h) [reset = X]

VPFE_DESTINATION_ID is shown in [Figure 13-35](#) and described in [Table 13-74](#).

Return to [Summary Table](#).

The Destination ID Register defines the destination ID value for error messages.

Table 13-73. VPFE_DESTINATION_ID Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0804h |

Figure 13-35. VPFE_DESTINATION_ID Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | DEST_ID | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-74. VPFE_DESTINATION_ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---------------------|
| 31-8 | RESERVED | R/W | X | |
| 7-0 | DEST_ID | R/W | 0h | The destination ID. |

13.38 VPFE_EXCEPTION_LOGGING_CONTROL Register (Offset = 820h) [reset = X]

VPFE_EXCEPTION_LOGGING_CONTROL is shown in [Figure 13-36](#) and described in [Table 13-76](#).

Return to [Summary Table](#).

The Exception Logging Control Register controls the exception logging.

Table 13-75.
VPFE_EXCEPTION_LOGGING_CONTROL Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0820h |

Figure 13-36. VPFE_EXCEPTION_LOGGING_CONTROL Register

| | | | | | | | |
|----------|----|----|----|----|----|--------------|-----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DISABLE_INTR | DISABLE_F |
| R/W-X | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-76. VPFE_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|--------------------------------------|
| 31-2 | RESERVED | R/W | X | |
| 1 | DISABLE_INTR | R/W | 0h | Disables logging interrupt when set. |
| 0 | DISABLE_F | R/W | 0h | Disables logging when set. |

13.39 VPFE_EXCEPTION_LOGGING_HEADER0 Register (Offset = 824h) [reset = 0h]

VPFE_EXCEPTION_LOGGING_HEADER0 is shown in [Figure 13-37](#) and described in [Table 13-78](#).

Return to [Summary Table](#).

The Exception Logging Header 0 Register contains the first word of the header.

Table 13-77.
VPFE_EXCEPTION_LOGGING_HEADER0 Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0824h |

Figure 13-37. VPFE_EXCEPTION_LOGGING_HEADER0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TYPE_F | | | | | | | | SRC_ID | | | | | | | | DEST_ID | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-78. VPFE_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------|------|-------|-------------------|
| 31-24 | TYPE_F | R | 0h | Type. 4 = RAT. |
| 23-8 | SRC_ID | R | 0h | Source ID. |
| 7-0 | DEST_ID | R | 0h | Destination ID. |

13.40 VPFE_EXCEPTION_LOGGING_HEADER1 Register (Offset = 828h) [reset = X]

VPFE_EXCEPTION_LOGGING_HEADER1 is shown in [Figure 13-38](#) and described in [Table 13-80](#).

Return to [Summary Table](#).

The Exception Logging Header 1 Register contains the second word of the header.

Table 13-79.
VPFE_EXCEPTION_LOGGING_HEADER1 Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0828h |

Figure 13-38. VPFE_EXCEPTION_LOGGING_HEADER1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|------|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| GROUP | | | | | | | | CODE | | | | | | | | RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-0h | | | | | | | | R-X | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-80. VPFE_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---------------------------------------|
| 31-24 | GROUP | R | 0h | Group. |
| 23-16 | CODE | R | 0h | Code. 1 = Boundary crossing error. |
| 15-0 | RESERVED | R | X | |

13.41 VPFE_EXCEPTION_LOGGING_DATA0 Register (Offset = 82Ch) [reset = 0h]

VPFE_EXCEPTION_LOGGING_DATA0 is shown in [Figure 13-39](#) and described in [Table 13-82](#).

Return to [Summary Table](#).

The Exception Logging Data 0 Register contains the first word of the data.

Table 13-81. VPFE_EXCEPTION_LOGGING_DATA0 Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 082Ch |

Figure 13-39. VPFE_EXCEPTION_LOGGING_DATA0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ADDR_L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-82. VPFE_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|------------------------|
| 31-0 | ADDR_L | R | 0h | Address lower 32 bits. |

13.42 VPFE_EXCEPTION_LOGGING_DATA1 Register (Offset = 830h) [reset = X]

VPFE_EXCEPTION_LOGGING_DATA1 is shown in [Figure 13-40](#) and described in [Table 13-84](#).

Return to [Summary Table](#).

The Exception Logging Data 1 Register contains the second word of the data.

Table 13-83. VPFE_EXCEPTION_LOGGING_DATA1 Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0830h |

Figure 13-40. VPFE_EXCEPTION_LOGGING_DATA1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | ADDR_H | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-84. VPFE_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|------------------------|
| 31-16 | RESERVED | R | X | |
| 15-0 | ADDR_H | R | 0h | Address upper 12 bits. |

13.43 VPFE_EXCEPTION_LOGGING_DATA2 Register (Offset = 834h) [reset = X]

VPFE_EXCEPTION_LOGGING_DATA2 is shown in [Figure 13-41](#) and described in [Table 13-86](#).

Return to [Summary Table](#).

The Exception Logging Data 2 Register contains the third word of the data.

**Table 13-85. VPFE_EXCEPTION_LOGGING_DATA2
Instances**

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0834h |

Figure 13-41. VPFE_EXCEPTION_LOGGING_DATA2 Register

| | | | | | | | |
|----------|----|-------|------|---------|-----------|------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | ROUTEID | | | |
| R-X | | | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ROUTEID | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | WRITE | READ | DEBUG | CACHEABLE | PRIV | SECURE |
| R-X | | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PRIV_ID | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-86. VPFE_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|-------------|
| 31-28 | RESERVED | R | X | |
| 27-16 | ROUTEID | R | 0h | Route ID. |
| 15-14 | RESERVED | R | X | |
| 13 | WRITE | R | 0h | Write. |
| 12 | READ | R | 0h | Read. |
| 11 | DEBUG | R | 0h | Debug. |
| 10 | CACHEABLE | R | 0h | Cacheable. |
| 9 | PRIV | R | 0h | Priv. |
| 8 | SECURE | R | 0h | Secure. |
| 7-0 | PRIV_ID | R | 0h | Priv ID. |

13.44 VPFE_EXCEPTION_LOGGING_DATA3 Register (Offset = 838h) [reset = X]

VPFE_EXCEPTION_LOGGING_DATA3 is shown in [Figure 13-42](#) and described in [Table 13-88](#).

Return to [Summary Table](#).

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Table 13-87. VPFE_EXCEPTION_LOGGING_DATA3 Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0838h |

Figure 13-42. VPFE_EXCEPTION_LOGGING_DATA3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | BYTECNT | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 13-88. VPFE_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-10 | RESERVED | R | X | |
| 9-0 | BYTECNT | R | 0h | Byte count. |

13.45 VPFE_EXCEPTION_PEND_SET Register (Offset = 840h) [reset = X]

VPFE_EXCEPTION_PEND_SET is shown in [Figure 13-43](#) and described in [Table 13-90](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

**Table 13-89. VPFE_EXCEPTION_PEND_SET
Instances**

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0840h |

Figure 13-43. VPFE_EXCEPTION_PEND_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PEND_SET |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-90. VPFE_EXCEPTION_PEND_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | PEND_SET | R/W1S | 0h | Write a 1 to set the exception pend signal. |

13.46 VPFE_EXCEPTION_PEND_CLEAR Register (Offset = 844h) [reset = X]

VPFE_EXCEPTION_PEND_CLEAR is shown in [Figure 13-44](#) and described in [Table 13-92](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Table 13-91. VPFE_EXCEPTION_PEND_CLEAR Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0844h |

Figure 13-44. VPFE_EXCEPTION_PEND_CLEAR Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PEND_CLR |
| R/W-X | | | | | | | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-92. VPFE_EXCEPTION_PEND_CLEAR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | PEND_CLR | R/W1C | 0h | Write a 1 to clear the exception pend signal. |

13.47 VPFE_EXCEPTION_ENABLE_SET Register (Offset = 848h) [reset = X]

VPFE_EXCEPTION_ENABLE_SET is shown in [Figure 13-45](#) and described in [Table 13-94](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

**Table 13-93. VPFE_EXCEPTION_ENABLE_SET
Instances**

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0848h |

Figure 13-45. VPFE_EXCEPTION_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE_SET |
| R/W-X | | | | | | | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 13-94. VPFE_EXCEPTION_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | ENABLE_SET | R/W1S | 0h | Write a 1 to set the exception interrupt enable signal. |

13.48 VPFE_EXCEPTION_ENABLE_CLEAR Register (Offset = 84Ch) [reset = X]

VPFE_EXCEPTION_ENABLE_CLEAR is shown in [Figure 13-46](#) and described in [Table 13-96](#).

Return to [Summary Table](#).

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Table 13-95. VPFE_EXCEPTION_ENABLE_CLEAR Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 084Ch |

Figure 13-46. VPFE_EXCEPTION_ENABLE_CLEAR Register

| | | | | | | | |
|----------|----|----|----|----|----|----|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | ENABLE_CLR |
| R/W-X | | | | | | | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 13-96. VPFE_EXCEPTION_ENABLE_CLEAR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|-------|-------|---|
| 31-1 | RESERVED | R/W | X | |
| 0 | ENABLE_CLR | R/W1C | 0h | Write a 1 to clear the exception interrupt enable signal. |

13.49 VPFE_EOI_REG Register (Offset = 850h) [reset = X]

VPFE_EOI_REG is shown in [Figure 13-47](#) and described in [Table 13-98](#).

Return to [Summary Table](#).

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 13-97. VPFE_EOI_REG Instances

| Instance | Physical Address |
|------------|------------------|
| VPFE0_MMRS | 02F0 0850h |

Figure 13-47. VPFE_EOI_REG Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | EOI_WR | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 13-98. VPFE_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--------------|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | EOI_WR | R/W | 0h | EOI Register |

14 GTC Registers

14.1 GTC0_GTC_CFG0 Registers

Table 14-2 lists the memory-mapped registers for the GTC0_GTC_CFG0. All register offset addresses not listed in Table 14-2 should be considered as reserved locations and the register contents should not be modified.

Table 14-1. GTC0_GTC_CFG0 Instances

| Instance | Base Address |
|---------------|--------------|
| GTC0_GTC_CFG0 | 00A8 0000h |

Table 14-2. GTC0_GTC_CFG0 Registers

| Offset | Acronym | Register Name | GTC0_GTC_CFG0 Physical Address |
|--------|-----------------------------|--|--------------------------------|
| 0h | GTC_PID | Generic control MMR peripheral ID register | 00A8 0000h |
| 4h | GTC_GTC_PID | GTC peripheral ID register | 00A8 0004h |
| 8h | GTC_PUSHEVT | Push event select register | 00A8 0008h |

14.1.1 GTC_PID Register (Offset = 0h) [reset = 61800209h]

GTC_PID is shown in [Figure 14-1](#) and described in [Table 14-4](#).

Return to [Summary Table](#).

This is the standard platform IP revision register which contains the ID and revision information of the MMR generator.

Table 14-3. GTC_PID Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG0 | 00A8 0000h |

Figure 14-1. GTC_PID Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-61800209h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 14-4. GTC_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-----------|--|
| 31-0 | REV | R | 61800209h | TI internal data. Identifies revision of peripheral. |

14.1.2 GTC_GTC_PID Register (Offset = 4h) [reset = X]

GTC_GTC_PID is shown in [Figure 14-2](#) and described in [Table 14-6](#).

Return to [Summary Table](#).

This is the standard platform IP revision register which contains the ID and revision information of the GTC peripheral.

Table 14-5. GTC_GTC_PID Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG0 | 00A8 0004h |

Figure 14-2. GTC_GTC_PID Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | REV | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | R-X | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 14-6. GTC_GTC_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | REV | R | X | TI internal data. Identifies revision of peripheral. |

14.1.3 GTC_PUSHEVT Register (Offset = 8h) [reset = 0h]

GTC_PUSHEVT is shown in [Figure 14-3](#) and described in [Table 14-8](#).

Return to [Summary Table](#).

Selects which bit of the count value to output as a push event for global timesync.

Table 14-7. GTC_PUSHEVT Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG0 | 00A8 0008h |

Figure 14-3. GTC_PUSHEVT Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | EXPBIT_SEL | | | | | |
| R-0h | | | | | | | | | | R/W-0h | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-8. GTC_PUSHEVT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 31-6 | RESERVED | R | 0h | Reserved. Always read as 0. |
| 5-0 | EXPBIT_SEL | R/W | 0h | This field controls the mux that selects which bit [63:0] of the system counter value is exported on the <i>push event</i> output. 0h = Select CNTR[0] 1h = Select CNTR[1] ... 3Fh = Select CNTR[63] |

14.2 GTC0_GTC_CFG1 Registers

Table 14-10 lists the memory-mapped registers for the GTC0_GTC_CFG1. All register offset addresses not listed in Table 14-10 should be considered as reserved locations and the register contents should not be modified.

Table 14-9. GTC0_GTC_CFG1 Instances

| Instance | Base Address |
|---------------|--------------|
| GTC0_GTC_CFG1 | 00A9 0000h |

Table 14-10. GTC0_GTC_CFG1 Registers

| Offset | Acronym | Register Name | GTC0_GTC_CFG1 Physical Address |
|--------|------------------------------|-------------------------------------|--------------------------------|
| 0h | GTC_CNTCR | Counter control register | 00A9 0000h |
| 4h | GTC_CNTSR | Counter status register | 00A9 0004h |
| 8h | GTC_CNTCV_LO | Counter count value (low) register | 00A9 0008h |
| Ch | GTC_CNTCV_HI | Counter count value (high) register | 00A9 000Ch |
| 20h | GTC_CNTFID0 | Counter frequency ID0 register | 00A9 0020h |
| 24h | GTC_CNTFID1 | Counter frequency ID1 register | 00A9 0024h |

14.2.1 GTC_CNTCR Register (Offset = 0h) [reset = 0h]

GTC_CNTCR is shown in [Figure 14-4](#) and described in [Table 14-12](#).

Return to [Summary Table](#).

This register enables the system counter and controls counter operation during debug.

Table 14-11. GTC_CNTCR Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG1 | 00A9 0000h |

Figure 14-4. GTC_CNTCR Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FCREQ | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FCREQ | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FCREQ | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | HDBG | EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 14-12. GTC_CNTCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-8 | FCREQ | R | 0h | Frequency change request. Indicates the number of the entry in the frequency table to select. For this device, this field is implemented as read-only, pointing to the base frequency table entry (000000h). |
| 7-2 | RESERVED | R | 0h | Reserved. Always read as 0. |
| 1 | HDBG | R/W | 0h | Halt on debug 0 = System counter ignores debug halt 1 = System counter is halted when debug halt is asserted |
| 0 | EN | R/W | 0h | Enable system counter 0 = System counter is disabled 1 = System counter is enabled |

14.2.2 GTC_CNTSR Register (Offset = 4h) [reset = X]

GTC_CNTSR is shown in [Figure 14-5](#) and described in [Table 14-14](#).

Return to [Summary Table](#).

This register provides system counter frequency status information.

Table 14-13. GTC_CNTSR Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG1 | 00A9 0004h |

Figure 14-5. GTC_CNTSR Register

| | | | | | | | |
|----------|----|----|----|----|----|------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FCACK | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FCACK | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FCACK | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DBGH | RESERVED |
| R-0h | | | | | | R-X | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 14-14. GTC_CNTSR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-8 | FCACK | R | 0h | Frequency change acknowledge. Indicates the currently selected entry in the frequency table. For this device, this field is tied to 0. |
| 7-2 | RESERVED | R | 0h | Reserved. Always read as 0. |
| 1 | DBGH | R | X | Debug halt. Indicates if the system counter is halted due to debug. 0 = System counter is not halted by a debug halt 1 = System counter is halted by a debug halt |
| 0 | RESERVED | R | 0h | Reserved. Always read as 0. |

14.2.3 GTC_CNTCV_LO Register (Offset = 8h) [reset = X]

GTC_CNTCV_LO is shown in [Figure 14-6](#) and described in [Table 14-16](#).

Return to [Summary Table](#).

Indicates the current system counter count value and can be used to set the system counter count value.

Table 14-15. GTC_CNTCV_LO Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG1 | 00A9 0008h |

Figure 14-6. GTC_CNTCV_LO Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNTVALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-16. GTC_CNTCV_LO Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | COUNTVALUE | R/W | 0h | Indicates bits [31:0] of the system counter value. This field is only writable when the system counter is disabled. The read value is the current value of system counter count [31:0]. |

14.2.4 GTC_CNTCV_HI Register (Offset = Ch) [reset = X]

GTC_CNTCV_HI is shown in [Figure 14-7](#) and described in [Table 14-18](#).

Return to [Summary Table](#).

Indicates the current system counter count value and can be used to set the system counter count value.

Table 14-17. GTC_CNTCV_HI Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG1 | 00A9 000Ch |

Figure 14-7. GTC_CNTCV_HI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNTVALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-18. GTC_CNTCV_HI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | COUNTVALUE | R/W | 0h | Indicates bits [63:32] of the system counter value. This field is only writable when the system counter is disabled. The read value is the current value of system counter count [63:32]. |

14.2.5 GTC_CNTFID0 Register (Offset = 20h) [reset = 0h]

GTC_CNTFID0 is shown in [Figure 14-8](#) and described in [Table 14-20](#).

Return to [Summary Table](#).

Indicates base frequency of the system counter. Device bootcode/firmware should write this register with the frequency of the selected GTC clock source before enabling the system counter.

Table 14-19. GTC_CNTFID0 Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG1 | 00A9 0020h |

Figure 14-8. GTC_CNTFID0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| FREQVALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 14-20. GTC_CNTFID0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|--|
| 31-0 | FREQVALUE | R/W | 0h | Indicates the base update frequency of the system counter in Hz. |

14.2.6 GTC_CNTFID1 Register (Offset = 24h) [reset = 0h]

GTC_CNTFID1 is shown in [Figure 14-9](#) and described in [Table 14-22](#).

Return to [Summary Table](#).

Indicates the system counter increment frequency.

Table 14-21. GTC_CNTFID1 Instances

| Instance | Physical Address |
|---------------|------------------|
| GTC0_GTC_CFG1 | 00A9 0024h |

Figure 14-9. GTC_CNTFID1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FREQVALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 14-22. GTC_CNTFID1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-0 | FREQVALUE | R | 0h | Frequency table end indicator. All 0s value marks the end of the frequency table. |

14.3 GTC0_GTC_CFG2 Registers

Table 14-24 lists the memory-mapped registers for the GTC0_GTC_CFG2. All register offset addresses not listed in Table 14-24 should be considered as reserved locations and the register contents should not be modified.

Table 14-23. GTC0_GTC_CFG2 Instances

| Instance | Base Address |
|---------------|--------------|
| GTC0_GTC_CFG2 | 00AA 0000h |

Table 14-24. GTC0_GTC_CFG2 Registers

| Offset | Acronym | Register Name | GTC0_GTC_CFG2 Physical Address |
|--------|-------------------------------|--|--------------------------------|
| 0h | GTC_CNTCVS_LO | Counter count value (low) status register | 00AA 0000h |
| 4h | GTC_CNTCVS_HI | Counter count value (high) status register | 00AA 0004h |

14.3.1 GTC_CNTCVS_LO Register (Offset = 0h) [reset = 0h]

GTC_CNTCVS_LO is shown in [Figure 14-10](#) and described in [Table 14-26](#).

Return to [Summary Table](#).

Indicates the current system counter count value. It reflects the same value as the CNTCV_LO register.

Table 14-25. GTC_CNTCVS_LO Instances

| Instance | Physical Address |
|--------------|------------------|
| GTC_R10_CFG1 | 00AA 0000h |

Figure 14-10. GTC_CNTCVS_LO Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| COUNTVALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 14-26. GTC_CNTCVS_LO Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 31-0 | COUNTVALUE | R | 0h | Indicates bits [31:0] of the system counter value. |

14.3.2 GTC_CNTCVS_HI Register (Offset = 4h) [reset = 0h]

GTC_CNTCVS_HI is shown in [Figure 14-11](#) and described in [Table 14-28](#).

Return to [Summary Table](#).

Indicates the current system counter count value. It reflects the same value as the CNTCV_HI register.

Table 14-27. GTC_CNTCVS_HI Instances

| Instance | Physical Address |
|--------------|------------------|
| GTC_R10_CFG1 | 00AA 0004h |

Figure 14-11. GTC_CNTCVS_HI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNTVALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 14-28. GTC_CNTCVS_HI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | COUNTVALUE | R | 0h | Indicates bits [63:32] of the system counter value. |

14.4 GTC0_GTC_CFG3 Registers

Table 14-30 lists the memory-mapped registers for the GTC0_GTC_CFG3. All register offset addresses not listed in Table 14-30 should be considered as reserved locations and the register contents should not be modified.

Table 14-29. GTC0_GTC_CFG3 Instances

| Instance | Base Address |
|---------------|--------------|
| GTC0_GTC_CFG3 | 00AB 0000h |

Table 14-30. GTC0_GTC_CFG3 Registers

| Offset | Acronym | Register Name | GTC0_GTC_CFG3 Physical Address |
|--------|-----------------------------|---------------------------|--------------------------------|
| 8h | GTC_CNTTIDR | Counter-timer ID register | 00AB 0000h |

14.4.1 GTC_CNTTIDR Register (Offset = 8h) [reset = 0h]

GTC_CNTTIDR is shown in [Figure 14-12](#) and described in [Table 14-32](#).

Return to [Summary Table](#).

Indicates the implemented timers in the memory map and their features. Because the platform does not implement memory-mapped timers, this register is set to all 0s.

Table 14-31. GTC_CNTTIDR Instances

| Instance | Physical Address |
|--------------|------------------|
| GTC_R10_CFG1 | 00AB 0000h |

Figure 14-12. GTC_CNTTIDR Register

| | | | | | | | | | | | | | | | |
|--------|----|----|----|--------|----|----|----|--------|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME7 | | | | FRAME6 | | | | FRAME5 | | | | FRAME4 | | | |
| R-0h | | | | R-0h | | | | R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRAME3 | | | | FRAME2 | | | | FRAME1 | | | | FRAME0 | | | |
| R-0h | | | | R-0h | | | | R-0h | | | | R-0h | | | |

LEGEND: R = Read Only; -n = value after reset

Table 14-32. GTC_CNTTIDR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 31-28 | FRAME7 | R | 0h | Indicates the features of timer frame 7 |
| 27-24 | FRAME6 | R | 0h | Indicates the features of timer frame 6 |
| 23-20 | FRAME5 | R | 0h | Indicates the features of timer frame 5 |
| 19-16 | FRAME4 | R | 0h | Indicates the features of timer frame 4 |
| 15-12 | FRAME3 | R | 0h | Indicates the features of timer frame 3 |
| 11-8 | FRAME2 | R | 0h | Indicates the features of timer frame 2 |
| 7-4 | FRAME1 | R | 0h | Indicates the features of timer frame 1 |
| 3-0 | FRAME0 | R | 0h | Indicates the features of timer frame 0 |

15 RTI Registers

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Table 15-2 lists the memory-mapped registers for the RTI. All register offset addresses not listed in Table 15-2 should be considered as reserved locations and the register contents should not be modified.

Table 15-1. RTI Instances

| Instance | Base Address |
|--------------|--------------|
| RTI0_CFG | 0220 0000h |
| RTI1_CFG | 0221 0000h |
| RTI15_CFG | 022F 0000h |
| RTI16_CFG | 0230 0000h |
| RTI24_CFG | 0238 0000h |
| RTI25_CFG | 0239 0000h |
| RTI28_CFG | 023C 0000h |
| RTI29_CFG | 023D 0000h |
| RTI30_CFG | 023E 0000h |
| RTI31_CFG | 023F 0000h |
| MCU_RTI0_CFG | 4060 0000h |
| MCU_RTI1_CFG | 4061 0000h |

Table 15-2. RTI Registers

| Offset | Acronym | Register Name | RTI0_CFG Physical Address | RTI1_CFG Physical Address |
|--------|------------------------------|--|---------------------------------|---------------------------------|
| 0h | RTI_GCTRL | RTI Global Control Register | 0220 0000h | 0221 0000h |
| 4h | RTI_TBCTRL | RTI Timebase Control Register | 0220 0004h | 0221 0004h |
| 8h | RTI_CAPCTRL | RTI Capture Control Register | 0220 0008h | 0221 0008h |
| Ch | RTI_COMPCTRL | RTI Compare Control Register | 0220 000Ch | 0221 000Ch |
| 10h | RTI_FRC0 | RTI Free Running Counter 0 Register | 0220 0010h | 0221 0010h |
| 14h | RTI_UC0 | RTI Up Counter 0 Register | 0220 0014h | 0221 0014h |
| 18h | RTI_CPUC0 | RTI Compare Up Counter 0 Register | 0220 0018h | 0221 0018h |
| 20h | RTI_CAFRC0 | RTI Capture Free Running Counter 0 Register | 0220 0020h | 0221 0020h |
| 24h | RTI_CAUC0 | RTI Capture Up Counter 0 Register | 0220 0024h | 0221 0024h |
| 30h | RTI_FRC1 | RTI Free Running Counter 1 Register | 0220 0030h | 0221 0030h |
| 34h | RTI_UC1 | RTI Up Counter 1 Register | 0220 0034h | 0221 0034h |
| 38h | RTI_CPUC1 | RTI Compare Up Counter 1 Register | 0220 0038h | 0221 0038h |
| 40h | RTI_CAFRC1 | RTI Capture Free Running Counter 1 Register | 0220 0040h | 0221 0040h |
| 44h | RTI_CAUC1 | RTI Capture Up Counter 1 Register | 0220 0044h | 0221 0044h |
| 50h | RTI_COMP0 | RTI Compare 0 Register | 0220 0050h | 0221 0050h |
| 54h | RTI_UDCP0 | RTI Update Compare 0 Register | 0220 0054h | 0221 0054h |
| 58h | RTI_COMP1 | RTI Compare 1 Register | 0220 0058h | 0221 0058h |
| 5Ch | RTI_UDCP1 | RTI Update Compare 1 Register | 0220 005Ch | 0221 005Ch |
| 60h | RTI_COMP2 | RTI Compare 2 Register | 0220 0060h | 0221 0060h |
| 64h | RTI_UDCP2 | RTI Update Compare 2 Register | 0220 0064h | 0221 0064h |
| 68h | RTI_COMP3 | RTI Compare 3 Register | 0220 0068h | 0221 0068h |
| 6Ch | RTI_UDCP3 | RTI Update Compare 3 Register | 0220 006Ch | 0221 006Ch |
| 70h | RTI_TBLCOMP | RTI External Clock Timebase Low Compare Register | 0220 0070h | 0221 0070h |

Table 15-2. RTI Registers (continued)

| Offset | Acronym | Register Name | RTI0_CFG Physical Address | RTI1_CFG Physical Address |
|--------|----------------------------------|---|---------------------------------|---------------------------------|
| 74h | RTI_TBHCOMP | RTI External Clock Timebase High Compare Register | 0220 0074h | 0221 0074h |
| 80h | RTI_SETINT | RTI Set/Status Interrupt Register | 0220 0080h | 0221 0080h |
| 84h | RTI_CLEARINT | RTI Clear/Status Interrupt Register | 0220 0084h | 0221 0084h |
| 88h | RTI_INTFLAG | RTI Interrupt Flag Register | 0220 0088h | 0221 0088h |
| 90h | RTI_DWDCTRL | Digital Watchdog Control Register | 0220 0090h | 0221 0090h |
| 94h | RTI_DWDPRLD | Digital Watchdog Preload Register | 0220 0094h | 0221 0094h |
| 98h | RTI_WDSTATUS | Watchdog Status Register | 0220 0098h | 0221 0098h |
| 9Ch | RTI_WDKEY | Watchdog Key Register | 0220 009Ch | 0221 009Ch |
| A0h | RTI_DWDCNTR | Digital Watchdog Down Counter | 0220 00A0h | 0221 00A0h |
| A4h | RTI_WWDRXNCTRL | Digital Windowed Watchdog Reaction Control | 0220 00A4h | 0221 00A4h |
| A8h | RTI_WWDSIZECTRL | Digital Windowed Watchdog Window Size Control | 0220 00A8h | 0221 00A8h |
| ACh | RTI_INTCLRENABLE | RTI Compare Interrupt Clear Enable Register | 0220 00ACh | 0221 00ACh |
| B0h | RTI_COMP0CLR | RTI Compare 0 Clear Register | 0220 00B0h | 0221 00B0h |
| B4h | RTI_COMP1CLR | RTI Compare 1 Clear Register | 0220 00B4h | 0221 00B4h |
| B8h | RTI_COMP2CLR | RTI Compare 2 Clear Register | 0220 00B8h | 0221 00B8h |
| BCh | RTI_COMP3CLR | RTI Compare 3 Clear Register | 0220 00BCh | 0221 00BCh |

Table 15-3. RTI Registers

| Offset | Acronym | Register Name | RTI15_CFG Physical Address | RTI16_CFG Physical Address |
|--------|------------------------------|---|----------------------------------|----------------------------------|
| 0h | RTI_GCTRL | RTI Global Control Register | 022F 0000h | 0230 0000h |
| 4h | RTI_TBCTRL | RTI Timebase Control Register | 022F 0004h | 0230 0004h |
| 8h | RTI_CAPCTRL | RTI Capture Control Register | 022F 0008h | 0230 0008h |
| Ch | RTI_COMPCTRL | RTI Compare Control Register | 022F 000Ch | 0230 000Ch |
| 10h | RTI_FRC0 | RTI Free Running Counter 0 Register | 022F 0010h | 0230 0010h |
| 14h | RTI_UC0 | RTI Up Counter 0 Register | 022F 0014h | 0230 0014h |
| 18h | RTI_CPUC0 | RTI Compare Up Counter 0 Register | 022F 0018h | 0230 0018h |
| 20h | RTI_CAFRC0 | RTI Capture Free Running Counter 0 Register | 022F 0020h | 0230 0020h |
| 24h | RTI_CAUC0 | RTI Capture Up Counter 0 Register | 022F 0024h | 0230 0024h |
| 30h | RTI_FRC1 | RTI Free Running Counter 1 Register | 022F 0030h | 0230 0030h |
| 34h | RTI_UC1 | RTI Up Counter 1 Register | 022F 0034h | 0230 0034h |
| 38h | RTI_CPUC1 | RTI Compare Up Counter 1 Register | 022F 0038h | 0230 0038h |
| 40h | RTI_CAFRC1 | RTI Capture Free Running Counter 1 Register | 022F 0040h | 0230 0040h |
| 44h | RTI_CAUC1 | RTI Capture Up Counter 1 Register | 022F 0044h | 0230 0044h |
| 50h | RTI_COMP0 | RTI Compare 0 Register | 022F 0050h | 0230 0050h |
| 54h | RTI_UDCP0 | RTI Update Compare 0 Register | 022F 0054h | 0230 0054h |
| 58h | RTI_COMP1 | RTI Compare 1 Register | 022F 0058h | 0230 0058h |
| 5Ch | RTI_UDCP1 | RTI Update Compare 1 Register | 022F 005Ch | 0230 005Ch |
| 60h | RTI_COMP2 | RTI Compare 2 Register | 022F 0060h | 0230 0060h |
| 64h | RTI_UDCP2 | RTI Update Compare 2 Register | 022F 0064h | 0230 0064h |
| 68h | RTI_COMP3 | RTI Compare 3 Register | 022F 0068h | 0230 0068h |
| 6Ch | RTI_UDCP3 | RTI Update Compare 3 Register | 022F 006Ch | 0230 006Ch |
| 70h | RTI_TBLCOMP | RTI External Clock Timebase Low Compare Register | 022F 0070h | 0230 0070h |
| 74h | RTI_TBHCOMP | RTI External Clock Timebase High Compare Register | 022F 0074h | 0230 0074h |
| 80h | RTI_SETINT | RTI Set/Status Interrupt Register | 022F 0080h | 0230 0080h |

Table 15-3. RTI Registers (continued)

| Offset | Acronym | Register Name | RTI15_CFG Physical Address | RTI16_CFG Physical Address |
|--------|----------------------------------|---|----------------------------------|----------------------------------|
| 84h | RTI_CLEARINT | RTI Clear/Status Interrupt Register | 022F 0084h | 0230 0084h |
| 88h | RTI_INTFLAG | RTI Interrupt Flag Register | 022F 0088h | 0230 0088h |
| 90h | RTI_DWDCTRL | Digital Watchdog Control Register | 022F 0090h | 0230 0090h |
| 94h | RTI_DWDPRLD | Digital Watchdog Preload Register | 022F 0094h | 0230 0094h |
| 98h | RTI_WDSTATUS | Watchdog Status Register | 022F 0098h | 0230 0098h |
| 9Ch | RTI_WDKEY | Watchdog Key Register | 022F 009Ch | 0230 009Ch |
| A0h | RTI_DWDCNTR | Digital Watchdog Down Counter | 022F 00A0h | 0230 00A0h |
| A4h | RTI_WWDRXNCTRL | Digital Windowed Watchdog Reaction Control | 022F 00A4h | 0230 00A4h |
| A8h | RTI_WWDSIZECTRL | Digital Windowed Watchdog Window Size Control | 022F 00A8h | 0230 00A8h |
| ACh | RTI_INTCLRENABLE | RTI Compare Interrupt Clear Enable Register | 022F 00ACh | 0230 00ACh |
| B0h | RTI_COMP0CLR | RTI Compare 0 Clear Register | 022F 00B0h | 0230 00B0h |
| B4h | RTI_COMP1CLR | RTI Compare 1 Clear Register | 022F 00B4h | 0230 00B4h |
| B8h | RTI_COMP2CLR | RTI Compare 2 Clear Register | 022F 00B8h | 0230 00B8h |
| BCh | RTI_COMP3CLR | RTI Compare 3 Clear Register | 022F 00BCh | 0230 00BCh |

Table 15-4. RTI Registers

| Offset | Acronym | Register Name | RTI24_CFG Physical Address | RTI25_CFG Physical Address |
|--------|------------------------------|---|----------------------------------|----------------------------------|
| 0h | RTI_GCTRL | RTI Global Control Register | 0238 0000h | 0239 0000h |
| 4h | RTI_TBCTRL | RTI Timebase Control Register | 0238 0004h | 0239 0004h |
| 8h | RTI_CAPCTRL | RTI Capture Control Register | 0238 0008h | 0239 0008h |
| Ch | RTI_COMPCTRL | RTI Compare Control Register | 0238 000Ch | 0239 000Ch |
| 10h | RTI_FRC0 | RTI Free Running Counter 0 Register | 0238 0010h | 0239 0010h |
| 14h | RTI_UC0 | RTI Up Counter 0 Register | 0238 0014h | 0239 0014h |
| 18h | RTI_CPUC0 | RTI Compare Up Counter 0 Register | 0238 0018h | 0239 0018h |
| 20h | RTI_CAFRC0 | RTI Capture Free Running Counter 0 Register | 0238 0020h | 0239 0020h |
| 24h | RTI_CAUC0 | RTI Capture Up Counter 0 Register | 0238 0024h | 0239 0024h |
| 30h | RTI_FRC1 | RTI Free Running Counter 1 Register | 0238 0030h | 0239 0030h |
| 34h | RTI_UC1 | RTI Up Counter 1 Register | 0238 0034h | 0239 0034h |
| 38h | RTI_CPUC1 | RTI Compare Up Counter 1 Register | 0238 0038h | 0239 0038h |
| 40h | RTI_CAFRC1 | RTI Capture Free Running Counter 1 Register | 0238 0040h | 0239 0040h |
| 44h | RTI_CAUC1 | RTI Capture Up Counter 1 Register | 0238 0044h | 0239 0044h |
| 50h | RTI_COMP0 | RTI Compare 0 Register | 0238 0050h | 0239 0050h |
| 54h | RTI_UDCP0 | RTI Update Compare 0 Register | 0238 0054h | 0239 0054h |
| 58h | RTI_COMP1 | RTI Compare 1 Register | 0238 0058h | 0239 0058h |
| 5Ch | RTI_UDCP1 | RTI Update Compare 1 Register | 0238 005Ch | 0239 005Ch |
| 60h | RTI_COMP2 | RTI Compare 2 Register | 0238 0060h | 0239 0060h |
| 64h | RTI_UDCP2 | RTI Update Compare 2 Register | 0238 0064h | 0239 0064h |
| 68h | RTI_COMP3 | RTI Compare 3 Register | 0238 0068h | 0239 0068h |
| 6Ch | RTI_UDCP3 | RTI Update Compare 3 Register | 0238 006Ch | 0239 006Ch |
| 70h | RTI_TBLCOMP | RTI External Clock Timebase Low Compare Register | 0238 0070h | 0239 0070h |
| 74h | RTI_TBHCOMP | RTI External Clock Timebase High Compare Register | 0238 0074h | 0239 0074h |
| 80h | RTI_SETINT | RTI Set/Status Interrupt Register | 0238 0080h | 0239 0080h |
| 84h | RTI_CLEARINT | RTI Clear/Status Interrupt Register | 0238 0084h | 0239 0084h |
| 88h | RTI_INTFLAG | RTI Interrupt Flag Register | 0238 0088h | 0239 0088h |

Table 15-4. RTI Registers (continued)

| Offset | Acronym | Register Name | RTI24_CFG Physical Address | RTI25_CFG Physical Address |
|--------|----------------------------------|---|----------------------------------|----------------------------------|
| 90h | RTI_DWDCTRL | Digital Watchdog Control Register | 0238 0090h | 0239 0090h |
| 94h | RTI_DWDPRLD | Digital Watchdog Preload Register | 0238 0094h | 0239 0094h |
| 98h | RTI_WDSTATUS | Watchdog Status Register | 0238 0098h | 0239 0098h |
| 9Ch | RTI_WDKEY | Watchdog Key Register | 0238 009Ch | 0239 009Ch |
| A0h | RTI_DWDCNTR | Digital Watchdog Down Counter | 0238 00A0h | 0239 00A0h |
| A4h | RTI_WWDRXNCTRL | Digital Windowed Watchdog Reaction Control | 0238 00A4h | 0239 00A4h |
| A8h | RTI_WWDSIZECTRL | Digital Windowed Watchdog Window Size Control | 0238 00A8h | 0239 00A8h |
| ACh | RTI_INTCLRENABLE | RTI Compare Interrupt Clear Enable Register | 0238 00ACh | 0239 00ACh |
| B0h | RTI_COMP0CLR | RTI Compare 0 Clear Register | 0238 00B0h | 0239 00B0h |
| B4h | RTI_COMP1CLR | RTI Compare 1 Clear Register | 0238 00B4h | 0239 00B4h |
| B8h | RTI_COMP2CLR | RTI Compare 2 Clear Register | 0238 00B8h | 0239 00B8h |
| BCh | RTI_COMP3CLR | RTI Compare 3 Clear Register | 0238 00BCh | 0239 00BCh |

Table 15-5. RTI Registers

| Offset | Acronym | Register Name | RTI28_CFG Physical Address | RTI29_CFG Physical Address |
|--------|------------------------------|---|----------------------------------|----------------------------------|
| 0h | RTI_GCTRL | RTI Global Control Register | 023C 0000h | 023D 0000h |
| 4h | RTI_TBCTRL | RTI Timebase Control Register | 023C 0004h | 023D 0004h |
| 8h | RTI_CAPCTRL | RTI Capture Control Register | 023C 0008h | 023D 0008h |
| Ch | RTI_COMPCTRL | RTI Compare Control Register | 023C 000Ch | 023D 000Ch |
| 10h | RTI_FRC0 | RTI Free Running Counter 0 Register | 023C 0010h | 023D 0010h |
| 14h | RTI_UC0 | RTI Up Counter 0 Register | 023C 0014h | 023D 0014h |
| 18h | RTI_CPUC0 | RTI Compare Up Counter 0 Register | 023C 0018h | 023D 0018h |
| 20h | RTI_CAFRC0 | RTI Capture Free Running Counter 0 Register | 023C 0020h | 023D 0020h |
| 24h | RTI_CAUC0 | RTI Capture Up Counter 0 Register | 023C 0024h | 023D 0024h |
| 30h | RTI_FRC1 | RTI Free Running Counter 1 Register | 023C 0030h | 023D 0030h |
| 34h | RTI_UC1 | RTI Up Counter 1 Register | 023C 0034h | 023D 0034h |
| 38h | RTI_CPUC1 | RTI Compare Up Counter 1 Register | 023C 0038h | 023D 0038h |
| 40h | RTI_CAFRC1 | RTI Capture Free Running Counter 1 Register | 023C 0040h | 023D 0040h |
| 44h | RTI_CAUC1 | RTI Capture Up Counter 1 Register | 023C 0044h | 023D 0044h |
| 50h | RTI_COMP0 | RTI Compare 0 Register | 023C 0050h | 023D 0050h |
| 54h | RTI_UDCP0 | RTI Update Compare 0 Register | 023C 0054h | 023D 0054h |
| 58h | RTI_COMP1 | RTI Compare 1 Register | 023C 0058h | 023D 0058h |
| 5Ch | RTI_UDCP1 | RTI Update Compare 1 Register | 023C 005Ch | 023D 005Ch |
| 60h | RTI_COMP2 | RTI Compare 2 Register | 023C 0060h | 023D 0060h |
| 64h | RTI_UDCP2 | RTI Update Compare 2 Register | 023C 0064h | 023D 0064h |
| 68h | RTI_COMP3 | RTI Compare 3 Register | 023C 0068h | 023D 0068h |
| 6Ch | RTI_UDCP3 | RTI Update Compare 3 Register | 023C 006Ch | 023D 006Ch |
| 70h | RTI_TBLCOMP | RTI External Clock Timebase Low Compare Register | 023C 0070h | 023D 0070h |
| 74h | RTI_TBHCOMP | RTI External Clock Timebase High Compare Register | 023C 0074h | 023D 0074h |
| 80h | RTI_SETINT | RTI Set/Status Interrupt Register | 023C 0080h | 023D 0080h |
| 84h | RTI_CLEARINT | RTI Clear/Status Interrupt Register | 023C 0084h | 023D 0084h |
| 88h | RTI_INTFLAG | RTI Interrupt Flag Register | 023C 0088h | 023D 0088h |
| 90h | RTI_DWDCTRL | Digital Watchdog Control Register | 023C 0090h | 023D 0090h |
| 94h | RTI_DWDPRLD | Digital Watchdog Preload Register | 023C 0094h | 023D 0094h |

Table 15-5. RTI Registers (continued)

| Offset | Acronym | Register Name | RTI28_CFG Physical Address | RTI29_CFG Physical Address |
|--------|----------------------------------|---|----------------------------------|----------------------------------|
| 98h | RTI_WDSTATUS | Watchdog Status Register | 023C 0098h | 023D 0098h |
| 9Ch | RTI_WDKEY | Watchdog Key Register | 023C 009Ch | 023D 009Ch |
| A0h | RTI_DWDCNTR | Digital Watchdog Down Counter | 023C 00A0h | 023D 00A0h |
| A4h | RTI_WWDRXNCTRL | Digital Windowed Watchdog Reaction Control | 023C 00A4h | 023D 00A4h |
| A8h | RTI_WWDSIZECTRL | Digital Windowed Watchdog Window Size Control | 023C 00A8h | 023D 00A8h |
| ACH | RTI_INTCLRENABLE | RTI Compare Interrupt Clear Enable Register | 023C 00ACH | 023D 00ACH |
| B0h | RTI_COMP0CLR | RTI Compare 0 Clear Register | 023C 00B0h | 023D 00B0h |
| B4h | RTI_COMP1CLR | RTI Compare 1 Clear Register | 023C 00B4h | 023D 00B4h |
| B8h | RTI_COMP2CLR | RTI Compare 2 Clear Register | 023C 00B8h | 023D 00B8h |
| BCh | RTI_COMP3CLR | RTI Compare 3 Clear Register | 023C 00BCh | 023D 00BCh |

Table 15-6. RTI Registers

| Offset | Acronym | Register Name | RTI30_CFG Physical Address | RTI31_CFG Physical Address |
|--------|------------------------------|---|----------------------------------|----------------------------------|
| 0h | RTI_GCTRL | RTI Global Control Register | 023E 0000h | 023F 0000h |
| 4h | RTI_TBCTRL | RTI Timebase Control Register | 023E 0004h | 023F 0004h |
| 8h | RTI_CAPCTRL | RTI Capture Control Register | 023E 0008h | 023F 0008h |
| Ch | RTI_COMPCTRL | RTI Compare Control Register | 023E 000Ch | 023F 000Ch |
| 10h | RTI_FRC0 | RTI Free Running Counter 0 Register | 023E 0010h | 023F 0010h |
| 14h | RTI_UC0 | RTI Up Counter 0 Register | 023E 0014h | 023F 0014h |
| 18h | RTI_CPUC0 | RTI Compare Up Counter 0 Register | 023E 0018h | 023F 0018h |
| 20h | RTI_CAFRC0 | RTI Capture Free Running Counter 0 Register | 023E 0020h | 023F 0020h |
| 24h | RTI_CAUC0 | RTI Capture Up Counter 0 Register | 023E 0024h | 023F 0024h |
| 30h | RTI_FRC1 | RTI Free Running Counter 1 Register | 023E 0030h | 023F 0030h |
| 34h | RTI_UC1 | RTI Up Counter 1 Register | 023E 0034h | 023F 0034h |
| 38h | RTI_CPUC1 | RTI Compare Up Counter 1 Register | 023E 0038h | 023F 0038h |
| 40h | RTI_CAFRC1 | RTI Capture Free Running Counter 1 Register | 023E 0040h | 023F 0040h |
| 44h | RTI_CAUC1 | RTI Capture Up Counter 1 Register | 023E 0044h | 023F 0044h |
| 50h | RTI_COMP0 | RTI Compare 0 Register | 023E 0050h | 023F 0050h |
| 54h | RTI_UDCP0 | RTI Update Compare 0 Register | 023E 0054h | 023F 0054h |
| 58h | RTI_COMP1 | RTI Compare 1 Register | 023E 0058h | 023F 0058h |
| 5Ch | RTI_UDCP1 | RTI Update Compare 1 Register | 023E 005Ch | 023F 005Ch |
| 60h | RTI_COMP2 | RTI Compare 2 Register | 023E 0060h | 023F 0060h |
| 64h | RTI_UDCP2 | RTI Update Compare 2 Register | 023E 0064h | 023F 0064h |
| 68h | RTI_COMP3 | RTI Compare 3 Register | 023E 0068h | 023F 0068h |
| 6Ch | RTI_UDCP3 | RTI Update Compare 3 Register | 023E 006Ch | 023F 006Ch |
| 70h | RTI_TBLCOMP | RTI External Clock Timebase Low Compare Register | 023E 0070h | 023F 0070h |
| 74h | RTI_TBHCOMP | RTI External Clock Timebase High Compare Register | 023E 0074h | 023F 0074h |
| 80h | RTI_SETINT | RTI Set/Status Interrupt Register | 023E 0080h | 023F 0080h |
| 84h | RTI_CLEARINT | RTI Clear/Status Interrupt Register | 023E 0084h | 023F 0084h |
| 88h | RTI_INTFLAG | RTI Interrupt Flag Register | 023E 0088h | 023F 0088h |
| 90h | RTI_DWDCTRL | Digital Watchdog Control Register | 023E 0090h | 023F 0090h |
| 94h | RTI_DWDPRLD | Digital Watchdog Preload Register | 023E 0094h | 023F 0094h |
| 98h | RTI_WDSTATUS | Watchdog Status Register | 023E 0098h | 023F 0098h |
| 9Ch | RTI_WDKEY | Watchdog Key Register | 023E 009Ch | 023F 009Ch |

Table 15-6. RTI Registers (continued)

| Offset | Acronym | Register Name | RTI30_CFG Physical Address | RTI31_CFG Physical Address |
|--------|---------------------------------|---|----------------------------------|----------------------------------|
| A0h | RTI_DWDCNTR | Digital Watchdog Down Counter | 023E 00A0h | 023F 00A0h |
| A4h | RTI_WWDRXNCTRL | Digital Windowed Watchdog Reaction Control | 023E 00A4h | 023F 00A4h |
| A8h | RTI_WWDSIZECTRL | Digital Windowed Watchdog Window Size Control | 023E 00A8h | 023F 00A8h |
| ACh | RTI_INTCLREABLE | RTI Compare Interrupt Clear Enable Register | 023E 00ACh | 023F 00ACh |
| B0h | RTI_COMP0CLR | RTI Compare 0 Clear Register | 023E 00B0h | 023F 00B0h |
| B4h | RTI_COMP1CLR | RTI Compare 1 Clear Register | 023E 00B4h | 023F 00B4h |
| B8h | RTI_COMP2CLR | RTI Compare 2 Clear Register | 023E 00B8h | 023F 00B8h |
| BCh | RTI_COMP3CLR | RTI Compare 3 Clear Register | 023E 00BCh | 023F 00BCh |

Table 15-7. RTI Registers

| Offset | Acronym | Register Name | MCU_RTI0_CFG Physical Address | MCU_RTI1_CFG Physical Address |
|--------|--------------------------------|---|-------------------------------------|-------------------------------------|
| 0h | RTI_GCTRL | RTI Global Control Register | 4060 0000h | 4061 0000h |
| 4h | RTI_TBCTRL | RTI Timebase Control Register | 4060 0004h | 4061 0004h |
| 8h | RTI_CAPCTRL | RTI Capture Control Register | 4060 0008h | 4061 0008h |
| Ch | RTI_COMPCTRL | RTI Compare Control Register | 4060 000Ch | 4061 000Ch |
| 10h | RTI_FRC0 | RTI Free Running Counter 0 Register | 4060 0010h | 4061 0010h |
| 14h | RTI_UC0 | RTI Up Counter 0 Register | 4060 0014h | 4061 0014h |
| 18h | RTI_CPUC0 | RTI Compare Up Counter 0 Register | 4060 0018h | 4061 0018h |
| 20h | RTI_CAFRC0 | RTI Capture Free Running Counter 0 Register | 4060 0020h | 4061 0020h |
| 24h | RTI_CAUC0 | RTI Capture Up Counter 0 Register | 4060 0024h | 4061 0024h |
| 30h | RTI_FRC1 | RTI Free Running Counter 1 Register | 4060 0030h | 4061 0030h |
| 34h | RTI_UC1 | RTI Up Counter 1 Register | 4060 0034h | 4061 0034h |
| 38h | RTI_CPUC1 | RTI Compare Up Counter 1 Register | 4060 0038h | 4061 0038h |
| 40h | RTI_CAFRC1 | RTI Capture Free Running Counter 1 Register | 4060 0040h | 4061 0040h |
| 44h | RTI_CAUC1 | RTI Capture Up Counter 1 Register | 4060 0044h | 4061 0044h |
| 50h | RTI_COMP0 | RTI Compare 0 Register | 4060 0050h | 4061 0050h |
| 54h | RTI_UDCP0 | RTI Update Compare 0 Register | 4060 0054h | 4061 0054h |
| 58h | RTI_COMP1 | RTI Compare 1 Register | 4060 0058h | 4061 0058h |
| 5Ch | RTI_UDCP1 | RTI Update Compare 1 Register | 4060 005Ch | 4061 005Ch |
| 60h | RTI_COMP2 | RTI Compare 2 Register | 4060 0060h | 4061 0060h |
| 64h | RTI_UDCP2 | RTI Update Compare 2 Register | 4060 0064h | 4061 0064h |
| 68h | RTI_COMP3 | RTI Compare 3 Register | 4060 0068h | 4061 0068h |
| 6Ch | RTI_UDCP3 | RTI Update Compare 3 Register | 4060 006Ch | 4061 006Ch |
| 70h | RTI_TBLCOMP | RTI External Clock Timebase Low Compare Register | 4060 0070h | 4061 0070h |
| 74h | RTI_TBHCOMP | RTI External Clock Timebase High Compare Register | 4060 0074h | 4061 0074h |
| 80h | RTI_SETINT | RTI Set/Status Interrupt Register | 4060 0080h | 4061 0080h |
| 84h | RTI_CLEARINT | RTI Clear/Status Interrupt Register | 4060 0084h | 4061 0084h |
| 88h | RTI_INTFLAG | RTI Interrupt Flag Register | 4060 0088h | 4061 0088h |
| 90h | RTI_DWDCTRL | Digital Watchdog Control Register | 4060 0090h | 4061 0090h |
| 94h | RTI_DWDPRLD | Digital Watchdog Preload Register | 4060 0094h | 4061 0094h |
| 98h | RTI_WDSTATUS | Watchdog Status Register | 4060 0098h | 4061 0098h |
| 9Ch | RTI_WDKEY | Watchdog Key Register | 4060 009Ch | 4061 009Ch |
| A0h | RTI_DWDCNTR | Digital Watchdog Down Counter | 4060 00A0h | 4061 00A0h |
| A4h | RTI_WWDRXNCTRL | Digital Windowed Watchdog Reaction Control | 4060 00A4h | 4061 00A4h |

Table 15-7. RTI Registers (continued)

| Offset | Acronym | Register Name | MCU_RT10_CFG Physical Address | MCU_RT11_CFG Physical Address |
|--------|-----------------------------------|---|-------------------------------------|-------------------------------------|
| A8h | RTI_WWDSIZECTRL | Digital Windowed Watchdog Window Size Control | 4060 00A8h | 4061 00A8h |
| ACH | RTI_INTCLREENABLE | RTI Compare Interrupt Clear Enable Register | 4060 00ACH | 4061 00ACH |
| B0h | RTI_COMP0CLR | RTI Compare 0 Clear Register | 4060 00B0h | 4061 00B0h |
| B4h | RTI_COMP1CLR | RTI Compare 1 Clear Register | 4060 00B4h | 4061 00B4h |
| B8h | RTI_COMP2CLR | RTI Compare 2 Clear Register | 4060 00B8h | 4061 00B8h |
| BCh | RTI_COMP3CLR | RTI Compare 3 Clear Register | 4060 00BCh | 4061 00BCh |

15.1 RTI_GCTRL Register (Offset = 0h) [reset = 0h]

RTI_GCTRL is shown in [Figure 15-1](#) and described in [Table 15-9](#).

[Return to Summary Table.](#)

Table 15-8. RTI_GCTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0000h |
| RTI1_CFG | 0221 0000h |
| RTI15_CFG | 022F 0000h |
| RTI16_CFG | 0230 0000h |
| RTI24_CFG | 0238 0000h |
| RTI25_CFG | 0239 0000h |
| RTI28_CFG | 023C 0000h |
| RTI29_CFG | 023D 0000h |
| RTI30_CFG | 023E 0000h |
| RTI31_CFG | 023F 0000h |
| MCU_RTI0_CFG | 4060 0000h |
| MCU_RTI1_CFG | 4061 0000h |

Figure 15-1. RTI_GCTRL Register

| | | | | | | | |
|----------|----------|----|----|----------|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | RESERVED | | | |
| R-0h | | | | R-0h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| COS | RESERVED | | | | | | |
| R/W-0h | | | | R-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CNT1EN | CNT0EN |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-9. RTI_GCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-20 | RESERVED | R | 0h | Reserved |
| 19-16 | RESERVED | R | 0h | Reserved |
| 15 | COS | R/W | 0h | Continue On Suspend. This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting. User and privilege mode (read): 0h = Counters are stopped while in debug mode 1h = Counters are running while in debug mode Privilege mode (write): 0h = Stop counters in debug mode 1h = Continue counting in debug mode |
| 14-2 | RESERVED | R | 0h | Reserved. |

Table 15-9. RTI_GCTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 1 | CNT1EN | R/W | 0h | Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block1 (UC1 and FRC1). User and privilege mode (read): 0h = Counters are stopped 1h = Counters are running Privilege mode (write): 0h = Stop counters 1h = Start counters |
| 0 | CNT0EN | R/W | 0h | Counter 0 Enable. The CNT0EN bit starts and stops the operation of counter block0 (UC0 and FRC0). User and privilege mode (read): 0h = Counters are stopped 1h = Counters are running Privilege mode (write): 0h = Stop counters 1h = Start counters |

15.2 RTI_TBCTRL Register (Offset = 4h) [reset = 0h]

RTI_TBCTRL is shown in [Figure 15-2](#) and described in [Table 15-11](#).

[Return to Summary Table.](#)

Table 15-10. RTI_TBCTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0004h |
| RTI1_CFG | 0221 0004h |
| RTI15_CFG | 022F 0004h |
| RTI16_CFG | 0230 0004h |
| RTI24_CFG | 0238 0004h |
| RTI25_CFG | 0239 0004h |
| RTI28_CFG | 023C 0004h |
| RTI29_CFG | 023D 0004h |
| RTI30_CFG | 023E 0004h |
| RTI31_CFG | 023F 0004h |
| MCU_RTI0_CFG | 4060 0004h |
| MCU_RTI1_CFG | 4061 0004h |

Figure 15-2. RTI_TBCTRL Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | INC | TBEXT |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-11. RTI_TBCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | INC | R/W | 0h | <p>This bit determines whether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected.</p> <p>User and privilege mode (read): 0h = FRC0 will not be incremented 1h = FRC0 will be incremented</p> <p>Privilege mode (write): 0h = Do not increment FRC0 on failing external clock 1h = Increment FRC0 on failing external clock</p> |

Table 15-11. RTI_TBCTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 0 | TBEXT | R/W | 0h | <p>The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurrence. The only source which is able to increment Free Running Counter 0 is NTUx. When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset. The selection if the external signal should be used, can only be done by software.</p> <p>User and privilege mode (read):</p> <p>0h = UC0 clocks FRC0</p> <p>1h = NTUx clocks FRC0</p> <p>Privilege mode (write):</p> <p>0h = MUX is switched to internal UC0 clocking scheme</p> <p>1h = MUX is switched to external NTUx clocking scheme</p> |

15.3 RTI_CAPCTRL Register (Offset = 8h) [reset = 0h]

RTI_CAPCTRL is shown in [Figure 15-3](#) and described in [Table 15-13](#).

Return to [Summary Table](#).

Table 15-12. RTI_CAPCTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0008h |
| RTI1_CFG | 0221 0008h |
| RTI15_CFG | 022F 0008h |
| RTI16_CFG | 0230 0008h |
| RTI24_CFG | 0238 0008h |
| RTI25_CFG | 0239 0008h |
| RTI28_CFG | 023C 0008h |
| RTI29_CFG | 023D 0008h |
| RTI30_CFG | 023E 0008h |
| RTI31_CFG | 023F 0008h |
| MCU_RTI0_CFG | 4060 0008h |
| MCU_RTI1_CFG | 4061 0008h |

Figure 15-3. RTI_CAPCTRL Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | CAPCNTR1 | CAPCNTR0 |
| R-0h | | | | | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-13. RTI_CAPCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | CAPCNTR1 | R/W | 0h | Capture Counter 1. This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1. User and privilege mode (read): 0h = Capture event is triggered by Capture Event Source 0. 1h = Capture event is triggered by Capture Event Source 1. Privilege mode (write): 0h = Enable capture event triggered by Capture Event Source 0. 1h = Enable capture event triggered by Capture Event Source 1. |

Table 15-13. RTI_CAPCTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 0 | CAPCNTR0 | R/W | 0h | <p>Capture Counter 0. This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0.</p> <p>User and privilege mode (read):</p> <p>0h = Capture event is triggered by Capture Event Source 0</p> <p>1h = Capture event is triggered by Capture Event Source 1</p> <p>Privilege mode (write):</p> <p>0h = Enable capture event triggered by Capture Event Source 0</p> <p>1h = Enable capture event triggered by Capture Event Source 1</p> |

15.4 RTI_COMPCTRL Register (Offset = Ch) [reset = 0h]

RTI_COMPCTRL is shown in [Figure 15-4](#) and described in [Table 15-15](#).

Return to [Summary Table](#).

Table 15-14. RTI_COMPCTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 000Ch |
| RTI1_CFG | 0221 000Ch |
| RTI15_CFG | 022F 000Ch |
| RTI16_CFG | 0230 000Ch |
| RTI24_CFG | 0238 000Ch |
| RTI25_CFG | 0239 000Ch |
| RTI28_CFG | 023C 000Ch |
| RTI29_CFG | 023D 000Ch |
| RTI30_CFG | 023E 000Ch |
| RTI31_CFG | 023F 000Ch |
| MCU_RTI0_CFG | 4060 000Ch |
| MCU_RTI1_CFG | 4061 000Ch |

Figure 15-4. RTI_COMPCTRL Register

| | | | | | | | |
|----------|----|----|----------|----------|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | COMPSEL3 | RESERVED | | | COMPSEL2 |
| R-0h | | | R/W-0h | R-0h | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | COMPSEL1 | RESERVED | | | COMPSEL0 |
| R-0h | | | R/W-0h | R-0h | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-15. RTI_COMPCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-13 | RESERVED | R | 0h | Reserved |
| 12 | COMPSEL3 | R/W | 0h | Compare Select 3. This bit determines the counter with which the compare value hold in compare register 3 is compared. User and privilege mode (read): 0h = Value will be compared with FRC 0 1h = Value will be compared with FRC 1 Privilege mode (write): 0h = Enable compare with FRC 0 1h = Enable compare with FRC 1 |
| 11-9 | RESERVED | R | 0h | Reserved |

Table 15-15. RTI_COMPCTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 8 | COMPSEL2 | R/W | 0h | Compare Select 2. This bit determines the counter with which the compare value hold in compare register 2 is compared. User and privilege mode (read): 0h = Value will be compared with FRC 0 1h = Value will be compared with FRC 1 Privilege mode (write): 0h = Enable compare with FRC 0 1h = Enable compare with FRC 1 |
| 7-5 | RESERVED | R | 0h | Reserved |
| 4 | COMPSEL1 | R/W | 0h | Compare Select 1. This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode (read): 0h = Value will be compared with FRC 0 1h = Value will be compared with FRC 1 Privilege mode (write): 0h = Enable compare with FRC 0 1h = Enable compare with FRC 1 |
| 3-1 | RESERVED | R | 0h | Reserved |
| 0 | COMPSEL0 | R/W | 0h | Compare Select 0. This bit determines the counter with which the compare value hold in compare register 0 is compared. User and privilege mode (read): 0h = Value will be compared with FRC 0 1h = Value will be compared with FRC 1 Privilege mode (write): 0h = Enable compare with FRC 0 1h = Enable compare with FRC 1 |

15.5 RTI_FRC0 Register (Offset = 10h) [reset = 0h]

RTI_FRC0 is shown in [Figure 15-5](#) and described in [Table 15-17](#).

Return to [Summary Table](#).

This registers holds the current value of the Free Running Counter 0 and will be updated continuously.

Table 15-16. RTI_FRC0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0010h |
| RTI1_CFG | 0221 0010h |
| RTI15_CFG | 022F 0010h |
| RTI16_CFG | 0230 0010h |
| RTI24_CFG | 0238 0010h |
| RTI25_CFG | 0239 0010h |
| RTI28_CFG | 023C 0010h |
| RTI29_CFG | 023D 0010h |
| RTI30_CFG | 023E 0010h |
| RTI31_CFG | 023F 0010h |
| MCU_RTI0_CFG | 4060 0010h |
| MCU_RTI1_CFG | 4061 0010h |

Figure 15-5. RTI_FRC0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRC0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-17. RTI_FRC0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | FRC0 | R/W | 0h | Free Running Counter 0. This registers holds the current value of the Free Running Counter 0 and will be updated continuously. User and privilege mode (read): current value of the counter Privilege mode (write): The counter can be preset by writing to this register. The counter increments then from this written value upwards. Presetting counters: If counters have to be preset, they have to be stopped from counting in the RTI_GCTRL register in order to ensure consistency between RTI_UC0 and RTI_FRC0. |

15.6 RTI_UC0 Register (Offset = 14h) [reset = 0h]

RTI_UC0 is shown in [Figure 15-6](#) and described in [Table 15-19](#).

Return to [Summary Table](#).

Table 15-18. RTI_UC0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0014h |
| RTI1_CFG | 0221 0014h |
| RTI15_CFG | 022F 0014h |
| RTI16_CFG | 0230 0014h |
| RTI24_CFG | 0238 0014h |
| RTI25_CFG | 0239 0014h |
| RTI28_CFG | 023C 0014h |
| RTI29_CFG | 023D 0014h |
| RTI30_CFG | 023E 0014h |
| RTI31_CFG | 023F 0014h |
| MCU_RTI0_CFG | 4060 0014h |
| MCU_RTI1_CFG | 4061 0014h |

Figure 15-6. RTI_UC0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UC0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-19. RTI_UC0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | UC0 | R/W | 0h | <p>Up Counter 0. This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0.</p> <p>User and privilege mode (read): Value of the counter when the Free Running Counter 0 was read.</p> <p>Privilege mode (write): The counter can be preset by writing to this register. The counter increments then from this written value upwards.</p> <p>Presetting counters:</p> <p>If counters have to be preset, they have to be stopped from counting in the RTI_GCTRL register in order to ensure consistency between RTI_UC0 and RTI_FRC0.</p> <p>Preset value concern:</p> <p>If the preset value is bigger than the compare value stored in register RTI_CPUC0 then it can take a long time until a compare matches, since RTI_UC0 has to count up until it overflows.</p> |

15.7 RTI_CPUC0 Register (Offset = 18h) [reset = 0h]

RTI_CPUC0 is shown in [Figure 15-7](#) and described in [Table 15-21](#).

[Return to Summary Table.](#)

Table 15-20. RTI_CPUC0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0018h |
| RTI1_CFG | 0221 0018h |
| RTI15_CFG | 022F 0018h |
| RTI16_CFG | 0230 0018h |
| RTI24_CFG | 0238 0018h |
| RTI25_CFG | 0239 0018h |
| RTI28_CFG | 023C 0018h |
| RTI29_CFG | 023D 0018h |
| RTI30_CFG | 023E 0018h |
| RTI31_CFG | 023F 0018h |
| MCU_RTI0_CFG | 4060 0018h |
| MCU_RTI1_CFG | 4061 0018h |

Figure 15-7. RTI_CPUC0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CPUC0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-21. RTI_CPUC0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CPUC0 | R/W | 0h | <p>Compare Up Counter 0. This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI.</p> <p>If CPUC0 = 0: $f_{FRC0} = (RTICLK)/(2^{32})$</p> <p>If CPUC0 \neq 0: $f_{FRC0} = (RTICLK)/(CPUC0+1)$</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write when TBEXT = 0): The compare value is updated</p> <p>Privilege mode (write when TBEXT = 1): The compare value is not changed</p> |

15.8 RTI_CAFRC0 Register (Offset = 20h) [reset = 0h]

RTI_CAFRC0 is shown in [Figure 15-8](#) and described in [Table 15-23](#).

[Return to Summary Table.](#)

Table 15-22. RTI_CAFRC0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0020h |
| RTI1_CFG | 0221 0020h |
| RTI15_CFG | 022F 0020h |
| RTI16_CFG | 0230 0020h |
| RTI24_CFG | 0238 0020h |
| RTI25_CFG | 0239 0020h |
| RTI28_CFG | 023C 0020h |
| RTI29_CFG | 023D 0020h |
| RTI30_CFG | 023E 0020h |
| RTI31_CFG | 023F 0020h |
| MCU_RTI0_CFG | 4060 0020h |
| MCU_RTI1_CFG | 4061 0020h |

Figure 15-8. RTI_CAFRC0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAFRC0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 15-23. RTI_CAFRC0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|---|
| 31-0 | CAFRC0 | R | 0h | Capture Free Running Counter 0. This registers captures the current value of the Free Running Counter 0 when an event occurs, controlled by the external capture control block. User and privilege mode (read): Value of Free Running Counter 0 on a capture event |

15.9 RTI_CAUC0 Register (Offset = 24h) [reset = 0h]

RTI_CAUC0 is shown in [Figure 15-9](#) and described in [Table 15-25](#).

[Return to Summary Table.](#)

Table 15-24. RTI_CAUC0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0024h |
| RTI1_CFG | 0221 0024h |
| RTI15_CFG | 022F 0024h |
| RTI16_CFG | 0230 0024h |
| RTI24_CFG | 0238 0024h |
| RTI25_CFG | 0239 0024h |
| RTI28_CFG | 023C 0024h |
| RTI29_CFG | 023D 0024h |
| RTI30_CFG | 023E 0024h |
| RTI31_CFG | 023F 0024h |
| MCU_RTI0_CFG | 4060 0024h |
| MCU_RTI1_CFG | 4061 0024h |

Figure 15-9. RTI_CAUC0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAUC0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 15-25. RTI_CAUC0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CAUC0 | R | 0h | Capture Up Counter 0. This registers captures the current value of the Up Counter 0 when an event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTI_CAFRC0 register has to be read first, before the RTI_CAUC0 register is read. This sequence ensures that the value of the RTI_CAUC0 register is the corresponding value to the RTI_CAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): Value of Up Counter 0 on a capture event |

15.10 RTI_FRC1 Register (Offset = 30h) [reset = 0h]

RTI_FRC1 is shown in [Figure 15-10](#) and described in [Table 15-27](#).

Return to [Summary Table](#).

Table 15-26. RTI_FRC1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0030h |
| RTI1_CFG | 0221 0030h |
| RTI15_CFG | 022F 0030h |
| RTI16_CFG | 0230 0030h |
| RTI24_CFG | 0238 0030h |
| RTI25_CFG | 0239 0030h |
| RTI28_CFG | 023C 0030h |
| RTI29_CFG | 023D 0030h |
| RTI30_CFG | 023E 0030h |
| RTI31_CFG | 023F 0030h |
| MCU_RTI0_CFG | 4060 0030h |
| MCU_RTI1_CFG | 4061 0030h |

Figure 15-10. RTI_FRC1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-27. RTI_FRC1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | FRC1 | R/W | 0h | Free Running Counter 1. This registers holds the current value of the Free Running Counter 1 and will be updated continuously. User and privilege mode (read): Current value of the counter Privilege mode (write): The counter can be preset by writing to this register. The counter increments then from this written value upwards. Presetting counters: If counters have to be preset, they have to be stopped from counting in the RTI_GCTRL register in order to ensure consistency between UC1 and FRC1. |

15.11 RTI_UC1 Register (Offset = 34h) [reset = 0h]

RTI_UC1 is shown in [Figure 15-11](#) and described in [Table 15-29](#).

Return to [Summary Table](#).

Table 15-28. RTI_UC1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0034h |
| RTI1_CFG | 0221 0034h |
| RTI15_CFG | 022F 0034h |
| RTI16_CFG | 0230 0034h |
| RTI24_CFG | 0238 0034h |
| RTI25_CFG | 0239 0034h |
| RTI28_CFG | 023C 0034h |
| RTI29_CFG | 023D 0034h |
| RTI30_CFG | 023E 0034h |
| RTI31_CFG | 023F 0034h |
| MCU_RTI0_CFG | 4060 0034h |
| MCU_RTI1_CFG | 4061 0034h |

Figure 15-11. RTI_UC1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-29. RTI_UC1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | UC1 | R/W | 0h | <p>Up Counter 1. This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1.</p> <p>User and privilege mode (read): Value of the counter when the Free Running Counter 1 was read</p> <p>Privilege mode (write): The counter can be preset by writing to this register. The counter increments then from this written value upwards.</p> <p>Presetting counters:</p> <p>If counters have to be preset, they have to be disabled in the RTI_GCTRL register in order to ensure consistency between UC1 and FRC1.</p> <p>Preset value concern:</p> <p>If the preset value is bigger than the compare value stored in register RTI_CPUC1 then it can take a long time until a compare matches, since UC1 has to count up until it overflows.</p> |

15.12 RTI_CPUC1 Register (Offset = 38h) [reset = 0h]

RTI_CPUC1 is shown in [Figure 15-12](#) and described in [Table 15-31](#).

Return to [Summary Table](#).

Table 15-30. RTI_CPUC1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0038h |
| RTI1_CFG | 0221 0038h |
| RTI15_CFG | 022F 0038h |
| RTI16_CFG | 0230 0038h |
| RTI24_CFG | 0238 0038h |
| RTI25_CFG | 0239 0038h |
| RTI28_CFG | 023C 0038h |
| RTI29_CFG | 023D 0038h |
| RTI30_CFG | 023E 0038h |
| RTI31_CFG | 023F 0038h |
| MCU_RTI0_CFG | 4060 0038h |
| MCU_RTI1_CFG | 4061 0038h |

Figure 15-12. RTI_CPUC1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CPUC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-31. RTI_CPUC1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CPUC1 | R/W | 0h | <p>Compare Up Counter 1. This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI.</p> <p>If CPUC1 = 0: $f_{FRC1} = (RTICLK)/(2^{32})$</p> <p>If CPUC1 \neq 0: $f_{FRC1} = (RTICLK)/(CPUC1+1)$</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): The compare value is updated</p> |

15.13 RTI_CAFRC1 Register (Offset = 40h) [reset = 0h]

RTI_CAFRC1 is shown in [Figure 15-13](#) and described in [Table 15-33](#).

[Return to Summary Table.](#)

Table 15-32. RTI_CAFRC1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0040h |
| RTI1_CFG | 0221 0040h |
| RTI15_CFG | 022F 0040h |
| RTI16_CFG | 0230 0040h |
| RTI24_CFG | 0238 0040h |
| RTI25_CFG | 0239 0040h |
| RTI28_CFG | 023C 0040h |
| RTI29_CFG | 023D 0040h |
| RTI30_CFG | 023E 0040h |
| RTI31_CFG | 023F 0040h |
| MCU_RTI0_CFG | 4060 0040h |
| MCU_RTI1_CFG | 4061 0040h |

Figure 15-13. RTI_CAFRC1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAFRC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 15-33. RTI_CAFRC1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------|------|-------|---|
| 31-0 | CAFRC1 | R | 0h | Capture Free Running Counter 1. This registers captures the current value of the Free Running Counter 1 when an event occurs, controlled by the external capture control block. User and privilege mode (read): Value of Free Running Counter 1 on a capture event |

15.14 RTI_CAUC1 Register (Offset = 44h) [reset = 0h]

RTI_CAUC1 is shown in [Figure 15-14](#) and described in [Table 15-35](#).

Return to [Summary Table](#).

Table 15-34. RTI_CAUC1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0044h |
| RTI1_CFG | 0221 0044h |
| RTI15_CFG | 022F 0044h |
| RTI16_CFG | 0230 0044h |
| RTI24_CFG | 0238 0044h |
| RTI25_CFG | 0239 0044h |
| RTI28_CFG | 023C 0044h |
| RTI29_CFG | 023D 0044h |
| RTI30_CFG | 023E 0044h |
| RTI31_CFG | 023F 0044h |
| MCU_RTI0_CFG | 4060 0044h |
| MCU_RTI1_CFG | 4061 0044h |

Figure 15-14. RTI_CAUC1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAUC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 15-35. RTI_CAUC1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CAUC1 | R | 0h | Capture Up Counter 1. This registers captures the current value of the Up Counter 1 when an event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTI_CAFRC1 register has to be read first, before the RTI_CAUC1 register is read. This sequence ensures that the value of the RTI_CAUC0 register is the corresponding value to the RTI_CAFRC0 register, even if another capture event happens in between the two reads. User and privilege mode (read): Value of Up Counter 1 on a capture event |

15.15 RTI_COMP0 Register (Offset = 50h) [reset = 0h]

RTI_COMP0 is shown in [Figure 15-15](#) and described in [Table 15-37](#).

[Return to Summary Table.](#)

Table 15-36. RTI_COMP0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0050h |
| RTI1_CFG | 0221 0050h |
| RTI15_CFG | 022F 0050h |
| RTI16_CFG | 0230 0050h |
| RTI24_CFG | 0238 0050h |
| RTI25_CFG | 0239 0050h |
| RTI28_CFG | 023C 0050h |
| RTI29_CFG | 023D 0050h |
| RTI30_CFG | 023E 0050h |
| RTI31_CFG | 023F 0050h |
| MCU_RTI0_CFG | 4060 0050h |
| MCU_RTI1_CFG | 4061 0050h |

Figure 15-15. RTI_COMP0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-37. RTI_COMP0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | COMP0 | R/W | 0h | <p>Compare 0. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.16 RTI_UDCP0 Register (Offset = 54h) [reset = 0h]

RTI_UDCP0 is shown in [Figure 15-16](#) and described in [Table 15-39](#).

Return to [Summary Table](#).

Table 15-38. RTI_UDCP0 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0054h |
| RTI1_CFG | 0221 0054h |
| RTI15_CFG | 022F 0054h |
| RTI16_CFG | 0230 0054h |
| RTI24_CFG | 0238 0054h |
| RTI25_CFG | 0239 0054h |
| RTI28_CFG | 023C 0054h |
| RTI29_CFG | 023D 0054h |
| RTI30_CFG | 023E 0054h |
| RTI31_CFG | 023F 0054h |
| MCU_RTI0_CFG | 4060 0054h |
| MCU_RTI1_CFG | 4061 0054h |

Figure 15-16. RTI_UDCP0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UDCP0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-39. RTI_UDCP0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | UDCP0 | R/W | 0h | Update Compare 0 Register. This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): Value to be added to the compare 0 register on the next compare match Privilege mode (write): New update value |

15.17 RTI_COMP1 Register (Offset = 58h) [reset = 0h]

RTI_COMP1 is shown in [Figure 15-17](#) and described in [Table 15-41](#).

[Return to Summary Table.](#)

Table 15-40. RTI_COMP1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0058h |
| RTI1_CFG | 0221 0058h |
| RTI15_CFG | 022F 0058h |
| RTI16_CFG | 0230 0058h |
| RTI24_CFG | 0238 0058h |
| RTI25_CFG | 0239 0058h |
| RTI28_CFG | 023C 0058h |
| RTI29_CFG | 023D 0058h |
| RTI30_CFG | 023E 0058h |
| RTI31_CFG | 023F 0058h |
| MCU_RTI0_CFG | 4060 0058h |
| MCU_RTI1_CFG | 4061 0058h |

Figure 15-17. RTI_COMP1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-41. RTI_COMP1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | COMP1 | R/W | 0h | <p>Compare 1. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.18 RTI_UDCP1 Register (Offset = 5Ch) [reset = 0h]

RTI_UDCP1 is shown in [Figure 15-18](#) and described in [Table 15-43](#).

Return to [Summary Table](#).

Table 15-42. RTI_UDCP1 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 005Ch |
| RTI1_CFG | 0221 005Ch |
| RTI15_CFG | 022F 005Ch |
| RTI16_CFG | 0230 005Ch |
| RTI24_CFG | 0238 005Ch |
| RTI25_CFG | 0239 005Ch |
| RTI28_CFG | 023C 005Ch |
| RTI29_CFG | 023D 005Ch |
| RTI30_CFG | 023E 005Ch |
| RTI31_CFG | 023F 005Ch |
| MCU_RTI0_CFG | 4060 005Ch |
| MCU_RTI1_CFG | 4061 005Ch |

Figure 15-18. RTI_UDCP1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UDCP1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-43. RTI_UDCP1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | UDCP1 | R/W | 0h | Update Compare 1 Register. This registers holds a value, which is added to the value in the compare 1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): Value to be added to the compare 1 register on the next compare match Privilege mode (write): New update value |

15.19 RTI_COMP2 Register (Offset = 60h) [reset = 0h]

RTI_COMP2 is shown in [Figure 15-19](#) and described in [Table 15-45](#).

[Return to Summary Table.](#)

Table 15-44. RTI_COMP2 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0060h |
| RTI1_CFG | 0221 0060h |
| RTI15_CFG | 022F 0060h |
| RTI16_CFG | 0230 0060h |
| RTI24_CFG | 0238 0060h |
| RTI25_CFG | 0239 0060h |
| RTI28_CFG | 023C 0060h |
| RTI29_CFG | 023D 0060h |
| RTI30_CFG | 023E 0060h |
| RTI31_CFG | 023F 0060h |
| MCU_RTI0_CFG | 4060 0060h |
| MCU_RTI1_CFG | 4061 0060h |

Figure 15-19. RTI_COMP2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-45. RTI_COMP2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | COMP2 | R/W | 0h | <p>Compare 2. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.20 RTI_UDCP2 Register (Offset = 64h) [reset = 0h]

RTI_UDCP2 is shown in [Figure 15-20](#) and described in [Table 15-47](#).

Return to [Summary Table](#).

This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.

Table 15-46. RTI_UDCP2 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0064h |
| RTI1_CFG | 0221 0064h |
| RTI15_CFG | 022F 0064h |
| RTI16_CFG | 0230 0064h |
| RTI24_CFG | 0238 0064h |
| RTI25_CFG | 0239 0064h |
| RTI28_CFG | 023C 0064h |
| RTI29_CFG | 023D 0064h |
| RTI30_CFG | 023E 0064h |
| RTI31_CFG | 023F 0064h |
| MCU_RTI0_CFG | 4060 0064h |
| MCU_RTI1_CFG | 4061 0064h |

Figure 15-20. RTI_UDCP2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UDCP2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-47. RTI_UDCP2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | UDCP2 | R/W | 0h | <p>Update Compare 2 Register. This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.</p> <p>User and privilege mode (read): Value to be added to the compare 2 register on the next compare match</p> <p>Privilege mode (write): New update value</p> |

15.21 RTI_COMP3 Register (Offset = 68h) [reset = 0h]

RTI_COMP3 is shown in [Figure 15-21](#) and described in [Table 15-49](#).

[Return to Summary Table.](#)

Table 15-48. RTI_COMP3 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0068h |
| RTI1_CFG | 0221 0068h |
| RTI15_CFG | 022F 0068h |
| RTI16_CFG | 0230 0068h |
| RTI24_CFG | 0238 0068h |
| RTI25_CFG | 0239 0068h |
| RTI28_CFG | 023C 0068h |
| RTI29_CFG | 023D 0068h |
| RTI30_CFG | 023E 0068h |
| RTI31_CFG | 023F 0068h |
| MCU_RTI0_CFG | 4060 0068h |
| MCU_RTI1_CFG | 4061 0068h |

Figure 15-21. RTI_COMP3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-49. RTI_COMP3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | COMP3 | R/W | 0h | <p>Compare 3. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.22 RTI_UDCP3 Register (Offset = 6Ch) [reset = 0h]

RTI_UDCP3 is shown in [Figure 15-22](#) and described in [Table 15-51](#).

Return to [Summary Table](#).

Table 15-50. RTI_UDCP3 Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 006Ch |
| RTI1_CFG | 0221 006Ch |
| RTI15_CFG | 022F 006Ch |
| RTI16_CFG | 0230 006Ch |
| RTI24_CFG | 0238 006Ch |
| RTI25_CFG | 0239 006Ch |
| RTI28_CFG | 023C 006Ch |
| RTI29_CFG | 023D 006Ch |
| RTI30_CFG | 023E 006Ch |
| RTI31_CFG | 023F 006Ch |
| MCU_RTI0_CFG | 4060 006Ch |
| MCU_RTI1_CFG | 4061 006Ch |

Figure 15-22. RTI_UDCP3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UDCP3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-51. RTI_UDCP3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | UDCP3 | R/W | 0h | Update Compare 3 Register. This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention. User and privilege mode (read): Value to be added to the compare 3 register on the next compare match Privilege mode (write): New update value |

15.23 RTI_TBLCOMP Register (Offset = 70h) [reset = 0h]

RTI_TBLCOMP is shown in [Figure 15-23](#) and described in [Table 15-53](#).

[Return to Summary Table.](#)

Table 15-52. RTI_TBLCOMP Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0070h |
| RTI1_CFG | 0221 0070h |
| RTI15_CFG | 022F 0070h |
| RTI16_CFG | 0230 0070h |
| RTI24_CFG | 0238 0070h |
| RTI25_CFG | 0239 0070h |
| RTI28_CFG | 023C 0070h |
| RTI29_CFG | 023D 0070h |
| RTI30_CFG | 023E 0070h |
| RTI31_CFG | 023F 0070h |
| MCU_RTI0_CFG | 4060 0070h |
| MCU_RTI1_CFG | 4061 0070h |

Figure 15-23. RTI_TBLCOMP Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBLCOMP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 15-53. RTI_TBLCOMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31-0 | TBLCOMP | R | 0h | Reserved |

15.24 RTI_TBHCOMP Register (Offset = 74h) [reset = 0h]

RTI_TBHCOMP is shown in [Figure 15-24](#) and described in [Table 15-55](#).

Return to [Summary Table](#).

Table 15-54. RTI_TBHCOMP Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0074h |
| RTI1_CFG | 0221 0074h |
| RTI15_CFG | 022F 0074h |
| RTI16_CFG | 0230 0074h |
| RTI24_CFG | 0238 0074h |
| RTI25_CFG | 0239 0074h |
| RTI28_CFG | 023C 0074h |
| RTI29_CFG | 023D 0074h |
| RTI30_CFG | 023E 0074h |
| RTI31_CFG | 023F 0074h |
| MCU_RTI0_CFG | 4060 0074h |
| MCU_RTI1_CFG | 4061 0074h |

Figure 15-24. RTI_TBHCOMP Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBHCOMP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-55. RTI_TBHCOMP Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31-0 | TBHCOMP | R | 0h | Reserved |

15.25 RTI_SETINT Register (Offset = 80h) [reset = 0h]

RTI_SETINT is shown in [Figure 15-25](#) and described in [Table 15-57](#).

Return to [Summary Table](#).

This register prevents the necessity of a read-modify-write operation if a particular interrupt should be enabled.

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Table 15-56. RTI_SETINT Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0080h |
| RTI1_CFG | 0221 0080h |
| RTI15_CFG | 022F 0080h |
| RTI16_CFG | 0230 0080h |
| RTI24_CFG | 0238 0080h |
| RTI25_CFG | 0239 0080h |
| RTI28_CFG | 023C 0080h |
| RTI29_CFG | 023D 0080h |
| RTI30_CFG | 023E 0080h |
| RTI31_CFG | 023F 0080h |
| MCU_RTI0_CFG | 4060 0080h |
| MCU_RTI1_CFG | 4061 0080h |

Figure 15-25. RTI_SETINT Register

| | | | | | | | |
|----------|----|----|----|----------|------------|------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | SETOVL1INT | SETOVL0INT | SETTBINT |
| R-0h | | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | SETDMA3 | SETDMA2 | SETDMA1 | SETDMA0 |
| R-0h | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | SETINT3 | SETINT2 | SETINT1 | SETINT0 |
| R-0h | | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 15-57. RTI_SETINT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-19 | RESERVED | R | 0h | Reserved |

Table 15-57. RTI_SETINT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|------------|-------|-------|---|
| 18 | SETOVL1INT | R/W1S | 0h | Set Free Running Counter 1 Overflow Interrupt. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |
| 17 | SETOVL0INT | R/W1S | 0h | Set Free Running Counter 0 Overflow Interrupt. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |
| 16 | SETTBINT | R/W1S | 0h | User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |
| 15-12 | RESERVED | R | 0h | Reserved |
| 11 | SETDMA3 | R/W1S | 0h | Set Compare DMA Request 3. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable DMA request |
| 10 | SETDMA2 | R/W1S | 0h | Set Compare DMA Request 2. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable DMA request |
| 9 | SETDMA1 | R/W1S | 0h | Set Compare DMA Request 1. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable DMA request |
| 8 | SETDMA0 | R/W1S | 0h | Set Compare DMA Request 0. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable DMA request |
| 7-4 | RESERVED | R | 0h | Reserved |

Table 15-57. RTI_SETINT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|-------|-------|---|
| 3 | SETINT3 | R/W1S | 0h | Set Compare Interrupt 3. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |
| 2 | SETINT2 | R/W1S | 0h | Set Compare Interrupt 2. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |
| 1 | SETINT1 | R/W1S | 0h | Set Compare Interrupt 1. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |
| 0 | SETINT0 | R/W1S | 0h | Set Compare Interrupt 0. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Enable interrupt |

15.26 RTI_CLEARINT Register (Offset = 84h) [reset = 0h]

RTI_CLEARINT is shown in [Figure 15-26](#) and described in [Table 15-59](#).

Return to [Summary Table](#).

This register prevents the necessity of a read-modify-write operation if a particular interrupt should be disabled.

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Table 15-58. RTI_CLEARINT Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0084h |
| RTI1_CFG | 0221 0084h |
| RTI15_CFG | 022F 0084h |
| RTI16_CFG | 0230 0084h |
| RTI24_CFG | 0238 0084h |
| RTI25_CFG | 0239 0084h |
| RTI28_CFG | 023C 0084h |
| RTI29_CFG | 023D 0084h |
| RTI30_CFG | 023E 0084h |
| RTI31_CFG | 023F 0084h |
| MCU_RTI0_CFG | 4060 0084h |
| MCU_RTI1_CFG | 4061 0084h |

Figure 15-26. RTI_CLEARINT Register

| | | | | | | | |
|----------|----|----|----|-----------|------------------|------------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | CLEAROVL1IN T | CLEAROVL0IN T | CLEARBTINT |
| R-0h | | | | R/W1C-0h | | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | CLEARDMA3 | CLEARDMA2 | CLEARDMA1 | CLEARDMA0 |
| R-0h | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | CLEARINT3 | CLEARINT2 | CLEARINT1 | CLEARINT0 |
| R-0h | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-59. RTI_CLEARINT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-19 | RESERVED | R | 0h | Reserved |

Table 15-59. RTI_CLEARINT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------------|-------|-------|--|
| 18 | CLEAROVL1INT | R/W1C | 0h | Clear Free Running Counter 1 Overflow Interrupt. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable interrupt |
| 17 | CLEAROVL0INT | R/W1C | 0h | Clear Free Running Counter 0 Overflow Interrupt. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable interrupt |
| 16 | CLEARTBINT | R/W1C | 0h | User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable interrupt |
| 15-12 | RESERVED | R | 0h | Reserved |
| 11 | CLEARDMA3 | R/W1C | 0h | Clear Compare DMA Request 3. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable DMA request |
| 10 | CLEARDMA2 | R/W1C | 0h | Clear Compare DMA Request 2. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable DMA request |
| 9 | CLEARDMA1 | R/W1C | 0h | Clear Compare DMA Request 1. User and privilege mode (read): 0h = DMA request is disabled 1h = DMA request is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable DMA request |
| 8 | CLEARDMA0 | R/W1C | 0h | Clear Compare DMA Request 0. |
| 7-4 | RESERVED | R | 0h | Reserved |
| 3 | CLEARINT3 | R/W1C | 0h | Clear Compare Interrupt 3. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable interrupt |

Table 15-59. RTI_CLEARINT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|-------|-------|--|
| 2 | CLEARINT2 | R/W1C | 0h | Clear Compare Interrupt 2. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable interrupt |
| 1 | CLEARINT1 | R/W1C | 0h | Clear Compare Interrupt 1. |
| 0 | CLEARINT0 | R/W1C | 0h | Clear Compare Interrupt 0. User and privilege mode (read): 0h = Interrupt is disabled 1h = Interrupt is enabled Privilege mode (write): 0h = Leaves the corresponding bit unchanged 1h = Disable interrupt |

15.27 RTI_INTFLAG Register (Offset = 88h) [reset = 0h]

RTI_INTFLAG is shown in [Figure 15-27](#) and described in [Table 15-61](#).

Return to [Summary Table](#).

The corresponding flags are set at every compare match of Free Running Counterx and RTICOMPx value, regardless if the interrupt is enabled or not.

Table 15-60. RTI_INTFLAG Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0088h |
| RTI1_CFG | 0221 0088h |
| RTI15_CFG | 022F 0088h |
| RTI16_CFG | 0230 0088h |
| RTI24_CFG | 0238 0088h |
| RTI25_CFG | 0239 0088h |
| RTI28_CFG | 023C 0088h |
| RTI29_CFG | 023D 0088h |
| RTI30_CFG | 023E 0088h |
| RTI31_CFG | 023F 0088h |
| MCU_RTI0_CFG | 4060 0088h |
| MCU_RTI1_CFG | 4061 0088h |

Figure 15-27. RTI_INTFLAG Register

| | | | | | | | |
|----------|----|----|----|----------|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | OVL1INT | OVL0INT | TBINT |
| R-0h | | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | INT3 | INT2 | INT1 | INT0 |
| R-0h | | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-61. RTI_INTFLAG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|-------|-------|--|
| 31-19 | RESERVED | R | 0h | Reserved |
| 18 | OVL1INT | R/W1C | 0h | Free Running Counter 1 Overflow Interrupt Flag. User and privilege mode (read): Determines if an interrupt is pending 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |

Table 15-61. RTI_INTFLAG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 17 | OVL0INT | R/W1C | 0h | Free Running Counter 0 Overflow Interrupt Flag. User and privilege mode (read): Determines if an interrupt is pending 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |
| 16 | TBINT | R/W1C | 0h | User and privilege mode (read): this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software. Determines if an interrupt is pending: 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |
| 15-4 | RESERVED | R | 0h | Reserved |
| 3 | INT3 | R/W1C | 0h | Interrupt Flag 3. User and privilege mode (read): Determines if an interrupt is pending 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |
| 2 | INT2 | R/W1C | 0h | Interrupt Flag 2. User and privilege mode (read): Determines if an interrupt is pending 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |
| 1 | INT1 | R/W1C | 0h | Interrupt Flag 1. User and privilege mode (read): Determines if an interrupt is pending 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |
| 0 | INT0 | R/W1C | 0h | Interrupt Flag 0. User and privilege mode (read): Determines if an interrupt is pending 0h = No interrupt pending 1h = Interrupt pending Privilege mode (write): 0h = Leaves the bit unchanged 1h = Set the bit to 0 |

15.28 RTI_DWDCTRL Register (Offset = 90h) [reset = 5312ACEDh]

RTI_DWDCTRL is shown in [Figure 15-28](#) and described in [Table 15-63](#).

Return to [Summary Table](#).

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

This register's functionality is dependent on whether the DWD is implemented to be always enabled or not. If the DWD is always enabled, then the DWD is automatically enabled after system reset is released and cannot be disabled by software. In that case, this register is redundant and any writes to this register have no effect on the DWD functionality. If, however, the DWD is not enabled upon release of system reset, then the software has to write to the DWDCTRL field in order to enable the DWD, as described below. Once enabled, the watchdog can only be disabled by a system reset. The application cannot disable the watchdog. The RTI_DWDCTRL register also implements a one-time-write constraint. That is, once the application writes to this register to enable the watchdog, all further writes are ignored.

Table 15-62. RTI_DWDCTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0090h |
| RTI1_CFG | 0221 0090h |
| RTI15_CFG | 022F 0090h |
| RTI16_CFG | 0230 0090h |
| RTI24_CFG | 0238 0090h |
| RTI25_CFG | 0239 0090h |
| RTI28_CFG | 023C 0090h |
| RTI29_CFG | 023D 0090h |
| RTI30_CFG | 023E 0090h |
| RTI31_CFG | 023F 0090h |
| MCU_RTI0_CFG | 4060 0090h |
| MCU_RTI1_CFG | 4061 0090h |

Figure 15-28. RTI_DWDCTRL Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DWDCTRL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-5312ACEDh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-63. RTI_DWDCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-----------|--|
| 31-0 | DWDCTRL | R/W | 5312ACEDh | <p>Digital Watchdog Control.</p> <p>User and privilege mode (read):</p> <p>5312ACEDh = DWD counter is disabled. This is the default value.</p> <p>A98559DAh = DWD counter is enabled</p> <p>Any other value = DWD counter state is unchanged (enabled or disabled)</p> <p>Privilege mode (write):</p> <p>A98559DAh = DWD counter is enabled</p> <p>Any other value = State of DWD counter is unchanged (stays enabled or disabled)</p> <p>Note: One-Write Functionality of DWDCTRL Register:</p> <p>The RTI_DWDCTRL register implements a one-write functionality, such that the application cannot write to this register more than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTI_DWDCTRL will only be enabled after a system reset again.</p> |

15.29 RTI_DWDPRLD Register (Offset = 94h) [reset = FFFh]

RTI_DWDPRLD is shown in [Figure 15-29](#) and described in [Table 15-65](#).

Return to [Summary Table](#).

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Table 15-64. RTI_DWDPRLD Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0094h |
| RTI1_CFG | 0221 0094h |
| RTI15_CFG | 022F 0094h |
| RTI16_CFG | 0230 0094h |
| RTI24_CFG | 0238 0094h |
| RTI25_CFG | 0239 0094h |
| RTI28_CFG | 023C 0094h |
| RTI29_CFG | 023D 0094h |
| RTI30_CFG | 023E 0094h |
| RTI31_CFG | 023F 0094h |
| MCU_RTI0_CFG | 4060 0094h |
| MCU_RTI1_CFG | 4061 0094h |

Figure 15-29. RTI_DWDPRLD Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | DWDPRLD | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | R/W-FFFh | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-65. RTI_DWDPRLD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-12 | RESERVED | R | 0h | Reserved |
| 11-0 | DWDPRLD | R/W | FFFh | <p>Digital Watchdog Preload Value.</p> <p>User and privilege mode (read): A read from this register in any CPU mode returns the current preload value.</p> <p>Privilege mode (write): If the DWD is always enabled after reset is released: The DWD starts counting down from the reset value of the counter, that is, 0x002DFFFF.</p> <p>The application can configure the DWD preload register any time before this down counter expires.</p> <p>When the application services the DWD, the preload register contents are copied left-justified into the DWD down counter and it starts counting down from that value.</p> <p>If the DWD is implemented such that the down counter is enabled by software: The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter.</p> <p>The expiration time of the DWD Down Counter can be determined with following equation: $ARRAY(0x1F75D70)$ where:</p> <p>$RTI_DWDPRLD = 0 \dots 4095$</p> |

15.30 RTI_WDSTATUS Register (Offset = 98h) [reset = 0h]

RTI_WDSTATUS is shown in [Figure 15-30](#) and described in [Table 15-67](#).

Return to [Summary Table](#).

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

The values of the following status bits will not be affected by a system reset. These bits are cleared by a power up reset, or by the application.

Table 15-66. RTI_WDSTATUS Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 0098h |
| RTI1_CFG | 0221 0098h |
| RTI15_CFG | 022F 0098h |
| RTI16_CFG | 0230 0098h |
| RTI24_CFG | 0238 0098h |
| RTI25_CFG | 0239 0098h |
| RTI28_CFG | 023C 0098h |
| RTI29_CFG | 023D 0098h |
| RTI30_CFG | 023E 0098h |
| RTI31_CFG | 023F 0098h |
| MCU_RTI0_CFG | 4060 0098h |
| MCU_RTI1_CFG | 4061 0098h |

Figure 15-30. RTI_WDSTATUS Register

| | | | | | | | |
|----------|----|----------|----------|----------|----------|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | DWWD_ST | END | START | KEYST | DWDST | AWDST |
| R-0h | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 15-67. RTI_WDSTATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-6 | RESERVED | R | 0h | Reserved |

Table 15-67. RTI_WDSTATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|-------|-------|---|
| 5 | DWWD_ST | R/W1C | 0h | <p>Windowed Watchdog Status. This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog.</p> <p>User and privilege mode (read):</p> <p>0h = No time-window violation has occurred.</p> <p>1h = A time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case.</p> <p>Privilege mode (write):</p> <p>0h = Leaves the current value unchanged.</p> <p>1h = Clears the bit to 0. This will also clear all other status flags in the RTI_WDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD.</p> |
| 4 | END | R/W1C | 0h | <p>Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag.</p> <p>User and privilege mode (read):</p> <p>0h = No end-time window violation has occurred.</p> <p>1h = The end-time defined by the windowed watchdog configuration has been violated.</p> <p>Privilege mode (write):</p> <p>0h = Leaves the current value unchanged.</p> <p>1h = Clears the bit to 0.</p> |
| 3 | START | R/W1C | 0h | <p>Windowed Watchdog End Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened.</p> <p>User and privilege mode (read):</p> <p>0h = No start-time window violation has occurred.</p> <p>1h = The start-time defined by the windowed watchdog configuration has been violated.</p> <p>Privilege mode (write):</p> <p>0h = Leaves the current value unchanged.</p> <p>1h = Clears the bit to 0.</p> |
| 2 | KEYST | R/W1C | 0h | <p>Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTI_WDKEY register.</p> <p>User and privilege mode (read):</p> <p>0h = No wrong key or key-sequence written</p> <p>1h = Wrong key or key-sequence written to RTI_WDKEY register</p> <p>Privilege mode (write):</p> <p>0h = Leaves the current value unchanged</p> <p>1h = Clears the bit to 0</p> |

Table 15-67. RTI_WDSTATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|-------|-------|--|
| 1 | DWDST | R/W1C | 0h | Digital Watchdog Status. Status flag and is maintained for compatibility reasons. User and privilege mode (read): 0h = DWD timeout period not expired 1h = DWD timeout period has expired Privilege mode (write): 0h = Leaves the current value unchanged 1h = Clears the bit to 0 |
| 0 | AWDST | R/W1C | 0h | Analog Watchdog Status. User and privilege mode (read): 0h = AWD pin 0 > 1 threshold not exceeded 1h = AWD pin 0 > 1 threshold exceeded Privilege mode (write): 0h = Leaves the current value unchanged 1h = Clears the bit to 0 |

15.31 RTI_WDKEY Register (Offset = 9Ch) [reset = A35Ch]

RTI_WDKEY is shown in [Figure 15-31](#) and described in [Table 15-69](#).

Return to [Summary Table](#).

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Table 15-68. RTI_WDKEY Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 009Ch |
| RTI1_CFG | 0221 009Ch |
| RTI15_CFG | 022F 009Ch |
| RTI16_CFG | 0230 009Ch |
| RTI24_CFG | 0238 009Ch |
| RTI25_CFG | 0239 009Ch |
| RTI28_CFG | 023C 009Ch |
| RTI29_CFG | 023D 009Ch |
| RTI30_CFG | 023E 009Ch |
| RTI31_CFG | 023F 009Ch |
| MCU_RTI0_CFG | 4060 009Ch |
| MCU_RTI1_CFG | 4061 009Ch |

Figure 15-31. RTI_WDKEY Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | WDKEY | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R/W-A35Ch | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-69. RTI_WDKEY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31-16 | RESERVED | R | 0h | Reserved |

Table 15-69. RTI_WDKEY Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 15-0 | WDKEY | R/W | A35Ch | <p>Watchdog Key.</p> <p>User and privilege mode reads are indeterminate.</p> <p>Privilege mode (write): A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1's.</p> <p>Writing any other value causes a digital watchdog reset.</p> <p>Note: Watchdog reset is not supported in this family of devices.</p> <p>Note: Register write access time precaution: The user has to take into account that the write to the register takes 3 RTI_ICLK cycle. This needs to be considered for the AWD/DWD expiration calculation.</p> <p>Example of a WDKEY sequence</p> <p>Step -> Value written to WDKEY -> Result</p> <p>1 -> 0x0A35C -> No Action</p> <p>2 -> 0x0A35C -> No Action</p> <p>3 -> 0x0E51A -> WDKEY is enabled for reset by next 0x0A35C</p> <p>4 -> 0x0E51A -> WDKEY is enabled for reset by next 0x0A35C</p> <p>5 -> 0x0E51A -> WDKEY is enabled for reset by next 0x0A35C</p> <p>6 -> 0x0A35C -> Watchdog is reset</p> <p>7 -> 0x0A35C -> No Action</p> <p>8 -> 0x0E51A -> WDKEY is enabled for reset by next 0x0A35C</p> <p>9 -> 0x0A35C -> Watchdog is reset</p> <p>10 -> 0x0E51A -> WDKEY is enabled for reset by next 0x0A35C</p> <p>11 -> 0x02345 -> System reset; incorrect value written to WDKEY</p> |

15.32 RTI_DWDCNTR Register (Offset = A0h) [reset = 01FFFFFFh]

RTI_DWDCNTR is shown in [Figure 15-32](#) and described in [Table 15-71](#).

Return to [Summary Table](#).

Note

Some of the RTI features described in this section may not be supported on this family of devices. For more information, see *RTI Not Supported Features*.

Table 15-70. RTI_DWDCNTR Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00A0h |
| RTI1_CFG | 0221 00A0h |
| RTI15_CFG | 022F 00A0h |
| RTI16_CFG | 0230 00A0h |
| RTI24_CFG | 0238 00A0h |
| RTI25_CFG | 0239 00A0h |
| RTI28_CFG | 023C 00A0h |
| RTI29_CFG | 023D 00A0h |
| RTI30_CFG | 023E 00A0h |
| RTI31_CFG | 023F 00A0h |
| MCU_RTI0_CFG | 4060 00A0h |
| MCU_RTI1_CFG | 4061 00A0h |

Figure 15-32. RTI_DWDCNTR Register

| | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|-------------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | DWDCNTR | | | | | | | |
| R-0h | | | | | | | | R-01FFFFFFh | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DWDCNTR | | | | | | | | | | | | | | | |
| R-01FFFFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 15-71. RTI_DWDCNTR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-----------|---|
| 31-25 | RESERVED | R | 0h | Reserved |
| 24-0 | DWDCNTR | R | 01FFFFFFh | Digital Watchdog Down Counter. The value of the DWDCNTR after a system reset is 01FFFFFFh. When the DWD is enabled and the DWD counter starts counting down from this value with an RTI_FCLK time base of 3 MHz, a watchdog reset will be generated in 1 second. User and privilege mode (read): Reads return the current counter value. Privilege mode (write): Writes don't have an effect. |

15.33 RTI_WWDRXNCTRL Register (Offset = A4h) [reset = 5h]

RTI_WWDRXNCTRL is shown in [Figure 15-33](#) and described in [Table 15-73](#).

[Return to Summary Table.](#)

Table 15-72. RTI_WWDRXNCTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00A4h |
| RTI1_CFG | 0221 00A4h |
| RTI15_CFG | 022F 00A4h |
| RTI16_CFG | 0230 00A4h |
| RTI24_CFG | 0238 00A4h |
| RTI25_CFG | 0239 00A4h |
| RTI28_CFG | 023C 00A4h |
| RTI29_CFG | 023D 00A4h |
| RTI30_CFG | 023E 00A4h |
| RTI31_CFG | 023F 00A4h |
| MCU_RTI0_CFG | 4060 00A4h |
| MCU_RTI1_CFG | 4061 00A4h |

Figure 15-33. RTI_WWDRXNCTRL Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | WWDRXN | | | |
| R-0h | | | | | | | | | | | | R/W-5h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-73. RTI_WWDRXNCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved |
| 3-0 | WWDRXN | R/W | 5h | <p>Digital Windowed Watchdog Reaction.</p> <p>User and privilege mode (read), privileged mode (write):</p> <p>5h = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>Note: Watchdog reset is not supported in this family of devices.</p> <p>Ah = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all. Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>Configuration of DWWD Reaction: The DWWD reaction can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.</p> |

15.34 RTI_WWDSIZECTRL Register (Offset = A8h) [reset = 5h]

RTI_WWDSIZECTRL is shown in [Figure 15-34](#) and described in [Table 15-75](#).

Return to [Summary Table](#).

Table 15-74. RTI_WWDSIZECTRL Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00A8h |
| RTI1_CFG | 0221 00A8h |
| RTI15_CFG | 022F 00A8h |
| RTI16_CFG | 0230 00A8h |
| RTI24_CFG | 0238 00A8h |
| RTI25_CFG | 0239 00A8h |
| RTI28_CFG | 023C 00A8h |
| RTI29_CFG | 023D 00A8h |
| RTI30_CFG | 023E 00A8h |
| RTI31_CFG | 023F 00A8h |
| MCU_RTI0_CFG | 4060 00A8h |
| MCU_RTI1_CFG | 4061 00A8h |

Figure 15-34. RTI_WWDSIZECTRL Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WWDSIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-5h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-75. RTI_WWDSIZECTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | WWDSIZE | R/W | 5h | <p>Digital Windowed Watchdog Window Size.</p> <p>User and privilege mode (read), privileged mode (write):</p> <p>Value written to WWDSIZE: 0000 0005h = 100% Window Size (The functionality is the same as the standard time-out digital watchdog.)</p> <p>Value written to WWDSIZE: 0000 0050h = 50% Window Size</p> <p>Value written to WWDSIZE: 0000 0500h = 25% Window Size</p> <p>Value written to WWDSIZE: 0000 5000h = 12.5% Window Size</p> <p>Value written to WWDSIZE: 0005 0000h = 6.25% Window Size</p> <p>Value written to WWDSIZE: 0050 0000h = 3.125% Window Size</p> <p>Value written to WWDSIZE: Any other value = 3.125% Window Size</p> <p>Incorrect value being written to watchdog window size control register: If an incorrect value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 5h, 50h, 500h, 5000h, 50000h, or 500000h, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration.</p> <p>Configuration of DWWD Window Size: The DWWD window size can be selected by the application even when the DWWD counter is already enabled. If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately. If a change to the WWDSIZE is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.</p> |

15.35 RTI_INTCLRENABLE Register (Offset = ACh) [reset = 05050505h]

RTI_INTCLRENABLE is shown in [Figure 15-35](#) and described in [Table 15-77](#).

[Return to Summary Table.](#)

Table 15-76. RTI_INTCLRENABLE Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00ACh |
| RTI1_CFG | 0221 00ACh |
| RTI15_CFG | 022F 00ACh |
| RTI16_CFG | 0230 00ACh |
| RTI24_CFG | 0238 00ACh |
| RTI25_CFG | 0239 00ACh |
| RTI28_CFG | 023C 00ACh |
| RTI29_CFG | 023D 00ACh |
| RTI30_CFG | 023E 00ACh |
| RTI31_CFG | 023F 00ACh |
| MCU_RTI0_CFG | 4060 00ACh |
| MCU_RTI1_CFG | 4061 00ACh |

Figure 15-35. RTI_INTCLRENABLE Register

| | | | | | | | |
|----------|----|----|----|---------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | INTCLRENABLE3 | | | |
| R-0h | | | | R/W-5h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | INTCLRENABLE2 | | | |
| R-0h | | | | R/W-5h | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | INTCLRENABLE1 | | | |
| R-0h | | | | R/W-5h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | INTCLRENABLE0 | | | |
| R-0h | | | | R/W-5h | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 15-77. RTI_INTCLRENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 31-28 | RESERVED | R | 0h | Reserved |
| 27-24 | INTCLRENABLE3 | R/W | 5h | Enables the auto-clear functionality on the compare 3 interrupt. User and Privileged mode (read): 5h = Auto-clear for compare 3 interrupt is disabled. Any other value = Auto-clear for compare 3 interrupt is enabled. Privileged mode (write): 5h = Disables the auto-clear functionality on the compare 3 interrupt. Any other value = Enables the auto-clear functionality on the compare 3 interrupt. |
| 23-20 | RESERVED | R | 0h | Reserved |

Table 15-77. RTI_INTCLRENABLE Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|---------------|------|-------|--|
| 19-16 | INTCLRENABLE2 | R/W | 5h | Enables the auto-clear functionality on the compare 2 interrupt. User and Privileged mode (read): 5h = Auto-clear for compare 2 interrupt is disabled. Any other value = Auto-clear for compare 2 interrupt is enabled. Privileged mode (write): 5h = Disables the auto-clear functionality on the compare 2 interrupt. Any other value = Enables the auto-clear functionality on the compare 2 interrupt. |
| 15-12 | RESERVED | R | 0h | Reserved |
| 11-8 | INTCLRENABLE1 | R/W | 5h | Enables the auto-clear functionality on the compare 1 interrupt. User and Privileged mode (read): 5h = Auto-clear for compare 1 interrupt is disabled. Any other value = Auto-clear for compare 1 interrupt is enabled. Privileged mode (write): 5h = Disables the auto-clear functionality on the compare 1 interrupt. Any other value = Enables the auto-clear functionality on the compare 1 interrupt. |
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | INTCLRENABLE0 | R/W | 5h | Enables the auto-clear functionality on the compare 0 interrupt. User and Privileged mode (read): 5h = Auto-clear for compare 0 interrupt is disabled. Any other value = Auto-clear for compare 0 interrupt is enabled. Privileged mode (write): 5h = Disables the auto-clear functionality on the compare 0 interrupt. Any other value = Enables the auto-clear functionality on the compare 0 interrupt. Hook-up of Compare Interrupt to a device pin: The RTI module generates up to 4 compare interrupts. The connection between one or more of these compare interrupt(s) to a device pin is completely device-dependent. Refer to the device datasheet to identify the actual pin(s) that connects to the compare interrupt(s). |

15.36 RTI_COMP0CLR Register (Offset = B0h) [reset = 0h]

RTI_COMP0CLR is shown in [Figure 15-36](#) and described in [Table 15-79](#).

Return to [Summary Table](#).

Table 15-78. RTI_COMP0CLR Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00B0h |
| RTI1_CFG | 0221 00B0h |
| RTI15_CFG | 022F 00B0h |
| RTI16_CFG | 0230 00B0h |
| RTI24_CFG | 0238 00B0h |
| RTI25_CFG | 0239 00B0h |
| RTI28_CFG | 023C 00B0h |
| RTI29_CFG | 023D 00B0h |
| RTI30_CFG | 023E 00B0h |
| RTI31_CFG | 023F 00B0h |
| MCU_RTI0_CFG | 4060 00B0h |
| MCU_RTI1_CFG | 4061 00B0h |

Figure 15-36. RTI_COMP0CLR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP0CLR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-79. RTI_COMP0CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | COMP0CLR | R/W | 0h | <p>Compare 0 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared.</p> <p>User and privilege mode (read): current compare value</p> <p>Privilege mode (write): update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.37 RTI_COMP1CLR Register (Offset = B4h) [reset = 0h]

RTI_COMP1CLR is shown in [Figure 15-37](#) and described in [Table 15-81](#).

[Return to Summary Table.](#)

Table 15-80. RTI_COMP1CLR Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00B4h |
| RTI1_CFG | 0221 00B4h |
| RTI15_CFG | 022F 00B4h |
| RTI16_CFG | 0230 00B4h |
| RTI24_CFG | 0238 00B4h |
| RTI25_CFG | 0239 00B4h |
| RTI28_CFG | 023C 00B4h |
| RTI29_CFG | 023D 00B4h |
| RTI30_CFG | 023E 00B4h |
| RTI31_CFG | 023F 00B4h |
| MCU_RTI0_CFG | 4060 00B4h |
| MCU_RTI1_CFG | 4061 00B4h |

Figure 15-37. RTI_COMP1CLR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP1CLR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-81. RTI_COMP1CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | COMP1CLR | R/W | 0h | <p>Compare 1 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 1 interrupt or DMA request line is cleared.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.38 RTI_COMP2CLR Register (Offset = B8h) [reset = 0h]

RTI_COMP2CLR is shown in [Figure 15-38](#) and described in [Table 15-83](#).

Return to [Summary Table](#).

Table 15-82. RTI_COMP2CLR Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00B8h |
| RTI1_CFG | 0221 00B8h |
| RTI15_CFG | 022F 00B8h |
| RTI16_CFG | 0230 00B8h |
| RTI24_CFG | 0238 00B8h |
| RTI25_CFG | 0239 00B8h |
| RTI28_CFG | 023C 00B8h |
| RTI29_CFG | 023D 00B8h |
| RTI30_CFG | 023E 00B8h |
| RTI31_CFG | 023F 00B8h |
| MCU_RTI0_CFG | 4060 00B8h |
| MCU_RTI1_CFG | 4061 00B8h |

Figure 15-38. RTI_COMP2CLR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP2CLR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-83. RTI_COMP2CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | COMP2CLR | R/W | 0h | <p>Compare 2 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 2 interrupt or DMA request line is cleared.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

15.39 RTI_COMP3CLR Register (Offset = BCh) [reset = 0h]

RTI_COMP3CLR is shown in [Figure 15-39](#) and described in [Table 15-85](#).

Return to [Summary Table](#).

Table 15-84. RTI_COMP3CLR Instances

| Instance | Physical Address |
|--------------|------------------|
| RTI0_CFG | 0220 00BCh |
| RTI1_CFG | 0221 00BCh |
| RTI15_CFG | 022F 00BCh |
| RTI16_CFG | 0230 00BCh |
| RTI24_CFG | 0238 00BCh |
| RTI25_CFG | 0239 00BCh |
| RTI28_CFG | 023C 00BCh |
| RTI29_CFG | 023D 00BCh |
| RTI30_CFG | 023E 00BCh |
| RTI31_CFG | 023F 00BCh |
| MCU_RTI0_CFG | 4060 00BCh |
| MCU_RTI1_CFG | 4061 00BCh |

Figure 15-39. RTI_COMP3CLR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMP3CLR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 15-85. RTI_COMP3CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-0 | COMP3CLR | R/W | 0h | <p>Compare 3 Clear. This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 3 interrupt or DMA request line is cleared.</p> <p>User and privilege mode (read): Current compare value</p> <p>Privilege mode (write): Update of the compare register with a new compare value</p> <p>Reset behavior:</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

16 Timers Registers

Table 16-2 lists the memory-mapped registers for the TIMER. All register offset addresses not listed in Table 16-2 should be considered as reserved locations and the register contents should not be modified.

Table 16-1. Timers Instances

| Instance | Base Address |
|----------------|--------------|
| TIMER0_CFG | 0240 0000h |
| TIMER1_CFG | 0241 0000h |
| TIMER2_CFG | 0242 0000h |
| TIMER3_CFG | 0243 0000h |
| TIMER4_CFG | 0244 0000h |
| TIMER5_CFG | 0245 0000h |
| TIMER6_CFG | 0246 0000h |
| TIMER7_CFG | 0247 0000h |
| TIMER8_CFG | 0248 0000h |
| TIMER9_CFG | 0249 0000h |
| TIMER10_CFG | 024A 0000h |
| TIMER11_CFG | 024B 0000h |
| TIMER12_CFG | 024C 0000h |
| TIMER13_CFG | 024D 0000h |
| TIMER14_CFG | 024E 0000h |
| TIMER15_CFG | 024F 0000h |
| TIMER16_CFG | 0250 0000h |
| TIMER17_CFG | 0251 0000h |
| TIMER18_CFG | 0252 0000h |
| TIMER19_CFG | 0253 0000h |
| MCU_TIMER0_CFG | 4040 0000h |
| MCU_TIMER1_CFG | 4041 0000h |
| MCU_TIMER2_CFG | 4042 0000h |
| MCU_TIMER3_CFG | 4043 0000h |
| MCU_TIMER4_CFG | 4044 0000h |
| MCU_TIMER5_CFG | 4045 0000h |
| MCU_TIMER6_CFG | 4046 0000h |
| MCU_TIMER7_CFG | 4047 0000h |
| MCU_TIMER8_CFG | 4048 0000h |
| MCU_TIMER9_CFG | 4049 0000h |

Table 16-2. Timers Registers

| Offset | Acronym | Register Name | TIMER0_CFG Physical Address | TIMER1_CFG Physical Address | TIMER2_CFG Physical Address |
|--------|-------------------------------------|-------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| 0h | TIMER_TIDR | Revision register | 0240 0000h | 0241 0000h | 0242 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 0240 0010h | 0241 0010h | 0242 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 0240 0020h | 0241 0020h | 0242 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 0240 0024h | 0241 0024h | 0242 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 0240 0028h | 0241 0028h | 0242 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 0240 002Ch | 0241 002Ch | 0242 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 0240 0030h | 0241 0030h | 0242 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 0240 0034h | 0241 0034h | 0242 0034h |
| 38h | TIMER_TCLR | Timer control register | 0240 0038h | 0241 0038h | 0242 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 0240 003Ch | 0241 003Ch | 0242 003Ch |

Table 16-2. Timers Registers (continued)

| Offset | Acronym | Register Name | TIMER0_CFG Physical Address | TIMER1_CFG Physical Address | TIMER2_CFG Physical Address |
|--------|-----------------------------|--|-----------------------------------|-----------------------------------|-----------------------------------|
| 40h | TIMER_TLDR | Timer load register | 0240 0040h | 0241 0040h | 0242 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 0240 0044h | 0241 0044h | 0242 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 0240 0048h | 0241 0048h | 0242 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 0240 004Ch | 0241 004Ch | 0242 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 0240 0050h | 0241 0050h | 0242 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 0240 0054h | 0241 0054h | 0242 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 0240 0058h | 0241 0058h | 0242 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 0240 005Ch | 0241 005Ch | 0242 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 0240 0060h | 0241 0060h | 0242 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 0240 0064h | 0241 0064h | 0242 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 0240 0068h | 0241 0068h | 0242 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 0240 006Ch | 0241 006Ch | 0242 006Ch |

Table 16-3. Timers Registers

| Offset | Acronym | Register Name | TIMER3_CFG Physical Address | TIMER4_CFG Physical Address | TIMER5_CFG Physical Address |
|--------|-------------------------------------|--|-----------------------------------|-----------------------------------|-----------------------------------|
| 0h | TIMER_TIDR | Revision register | 0243 0000h | 0244 0000h | 0245 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 0243 0010h | 0244 0010h | 0245 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 0243 0020h | 0244 0020h | 0245 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 0243 0024h | 0244 0024h | 0245 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 0243 0028h | 0244 0028h | 0245 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 0243 002Ch | 0244 002Ch | 0245 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 0243 0030h | 0244 0030h | 0245 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 0243 0034h | 0244 0034h | 0245 0034h |
| 38h | TIMER_TCLR | Timer control register | 0243 0038h | 0244 0038h | 0245 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 0243 003Ch | 0244 003Ch | 0245 003Ch |
| 40h | TIMER_TLDR | Timer load register | 0243 0040h | 0244 0040h | 0245 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 0243 0044h | 0244 0044h | 0245 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 0243 0048h | 0244 0048h | 0245 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 0243 004Ch | 0244 004Ch | 0245 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 0243 0050h | 0244 0050h | 0245 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 0243 0054h | 0244 0054h | 0245 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 0243 0058h | 0244 0058h | 0245 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 0243 005Ch | 0244 005Ch | 0245 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 0243 0060h | 0244 0060h | 0245 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 0243 0064h | 0244 0064h | 0245 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 0243 0068h | 0244 0068h | 0245 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 0243 006Ch | 0244 006Ch | 0245 006Ch |

Table 16-4. Timers Registers

| Offset | Acronym | Register Name | TIMER6_CFG Physical Address | TIMER7_CFG Physical Address | TIMER8_CFG Physical Address |
|--------|-------------------------------------|--|-----------------------------------|-----------------------------------|-----------------------------------|
| 0h | TIMER_TIDR | Revision register | 0246 0000h | 0247 0000h | 0248 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 0246 0010h | 0247 0010h | 0248 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 0246 0020h | 0247 0020h | 0248 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 0246 0024h | 0247 0024h | 0248 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 0246 0028h | 0247 0028h | 0248 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 0246 002Ch | 0247 002Ch | 0248 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 0246 0030h | 0247 0030h | 0248 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 0246 0034h | 0247 0034h | 0248 0034h |
| 38h | TIMER_TCLR | Timer control register | 0246 0038h | 0247 0038h | 0248 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 0246 003Ch | 0247 003Ch | 0248 003Ch |
| 40h | TIMER_TLDR | Timer load register | 0246 0040h | 0247 0040h | 0248 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 0246 0044h | 0247 0044h | 0248 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 0246 0048h | 0247 0048h | 0248 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 0246 004Ch | 0247 004Ch | 0248 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 0246 0050h | 0247 0050h | 0248 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 0246 0054h | 0247 0054h | 0248 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 0246 0058h | 0247 0058h | 0248 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 0246 005Ch | 0247 005Ch | 0248 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 0246 0060h | 0247 0060h | 0248 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 0246 0064h | 0247 0064h | 0248 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 0246 0068h | 0247 0068h | 0248 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 0246 006Ch | 0247 006Ch | 0248 006Ch |

Table 16-5. Timers Registers

| Offset | Acronym | Register Name | TIMER9_CFG Physical Address | TIMER10_CFG Physical Address | TIMER11_CFG Physical Address |
|--------|-------------------------------------|--|-----------------------------------|------------------------------------|------------------------------------|
| 0h | TIMER_TIDR | Revision register | 0249 0000h | 024A 0000h | 024B 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 0249 0010h | 024A 0010h | 024B 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 0249 0020h | 024A 0020h | 024B 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 0249 0024h | 024A 0024h | 024B 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 0249 0028h | 024A 0028h | 024B 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 0249 002Ch | 024A 002Ch | 024B 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 0249 0030h | 024A 0030h | 024B 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 0249 0034h | 024A 0034h | 024B 0034h |
| 38h | TIMER_TCLR | Timer control register | 0249 0038h | 024A 0038h | 024B 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 0249 003Ch | 024A 003Ch | 024B 003Ch |
| 40h | TIMER_TLDR | Timer load register | 0249 0040h | 024A 0040h | 024B 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 0249 0044h | 024A 0044h | 024B 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 0249 0048h | 024A 0048h | 024B 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 0249 004Ch | 024A 004Ch | 024B 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 0249 0050h | 024A 0050h | 024B 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 0249 0054h | 024A 0054h | 024B 0054h |

Table 16-5. Timers Registers (continued)

| Offset | Acronym | Register Name | TIMER9_CFG Physical Address | TIMER10_CFG Physical Address | TIMER11_CFG Physical Address |
|--------|-----------------------------|--|-----------------------------------|------------------------------------|------------------------------------|
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 0249 0058h | 024A 0058h | 024B 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 0249 005Ch | 024A 005Ch | 024B 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 0249 0060h | 024A 0060h | 024B 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 0249 0064h | 024A 0064h | 024B 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 0249 0068h | 024A 0068h | 024B 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 0249 006Ch | 024A 006Ch | 024B 006Ch |

Table 16-6. Timers Registers

| Offset | Acronym | Register Name | TIMER12_CFG Physical Address | TIMER13_CFG Physical Address | TIMER14_CFG Physical Address |
|--------|-------------------------------------|--|------------------------------------|------------------------------------|------------------------------------|
| 0h | TIMER_TIDR | Revision register | 024C 0000h | 024D 0000h | 024E 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 024C 0010h | 024D 0010h | 024E 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 024C 0020h | 024D 0020h | 024E 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 024C 0024h | 024D 0024h | 024E 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 024C 0028h | 024D 0028h | 024E 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 024C 002Ch | 024D 002Ch | 024E 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 024C 0030h | 024D 0030h | 024E 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 024C 0034h | 024D 0034h | 024E 0034h |
| 38h | TIMER_TCLR | Timer control register | 024C 0038h | 024D 0038h | 024E 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 024C 003Ch | 024D 003Ch | 024E 003Ch |
| 40h | TIMER_TLDR | Timer load register | 024C 0040h | 024D 0040h | 024E 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 024C 0044h | 024D 0044h | 024E 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 024C 0048h | 024D 0048h | 024E 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 024C 004Ch | 024D 004Ch | 024E 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 024C 0050h | 024D 0050h | 024E 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 024C 0054h | 024D 0054h | 024E 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 024C 0058h | 024D 0058h | 024E 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 024C 005Ch | 024D 005Ch | 024E 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 024C 0060h | 024D 0060h | 024E 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 024C 0064h | 024D 0064h | 024E 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 024C 0068h | 024D 0068h | 024E 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 024C 006Ch | 024D 006Ch | 024E 006Ch |

Table 16-7. Timers Registers

| Offset | Acronym | Register Name | TIMER15_CFG Physical Address | TIMER16_CFG Physical Address | TIMER17_CFG Physical Address |
|--------|-------------------------------------|-------------------------------|------------------------------------|------------------------------------|------------------------------------|
| 0h | TIMER_TIDR | Revision register | 024F 0000h | 0250 0000h | 0251 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 024F 0010h | 0250 0010h | 0251 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 024F 0020h | 0250 0020h | 0251 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 024F 0024h | 0250 0024h | 0251 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 024F 0028h | 0250 0028h | 0251 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 024F 002Ch | 0250 002Ch | 0251 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 024F 0030h | 0250 0030h | 0251 0030h |

Table 16-7. Timers Registers (continued)

| Offset | Acronym | Register Name | TIMER15_CFG Physical Address | TIMER16_CFG Physical Address | TIMER17_CFG Physical Address |
|--------|---------------------------------|--|------------------------------------|------------------------------------|------------------------------------|
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 024F 0034h | 0250 0034h | 0251 0034h |
| 38h | TIMER_TCLR | Timer control register | 024F 0038h | 0250 0038h | 0251 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 024F 003Ch | 0250 003Ch | 0251 003Ch |
| 40h | TIMER_TLDR | Timer load register | 024F 0040h | 0250 0040h | 0251 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 024F 0044h | 0250 0044h | 0251 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 024F 0048h | 0250 0048h | 0251 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 024F 004Ch | 0250 004Ch | 0251 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 024F 0050h | 0250 0050h | 0251 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 024F 0054h | 0250 0054h | 0251 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 024F 0058h | 0250 0058h | 0251 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 024F 005Ch | 0250 005Ch | 0251 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 024F 0060h | 0250 0060h | 0251 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 024F 0064h | 0250 0064h | 0251 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 024F 0068h | 0250 0068h | 0251 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 024F 006Ch | 0250 006Ch | 0251 006Ch |

Table 16-8. Timers Registers

| Offset | Acronym | Register Name | TIMER18_CFG Physical Address | TIMER19_CFG Physical Address |
|--------|-------------------------------------|--|---------------------------------|---------------------------------|
| 0h | TIMER_TIDR | Revision register | 0252 0000h | 0253 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 0252 0010h | 0253 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 0252 0020h | 0253 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 0252 0024h | 0253 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 0252 0028h | 0253 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 0252 002Ch | 0253 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 0252 0030h | 0253 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 0252 0034h | 0253 0034h |
| 38h | TIMER_TCLR | Timer control register | 0252 0038h | 0253 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 0252 003Ch | 0253 003Ch |
| 40h | TIMER_TLDR | Timer load register | 0252 0040h | 0253 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 0252 0044h | 0253 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 0252 0048h | 0253 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 0252 004Ch | 0253 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 0252 0050h | 0253 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 0252 0054h | 0253 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 0252 0058h | 0253 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 0252 005Ch | 0253 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 0252 0060h | 0253 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 0252 0064h | 0253 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 0252 0068h | 0253 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 0252 006Ch | 0253 006Ch |

Table 16-9. Timers Registers

| Offset | Acronym | Register Name | MCU_TIMER0_CFG Physical Address | MCU_TIMER1_CFG Physical Address | MCU_TIMER2_CFG Physical Address |
|--------|-------------------------------------|--|---------------------------------|---------------------------------|---------------------------------|
| 0h | TIMER_TIDR | Revision register | 4040 0000h | 4041 0000h | 4042 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 4040 0010h | 4041 0010h | 4042 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 4040 0020h | 4041 0020h | 4042 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 4040 0024h | 4041 0024h | 4042 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 4040 0028h | 4041 0028h | 4042 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 4040 002Ch | 4041 002Ch | 4042 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 4040 0030h | 4041 0030h | 4042 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 4040 0034h | 4041 0034h | 4042 0034h |
| 38h | TIMER_TCLR | Timer control register | 4040 0038h | 4041 0038h | 4042 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 4040 003Ch | 4041 003Ch | 4042 003Ch |
| 40h | TIMER_TLDR | Timer load register | 4040 0040h | 4041 0040h | 4042 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 4040 0044h | 4041 0044h | 4042 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 4040 0048h | 4041 0048h | 4042 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 4040 004Ch | 4041 004Ch | 4042 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 4040 0050h | 4041 0050h | 4042 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 4040 0054h | 4041 0054h | 4042 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 4040 0058h | 4041 0058h | 4042 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 4040 005Ch | 4041 005Ch | 4042 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 4040 0060h | 4041 0060h | 4042 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 4040 0064h | 4041 0064h | 4042 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 4040 0068h | 4041 0068h | 4042 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 4040 006Ch | 4041 006Ch | 4042 006Ch |

Table 16-10. Timers Registers

| Offset | Acronym | Register Name | MCU_TIMER3_CFG Physical Address | MCU_TIMER4_CFG Physical Address |
|--------|-------------------------------------|--|---------------------------------|---------------------------------|
| 0h | TIMER_TIDR | Revision register | 4043 0000h | 4044 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 4043 0010h | 4044 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 4043 0020h | 4044 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 4043 0024h | 4044 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 4043 0028h | 4044 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 4043 002Ch | 4044 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 4043 0030h | 4044 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 4043 0034h | 4044 0034h |
| 38h | TIMER_TCLR | Timer control register | 4043 0038h | 4044 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 4043 003Ch | 4044 003Ch |
| 40h | TIMER_TLDR | Timer load register | 4043 0040h | 4044 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 4043 0044h | 4044 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 4043 0048h | 4044 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 4043 004Ch | 4044 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 4043 0050h | 4044 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 4043 0054h | 4044 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 4043 0058h | 4044 0058h |

Table 16-10. Timers Registers (continued)

| Offset | Acronym | Register Name | MCU_TIMER3_CFG Physical Address | MCU_TIMER4_CFG Physical Address |
|--------|----------------------------|-----------------------------------|---------------------------------|---------------------------------|
| 5Ch | TIMER_TPIR | Timer positive increment register | 4043 005Ch | 4044 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 4043 0060h | 4044 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 4043 0064h | 4044 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 4043 0068h | 4044 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 4043 006Ch | 4044 006Ch |

Table 16-11. Timers Registers

| Offset | Acronym | Register Name | MCU_TIMER5_CFG Physical Address | MCU_TIMER6_CFG Physical Address |
|--------|-------------------------------------|--|---------------------------------|---------------------------------|
| 0h | TIMER_TIDR | Revision register | 4045 0000h | 4046 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 4045 0010h | 4046 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 4045 0020h | 4046 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 4045 0024h | 4046 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 4045 0028h | 4046 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 4045 002Ch | 4046 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 4045 0030h | 4046 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 4045 0034h | 4046 0034h |
| 38h | TIMER_TCLR | Timer control register | 4045 0038h | 4046 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 4045 003Ch | 4046 003Ch |
| 40h | TIMER_TLDR | Timer load register | 4045 0040h | 4046 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 4045 0044h | 4046 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 4045 0048h | 4046 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 4045 004Ch | 4046 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 4045 0050h | 4046 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 4045 0054h | 4046 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 4045 0058h | 4046 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 4045 005Ch | 4046 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 4045 0060h | 4046 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 4045 0064h | 4046 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 4045 0068h | 4046 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 4045 006Ch | 4046 006Ch |

Table 16-12. Timers Registers

| Offset | Acronym | Register Name | MCU_TIMER7_CFG Physical Address | MCU_TIMER8_CFG Physical Address | MCU_TIMER9_CFG Physical Address |
|--------|-------------------------------------|-------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 0h | TIMER_TIDR | Revision register | 4047 0000h | 4048 0000h | 4049 0000h |
| 10h | TIMER_TIOCP_CFG | CBASS0 Configuration register | 4047 0010h | 4048 0010h | 4049 0010h |
| 20h | TIMER_IRQ_EOI | End-Of-Interrupt register | 4047 0020h | 4048 0020h | 4049 0020h |
| 24h | TIMER_IRQSTATUS_RAW | Timer raw status register | 4047 0024h | 4048 0024h | 4049 0024h |
| 28h | TIMER_IRQSTATUS | Timer status register | 4047 0028h | 4048 0028h | 4049 0028h |
| 2Ch | TIMER_IRQSTATUS_SET | Interrupt enable register | 4047 002Ch | 4048 002Ch | 4049 002Ch |
| 30h | TIMER_IRQSTATUS_CLR | Interrupt disable register | 4047 0030h | 4048 0030h | 4049 0030h |
| 34h | TIMER_IRQWAKEEN | Wake-up enable register | 4047 0034h | 4048 0034h | 4049 0034h |
| 38h | TIMER_TCLR | Timer control register | 4047 0038h | 4048 0038h | 4049 0038h |
| 3Ch | TIMER_TCRR | Timer counter register | 4047 003Ch | 4048 003Ch | 4049 003Ch |

Table 16-12. Timers Registers (continued)

| Offset | Acronym | Register Name | MCU_TIMER7_ CFG Physical Address | MCU_TIMER8_ CFG Physical Address | MCU_TIMER9_ CFG Physical Address |
|--------|-----------------------------|--|--|--|--|
| 40h | TIMER_TLDR | Timer load register | 4047 0040h | 4048 0040h | 4049 0040h |
| 44h | TIMER_TTGR | Timer trigger register | 4047 0044h | 4048 0044h | 4049 0044h |
| 48h | TIMER_TWPS | Timer write-posted register | 4047 0048h | 4048 0048h | 4049 0048h |
| 4Ch | TIMER_TMAR | Timer match register | 4047 004Ch | 4048 004Ch | 4049 004Ch |
| 50h | TIMER_TCAR1 | First captured value of the timer counter | 4047 0050h | 4048 0050h | 4049 0050h |
| 54h | TIMER_TSICR | Timer synchronous interface control register | 4047 0054h | 4048 0054h | 4049 0054h |
| 58h | TIMER_TCAR2 | Second captured value of the timer counter | 4047 0058h | 4048 0058h | 4049 0058h |
| 5Ch | TIMER_TPIR | Timer positive increment register | 4047 005Ch | 4048 005Ch | 4049 005Ch |
| 60h | TIMER_TNIR | Timer negative increment register | 4047 0060h | 4048 0060h | 4049 0060h |
| 64h | TIMER_TCVR | Timer CVR counter register | 4047 0064h | 4048 0064h | 4049 0064h |
| 68h | TIMER_TOCR | Timer overflow counter register | 4047 0068h | 4048 0068h | 4049 0068h |
| 6Ch | TIMER_TOWR | Timer overflow wrapping register | 4047 006Ch | 4048 006Ch | 4049 006Ch |

16.1 TIMER_TIDR Register (Offset = 0h) [reset = 5000 3900h]

TIMER_TIDR is shown in [Figure 16-1](#) and described in [Table 16-14](#).

Return to [Summary Table](#).

This read-only register contains the revision number of the module. A write to this register has no effect. This register is used by software to track features, bugs, and compatibility.

Table 16-13. TIMER_TIDR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0000h |
| TIMER1_CFG | 0241 0000h |
| TIMER2_CFG | 0242 0000h |
| TIMER3_CFG | 0243 0000h |
| TIMER4_CFG | 0244 0000h |
| TIMER5_CFG | 0245 0000h |
| TIMER6_CFG | 0246 0000h |
| TIMER7_CFG | 0247 0000h |
| TIMER8_CFG | 0248 0000h |
| TIMER9_CFG | 0249 0000h |
| TIMER10_CFG | 024A 0000h |
| TIMER11_CFG | 024B 0000h |
| TIMER12_CFG | 024C 0000h |
| TIMER13_CFG | 024D 0000h |
| TIMER14_CFG | 024E 0000h |
| TIMER15_CFG | 024F 0000h |
| TIMER16_CFG | 0250 0000h |
| TIMER17_CFG | 0251 0000h |
| TIMER18_CFG | 0252 0000h |
| TIMER19_CFG | 0253 0000h |
| MCU_TIMER0_CFG | 4040 0000h |
| MCU_TIMER1_CFG | 4041 0000h |
| MCU_TIMER2_CFG | 4042 0000h |
| MCU_TIMER3_CFG | 4043 0000h |
| MCU_TIMER4_CFG | 4044 0000h |
| MCU_TIMER5_CFG | 4045 0000h |
| MCU_TIMER6_CFG | 4046 0000h |
| MCU_TIMER7_CFG | 4047 0000h |
| MCU_TIMER8_CFG | 4048 0000h |
| MCU_TIMER9_CFG | 4049 0000h |

Figure 16-1. TIMER_TIDR Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| REVISION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-5000 3900h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 16-14. TIMER_TIDR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|------------|-------------|
| 31-0 | REVISION | R | 5000 3900h | IP Revision |

16.2 TIMER_TIOCP_CFG Register (Offset = 10h) [reset = 8h]

TIMER_TIOCP_CFG is shown in [Figure 16-2](#) and described in [Table 16-16](#).

Return to [Summary Table](#).

This register controls the various parameters of the CBASS0/MCU_CBASS0 interface.

Note

Some of the timers features described in this section may not be supported on this family of devices. For more information, see *Timers Not Supported Features*.

Table 16-15. TIMER_TIOCP_CFG Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0010h |
| TIMER1_CFG | 0241 0010h |
| TIMER2_CFG | 0242 0010h |
| TIMER3_CFG | 0243 0010h |
| TIMER4_CFG | 0244 0010h |
| TIMER5_CFG | 0245 0010h |
| TIMER6_CFG | 0246 0010h |
| TIMER7_CFG | 0247 0010h |
| TIMER8_CFG | 0248 0010h |
| TIMER9_CFG | 0249 0010h |
| TIMER10_CFG | 024A 0010h |
| TIMER11_CFG | 024B 0010h |
| TIMER12_CFG | 024C 0010h |
| TIMER13_CFG | 024D 0010h |
| TIMER14_CFG | 024E 0010h |
| TIMER15_CFG | 024F 0010h |
| TIMER16_CFG | 0250 0010h |
| TIMER17_CFG | 0251 0010h |
| TIMER18_CFG | 0252 0010h |
| TIMER19_CFG | 0253 0010h |
| MCU_TIMER0_CFG | 4040 0010h |
| MCU_TIMER1_CFG | 4041 0010h |
| MCU_TIMER2_CFG | 4042 0010h |
| MCU_TIMER3_CFG | 4043 0010h |
| MCU_TIMER4_CFG | 4044 0010h |
| MCU_TIMER5_CFG | 4045 0010h |
| MCU_TIMER6_CFG | 4046 0010h |
| MCU_TIMER7_CFG | 4047 0010h |
| MCU_TIMER8_CFG | 4048 0010h |
| MCU_TIMER9_CFG | 4049 0010h |

Figure 16-2. TIMER_TIOCP_CFG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |

Figure 16-2. TIMER_TIOCP_CFG Register (continued)

| | | | | | | | |
|----------|----|----|----|----------|----|---------|-----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | IDLEMODE | | EMUFREE | SOFTRESET |
| R-0h | | | | R/W-2h | | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-16. TIMER_TIOCP_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-4 | RESERVED | R | 0h | Reserved |
| 3-2 | IDLEMODE | R/W | 2h | Power management, req/ack control 0h = Force-idle mode: local target idle state follows (acknowledges) the system clock stop requests unconditionally, that is, regardless of the IP module internal requirements. Back-up mode, for debug only. 1h = No-idle mode: local target never enters idle state. Back-up mode, for debug only. 2h = Smart-idle mode: local target idle state eventually follows (acknowledges) the system clock stop requests, depending on the IP module internal requirements. IP module should not generate (IRQ-request-related) wake-up events. 3h = Smart-idle wake-up-capable mode: local target idle state eventually follows (acknowledges) the system clock stop requests, depending on the IP module internal requirements. IP module may generate (IRQ-request-related) wake-up events when in IDLE state. Mode is relevant only if the appropriate IP modules wake-up output(s) is (are) implemented. |
| 1 | EMUFREE | R/W | 0h | Emulation mode 0h = The timer is frozen in emulation mode (PINSUSPENDN signal active). 1h = The timer runs free, regardless of PINSUSPENDN value. |
| 0 | SOFTRESET | R/W | 0h | Software reset Read 0h = Reset done, no pending action Write 0h = No action Read 1h = Initiate software reset Write 1h = Reset ongoing. |

16.3 TIMER_IRQ_EOI Register (Offset = 20h) [reset = 0h]

TIMER_IRQ_EOI is shown in [Figure 16-3](#) and described in [Table 16-18](#).

Return to [Summary Table](#).

Software End-Of-Interrupt: Allows the generation of further pulses on the interrupt line, if a new interrupt event is pending, when using the pulsed output. Unused when using the level interrupt line (depending on module integration).

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 16-17. TIMER_IRQ_EOI Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0020h |
| TIMER1_CFG | 0241 0020h |
| TIMER2_CFG | 0242 0020h |
| TIMER3_CFG | 0243 0020h |
| TIMER4_CFG | 0244 0020h |
| TIMER5_CFG | 0245 0020h |
| TIMER6_CFG | 0246 0020h |
| TIMER7_CFG | 0247 0020h |
| TIMER8_CFG | 0248 0020h |
| TIMER9_CFG | 0249 0020h |
| TIMER10_CFG | 024A 0020h |
| TIMER11_CFG | 024B 0020h |
| TIMER12_CFG | 024C 0020h |
| TIMER13_CFG | 024D 0020h |
| TIMER14_CFG | 024E 0020h |
| TIMER15_CFG | 024F 0020h |
| TIMER16_CFG | 0250 0020h |
| TIMER17_CFG | 0251 0020h |
| TIMER18_CFG | 0252 0020h |
| TIMER19_CFG | 0253 0020h |
| MCU_TIMER0_CFG | 4040 0020h |
| MCU_TIMER1_CFG | 4041 0020h |
| MCU_TIMER2_CFG | 4042 0020h |
| MCU_TIMER3_CFG | 4043 0020h |
| MCU_TIMER4_CFG | 4044 0020h |
| MCU_TIMER5_CFG | 4045 0020h |
| MCU_TIMER6_CFG | 4046 0020h |
| MCU_TIMER7_CFG | 4047 0020h |
| MCU_TIMER8_CFG | 4048 0020h |
| MCU_TIMER9_CFG | 4049 0020h |

Figure 16-3. TIMER_IRQ_EOI Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |

Figure 16-3. TIMER_IRQ_EOI Register (continued)

| | | | | | | | |
|----------|----|----|----|----|----|---|-------------|
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | LINE_NUMBER |
| R-0h | | | | | | | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-18. TIMER_IRQ_EOI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 31-1 | RESERVED | R | 0h | Reserved |
| 0 | LINE_NUMBER | R/W | 0h | Write the number of the interrupt line to apply a SW EOI to it. Note that there is only a single line (that is number 0). Read 0h = Read always returns 0. Write 0h = SW EOI on interrupt line Write 1h = No action |

16.4 TIMER_IRQSTATUS_RAW Register (Offset = 24h) [reset = 0h]

TIMER_IRQSTATUS_RAW is shown in [Figure 16-4](#) and described in [Table 16-20](#).

Return to [Summary Table](#).

Component interrupt-request status. Check the corresponding secondary status register. Raw status is set even if event is not enabled. Write 1 to set the (raw) status, mostly for debug.

Table 16-19. TIMER_IRQSTATUS_RAW Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0024h |
| TIMER1_CFG | 0241 0024h |
| TIMER2_CFG | 0242 0024h |
| TIMER3_CFG | 0243 0024h |
| TIMER4_CFG | 0244 0024h |
| TIMER5_CFG | 0245 0024h |
| TIMER6_CFG | 0246 0024h |
| TIMER7_CFG | 0247 0024h |
| TIMER8_CFG | 0248 0024h |
| TIMER9_CFG | 0249 0024h |
| TIMER10_CFG | 024A 0024h |
| TIMER11_CFG | 024B 0024h |
| TIMER12_CFG | 024C 0024h |
| TIMER13_CFG | 024D 0024h |
| TIMER14_CFG | 024E 0024h |
| TIMER15_CFG | 024F 0024h |
| TIMER16_CFG | 0250 0024h |
| TIMER17_CFG | 0251 0024h |
| TIMER18_CFG | 0252 0024h |
| TIMER19_CFG | 0253 0024h |
| MCU_TIMER0_CFG | 4040 0024h |
| MCU_TIMER1_CFG | 4041 0024h |
| MCU_TIMER2_CFG | 4042 0024h |
| MCU_TIMER3_CFG | 4043 0024h |
| MCU_TIMER4_CFG | 4044 0024h |
| MCU_TIMER5_CFG | 4045 0024h |
| MCU_TIMER6_CFG | 4046 0024h |
| MCU_TIMER7_CFG | 4047 0024h |
| MCU_TIMER8_CFG | 4048 0024h |
| MCU_TIMER9_CFG | 4049 0024h |

Figure 16-4. TIMER_IRQSTATUS_RAW Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |

Figure 16-4. TIMER_IRQSTATUS_RAW Register (continued)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|-------------|-------------|-------------|
| RESERVED | | | | | TCAR_IT_FLG | OVF_IT_FLAG | MAT_IT_FLAG |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-20. TIMER_IRQSTATUS_RAW Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved |
| 2 | TCAR_IT_FLAG | R/W | 0h | IRQ status for capture Read 0h = No event pending Write 0h = No action Read 1h = IRQ event pending Write 1h = Trigger IRQ event by software. |
| 1 | OVF_IT_FLAG | R/W | 0h | IRQ status for overflow Read 0h = No event pending Write 0h = No action Read 1h = IRQ event pending Write 1h = Trigger IRQ event by software. |
| 0 | MAT_IT_FLAG | R/W | 0h | IRQ status for match Read 0h = No event pending Write 0h = No action Read 1h = IRQ event pending Write 1h = Trigger IRQ event by software. |

16.5 TIMER_IRQSTATUS Register (Offset = 28h) [reset = 0h]

TIMER_IRQSTATUS is shown in [Figure 16-5](#) and described in [Table 16-22](#).

Return to [Summary Table](#).

Component interrupt-request status. Check the corresponding secondary status register. Enabled status is not set unless event is enabled. Write 1 to clear the status after interrupt has been serviced (raw status gets cleared, that is, even if not enabled).

Table 16-21. TIMER_IRQSTATUS Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0028h |
| TIMER1_CFG | 0241 0028h |
| TIMER2_CFG | 0242 0028h |
| TIMER3_CFG | 0243 0028h |
| TIMER4_CFG | 0244 0028h |
| TIMER5_CFG | 0245 0028h |
| TIMER6_CFG | 0246 0028h |
| TIMER7_CFG | 0247 0028h |
| TIMER8_CFG | 0248 0028h |
| TIMER9_CFG | 0249 0028h |
| TIMER10_CFG | 024A 0028h |
| TIMER11_CFG | 024B 0028h |
| TIMER12_CFG | 024C 0028h |
| TIMER13_CFG | 024D 0028h |
| TIMER14_CFG | 024E 0028h |
| TIMER15_CFG | 024F 0028h |
| TIMER16_CFG | 0250 0028h |
| TIMER17_CFG | 0251 0028h |
| TIMER18_CFG | 0252 0028h |
| TIMER19_CFG | 0253 0028h |
| MCU_TIMER0_CFG | 4040 0028h |
| MCU_TIMER1_CFG | 4041 0028h |
| MCU_TIMER2_CFG | 4042 0028h |
| MCU_TIMER3_CFG | 4043 0028h |
| MCU_TIMER4_CFG | 4044 0028h |
| MCU_TIMER5_CFG | 4045 0028h |
| MCU_TIMER6_CFG | 4046 0028h |
| MCU_TIMER7_CFG | 4047 0028h |
| MCU_TIMER8_CFG | 4048 0028h |
| MCU_TIMER9_CFG | 4049 0028h |

Figure 16-5. TIMER_IRQSTATUS Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |

Figure 16-5. TIMER_IRQSTATUS Register (continued)

| R-0h | | | | | | | |
|----------|---|---|---|---|-------------|-------------|-------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | TCAR_IT_FLG | OVF_IT_FLAG | MAT_IT_FLAG |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-22. TIMER_IRQSTATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved |
| 2 | TCAR_IT_FLAG | R/W | 0h | IRQ status for capture Read 0h = No event pending Write 0h = No action Read 1h = IRQ event pending Write 1h = Clear any pending event. |
| 1 | OVF_IT_FLAG | R/W | 0h | IRQ status for overflow Read 0h = No event pending Write 0h = No action Read 1h = IRQ event pending Write 1h = Clear any pending event. |
| 0 | MAT_IT_FLAG | R/W | 0h | IRQ status for match Read 0h = No event pending Write 0h = No action Read 1h = IRQ event pending Write 1h = Clear any pending event. |

16.6 TIMER_IRQSTATUS_SET Register (Offset = 2Ch) [reset = 0h]

TIMER_IRQSTATUS_SET is shown in [Figure 16-6](#) and described in [Table 16-24](#).

Return to [Summary Table](#).

Component interrupt-request enable. Write 1 to set (enable interrupt). Readout equal to corresponding *_CLR register.

Table 16-23. TIMER_IRQSTATUS_SET Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 002Ch |
| TIMER1_CFG | 0241 002Ch |
| TIMER2_CFG | 0242 002Ch |
| TIMER3_CFG | 0243 002Ch |
| TIMER4_CFG | 0244 002Ch |
| TIMER5_CFG | 0245 002Ch |
| TIMER6_CFG | 0246 002Ch |
| TIMER7_CFG | 0247 002Ch |
| TIMER8_CFG | 0248 002Ch |
| TIMER9_CFG | 0249 002Ch |
| TIMER10_CFG | 024A 002Ch |
| TIMER11_CFG | 024B 002Ch |
| TIMER12_CFG | 024C 002Ch |
| TIMER13_CFG | 024D 002Ch |
| TIMER14_CFG | 024E 002Ch |
| TIMER15_CFG | 024F 002Ch |
| TIMER16_CFG | 0250 002Ch |
| TIMER17_CFG | 0251 002Ch |
| TIMER18_CFG | 0252 002Ch |
| TIMER19_CFG | 0253 002Ch |
| MCU_TIMER0_CFG | 4040 002Ch |
| MCU_TIMER1_CFG | 4041 002Ch |
| MCU_TIMER2_CFG | 4042 002Ch |
| MCU_TIMER3_CFG | 4043 002Ch |
| MCU_TIMER4_CFG | 4044 002Ch |
| MCU_TIMER5_CFG | 4045 002Ch |
| MCU_TIMER6_CFG | 4046 002Ch |
| MCU_TIMER7_CFG | 4047 002Ch |
| MCU_TIMER8_CFG | 4048 002Ch |
| MCU_TIMER9_CFG | 4049 002Ch |

Figure 16-6. TIMER_IRQSTATUS_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |

Figure 16-6. TIMER_IRQSTATUS_SET Register (continued)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|--------------|-------------|-------------|
| RESERVED | | | | | TCAR_EN_FLAG | OVF_EN_FLAG | MAT_EN_FLAG |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-24. TIMER_IRQSTATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved |
| 2 | TCAR_EN_FLAG | R/W | 0h | IRQ enable for compare Read 0h = IRQ event is disabled Write 0h = No action Read 1h = IRQ event is enabled Write 1h = Set IRQ enable. |
| 1 | OVF_EN_FLAG | R/W | 0h | IRQ enable for overflow Read 0h = IRQ event is disabled Write 0h = No action Read 1h = IRQ event is enabled. Write 1h = Set IRQ enable. |
| 0 | MAT_EN_FLAG | R/W | 0h | IRQ enable for match Read 0h = IRQ event is disabled Write 0h = No action Read 1h = IRQ event is enabled. Write 1h = Set IRQ enable. |

16.7 TIMER_IRQSTATUS_CLR Register (Offset = 30h) [reset = 0h]

TIMER_IRQSTATUS_CLR is shown in [Figure 16-7](#) and described in [Table 16-26](#).

Return to [Summary Table](#).

Component interrupt-request enable. Write 1 to clear (disable interrupt). Readout equal to corresponding *_SET register.

Table 16-25. TIMER_IRQSTATUS_CLR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0030h |
| TIMER1_CFG | 0241 0030h |
| TIMER2_CFG | 0242 0030h |
| TIMER3_CFG | 0243 0030h |
| TIMER4_CFG | 0244 0030h |
| TIMER5_CFG | 0245 0030h |
| TIMER6_CFG | 0246 0030h |
| TIMER7_CFG | 0247 0030h |
| TIMER8_CFG | 0248 0030h |
| TIMER9_CFG | 0249 0030h |
| TIMER10_CFG | 024A 0030h |
| TIMER11_CFG | 024B 0030h |
| TIMER12_CFG | 024C 0030h |
| TIMER13_CFG | 024D 0030h |
| TIMER14_CFG | 024E 0030h |
| TIMER15_CFG | 024F 0030h |
| TIMER16_CFG | 0250 0030h |
| TIMER17_CFG | 0251 0030h |
| TIMER18_CFG | 0252 0030h |
| TIMER19_CFG | 0253 0030h |
| MCU_TIMER0_CFG | 4040 0030h |
| MCU_TIMER1_CFG | 4041 0030h |
| MCU_TIMER2_CFG | 4042 0030h |
| MCU_TIMER3_CFG | 4043 0030h |
| MCU_TIMER4_CFG | 4044 0030h |
| MCU_TIMER5_CFG | 4045 0030h |
| MCU_TIMER6_CFG | 4046 0030h |
| MCU_TIMER7_CFG | 4047 0030h |
| MCU_TIMER8_CFG | 4048 0030h |
| MCU_TIMER9_CFG | 4049 0030h |

Figure 16-7. TIMER_IRQSTATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |

Figure 16-7. TIMER_IRQSTATUS_CLR Register (continued)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|--------------|-------------|-------------|
| RESERVED | | | | | TCAR_EN_FLAG | OVF_EN_FLAG | MAT_EN_FLAG |
| R-0h | | | | | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-26. TIMER_IRQSTATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved |
| 2 | TCAR_EN_FLAG | R/W | 0h | IRQ enable for compare Read 0h = IRQ event is disabled Write 0h = No action Read 1h = IRQ event is enabled. Write 1h = Clear IRQ enable. |
| 1 | OVF_EN_FLAG | R/W | 0h | IRQ enable for overflow Read 0h = IRQ event is disabled Write 0h = No action Read 1h = IRQ event is enabled. Write 1h = Clear IRQ enable. |
| 0 | MAT_EN_FLAG | R/W | 0h | IRQ enable for match Read 0h = IRQ event is disabled Write 0h = No action Read 1h = IRQ event is enabled. Write 1h = Clear IRQ enable. |

16.8 TIMER_IRQWAKEEN Register (Offset = 34h) [reset = 0h]

TIMER_IRQWAKEEN is shown in [Figure 16-8](#) and described in [Table 16-28](#).

Return to [Summary Table](#).

Wake-up-enabled events taking place when module is idle should generate an asynchronous wake-up.

Table 16-27. TIMER_IRQWAKEEN Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0034h |
| TIMER1_CFG | 0241 0034h |
| TIMER2_CFG | 0242 0034h |
| TIMER3_CFG | 0243 0034h |
| TIMER4_CFG | 0244 0034h |
| TIMER5_CFG | 0245 0034h |
| TIMER6_CFG | 0246 0034h |
| TIMER7_CFG | 0247 0034h |
| TIMER8_CFG | 0248 0034h |
| TIMER9_CFG | 0249 0034h |
| TIMER10_CFG | 024A 0034h |
| TIMER11_CFG | 024B 0034h |
| TIMER12_CFG | 024C 0034h |
| TIMER13_CFG | 024D 0034h |
| TIMER14_CFG | 024E 0034h |
| TIMER15_CFG | 024F 0034h |
| TIMER16_CFG | 0250 0034h |
| TIMER17_CFG | 0251 0034h |
| TIMER18_CFG | 0252 0034h |
| TIMER19_CFG | 0253 0034h |
| MCU_TIMER0_CFG | 4040 0034h |
| MCU_TIMER1_CFG | 4041 0034h |
| MCU_TIMER2_CFG | 4042 0034h |
| MCU_TIMER3_CFG | 4043 0034h |
| MCU_TIMER4_CFG | 4044 0034h |
| MCU_TIMER5_CFG | 4045 0034h |
| MCU_TIMER6_CFG | 4046 0034h |
| MCU_TIMER7_CFG | 4047 0034h |
| MCU_TIMER8_CFG | 4048 0034h |
| MCU_TIMER9_CFG | 4049 0034h |

Figure 16-8. TIMER_IRQWAKEEN Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Figure 16-8. TIMER_IRQWAKEEN Register (continued)

| | | | |
|----------|-------------------|-----------------|-----------------|
| RESERVED | TCAR_WUP_EN NA | OVF_WUP_EN A | MAT_WUP_EN A |
| R-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-28. TIMER_IRQWAKEEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------|------|-------|---|
| 31-3 | RESERVED | R | 0h | Reserved |
| 2 | TCAR_WUP_ENA | R/W | 0h | Wake-up generation for compare 0h = Wake-up disabled 1h = Wake-up enabled. |
| 1 | OVF_WUP_ENA | R/W | 0h | Wake-up generation for overflow 0h = Wake-up disabled 1h = Wake-up enabled. |
| 0 | MAT_WUP_ENA | R/W | 0h | Wake-up generation for match 0h = Wake-up disabled 1h = Wake-up enabled. |

16.9 TIMER_TCLR Register (Offset = 38h) [reset = 0h]

TIMER_TCLR is shown in [Figure 16-9](#) and described in [Table 16-30](#).

Return to [Summary Table](#).

This register controls optional features specific to the timer functionality.

Table 16-29. TIMER_TCLR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0038h |
| TIMER1_CFG | 0241 0038h |
| TIMER2_CFG | 0242 0038h |
| TIMER3_CFG | 0243 0038h |
| TIMER4_CFG | 0244 0038h |
| TIMER5_CFG | 0245 0038h |
| TIMER6_CFG | 0246 0038h |
| TIMER7_CFG | 0247 0038h |
| TIMER8_CFG | 0248 0038h |
| TIMER9_CFG | 0249 0038h |
| TIMER10_CFG | 024A 0038h |
| TIMER11_CFG | 024B 0038h |
| TIMER12_CFG | 024C 0038h |
| TIMER13_CFG | 024D 0038h |
| TIMER14_CFG | 024E 0038h |
| TIMER15_CFG | 024F 0038h |
| TIMER16_CFG | 0250 0038h |
| TIMER17_CFG | 0251 0038h |
| TIMER18_CFG | 0252 0038h |
| TIMER19_CFG | 0253 0038h |
| MCU_TIMER0_CFG | 4040 0038h |
| MCU_TIMER1_CFG | 4041 0038h |
| MCU_TIMER2_CFG | 4042 0038h |
| MCU_TIMER3_CFG | 4043 0038h |
| MCU_TIMER4_CFG | 4044 0038h |
| MCU_TIMER5_CFG | 4045 0038h |
| MCU_TIMER6_CFG | 4046 0038h |
| MCU_TIMER7_CFG | 4047 0038h |
| MCU_TIMER8_CFG | 4048 0038h |
| MCU_TIMER9_CFG | 4049 0038h |

Figure 16-9. TIMER_TCLR Register

| | | | | | | | |
|----------|---------|-----------|--------|--------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | GPO_CFG | CAPT_MODE | PT | TRG | | TCM | |
| R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Figure 16-9. TIMER_TCLR Register (continued)

| | | | | | |
|--------|--------|--------|--------|--------|--------|
| SCPWM | CE | PRE | PTV | AR | ST |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-30. TIMER_TCLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| 31-15 | RESERVED | R | 0h | Reserved |
| 14 | GPO_CFG | R/W | 0h | General-purpose output - this bit is used to as an output enable for the TIMER IO pin. 0h = TIMER IO pin functions as PWM output. 1h = TIMER IO pin functions as TRIGGER input. |
| 13 | CAPT_MODE | R/W | 0h | Capture mode select bit (first/second) 0h = Single capture: Capture the first enabled capture event in TIMER_TCAR1. 1h = Capture on second event: Capture the second enabled capture event in TIMER_TCAR1 and the second enabled capture event in TIMER_TCAR2. |
| 12 | PT | R/W | 0h | Pulse or toggle mode on POTIMERPWM output pin 0h = Pulse modulation 1h = Toggle modulation. |
| 11-10 | TRG | R/W | 0h | Trigger output mode on POTIMERPWM output pin 0h = No trigger 1h = Trigger on overflow. 2h = Trigger on overflow and match 3h = Reserved. |
| 9-8 | TCM | R/W | 0h | Transition capture mode on EVENT_CAPTURE input pin (When the TCM field passed from (00) to any other combination, the TCAR_IT_FLAG and the edge detection logic are cleared.) 0h = No capture 1h = Capture on rising edges of EVENT_CAPTURE pin 2h = Capture on falling edges of EVENT_CAPTURE pin 3h = Capture on both edges of EVENT_CAPTURE pin. |
| 7 | SCPWM | R/W | 0h | Pulse width modulation output pin default setting This bit must be set or clear while the timer is stopped or the trigger is off. 0h = Clear the POTIMERPWM output pin and select positive pulse for pulse mode. 1h = Set the POTIMERPWM output pin and select negative pulse for pulse mode. |
| 6 | CE | R/W | 0h | Compare enable 0h = Compare mode is disable. 1h = Compare mode is enable. |
| 5 | PRE | R/W | 0h | Prescaler enable 0h = The timer clock input pin clocks the counter. 1h = The divided input pin clocks the counter. |
| 4-2 | PTV | R/W | 0h | Prescale clock timer value The timer counter is prescaled with the value $2^{(PTV+1)}$. Example: PTV = 3, counter increases value (if started) after 16 functional clock periods. |

Table 16-30. TIMER_TCLR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 1 | AR | R/W | 0h | Autoreload mode 0h = One shot timer 1h = Autoreload timer |
| 0 | ST | R/W | 0h | Start/stop timer control 0h = Stop timer: Only the counter is frozen. If one-shot mode selected (AR = 0), this bit is automatically reset by internal logic when the counter is overflowed. 1h = Start timer. |

16.10 TIMER_TCR Register (Offset = 3Ch) [reset = 0h]

TIMER_TCR is shown in [Figure 16-10](#) and described in [Table 16-32](#).

Return to [Summary Table](#).

This register holds the value of the internal counter.

Table 16-31. TIMER_TCR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 003Ch |
| TIMER1_CFG | 0241 003Ch |
| TIMER2_CFG | 0242 003Ch |
| TIMER3_CFG | 0243 003Ch |
| TIMER4_CFG | 0244 003Ch |
| TIMER5_CFG | 0245 003Ch |
| TIMER6_CFG | 0246 003Ch |
| TIMER7_CFG | 0247 003Ch |
| TIMER8_CFG | 0248 003Ch |
| TIMER9_CFG | 0249 003Ch |
| TIMER10_CFG | 024A 003Ch |
| TIMER11_CFG | 024B 003Ch |
| TIMER12_CFG | 024C 003Ch |
| TIMER13_CFG | 024D 003Ch |
| TIMER14_CFG | 024E 003Ch |
| TIMER15_CFG | 024F 003Ch |
| TIMER16_CFG | 0250 003Ch |
| TIMER17_CFG | 0251 003Ch |
| TIMER18_CFG | 0252 003Ch |
| TIMER19_CFG | 0253 003Ch |
| MCU_TIMER0_CFG | 4040 003Ch |
| MCU_TIMER1_CFG | 4041 003Ch |
| MCU_TIMER2_CFG | 4042 003Ch |
| MCU_TIMER3_CFG | 4043 003Ch |
| MCU_TIMER4_CFG | 4044 003Ch |
| MCU_TIMER5_CFG | 4045 003Ch |
| MCU_TIMER6_CFG | 4046 003Ch |
| MCU_TIMER7_CFG | 4047 003Ch |
| MCU_TIMER8_CFG | 4048 003Ch |
| MCU_TIMER9_CFG | 4049 003Ch |

Figure 16-10. TIMER_TCR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TIMER_COUNTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-32. TIMER_TCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|------------------------|
| 31-0 | TIMER_COUNTER | R/W | 0h | Value of timer counter |

16.11 TIMER_TLDR Register (Offset = 40h) [reset = 0h]

TIMER_TLDR is shown in [Figure 16-11](#) and described in [Table 16-34](#).

[Return to Summary Table.](#)

This register holds the timer load value.

Table 16-33. TIMER_TLDR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0040h |
| TIMER1_CFG | 0241 0040h |
| TIMER2_CFG | 0242 0040h |
| TIMER3_CFG | 0243 0040h |
| TIMER4_CFG | 0244 0040h |
| TIMER5_CFG | 0245 0040h |
| TIMER6_CFG | 0246 0040h |
| TIMER7_CFG | 0247 0040h |
| TIMER8_CFG | 0248 0040h |
| TIMER9_CFG | 0249 0040h |
| TIMER10_CFG | 024A 0040h |
| TIMER11_CFG | 024B 0040h |
| TIMER12_CFG | 024C 0040h |
| TIMER13_CFG | 024D 0040h |
| TIMER14_CFG | 024E 0040h |
| TIMER15_CFG | 024F 0040h |
| TIMER16_CFG | 0250 0040h |
| TIMER17_CFG | 0251 0040h |
| TIMER18_CFG | 0252 0040h |
| TIMER19_CFG | 0253 0040h |
| MCU_TIMER0_CFG | 4040 0040h |
| MCU_TIMER1_CFG | 4041 0040h |
| MCU_TIMER2_CFG | 4042 0040h |
| MCU_TIMER3_CFG | 4043 0040h |
| MCU_TIMER4_CFG | 4044 0040h |
| MCU_TIMER5_CFG | 4045 0040h |
| MCU_TIMER6_CFG | 4046 0040h |
| MCU_TIMER7_CFG | 4047 0040h |
| MCU_TIMER8_CFG | 4048 0040h |
| MCU_TIMER9_CFG | 4049 0040h |

Figure 16-11. TIMER_TLDR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LOAD_VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-34. TIMER_TLDR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | LOAD_VALUE | R/W | 0h | Timer counter value loaded on overflow in autoreload mode or on TIMER_TTGR write access. LOAD_VALUE must be different than the timer overflow value (FFFF FFFFh). |

16.12 TIMER_TTGR Register (Offset = 44h) [reset = Fh]

TIMER_TTGR is shown in [Figure 16-12](#) and described in [Table 16-36](#).

Return to [Summary Table](#).

This register triggers a counter reload of timer by writing any value in it. The read value of this register is always FFFF FFFFh.

Table 16-35. TIMER_TTGR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0044h |
| TIMER1_CFG | 0241 0044h |
| TIMER2_CFG | 0242 0044h |
| TIMER3_CFG | 0243 0044h |
| TIMER4_CFG | 0244 0044h |
| TIMER5_CFG | 0245 0044h |
| TIMER6_CFG | 0246 0044h |
| TIMER7_CFG | 0247 0044h |
| TIMER8_CFG | 0248 0044h |
| TIMER9_CFG | 0249 0044h |
| TIMER10_CFG | 024A 0044h |
| TIMER11_CFG | 024B 0044h |
| TIMER12_CFG | 024C 0044h |
| TIMER13_CFG | 024D 0044h |
| TIMER14_CFG | 024E 0044h |
| TIMER15_CFG | 024F 0044h |
| TIMER16_CFG | 0250 0044h |
| TIMER17_CFG | 0251 0044h |
| TIMER18_CFG | 0252 0044h |
| TIMER19_CFG | 0253 0044h |
| MCU_TIMER0_CFG | 4040 0044h |
| MCU_TIMER1_CFG | 4041 0044h |
| MCU_TIMER2_CFG | 4042 0044h |
| MCU_TIMER3_CFG | 4043 0044h |
| MCU_TIMER4_CFG | 4044 0044h |
| MCU_TIMER5_CFG | 4045 0044h |
| MCU_TIMER6_CFG | 4046 0044h |
| MCU_TIMER7_CFG | 4047 0044h |
| MCU_TIMER8_CFG | 4048 0044h |
| MCU_TIMER9_CFG | 4049 0044h |

Figure 16-12. TIMER_TTGR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TTGR_VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-Fh | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-36. TIMER_TTGR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 31-0 | TTGR_VALUE | R/W | Fh | Writing to the TIMER_TTGR register causes the TIMER_TCRR to be loaded from TIMER_TLDR and the prescaler counter to be cleared. Reload is done regardless of the AR field value of the TIMER_TCLR register. |

16.13 TIMER_TWPS Register (Offset = 48h) [reset = 0h]

TIMER_TWPS is shown in [Figure 16-13](#) and described in [Table 16-38](#).

Return to [Summary Table](#).

This register contains the write posting bits for all writable functional registers.

Table 16-37. TIMER_TWPS Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0048h |
| TIMER1_CFG | 0241 0048h |
| TIMER2_CFG | 0242 0048h |
| TIMER3_CFG | 0243 0048h |
| TIMER4_CFG | 0244 0048h |
| TIMER5_CFG | 0245 0048h |
| TIMER6_CFG | 0246 0048h |
| TIMER7_CFG | 0247 0048h |
| TIMER8_CFG | 0248 0048h |
| TIMER9_CFG | 0249 0048h |
| TIMER10_CFG | 024A 0048h |
| TIMER11_CFG | 024B 0048h |
| TIMER12_CFG | 024C 0048h |
| TIMER13_CFG | 024D 0048h |
| TIMER14_CFG | 024E 0048h |
| TIMER15_CFG | 024F 0048h |
| TIMER16_CFG | 0250 0048h |
| TIMER17_CFG | 0251 0048h |
| TIMER18_CFG | 0252 0048h |
| TIMER19_CFG | 0253 0048h |
| MCU_TIMER0_CFG | 4040 0048h |
| MCU_TIMER1_CFG | 4041 0048h |
| MCU_TIMER2_CFG | 4042 0048h |
| MCU_TIMER3_CFG | 4043 0048h |
| MCU_TIMER4_CFG | 4044 0048h |
| MCU_TIMER5_CFG | 4045 0048h |
| MCU_TIMER6_CFG | 4046 0048h |
| MCU_TIMER7_CFG | 4047 0048h |
| MCU_TIMER8_CFG | 4048 0048h |
| MCU_TIMER9_CFG | 4049 0048h |

Figure 16-13. TIMER_TWPS Register

| | | | | | | | |
|----------|----|----|----|----|----|-----------------|-----------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | W_PEND_TOW R | W_PEND_TOC R |
| R-0h | | | | | | R-0h | R-0h |

Figure 16-13. TIMER_TWPS Register (continued)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|-------------|-------------|------------------|------------------|------------------|------------------|------------------|
| W_PEND_TCV R | W_PEND_TNIR | W_PEND_TPIR | W_PEND_TMAR R | W_PEND_TTGR R | W_PEND_TLDR R | W_PEND_TCRR R | W_PEND_TCLR R |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 16-38. TIMER_TWPS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-10 | RESERVED | R | 0h | Reserved |
| 9 | W_PEND_TOWR | R | 0h | Write pending for the TIMER_TOWR register Read 0h = No write pending Read 1h = Write pending. |
| 8 | W_PEND_TOCR | R | 0h | Write pending for the TIMER_TOCR register Read 0h = No write pending Read 1h = Write pending. |
| 7 | W_PEND_TCVR | R | 0h | Write pending for the TIMER_TCVR register Read 0h = No write pending Read 1h = Write pending. |
| 6 | W_PEND_TNIR | R | 0h | Write pending for the TIMER_TNIR register Read 0h = No negative increment register write pending Read 1h = Negative increment register write pending. |
| 5 | W_PEND_TPIR | R | 0h | Write pending for the TIMER_TPIR register Read 0h = No positive increment register write pending Read 1h = Positive increment register write pending. |
| 4 | W_PEND_TMAR | R | 0h | Write pending for the TIMER_TMAR register Read 0h = No write pending Read 1h = Write pending. |
| 3 | W_PEND_TTGR | R | 0h | Write pending for the TIMER_TTGR register Read 0h = No write pending Read 1h = Write pending. |
| 2 | W_PEND_TLDR | R | 0h | Write pending for the TIMER_TLDR register Read 0h = No write pending Read 1h = Write pending. |
| 1 | W_PEND_TCRR | R | 0h | Write pending for the TIMER_TCRR register Read 0h = No write pending Read 1h = Write pending. |
| 0 | W_PEND_TCLR | R | 0h | Write pending for the TIMER_TCLR register Read 0h = No write pending Read 1h = Write pending. |

16.14 TIMER_TMAR Register (Offset = 4Ch) [reset = 0h]

TIMER_TMAR is shown in [Figure 16-14](#) and described in [Table 16-40](#).

Return to [Summary Table](#).

The TIMER_TMAR register holds the match value to be compared with the counter's value.

Table 16-39. TIMER_TMAR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 004Ch |
| TIMER1_CFG | 0241 004Ch |
| TIMER2_CFG | 0242 004Ch |
| TIMER3_CFG | 0243 004Ch |
| TIMER4_CFG | 0244 004Ch |
| TIMER5_CFG | 0245 004Ch |
| TIMER6_CFG | 0246 004Ch |
| TIMER7_CFG | 0247 004Ch |
| TIMER8_CFG | 0248 004Ch |
| TIMER9_CFG | 0249 004Ch |
| TIMER10_CFG | 024A 004Ch |
| TIMER11_CFG | 024B 004Ch |
| TIMER12_CFG | 024C 004Ch |
| TIMER13_CFG | 024D 004Ch |
| TIMER14_CFG | 024E 004Ch |
| TIMER15_CFG | 024F 004Ch |
| TIMER16_CFG | 0250 004Ch |
| TIMER17_CFG | 0251 004Ch |
| TIMER18_CFG | 0252 004Ch |
| TIMER19_CFG | 0253 004Ch |
| MCU_TIMER0_CFG | 4040 004Ch |
| MCU_TIMER1_CFG | 4041 004Ch |
| MCU_TIMER2_CFG | 4042 004Ch |
| MCU_TIMER3_CFG | 4043 004Ch |
| MCU_TIMER4_CFG | 4044 004Ch |
| MCU_TIMER5_CFG | 4045 004Ch |
| MCU_TIMER6_CFG | 4046 004Ch |
| MCU_TIMER7_CFG | 4047 004Ch |
| MCU_TIMER8_CFG | 4048 004Ch |
| MCU_TIMER9_CFG | 4049 004Ch |

Figure 16-14. TIMER_TMAR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMPARE_VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-40. TIMER_TMAR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-0 | COMPARE_VALUE | R/W | 0h | Value to be compared to the timer counter |

16.15 TIMER_TCAR1 Register (Offset = 50h) [reset = 0h]

TIMER_TCAR1 is shown in [Figure 16-15](#) and described in [Table 16-42](#).

Return to [Summary Table](#).

This register holds the first captured value of the counter register.

Table 16-41. TIMER_TCAR1 Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0050h |
| TIMER1_CFG | 0241 0050h |
| TIMER2_CFG | 0242 0050h |
| TIMER3_CFG | 0243 0050h |
| TIMER4_CFG | 0244 0050h |
| TIMER5_CFG | 0245 0050h |
| TIMER6_CFG | 0246 0050h |
| TIMER7_CFG | 0247 0050h |
| TIMER8_CFG | 0248 0050h |
| TIMER9_CFG | 0249 0050h |
| TIMER10_CFG | 024A 0050h |
| TIMER11_CFG | 024B 0050h |
| TIMER12_CFG | 024C 0050h |
| TIMER13_CFG | 024D 0050h |
| TIMER14_CFG | 024E 0050h |
| TIMER15_CFG | 024F 0050h |
| TIMER16_CFG | 0250 0050h |
| TIMER17_CFG | 0251 0050h |
| TIMER18_CFG | 0252 0050h |
| TIMER19_CFG | 0253 0050h |
| MCU_TIMER0_CFG | 4040 0050h |
| MCU_TIMER1_CFG | 4041 0050h |
| MCU_TIMER2_CFG | 4042 0050h |
| MCU_TIMER3_CFG | 4043 0050h |
| MCU_TIMER4_CFG | 4044 0050h |
| MCU_TIMER5_CFG | 4045 0050h |
| MCU_TIMER6_CFG | 4046 0050h |
| MCU_TIMER7_CFG | 4047 0050h |
| MCU_TIMER8_CFG | 4048 0050h |
| MCU_TIMER9_CFG | 4049 0050h |

Figure 16-15. TIMER_TCAR1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAPTURE_VALUE1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 16-42. TIMER_TCAR1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|---|
| 31-0 | CAPTURE_VALUE1 | R | 0h | First timer counter value captured on an external event trigger |

16.16 TIMER_TSICR Register (Offset = 54h) [reset = 4h]

TIMER_TSICR is shown in [Figure 16-16](#) and described in [Table 16-44](#).

Return to [Summary Table](#).

Timer synchronous interface control register

Table 16-43. TIMER_TSICR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0054h |
| TIMER1_CFG | 0241 0054h |
| TIMER2_CFG | 0242 0054h |
| TIMER3_CFG | 0243 0054h |
| TIMER4_CFG | 0244 0054h |
| TIMER5_CFG | 0245 0054h |
| TIMER6_CFG | 0246 0054h |
| TIMER7_CFG | 0247 0054h |
| TIMER8_CFG | 0248 0054h |
| TIMER9_CFG | 0249 0054h |
| TIMER10_CFG | 024A 0054h |
| TIMER11_CFG | 024B 0054h |
| TIMER12_CFG | 024C 0054h |
| TIMER13_CFG | 024D 0054h |
| TIMER14_CFG | 024E 0054h |
| TIMER15_CFG | 024F 0054h |
| TIMER16_CFG | 0250 0054h |
| TIMER17_CFG | 0251 0054h |
| TIMER18_CFG | 0252 0054h |
| TIMER19_CFG | 0253 0054h |
| MCU_TIMER0_CFG | 4040 0054h |
| MCU_TIMER1_CFG | 4041 0054h |
| MCU_TIMER2_CFG | 4042 0054h |
| MCU_TIMER3_CFG | 4043 0054h |
| MCU_TIMER4_CFG | 4044 0054h |
| MCU_TIMER5_CFG | 4045 0054h |
| MCU_TIMER6_CFG | 4046 0054h |
| MCU_TIMER7_CFG | 4047 0054h |
| MCU_TIMER8_CFG | 4048 0054h |
| MCU_TIMER9_CFG | 4049 0054h |

Figure 16-16. TIMER_TSICR Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Figure 16-16. TIMER_TSICR Register (continued)

| RESERVED | READ_AFTER_IDLE | READ_MODE | POSTED | SFT | RESERVED |
|----------|-----------------|-----------|--------|--------|----------|
| R-0h | W-0h | W-0h | R/W-1h | R/W-0h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; W = Write Only; -n = value after reset

Table 16-44. TIMER_TSICR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|--|
| 31-5 | RESERVED | R | 0h | Reserved |
| 4 | READ_AFTER_IDLE | W | 0h | Select if the synchronization mechanism used for first TIMER_TCRR read operation after idle state is active. Field values: 0h = The synchronization mechanism is enabled. 1h = The synchronization mechanism is disabled. |
| 3 | READ_MODE | W | 0h | Select posted/non-posted mode for read operation: NOTE: When the module is configured in posted mode (POSTED = '1'), this bit is not used. 0h = When the module is configured in non-posted mode (POSTED = '0'), the read operation is executed as read posted. 1h = When the module is configured in non-posted mode (POSTED = '0'), the read operation is executed as read non-posted. |
| 2 | POSTED | R/W | 1h | Posted mode selection. 0h = Posted mode inactive: Delay the command accept output signal. 1h = Posted mode active. |
| 1 | SFT | R/W | 0h | This bit resets the TIMER_TSICR[2] POSTED bit to the default value determined by the hardware configuration set at design integration time. 0h = Reset is inactive. 1h = Reset is asserted. |
| 0 | RESERVED | R | 0h | Reserved |

16.17 TIMER_TCAR2 Register (Offset = 58h) [reset = 0h]

TIMER_TCAR2 is shown in [Figure 16-17](#) and described in [Table 16-46](#).

[Return to Summary Table.](#)

This register holds the second captured value of the counter register.

Table 16-45. TIMER_TCAR2 Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0058h |
| TIMER1_CFG | 0241 0058h |
| TIMER2_CFG | 0242 0058h |
| TIMER3_CFG | 0243 0058h |
| TIMER4_CFG | 0244 0058h |
| TIMER5_CFG | 0245 0058h |
| TIMER6_CFG | 0246 0058h |
| TIMER7_CFG | 0247 0058h |
| TIMER8_CFG | 0248 0058h |
| TIMER9_CFG | 0249 0058h |
| TIMER10_CFG | 024A 0058h |
| TIMER11_CFG | 024B 0058h |
| TIMER12_CFG | 024C 0058h |
| TIMER13_CFG | 024D 0058h |
| TIMER14_CFG | 024E 0058h |
| TIMER15_CFG | 024F 0058h |
| TIMER16_CFG | 0250 0058h |
| TIMER17_CFG | 0251 0058h |
| TIMER18_CFG | 0252 0058h |
| TIMER19_CFG | 0253 0058h |
| MCU_TIMER0_CFG | 4040 0058h |
| MCU_TIMER1_CFG | 4041 0058h |
| MCU_TIMER2_CFG | 4042 0058h |
| MCU_TIMER3_CFG | 4043 0058h |
| MCU_TIMER4_CFG | 4044 0058h |
| MCU_TIMER5_CFG | 4045 0058h |
| MCU_TIMER6_CFG | 4046 0058h |
| MCU_TIMER7_CFG | 4047 0058h |
| MCU_TIMER8_CFG | 4048 0058h |
| MCU_TIMER9_CFG | 4049 0058h |

Figure 16-17. TIMER_TCAR2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CAPTURE_VALUE2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 16-46. TIMER_TCAR2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------------|------|-------|--|
| 31-0 | CAPTURE_VALUE2 | R | 0h | Second timer counter value captured on an external event trigger |

16.18 TIMER_TPIR Register (Offset = 5Ch) [reset = 0h]

TIMER_TPIR is shown in [Figure 16-18](#) and described in [Table 16-48](#).

Return to [Summary Table](#).

This register is used for 1-ms tick generation. The TIMER_TPIR register holds the value of the positive increment. The value of this register is added to the value of TIMER_TCVR to determine whether next value loaded in TIMER_TCRR is the subperiod value or the overperiod value.

Table 16-47. TIMER_TPIR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 005Ch |
| TIMER1_CFG | 0241 005Ch |
| TIMER2_CFG | 0242 005Ch |
| TIMER3_CFG | 0243 005Ch |
| TIMER4_CFG | 0244 005Ch |
| TIMER5_CFG | 0245 005Ch |
| TIMER6_CFG | 0246 005Ch |
| TIMER7_CFG | 0247 005Ch |
| TIMER8_CFG | 0248 005Ch |
| TIMER9_CFG | 0249 005Ch |
| TIMER10_CFG | 024A 005Ch |
| TIMER11_CFG | 024B 005Ch |
| TIMER12_CFG | 024C 005Ch |
| TIMER13_CFG | 024D 005Ch |
| TIMER14_CFG | 024E 005Ch |
| TIMER15_CFG | 024F 005Ch |
| TIMER16_CFG | 0250 005Ch |
| TIMER17_CFG | 0251 005Ch |
| TIMER18_CFG | 0252 005Ch |
| TIMER19_CFG | 0253 005Ch |
| MCU_TIMER0_CFG | 4040 005Ch |
| MCU_TIMER1_CFG | 4041 005Ch |
| MCU_TIMER2_CFG | 4042 005Ch |
| MCU_TIMER3_CFG | 4043 005Ch |
| MCU_TIMER4_CFG | 4044 005Ch |
| MCU_TIMER5_CFG | 4045 005Ch |
| MCU_TIMER6_CFG | 4046 005Ch |
| MCU_TIMER7_CFG | 4047 005Ch |
| MCU_TIMER8_CFG | 4048 005Ch |
| MCU_TIMER9_CFG | 4049 005Ch |

Figure 16-18. TIMER_TPIR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POSITIVE_INC_VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-48. TIMER_TPIR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---------------------------------|
| 31-0 | POSITIVE_INC_VALUE | R/W | 0h | Value of the positive increment |

16.19 TIMER_TNIR Register (Offset = 60h) [reset = 0h]

TIMER_TNIR is shown in [Figure 16-19](#) and described in [Table 16-50](#).

Return to [Summary Table](#).

This register is used for 1-ms tick generation. The TIMER_TNIR register holds the value of the negative increment. The value of this register is added to the value of the TIMER_TCVR to determine whether next value loaded in TIMER_TCRR is the subperiod value or the overperiod value.

Table 16-49. TIMER_TNIR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0060h |
| TIMER1_CFG | 0241 0060h |
| TIMER2_CFG | 0242 0060h |
| TIMER3_CFG | 0243 0060h |
| TIMER4_CFG | 0244 0060h |
| TIMER5_CFG | 0245 0060h |
| TIMER6_CFG | 0246 0060h |
| TIMER7_CFG | 0247 0060h |
| TIMER8_CFG | 0248 0060h |
| TIMER9_CFG | 0249 0060h |
| TIMER10_CFG | 024A 0060h |
| TIMER11_CFG | 024B 0060h |
| TIMER12_CFG | 024C 0060h |
| TIMER13_CFG | 024D 0060h |
| TIMER14_CFG | 024E 0060h |
| TIMER15_CFG | 024F 0060h |
| TIMER16_CFG | 0250 0060h |
| TIMER17_CFG | 0251 0060h |
| TIMER18_CFG | 0252 0060h |
| TIMER19_CFG | 0253 0060h |
| MCU_TIMER0_CFG | 4040 0060h |
| MCU_TIMER1_CFG | 4041 0060h |
| MCU_TIMER2_CFG | 4042 0060h |
| MCU_TIMER3_CFG | 4043 0060h |
| MCU_TIMER4_CFG | 4044 0060h |
| MCU_TIMER5_CFG | 4045 0060h |
| MCU_TIMER6_CFG | 4046 0060h |
| MCU_TIMER7_CFG | 4047 0060h |
| MCU_TIMER8_CFG | 4048 0060h |
| MCU_TIMER9_CFG | 4049 0060h |

Figure 16-19. TIMER_TNIR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NEGATIVE_INV_VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-50. TIMER_TNIR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|--------------------|------|-------|---------------------------------|
| 31-0 | NEGATIVE_INV_VALUE | R/W | 0h | Value of the negative increment |

16.20 TIMER_TCVR Register (Offset = 64h) [reset = 0h]

TIMER_TCVR is shown in [Figure 16-20](#) and described in [Table 16-52](#).

Return to [Summary Table](#).

This register is used for 1-ms tick generation. The TIMER_TCVR register determines whether next value loaded in TIMER_TCRR is the subperiod value or the overperiod value.

Table 16-51. TIMER_TCVR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0064h |
| TIMER1_CFG | 0241 0064h |
| TIMER2_CFG | 0242 0064h |
| TIMER3_CFG | 0243 0064h |
| TIMER4_CFG | 0244 0064h |
| TIMER5_CFG | 0245 0064h |
| TIMER6_CFG | 0246 0064h |
| TIMER7_CFG | 0247 0064h |
| TIMER8_CFG | 0248 0064h |
| TIMER9_CFG | 0249 0064h |
| TIMER10_CFG | 024A 0064h |
| TIMER11_CFG | 024B 0064h |
| TIMER12_CFG | 024C 0064h |
| TIMER13_CFG | 024D 0064h |
| TIMER14_CFG | 024E 0064h |
| TIMER15_CFG | 024F 0064h |
| TIMER16_CFG | 0250 0064h |
| TIMER17_CFG | 0251 0064h |
| TIMER18_CFG | 0252 0064h |
| TIMER19_CFG | 0253 0064h |
| MCU_TIMER0_CFG | 4040 0064h |
| MCU_TIMER1_CFG | 4041 0064h |
| MCU_TIMER2_CFG | 4042 0064h |
| MCU_TIMER3_CFG | 4043 0064h |
| MCU_TIMER4_CFG | 4044 0064h |
| MCU_TIMER5_CFG | 4045 0064h |
| MCU_TIMER6_CFG | 4046 0064h |
| MCU_TIMER7_CFG | 4047 0064h |
| MCU_TIMER8_CFG | 4048 0064h |
| MCU_TIMER9_CFG | 4049 0064h |

Figure 16-20. TIMER_TCVR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COUNTER_VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 16-52. TIMER_TCVR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|----------------------|
| 31-0 | COUNTER_VALUE | R/W | 0h | Value of CVR counter |

16.21 TIMER_TOCR Register (Offset = 68h) [reset = 0h]

TIMER_TOCR is shown in [Figure 16-21](#) and described in [Table 16-54](#).

[Return to Summary Table.](#)

This register is used to mask the tick interrupt for a selected number of ticks.

Table 16-53. TIMER_TOCR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 0068h |
| TIMER1_CFG | 0241 0068h |
| TIMER2_CFG | 0242 0068h |
| TIMER3_CFG | 0243 0068h |
| TIMER4_CFG | 0244 0068h |
| TIMER5_CFG | 0245 0068h |
| TIMER6_CFG | 0246 0068h |
| TIMER7_CFG | 0247 0068h |
| TIMER8_CFG | 0248 0068h |
| TIMER9_CFG | 0249 0068h |
| TIMER10_CFG | 024A 0068h |
| TIMER11_CFG | 024B 0068h |
| TIMER12_CFG | 024C 0068h |
| TIMER13_CFG | 024D 0068h |
| TIMER14_CFG | 024E 0068h |
| TIMER15_CFG | 024F 0068h |
| TIMER16_CFG | 0250 0068h |
| TIMER17_CFG | 0251 0068h |
| TIMER18_CFG | 0252 0068h |
| TIMER19_CFG | 0253 0068h |
| MCU_TIMER0_CFG | 4040 0068h |
| MCU_TIMER1_CFG | 4041 0068h |
| MCU_TIMER2_CFG | 4042 0068h |
| MCU_TIMER3_CFG | 4043 0068h |
| MCU_TIMER4_CFG | 4044 0068h |
| MCU_TIMER5_CFG | 4045 0068h |
| MCU_TIMER6_CFG | 4046 0068h |
| MCU_TIMER7_CFG | 4047 0068h |
| MCU_TIMER8_CFG | 4048 0068h |
| MCU_TIMER9_CFG | 4049 0068h |

Figure 16-21. TIMER_TOCR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | OVF_COUNTER_VALUE | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-54. TIMER_TOCR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|------|-------|---------------------------|
| 31-24 | RESERVED | R | 0h | Reads return 0. |
| 23-0 | OVF_COUNTER_VALUE | R/W | 0h | Number of overflow events |

16.22 TIMER_TOWR Register (Offset = 6Ch) [reset = 0h]

TIMER_TOWR is shown in [Figure 16-22](#) and described in [Table 16-56](#).

Return to [Summary Table](#).

This register holds the number of masked overflow interrupts.

Table 16-55. TIMER_TOWR Instances

| Instance | Physical Address |
|----------------|------------------|
| TIMER0_CFG | 0240 006Ch |
| TIMER1_CFG | 0241 006Ch |
| TIMER2_CFG | 0242 006Ch |
| TIMER3_CFG | 0243 006Ch |
| TIMER4_CFG | 0244 006Ch |
| TIMER5_CFG | 0245 006Ch |
| TIMER6_CFG | 0246 006Ch |
| TIMER7_CFG | 0247 006Ch |
| TIMER8_CFG | 0248 006Ch |
| TIMER9_CFG | 0249 006Ch |
| TIMER10_CFG | 024A 006Ch |
| TIMER11_CFG | 024B 006Ch |
| TIMER12_CFG | 024C 006Ch |
| TIMER13_CFG | 024D 006Ch |
| TIMER14_CFG | 024E 006Ch |
| TIMER15_CFG | 024F 006Ch |
| TIMER16_CFG | 0250 006Ch |
| TIMER17_CFG | 0251 006Ch |
| TIMER18_CFG | 0252 006Ch |
| TIMER19_CFG | 0253 006Ch |
| MCU_TIMER0_CFG | 4040 006Ch |
| MCU_TIMER1_CFG | 4041 006Ch |
| MCU_TIMER2_CFG | 4042 006Ch |
| MCU_TIMER3_CFG | 4043 006Ch |
| MCU_TIMER4_CFG | 4044 006Ch |
| MCU_TIMER5_CFG | 4045 006Ch |
| MCU_TIMER6_CFG | 4046 006Ch |
| MCU_TIMER7_CFG | 4047 006Ch |
| MCU_TIMER8_CFG | 4048 006Ch |
| MCU_TIMER9_CFG | 4049 006Ch |

Figure 16-22. TIMER_TOWR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | OVF_WRAPPING_VALUE | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 16-56. TIMER_TOWR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------------|------|-------|-----------------------------|
| 31-24 | RESERVED | R | 0h | Reads return 0. |
| 23-0 | OVF_WRAPPING_VALUE | R/W | 0h | Number of masked interrupts |

17 DCC Registers

Table 17-2 lists the memory-mapped registers for the DCC registers. All register offset addresses not listed in Table 17-2 through Table 17-7 should be considered as reserved locations and the register contents should not be modified.

Table 17-1. DCC Instances

| Instance | Base Address |
|----------|--------------|
| DCC0 | 0080 0000h |
| DCC1 | 0080 4000h |
| DCC2 | 0080 8000h |
| DCC3 | 0080 C000h |
| DCC4 | 0081 0000h |
| DCC5 | 0081 4000h |
| DCC6 | 0081 8000h |
| DCC7 | 0081 C000h |
| DCC8 | 0082 0000h |
| DCC9 | 0082 4000h |
| DCC10 | 0082 8000h |
| DCC11 | 0082 C000h |
| DCC12 | 0083 0000h |
| MCU_DCC0 | 4010 0000h |
| MCU_DCC1 | 4011 0000h |
| MCU_DCC2 | 4012 0000h |

Table 17-2. DCC Registers

| Offset | Acronym | Register Name | DCC0 Physical Address | DCC1 Physical Address | DCC2 Physical Address |
|--------|--------------------------------|-----------------------------------|-----------------------|-----------------------|-----------------------|
| 0h | DCC_GCTRL | DCC Global Control Register | 0080 0000h | 0080 4000h | 0080 8000h |
| 4h | DCC_REV | DCC Revision ID | 0080 0004h | 0080 4004h | 0080 8004h |
| 8h | DCC_CNTSEED0 | Count0 Seed Value Register | 0080 0008h | 0080 4008h | 0080 8008h |
| Ch | DCC_VALIDSEED0 | Valid0 Seed Value Register | 0080 000Ch | 0080 400Ch | 0080 800Ch |
| 10h | DCC_CNTSEED1 | Count1 Seed Value Register | 0080 0010h | 0080 4010h | 0080 8010h |
| 14h | DCC_STATUS | DCC Status Register | 0080 0014h | 0080 4014h | 0080 8014h |
| 18h | DCC_CNT0 | Count0 Value Register | 0080 0018h | 0080 4018h | 0080 8018h |
| 1Ch | DCC_VALID0 | Valid0 Value Register | 0080 001Ch | 0080 401Ch | 0080 801Ch |
| 20h | DCC_CNT1 | Count1 Value Register | 0080 0020h | 0080 4020h | 0080 8020h |
| 24h | DCC_CLKSRC1 | Clock Source Selection Register 1 | 0080 0024h | 0080 4024h | 0080 8024h |
| 28h | DCC_CLKSRC0 | Clock Source Selection Register 0 | 0080 0028h | 0080 4028h | 0080 8028h |
| 2Ch | DCC_GCTRL2 | DCC Global Control Register 2 | 0080 002Ch | 0080 402Ch | 0080 802Ch |
| 30h | DCC_STATUS2 | DCC FIFO Status Register | 0080 0030h | 0080 4030h | 0080 8030h |
| 34h | DCC_ERRCNT | Error Count Register | 0080 0034h | 0080 4034h | 0080 8034h |

Table 17-3. DCC Registers

| Offset | Acronym | Register Name | DCC3 Physical Address | DCC4 Physical Address | DCC5 Physical Address |
|--------|--------------------------------|-----------------------------|-----------------------|-----------------------|-----------------------|
| 0h | DCC_GCTRL | DCC Global Control Register | 0080 C000h | 0081 0000h | 0081 4000h |
| 4h | DCC_REV | DCC Revision ID | 0080 C004h | 0081 0004h | 0081 4004h |
| 8h | DCC_CNTSEED0 | Count0 Seed Value Register | 0080 C008h | 0081 0008h | 0081 4008h |
| Ch | DCC_VALIDSEED0 | Valid0 Seed Value Register | 0080 C00Ch | 0081 000Ch | 0081 400Ch |
| 10h | DCC_CNTSEED1 | Count1 Seed Value Register | 0080 C010h | 0081 0010h | 0081 4010h |
| 14h | DCC_STATUS | DCC Status Register | 0080 C014h | 0081 0014h | 0081 4014h |

Table 17-3. DCC Registers (continued)

| Offset | Acronym | Register Name | DCC3 Physical Address | DCC4 Physical Address | DCC5 Physical Address |
|--------|-----------------------------|-----------------------------------|-----------------------|-----------------------|-----------------------|
| 18h | DCC_CNT0 | Count0 Value Register | 0080 C018h | 0081 0018h | 0081 4018h |
| 1Ch | DCC_VALID0 | Valid0 Value Register | 0080 C01Ch | 0081 001Ch | 0081 401Ch |
| 20h | DCC_CNT1 | Count1 Value Register | 0080 C020h | 0081 0020h | 0081 4020h |
| 24h | DCC_CLKSRC1 | Clock Source Selection Register 1 | 0080 C024h | 0081 0024h | 0081 4024h |
| 28h | DCC_CLKSRC0 | Clock Source Selection Register 0 | 0080 C028h | 0081 0028h | 0081 4028h |
| 2Ch | DCC_GCTRL2 | DCC Global Control Register 2 | 0080 C02Ch | 0081 002Ch | 0081 402Ch |
| 30h | DCC_STATUS2 | DCC FIFO Status Register | 0080 C030h | 0081 0030h | 0081 4030h |
| 34h | DCC_ERRCNT | Error Count Register | 0080 C034h | 0081 0034h | 0081 4034h |

Table 17-4. DCC Registers

| Offset | Acronym | Register Name | DCC6 Physical Address | DCC7 Physical Address | DCC8 Physical Address |
|--------|--------------------------------|-----------------------------------|-----------------------|-----------------------|-----------------------|
| 0h | DCC_GCTRL | DCC Global Control Register | 0081 8000h | 0081 C000h | 0082 0000h |
| 4h | DCC_REV | DCC Revision ID | 0081 8004h | 0081 C004h | 0082 0004h |
| 8h | DCC_CNTSEED0 | Count0 Seed Value Register | 0081 8008h | 0081 C008h | 0082 0008h |
| Ch | DCC_VALIDSEED0 | Valid0 Seed Value Register | 0081 800Ch | 0081 C00Ch | 0082 000Ch |
| 10h | DCC_CNTSEED1 | Count1 Seed Value Register | 0081 8010h | 0081 C010h | 0082 0010h |
| 14h | DCC_STATUS | DCC Status Register | 0081 8014h | 0081 C014h | 0082 0014h |
| 18h | DCC_CNT0 | Count0 Value Register | 0081 8018h | 0081 C018h | 0082 0018h |
| 1Ch | DCC_VALID0 | Valid0 Value Register | 0081 801Ch | 0081 C01Ch | 0082 001Ch |
| 20h | DCC_CNT1 | Count1 Value Register | 0081 8020h | 0081 C020h | 0082 0020h |
| 24h | DCC_CLKSRC1 | Clock Source Selection Register 1 | 0081 8024h | 0081 C024h | 0082 0024h |
| 28h | DCC_CLKSRC0 | Clock Source Selection Register 0 | 0081 8028h | 0081 C028h | 0082 0028h |
| 2Ch | DCC_GCTRL2 | DCC Global Control Register 2 | 0081 802Ch | 0081 C02Ch | 0082 002Ch |
| 30h | DCC_STATUS2 | DCC FIFO Status Register | 0081 8030h | 0081 C030h | 0082 0030h |
| 34h | DCC_ERRCNT | Error Count Register | 0081 8034h | 0081 C034h | 0082 0034h |

Table 17-5. DCC Registers

| Offset | Acronym | Register Name | DCC9 Physical Address | DCC10 Physical Address | DCC11 Physical Address |
|--------|--------------------------------|-----------------------------------|-----------------------|------------------------|------------------------|
| 0h | DCC_GCTRL | DCC Global Control Register | 0082 4000h | 0082 8000h | 0082 C000h |
| 4h | DCC_REV | DCC Revision ID | 0082 4004h | 0082 8004h | 0082 C004h |
| 8h | DCC_CNTSEED0 | Count0 Seed Value Register | 0082 4008h | 0082 8008h | 0082 C008h |
| Ch | DCC_VALIDSEED0 | Valid0 Seed Value Register | 0082 400Ch | 0082 800Ch | 0082 C00Ch |
| 10h | DCC_CNTSEED1 | Count1 Seed Value Register | 0082 4010h | 0082 8010h | 0082 C010h |
| 14h | DCC_STATUS | DCC Status Register | 0082 4014h | 0082 8014h | 0082 C014h |
| 18h | DCC_CNT0 | Count0 Value Register | 0082 4018h | 0082 8018h | 0082 C018h |
| 1Ch | DCC_VALID0 | Valid0 Value Register | 0082 401Ch | 0082 801Ch | 0082 C01Ch |
| 20h | DCC_CNT1 | Count1 Value Register | 0082 4020h | 0082 8020h | 0082 C020h |
| 24h | DCC_CLKSRC1 | Clock Source Selection Register 1 | 0082 4024h | 0082 8024h | 0082 C024h |
| 28h | DCC_CLKSRC0 | Clock Source Selection Register 0 | 0082 4028h | 0082 8028h | 0082 C028h |
| 2Ch | DCC_GCTRL2 | DCC Global Control Register 2 | 0082 402Ch | 0082 802Ch | 0082 C02Ch |
| 30h | DCC_STATUS2 | DCC FIFO Status Register | 0082 4030h | 0082 8030h | 0082 C030h |
| 34h | DCC_ERRCNT | Error Count Register | 0082 4034h | 0082 8034h | 0082 C034h |

Table 17-6. DCC Registers

| Offset | Acronym | Register Name | DCC12 Physical Address |
|--------|--------------------------------|-----------------------------------|------------------------|
| 0h | DCC_GCTRL | DCC Global Control Register | 0083 0000h |
| 4h | DCC_REV | DCC Revision ID | 0083 0004h |
| 8h | DCC_CNTSEED0 | Count0 Seed Value Register | 0083 0008h |
| Ch | DCC_VALIDSEED0 | Valid0 Seed Value Register | 0083 000Ch |
| 10h | DCC_CNTSEED1 | Count1 Seed Value Register | 0083 0010h |
| 14h | DCC_STATUS | DCC Status Register | 0083 0014h |
| 18h | DCC_CNT0 | Count0 Value Register | 0083 0018h |
| 1Ch | DCC_VALID0 | Valid0 Value Register | 0083 001Ch |
| 20h | DCC_CNT1 | Count1 Value Register | 0083 0020h |
| 24h | DCC_CLKSRC1 | Clock Source Selection Register 1 | 0083 0024h |
| 28h | DCC_CLKSRC0 | Clock Source Selection Register 0 | 0083 0028h |
| 2Ch | DCC_GCTRL2 | DCC Global Control Register 2 | 0083 002Ch |
| 30h | DCC_STATUS2 | DCC FIFO Status Register | 0083 0030h |
| 34h | DCC_ERRCNT | Error Count Register | 0083 0034h |

Table 17-7. DCC Registers

| Offset | Acronym | Register Name | MCU_DCC0 Physical Address | MCU_DCC1 Physical Address | MCU_DCC2 Physical Address |
|--------|--------------------------------|-----------------------------------|---------------------------|---------------------------|---------------------------|
| 0h | DCC_GCTRL | DCC Global Control Register | 4010 0000h | 4011 0000h | 4012 0000h |
| 4h | DCC_REV | DCC Revision ID | 4010 0004h | 4011 0004h | 4012 0004h |
| 8h | DCC_CNTSEED0 | Count0 Seed Value Register | 4010 0008h | 4011 0008h | 4012 0008h |
| Ch | DCC_VALIDSEED0 | Valid0 Seed Value Register | 4010 000Ch | 4011 000Ch | 4012 000Ch |
| 10h | DCC_CNTSEED1 | Count1 Seed Value Register | 4010 0010h | 4011 0010h | 4012 0010h |
| 14h | DCC_STATUS | DCC Status Register | 4010 0014h | 4011 0014h | 4012 0014h |
| 18h | DCC_CNT0 | Count0 Value Register | 4010 0018h | 4011 0018h | 4012 0018h |
| 1Ch | DCC_VALID0 | Valid0 Value Register | 4010 001Ch | 4011 001Ch | 4012 001Ch |
| 20h | DCC_CNT1 | Count1 Value Register | 4010 0020h | 4011 0020h | 4012 0020h |
| 24h | DCC_CLKSRC1 | Clock Source Selection Register 1 | 4010 0024h | 4011 0024h | 4012 0024h |
| 28h | DCC_CLKSRC0 | Clock Source Selection Register 0 | 4010 0028h | 4011 0028h | 4012 0028h |
| 2Ch | DCC_GCTRL2 | DCC Global Control Register 2 | 4010 002Ch | 4011 002Ch | 4012 002Ch |
| 30h | DCC_STATUS2 | DCC FIFO Status Register | 4010 0030h | 4011 0030h | 4012 0030h |
| 34h | DCC_ERRCNT | Error Count Register | 4010 0034h | 4011 0034h | 4012 0034h |

17.1 DCC_GCTRL Register (Offset = 0h) [reset = X]

DCC_GCTRL is shown in [Figure 17-1](#) and described in [Table 17-9](#).

Return to [Summary Table](#).

Starts / stops the counters. Clears the error signal.

Table 17-8. DCC_GCTRL Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0000h |
| DCC1 | 0080 4000h |
| DCC2 | 0080 8000h |
| DCC3 | 0080 C000h |
| DCC4 | 0081 0000h |
| DCC5 | 0081 4000h |
| DCC6 | 0081 8000h |
| DCC7 | 0081 C000h |
| DCC8 | 0082 0000h |
| DCC9 | 0082 4000h |
| DCC10 | 0082 8000h |
| DCC11 | 0082 C000h |
| DCC12 | 0083 0000h |
| MCU_DCC0 | 4010 0000h |
| MCU_DCC1 | 4011 0000h |
| MCU_DCC2 | 4012 0000h |

Figure 17-1. DCC_GCTRL Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|------------|----|----|----|--------|----|----|----|--------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DONEENA | | | | SINGLESHOT | | | | ERRENA | | | | DCCENA | | | |
| R/W-5h | | | | R/W-5h | | | | R/W-5h | | | | R/W-5h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-9. DCC_GCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15-12 | DONEENA | R/W | 5h | The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCC_STAT register. User, privilege, and debug mode (read): 0101 = the done signal is disabled others = the done signal is enabled Privilege and debug mode (write): 0101 = disable done signal generation others = enable done signal generation |

Table 17-9. DCC_GCTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 11-8 | SINGLESHOT | R/W | 5h | <p>The SINGLESHOT bit enables/disables repetitive operation of the DCC.</p> <p>User, privilege, and debug mode (read):</p> <p>1010 = stop counting when counter0 and valid0 both reach zero</p> <p>1011 = stop counting when counter1 reaches zero</p> <p>others = continuously repeat (until error)</p> <p>Privilege and debug mode (write):</p> <p>1010 = stop counting when counter0 and valid0 both reach zero</p> <p>1011 = stop counting when counter1 reaches zero</p> <p>others = continuously repeat (until error)</p> |
| 7-4 | ERRENA | R/W | 5h | <p>The ERRENA bit enables/disables the error signal.</p> <p>User, privilege, and debug mode (read):</p> <p>0101 = the error signal is disabled</p> <p>others = the error signal is enabled</p> <p>Privilege and debug mode (write):</p> <p>0101 = disable error signal generation</p> <p>others = enable error signal generation</p> |
| 3-0 | DCCENA | R/W | 5h | <p>The DCCENA bit starts and stops the operation of the dcc.</p> <p>User, privilege, and debug mode (read):</p> <p>0101 = counters are stopped</p> <p>others = counters are running</p> <p>Privilege and debug mode (write):</p> <p>0101 = stop counters and error-checking</p> <p>others = load the counters with their seed values and begin counting</p> |

17.2 DCC_REV Register (Offset = 4h) [reset = X]

DCC_REV is shown in [Figure 17-2](#) and described in [Table 17-11](#).

Return to [Summary Table](#).

Specifies the module version.

Table 17-10. DCC_REV Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0004h |
| DCC1 | 0080 4004h |
| DCC2 | 0080 8004h |
| DCC3 | 0080 C004h |
| DCC4 | 0081 0004h |
| DCC5 | 0081 4004h |
| DCC6 | 0081 8004h |
| DCC7 | 0081 C004h |
| DCC8 | 0082 0004h |
| DCC9 | 0082 4004h |
| DCC10 | 0082 8004h |
| DCC11 | 0082 C004h |
| DCC12 | 0083 0004h |
| MCU_DCC0 | 4010 0004h |
| MCU_DCC1 | 4011 0004h |
| MCU_DCC2 | 4012 0004h |

Figure 17-2. DCC_REV Register

| | | | | | | | |
|--------|----|----------|----|-------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SCHEME | | RESERVED | | FUNC | | | |
| R-1h | | R-X | | R-0h | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FUNC | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RTL | | | | MAJOR | | | |
| R-0h | | | | R-2h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM | | MINOR | | | | | |
| R-0h | | R-4h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 17-11. DCC_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-30 | SCHEME | R | 1h | User, privilege, and debug mode (read): Returns 01. Privilege and debug mode (write): Writes have no effect. |
| 29-28 | RESERVED | R | X | |

Table 17-11. DCC_REV Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|---|
| 27-16 | FUNC | R | 0h | Reflects software-compatibility. If there is no level of software compatibility, a unique func number is assigned for compatible modules, the same number is maintained. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect. |
| 15-11 | RTL | R | 0h | Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect. |
| 10-8 | MAJOR | R | 2h | Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module. User, privilege, and debug mode (read): 0x2 Privilege and debug mode (write): Writes have no effect. |
| 7-6 | CUSTOM | R | 0h | Indicates a special version of the module. May not be supported by standard software. User, privilege, and debug mode (read): 0x0 Privilege and debug mode (write): Writes have no effect. |
| 5-0 | MINOR | R | 4h | Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module. User, privilege, and debug mode (read): 0x4 Privilege and debug mode (write): Writes have no effect. |

17.3 DCC_CNTSEED0 Register (Offset = 8h) [reset = X]

DCC_CNTSEED0 is shown in [Figure 17-3](#) and described in [Table 17-13](#).

Return to [Summary Table](#).

Seed value for the counter attached to clock source 0

Table 17-12. DCC_CNTSEED0 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0008h |
| DCC1 | 0080 4008h |
| DCC2 | 0080 8008h |
| DCC3 | 0080 C008h |
| DCC4 | 0081 0008h |
| DCC5 | 0081 4008h |
| DCC6 | 0081 8008h |
| DCC7 | 0081 C008h |
| DCC8 | 0082 0008h |
| DCC9 | 0082 4008h |
| DCC10 | 0082 8008h |
| DCC11 | 0082 C008h |
| DCC12 | 0083 0008h |
| MCU_DCC0 | 4010 0008h |
| MCU_DCC1 | 4011 0008h |
| MCU_DCC2 | 4012 0008h |

Figure 17-3. DCC_CNTSEED0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | COUNTSEED0 | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-13. DCC_CNTSEED0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19-0 | COUNTSEED0 | R/W | 0h | <p>This field contains the seed value that gets loaded into counter 0 (clock source 0).</p> <p>User, privilege, and debug mode (read): Returns the current seed value for counter 0.</p> <p>Privilege and debug mode (write): Sets the current seed value for counter 0.</p> |

17.4 DCC_VALIDSEED0 Register (Offset = Ch) [reset = X]

DCC_VALIDSEED0 is shown in [Figure 17-4](#) and described in [Table 17-15](#).

Return to [Summary Table](#).

Seed value for the timeout counter attached to clock source 0.

Table 17-14. DCC_VALIDSEED0 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 000Ch |
| DCC1 | 0080 400Ch |
| DCC2 | 0080 800Ch |
| DCC3 | 0080 C00Ch |
| DCC4 | 0081 000Ch |
| DCC5 | 0081 400Ch |
| DCC6 | 0081 800Ch |
| DCC7 | 0081 C00Ch |
| DCC8 | 0082 000Ch |
| DCC9 | 0082 400Ch |
| DCC10 | 0082 800Ch |
| DCC11 | 0082 C00Ch |
| DCC12 | 0083 000Ch |
| MCU_DCC0 | 4010 000Ch |
| MCU_DCC1 | 4011 000Ch |
| MCU_DCC2 | 4012 000Ch |

Figure 17-4. DCC_VALIDSEED0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | VALIDSEED0 | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-15. DCC_VALIDSEED0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | VALIDSEED0 | R/W | 0h | <p>This field contains the seed value that gets loaded into the valid duration counter for clock source 0.</p> <p>User, privilege, and debug mode (read): Returns the current seed value for VALID0.</p> <p>Privilege and debug mode (write): Sets the current seed value for VALID0.</p> |

17.5 DCC_CNTSEED1 Register (Offset = 10h) [reset = X]

DCC_CNTSEED1 is shown in [Figure 17-5](#) and described in [Table 17-17](#).

Return to [Summary Table](#).

Seed value for the counter attached to clock source 1.

Table 17-16. DCC_CNTSEED1 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0010h |
| DCC1 | 0080 4010h |
| DCC2 | 0080 8010h |
| DCC3 | 0080 C010h |
| DCC4 | 0081 0010h |
| DCC5 | 0081 4010h |
| DCC6 | 0081 8010h |
| DCC7 | 0081 C010h |
| DCC8 | 0082 0010h |
| DCC9 | 0082 4010h |
| DCC10 | 0082 8010h |
| DCC11 | 0082 C010h |
| DCC12 | 0083 0010h |
| MCU_DCC0 | 4010 0010h |
| MCU_DCC1 | 4011 0010h |
| MCU_DCC2 | 4012 0010h |

Figure 17-5. DCC_CNTSEED1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | COUNTSEED1 | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-17. DCC_CNTSEED1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------|------|-------|--|
| 31-20 | RESERVED | R/W | X | |
| 19-0 | COUNTSEED1 | R/W | 0h | <p>This field contains the seed value that gets loaded into counter 1 (clock source 1).</p> <p>User, privilege, and debug mode (read): Returns the current seed value for counter 1.</p> <p>Privilege and debug mode (write): Sets the current seed value for counter 1.</p> |

17.6 DCC_STATUS Register (Offset = 14h) [reset = X]

DCCSTATUS is shown in [Figure 17-6](#) and described in [Table 17-19](#).

Return to [Summary Table](#).

Specifies the status of the DCC Module.

Table 17-18. DCC_STATUS Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0014h |
| DCC1 | 0080 4014h |
| DCC2 | 0080 8014h |
| DCC3 | 0080 C014h |
| DCC4 | 0081 0014h |
| DCC5 | 0081 4014h |
| DCC6 | 0081 8014h |
| DCC7 | 0081 C014h |
| DCC8 | 0082 0014h |
| DCC9 | 0082 4014h |
| DCC10 | 0082 8014h |
| DCC11 | 0082 C014h |
| DCC12 | 0083 0014h |
| MCU_DCC0 | 4010 0014h |
| MCU_DCC1 | 4011 0014h |
| MCU_DCC2 | 4012 0014h |

Figure 17-6. DCC_STATUS Register

| | | | | | | | |
|----------|----|----|----|----|----|--------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DONE | ERR |
| R/W-X | | | | | | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write ; -n = value after reset

Table 17-19. DCC_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31-2 | RESERVED | R/W | X | |

Table 17-19. DCC_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--|
| 1 | DONE | R/W | 0h | Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = single-shot mode is not done 1 = single-shot mode is done Privilege and debug mode (write): 0 = no effect 1 = clear the done flag |
| 0 | ERR | R/W | 0h | Indicates whether or not an error has occurred. Writing a 1 to this bit clears the flag. User, privilege, and debug mode (read): 0 = an error has not occurred 1 = an error has occurred Privilege and debug mode (write): 0 = no effect 1 = clear the error flag |

17.7 DCC_CNT0 Register (Offset = 18h) [reset = X]

DCC_CNT0 is shown in [Figure 17-7](#) and described in [Table 17-21](#).

Return to [Summary Table](#).

Value of the counter attached to clock source 0.

Table 17-20. DCC_CNT0 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0018h |
| DCC1 | 0080 4018h |
| DCC2 | 0080 8018h |
| DCC3 | 0080 C018h |
| DCC4 | 0081 0018h |
| DCC5 | 0081 4018h |
| DCC6 | 0081 8018h |
| DCC7 | 0081 C018h |
| DCC8 | 0082 0018h |
| DCC9 | 0082 4018h |
| DCC10 | 0082 8018h |
| DCC11 | 0082 C018h |
| DCC12 | 0083 0018h |
| MCU_DCC0 | 4010 0018h |
| MCU_DCC1 | 4011 0018h |
| MCU_DCC2 | 4012 0018h |

Figure 17-7. DCC_CNT0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | COUNT0 | | | | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 17-21. DCC_CNT0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-20 | RESERVED | R | X | |
| 19-0 | COUNT0 | R | 0h | <p>This field contains the current value of counter 0.</p> <p>User, privilege, and debug mode (read): Returns the current value for counter 0.</p> <p>Privilege and debug mode (write): Writes have no effect.</p> |

17.8 DCC_VALID0 Register (Offset = 1Ch) [reset = X]

DCC_VALID0 is shown in [Figure 17-8](#) and described in [Table 17-23](#).

Return to [Summary Table](#).

Value of the valid counter attached to clock source 0.

Table 17-22. DCC_VALID0 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 001Ch |
| DCC1 | 0080 401Ch |
| DCC2 | 0080 801Ch |
| DCC3 | 0080 C01Ch |
| DCC4 | 0081 001Ch |
| DCC5 | 0081 401Ch |
| DCC6 | 0081 801Ch |
| DCC7 | 0081 C01Ch |
| DCC8 | 0082 001Ch |
| DCC9 | 0082 401Ch |
| DCC10 | 0082 801Ch |
| DCC11 | 0082 C01Ch |
| DCC12 | 0083 001Ch |
| MCU_DCC0 | 4010 001Ch |
| MCU_DCC1 | 4011 001Ch |
| MCU_DCC2 | 4012 001Ch |

Figure 17-8. DCC_VALID0 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | VALID0 | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 17-23. DCC_VALID0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | VALID0 | R | 0h | <p>This field contains the current value of valid counter 0.</p> <p>User, privilege, and debug mode (read): Returns the current value for valid counter 0.</p> <p>Privilege and debug mode (write): writes have no effect.</p> |

17.9 DCC_CNT1 Register (Offset = 20h) [reset = X]

DCC_CNT1 is shown in [Figure 17-9](#) and described in [Table 17-25](#).

Return to [Summary Table](#).

Value of the counter attached to clock source 1.

Table 17-24. DCC_CNT1 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0020h |
| DCC1 | 0080 4020h |
| DCC2 | 0080 8020h |
| DCC3 | 0080 C020h |
| DCC4 | 0081 0020h |
| DCC5 | 0081 4020h |
| DCC6 | 0081 8020h |
| DCC7 | 0081 C020h |
| DCC8 | 0082 0020h |
| DCC9 | 0082 4020h |
| DCC10 | 0082 8020h |
| DCC11 | 0082 C020h |
| DCC12 | 0083 0020h |
| MCU_DCC0 | 4010 0020h |
| MCU_DCC1 | 4011 0020h |
| MCU_DCC2 | 4012 0020h |

Figure 17-9. DCC_CNT1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | COUNT1 | | | | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 17-25. DCC_CNT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-20 | RESERVED | R | X | |
| 19-0 | COUNT1 | R | 0h | This field contains the current value of counter 1. User, privilege, and debug mode (read): Returns the current value for counter 1. Privilege and debug mode (write): writes have no effect. |

17.10 DCC_CLKSRC1 Register (Offset = 24h) [reset = X]

DCC_CLKSRC1 is shown in [Figure 17-10](#) and described in [Table 17-27](#).

Return to [Summary Table](#).

Selects the clock source for counter 1.

Table 17-26. DCC_CLKSRC1 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0024h |
| DCC1 | 0080 4024h |
| DCC2 | 0080 8024h |
| DCC3 | 0080 C024h |
| DCC4 | 0081 0024h |
| DCC5 | 0081 4024h |
| DCC6 | 0081 8024h |
| DCC7 | 0081 C024h |
| DCC8 | 0082 0024h |
| DCC9 | 0082 4024h |
| DCC10 | 0082 8024h |
| DCC11 | 0082 C024h |
| DCC12 | 0083 0024h |
| MCU_DCC0 | 4010 0024h |
| MCU_DCC1 | 4011 0024h |
| MCU_DCC2 | 4012 0024h |

Figure 17-10. DCC_CLKSRC1 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----------|----|----|----|----|----|----|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| KEY | | | | RESERVED | | | | | | | | CLKSRC1 | | | |
| R/W-5h | | | | R/W-X | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-27. DCC_CLKSRC1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-12 | KEY | R/W | 5h | This field enables or disables clock source selection for counter 1. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 1. others: Clock source selection is disabled. The secondary oscillator (clock source 1) is selected for counter 1. |
| 11-5 | RESERVED | R/W | X | |

Table 17-27. DCC_CLKSRC1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 4-0 | CLKSRC1 | R/W | 0h | <p>This field specifies the clock source for counter 1, when the KEY field enables this feature.</p> <p>User, privilege, and debug mode (read): Returns the current value of CLKSRC.</p> <p>Privilege and debug mode (write): Sets the value of CLKSRC.</p> |

17.11 DCC_CLKSRC0 Register (Offset = 28h) [reset = X]

DCC_CLKSRC0 is shown in [Figure 17-11](#) and described in [Table 17-29](#).

Return to [Summary Table](#).

Selects the clock source for counter 0.

Table 17-28. DCC_CLKSRC0 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0028h |
| DCC1 | 0080 4028h |
| DCC2 | 0080 8028h |
| DCC3 | 0080 C028h |
| DCC4 | 0081 0028h |
| DCC5 | 0081 4028h |
| DCC6 | 0081 8028h |
| DCC7 | 0081 C028h |
| DCC8 | 0082 0028h |
| DCC9 | 0082 4028h |
| DCC10 | 0082 8028h |
| DCC11 | 0082 C028h |
| DCC12 | 0083 0028h |
| MCU_DCC0 | 4010 0028h |
| MCU_DCC1 | 4011 0028h |
| MCU_DCC2 | 4012 0028h |

Figure 17-11. DCC_CLKSRC0 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----------|----|----|----|----|----|----|----|---------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| KEY | | | | RESERVED | | | | | | | | CLKSRC0 | | | |
| R/W-0h | | | | R/W-X | | | | | | | | R/W-5h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-29. DCC_CLKSRC0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | RESERVED | R/W | X | |
| 15-12 | KEY | R/W | 0h | This field enables or disables clock source selection for counter 0. User, privilege, and debug mode (read): Returns the current value of the key. Privilege and debug mode (write): Sets the key value. Key values: 1010: The CLKSRC field selects the clock source for counter 0. others: Clock source selection is disabled. The external oscillator (XTAL) is selected for counter 0. |
| 11-4 | RESERVED | R/W | X | |

Table 17-29. DCC_CLKSRC0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 3-0 | CLKSRC0 | R/W | 5h | <p>This field specifies the clock source for counter 0.</p> <p>User, privilege, and debug mode (read): Returns the current value of CLKSRC0.</p> <p>Privilege and debug mode (write): Sets the value of CLKSRC0.</p> |

17.12 DCC_GCTRL2 Register (Offset = 2Ch) [reset = X]

DCC_GCTRL2 is shown in [Figure 17-12](#) and described in [Table 17-31](#).

Return to [Summary Table](#).

Allows configuring different modes of operation for DCC.

Table 17-30. DCC_GCTRL2 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 002Ch |
| DCC1 | 0080 402Ch |
| DCC2 | 0080 802Ch |
| DCC3 | 0080 C02Ch |
| DCC4 | 0081 002Ch |
| DCC5 | 0081 402Ch |
| DCC6 | 0081 802Ch |
| DCC7 | 0081 C02Ch |
| DCC8 | 0082 002Ch |
| DCC9 | 0082 402Ch |
| DCC10 | 0082 802Ch |
| DCC11 | 0082 C02Ch |
| DCC12 | 0083 002Ch |
| MCU_DCC0 | 4010 002Ch |
| MCU_DCC1 | 4011 002Ch |
| MCU_DCC2 | 4012 002Ch |

Figure 17-12. DCC_GCTRL2 Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|-------------|----|----|----|-----------|----|----|----|-------------|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | FIFO_NONERR | | | | FIFO_READ | | | | CONT_ON_ERR | | | |
| R/W-X | | | | R/W-5h | | | | R/W-5h | | | | R/W-5h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-31. DCC_GCTRL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-12 | RESERVED | R/W | X | |
| 11-8 | FIFO_NONERR | R/W | 5h | <p>Enables/disables FIFO writes without the error event on completion of comparison window.</p> <p>User, privilege, and debug mode (read): Returns the current field value.</p> <p>Privilege and debug mode (write): Sets the value of field value.</p> <p>Source values: 0101: Counter values are captured to non-full FIFO only upon Error event. Others: Write counter values to non-full FIFO upon completion of comparison window regardless of error or not.</p> |

Table 17-31. DCC_GCTRL2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7-4 | FIFO_READ | R/W | 5h | <p>Enables the counter read registers reflect FIFO output instead of the live counter value.</p> <p>User, privilege, and debug mode (read): Returns the current field value.</p> <p>Privilege and debug mode (write): Sets the value of field value.</p> <p>Source values: 0101: Counter value is read directly. Others: Counters FIFO output is read.</p> |
| 3-0 | CONT_ON_ERR | R/W | 5h | <p>Continues to next window of comparison despite the error condition.</p> <p>User, privilege, and debug mode (read): Returns the current field value.</p> <p>Privilege and debug mode (write): Sets the value of field value.</p> <p>Enable values: 0101: Comparison and counter reload is stopped from advancing if error is detected. Others: Counters get reloaded with seed and continue counting despite the error condition.</p> |

17.13 DCC_STATUS2 Register (Offset = 30h) [reset = X]

DCC_STATUS2 is shown in [Figure 17-13](#) and described in [Table 17-33](#).

Return to [Summary Table](#).

Specifies the status of the DCC FIFOs.

Table 17-32. DCC_STATUS2 Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0030h |
| DCC1 | 0080 4030h |
| DCC2 | 0080 8030h |
| DCC3 | 0080 C030h |
| DCC4 | 0081 0030h |
| DCC5 | 0081 4030h |
| DCC6 | 0081 8030h |
| DCC7 | 0081 C030h |
| DCC8 | 0082 0030h |
| DCC9 | 0082 4030h |
| DCC10 | 0082 8030h |
| DCC11 | 0082 C030h |
| DCC12 | 0083 0030h |
| MCU_DCC0 | 4010 0030h |
| MCU_DCC1 | 4011 0030h |
| MCU_DCC2 | 4012 0030h |

Figure 17-13. DCC_STATUS2 Register

| | | | | | | | |
|----------|----|------------------|------------------|------------------|-------------------|-------------------|-------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | COUNT1_FIFO_FULL | VALID0_FIFO_FULL | COUNT0_FIFO_FULL | COUNT1_FIFO_EMPTY | VALID0_FIFO_EMPTY | COUNT0_FIFO_EMPTY |
| R-X | | R-0h | R-0h | R-0h | R-1h | R-1h | R-1h |

LEGEND: R = Read Only; -n = value after reset

Table 17-33. DCC_STATUS2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-6 | RESERVED | R | X | |
| 5 | COUNT1_FIFO_FULL | R | 0h | Count1 FIFO Full. Indicates whether Count1 FIFO is full. User, privilege, and debug mode (read): 0: Count1 FIFO is not full 1: Count1 FIFO is full. Privilege and debug mode (write): Writes have no effect. |

Table 17-33. DCC_STATUS2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 4 | VALID0_FIFO_FULL | R | 0h | Valid0 FIFO Full. Indicates whether Valid0 FIFO is full. User, privilege, and debug mode (read): 0: Valid0 FIFO is not full 1: Valid0 FIFO is full. Privilege and debug mode (write): Writes have no effect. |
| 3 | COUNT0_FIFO_FULL | R | 0h | Count0 FIFO Full. Indicates whether Count0 FIFO is full. User, privilege, and debug mode (read): 0: Count0 FIFO is not full 1: Count0 FIFO is full. Privilege and debug mode (write): Writes have no effect. |
| 2 | COUNT1_FIFO_EMPTY | R | 1h | Count1 FIFO Empty. Indicates whether Count1 FIFO is empty. User, privilege, and debug mode (read): 0: Count1 FIFO is not empty 1: Count1 FIFO is empty. Privilege and debug mode (write): Writes have no effect. |
| 1 | VALID0_FIFO_EMPTY | R | 1h | Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty. User, privilege, and debug mode (read): 0: Valid0 FIFO is not empty 1: Valid0 FIFO is empty. Privilege and debug mode (write): Writes have no effect. |
| 0 | COUNT0_FIFO_EMPTY | R | 1h | Count0 FIFO Empty. Indicates whether Count0 FIFO is empty. User, privilege, and debug mode (read): 0: Count0 FIFO is not empty 1: Count0 FIFO is empty. Privilege and debug mode (write): Writes have no effect. |

17.14 DCC_ERRCNT Register (Offset = 34h) [reset = X]

DCC_ERRCNT is shown in [Figure 17-14](#) and described in [Table 17-35](#).

Return to [Summary Table](#).

Counts number of errors since last clear.

Table 17-34. DCC_ERRCNT Instances

| Instance | Physical Address |
|----------|------------------|
| DCC0 | 0080 0034h |
| DCC1 | 0080 4034h |
| DCC2 | 0080 8034h |
| DCC3 | 0080 C034h |
| DCC4 | 0081 0034h |
| DCC5 | 0081 4034h |
| DCC6 | 0081 8034h |
| DCC7 | 0081 C034h |
| DCC8 | 0082 0034h |
| DCC9 | 0082 4034h |
| DCC10 | 0082 8034h |
| DCC11 | 0082 C034h |
| DCC12 | 0083 0034h |
| MCU_DCC0 | 4010 0034h |
| MCU_DCC1 | 4011 0034h |
| MCU_DCC2 | 4012 0034h |

Figure 17-14. DCC_ERRCNT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | ERRCNT | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 17-35. DCC_ERRCNT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-10 | RESERVED | R/W | X | |
| 9-0 | ERRCNT | R/W | 0h | Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it. |

18 ESM Registers

Table 18-2 lists the memory-mapped registers for the ESM. All register offset addresses not listed in Table 18-2 should be considered as reserved locations and the register contents should not be modified.

Table 18-1. ESM Instances

| Instance | Base Address |
|---------------|--------------|
| ESM0_CFG | 0070 0000h |
| MCU_ESM0_CFG | 4080 0000h |
| WKUP_ESM0_CFG | 4208 0000h |

Table 18-2. ESM Registers

| Offset | Acronym | Register Name | ESM0_CFG Physical Address | MCU_ESM0_C FG Physical Address | WKUP_ESM0 _CFG Physical Address |
|-------------------|-----------------------------------|---|---------------------------------|--------------------------------------|--|
| 0h | ESM_PID | Revision Register | 0070 0000h | 4080 0000h | 4208 0000h |
| 4h | ESM_INFO | Info Register | 0070 0004h | 4080 0004h | 4208 0004h |
| 8h | ESM_EN | Global Enable Register | 0070 0008h | 4080 0008h | 4208 0008h |
| Ch | ESM_SFT_RST | Global Soft Reset Register | 0070 000Ch | 4080 000Ch | 4208 000Ch |
| 10h | ESM_ERR_RAW | Config Error Raw Status/Set Register | 0070 0010h | 4080 0010h | 4208 0010h |
| 14h | ESM_ERR_STS | Config Error Interrupt Enable Status/ Clear Register | 0070 0014h | 4080 0014h | 4208 0014h |
| 18h | ESM_ERR_EN_SET | Config Error Interrupt Enable Set Register | 0070 0018h | 4080 0018h | 4208 0018h |
| 1Ch | ESM_ERR_EN_CLR | Config Error Interrupt Enabled Clear Register | 0070 001Ch | 4080 001Ch | 4208 001Ch |
| 20h | ESM_LOW_PRI | Low Priority Prioritized Register | 0070 0020h | 4080 0020h | 4208 0020h |
| 24h | ESM_HI_PRI | High Priority Prioritized Register | 0070 0024h | 4080 0024h | 4208 0024h |
| 28h | ESM_LOW | Low Priority Interrupt Status Register | 0070 0028h | 4080 0028h | 4208 0028h |
| 2Ch | ESM_HI | High Priority Interrupt Status Register | 0070 002Ch | 4080 002Ch | 4208 002Ch |
| 30h | ESM_EOI | ESM_EOI Interrupt Register | 0070 0030h | 4080 0030h | 4208 0030h |
| 40h | ESM_PIN_CTRL | Error Pin Control Register | 0070 0040h | 4080 0040h | 4208 0040h |
| 44h | ESM_PIN_STS | Error Pin Status Register | 0070 0044h | 4080 0044h | 4208 0044h |
| 48h | ESM_PIN_CNTR | Error Counter Value Register | 0070 0048h | 4080 0048h | 4208 0048h |
| 4Ch | ESM_PIN_CNTR_PRE | Error Counter Value Pre-Load Register | 0070 004Ch | 4080 004Ch | 4208 004Ch |
| 400h + formula | ESM_RAW_j | Config Error Raw Status/Set Register | 0070 0400h + formula | 4080 0400h + formula | 4208 0400h + formula |
| 404h + formula | ESM_STS_j | Level Error Interrupt Enable Status/ Clear Register | 0070 0404h + formula | 4080 0404h + formula | 4208 0404h + formula |
| 408h + formula | ESM_INTR_EN_SET_j | Level Error Interrupt Enable Set Register | 0070 0408h + formula | 4080 0408h + formula | 4208 0408h + formula |
| 40Ch + formula | ESM_INTR_EN_CLR_j | Level Error Interrupt Enabled Clear Register | 0070 040Ch + formula | 4080 040Ch + formula | 4208 040Ch + formula |
| 410h + formula | ESM_INT_PRIO_j | Level Error Interrupt Enabled Clear Register | 0070 0410h + formula | 4080 0410h + formula | 4208 0410h + formula |
| 414h + formula | ESM_PIN_EN_SET_j | Level Error Interrupt Enabled Clear Register | 0070 0414h + formula | 4080 0414h + formula | 4208 0414h + formula |
| 418h + formula | ESM_PIN_EN_CLR_j | Level Error Interrupt Enabled Clear Register | 0070 0418h + formula | 4080 0418h + formula | 4208 0418h + formula |

18.1 ESM_PID Register (Offset = 0h) [reset = 6FE02900h]

ESM_PID is shown in [Figure 18-1](#) and described in [Table 18-4](#).

Return to [Summary Table](#).

The Revision Register contains the major and minor revisions for the module.

Table 18-3. ESM_PID Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0000h |
| MCU_ESM0_CFG | 4080 0000h |
| WKUP_ESM0_CFG | 4208 0000h |

Figure 18-1. ESM_PID Register

| | | | | | | | | | | | | | | | |
|--------|----|------|----|--------|-------|----|----|--------|----|-------|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SCHEME | | BU | | FUNC | | | | | | | | | | | |
| R-1h | | R-2h | | R-FE0h | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTL | | | | | MAJOR | | | CUSTOM | | MINOR | | | | | |
| R-5h | | | | | R-1h | | | R-0h | | R-0h | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-4. ESM_PID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------|------|-------|--|
| 31-30 | SCHEME | R | 1h | ESM_PID register scheme Always reads as 1h. Writes have no affect. |
| 29-28 | BU | R | 2h | Business Unit: 2h = Processors |
| 27-16 | FUNC | R | FE0h | Module ID. Always read as the assigned functional ID. Writes have no affect. |
| 15-11 | RTL | R | 5h | RTL revision. Will vary depending on release. |
| 10-8 | MAJOR | R | 1h | Major revision |
| 7-6 | CUSTOM | R | 0h | Custom. Special version. |
| 5-0 | MINOR | R | 0h | Minor revision |

18.2 ESM_INFO Register (Offset = 4h) [reset = X]

ESM_INFO is shown in [Figure 18-2](#) and described in [Table 18-6](#).

Return to [Summary Table](#).

The Info Register gives the configuration information of this ESM.

Table 18-5. ESM_INFO Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0004h |
| MCU_ESM0_CFG | 4080 0004h |
| WKUP_ESM0_CFG | 4208 0004h |

Figure 18-2. ESM_INFO Register

| | | | | | | | |
|--------------|----------|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LAST_RESET | RESERVED | | | | | | |
| R-0h | R-X | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| PULSE_GROUPS | | | | | | | |
| R-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GROUPS | | | | | | | |
| R-X | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-6. ESM_INFO Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|---------------------|---|
| 31 | LAST_RESET | R | 0h | This bit indicates whether the last reset was a Warm or Power-On Rest 0h = Last reset was a Power On Reset 1h = Last reset was a Warm Reset |
| 30-16 | RESERVED | R | X | Always read as 0h. Writes have no affect. |
| 15-8 | PULSE_GROUPS | R | X (see description) | Indicates the number of event groups that are pulse (as opposed to level) driven. X = 1h for WKUP_ESM0_CFG X = 1h for MCU_ESM0_CFG X = 1h for ESM0_CFG |
| 7-0 | GROUPS | R | X (see description) | Indicates the total number of groups that exist in the ESM. X = 3h for WKUP_ESM0_CFG X = 4h for MCU_ESM0_CFG X = 8h for ESM0_CFG |

18.3 ESM_EN Register (Offset = 8h) [reset = X]

ESM_EN is shown in [Figure 18-3](#) and described in [Table 18-8](#).

Return to [Summary Table](#).

The Global Enable Register has the master interrupt mask

Table 18-7. ESM_EN Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0008h |
| MCU_ESM0_CFG | 4080 0008h |
| WKUP_ESM0_CFG | 4208 0008h |

Figure 18-3. ESM_EN Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|--------|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | KEY | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-8. ESM_EN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 3-0 | KEY | R/W | 0h | <p>This field is the global mask for all interrupts. It is reset by the warm reset. The purpose is to leave all of the raw status and per-interrupt enable bits alone so that, after a warm reset, software may observe the state of the ESM before the warm reset and try to debug what may have caused the reset.</p> <p>0h = All interrupts are disabled Fh = All interrupts are enabled Others = These are an invalid state. Software should never write these values. If these values are ever read, they indicate that an error has occurred. In this state, all interrupts are enabled (biased to false enable).</p> |

18.4 ESM_SFT_RST Register (Offset = Ch) [reset = X]

ESM_SFT_RST is shown in [Figure 18-4](#) and described in [Table 18-10](#).

Return to [Summary Table](#).

The Global Soft Reset Register controls the global clear for raw status and enables

Table 18-9. ESM_SFT_RST Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 000Ch |
| MCU_ESM0_CFG | 4080 000Ch |
| WKUP_ESM0_CFG | 4208 000Ch |

Figure 18-4. ESM_SFT_RST Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|------|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | KEY | | | |
| W-X | | | | | | | | | | | | | | | | | | | | | | | | | | | | W-0h | | | |

LEGEND: W = Write Only; -n = value after reset

Table 18-10. ESM_SFT_RST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | W | X | Always read as 0h. Writes have no affect. |
| 3-0 | KEY | W | 0h | Global Soft Reset field. Writing to this field can cause all of the raw status and all enables to be cleared. This can be used to reset the ESM state after debugging because of a warm reset. 0h (R) = Always read as 0h Fh (W) = Clear all raw status and enable bits Others (W) = No effect |

18.5 ESM_ERR_RAW Register (Offset = 10h) [reset = X]

ESM_ERR_RAW is shown in [Figure 18-5](#) and described in [Table 18-12](#).

Return to [Summary Table](#).

Raw Status/Set Register for Configuration Errors

Table 18-11. ESM_ERR_RAW Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0010h |
| MCU_ESM0_CFG | 4080 0010h |
| WKUP_ESM0_CFG | 4208 0010h |

Figure 18-5. ESM_ERR_RAW Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | STS | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | | | | | R/W1S-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-12. ESM_ERR_RAW Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 7-0 | STS | R/W1S | 0h | <p>This is the raw status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h.</p> <p>Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7</p> <p>0h (R) = Inactive 1h (R) = Active/Pending 0h (W) = No effect 1h (W) = Set to Interrupt Raw Status</p> <p>Note: Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for:</p> <p>Bit 2 - Bit 0 for WKUP_ESM0_CFG (3 groups) Bit 3 - Bit 0 for MCU_ESM0_CFG (4 groups) Bit 7 - Bit 0 for ESM0_CFG (8 groups)</p> |

18.6 ESM_ERR_STS Register (Offset = 14h) [reset = X]

ESM_ERR_STS is shown in [Figure 18-6](#) and described in [Table 18-14](#).

Return to [Summary Table](#).

Config Error Enable and Clear Register

Table 18-13. ESM_ERR_STS Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0014h |
| MCU_ESM0_CFG | 4080 0014h |
| WKUP_ESM0_CFG | 4208 0014h |

Figure 18-6. ESM_ERR_STS Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|----------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | MSK | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | | | | | R/W1C-0h | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-14. ESM_ERR_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 7-0 | MSK | R/W1C | 0h | <p>This is the masked status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7</p> <p>0h (R) = Inactive or Disabled 1h (R) = Active/Pending and Enabled 0h (W) = No effect 1h (W) = Clear Interrupt Raw Status</p> <p>Note: Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for: Bit 2 - Bit 0 for WKUP_ESM0_CFG (3 groups) Bit 3 - Bit 0 for MCU_ESM0_CFG (4 groups) Bit 7 - Bit 0 for ESM0_CFG (8 groups)</p> |

18.7 ESM_ERR_EN_SET Register (Offset = 18h) [reset = X]

ESM_ERR_EN_SET is shown in [Figure 18-7](#) and described in [Table 18-16](#).

[Return to Summary Table.](#)

Config Error Enable Set Register

Table 18-15. ESM_ERR_EN_SET Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0018h |
| MCU_ESM0_CFG | 4080 0018h |
| WKUP_ESM0_CFG | 4208 0018h |

Figure 18-7. ESM_ERR_EN_SET Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | MSK | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W1S-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-16. ESM_ERR_EN_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 7-0 | MSK | R/W1S | 0h | <p>This is the mask enable for errors in the configuration for Group N. If the corresponding bit and the ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7</p> <p>0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Set Enable</p> <p>Note: Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for: Bit 2 - Bit 0 for WKUP_ESM0_CFG (3 groups) Bit 3 - Bit 0 for MCU_ESM0_CFG (4 groups) Bit 7 - Bit 0 for ESM0_CFG (8 groups)</p> |

18.8 ESM_ERR_EN_CLR Register (Offset = 1Ch) [reset = X]

ESM_ERR_EN_CLR is shown in [Figure 18-8](#) and described in [Table 18-18](#).

Return to [Summary Table](#).

Config Error Interrupt Enabled Clear register

Table 18-17. ESM_ERR_EN_CLR Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 001Ch |
| MCU_ESM0_CFG | 4080 001Ch |
| WKUP_ESM0_CFG | 4208 001Ch |

Figure 18-8. ESM_ERR_EN_CLR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | MSK | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W1C-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-18. ESM_ERR_EN_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-8 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 7-0 | MSK | R/W1C | 0h | <p>This is the mask clear for errors in the configuration for Group N. If the corresponding bit and the ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Bit 0 - Group 0 Bit 1 - Group 1 ... Bit 7 - Group 7</p> <p>0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Clear Enable</p> <p>Note: Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. The following bits are available (not reserved) for:</p> <p>Bit 2 - Bit 0 for WKUP_ESM0_CFG (3 groups) Bit 3 - Bit 0 for MCU_ESM0_CFG (4 groups) Bit 7 - Bit 0 for ESM0_CFG (8 groups)</p> |

18.9 ESM_LOW_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

ESM_LOW_PRI is shown in [Figure 18-9](#) and described in [Table 18-20](#).

Return to [Summary Table](#).

Shows which is the highest priority outstanding low priority interrupt

Table 18-19. ESM_LOW_PRI Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0020h |
| MCU_ESM0_CFG | 4080 0020h |
| WKUP_ESM0_CFG | 4208 0020h |

Figure 18-9. ESM_LOW_PRI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLS | | | | | | | | | | | | | | | | LVL | | | | | | | | | | | | | | | |
| R-FFFFh | | | | | | | | | | | | | | | | R-FFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-20. ESM_LOW_PRI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|--|
| 31-16 | PLS | R | FFFFh | Indicates what the highest priority low priority interrupt caused by a pulse number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for high priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x2. A value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event. |
| 15-0 | LVL | R | FFFFh | Indicates what the highest priority low priority interrupt caused by a level number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for High Priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x2. A value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event. |

18.10 ESM_HI_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

ESM_HI_PRI is shown in [Figure 18-10](#) and described in [Table 18-22](#).

[Return to Summary Table.](#)

Shows which is the highest priority outstanding high priority interrupt

Table 18-21. ESM_HI_PRI Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0024h |
| MCU_ESM0_CFG | 4080 0024h |
| WKUP_ESM0_CFG | 4208 0024h |

Figure 18-10. ESM_HI_PRI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PLS | | | | | | | | | | | | | | | | LVL | | | | | | | | | | | | | | | |
| R-FFFFh | | | | | | | | | | | | | | | | R-FFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-22. ESM_HI_PRI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|---|
| 31-16 | PLS | R | FFFFh | <p>Indicates what the highest priority high priority interrupt caused by a pulse number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for high priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x0. A value of all ones (0xFFFF) indicates that there are no high priority interrupts pending.</p> <p>This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.</p> |
| 15-0 | LVL | R | FFFFh | <p>Indicates what the highest priority low priority interrupt caused by a level number is. The lowest event has the highest priority. I.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for high priority while Global Events 2, 3, and 4 are configured for low priority, then the value of this field will be 0x0. A value of all ones (0xFFFF) indicates that there are no high priority interrupts pending.</p> <p>This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.</p> |

18.11 ESM_LOW Register (Offset = 28h) [reset = 0h]

ESM_LOW is shown in [Figure 18-11](#) and described in [Table 18-24](#).

Return to [Summary Table](#).

Shows which groups have outstanding low priority interrupts

Table 18-23. ESM_LOW Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0028h |
| MCU_ESM0_CFG | 4080 0028h |
| WKUP_ESM0_CFG | 4208 0028h |

Figure 18-11. ESM_LOW Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-24. ESM_LOW Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | STS | R | 0h | Indicates which Event Groups have one or more low priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc... (bit N is for Event Group N). 0h (R) = Inactive 1h (R) = Active/Pending |

18.12 ESM_HI Register (Offset = 2Ch) [reset = 0h]

ESM_HI is shown in [Figure 18-12](#) and described in [Table 18-26](#).

Return to [Summary Table](#).

Shows which groups have outstanding high priority interrupts

Table 18-25. ESM_HI Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 002Ch |
| MCU_ESM0_CFG | 4080 002Ch |
| WKUP_ESM0_CFG | 4208 002Ch |

Figure 18-12. ESM_HI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-26. ESM_HI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | STS | R | 0h | Indicates which Event Groups have one or more high priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc... (bit N is for Event Group N). 0h (R) = Inactive 1h (R) = Active/Pending |

18.13 ESM_EOI Register (Offset = 30h) [reset = X]

ESM_EOI is shown in [Figure 18-13](#) and described in [Table 18-28](#).

Return to [Summary Table](#).

End of Interrupt Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 18-27. ESM_EOI Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0030h |
| MCU_ESM0_CFG | 4080 0030h |
| WKUP_ESM0_CFG | 4208 0030h |

Figure 18-13. ESM_EOI Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | KEY | | | | | | | | | | | | | |
| W-X | | | | | | | | | | | | | | | | | | W-0h | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 18-28. ESM_EOI Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | W | X | Always read as 0h. Writes have no affect. |
| 10-0 | KEY | W | 0h | <p>This is the interrupt being serviced. Writing the corresponding vector to this field will cause a re-evaluation of interrupts. If, when the vector is written, there are still pending interrupts, a new pulse will be generated. Reads always return 0.</p> <p>0h (W) = Configuration error interrupt</p> <p>1h (W) = Low priority error interrupt</p> <p>2h (W) = High priority error interrupt</p> <p>3h – 2047h (W) = Reserved (writes have no effect)</p> |

18.14 ESM_PIN_CTRL Register (Offset = 40h) [reset = X]

ESM_PIN_CTRL is shown in [Figure 18-14](#) and described in [Table 18-30](#).

Return to [Summary Table](#).

This register controls the SAFETY_ERRORn pin output

Table 18-29. ESM_PIN_CTRL Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0040h |
| MCU_ESM0_CFG | 4080 0040h |
| WKUP_ESM0_CFG | 4208 0040h |

Figure 18-14. ESM_PIN_CTRL Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|--------|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | | | | | KEY | | | |
| R/W-X | | | | | | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-30. ESM_PIN_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-4 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 3-0 | KEY | R/W | 0h | <p>Pin control key. This field controls behavior of the error pin. Note, during reset the field is 0h, but the error pin is asserted (active low). Immediately after reset, the error pin de-asserts. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0. A global soft reset will also CLEAR all pending faults.</p> <p>0h = Normal Mode: Error pin will activate when an enabled Error Event occurs.</p> <p>5h = CLEAR Event: generates a CLEAR event to the ESM state machine. Key will return to Normal Mode (0h) on the next cycle.</p> <p>Ah = Force Error Mode: Forces the error pin to active. To clear the error pin (return to the ESM_IDLE state) write this field back to Normal Mode (writing a CLEAR event will also work). Software may only write to Force Error Mode while in IDLE. Attempting Force Error while in another state will have no effect</p> <p>All Other Values = Normal Mode: Writing any of these values will have no effect. Reading any of these values indicate that one or more bits have experienced a single event upset and software should write the field back to 0h. The ESM will continue to operate in Normal Mode.</p> |

18.15 ESM_PIN_STS Register (Offset = 44h) [reset = X]

ESM_PIN_STS is shown in [Figure 18-15](#) and described in [Table 18-32](#).

Return to [Summary Table](#).

This register reflects the status of the error_pin_n output

Table 18-31. ESM_PIN_STS Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0044h |
| MCU_ESM0_CFG | 4080 0044h |
| WKUP_ESM0_CFG | 4208 0044h |

Figure 18-15. ESM_PIN_STS Register

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | VAL |
| R-X | | | | | | | | | | | | | | | R-X |

LEGEND: R = Read Only; -n = value after reset

Table 18-32. ESM_PIN_STS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|---------------------|--|
| 31-1 | RESERVED | R | X | Always read as 0h. Writes have no affect. |
| 0 | VAL | R | X (see description) | <p>This field indicates the status of the error pin as looped back from the I/O. This field reflects the state of the ERR_I pin. Since the ERR_O pin is only affected by Power-On-Reset, then the value of this field may be 1h after the release of Warm Reset.</p> <p>0h (R) = Asserted (pin is active, low) 1h (R) = De-Asserted (pin is inactive, high)</p> <p>Note: While in reset the error pin is actually active (asserted low), but goes inactive immediately after the de-assertion of Power-on-Reset. Hence, the value that will be read after Power-on-Reset is 1h, but may be 0h after a warm reset.</p> |

18.16 ESM_PIN_CNTR Register (Offset = 48h) [reset = X]

ESM_PIN_CNTR is shown in [Figure 18-16](#) and described in [Table 18-34](#).

Return to [Summary Table](#).

This register shows the current value of the error pin counter

Table 18-33. ESM_PIN_CNTR Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 0048h |
| MCU_ESM0_CFG | 4080 0048h |
| WKUP_ESM0_CFG | 4208 0048h |

Figure 18-16. ESM_PIN_CNTR Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COUNT | | | | | | | | | | | | | | | | | | | | | | | |
| R-X | | | | | | | | R-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 18-34. ESM_PIN_CNTR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-24 | RESERVED | R | X | Always read as 0h. Writes have no affect. |
| 23-0 | COUNT | R | 0h | This field indicates the current value of the time interval counter. See ESM_PIN_CNTR_PRE register for a description. This register is reloaded to the counter_preload value on entry to the ESM_ERROR state from ESM_IDLE and counts down by one per clock cycle. Once the counter has reached 0, the minimum time interval has expired. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h. |

18.17 ESM_PIN_CNTR_PRE Register (Offset = 4Ch) [reset = X]

ESM_PIN_CNTR_PRE is shown in [Figure 18-17](#) and described in [Table 18-36](#).

Return to [Summary Table](#).

This register contains the value that is loaded in to the Error Counter

Table 18-35. ESM_PIN_CNTR_PRE Instances

| Instance | Physical Address |
|---------------|------------------|
| ESM0_CFG | 0070 004Ch |
| MCU_ESM0_CFG | 4080 004Ch |
| WKUP_ESM0_CFG | 4208 004Ch |

Figure 18-17. ESM_PIN_CNTR_PRE Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | COUNT | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-36. ESM_PIN_CNTR_PRE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-24 | RESERVED | R/W | X | Always read as 0h. Writes have no affect. |
| 23-0 | COUNT | R/W | 0h | This is the value that will be pre-loaded in to the counter field of the ESM_PIN_CNTR register whenever the ESM enters the ESM_ERROR state from ESM_IDLE. The default value is determined based on the ESM clock frequency, so that there is a minimum low time of 100µs. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0h. |

18.18 ESM_RAW_j Register (Offset = 400h + formula) [reset = 0h]

ESM_RAW_j is shown in [Figure 18-18](#) and described in [Table 18-38](#).

Return to [Summary Table](#).

Raw Status/Set Register for Group A Errors

Offset = 400h + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-37. ESM_RAW_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 0400h + formula |
| MCU_ESM0_CFG | 4080 0400h + formula |
| WKUP_ESM0_CFG | 4208 0400h + formula |

Figure 18-18. ESM_RAW_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W1S-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-38. ESM_RAW_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|-------|-------|---|
| 31-0 | STS | R/W1S | 0h | <p>This is the raw status of the events in group N. Each bit corresponds to event Q where $Q = N \times 32 + \text{Bit}$ (Example: bit 0 is event $N \times 32 + 0$, bit 1 is $N \times 32 + 1$ etc...)</p> <p>For Level events, the raw status is the event input synchronized to the ESM clock and stored in a multi-bit (for redundancy) internal register.</p> <p>For Pulse events, the raw status is multi-bit (for redundancy) internal register that is set when two of the three edge detection circuits on the redundant event capture a rising edge.</p> <p>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h (R) = Inactive 1h (R) = Active/Pending 0h (W) = No effect 1h (W) = Set to Interrupt Raw Status</p> |

18.19 ESM_STS_j Register (Offset = 404h + formula) [reset = 0h]

ESM_STS_j is shown in [Figure 18-19](#) and described in [Table 18-40](#).

Return to [Summary Table](#).

Error Enable and Clear Register

Offset = 404h + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-39. ESM_STS_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 0404h + formula |
| MCU_ESM0_CFG | 4080 0404h + formula |
| WKUP_ESM0_CFG | 4208 0404h + formula |

Figure 18-19. ESM_STS_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W1C-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-40. ESM_STS_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|-------|-------|--|
| 31-0 | MSK | R/W1C | 0h | <p>This is the masked status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc...) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h (R) = Inactive or Disabled 1h (R) = Active/Pending and Enabled 0h (W) = No effect 1h (W) = Clear Interrupt Raw Status</p> |

18.20 ESM_INTR_EN_SET_j Register (Offset = 408h + formula) [reset = 0h]

ESM_INTR_EN_SET_j is shown in [Figure 18-20](#) and described in [Table 18-42](#).

Return to [Summary Table](#).

Level Error Enable Set Register

Offset = 408h + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-41. ESM_INTR_EN_SET_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 0408h + formula |
| MCU_ESM0_CFG | 4080 0408h + formula |
| WKUP_ESM0_CFG | 4208 0408h + formula |

Figure 18-20. ESM_INTR_EN_SET_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W1S-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-42. ESM_INTR_EN_SET_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|-------|-------|---|
| 31-0 | MSK | R/W1S | 0h | <p>This field is used to enable the mask of events in group N. Each bit corresponds to event Q where $Q = N * 32 + \text{Bit}$ (Example: bit 0 is event $N * 32 + 0$, bit 1 is $N * 32 + 1$ etc...). If the corresponding bit and the global enable ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Set Enable</p> |

18.21 ESM_INTR_EN_CLR_j Register (Offset = 40Ch + formula) [reset = 0h]

ESM_INTR_EN_CLR_j is shown in [Figure 18-21](#) and described in [Table 18-44](#).

Return to [Summary Table](#).

Level Error Interrupt Enabled Clear register

Offset = 40Ch + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-43. ESM_INTR_EN_CLR_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 040Ch + formula |
| MCU_ESM0_CFG | 4080 040Ch + formula |
| WKUP_ESM0_CFG | 4208 040Ch + formula |

Figure 18-21. ESM_INTR_EN_CLR_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W1C-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-44. ESM_INTR_EN_CLR_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|-------|-------|---|
| 31-0 | MSK | R/W1C | 0h | <p>This field is used to disable the mask of events in group N. Each bit corresponds to event Q where $Q = N \times 32 + \text{Bit}$ (Example: bit 0 is event $N \times 32 + 0$, bit 1 is $N \times 32 + 1$ etc...). If the corresponding bit and the global enable ESM_EN are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Clear Enable</p> |

18.22 ESM_INT_PRIO_j Register (Offset = 410h + formula) [reset = 0h]

ESM_INT_PRIO_j is shown in [Figure 18-22](#) and described in [Table 18-46](#).

Return to [Summary Table](#).

Level Error Interrupt Enabled Clear register

Offset = 410h + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-45. ESM_INT_PRIO_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 0410h + formula |
| MCU_ESM0_CFG | 4080 0410h + formula |
| WKUP_ESM0_CFG | 4208 0410h + formula |

Figure 18-22. ESM_INT_PRIO_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 18-46. ESM_INT_PRIO_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|--|
| 31-0 | MSK | R/W | 0h | <p>This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group N. Each bit corresponds to event Q where $Q = N \times 32 + \text{Bit}$ (Example: bit 0 is event $N \times 32 + 0$, bit 1 is $N \times 32 + 1$ etc...) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h = Low priority interrupt (default) 1h = High priority interrupt</p> |

18.23 ESM_PIN_EN_SET_j Register (Offset = 414h + formula) [reset = 0h]

ESM_PIN_EN_SET_j is shown in [Figure 18-23](#) and described in [Table 18-48](#).

Return to [Summary Table](#).

Level Error Interrupt Enabled Clear register

Offset = 414h + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-47. ESM_PIN_EN_SET_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 0414h + formula |
| MCU_ESM0_CFG | 4080 0414h + formula |
| WKUP_ESM0_CFG | 4208 0414h + formula |

Figure 18-23. ESM_PIN_EN_SET_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W1S-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 18-48. ESM_PIN_EN_SET_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|-------|-------|--|
| 31-0 | MSK | R/W1S | 0h | <p>This field is used to enable the mask of events in group N. Each bit corresponds to event Q where $Q = N * 32 + \text{Bit}$ (Example: bit 0 is event $N * 32 + 0$, bit 1 is $N * 32 + 1$ etc...) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Set Enable. Corresponding event, when set, will count as a pending error event for the ESM state machine.</p> |

18.24 ESM_PIN_EN_CLR_j Register (Offset = 418h + formula) [reset = 0h]

ESM_PIN_EN_CLR_j is shown in [Figure 18-24](#) and described in [Table 18-50](#).

Return to [Summary Table](#).

Level Error Interrupt Enabled Clear register

Offset = 418h + (j * 20h); where

j = 0h to 2h for WKUP_ESM0_CFG

j = 0h to 3h for MCU_ESM0_CFG

j = 0h to 7h for ESM0_CFG

Table 18-49. ESM_PIN_EN_CLR_j Instances

| Instance | Physical Address |
|---------------|----------------------|
| ESM0_CFG | 0070 0418h + formula |
| MCU_ESM0_CFG | 4080 0418h + formula |
| WKUP_ESM0_CFG | 4208 0418h + formula |

Figure 18-24. ESM_PIN_EN_CLR_j Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MSK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W1C-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 18-50. ESM_PIN_EN_CLR_j Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|-------|-------|--|
| 31-0 | MSK | R/W1C | 0h | <p>This field is used to enable the mask of events in group N. Each bit corresponds to event Q where $Q = N * 32 + \text{Bit}$ (Example: bit 0 is event $N * 32 + 0$, bit 1 is $N * 32 + 1$ etc...) This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>0h (R) = Disabled 1h (R) = Enabled 0h (W) = No effect 1h (W) = Clear Enable. Corresponding events will no longer count as pending error events for the ESM state machine</p> |

19 MCRC Registers

Table 19-2 lists the memory-mapped registers for the NAVSS0_MCRC. All register offset addresses not listed in Table 19-2 should be considered as reserved locations and the register contents should not be modified.

This is the MMR register region for the mcrc64_regs component

Table 19-1. NAVSS0_MCRC Instances

| Instance | Base Address |
|-----------------|--------------|
| NAVSS0_MCRC | 31F7 0000h |
| MCU_NAVSS0_MCRC | 2A26 4000h |

Table 19-2. NAVSS0_MCRC Registers

| Offset | Acronym | Register Name | NAVSS0_MCRC Physical Address | MCU_NAVSS0_MCRC Physical Address |
|--------|---|---|------------------------------|----------------------------------|
| 0h | MCRC_CRC_CTRL0 | CRC Global Control Register 0 | 31F7 0000h | 2A26 4000h |
| 8h | MCRC_CRC_CTRL1 | CRC Global Control Register 1 | 31F7 0008h | 2A26 4008h |
| 10h | MCRC_CRC_CTRL2 | CRC Global Control Register 2 | 31F7 0010h | 2A26 4010h |
| 18h | MCRC_CRC_INTS | CRC Interrupt Enable Set Register | 31F7 0018h | 2A26 4018h |
| 20h | MCRC_CRC_INTR | CRC Interrupt Enable Reset Register | 31F7 0020h | 2A26 4020h |
| 28h | MCRC_CRC_STATUS | CRC Interrupt Status Register | 31F7 0028h | 2A26 4028h |
| 30h | MCRC_CRC_INT_OFFSET_REG | CRC Interrupt Offset | 31F7 0030h | 2A26 4030h |
| 38h | MCRC_CRC_BUSY | CRC Busy Register | 31F7 0038h | 2A26 4038h |
| 40h | MCRC_CRC_PCOUNT_REG1 | CRC Pattern Counter Preload Register1 | 31F7 0040h | 2A26 4040h |
| 44h | MCRC_CRC_SCOUNT_REG1 | CRC Sector Counter Preload Register1 | 31F7 0044h | 2A26 4044h |
| 48h | MCRC_CRC_CURSEC_REG1 | CRC Current Sector Register 1 | 31F7 0048h | 2A26 4048h |
| 4Ch | MCRC_CRC_WDTPLD1 | CRC channel 1 Watchdog Timeout Preload Register A | 31F7 004Ch | 2A26 404Ch |
| 50h | MCRC_CRC_BCTOPLD1 | CRC channel 1 Block Complete Timeout Preload Register B | 31F7 0050h | 2A26 4050h |
| 60h | MCRC_PSA_SIGREGL1 | Channel 1 PSA signature low register | 31F7 0060h | 2A26 4060h |
| 64h | MCRC_PSA_SIGREGH1 | Channel 1 PSA signature high register | 31F7 0064h | 2A26 4064h |
| 68h | MCRC_CRC_REGL1 | Channel 1 CRC value low register | 31F7 0068h | 2A26 4068h |
| 6Ch | MCRC_CRC_REGH1 | Channel 1 CRC value high register | 31F7 006Ch | 2A26 406Ch |
| 70h | MCRC_PSA_SECSIGREGL1 | Channel 1 PSA sector signature low register | 31F7 0070h | 2A26 4070h |
| 74h | MCRC_PSA_SECSIGREGH1 | Channel 1 PSA sector signature high register | 31F7 0074h | 2A26 4074h |
| 78h | MCRC_RAW_DATAAREGL1 | Channel 1 Raw Data Low Register | 31F7 0078h | 2A26 4078h |
| 7Ch | MCRC_RAW_DATAAREGH1 | Channel 1 Raw Data High Register | 31F7 007Ch | 2A26 407Ch |
| 80h | MCRC_CRC_PCOUNT_REG2 | CRC Pattern Counter Preload Register2 | 31F7 0080h | 2A26 4080h |
| 84h | MCRC_CRC_SCOUNT_REG2 | CRC Sector Counter Preload Register2 | 31F7 0084h | 2A26 4084h |
| 88h | MCRC_CRC_CURSEC_REG2 | CRC Current Sector Register 2 | 31F7 0088h | 2A26 4088h |
| 8Ch | MCRC_CRC_WDTPLD2 | CRC channel 2 Watchdog Timeout Preload Register | 31F7 008Ch | 2A26 408Ch |
| 90h | MCRC_CRC_BCTOPLD2 | CRC channel 2 Block Complete Timeout Preload Register | 31F7 0090h | 2A26 4090h |
| A0h | MCRC_PSA_SIGREGL2 | Channel 2 PSA signature low register | 31F7 00A0h | 2A26 40A0h |
| A4h | MCRC_PSA_SIGREGH2 | Channel 2 PSA signature high register | 31F7 00A4h | 2A26 40A4h |
| A8h | MCRC_CRC_REGL2 | Channel 2 CRC value low register | 31F7 00A8h | 2A26 40A8h |
| ACH | MCRC_CRC_REGH2 | Channel 2 CRC value high register | 31F7 00ACH | 2A26 40ACH |

Table 19-2. NAVSS0_MCRC Registers (continued)

| Offset | Acronym | Register Name | NAVSS0_MCRC Physical Address | MCU_NAVSS0_MC RC Physical Address |
|-------------------|---|---|---------------------------------|---|
| B0h | MCRC_PSA_SECSIGREGL2 | Channel 2 PSA sector signature low register | 31F7 00B0h | 2A26 40B0h |
| B4h | MCRC_PSA_SECSIGREGH2 | Channel 2 PSA sector signature high register | 31F7 00B4h | 2A26 40B4h |
| B8h | MCRC_RAW_DATAAREGL2 | Channel 2 Raw Data Low Register | 31F7 00B8h | 2A26 40B8h |
| BCh | MCRC_RAW_DATAAREGH2 | Channel 2 Raw Data High Register | 31F7 00BCh | 2A26 40BCh |
| C0h | MCRC_CRC_PCOUNT_REG3 | CRC Pattern Counter Preload Register3 | 31F7 00C0h | 2A26 40C0h |
| C4h | MCRC_CRC_SCOUNT_REG3 | CRC Sector Counter Preload Register3 | 31F7 00C4h | 2A26 40C4h |
| C8h | MCRC_CRC_CURSEC_REG3 | CRC Current Sector Register 3 | 31F7 00C8h | 2A26 40C8h |
| CCh | MCRC_CRC_WDTPOLD3 | CRC channel 3 Watchdog Timeout Preload Register | 31F7 00CCh | 2A26 40CCh |
| D0h | MCRC_CRC_BCTOPLD3 | CRC channel 3 Block Complete Timeout Preload Register | 31F7 00D0h | 2A26 40D0h |
| E0h | MCRC_PSA_SIGREGL3 | Channel 3 PSA signature low register | 31F7 00E0h | 2A26 40E0h |
| E4h | MCRC_PSA_SIGREGH3 | Channel 3 PSA signature high register | 31F7 00E4h | 2A26 40E4h |
| E8h | MCRC_CRC_REGL3 | Channel 3 CRC value low register | 31F7 00E8h | 2A26 40E8h |
| ECh | MCRC_CRC_REGH3 | Channel 3 CRC value high register | 31F7 00ECh | 2A26 40ECh |
| F0h | MCRC_PSA_SECSIGREGL3 | Channel 3 PSA sector signature low register | 31F7 00F0h | 2A26 40F0h |
| F4h | MCRC_PSA_SECSIGREGH3 | Channel 3 PSA sector signature high register | 31F7 00F4h | 2A26 40F4h |
| F8h | MCRC_RAW_DATAAREGL3 | Channel 3 Raw Data Low Register | 31F7 00F8h | 2A26 40F8h |
| FCh | MCRC_RAW_DATAAREGH3 | Channel 3 Raw Data High Register | 31F7 00FCh | 2A26 40FCh |
| 100h | MCRC_CRC_PCOUNT_REG4 | CRC Pattern Counter Preload Register4 | 31F7 0100h | 2A26 4100h |
| 104h | MCRC_CRC_SCOUNT_REG4 | CRC Sector Counter Preload Register4 | 31F7 0104h | 2A26 4104h |
| 108h | MCRC_CRC_CURSEC_REG4 | CRC Current Sector Register 4 | 31F7 0108h | 2A26 4108h |
| 10Ch | MCRC_CRC_WDTPOLD4 | CRC channel 4 Watchdog Timeout Preload Register | 31F7 010Ch | 2A26 410Ch |
| 110h | MCRC_CRC_BCTOPLD4 | CRC channel 4 Block Complete Timeout Preload Register | 31F7 0110h | 2A26 4110h |
| 120h | MCRC_PSA_SIGREGL4 | Channel 4 PSA signature low register | 31F7 0120h | 2A26 4120h |
| 124h | MCRC_PSA_SIGREGH4 | Channel 4 PSA signature high register | 31F7 0124h | 2A26 4124h |
| 128h | MCRC_CRC_REGL4 | Channel 4 CRC value low register | 31F7 0128h | 2A26 4128h |
| 12Ch | MCRC_CRC_REGH4 | Channel 4 CRC value high register | 31F7 012Ch | 2A26 412Ch |
| 130h | MCRC_PSA_SECSIGREGL4 | Channel 4 PSA sector signature low register | 31F7 0130h | 2A26 4130h |
| 134h | MCRC_PSA_SECSIGREGH4 | Channel 4 PSA sector signature high register | 31F7 0134h | 2A26 4134h |
| 138h | MCRC_RAW_DATAAREGL4 | Channel 4 Raw Data Low Register | 31F7 0138h | 2A26 4138h |
| 13Ch | MCRC_RAW_DATAAREGH4 | Channel 4 Raw Data High Register | 31F7 013Ch | 2A26 413Ch |
| 140h | MCRC_BUS_SEL | Data bus tracing selection | 31F7 0140h | 2A26 4140h |
| 200h + formula | MCRC_I0_PSA_SIGREG1_CPY_Y | Channel 1 PSA signature block region | 31F7 0200h + formula | 2A26 4200h + formula |
| 280h + formula | MCRC_I0_PSA_SIGREG2_CPY_Y | Channel 2 PSA signature block region | 31F7 0280h + formula | 2A26 4280h + formula |
| 300h + formula | MCRC_I0_PSA_SIGREG3_CPY_Y | Channel 3 PSA signature block region | 31F7 0300h + formula | 2A26 4300h + formula |

Table 19-2. NAVSS0_MCRC Registers (continued)

| Offset | Acronym | Register Name | NAVSS0_MCRC Physical Address | MCU_NAVSS0_MC RC Physical Address |
|-------------------|---|--------------------------------------|---------------------------------|---|
| 380h + formula | MCRC_I0_PSA_SIGREG4_CPY_Y | Channel 4 PSA signature block region | 31F7 0380h + formula | 2A26 4380h + formula |

19.1 MCRC_CRC_CTRL0 Register (Offset = 0h) [reset = X]

MCRC_CRC_CTRL0 is shown in [Figure 19-1](#) and described in [Table 19-4](#).

Return to [Summary Table](#).

CRC Global Control Register 0

Table 19-3. MCRC_CRC_CTRL0 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0000h |
| MCU_NAVSS0_MCRC | 2A26 4000h |

Figure 19-1. MCRC_CRC_CTRL0 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | CH4_PSA_SWRE |
| R/W-X | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | CH3_PSA_SWRE |
| R/W-X | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | CH2_PSA_SWRE |
| R/W-X | | | | | | | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | CH1_PSA_SWRE |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-4. MCRC_CRC_CTRL0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-25 | RESERVED | R/W | X | |
| 24 | CH4_PSA_SWRE | R/W | 0h | Channel 4 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset |
| 23-17 | RESERVED | R/W | X | |
| 16 | CH3_PSA_SWRE | R/W | 0h | Channel 3 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset |
| 15-9 | RESERVED | R/W | X | |
| 8 | CH2_PSA_SWRE | R/W | 0h | Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by writing a 0 . 0 = PSA Signature Register not reset 1 = PSA Signature Register reset |
| 7-1 | RESERVED | R/W | X | |

Table 19-4. MCRC_CRC_CTRL0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 0 | CH1_PSA_SWRE | R/W | 0h | <p>Channel 1 PSA Software Reset.</p> <p>When set, the PSA Signature Register is reset to all zero.</p> <p>Software reset does not reset software reset bit itself.</p> <p>Therefore, CPU is required to clear this bit by writing a 0 .</p> <p>0 = PSA Signature Register not reset</p> <p>1 = PSA Signature Register reset</p> |

19.2 MCRC_CRC_CTRL1 Register (Offset = 8h) [reset = X]

MCRC_CRC_CTRL1 is shown in [Figure 19-2](#) and described in [Table 19-6](#).

Return to [Summary Table](#).

CRC Global Control Register 1

Table 19-5. MCRC_CRC_CTRL1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0008h |
| MCU_NAVSS0_MCRC | 2A26 4008h |

Figure 19-2. MCRC_CRC_CTRL1 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | PWDN |
| R/W-X | | | | | | | R/W-0h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-6. MCRC_CRC_CTRL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-1 | RESERVED | R/W | X | |
| 0 | PWDN | R/W | 0h | Power Down. When set, MCRC moduleMCRC Module is put in power down mode. 0 = MCRC is not in power down mode. 1 = MCRC is in power down mode. |

19.3 MCRC_CRC_CTRL2 Register (Offset = 10h) [reset = X]

MCRC_CRC_CTRL2 is shown in [Figure 19-3](#) and described in [Table 19-8](#).

Return to [Summary Table](#).

Channel Mode Control Register

Table 19-7. MCRC_CRC_CTRL2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0010h |
| MCU_NAVSS0_MCRC | 2A26 4010h |

Figure 19-3. MCRC_CRC_CTRL2 Register

| | | | | | | | |
|----------|----|----|-----------------|----------|----|----------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | CH4_MODE | |
| R/W-X | | | | | | R/W-0h | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | CH3_MODE | |
| R/W-X | | | | | | R/W-0h | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | CH2_MODE | |
| R/W-X | | | | | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CH1_TRACEE N | RESERVED | | CH1_MODE | |
| R/W-X | | | R/W-0h | R/W-X | | R/W-0h | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-8. MCRC_CRC_CTRL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-26 | RESERVED | R/W | X | |
| 25-24 | CH4_MODE | R/W | 0h | Channel 4 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode For all four channels the seed value can be first planted into PSA register before the Channel Mode is switched to Full-CPU mode since host CPU controls the amount of data for compression. During AUTO mode, the PSA register is automatically reset to zero at the end of each sector compression. |
| 23-18 | RESERVED | R/W | X | |
| 17-16 | CH3_MODE | R/W | 0h | Channel 3 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode |

Table 19-8. MCRC_CRC_CTRL2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 15-10 | RESERVED | R/W | X | |
| 9-8 | CH2_MODE | R/W | 0h | Channel 2 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode |
| 7-5 | RESERVED | R/W | X | |
| 4 | CH1_TRACEEN | R/W | 0h | Channel 1 Data Trace Enable When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses. 0 = Data Trace disable 1 = Data Trace enable |
| 3-2 | RESERVED | R/W | X | |
| 1-0 | CH1_MODE | R/W | 0h | Channel 1 Mode. 00 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register. 01 = AUTO mode 10 = Semi-CPU mode 11 = Full-CPU mode |

19.4 MCRC_CRC_INTS Register (Offset = 18h) [reset = X]

MCRC_CRC_INTS is shown in [Figure 19-4](#) and described in [Table 19-10](#).

Return to [Summary Table](#).

CRC Interrupt Enable Set Register

Table 19-9. MCRC_CRC_INTS Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0018h |
| MCU_NAVSS0_MCRC | 2A26 4018h |

Figure 19-4. MCRC_CRC_INTS Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|----|----|-------------------|--------------|-------------|---------------|-------------|
| RESERVED | | | CH4_TIME_OUT_ENS_ | CH4_UNDERENS | CH4_OVERENS | CH4_CRC_FAILS | CH4_CCITENS |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | CH3_TIME_OUT_ENS_ | CH3_UNDERENS | CH3_OVERENS | CH3_CRC_FAILS | CH3_CCITENS |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | CH2_TIME_OUT_ENS_ | CH2_UNDERENS | CH2_OVERENS | CH2_CRC_FAILS | CH2_CCITENS |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CH1_TIME_OUT_ENS_ | CH1_UNDERENS | CH1_OVERENS | CH1_CRC_FAILS | CH1_CCITENS |
| R/W-X | | | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 19-10. MCRC_CRC_INTS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------------|-------|-------|--|
| 31-29 | RESERVED | R/W | X | |
| 28 | CH4_TIME_OUT_ENS_ | R/W1S | 0h | Channel 4 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 27 | CH4_UNDERENS | R/W1S | 0h | Channel 4 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |

Table 19-10. MCRC_CRC_INTS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|---|
| 26 | CH4_OVERENS | R/W1S | 0h | Channel 4 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |
| 25 | CH4_CRC_FAILENS | R/W1S | 0h | Channel 4 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |
| 24 | CH4_CCITENS | R/W1S | 0h | Channel 4 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable |
| 23-21 | RESERVED | R/W | X | |
| 20 | CH3_TIME_OUT_ENS | R/W1S | 0h | Channel 3 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 19 | CH3_UNDERENS | R/W1S | 0h | Channel 3 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |
| 18 | CH3_OVERENS | R/W1S | 0h | Channel 3 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |

Table 19-10. MCRC_CRC_INTS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------------|-------|-------|---|
| 17 | CH3_CRC_FAILENS | R/W1S | 0h | Channel 3 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |
| 16 | CH3_CCITENS | R/W1S | 0h | Channel 3 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable |
| 15-13 | RESERVED | R/W | X | |
| 12 | CH2_TIME_OUT_ENS_ | R/W1S | 0h | Channel 2 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 11 | CH2_UNDERENS | R/W1S | 0h | Channel 2 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |
| 10 | CH2_OVERENS | R/W1S | 0h | Channel 2 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |
| 9 | CH2_CRC_FAILENS | R/W1S | 0h | Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |

Table 19-10. MCRC_CRC_INTS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 8 | CH2_CCITENS | R/W1S | 0h | Channel 2 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable |
| 7-5 | RESERVED | R/W | X | |
| 4 | CH1_TIME_OUT_ENS_ | R/W1S | 0h | Channel 1 Timeout Interrupt Enable Bit Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 3 | CH1_UNDERENS | R/W1S | 0h | Channel 1 Underrun Interrupt Enable Bit Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |
| 2 | CH1_OVERENS | R/W1S | 0h | Channel 1 Overrun Interrupt Enable Bit Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |
| 1 | CH1_CRC_FAILENS | R/W1S | 0h | Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |
| 0 | CH1_CCITENS | R/W1S | 0h | Channel 1 Compression Complete Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt enable |

19.5 MCRC_CRC_INTR Register (Offset = 20h) [reset = X]

MCRC_CRC_INTR is shown in [Figure 19-5](#) and described in [Table 19-12](#).

Return to [Summary Table](#).

CRC Interrupt Enable Reset Register

Table 19-11. MCRC_CRC_INTR Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0020h |
| MCU_NAVSS0_MCRC | 2A26 4020h |

Figure 19-5. MCRC_CRC_INTR Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|----|----|------------------|--------------|-------------|----------------|-------------|
| RESERVED | | | CH4_TIME_OUT_ENR | CH4_UNDERENR | CH4_OVERENR | CH4_CRC_FAILNR | CH4_CCITENR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | CH3_TIME_OUT_ENR | CH3_UNDERENR | CH3_OVERENR | CH3_CRC_FAILNR | CH3_CCITENR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | CH2_TIME_OUT_ENR | CH2_UNDERENR | CH2_OVERENR | CH2_CRC_FAILNR | CH2_CCITENR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CH1_TIME_OUT_ENR | CH1_UNDERENR | CH1_OVERENR | CH1_CRC_FAILNR | CH1_CCITENR |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-12. MCRC_CRC_INTR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-29 | RESERVED | R/W | X | |
| 28 | CH4_TIME_OUT_ENR | R/W1C | 0h | Channel 4 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 27 | CH4_UNDERENR | R/W1C | 0h | Channel 4 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |

Table 19-12. MCRC_CRC_INTR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------------|-------|-------|--|
| 26 | CH4_OVERENR | R/W1C | 0h | Channel 4 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |
| 25 | CH4_CRC_FAILENR | R/W1C | 0h | Channel 4 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |
| 24 | CH4_CCITENR | R/W1C | 0h | Channel 4 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable |
| 23-21 | RESERVED | R/W | X | |
| 20 | CH3_TIME_OUT_ENR_ | R/W1C | 0h | Channel 3 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 19 | CH3_UNDERENR | R/W1C | 0h | Channel 3 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |
| 18 | CH3_OVERENR | R/W1C | 0h | Channel 3 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |

Table 19-12. MCRC_CRC_INTR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------------|-------|-------|---|
| 17 | CH3_CRC_FAILENR | R/W1C | 0h | Channel 3 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |
| 16 | CH3_CCITENR | R/W1C | 0h | Channel 3 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable |
| 15-13 | RESERVED | R/W | X | |
| 12 | CH2_TIME_OUT_ENR_ | R/W1C | 0h | Channel 2 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 11 | CH2_UNDERENR | R/W1C | 0h | Channel 2 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |
| 10 | CH2_OVERENR | R/W1C | 0h | Channel 2 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |
| 9 | CH2_CRC_FAILENR | R/W1C | 0h | Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |

Table 19-12. MCRC_CRC_INTR Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 8 | CH2_CCITENR | R/W1C | 0h | Channel 2 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable |
| 7-5 | RESERVED | R/W | X | |
| 4 | CH1_TIME_OUT_ENR_ | R/W1C | 0h | Channel 1 Timeout Interrupt Disable Bit Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Timeout Interrupt disable 1 = Timeout Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Timeout Interrupt enable |
| 3 | CH1_UNDERENR | R/W1C | 0h | Channel 1 Underrun Interrupt Disable Bit Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Underrun Interrupt disable 1 = Underrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Underrun Interrupt enable |
| 2 | CH1_OVERENR | R/W1C | 0h | Channel 1 Overrun Interrupt Disable Bit Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = Overrun Interrupt disable 1 = Overrun Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Overrun Interrupt enable |
| 1 | CH1_CRC_FAILENR | R/W1C | 0h | Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable). User and privileged mode read: 0 = CRC Fail Interrupt disable 1 = CRC Fail Interrupt enable User and privileged mode write: 0 = Has no effect 1 = CRC Fail Interrupt enable |
| 0 | CH1_CCITENR | R/W1C | 0h | Channel 1 Compression Complete Interrupt Disable Bit Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status (interrupt enable/disable) User and privileged mode read: 0 = Compression Complete Interrupt disable 1 = Compression Complete Interrupt enable User and privileged mode write: 0 = Has no effect 1 = Compression Complete Interrupt disable |

19.6 MCRC_CRC_STATUS Register (Offset = 28h) [reset = X]

MCRC_CRC_STATUS is shown in [Figure 19-6](#) and described in [Table 19-14](#).

Return to [Summary Table](#).

CRC Interrupt Status Register

Table 19-13. MCRC_CRC_STATUS Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0028h |
| MCU_NAVSS0_MCRC | 2A26 4028h |

Figure 19-6. MCRC_CRC_STATUS Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------|----|----|--------------|-----------|----------|--------------|----------|
| RESERVED | | | CH4_TIME_OUT | CH4_UNDER | CH4_OVER | CH4_CRC_FAIL | CH4_CCIT |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | CH3_TIME_OUT | CH3_UNDER | CH3_OVER | CH3_CRC_FAIL | CH3_CCIT |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | CH2_TIME_OUT | CH2_UNDER | CH2_OVER | CH2_CRC_FAIL | CH2_CCIT |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | CH1_TIME_OUT | CH1_UNDER | CH1_OVER | CH1_CRC_FAIL | CH1_CCIT |
| R/W-X | | | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 19-14. MCRC_CRC_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|-------|-------|--|
| 31-29 | RESERVED | R/W | X | |
| 28 | CH4_TIME_OUT | R/W1C | 0h | Channel 4 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in both AUTO and Semi-CPU mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active |
| 27 | CH4_UNDER | R/W1C | 0h | Channel 4 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active |
| 26 | CH4_OVER | R/W1C | 0h | Channel 4 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in either AUTO or Semi-CPU mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active |

Table 19-14. MCRC_CRC_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|--------------|-------|-------|--|
| 25 | CH4_CRC_FAIL | R/W1C | 0h | Channel 4 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active |
| 24 | CH4_CCIT | R/W1C | 0h | Channel 4 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active |
| 23-21 | RESERVED | R/W | X | |
| 20 | CH3_TIME_OUT | R/W1C | 0h | Channel 3 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in both AUTO and Semi-CPU mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active |
| 19 | CH3_UNDER | R/W1C | 0h | Channel 3 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active |
| 18 | CH3_OVER | R/W1C | 0h | Channel 3 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in either AUTO or Semi-CPU mode 0 = No overrun interrupt is active 1 = Overrun interrupt is active |
| 17 | CH3_CRC_FAIL | R/W1C | 0h | Channel 3 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active |
| 16 | CH3_CCIT | R/W1C | 0h | Channel 3 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active |
| 15-13 | RESERVED | R/W | X | |
| 12 | CH2_TIME_OUT | R/W1C | 0h | Channel 2 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in both AUTO and Semi-CPU mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active |
| 11 | CH2_UNDER | R/W1C | 0h | Channel 2 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active |
| 10 | CH2_OVER | R/W1C | 0h | Channel 2 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in either AUTO or Semi-CPU mode. 0 = No overrun interrupt is active 1 = Overrun interrupt is active |

Table 19-14. MCRC_CRC_STATUS Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|-------|-------|--|
| 9 | CH2_CRC_FAIL | R/W1C | 0h | Channel 2 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active |
| 8 | CH2_CCIT | R/W1C | 0h | Channel 2 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active |
| 7-5 | RESERVED | R/W | X | |
| 4 | CH1_TIME_OUT | R/W1C | 0h | Channel 1 CRC Timeout Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in both AUTO and Semi-CPU mode. 0 = No timeout interrupt is active 1 = Timeout interrupt is active |
| 3 | CH1_UNDER | R/W1C | 0h | Channel 1 CRC Underrun Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only 0 = No underrun interrupt is active 1 = Underrun interrupt is active |
| 2 | CH1_OVER | R/W1C | 0h | Channel 1 CRC Overrun Status Flag This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in either AUTO or Semi-CPU mode. 0 = No overrun interrupt is active 1 = Overrun interrupt is active |
| 1 | CH1_CRC_FAIL | R/W1C | 0h | Channel 1 CRC Compare Fail Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only. 0 = No CRC compare fail interrupt is active 1 = CRC compare fail interrupt is active |
| 0 | CH1_CCIT | R/W1C | 0h | Channel 1 CRC Pattern Compression Complete Status Flag. This bit is cleared by writing a 1 to it only. Writing 0 has no effect. This bit is only set in Semi-CPU mode. 0 = No CRC pattern compression complete interrupt is active 1 = CRC pattern compression complete interrupt is active |

19.7 MCRC_CRC_INT_OFFSET_REG Register (Offset = 30h) [reset = X]

MCRC_CRC_INT_OFFSET_REG is shown in [Figure 19-7](#) and described in [Table 19-16](#).

Return to [Summary Table](#).

CRC Interrupt Offset

Table 19-15. MCRC_CRC_INT_OFFSET_REG Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0030h |
| MCU_NAVSS0_MCRC | 2A26 4030h |

Figure 19-7. MCRC_CRC_INT_OFFSET_REG Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|------|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | | CRC | | | | | | | |
| R-X | | | | | | | | | | | | | | | | | | | | | | | | R-0h | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-16. MCRC_CRC_INT_OFFSET_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-8 | RESERVED | R | X | |
| 7-0 | CRC | R | 0h | Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register automatically clears the respective interrupt flag. |

19.8 MCRC_CRC_BUSY Register (Offset = 38h) [reset = X]

MCRC_CRC_BUSY is shown in [Figure 19-8](#) and described in [Table 19-18](#).

Return to [Summary Table](#).

CRC Busy Register

Table 19-17. MCRC_CRC_BUSY Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0038h |
| MCU_NAVSS0_MCRC | 2A26 4038h |

Figure 19-8. MCRC_CRC_BUSY Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | CH4_BUSY |
| R-X | | | | | | | R-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | CH3_BUSY |
| R-X | | | | | | | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | CH2_BUSY |
| R-X | | | | | | | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | CH1_BUSY |
| R-X | | | | | | | R-0h |

LEGEND: R = Read Only; -n = value after reset

Table 19-18. MCRC_CRC_BUSY Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-25 | RESERVED | R | X | |
| 24 | CH4_BUSY | R | 0h | During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |
| 23-17 | RESERVED | R | X | |
| 16 | CH3_BUSY | R | 0h | During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |
| 15-9 | RESERVED | R | X | |
| 8 | CH2_BUSY | R | 0h | During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |
| 7-1 | RESERVED | R | X | |
| 0 | CH1_BUSY | R | 0h | During AUTO or Semi-CPU mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |

19.9 MCRC_CRC_PCOUNT_REG1 Register (Offset = 40h) [reset = X]

MCRC_CRC_PCOUNT_REG1 is shown in [Figure 19-9](#) and described in [Table 19-20](#).

Return to [Summary Table](#).

CRC Pattern Counter Preload Register1

Table 19-19. MCRC_CRC_PCOUNT_REG1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0040h |
| MCU_NAVSS0_MCRC | 2A26 4040h |

Figure 19-9. MCRC_CRC_PCOUNT_REG1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | CRC_PAT_COUNT1 | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-20. MCRC_CRC_PCOUNT_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-20 | RESERVED | R/W | X | |
| 19-0 | CRC_PAT_COUNT1 | R/W | 0h | Channel 1 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

19.10 MCRC_CRC_SCOUNT_REG1 Register (Offset = 44h) [reset = X]

MCRC_CRC_SCOUNT_REG1 is shown in [Figure 19-10](#) and described in [Table 19-22](#).

Return to [Summary Table](#).

CRC Sector Counter Preload Register1

Table 19-21. MCRC_CRC_SCOUNT_REG1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0044h |
| MCU_NAVSS0_MCRC | 2A26 4044h |

Figure 19-10. MCRC_CRC_SCOUNT_REG1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_SEC_COUNT1 | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-22. MCRC_CRC_SCOUNT_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | CRC_SEC_COUNT1 | R/W | 0h | Channel 1 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

19.11 MCRC_CRC_CURSEC_REG1 Register (Offset = 48h) [reset = X]

MCRC_CRC_CURSEC_REG1 is shown in [Figure 19-11](#) and described in [Table 19-24](#).

Return to [Summary Table](#).

CRC Current Sector Register 1

Table 19-23. MCRC_CRC_CURSEC_REG1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0048h |
| MCU_NAVSS0_MCRC | 2A26 4048h |

Figure 19-11. MCRC_CRC_CURSEC_REG1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_CURSEC1 | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-24. MCRC_CRC_CURSEC_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | CRC_CURSEC1 | R | 0h | <p>Channel 1 Current Sector ID Register.</p> <p>In AUTO mode, this register contains the current sector number of which the signature verification fails.</p> <p>The sector counter is a free running up counter.</p> <p>When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU.</p> <p>While it is frozen, it does not capture another erroneous sector number.</p> <p>When this condition happens, an overrun interrupt is generated instead.</p> <p>Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.</p> |

19.12 MCRC_CRC_WDTPLD1 Register (Offset = 31F7004Ch) [reset = X]

MCRC_CRC_WDTPLD1 is shown in [Figure 19-12](#) and described in [Table 19-26](#).

Return to [Summary Table](#).

CRC channel 1 Watchdog Timeout Preload Register A

Table 19-25. MCRC_CRC_WDTPLD1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 004Ch |
| MCU_NAVSS0_MCRC | 2A26 404Ch |

Figure 19-12. MCRC_CRC_WDTPLD1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_WDTPD1 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-26. MCRC_CRC_WDTPLD1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_WDTPLD1 | R/W | 0h | Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

19.13 MCRC_CRC_BCTOPLD1 Register (Offset = 50h) [reset = X]

MCRC_CRC_BCTOPLD1 is shown in [Figure 19-13](#) and described in [Table 19-28](#).

Return to [Summary Table](#).

CRC channel 1 Block Complete Timeout Preload Register B

Table 19-27. MCRC_CRC_BCTOPLD1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0050h |
| MCU_NAVSS0_MCRC | 2A26 4050h |

Figure 19-13. MCRC_CRC_BCTOPLD1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_BCTOPLD1 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-28. MCRC_CRC_BCTOPLD1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_BCTOPLD1 | R/W | 0h | Channel 1 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. |

19.14 MCRC_PSA_SIGREGL1 Register (Offset = 60h) [reset = 0h]

MCRC_PSA_SIGREGL1 is shown in [Figure 19-14](#) and described in [Table 19-30](#).

Return to [Summary Table](#).

Channel 1 PSA signature low register

Table 19-29. MCRC_PSA_SIGREGL1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0060h |
| MCU_NAVSS0_MCRC | 2A26 4060h |

Figure 19-14. MCRC_PSA_SIGREGL1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-30. MCRC_PSA_SIGREGL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---|
| 31-0 | PSASIG1 | R/W | 0h | Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register. |

19.15 MCRC_PSA_SIGREGH1 Register (Offset = 64h) [reset = 0h]

MCRC_PSA_SIGREGH1 is shown in [Figure 19-15](#) and described in [Table 19-32](#).

Return to [Summary Table](#).

Channel 1 PSA signature high register

Table 19-31. MCRC_PSA_SIGREGH1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0064h |
| MCU_NAVSS0_MCRC | 2A26 4064h |

Figure 19-15. MCRC_PSA_SIGREGH1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG1_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-32. MCRC_PSA_SIGREGH1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-0 | PSASIG1_63_32 | R/W | 0h | Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register. |

19.16 MCRC_CRC_REGL1 Register (Offset = 68h) [reset = 0h]

MCRC_CRC_REGL1 is shown in [Figure 19-16](#) and described in [Table 19-34](#).

Return to [Summary Table](#).

Channel 1 CRC value low register

Table 19-33. MCRC_CRC_REGL1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0068h |
| MCU_NAVSS0_MCRC | 2A26 4068h |

Figure 19-16. MCRC_CRC_REGL1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-34. MCRC_CRC_REGL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CRC1 | R/W | 0h | Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] register. |

19.17 MCRC_CRC_REGH1 Register (Offset = 6Ch) [reset = 0h]

MCRC_CRC_REGH1 is shown in [Figure 19-17](#) and described in [Table 19-36](#).

Return to [Summary Table](#).

Channel 1 CRC value high register

Table 19-35. MCRC_CRC_REGH1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 006Ch |
| MCU_NAVSS0_MCRC | 2A26 406Ch |

Figure 19-17. MCRC_CRC_REGH1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC1_47_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-36. MCRC_CRC_REGH1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | CRC1_47_32 | R/W | 0h | Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register. |

19.18 MCRC_PSA_SECSIGREGL1 Register (Offset = 31F70070h) [reset = 0h]

MCRC_PSA_SECSIGREGL1 is shown in [Figure 19-18](#) and described in [Table 19-38](#).

Return to [Summary Table](#).

Channel 1 PSA sector signature low register

Table 19-37. MCRC_PSA_SECSIGREGL1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0070h |
| MCU_NAVSS0_MCRC | 2A26 4070h |

Figure 19-18. MCRC_PSA_SECSIGREGL1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-38. MCRC_PSA_SECSIGREGL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | PSASECSIG1 | R | 0h | Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register. |

19.19 MCRC_PSA_SECSIGREGH1 Register (Offset = 31F70074h) [reset = 0h]

MCRC_PSA_SECSIGREGH1 is shown in [Figure 19-19](#) and described in [Table 19-40](#).

Return to [Summary Table](#).

Channel 1 PSA sector signature high register

Table 19-39. MCRC_PSA_SECSIGREGH1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0074h |
| MCU_NAVSS0_MCRC | 2A26 4074h |

Figure 19-19. MCRC_PSA_SECSIGREGH1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG1_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-40. MCRC_PSA_SECSIGREGH1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-0 | PSASECSIG1_63_32 | R | 0h | Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register. |

19.20 MCRC_RAW_DATAREGL1 Register (Offset = 78h) [reset = 0h]

MCRC_RAW_DATAREGL1 is shown in [Figure 19-20](#) and described in [Table 19-42](#).

Return to [Summary Table](#).

Channel 1 Raw Data Low Register

Table 19-41. MCRC_RAW_DATAREGL1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0078h |
| MCU_NAVSS0_MCRC | 2A26 4078h |

Figure 19-20. MCRC_RAW_DATAREGL1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-42. MCRC_RAW_DATAREGL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-0 | RAW_DATA1 | R | 0h | Channel 1 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data. |

19.21 MCRC_RAW_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

MCRC_RAW_DATAREGH1 is shown in [Figure 19-21](#) and described in [Table 19-44](#).

Return to [Summary Table](#).

Channel 1 Raw Data High Register

Table 19-43. MCRC_RAW_DATAREGH1 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 007Ch |
| MCU_NAVSS0_MCRC | 2A26 407Ch |

Figure 19-21. MCRC_RAW_DATAREGH1 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA1_47_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-44. MCRC_RAW_DATAREGH1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-0 | RAW_DATA1_47_32 | R | 0h | Channel 1 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data. |

19.22 MCRC_CRC_PCOUNT_REG2 Register (Offset = 80h) [reset = X]

MCRC_CRC_PCOUNT_REG2 is shown in [Figure 19-22](#) and described in [Table 19-46](#).

Return to [Summary Table](#).

CRC Pattern Counter Preload Register2

Table 19-45. MCRC_CRC_PCOUNT_REG2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0080h |
| MCU_NAVSS0_MCRC | 2A26 4080h |

Figure 19-22. MCRC_CRC_PCOUNT_REG2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | CRC_PAT_COUNT2 | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-46. MCRC_CRC_PCOUNT_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-20 | RESERVED | R/W | X | |
| 19-0 | CRC_PAT_COUNT2 | R/W | 0h | CRC Pattern Counter Preload Register 2 This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

19.23 MCRC_CRC_SCOUNT_REG2 Register (Offset = 84h) [reset = X]

MCRC_CRC_SCOUNT_REG2 is shown in [Figure 19-23](#) and described in [Table 19-48](#).

Return to [Summary Table](#).

CRC Sector Counter Preload Register2

Table 19-47. MCRC_CRC_SCOUNT_REG2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0084h |
| MCU_NAVSS0_MCRC | 2A26 4084h |

Figure 19-23. MCRC_CRC_SCOUNT_REG2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_SEC_COUNT2 | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-48. MCRC_CRC_SCOUNT_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | CRC_SEC_COUNT2 | R/W | 0h | Channel 2 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

19.24 MCRC_CRC_CURSEC_REG2 Register (Offset = 88h) [reset = X]

MCRC_CRC_CURSEC_REG2 is shown in [Figure 19-24](#) and described in [Table 19-50](#).

Return to [Summary Table](#).

CRC Current Sector Register 2

Table 19-49. MCRC_CRC_CURSEC_REG2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0088h |
| MCU_NAVSS0_MCRC | 2A26 4088h |

Figure 19-24. MCRC_CRC_CURSEC_REG2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_CURSEC2 | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-50. MCRC_CRC_CURSEC_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | CRC_CURSEC2 | R | 0h | <p>Channel 2 Current Sector ID Register.</p> <p>In AUTO mode, this register contains the current sector number of which the signature verification fails.</p> <p>The sector counter is a free running up counter.</p> <p>When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU.</p> <p>While it is frozen, it does not capture another erroneous sector number.</p> <p>When this condition happens, an overrun interrupt is generated instead.</p> <p>Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.</p> |

19.25 MCRC_CRC_WDTPLD2 Register (Offset = 8Ch) [reset = X]

MCRC_CRC_WDTPLD2 is shown in [Figure 19-25](#) and described in [Table 19-52](#).

Return to [Summary Table](#).

CRC channel 2 Watchdog Timeout Preload Register

Table 19-51. MCRC_CRC_WDTPLD2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 008Ch |
| MCU_NAVSS0_MCRC | 2A26 408Ch |

Figure 19-25. MCRC_CRC_WDTPLD2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_WDTPD2 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-52. MCRC_CRC_WDTPLD2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_WDTPLD2 | R/W | 0h | Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

19.26 MCRC_CRC_BCTOPLD2 Register (Offset = 90h) [reset = X]

MCRC_CRC_BCTOPLD2 is shown in [Figure 19-26](#) and described in [Table 19-54](#).

Return to [Summary Table](#).

CRC channel 2 Block Complete Timeout Preload Register

Table 19-53. MCRC_CRC_BCTOPLD2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0090h |
| MCU_NAVSS0_MCRC | 2A26 4090h |

Figure 19-26. MCRC_CRC_BCTOPLD2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_BCTOPLD2 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-54. MCRC_CRC_BCTOPLD2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_BCTOPLD2 | R/W | 0h | Channel 2 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated. |

19.27 MCRC_PSA_SIGREGL2 Register (Offset = A0h) [reset = 0h]

MCRC_PSA_SIGREGL2 is shown in [Figure 19-27](#) and described in [Table 19-56](#).

Return to [Summary Table](#).

Channel 2 PSA signature low register

Table 19-55. MCRC_PSA_SIGREGL2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00A0h |
| MCU_NAVSS0_MCRC | 2A26 40A0h |

Figure 19-27. MCRC_PSA_SIGREGL2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-56. MCRC_PSA_SIGREGL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---|
| 31-0 | PSASIG2 | R/W | 0h | Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register. |

19.28 MCRC_PSA_SIGREGH2 Register (Offset = A4h) [reset = 0h]

MCRC_PSA_SIGREGH2 is shown in [Figure 19-28](#) and described in [Table 19-58](#).

Return to [Summary Table](#).

Channel 2 PSA signature high register

Table 19-57. MCRC_PSA_SIGREGH2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00A4h |
| MCU_NAVSS0_MCRC | 2A26 40A4h |

Figure 19-28. MCRC_PSA_SIGREGH2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG2_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-58. MCRC_PSA_SIGREGH2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-0 | PSASIG2_63_32 | R/W | 0h | Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register. |

19.29 MCRC_CRC_REGL2 Register (Offset = A8h) [reset = 0h]

MCRC_CRC_REGL2 is shown in [Figure 19-29](#) and described in [Table 19-60](#).

Return to [Summary Table](#).

Channel 2 CRC value low register

Table 19-59. MCRC_CRC_REGL2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00A8h |
| MCU_NAVSS0_MCRC | 2A26 40A8h |

Figure 19-29. MCRC_CRC_REGL2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-60. MCRC_CRC_REGL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CRC2 | R/W | 0h | Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register. |

19.30 MCRC_CRC_REGH2 Register (Offset = ACh) [reset = 0h]

MCRC_CRC_REGH2 is shown in [Figure 19-30](#) and described in [Table 19-62](#).

Return to [Summary Table](#).

Channel 2 CRC value high register

Table 19-61. MCRC_CRC_REGH2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00ACh |
| MCU_NAVSS0_MCRC | 2A26 40ACh |

Figure 19-30. MCRC_CRC_REGH2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC2_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-62. MCRC_CRC_REGH2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | CRC2_63_32 | R/W | 0h | Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register. |

19.31 MCRC_PSA_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

MCRC_PSA_SECSIGREGL2 is shown in [Figure 19-31](#) and described in [Table 19-64](#).

Return to [Summary Table](#).

Channel 2 PSA sector signature low register

Table 19-63. MCRC_PSA_SECSIGREGL2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00B0h |
| MCU_NAVSS0_MCRC | 2A26 40B0h |

Figure 19-31. MCRC_PSA_SECSIGREGL2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-64. MCRC_PSA_SECSIGREGL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | PSASECSIG2 | R | 0h | Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register. |

19.32 MCRC_PSA_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

MCRC_PSA_SECSIGREGH2 is shown in [Figure 19-32](#) and described in [Table 19-66](#).

Return to [Summary Table](#).

Channel 2 PSA sector signature high register

Table 19-65. MCRC_PSA_SECSIGREGH2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00B4h |
| MCU_NAVSS0_MCRC | 2A26 40B4h |

Figure 19-32. MCRC_PSA_SECSIGREGH2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG2_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-66. MCRC_PSA_SECSIGREGH2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-0 | PSASECSIG2_63_32 | R | 0h | Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register. |

19.33 MCRC_RAW_DATAREGL2 Register (Offset = B8h) [reset = 0h]

MCRC_RAW_DATAREGL2 is shown in [Figure 19-33](#) and described in [Table 19-68](#).

Return to [Summary Table](#).

Channel 2 Raw Data Low Register

Table 19-67. MCRC_RAW_DATAREGL2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00B8h |
| MCU_NAVSS0_MCRC | 2A26 40B8h |

Figure 19-33. MCRC_RAW_DATAREGL2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-68. MCRC_RAW_DATAREGL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-0 | RAW_DATA2 | R | 0h | Channel 2 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data. |

19.34 MCRC_RAW_DATAREGH2 Register (Offset = BCh) [reset = 0h]

MCRC_RAW_DATAREGH2 is shown in [Figure 19-34](#) and described in [Table 19-70](#).

Return to [Summary Table](#).

Channel 2 Raw Data High Register

Table 19-69. MCRC_RAW_DATAREGH2 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00BCh |
| MCU_NAVSS0_MCRC | 2A26 40BCh |

Figure 19-34. MCRC_RAW_DATAREGH2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA2_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-70. MCRC_RAW_DATAREGH2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-0 | RAW_DATA2_63_32 | R | 0h | Channel 2 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data. |

19.35 MCRC_CRC_PCOUNT_REG3 Register (Offset = C0h) [reset = X]

MCRC_CRC_PCOUNT_REG3 is shown in [Figure 19-35](#) and described in [Table 19-72](#).

Return to [Summary Table](#).

CRC Pattern Counter Preload Register3

Table 19-71. MCRC_CRC_PCOUNT_REG3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00C0h |
| MCU_NAVSS0_MCRC | 2A26 40C0h |

Figure 19-35. MCRC_CRC_PCOUNT_REG3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | CRC_PAT_COUNT3 | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-72. MCRC_CRC_PCOUNT_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-20 | RESERVED | R/W | X | |
| 19-0 | CRC_PAT_COUNT3 | R/W | 0h | Channel 3 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

19.36 MCRC_CRC_SCOUNT_REG3 Register (Offset = C4h) [reset = X]

MCRC_CRC_SCOUNT_REG3 is shown in [Figure 19-36](#) and described in [Table 19-74](#).

Return to [Summary Table](#).

CRC Sector Counter Preload Register3

Table 19-73. MCRC_CRC_SCOUNT_REG3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00C4h |
| MCU_NAVSS0_MCRC | 2A26 40C4h |

Figure 19-36. MCRC_CRC_SCOUNT_REG3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_SEC_COUNT3 | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-74. MCRC_CRC_SCOUNT_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | CRC_SEC_COUNT3 | R/W | 0h | Channel 3 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

19.37 MCRC_CRC_CURSEC_REG3 Register (Offset = C8h) [reset = X]

MCRC_CRC_CURSEC_REG3 is shown in [Figure 19-37](#) and described in [Table 19-76](#).

Return to [Summary Table](#).

CRC Current Sector Register 3

Table 19-75. MCRC_CRC_CURSEC_REG3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00C8h |
| MCU_NAVSS0_MCRC | 2A26 40C8h |

Figure 19-37. MCRC_CRC_CURSEC_REG3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_CURSEC3 | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-76. MCRC_CRC_CURSEC_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | CRC_CURSEC3 | R | 0h | <p>Channel 3 Current Sector ID Register.</p> <p>In AUTO mode, this register contains the current sector number of which the signature verification fails.</p> <p>The sector counter is a free running up counter.</p> <p>When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU.</p> <p>While it is frozen, it does not capture another erroneous sector number.</p> <p>When this condition happens, an overrun interrupt is generated instead.</p> <p>Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.</p> |

19.38 MCRC_CRC_WDTPLD3 Register (Offset = CCh) [reset = X]

MCRC_CRC_WDTPLD3 is shown in [Figure 19-38](#) and described in [Table 19-78](#).

Return to [Summary Table](#).

CRC channel 3 Watchdog Timeout Preload Register

Table 19-77. MCRC_CRC_WDTPLD3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00CCh |
| MCU_NAVSS0_MCRC | 2A26 40CCh |

Figure 19-38. MCRC_CRC_WDTPLD3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_WDTPD3 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-78. MCRC_CRC_WDTPLD3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_WDTPLD3 | R/W | 0h | Channel 3 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

19.39 MCRC_CRC_BCTOPLD3 Register (Offset = D0h) [reset = X]

MCRC_CRC_BCTOPLD3 is shown in [Figure 19-39](#) and described in [Table 19-80](#).

Return to [Summary Table](#).

CRC channel 3 Block Complete Timeout Preload Register

Table 19-79. MCRC_CRC_BCTOPLD3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00D0h |
| MCU_NAVSS0_MCRC | 2A26 40D0h |

Figure 19-39. MCRC_CRC_BCTOPLD3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_BCTOPLD3 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-80. MCRC_CRC_BCTOPLD3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_BCTOPLD3 | R/W | 0h | Channel 3 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated. |

19.40 MCRC_PSA_SIGREGL3 Register (Offset = E0h) [reset = 0h]

MCRC_PSA_SIGREGL3 is shown in [Figure 19-40](#) and described in [Table 19-82](#).

Return to [Summary Table](#).

Channel 3 PSA signature low register

Table 19-81. MCRC_PSA_SIGREGL3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00E0h |
| MCU_NAVSS0_MCRC | 2A26 40E0h |

Figure 19-40. MCRC_PSA_SIGREGL3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-82. MCRC_PSA_SIGREGL3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|---|
| 31-0 | PSASIG3 | R/W | 0h | Channel 3 PSA Signature Low Register. This register contains the value stored at PSASIG3[31:0] register. |

19.41 MCRC_PSA_SIGREGH3 Register (Offset = E4h) [reset = 0h]

MCRC_PSA_SIGREGH3 is shown in [Figure 19-41](#) and described in [Table 19-84](#).

Return to [Summary Table](#).

Channel 3 PSA signature high register

Table 19-83. MCRC_PSA_SIGREGH3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00E4h |
| MCU_NAVSS0_MCRC | 2A26 40E4h |

Figure 19-41. MCRC_PSA_SIGREGH3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG3_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-84. MCRC_PSA_SIGREGH3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-0 | PSASIG3_63_32 | R/W | 0h | Channel 3 PSA Signature High Register. This register contains the value stored at PSASIG3[63:32] register. |

19.42 MCRC_CRC_REGL3 Register (Offset = E8h) [reset = 0h]

MCRC_CRC_REGL3 is shown in [Figure 19-42](#) and described in [Table 19-86](#).

Return to [Summary Table](#).

Channel 3 CRC value low register

Table 19-85. MCRC_CRC_REGL3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00E8h |
| MCU_NAVSS0_MCRC | 2A26 40E8h |

Figure 19-42. MCRC_CRC_REGL3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC3 | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-86. MCRC_CRC_REGL3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|---|
| 31-0 | CRC3 | R/W | 0h | Channel 3 CRC Value Low Register. This register contains the current known good signature value stored at CRC3[31:0] register. |

19.43 MCRC_CRC_REGH3 Register (Offset = ECh) [reset = 0h]

MCRC_CRC_REGH3 is shown in [Figure 19-43](#) and described in [Table 19-88](#).

Return to [Summary Table](#).

Channel 3 CRC value high register

Table 19-87. MCRC_CRC_REGH3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00ECh |
| MCU_NAVSS0_MCRC | 2A26 40ECh |

Figure 19-43. MCRC_CRC_REGH3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC3_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-88. MCRC_CRC_REGH3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | CRC3_63_32 | R/W | 0h | Channel 3 CRC Value High Register. This register contains the current known good signature value stored at CRC3[63:32] register. |

19.44 MCRC_PSA_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

MCRC_PSA_SECSIGREGL3 is shown in [Figure 19-44](#) and described in [Table 19-90](#).

Return to [Summary Table](#).

Channel 3 PSA sector signature low register

Table 19-89. MCRC_PSA_SECSIGREGL3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00F0h |
| MCU_NAVSS0_MCRC | 2A26 40F0h |

Figure 19-44. MCRC_PSA_SECSIGREGL3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-90. MCRC_PSA_SECSIGREGL3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|---|
| 31-0 | PSASECSIG3 | R | 0h | Channel 3 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG3[31:0] register. |

19.45 MCRC_PSA_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

MCRC_PSA_SECSIGREGH3 is shown in [Figure 19-45](#) and described in [Table 19-92](#).

Return to [Summary Table](#).

Channel 3 PSA sector signature high register

Table 19-91. MCRC_PSA_SECSIGREGH3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00F4h |
| MCU_NAVSS0_MCRC | 2A26 40F4h |

Figure 19-45. MCRC_PSA_SECSIGREGH3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG3_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-92. MCRC_PSA_SECSIGREGH3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-0 | PSASECSIG3_63_32 | R | 0h | Channel 3 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG3[63:32] register. |

19.46 MCRC_RAW_DATAREGL3 Register (Offset = F8h) [reset = 0h]

MCRC_RAW_DATAREGL3 is shown in [Figure 19-46](#) and described in [Table 19-94](#).

Return to [Summary Table](#).

Channel 3 Raw Data Low Register

Table 19-93. MCRC_RAW_DATAREGL3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00F8h |
| MCU_NAVSS0_MCRC | 2A26 40F8h |

Figure 19-46. MCRC_RAW_DATAREGL3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-94. MCRC_RAW_DATAREGL3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-0 | RAW_DATA3 | R | 0h | Channel 3 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data. |

19.47 MCRC_RAW_DATAREGH3 Register (Offset = FCh) [reset = 0h]

MCRC_RAW_DATAREGH3 is shown in [Figure 19-47](#) and described in [Table 19-96](#).

Return to [Summary Table](#).

Channel 3 Raw Data High Register

Table 19-95. MCRC_RAW_DATAREGH3 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 00FCh |
| MCU_NAVSS0_MCRC | 2A26 40FCh |

Figure 19-47. MCRC_RAW_DATAREGH3 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA3_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-96. MCRC_RAW_DATAREGH3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-0 | RAW_DATA3_63_32 | R | 0h | Channel 3 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data. |

19.48 MCRC_CRC_PCOUNT_REG4 Register (Offset = 100h) [reset = X]

MCRC_CRC_PCOUNT_REG4 is shown in [Figure 19-48](#) and described in [Table 19-98](#).

Return to [Summary Table](#).

CRC Pattern Counter Preload Register4

Table 19-97. MCRC_CRC_PCOUNT_REG4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0100h |
| MCU_NAVSS0_MCRC | 2A26 4100h |

Figure 19-48. MCRC_CRC_PCOUNT_REG4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | CRC_PAT_COUNT4 | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-98. MCRC_CRC_PCOUNT_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|---|
| 31-20 | RESERVED | R/W | X | |
| 19-0 | CRC_PAT_COUNT4 | R/W | 0h | Channel 4 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

19.49 MCRC_CRC_SCOUNT_REG4 Register (Offset = 104h) [reset = X]

MCRC_CRC_SCOUNT_REG4 is shown in [Figure 19-49](#) and described in [Table 19-100](#).

Return to [Summary Table](#).

CRC Sector Counter Preload Register4

Table 19-99. MCRC_CRC_SCOUNT_REG4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0104h |
| MCU_NAVSS0_MCRC | 2A26 4104h |

Figure 19-49. MCRC_CRC_SCOUNT_REG4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_SEC_COUNT4 | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-100. MCRC_CRC_SCOUNT_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------------|------|-------|--|
| 31-16 | RESERVED | R/W | X | |
| 15-0 | CRC_SEC_COUNT4 | R/W | 0h | Channel 4 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

19.50 MCRC_CRC_CURSEC_REG4 Register (Offset = 31F70108h) [reset = X]

MCRC_CRC_CURSEC_REG4 is shown in [Figure 19-50](#) and described in [Table 19-102](#).

Return to [Summary Table](#).

CRC Current Sector Register 4

**Table 19-101. MCRC_CRC_CURSEC_REG4
Instances**

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0108h |
| MCU_NAVSS0_MCRC | 2A26 4108h |

Figure 19-50. MCRC_CRC_CURSEC_REG4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | | | | | | CRC_CURSEC4 | | | | | | | | | | | | | | | |
| R-X | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-102. MCRC_CRC_CURSEC_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|--|
| 31-16 | RESERVED | R | X | |
| 15-0 | CRC_CURSEC4 | R | 0h | <p>In AUTO mode, this register contains the current sector number of which the signature verification fails.</p> <p>The sector counter is a free running up counter.</p> <p>When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU.</p> <p>While it is frozen, it does not capture another erroneous sector number.</p> <p>When this condition happens, an overrun interrupt is generated instead.</p> <p>Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number.</p> <p>In Semi-CPU mode, this register is used to indicate the sector number for which the compression complete has last happened.</p> |

19.51 MCRC_CRC_WDTPLD4 Register (Offset = 10Ch) [reset = X]

MCRC_CRC_WDTPLD4 is shown in [Figure 19-51](#) and described in [Table 19-104](#).

Return to [Summary Table](#).

CRC channel 4 Watchdog Timeout Preload Register

Table 19-103. MCRC_CRC_WDTPLD4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 010Ch |
| MCU_NAVSS0_MCRC | 2A26 410Ch |

Figure 19-51. MCRC_CRC_WDTPLD4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_WDTPD4 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-104. MCRC_CRC_WDTPLD4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_WDTPLD4 | R/W | 0h | This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

19.52 MCRC_CRC_BCTOPLD4 Register (Offset = 110h) [reset = X]

MCRC_CRC_BCTOPLD4 is shown in [Figure 19-52](#) and described in [Table 19-106](#).

Return to [Summary Table](#).

CRC channel 4 Block Complete Timeout Preload Register

Table 19-105. MCRC_CRC_BCTOPLD4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0110h |
| MCU_NAVSS0_MCRC | 2A26 4110h |

Figure 19-52. MCRC_CRC_BCTOPLD4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|--------------|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | CRC_BCTOPLD4 | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-X | | | | | | | | R/W-0h | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-106. MCRC_CRC_BCTOPLD4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| 31-24 | RESERVED | R/W | X | |
| 23-0 | CRC_BCTOPLD4 | R/W | 0h | This register contains the number of clock cycles within which the CRC of an entire block needs to complete before a timeout interrupt is generated. |

19.53 MCRC_PSA_SIGREGL4 Register (Offset = 120h) [reset = 0h]

MCRC_PSA_SIGREGL4 is shown in [Figure 19-53](#) and described in [Table 19-108](#).

Return to [Summary Table](#).

Channel 4 PSA signature low register

Table 19-107. MCRC_PSA_SIGREGL4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0120h |
| MCU_NAVSS0_MCRC | 2A26 4120h |

Figure 19-53. MCRC_PSA_SIGREGL4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-108. MCRC_PSA_SIGREGL4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | PSASIG4 | R/W | 0h | This register contains the value stored at PSASIG4[31:0] register. |

19.54 MCRC_PSA_SIGREGH4 Register (Offset = 124h) [reset = 0h]

MCRC_PSA_SIGREGH4 is shown in [Figure 19-54](#) and described in [Table 19-110](#).

Return to [Summary Table](#).

Channel 4 PSA signature high register

Table 19-109. MCRC_PSA_SIGREGH4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0124h |
| MCU_NAVSS0_MCRC | 2A26 4124h |

Figure 19-54. MCRC_PSA_SIGREGH4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASIG4_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-110. MCRC_PSA_SIGREGH4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------|------|-------|---|
| 31-0 | PSASIG4_63_32 | R/W | 0h | This register contains the value stored at PSASIG4[63:32] register. |

19.55 MCRC_CRC_REGL4 Register (Offset = 31F70128h) [reset = 0h]

MCRC_CRC_REGL4 is shown in [Figure 19-55](#) and described in [Table 19-112](#).

Return to [Summary Table](#).

Channel 4 CRC value low register

Table 19-111. MCRC_CRC_REGL4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0128h |
| MCU_NAVSS0_MCRC | 2A26 4128h |

Figure 19-55. MCRC_CRC_REGL4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-112. MCRC_CRC_REGL4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-----------------------------------|
| 31-0 | CRC4 | R/W | 0h | Channel 4 CRC Value Low Register. |

19.56 MCRC_CRC_REGH4 Register (Offset = 12Ch) [reset = 0h]

MCRC_CRC_REGH4 is shown in [Figure 19-56](#) and described in [Table 19-114](#).

Return to [Summary Table](#).

Channel 4 CRC value high register

Table 19-113. MCRC_CRC_REGH4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 012Ch |
| MCU_NAVSS0_MCRC | 2A26 412Ch |

Figure 19-56. MCRC_CRC_REGH4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC4_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-114. MCRC_CRC_REGH4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|------------------------------------|
| 31-0 | CRC4_63_32 | R/W | 0h | Channel 4 CRC Value High Register. |

19.57 MCRC_PSA_SECSIGREGL4 Register (Offset = 31F70130h) [reset = 0h]

MCRC_PSA_SECSIGREGL4 is shown in [Figure 19-57](#) and described in [Table 19-116](#).

Return to [Summary Table](#).

Channel 4 PSA sector signature low register

Table 19-115. MCRC_PSA_SECSIGREGL4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0130h |
| MCU_NAVSS0_MCRC | 2A26 4130h |

Figure 19-57. MCRC_PSA_SECSIGREGL4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-116. MCRC_PSA_SECSIGREGL4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------|------|-------|--|
| 31-0 | PSASECSIG4 | R | 0h | Channel 4 PSA Sector Signature Low Register. |

19.58 MCRC_PSA_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

MCRC_PSA_SECSIGREGH4 is shown in [Figure 19-58](#) and described in [Table 19-118](#).

Return to [Summary Table](#).

Channel 4 PSA sector signature high register

Table 19-117. MCRC_PSA_SECSIGREGH4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0134h |
| MCU_NAVSS0_MCRC | 2A26 4134h |

Figure 19-58. MCRC_PSA_SECSIGREGH4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PSASECSIG4_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-118. MCRC_PSA_SECSIGREGH4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|---|
| 31-0 | PSASECSIG4_63_32 | R | 0h | Channel 4 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG4[63:32] register. |

19.59 MCRC_RAW_DATAREGL4 Register (Offset = 138h) [reset = 0h]

MCRC_RAW_DATAREGL4 is shown in [Figure 19-59](#) and described in [Table 19-120](#).

Return to [Summary Table](#).

Channel 4 Raw Data Low Register

Table 19-119. MCRC_RAW_DATAREGL4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0138h |
| MCU_NAVSS0_MCRC | 2A26 4138h |

Figure 19-59. MCRC_RAW_DATAREGL4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-120. MCRC_RAW_DATAREGL4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------|------|-------|---|
| 31-0 | RAW_DATA4 | R | 0h | Channel 4 Raw Data Low Register. This register contains bit 31:0 of the uncompressed raw data. |

19.60 MCRC_RAW_DATAREGH4 Register (Offset = 31F7013Ch) [reset = 0h]

MCRC_RAW_DATAREGH4 is shown in [Figure 19-60](#) and described in [Table 19-122](#).

Return to [Summary Table](#).

Channel 4 Raw Data High Register

Table 19-121. MCRC_RAW_DATAREGH4 Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 013Ch |
| MCU_NAVSS0_MCRC | 2A26 413Ch |

Figure 19-60. MCRC_RAW_DATAREGH4 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAW_DATA4_63_32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 19-122. MCRC_RAW_DATAREGH4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-----------------|------|-------|---|
| 31-0 | RAW_DATA4_63_32 | R | 0h | Channel 4 Raw Data High Register. This register contains bit 63:32 of the uncompressed raw data. |

19.61 MCRC_BUS_SEL Register (Offset = 140h) [reset = X]

MCRC_BUS_SEL is shown in [Figure 19-61](#) and described in [Table 19-124](#).

Return to [Summary Table](#).

Data bus tracing selection

Table 19-123. MCRC_BUS_SEL Instances

| Instance | Physical Address |
|-----------------|------------------|
| NAVSS0_MCRC | 31F7 0140h |
| MCU_NAVSS0_MCRC | 2A26 4140h |

Figure 19-61. MCRC_BUS_SEL Register

| | | | | | | | |
|----------|----|----|----|----|--------|---------|---------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R/W-X | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | MEN | DTC_MEN | ITC_MEN |
| R/W-X | | | | | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R/W = Read/Write; -n = value after reset

Table 19-124. MCRC_BUS_SEL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-3 | RESERVED | R/W | X | |
| 2 | MEN | R/W | 1h | Enable/disables the tracing of VBUSM 0: Tracing of VBUSM master bus has been disabled 1: Tracing of VBUSM master bus has been enabled |
| 1 | DTC_MEN | R/W | 1h | Enable/disables the tracing of data TCM 0: Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled 1: Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled |
| 0 | ITC_MEN | R/W | 1h | Enable/disables the tracing of instruction TCM 0: Tracing of ITCM bus has been disabled 1: Tracing of ITCM bus has been enabled Please refer the description of CPU Data trace at page 1-21 for the priority between different data buses. |

19.62 MCRC_I0_PSA_SIGREG1_CPY_Y Register (Offset = 200h + formula) [reset = 0h]

MCRC_I0_PSA_SIGREG1_CPY_Y is shown in [Figure 19-62](#) and described in [Table 19-126](#).

Return to [Summary Table](#).

Channel 1 PSA signature block region

Offset = 200h + (y * 4h); where y = 0h to 1Fh

**Table 19-125. MCRC_I0_PSA_SIGREG1_CPY_Y
Instances**

| Instance | Physical Address |
|-----------------|----------------------|
| NAVSS0_MCRC | 31F7 0200h + formula |
| MCU_NAVSS0_MCRC | 2A26 4200h + formula |

Figure 19-62. MCRC_I0_PSA_SIGREG1_CPY_Y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I0_PSA_SIG1_CPY0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 19-126. MCRC_I0_PSA_SIGREG1_CPY_Y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-0 | I0_PSA_SIG1_CPY0 | W | 0h | This register is a 128 byte block copy of the PSASIG1 register for DMA destination, it is write only, the result can be found in the PSASIG1 register. |

19.63 MCRC_I0_PSA_SIGREG2_CPY_Y Register (Offset = 280h + formula) [reset = 0h]

MCRC_I0_PSA_SIGREG2_CPY_Y is shown in [Figure 19-63](#) and described in [Table 19-128](#).

Return to [Summary Table](#).

Channel 2 PSA signature block region

Offset = 280h + (y * 4h); where y = 0h to 1Fh

Table 19-127. MCRC_I0_PSA_SIGREG2_CPY_Y Instances

| Instance | Physical Address |
|-----------------|----------------------|
| NAVSS0_MCRC | 31F7 0280h + formula |
| MCU_NAVSS0_MCRC | 2A26 4280h + formula |

Figure 19-63. MCRC_I0_PSA_SIGREG2_CPY_Y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I0_PSA_SIG2_CPY0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 19-128. MCRC_I0_PSA_SIGREG2_CPY_Y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-0 | I0_PSA_SIG2_CPY0 | W | 0h | This register is a 128 byte block copy of the PSASIG2 register for DMA destination, it is write only, the result can be found in the PSASIG2 register. |

19.64 MCRC_I0_PSA_SIGREG3_CPY_Y Register (Offset = 300h + formula) [reset = 0h]

MCRC_I0_PSA_SIGREG3_CPY_Y is shown in [Figure 19-64](#) and described in [Table 19-130](#).

Return to [Summary Table](#).

Channel 3 PSA signature block region

Offset = 300h + (y * 4h); where y = 0h to 1Fh

**Table 19-129. MCRC_I0_PSA_SIGREG3_CPY_Y
Instances**

| Instance | Physical Address |
|-----------------|----------------------|
| NAVSS0_MCRC | 31F7 0300h + formula |
| MCU_NAVSS0_MCRC | 2A26 4300h + formula |

Figure 19-64. MCRC_I0_PSA_SIGREG3_CPY_Y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I0_PSA_SIG3_CPY0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 19-130. MCRC_I0_PSA_SIGREG3_CPY_Y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-0 | I0_PSA_SIG3_CPY0 | W | 0h | This register is a 128 byte block copy of the PSASIG3 register for DMA destination, it is write only, the result can be found in the PSASIG3 register. |

19.65 MCRC_I0_PSA_SIGREG4_CPY_Y Register (Offset = 380h + formula) [reset = 0h]

MCRC_I0_PSA_SIGREG4_CPY_Y is shown in [Figure 19-65](#) and described in [Table 19-132](#).

Return to [Summary Table](#).

Channel 4 PSA signature block region

Offset = 380h + (y * 4h); where y = 0h to 1Fh

Table 19-131. MCRC_I0_PSA_SIGREG4_CPY_Y Instances

| Instance | Physical Address |
|-----------------|----------------------|
| NAVSS0_MCRC | 31F7 0380h + formula |
| MCU_NAVSS0_MCRC | 2A26 4380h + formula |

Figure 19-65. MCRC_I0_PSA_SIGREG4_CPY_Y Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I0_PSA_SIG4_CPY0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: W = Write Only; -n = value after reset

Table 19-132. MCRC_I0_PSA_SIGREG4_CPY_Y Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|------------------|------|-------|--|
| 31-0 | I0_PSA_SIG4_CPY0 | W | 0h | This register is a 128 byte block copy of the PSASIG4 register for DMA destination, it is write only, the result can be found in the PSASIG4 register. |

20 ECC Aggregator Registers

Table 20-1 lists the memory-mapped registers for an ECC Aggregator (ECC_AGGR). All register offset addresses not listed in Table 20-1 should be considered as reserved locations and the register contents should not be modified.

Note

This section shows all possible registers and bits which an ECC aggregator may have. For specific physical addresses and particular ECC aggregator registers associated with each ECC protected module or subsystem, see the corresponding *Registers* section.

Table 20-1. ECC_AGGR Registers

| Offset | Acronym | Register Name |
|--------------------------------------|---|---|
| 0h | ECC_REV | Aggregator Revision Register |
| 8h | ECC_VECTOR | ECC Vector Register |
| Ch | ECC_STAT | Misc Status Register |
| ECC Wrapper Registers | | |
| 10h | ECC_WRAP_REV | ECC Wrapper Revision Register |
| 14h | ECC_CTRL | ECC RAM Control Register |
| 18h | ECC_ERR_CTRL1 | ECC RAM Error Control 1 Register |
| 1Ch | ECC_ERR_CTRL2 | ECC RAM Error Control 2 Register |
| 20h | ECC_ERR_STAT1 | ECC RAM Error Status 1 Register |
| 24h | ECC_ERR_STAT2 | ECC RAM Error Status 2 Register |
| 28h | ECC_ERR_STAT3 | ECC RAM Error Status 3 Register |
| Interconnect ECC Component Registers | | |
| 10h | ECC_CBASS_REV | Interconnect ECC Component Revision Register |
| 14h | ECC_CBASS_CTRL | Interconnect ECC Component Control Register |
| 18h | ECC_CBASS_ERR_CTRL1 | Interconnect ECC Component Error Control 1 Register |
| 1Ch | ECC_CBASS_ERR_CTRL2 | Interconnect ECC Component Error Control 2 Register |
| 20h | ECC_CBASS_ERR_STAT1 | Interconnect ECC Component Error Status 1 Register |
| 24h | ECC_CBASS_ERR_STAT2 | Interconnect ECC Component Error Status 2 Register |
| 3Ch | ECC_SEC_EOI_REG | EOI Register for Correctable Error |
| 40h | ECC_SEC_STATUS_REG0 | Interrupt Status Register 0 for Correctable Error |
| 44h | ECC_SEC_STATUS_REG1 | Interrupt Status Register 1 for Correctable Error |
| 48h | ECC_SEC_STATUS_REG2 | Interrupt Status Register 2 for Correctable Error |
| 4Ch | ECC_SEC_STATUS_REG3 | Interrupt Status Register 3 for Correctable Error |
| 50h | ECC_SEC_STATUS_REG4 | Interrupt Status Register 4 for Correctable Error |
| 54h | ECC_SEC_STATUS_REG5 | Interrupt Status Register 5 for Correctable Error |
| 58h | ECC_SEC_STATUS_REG6 | Interrupt Status Register 6 for Correctable Error |
| 5Ch | ECC_SEC_STATUS_REG7 | Interrupt Status Register 7 for Correctable Error |
| 80h | ECC_SEC_ENABLE_SET_REG0 | Interrupt Enable Register 0 for Correctable Error |
| 84h | ECC_SEC_ENABLE_SET_REG1 | Interrupt Enable Register 1 for Correctable Error |
| 88h | ECC_SEC_ENABLE_SET_REG2 | Interrupt Enable Register 2 for Correctable Error |
| 8Ch | ECC_SEC_ENABLE_SET_REG3 | Interrupt Enable Register 3 for Correctable Error |
| 90h | ECC_SEC_ENABLE_SET_REG4 | Interrupt Enable Register 4 for Correctable Error |
| 94h | ECC_SEC_ENABLE_SET_REG5 | Interrupt Enable Register 5 for Correctable Error |
| 98h | ECC_SEC_ENABLE_SET_REG6 | Interrupt Enable Register 6 for Correctable Error |
| 9Ch | ECC_SEC_ENABLE_SET_REG7 | Interrupt Enable Register 7 for Correctable Error |
| C0h | ECC_SEC_ENABLE_CLR_REG0 | Interrupt Disable Register 0 for Correctable Error |

Table 20-1. ECC_AGGR Registers (continued)

| Offset | Acronym | Register Name |
|--------|---|--|
| C4h | ECC_SEC_ENABLE_CLR_REG1 | Interrupt Disable Register 1 for Correctable Error |
| C8h | ECC_SEC_ENABLE_CLR_REG2 | Interrupt Disable Register 2 for Correctable Error |
| CCh | ECC_SEC_ENABLE_CLR_REG3 | Interrupt Disable Register 3 for Correctable Error |
| D0h | ECC_SEC_ENABLE_CLR_REG4 | Interrupt Disable Register 4 for Correctable Error |
| D4h | ECC_SEC_ENABLE_CLR_REG5 | Interrupt Disable Register 5 for Correctable Error |
| D8h | ECC_SEC_ENABLE_CLR_REG6 | Interrupt Disable Register 6 for Correctable Error |
| DCh | ECC_SEC_ENABLE_CLR_REG7 | Interrupt Disable Register 7 for Correctable Error |
| 13Ch | ECC_DED_EOI_REG | EOI Register for Non-correctable Error |
| 140h | ECC_DED_STATUS_REG0 | Interrupt Status Register 0 for Non-correctable Error |
| 144h | ECC_DED_STATUS_REG1 | Interrupt Status Register 1 for Non-correctable Error |
| 148h | ECC_DED_STATUS_REG2 | Interrupt Status Register 2 for Non-correctable Error |
| 14Ch | ECC_DED_STATUS_REG3 | Interrupt Status Register 3 for Non-correctable Error |
| 150h | ECC_DED_STATUS_REG4 | Interrupt Status Register 4 for Non-correctable Error |
| 154h | ECC_DED_STATUS_REG5 | Interrupt Status Register 5 for Non-correctable Error |
| 158h | ECC_DED_STATUS_REG6 | Interrupt Status Register 6 for Non-correctable Error |
| 15Ch | ECC_DED_STATUS_REG7 | Interrupt Status Register 7 for Non-correctable Error |
| 180h | ECC_DED_ENABLE_SET_REG0 | Interrupt Enable Register 0 for Non-correctable Error |
| 184h | ECC_DED_ENABLE_SET_REG1 | Interrupt Enable Register 1 for Non-correctable Error |
| 188h | ECC_DED_ENABLE_SET_REG2 | Interrupt Enable Register 2 for Non-correctable Error |
| 18Ch | ECC_DED_ENABLE_SET_REG3 | Interrupt Enable Register 3 for Non-correctable Error |
| 190h | ECC_DED_ENABLE_SET_REG4 | Interrupt Enable Register 4 for Non-correctable Error |
| 194h | ECC_DED_ENABLE_SET_REG5 | Interrupt Enable Register 5 for Non-correctable Error |
| 198h | ECC_DED_ENABLE_SET_REG6 | Interrupt Enable Register 6 for Non-correctable Error |
| 19Ch | ECC_DED_ENABLE_SET_REG7 | Interrupt Enable Register 7 for Non-correctable Error |
| 1C0h | ECC_DED_ENABLE_CLR_REG0 | Interrupt Disable Register 0 for Non-correctable Error |
| 1C4h | ECC_DED_ENABLE_CLR_REG1 | Interrupt Disable Register 1 for Non-correctable Error |
| 1C8h | ECC_DED_ENABLE_CLR_REG2 | Interrupt Disable Register 2 for Non-correctable Error |
| 1CCh | ECC_DED_ENABLE_CLR_REG3 | Interrupt Disable Register 3 for Non-correctable Error |
| 1D0h | ECC_DED_ENABLE_CLR_REG4 | Interrupt Disable Register 4 for Non-correctable Error |
| 1D4h | ECC_DED_ENABLE_CLR_REG5 | Interrupt Disable Register 5 for Non-correctable Error |
| 1D8h | ECC_DED_ENABLE_CLR_REG6 | Interrupt Disable Register 6 for Non-correctable Error |
| 1DCh | ECC_DED_ENABLE_CLR_REG7 | Interrupt Disable Register 7 for Non-correctable Error |
| 200h | ECC_AGGR_ENABLE_SET | Aggregator Interrupt Enable Register |
| 204h | ECC_AGGR_ENABLE_CLR | Aggregator Interrupt Disable Register |
| 208h | ECC_AGGR_STATUS_SET | Aggregator Interrupt Status Set Register |
| 20Ch | ECC_AGGR_STATUS_CLR | Aggregator Interrupt Status Clear Register |

20.1 ECC_REV Register (Offset = 0h) [reset = 66A0A600h]

ECC_REV is shown in [Figure 20-1](#) and described in [Table 20-2](#).

Return to [Summary Table](#).

Aggregator Revision Register

Revision parameters.

Figure 20-1. ECC_REV Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-66A0A600h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 20-2. ECC_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-----------|-------------------|
| 31-0 | REV | R | 66A0A600h | TI internal data. |

20.2 ECC_VECTOR Register (Offset = 8h) [reset = 0h]

ECC_VECTOR is shown in [Figure 20-2](#) and described in [Table 20-3](#).

Return to [Summary Table](#).

ECC Vector Register

Figure 20-2. ECC_VECTOR Register

| | | | | | | | |
|------------------|----------|----|----|----|------------|----|---------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | RD_SVBUS_DONE |
| R-0h | | | | | | | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD_SVBUS_ADDRESS | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RD_SVBUS | RESERVED | | | | ECC_VECTOR | | |
| R/W1S-0h | R-0h | | | | R/W-0h | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_VECTOR | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-3. ECC_VECTOR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|--|
| 31-25 | RESERVED | R | 0 | Reserved |
| 24 | RD_SVBUS_DONE | R/W1C | 0h | Status to indicate if read on the ECC serial interface is complete. Write of any value clears this bit. 0h - Read not complete 1h - Read complete |
| 23-16 | RD_SVBUS_ADDRESS | R/W | 0h | Read Address. Can be any of the registers (0x10 - 0x24). |
| 15 | RD_SVBUS | R/W1S | 0h | Read Trigger. Write 1h to trigger a read on the ECC serial interface. Note NOTE: In normal operation (that is, in ECC mode), this bit is 1h only for a single cycle and thus cannot be read back. |
| 14-11 | RESERVED | R | 0 | Reserved |
| 10-0 | ECC_VECTOR | R/W | 0h | ECC endpoint ID. Value written to select which ECC endpoint to control or read status from. |

20.3 ECC_STAT Register (Offset = Ch) [reset = X]

ECC_STAT is shown in [Figure 20-3](#) and described in [Table 20-4](#).

Return to [Summary Table](#).

Misc Status Register

Figure 20-3. ECC_STAT Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | | | | | NUM_RAMs | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | R-Xh | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 20-4. ECC_STAT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-11 | RESERVED | R | 0 | Reserved |
| 10-0 | NUM_RAMs | R | Xh | Indicates the number of ECC endpoints serviced by the ECC aggregator. |

20.4 ECC_WRAP_REV Register (Offset = 10h) [reset = 66A49A02h]

ECC_WRAP_REV is shown in [Figure 20-4](#) and described in [Table 20-5](#).

Return to [Summary Table](#).

ECC Wrapper Revision Register

Revision parameters.

Figure 20-4. ECC_WRAP_REV Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| REV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-66A49A02h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 20-5. ECC_WRAP_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-----------|-------------------|
| 31-0 | REV | R | 66A49A02h | TI internal data. |

20.5 ECC_CTRL Register (Offset = 14h) [reset = 00000187h]

ECC_CTRL is shown in [Figure 20-5](#) and described in [Table 20-6](#).

Return to [Summary Table](#).

ECC RAM Control Register

Figure 20-5. ECC_CTRL Register

| | | | | | | | |
|------------------|------------|-------------|-----------|-----------|------------|-----------|-------------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | CHECK_SVBU S_TIMEOUT |
| R-0h | | | | | | | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHECK_PARIT Y | ERROR_ONCE | FORCE_N_ROW | FORCE_DED | FORCE_SEC | ENABLE_RMW | ECC_CHECK | ECC_ENABLE |
| R/W-1h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | R/W-1h | R/W-1h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 20-6. ECC_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------------------|------|-------|---|
| 31-9 | RESERVED | R | 0 | Reserved |
| 8 | CHECK_SVBUS_TIMEOUT | R/W | 1h | Enable ECC serial interface timeout mechanism 0h - Timeout mechanism disabled 1h - Timeout mechanism enabled |
| 7 | CHECK_PARITY | R/W | 1h | Enables parity checking on internal data 0h - Parity checking disabled 1h - Parity checking enabled |
| 6 | ERROR_ONCE | R/W | 0h | Force error only once. If this bit is set to 1h, the FORCE_SEC/FORCE_DED injects an error to the specified row only once. The FORCE_SEC bit is cleared the cycle after the error is generated. For double-bit errors, the FORCE_DED bit is cleared the cycle following the double-bit error. Any subsequent reads do not force an error. |
| 5 | FORCE_N_ROW | R/W | 0h | Force error on any RAM read Force single or double-bit error on the next RAM access. For write through mode this applies to writes as well as reads. |
| 4 | FORCE_DED | R/W | 0h | Force double-bit error. Cleared the cycle following the error if ERROR_ONCE is 1h. For write through mode this applies to writes as well as reads. |
| 3 | FORCE_SEC | R/W | 0h | Force single-bit error. Cleared the cycle following the error if ERROR_ONCE is 1h. For write through mode this applies to writes as well as reads. |

Table 20-6. ECC_CTRL Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|--|
| 2 | ENABLE_RMW | R/W | 1h | <p>Enable read-modify-write on partial word writes.</p> <p>0h - Read-modify-write disabled</p> <p>1h - Read-modify-write enabled</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: If disabled, ECC detection and correction does no longer work and if re-enabled the RAM contents must all be rewritten to correct ECC codes. The reset value of this bit is 0h in inject only mode and 1h in ECC mode.</p> <hr/> |
| 1 | ECC_CHECK | R/W | 1h | <p>Enable ECC check.</p> <p>0h - ECC check disabled</p> <p>1h - ECC check enabled</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: ECC is completely bypassed if both ECC_ENABLE and ECC_CHECK are 0h. The reset value of this bit is 0h in inject only mode and 1h in ECC mode.</p> <hr/> |
| 0 | ECC_ENABLE | R/W | 1h | <p>Enable ECC generation.</p> <p>0h - ECC generation disabled</p> <p>1h - ECC generation enabled</p> |

20.6 ECC_ERR_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC_ERR_CTRL1 is shown in [Figure 20-6](#) and described in [Table 20-7](#).

Return to [Summary Table](#).

ECC RAM Error Control 1 Register

Figure 20-6. ECC_ERR_CTRL1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ECC_ROW | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 20-7. ECC_ERR_CTRL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | ECC_ROW | R/W | 0h | Row address where single or double-bit error needs to be applied. This is ignored if ECC_CTRL[5] FORCE_N_ROW bit is set to 1h. |

20.7 ECC_ERR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC_ERR_CTRL2 is shown in [Figure 20-7](#) and described in [Table 20-8](#).

Return to [Summary Table](#).

ECC RAM Error Control 2 Register

Figure 20-7. ECC_ERR_CTRL2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| ECC_BIT2 | | | | | | | | | | | | | | | | ECC_BIT1 | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | | |

LEGEND: R/W = Read/Write; -n = value after reset

Table 20-8. ECC_ERR_CTRL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| 31-16 | ECC_BIT2 | R/W | 0h | Data bit that needs to be flipped if double-bit error has to be forced. The ECC_CTRL[4] FORCE_DED bit must be set to 1h for these values to take affect. |
| 15-0 | ECC_BIT1 | R/W | 0h | Data bit that needs to be flipped if single-bit error has to be forced. The ECC_CTRL[3] FORCE_SEC bit must be set to 1h for these values to take affect. |

20.8 ECC_ERR_STAT1 Register (Offset = 20h) [reset = 0h]

ECC_ERR_STAT1 is shown in [Figure 20-8](#) and described in [Table 20-9](#).

Return to [Summary Table](#).

ECC RAM Error Status 1 Register

Figure 20-8. ECC_ERR_STAT1 Register

| | | | | | | | |
|------------------|----------------|----|---------------|-------------|----|-------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_BIT1 | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_BIT1 | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLR_CTRL_REG_ERR | CLR_PARITY_ERR | | CLR_ECC_OTHER | CLR_ECC_DED | | CLR_ECC_SEC | |
| R/W1C-0h | R/W-0h | | R/W1C-0h | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CTR_REG_ERR | PARITY_ERR | | ECC_OTHER | ECC_DED | | ECC_SEC | |
| R/W1S-0h | R/W1S-0h | | R/W1S-0h | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-9. ECC_ERR_STAT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|-------|-------|---|
| 31-16 | ECC_BIT1 | R | 0h | Indicates the bit position in the RAM data that is in error. For example, a value of 1h indicates that bit [1] in the RAM data is in error. This is valid only for single-bit errors. Note NOTE: Not used in inject only mode. Always read as 0h. |
| 15 | CLR_CTRL_REG_ERR | R/W1C | 0h | Clear the CTR_REG_ERR bit. A write of 1h clears this bit and the CTR_REG_ERR bit, but if the redundancy protected bits in the ECC_CTRL register have not been written to a known state to correct the error, this flag is immediately set again. |
| 14-13 | CLR_PARITY_ERR | R/W | 0h | A write of a non-zero value to this field decrements the CLR_ECC_DED and ECC_DED fields by that value. If the value written is less than the current one, the non-correctable interrupt (ECC_DED_INT) stays asserted. If the value to decrement is more than the current value, the result is 0. 0h - No parity errors have occurred 1h - 1 parity error has occurred 2h - 2 parity errors have occurred 3h - 3 or more parity errors have occurred |
| 12 | CLR_ECC_OTHER | R/W1C | 0h | Clear other error status. 1h indicates a successive single-bit error. Writing 1h clears the status bit. |

Table 20-9. ECC_ERR_STAT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-------|-------------|-------|-------|--|
| 11-10 | CLR_ECC_DED | R/W | 0h | <p>A write of a non-zero value to this field decrements it and the ECC_DED field by that value. If the value written is less than the current one, the non-correctable interrupt (ECC_DED_INT) stays asserted. If the value to decrement is more than the current value, the result is 0.</p> <p>0h - No double-bit errors have occurred 1h - 1 double-bit has error occurred 2h - 2 double-bit have errors occurred 3h - 3 or more double-bit errors have occurred</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: Not used in inject only mode. Always read as 0h.</p> <hr/> |
| 9-8 | CLR_ECC_SEC | R/W | 0h | <p>A write of a non-zero value to this field decrements it and the ECC_SEC field by that value. If the value written is less than the current one, the correctable interrupt (ECC_SEC_INT) stays asserted. If the value to decrement is more than the current value, the result is 0.</p> <p>0h - No single-bit errors have occurred 1h - 1 single-bit has occurred 2h - 2 single-bit have occurred 3h - 3 or more single-bit have occurred</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: Not used in inject only mode. Always read as 0h.</p> <hr/> |
| 7 | CTR_REG_ERR | R/W1S | 0h | <p>Indicates that a redundancy protected bit in the ECC_CTRL register has been flipped. This means that the redundancy logic have detected a state where not all values are the same and has defaulted to the reset state. Software needs to re-write these registers to a known state. A write of 1h sets this bit.</p> <p>0h - Bit not flipped 1h - Bit flipped</p> |
| 6-5 | PARITY_ERR | R/W1S | 0h | <p>2-bit saturating counter for the number of parity errors that have occurred since last cleared. This is also a status set register and a non-zero value sets the level interrupt. Software can also write a value to the CLR_PARITY_ERR field to decrement this counter.</p> <p>0h - No parity errors have occurred 1h - 1 parity error has occurred 2h - 2 parity errors have occurred 3h - 3 or more parity errors have occurred</p> |
| 4 | ECC_OTHER | R/W1S | 0h | <p>1h - Indicates that successive single-bit errors have occurred while a write-back is still pending. Software can also write 1h to set the pending status and write 1h to the corresponding clear bit to clear the status.</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: Not used in inject only mode. Always read as 0h.</p> <hr/> |

Table 20-9. ECC_ERR_STAT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 3-2 | ECC_DED | R/W | 0h | <p>2-bit saturating counter for the number of double-bit errors that have occurred since last cleared. This is also a status set register and a non-zero value sets the level interrupt. Software can also write a value to the CLR_ECC_SEC field to decrement this counter.</p> <p>0h - No double-bit errors have occurred 1h - 1 double-bit has error occurred 2h - 2 double-bit have errors occurred 3h - 3 or more double-bit errors have occurred</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: Not used in inject only mode. Always read as 0h.</p> <hr/> |
| 1-0 | ECC_SEC | R/W | 0h | <p>2-bit saturating counter for the number of single-bit errors that have occurred since last cleared. This is also a status set register and a non-zero value sets the level interrupt. Software can also write a value to the CLR_ECC_SEC field to decrement this counter.</p> <p>0h - No single-bit errors have occurred 1h - 1 single-bit has occurred 2h - 2 single-bit have occurred 3h - 3 or more single-bit have occurred</p> <hr/> <p style="text-align: center;">Note</p> <p>NOTE: Not used in inject only mode. Always read as 0h.</p> <hr/> |

20.9 ECC_ERR_STAT2 Register (Offset = 24h) [reset = 0h]

ECC_ERR_STAT2 is shown in [Figure 20-9](#) and described in [Table 20-10](#).

Return to [Summary Table](#).

ECC RAM Error Status 2 Register

Figure 20-9. ECC_ERR_STAT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_ROW | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 20-10. ECC_ERR_STAT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 31-0 | ECC_ROW | R | 0h | Row address where the single or double-bit error has occurred. <div style="text-align: center;">Note</div> NOTE: Not used in inject only mode. Always read as 0h. |

20.10 ECC_ERR_STAT3 Register (Offset = 28h) [reset = 0h]

ECC_ERR_STAT3 is shown in [Figure 20-10](#) and described in [Table 20-11](#).

Return to [Summary Table](#).

ECC RAM Error Status 3 Register

Figure 20-10. ECC_ERR_STAT3 Register

| | | | | | | | |
|----------|----|----|----|----|----|---------------------------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | CLR_SVBUS_T IMEOUT_ERR | RESERVED |
| R-0h | | | | | | R/W1C-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | SVBUS_TIMEO UT_ERR | WB_PEND |
| R-0h | | | | | | R/W1S-0h | R-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-11. ECC_ERR_STAT3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-----------------------|-------|-------|--|
| 31-10 | RESERVED | R | 0 | Reserved |
| 9 | CLR_SVBUS_TIMEOUT_ERR | R/W1C | 0h | Clear ECC serial interface timeout error status 0h - No effect 1h - Clears this bit and the SVBUS_TIMEOUT_ERR bit |
| 8-2 | RESERVED | R | 0 | Reserved |
| 1 | SVBUS_TIMEOUT_ERR | R/W1S | 0h | ECC serial interface timeout error. Write a 1h to set the flag 0h - No timeout error 1h - Timeout error |
| 0 | WB_PEND | R | 0h | Delayed write-back pending status. 0h - An ECC data correction write-back is not pending 1h - An ECC data correction write-back is pending |
| | | | | <p>Note</p> <p>NOTE: Not used in inject only mode. Always read as 0h.</p> |

20.11 ECC_CBASS_REV Register (Offset = 10h) [reset = X]

ECC_CBASS_REV is shown in [Figure 20-11](#) and described in [Table 20-12](#).

Return to [Summary Table](#).

Interconnect ECC Component Revision Register.

Figure 20-11. ECC_CBASS_REV Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | REV | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | R-Xh | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 20-12. ECC_CBASS_REV Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------|------|-------|-------------------|
| 31-0 | REV | R | Xh | TI internal data. |

20.12 ECC_CBASS_CTRL Register (Offset = 14h) [reset = 2h]

ECC_CBASS_CTRL is shown in [Figure 20-12](#) and described in [Table 20-13](#).

Return to [Summary Table](#).

Interconnect ECC Component Control Register.

Figure 20-12. ECC_CBASS_CTRL Register

| | | | | | | | |
|----------|----|-------------|----------|-------------|----------|-----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | ECC_PATTERN | | | |
| R-0h | | | | R/W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | FORCE_N_BIT | FORCE_DE | FORCE_SE | RESERVED | ECC_CHECK | RESERVED |
| R-0h | | R/W-0h | R/W-0h | R/W-0h | R-0h | R/W-1h | R-0h |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 20-13. ECC_CBASS_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------------|------|-------|---|
| 31-12 | RESERVED | R | 0h | Reserved |
| 11-8 | ECC_PATTERN | R/W | 0h | Data pattern to be used for injection. 0h = 0s 1h = Fs 2h = As 3h = 5s |
| 7-6 | RESERVED | R | 0h | Reserved |
| 5 | FORCE_N_BIT | R/W | 0h | Update injection fields after the injection to setup for the next incremental injection. 0h = Keep current settings after injection 1h = Increment to next bit or group after injection |
| 4 | FORCE_DE | R/W | 0h | Inject a double bit error when set. Automatically cleared when injection completes. |
| 3 | FORCE_SE | R/W | 0h | Inject a single bit error when set. Automatically cleared when injection completes. |
| 2 | RESERVED | R | 0h | Reserved |
| 1 | ECC_CHECK | R/W | 1h | Enable checkers. 0h = Disabled 1h = Enabled |
| 0 | RESERVED | R | 0h | Reserved |

20.13 ECC_CBASS_ERR_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC_CBASS_ERR_CTRL1 is shown in [Figure 20-13](#) and described in [Table 20-14](#).

Return to [Summary Table](#).

Interconnect ECC Component Error Control 1 Register.

This register allows setting the injection data.

Figure 20-13. ECC_CBASS_ERR_CTRL1 Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | ECC_BIT1 |
| R-0h | | | | | | | R/W-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_BIT1 | | | | | | | |
| R/W-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| ECC_GRP | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ECC_GRP | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 20-14. ECC_CBASS_ERR_CTRL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|-------------------------------|
| 31-25 | RESERVED | R | 0h | Reserved |
| 24-16 | ECC_BIT1 | R/W | 0h | First bit to inject an error. |
| 15-0 | ECC_GRP | R/W | 0h | Group of checker to inject. |

20.14 ECC_CBASS_ERR_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC_CBASS_ERR_CTRL2 is shown in [Figure 20-14](#) and described in [Table 20-15](#).

Return to [Summary Table](#).

Interconnect ECC Component Error Control 2 Register.

This register allows setting the injection data.

Figure 20-14. ECC_CBASS_ERR_CTRL2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----------|---|---|---|---|---|---|---|---|--|--|--|--|--|--|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | |
| RESERVED | | | | | | | | | | | | | | | | | | | | | | | ECC_BIT2 | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | | | | | | | | R/W-0h | | | | | | | | | | | | | | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 20-15. ECC_CBASS_ERR_CTRL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|---|
| 31-9 | RESERVED | R | 0h | Reserved |
| 8-0 | ECC_BIT2 | R/W | 0h | Second bit to inject an error. Only valid if ECC_CBASS_CTRL[4] FORCE_DE is set. |

20.15 ECC_CBASS_ERR_STAT1 Register (Offset = 20h) [reset = 0h]

ECC_CBASS_ERR_STAT1 is shown in [Figure 20-15](#) and described in [Table 20-16](#).

Return to [Summary Table](#).

Interconnect ECC Component Error Status 1 Register.

This register allows reading the captured error data.

Figure 20-15. ECC_CBASS_ERR_STAT1 Register

| | | | | | | | |
|------------------|----|------------------|----|--------------|----|--------------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ERR_GRP | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ERR_GRP | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| INJ_UNC_PEND_CLR | | INJ_COR_PEND_CLR | | UNC_PEND_CLR | | COR_PEND_CLR | |
| R/WD-0h | | R/WD-0h | | R/WD-0h | | R/WD-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INJ_UNC_PEND | | INJ_COR_PEND | | UNC_PEND | | COR_PEND | |
| R/WI-0h | | R/WI-0h | | R/WI-0h | | R/WI-0h | |

LEGEND: R = Read Only; R/WD = Read/Write to Decrement Field; R/WI = Read/Write to Increment Field; -n = value after reset

Table 20-16. ECC_CBASS_ERR_STAT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|------------------|------|-------|--|
| 31-16 | ERR_GRP | R | 0h | Specific checker that reported the error. |
| 15-14 | INJ_UNC_PEND_CLR | R/WD | 0h | Number of injected uncorrected pending interrupts (same value as UNC_PEND). Writing decrements INJ_UNC_PEND by that value. |
| 13-12 | INJ_COR_PEND_CLR | R/WD | 0h | Number of injected corrected pending interrupts (same value as COR_PEND). Writing decrements INJ_COR_PEND by that value. |
| 11-10 | UNC_PEND_CLR | R/WD | 0h | Number of uncorrected pending interrupts (same value as UNC_PEND). Writing decrements UNC_PEND by that value. |
| 9-8 | COR_PEND_CLR | R/WD | 0h | Number of corrected pending interrupts (same value as COR_PEND). Writing decrements COR_PEND by that value. |
| 7-6 | INJ_UNC_PEND | R/WI | 0h | Number of injected uncorrected pending interrupts. Writing increments by that value. |
| 5-4 | INJ_COR_PEND | R/WI | 0h | Number of injected corrected pending interrupts. Writing increments by that value. |
| 3-2 | UNC_PEND | R/WI | 0h | Number of uncorrected pending interrupts. Writing increments by that value. |
| 1-0 | COR_PEND | R/WI | 0h | Number of corrected pending interrupts. Writing increments by that value. |

20.16 ECC_CBASS_ERR_STAT2 Register (Offset = 24h) [reset = 0h]

ECC_CBASS_ERR_STAT2 is shown in [Figure 20-16](#) and described in [Table 20-17](#).

Return to [Summary Table](#).

Interconnect ECC Component Error Status 2 Register.

This register allows reading the captured error data.

Figure 20-16. ECC_CBASS_ERR_STAT2 Register

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ERR_TYPE | | | | | | | | | | | | | | | | ERR_BIT | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | | | | | | | | | R-0h | | | | | | | | | | | | | | | |

LEGEND: R = Read Only; -n = value after reset

Table 20-17. ECC_CBASS_ERR_STAT2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| 31-16 | ERR_TYPE | R | 0h | This field is not supported and can read any value and be ignored. |
| 15-0 | ERR_BIT | R | 0h | Bit that caused the error. Always valid for EDC single bit corrected errors or redundant errors. Identifies parity segment number (but not the exact bit) with a parity error. This field is not valid for EDC double bit errors. |

20.17 ECC_SEC_EOI_REG Register (Offset = 3Ch) [reset = 0h]

ECC_SEC_EOI_REG is shown in [Figure 20-17](#) and described in [Table 20-18](#).

Return to [Summary Table](#).

SEC EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Figure 20-17. ECC_SEC_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R-0h | | | | | | | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-18. ECC_SEC_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-1 | RESERVED | R | 0 | Reserved |
| 0 | EOI_WR | R/W1S | 0h | Write of 1h to this register indicates that software has serviced the correctable interrupt and next interrupt can be sent to the host. This bit is self clearing and read returns a zero. |

20.18 ECC_SEC_STATUS_REG0 Register (Offset = 40h) [reset = 0h]

ECC_SEC_STATUS_REG0 is shown in [Figure 20-18](#) and described in [Table 20-19](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-18. ECC_SEC_STATUS_REG0 Register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM31_PEND | RAM30_PEND | RAM29_PEND | RAM28_PEND | RAM27_PEND | RAM26_PEND | RAM25_PEND | RAM24_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM23_PEND | RAM22_PEND | RAM21_PEND | RAM20_PEND | RAM19_PEND | RAM18_PEND | RAM17_PEND | RAM16_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM15_PEND | RAM14_PEND | RAM13_PEND | RAM12_PEND | RAM11_PEND | RAM10_PEND | RAM9_PEND | RAM8_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM7_PEND | RAM6_PEND | RAM5_PEND | RAM4_PEND | RAM3_PEND | RAM2_PEND | RAM1_PEND | RAM0_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-19. ECC_SEC_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 31 | RAM31_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 31. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM30_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 30. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM29_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 29. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM28_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 28. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM27_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 27. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM26_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 26. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM25_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 25. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM24_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 24. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-19. ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 23 | RAM23_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 23. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM22_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 22. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM21_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 21. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM20_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 20. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM19_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 19. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM18_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 18. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM17_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 17. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM16_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 16. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM15_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 15. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM14_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 14. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM13_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 13. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM12_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 12. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM11_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 11. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM10_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 10. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM9_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 9. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM8_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 8. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-19. ECC_SEC_STATUS_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|-------|-------|--|
| 7 | RAM7_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 7. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM6_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 6. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM5_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 5. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM4_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 4. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM3_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 3. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM2_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 2. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM1_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 1. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM0_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 0. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.19 ECC_SEC_STATUS_REG1 Register (Offset = 44h) [reset = 0h]

ECC_SEC_STATUS_REG1 is shown in [Figure 20-19](#) and described in [Table 20-20](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-19. ECC_SEC_STATUS_REG1 Register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM63_PEND | RAM62_PEND | RAM61_PEND | RAM60_PEND | RAM59_PEND | RAM58_PEND | RAM57_PEND | RAM56_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM55_PEND | RAM54_PEND | RAM53_PEND | RAM52_PEND | RAM51_PEND | RAM50_PEND | RAM49_PEND | RAM48_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM47_PEND | RAM46_PEND | RAM45_PEND | RAM44_PEND | RAM43_PEND | RAM42_PEND | RAM41_PEND | RAM40_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM39_PEND | RAM38_PEND | RAM37_PEND | RAM36_PEND | RAM35_PEND | RAM34_PEND | RAM33_PEND | RAM32_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-20. ECC_SEC_STATUS_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 31 | RAM63_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 63. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM62_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 62. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM61_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 61. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM60_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 60. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM59_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 59. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM58_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 58. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM57_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 57. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM56_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 56. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-20. ECC_SEC_STATUS_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 23 | RAM55_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 55. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM54_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 54. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM53_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 53. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM52_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 52. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM51_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 51. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM50_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 50. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM49_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 49. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM48_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 48. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM47_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 47. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM46_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 46. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM45_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 45. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM44_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 44. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM43_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 43. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM42_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 42. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM41_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 41. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM40_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 40. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-20. ECC_SEC_STATUS_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 7 | RAM39_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 39. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM38_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 38. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM37_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 37. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM36_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 36. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM35_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 35. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM34_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 34. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM33_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 33. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM32_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 32. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.20 ECC_SEC_STATUS_REG2 Register (Offset = 48h) [reset = 0h]

ECC_SEC_STATUS_REG2 is shown in [Figure 20-20](#) and described in [Table 20-21](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-20. ECC_SEC_STATUS_REG2 Register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM95_PEND | RAM94_PEND | RAM93_PEND | RAM92_PEND | RAM91_PEND | RAM90_PEND | RAM89_PEND | RAM88_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM87_PEND | RAM86_PEND | RAM85_PEND | RAM84_PEND | RAM83_PEND | RAM82_PEND | RAM81_PEND | RAM80_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM79_PEND | RAM78_PEND | RAM77_PEND | RAM76_PEND | RAM75_PEND | RAM74_PEND | RAM73_PEND | RAM72_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM71_PEND | RAM70_PEND | RAM69_PEND | RAM68_PEND | RAM67_PEND | RAM66_PEND | RAM65_PEND | RAM64_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-21. ECC_SEC_STATUS_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 31 | RAM95_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 95. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM94_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 94. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM93_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 93. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM92_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 92. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM91_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 91. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM90_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 90. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM89_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 89. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM88_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 88. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-21. ECC_SEC_STATUS_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 23 | RAM87_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 87. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM86_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 86. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM85_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 85. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM84_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 84. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM83_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 83. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM82_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 82. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM81_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 81. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM80_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 80. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM79_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 79. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM78_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 78. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM77_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 77. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM76_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 76. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM75_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 75. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM74_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 74. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM73_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 73. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM72_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 72. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-21. ECC_SEC_STATUS_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 7 | RAM71_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 71. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM70_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 70. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM69_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 69. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM68_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 68. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM67_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 67. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM66_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 66. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM65_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 65. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM64_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 64. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.21 ECC_SEC_STATUS_REG3 Register (Offset = 4Ch) [reset = 0h]

ECC_SEC_STATUS_REG3 is shown in [Figure 20-21](#) and described in [Table 20-22](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-21. ECC_SEC_STATUS_REG3 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM127_PEND | RAM126_PEND | RAM125_PEND | RAM124_PEND | RAM123_PEND | RAM122_PEND | RAM121_PEND | RAM120_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM119_PEND | RAM118_PEND | RAM117_PEND | RAM116_PEND | RAM115_PEND | RAM114_PEND | RAM113_PEND | RAM112_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM111_PEND | RAM110_PEND | RAM109_PEND | RAM108_PEND | RAM107_PEND | RAM106_PEND | RAM105_PEND | RAM104_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM103_PEND | RAM102_PEND | RAM101_PEND | RAM100_PEND | RAM99_PEND | RAM98_PEND | RAM97_PEND | RAM96_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-22. ECC_SEC_STATUS_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM127_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 127. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM126_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 126. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM125_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 125. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM124_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 124. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM123_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 123. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM122_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 122. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM121_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 121. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM120_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 120. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-22. ECC_SEC_STATUS_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 23 | RAM119_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 119. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM118_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 118. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM117_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 117. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM116_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 116. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM115_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 115. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM114_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 114. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM113_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 113. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM112_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 112. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM111_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 111. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM110_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 110. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM109_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 109. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM108_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 108. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM107_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 107. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM106_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 106. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM105_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 105. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM104_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 104. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-22. ECC_SEC_STATUS_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 7 | RAM103_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 103. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM102_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 102. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM101_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 101. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM100_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 100. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM99_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 99. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM98_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 98. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM97_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 97. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM96_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 96. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.22 ECC_SEC_STATUS_REG4 Register (Offset = 50h) [reset = 0h]

ECC_SEC_STATUS_REG4 is shown in [Figure 20-22](#) and described in [Table 20-23](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-22. ECC_SEC_STATUS_REG4 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM159_PEND | RAM158_PEND | RAM157_PEND | RAM156_PEND | RAM155_PEND | RAM154_PEND | RAM153_PEND | RAM152_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM151_PEND | RAM150_PEND | RAM149_PEND | RAM148_PEND | RAM147_PEND | RAM146_PEND | RAM145_PEND | RAM144_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM143_PEND | RAM142_PEND | RAM141_PEND | RAM140_PEND | RAM139_PEND | RAM138_PEND | RAM137_PEND | RAM136_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM135_PEND | RAM134_PEND | RAM133_PEND | RAM132_PEND | RAM131_PEND | RAM130_PEND | RAM129_PEND | RAM128_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-23. ECC_SEC_STATUS_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM159_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 159. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM158_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 158. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM157_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 157. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM156_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 156. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM155_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 155. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM154_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 154. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM153_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 153. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM152_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 152. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-23. ECC_SEC_STATUS_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 23 | RAM151_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 151. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM150_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 150. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM149_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 149. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM148_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 148. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM147_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 147. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM146_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 146. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM145_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 145. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM144_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 144. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM143_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 143. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM142_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 142. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM141_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 141. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM140_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 140. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM139_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 139. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM138_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 138. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM137_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 137. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM136_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 136. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-23. ECC_SEC_STATUS_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 7 | RAM135_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 135. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM134_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 134. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM133_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 133. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM132_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 132. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM131_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 131. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM130_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 130. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM129_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 129. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM128_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 128. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.23 ECC_SEC_STATUS_REG5 Register (Offset = 54h) [reset = 0h]

ECC_SEC_STATUS_REG5 is shown in [Figure 20-23](#) and described in [Table 20-24](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-23. ECC_SEC_STATUS_REG5 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM191_PEND | RAM190_PEND | RAM189_PEND | RAM188_PEND | RAM187_PEND | RAM186_PEND | RAM185_PEND | RAM184_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM183_PEND | RAM182_PEND | RAM181_PEND | RAM180_PEND | RAM179_PEND | RAM178_PEND | RAM177_PEND | RAM176_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM175_PEND | RAM174_PEND | RAM173_PEND | RAM172_PEND | RAM171_PEND | RAM170_PEND | RAM169_PEND | RAM168_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM167_PEND | RAM166_PEND | RAM165_PEND | RAM164_PEND | RAM163_PEND | RAM162_PEND | RAM161_PEND | RAM160_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-24. ECC_SEC_STATUS_REG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM191_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 191. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM190_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 190. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM189_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 189. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM188_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 188. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM187_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 187. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM186_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 186. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM185_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 185. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM184_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 184. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-24. ECC_SEC_STATUS_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 23 | RAM183_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 183. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM182_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 182. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM181_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 181. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM180_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 180. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM179_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 179. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM178_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 178. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM177_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 177. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM176_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 176. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM175_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 175. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM174_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 174. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM173_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 173. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM172_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 172. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM171_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 171. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM170_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 170. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM169_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 169. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM168_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 168. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-24. ECC_SEC_STATUS_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 7 | RAM167_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 167. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM166_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 166. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM165_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 165. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM164_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 164. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM163_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 163. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM162_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 162. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM161_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 161. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM160_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 160. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.24 ECC_SEC_STATUS_REG6 Register (Offset = 58h) [reset = 0h]

ECC_SEC_STATUS_REG6 is shown in [Figure 20-24](#) and described in [Table 20-25](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-24. ECC_SEC_STATUS_REG6 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM223_PEND | RAM222_PEND | RAM221_PEND | RAM220_PEND | RAM219_PEND | RAM218_PEND | RAM217_PEND | RAM216_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM215_PEND | RAM214_PEND | RAM213_PEND | RAM212_PEND | RAM211_PEND | RAM210_PEND | RAM209_PEND | RAM208_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM207_PEND | RAM206_PEND | RAM205_PEND | RAM204_PEND | RAM203_PEND | RAM202_PEND | RAM201_PEND | RAM200_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM199_PEND | RAM198_PEND | RAM197_PEND | RAM196_PEND | RAM195_PEND | RAM194_PEND | RAM193_PEND | RAM192_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-25. ECC_SEC_STATUS_REG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM223_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 223. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM222_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 222. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM221_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 221. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM220_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 220. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM219_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 219. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM218_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 218. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM217_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 217. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM216_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 216. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-25. ECC_SEC_STATUS_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 23 | RAM215_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 215. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM214_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 214. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM213_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 213. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM212_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 212. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM211_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 211. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM210_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 210. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM209_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 209. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM208_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 208. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM207_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 207. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM206_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 206. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM205_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 205. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM204_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 204. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM203_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 203. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM202_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 202. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM201_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 201. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM200_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 200. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-25. ECC_SEC_STATUS_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 7 | RAM199_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 199. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM198_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 198. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM197_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 197. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM196_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 196. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM195_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 195. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM194_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 194. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM193_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 193. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM192_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 192. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.25 ECC_SEC_STATUS_REG7 Register (Offset = 5Ch) [reset = 0h]

ECC_SEC_STATUS_REG7 is shown in [Figure 20-25](#) and described in [Table 20-26](#).

Return to [Summary Table](#).

Interrupt status register for correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-25. ECC_SEC_STATUS_REG7 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM255_PEND | RAM254_PEND | RAM253_PEND | RAM252_PEND | RAM251_PEND | RAM250_PEND | RAM249_PEND | RAM248_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM247_PEND | RAM246_PEND | RAM245_PEND | RAM244_PEND | RAM243_PEND | RAM242_PEND | RAM241_PEND | RAM240_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM239_PEND | RAM238_PEND | RAM237_PEND | RAM236_PEND | RAM235_PEND | RAM234_PEND | RAM233_PEND | RAM232_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM231_PEND | RAM230_PEND | RAM229_PEND | RAM228_PEND | RAM227_PEND | RAM226_PEND | RAM225_PEND | RAM224_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-26. ECC_SEC_STATUS_REG7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM255_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 255. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 30 | RAM254_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 254. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 29 | RAM253_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 253. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 28 | RAM252_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 252. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 27 | RAM251_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 251. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 26 | RAM250_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 250. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 25 | RAM249_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 249. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 24 | RAM248_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 248. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-26. ECC_SEC_STATUS_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 23 | RAM247_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 247. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 22 | RAM246_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 246. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 21 | RAM245_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 245. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 20 | RAM244_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 244. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 19 | RAM243_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 243. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 18 | RAM242_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 242. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 17 | RAM241_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 241. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 16 | RAM240_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 240. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 15 | RAM239_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 239. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 14 | RAM238_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 238. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 13 | RAM237_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 237. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 12 | RAM236_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 236. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 11 | RAM235_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 235. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 10 | RAM234_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 234. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 9 | RAM233_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 233. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 8 | RAM232_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 232. 0h - Correctable error not occurred 1h - Correctable error occurred |

Table 20-26. ECC_SEC_STATUS_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 7 | RAM231_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 231. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 6 | RAM230_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 230. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 5 | RAM229_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 229. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 4 | RAM228_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 228. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 3 | RAM227_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 227. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 2 | RAM226_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 226. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 1 | RAM225_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 225. 0h - Correctable error not occurred 1h - Correctable error occurred |
| 0 | RAM224_PEND | R/W1S | 0h | Correctable error interrupt status for ECC endpoint with ID = 224. 0h - Correctable error not occurred 1h - Correctable error occurred |

20.26 ECC_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG0 is shown in [Figure 20-26](#) and described in [Table 20-27](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-26. ECC_SEC_ENABLE_SET_REG0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM31_ENABL E_SET | RAM30_ENABL E_SET | RAM29_ENABL E_SET | RAM28_ENABL E_SET | RAM27_ENABL E_SET | RAM26_ENABL E_SET | RAM25_ENABL E_SET | RAM24_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM23_ENABL E_SET | RAM22_ENABL E_SET | RAM21_ENABL E_SET | RAM20_ENABL E_SET | RAM19_ENABL E_SET | RAM18_ENABL E_SET | RAM17_ENABL E_SET | RAM16_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM15_ENABL E_SET | RAM14_ENABL E_SET | RAM13_ENABL E_SET | RAM12_ENABL E_SET | RAM11_ENABL E_SET | RAM10_ENABL E_SET | RAM9_ENABL E_SET | RAM8_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM7_ENABL E_SET | RAM6_ENABL E_SET | RAM5_ENABL E_SET | RAM4_ENABL E_SET | RAM3_ENABL E_SET | RAM2_ENABL E_SET | RAM1_ENABL E_SET | RAM0_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-27. ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM31_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 31. Write 1h to enable the interrupt |
| 30 | RAM30_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 30. Write 1h to enable the interrupt |
| 29 | RAM29_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 29. Write 1h to enable the interrupt |
| 28 | RAM28_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 28. Write 1h to enable the interrupt |
| 27 | RAM27_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 27. Write 1h to enable the interrupt |
| 26 | RAM26_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 26. Write 1h to enable the interrupt |
| 25 | RAM25_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 25. Write 1h to enable the interrupt |
| 24 | RAM24_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 24. Write 1h to enable the interrupt |
| 23 | RAM23_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 23. Write 1h to enable the interrupt |
| 22 | RAM22_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 22. Write 1h to enable the interrupt |

Table 20-27. ECC_SEC_ENABLE_SET_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM21_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 21. Write 1h to enable the interrupt |
| 20 | RAM20_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 20. Write 1h to enable the interrupt |
| 19 | RAM19_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 19. Write 1h to enable the interrupt |
| 18 | RAM18_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 18. Write 1h to enable the interrupt |
| 17 | RAM17_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 17. Write 1h to enable the interrupt |
| 16 | RAM16_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 16. Write 1h to enable the interrupt |
| 15 | RAM15_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 15. Write 1h to enable the interrupt |
| 14 | RAM14_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 14. Write 1h to enable the interrupt |
| 13 | RAM13_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 13. Write 1h to enable the interrupt |
| 12 | RAM12_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 12. Write 1h to enable the interrupt |
| 11 | RAM11_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 11. Write 1h to enable the interrupt |
| 10 | RAM10_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 10. Write 1h to enable the interrupt |
| 9 | RAM9_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 9. Write 1h to enable the interrupt |
| 8 | RAM8_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 8. Write 1h to enable the interrupt |
| 7 | RAM7_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 7. Write 1h to enable the interrupt |
| 6 | RAM6_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 6. Write 1h to enable the interrupt |
| 5 | RAM5_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 5. Write 1h to enable the interrupt |
| 4 | RAM4_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 4. Write 1h to enable the interrupt |
| 3 | RAM3_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 3. Write 1h to enable the interrupt |
| 2 | RAM2_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 2. Write 1h to enable the interrupt |
| 1 | RAM1_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 1. Write 1h to enable the interrupt |
| 0 | RAM0_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 0. Write 1h to enable the interrupt |

20.27 ECC_SEC_ENABLE_SET_REG1 Register (Offset = 84h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG1 is shown in [Figure 20-27](#) and described in [Table 20-28](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-27. ECC_SEC_ENABLE_SET_REG1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM63_ENABL E_SET | RAM62_ENABL E_SET | RAM61_ENABL E_SET | RAM60_ENABL E_SET | RAM59_ENABL E_SET | RAM58_ENABL E_SET | RAM57_ENABL E_SET | RAM56_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM55_ENABL E_SET | RAM54_ENABL E_SET | RAM53_ENABL E_SET | RAM52_ENABL E_SET | RAM51_ENABL E_SET | RAM50_ENABL E_SET | RAM49_ENABL E_SET | RAM48_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM47_ENABL E_SET | RAM46_ENABL E_SET | RAM45_ENABL E_SET | RAM44_ENABL E_SET | RAM43_ENABL E_SET | RAM42_ENABL E_SET | RAM41_ENABL E_SET | RAM40_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM39_ENABL E_SET | RAM38_ENABL E_SET | RAM37_ENABL E_SET | RAM36_ENABL E_SET | RAM35_ENABL E_SET | RAM34_ENABL E_SET | RAM33_ENABL E_SET | RAM32_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-28. ECC_SEC_ENABLE_SET_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM63_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 63. Write 1h to enable the interrupt |
| 30 | RAM62_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 62. Write 1h to enable the interrupt |
| 29 | RAM61_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 61. Write 1h to enable the interrupt |
| 28 | RAM60_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 60. Write 1h to enable the interrupt |
| 27 | RAM59_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 59. Write 1h to enable the interrupt |
| 26 | RAM58_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 58. Write 1h to enable the interrupt |
| 25 | RAM57_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 57. Write 1h to enable the interrupt |
| 24 | RAM56_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 56. Write 1h to enable the interrupt |
| 23 | RAM55_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 55. Write 1h to enable the interrupt |
| 22 | RAM54_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 54. Write 1h to enable the interrupt |

Table 20-28. ECC_SEC_ENABLE_SET_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM53_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 53. Write 1h to enable the interrupt |
| 20 | RAM52_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 52. Write 1h to enable the interrupt |
| 19 | RAM51_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 51. Write 1h to enable the interrupt |
| 18 | RAM50_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 50. Write 1h to enable the interrupt |
| 17 | RAM49_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 49. Write 1h to enable the interrupt |
| 16 | RAM48_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 48. Write 1h to enable the interrupt |
| 15 | RAM47_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 47. Write 1h to enable the interrupt |
| 14 | RAM46_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 46. Write 1h to enable the interrupt |
| 13 | RAM45_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 45. Write 1h to enable the interrupt |
| 12 | RAM44_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 44. Write 1h to enable the interrupt |
| 11 | RAM43_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 43. Write 1h to enable the interrupt |
| 10 | RAM42_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 42. Write 1h to enable the interrupt |
| 9 | RAM41_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 41. Write 1h to enable the interrupt |
| 8 | RAM40_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 40. Write 1h to enable the interrupt |
| 7 | RAM39_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 39. Write 1h to enable the interrupt |
| 6 | RAM38_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 38. Write 1h to enable the interrupt |
| 5 | RAM37_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 37. Write 1h to enable the interrupt |
| 4 | RAM36_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 36. Write 1h to enable the interrupt |
| 3 | RAM35_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 35. Write 1h to enable the interrupt |
| 2 | RAM34_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 34. Write 1h to enable the interrupt |
| 1 | RAM33_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 33. Write 1h to enable the interrupt |
| 0 | RAM32_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 32. Write 1h to enable the interrupt |

20.28 ECC_SEC_ENABLE_SET_REG2 Register (Offset = 88h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG2 is shown in [Figure 20-28](#) and described in [Table 20-29](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-28. ECC_SEC_ENABLE_SET_REG2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM95_ENABL E_SET | RAM94_ENABL E_SET | RAM93_ENABL E_SET | RAM92_ENABL E_SET | RAM91_ENABL E_SET | RAM90_ENABL E_SET | RAM89_ENABL E_SET | RAM88_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM87_ENABL E_SET | RAM86_ENABL E_SET | RAM85_ENABL E_SET | RAM84_ENABL E_SET | RAM83_ENABL E_SET | RAM82_ENABL E_SET | RAM81_ENABL E_SET | RAM80_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM79_ENABL E_SET | RAM78_ENABL E_SET | RAM77_ENABL E_SET | RAM76_ENABL E_SET | RAM75_ENABL E_SET | RAM74_ENABL E_SET | RAM73_ENABL E_SET | RAM72_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM71_ENABL E_SET | RAM70_ENABL E_SET | RAM69_ENABL E_SET | RAM68_ENABL E_SET | RAM67_ENABL E_SET | RAM66_ENABL E_SET | RAM65_ENABL E_SET | RAM64_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-29. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM95_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 95. Write 1h to enable the interrupt |
| 30 | RAM94_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 94. Write 1h to enable the interrupt |
| 29 | RAM93_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 93. Write 1h to enable the interrupt |
| 28 | RAM92_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 92. Write 1h to enable the interrupt |
| 27 | RAM91_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 91. Write 1h to enable the interrupt |
| 26 | RAM90_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 90. Write 1h to enable the interrupt |
| 25 | RAM89_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 89. Write 1h to enable the interrupt |
| 24 | RAM88_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 88. Write 1h to enable the interrupt |
| 23 | RAM87_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 87. Write 1h to enable the interrupt |
| 22 | RAM86_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 86. Write 1h to enable the interrupt |

Table 20-29. ECC_SEC_ENABLE_SET_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM85_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 85. Write 1h to enable the interrupt |
| 20 | RAM84_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 84. Write 1h to enable the interrupt |
| 19 | RAM83_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 83. Write 1h to enable the interrupt |
| 18 | RAM82_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 82. Write 1h to enable the interrupt |
| 17 | RAM81_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 81. Write 1h to enable the interrupt |
| 16 | RAM80_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 80. Write 1h to enable the interrupt |
| 15 | RAM79_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 79. Write 1h to enable the interrupt |
| 14 | RAM78_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 78. Write 1h to enable the interrupt |
| 13 | RAM77_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 77. Write 1h to enable the interrupt |
| 12 | RAM76_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 76. Write 1h to enable the interrupt |
| 11 | RAM75_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 75. Write 1h to enable the interrupt |
| 10 | RAM74_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 74. Write 1h to enable the interrupt |
| 9 | RAM73_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 73. Write 1h to enable the interrupt |
| 8 | RAM72_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 72. Write 1h to enable the interrupt |
| 7 | RAM71_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 71. Write 1h to enable the interrupt |
| 6 | RAM70_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 70. Write 1h to enable the interrupt |
| 5 | RAM69_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 69. Write 1h to enable the interrupt |
| 4 | RAM68_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 68. Write 1h to enable the interrupt |
| 3 | RAM67_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 67. Write 1h to enable the interrupt |
| 2 | RAM66_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 66. Write 1h to enable the interrupt |
| 1 | RAM65_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 65. Write 1h to enable the interrupt |
| 0 | RAM64_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 64. Write 1h to enable the interrupt |

20.29 ECC_SEC_ENABLE_SET_REG3 Register (Offset = 8Ch) [reset = 0h]

ECC_SEC_ENABLE_SET_REG3 is shown in [Figure 20-29](#) and described in [Table 20-30](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-29. ECC_SEC_ENABLE_SET_REG3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM127_ENAB LE_SET | RAM126_ENAB LE_SET | RAM125_ENAB LE_SET | RAM124_ENAB LE_SET | RAM123_ENAB LE_SET | RAM122_ENAB LE_SET | RAM121_ENAB LE_SET | RAM120_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM119_ENAB LE_SET | RAM118_ENAB LE_SET | RAM117_ENAB LE_SET | RAM116_ENAB LE_SET | RAM115_ENAB LE_SET | RAM114_ENAB LE_SET | RAM113_ENAB LE_SET | RAM112_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM111_ENAB LE_SET | RAM110_ENAB LE_SET | RAM109_ENAB LE_SET | RAM108_ENAB LE_SET | RAM107_ENAB LE_SET | RAM106_ENAB LE_SET | RAM105_ENAB LE_SET | RAM104_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM103_ENAB LE_SET | RAM102_ENAB LE_SET | RAM101_ENAB LE_SET | RAM100_ENAB LE_SET | RAM99_ENABL E_SET | RAM98_ENABL E_SET | RAM97_ENABL E_SET | RAM96_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-30. ECC_SEC_ENABLE_SET_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM127_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 127. Write 1h to enable the interrupt |
| 30 | RAM126_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 126. Write 1h to enable the interrupt |
| 29 | RAM125_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 125. Write 1h to enable the interrupt |
| 28 | RAM124_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 124. Write 1h to enable the interrupt |
| 27 | RAM123_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 123. Write 1h to enable the interrupt |
| 26 | RAM122_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 122. Write 1h to enable the interrupt |
| 25 | RAM121_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 121. Write 1h to enable the interrupt |
| 24 | RAM120_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 120. Write 1h to enable the interrupt |
| 23 | RAM119_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 119. Write 1h to enable the interrupt |
| 22 | RAM118_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 118. Write 1h to enable the interrupt |

Table 20-30. ECC_SEC_ENABLE_SET_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM117_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 117. Write 1h to enable the interrupt |
| 20 | RAM116_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 116. Write 1h to enable the interrupt |
| 19 | RAM115_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 115. Write 1h to enable the interrupt |
| 18 | RAM114_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 114. Write 1h to enable the interrupt |
| 17 | RAM113_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 113. Write 1h to enable the interrupt |
| 16 | RAM112_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 112. Write 1h to enable the interrupt |
| 15 | RAM111_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 111. Write 1h to enable the interrupt |
| 14 | RAM110_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 110. Write 1h to enable the interrupt |
| 13 | RAM109_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 109. Write 1h to enable the interrupt |
| 12 | RAM108_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 108. Write 1h to enable the interrupt |
| 11 | RAM107_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 107. Write 1h to enable the interrupt |
| 10 | RAM106_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 106. Write 1h to enable the interrupt |
| 9 | RAM105_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 105. Write 1h to enable the interrupt |
| 8 | RAM104_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 104. Write 1h to enable the interrupt |
| 7 | RAM103_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 103. Write 1h to enable the interrupt |
| 6 | RAM102_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 102. Write 1h to enable the interrupt |
| 5 | RAM101_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 101. Write 1h to enable the interrupt |
| 4 | RAM100_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 100. Write 1h to enable the interrupt |
| 3 | RAM99_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 99. Write 1h to enable the interrupt |
| 2 | RAM98_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 98. Write 1h to enable the interrupt |
| 1 | RAM97_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 97. Write 1h to enable the interrupt |
| 0 | RAM96_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 96. Write 1h to enable the interrupt |

20.30 ECC_SEC_ENABLE_SET_REG4 Register (Offset = 90h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG4 is shown in [Figure 20-30](#) and described in [Table 20-31](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-30. ECC_SEC_ENABLE_SET_REG4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| RAM159_ENABLE_SET | RAM158_ENABLE_SET | RAM157_ENABLE_SET | RAM156_ENABLE_SET | RAM155_ENABLE_SET | RAM154_ENABLE_SET | RAM153_ENABLE_SET | RAM152_ENABLE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM151_ENABLE_SET | RAM150_ENABLE_SET | RAM149_ENABLE_SET | RAM148_ENABLE_SET | RAM147_ENABLE_SET | RAM146_ENABLE_SET | RAM145_ENABLE_SET | RAM144_ENABLE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM143_ENABLE_SET | RAM142_ENABLE_SET | RAM141_ENABLE_SET | RAM140_ENABLE_SET | RAM139_ENABLE_SET | RAM138_ENABLE_SET | RAM137_ENABLE_SET | RAM136_ENABLE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM135_ENABLE_SET | RAM134_ENABLE_SET | RAM133_ENABLE_SET | RAM132_ENABLE_SET | RAM131_ENABLE_SET | RAM130_ENABLE_SET | RAM129_ENABLE_SET | RAM128_ENABLE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-31. ECC_SEC_ENABLE_SET_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM159_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 159. Write 1h to enable the interrupt |
| 30 | RAM158_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 158. Write 1h to enable the interrupt |
| 29 | RAM157_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 157. Write 1h to enable the interrupt |
| 28 | RAM156_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 156. Write 1h to enable the interrupt |
| 27 | RAM155_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 155. Write 1h to enable the interrupt |
| 26 | RAM154_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 154. Write 1h to enable the interrupt |
| 25 | RAM153_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 153. Write 1h to enable the interrupt |
| 24 | RAM152_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 152. Write 1h to enable the interrupt |
| 23 | RAM151_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 151. Write 1h to enable the interrupt |
| 22 | RAM150_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 150. Write 1h to enable the interrupt |

Table 20-31. ECC_SEC_ENABLE_SET_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM149_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 149. Write 1h to enable the interrupt |
| 20 | RAM148_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 148. Write 1h to enable the interrupt |
| 19 | RAM147_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 147. Write 1h to enable the interrupt |
| 18 | RAM146_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 146. Write 1h to enable the interrupt |
| 17 | RAM145_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 145. Write 1h to enable the interrupt |
| 16 | RAM144_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 144. Write 1h to enable the interrupt |
| 15 | RAM143_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 143. Write 1h to enable the interrupt |
| 14 | RAM142_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 142. Write 1h to enable the interrupt |
| 13 | RAM141_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 141. Write 1h to enable the interrupt |
| 12 | RAM140_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 140. Write 1h to enable the interrupt |
| 11 | RAM139_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 139. Write 1h to enable the interrupt |
| 10 | RAM138_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 138. Write 1h to enable the interrupt |
| 9 | RAM137_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 137. Write 1h to enable the interrupt |
| 8 | RAM136_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 136. Write 1h to enable the interrupt |
| 7 | RAM135_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 135. Write 1h to enable the interrupt |
| 6 | RAM134_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 134. Write 1h to enable the interrupt |
| 5 | RAM133_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 133. Write 1h to enable the interrupt |
| 4 | RAM132_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 132. Write 1h to enable the interrupt |
| 3 | RAM131_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 131. Write 1h to enable the interrupt |
| 2 | RAM130_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 130. Write 1h to enable the interrupt |
| 1 | RAM129_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 129. Write 1h to enable the interrupt |
| 0 | RAM128_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 128. Write 1h to enable the interrupt |

20.31 ECC_SEC_ENABLE_SET_REG5 Register (Offset = 94h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG5 is shown in [Figure 20-31](#) and described in [Table 20-32](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-31. ECC_SEC_ENABLE_SET_REG5 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM191_ENAB LE_SET | RAM190_ENAB LE_SET | RAM189_ENAB LE_SET | RAM188_ENAB LE_SET | RAM187_ENAB LE_SET | RAM186_ENAB LE_SET | RAM185_ENAB LE_SET | RAM184_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM183_ENAB LE_SET | RAM182_ENAB LE_SET | RAM181_ENAB LE_SET | RAM180_ENAB LE_SET | RAM179_ENAB LE_SET | RAM178_ENAB LE_SET | RAM177_ENAB LE_SET | RAM176_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM175_ENAB LE_SET | RAM174_ENAB LE_SET | RAM173_ENAB LE_SET | RAM172_ENAB LE_SET | RAM171_ENAB LE_SET | RAM170_ENAB LE_SET | RAM169_ENAB LE_SET | RAM168_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM167_ENAB LE_SET | RAM166_ENAB LE_SET | RAM165_ENAB LE_SET | RAM164_ENAB LE_SET | RAM163_ENAB LE_SET | RAM162_ENAB LE_SET | RAM161_ENAB LE_SET | RAM160_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-32. ECC_SEC_ENABLE_SET_REG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM191_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 191. Write 1h to enable the interrupt |
| 30 | RAM190_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 190. Write 1h to enable the interrupt |
| 29 | RAM189_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 189. Write 1h to enable the interrupt |
| 28 | RAM188_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 188. Write 1h to enable the interrupt |
| 27 | RAM187_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 187. Write 1h to enable the interrupt |
| 26 | RAM186_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 186. Write 1h to enable the interrupt |
| 25 | RAM185_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 185. Write 1h to enable the interrupt |
| 24 | RAM184_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 184. Write 1h to enable the interrupt |
| 23 | RAM183_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 183. Write 1h to enable the interrupt |
| 22 | RAM182_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 182. Write 1h to enable the interrupt |

Table 20-32. ECC_SEC_ENABLE_SET_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM181_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 181. Write 1h to enable the interrupt |
| 20 | RAM180_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 180. Write 1h to enable the interrupt |
| 19 | RAM179_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 179. Write 1h to enable the interrupt |
| 18 | RAM178_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 178. Write 1h to enable the interrupt |
| 17 | RAM177_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 177. Write 1h to enable the interrupt |
| 16 | RAM176_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 176. Write 1h to enable the interrupt |
| 15 | RAM175_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 175. Write 1h to enable the interrupt |
| 14 | RAM174_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 174. Write 1h to enable the interrupt |
| 13 | RAM173_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 173. Write 1h to enable the interrupt |
| 12 | RAM172_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 172. Write 1h to enable the interrupt |
| 11 | RAM171_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 171. Write 1h to enable the interrupt |
| 10 | RAM170_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 170. Write 1h to enable the interrupt |
| 9 | RAM169_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 169. Write 1h to enable the interrupt |
| 8 | RAM168_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 168. Write 1h to enable the interrupt |
| 7 | RAM167_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 167. Write 1h to enable the interrupt |
| 6 | RAM166_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 166. Write 1h to enable the interrupt |
| 5 | RAM165_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 165. Write 1h to enable the interrupt |
| 4 | RAM164_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 164. Write 1h to enable the interrupt |
| 3 | RAM163_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 163. Write 1h to enable the interrupt |
| 2 | RAM162_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 162. Write 1h to enable the interrupt |
| 1 | RAM161_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 161. Write 1h to enable the interrupt |
| 0 | RAM160_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 160. Write 1h to enable the interrupt |

20.32 ECC_SEC_ENABLE_SET_REG6 Register (Offset = 98h) [reset = 0h]

ECC_SEC_ENABLE_SET_REG6 is shown in [Figure 20-32](#) and described in [Table 20-33](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-32. ECC_SEC_ENABLE_SET_REG6 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM223_ENAB LE_SET | RAM222_ENAB LE_SET | RAM221_ENAB LE_SET | RAM220_ENAB LE_SET | RAM219_ENAB LE_SET | RAM218_ENAB LE_SET | RAM217_ENAB LE_SET | RAM216_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM215_ENAB LE_SET | RAM214_ENAB LE_SET | RAM213_ENAB LE_SET | RAM212_ENAB LE_SET | RAM211_ENAB LE_SET | RAM210_ENAB LE_SET | RAM209_ENAB LE_SET | RAM208_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM207_ENAB LE_SET | RAM206_ENAB LE_SET | RAM205_ENAB LE_SET | RAM204_ENAB LE_SET | RAM203_ENAB LE_SET | RAM202_ENAB LE_SET | RAM201_ENAB LE_SET | RAM200_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM199_ENAB LE_SET | RAM198_ENAB LE_SET | RAM197_ENAB LE_SET | RAM196_ENAB LE_SET | RAM195_ENAB LE_SET | RAM194_ENAB LE_SET | RAM193_ENAB LE_SET | RAM192_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-33. ECC_SEC_ENABLE_SET_REG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM223_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 223. Write 1h to enable the interrupt |
| 30 | RAM222_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 222. Write 1h to enable the interrupt |
| 29 | RAM221_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 221. Write 1h to enable the interrupt |
| 28 | RAM220_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 220. Write 1h to enable the interrupt |
| 27 | RAM219_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 219. Write 1h to enable the interrupt |
| 26 | RAM218_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 218. Write 1h to enable the interrupt |
| 25 | RAM217_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 217. Write 1h to enable the interrupt |
| 24 | RAM216_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 216. Write 1h to enable the interrupt |
| 23 | RAM215_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 215. Write 1h to enable the interrupt |
| 22 | RAM214_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 214. Write 1h to enable the interrupt |

Table 20-33. ECC_SEC_ENABLE_SET_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM213_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 213. Write 1h to enable the interrupt |
| 20 | RAM212_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 212. Write 1h to enable the interrupt |
| 19 | RAM211_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 211. Write 1h to enable the interrupt |
| 18 | RAM210_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 210. Write 1h to enable the interrupt |
| 17 | RAM209_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 209. Write 1h to enable the interrupt |
| 16 | RAM208_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 208. Write 1h to enable the interrupt |
| 15 | RAM207_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 207. Write 1h to enable the interrupt |
| 14 | RAM206_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 206. Write 1h to enable the interrupt |
| 13 | RAM205_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 205. Write 1h to enable the interrupt |
| 12 | RAM204_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 204. Write 1h to enable the interrupt |
| 11 | RAM203_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 203. Write 1h to enable the interrupt |
| 10 | RAM202_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 202. Write 1h to enable the interrupt |
| 9 | RAM201_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 201. Write 1h to enable the interrupt |
| 8 | RAM200_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 200. Write 1h to enable the interrupt |
| 7 | RAM199_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 199. Write 1h to enable the interrupt |
| 6 | RAM198_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 198. Write 1h to enable the interrupt |
| 5 | RAM197_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 197. Write 1h to enable the interrupt |
| 4 | RAM196_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 196. Write 1h to enable the interrupt |
| 3 | RAM195_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 195. Write 1h to enable the interrupt |
| 2 | RAM194_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 194. Write 1h to enable the interrupt |
| 1 | RAM193_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 193. Write 1h to enable the interrupt |
| 0 | RAM192_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 192. Write 1h to enable the interrupt |

20.33 ECC_SEC_ENABLE_SET_REG7 Register (Offset = 9Ch) [reset = 0h]

ECC_SEC_ENABLE_SET_REG7 is shown in [Figure 20-33](#) and described in [Table 20-34](#).

Return to [Summary Table](#).

Interrupt enable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-33. ECC_SEC_ENABLE_SET_REG7 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM255_ENAB LE_SET | RAM254_ENAB LE_SET | RAM253_ENAB LE_SET | RAM252_ENAB LE_SET | RAM251_ENAB LE_SET | RAM250_ENAB LE_SET | RAM249_ENAB LE_SET | RAM248_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM247_ENAB LE_SET | RAM246_ENAB LE_SET | RAM245_ENAB LE_SET | RAM244_ENAB LE_SET | RAM243_ENAB LE_SET | RAM242_ENAB LE_SET | RAM241_ENAB LE_SET | RAM240_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM239_ENAB LE_SET | RAM238_ENAB LE_SET | RAM237_ENAB LE_SET | RAM236_ENAB LE_SET | RAM235_ENAB LE_SET | RAM234_ENAB LE_SET | RAM233_ENAB LE_SET | RAM232_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM231_ENAB LE_SET | RAM230_ENAB LE_SET | RAM229_ENAB LE_SET | RAM228_ENAB LE_SET | RAM227_ENAB LE_SET | RAM226_ENAB LE_SET | RAM225_ENAB LE_SET | RAM224_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-34. ECC_SEC_ENABLE_SET_REG7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM255_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 255. Write 1h to enable the interrupt |
| 30 | RAM254_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 254. Write 1h to enable the interrupt |
| 29 | RAM253_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 253. Write 1h to enable the interrupt |
| 28 | RAM252_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 252. Write 1h to enable the interrupt |
| 27 | RAM251_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 251. Write 1h to enable the interrupt |
| 26 | RAM250_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 250. Write 1h to enable the interrupt |
| 25 | RAM249_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 249. Write 1h to enable the interrupt |
| 24 | RAM248_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 248. Write 1h to enable the interrupt |
| 23 | RAM247_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 247. Write 1h to enable the interrupt |
| 22 | RAM246_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 246. Write 1h to enable the interrupt |

Table 20-34. ECC_SEC_ENABLE_SET_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM245_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 245. Write 1h to enable the interrupt |
| 20 | RAM244_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 244. Write 1h to enable the interrupt |
| 19 | RAM243_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 243. Write 1h to enable the interrupt |
| 18 | RAM242_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 242. Write 1h to enable the interrupt |
| 17 | RAM241_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 241. Write 1h to enable the interrupt |
| 16 | RAM240_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 240. Write 1h to enable the interrupt |
| 15 | RAM239_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 239. Write 1h to enable the interrupt |
| 14 | RAM238_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 238. Write 1h to enable the interrupt |
| 13 | RAM237_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 237. Write 1h to enable the interrupt |
| 12 | RAM236_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 236. Write 1h to enable the interrupt |
| 11 | RAM235_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 235. Write 1h to enable the interrupt |
| 10 | RAM234_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 234. Write 1h to enable the interrupt |
| 9 | RAM233_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 233. Write 1h to enable the interrupt |
| 8 | RAM232_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 232. Write 1h to enable the interrupt |
| 7 | RAM231_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 231. Write 1h to enable the interrupt |
| 6 | RAM230_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 230. Write 1h to enable the interrupt |
| 5 | RAM229_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 229. Write 1h to enable the interrupt |
| 4 | RAM228_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 228. Write 1h to enable the interrupt |
| 3 | RAM227_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 227. Write 1h to enable the interrupt |
| 2 | RAM226_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 226. Write 1h to enable the interrupt |
| 1 | RAM225_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 225. Write 1h to enable the interrupt |
| 0 | RAM224_ENABLE_SET | R/W1S | 0h | Correctable error interrupt enable for ECC endpoint with ID = 224. Write 1h to enable the interrupt |

20.34 ECC_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG0 is shown in [Figure 20-34](#) and described in [Table 20-35](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-34. ECC_SEC_ENABLE_CLR_REG0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM31_ENABL E_CLR | RAM30_ENABL E_CLR | RAM29_ENABL E_CLR | RAM28_ENABL E_CLR | RAM27_ENABL E_CLR | RAM26_ENABL E_CLR | RAM25_ENABL E_CLR | RAM24_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM23_ENABL E_CLR | RAM22_ENABL E_CLR | RAM21_ENABL E_CLR | RAM20_ENABL E_CLR | RAM19_ENABL E_CLR | RAM18_ENABL E_CLR | RAM17_ENABL E_CLR | RAM16_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM15_ENABL E_CLR | RAM14_ENABL E_CLR | RAM13_ENABL E_CLR | RAM12_ENABL E_CLR | RAM11_ENABL E_CLR | RAM10_ENABL E_CLR | RAM9_ENABL E_CLR | RAM8_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM7_ENABL E_CLR | RAM6_ENABL E_CLR | RAM5_ENABL E_CLR | RAM4_ENABL E_CLR | RAM3_ENABL E_CLR | RAM2_ENABL E_CLR | RAM1_ENABL E_CLR | RAM0_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-35. ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM31_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 31. Write 1h to disable the interrupt |
| 30 | RAM30_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 30. Write 1h to disable the interrupt |
| 29 | RAM29_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 29. Write 1h to disable the interrupt |
| 28 | RAM28_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 28. Write 1h to disable the interrupt |
| 27 | RAM27_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 27. Write 1h to disable the interrupt |
| 26 | RAM26_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 26. Write 1h to disable the interrupt |
| 25 | RAM25_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 25. Write 1h to disable the interrupt |
| 24 | RAM24_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 24. Write 1h to disable the interrupt |
| 23 | RAM23_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 23. Write 1h to disable the interrupt |
| 22 | RAM22_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 22. Write 1h to disable the interrupt |

Table 20-35. ECC_SEC_ENABLE_CLR_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM21_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 21. Write 1h to disable the interrupt |
| 20 | RAM20_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 20. Write 1h to disable the interrupt |
| 19 | RAM19_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 19. Write 1h to disable the interrupt |
| 18 | RAM18_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 18. Write 1h to disable the interrupt |
| 17 | RAM17_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 17. Write 1h to disable the interrupt |
| 16 | RAM16_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 16. Write 1h to disable the interrupt |
| 15 | RAM15_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 15. Write 1h to disable the interrupt |
| 14 | RAM14_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 14. Write 1h to disable the interrupt |
| 13 | RAM13_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 13. Write 1h to disable the interrupt |
| 12 | RAM12_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 12. Write 1h to disable the interrupt |
| 11 | RAM11_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 11. Write 1h to disable the interrupt |
| 10 | RAM10_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 10. Write 1h to disable the interrupt |
| 9 | RAM9_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 9. Write 1h to disable the interrupt |
| 8 | RAM8_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 8. Write 1h to disable the interrupt |
| 7 | RAM7_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 7. Write 1h to disable the interrupt |
| 6 | RAM6_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 6. Write 1h to disable the interrupt |
| 5 | RAM5_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 5. Write 1h to disable the interrupt |
| 4 | RAM4_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 4. Write 1h to disable the interrupt |
| 3 | RAM3_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 3. Write 1h to disable the interrupt |
| 2 | RAM2_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 2. Write 1h to disable the interrupt |
| 1 | RAM1_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 1. Write 1h to disable the interrupt |
| 0 | RAM0_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 0. Write 1h to disable the interrupt |

20.35 ECC_SEC_ENABLE_CLR_REG1 Register (Offset = C4h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG1 is shown in [Figure 20-35](#) and described in [Table 20-36](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-35. ECC_SEC_ENABLE_CLR_REG1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM63_ENABL E_CLR | RAM62_ENABL E_CLR | RAM61_ENABL E_CLR | RAM60_ENABL E_CLR | RAM59_ENABL E_CLR | RAM58_ENABL E_CLR | RAM57_ENABL E_CLR | RAM56_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM55_ENABL E_CLR | RAM54_ENABL E_CLR | RAM53_ENABL E_CLR | RAM52_ENABL E_CLR | RAM51_ENABL E_CLR | RAM50_ENABL E_CLR | RAM49_ENABL E_CLR | RAM48_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM47_ENABL E_CLR | RAM46_ENABL E_CLR | RAM45_ENABL E_CLR | RAM44_ENABL E_CLR | RAM43_ENABL E_CLR | RAM42_ENABL E_CLR | RAM41_ENABL E_CLR | RAM40_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM39_ENABL E_CLR | RAM38_ENABL E_CLR | RAM37_ENABL E_CLR | RAM36_ENABL E_CLR | RAM35_ENABL E_CLR | RAM34_ENABL E_CLR | RAM33_ENABL E_CLR | RAM32_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-36. ECC_SEC_ENABLE_CLR_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM63_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 63. Write 1h to disable the interrupt |
| 30 | RAM62_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 62. Write 1h to disable the interrupt |
| 29 | RAM61_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 61. Write 1h to disable the interrupt |
| 28 | RAM60_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 60. Write 1h to disable the interrupt |
| 27 | RAM59_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 59. Write 1h to disable the interrupt |
| 26 | RAM58_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 58. Write 1h to disable the interrupt |
| 25 | RAM57_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 57. Write 1h to disable the interrupt |
| 24 | RAM56_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 56. Write 1h to disable the interrupt |
| 23 | RAM55_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 55. Write 1h to disable the interrupt |
| 22 | RAM54_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 54. Write 1h to disable the interrupt |

Table 20-36. ECC_SEC_ENABLE_CLR_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM53_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 53. Write 1h to disable the interrupt |
| 20 | RAM52_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 52. Write 1h to disable the interrupt |
| 19 | RAM51_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 51. Write 1h to disable the interrupt |
| 18 | RAM50_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 50. Write 1h to disable the interrupt |
| 17 | RAM49_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 49. Write 1h to disable the interrupt |
| 16 | RAM48_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 48. Write 1h to disable the interrupt |
| 15 | RAM47_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 47. Write 1h to disable the interrupt |
| 14 | RAM46_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 46. Write 1h to disable the interrupt |
| 13 | RAM45_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 45. Write 1h to disable the interrupt |
| 12 | RAM44_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 44. Write 1h to disable the interrupt |
| 11 | RAM43_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 43. Write 1h to disable the interrupt |
| 10 | RAM42_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 42. Write 1h to disable the interrupt |
| 9 | RAM41_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 41. Write 1h to disable the interrupt |
| 8 | RAM40_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 40. Write 1h to disable the interrupt |
| 7 | RAM39_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 39. Write 1h to disable the interrupt |
| 6 | RAM38_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 38. Write 1h to disable the interrupt |
| 5 | RAM37_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 37. Write 1h to disable the interrupt |
| 4 | RAM36_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 36. Write 1h to disable the interrupt |
| 3 | RAM35_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 35. Write 1h to disable the interrupt |
| 2 | RAM34_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 34. Write 1h to disable the interrupt |
| 1 | RAM33_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 33. Write 1h to disable the interrupt |
| 0 | RAM32_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 32. Write 1h to disable the interrupt |

20.36 ECC_SEC_ENABLE_CLR_REG2 Register (Offset = C8h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG2 is shown in [Figure 20-36](#) and described in [Table 20-37](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-36. ECC_SEC_ENABLE_CLR_REG2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM95_ENABL E_CLR | RAM94_ENABL E_CLR | RAM93_ENABL E_CLR | RAM92_ENABL E_CLR | RAM91_ENABL E_CLR | RAM90_ENABL E_CLR | RAM89_ENABL E_CLR | RAM88_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM87_ENABL E_CLR | RAM86_ENABL E_CLR | RAM85_ENABL E_CLR | RAM84_ENABL E_CLR | RAM83_ENABL E_CLR | RAM82_ENABL E_CLR | RAM81_ENABL E_CLR | RAM80_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM79_ENABL E_CLR | RAM78_ENABL E_CLR | RAM77_ENABL E_CLR | RAM76_ENABL E_CLR | RAM75_ENABL E_CLR | RAM74_ENABL E_CLR | RAM73_ENABL E_CLR | RAM72_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM71_ENABL E_CLR | RAM70_ENABL E_CLR | RAM69_ENABL E_CLR | RAM68_ENABL E_CLR | RAM67_ENABL E_CLR | RAM66_ENABL E_CLR | RAM65_ENABL E_CLR | RAM64_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-37. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM95_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 95. Write 1h to disable the interrupt |
| 30 | RAM94_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 94. Write 1h to disable the interrupt |
| 29 | RAM93_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 93. Write 1h to disable the interrupt |
| 28 | RAM92_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 92. Write 1h to disable the interrupt |
| 27 | RAM91_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 91. Write 1h to disable the interrupt |
| 26 | RAM90_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 90. Write 1h to disable the interrupt |
| 25 | RAM89_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 89. Write 1h to disable the interrupt |
| 24 | RAM88_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 88. Write 1h to disable the interrupt |
| 23 | RAM87_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 87. Write 1h to disable the interrupt |
| 22 | RAM86_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 86. Write 1h to disable the interrupt |

Table 20-37. ECC_SEC_ENABLE_CLR_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM85_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 85. Write 1h to disable the interrupt |
| 20 | RAM84_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 84. Write 1h to disable the interrupt |
| 19 | RAM83_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 83. Write 1h to disable the interrupt |
| 18 | RAM82_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 82. Write 1h to disable the interrupt |
| 17 | RAM81_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 81. Write 1h to disable the interrupt |
| 16 | RAM80_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 80. Write 1h to disable the interrupt |
| 15 | RAM79_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 79. Write 1h to disable the interrupt |
| 14 | RAM78_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 78. Write 1h to disable the interrupt |
| 13 | RAM77_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 77. Write 1h to disable the interrupt |
| 12 | RAM76_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 76. Write 1h to disable the interrupt |
| 11 | RAM75_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 75. Write 1h to disable the interrupt |
| 10 | RAM74_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 74. Write 1h to disable the interrupt |
| 9 | RAM73_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 73. Write 1h to disable the interrupt |
| 8 | RAM72_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 72. Write 1h to disable the interrupt |
| 7 | RAM71_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 71. Write 1h to disable the interrupt |
| 6 | RAM70_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 70. Write 1h to disable the interrupt |
| 5 | RAM69_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 69. Write 1h to disable the interrupt |
| 4 | RAM68_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 68. Write 1h to disable the interrupt |
| 3 | RAM67_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 67. Write 1h to disable the interrupt |
| 2 | RAM66_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 66. Write 1h to disable the interrupt |
| 1 | RAM65_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 65. Write 1h to disable the interrupt |
| 0 | RAM64_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 64. Write 1h to disable the interrupt |

20.37 ECC_SEC_ENABLE_CLR_REG3 Register (Offset = CCh) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG3 is shown in [Figure 20-37](#) and described in [Table 20-38](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-37. ECC_SEC_ENABLE_CLR_REG3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM127_ENAB LE_CLR | RAM126_ENAB LE_CLR | RAM125_ENAB LE_CLR | RAM124_ENAB LE_CLR | RAM123_ENAB LE_CLR | RAM122_ENAB LE_CLR | RAM121_ENAB LE_CLR | RAM120_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM119_ENAB LE_CLR | RAM118_ENAB LE_CLR | RAM117_ENAB LE_CLR | RAM116_ENAB LE_CLR | RAM115_ENAB LE_CLR | RAM114_ENAB LE_CLR | RAM113_ENAB LE_CLR | RAM112_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM111_ENAB LE_CLR | RAM110_ENAB LE_CLR | RAM109_ENAB LE_CLR | RAM108_ENAB LE_CLR | RAM107_ENAB LE_CLR | RAM106_ENAB LE_CLR | RAM105_ENAB LE_CLR | RAM104_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM103_ENAB LE_CLR | RAM102_ENAB LE_CLR | RAM101_ENAB LE_CLR | RAM100_ENAB LE_CLR | RAM99_ENABL E_CLR | RAM98_ENABL E_CLR | RAM97_ENABL E_CLR | RAM96_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-38. ECC_SEC_ENABLE_CLR_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM127_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 127. Write 1h to disable the interrupt |
| 30 | RAM126_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 126. Write 1h to disable the interrupt |
| 29 | RAM125_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 125. Write 1h to disable the interrupt |
| 28 | RAM124_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 124. Write 1h to disable the interrupt |
| 27 | RAM123_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 123. Write 1h to disable the interrupt |
| 26 | RAM122_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 122. Write 1h to disable the interrupt |
| 25 | RAM121_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 121. Write 1h to disable the interrupt |
| 24 | RAM120_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 120. Write 1h to disable the interrupt |
| 23 | RAM119_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 119. Write 1h to disable the interrupt |
| 22 | RAM118_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 118. Write 1h to disable the interrupt |

Table 20-38. ECC_SEC_ENABLE_CLR_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM117_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 117. Write 1h to disable the interrupt |
| 20 | RAM116_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 116. Write 1h to disable the interrupt |
| 19 | RAM115_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 115. Write 1h to disable the interrupt |
| 18 | RAM114_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 114. Write 1h to disable the interrupt |
| 17 | RAM113_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 113. Write 1h to disable the interrupt |
| 16 | RAM112_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 112. Write 1h to disable the interrupt |
| 15 | RAM111_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 111. Write 1h to disable the interrupt |
| 14 | RAM110_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 110. Write 1h to disable the interrupt |
| 13 | RAM109_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 109. Write 1h to disable the interrupt |
| 12 | RAM108_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 108. Write 1h to disable the interrupt |
| 11 | RAM107_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 107. Write 1h to disable the interrupt |
| 10 | RAM106_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 106. Write 1h to disable the interrupt |
| 9 | RAM105_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 105. Write 1h to disable the interrupt |
| 8 | RAM104_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 104. Write 1h to disable the interrupt |
| 7 | RAM103_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 103. Write 1h to disable the interrupt |
| 6 | RAM102_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 102. Write 1h to disable the interrupt |
| 5 | RAM101_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 101. Write 1h to disable the interrupt |
| 4 | RAM100_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 100. Write 1h to disable the interrupt |
| 3 | RAM99_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 99. Write 1h to disable the interrupt |
| 2 | RAM98_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 98. Write 1h to disable the interrupt |
| 1 | RAM97_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 97. Write 1h to disable the interrupt |
| 0 | RAM96_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 96. Write 1h to disable the interrupt |

20.38 ECC_SEC_ENABLE_CLR_REG4 Register (Offset = D0h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG4 is shown in [Figure 20-38](#) and described in [Table 20-39](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-38. ECC_SEC_ENABLE_CLR_REG4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| RAM159_ENABLE_CLR | RAM158_ENABLE_CLR | RAM157_ENABLE_CLR | RAM156_ENABLE_CLR | RAM155_ENABLE_CLR | RAM154_ENABLE_CLR | RAM153_ENABLE_CLR | RAM152_ENABLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM151_ENABLE_CLR | RAM150_ENABLE_CLR | RAM149_ENABLE_CLR | RAM148_ENABLE_CLR | RAM147_ENABLE_CLR | RAM146_ENABLE_CLR | RAM145_ENABLE_CLR | RAM144_ENABLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM143_ENABLE_CLR | RAM142_ENABLE_CLR | RAM141_ENABLE_CLR | RAM140_ENABLE_CLR | RAM139_ENABLE_CLR | RAM138_ENABLE_CLR | RAM137_ENABLE_CLR | RAM136_ENABLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM135_ENABLE_CLR | RAM134_ENABLE_CLR | RAM133_ENABLE_CLR | RAM132_ENABLE_CLR | RAM131_ENABLE_CLR | RAM130_ENABLE_CLR | RAM129_ENABLE_CLR | RAM128_ENABLE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-39. ECC_SEC_ENABLE_CLR_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM159_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 159. Write 1h to disable the interrupt |
| 30 | RAM158_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 158. Write 1h to disable the interrupt |
| 29 | RAM157_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 157. Write 1h to disable the interrupt |
| 28 | RAM156_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 156. Write 1h to disable the interrupt |
| 27 | RAM155_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 155. Write 1h to disable the interrupt |
| 26 | RAM154_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 154. Write 1h to disable the interrupt |
| 25 | RAM153_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 153. Write 1h to disable the interrupt |
| 24 | RAM152_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 152. Write 1h to disable the interrupt |
| 23 | RAM151_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 151. Write 1h to disable the interrupt |
| 22 | RAM150_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 150. Write 1h to disable the interrupt |

Table 20-39. ECC_SEC_ENABLE_CLR_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM149_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 149. Write 1h to disable the interrupt |
| 20 | RAM148_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 148. Write 1h to disable the interrupt |
| 19 | RAM147_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 147. Write 1h to disable the interrupt |
| 18 | RAM146_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 146. Write 1h to disable the interrupt |
| 17 | RAM145_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 145. Write 1h to disable the interrupt |
| 16 | RAM144_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 144. Write 1h to disable the interrupt |
| 15 | RAM143_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 143. Write 1h to disable the interrupt |
| 14 | RAM142_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 142. Write 1h to disable the interrupt |
| 13 | RAM141_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 141. Write 1h to disable the interrupt |
| 12 | RAM140_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 140. Write 1h to disable the interrupt |
| 11 | RAM139_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 139. Write 1h to disable the interrupt |
| 10 | RAM138_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 138. Write 1h to disable the interrupt |
| 9 | RAM137_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 137. Write 1h to disable the interrupt |
| 8 | RAM136_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 136. Write 1h to disable the interrupt |
| 7 | RAM135_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 135. Write 1h to disable the interrupt |
| 6 | RAM134_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 134. Write 1h to disable the interrupt |
| 5 | RAM133_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 133. Write 1h to disable the interrupt |
| 4 | RAM132_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 132. Write 1h to disable the interrupt |
| 3 | RAM131_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 131. Write 1h to disable the interrupt |
| 2 | RAM130_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 130. Write 1h to disable the interrupt |
| 1 | RAM129_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 129. Write 1h to disable the interrupt |
| 0 | RAM128_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 128. Write 1h to disable the interrupt |

20.39 ECC_SEC_ENABLE_CLR_REG5 Register (Offset = D4h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG5 is shown in [Figure 20-39](#) and described in [Table 20-40](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-39. ECC_SEC_ENABLE_CLR_REG5 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM191_ENAB LE_CLR | RAM190_ENAB LE_CLR | RAM189_ENAB LE_CLR | RAM188_ENAB LE_CLR | RAM187_ENAB LE_CLR | RAM186_ENAB LE_CLR | RAM185_ENAB LE_CLR | RAM184_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM183_ENAB LE_CLR | RAM182_ENAB LE_CLR | RAM181_ENAB LE_CLR | RAM180_ENAB LE_CLR | RAM179_ENAB LE_CLR | RAM178_ENAB LE_CLR | RAM177_ENAB LE_CLR | RAM176_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM175_ENAB LE_CLR | RAM174_ENAB LE_CLR | RAM173_ENAB LE_CLR | RAM172_ENAB LE_CLR | RAM171_ENAB LE_CLR | RAM170_ENAB LE_CLR | RAM169_ENAB LE_CLR | RAM168_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM167_ENAB LE_CLR | RAM166_ENAB LE_CLR | RAM165_ENAB LE_CLR | RAM164_ENAB LE_CLR | RAM163_ENAB LE_CLR | RAM162_ENAB LE_CLR | RAM161_ENAB LE_CLR | RAM160_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-40. ECC_SEC_ENABLE_CLR_REG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM191_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 191. Write 1h to disable the interrupt |
| 30 | RAM190_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 190. Write 1h to disable the interrupt |
| 29 | RAM189_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 189. Write 1h to disable the interrupt |
| 28 | RAM188_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 188. Write 1h to disable the interrupt |
| 27 | RAM187_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 187. Write 1h to disable the interrupt |
| 26 | RAM186_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 186. Write 1h to disable the interrupt |
| 25 | RAM185_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 185. Write 1h to disable the interrupt |
| 24 | RAM184_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 184. Write 1h to disable the interrupt |
| 23 | RAM183_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 183. Write 1h to disable the interrupt |
| 22 | RAM182_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 182. Write 1h to disable the interrupt |

Table 20-40. ECC_SEC_ENABLE_CLR_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM181_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 181. Write 1h to disable the interrupt |
| 20 | RAM180_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 180. Write 1h to disable the interrupt |
| 19 | RAM179_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 179. Write 1h to disable the interrupt |
| 18 | RAM178_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 178. Write 1h to disable the interrupt |
| 17 | RAM177_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 177. Write 1h to disable the interrupt |
| 16 | RAM176_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 176. Write 1h to disable the interrupt |
| 15 | RAM175_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 175. Write 1h to disable the interrupt |
| 14 | RAM174_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 174. Write 1h to disable the interrupt |
| 13 | RAM173_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 173. Write 1h to disable the interrupt |
| 12 | RAM172_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 172. Write 1h to disable the interrupt |
| 11 | RAM171_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 171. Write 1h to disable the interrupt |
| 10 | RAM170_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 170. Write 1h to disable the interrupt |
| 9 | RAM169_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 169. Write 1h to disable the interrupt |
| 8 | RAM168_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 168. Write 1h to disable the interrupt |
| 7 | RAM167_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 167. Write 1h to disable the interrupt |
| 6 | RAM166_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 166. Write 1h to disable the interrupt |
| 5 | RAM165_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 165. Write 1h to disable the interrupt |
| 4 | RAM164_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 164. Write 1h to disable the interrupt |
| 3 | RAM163_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 163. Write 1h to disable the interrupt |
| 2 | RAM162_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 162. Write 1h to disable the interrupt |
| 1 | RAM161_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 161. Write 1h to disable the interrupt |
| 0 | RAM160_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 160. Write 1h to disable the interrupt |

20.40 ECC_SEC_ENABLE_CLR_REG6 Register (Offset = D8h) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG6 is shown in [Figure 20-40](#) and described in [Table 20-41](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-40. ECC_SEC_ENABLE_CLR_REG6 Register

| | | | | | | | |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM223_ENAB LE_CLR | RAM222_ENAB LE_CLR | RAM221_ENAB LE_CLR | RAM220_ENAB LE_CLR | RAM219_ENAB LE_CLR | RAM218_ENAB LE_CLR | RAM217_ENAB LE_CLR | RAM216_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM215_ENAB LE_CLR | RAM214_ENAB LE_CLR | RAM213_ENAB LE_CLR | RAM212_ENAB LE_CLR | RAM211_ENAB LE_CLR | RAM210_ENAB LE_CLR | RAM209_ENAB LE_CLR | RAM208_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM207_ENAB LE_CLR | RAM206_ENAB LE_CLR | RAM205_ENAB LE_CLR | RAM204_ENAB LE_CLR | RAM203_ENAB LE_CLR | RAM202_ENAB LE_CLR | RAM201_ENAB LE_CLR | RAM200_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM199_ENAB LE_CLR | RAM198_ENAB LE_CLR | RAM197_ENAB LE_CLR | RAM196_ENAB LE_CLR | RAM195_ENAB LE_CLR | RAM194_ENAB LE_CLR | RAM193_ENAB LE_CLR | RAM192_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-41. ECC_SEC_ENABLE_CLR_REG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM223_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 223. Write 1h to disable the interrupt |
| 30 | RAM222_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 222. Write 1h to disable the interrupt |
| 29 | RAM221_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 221. Write 1h to disable the interrupt |
| 28 | RAM220_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 220. Write 1h to disable the interrupt |
| 27 | RAM219_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 219. Write 1h to disable the interrupt |
| 26 | RAM218_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 218. Write 1h to disable the interrupt |
| 25 | RAM217_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 217. Write 1h to disable the interrupt |
| 24 | RAM216_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 216. Write 1h to disable the interrupt |
| 23 | RAM215_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 215. Write 1h to disable the interrupt |
| 22 | RAM214_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 214. Write 1h to disable the interrupt |

Table 20-41. ECC_SEC_ENABLE_CLR_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM213_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 213. Write 1h to disable the interrupt |
| 20 | RAM212_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 212. Write 1h to disable the interrupt |
| 19 | RAM211_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 211. Write 1h to disable the interrupt |
| 18 | RAM210_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 210. Write 1h to disable the interrupt |
| 17 | RAM209_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 209. Write 1h to disable the interrupt |
| 16 | RAM208_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 208. Write 1h to disable the interrupt |
| 15 | RAM207_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 207. Write 1h to disable the interrupt |
| 14 | RAM206_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 206. Write 1h to disable the interrupt |
| 13 | RAM205_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 205. Write 1h to disable the interrupt |
| 12 | RAM204_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 204. Write 1h to disable the interrupt |
| 11 | RAM203_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 203. Write 1h to disable the interrupt |
| 10 | RAM202_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 202. Write 1h to disable the interrupt |
| 9 | RAM201_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 201. Write 1h to disable the interrupt |
| 8 | RAM200_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 200. Write 1h to disable the interrupt |
| 7 | RAM199_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 199. Write 1h to disable the interrupt |
| 6 | RAM198_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 198. Write 1h to disable the interrupt |
| 5 | RAM197_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 197. Write 1h to disable the interrupt |
| 4 | RAM196_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 196. Write 1h to disable the interrupt |
| 3 | RAM195_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 195. Write 1h to disable the interrupt |
| 2 | RAM194_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 194. Write 1h to disable the interrupt |
| 1 | RAM193_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 193. Write 1h to disable the interrupt |
| 0 | RAM192_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 192. Write 1h to disable the interrupt |

20.41 ECC_SEC_ENABLE_CLR_REG7 Register (Offset = DCh) [reset = 0h]

ECC_SEC_ENABLE_CLR_REG7 is shown in [Figure 20-41](#) and described in [Table 20-42](#).

Return to [Summary Table](#).

Interrupt disable register for correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-41. ECC_SEC_ENABLE_CLR_REG7 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM255_ENAB LE_CLR | RAM254_ENAB LE_CLR | RAM253_ENAB LE_CLR | RAM252_ENAB LE_CLR | RAM251_ENAB LE_CLR | RAM250_ENAB LE_CLR | RAM249_ENAB LE_CLR | RAM248_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM247_ENAB LE_CLR | RAM246_ENAB LE_CLR | RAM245_ENAB LE_CLR | RAM244_ENAB LE_CLR | RAM243_ENAB LE_CLR | RAM242_ENAB LE_CLR | RAM241_ENAB LE_CLR | RAM240_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM239_ENAB LE_CLR | RAM238_ENAB LE_CLR | RAM237_ENAB LE_CLR | RAM236_ENAB LE_CLR | RAM235_ENAB LE_CLR | RAM234_ENAB LE_CLR | RAM233_ENAB LE_CLR | RAM232_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM231_ENAB LE_CLR | RAM230_ENAB LE_CLR | RAM229_ENAB LE_CLR | RAM228_ENAB LE_CLR | RAM227_ENAB LE_CLR | RAM226_ENAB LE_CLR | RAM225_ENAB LE_CLR | RAM224_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-42. ECC_SEC_ENABLE_CLR_REG7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 31 | RAM255_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 255. Write 1h to disable the interrupt |
| 30 | RAM254_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 254. Write 1h to disable the interrupt |
| 29 | RAM253_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 253. Write 1h to disable the interrupt |
| 28 | RAM252_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 252. Write 1h to disable the interrupt |
| 27 | RAM251_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 251. Write 1h to disable the interrupt |
| 26 | RAM250_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 250. Write 1h to disable the interrupt |
| 25 | RAM249_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 249. Write 1h to disable the interrupt |
| 24 | RAM248_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 248. Write 1h to disable the interrupt |
| 23 | RAM247_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 247. Write 1h to disable the interrupt |
| 22 | RAM246_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 246. Write 1h to disable the interrupt |

Table 20-42. ECC_SEC_ENABLE_CLR_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|---|
| 21 | RAM245_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 245. Write 1h to disable the interrupt |
| 20 | RAM244_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 244. Write 1h to disable the interrupt |
| 19 | RAM243_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 243. Write 1h to disable the interrupt |
| 18 | RAM242_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 242. Write 1h to disable the interrupt |
| 17 | RAM241_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 241. Write 1h to disable the interrupt |
| 16 | RAM240_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 240. Write 1h to disable the interrupt |
| 15 | RAM239_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 239. Write 1h to disable the interrupt |
| 14 | RAM238_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 238. Write 1h to disable the interrupt |
| 13 | RAM237_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 237. Write 1h to disable the interrupt |
| 12 | RAM236_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 236. Write 1h to disable the interrupt |
| 11 | RAM235_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 235. Write 1h to disable the interrupt |
| 10 | RAM234_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 234. Write 1h to disable the interrupt |
| 9 | RAM233_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 233. Write 1h to disable the interrupt |
| 8 | RAM232_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 232. Write 1h to disable the interrupt |
| 7 | RAM231_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 231. Write 1h to disable the interrupt |
| 6 | RAM230_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 230. Write 1h to disable the interrupt |
| 5 | RAM229_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 229. Write 1h to disable the interrupt |
| 4 | RAM228_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 228. Write 1h to disable the interrupt |
| 3 | RAM227_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 227. Write 1h to disable the interrupt |
| 2 | RAM226_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 226. Write 1h to disable the interrupt |
| 1 | RAM225_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 225. Write 1h to disable the interrupt |
| 0 | RAM224_ENABLE_CLR | R/W1C | 0h | Correctable error interrupt disable for ECC endpoint with ID = 224. Write 1h to disable the interrupt |

20.42 ECC_DED_EOI_REG Register (Offset = 13Ch) [reset = 0h]

ECC_DED_EOI_REG is shown in [Figure 20-42](#) and described in [Table 20-43](#).

Return to [Summary Table](#).

DED EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Figure 20-42. ECC_DED_EOI_REG Register

| | | | | | | | |
|----------|----|----|----|----|----|----|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | EOI_WR |
| R-0h | | | | | | | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-43. ECC_DED_EOI_REG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|--|
| 31-1 | RESERVED | R | 0 | Reserved |
| 0 | EOI_WR | R/W1S | 0h | Write of 1h to this register indicates that software has serviced the non-correctable interrupt and next interrupt can be sent to the host. This bit is self clearing and read returns a zero. |

20.43 ECC_DED_STATUS_REG0 Register (Offset = 140h) [reset = 0h]

ECC_DED_STATUS_REG0 is shown in [Figure 20-43](#) and described in [Table 20-44](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-43. ECC_DED_STATUS_REG0 Register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM31_PEND | RAM30_PEND | RAM29_PEND | RAM28_PEND | RAM27_PEND | RAM26_PEND | RAM25_PEND | RAM24_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM23_PEND | RAM22_PEND | RAM21_PEND | RAM20_PEND | RAM19_PEND | RAM18_PEND | RAM17_PEND | RAM16_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM15_PEND | RAM14_PEND | RAM13_PEND | RAM12_PEND | RAM11_PEND | RAM10_PEND | RAM9_PEND | RAM8_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM7_PEND | RAM6_PEND | RAM5_PEND | RAM4_PEND | RAM3_PEND | RAM2_PEND | RAM1_PEND | RAM0_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-44. ECC_DED_STATUS_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 31 | RAM31_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 31. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM30_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 30. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM29_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 29. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM28_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 28. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM27_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 27. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM26_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 26. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 25 | RAM25_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 25. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM24_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 24. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-44. ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 23 | RAM23_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 23. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM22_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 22. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM21_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 21. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM20_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 20. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM19_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 19. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM18_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 18. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM17_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 17. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM16_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 16. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM15_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 15. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM14_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 14. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 13 | RAM13_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 13. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM12_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 12. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM11_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 11. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM10_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 10. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM9_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 9. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM8_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 8. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-44. ECC_DED_STATUS_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------|-------|-------|--|
| 7 | RAM7_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 7. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM6_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 6. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM5_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 5. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM4_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 4. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM3_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 3. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM2_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 2. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 1 | RAM1_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 1. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM0_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 0. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.44 ECC_DED_STATUS_REG1 Register (Offset = 144h) [reset = 0h]

ECC_DED_STATUS_REG1 is shown in [Figure 20-44](#) and described in [Table 20-45](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-44. ECC_DED_STATUS_REG1 Register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM63_PEND | RAM62_PEND | RAM61_PEND | RAM60_PEND | RAM59_PEND | RAM58_PEND | RAM57_PEND | RAM56_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM55_PEND | RAM54_PEND | RAM53_PEND | RAM52_PEND | RAM51_PEND | RAM50_PEND | RAM49_PEND | RAM48_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM47_PEND | RAM46_PEND | RAM45_PEND | RAM44_PEND | RAM43_PEND | RAM42_PEND | RAM41_PEND | RAM40_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM39_PEND | RAM38_PEND | RAM37_PEND | RAM36_PEND | RAM35_PEND | RAM34_PEND | RAM33_PEND | RAM32_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-45. ECC_DED_STATUS_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 31 | RAM63_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 63. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM62_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 62. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM61_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 61. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM60_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 60. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM59_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 59. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM58_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 58. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 25 | RAM57_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 57. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM56_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 56. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-45. ECC_DED_STATUS_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 23 | RAM55_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 55. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM54_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 54. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM53_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 53. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM52_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 52. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM51_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 51. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM50_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 50. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM49_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 49. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM48_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 48. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM47_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 47. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM46_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 46. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 13 | RAM45_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 45. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM44_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 44. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM43_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 43. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM42_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 42. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM41_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 41. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM40_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 40. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-45. ECC_DED_STATUS_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 7 | RAM39_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 39. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM38_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 38. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM37_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 37. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM36_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 36. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM35_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 35. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM34_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 34. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 1 | RAM33_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 33. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM32_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 32. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.45 ECC_DED_STATUS_REG2 Register (Offset = 148h) [reset = 0h]

ECC_DED_STATUS_REG2 is shown in [Figure 20-45](#) and described in [Table 20-46](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-45. ECC_DED_STATUS_REG2 Register

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM95_PEND | RAM94_PEND | RAM93_PEND | RAM92_PEND | RAM91_PEND | RAM90_PEND | RAM89_PEND | RAM88_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM87_PEND | RAM86_PEND | RAM85_PEND | RAM84_PEND | RAM83_PEND | RAM82_PEND | RAM81_PEND | RAM80_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM79_PEND | RAM78_PEND | RAM77_PEND | RAM76_PEND | RAM75_PEND | RAM74_PEND | RAM73_PEND | RAM72_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM71_PEND | RAM70_PEND | RAM69_PEND | RAM68_PEND | RAM67_PEND | RAM66_PEND | RAM65_PEND | RAM64_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-46. ECC_DED_STATUS_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 31 | RAM95_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 95. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM94_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 94. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM93_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 93. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM92_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 92. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM91_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 91. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM90_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 90. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 25 | RAM89_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 89. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM88_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 88. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-46. ECC_DED_STATUS_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 23 | RAM87_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 87. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM86_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 86. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM85_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 85. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM84_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 84. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM83_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 83. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM82_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 82. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM81_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 81. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM80_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 80. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM79_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 79. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM78_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 78. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 13 | RAM77_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 77. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM76_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 76. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM75_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 75. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM74_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 74. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM73_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 73. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM72_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 72. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-46. ECC_DED_STATUS_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 7 | RAM71_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 71. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM70_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 70. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM69_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 69. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM68_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 68. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM67_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 67. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM66_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 66. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 1 | RAM65_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 65. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM64_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 64. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.46 ECC_DED_STATUS_REG3 Register (Offset = 14Ch) [reset = 0h]

ECC_DED_STATUS_REG3 is shown in [Figure 20-46](#) and described in [Table 20-47](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-46. ECC_DED_STATUS_REG3 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM127_PEND | RAM126_PEND | RAM125_PEND | RAM124_PEND | RAM123_PEND | RAM122_PEND | RAM121_PEND | RAM120_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM119_PEND | RAM118_PEND | RAM117_PEND | RAM116_PEND | RAM115_PEND | RAM114_PEND | RAM113_PEND | RAM112_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM111_PEND | RAM110_PEND | RAM109_PEND | RAM108_PEND | RAM107_PEND | RAM106_PEND | RAM105_PEND | RAM104_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM103_PEND | RAM102_PEND | RAM101_PEND | RAM100_PEND | RAM99_PEND | RAM98_PEND | RAM97_PEND | RAM96_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-47. ECC_DED_STATUS_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM127_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 127. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM126_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 126. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM125_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 125. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM124_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 124. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM123_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 123. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM122_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 122. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-47. ECC_DED_STATUS_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 25 | RAM121_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 121. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM120_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 120. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 23 | RAM119_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 119. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM118_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 118. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM117_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 117. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM116_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 116. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM115_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 115. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM114_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 114. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM113_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 113. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM112_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 112. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM111_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 111. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM110_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 110. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-47. ECC_DED_STATUS_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 13 | RAM109_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 109. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM108_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 108. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM107_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 107. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM106_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 106. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM105_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 105. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM104_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 104. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 7 | RAM103_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 103. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM102_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 102. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM101_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 101. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM100_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 100. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM99_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 99. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM98_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 98. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 1 | RAM97_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 97. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-47. ECC_DED_STATUS_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------|-------|-------|---|
| 0 | RAM96_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 96. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.47 ECC_DED_STATUS_REG4 Register (Offset = 150h) [reset = 0h]

ECC_DED_STATUS_REG4 is shown in [Figure 20-47](#) and described in [Table 20-48](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-47. ECC_DED_STATUS_REG4 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM159_PEND | RAM158_PEND | RAM157_PEND | RAM156_PEND | RAM155_PEND | RAM154_PEND | RAM153_PEND | RAM152_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM151_PEND | RAM150_PEND | RAM149_PEND | RAM148_PEND | RAM147_PEND | RAM146_PEND | RAM145_PEND | RAM144_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM143_PEND | RAM142_PEND | RAM141_PEND | RAM140_PEND | RAM139_PEND | RAM138_PEND | RAM137_PEND | RAM136_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM135_PEND | RAM134_PEND | RAM133_PEND | RAM132_PEND | RAM131_PEND | RAM130_PEND | RAM129_PEND | RAM128_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-48. ECC_DED_STATUS_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM159_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 159. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM158_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 158. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM157_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 157. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM156_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 156. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM155_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 155. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM154_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 154. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-48. ECC_DED_STATUS_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 25 | RAM153_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 153. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM152_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 152. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 23 | RAM151_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 151. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM150_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 150. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM149_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 149. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM148_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 148. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM147_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 147. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM146_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 146. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM145_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 145. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM144_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 144. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM143_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 143. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM142_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 142. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-48. ECC_DED_STATUS_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 13 | RAM141_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 141. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM140_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 140. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM139_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 139. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM138_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 138. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM137_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 137. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM136_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 136. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 7 | RAM135_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 135. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM134_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 134. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM133_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 133. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM132_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 132. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM131_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 131. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM130_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 130. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-48. ECC_DED_STATUS_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 1 | RAM129_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 129. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM128_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 128. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.48 ECC_DED_STATUS_REG5 Register (Offset = 154h) [reset = 0h]

ECC_DED_STATUS_REG5 is shown in [Figure 20-48](#) and described in [Table 20-49](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-48. ECC_DED_STATUS_REG5 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM191_PEND | RAM190_PEND | RAM189_PEND | RAM188_PEND | RAM187_PEND | RAM186_PEND | RAM185_PEND | RAM184_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM183_PEND | RAM182_PEND | RAM181_PEND | RAM180_PEND | RAM179_PEND | RAM178_PEND | RAM177_PEND | RAM176_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM175_PEND | RAM174_PEND | RAM173_PEND | RAM172_PEND | RAM171_PEND | RAM170_PEND | RAM169_PEND | RAM168_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM167_PEND | RAM166_PEND | RAM165_PEND | RAM164_PEND | RAM163_PEND | RAM162_PEND | RAM161_PEND | RAM160_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-49. ECC_DED_STATUS_REG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM191_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 191. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM190_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 190. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM189_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 189. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM188_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 188. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM187_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 187. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM186_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 186. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-49. ECC_DED_STATUS_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 25 | RAM185_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 185. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM184_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 184. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 23 | RAM183_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 183. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM182_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 182. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM181_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 181. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM180_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 180. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM179_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 179. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM178_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 178. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM177_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 177. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM176_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 176. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM175_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 175. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM174_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 174. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-49. ECC_DED_STATUS_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 13 | RAM173_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 173. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM172_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 172. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM171_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 171. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM170_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 170. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM169_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 169. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM168_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 168. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 7 | RAM167_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 167. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM166_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 166. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM165_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 165. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM164_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 164. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM163_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 163. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM162_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 162. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-49. ECC_DED_STATUS_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 1 | RAM161_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 161. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM160_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 160. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.49 ECC_DED_STATUS_REG6 Register (Offset = 158h) [reset = 0h]

ECC_DED_STATUS_REG6 is shown in [Figure 20-49](#) and described in [Table 20-50](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-49. ECC_DED_STATUS_REG6 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM223_PEND | RAM222_PEND | RAM221_PEND | RAM220_PEND | RAM219_PEND | RAM218_PEND | RAM217_PEND | RAM216_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM215_PEND | RAM214_PEND | RAM213_PEND | RAM212_PEND | RAM211_PEND | RAM210_PEND | RAM209_PEND | RAM208_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM207_PEND | RAM206_PEND | RAM205_PEND | RAM204_PEND | RAM203_PEND | RAM202_PEND | RAM201_PEND | RAM200_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM199_PEND | RAM198_PEND | RAM197_PEND | RAM196_PEND | RAM195_PEND | RAM194_PEND | RAM193_PEND | RAM192_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-50. ECC_DED_STATUS_REG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM223_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 223. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM222_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 222. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM221_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 221. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM220_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 220. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM219_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 219. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM218_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 218. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-50. ECC_DED_STATUS_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 25 | RAM217_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 217. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM216_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 216. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 23 | RAM215_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 215. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM214_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 214. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM213_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 213. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM212_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 212. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM211_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 211. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM210_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 210. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM209_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 209. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM208_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 208. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM207_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 207. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM206_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 206. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-50. ECC_DED_STATUS_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 13 | RAM205_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 205. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM204_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 204. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM203_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 203. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM202_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 202. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM201_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 201. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM200_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 200. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 7 | RAM199_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 199. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM198_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 198. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM197_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 197. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM196_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 196. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM195_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 195. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM194_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 194. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-50. ECC_DED_STATUS_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 1 | RAM193_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 193. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM192_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 192. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.50 ECC_DED_STATUS_REG7 Register (Offset = 15Ch) [reset = 0h]

ECC_DED_STATUS_REG7 is shown in [Figure 20-50](#) and described in [Table 20-51](#).

Return to [Summary Table](#).

Interrupt status register for non-correctable error. Each bit corresponds to the status from an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-50. ECC_DED_STATUS_REG7 Register

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM255_PEND | RAM254_PEND | RAM253_PEND | RAM252_PEND | RAM251_PEND | RAM250_PEND | RAM249_PEND | RAM248_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM247_PEND | RAM246_PEND | RAM245_PEND | RAM244_PEND | RAM243_PEND | RAM242_PEND | RAM241_PEND | RAM240_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM239_PEND | RAM238_PEND | RAM237_PEND | RAM236_PEND | RAM235_PEND | RAM234_PEND | RAM233_PEND | RAM232_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM231_PEND | RAM230_PEND | RAM229_PEND | RAM228_PEND | RAM227_PEND | RAM226_PEND | RAM225_PEND | RAM224_PEND |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-51. ECC_DED_STATUS_REG7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 31 | RAM255_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 255. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 30 | RAM254_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 254. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 29 | RAM253_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 253. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 28 | RAM252_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 252. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 27 | RAM251_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 251. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 26 | RAM250_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 250. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-51. ECC_DED_STATUS_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 25 | RAM249_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 249. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 24 | RAM248_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 248. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 23 | RAM247_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 247. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 22 | RAM246_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 246. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 21 | RAM245_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 245. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 20 | RAM244_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 244. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 19 | RAM243_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 243. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 18 | RAM242_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 242. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 17 | RAM241_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 241. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 16 | RAM240_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 240. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 15 | RAM239_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 239. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 14 | RAM238_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 238. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-51. ECC_DED_STATUS_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 13 | RAM237_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 237. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 12 | RAM236_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 236. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 11 | RAM235_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 235. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 10 | RAM234_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 234. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 9 | RAM233_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 233. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 8 | RAM232_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 232. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 7 | RAM231_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 231. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 6 | RAM230_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 230. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 5 | RAM229_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 229. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 4 | RAM228_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 228. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 3 | RAM227_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 227. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 2 | RAM226_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 226. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

Table 20-51. ECC_DED_STATUS_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|-------|-------|--|
| 1 | RAM225_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 225. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |
| 0 | RAM224_PEND | R/W1S | 0h | Non-correctable error interrupt status for ECC endpoint with ID = 224. 0h - Non-correctable error not occurred 1h - Non-correctable error occurred |

20.51 ECC_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = 0h]

ECC_DED_ENABLE_SET_REG0 is shown in [Figure 20-51](#) and described in [Table 20-52](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-51. ECC_DED_ENABLE_SET_REG0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM31_ENABL E_SET | RAM30_ENABL E_SET | RAM29_ENABL E_SET | RAM28_ENABL E_SET | RAM27_ENABL E_SET | RAM26_ENABL E_SET | RAM25_ENABL E_SET | RAM24_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM23_ENABL E_SET | RAM22_ENABL E_SET | RAM21_ENABL E_SET | RAM20_ENABL E_SET | RAM19_ENABL E_SET | RAM18_ENABL E_SET | RAM17_ENABL E_SET | RAM16_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM15_ENABL E_SET | RAM14_ENABL E_SET | RAM13_ENABL E_SET | RAM12_ENABL E_SET | RAM11_ENABL E_SET | RAM10_ENABL E_SET | RAM9_ENABL E_SET | RAM8_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM7_ENABL E_SET | RAM6_ENABL E_SET | RAM5_ENABL E_SET | RAM4_ENABL E_SET | RAM3_ENABL E_SET | RAM2_ENABL E_SET | RAM1_ENABL E_SET | RAM0_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-52. ECC_DED_ENABLE_SET_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM31_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 31. Write 1h to enable the interrupt |
| 30 | RAM30_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 30. Write 1h to enable the interrupt |
| 29 | RAM29_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 29. Write 1h to enable the interrupt |
| 28 | RAM28_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 28. Write 1h to enable the interrupt |
| 27 | RAM27_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 27. Write 1h to enable the interrupt |
| 26 | RAM26_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 26. Write 1h to enable the interrupt |
| 25 | RAM25_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 25. Write 1h to enable the interrupt |
| 24 | RAM24_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 24. Write 1h to enable the interrupt |
| 23 | RAM23_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 23. Write 1h to enable the interrupt |
| 22 | RAM22_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 22. Write 1h to enable the interrupt |

Table 20-52. ECC_DED_ENABLE_SET_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM21_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 21. Write 1h to enable the interrupt |
| 20 | RAM20_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 20. Write 1h to enable the interrupt |
| 19 | RAM19_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 19. Write 1h to enable the interrupt |
| 18 | RAM18_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 18. Write 1h to enable the interrupt |
| 17 | RAM17_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 17. Write 1h to enable the interrupt |
| 16 | RAM16_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 16. Write 1h to enable the interrupt |
| 15 | RAM15_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 15. Write 1h to enable the interrupt |
| 14 | RAM14_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 14. Write 1h to enable the interrupt |
| 13 | RAM13_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 13. Write 1h to enable the interrupt |
| 12 | RAM12_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 12. Write 1h to enable the interrupt |
| 11 | RAM11_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 11. Write 1h to enable the interrupt |
| 10 | RAM10_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 10. Write 1h to enable the interrupt |
| 9 | RAM9_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 9. Write 1h to enable the interrupt |
| 8 | RAM8_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 8. Write 1h to enable the interrupt |
| 7 | RAM7_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 7. Write 1h to enable the interrupt |
| 6 | RAM6_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 6. Write 1h to enable the interrupt |
| 5 | RAM5_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 5. Write 1h to enable the interrupt |
| 4 | RAM4_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 4. Write 1h to enable the interrupt |
| 3 | RAM3_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 3. Write 1h to enable the interrupt |
| 2 | RAM2_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 2. Write 1h to enable the interrupt |
| 1 | RAM1_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 1. Write 1h to enable the interrupt |
| 0 | RAM0_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 0. Write 1h to enable the interrupt |

20.52 ECC_DED_ENABLE_SET_REG1 Register (Offset = 184h) [reset = 0h]

ECC_DED_ENABLE_SET_REG1 is shown in [Figure 20-52](#) and described in [Table 20-53](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-52. ECC_DED_ENABLE_SET_REG1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM63_ENABL E_SET | RAM62_ENABL E_SET | RAM61_ENABL E_SET | RAM60_ENABL E_SET | RAM59_ENABL E_SET | RAM58_ENABL E_SET | RAM57_ENABL E_SET | RAM56_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM55_ENABL E_SET | RAM54_ENABL E_SET | RAM53_ENABL E_SET | RAM52_ENABL E_SET | RAM51_ENABL E_SET | RAM50_ENABL E_SET | RAM49_ENABL E_SET | RAM48_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM47_ENABL E_SET | RAM46_ENABL E_SET | RAM45_ENABL E_SET | RAM44_ENABL E_SET | RAM43_ENABL E_SET | RAM42_ENABL E_SET | RAM41_ENABL E_SET | RAM40_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM39_ENABL E_SET | RAM38_ENABL E_SET | RAM37_ENABL E_SET | RAM36_ENABL E_SET | RAM35_ENABL E_SET | RAM34_ENABL E_SET | RAM33_ENABL E_SET | RAM32_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-53. ECC_DED_ENABLE_SET_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM63_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 63. Write 1h to enable the interrupt |
| 30 | RAM62_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 62. Write 1h to enable the interrupt |
| 29 | RAM61_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 61. Write 1h to enable the interrupt |
| 28 | RAM60_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 60. Write 1h to enable the interrupt |
| 27 | RAM59_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 59. Write 1h to enable the interrupt |
| 26 | RAM58_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 58. Write 1h to enable the interrupt |
| 25 | RAM57_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 57. Write 1h to enable the interrupt |
| 24 | RAM56_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 56. Write 1h to enable the interrupt |
| 23 | RAM55_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 55. Write 1h to enable the interrupt |
| 22 | RAM54_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 54. Write 1h to enable the interrupt |

Table 20-53. ECC_DED_ENABLE_SET_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM53_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 53. Write 1h to enable the interrupt |
| 20 | RAM52_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 52. Write 1h to enable the interrupt |
| 19 | RAM51_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 51. Write 1h to enable the interrupt |
| 18 | RAM50_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 50. Write 1h to enable the interrupt |
| 17 | RAM49_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 49. Write 1h to enable the interrupt |
| 16 | RAM48_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 48. Write 1h to enable the interrupt |
| 15 | RAM47_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 47. Write 1h to enable the interrupt |
| 14 | RAM46_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 46. Write 1h to enable the interrupt |
| 13 | RAM45_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 45. Write 1h to enable the interrupt |
| 12 | RAM44_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 44. Write 1h to enable the interrupt |
| 11 | RAM43_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 43. Write 1h to enable the interrupt |
| 10 | RAM42_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 42. Write 1h to enable the interrupt |
| 9 | RAM41_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 41. Write 1h to enable the interrupt |
| 8 | RAM40_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 40. Write 1h to enable the interrupt |
| 7 | RAM39_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 39. Write 1h to enable the interrupt |
| 6 | RAM38_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 38. Write 1h to enable the interrupt |
| 5 | RAM37_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 37. Write 1h to enable the interrupt |
| 4 | RAM36_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 36. Write 1h to enable the interrupt |
| 3 | RAM35_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 35. Write 1h to enable the interrupt |
| 2 | RAM34_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 34. Write 1h to enable the interrupt |
| 1 | RAM33_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 33. Write 1h to enable the interrupt |
| 0 | RAM32_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 32. Write 1h to enable the interrupt |

20.53 ECC_DED_ENABLE_SET_REG2 Register (Offset = 188h) [reset = 0h]

ECC_DED_ENABLE_SET_REG2 is shown in [Figure 20-53](#) and described in [Table 20-54](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-53. ECC_DED_ENABLE_SET_REG2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM95_ENABL E_SET | RAM94_ENABL E_SET | RAM93_ENABL E_SET | RAM92_ENABL E_SET | RAM91_ENABL E_SET | RAM90_ENABL E_SET | RAM89_ENABL E_SET | RAM88_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM87_ENABL E_SET | RAM86_ENABL E_SET | RAM85_ENABL E_SET | RAM84_ENABL E_SET | RAM83_ENABL E_SET | RAM82_ENABL E_SET | RAM81_ENABL E_SET | RAM80_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM79_ENABL E_SET | RAM78_ENABL E_SET | RAM77_ENABL E_SET | RAM76_ENABL E_SET | RAM75_ENABL E_SET | RAM74_ENABL E_SET | RAM73_ENABL E_SET | RAM72_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM71_ENABL E_SET | RAM70_ENABL E_SET | RAM69_ENABL E_SET | RAM68_ENABL E_SET | RAM67_ENABL E_SET | RAM66_ENABL E_SET | RAM65_ENABL E_SET | RAM64_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-54. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 31 | RAM95_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 95. Write 1h to enable the interrupt |
| 30 | RAM94_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 94. Write 1h to enable the interrupt |
| 29 | RAM93_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 93. Write 1h to enable the interrupt |
| 28 | RAM92_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 92. Write 1h to enable the interrupt |
| 27 | RAM91_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 91. Write 1h to enable the interrupt |
| 26 | RAM90_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 90. Write 1h to enable the interrupt |
| 25 | RAM89_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 89. Write 1h to enable the interrupt |
| 24 | RAM88_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 88. Write 1h to enable the interrupt |
| 23 | RAM87_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 87. Write 1h to enable the interrupt |
| 22 | RAM86_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 86. Write 1h to enable the interrupt |

Table 20-54. ECC_DED_ENABLE_SET_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|--|
| 21 | RAM85_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 85. Write 1h to enable the interrupt |
| 20 | RAM84_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 84. Write 1h to enable the interrupt |
| 19 | RAM83_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 83. Write 1h to enable the interrupt |
| 18 | RAM82_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 82. Write 1h to enable the interrupt |
| 17 | RAM81_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 81. Write 1h to enable the interrupt |
| 16 | RAM80_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 80. Write 1h to enable the interrupt |
| 15 | RAM79_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 79. Write 1h to enable the interrupt |
| 14 | RAM78_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 78. Write 1h to enable the interrupt |
| 13 | RAM77_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 77. Write 1h to enable the interrupt |
| 12 | RAM76_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 76. Write 1h to enable the interrupt |
| 11 | RAM75_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 75. Write 1h to enable the interrupt |
| 10 | RAM74_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 74. Write 1h to enable the interrupt |
| 9 | RAM73_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 73. Write 1h to enable the interrupt |
| 8 | RAM72_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 72. Write 1h to enable the interrupt |
| 7 | RAM71_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 71. Write 1h to enable the interrupt |
| 6 | RAM70_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 70. Write 1h to enable the interrupt |
| 5 | RAM69_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 69. Write 1h to enable the interrupt |
| 4 | RAM68_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 68. Write 1h to enable the interrupt |
| 3 | RAM67_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 67. Write 1h to enable the interrupt |
| 2 | RAM66_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 66. Write 1h to enable the interrupt |
| 1 | RAM65_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 65. Write 1h to enable the interrupt |
| 0 | RAM64_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 64. Write 1h to enable the interrupt |

20.54 ECC_DED_ENABLE_SET_REG3 Register (Offset = 18Ch) [reset = 0h]

ECC_DED_ENABLE_SET_REG3 is shown in [Figure 20-54](#) and described in [Table 20-55](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-54. ECC_DED_ENABLE_SET_REG3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM127_ENAB LE_SET | RAM126_ENAB LE_SET | RAM125_ENAB LE_SET | RAM124_ENAB LE_SET | RAM123_ENAB LE_SET | RAM122_ENAB LE_SET | RAM121_ENAB LE_SET | RAM120_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM119_ENAB LE_SET | RAM118_ENAB LE_SET | RAM117_ENAB LE_SET | RAM116_ENAB LE_SET | RAM115_ENAB LE_SET | RAM114_ENAB LE_SET | RAM113_ENAB LE_SET | RAM112_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM111_ENAB LE_SET | RAM110_ENAB LE_SET | RAM109_ENAB LE_SET | RAM108_ENAB LE_SET | RAM107_ENAB LE_SET | RAM106_ENAB LE_SET | RAM105_ENAB LE_SET | RAM104_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM103_ENAB LE_SET | RAM102_ENAB LE_SET | RAM101_ENAB LE_SET | RAM100_ENAB LE_SET | RAM99_ENABL E_SET | RAM98_ENABL E_SET | RAM97_ENABL E_SET | RAM96_ENABL E_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-55. ECC_DED_ENABLE_SET_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM127_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 127. Write 1h to enable the interrupt |
| 30 | RAM126_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 126. Write 1h to enable the interrupt |
| 29 | RAM125_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 125. Write 1h to enable the interrupt |
| 28 | RAM124_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 124. Write 1h to enable the interrupt |
| 27 | RAM123_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 123. Write 1h to enable the interrupt |
| 26 | RAM122_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 122. Write 1h to enable the interrupt |
| 25 | RAM121_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 121. Write 1h to enable the interrupt |

Table 20-55. ECC_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM120_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 120. Write 1h to enable the interrupt |
| 23 | RAM119_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 119. Write 1h to enable the interrupt |
| 22 | RAM118_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 118. Write 1h to enable the interrupt |
| 21 | RAM117_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 117. Write 1h to enable the interrupt |
| 20 | RAM116_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 116. Write 1h to enable the interrupt |
| 19 | RAM115_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 115. Write 1h to enable the interrupt |
| 18 | RAM114_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 114. Write 1h to enable the interrupt |
| 17 | RAM113_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 113. Write 1h to enable the interrupt |
| 16 | RAM112_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 112. Write 1h to enable the interrupt |
| 15 | RAM111_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 111. Write 1h to enable the interrupt |
| 14 | RAM110_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 110. Write 1h to enable the interrupt |
| 13 | RAM109_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 109. Write 1h to enable the interrupt |
| 12 | RAM108_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 108. Write 1h to enable the interrupt |
| 11 | RAM107_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 107. Write 1h to enable the interrupt |
| 10 | RAM106_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 106. Write 1h to enable the interrupt |
| 9 | RAM105_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 105. Write 1h to enable the interrupt |

Table 20-55. ECC_DED_ENABLE_SET_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM104_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 104. Write 1h to enable the interrupt |
| 7 | RAM103_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 103. Write 1h to enable the interrupt |
| 6 | RAM102_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 102. Write 1h to enable the interrupt |
| 5 | RAM101_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 101. Write 1h to enable the interrupt |
| 4 | RAM100_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 100. Write 1h to enable the interrupt |
| 3 | RAM99_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 99. Write 1h to enable the interrupt |
| 2 | RAM98_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 98. Write 1h to enable the interrupt |
| 1 | RAM97_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 97. Write 1h to enable the interrupt |
| 0 | RAM96_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 96. Write 1h to enable the interrupt |

20.55 ECC_DED_ENABLE_SET_REG4 Register (Offset = 190h) [reset = 0h]

ECC_DED_ENABLE_SET_REG4 is shown in [Figure 20-55](#) and described in [Table 20-56](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-55. ECC_DED_ENABLE_SET_REG4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM159_ENAB LE_SET | RAM158_ENAB LE_SET | RAM157_ENAB LE_SET | RAM156_ENAB LE_SET | RAM155_ENAB LE_SET | RAM154_ENAB LE_SET | RAM153_ENAB LE_SET | RAM152_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM151_ENAB LE_SET | RAM150_ENAB LE_SET | RAM149_ENAB LE_SET | RAM148_ENAB LE_SET | RAM147_ENAB LE_SET | RAM146_ENAB LE_SET | RAM145_ENAB LE_SET | RAM144_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM143_ENAB LE_SET | RAM142_ENAB LE_SET | RAM141_ENAB LE_SET | RAM140_ENAB LE_SET | RAM139_ENAB LE_SET | RAM138_ENAB LE_SET | RAM137_ENAB LE_SET | RAM136_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM135_ENAB LE_SET | RAM134_ENAB LE_SET | RAM133_ENAB LE_SET | RAM132_ENAB LE_SET | RAM131_ENAB LE_SET | RAM130_ENAB LE_SET | RAM129_ENAB LE_SET | RAM128_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-56. ECC_DED_ENABLE_SET_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM159_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 159. Write 1h to enable the interrupt |
| 30 | RAM158_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 158. Write 1h to enable the interrupt |
| 29 | RAM157_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 157. Write 1h to enable the interrupt |
| 28 | RAM156_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 156. Write 1h to enable the interrupt |
| 27 | RAM155_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 155. Write 1h to enable the interrupt |
| 26 | RAM154_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 154. Write 1h to enable the interrupt |
| 25 | RAM153_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 153. Write 1h to enable the interrupt |

Table 20-56. ECC_DED_ENABLE_SET_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM152_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 152. Write 1h to enable the interrupt |
| 23 | RAM151_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 151. Write 1h to enable the interrupt |
| 22 | RAM150_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 150. Write 1h to enable the interrupt |
| 21 | RAM149_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 149. Write 1h to enable the interrupt |
| 20 | RAM148_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 148. Write 1h to enable the interrupt |
| 19 | RAM147_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 147. Write 1h to enable the interrupt |
| 18 | RAM146_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 146. Write 1h to enable the interrupt |
| 17 | RAM145_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 145. Write 1h to enable the interrupt |
| 16 | RAM144_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 144. Write 1h to enable the interrupt |
| 15 | RAM143_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 143. Write 1h to enable the interrupt |
| 14 | RAM142_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 142. Write 1h to enable the interrupt |
| 13 | RAM141_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 141. Write 1h to enable the interrupt |
| 12 | RAM140_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 140. Write 1h to enable the interrupt |
| 11 | RAM139_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 139. Write 1h to enable the interrupt |
| 10 | RAM138_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 138. Write 1h to enable the interrupt |
| 9 | RAM137_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 137. Write 1h to enable the interrupt |

Table 20-56. ECC_DED_ENABLE_SET_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM136_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 136. Write 1h to enable the interrupt |
| 7 | RAM135_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 135. Write 1h to enable the interrupt |
| 6 | RAM134_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 134. Write 1h to enable the interrupt |
| 5 | RAM133_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 133. Write 1h to enable the interrupt |
| 4 | RAM132_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 132. Write 1h to enable the interrupt |
| 3 | RAM131_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 131. Write 1h to enable the interrupt |
| 2 | RAM130_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 130. Write 1h to enable the interrupt |
| 1 | RAM129_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 129. Write 1h to enable the interrupt |
| 0 | RAM128_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 128. Write 1h to enable the interrupt |

20.56 ECC_DED_ENABLE_SET_REG5 Register (Offset = 194h) [reset = 0h]

ECC_DED_ENABLE_SET_REG5 is shown in [Figure 20-56](#) and described in [Table 20-57](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-56. ECC_DED_ENABLE_SET_REG5 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM191_ENAB LE_SET | RAM190_ENAB LE_SET | RAM189_ENAB LE_SET | RAM188_ENAB LE_SET | RAM187_ENAB LE_SET | RAM186_ENAB LE_SET | RAM185_ENAB LE_SET | RAM184_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM183_ENAB LE_SET | RAM182_ENAB LE_SET | RAM181_ENAB LE_SET | RAM180_ENAB LE_SET | RAM179_ENAB LE_SET | RAM178_ENAB LE_SET | RAM177_ENAB LE_SET | RAM176_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM175_ENAB LE_SET | RAM174_ENAB LE_SET | RAM173_ENAB LE_SET | RAM172_ENAB LE_SET | RAM171_ENAB LE_SET | RAM170_ENAB LE_SET | RAM169_ENAB LE_SET | RAM168_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM167_ENAB LE_SET | RAM166_ENAB LE_SET | RAM165_ENAB LE_SET | RAM164_ENAB LE_SET | RAM163_ENAB LE_SET | RAM162_ENAB LE_SET | RAM161_ENAB LE_SET | RAM160_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-57. ECC_DED_ENABLE_SET_REG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM191_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 191. Write 1h to enable the interrupt |
| 30 | RAM190_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 190. Write 1h to enable the interrupt |
| 29 | RAM189_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 189. Write 1h to enable the interrupt |
| 28 | RAM188_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 188. Write 1h to enable the interrupt |
| 27 | RAM187_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 187. Write 1h to enable the interrupt |
| 26 | RAM186_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 186. Write 1h to enable the interrupt |
| 25 | RAM185_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 185. Write 1h to enable the interrupt |

Table 20-57. ECC_DED_ENABLE_SET_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM184_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 184. Write 1h to enable the interrupt |
| 23 | RAM183_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 183. Write 1h to enable the interrupt |
| 22 | RAM182_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 182. Write 1h to enable the interrupt |
| 21 | RAM181_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 181. Write 1h to enable the interrupt |
| 20 | RAM180_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 180. Write 1h to enable the interrupt |
| 19 | RAM179_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 179. Write 1h to enable the interrupt |
| 18 | RAM178_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 178. Write 1h to enable the interrupt |
| 17 | RAM177_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 177. Write 1h to enable the interrupt |
| 16 | RAM176_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 176. Write 1h to enable the interrupt |
| 15 | RAM175_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 175. Write 1h to enable the interrupt |
| 14 | RAM174_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 174. Write 1h to enable the interrupt |
| 13 | RAM173_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 173. Write 1h to enable the interrupt |
| 12 | RAM172_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 172. Write 1h to enable the interrupt |
| 11 | RAM171_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 171. Write 1h to enable the interrupt |
| 10 | RAM170_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 170. Write 1h to enable the interrupt |
| 9 | RAM169_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 169. Write 1h to enable the interrupt |

Table 20-57. ECC_DED_ENABLE_SET_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM168_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 168. Write 1h to enable the interrupt |
| 7 | RAM167_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 167. Write 1h to enable the interrupt |
| 6 | RAM166_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 166. Write 1h to enable the interrupt |
| 5 | RAM165_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 165. Write 1h to enable the interrupt |
| 4 | RAM164_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 164. Write 1h to enable the interrupt |
| 3 | RAM163_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 163. Write 1h to enable the interrupt |
| 2 | RAM162_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 162. Write 1h to enable the interrupt |
| 1 | RAM161_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 161. Write 1h to enable the interrupt |
| 0 | RAM160_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 160. Write 1h to enable the interrupt |

20.57 ECC_DED_ENABLE_SET_REG6 Register (Offset = 198h) [reset = 0h]

ECC_DED_ENABLE_SET_REG6 is shown in [Figure 20-57](#) and described in [Table 20-58](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-57. ECC_DED_ENABLE_SET_REG6 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM223_ENAB LE_SET | RAM222_ENAB LE_SET | RAM221_ENAB LE_SET | RAM220_ENAB LE_SET | RAM219_ENAB LE_SET | RAM218_ENAB LE_SET | RAM217_ENAB LE_SET | RAM216_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM215_ENAB LE_SET | RAM214_ENAB LE_SET | RAM213_ENAB LE_SET | RAM212_ENAB LE_SET | RAM211_ENAB LE_SET | RAM210_ENAB LE_SET | RAM209_ENAB LE_SET | RAM208_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM207_ENAB LE_SET | RAM206_ENAB LE_SET | RAM205_ENAB LE_SET | RAM204_ENAB LE_SET | RAM203_ENAB LE_SET | RAM202_ENAB LE_SET | RAM201_ENAB LE_SET | RAM200_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM199_ENAB LE_SET | RAM198_ENAB LE_SET | RAM197_ENAB LE_SET | RAM196_ENAB LE_SET | RAM195_ENAB LE_SET | RAM194_ENAB LE_SET | RAM193_ENAB LE_SET | RAM192_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-58. ECC_DED_ENABLE_SET_REG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM223_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 223. Write 1h to enable the interrupt |
| 30 | RAM222_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 222. Write 1h to enable the interrupt |
| 29 | RAM221_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 221. Write 1h to enable the interrupt |
| 28 | RAM220_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 220. Write 1h to enable the interrupt |
| 27 | RAM219_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 219. Write 1h to enable the interrupt |
| 26 | RAM218_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 218. Write 1h to enable the interrupt |
| 25 | RAM217_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 217. Write 1h to enable the interrupt |

Table 20-58. ECC_DED_ENABLE_SET_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM216_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 216. Write 1h to enable the interrupt |
| 23 | RAM215_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 215. Write 1h to enable the interrupt |
| 22 | RAM214_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 214. Write 1h to enable the interrupt |
| 21 | RAM213_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 213. Write 1h to enable the interrupt |
| 20 | RAM212_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 212. Write 1h to enable the interrupt |
| 19 | RAM211_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 211. Write 1h to enable the interrupt |
| 18 | RAM210_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 210. Write 1h to enable the interrupt |
| 17 | RAM209_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 209. Write 1h to enable the interrupt |
| 16 | RAM208_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 208. Write 1h to enable the interrupt |
| 15 | RAM207_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 207. Write 1h to enable the interrupt |
| 14 | RAM206_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 206. Write 1h to enable the interrupt |
| 13 | RAM205_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 205. Write 1h to enable the interrupt |
| 12 | RAM204_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 204. Write 1h to enable the interrupt |
| 11 | RAM203_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 203. Write 1h to enable the interrupt |
| 10 | RAM202_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 202. Write 1h to enable the interrupt |
| 9 | RAM201_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 201. Write 1h to enable the interrupt |

Table 20-58. ECC_DED_ENABLE_SET_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM200_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 200. Write 1h to enable the interrupt |
| 7 | RAM199_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 199. Write 1h to enable the interrupt |
| 6 | RAM198_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 198. Write 1h to enable the interrupt |
| 5 | RAM197_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 197. Write 1h to enable the interrupt |
| 4 | RAM196_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 196. Write 1h to enable the interrupt |
| 3 | RAM195_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 195. Write 1h to enable the interrupt |
| 2 | RAM194_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 194. Write 1h to enable the interrupt |
| 1 | RAM193_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 193. Write 1h to enable the interrupt |
| 0 | RAM192_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 192. Write 1h to enable the interrupt |

20.58 ECC_DED_ENABLE_SET_REG7 Register (Offset = 19Ch) [reset = 0h]

ECC_DED_ENABLE_SET_REG7 is shown in [Figure 20-58](#) and described in [Table 20-59](#).

Return to [Summary Table](#).

Interrupt enable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-58. ECC_DED_ENABLE_SET_REG7 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM255_ENAB LE_SET | RAM254_ENAB LE_SET | RAM253_ENAB LE_SET | RAM252_ENAB LE_SET | RAM251_ENAB LE_SET | RAM250_ENAB LE_SET | RAM249_ENAB LE_SET | RAM248_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM247_ENAB LE_SET | RAM246_ENAB LE_SET | RAM245_ENAB LE_SET | RAM244_ENAB LE_SET | RAM243_ENAB LE_SET | RAM242_ENAB LE_SET | RAM241_ENAB LE_SET | RAM240_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM239_ENAB LE_SET | RAM238_ENAB LE_SET | RAM237_ENAB LE_SET | RAM236_ENAB LE_SET | RAM235_ENAB LE_SET | RAM234_ENAB LE_SET | RAM233_ENAB LE_SET | RAM232_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM231_ENAB LE_SET | RAM230_ENAB LE_SET | RAM229_ENAB LE_SET | RAM228_ENAB LE_SET | RAM227_ENAB LE_SET | RAM226_ENAB LE_SET | RAM225_ENAB LE_SET | RAM224_ENAB LE_SET |
| R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h | R/W1S-0h |

LEGEND: R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-59. ECC_DED_ENABLE_SET_REG7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM255_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 255. Write 1h to enable the interrupt |
| 30 | RAM254_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 254. Write 1h to enable the interrupt |
| 29 | RAM253_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 253. Write 1h to enable the interrupt |
| 28 | RAM252_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 252. Write 1h to enable the interrupt |
| 27 | RAM251_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 251. Write 1h to enable the interrupt |
| 26 | RAM250_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 250. Write 1h to enable the interrupt |
| 25 | RAM249_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 249. Write 1h to enable the interrupt |

Table 20-59. ECC_DED_ENABLE_SET_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM248_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 248. Write 1h to enable the interrupt |
| 23 | RAM247_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 247. Write 1h to enable the interrupt |
| 22 | RAM246_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 246. Write 1h to enable the interrupt |
| 21 | RAM245_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 245. Write 1h to enable the interrupt |
| 20 | RAM244_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 244. Write 1h to enable the interrupt |
| 19 | RAM243_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 243. Write 1h to enable the interrupt |
| 18 | RAM242_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 242. Write 1h to enable the interrupt |
| 17 | RAM241_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 241. Write 1h to enable the interrupt |
| 16 | RAM240_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 240. Write 1h to enable the interrupt |
| 15 | RAM239_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 239. Write 1h to enable the interrupt |
| 14 | RAM238_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 238. Write 1h to enable the interrupt |
| 13 | RAM237_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 237. Write 1h to enable the interrupt |
| 12 | RAM236_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 236. Write 1h to enable the interrupt |
| 11 | RAM235_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 235. Write 1h to enable the interrupt |
| 10 | RAM234_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 234. Write 1h to enable the interrupt |
| 9 | RAM233_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 233. Write 1h to enable the interrupt |

Table 20-59. ECC_DED_ENABLE_SET_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM232_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 232. Write 1h to enable the interrupt |
| 7 | RAM231_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 231. Write 1h to enable the interrupt |
| 6 | RAM230_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 230. Write 1h to enable the interrupt |
| 5 | RAM229_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 229. Write 1h to enable the interrupt |
| 4 | RAM228_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 228. Write 1h to enable the interrupt |
| 3 | RAM227_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 227. Write 1h to enable the interrupt |
| 2 | RAM226_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 226. Write 1h to enable the interrupt |
| 1 | RAM225_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 225. Write 1h to enable the interrupt |
| 0 | RAM224_ENABLE_SET | R/W1S | 0h | Non-correctable error interrupt enable for ECC endpoint with ID = 224. Write 1h to enable the interrupt |

20.59 ECC_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG0 is shown in [Figure 20-59](#) and described in [Table 20-60](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-59. ECC_DED_ENABLE_CLR_REG0 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM31_ENABL E_CLR | RAM30_ENABL E_CLR | RAM29_ENABL E_CLR | RAM28_ENABL E_CLR | RAM27_ENABL E_CLR | RAM26_ENABL E_CLR | RAM25_ENABL E_CLR | RAM24_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM23_ENABL E_CLR | RAM22_ENABL E_CLR | RAM21_ENABL E_CLR | RAM20_ENABL E_CLR | RAM19_ENABL E_CLR | RAM18_ENABL E_CLR | RAM17_ENABL E_CLR | RAM16_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM15_ENABL E_CLR | RAM14_ENABL E_CLR | RAM13_ENABL E_CLR | RAM12_ENABL E_CLR | RAM11_ENABL E_CLR | RAM10_ENABL E_CLR | RAM9_ENABL E_CLR | RAM8_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM7_ENABL E_CLR | RAM6_ENABL E_CLR | RAM5_ENABL E_CLR | RAM4_ENABL E_CLR | RAM3_ENABL E_CLR | RAM2_ENABL E_CLR | RAM1_ENABL E_CLR | RAM0_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-60. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 31 | RAM31_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 31. Write 1h to disable the interrupt |
| 30 | RAM30_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 30. Write 1h to disable the interrupt |
| 29 | RAM29_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 29. Write 1h to disable the interrupt |
| 28 | RAM28_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 28. Write 1h to disable the interrupt |
| 27 | RAM27_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 27. Write 1h to disable the interrupt |
| 26 | RAM26_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 26. Write 1h to disable the interrupt |
| 25 | RAM25_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 25. Write 1h to disable the interrupt |

Table 20-60. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 24 | RAM24_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 24. Write 1h to disable the interrupt |
| 23 | RAM23_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 23. Write 1h to disable the interrupt |
| 22 | RAM22_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 22. Write 1h to disable the interrupt |
| 21 | RAM21_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 21. Write 1h to disable the interrupt |
| 20 | RAM20_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 20. Write 1h to disable the interrupt |
| 19 | RAM19_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 19. Write 1h to disable the interrupt |
| 18 | RAM18_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 18. Write 1h to disable the interrupt |
| 17 | RAM17_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 17. Write 1h to disable the interrupt |
| 16 | RAM16_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 16. Write 1h to disable the interrupt |
| 15 | RAM15_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 15. Write 1h to disable the interrupt |
| 14 | RAM14_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 14. Write 1h to disable the interrupt |
| 13 | RAM13_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 13. Write 1h to disable the interrupt |
| 12 | RAM12_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 12. Write 1h to disable the interrupt |
| 11 | RAM11_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 11. Write 1h to disable the interrupt |
| 10 | RAM10_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 10. Write 1h to disable the interrupt |
| 9 | RAM9_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 9. Write 1h to disable the interrupt |

Table 20-60. ECC_DED_ENABLE_CLR_REG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|-------|-------|---|
| 8 | RAM8_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 8. Write 1h to disable the interrupt |
| 7 | RAM7_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 7. Write 1h to disable the interrupt |
| 6 | RAM6_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 6. Write 1h to disable the interrupt |
| 5 | RAM5_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 5. Write 1h to disable the interrupt |
| 4 | RAM4_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 4. Write 1h to disable the interrupt |
| 3 | RAM3_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 3. Write 1h to disable the interrupt |
| 2 | RAM2_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 2. Write 1h to disable the interrupt |
| 1 | RAM1_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 1. Write 1h to disable the interrupt |
| 0 | RAM0_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 0. Write 1h to disable the interrupt |

20.60 ECC_DED_ENABLE_CLR_REG1 Register (Offset = 1C4h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG1 is shown in [Figure 20-60](#) and described in [Table 20-61](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-60. ECC_DED_ENABLE_CLR_REG1 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM63_ENABL E_CLR | RAM62_ENABL E_CLR | RAM61_ENABL E_CLR | RAM60_ENABL E_CLR | RAM59_ENABL E_CLR | RAM58_ENABL E_CLR | RAM57_ENABL E_CLR | RAM56_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM55_ENABL E_CLR | RAM54_ENABL E_CLR | RAM53_ENABL E_CLR | RAM52_ENABL E_CLR | RAM51_ENABL E_CLR | RAM50_ENABL E_CLR | RAM49_ENABL E_CLR | RAM48_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM47_ENABL E_CLR | RAM46_ENABL E_CLR | RAM45_ENABL E_CLR | RAM44_ENABL E_CLR | RAM43_ENABL E_CLR | RAM42_ENABL E_CLR | RAM41_ENABL E_CLR | RAM40_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM39_ENABL E_CLR | RAM38_ENABL E_CLR | RAM37_ENABL E_CLR | RAM36_ENABL E_CLR | RAM35_ENABL E_CLR | RAM34_ENABL E_CLR | RAM33_ENABL E_CLR | RAM32_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-61. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 31 | RAM63_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 63. Write 1h to disable the interrupt |
| 30 | RAM62_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 62. Write 1h to disable the interrupt |
| 29 | RAM61_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 61. Write 1h to disable the interrupt |
| 28 | RAM60_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 60. Write 1h to disable the interrupt |
| 27 | RAM59_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 59. Write 1h to disable the interrupt |
| 26 | RAM58_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 58. Write 1h to disable the interrupt |
| 25 | RAM57_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 57. Write 1h to disable the interrupt |

Table 20-61. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 24 | RAM56_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 56. Write 1h to disable the interrupt |
| 23 | RAM55_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 55. Write 1h to disable the interrupt |
| 22 | RAM54_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 54. Write 1h to disable the interrupt |
| 21 | RAM53_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 53. Write 1h to disable the interrupt |
| 20 | RAM52_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 52. Write 1h to disable the interrupt |
| 19 | RAM51_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 51. Write 1h to disable the interrupt |
| 18 | RAM50_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 50. Write 1h to disable the interrupt |
| 17 | RAM49_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 49. Write 1h to disable the interrupt |
| 16 | RAM48_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 48. Write 1h to disable the interrupt |
| 15 | RAM47_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 47. Write 1h to disable the interrupt |
| 14 | RAM46_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 46. Write 1h to disable the interrupt |
| 13 | RAM45_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 45. Write 1h to disable the interrupt |
| 12 | RAM44_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 44. Write 1h to disable the interrupt |
| 11 | RAM43_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 43. Write 1h to disable the interrupt |
| 10 | RAM42_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 42. Write 1h to disable the interrupt |
| 9 | RAM41_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 41. Write 1h to disable the interrupt |

Table 20-61. ECC_DED_ENABLE_CLR_REG1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 8 | RAM40_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 40. Write 1h to disable the interrupt |
| 7 | RAM39_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 39. Write 1h to disable the interrupt |
| 6 | RAM38_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 38. Write 1h to disable the interrupt |
| 5 | RAM37_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 37. Write 1h to disable the interrupt |
| 4 | RAM36_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 36. Write 1h to disable the interrupt |
| 3 | RAM35_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 35. Write 1h to disable the interrupt |
| 2 | RAM34_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 34. Write 1h to disable the interrupt |
| 1 | RAM33_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 33. Write 1h to disable the interrupt |
| 0 | RAM32_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 32. Write 1h to disable the interrupt |

20.61 ECC_DED_ENABLE_CLR_REG2 Register (Offset = 1C8h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG2 is shown in [Figure 20-61](#) and described in [Table 20-62](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-61. ECC_DED_ENABLE_CLR_REG2 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| RAM95_ENABL E_CLR | RAM94_ENABL E_CLR | RAM93_ENABL E_CLR | RAM92_ENABL E_CLR | RAM91_ENABL E_CLR | RAM90_ENABL E_CLR | RAM89_ENABL E_CLR | RAM88_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM87_ENABL E_CLR | RAM86_ENABL E_CLR | RAM85_ENABL E_CLR | RAM84_ENABL E_CLR | RAM83_ENABL E_CLR | RAM82_ENABL E_CLR | RAM81_ENABL E_CLR | RAM80_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM79_ENABL E_CLR | RAM78_ENABL E_CLR | RAM77_ENABL E_CLR | RAM76_ENABL E_CLR | RAM75_ENABL E_CLR | RAM74_ENABL E_CLR | RAM73_ENABL E_CLR | RAM72_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM71_ENABL E_CLR | RAM70_ENABL E_CLR | RAM69_ENABL E_CLR | RAM68_ENABL E_CLR | RAM67_ENABL E_CLR | RAM66_ENABL E_CLR | RAM65_ENABL E_CLR | RAM64_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-62. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 31 | RAM95_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 95. Write 1h to disable the interrupt |
| 30 | RAM94_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 94. Write 1h to disable the interrupt |
| 29 | RAM93_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 93. Write 1h to disable the interrupt |
| 28 | RAM92_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 92. Write 1h to disable the interrupt |
| 27 | RAM91_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 91. Write 1h to disable the interrupt |
| 26 | RAM90_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 90. Write 1h to disable the interrupt |
| 25 | RAM89_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 89. Write 1h to disable the interrupt |

Table 20-62. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 24 | RAM88_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 88. Write 1h to disable the interrupt |
| 23 | RAM87_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 87. Write 1h to disable the interrupt |
| 22 | RAM86_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 86. Write 1h to disable the interrupt |
| 21 | RAM85_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 85. Write 1h to disable the interrupt |
| 20 | RAM84_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 84. Write 1h to disable the interrupt |
| 19 | RAM83_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 83. Write 1h to disable the interrupt |
| 18 | RAM82_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 82. Write 1h to disable the interrupt |
| 17 | RAM81_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 81. Write 1h to disable the interrupt |
| 16 | RAM80_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 80. Write 1h to disable the interrupt |
| 15 | RAM79_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 79. Write 1h to disable the interrupt |
| 14 | RAM78_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 78. Write 1h to disable the interrupt |
| 13 | RAM77_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 77. Write 1h to disable the interrupt |
| 12 | RAM76_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 76. Write 1h to disable the interrupt |
| 11 | RAM75_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 75. Write 1h to disable the interrupt |
| 10 | RAM74_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 74. Write 1h to disable the interrupt |
| 9 | RAM73_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 73. Write 1h to disable the interrupt |

Table 20-62. ECC_DED_ENABLE_CLR_REG2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|------------------|-------|-------|---|
| 8 | RAM72_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 72. Write 1h to disable the interrupt |
| 7 | RAM71_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 71. Write 1h to disable the interrupt |
| 6 | RAM70_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 70. Write 1h to disable the interrupt |
| 5 | RAM69_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 69. Write 1h to disable the interrupt |
| 4 | RAM68_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 68. Write 1h to disable the interrupt |
| 3 | RAM67_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 67. Write 1h to disable the interrupt |
| 2 | RAM66_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 66. Write 1h to disable the interrupt |
| 1 | RAM65_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 65. Write 1h to disable the interrupt |
| 0 | RAM64_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 64. Write 1h to disable the interrupt |

20.62 ECC_DED_ENABLE_CLR_REG3 Register (Offset = 1CCh) [reset = 0h]

ECC_DED_ENABLE_CLR_REG3 is shown in [Figure 20-62](#) and described in [Table 20-63](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-62. ECC_DED_ENABLE_CLR_REG3 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM127_ENAB LE_CLR | RAM126_ENAB LE_CLR | RAM125_ENAB LE_CLR | RAM124_ENAB LE_CLR | RAM123_ENAB LE_CLR | RAM122_ENAB LE_CLR | RAM121_ENAB LE_CLR | RAM120_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM119_ENAB LE_CLR | RAM118_ENAB LE_CLR | RAM117_ENAB LE_CLR | RAM116_ENAB LE_CLR | RAM115_ENAB LE_CLR | RAM114_ENAB LE_CLR | RAM113_ENAB LE_CLR | RAM112_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM111_ENAB LE_CLR | RAM110_ENAB LE_CLR | RAM109_ENAB LE_CLR | RAM108_ENAB LE_CLR | RAM107_ENAB LE_CLR | RAM106_ENAB LE_CLR | RAM105_ENAB LE_CLR | RAM104_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM103_ENAB LE_CLR | RAM102_ENAB LE_CLR | RAM101_ENAB LE_CLR | RAM100_ENAB LE_CLR | RAM99_ENABL E_CLR | RAM98_ENABL E_CLR | RAM97_ENABL E_CLR | RAM96_ENABL E_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-63. ECC_DED_ENABLE_CLR_REG3 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM127_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 127. Write 1h to disable the interrupt |
| 30 | RAM126_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 126. Write 1h to disable the interrupt |
| 29 | RAM125_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 125. Write 1h to disable the interrupt |
| 28 | RAM124_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 124. Write 1h to disable the interrupt |
| 27 | RAM123_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 123. Write 1h to disable the interrupt |
| 26 | RAM122_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 122. Write 1h to disable the interrupt |
| 25 | RAM121_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 121. Write 1h to disable the interrupt |

Table 20-63. ECC_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM120_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 120. Write 1h to disable the interrupt |
| 23 | RAM119_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 119. Write 1h to disable the interrupt |
| 22 | RAM118_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 118. Write 1h to disable the interrupt |
| 21 | RAM117_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 117. Write 1h to disable the interrupt |
| 20 | RAM116_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 116. Write 1h to disable the interrupt |
| 19 | RAM115_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 115. Write 1h to disable the interrupt |
| 18 | RAM114_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 114. Write 1h to disable the interrupt |
| 17 | RAM113_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 113. Write 1h to disable the interrupt |
| 16 | RAM112_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 112. Write 1h to disable the interrupt |
| 15 | RAM111_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 111. Write 1h to disable the interrupt |
| 14 | RAM110_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 110. Write 1h to disable the interrupt |
| 13 | RAM109_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 109. Write 1h to disable the interrupt |
| 12 | RAM108_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 108. Write 1h to disable the interrupt |
| 11 | RAM107_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 107. Write 1h to disable the interrupt |
| 10 | RAM106_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 106. Write 1h to disable the interrupt |
| 9 | RAM105_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 105. Write 1h to disable the interrupt |

Table 20-63. ECC_DED_ENABLE_CLR_REG3 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM104_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 104. Write 1h to disable the interrupt |
| 7 | RAM103_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 103. Write 1h to disable the interrupt |
| 6 | RAM102_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 102. Write 1h to disable the interrupt |
| 5 | RAM101_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 101. Write 1h to disable the interrupt |
| 4 | RAM100_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 100. Write 1h to disable the interrupt |
| 3 | RAM99_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 99. Write 1h to disable the interrupt |
| 2 | RAM98_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 98. Write 1h to disable the interrupt |
| 1 | RAM97_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 97. Write 1h to disable the interrupt |
| 0 | RAM96_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 96. Write 1h to disable the interrupt |

20.63 ECC_DED_ENABLE_CLR_REG4 Register (Offset = 1D0h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG4 is shown in [Figure 20-63](#) and described in [Table 20-64](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-63. ECC_DED_ENABLE_CLR_REG4 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM159_ENAB LE_CLR | RAM158_ENAB LE_CLR | RAM157_ENAB LE_CLR | RAM156_ENAB LE_CLR | RAM155_ENAB LE_CLR | RAM154_ENAB LE_CLR | RAM153_ENAB LE_CLR | RAM152_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM151_ENAB LE_CLR | RAM150_ENAB LE_CLR | RAM149_ENAB LE_CLR | RAM148_ENAB LE_CLR | RAM147_ENAB LE_CLR | RAM146_ENAB LE_CLR | RAM145_ENAB LE_CLR | RAM144_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM143_ENAB LE_CLR | RAM142_ENAB LE_CLR | RAM141_ENAB LE_CLR | RAM140_ENAB LE_CLR | RAM139_ENAB LE_CLR | RAM138_ENAB LE_CLR | RAM137_ENAB LE_CLR | RAM136_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM135_ENAB LE_CLR | RAM134_ENAB LE_CLR | RAM133_ENAB LE_CLR | RAM132_ENAB LE_CLR | RAM131_ENAB LE_CLR | RAM130_ENAB LE_CLR | RAM129_ENAB LE_CLR | RAM128_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-64. ECC_DED_ENABLE_CLR_REG4 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM159_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 159. Write 1h to disable the interrupt |
| 30 | RAM158_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 158. Write 1h to disable the interrupt |
| 29 | RAM157_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 157. Write 1h to disable the interrupt |
| 28 | RAM156_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 156. Write 1h to disable the interrupt |
| 27 | RAM155_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 155. Write 1h to disable the interrupt |
| 26 | RAM154_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 154. Write 1h to disable the interrupt |
| 25 | RAM153_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 153. Write 1h to disable the interrupt |

Table 20-64. ECC_DED_ENABLE_CLR_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM152_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 152. Write 1h to disable the interrupt |
| 23 | RAM151_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 151. Write 1h to disable the interrupt |
| 22 | RAM150_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 150. Write 1h to disable the interrupt |
| 21 | RAM149_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 149. Write 1h to disable the interrupt |
| 20 | RAM148_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 148. Write 1h to disable the interrupt |
| 19 | RAM147_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 147. Write 1h to disable the interrupt |
| 18 | RAM146_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 146. Write 1h to disable the interrupt |
| 17 | RAM145_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 145. Write 1h to disable the interrupt |
| 16 | RAM144_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 144. Write 1h to disable the interrupt |
| 15 | RAM143_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 143. Write 1h to disable the interrupt |
| 14 | RAM142_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 142. Write 1h to disable the interrupt |
| 13 | RAM141_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 141. Write 1h to disable the interrupt |
| 12 | RAM140_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 140. Write 1h to disable the interrupt |
| 11 | RAM139_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 139. Write 1h to disable the interrupt |
| 10 | RAM138_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 138. Write 1h to disable the interrupt |
| 9 | RAM137_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 137. Write 1h to disable the interrupt |

Table 20-64. ECC_DED_ENABLE_CLR_REG4 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM136_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 136. Write 1h to disable the interrupt |
| 7 | RAM135_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 135. Write 1h to disable the interrupt |
| 6 | RAM134_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 134. Write 1h to disable the interrupt |
| 5 | RAM133_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 133. Write 1h to disable the interrupt |
| 4 | RAM132_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 132. Write 1h to disable the interrupt |
| 3 | RAM131_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 131. Write 1h to disable the interrupt |
| 2 | RAM130_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 130. Write 1h to disable the interrupt |
| 1 | RAM129_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 129. Write 1h to disable the interrupt |
| 0 | RAM128_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 128. Write 1h to disable the interrupt |

20.64 ECC_DED_ENABLE_CLR_REG5 Register (Offset = 1D4h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG5 is shown in [Figure 20-64](#) and described in [Table 20-65](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-64. ECC_DED_ENABLE_CLR_REG5 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM191_ENAB LE_CLR | RAM190_ENAB LE_CLR | RAM189_ENAB LE_CLR | RAM188_ENAB LE_CLR | RAM187_ENAB LE_CLR | RAM186_ENAB LE_CLR | RAM185_ENAB LE_CLR | RAM184_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM183_ENAB LE_CLR | RAM182_ENAB LE_CLR | RAM181_ENAB LE_CLR | RAM180_ENAB LE_CLR | RAM179_ENAB LE_CLR | RAM178_ENAB LE_CLR | RAM177_ENAB LE_CLR | RAM176_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM175_ENAB LE_CLR | RAM174_ENAB LE_CLR | RAM173_ENAB LE_CLR | RAM172_ENAB LE_CLR | RAM171_ENAB LE_CLR | RAM170_ENAB LE_CLR | RAM169_ENAB LE_CLR | RAM168_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM167_ENAB LE_CLR | RAM166_ENAB LE_CLR | RAM165_ENAB LE_CLR | RAM164_ENAB LE_CLR | RAM163_ENAB LE_CLR | RAM162_ENAB LE_CLR | RAM161_ENAB LE_CLR | RAM160_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-65. ECC_DED_ENABLE_CLR_REG5 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM191_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 191. Write 1h to disable the interrupt |
| 30 | RAM190_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 190. Write 1h to disable the interrupt |
| 29 | RAM189_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 189. Write 1h to disable the interrupt |
| 28 | RAM188_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 188. Write 1h to disable the interrupt |
| 27 | RAM187_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 187. Write 1h to disable the interrupt |
| 26 | RAM186_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 186. Write 1h to disable the interrupt |
| 25 | RAM185_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 185. Write 1h to disable the interrupt |

Table 20-65. ECC_DED_ENABLE_CLR_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM184_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 184. Write 1h to disable the interrupt |
| 23 | RAM183_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 183. Write 1h to disable the interrupt |
| 22 | RAM182_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 182. Write 1h to disable the interrupt |
| 21 | RAM181_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 181. Write 1h to disable the interrupt |
| 20 | RAM180_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 180. Write 1h to disable the interrupt |
| 19 | RAM179_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 179. Write 1h to disable the interrupt |
| 18 | RAM178_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 178. Write 1h to disable the interrupt |
| 17 | RAM177_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 177. Write 1h to disable the interrupt |
| 16 | RAM176_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 176. Write 1h to disable the interrupt |
| 15 | RAM175_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 175. Write 1h to disable the interrupt |
| 14 | RAM174_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 174. Write 1h to disable the interrupt |
| 13 | RAM173_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 173. Write 1h to disable the interrupt |
| 12 | RAM172_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 172. Write 1h to disable the interrupt |
| 11 | RAM171_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 171. Write 1h to disable the interrupt |
| 10 | RAM170_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 170. Write 1h to disable the interrupt |
| 9 | RAM169_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 169. Write 1h to disable the interrupt |

Table 20-65. ECC_DED_ENABLE_CLR_REG5 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM168_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 168. Write 1h to disable the interrupt |
| 7 | RAM167_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 167. Write 1h to disable the interrupt |
| 6 | RAM166_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 166. Write 1h to disable the interrupt |
| 5 | RAM165_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 165. Write 1h to disable the interrupt |
| 4 | RAM164_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 164. Write 1h to disable the interrupt |
| 3 | RAM163_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 163. Write 1h to disable the interrupt |
| 2 | RAM162_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 162. Write 1h to disable the interrupt |
| 1 | RAM161_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 161. Write 1h to disable the interrupt |
| 0 | RAM160_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 160. Write 1h to disable the interrupt |

20.65 ECC_DED_ENABLE_CLR_REG6 Register (Offset = 1D8h) [reset = 0h]

ECC_DED_ENABLE_CLR_REG6 is shown in [Figure 20-65](#) and described in [Table 20-66](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-65. ECC_DED_ENABLE_CLR_REG6 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM223_ENAB LE_CLR | RAM222_ENAB LE_CLR | RAM221_ENAB LE_CLR | RAM220_ENAB LE_CLR | RAM219_ENAB LE_CLR | RAM218_ENAB LE_CLR | RAM217_ENAB LE_CLR | RAM216_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM215_ENAB LE_CLR | RAM214_ENAB LE_CLR | RAM213_ENAB LE_CLR | RAM212_ENAB LE_CLR | RAM211_ENAB LE_CLR | RAM210_ENAB LE_CLR | RAM209_ENAB LE_CLR | RAM208_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM207_ENAB LE_CLR | RAM206_ENAB LE_CLR | RAM205_ENAB LE_CLR | RAM204_ENAB LE_CLR | RAM203_ENAB LE_CLR | RAM202_ENAB LE_CLR | RAM201_ENAB LE_CLR | RAM200_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM199_ENAB LE_CLR | RAM198_ENAB LE_CLR | RAM197_ENAB LE_CLR | RAM196_ENAB LE_CLR | RAM195_ENAB LE_CLR | RAM194_ENAB LE_CLR | RAM193_ENAB LE_CLR | RAM192_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-66. ECC_DED_ENABLE_CLR_REG6 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM223_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 223. Write 1h to disable the interrupt |
| 30 | RAM222_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 222. Write 1h to disable the interrupt |
| 29 | RAM221_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 221. Write 1h to disable the interrupt |
| 28 | RAM220_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 220. Write 1h to disable the interrupt |
| 27 | RAM219_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 219. Write 1h to disable the interrupt |
| 26 | RAM218_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 218. Write 1h to disable the interrupt |
| 25 | RAM217_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 217. Write 1h to disable the interrupt |

Table 20-66. ECC_DED_ENABLE_CLR_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM216_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 216. Write 1h to disable the interrupt |
| 23 | RAM215_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 215. Write 1h to disable the interrupt |
| 22 | RAM214_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 214. Write 1h to disable the interrupt |
| 21 | RAM213_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 213. Write 1h to disable the interrupt |
| 20 | RAM212_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 212. Write 1h to disable the interrupt |
| 19 | RAM211_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 211. Write 1h to disable the interrupt |
| 18 | RAM210_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 210. Write 1h to disable the interrupt |
| 17 | RAM209_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 209. Write 1h to disable the interrupt |
| 16 | RAM208_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 208. Write 1h to disable the interrupt |
| 15 | RAM207_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 207. Write 1h to disable the interrupt |
| 14 | RAM206_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 206. Write 1h to disable the interrupt |
| 13 | RAM205_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 205. Write 1h to disable the interrupt |
| 12 | RAM204_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 204. Write 1h to disable the interrupt |
| 11 | RAM203_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 203. Write 1h to disable the interrupt |
| 10 | RAM202_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 202. Write 1h to disable the interrupt |
| 9 | RAM201_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 201. Write 1h to disable the interrupt |

Table 20-66. ECC_DED_ENABLE_CLR_REG6 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM200_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 200. Write 1h to disable the interrupt |
| 7 | RAM199_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 199. Write 1h to disable the interrupt |
| 6 | RAM198_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 198. Write 1h to disable the interrupt |
| 5 | RAM197_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 197. Write 1h to disable the interrupt |
| 4 | RAM196_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 196. Write 1h to disable the interrupt |
| 3 | RAM195_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 195. Write 1h to disable the interrupt |
| 2 | RAM194_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 194. Write 1h to disable the interrupt |
| 1 | RAM193_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 193. Write 1h to disable the interrupt |
| 0 | RAM192_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 192. Write 1h to disable the interrupt |

20.66 ECC_DED_ENABLE_CLR_REG7 Register (Offset = 1DCh) [reset = 0h]

ECC_DED_ENABLE_CLR_REG7 is shown in [Figure 20-66](#) and described in [Table 20-67](#).

Return to [Summary Table](#).

Interrupt disable register for non-correctable error. Each bit corresponds to an ECC endpoint. Depending on the number of ECC endpoints associated with a module or subsystem some of the bits may not be used.

Figure 20-66. ECC_DED_ENABLE_CLR_REG7 Register

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| RAM255_ENAB LE_CLR | RAM254_ENAB LE_CLR | RAM253_ENAB LE_CLR | RAM252_ENAB LE_CLR | RAM251_ENAB LE_CLR | RAM250_ENAB LE_CLR | RAM249_ENAB LE_CLR | RAM248_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM247_ENAB LE_CLR | RAM246_ENAB LE_CLR | RAM245_ENAB LE_CLR | RAM244_ENAB LE_CLR | RAM243_ENAB LE_CLR | RAM242_ENAB LE_CLR | RAM241_ENAB LE_CLR | RAM240_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAM239_ENAB LE_CLR | RAM238_ENAB LE_CLR | RAM237_ENAB LE_CLR | RAM236_ENAB LE_CLR | RAM235_ENAB LE_CLR | RAM234_ENAB LE_CLR | RAM233_ENAB LE_CLR | RAM232_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM231_ENAB LE_CLR | RAM230_ENAB LE_CLR | RAM229_ENAB LE_CLR | RAM228_ENAB LE_CLR | RAM227_ENAB LE_CLR | RAM226_ENAB LE_CLR | RAM225_ENAB LE_CLR | RAM224_ENAB LE_CLR |
| R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

LEGEND: R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-67. ECC_DED_ENABLE_CLR_REG7 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 31 | RAM255_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 255. Write 1h to disable the interrupt |
| 30 | RAM254_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 254. Write 1h to disable the interrupt |
| 29 | RAM253_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 253. Write 1h to disable the interrupt |
| 28 | RAM252_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 252. Write 1h to disable the interrupt |
| 27 | RAM251_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 251. Write 1h to disable the interrupt |
| 26 | RAM250_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 250. Write 1h to disable the interrupt |
| 25 | RAM249_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 249. Write 1h to disable the interrupt |

Table 20-67. ECC_DED_ENABLE_CLR_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 24 | RAM248_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 248. Write 1h to disable the interrupt |
| 23 | RAM247_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 247. Write 1h to disable the interrupt |
| 22 | RAM246_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 246. Write 1h to disable the interrupt |
| 21 | RAM245_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 245. Write 1h to disable the interrupt |
| 20 | RAM244_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 244. Write 1h to disable the interrupt |
| 19 | RAM243_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 243. Write 1h to disable the interrupt |
| 18 | RAM242_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 242. Write 1h to disable the interrupt |
| 17 | RAM241_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 241. Write 1h to disable the interrupt |
| 16 | RAM240_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 240. Write 1h to disable the interrupt |
| 15 | RAM239_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 239. Write 1h to disable the interrupt |
| 14 | RAM238_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 238. Write 1h to disable the interrupt |
| 13 | RAM237_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 237. Write 1h to disable the interrupt |
| 12 | RAM236_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 236. Write 1h to disable the interrupt |
| 11 | RAM235_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 235. Write 1h to disable the interrupt |
| 10 | RAM234_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 234. Write 1h to disable the interrupt |
| 9 | RAM233_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 233. Write 1h to disable the interrupt |

Table 20-67. ECC_DED_ENABLE_CLR_REG7 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|-------|-------|--|
| 8 | RAM232_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 232. Write 1h to disable the interrupt |
| 7 | RAM231_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 231. Write 1h to disable the interrupt |
| 6 | RAM230_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 230. Write 1h to disable the interrupt |
| 5 | RAM229_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 229. Write 1h to disable the interrupt |
| 4 | RAM228_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 228. Write 1h to disable the interrupt |
| 3 | RAM227_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 227. Write 1h to disable the interrupt |
| 2 | RAM226_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 226. Write 1h to disable the interrupt |
| 1 | RAM225_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 225. Write 1h to disable the interrupt |
| 0 | RAM224_ENABLE_CLR | R/W1C | 0h | Non-correctable error interrupt disable for ECC endpoint with ID = 224. Write 1h to disable the interrupt |

20.67 ECC_AGGR_ENABLE_SET Register (Offset = 200h) [reset = 0h]

ECC_AGGR_ENABLE_SET is shown in [Figure 20-67](#) and described in [Table 20-68](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Set Register

Figure 20-67. ECC_AGGR_ENABLE_SET Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R-0h | | | | | | R/W1S-0h | R/W1S-0h |

LEGEND: R = Read Only; R/W1S = Read/Write 1 to Set Bit; -n = value after reset

Table 20-68. ECC_AGGR_ENABLE_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R | 0h | Reserved |
| 1 | TIMEOUT | R/W1S | 0h | Interrupt enable set for ECC serial interface timeout errors. Write 1h to enable timeout errors. |
| 0 | PARITY | R/W1S | 0h | Interrupt enable set for parity errors. Write 1h to enable parity errors. |

20.68 ECC_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = 0h]

ECC_AGGR_ENABLE_CLR is shown in [Figure 20-68](#) and described in [Table 20-69](#).

Return to [Summary Table](#).

Aggregator Interrupt Enable Clear Register

Figure 20-68. ECC_AGGR_ENABLE_CLR Register

| | | | | | | | |
|----------|----|----|----|----|----|----------|----------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | TIMEOUT | PARITY |
| R-0h | | | | | | R/W1C-0h | R/W1C-0h |

LEGEND: R = Read Only; R/W1C = Read/Write 1 to Clear Bit; -n = value after reset

Table 20-69. ECC_AGGR_ENABLE_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|-------|-------|---|
| 31-2 | RESERVED | R | 0 | Reserved |
| 1 | TIMEOUT | R/W1C | 0h | Interrupt disable for ECC serial interface timeout errors. Write 1h to disable timeout errors. |
| 0 | PARITY | R/W1C | 0h | Interrupt disable for parity errors. Write 1h to disable parity errors. |

20.69 ECC_AGGR_STATUS_SET Register (Offset = 208h) [reset = 0h]

ECC_AGGR_STATUS_SET is shown in [Figure 20-69](#) and described in [Table 20-70](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Set Register

Figure 20-69. ECC_AGGR_STATUS_SET Register

| | | | | | | | |
|----------|----|----|----|---------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R-0h | | | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 20-70. ECC_AGGR_STATUS_SET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R | 0 | Reserved |
| 3-2 | TIMEOUT | R/W | 0h | 2-bit saturating counter for the number of timeout errors that have occurred since last cleared. A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this field goes from 0h to non-zero value a level interrupt is asserted. If the value is non-zero then the interrupt remains asserted. 0h - No timeout errors have occurred 1h - 1 timeout error has occurred 2h - 2 timeout errors have occurred 3h - 3 or more timeout error have occurred |
| 1-0 | PARITY | R/W | 0h | 2-bit saturating counter for the number of parity errors that have occurred since last cleared. A write of a non-zero value to this field increments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this field goes from 0h to non-zero value a level interrupt is asserted. If the value is non-zero then the interrupt remains asserted. 0h - No parity errors have occurred 1h - 1 parity error has occurred 2h - 2 parity errors have occurred 3h - 3 or more parity errors have occurred |

20.70 ECC_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = 0h]

ECC_AGGR_STATUS_CLR is shown in [Figure 20-70](#) and described in [Table 20-71](#).

Return to [Summary Table](#).

Aggregator Interrupt Status Clear Register

Figure 20-70. ECC_AGGR_STATUS_CLR Register

| | | | | | | | |
|----------|----|----|----|---------|----|--------|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | TIMEOUT | | PARITY | |
| R-0h | | | | R/W-0h | | R/W-0h | |

LEGEND: R = Read Only; R/W = Read/Write; -n = value after reset

Table 20-71. ECC_AGGR_STATUS_CLR Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|----------|------|-------|--|
| 31-4 | RESERVED | R | 0 | Reserved |
| 3-2 | TIMEOUT | R/W | 0h | Interrupt status clear for ECC serial interface timeout errors. A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting value is not zero, then the pending level interrupt stays asserted. If the value written is more than the counter value, then the result is zero. 0h - No timeout errors have occurred 1h - 1 timeout error has occurred 2h - 2 timeout errors have occurred 3h - 3 or more timeout error have occurred |
| 1-0 | PARITY | R/W | 0h | Interrupt status clear for parity errors. A write of a non-zero value to this register decrements that many from the parity fields. If the resulting value is not zero, then the pending level interrupt stays asserted. If the value written is more than the counter value, then the result is zero. 0h - No parity errors have occurred 1h - 1 parity error has occurred 2h - 2 parity errors have occurred 3h - 3 or more parity errors have occurred |

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