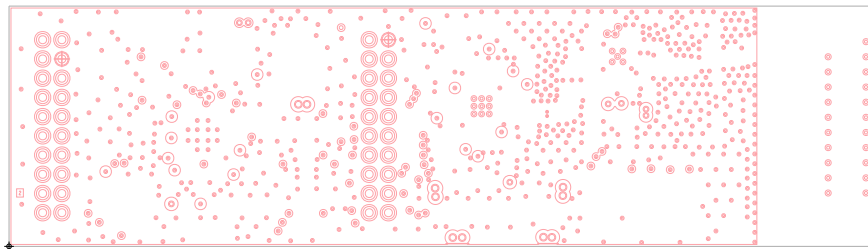
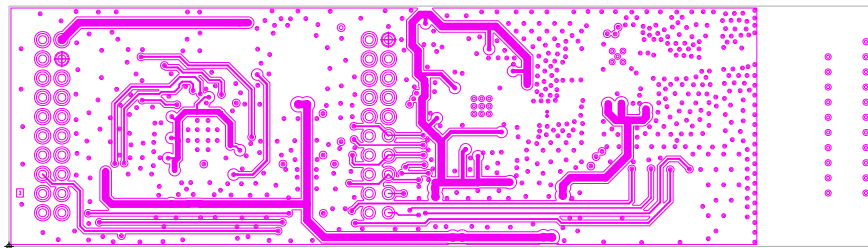


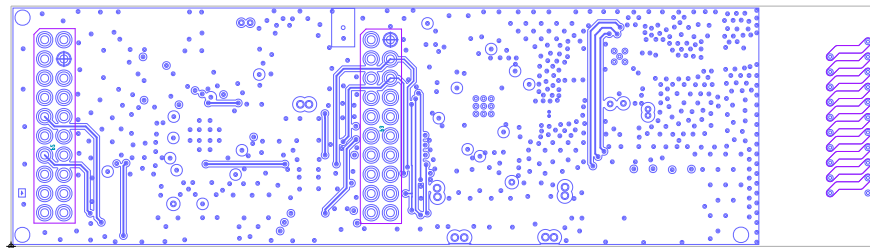
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90		LAYER DESCRIPTION: Top Layer Assembly-Top	
PROJECT NUMBER: XXXXXX		BOARD REV: A	RELEASE DATE: 2015-10-19
		SHEET NUMBER: 11 of 10	



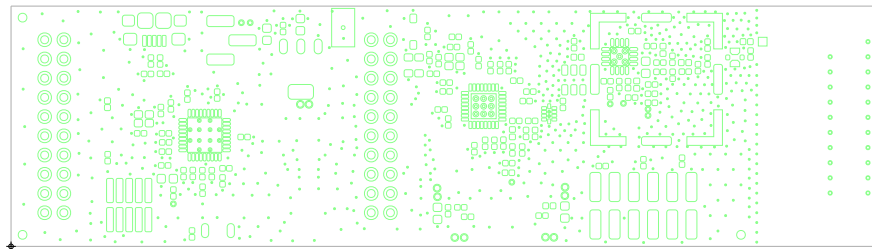
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90	LAYER DESCRIPTION: Layer-2		
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 2 of 10



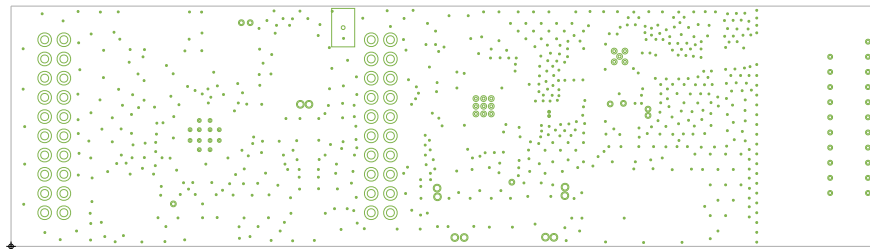
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90	LAYER DESCRIPTION: Layer-3		
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 3 of 10



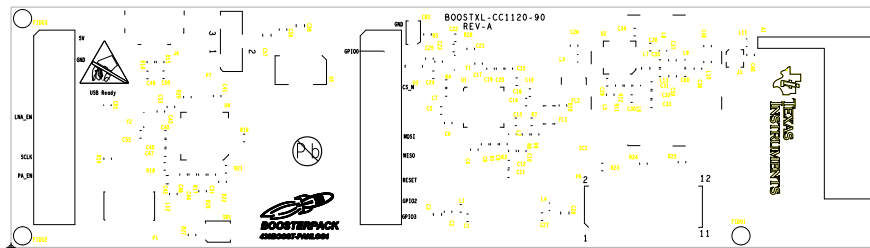
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90	LAYER DESCRIPTION: <i>revD</i> <i>mottoB</i> <i>Assembly-Bottom</i>		
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: <i>42</i> of <i>120</i>



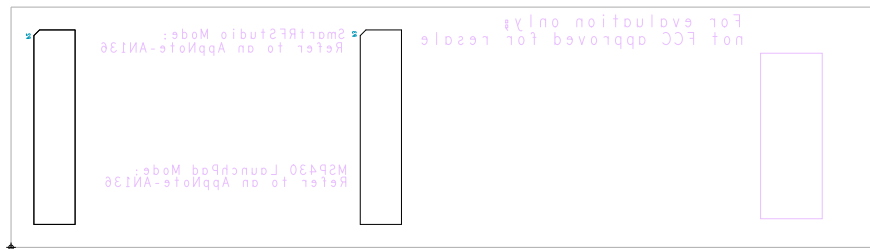
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90		LAYER DESCRIPTION: Soldermask-Top	
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 5 of 10



CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90		LAYER DESCRIPTION: Soldermask-Bottom	
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 6 of 10

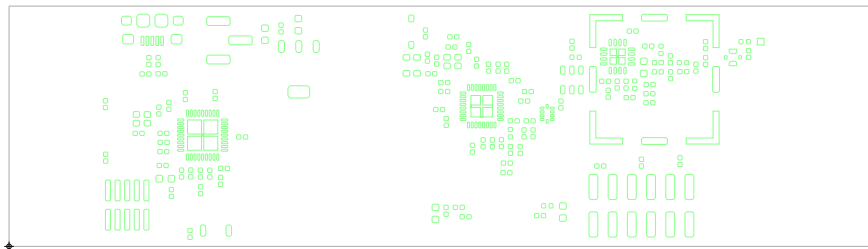


CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90		LAYER DESCRIPTION: Silkscreen-Top	
PROJECT NUMBER: XXXXXX		BOARD REV: A	RELEASE DATE: 2015-10-19
		SHEET NUMBER: 7 of 10	



CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90	LAYER DESCRIPTION: <i>Silkscreen-Bottom</i>		
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: <i>8</i> of 10



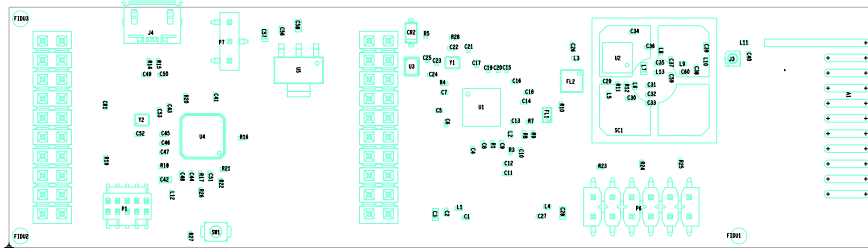


CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90		LAYER DESCRIPTION: Pastemask - Top	
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 9 of 10



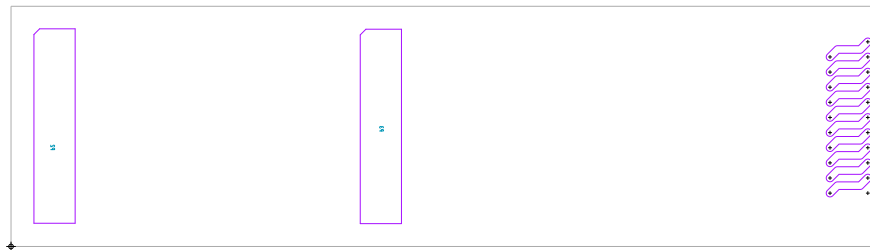
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90	LAYER DESCRIPTION: Pastemask-Bottom		
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 10 of 10

Note: Connectors P2 and P3 should be mounted from the Bottom side. The pins of the connectors should appear on the TOP side



CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90		LAYER DESCRIPTION: Assembly-Top	
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 1 of 2

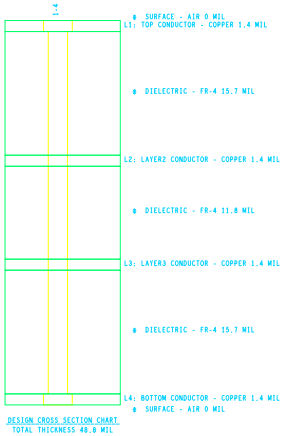
Note: Connectors P2 and P3 should be mounted from the Bottom side. The pins of the connectors should appear on the TOP side



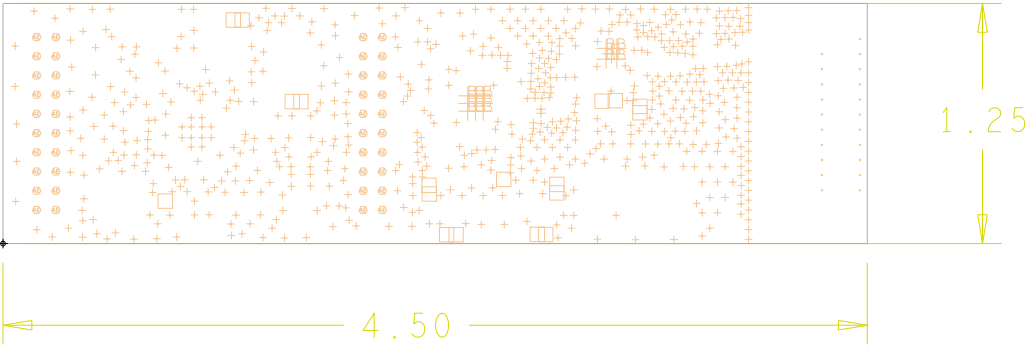
CUSTOMER: Texas Instruments			
BOARD NAME: BOOSTXL-CC120-90	LAYER DESCRIPTION: Assembly-Bottom		
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 2 of 2

FAB NOTES:  
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE NOTED.  
2. ALL FABRICATES TO IPC-6013 TYPE 2. WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2, CURRENT REVISIONS.  
3. BOARD MATERIAL SHALL BE 10/10/40 50/50 ISOLA FR-3700R OR EQUIVALENT AND LEAD-FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED IPC-4101B. RoHS CERTIFICATE OF CONFORMANCE SHALL BE DELIVERED WITH EACH LOT.  
4. BOARD MATERIAL CONDUCTOR THICKNESS SHALL BE 1.4 MIL. PREFERRED AND UL GREEN NUMBER SHOULD BE MARKED ON PLATING BOARD.  
5. OVERALL BOARD THICKNESS TO BE .040" +/- .005" AND APPLIED AFTER ALL LAMINATION AND PLATING PROCESSES, MEASURED FROM COPPER TO COPPER.  
6. MAX. WIP & WIP OFF DOTS PER INCH:  
7. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED IPC-D-259 NETLIST.  
8. 28 MIL TRACES ON LAYER 1 ARE 50 OHMS +/-10%. THEY ARE REFERENCE TO LAYER 2 GROUND.

PROCESS NOTES:  
1. APPLY LPT1 SOLDERMASK OVER BARE COPPER (SMORC). SOLDERMASK SHALL CONFORM TO IPC-SM-840, CLASS H, CURRENT REV. COLOR OF MASK TO BE RED.  
2. PLATE ALL EXPOSED AREAS WITH ELECTROPLATED NICKEL. IMMERSION GOLD. NICKEL 100 MICRO INCHES MIN. MINIMUM 1/8 MICRO INCHES MIN.  
3. SOLDERMASK ARTWORK HAS ZERO (0) OVERLAP PASS. FABRICATION TOLERANCE IS ALLOWED TO ADJUST THE COMPONENT SOLDERMASK PADS TO MEET THEIR TOOLING REQUIREMENTS.  
4. APPLY NON-CONDUCTIVE LPT1 SILKSCREEN OR EQUIVALENT PER THE ARTWORK. COLOR: WHITE.  
5. ALL VIAS ARE TENTED



DRILL CHART: TOP to BOTTOM					
ALL UNITS ARE IN MILS					
FIGURE	SIZE	TOLERANCE	PLATED	QTY	
+	8.0	+3.0/-3.0	PLATED	2	
+	10.0	+3.0/-3.0	PLATED	672	
⊢	15.0	+3.0/-3.0	PLATED	14	
.	15.75	+3.0/-3.0	PLATED	21	
+	20.0	+3.0/-3.0	PLATED	1	
□	20.0	+3.0/-3.0	PLATED	8	
□	30.0	+3.0/-3.0	PLATED	10	
⊙	41.34	+3.0/-3.0	PLATED	40	



CUSTOMER: Texas Instruments			
BOARD NAME: BO0STXL-CC120-90		LAYER DESCRIPTION: Fabrication Drawing	
PROJECT NUMBER: XXXXXX	BOARD REV: A	RELEASE DATE: 2015-10-19	SHEET NUMBER: 1 of 1

