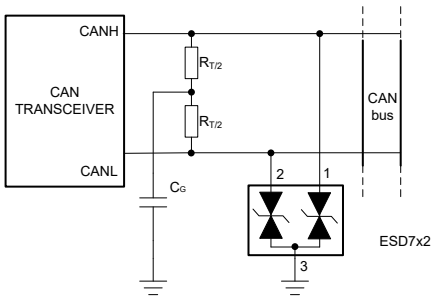
ESD752 24V, 2-Channel ESD Protection Diode in DFN1110 Industry Standard Package for In-Vehicle Networks

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±30kV contact discharge
  - ±30kV air-gap discharge
- Tested in compliance to IEC 61000-4-5
- 24V working voltage
- Bidirectional ESD protection
- 2-channel device provides complete ESD protection with single component
- Low clamping voltage protects downstream components
- I/O capacitance = 3pF (typical)
- DFN1110 (DXA) small, standard, common footprint

2 Applications

- Industrial control networks:
  - Smart distribution system (SDS)
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4
  - 4/20mA circuits
  - PLC surge protection
  - ADC surge protection



ESD752 Typical Application

3 Description

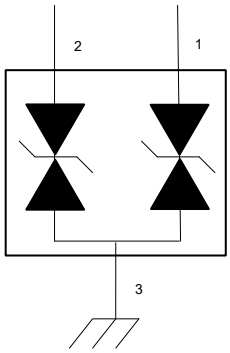
ESD752 is a bidirectional ESD protection diode for Controller Area Network (CAN) interface protection. ESD752 is rated to dissipate contact ESD strikes specified in the IEC 61000-4-2 standard. The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key as industrial systems require a high level of robustness and reliability for safety applications.

This device features a low IO capacitance per channel and a pin-out to suit two CAN bus lines (CANH and CANL) from the damage caused by ElectroStatic Discharge (ESD) and other transients. Additionally, the 3pF (typical) line capacitance of ESD752 is suitable for CAN, CANFD, CAN SiC, and CAN-XL applications that can support data rates up to 20Mbps.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
ESD752	DXA (DFN1110, 3)	1.1mm × 1.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

Table of Contents

4 Pin Configuration and Functions

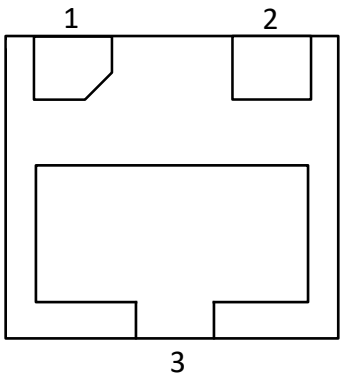


Figure 4-1. DXA Package, 3-Pin DFN1110 (Bottom View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20µs) at 25°C		210	W
Peak pulse	IEC 61000-4-5 current (t_p - 8/20µs) at 25°C		4.7	A
T_A	Operating free-air temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

5.5 Thermal Information

THERMAL METRIC[1]		ESD752 DXA (DFN1110-3) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	284.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	147.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	127.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	126.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–24		24	V
V_{BR}	Breakdown voltage	I_{IO} = 10mA, IO to GND, both Positive and Negative	25.5		35.5	V
I_{LEAK}	Leakage current	V_{IO} = ±24V, IO to GND	-50	1.2	50	nA
V_{CLAMP}	Clamping voltage[2]	I_{PP} = 4.7A, t_p = 8/20µs, IO to GND		37		V
V_{CLAMP}	Clamping voltage[3]	I_{PP} = 16A, TLP, O to GND		38		V
R_{DYN}	Dynamic resistance[3]	IO to GND		0.43		Ω
		GND to IO		0.43		
C_L	Line capacitance	V_{IO} = 0V, f = 1MHz, V_{p-p} = 30mV		3		pF

(1) Measurements made on both IO channels
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

5.7 Typical Characteristics

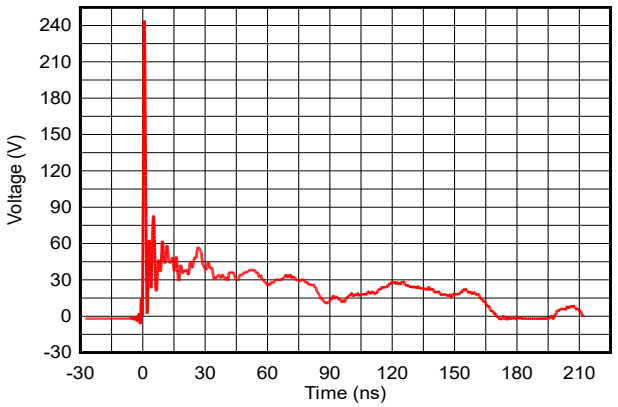


Figure 5-1. +8kV Clamped IEC Waveform

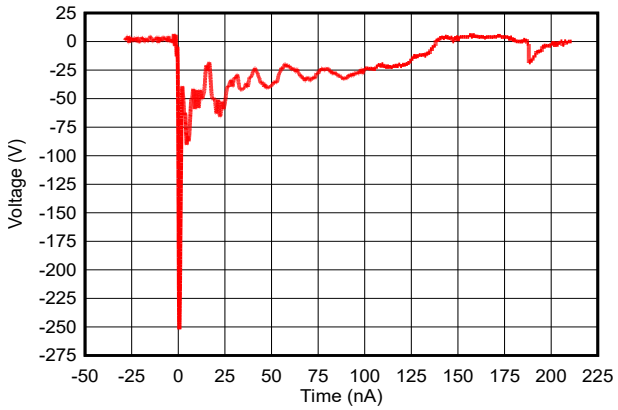


Figure 5-2. -8kV Clamped IEC Waveform

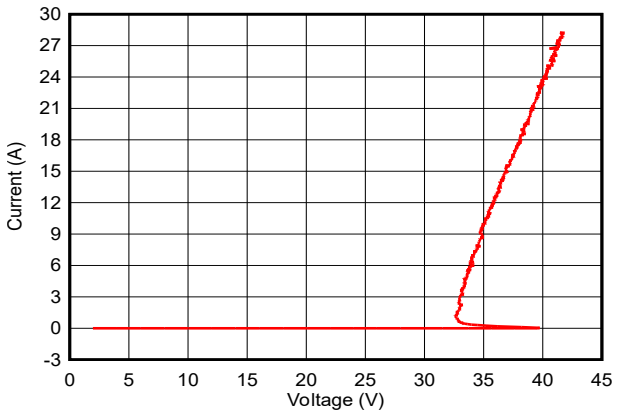


Figure 5-3. Positive TLP Curve

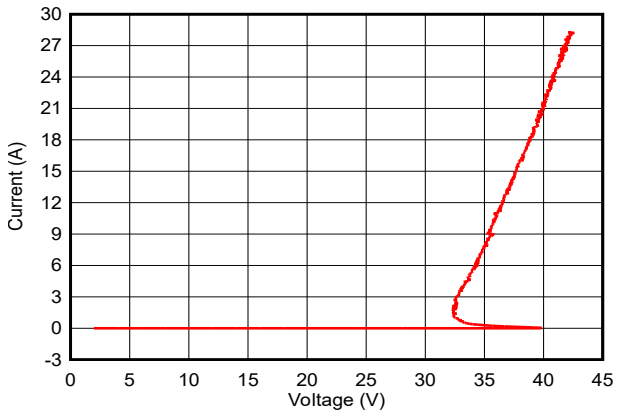


Figure 5-4. Negative TLP Curve

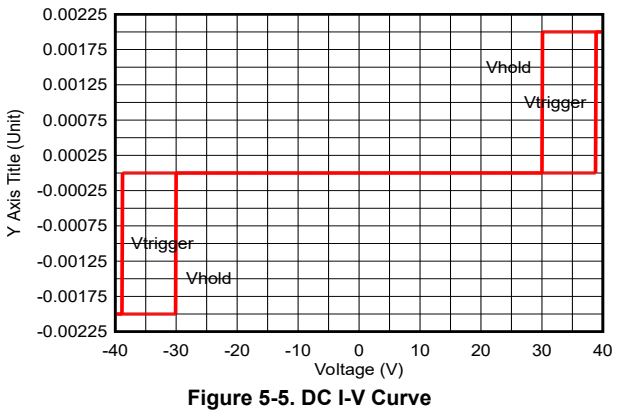


Figure 5-5. DC I-V Curve

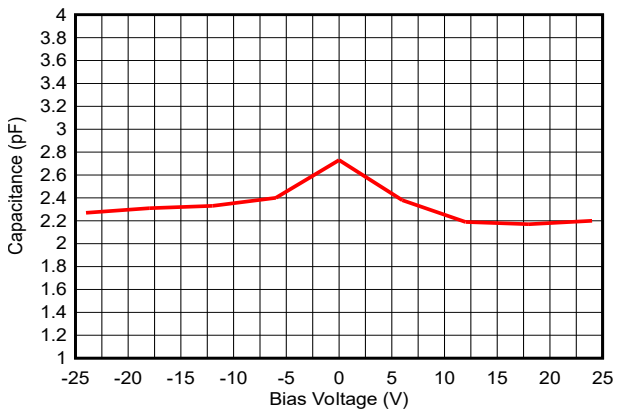


Figure 5-6. Bias Voltage vs Capacitance

5.7 Typical Characteristics (continued)

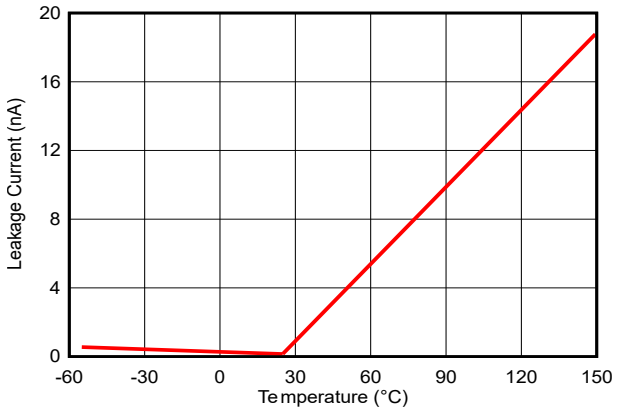


Figure 5-7. Leakage Current vs Temperature

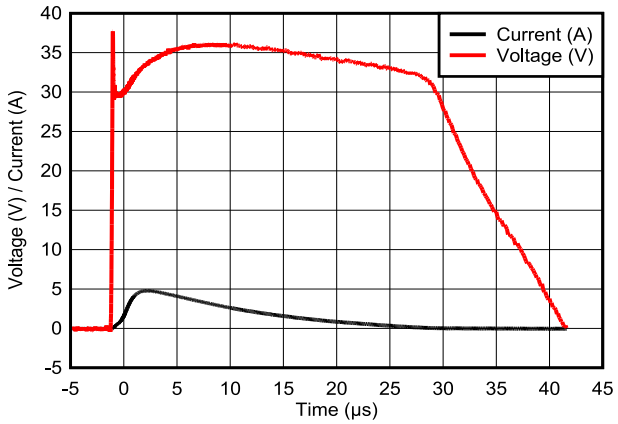


Figure 5-8. 8/20µs Surge Response

6 Layout

6.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 3 is connected to ground, use a thick and short trace for this return path.

6.2 Layout Example

This example is typical of a dual channel differential data pair application, such as CAN.

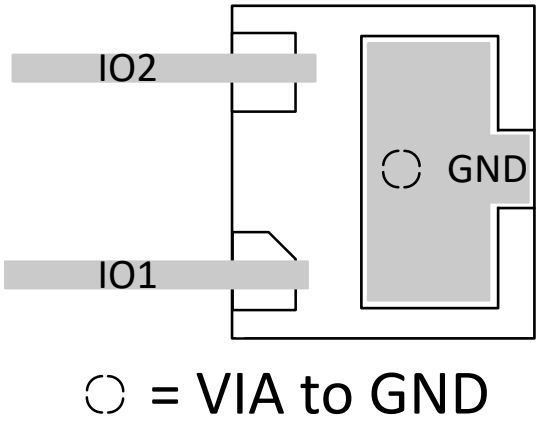


Figure 6-1. Routing with DXA Package

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Protecting Automotive Can Bus Systems from ESD Overvoltage Events* application note
- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.4 Trademarks

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD752DBZR	Active	Production	SOT-23 (DBZ) | 3	3000 | JUMBO T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8
ESD752DBZR.B	Active	Production	SOT-23 (DBZ) | 3	3000 | JUMBO T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8
ESD752DCKR	Active	Production	SC70 (DCK) | 3	3000 | JUMBO T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 150	1MP
ESD752DCKR.B	Active	Production	SC70 (DCK) | 3	3000 | JUMBO T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 150	1MP
ESD752DXAR	Active	Production	USON (DXA) | 3	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-55 to 150	1WW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

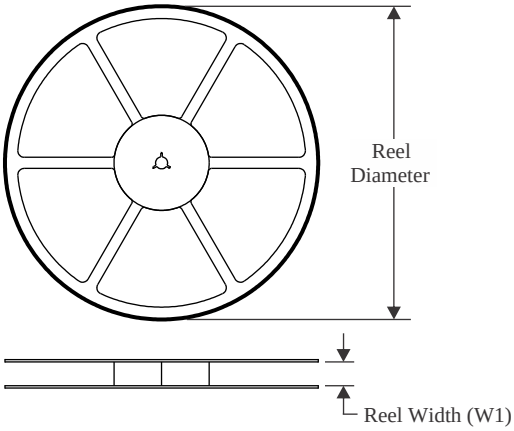
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

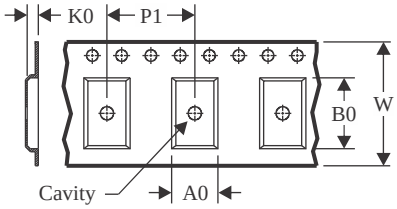
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

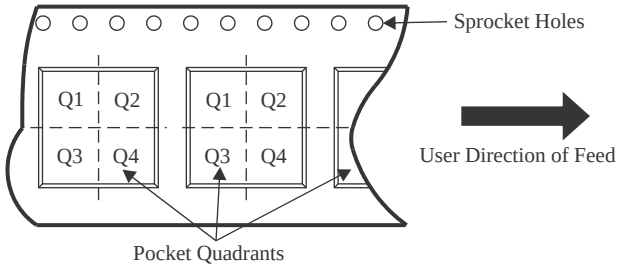


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

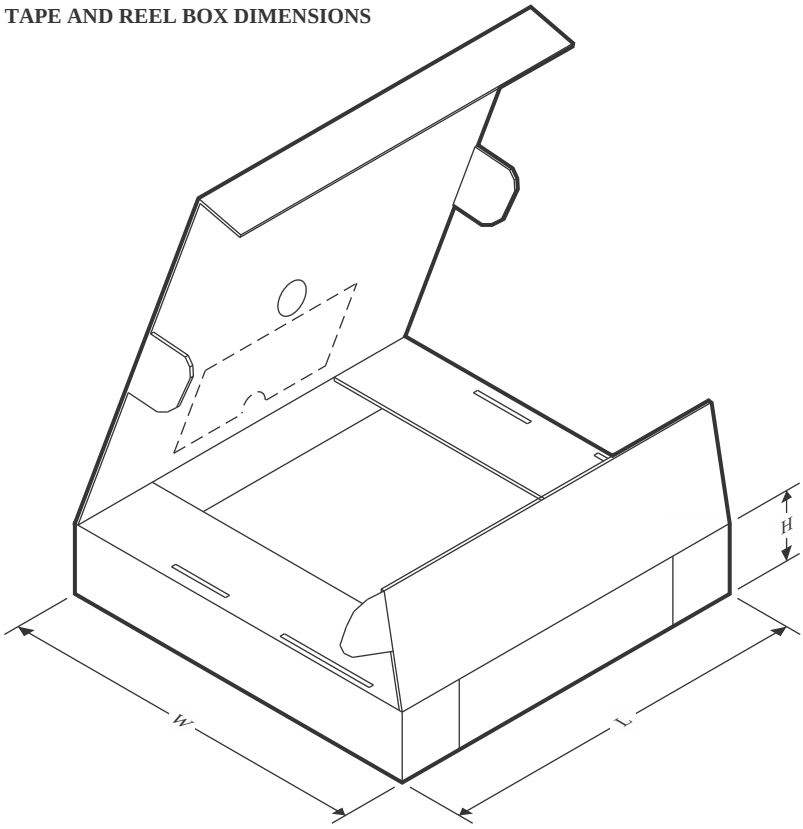
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD752DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD752DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

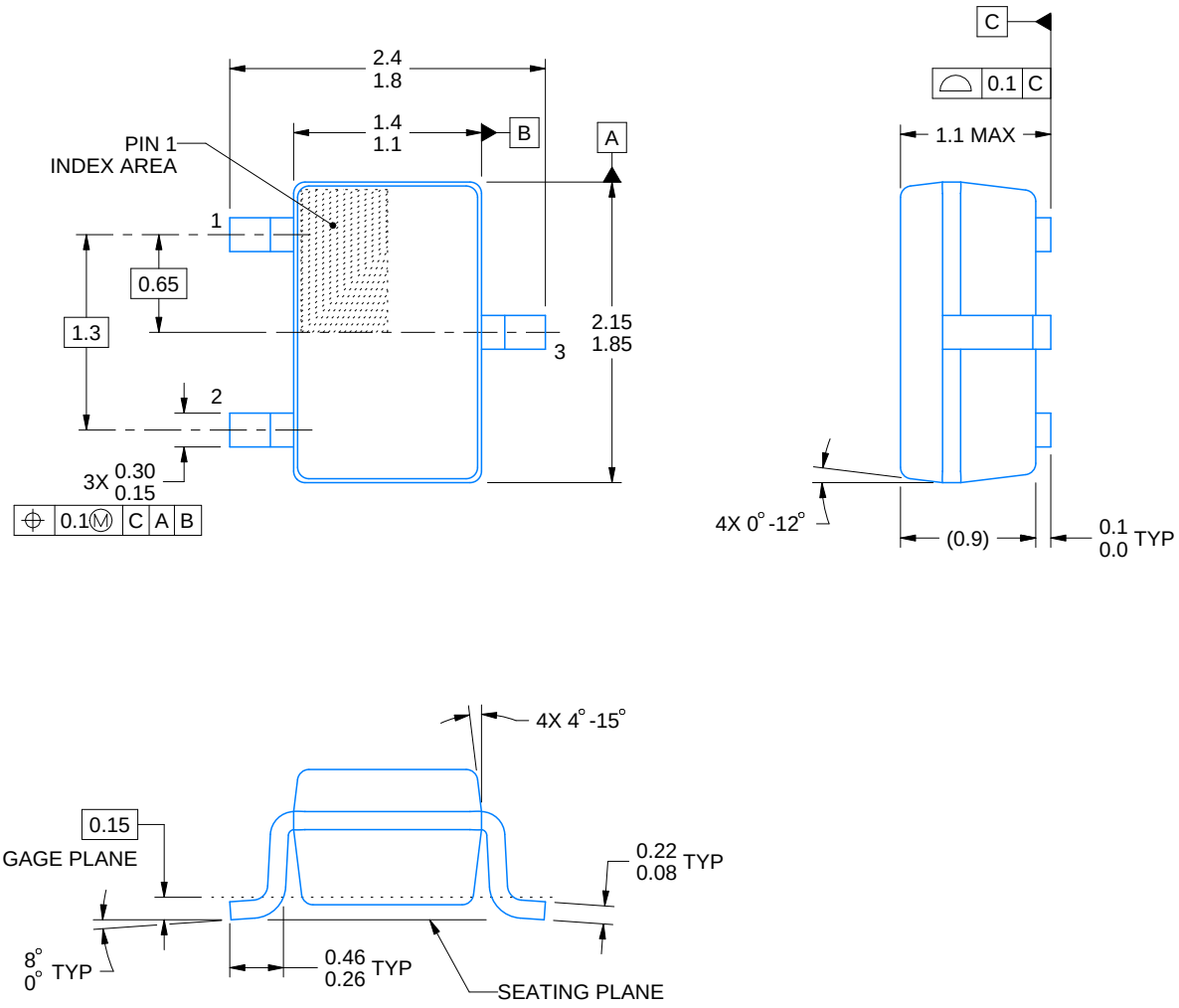
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD752DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD752DCKR	SC70	DCK	3	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

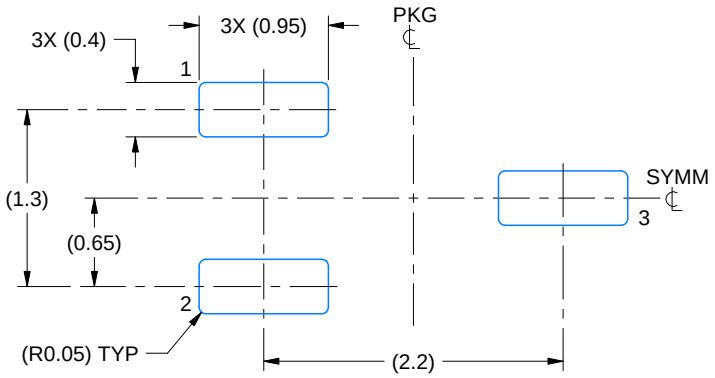
SMALL OUTLINE TRANSISTOR SC70



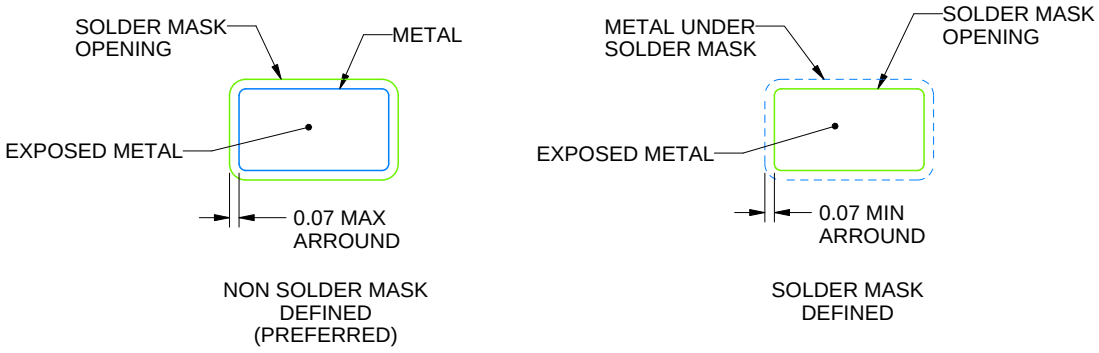
4220745/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

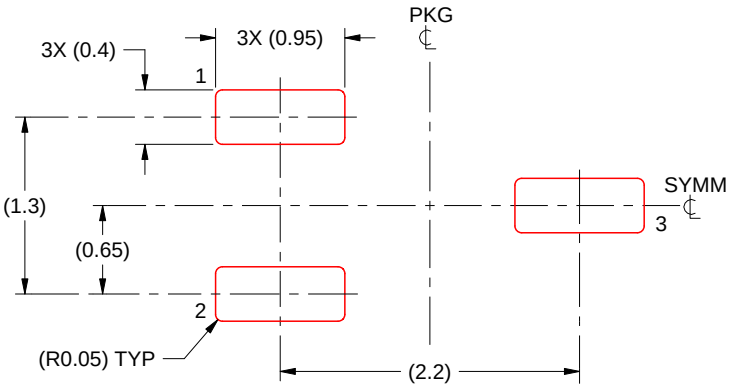


SOLDER MASK DETAILS

4220745/F 11/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

NOTES: (continued)

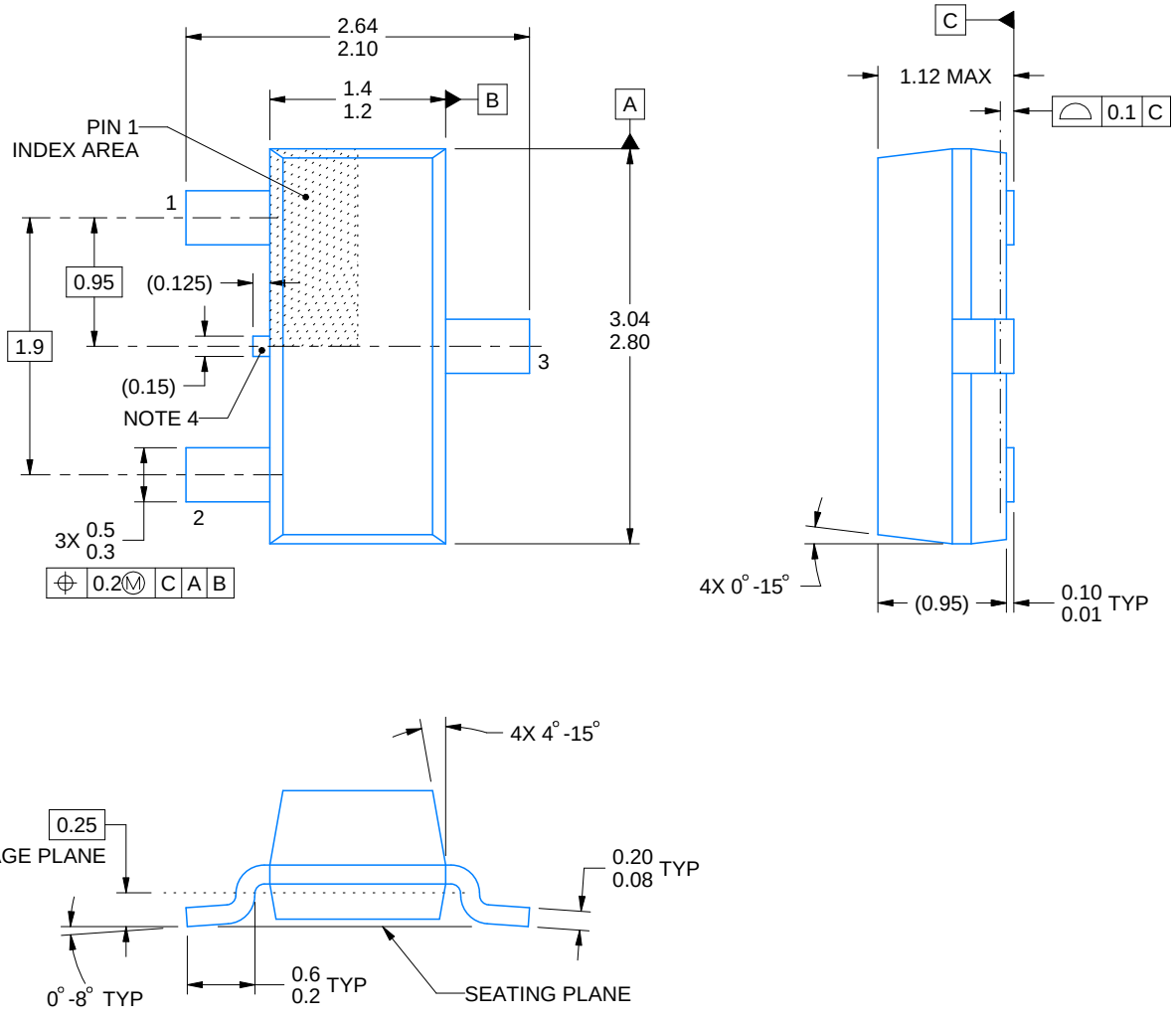
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

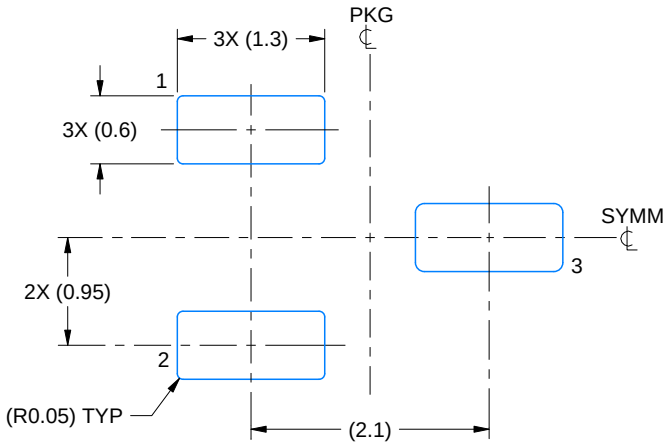
SMALL OUTLINE TRANSISTOR



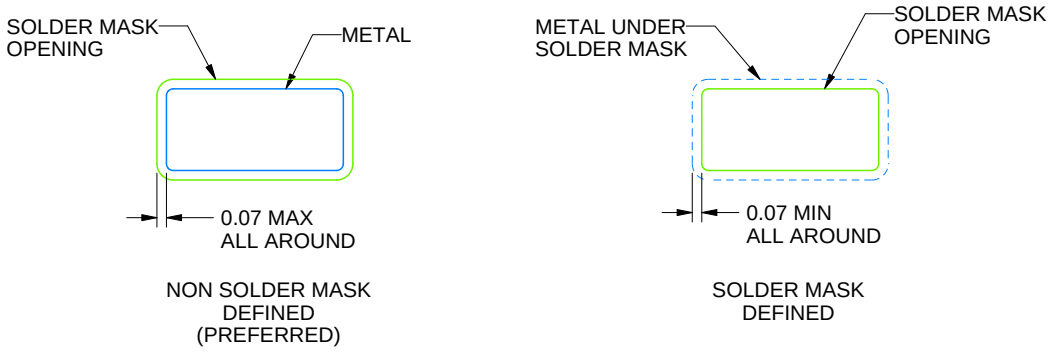
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

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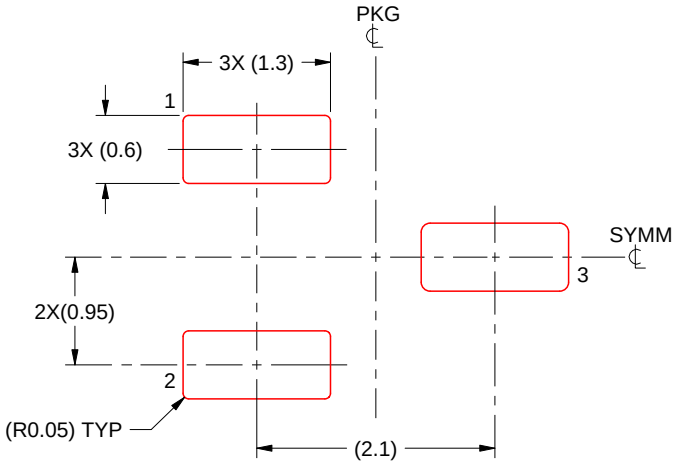
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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