SBOS312B − JULY 2004 − REVISED DECEMBER 2004

Stereo Audio Volume Control

FEATURES

- **DIGITALLY-CONTROLLED ANALOG VOLUME CONTROL:**
  - **Two Independent Audio Channels**
  - **Serial Control Interface**
  - **Zero Crossing Detection**
  - **Mute Function**
- **WIDE GAIN AND ATTENUATION RANGE:**
  +31.5dB to −95.5dB with 0.5dB Steps
- **LOW NOISE AND DISTORTION:**
  120dB Dynamic Range
  0.0003% THD+N at 1kHz
- **LOW INTERCHANNEL CROSSTALK:**
  −126dBFS
- **NOISE-FREE LEVEL TRANSITIONS**
- **POWER SUPPLIES: ±15V Analog, +5V Digital**
- **AVAILABLE IN SOL−16 PACKAGE**
- **PIN-FOR-PIN COMPATIBLE WITH THE PGA2310**

APPLICATIONS

- **AUDIO AMPLIFIERS**
- **MIXING CONSOLES**
- **MULTI-TRACK RECORDERS**
- **BROADCAST STUDIO EQUIPMENT**
- **MUSICAL INSTRUMENTS**
- **EFFECTS PROCESSORS**
- **A/V RECEIVERS**
- **CAR AUDIO SYSTEMS**

DESCRIPTION

The PGA2320 is a high-performance, stereo audio volume control designed for professional and high-end consumer audio systems. The ability to operate from ±15V analog power supplies enables the PGA2320 to process input signals with large voltage swings, thereby preserving the dynamic range available in the overall signal path. Using high performance operational amplifier stages internal to the PGA2320 yields low noise and distortion, while providing the capability to drive 600Ω loads directly without buffering. The three-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining of multiple PGA2320 devices.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[(1)]

		PGA2320	UNIT
Supply voltage	V_A+	+15.5	V
	V_A-	−15.5	V
	V_D+	+5.5	V
Analog input voltage		0 to V_A+, V_A-	V
Digital input voltage		−0.3 to V_D+	V
Operating temperature range		−40 to +85	°C
Storage temperature range		−65 to +150	°C
Junction temperature		+150	°C
Lead temperature (soldering, 10s)		+300	°C
Package temperature (IR, reflow, 10s)		+235	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PACKAGE/ORDERING INFORMATION

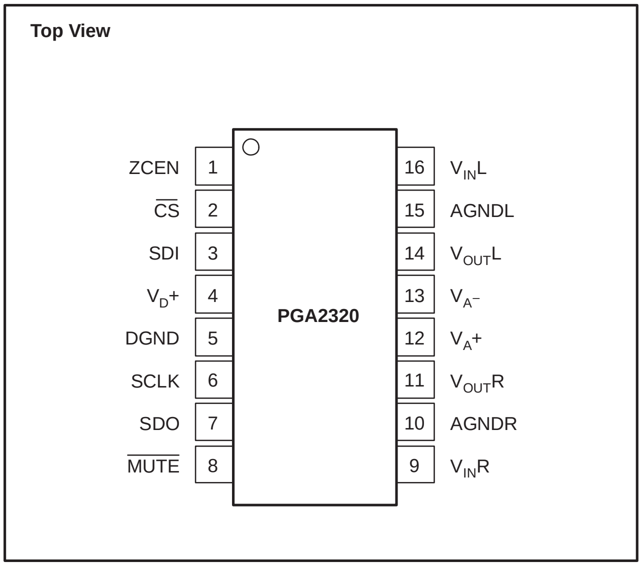
For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_A+ = +15V, V_A− = −15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 20Hz to 20kHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PGA2320 MIN	TYP	MAX	UNIT
DC CHARACTERISTICS					
Step Size			0.5		dB
Gain Error	Gain Setting = 31.5dB		±0.1		dB
Gain Matching			±0.1		dB
Input Resistance			12		kΩ
Input Capacitance			18		pF
AC CHARACTERISTICS					
THD+N	V_{IN} = 10V_{PP}, f = 1kHz		0.0003	0.001	%
Dynamic Range	V_{IN} = AGND, Gain = 0dB	115	120		dB
Voltage Range, Input and Output		(V_A−) + 0.86		(V_A+) − 0.86	V
Output Noise	V_{IN} = AGND, Gain = 0dB		10.5	17.5	μV_{RMS}
Interchannel Crosstalk	f = 1kHz		−126		dBFS
OUTPUT BUFFER					
Offset Voltage	V_{IN} = AGND, Gain = 0dB		1	7.5	mV
Load Capacitance Stability			1000		pF
Short-Circuit Current			75		mA
Unity-Gain Bandwidth, Small Signal			1		MHz
DIGITAL CHARACTERISTICS					
High-Level Input Voltage, V_{IH}		+2.0		V_D+	V
Low-Level Input Voltage, V_{IL}		−0.3		0.8	V
High-Level Output Voltage, V_{OH}	I_O = 200µA	(V_D+) − 1.0			V
Low-Level Output Voltage, V_{OL}	I_O = −2mA			0.4	V
Input Leakage Current			1	10	µA
SWITCHING CHARACTERISTICS					
Serial Clock (SCLK) Frequency	t_{SCLK}	0		6.25	MHz
Serial Clock (SCLK) Pulse Width Low	t_{PH}	80			ns
Serial Clock (SCLK) Pulse Width High	t_{PL}	80			ns
$\overline{\text{MUTE}}$ Pulse Width Low	t_{MI}	2.0			ms
Input Timing					
SDI Setup Time	t_{SDS}	20			ns
SDI Hold Time	t_{SDH}	20			ns
$\overline{\text{CS}}$ Falling to SCLK Rising	t_{CSCR}	90			ns
SCLK Falling to $\overline{\text{CS}}$ Rising	t_{CFCS}	35			ns
Output Timing					
$\overline{\text{CS}}$ Low to SDO Active	t_{CSO}			35	ns
SCLK Falling to SDO Data Valid	t_{CFDO}			60	ns
POWER SUPPLY					
Operating Voltage					
V_A+		+4.5	+15	+15.5	V
V_A−		−4.5	−15	−15.5	V
V_D+		+4.5	+5	+5.5	V
Quiescent Current					
I_A+	V_A+ = +15V		11	16	mA
I_A−	V_A− = −15V		11	16	mA
I_D+	V_D+ = +5V		0.6	1.5	mA

PIN CONFIGURATION

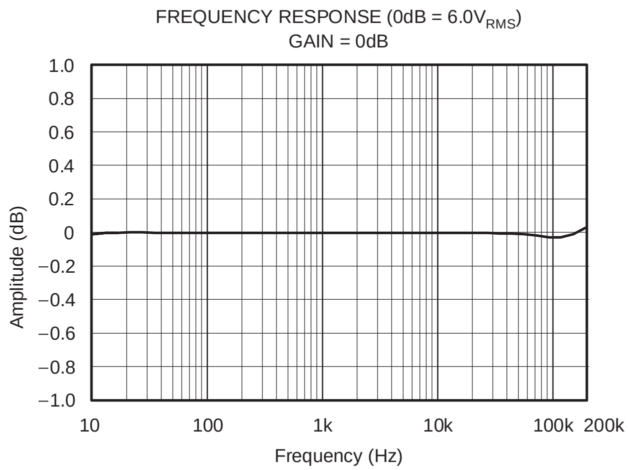


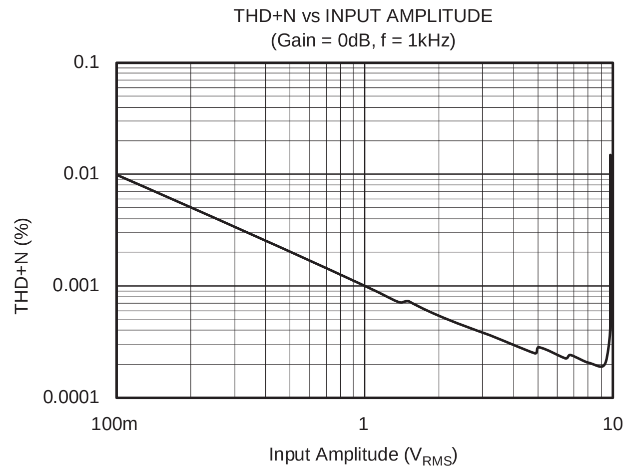
PIN ASSIGNMENTS

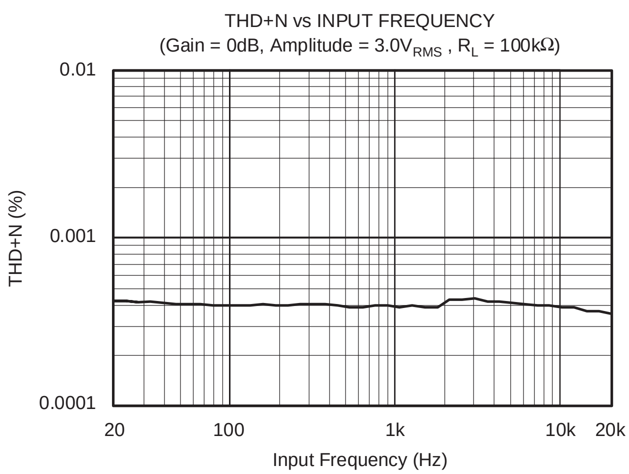
PIN	NAME	FUNCTION
1	ZCEN	Zero Crossing Enable Input (Active High)
2	$\overline{CS}$	Chip-Select Input (Active Low)
3	SDI	Serial Data input
4	V_D+	Digital Power Supply, +5V
5	DGND	Digital Ground
6	SCLK	Serial Clock Input
7	SDO	Serial Data Output
8	$\overline{MUTE}$	Mute Control Input (Active Low)
9	$V_{IN}R$	Analog Input, Right Channel
10	AGNDR	Analog Ground, Right Channel
11	$V_{OUT}R$	Analog Output, Right Channel
12	V_A+	Analog Power Supply, +15V
13	V_A−	Analog Power Supply, −15V
14	$V_{OUT}L$	Analog Output, Left Channel
15	AGNDL	Analog Ground, Left Channel
16	$V_{IN}L$	Analog Input, Left Channel

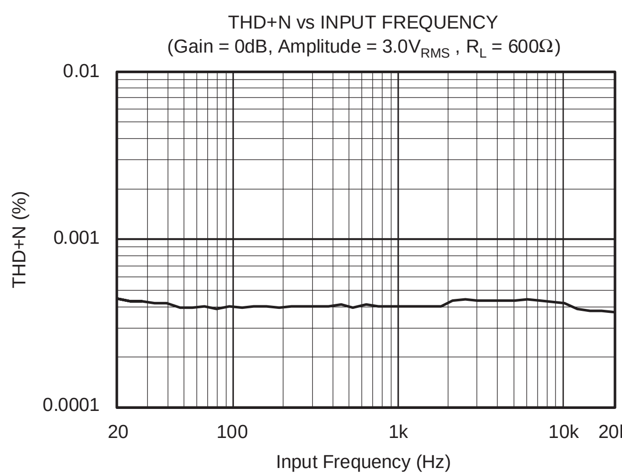
TYPICAL CHARACTERISTICS

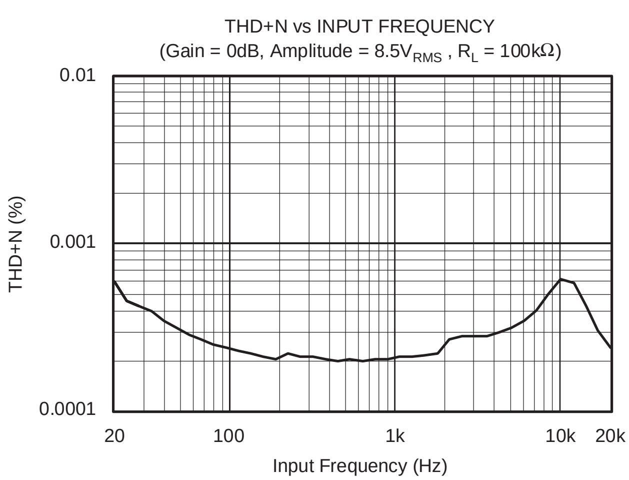
At T_A = +25°C, V_A+ = +15V, V_A− = −15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 20Hz to 20kHz, unless otherwise noted.

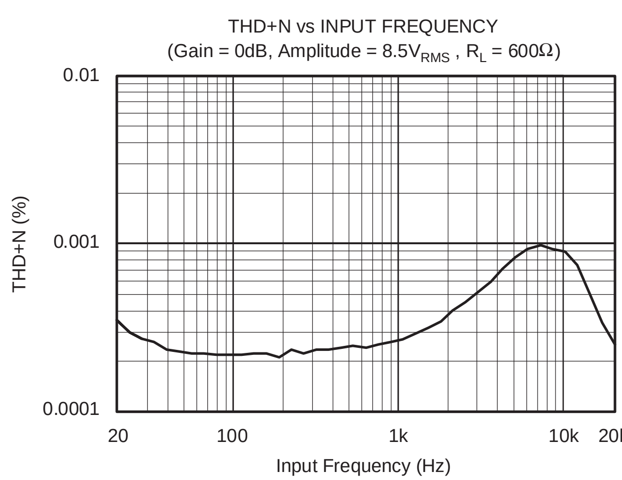






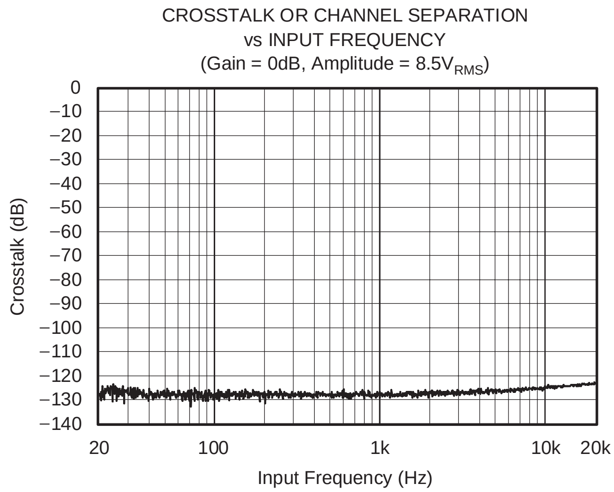






TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_A+ = +15V, V_A− = −15V, V_D+ = +5V, R_L = 100kΩ, C_L = 20pF, BW measure = 20Hz to 20kHz, unless otherwise noted.



GENERAL DESCRIPTION

The PGA2320 is a stereo audio volume control. It may be used in a wide array of professional and consumer audio equipment. The PGA2320 is fabricated in a mixed-signal BiCMOS process in order to take advantage of the superior analog characteristics that the process offers.

The heart of the PGA2320 is a resistor network, an analog switch array, and a high-performance bipolar op amp stage. The switches are used to select taps in the resistor network that, in turn, determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. Figure 1 shows a functional block diagram of the PGA2320.

POWER-UP STATE

On power up, all internal flip-flops are reset. The gain byte value for both the left and right channels are set to 00_{HEX}, or mute condition. The gain will remain at this setting until the host controller programs new settings for each channel via the serial control port.

ANALOG INPUTS AND OUTPUTS

The PGA2320 includes two independent channels, referred to as the left and right channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are named $V_{IN}R$ (pin 9) and $V_{IN}L$ (pin 16), while the outputs are named $V_{OUT}R$ (pin 11) and $V_{OUT}L$ (pin 14).

It is important to drive the PGA2320 with a low source impedance. If a source impedance of greater than 600Ω is used, the distortion performance of the PGA2320 will begin to degrade.

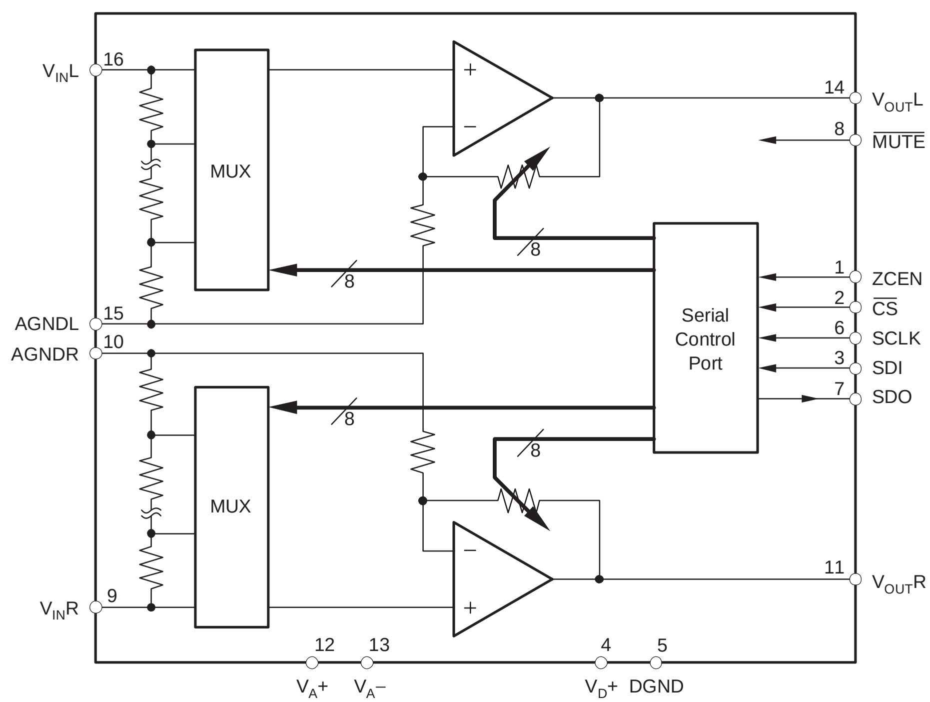


Figure 1. PGA2320 Block Diagram

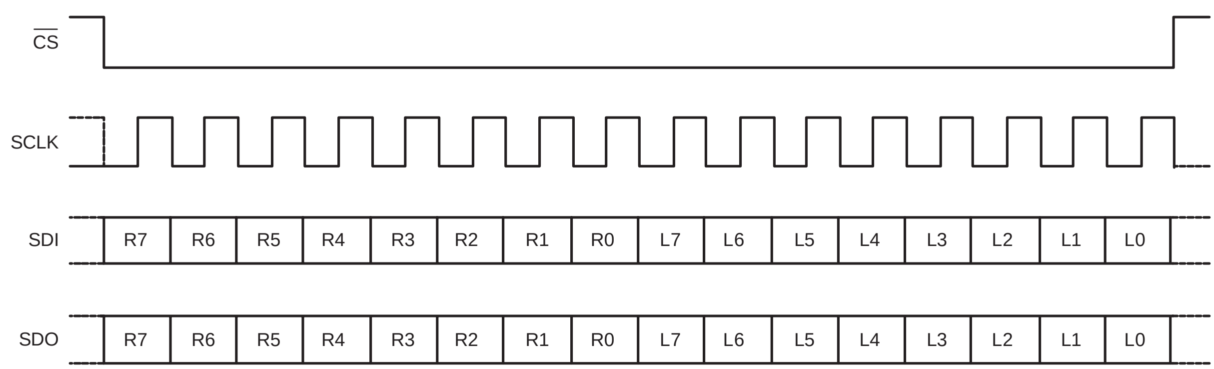
SERIAL CONTROL PORT

The serial control port is utilized to program the gain settings for the PGA2320. The serial control port includes three input pins and one output pin. The inputs include $\overline{CS}$ (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

The $\overline{CS}$ pin functions as the chip select input. Data may be written to the PGA2320 only when $\overline{CS}$ is low. SDI is the serial data input pin. Control data is provided as a 16-bit word at the SDI pin, 8 bits each for the left and right channel gain settings. Data is formatted as MSB first, straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and is used when daisy-chaining multiple PGA2320 devices. Daisy-chain operation is described in detail later in this section. SDO is a tristate output, and assumes a high impedance state when $\overline{CS}$ is high.

The protocol for the serial control port is shown in Figure 2. See Figure 3 for detailed timing specifications of the serial control port.



Gain Byte Format is MSB First, Straight Binary
R0 is the Least Significant Bit of the Right Channel Gain Byte
R7 is the Most Significant Bit of the Right Channel Gain Byte
L0 is the Least Significant Bit of the Left Channel Gain Byte
L7 is the Most Significant Bit of the Left Channel Gain Byte
SDI is latched on the rising edge of SCLK
SDO transitions on the falling edge of SCLK

Figure 2. Serial Interface Protocol

GAIN SETTINGS

The gain for each channel is set by its corresponding 8-bit code, either R[7:0] or L[7:0]; see Figure 2. The gain code data is straight binary format. If we let *N* equal the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

For N = 0:

Mute Condition. The input multiplexer is connected to analog ground (AGNDR or AGNDL).

For N = 1 to 255:

Gain (dB) = 31.5 − [0.5 • (255 − N)]

This results in a gain range of +31.5dB (with N = 255) to −95.5dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and timeout circuitry is discussed later in this data sheet.

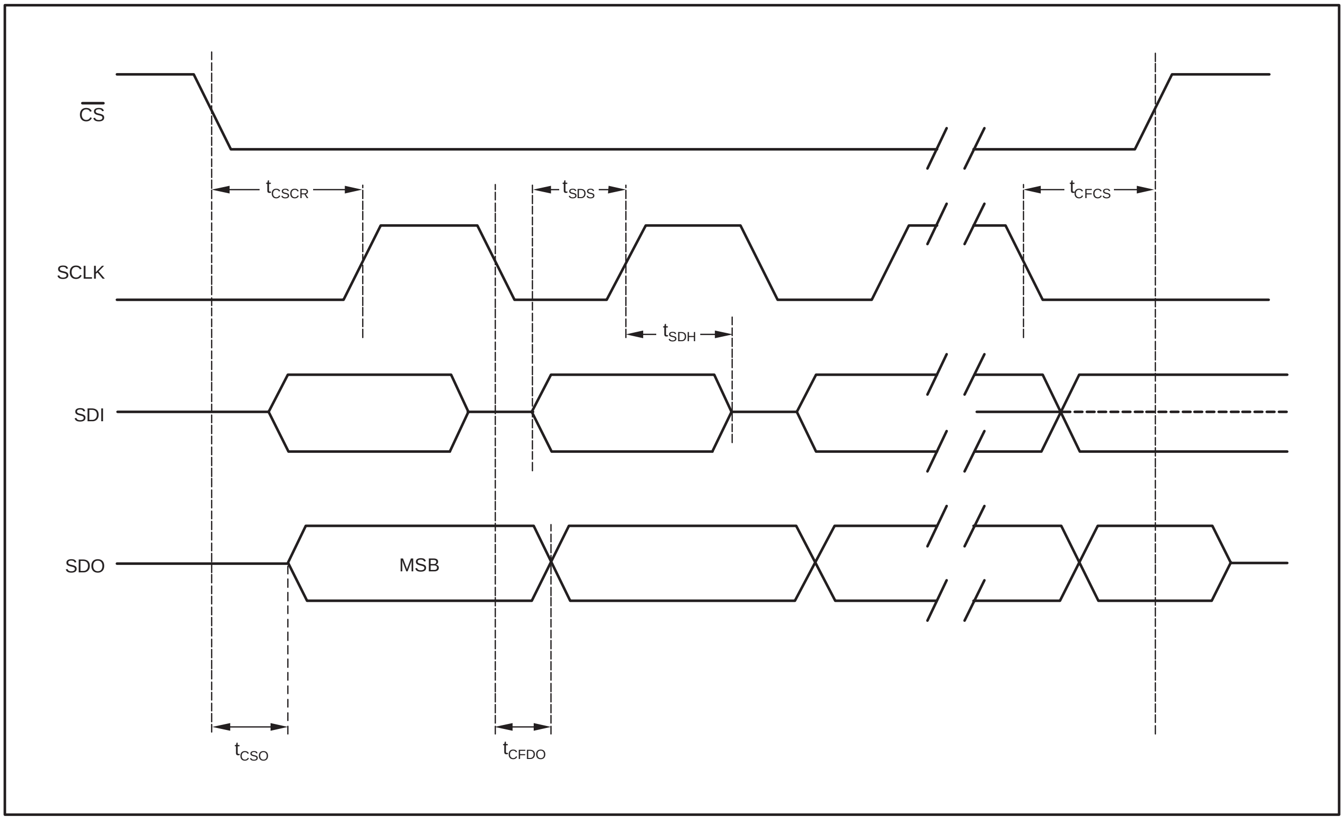


Figure 3. Serial Interface Timing Requirements

DAISY-CHAINING MULTIPLE PGA2320 DEVICES

In order to reduce the number of control signals required to support multiple PGA2320 devices on a printed circuit board, the serial control port supports daisy-chaining of multiple PGA2320 devices. Figure 4 shows the connection requirements for daisy-chain operation. This arrangement allows a three-wire serial interface to control many PGA2320 devices.

As shown in Figure 4, the SDO pin from device #1 is connected to the SDI input of device #2, and is repeated for additional devices. This configuration in turn forms a large shift register, in which gain data may be written for all PGA2320s connected to the serial bus. The length of the shift register is 16 x *N* bits, where *N* is equal to the number of PGA2320 devices included in the chain. The $\overline{CS}$ input must remain low for 16 x *N* SCLK periods, where *N* is the number of devices connected in the chain, in order to allow enough SCLK cycles to load all devices.

ZERO CROSSING DETECTION

The PGA2320 includes a zero crossing detection function that can provide for noise-free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is low, zero crossing detection is disabled. When ZCEN is high, zero crossing detection will be enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting will not be latched until either two zero crossings are detected, or a timeout period of 16ms has elapsed without detecting two zero crossings. In the case of a timeout, the new gain setting takes effect with no attempt to minimize audible artifacts.

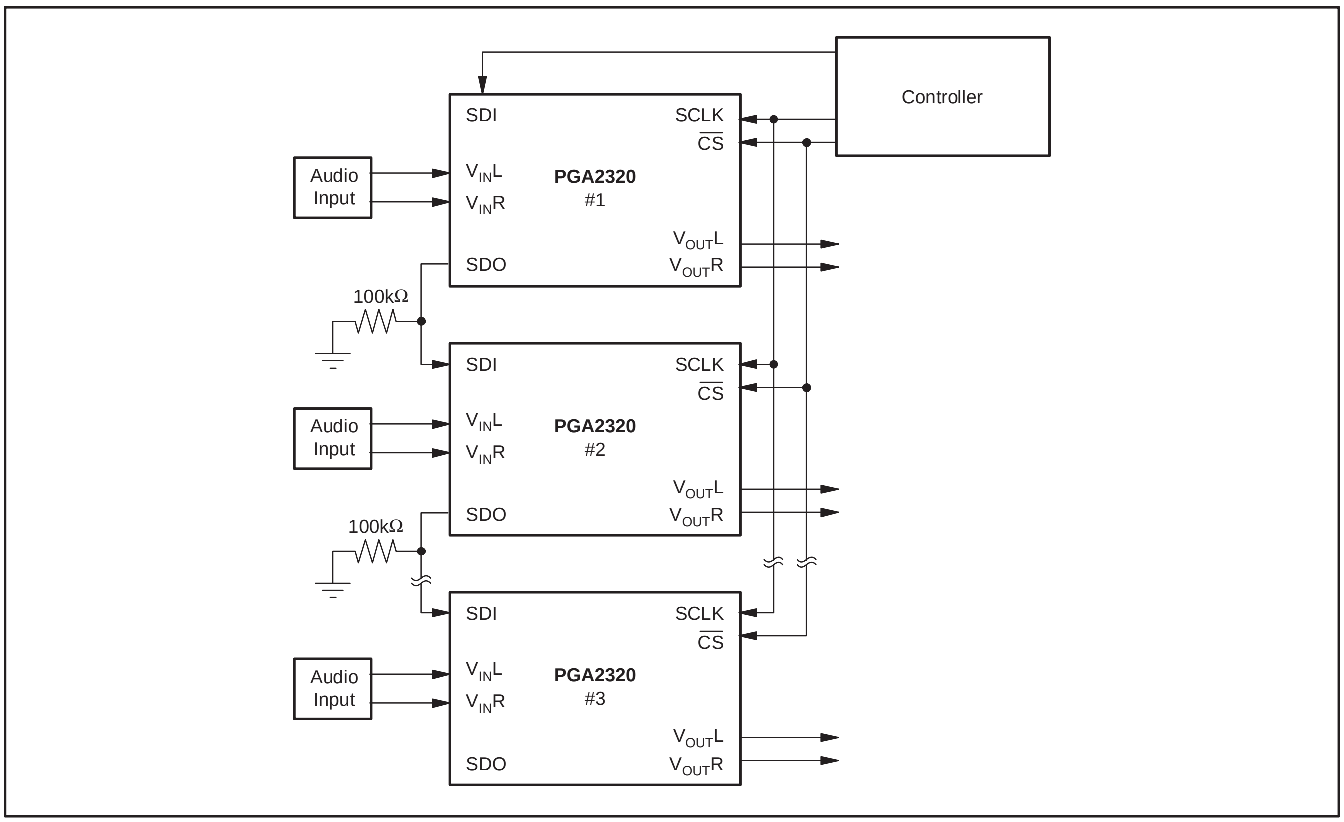


Figure 4. Daisy-Chaining Multiple PGA2320 Devices

MUTE FUNCTION

The PGA2320 includes a mute function. This function may be activated by either the $\overline{\text{MUTE}}$ input (pin 8), or by setting the gain byte value for one or both channels to 00_{HEX}. The $\overline{\text{MUTE}}$ pin may be used to mute both channels, while the gain setting may be used to selectively mute the left and right channels. Muting is accomplished by switching the input multiplexer to analog ground (AGNDR or AGNDL) with zero crossing enabled.

The $\overline{\text{MUTE}}$ pin is active low. When $\overline{\text{MUTE}}$ is low, each channel will be muted following the next zero crossing event or timeout that occurs on that channel. If $\overline{\text{MUTE}}$ becomes active while $\overline{\text{CS}}$ is also active, the mute will take effect once the $\overline{\text{CS}}$ pin goes high. When the $\overline{\text{MUTE}}$ pin is high, the PGA2320 operates normally, with the mute function disabled.

APPLICATIONS INFORMATION

This section includes additional information that is pertinent to designing the PGA2320 into an end application.

RECOMMENDED CONNECTION DIAGRAM

Figure 5 depicts the recommended connections for the PGA2320. Power-supply bypass capacitors should be placed as close to the PGA2320 package as physically possible.

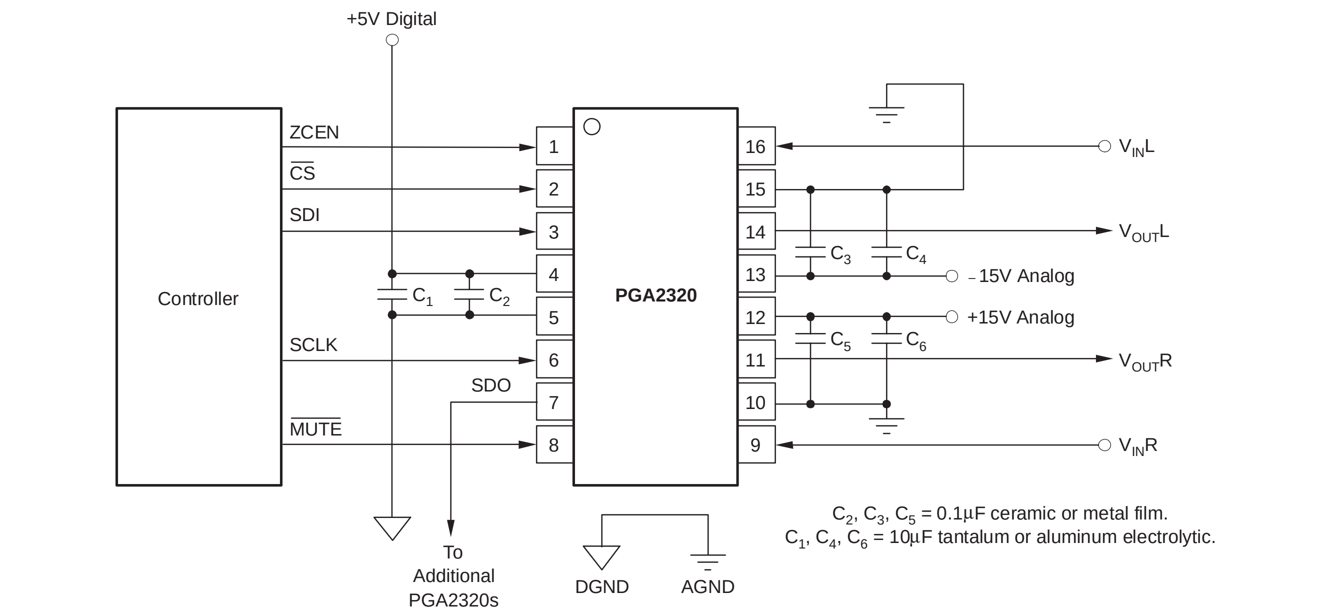


Figure 5. Recommended Connection Diagram

PRINTED CIRCUIT BOARD LAYOUT GUIDELINES

It is recommended that the ground planes for the digital and analog sections of the printed circuit board (PCB) be separate from one another. The planes should be connected at a single point. Figure 6 shows the recommended PCB floor plan for the PGA2320.

The PGA2320 is mounted so that it straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board, while pins 9 through 16 are on the analog side of the board.

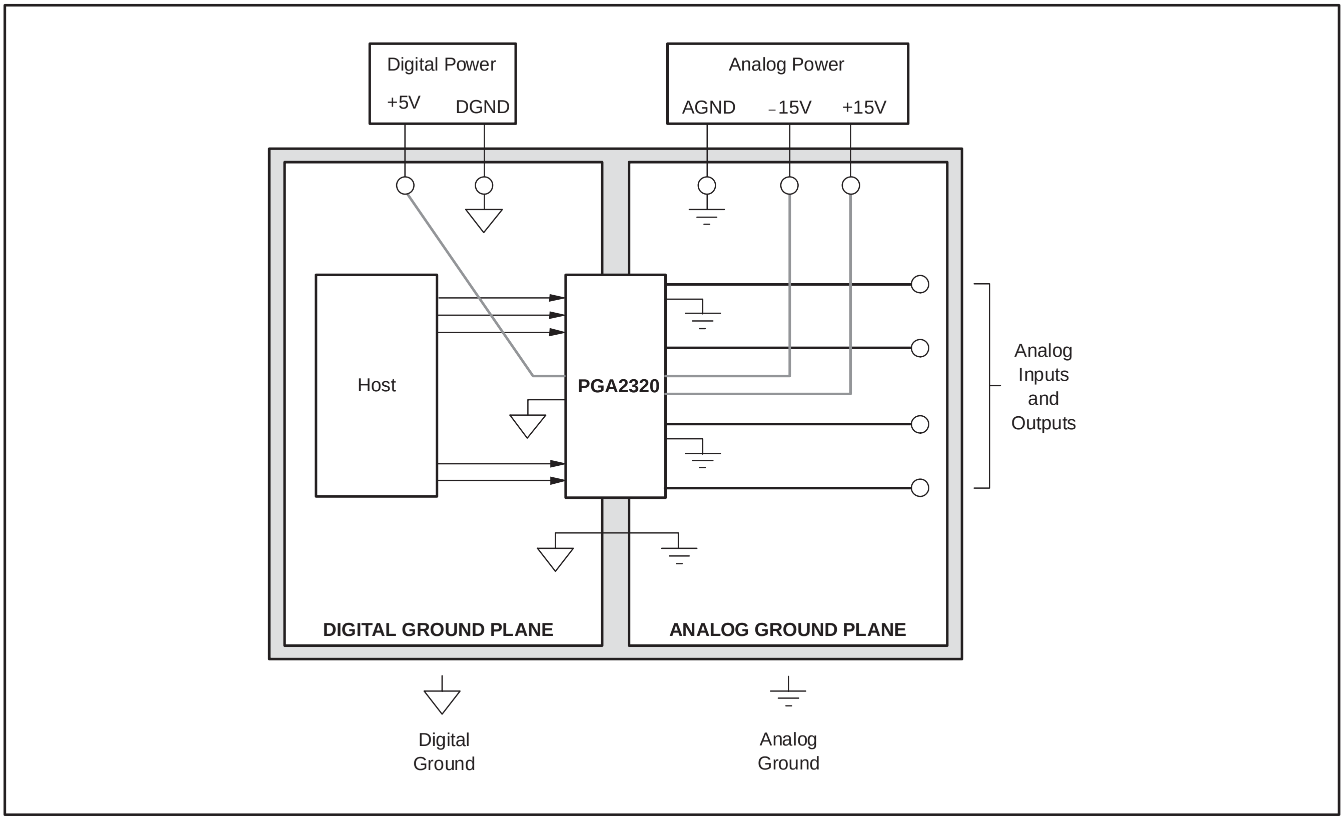


Figure 6. Typical PCB Layout Floor Plan

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PGA2320IDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2320I
PGA2320IDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2320I
PGA2320IDW1G4	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2320I
PGA2320IDW1G4.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2320I
PGA2320IDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2320I
PGA2320IDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2320I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

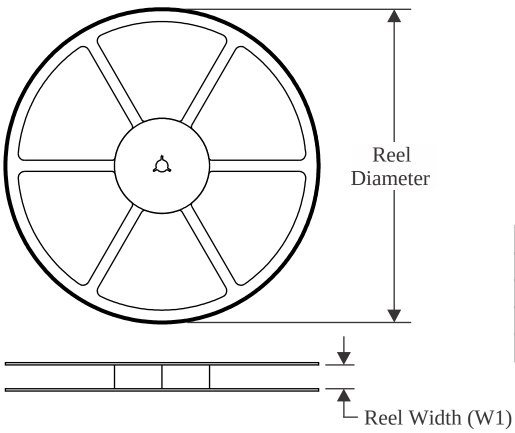
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

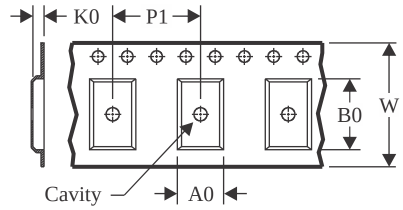
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

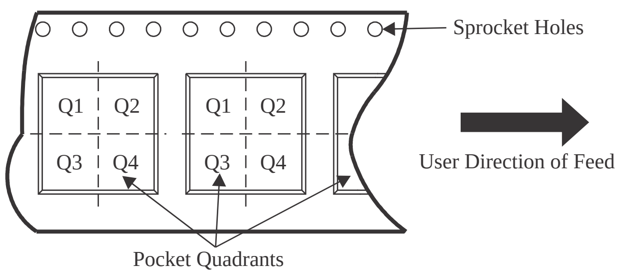


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

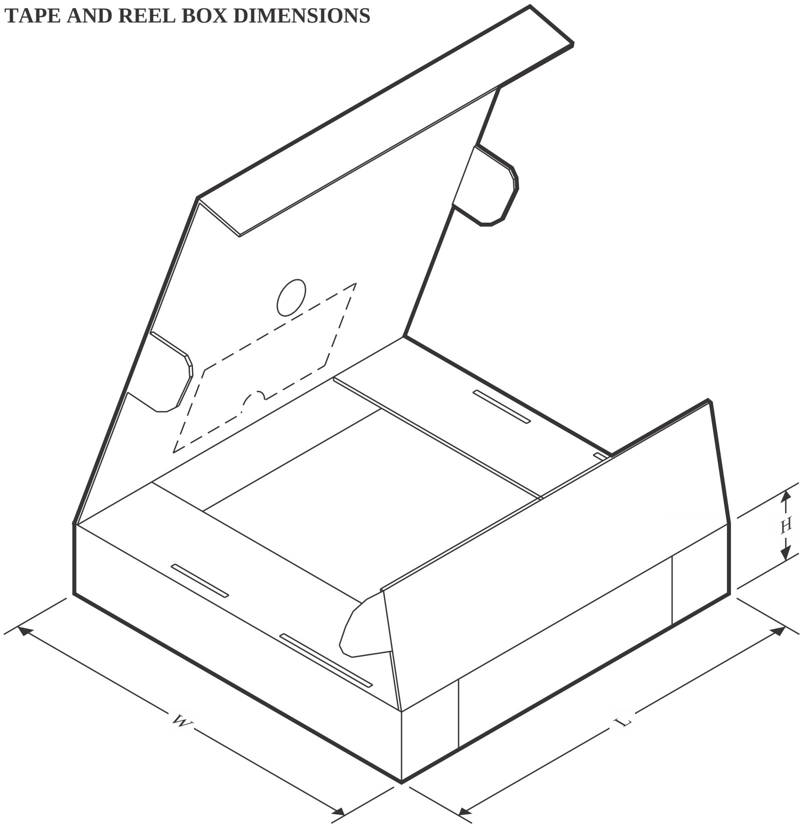
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA2320IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

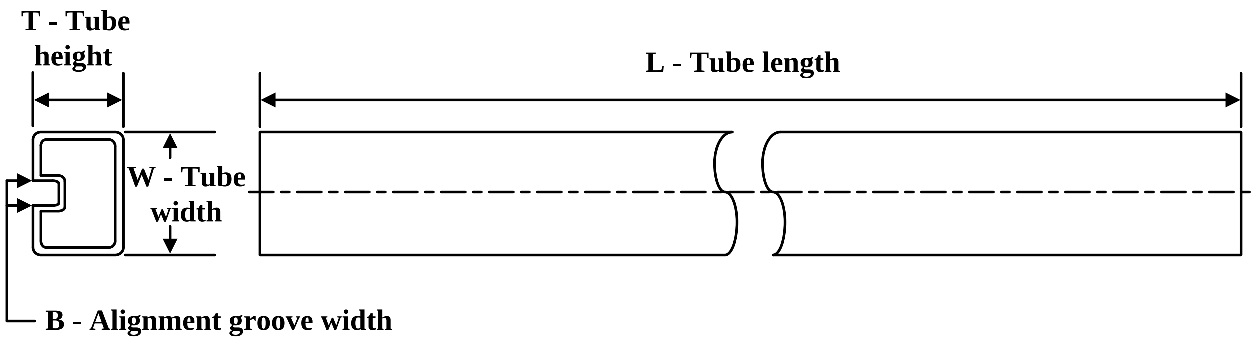
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA2320IDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA2320IDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
PGA2320IDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
PGA2320IDW1G4	DW	SOIC	16	40	506.98	12.7	4826	6.6
PGA2320IDW1G4.A	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

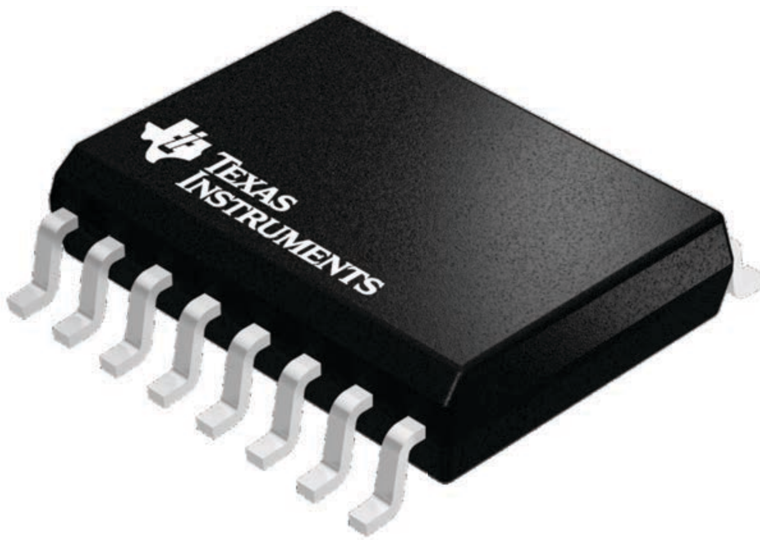
DW 16

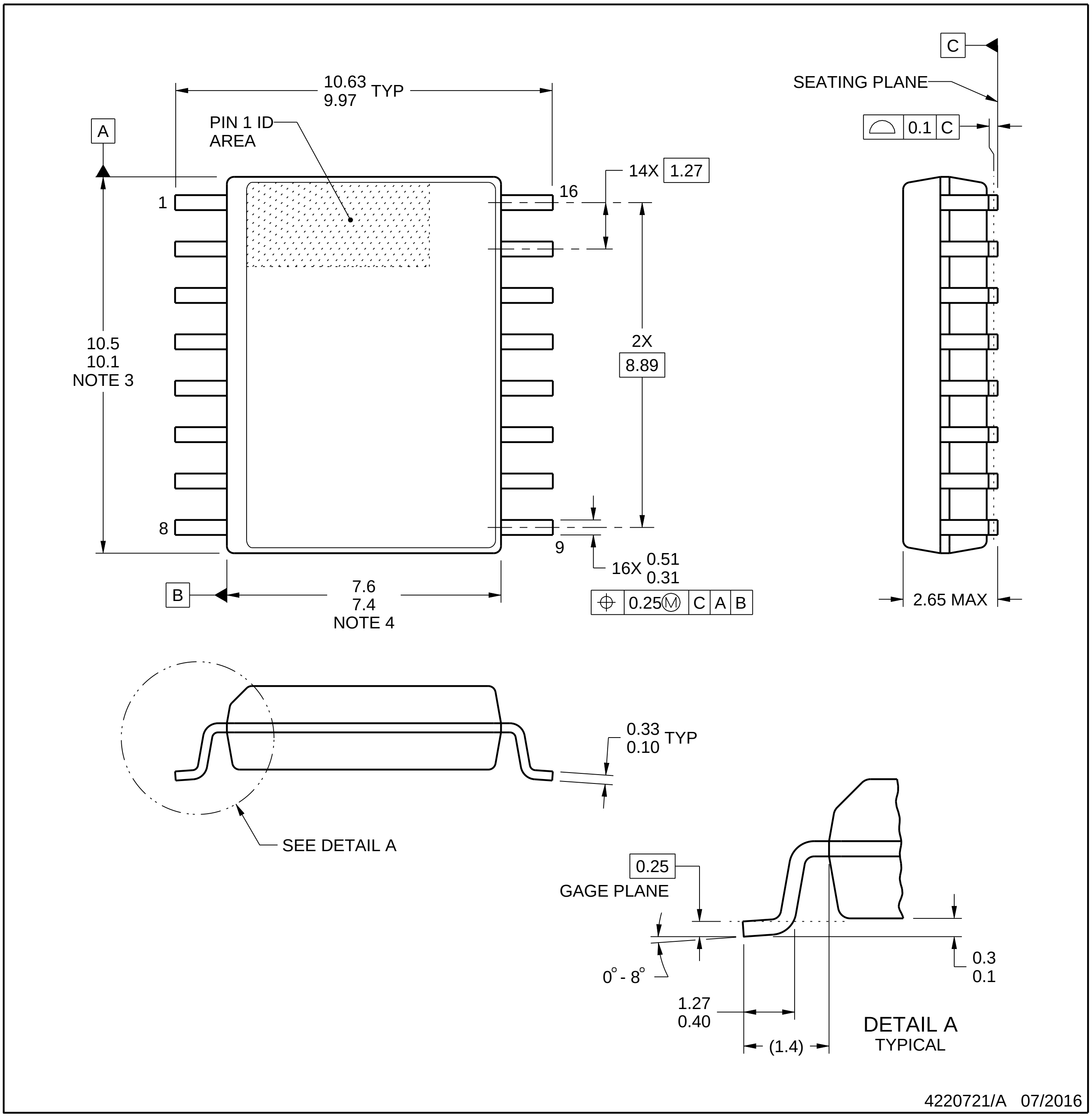
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

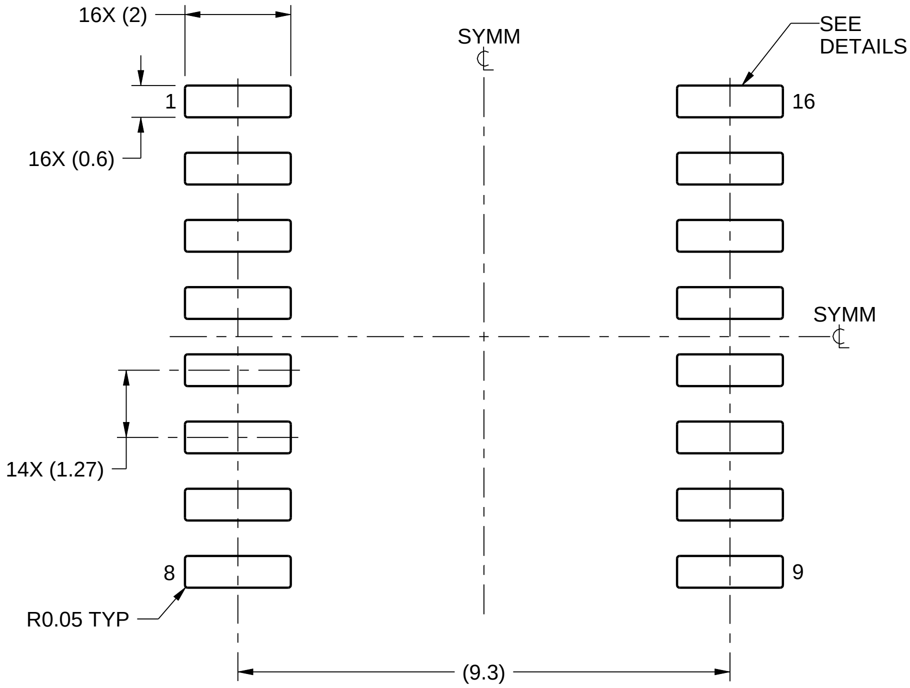
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



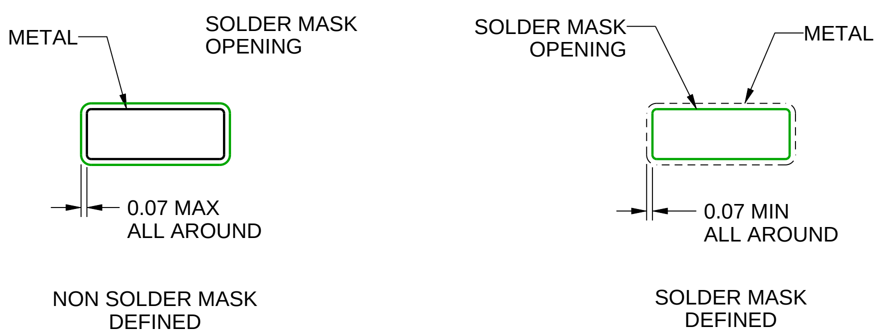


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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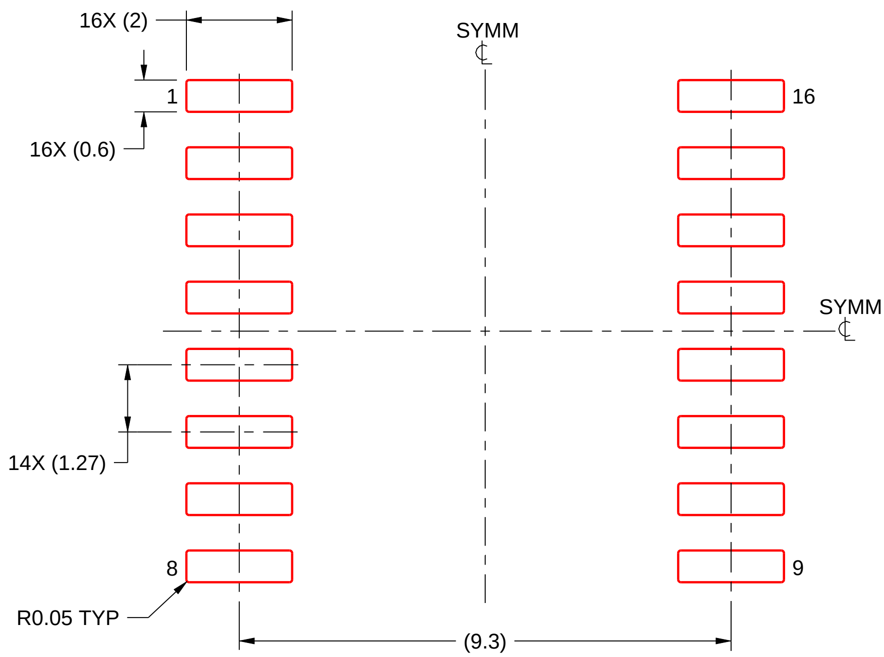
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.