DUAL PERIPHERAL DRIVER

Check for Samples: SN65472-EP

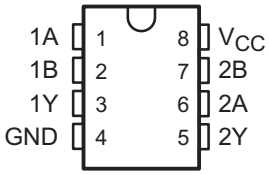
FEATURES

- **Characterized for Use up to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**

SUPPORTS INDUSTRIAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extended (–40°C to 125°C) Temperature Ranges** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

D PACKAGE
(TOP VIEW)



(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION

The SN65472 dual peripheral driver is functionally interchangeable with series SN75452B and series SN75462 peripheral drivers, but is designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than series 75452B (limits are the same as series SN75462). Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN65472 is a dual peripheral NAND driver (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

This device is characterized for operation from -40°C to 125°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

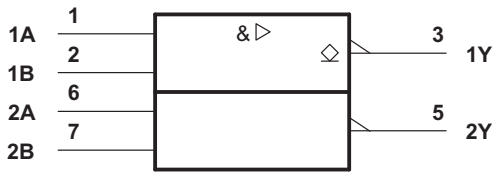
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-40°C to 125°C	SOIC − D	Tape of 75	SN65472DEP	65472	V62/13618-01XE-T
		Reel of 2500	SN65472DREP	65472	V62/13618-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

LOGIC SYMBOL



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)

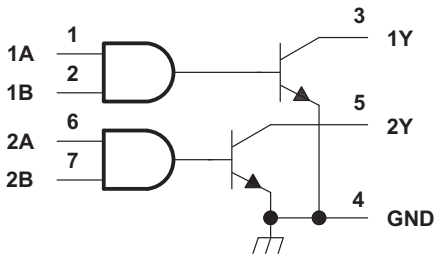
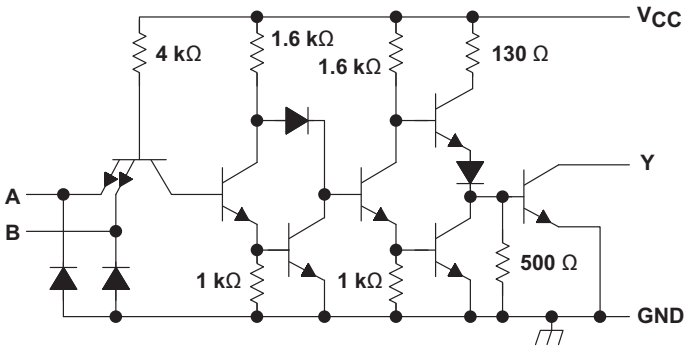


Table 1. FUNCTION TABLE (EACH DRIVER)

INPUTS		Y(1)
A	B	
L	L	H (Off state)
L	H	H (Off state)
H	L	H (Off state)
H	H	L (On state)

(1) positive logic: $Y = \overline{AB}$ or $\overline{A} + \overline{B}$

SCHEMATIC (EACH DRIVER)



Resistor values shown are nominal.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		7	V
V_I	Input voltage		5.5	V
	Inter-emitter voltage(3)		5.5	V
V_O	Off-state output voltage		70	V
I_O	Continuous collector or output current(4)		400	mA
	Peak collector or output current (t_w ≤ 10 ms, duty cycle ≤ 50%)(4)		500	mA
T_J	Absolute maximum junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the network GND, unless otherwise specified.
(3) This is the voltage between two emitters, A and B.
(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

THERMAL INFORMATION

THERMAL METRIC(1)		SN65472-EP	UNITS
		D	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	115.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	59.7	
θ_{JB}	Junction-to-board thermal resistance(4)	56.2	
ψ_{JT}	Junction-to-top characterization parameter(5)	13.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	55.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2.1			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature range	-40		85	°C
T_J	Operating virtual junction temperature	-40		125	°C

ELECTRICAL CHARACTERISTICS

These specifications apply for -40°C ≤ T_J ≤ 125°C (unless otherwise noted)

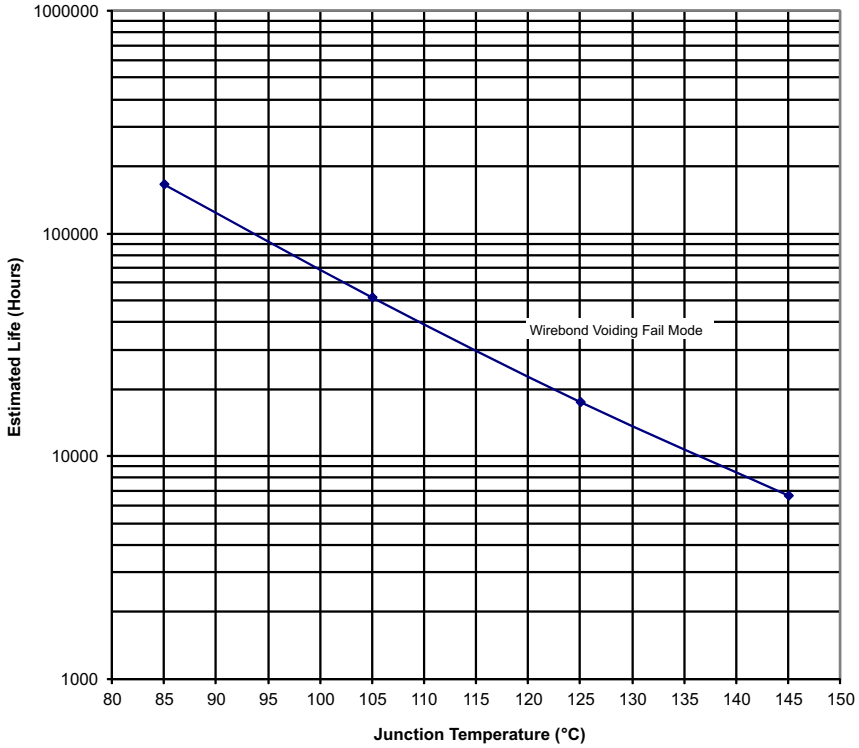
PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = – 12 mA		-1.2	-1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			270	µA
V_{OL}	Low level output voltage	V_{CC} = 4.75 V, V_{IL}= 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL}= 0.8 V, I_{OL} = 300 mA		0.5	0.75	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			44	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		-1	-1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		61	76	mA

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, see Figure 2		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, see Figure 2		30	50	ns
t_{TLH}	Transition time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, see Figure 2		13	25	ns
t_{THL}	Transition time, high-to-low-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, see Figure 2		10	20	ns
V_{OH}	High level output voltage after switching	V_S = 55 V, I_O ≈ 300 mA, see Figure 3	V_S - 18			mV

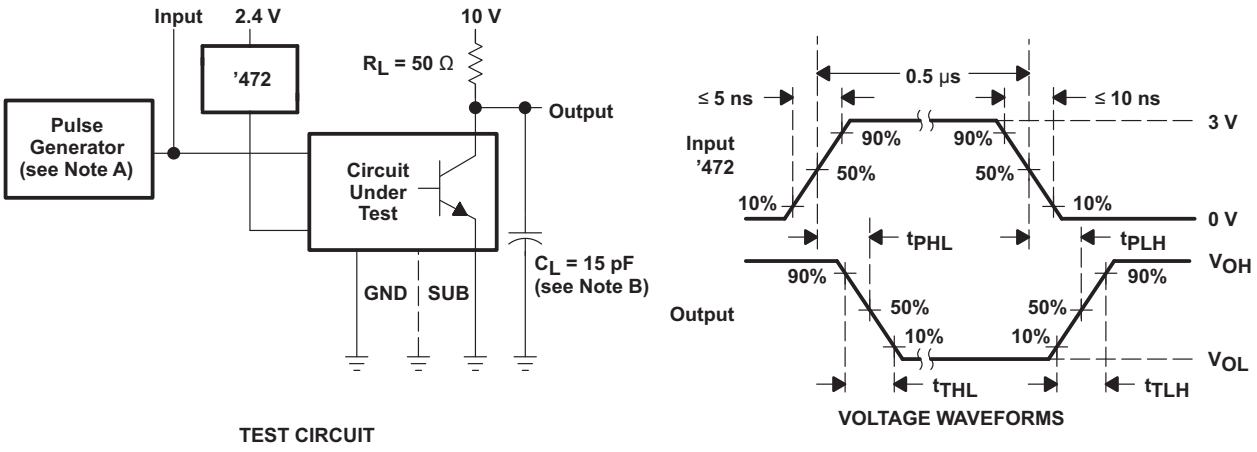


(1) See Datasheet for Absolute Maximum and minimum Recommended Operating Conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

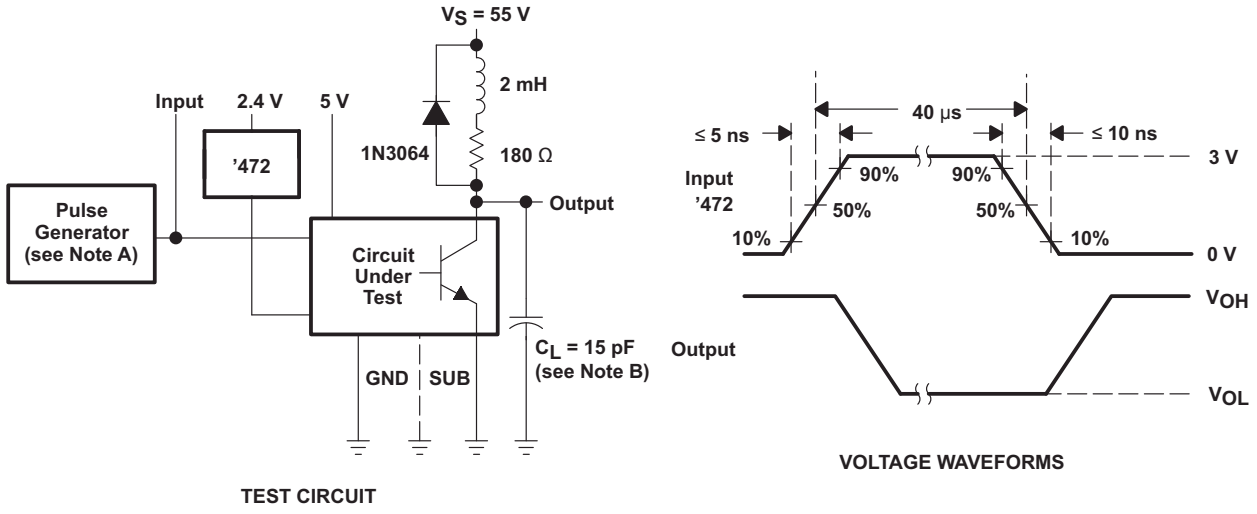
Figure 1. SN65472-EP Wirebond Life Derating Chart

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Switching Times



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Latch-Up Test

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65472DEP	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65472
SN65472DEP.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65472
SN65472DREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65472
SN65472DREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65472
V62/13618-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65472
V62/13618-01XE-T	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65472

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

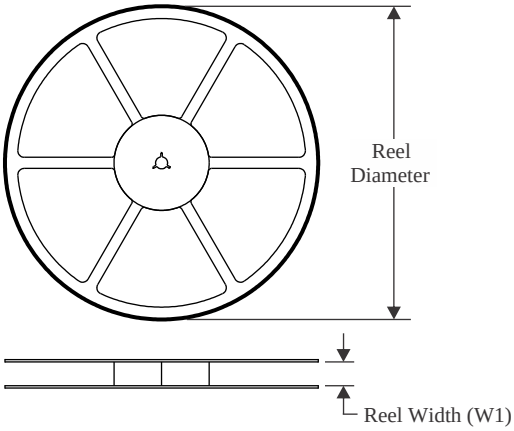
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

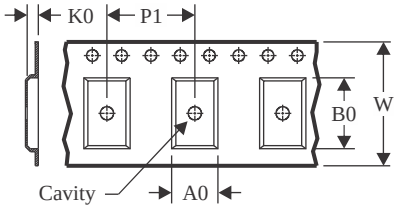
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

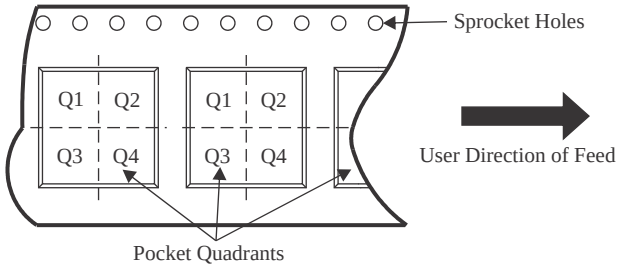


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

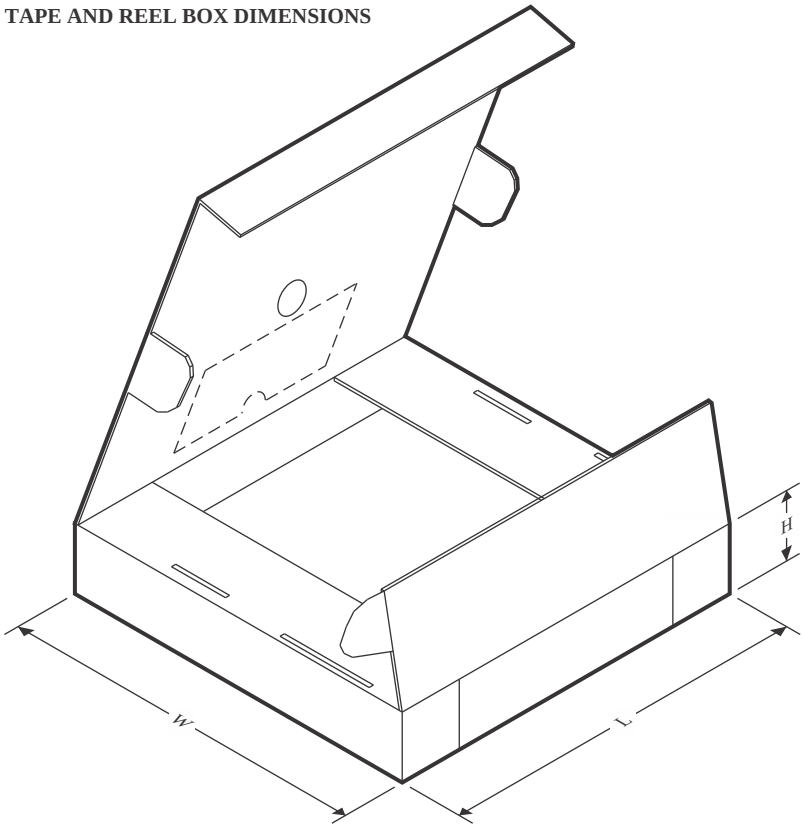
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65472DREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

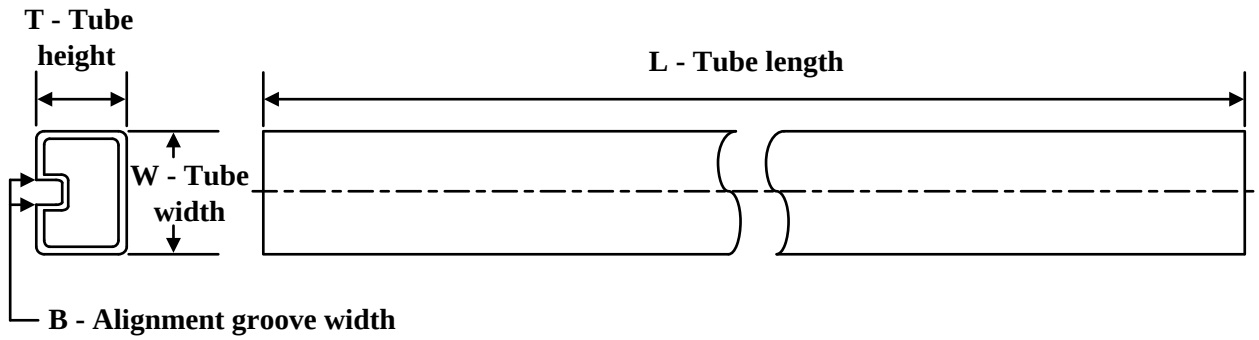
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

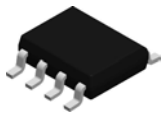
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65472DREP	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65472DEP	D	SOIC	8	75	507	8	3940	4.32
SN65472DEP.A	D	SOIC	8	75	507	8	3940	4.32
V62/13618-01XE-T	D	SOIC	8	75	507	8	3940	4.32

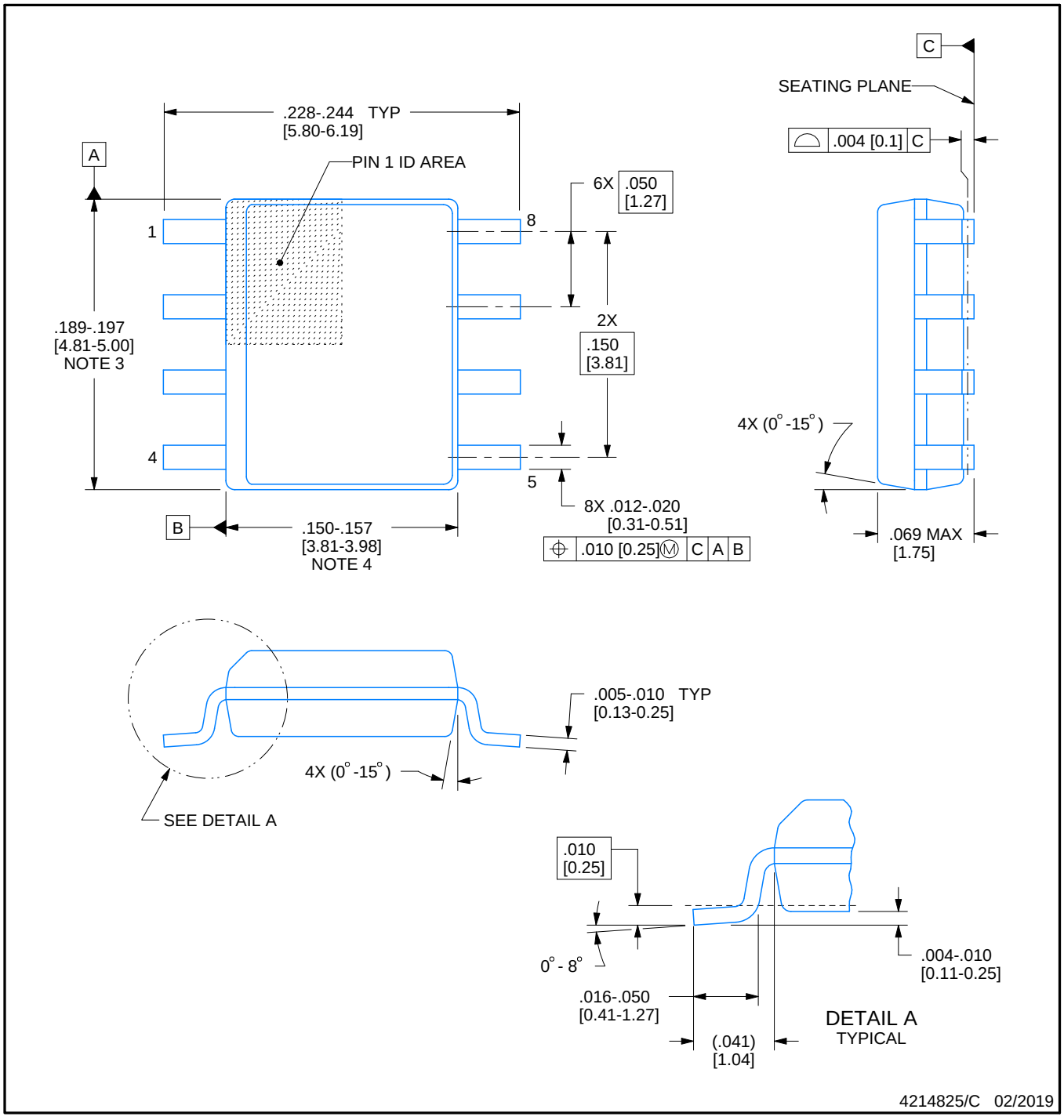


PACKAGE OUTLINE

D0008A

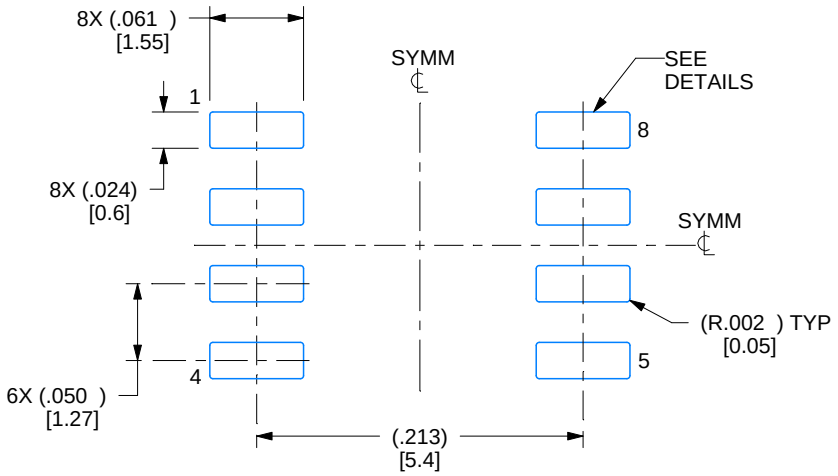
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

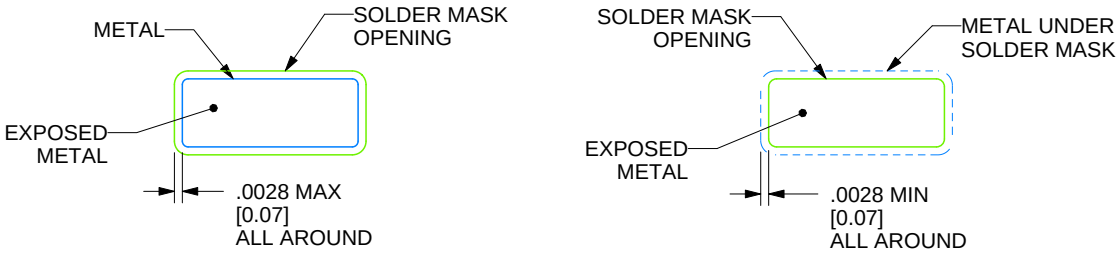


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

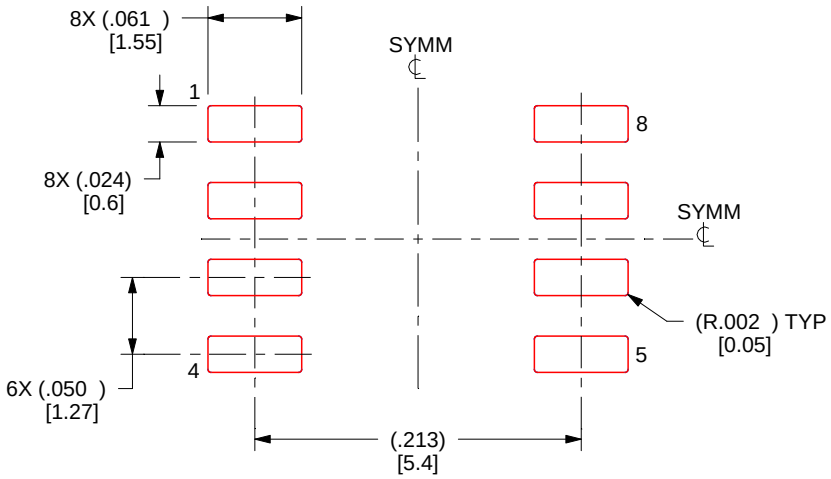
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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