SN74HC253-Q1 Automotive Dual 4-Line To 1-Line Data Selector/Multiplexer With 3-State Outputs

1 Features

- Qualified for automotive applications
- 3-State Version of ’HC153
- Wide operating voltage range of 2V to 6V
- High-current inverting outputs drive up to 15 LSTTL loads
- Low power consumption, 80µA max I_{CC}
- Typical t_{pd} = 9ns
- ±6mA output drive at 5V
- Low input current of 1µA max
- Permit multiplexing from n lines to one line
- Perform parallel-to-serial conversion

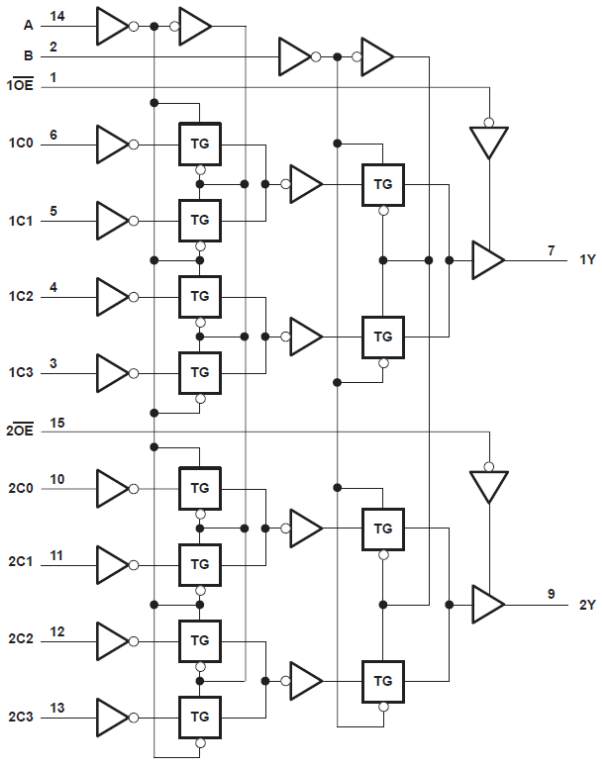
2 Description

The SN74HC253-Q1 devices contain two independent data selectors/multiplexers with full binary decoding to select 1-of-4 data sources and features strobe- controlled ($\overline{OE}$) 3-state outputs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74HC253-Q1	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm

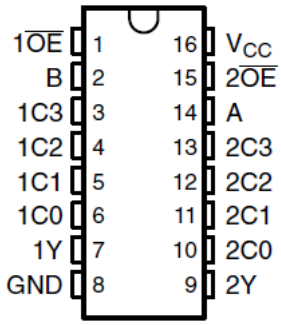
(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

Table of Contents

3 Pin Configuration and Functions



D Package,
16-Pin SOIC
(Top View)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1$\overline{OE}$	1	Input	Channel 1 output enable
B	2	Input	B select
1C3	3	Input	Channel 1 input 3
1C2	4	Input	Channel 1 input 2
1C1	5	Input	Channel 1 input 1
1C0	6	Input	Channel 1 input 0
1Y	7	Output	Channel 1 output
GND	8	Input	Ground
2Y	9	Output	Channel 2 output
2C0	10	Input	Channel 2 input 0
2C1	11	Input	Channel 2 input 1
2C2	12	Input	Channel 2 input 2
2C3	13	Input	Channel 2 input 3
A	14	Input	A select
2$\overline{OE}$	15	Input	Channel 2 output enable
V_{CC}	16	—	Power

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply Voltage		-0.5	7	V
I_{IK}	Input clamp current(2)	(V_I < 0 or V_I > V_{CC})		±20	mA
I_{OK}	Output clamp current(2)	(V_O < 0 or V_O > V_{CC})		±20	mA
I_O	Continuous output current	(V_O = 0 to V_{CC})		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2000	V

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5			V
		V_{CC} = 4.5V	3.15			
		V_{CC} = 6V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2V			0.5	V
		V_{CC} = 4.5V			1.35	
		V_{CC} = 6V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V			1000	ns
		V_{CC} = 4.5V			500	
		V_{CC} = 6V			400	
T_A	Operating free-air temperature		-40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *implications of Slow or Floating CMOS Inputs*,literature number SCBA004

4.4 Thermal Information

THERMAL METRIC		SN74HC253-Q1 D (SOIC) 16 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	73	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = – 20μA	2	1.9	1.998		1.9		V
			4.5	4.4	4.499		4.4		
			6	5.9	5.999		5.9		
		I_{OH} = −6 mA	4.5	3.98	4.3		3.7		
		I_{OH} = −7.8 mA	6	5.48	5.8		5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20μA	2		0.002	0.1		0.1	V
			4.5		0.001	0.1		0.1	
			6		0.001	0.1		0.1	
		I_{OL} = 6mA	4.5		0.17	0.26		0.4	
		I_{OL} = 7.8mA	6		0.15	0.26		0.4	
I_I	V_I = V_{CC} or 0		6		±0.1	±100		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6		±0.01	±0.5		±10	μA
I_{CC}	V_I = V_{CC} or 0	I_O = 0	6			8		160	μA
C_i			2 to 6		3	10		10	pF

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

4.6 Switching Characteristics, C_L = 50pF

over operating free-air temperature range, C_L = 50pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A or B	Any Y	2		62	150		225	ns
			4.5		19	30		45	
			6		16	26		38	
	Data (Any C)	Y	2		54	126		210	
			4.5		16	28		42	
			6		13	23		36	
t_{en}	$\overline{OE}$	Y	2		28	100		150	ns
			4.5		11	20		30	
			6		9	17		26	
t_{dis}	$\overline{OE}$	Y	2		21	135		203	ns
			4.5		14	30		45	
			6		12	35		38	
t_t		Y	2		28	60		90	ns
			4.5		8	12		18	
			6		6	10		15	

4.7 Switching Characteristics, C_L = 150pF

over operating free-air temperature range, C_L = 150pF (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A or B	Any Y	2		76	235		355	ns
			4.5		23	47		71	
			6		20	41		60	
	Data (Any C)	Y	2		68	220		335	
			4.5		20	44		67	
			6		17	38		57	
t_{en}	$\overline{OE}$	Y	2		44	185		280	ns
			4.5		16	37		56	
			6		14	32		48	
t_t		Y	2		45	210		315	ns
			4.5		17	42		63	
			6		13	36		53	

4.8 Operating Characteristics

T_A = 25°C

		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per multiplexer	No load	45	pF

5 Parameter Measurement Information

Load Circuit and Voltage Waveforms

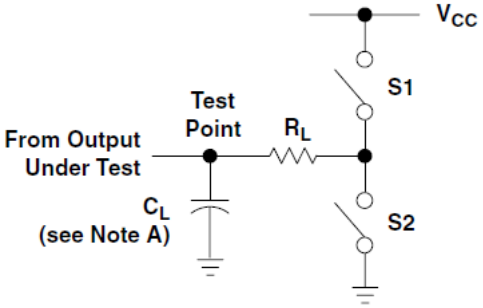


Figure 5-1. Load Circuit

PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		--	50 pF or 150 pF	Open	Open

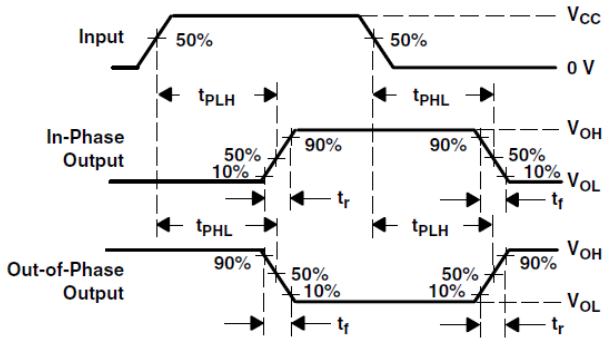


Figure 5-2. Voltage Waveforms
Propagation Delay And Output Transition Times

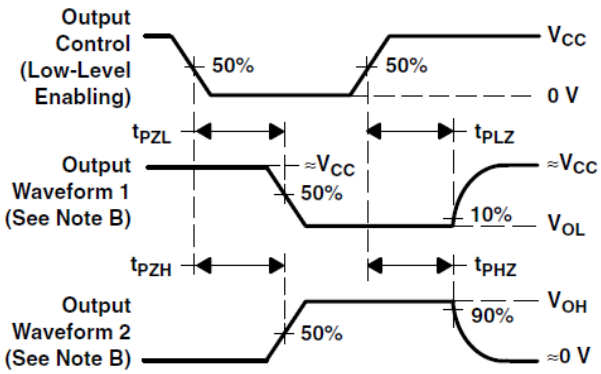


Figure 5-3. Voltage Waveforms
Enable and Disable Times For 3-State Outputs

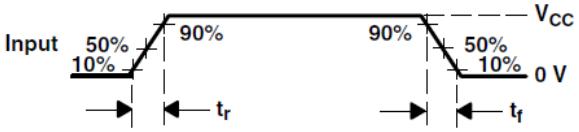


Figure 5-4. Voltage Waveform Input Rise and Fall Times

A. C_L includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having he following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6ns, t_f = 6ns

D. The outputs are measured one at a time with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

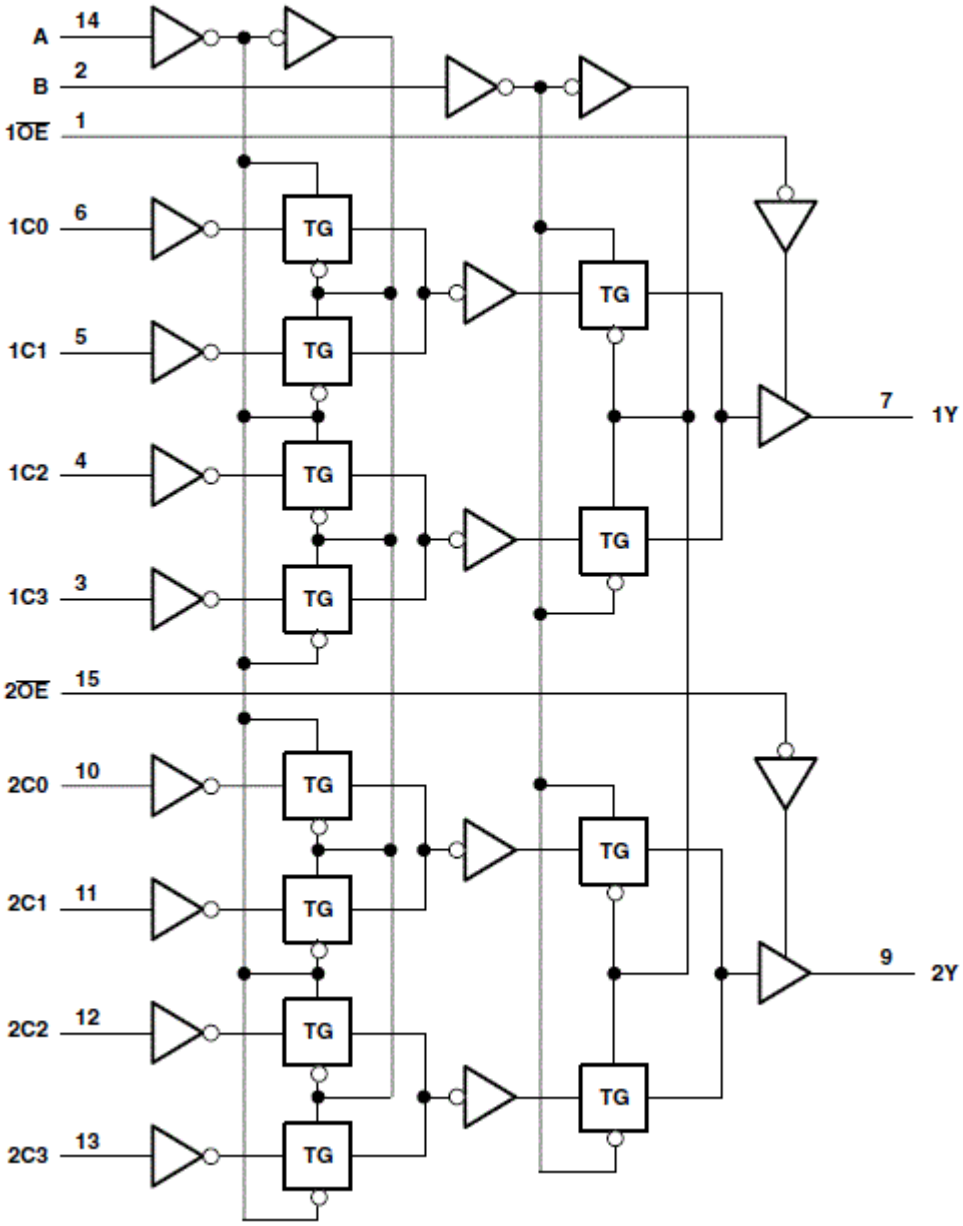
6 Detailed Description

6.1 Overview

Each data selector/multiplexer contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable ($\overline{OE}$) input. The outputs are disabled when their respective $\overline{OE}$ is high.

6.2 Functional Block Diagram



6.3 Device Functional Modes

Table 6-1. Function Table

INPUTS							OUTPUT Y
SELECT(1)		DATA				$\overline{OE}$	
B	A	C0	C1	C2	C3		
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

(1) Select inputs A and B are common to both sections.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

7.2.2 Layout Example

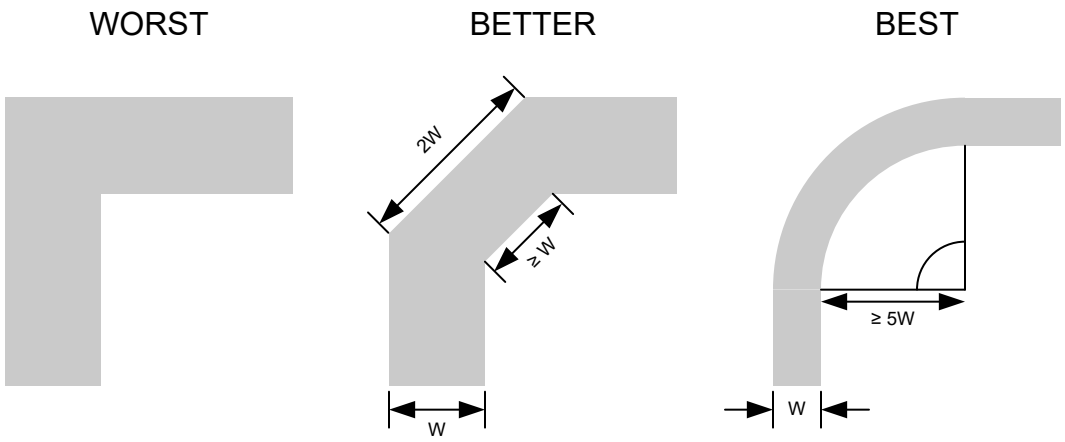


Figure 7-1. Example Trace Corners for Improved Signal Integrity

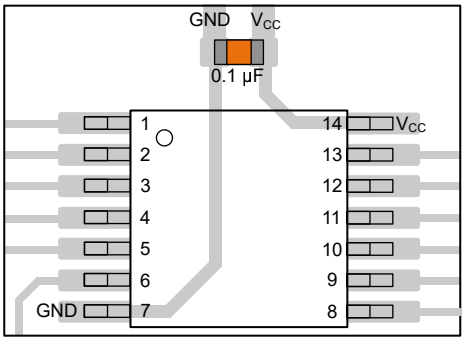


Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages

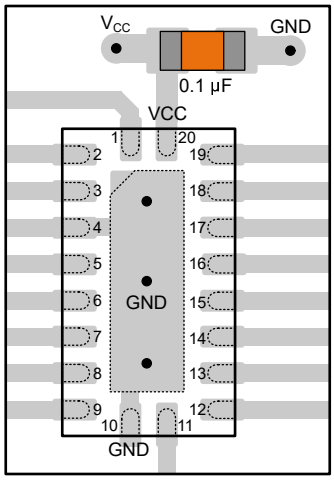


Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages

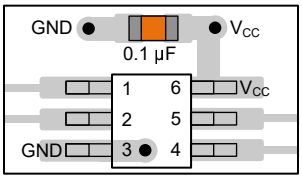


Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

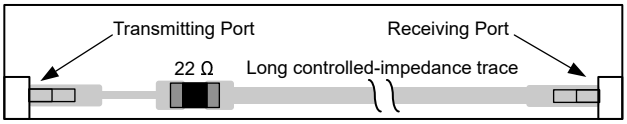


Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2008) to Revision B (January 2025)	Page
• Updated the numbering, formatting, tables, figures and cross-references throughout the document to reflect modern data sheet standards	1
• Added *Package Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted references to machine model throughout data sheet	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC253QDRG4Q1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC253QQ1
SN74HC253QDRG4Q1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC253QQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74HC253-Q1 :

- Catalog : SN74HC253

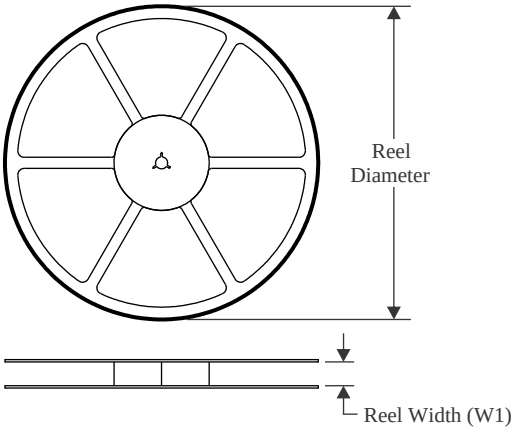
- Enhanced Product : SN74HC253-EP
- Military : SN54HC253

NOTE: Qualified Version Definitions:

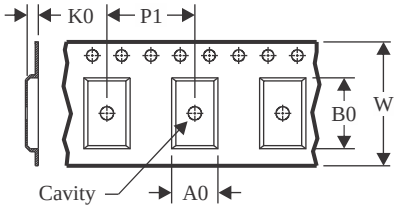
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

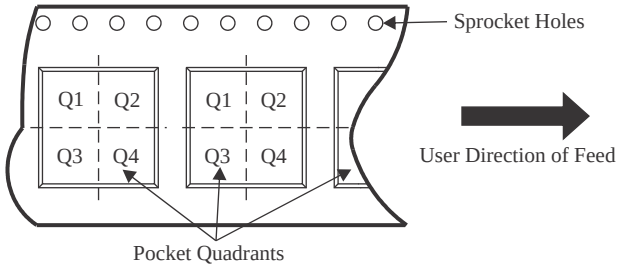


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

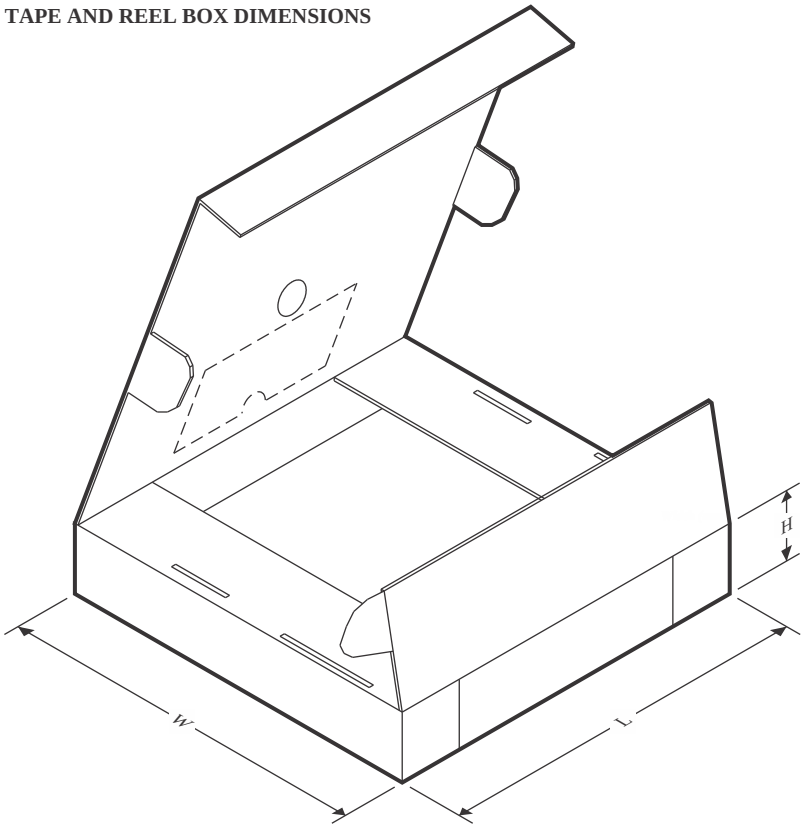
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC253QDRG4Q1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

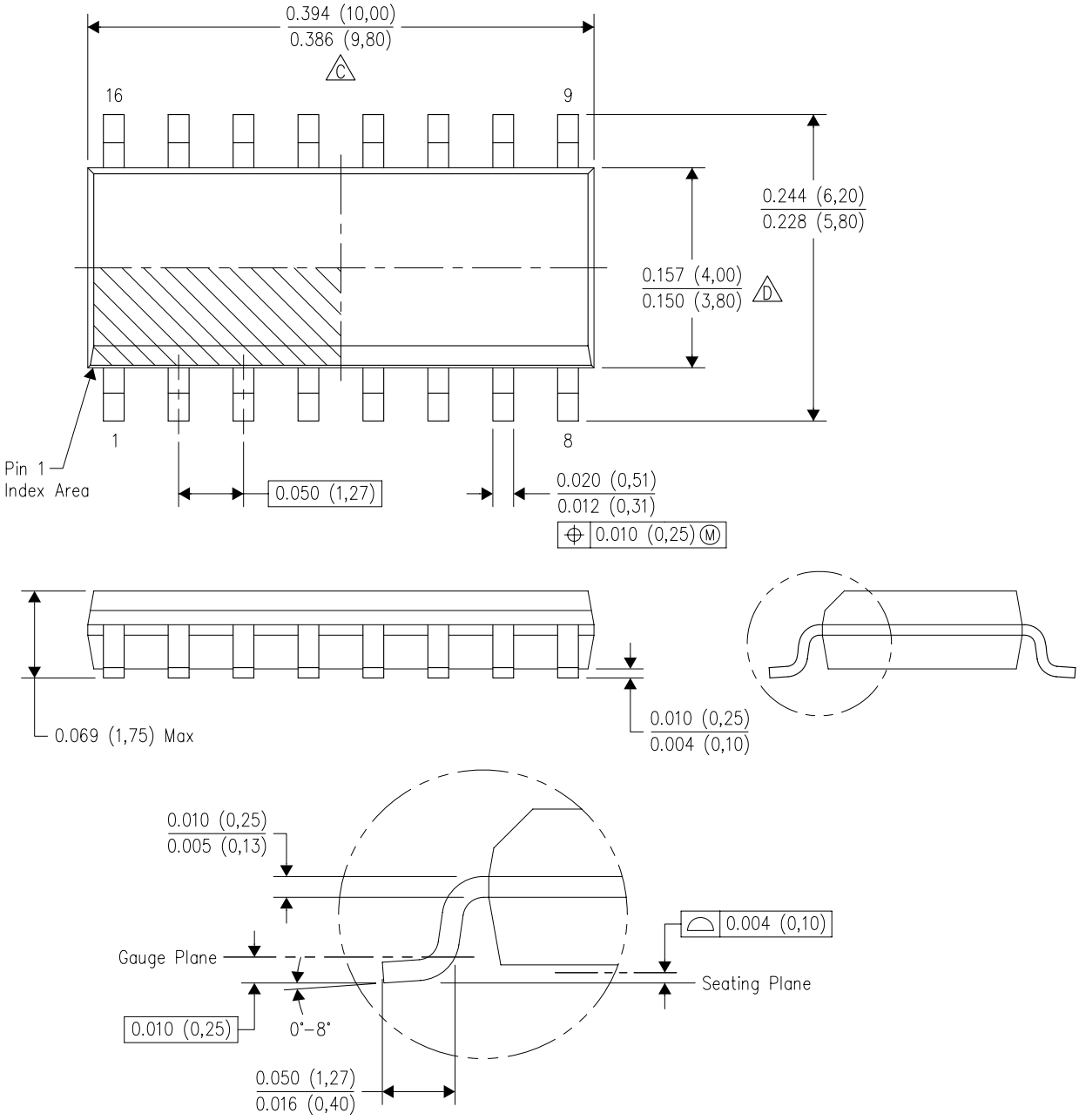
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC253QDRG4Q1	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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Last updated 10/2025