

## SN74LVC2GU04Q1 Dual Unbuffered Inverter

### 1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
- Supports 5V  $V_{CC}$  operation
- Inputs accept voltages to 5.5V
- Max  $t_{pd}$  of 3.7ns at 3.3V
- Low power consumption, 10 $\mu\text{A}$  max  $I_{CC}$
- $\pm 24\text{mA}$  Output drive at 3.3V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2\text{V}$  at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
- Can be used as a down translator to translate inputs from a max of 5.5V down to the  $V_{CC}$  level
- Unbuffered outputs

### 2 Applications

- [AV receivers](#)
- [Desktop or notebook PCs](#)
- Blu-ray players and home theaters
- DVD recorders and players
- Digital radio or internet radio players
- Digital video cameras (DVC)
- Embedded PCs
- GPS: Personal navigation devices
- Mobile internet devices
- Network projector front-ends
- Portable media players
- Pro audio mixers

- Smoke detectors
- Solid-state drive (SSD): enterprise
- High-definition (HDTV)
- Tablets: enterprise
- Audio docks: portable
- DLP front projection systems
- DVR and DVS
- Digital picture frame (DPF)
- Digital still cameras

### 3 Description

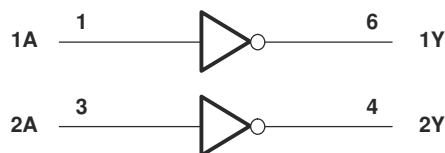
This dual inverter is designed for 1.65V to 5.5V  $V_{CC}$  operation.

The SN74LVC2GU04-Q1 device contains two inverters with unbuffered outputs and performs the Boolean function  $Y = \bar{A}$ .

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE (NOM) <sup>(3)</sup>
SN74LVC2GU04-Q1	DRY (SON, 6)	1.45mm × 1.00mm	1.45mm × 1.00mm
	DCK (SC-70, 6)	2.00mm × 2.10mm	2.00mm × 1.25mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



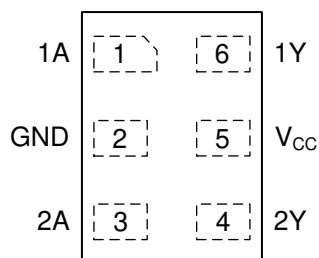
**Logic Diagram (Positive Logic)**



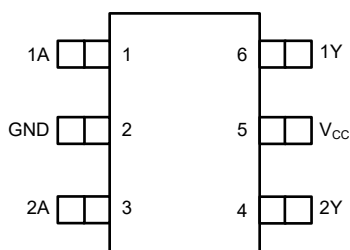
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## 4 Pin Configuration and Functions



**Figure 4-1. DRY Package 6-Pin SON Top View**



**Figure 4-2. DCK Package 6-Pin SC70 Top View**

**Table 4-1. Pin Functions**

PIN			I/O	DESCRIPTION
NAME	DRY (SON) <sup>(1)</sup>	DCK (SC70)		
1A	1	1	I	Input
1Y	6	6	O	Output
2A	3	3	I	Input
2Y	4	4	O	Output
V <sub>CC</sub>	5	5	—	Positive Supply
GND	2	2	—	Ground

(1) See Package drawing at the end of the data sheet for dimensions

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		–0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>		–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
T <sub>A</sub>	Operating free-air temperature		–40	125	°C
T <sub>J</sub>	Operating junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 5.2 ESD Ratings

			MAX	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD Classification Level	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

(1)			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	I <sub>O</sub> = –100µA	0.75 × V <sub>CC</sub>		V
V <sub>IL</sub>	Low-level input voltage	I <sub>O</sub> = 100µA		0.25 × V <sub>CC</sub>	V
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65V		–4	mA
		V <sub>CC</sub> = 2.3V		–8	
		V <sub>CC</sub> = 3V		–16	
				–24	
		V <sub>CC</sub> = 4.5V		–32	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65V		4	mA
		V <sub>CC</sub> = 2.3V		8	
		V <sub>CC</sub> = 3V		16	
				24	
		V <sub>CC</sub> = 4.5V		32	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DCK	DRY	UNIT
		(6 PINS)	(6 PINS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	187.7	233.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	115.2	144.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	48.4	119.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	30.9	15.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	48.2	119.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application note](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	–40°C to 85°C			–40°C to 125°C			UNIT
				MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>		V <sub>IL</sub> = 0V	I <sub>OH</sub> = –100μA	1.65V to 5.5V	V <sub>CC</sub> – 0.1		V <sub>CC</sub> – 0.1			V
			I <sub>OH</sub> = –4mA	1.65 V	1.2		1.2			
			I <sub>OH</sub> = –8mA	2.3 V	1.9		1.9			
			I <sub>OH</sub> = –16mA	3V	2.4		2.4			
			I <sub>OH</sub> = –24mA		2.3		2.3			
			I <sub>OH</sub> = –32mA	4.5 V	3.8		3.8			
V <sub>OL</sub>		V <sub>IH</sub> = V <sub>CC</sub>	I <sub>OL</sub> = 100μA	1.65V to 5.5V		0.1			0.1	V
			I <sub>OL</sub> = 4mA	1.65 V		0.45			0.45	
			I <sub>OL</sub> = 8mA	2.3 V		0.3			0.3	
			I <sub>OL</sub> = 16mA	3V		0.4			0.4	
			I <sub>OL</sub> = 24mA			0.55			0.55	
			I <sub>OL</sub> = 32mA	4.5 V		0.55			0.55	
I <sub>I</sub>	A inputs	V <sub>I</sub> = 5.5V or GND	0 to 5.5 V			±5			±5	μA
I <sub>CC</sub>		V <sub>I</sub> = 5.5V or GND, I <sub>O</sub> = 0	1.65V to 5.5V			10			10	μA
C <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		7					pF

(1) All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

## 5.6 Switching Characteristics – -40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 85°C								UNIT
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1.2	5.5	1	4	1.1	3.7	1	3	ns

## 5.7 Switching Characteristics – -40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C to 125°C								UNIT
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 5V ± 0.5V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1.2	6.3	1	4.5	1.1	4.2	1	3.5	ns

## 5.8 Operating Characteristics

$T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8V$	$V_{CC} = 2.5V$	$V_{CC} = 3.3V$	$V_{CC} = 5V$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	$f = 10MHz$	7	7	8	23	pF

## 5.9 Typical Characteristic

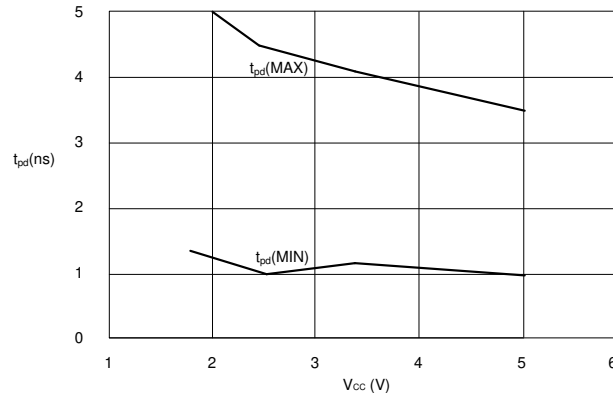
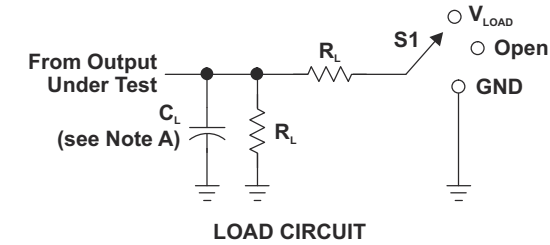


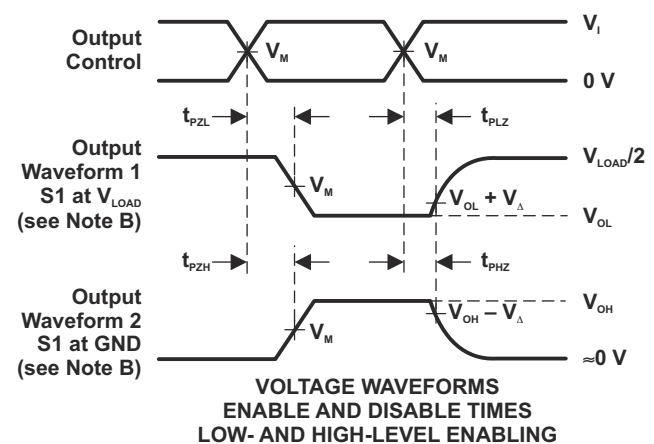
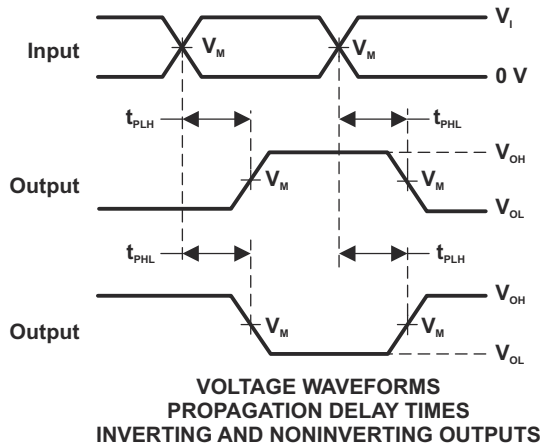
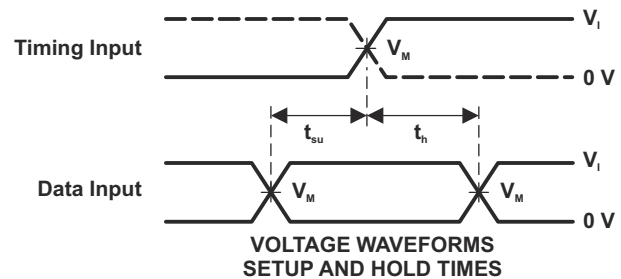
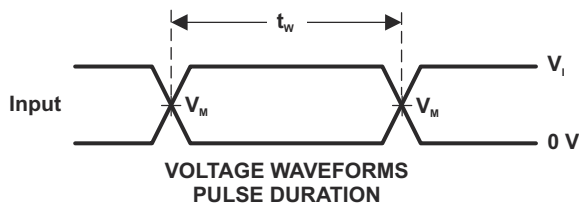
Figure 5-1.  $t_{pd}$  vs  $V_{CC}$

## 6 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{on}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

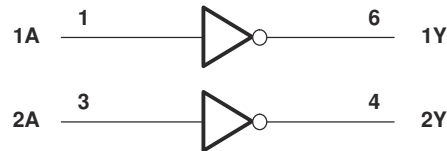
Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74LVC2GU04Q1 device contains two inverters with unbuffered outputs with a maximum sink current of 32mA.

### 7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

### 7.3 Feature Description

#### 7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high-drive capability of this device creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to overcurrent. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

#### 7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst-case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using Ohm's law ( $R = V \div I$ ).

Signals that are applied to the inputs need to have fast edge rates, as shown by  $\Delta t/\Delta v$  in the [Recommended Operating Conditions](#), to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

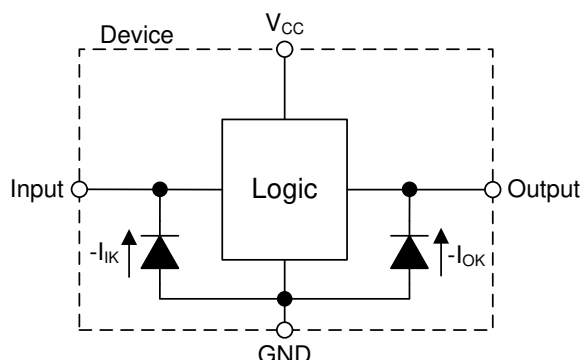


### 7.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in [Figure 7-1](#).

**CAUTION**

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

### 7.3.5 Unbuffered Logic

A standard CMOS logic function typically consists of at least three stages: the input inverter, the logic function, and the output inverter. Some devices have multiple stages at the input or output for various reasons. An unbuffered CMOS logic function eliminates the extra input and output stages; the device only contains the required logic function which is directly driven from the inputs and directly drives the outputs.

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. To learn more about how to use an unbuffered inverter in an oscillator circuit, see [Use of the CMOS Unbuffered Inverter in Oscillator Circuits](#).

## 7.4 Device Functional Modes

**Table 7-1. Function Table  
(Each Inverter)**

INPUT A	OUTPUT Y
H	L
L	H

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. An example application circuit is shown in [Figure 8-1](#). To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the [Use of the CMOS Unbuffered Inverter in Oscillator Circuits](#) application report.

### 8.2 Typical Application

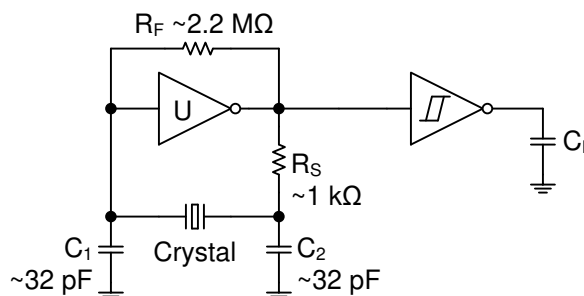


Figure 8-1. Typical Application Diagram

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the [Use of the CMOS Unbuffered Inverter in Oscillator Circuits](#) application report.

1. Recommended Input Conditions
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in [Recommended Operating Conditions](#).
  - Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in [Recommended Operating Conditions](#) at any valid  $V_{CC}$ .
2. Absolute Maximum Output Conditions
  - Load currents must not exceed ( $I_O$  max) per output and must not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in [Absolute Maximum Ratings](#).
  - Outputs must not be pulled above the voltage rated in the [Absolute Maximum Ratings](#).

### 8.2.3 Application Curve

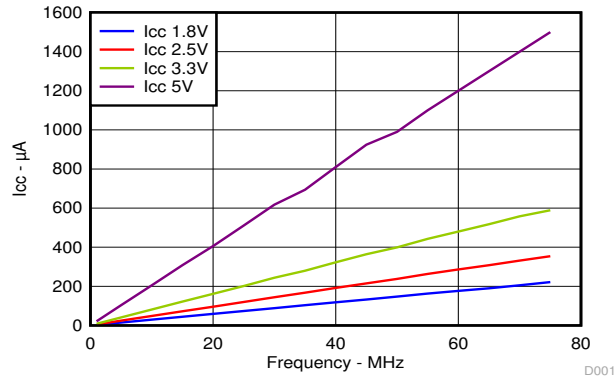


Figure 8-2. I<sub>CC</sub> vs Frequency

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

The V<sub>CC</sub> pin must have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.

An example layout is given in [Figure 8-3](#) for the DRY (SON) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

### 8.4.2 Layout Example

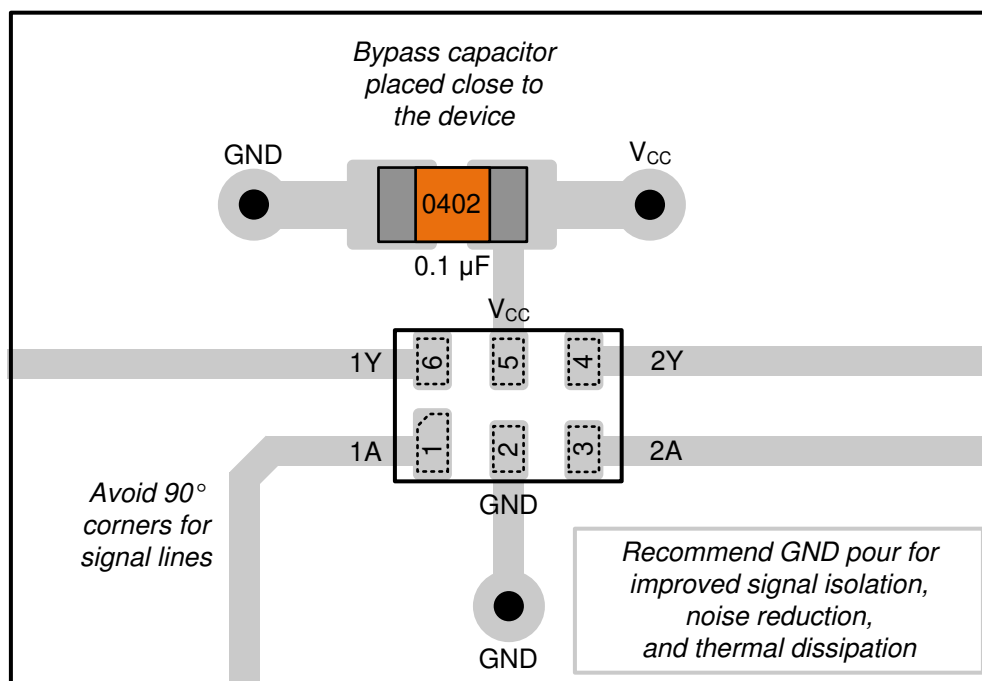


Figure 8-3. Layout example for DRY package

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

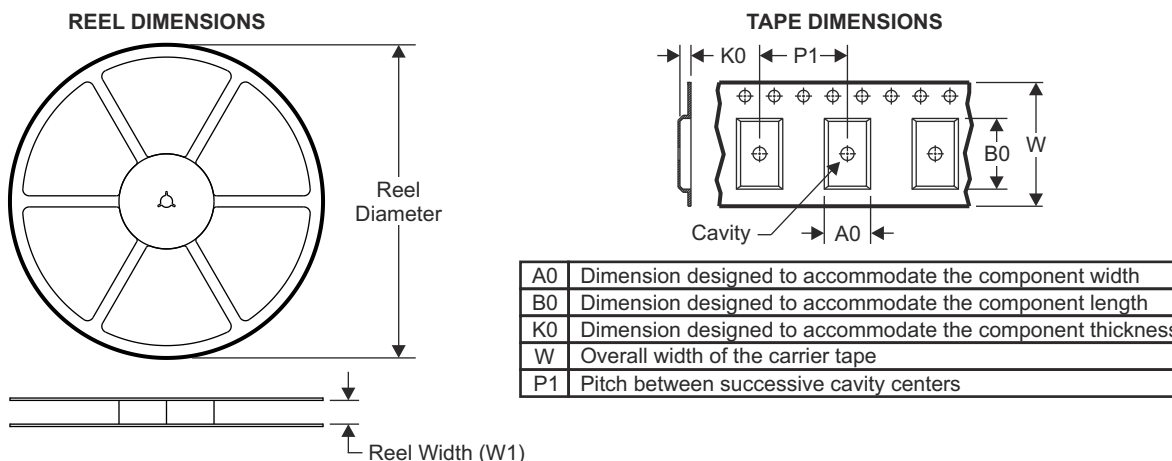
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2019) to Revision A (October 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added DCK package option .....	1
• Added DCK Thermal Information .....	5

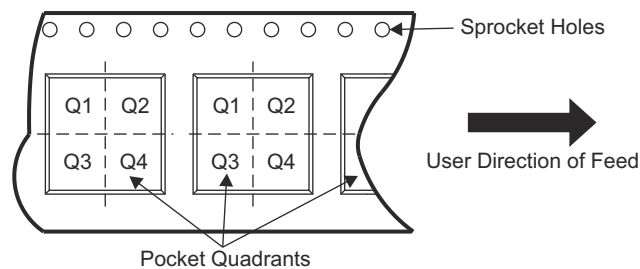
## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 11.1 Tape and Reel Information

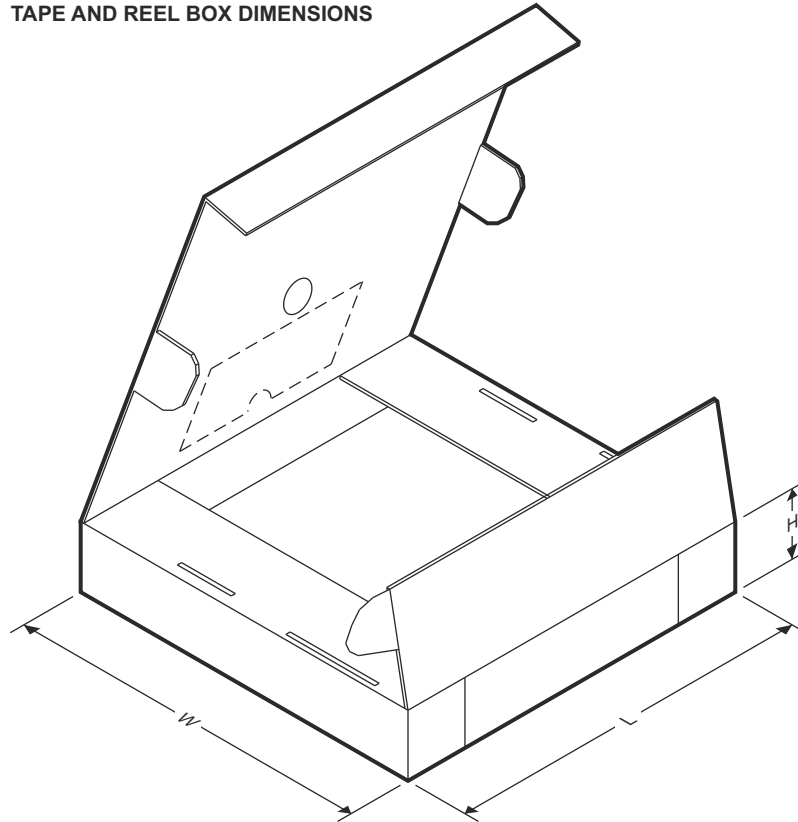


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCLVC2GU04QDCKR Q1	SC70	DKK	6	3000	180	8.4	2.3	2.5	1.2	4	8	Q3
1P2GU04QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

# TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCLVC2GU04QDCKRQ1	SC70	DCK	6	3000	210	185	35
1P2GU04QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

## 11.2 Mechanical Data

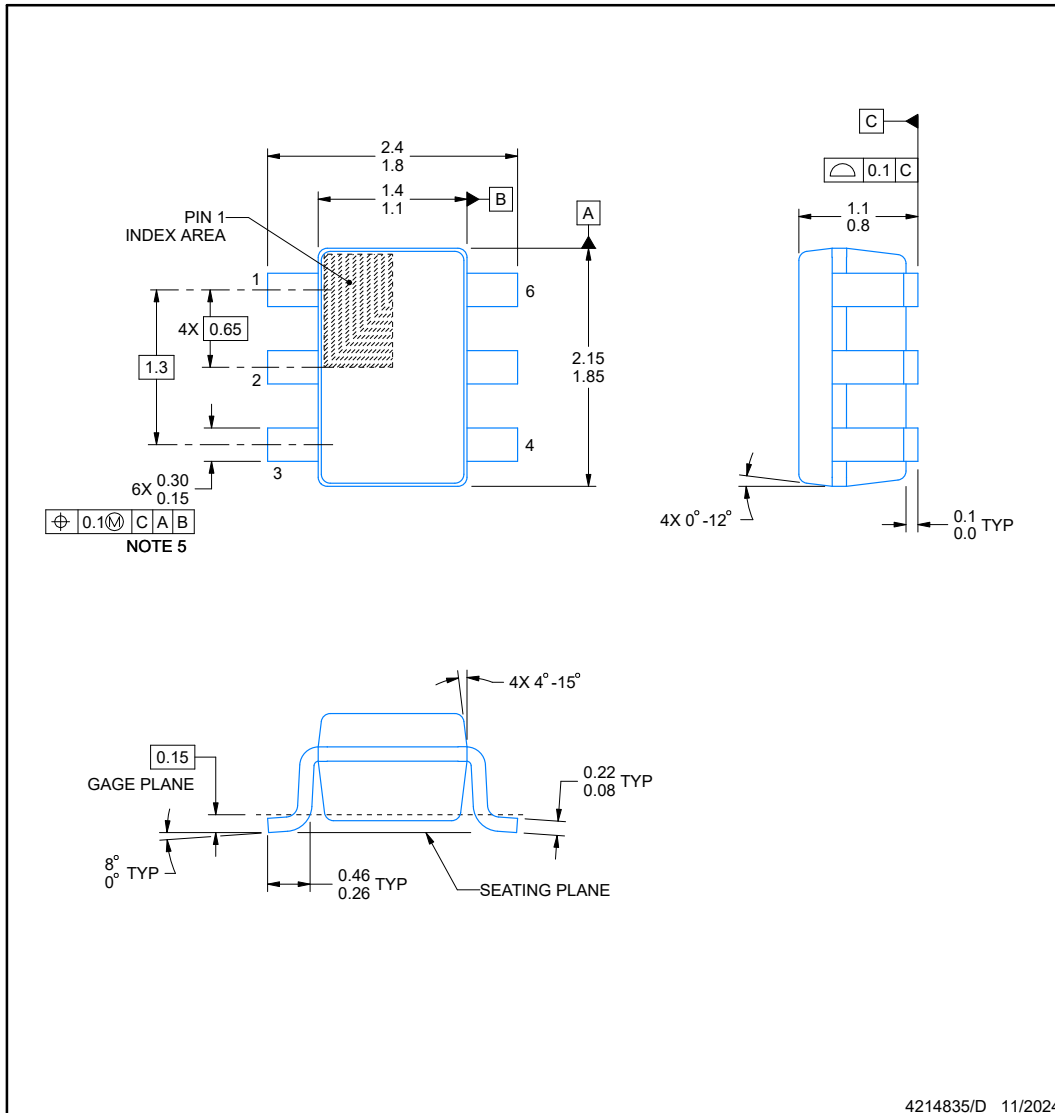
**DCK0006A**



### PACKAGE OUTLINE

**SOT - 1.1 max height**

SMALL OUTLINE TRANSISTOR



#### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

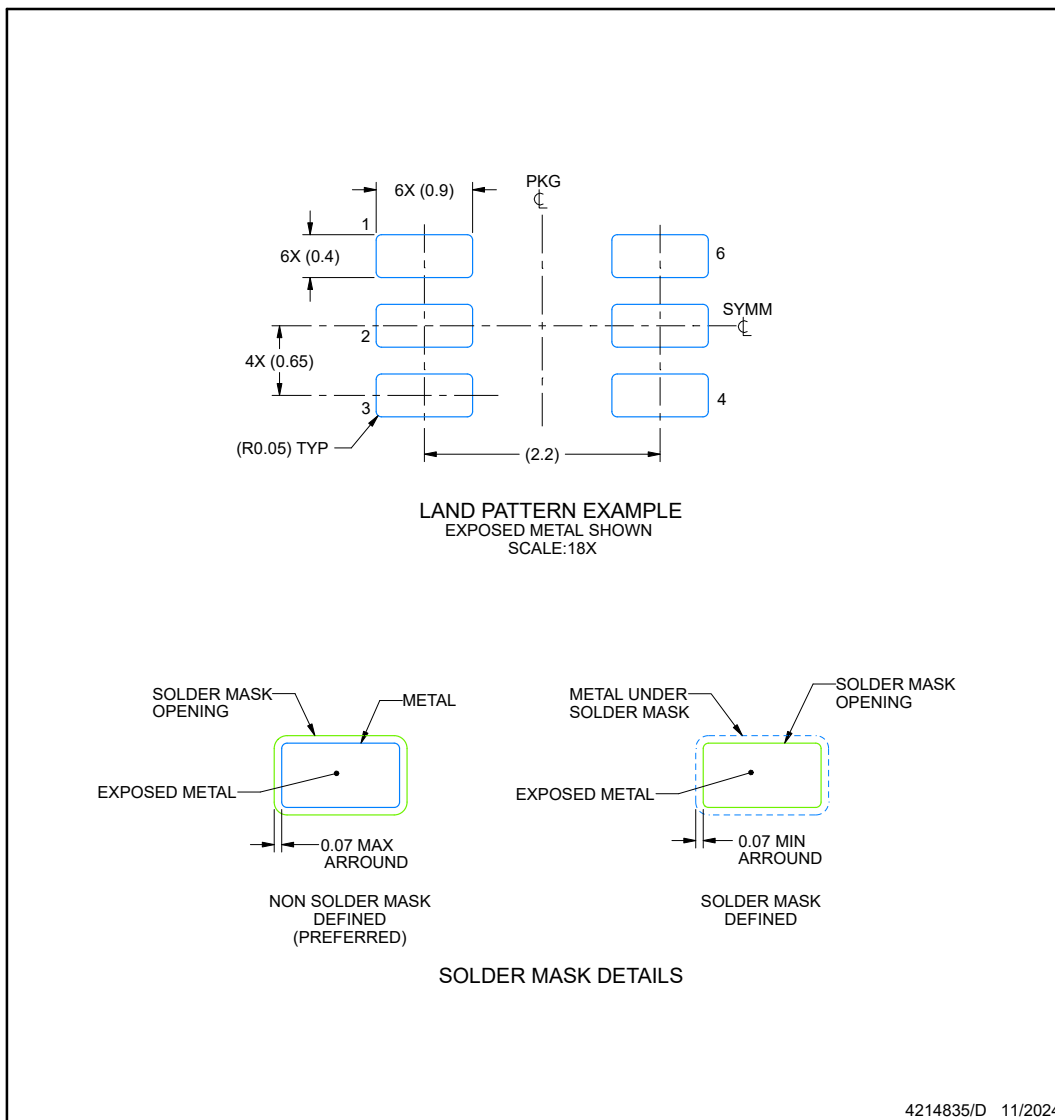


## EXAMPLE BOARD LAYOUT

**DCK0006A**

**SOT - 1.1 max height**

SMALL OUTLINE TRANSISTOR

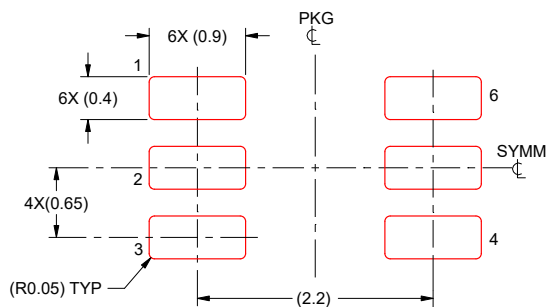


NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN****DCK0006A****SOT - 1.1 max height**

SMALL OUTLINE TRANSISTOR

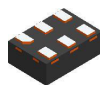


SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

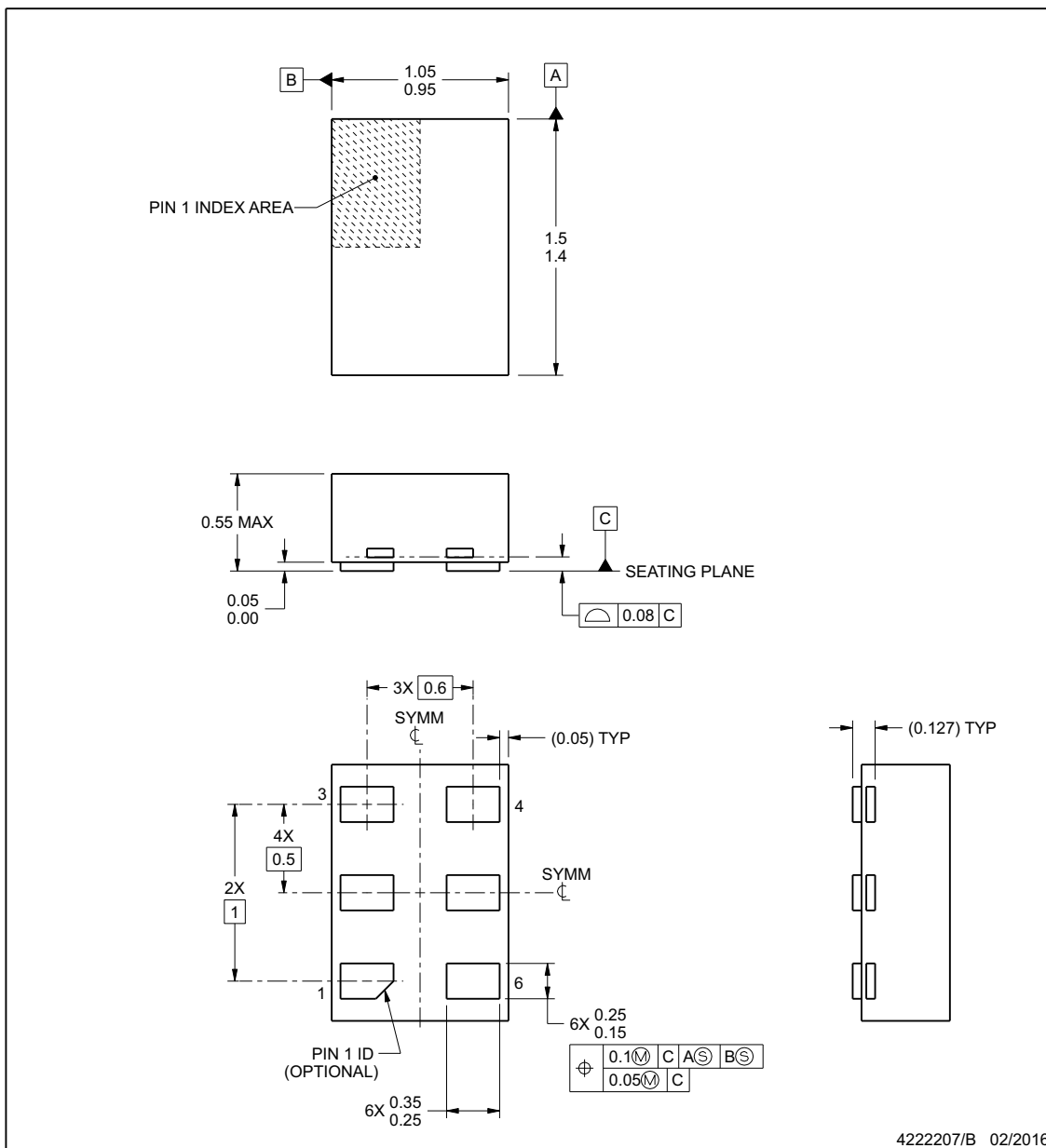


## PACKAGE OUTLINE

**DRY0006B**

**USON - 0.55 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

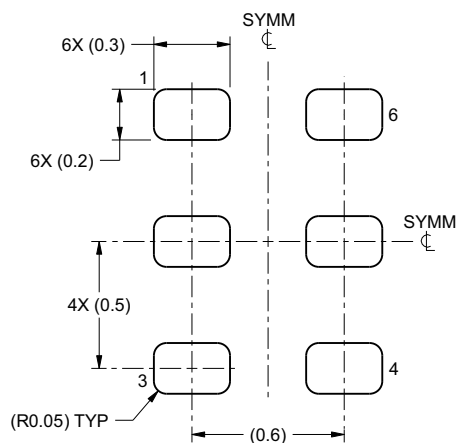


### NOTES:

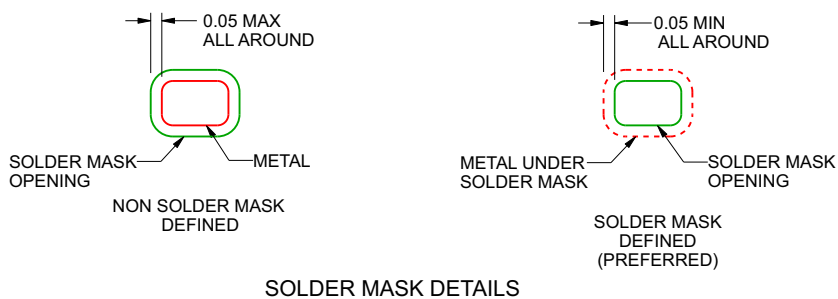
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**EXAMPLE BOARD LAYOUT****DRY0006B****USON - 0.55 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PKG SOLDER PADS  
SCALE:40X



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NOTES: (continued)

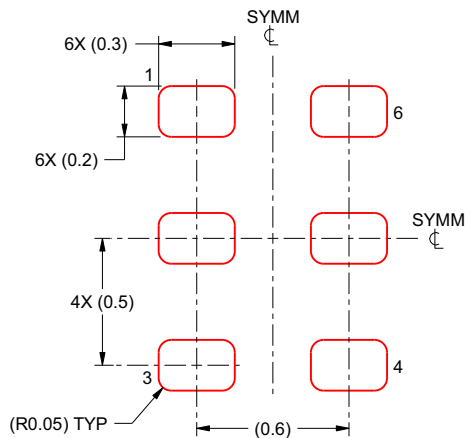
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slue271).

## EXAMPLE STENCIL DESIGN

**DRY0006B**

**USON - 0.55 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">1P2GU04QDRYRQ1</a>	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FZ
1P2GU04QDRYRQ1.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FZ
<a href="#">CLVC2GU04QDCKRQ1</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	1KR
<a href="#">PCLVC2GU04QDCKRQ1</a>	Active	Preproduction	SC70 (DCK)   6	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LVC2GU04-Q1 :**

- Catalog : [SN74LVC2GU04](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



### SOT - 1.1 max height

The technical drawing illustrates the geometry of a connector housing through three distinct views:

- Front View (Top Left):** Shows the main body with dimensions 2.4, 1.8, 1.4, 1.1, 1.3, 0.65, 2.15, 1.85, and 0.30. It includes feature callouts A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, P, Q, R, S, T, U, V, W, X, Y, Z, AA, AB, AC, AD, AE, AF, AG, AH, AI, AJ, AK, AL, AM, AN, AO, AP, AQ, AR, AS, AT, AU, AV, AW, AX, AY, AZ, BA, BB, BC, BD, BE, BF, BG, BH, BI, BJ, BK, BL, BM, BN, BO, BP, BQ, BR, BS, BT, BU, BV, BW, BX, BY, BZ, CA, CB, CC, CD, CE, CF, CG, CH, CI, CJ, CK, CL, CM, CN, CO, CP, CQ, CR, CS, CT, CU, CV, CW, CX, CY, CZ, DA, DB, DC, DD, DE, DF, DG, DH, DI, DJ, DK, DL, DM, DN, DO, DP, DQ, DR, DS, DT, DU, DV, DW, DX, DY, DZ, EA, EB, EC, ED, EE, EF, EG, EH, EI, EJ, EK, EL, EM, EN, EO, EP, EQ, ER, ES, ET, EU, EV, EW, EX, EY, EZ, FA, FB, FC, FD, FE, FF, FG, FH, FI, FJ, FK, FL, FM, FN, FO, FP, FQ, FR, FS, FT, FU, FV, FW, FX, FY, FZ, GA, GB, GC, GD, GE, GF, GG, GH, GI, GJ, GK, GL, GM, GN, GO, GP, GQ, GR, GS, GT, GU, GV, GW, GX, GY, GZ, HA, HB, HC, HD, HE, HF, HG, HH, HI, HJ, HK, HL, HM, HN, HO, HP, HQ, HR, HS, HT, HU, HV, HW, HX, HY, HZ, IA, IB, IC, ID, IE, IF, IG, IH, II, IJ, IK, IL, IM, IN, IO, IP, IQ, IR, IS, IT, IU, IV, IW, IX, IY, IZ, JA, JB, JC, JD, JE, JF, JG, JH, JI, JJ, JK, JL, JM, JN, JO, JP, JQ, JR, JS, JT, JU, JV, JW, JX, JY, JZ, KA, KB, KC, KD, KE, KF, KG, KH, KI, KJ, KK, KL, KM, KN, KO, KP, KQ, KR, KS, KT, KU, KV, KW, KX, KY, KZ, LA, LB, LC, LD, LE, LF, LG, LH, LI, LJ, LK, LL, LM, LN, LO, LP, LQ, LR, LS, LT, LU, LV, LW, LX, LY, LZ, MA, MB, MC, MD, ME, MF, MG, MH, MI, MJ, MK, ML, MM, MN, MO, MP, MQ, MR, MS, MT, MU, MV, MW, MX, MY, MZ, NA, NB, NC, ND, NE, NF, NG, NH, NI, NJ, NK, NL, NM, NN, NO, NP, NQ, NR, NS, NT, NU, NV, NW, NX, NY, NZ, OA, OB, OC, OD, OE, OF, OG, OH, OI, OJ, OK, OL, OM, ON, OO, OP, OQ, OR, OS, OT, OU, OV, OW, OX, OY, OZ, PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ, PK, PL, PM, PN, PO, PP, PQ, PR, PS, PT, PU, PV, PW, PX, PY, PZ, QA, QB, QC, QD, QE, QF, QG, QH, QI, QJ, QK, QL, QM, QN, QO, QP, QQ, QR, QS, QT, QU, QV, QW, QX, QY, QZ, RA, RB, RC, RD, RE, RF, RG, RH, RI, RJ, RK, RL, RM, RN, RO, RP, RQ, RR, RS, RT, RU, RV, RW, RX, RY, RZ, SA, SB, SC, SD, SE, SF, SG, SH, SI, SJ, SK, SL, SM, SN, SO, SP, SQ, SR, SS, ST, SU, SV, SW, SX, SY, SZ, TA, TB, TC, TD, TE, TF, TG, TH, TI, TJ, TK, TL, TM, TN, TO, TP, TQ, TR, TS, TT, TU, TV, TW, TX, TY, TZ, UA, UB, UC, UD, UE, UF, UG, UH, UI, UJ, UK, UL, UM, UN, UO, UP, UQ, UR, US, UT, UU, UV, UW, UX, UY, UZ, VA, VB, VC, VD, VE, VF, VG, VH, VI, VJ, VK, VL, VM, VN, VO, VP, VQ, VR, VS, VT, VU, VV, VW, VX, VY, VZ, WA, WB, WC, WD, WE, WF, WG, WH, WI, WJ, WK, WL, WM, WN, WO, WP, WQ, WR, WS, WT, WU, WV, WW, WX, WY, WZ, XA, XB, XC, XD, Xe, XF, XG, XH, XI, XJ, XK, XL, XM, XN, XO, XP, XQ, XR, XS, XT, XU, XV, XW, XX, XY, XZ, YA, YB, YC, YD, YE, YF, YG, YH, YI, YJ, YK, YL, YM, YN, YO, YP, YQ, YR, YS, YT, YU, YV, YW, YX, YY, YZ, ZA, ZB, ZC, ZD, ZE, ZF, ZG, ZH, ZI, ZJ, ZK, ZL, ZM, ZN, ZO, ZP, ZQ, ZR, ZS, ZT, ZU, ZV, ZW, ZX, ZY, ZZ.

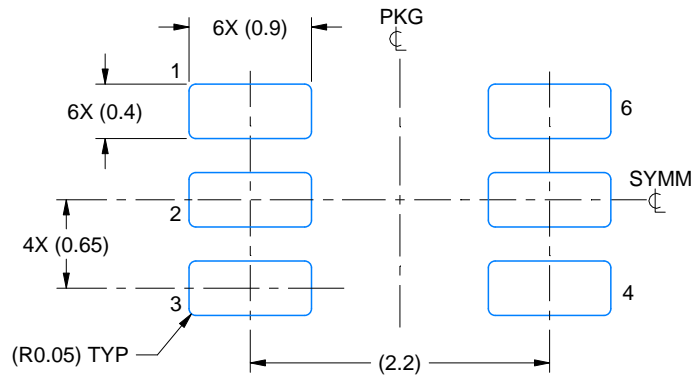
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

4. Falls within JEDEC MO-203 variation AB.





LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X

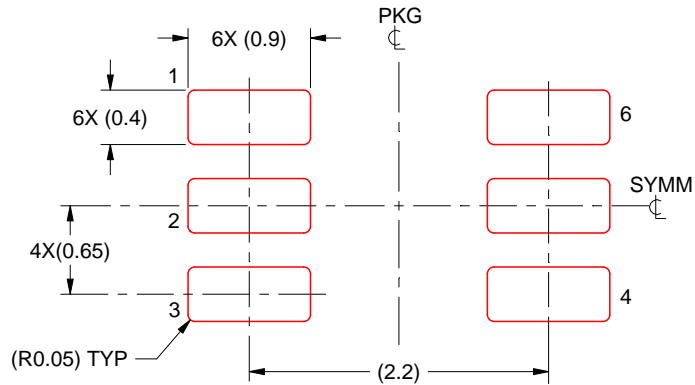


SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 THICK STENCIL  
 SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G



## PACKAGE OUTLINE

## USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

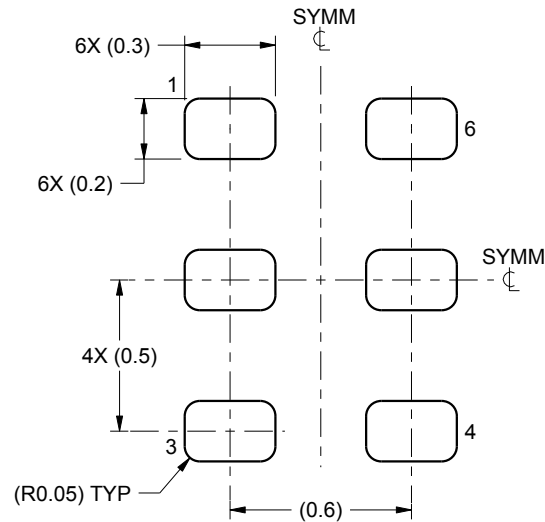
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

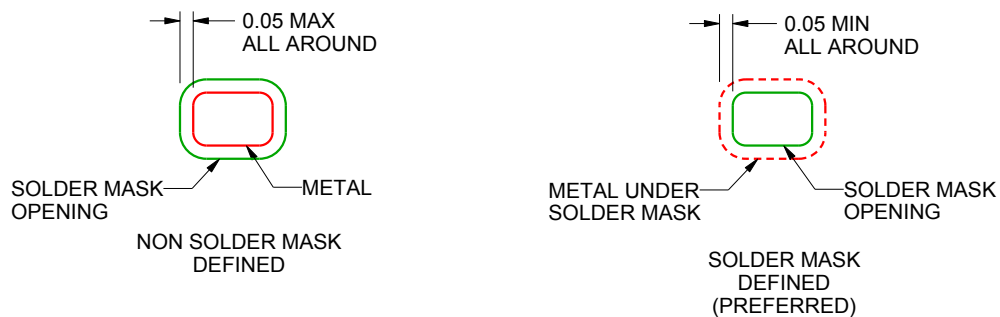
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

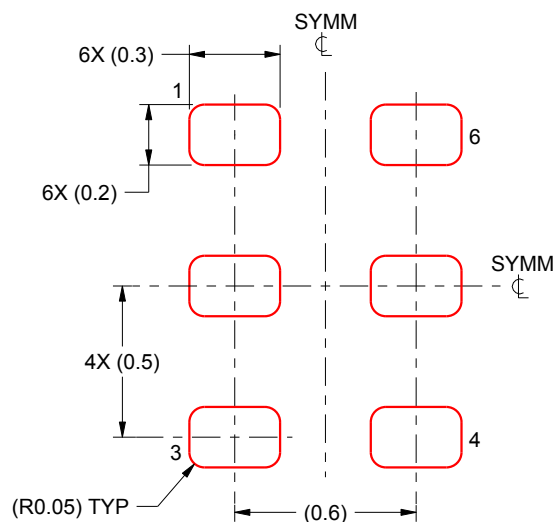
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).

## EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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