TPS371K-Q1 Automotive 1500V Window (OV & UV) Supervisor with Integrated Buffer for 400V and 800V DC-Link Voltage Measurements

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C
- Functional Safety-Compliant Targeted (Preview)
  - Development targeted for functional safety applications
  - Documentation to aid ISO 26262 system design
- Overvoltage and undervoltage fault monitor for 400V & 800V BMS and DC-Link
  - 1% overvoltage and undervoltage outputs
  - Fast detection time (<5µs) to help minimize system fault tolerant time interval
  - 30V to 60V Low UV output
- Device flexibility to meet design requirements
  - User selectable adjustable overvoltage and undervoltage thresholds
  - User programmable capacitor-based glitch rejection and deassertion delay
- Integrated buffer for ADC monitoring
  - High accuracy 0.35% (maximum) scaled down voltage of sense pin
  - VSENSE pin can directly drive high-speed ADC inputs
- Designed for safety applications (Preview)
  - Output latching feature to help bring system to safe state
  - Built-In Self-Test to monitor device functionality and enhance system protection

2 Applications

- High-voltage battery system
- Traction inverter
- Integrated high voltage (OBC & DC/DC)
- DC/DC converter system

3 Description

TPS371K-Q1 is an automotive supervisor for voltage monitoring with an integrated buffer for 400V and 800V DC-link voltage measurements. The TPS371K-Q1 eliminates large resistor ladders with the integrated high voltage ladder. This device's SENSE pin can be directly connected to 400V or 800V automotive battery systems and DC-Link for continuous monitoring of overvoltage (OV), undervoltage (UV), and low undervoltage (LUV) conditions. The TPS371K-Q1 offers CTS for programmable glitch rejection for noisy environments.

The TPS371K-Q1 has a integrated high-speed buffer VSENSE for supply voltage measurements. The buffer has a low output impedance which can directly drive ADC inputs. VSENSE is a scaled down voltage of the SENSE pin input.

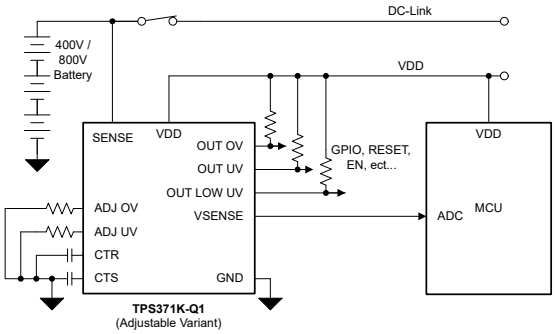
The combination of voltage supervisor and integrated buffer allows for the smallest signal chain size for direct monitoring of 400V and 800V systems. This combination also allows for redundant digital and analog always on voltage fault monitoring.

The TPS371K-Q1 is available in a 12.8mm × 7.4mm SOIC 15-pin package. TPS371K-Q1 operates over -40°C to +125°C T_A.

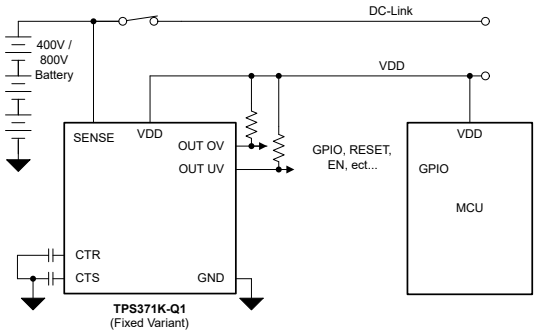
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS371K-Q1	SOIC (15) (DFX)	12.8mm × 7.4mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit Adjustable Version



Typical Application Circuit Fixed Version

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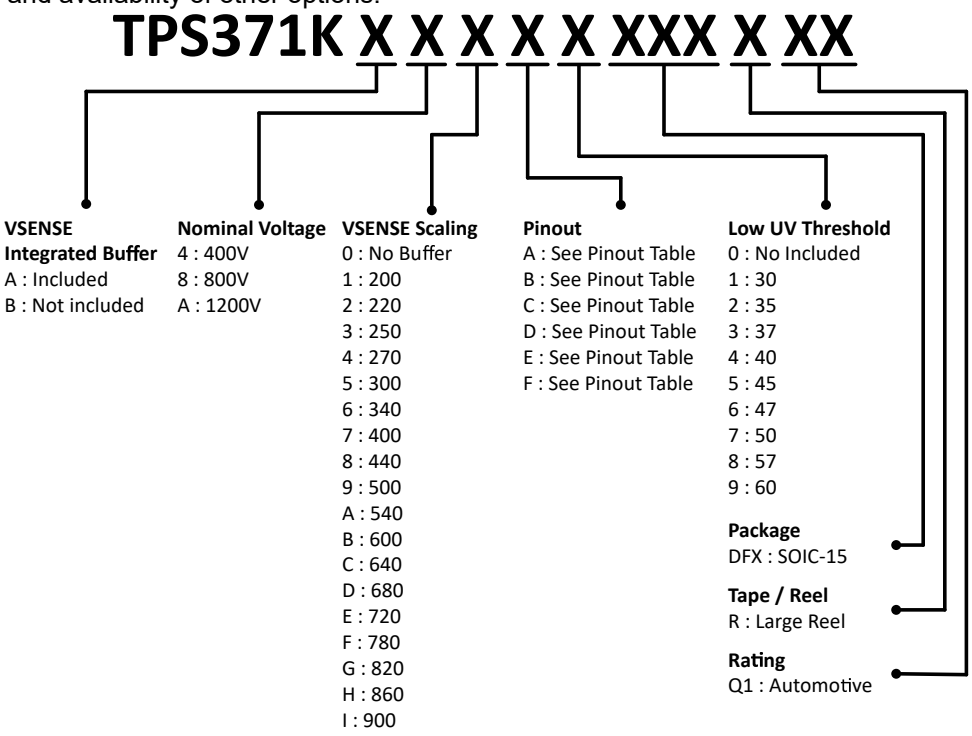
4 Device Comparison

Device Decoder shows some of the device naming nomenclature of the TPS371K-Q1 adjustable option. Not all device namings follow this nomenclature table. For a detailed breakdown of every adjustable and fixed voltage threshold variant see Device Nomenclature for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.



1. Not all TPS371K-Q1 devices can be decoded by this table. Refer to Device Nomenclature for a decoding table by part number and for fixed threshold variants.
2. For 400V TPS371K-Q1, the undervoltage threshold can be between 180V to 300V and overvoltage can be between 440V to 540V.
3. For 800V TPS371K-Q1, the undervoltage threshold can be between 360V to 600V and overvoltage can be between 860V to 1080V.
4. For 1200V TPS371K-Q1, the undervoltage threshold can be between 540V to 900V and overvoltage can be between 1290V to 1500V.

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5 Pin Configuration and Functions

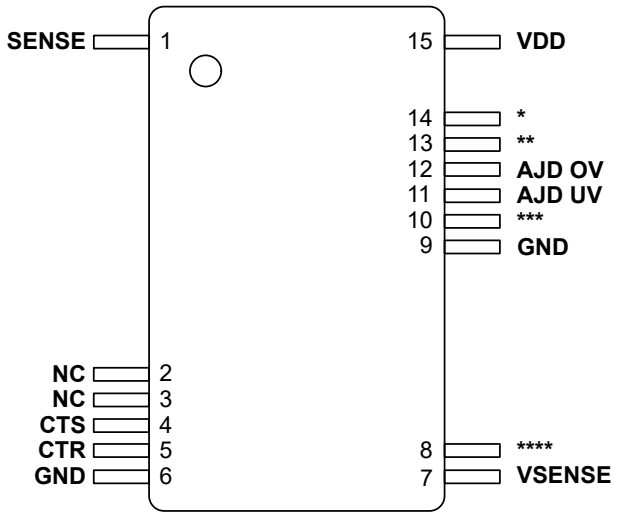

Figure 5-1. DFX Package, 15-Pin SOIC, TPS371KA-Q1 Adjustable Version (Top View)

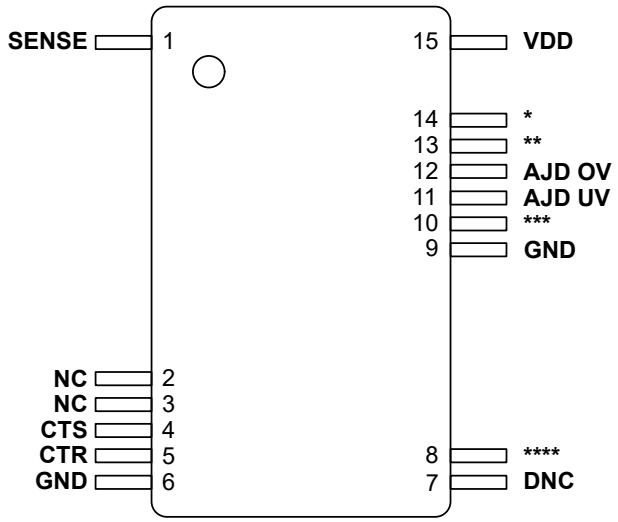

Figure 5-2. DFX Package, 15-Pin SOIC, TPS371KB-Q1 Adjustable Version (Top View)

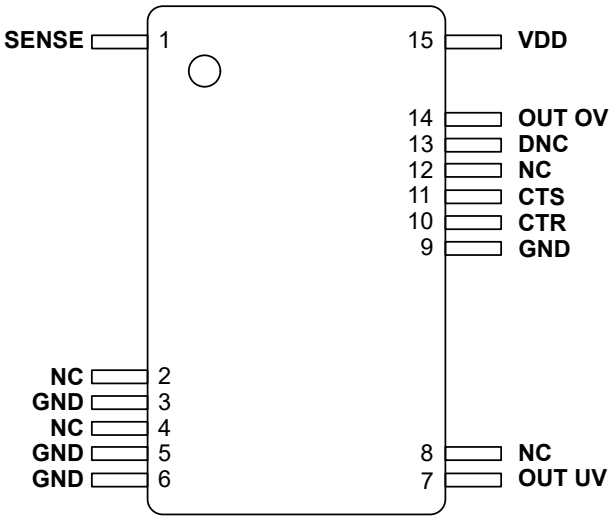

Figure 5-3. DFX Package, 15-Pin SOIC, TPS371K -Q1 Fixed Version (Top View)

Table 5-1. Pinout Table

OPN Pinout	Pin 8****	Pin 10 ***	Pin 13 **	Pin 14 *
A	BIST EN	BIST	OUT UV	OUT OV
B	NC	NC	OUT UV	OUT OV
C	BIST EN	LOW UV & BIST	OUT UV	OUT OV
D	NC	LOW UV	OUT UV	OUT OV
E	BIST EN	BIST	LOW UV	OUT OV
F	NC	NC	LOW UV	OUT OV

Table 5-2. Pin Functions

PIN				I/O	DESCRIPTION
NAME	TPS371 KANO.	TPS371 KBNO.	TPS371 K Fixed NO.		
SENSE	1	1	1	I	**Sense Voltage:** Connect this pin to the voltage rail that must be monitored.
GND	4, 7	4, 7	4,5,6,9	-	**Ground.** All GND pins must be electrically connected to the board ground.
CTR	5	5	10	O	**Release Time Delay:** User-programmable release time delay for output pins. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Device Nomenclature table for output pin configurations.
CTS	6	6	11	O	**SENSE Time Delay:** User-programmable sense time delay for SENSE. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Device Nomenclature table for output pin configurations.
VSENSE	9	-	-	O	**Voltage SENSE**: The output of the integrated buffer that is a scaled down voltage of the SENSE pin. See Device Nomenclature table for output pin configurations.
ADJ UV	11	11	-	I	**Adjustable Undervoltage Threshold**: User can program the internal undervoltage thresholds by using external resistors to set a voltage at start-up. See voltage threshold table for selectable threshold options.
ADJ OV	12	12	-	I	**Adjustable Overvoltage Threshold**: User can program the internal overvoltage threshold by using external resistors to set a voltage at start-up. See voltage threshold table for selectable threshold options.
OUT UV	See Pinout Table	See Pinout Table	7	O	**Output Undervoltage Signal:** OUT UV asserts when SENSE crosses the undervoltage threshold. Assertion time delay is either fixed or set by CTS. OUT UV remains asserted for the release time delay period after SENSE transitions out of a fault condition. The active low open-drain release output requires an external pullup resistor. See Device Nomenclature table for OUT UV threshold and timing configurations. Output topology: **Open-Drain Active-Low**
OUT OV	See Pinout Table	See Pinout Table	14	O	**Output Overvoltage Signal:** OUT OV asserts when SENSE crosses the Overvoltage threshold. Assertion time delay is either fixed or set by CTS. OUT OV remains asserted for the release time delay period after SENSE transitions out of a fault condition. The active low open-drain release output requires an external pullup resistor. See Device Nomenclature table for OUT OV threshold and timing configurations. Output topology: **Open-Drain Active-Low**
LOW UV	See Pinout Table	See Pinout Table	-	O	**Output Low Undervoltage Signal:** OUT Low UV asserts when SENSE crosses the Low Overvoltage threshold after the sense time delay, set by CTS. OUT Low UV remains asserted for the release time delay period after SENSE transitions out of a fault condition. The active low open-drain release output requires an external pullup resistor. Output topology: **Open-Drain Active-Low**
BIST	See Pinout Table	See Pinout Table	-	O	**Output Built-in Self-test (BIST):** BIST asserts when BIST is in operation. BIST operation is initiated at device start-up and by a rising edge on BIST_EN pin. BIST is a device diagnostic test that checks for internal failures. If there is a failure, BIST stays asserted. Upon successful BIST, BIST pin de-asserts. Output topology: **Open-Drain Active-Low**
BIST_EN	See Pinout Table	See Pinout Table	-	I	**Built-in Self-test Enable (BIST EN):** A rising edge on BIST enable pin initiates the BIST. For variants with latch, BIST EN also enables and disables latch.
VDD	15	15	15	I	**Input Supply Voltage:** Supply voltage pin. Bypass with a 0.1µF capacitor to GND for noisy environments.

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Table 5-2. Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	TPS371 KANO.	TPS371 KBNO.	TPS371 K Fixed NO.		
NC	2, 3, 8	2, 3, 8	2, 4, 8, 12	-	**No Connect:** Leave pins floating or connect to GND.
DNC	-	7	13	-	**Do Not Connect:** Leave pins floating for proper operation.

6 Device and Documentation Support

6.1 Device Nomenclature

Device Decoder in Table 5-1 describe how to decode certain device function of the device based on the orderable part number. Not all part numbers follow this nomenclature. Use Table 6-1 as the part number decoding table for all devices.

Table 6-1. Device Configuration Table

ORDERABLE PART NAME	Thresholds	OV Threshold	OV Hysteresis	UV Threshold	UV Hysteresis	Low UV Threshold	Time Delay	VSENSE Scale
PTPS371KVM5DFXRQ1	Fixed	900V	2%	N/A	N/A	N/A	ADJ CTS ADJ CTR	N/A

6.2 Documentation Support

6.2.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *Sensitivity Analysis for Power Supply Design*, SLVA481

6.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.5 Trademarks

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6.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

ADVANCE INFORMATION

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PPS371KA8C89DFXRQ1	Active	Preproduction	SSOP (DFX) | 15	750 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

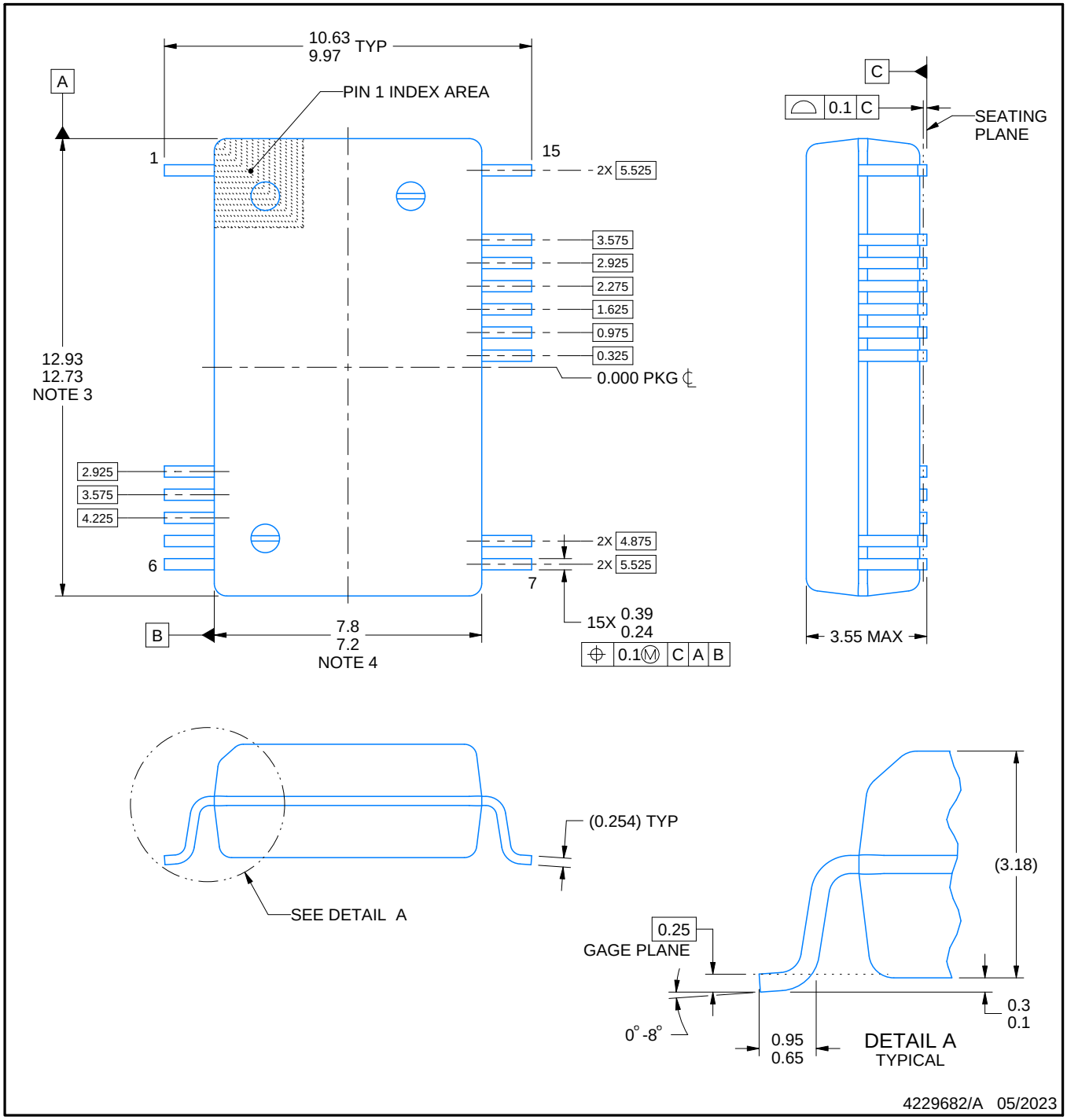
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DFX0015A

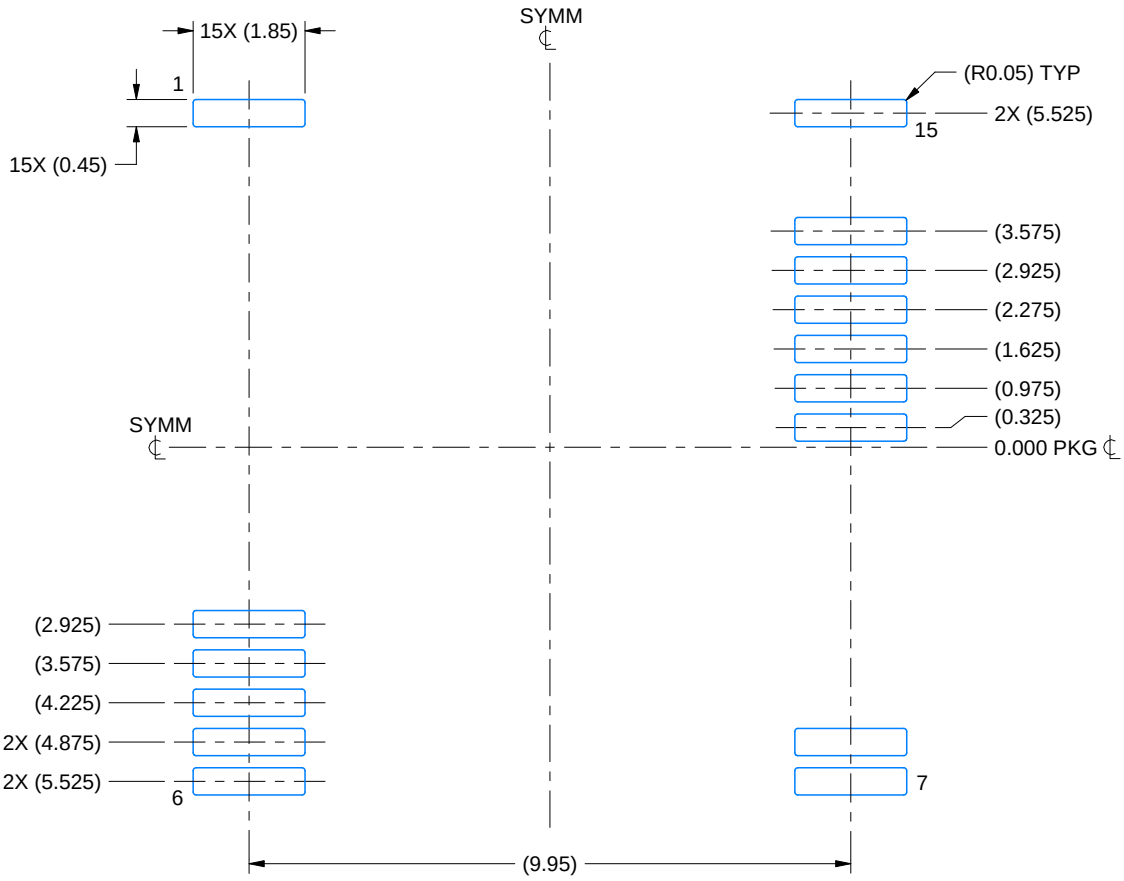
SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE

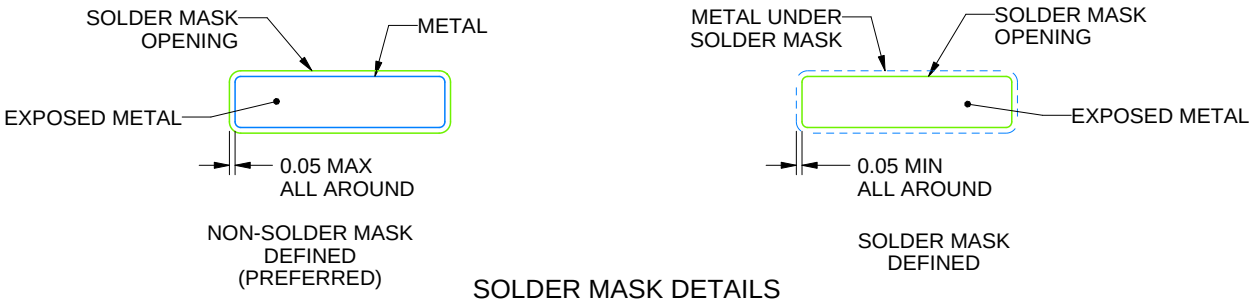


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4229682/A 05/2023

NOTES: (continued)

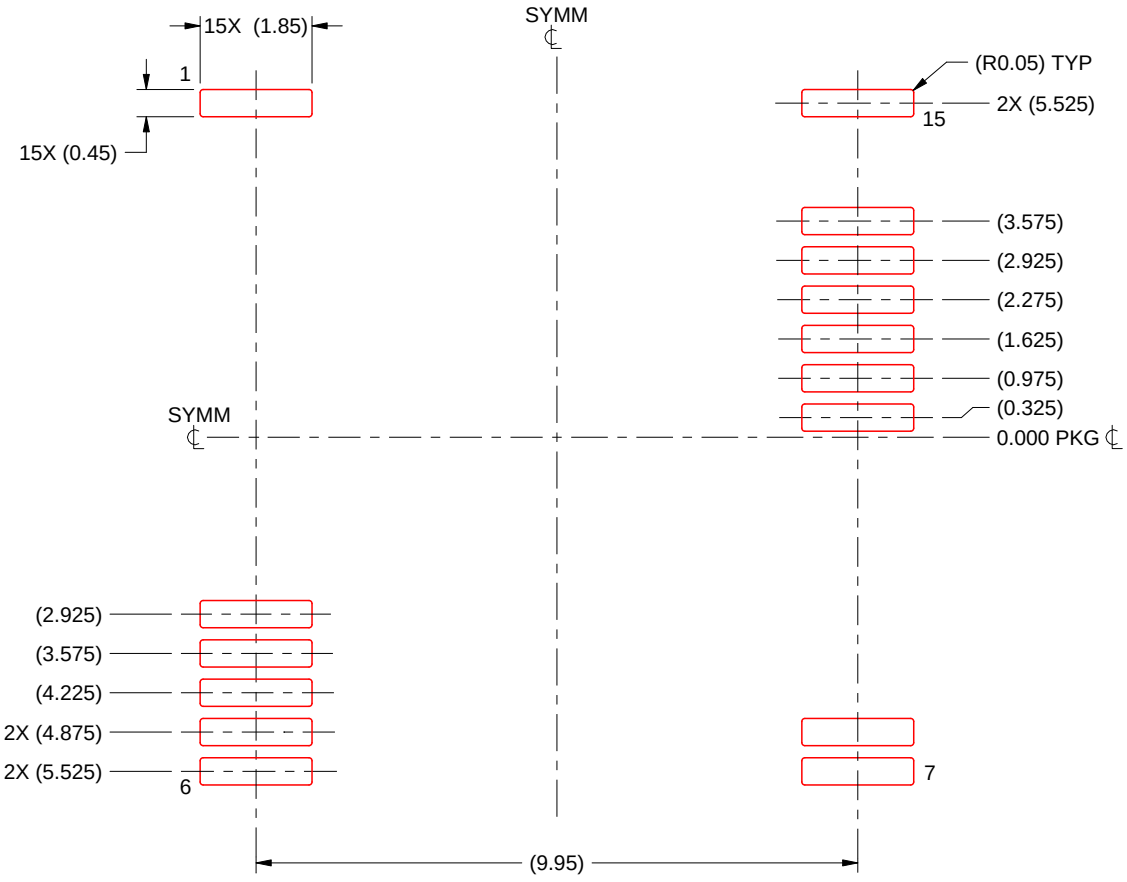
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFX0015A

SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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