TPS61381-Q1 Automotive 400kHz, 40V, 15A Boost Converter with LDO Charger and Battery State of Health Detection

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- I2C programmable LDO charger
  - Supports charger input voltage (VOUT Pin) up to 21V, absmax up to 40V to withstand load dump
  - Supports multi-chemistry battery charging profile of 1-5 cell NiMH, 1-2 cell Li-Ion, LiFePO4, 1-4 cell super capacitor
  - Programmable charging current 50mA and 100mA
  - Wide battery voltage operating range 0V to 12V
  - Programmable charging timer up to 32h
  - NTC thermistor input to monitor battery temperature
- Programmable boost converter supporting 12V car battery back-up power system
  - Programmable output voltage range: 5V to 12V
  - Programmable boost average input current limit from 5A to 15A
  - Back-up battery (BUB) voltage in boost mode: 0.5V to 12V
    - Minimum 3V for start up
    - Can start up at 1V when Vout>5V
  - <20us automatic transition into the boost mode when 12V system voltage drops
- Backup battery State-of-Health(SOH) detection
  - Adjustable discharge current from 0A to 1.5A
  - Multi-signal analog output(AVI pin) of battery voltage, discharge current and battery temperature
- Lower quiescent current and leakage current
  - 20μA quiescent current in standby mode
  - < 1μA shutdown current
  - < 1μA leakage current for pins connected to the back up battery
- EMI mitigation
  - 400kHz fix switching frequency
  - Optional programmable spread spectrum
- 3mm × 4mm 25-pin package with wettable flank

2 Applications

- Emergency call(eCall)

3 Description

The TPS61381-Q1 is 400kHz, 40V, 15A automotive bi-directional boost converter/ LDO charger with battery state of health detection function designed for back-up power systems like TBOX or e-call. The converter supports absmax voltage up to 40V on VOUT pin to withstand load-dump condition and supports direct connection with 12V car battery.

The TPS61381-Q1 integrates I2C configurable LDO charger supporting NiMH, Li-Ion, LiFePO4, super capacitor.

TPS61381-Q1 integrates boost function that operates over 0.5V to 12V BUB voltage and 5-12V output voltage. The device applies fix frequency peak current control scheme with optional spread spectrum to minimize EMI. The boost function supports 5A-15A programmable average current limit.

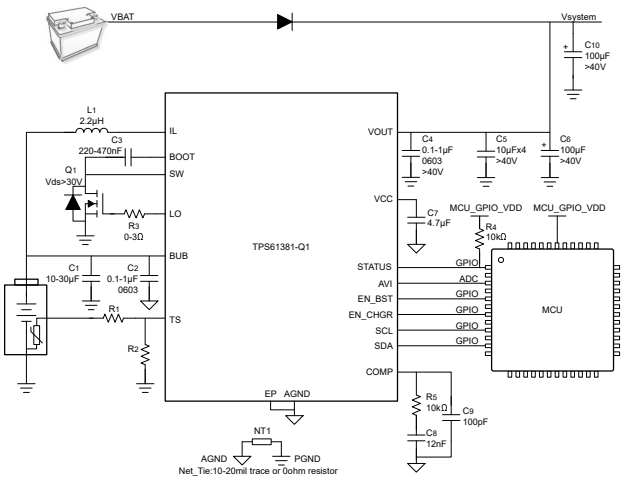
The TPS61381-Q1 integrates battery health detection feature which discharge the battery with a constant current and detects the voltage drop across the battery internal resistance.

The TPS61381-Q1 is available in a 3mm × 4mm QFN package with wettable flank. Care must be taken when designing the PCB with TPS61381-Q1, view Section 8.4.2 for details.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS61381-Q1	RAV	3.0mm × 4.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit

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4 Pin Configuration and Functions

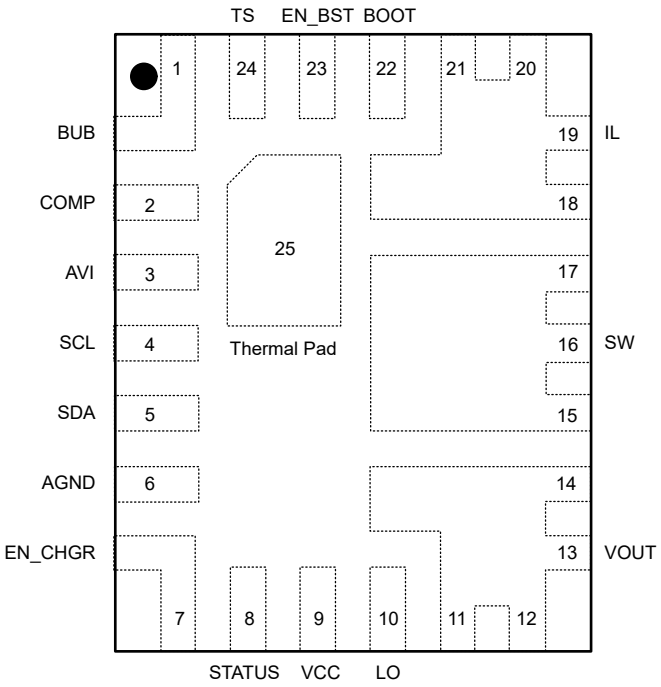


Figure 4-1. 24-Pin QFN with Wettable Flank Package (Top View)

TERMINAL		I/O	DESCRIPTION
NAME	RAV		
BUB	1	I	Back up battery voltage sensing pin. Connect BUB as close as possible to the battery's positive terminal for the most accurate voltage sense.
COMP	2	O	External compensation pin. This pin is the output of the transconductance amplifier. Connect a compensation network from the COMP pin to AGND.
AVI	3	O	Analog voltage output pin for battery State of Health (SOH) detection function. AVI pin can be configured to output back-up battery voltage, discharge current and back up battery temperature. The pin has internal 125kΩ pulldown resistance to AGND when AVI output is disabled.
SCL	4	I	Clock pin for I2C interface.
SDA	5	I/O	Data pin for I2C interface.
AGND	6	G	Signal ground pin. Connect with PGND (Low side MOSFET source) through 20mil wire or 0Ω resistor. View Section 8.4.2 for detailed GND connection.
EN_CHGR	7	I	Charger function enable pin. Drive this pin high / low to enable / disable the charger function.
STATUS	8	O	STATUS indication output pin. Open drain output for STATUS indication function. Output low when entering boost mode by default. Selectable by I2C to to output other signals.
VCC	9	O	Internal regulator output. Used as supply to internal control circuits. Do not connect this pin to any external loads. Connect 2.2-4.7μF capacitor from this pin to AGND
LO	10	O	Gate driver pin for low-side MOSFET
VOUT	11, 12, 13, 14	P	Boost converter output pin.

TERMINAL		I/O	DESCRIPTION
NAME	RAV		
SW	15, 16, 17	P	Device switch pins and the switch node of the regulator. Connect to the low side MOSFET drain.
IL	18, 19, 20, 21	P	Boost converter input pin. Connect to the inductor.
BOOT	22	O	Power supply for the high-side MOSFET gate driver. Connect a 100nF-470nF capacitor between the SW node and BOOT. An internal diode charges the capacitor while SW node is low.
EN_BST	23	I	Boost function enable pin. Drive this pin high / low to enable / disable the boost function.
TS	24	I	Temperature qualification voltage input pin. Connect a negative temperature coefficient (NTC) thermistor directly from TS to GND (AT103-2 recommended). Charge suspends when the TS pin voltage is out of range.
EP	25	G	Thermal pad. Connect with AGND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals	SW, VOUT	–0.3	40	V
	IL	–0.3	18	V
	BUB, EN_BST, EN_CHGR, STATUS	–0.3	15	V
	LO, TS, AVI, SDA, SCL, VCC, COMP	–0.3	6	V
	BOOT to SW	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(2)	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins(3)	±500	
$V_{(ESD)}$ (1)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins(3)	±750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BUB}	Back-up battery voltage range	0.5		12	V
V_{OUT}	Output voltage range	Vin		20	V
L	Effective inductance range for 400kHz frequency	1*0.7	2.2		µH
C_I	Effective input capacitance range, (disable BuB voltage loop)		10		µF
C_I	Effective input capacitance range, (enable BuB voltage loop), BUB IR<100mohm			10	µF
C_I	Effective input capacitance range, (enable BuB voltage loop), BUB IR<400mohm			5	µF
C_O	Effective output capacitance range	30	220		µF
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		PKG DES (16 PINS)	PKG DES (16 PINS)	UNIT
		Standard	EVM(2)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.4	25.49	°C/W

THERMAL METRIC(1)		PKG DES (16 PINS) Standard	PKG DES (16 PINS) EVM(2)	UNIT
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.0	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.9	13.05	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	23.6	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS61381QEVM-126, 4-layer, 2oz copper, 116mmx76mm PCB.

5.5 Electrical Characteristics

T_J = -40°C to 150°C, V_{BUB} = 3.6V and V_{OUT} = 12V(LDO charger mode), V_{OUT} = 6.2V(boost mode). Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{BUB}	Back-up battery voltage range		0		13	V
V_{BUB_UVLO}	Under-voltage lockout threshold	V_{BUB} rising with V_{OUT} = 0V			2.8	V
		V_{BUB} rising with V_{OUT}>5V or V_{CC} >4.5V, boost mode active			1	V
		V_{BUB} falling with V_{OUT} > V_{VOUT_UVLO}, boost mode active			0.5	V
V_{VOUT_UVLO}	Under-voltage lockout threshold	V_{OUT} rising			3.5	V
$V_{VOUT\_UVLO\_HYS}$	V_{VOUT_UVLO} hysteresis				300	mV
$I_{Q\_BOOST\_STANDBY}$	Quiescent current into BUB pin at boost and standby mode	Boost is enable, LDO is disable, SOH disable, No load, No switching, Vout_target = 6.2 V, V_{OUT} = 10 V to 18 V, T_J up to 85°C, Vout is pre-biased.		0.01	0.1	uA
	Quiescent current into VOUT pin at boost and standby mode	Boost is enable, LDO is disable, SOH disable, No load, No switching, Vout_target = 6.2 V, V_{OUT} = 10 V to 18 V, T_J up to 85°C, Vout is pre-biased.		20	30	uA
$I_{Q\_LDO\_STANDBY}$	Quiescent current into BUB pin at LDO and standby mode	LDO mode enabled and boost mode disable, SOH disable, No load, No switching, No active re-charge, Vout = 12 V, V_{BUB} > target, T_J up to 85°C		0.01	0.1	uA
	Quiescent current into VOUT pin at LDO and standby mode	LDO mode enabled and boost mode disable, SOH disable, No load, No switching, No active re-charge, Vout = 12 V V_{BUB} > target, T_J up to 85°C		20	30	uA
I_{SD}	Shutdown current into BUB pin	EN_BST=0 and EN_CHGR=0, T_J up to 85°C		0.2	1	uA
	Shutdown current into VOUT pin	EN_BST=0 and EN_CHGR=0, T_J up to 85°C		0.2	1	uA
I_{VOUT_LKG}	Leakage current into VOUT pin ， Q2 leakage current	V_{SW} = V_{IL} = 0V and V_{OUT} = 10 V to 18 V, IC disabled, T_J up to 85°C		0.1	10	uA
I_{IL_LKG}	Leakage current into IL pin, Q leakage current	V_{SW} = V_{OUT} = 0V and V_{IL} = 0 V to 4.8 V, IC disabled, T_J up to 85°C		0.1	10	uA
V_{CC}	Internal regulator output	Icc=20mA	5	5.2	5.35	V
BOOST OUTPUT						
V_{OUT}	Output voltage setting range	Programmable by I2C	5		12	V

T_J = -40°C to 150°C, V_{BUB} = 3.6V and V_{OUT} = 12V(LDO charger mode), V_{OUT} = 6.2V(boost mode). Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT\_PWM\_ACY}$	Output voltage accuracy	PWM or FPWM	–2.5		2.5	%
$V_{OUT\_PFM\_ACY}$		PFM		1.5		%
$V_{OUT\_STANDBY}$	Boost standby threshold	Vout rising		6		%
V_{OUT_OVP}	Charger and boost output over voltage protection, rising			23		V
	Charger and boost output over voltage protection, falling			21		V
t_{OFF_min}	Min. off time	Boost mode, low side		100	157	ns
Duty_min_down_mode	Minimum duty at boost mode			6	11	%
I_{LIM_boost}	Average current limit accuracy in boost mode	I_{LIM_boost} = 5A	4	5	6	A
		I_{LIM_boost} = 10A	8	10	12	A
		I_{LIM_boost} = 15A	11	15	18	A
I_{peak_boost}	Absolute peak current limit range in boost mode	I_{LIM_boost} = 5A or 10A		15		A
		I_{LIM_boost} = 15A		30		A
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on resistance	VCC = 5.0V		20		mΩ
$R_{DS(on)}$	Isolation MOSFET on resistance	VCC = 5.0V		6		mΩ
f_{SW}	Switching frequency		360	400	440	kHz
GATE DRIVER						
V_{DRV_L}	Low-state voltage drop	100-mA sinking		0.08		V
V_{DRV_H}	High-state voltage drop	VCC – VDRV, 100-mA sourcing		0.18		V
CHARGER CC/CV						
V_{BUB}	BUB CV setting voltage range		1.7		12	V
	V_{BUB} accuracy	For Li-ion and LiFePO4,T_J = -20°C ~ 85°C	–1		1	%
	V_{BUB} accuracy	For Supercap,T_J = -20°C ~ 85°C	–2		2	%
I_{CC}	Charging current setting range		50		100	mA
	I_{CC} accuracy	50 mA =< I_{CC} < 100mA,T_J = -20°C ~ 85°C	–20		20	%
V_{BUB_SHORT}	BUB short circuit voltage rising threshold, per cell for Li-ion battery	V_{BUB} rising,T_J = -20°C ~ 85°C	2.1	2.2	2.3	V
V_{BUB_SHORT}	BUB short circuit voltage rising threshold, per cell for LiFePO4 battery	V_{BUB} rising,T_J = -20°C ~ 85°C	1.1	1.2	1.3	V
$V_{BUB\_SHORT\_HYS}$	Hysteresis			170		mV
I_{SHORT}	BUB short current			15		mA
V_{BUB_LOWV}	Pre-charge to fast-charge transient threshold, per cell for Li-ion battery	V_{BUB} rising,T_J = -20°C ~ 85°C	2.7	2.8	3	V
V_{BUB_LOWV}	Pre-charge to fast-charge transient threshold, per cell for LiFePO4 battery	V_{BUB} rising,T_J = -20°C ~ 85°C	1.9	2	2.1	V
$V_{BUB\_LOWV\_HYS}$	Hysteresis, per cell	V_{BUB} falling		100		mV
$I_{precharge}$	Precharge current	I_{CC} = 100mA		30		mA
V_{RECHG_HYS}	Battery recharge threshold, per cell for Li-ion battery	V_{BUB} falling, V_{BUB_CV} - V_{BUB}, T_J = -20°C ~ 85°C	50	100	200	mV

T_J = -40°C to 150°C, V_{BUB} = 3.6V and V_{OUT} = 12V(LDO charger mode), V_{OUT} = 6.2V(boost mode). Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RECHG_HYS}	Battery recharge threshold, per cell for LiFePO4 battery	V_{BUB} falling, V_{BUB_CV} - V_{BUB} , T_J = -20°C ~ 85°C	150	200	285	mV
V_{RECHG_HYS}	Battery recharge threshold, per cell for supercap	V_{BUB} falling, V_{BUB_CV} - V_{BUB}, V_{BUB} = 2.5 V, T_J = -20°C ~ 85°C	110	150	200	mV
V_{CHG_NiMH}	Battery charge threshold, per cell for NiMH battery	T_J = -20°C ~ 85°C	1.31	1.34	1.365	V
V_{BUB_OVP}	BUB overvoltage threshold for Li-ion / LiFePO4 / Supercap	Rising, As percentage of V_{BUB} , T_J = -20°C ~ 85°C	101	104	106	%
V_{BUB_OVP}	BUB overvoltage threshold, per cell for NiMH battery	Rising,T_J = -20°C ~ 85°C	1.65	1.7	1.75	V
$t_{CHARGING}$	Charging timer accuracy		7	8	9	hr
t_{SAFETY}	Safety timer accuracy		9	10	11.5	hr
$t_{ON\_INTERMITTENT}$	On time in intermittent charge			2		s
$t_{OFF\_INTERMITTENT}$	Off time in intermittent charge			58		s
BATTERY-PACK NTC MONITOR						
I_{TS_BIAS}	TS nominal bias current	T_J = -20°C ~ 85°C	35.5	38	40	uA
V_{COLD}	Cold temperature threshold	TS pin voltage rising (approx. 0°C)	0.99	1.04	1.09	V
	Cold temperature exit threshold	TS pin voltage falling (approx. 4°C)	0.83	0.88	0.93	V
V_{HOT}	Hot temperature threshold	TS pin voltage falling (approx. 45°C)	176	188	200	mV
	Hot temperature exit threshold	TS pin voltage rising (approx. 40°C)	208	220	232	mV
V_{TS_CLAMP}	TS maximum voltage clamp	TS pin open circuit(float)	2.3	2.6	2.9	V
BATTERY HEALTH DETECTION						
$I_{DISCHARGE}$	Discharge current range		0		1.5	A
	Discharge current accuracy	T_J = 25°C	480	500	520	mA
	Discharge current accuracy	T_J = -20°C ~ 85°C	470	500	520	mA
$V_{DISCHARGE\_AVI}$	Discharge current measurement voltage range		0		3.3	V
	Discharge current measurement voltage accuracy	$I_{DISCHARGE}$ = 500mA, ratio=2, T_J = 25°C	-3.2		3.2	%
	Discharge current measurement voltage accuracy	$I_{DISCHARGE}$ = 500mA, ratio=2, T_J = -20°C ~ 85°C	–4		4	%
V_{BUB_AVI}	BUB voltage measurement range		0		3.3	V
	BUB voltage measurement accuracy	T_J = -20°C ~ 85°C, ratio = 0.5	-0.3		0.15	%
		T_J = -20°C ~ 85°C, ratio = 1	-0.1		0.1	%
V_{TEMP_AVI}	BUB temperature measurement range		0		3.3	V
	BUB measurement accuracy	T_J = -20°C ~ 85°C	-0.4		0.6	%
LOGIC INTERFACE						
V_{I2C_IO}	IO voltage range for I2C		1.7		5.5	V
V_{I2C_H}	I^2C input high threshold	V_{CC} = 2.7V to 5.5V			1.2	V
V_{I2C_L}	I^2C input low threshold	V_{CC} = 2.7V to 5.5V	0.4			V
V_{EN_H}	EN_BST and EN_CHG logic high threshold	V_{CC} = 2.7V to 5.5V			1.2	V
V_{EN_L}	EN_BST and EN_CHG logic low threshold	V_{CC} = 2.7V to 5.5V	0.4			V
THERMAL PROTECTION						

T_J = -40°C to 150°C, V_{BUB} = 3.6V and V_{OUT} = 12V(LDO charger mode), V_{OUT} = 6.2V(boost mode). Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown	T_J rising		175		°C
T_{SD_HYS}	Thermal shutdown hysteresis			15		°C

5.6 I2C Timing Characteristics

T_J = -40°C to 150°C, V_{CC} = 5 V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C TIMING						
f_{SCL}	SCL clock frequency		100		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	Fast mode plus	0.5			µs
$t_{HD(STA)}$	Hold time (repeated) START condition		260			ns
t_{LOW}	Low period of the SCL clock		0.5			µs
t_{HIGH}	High period of the SCL clock		260			ns
$t_{SU(STA)}$	Setup time for a repeated START condition		260			ns
$t_{SU(DAT)}$	Data setup time		50			ns
$t_{HD(DAT)}$	Data hold time		0			µs
t_{RCL}	Rise time of SCL signal				120	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an ACK bit				120	ns
t_{FCL}	Fall time of SCL signal				120	ns
t_{RDA}	Rise time of SDA signal				120	ns
t_{FDA}	Fall time of SDA signal				120	ns
$t_{SU(STO)}$	Setup time of STOP condition		260			ns
C_B	Capacitive load for SDA and SCL				200	pF

5.7 Typical Characteristics

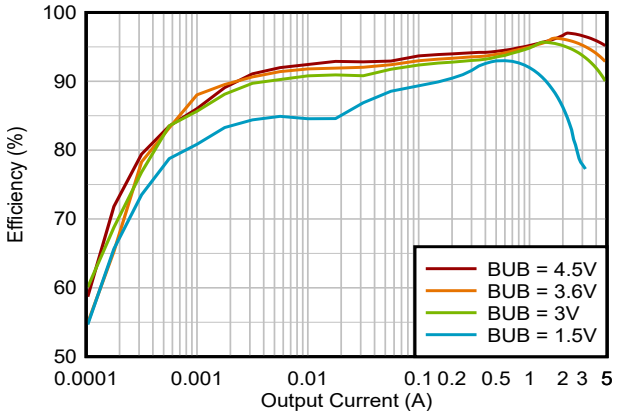


Figure 5-1. Boost Efficiency vs Output Current, V_{OUT} = 6.2V, PFM

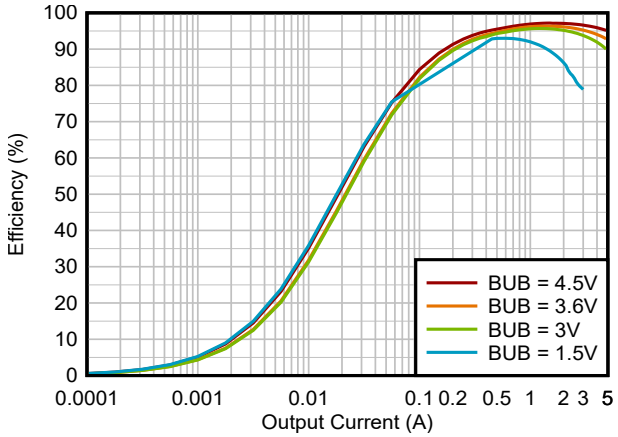


Figure 5-2. Boost Efficiency vs Output Current, V_{OUT} = 6.2V, FPWM

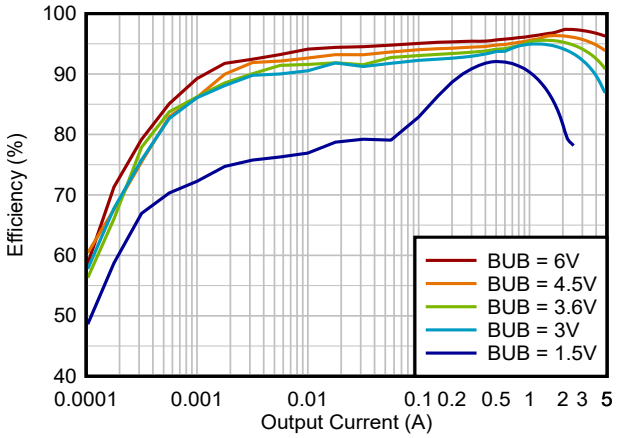


Figure 5-3. Boost Efficiency vs Output Current, V_{OUT} = 8V, PFM

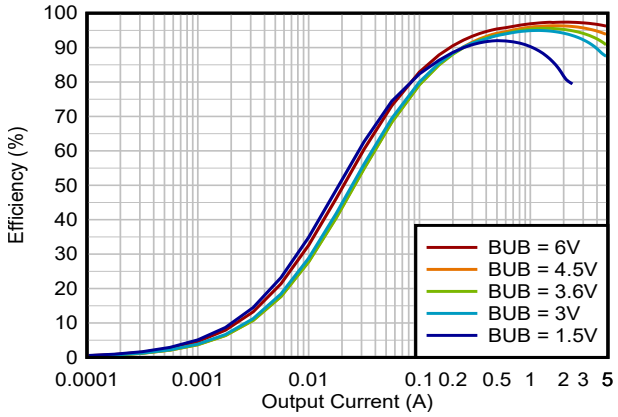


Figure 5-4. Boost Efficiency vs Output Current, V_{OUT} = 8V, FPWM

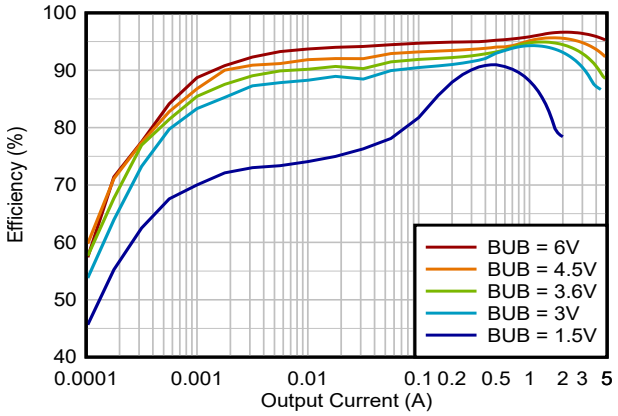


Figure 5-5. Boost Efficiency vs Output Current, V_{OUT} = 10V, PFM

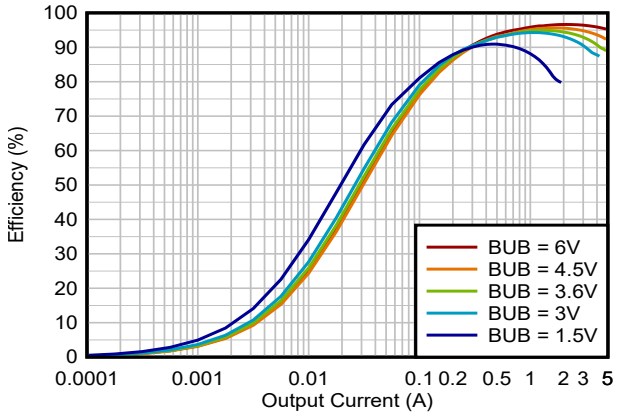


Figure 5-6. Boost Efficiency vs Output Current, V_{OUT} = 10V, FPWM

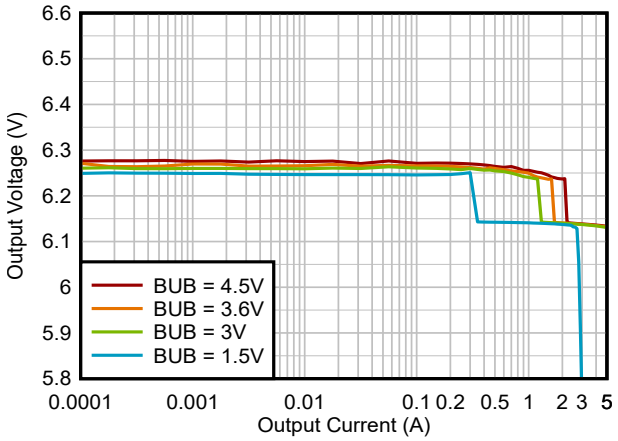


Figure 5-7. Output Voltage vs Output Current, V_{OUT} = 6.2V, PFM

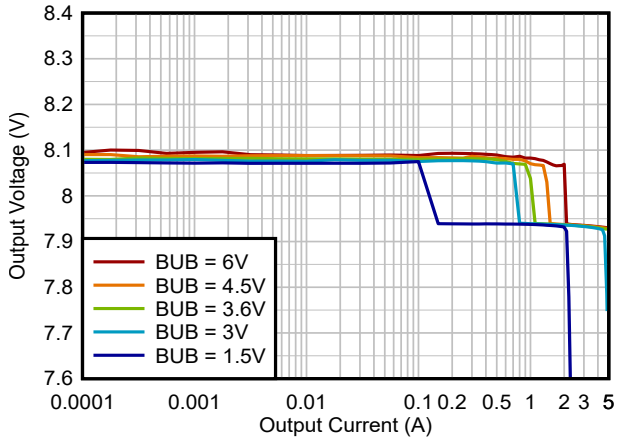


Figure 5-8. Output Voltage vs Output Current, V_{OUT} = 8V, PFM

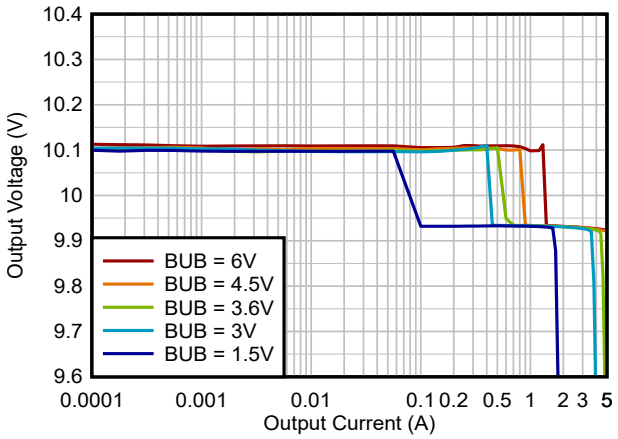


Figure 5-9. Output Voltage vs Output Current, V_{OUT} = 10V, PFM

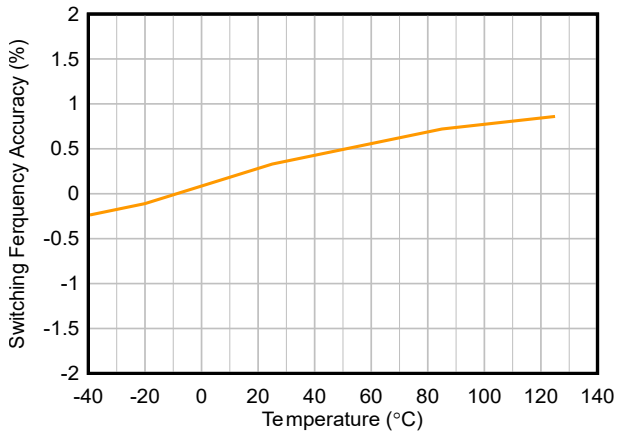


Figure 5-10. Switching Frequency vs Temperature, FPWM, V_{BUB} = 3.6V, V_{OUT} = 6.2V

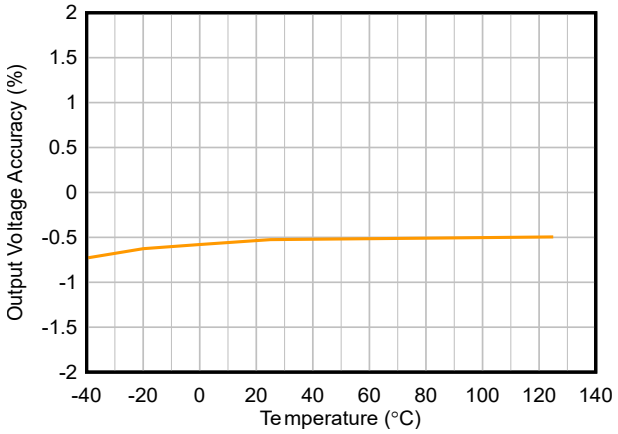


Figure 5-11. Output Voltage Accuracy vs Temperature, FPWM, V_{BUB} = 3.6V, V_{OUT} = 6.2V

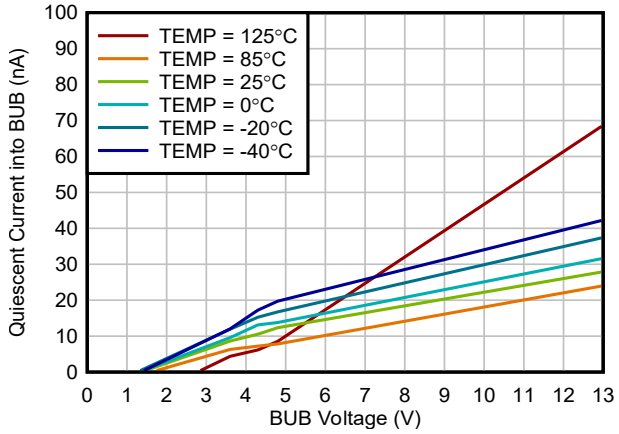


Figure 5-12. Quiescent Current into BUB vs BUB Voltage, V_{OUT} = 12V

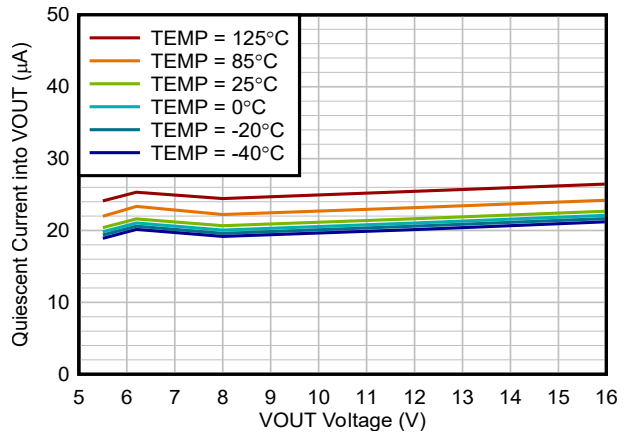


Figure 5-13. Quiescent Current into VOUT vs VOUT Voltage, V_{BUB} = 3.6V

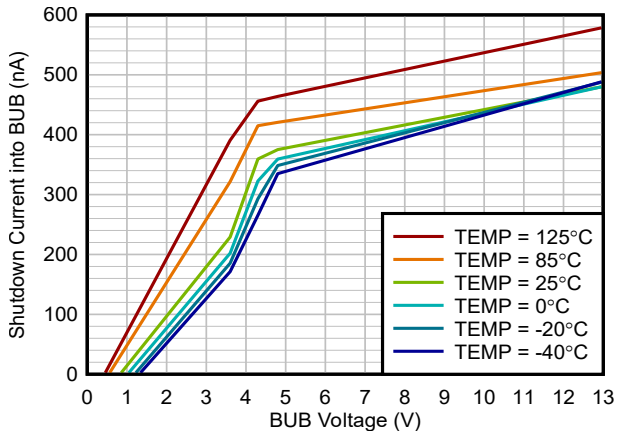


Figure 5-14. Shutdown Current into BUB vs BUB Voltage, V_{OUT} = 12V

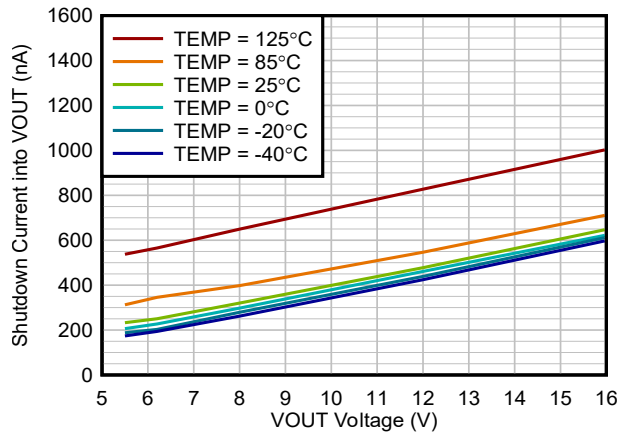


Figure 5-15. Shutdown Current into VOUT vs VOUT Voltage, V_{BUB} = 3.6V

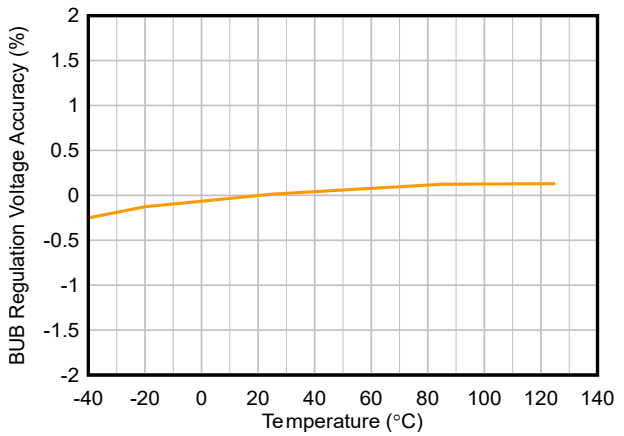


Figure 5-16. Battery Regulation Voltage Accuracy vs Temperature, I_{charge} = 100mA

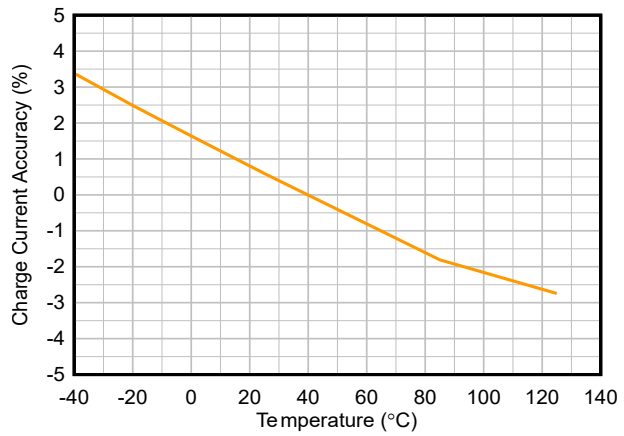


Figure 5-17. Charge Current Accuracy vs Temperature, I_{charge} = 100mA

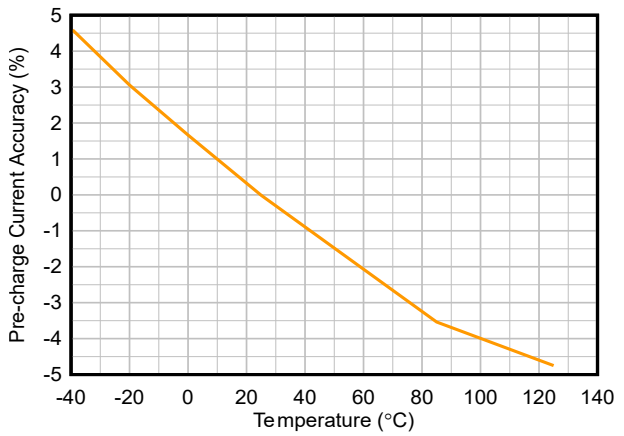


Figure 5-18. Precharge Current Accuracy vs Temperature

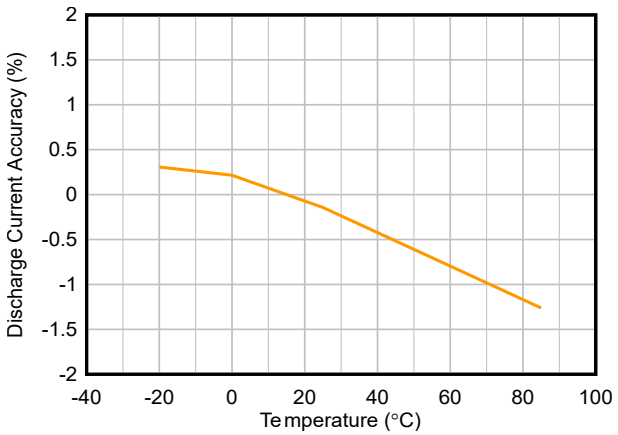


Figure 5-19. Discharge Current Accuracy vs Temperature, $I_{discharge}$ = 500mA

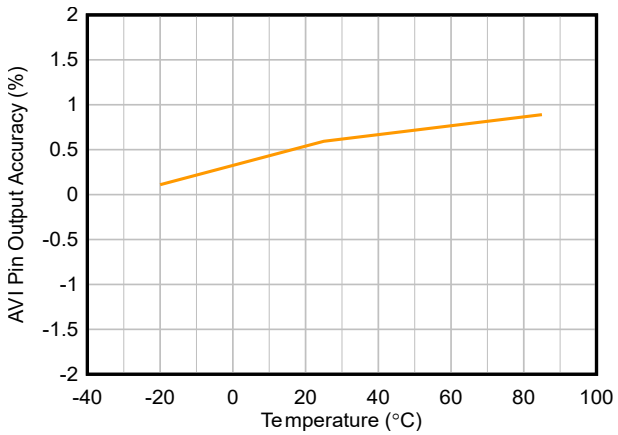


Figure 5-20. AVI Pin Discharge Current Output Accuracy vs Temperature, $I_{discharge}$ = 500mA, Ratio = 2

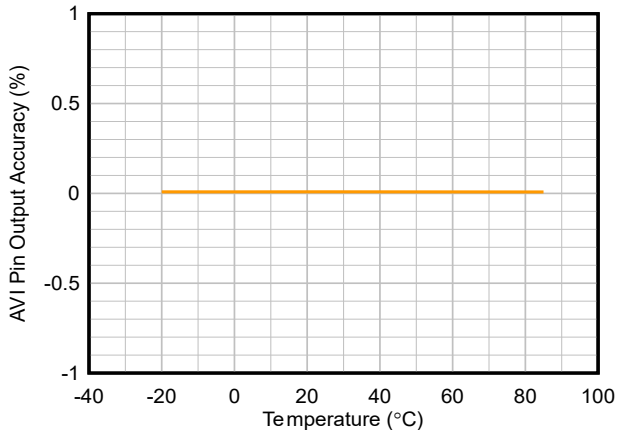


Figure 5-21. AVI Pin BUB Voltage Output Accuracy vs Temperature, Ratio = 1

6 Detailed Description

6.1 Overview

The TPS61381-Q1 is a bi-directional boost converter / LDO charger with battery State-of Health (SOH) detection function. The device provides an integrated power solution in back-up power system like TBOX and e-Call applications. The converter supports 40V voltage rating on VOUT pin to withstand load-dump condition and support direct connection with 12V car battery. The converter supports boost function for back up power system. The IC automaticly switch to boost mode when car battery malfunction occurs and voltage drop on the system side is detected.

The TPS61381-Q1 integrates boost function that operates over a wide range of 0.5V to 13V BUB voltage and 5V to 12V programmable output voltage in boost mode.The device uses fix frequency peak current mode control scheme which provides simplified loop compensation, rapid response to load transients and inherent line voltage rejection. An error amplifier compares the feedback voltage with the internal reference voltage. The output of the error amplifier determines the peak inductor current. The IC also supports 5A-15A selectable average current limit.

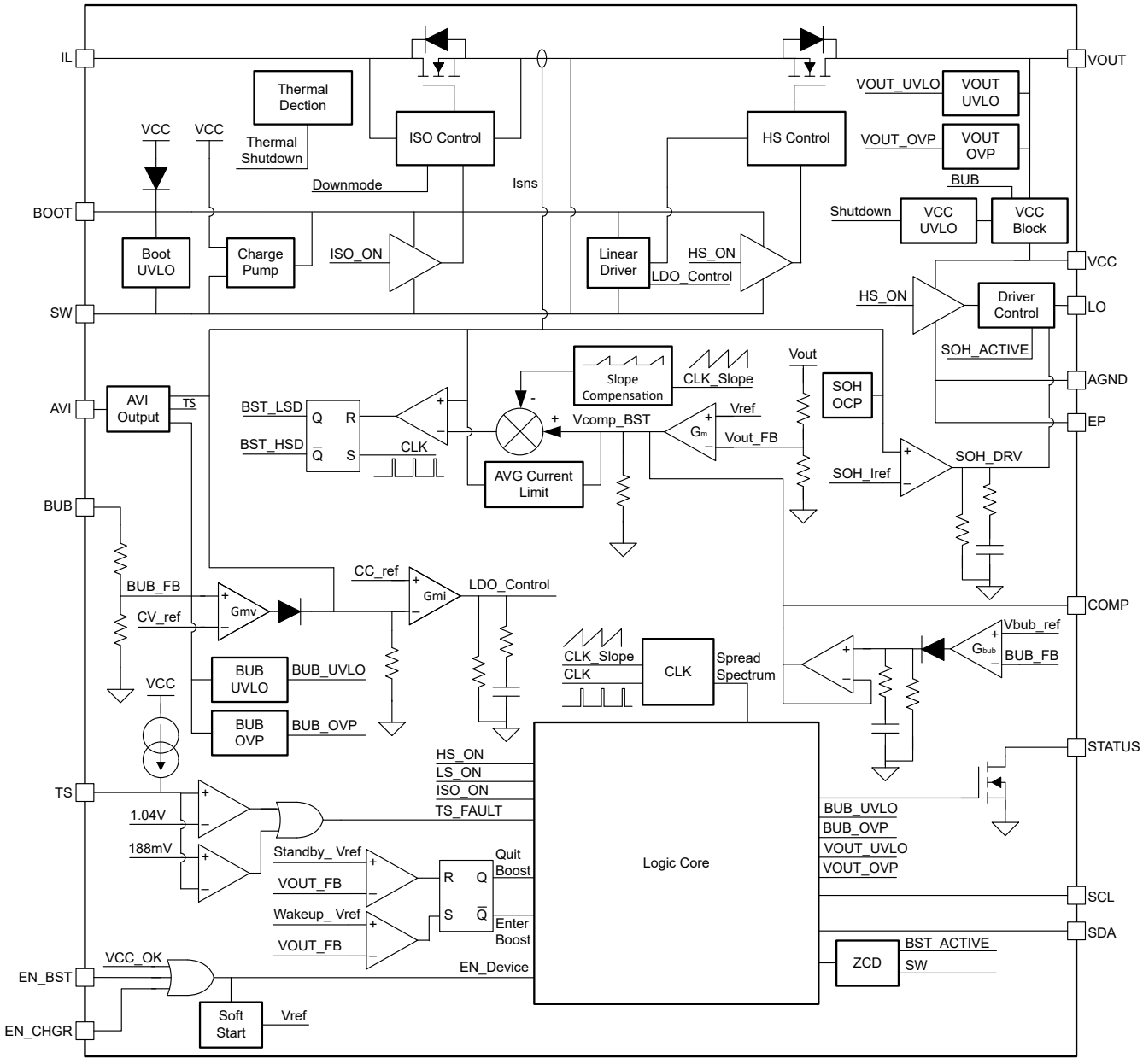
The TPS61381-Q1 integrates an I2C configurable constant-current / constant-voltage (CC/CV) LDO charger to charge the battery. The charger function supports 1 to 5 cell NiMH, 1 to 2 cell Li-Ion, Li-Poly, LiFePO4 and 1 to 4 cell super capacitor. The device supports battery temperature monitor function which connects TS pin to battery NTC to detect battery temperature and pauses charging when high/low temperature is detected.

The TPS61381-Q1 integrates battery State-of Health (SOH) detection feature which discharge the battery with a constant current and detect the voltage drop across the battery internal resistance. By controlling back-up battery discharge current by I2C interface and output the detected BUB voltage to MCU. The MCU can calculate the internal resistance and diagnostic the battery health.

An internal oscillator operates with fixed 400kHz and provide clock for the IC switching cycle. To minimize EMI, TPS61381-Q1 can dither the switching frequency at ±7% of the 400kHz switching frequency.

The TPS61381-Q1 is available in a 3mm × 4mm QFN package with wettable flank.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 VCC Power Supply and UVLO Logic

An internal VCC_LDO sinks current from either BUB or VOUT pin to power VCC to 5.2V target depending on BUB and VOUT voltage and operating mode. The IC is enabled only when at least one of its EN pins is high and VCC voltage>2.8V.

A ceramic capacitor is connected between the VCC pin and AGND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The effective capacitance of this ceramic capacitor should be above 1µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3V is recommended.

TPS61381-Q1 applies undervoltage lockout (UVLO) logic on BUB, VOUT and VCC pin depending on different operating mode. Sufficient voltage must be applied to ensure proper function of the IC.

Table 6-1. UVLO Logic

Operating Mode	VBUB	VOUT	VCC
Boost Mode	>V_{BUB_UVLO}	>0V	>2.8V
Charger Mode	>0V	>V_{VOUT_UVLO}	>2.8V
SOH Mode	>0V	>V_{VOUT_UVLO}	>2.8V
Standby Mode	>0V	>V_{VOUT_UVLO}	>2.8V

6.3.2 Enable or Shutdown

TPS61381Q applies two EN pins to configure operating modes of the device. The I2C interface function can be enabled by either EN_BST pin or EN_CHGR pin. After device enabled, the device enters its operating mode depending on EN pins, I2C configuration and VOUT voltage. Check Section 6.3.3 for details about operation modes.

Table 6-2. Enable or Shutdown Logic

EN pins configuration	I2C EN bits configuration	Device State	I2C Interface	Device Current Consumption
EN_CHGR pin = 0 AND EN_BST pin = 0	X	Shutdown	Disabled Register Reset	<1µA(typ)
EN_CHGR pin = 1 AND EN_BST pin = 0	CHGR_SOH_EN bit = 00b	Standby	Enabled	20µA(typ)
EN_CHGR pin = 0 AND EN_BST pin = 1	CHGR_SOH_EN bit = 00b	Standby	Enabled	20µA(typ)
EN_CHGR pin = 1	CHGR_SOH_EN bit = 01b/10b	Device Active	Enabled	According to working condition
EN_BST pin = 1	BST_EN bit = 1	Device Active	Enabled	According to working condition

When TPS61381-Q1 is disabled by EN pin (EN_BST=0 AND EN_CHGR=0), the device is completely Shutdown. Under shutdown state, the device consumes less than 1µA shutdown current, I2C registers are reset to default and I2C interface is disabled. When the device is disabled by EN bit (BST_EN = 0 AND CHGR_SOH_EN = 0), the device enters standby state. Current consumption under this state is 20µA, I2C register contents are kept and I2C interface is active.

During shutdown and standby state, TPS61381-Q1 supports true disconnection function and the back up battery is completely disconnected from the output.

6.3.3 Device Operating Modes and Control Logic

TPS61381-Q1 supports four operating modes for its main functions: charger mode, boost mode, State-of-Health (SOH) mode and standby mode. The power structure of each modes are depicted by figures below:

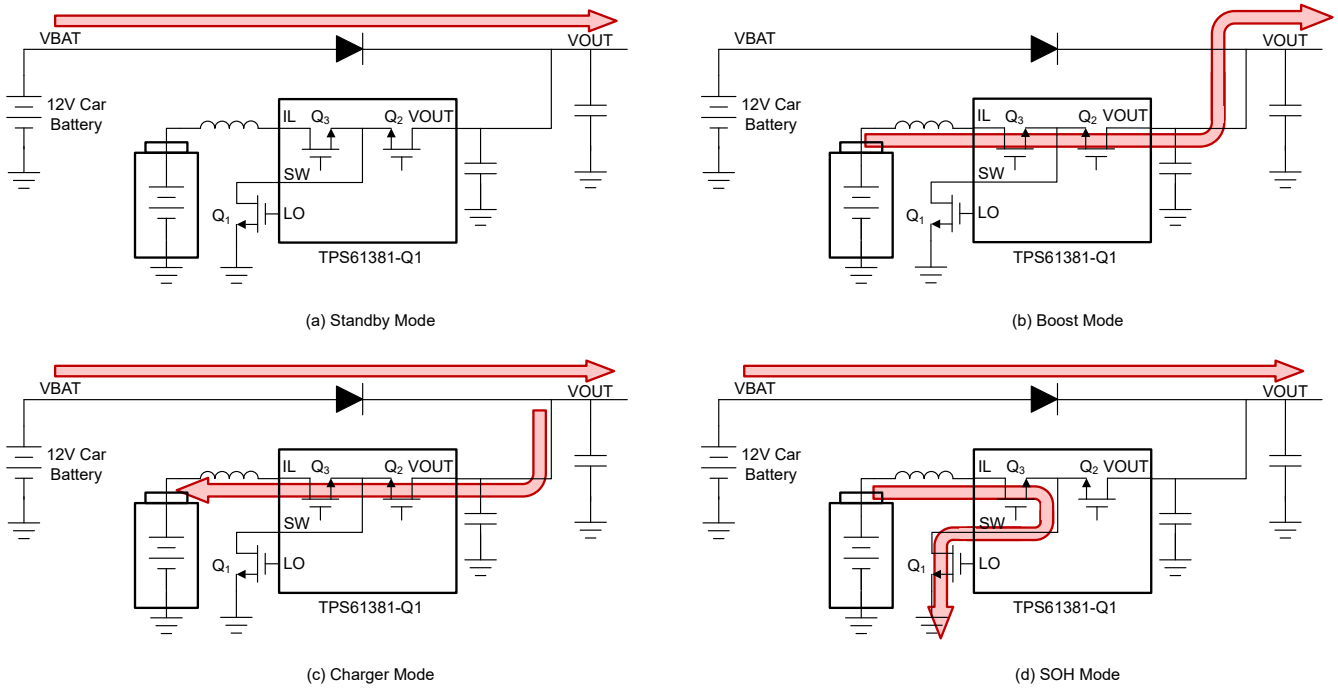


Figure 6-1. TPS61381-Q1 Operating Modes

TPS61381-Q1 applies AND logic on its EN pins and I2C EN bits. The boost function is enabled when EN_BST pin and BST_EN bit is both high. Charger is enabled when EN_CHGR pin is high and CHGR_SOH_EN bit is 01b. SOH is enabled when EN_CHGR pin is high and CHGR_SOH_EN bit is 10b.

Table 6-3. Operating Modes Control Logic

Boost enable: EN_BST pin AND BST_EN bit	Charger/SOH enable: EN_CHGR AND CHGR_SOH_EN bit	Device State	Device Operation
EN_BST = 0 or BST_EN = 0	EN_CHGR = 1 and CHGR_SOH_EN = 01b	Pure charger	Charger Active.
EN_BST = 0 or BST_EN = 0	EN_CHGR = 1 and CHGR_SOH_EN = 10b	Pure SOH	SOH Active.
EN_BST = 1 and BST_EN = 1	EN_CHGR = 0 or CHGR_SOH_EN=00b	Automatic boost and standby	• Boost Active: V_{OUT} < BST_WAKE • Standby Active: V_{OUT} > $V_{OUT\_STANDBY}$(106%V_{OUT_TARGET})
EN_BST = 1 and BST_EN = 1	EN_CHGR = 1 and CHGR_SOH_EN = 01b	Automatic boost and charger mode	• Boost Active: V_{OUT} < BST_WAKE • Charger Active: V_{OUT} > $V_{OUT\_STANDBY}$(106%V_{OUT_TARGET})
EN_BST = 1 and BST_EN = 1	EN_CHGR = 1 and CHGR_SOH_EN = 10b	Automatic boost and SOH mode	• Boost Active: V_{OUT} < BST_WAKE • SOH Active: V_{OUT} > $V_{OUT\_STANDBY}$(106%V_{OUT_TARGET})

When multiple functions are enabled, TPS61381-Q1 monitors system voltage by VOUT pin to decide which function mode to enter. The IC stays in standby/ charger or SOH mode (depending on which function is enabled) when system voltage is sufficient and automatically transition into boost mode when car battery malfunction occurs and voltage drop on system voltage is detected. The different operation modes are shown in the Functional State Diagram.

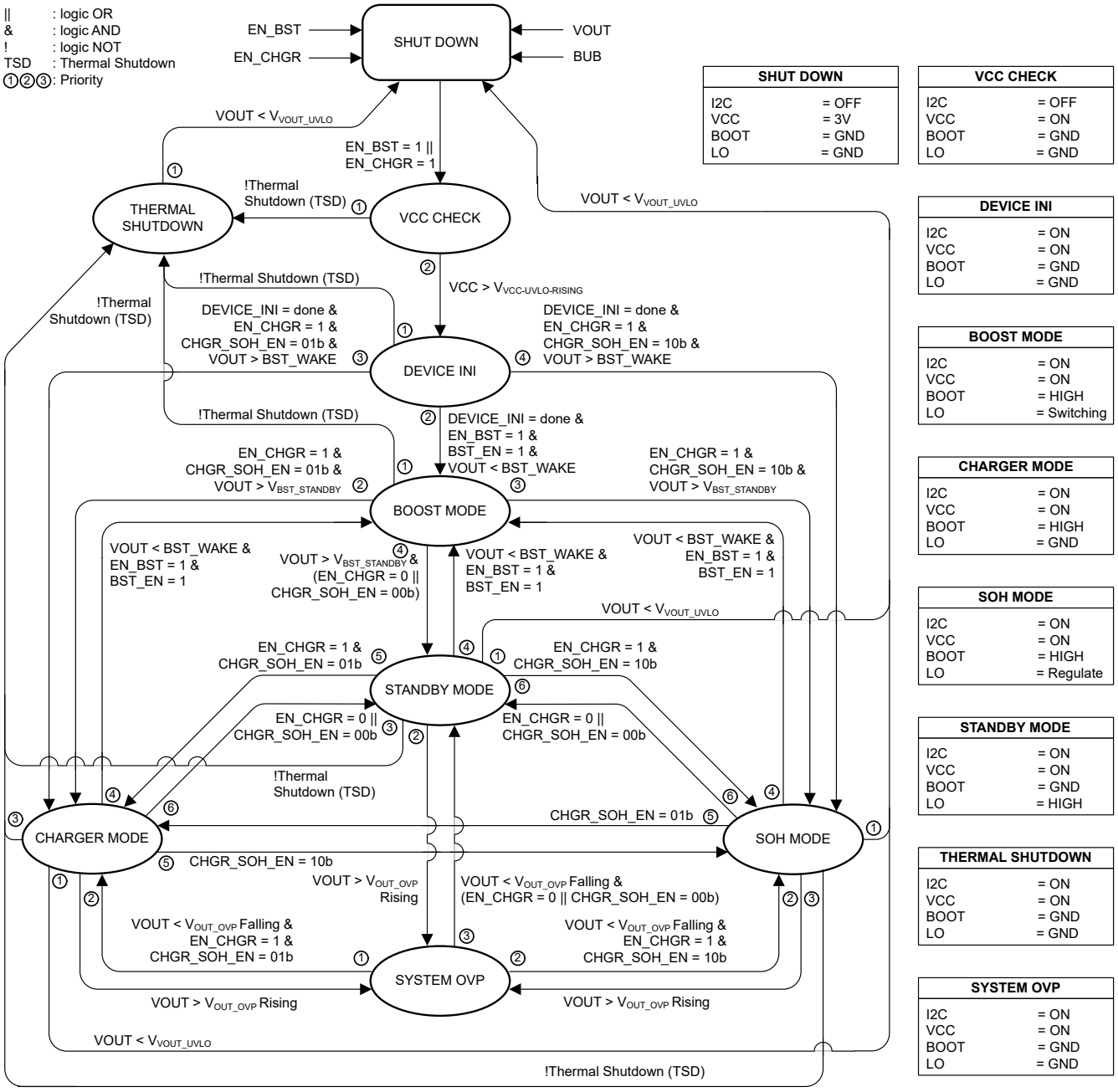


Figure 6-2. Functional State Diagram

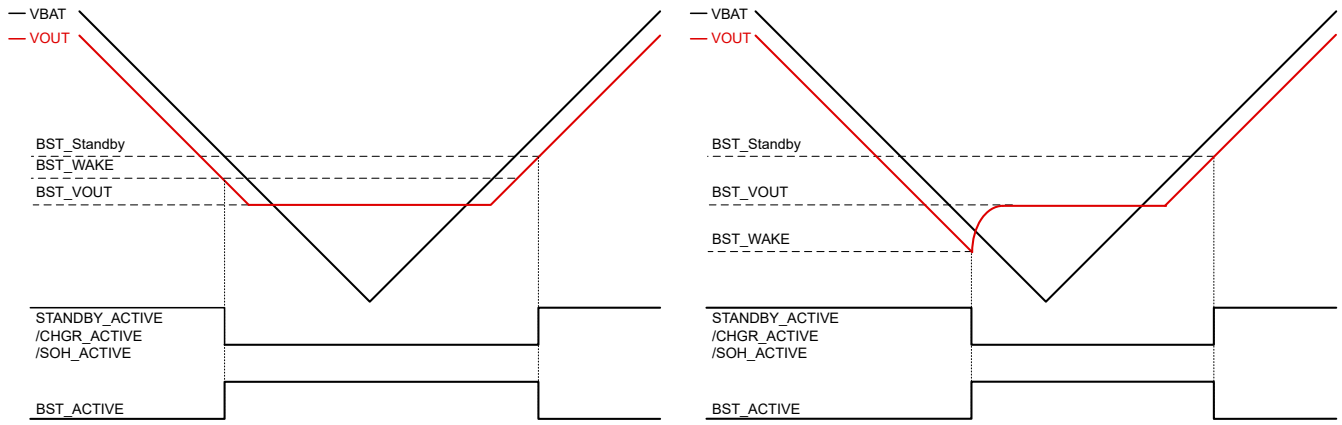


Figure 6-3. Automatic Boost and Standby/Charger/SOH Transition Logic

6.3.4 Configured as Status Indicator

TPS61381-Q1 supports status indication function with its STATUS pin. The STATUS pin operates as an open-drain digital output to indicate the IC status or trigger interrupt of your system MCU.

TPS61381-Q1 STATUS pin supports indicating multiple items by configuring I2C register 0DH (Bit 3 to Bit 7). The pin is set to indicate BST_ACTIVE (boost active) status by default. When the device enters boost mode, the STATUS pin is pulled low to indicate a boost active status. The pin can also be configured to output charge done, thermal shutdown or TS fault signal. If multiple status items are selected, the pin output the NOR logic of all items (Pull low if any of the status is triggered).

Table 6-4. STATUS Pin Indication Items

Register 0DH Bit	Selected Item	Discription
[7]	INC_BST	BST_ACTIVE status is included in the STATUS pin. Output low when entering boost mode.
[6]	INC_ABST	ALRT_BST_ACTIVE status is included in the STATUS pin. Output low when boost mode has been entered since last read.
[5]	INC_ADN	ALRT_CHGR_DONE status is included in the STATUS pin. Output low when charge done has been triggered since last read.
[4]	INC_TSD	THRM_SD status is included in the STATUS pin. Output low when thermal shutdown protection is triggered.
[3]	INC_TSFAULT	TS_FAULT status is included in the STATUS pin. Output low when TS pin detects cold/hot temperature over range.

6.3.5 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 175°C (typical). After thermal shutdown occurs, hysteresis prevents the device from toggling until the junction temperature drops to approximately 160°C. When the junction temperature falls below 160°C (typical), TPS61381-Q1 attempts to re-start.

6.4 Charger Feature Description

TPS61381-Q1 integrates LDO charger function with complete charging strategy for mutiple types of back up battery. By setting the battery type, cell number, charging current, charging voltage and charging timer, TPS61381Q automatically applies corresponding charging strategy for the selected battery chemistry.

- Supports mutiple types of back up battery: NiMH(1S 2S 3S 4S 5S), LiFePO4(1S 2S), Li-ion(1S 2S), Super Capcitor(1S 2S 3S 4S)
- Optional charging current: 50mA to 100mA (Selectable by I2C)
- Support charger status indication by I2C interface: Register 08H (CHGR_STATUS)

TPS61381-Q1 supports mutiple safety protection and monitition functions for both battery charging and system operations. Charging safety timer, back up battery overvoltage protection, charger anti-reverse protection and battery cold/hot temperature protections are applied to ensure the battery safety during charger operation. Also, TPS61381Q indicates the charger status and fault condition by CHGR_STATUS and FAULT_CONDITION registers .

6.4.1 Charger Enable

TPS61381-Q1 charger function is enabled when:

- EN_CHGR pin is high
- CHGR_SOH_EN=01b (I2C Register 0BH: CONTROL_STATUS, Bit [6:5])
- VOUT < V_{OUT_OVP}
- VCC > 2.8V

After charger function is enabled, the IC enters charger mode when VOUT > boost wake-up threshold (Set by I2C BST_WAKE bits).

When charger mode is active, TPS61381-Q1 charge the back-up battery (BUB pin). The charger only support step down operation. So if VOUT drops below 100mV+BUB Voltage, the charger turn off all power MOSFETs to protect itself.

6.4.2 LDO Charger

TPS61381-Q1 supports LDO charger function with 50mA or 100mA charging current. In charger mode, Q_2 is regulated in saturation region to control the charging current while Q_3 is fully turned on. Please ensure VOUT voltage over 0.6V+BUB Voltage to ensure Q_2 stays in saturation region.

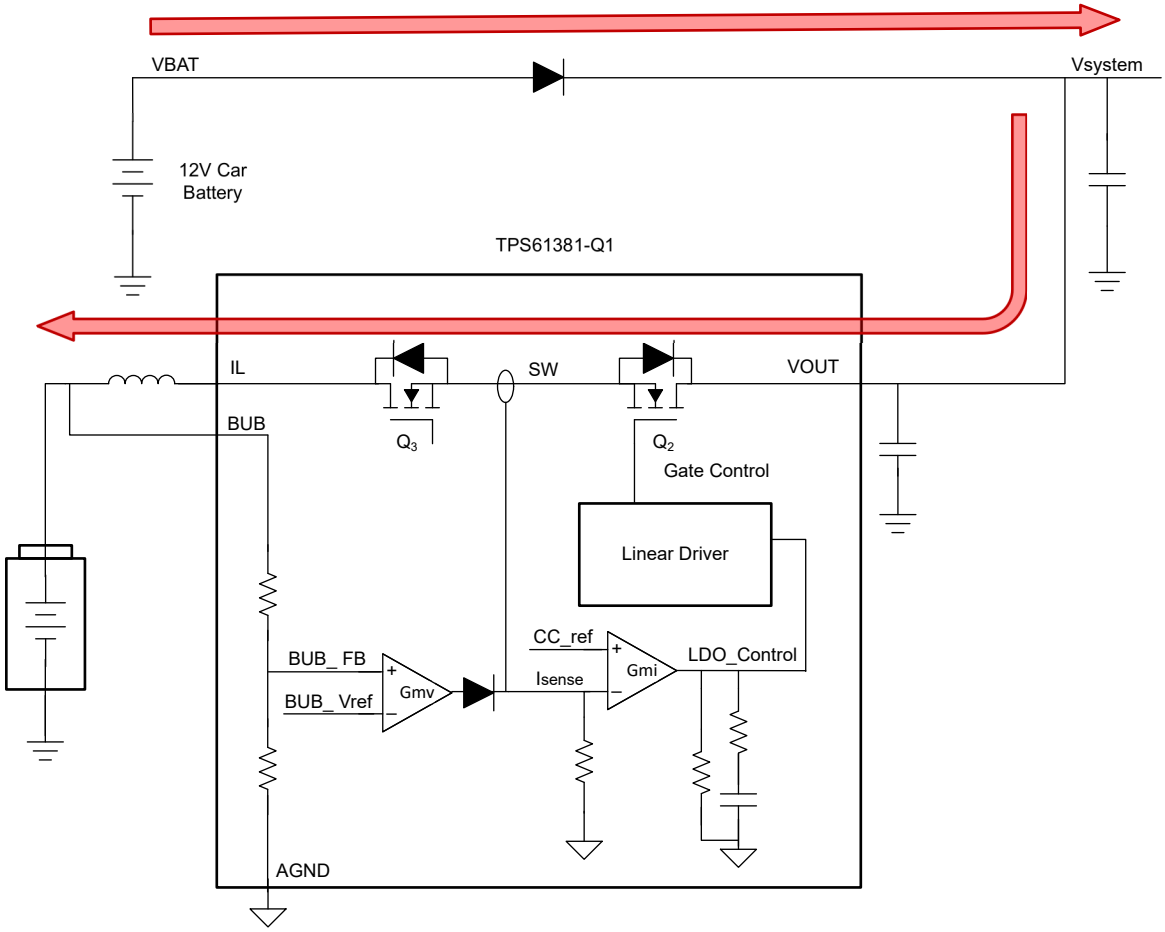


Figure 6-4. Linear Charger Structure

TPS61381Q supports multiple battery chemistry including NiMH battery, Li-ion battery, LiFePO4 battery and super capacitor. By setting I2C BUB_TYP bits (Register 04H: CHGR_SET1 bit [6:7]), TPS61381Q charges back up battery with the integrated charging profile for the selected battery type.

6.4.3 NiMH Battery Charging Profile

In NiMH charging mode, TPS61381-Q1 charges batteries with a time-controlled charging profile consisting of two phases: continuous charge and intermittent charge (optional).

Before initiating a NiMH charging cycle, the device checks the battery status. If back up battery voltage (VBUB) is above 1.34V*cell number (Set by I2C bit BUB_CELL, Register 05H: CHGR_SET2), the device consider back up battery as fully charged. The device does not start charging and I2C CHG_DONE bit (Register 08H: CHGR_STATUS) sets 1 to indicate that the charging cycle is done.

If the initial back up battery voltage is below 1.34V×cell number, TPS61381Q enters continuous charge phase. The back up battery is charged with constant current controlled by a pre-set timer. Charging current and the duration for continuous charging phase can be programmed by I2C interface (Register 04H to 05H: BUB_CC, BUB_NIMH_TIMER). After timer is done and the continuous charge phase finishes, TPS61381-Q1 sets I2C bit CHG_DONE bit (Register 08H: CHGR_STATUS) to 1 to indicate the charging cycle is done.

If the re-charge function is disabled (Set by I2C bit BUB_TER, Register 06H: CHGR_SET3), the IC stops charging after continuous charging phase is finished. User can restart charging by toggling the EN_CHGR pin or I2C CHGR_EN bit, this clears the CHGR_MODE_DONE bit and restart the continuous charge phase.

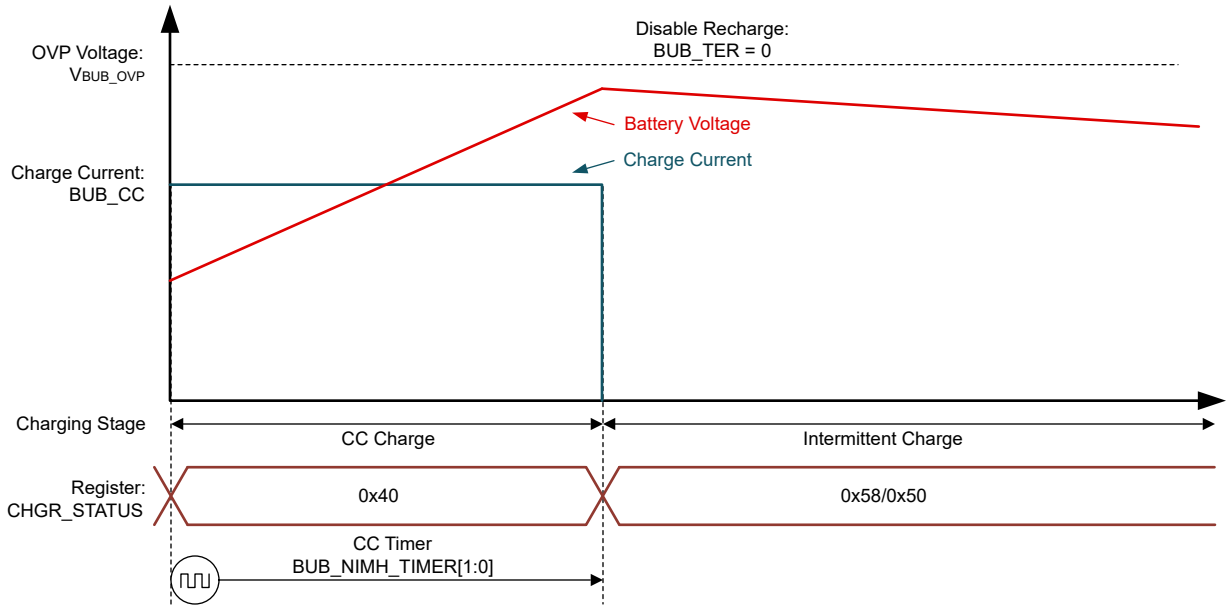


Figure 6-5. NiMH Battery Charging Profile， Re-charge Disabled

If the re-charge is enabled (Set by I2C bit BUB_TER, Register 06H: CHGR_SET3), the device enters intermittent charging phase after continuous charging phase is finished. In this phase, the IC replenishes the natural self-discharge of NiMH by charging the battery intermittently with pulse charge cycle (2s on and 58s off).

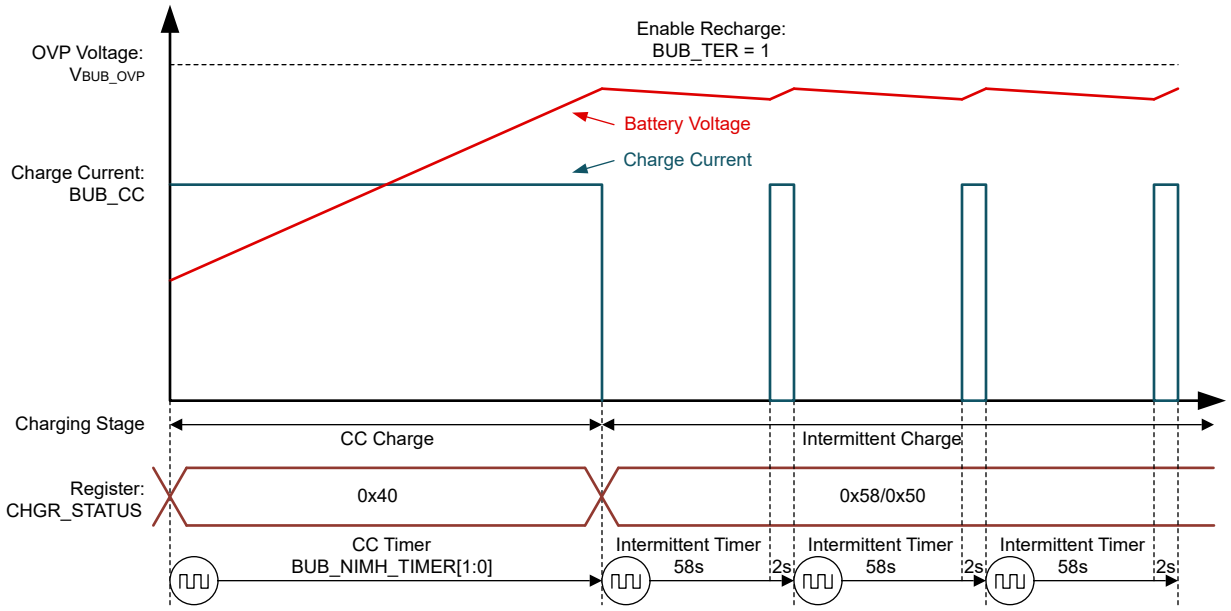


Figure 6-6. NiMH Battery Charging Profile， Re-charge Enabled

TPS61381-Q1 monitors the battery voltage during all charging phases, if the battery voltage is above 1.70V×cell number, the device stops charging and set I2C bit BUB_OVP (Register 0CH: FAULT_CONDITION) to 1 to indicate a overvoltage protection.

6.4.4 Lithium Battery Charging Profile

In Lithium charging mode, TPS61381-Q1 charges batteries with a voltage-controlled charging profile consisting of four phases: trickle charge, pre-charge, CC charge and CV charge.

When the back up battery voltage is below V_{BUB_SHORT} threshold, the device enters trickle charge phase. In this phase, the device charges the battery by 12.5mA to ensure safety of the Lithium battery.

When the battery voltage is charged to V_{BUB_SHORT} threshold but still below V_{BUB_LOWV} threshold , the device enters pre-charge phase. In this phase, the device charges the battery with 20% of the CC current set in I2C BUB_CC bits (Register 05H: CHGR_SET2). Lithium battery within this voltage range is considered as normal but low battery, so charging current is limited at 20% of CC current to protect battery life.

If the battery voltage does not reach V_{BUB_LWV} threshold within 30 minutes. The battery is considered damaged and internal short-circuit. The IC terminates charging and I2C bit BUB_SHORT (Register 0CH: FAULT_CONDITION) is set to 1 to indicate a battery short situation.

After battery voltage reaches VBUB_LOWV threshold, the device enters CC charge phase. In this phase, the device charges the battery by CC current (Set by I2C Register 05H: CHGR_SET2, BUB_CC bits).

After battery is charged to its target voltage (Set by I2C bits BUB_CV and BUB_CELL), TPS61381-Q1 enters CV charge phase. The device decrease charging current to regulate battery voltage until the charging current drops below termination threshold I_{TERM}(Set by Register 06H: CHGR_SET3, CHG_TEM_CURRENT bit), then the device terminate charging.

If configured as recharge disabled (By I2C bits BUB_TER), the device does not re-charge after terminated unless the EN_CHGR pin or CHGR_EN bit is toggled.

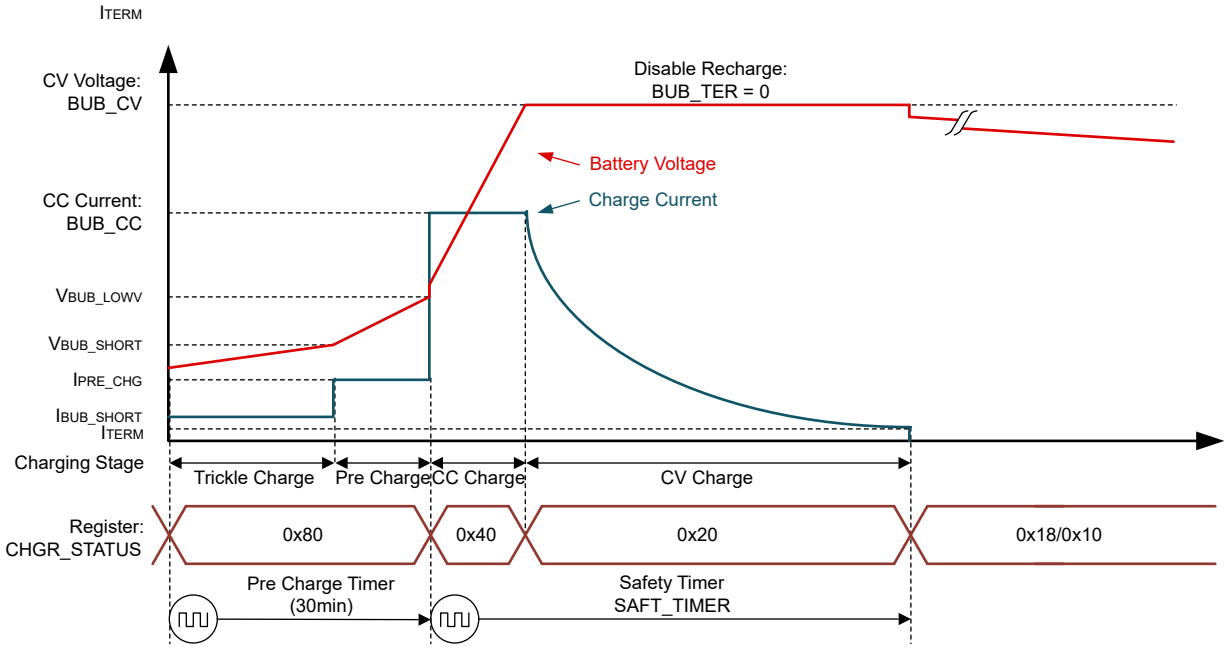


Figure 6-7. Lithium-based Battery Charging Profile, Re-Charge Disabled

If configured as recharge enabled, the device pause charging temporary and automatically re-charge when BUB voltage drops below V_{RECHG} threshold.

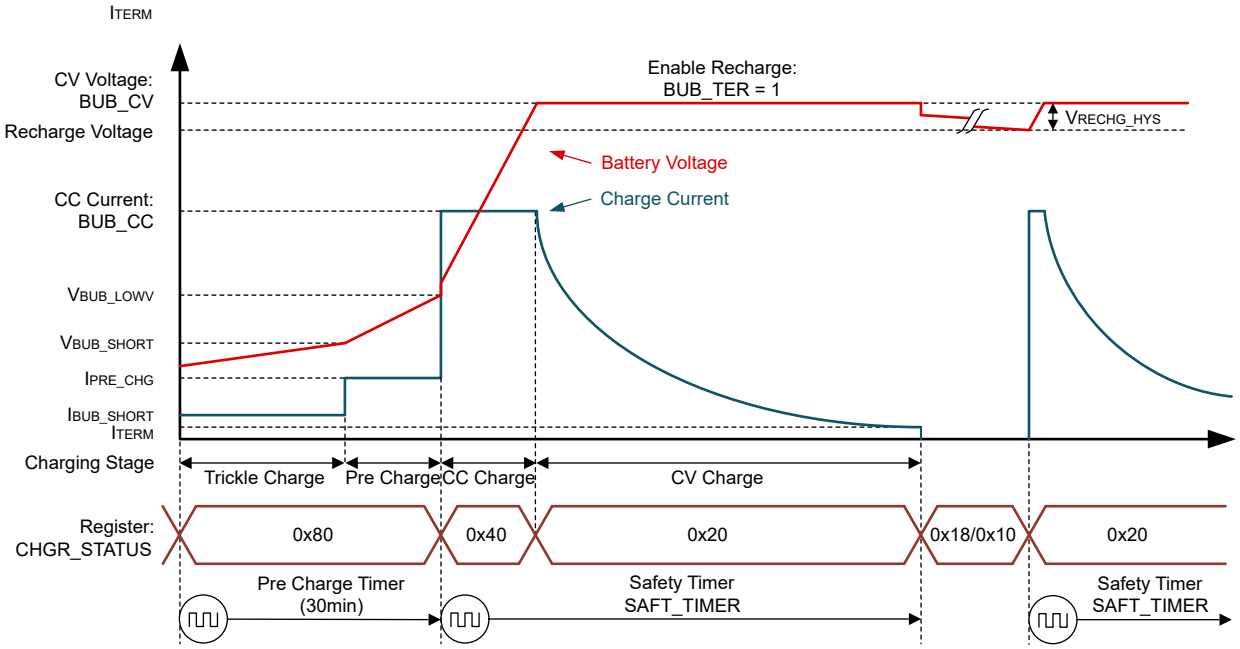


Figure 6-8. Lithium-based Battery Charging Profile, Re-Charge Enabled

6.4.5 Super Capacitor Charging Profile

In super capacitor charging mode, TPS61381-Q1 charges batteries with a voltage-controlled charging profile consisting of two phases:CC Charge, CV Charge.

When the back up super capacitor voltage is below target voltage (Set by I2C bits BUB_CV and BUB_CELL) , the device enters CC charge phase. In this phase, the device charges the super capacitor by CC current configured by BUB_CC bits.

After super capacitor is charged to its target voltage, TPS61381-Q1 enters CV charge phase. The device decrease charging current to regulate the super capacitor voltage until the current drops below a pre-set threshold, then the device terminate charging.

If configured as recharge disabled (By I2C bits BUB_TER), the device does not re-charge after terminated unless the EN_CHGR pin or CHGR_EN bit is toggled.

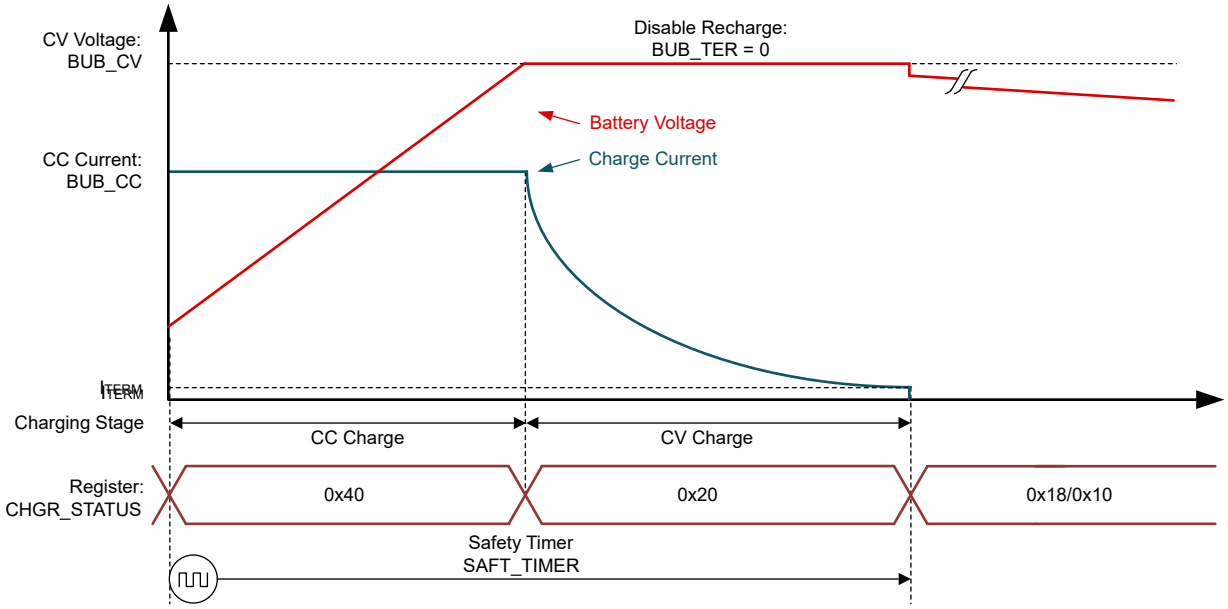


Figure 6-9. Supercap Charging Profile, Re-Charge Disabled

If configured as recharge enabled, the device pause charging temporary and automatically re-charge when BUB voltage drops below V_{RECHG} threshold.

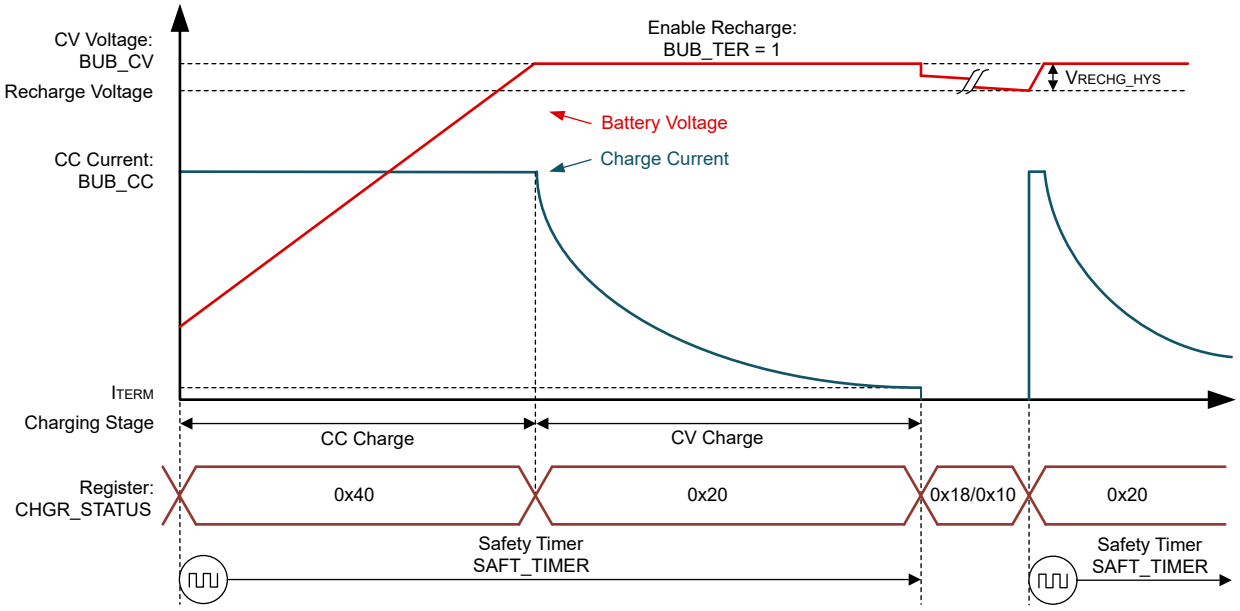


Figure 6-10. Supercap Charging Profile, Re-Charge Enabled

6.4.6 Battery Cold, Hot Temperature (TS Pin)

TPS61381-Q1 supports battery low, high temperature moniting function by sensing the voltage on TS pin. The negative temperature coefficient (NTC) thermistor in battery should be connected within a resistor network (Shown in Figure 6-11). TS pin sources 38uA into the resistor network and generate voltage on TS pin during charger and SOH mode. Battery charging is allowed only when the TS pin voltage stays between V_{COLD} and V_{HOT} thresholds (188mA~1.04V). If the battery temperature exceeds normal range and TS pin voltage becomes outside the thresholds, the device stops charging and set the TS_FAULT bit to 1 (Register 0CH: FAULT_CONDITION). Once battery temperature returns to normal range and TS pin voltage returns between threshold, charging operation resumes automatically.

The temperature window can be modified by the resistance of the resistor network:

$$R_p = \frac{-1.23(R_{HT} - R_{LT}) + \sqrt{0.73(R_{LT} - R_{HT})(R_{LT} - R_{HT} + 24156)}}{7.6 \times 10^{-5} \cdot (R_{LT} - R_{HT}) - 1.704} \quad (1)$$

$$R_s = \frac{1.23(R_{LT} - R_{HT}) + \sqrt{0.73(R_{LT} - R_{HT})(R_{LT} - R_{HT} + 24156)}}{1.704} - 1.22R_{LT} + 0.22R_{HT} \quad (2)$$

Where R_{HT} & R_{LT} are the NTC resistance under your highest & lowest temperature

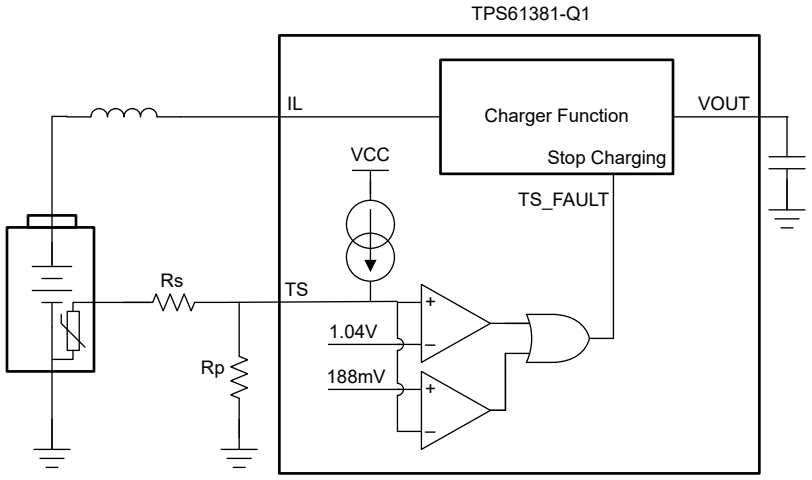


Figure 6-11. TS resistor network for modified temperature window

Taking 103AT-2 as an example, the recommended resistor values for different temperature charging windows are given below:

Table 6-5. Recommended Resistor Values for Different Temperature Charging Windows

TEMPERATURE CHARGING WINDOW	R_S	R_P
0°C to 60°C	2.1kΩ	488 kΩ
−10°C to 60°C	2.5kΩ	70 kΩ
−10°C to 50°C	1.3 kΩ	74 kΩ

If temperature sensing is not required in the application, connect a fixed 10-kΩ resistor from TS to GND to disable temperature sensing and protection.

6.4.7 Charger Protection and Fault Condition Indication

TPS61381-Q1 applies multiple fault protection function to ensure battery life and safety during charging operation. Fault conditions of the charger operation can be monitored through I2C regisiter (Register 0CH: FAULT_CONDITION). When these fault condition occurs, the device pauses charging operation and set the corresponding I2C register bit high to indicate the fault condition.

Fault Item	Description	Fault Indication	Device Behavior
CHGR_RVS	• Charger reverse current protection. • Triggered when V_{OUT} < V_{BUB} + 100mV.	No Flag	• Pause charging • Pause charger timer. • Recover automatically when fault condition is removed
SYSTEM_OVP	• System overvoltage protection fault. • Triggered when V_{OUT} >23V.	Indicated by Register 0CH: FAULT_CONDITION, SYSTEM_OVP bit	
TS_FAULT	• Battery out of cold/hot temperature range • Triggered when TS pin voltage >1.04V or <188mV	Indicated by Register 0CH: FAULT_CONDITION, TS_FAULT bit	
BUB_SHORT	• Battery short-circuit fault for Li-ion/LiFePO4 battery • Triggered when BUB voltage is still <V_{BUB_LOWV} after 30 minutes charging • Only availible for Li-ion and Li-FePO4 battery	Indicated by Register 0CH: FAULT_CONDITION, BUB_SHORT bit	• Stop charging. • Does not recover automatically • Toggle EN_CHGR pin or CHGR_EN bit to reset fault status
BUB_OVP	• Battery over voltage fault • NiMH battery: Triggered when BUB voltage >1.7V per cell • Other battery type: Triggered when BUB voltage is 4% over target voltage	Indicated by Register 0CH: FAULT_CONDITION, BUB_OVP bit	
TIMER_FAULT	• Charger safety timer fault for Li-ion and Li-FePO4 • Triggered when charging time out of safety timer range	Indicated by Register 0CH: FAULT_CONDITION, TIMER_FAULT bit	
THRM_SD	• Thermal shutdown • Triggered when junction temperature >175°C	Indicated by Register 0CH: FAULT_CONDITION, THRM_SD bit	• Pause charging. • Reset charger timer • Recover automatically when fault condition is removed

6.5 Boost Feature Description

The TPS61381-Q1 integrates synchronous boost converter with load disconnect function. The boost function supports input voltage from 0.5V to 13V and output voltage up to 12V with 5-15A programmable average input current limit. The boost function operates with fixed 400kHz switching frequency with optional spread spectrum to achieve EMI performance for automotive applications.

6.5.1 Enable and Start up

TPS61381-Q1 enable its boost function EN_BST pin is high and I2C BST_EN bit is both 1. After boost function is enabled, the TPS61381-Q1 keeps monitoring VOUT voltage and enters boost mode when VOUT drops below wake up voltage threshold.

When entering boost mode, TPS61381-Q1 checkes its BUB pin voltage for undervoltage lockout (UVLO) function. If Vout>2.8V, the UVLO threshold is 1V. If Vout<2.8V, the UVLO threshold is 2.8V. The IC starts boosting only when BUB voltage is over UVLO threshold.

TPS61381-Q1 applies 30us start-up time to ensure its boost can start up quickly when power interruption of your system is detected. So the boost start up current can be up to its input current limit (default 15A). Set I2C current limit to 5A before enable boost if you need a smaller start up current and slower start up.

6.5.1.1 Automatic Transition into Boost Mode

For back-up power application, TPS61381-Q1 detects system voltage with VOUT pin (Connected to your system power rail) and automatically transition into boost mode when a power interruption of your system is detected. Taking automatic boost and standby mode as an example, the device works in standby mode when Vout is normal. When the power failure occurs and Vout drops below than min{V_{BST_WAKEUP}(Set by I2C bits BST_WAKE), $V_{BST\_STANDBY}$ (BST_VOUT ×106%)}, the device enters boost mode to maintain the output voltage.

When the 12V main battery recovers and Vout rises higher than $V_{BST\_STANDBY}$, the device enter standby mode.

The V_{BST_WAKEUP} is configured to BST_VOUT ×103% (BST_WAKE = 111b) by default to achieve smaller voltage drop during transition into boost mode. But TPS61381-Q1 also allows configuring V_{BST_WAKEUP} lower than boost output voltage to avoid entering boost mode at temporary voltage drop like cold crank conditions. User can decide to choose higher V_{BST_WAKEUP} for smaller voltage drop or choose lower V_{BST_WAKEUP} to avoid entering boost mode at cold crank condition and improve back up battery life.

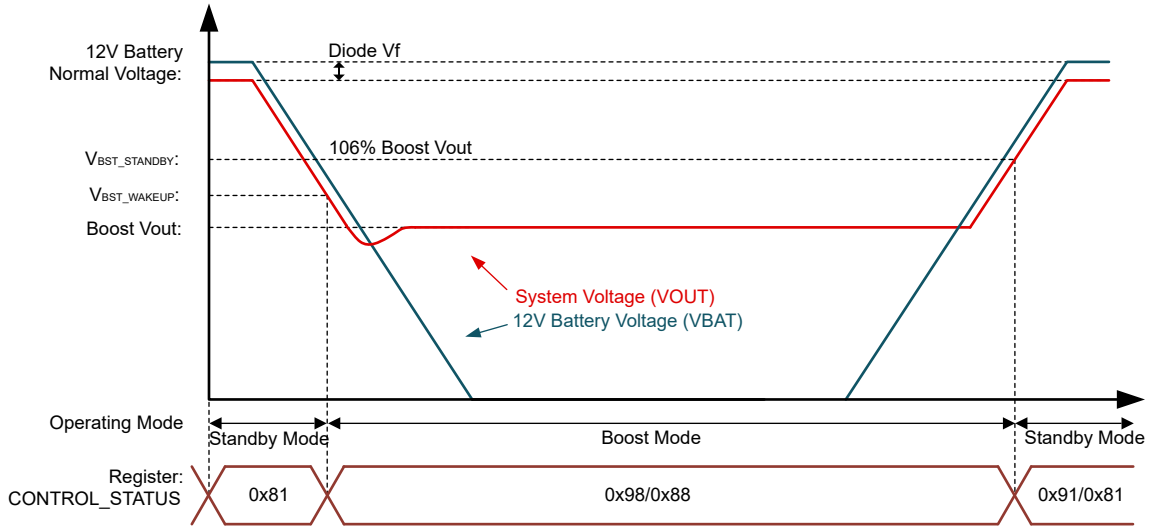


Figure 6-12. Case1: V_{BST_WAKEUP} > BST_VOUT

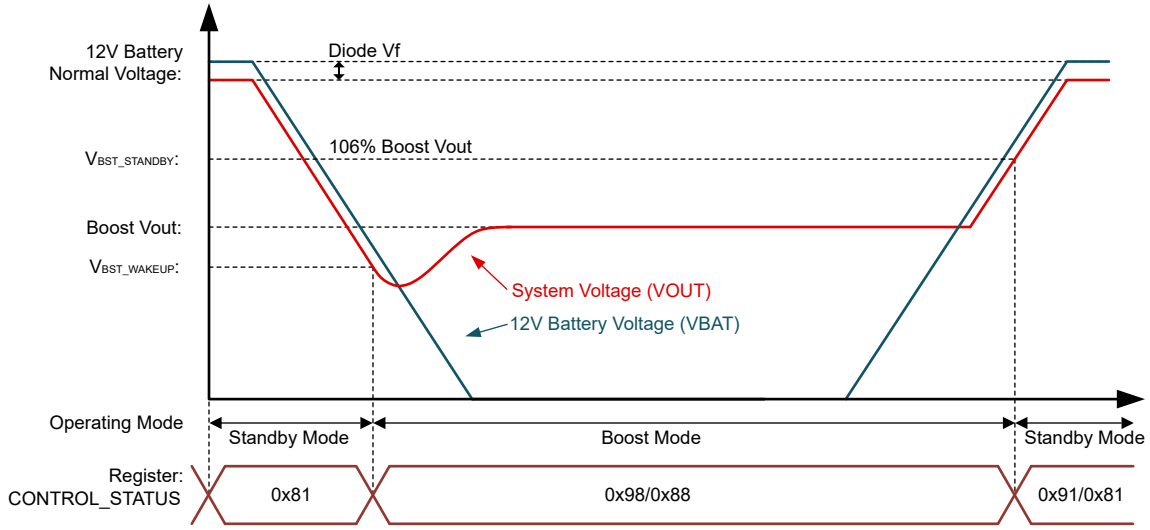


Figure 6-13. Case2: V_{BST_WAKEUP} < BST_VOUT

6.5.1.2 Manual Transition into Boost Mode

TPS61381Q also supports manual transition into boost mode by controlling external EN pins. Manual transition by EN pins allows user to shutdown the IC when 12V battery voltage is normal and saves quiescent current. But external voltage detection circuit and MCU are required to control EN pins.

The device requires 50us(t_{EN_delay1}) delay time to initialize its internal circuit from shutdown mode. After initialized, the device takes about 20µs(t_{EN_delay2}) delay time from standby mode to boost mode.

For back up power applications, TI suggests setting up two threshold to enable our device. Use the $V_{Pre\text{-}WAKEUP}$ threshold to control EN_CHGR pin and initialize the deivce in advance. And use the V_{BST_EN} threshold to control EN_BST pin. This EN sequence can reduce the delay time entering boost mode (Only t_{EN_delay2}).

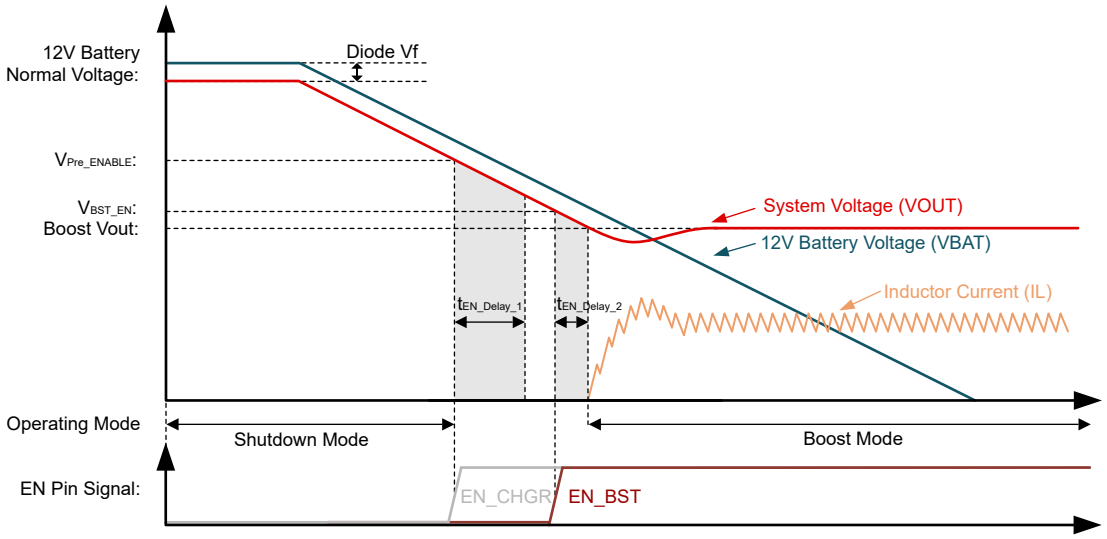


Figure 6-14. Manual Transition into Boost Mode

6.5.2 Down Mode

The TPS61381-Q1 enters down mode when BUB voltage is higher than output voltage during boost mode. During downmode TPS61381-Q1 high-side and low-side FETs works the same way as in boost operation, while the isolation FET Q_3 is regulated in saturation region during high side on phase. This allows the device to regulate its output voltage at target value even when $V_{BUB} > V_{OUT}$.

With its Q_3 operates in saturation region, downmode generates a lot of loss and heat compared to normal boost operation. Therefore current limit threshold is reduced in downmode to avoid overheating. When BUB-VOUT is over 8V, the peak inductor current is limited to 2.33A. When BUB-VOUT is between 4-8V, the peak current limit is 2.95A. When BUB-VOUT is between 0-4V, the peak current limit is 4.41A. Also, because of the high loss and low efficiency, this mode is only for start up and output short protection. Please avoid $V_{BUB} > V_{OUT}$ condition during normal operation.

6.5.3 Output Short- to-Ground Protection

TPS61381-Q1 applies optional output short protection to protect the IC from damage during output short-circuit condition. The short circuit protection is disabled by default and can be enabled by I2C SCP_EN bits. If the output short occurred and the output voltage is pulled below the BUB voltage, the device enters short circuit protection operation in which downmode is applied to control inductor current.

For system safety, TI recommends enabling short circuit protection function.

After SCP_EN bit is enabled and short circuit protection is triggered, TPS61381-Q1 applies peak current limit to protect the IC from overheating. When BUB-VOUT is over 8V, the peak inductor current is limited to 2.33A. When BUB-VOUT is between 4-8V, the peak current limit is 2.95A. When BUB-VOUT is between 0-4V, the peak current limit is 4.41A.

TPS61381-Q1 applies hiccup control for short circuit protection to avoid overheating in downmode, the device keeps switching for 2ms, stopping for 65ms and repeats this cycle to reduce the average current and power consumption.

6.5.4 Boost Control Loop

TPS61381-Q1 applies fix-frequency peak current control scheme, the internal oscillator supports 400kHz switching frequency.

The TPS61381-Q1 operates with fixed-frequency pulse width modulation (PWM) from medium to heavy load. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on. The inductor current ramps up to a peak current that is determined by the output of the internal error amplifier (V_{EA}). Once the switching peak current triggers the output of the EA, the low-side N-MOSFET is turned off and the high-side N-MOSFET is turned on after a short dead time. The high-side N-MOSFET switch is not turned off until the next cycle as determined by the internal oscillator. The low-side switch turns on again after a short dead time and the switching cycle is repeated.

6.5.5 Current Limit Operation

TPS61381-Q1 implements both peak current and average inductor current limit function to protect the device from overload and back up battery from over-discharging. The average current limit can be programmed by I2C BST_ILIM bits.

Besides the average current limit, peak current limit protection is applied to protect the device against overcurrent conditions. In boost operation, the peak current limit threshold is determined by average current limit. With the average current limit set to 5A or 10A, the peak current is limited to 15A, otherwise the peak current is limited to 30A. The peak current limit can enable or disable by I2C BST_ILIM_EN bit. In downmode operation, the peak current limit is reduced depending on VOUT and BUB voltage to avoid IC overheating.

6.5.6 Functional Modes at Light Load

In light load condition, the TPS61381-Q1 can work in either auto PFM or forced PWM (FPWM) mode to meet different application requirements. Auto PFM mode decreases switching frequency under light load. This strategy reduces switching loss and improves higher efficiency at light load condition. FPWM mode force the converter to keep switching with fixed frequency under light load. FPWM improves EMI performance and reduces output ripple, but sacrifices light load efficiency compared to PFM mode.

TPS61381-Q1 is configured to auto PFM mode by default. Write I2C BST_PFM bit (Register 01H, BOOST_SET1) as 1 to switch to FPWM mode.

Care must be taken for back up power applications, FPWM allows reverse current into back up battery when VOUT is higher than boost output target. Reverse current into BUB is usually not favorable for the back up battery. So TI recommend PFM mode during transition into boost mode.

6.5.6.1 Auto PFM Mode

The TPS61381-Q1 can apply auto PFM operation to improve efficiency at light load. Auto PFM mode is applied by enabling the PFM function in the internal register. When the TPS61381-Q1 operates at light load condition, the output of the internal error amplifier decreases to make the inductor peak current down and deliver less power to the load. When the inductor current decreases to I_{CLAMP_LOW} (peak current approximately 4A), the output voltage of the error amplifier is clamped by the internal circuit and does not further reduce. If the load current reduces further, the inductor current is clamped and V_{OUT} will increase. When the output voltage hits the PFM reference voltage (101.5% Vout_target), the device pauses switching. The load is supplied by the output capacitor, and the output voltage declines. When the output voltage falls below 100.5% Vout_target, the device starts switching again to ramp up the output voltage.

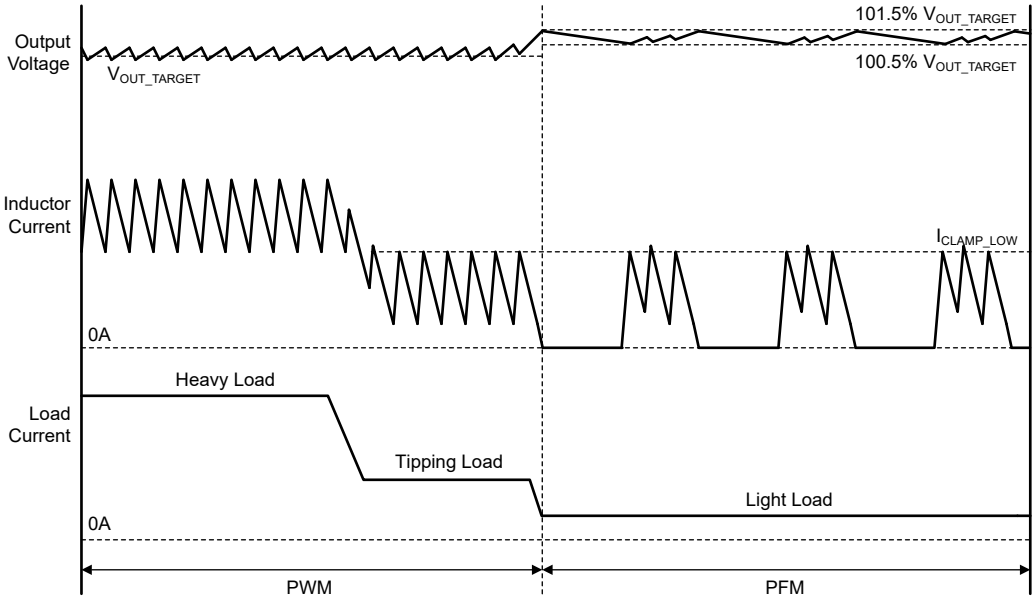


Figure 6-15. PWM and PFM operation

6.5.6.2 Forced PWM Mode

TPS61381-Q1 can also apply force PWM (FPWM) operation to reduce output ripple and improve EMI performance. In the FPWM mode, the TPS61381-Q1 keeps the switching frequency constant in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor current down and deliver less power from input to output. When the output current further reduces, the current through the inductor decreases to zero during the off-time. The high-side MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency is low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

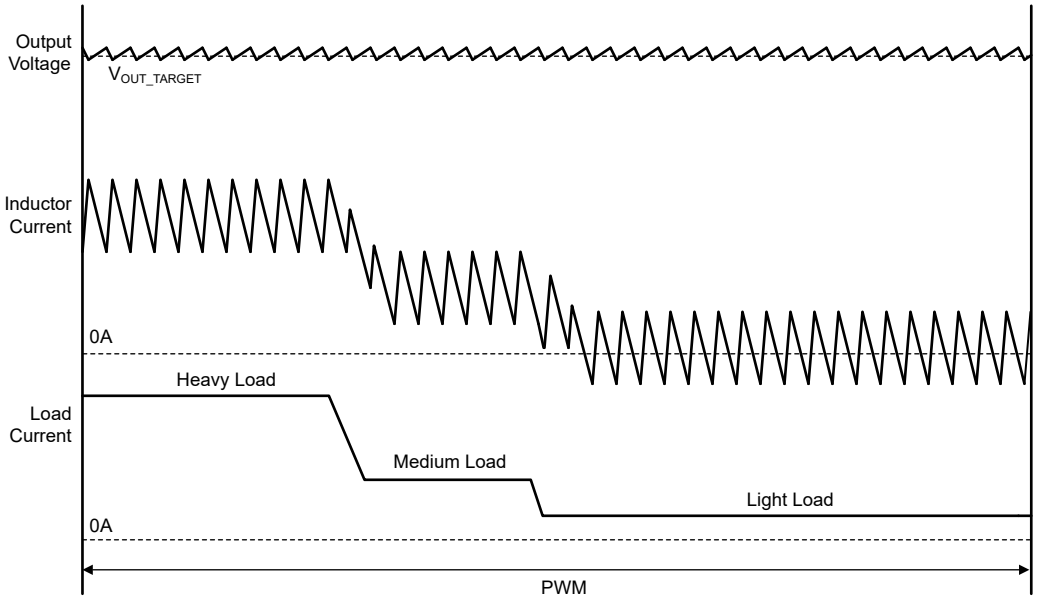


Figure 6-16. PWM and PFM operation

6.5.7 Duty Cycle Limitation

TPS61381-Q1 triggers maximum duty cycle limitation when the low-side MOS off time is about 100ns. When V_{BUB} is too low and the max duty cycle is met, the device clampes its duty and output voltage can not be regulated. So the avilable Vin range is limited by:

$$V_{BUB} < (1 - D_{min})V_{OUT} \quad (3)$$

$$V_{BUB} > t_{OFFmin}V_{OUT}f_{sw} \quad (4)$$

6.5.8 BUB Voltage Loop

The TPS61381-Q1 applies BUB voltage loop to protect back up battery with high internal impedance. like batteries at low battery, cold temperature or the end of its life. This function allows the battery to output its maximum power and maitain its voltage over boost UVLO threshold when the battery has high internal resistance and cannot output enough power for the output. This function is enabled by I2C BST_VINLOOP_EN bits and the input target voltage is programmed by BST_VINLOOP bits.

When the BUB voltage is higher than input target voltage, the BUB voltage loop is not activated. When the BUB voltage is lower than input target voltage, the BUB voltage loop takes over the controlling loop and try decreasing its inductor current to maintain its input voltage. So by allowing the V_{OUT} to drop below V_{OUT_TARGET}, TPS61381-Q1 turns to control its input voltage by which the battery can match its output impedence with internal impedence and output its maximum power.

6.5.9 Spread Spectrum

TPS61381-Q1 implements optional switching frequency dithering for boost function to improve the EMI performance. The device uses a triangle jitter to spread the switching frequency by ±7% . The modulation frequency of the spread spectrum is optional programmable by I2C BST_SS bits.

Table 6-6. Spread Spectrum and Optional Modulation Frequency

BST_SS Bits	Spread Spectrum	Modulation Frequency
00	No Spread Spectrum	No Spread Spectrum
01	±7% Spread Spectrum	6.5 kHz
10	±7% Spread Spectrum	3.2 kHz
11	±7% Spread Spectrum	1.6 kHz

6.6 Battery State-of-Health (SOH) Detection Feature Description

The battery state-of-health (SOH) detection function allows TPS61381-Q1 to detect the internal resistance of the backup battery (BUB). When the EN_CHGR pin is high and CHGR_SOH_EN=10b, the SOH function is enabled. After enabled, the device enters SOH mode when VOUT> wake up voltage.

In SOH mode, the backup battery is discharged by a constant current programmed by I2C SOH_I bits. During the test, the TPS61381-Q1 AVI pin can be configured to output the backup battery's voltage, discharge current and the battery temperature with the ratio selected by I2C. Connect AVI pin to your MCU ADC to acquire and calculate internal resistance.

The ISO FET Q3 is turned on during SOH mode. So TI suggests the output voltage is higher than BUB voltage during SOH operation to avoid inrush current through high side body diode.

6.6.1 SOH Mode Operation

During SOH mode, the TPS61381-Q1 fully turns on its isolation MOSFET Q3 and regulate the gate voltage of the low-side MOSFET Q2 with LO pin. In this way, low side MOSFET operates in saturation area and discharge the back up battery by constant current. TI recommend 500mA discharge current to achieve best accuracy. By sensing the battery open voltage, voltage with discharge current and discharge current, the battery internal resistance R_{bat}can be given by:

$$R_{bat} = \frac{V_{open} - V_{dischg}}{I_{dischg}} \quad (5)$$

where:

- V_{open} is the battery voltage without discharge current
- V_{dischg} is the battery voltage with discharge current
- I_{dischg} is the discharge current

According to the recommendation from battery manufacturer , it is recommened to discharge battery with 500mA I_{dischg} for 500ms and then read V_{dischg}

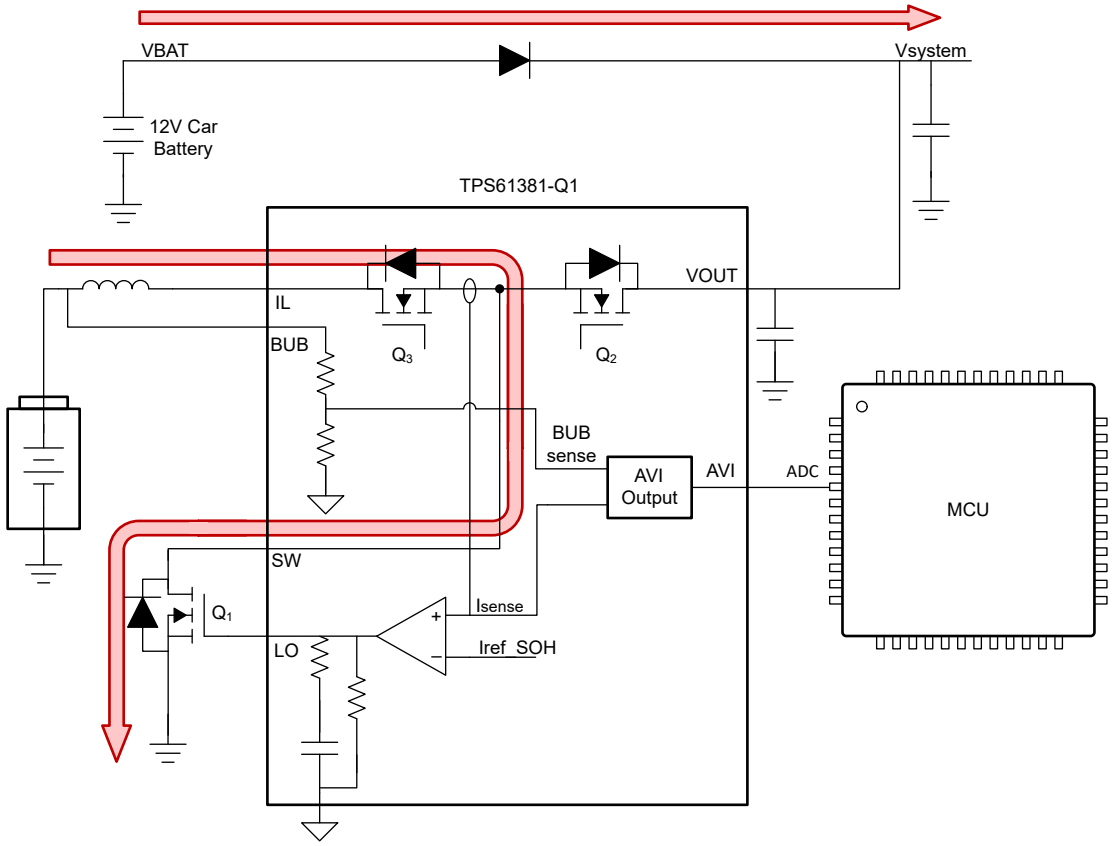


Figure 6-17. Typical Operation of SOH

6.6.2 Multi-Signal Output in AVI Pin

The AVI pin can output three optional signals, battery voltage, battery discharge current and battery temperature. The output item is selected by I2C SOH_AVI_EN bits. So MCU can use one ADC channel to read all signal and help ADC resource can be saved.

The AVI pin voltage is limited to <3.3V to protect MCU ADC pin. The ratio from measured item to AVI output can be selected by I2C AVI_I_RATIO or AVI_V_RATIO bits. TI recommend AVI_I_RATIO = 2 with 500mA discharge current to achieve best accuracy

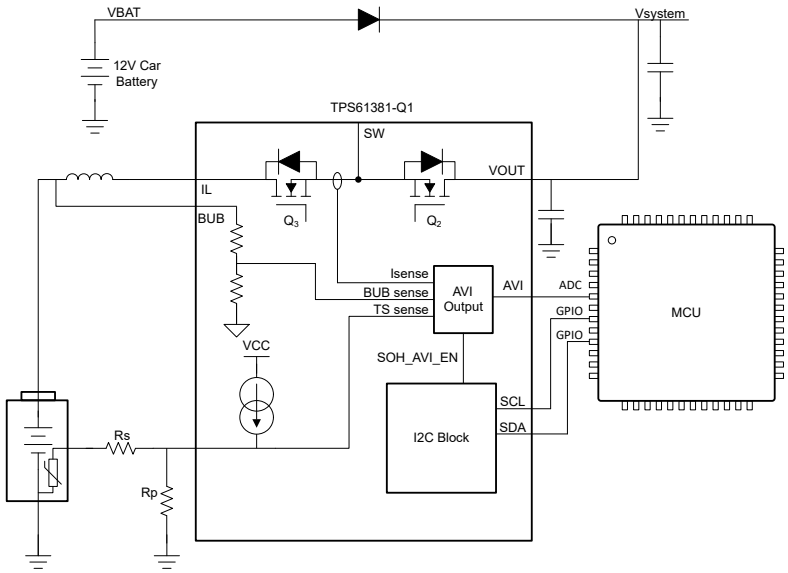


Figure 6-18. AVI pin connection

6.6.3 Calculate Impedance of BUB

Steps below gives an example on how to calculate the internal impedance of the back up battery with your system MCU :

- Set SOH discharge current to 0A (Register 0x09: SOH_SET1, SOH_I bits)
- Set AVI pin ratio to the backup battery voltage as 1 (Register 0x10: SOH_SET2, SOH_V_RATIO bits)
- Set AVI pin ratio to the discharge current as 2 (Register 0x10: SOH_SET2, SOH_I_RATIO bits)
- Select AVI pin output as battery voltage (Register 0x10: SOH_SET2, SOH_AVI_EN bits)
- Enable SOH function (Register 0x0B: CONTROL_STATUS, CHGR_SOH_EN bits)
- Wait for about 1ms for AVI output voltage to stabilize.
- Read the back-up battery voltage at AVI pin with the MCU ADC (V_{BUB1})
- Set SOH discharge current to 500mA (Register 0x09: SOH_SET1, SOH_I bits)
- Discharge for 500ms (Depending on battery characteristic, NiMH usually requires 500ms).
- Read the back-up battery voltage at AVI pin with the MCU ADC (V_{BUB2})
- Select AVI pin output as discharge current (Register 0x10: SOH_SET2, SOH_AVI_EN bits)
- Wait for about 1ms for AVI output voltage to stabilize.
- Read the discharge current at AVI pin with the MCU ADC (I_{BUB2})

MCU can use below equation to calculate the internal impedance of the back-up battery and detect the battery state of health.

$$R_{BUB} = (V_{BUB1} - V_{BUB2}) / I_{BUB} \quad (6)$$

6.7 I²C Serial Interface

The TPS61381-Q1 uses I²C interface for flexible converter parameter programming. I²C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I²C devices can be considered as masters or slaves when performing data transfers. A master is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The TPS61381-Q1 operates as a slave device with address 31h. Receiving control inputs from the master device like a microcontroller or a digital signal processor reads and writes the internal registers 00h through 0Eh. The I²C interface of the TPS61381-Q1 supports both standard mode (up to 100 kbit/s) and fast mode plus (up to 400 kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

6.7.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

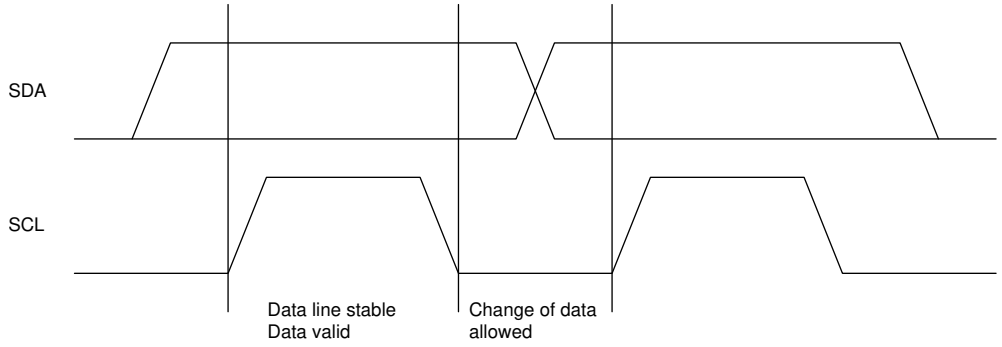


Figure 6-19. I²C Data Validity

6.7.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

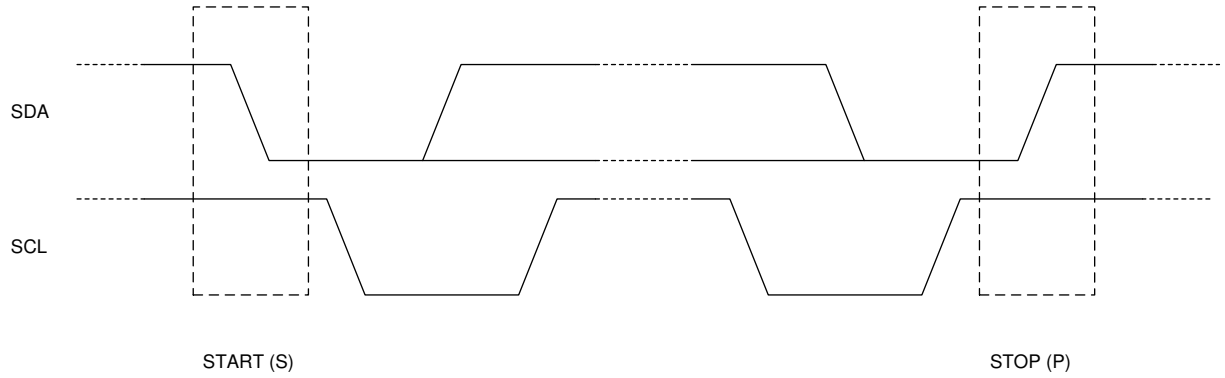


Figure 6-20. I²C START and STOP Conditions

6.7.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

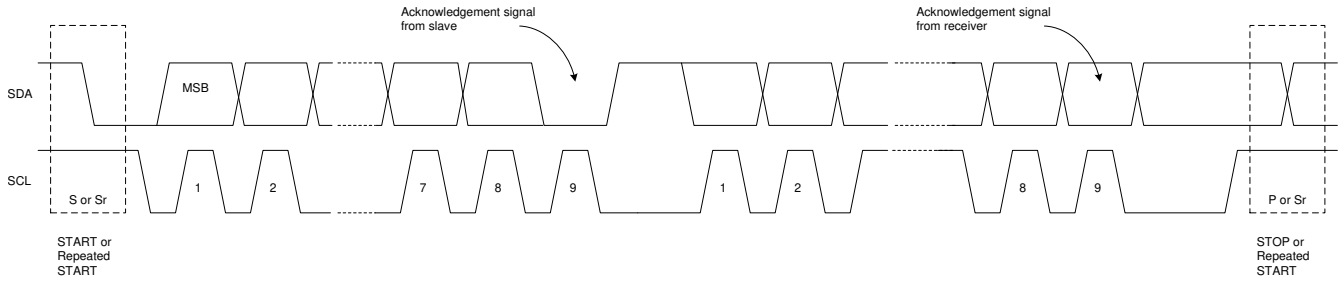


Figure 6-21. Byte Format

6.7.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse.

The Not Acknowledge signal is when SDA remains high level during the 9th clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

6.7.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

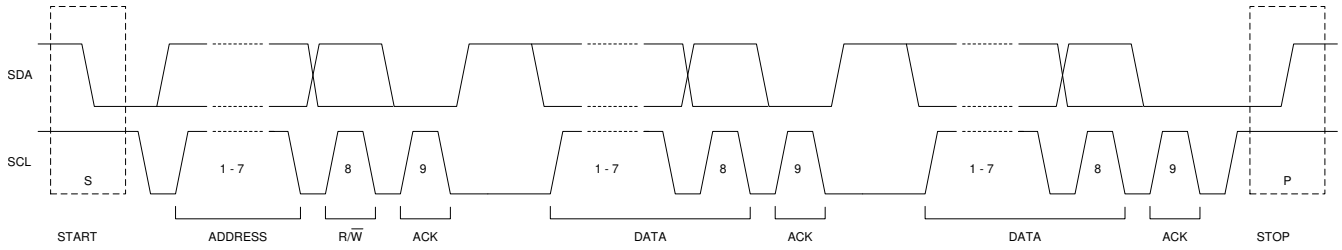


Figure 6-22. Slave Address and Data Direction

6.7.6 Single Read and Write

The images below show the single-byte write and single-byte read format of the I²C communication.

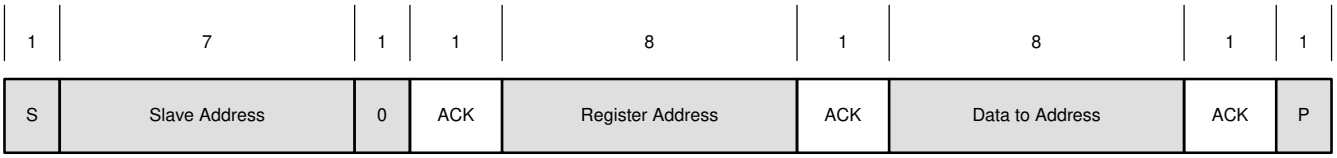


Figure 6-23. Single-byte Write

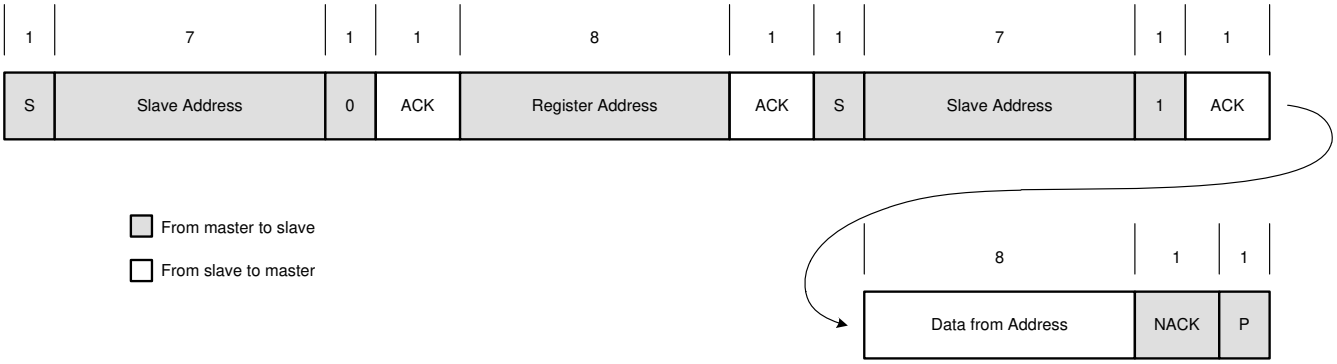


Figure 6-24. Single-byte Read

If the register address is not defined, the TPS61381-Q1 sends back NACK and goes back to the idle state.

6.7.7 Multi-Read and Multi-Write

The TPS61381-Q1 supports multi-read and multi-write.

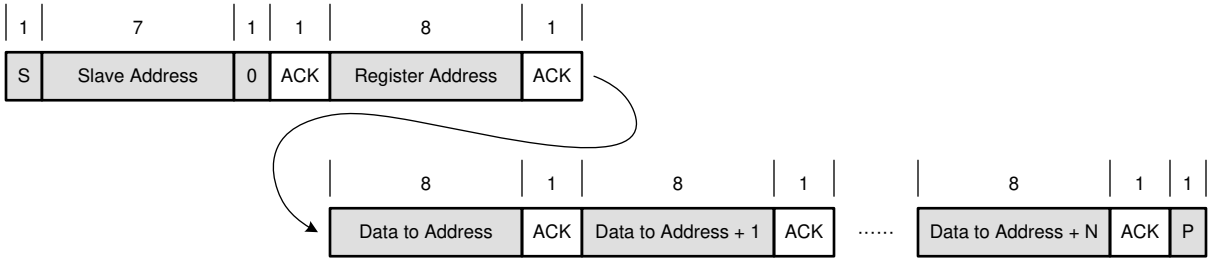


Figure 6-25. Multi-byte Write

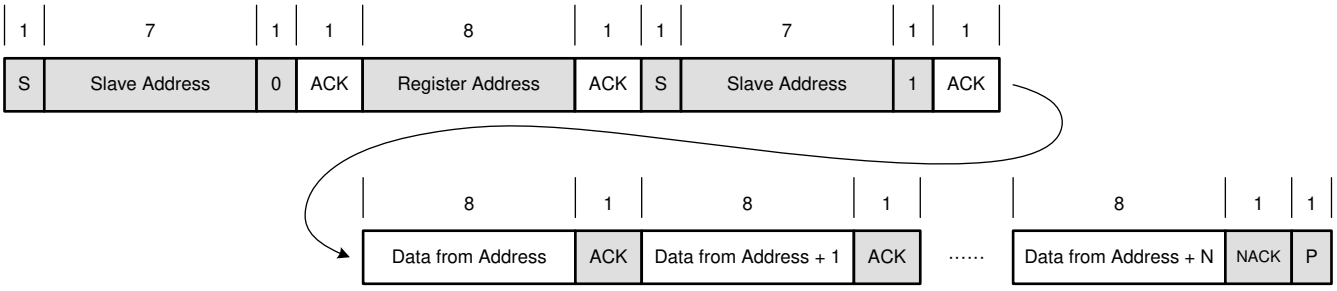


Figure 6-26. Multi-byte Read

7 Register Maps

Table 7-1 lists the memory-mapped registers for the device registers. All register offset addresses not listed in Table 7-1 should be considered as reserved locations, and the register contents should not be modified.

Table 7-1. Device Registers

Address	Register Name	Type	Description	Section
00H	CHIP_ID	R	DIE_TYPE provides information on the chip and silicon revision	
01H	BOOST_SET1	R/W	Boost set1: frequency, PFM or FPWM, spread spectrum, short protection, output discharge	
02H	BOOST_SET2	R/W	Boost set2: Vout, current limit	
03H	BOOST_SET3	R/W	Boost set2: BUB voltage loop, boost wake up threshold.	
04H	CHGR_SET1	R/W	Charger set1: battery type, CV voltage, NiMH timer.	
05H	CHGR_SET2	R/W	Charger set2: cell number, CC current	
06H	CHGR_SET3	R/W	Charger set3: termination current	
07H	CHGR_SET4	R/W	Charger set4: safety timer	
08H	CHGR_STATUS	R	Charger status: pre-charge, CC phase, CV phase, charge done,	
09H	SOH_SET1	R/W	SOH set1: discharge current	
0AH	SOH_SET2	R/W	SOH set2: AVI pin to current ratio, AVI pin to voltage ratio, AVI output selection.	
0BH	CONTROL_STATUS	R/W or R	Control status: Boost enable, charger or SOH enable, boost active, charger active, SOH active, standby active.	
0CH	FAULT_CONDITION	R	Fault flag: Vout OVP, battery is OVP, thermal shutdown signal, short, out of safety time and out of temperature and device thermal shutdown	
0DH	STATUS_PIN_SET	R/W	STATUS pin output selection: including boost, charger done and thermal shutdown	
0EH	SW_RST	W	Software reset: resets the entire part to its original default conditions	

7.1 Register 00H: CHIP_ID

Figure 7-1. CHIP_ID

7	6	5	4	3	2	1	0
CHIP_ID							
R-00001100b							

Table 7-2. CHIP_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:0]	CHIP_ID	R	0x0C	Provides information on the chip and silicon version.

7.2 Register 01H: BOOST_SET1

Figure 7-2. BOOST_SET1

7	6	5	4	3	2	1	0
Reserved	BST_PFM	BST_PFM		BST_SCP	Reserved		
R/W-0b	R/W-0b	R/W-01b		R/W-0b	R/W-000b		

Table 7-3. BOOST_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7]	Reserved	R	0	Reserved
[6]	BST_PFM	R/W	0	0 = PFM, auto PFM at light load 1 = FPWM, force PWM at light load TI recommend PFM for bi-directional application.
[5:4]	BST_SS	R/W	01b	00b = no spread spectrum 01b = 6.5 kHz modulation frequency 10b = 3.2 kHz modulation frequency 11b = 1.6 kHz modulation frequency
[3]	BST_SCP	R/W	0	0 = Boost output short circuit protection disabled 1 = Boost output short circuit protection enabled TI recommend enabling short circuit protection for system safety.
[2:0]	Reserved	R	000b	Reserved

7.3 Register 02H: BOOST_SET2

Figure 7-3. BOOST_SET2

7	6	5	4	3	2	1	0
BST_VOUT				Reserved	BST_ILIM		BST_ILIM_EN
R/W-0011b				R-0b	R/W-10b		R-1b

Table 7-4. BOOST_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:4]	BST_VOUT	R/W	0011b	Set output target voltage 0000b=5V 0001b=5.5V 0010b=6V 0011b=6.2V 0100b=6.5V 0101b=6.8V 0110b=7.1V 0111b=7.5V 1000b=8V 1001b=8.5V 1010b=9V 1011b=9.5V 1100b=10V 1101b=10.5V 1110b=11V 1111b=12V
[3]	Reserved	R	0	Reserved
[2:1]	BST_ILIM	R/W	10b	Boost average current limit 00b=5A 01b=10A 10b=15A
[0]	BST_ILIM_EN	R/W	1	0=disable boost peak current limit 1=enable boost peak current limit If average current=5A or 10A, the peak current limit is 15A; otherwise the peak current limit is 30A.

7.4 Register 03H: BOOST_SET3

Figure 7-4. BOOST_SET3

7	6	5	4	3	2	1	0
BST_VINLOOP		BST_VINLOOP_EN	BST_WAKE			Reserved	
R/W-10b		R/W-0b	R/W-111b			R-00b	

Figure 7-5. BOOST_SET3 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:6]	BST_VINLOOP	R/W	10b	Set input voltage regulation voltage 00b=1V 01b=1.2V 10b=1.5V 11b=2V
[5]	BST_VINLOOP_EN	R/W	0	0=disable input voltage loop 1=enable input voltage loop
[4:2]	BST_WAKE	R/W	111b	Set boost automatically wake-up threshold, VOUT falling 000b=4.5V 001b=5V 010b=5.5V 011b=6V 100b=6.5V 101b= 7.5V 110b=8V 111b=Vout_target+3%
[1:0]	Reserved	R	00b	Reserved

7.5 Register 04H: CHGR_SET1

Figure 7-6. CHGR_SET1

7	6	5	4	3	2	1	0
BUB_TYP		BST_VINLOOP_EN				BST_WAKE	
R/W-00b		R/W-0000b				R/W-00b	

Figure 7-7. CHGR_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:6]	BUB_TYP	R/W	00b	Set the back-up battery charging strategy 00b=Li-ion charging profile, precharge+CC+CV 01b=LiFePO4 charging profile, precharge+CC+CV 10b=NiMH charging profile, CC + timer 11b=Super capacitor charging profile, CC+CV
[5:2]	BUB_CV	R/W	0000b	Set CV voltage 0000b=1.7V (supercap) 0001b=2.0V (supercap) 0010b=2.2V (supercap) 0011b=2.4V (supercap) 0100b=2.5V (supercap) 0101b=2.7V (supercap) 0110b=3.0V (supercap) 0111b=3.5V (LiFePO4) 1000b=3.6V (LiFePO4) 1001b=3.7V (LiFePO4) 1010b=3.8V (Li-ion) 1011b=3.9V (Li-ion) 1100b=4.05V (Li-ion) 1101b=4.10V (Li-ion) 1110b=4.20V (Li-ion) 1111b=4.35V (Li-ion) Note: this register is inactive for NiMH battery.
[1:0]	BUB_NIMH_TIMER	R/W	00b	Set the NiMH battery charging time 00b=4h 01b=8h 10b=16h 11b=32h

7.6 Register 05H: CHGR_SET2

Figure 7-8. CHGR_SET2

7	6	5	4	3	2	1	0
BUB_CELL			Reserved			BUB_CC	
R/W-000b			R-000b			R/W-00b	

Figure 7-9. CHGR_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:5]	BUB_CELL	R/W	000b	The number cell of back-up battery Li-ion supports up to 2s, NiMH support up to 5s Supercap support up to 4s 000b=1 001b=2 010b=3 011b=4 100b=5
[4:2]	Reserved	R	000b	Reserved
[1:0]	BUB_CC	R/W	00b	Set CC current 00b=50mA 01b=100mA

7.7 Register 06H: CHGR_SET3

Figure 7-10. CHGR_SET3

7	6	5	4	3	2	1	0
Reserved					BUB_TER	CHG_TEM_CURRENT	Reserved
R-00000b					R/W-0b	R/W-0b	R-0b

Figure 7-11. CHGR_SET3 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:3]	Reserved	R	00000b	Reserved
[2]	BUB_TER	R/W	0	After fully charged, re-charge or not. For NiMH battery, enable intermittent charging For Li-ion, LiFePO4 or super capacitor battery, start recharge when battery voltage is lower than recharge voltage. 0=disable re-charge 1=enable re-charge
[1]	CHG_TEM_CURRENT	R/W	0	0= 10% * Icc 1=20% * Icc Note: this bit is active for Li-ion, LiFePO4 and super capacitor.
[0]	Reserved	R	0	Reserved

7.8 Register 07H: CHGR_SET4

Figure 7-12. CHGR_SET4

7	6	5	4	3	2	1	0
SAFT_TIMER_EN	SAFT_TIMER	CHG_TEM_CURRENT					
R/W-1b	R/W-1b	R-00000b					

Figure 7-13. CHGR_SET4 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7]	SAFT_TIMER_EN	R/W	1	0=disable the safety time of Li-ion charger 1= enable the safety time of Li-ion charger
[6]	SAFT_TIMER	R/W	1	0=5hr 0=10hr
[5:0]	Reserved	R	00000b	Reserved

7.9 Register 08H: CHGR_STATUS

Figure 7-14. CHGR_STATUS

7	6	5	4	3	2	1	0
CHGR_MODE_PRE	CHGR_MODE_CC	CHGR_MODE_CV	CHGR_MODE_DONE	ALRT_CHGR_MODE_DONE	Reserved		
R-0b	R-0b	R-0b	R-0b	R-0b	R-000b		

Figure 7-15. CHGR_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
[7]	CHGR_MODE_PRE	R	0	Read only that provides information on the charger operation mode 0=Charger is not operating in pre-charge stage 1=Charger is operating in pre-charge stage
[6]	CHGR_MODE_CC	R	0	Read only that provides information on the charger operation mode 0=Charger is not operating in CC stage 1=Charger is operating in CC stage
[5]	CHGR_MODE_CV	R	0	Read only that provides information on the charger operation mode 0=Charger is not operating in CV stage 1=Charger is operating in CV stage
[4]	CHGR_MODE_DONE	R	0	Read only that provides information on the charger operation mode 0= Charge done not triggered. 1= Charge done triggered.
[3]	ALRT_CHGR_MODE_DONE	R	0	Read only that provides information on the charger operation mode. 0= charging is no done since the last read 1=charging is done since the last read Latch after set, clear-on-read
[2:0]	Reserved	R	000b	Reserved

7.10 Register 09H: SOH_SET1

Figure 7-16. SOH_SET1

7	6	5	4	3	2	1	0
SOH_I			Reserved				
R/W-000b			R-00000b				

Figure 7-17. SOH_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:5]	SOH_I	R/W	000b	Set SOH discharge current 000b=0A 001b=100mA (Recommend AVI_I_RATIO=2) 010b=200mA (Recommend AVI_I_RATIO=2) 011b=300mA (Recommend AVI_I_RATIO=2) 100b=500mA (Recommend AVI_I_RATIO=2) 101b=800mA (Recommend AVI_I_RATIO=2) 110b=1A (Recommend AVI_I_RATIO=2) 111b=1.5A (Recommend AVI_I_RATIO=1)
[4:0]	Reserved	R	00000b	Reserved

7.11 Register 0AH: SOH_SET2

Figure 7-18. SOH_SET2

7	6	5	4	3	2	1	0
AVI_I_RATIO		AVI_V_RATIO		Reserved		SOH_AVI_EN	
R/W-01b		R/W-10b		R-00b		R/W-00b	

Figure 7-19. SOH_SET2 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:6]	AVI_I_RATIO	R/W	01b	AVI pin ratio to the discharge current. The voltage of AVI pin = AVI_I_RATIO × discharge current 00b=1/2 01b=1 10b=2
[5:4]	AVI_V_RATIO	R/W	10b	AVI pin ratio to the back-up battery voltage. The voltage of AVI pin = AVI_V_RATIO × back-up battery voltage 00b=1/4 (Recommended for 2S Lithium, 3-4S super capacitor) 01b=1/2(Recommended for 1S Lithium, 2-4S NiMH, 2S super capacitor) 10b=1 (Recommended for 1S NiMH, 1S super capacitor)
[3:2]	Reserved	R	00b	Reserved
[1:0]	SOH_AVI_EN	R/W	00b	Enable AVI pin output and choose I, V or T output signal 00b=disable AVI pin output, internal 125kΩ pulldown to AGND. 01b=Enable back-up battery voltage output 10b=Enable discharge current output 11b=Enable battery temperature output

7.12 Register 0BH: CONTROL_STATUS

Figure 7-20. CONTROL_STATUS

7	6	5	4	3	2	1	0
BST_EN	CHGR_SOH_EN		ALRT_BST_ACTIVE	BST_ACTIVE	CHGR_ACTIVE	SOH_ACTIVE	STANDBY_ACTIVE
R/W-1b	R/W-00b		R-0b	R-0b	R-0b	R-0b	R-0b

Figure 7-21. CONTROL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
[7]	BST_EN	R/W	1	0=disable boost function 1= enable boost function
[6:5]	CHGR_SOH_EN	R/W	00b	00b=disable charger and SOH function 01b= enable charger function 10b=enable SOH function
[4]	ALRT_BST_ACTIVE	R	0	Read only. Provides information about the system operating mode 0= boost mode has not been activated since the last read 1= boost mode has been activated since the last read Latch after set, clear-on-read
[3]	BST_ACTIVE	R	0	Read only. Provides information about the system operating mode 0= boost mode is not active 1= boost mode is active
[2]	CHGR_ACTIVE	R	0	Read only. Provides information about the system operation mode 0=charger mode is not active 1= charger mode is active
[1]	SOH_ACTIVE	R	0	Read only. Provides information about the system operation mode 0=SOH mode is not active 1= SOH mode is active
[0]	STANDBY_ACTIVE	R	0	Read only. Provides information about the system operation mode 0=standby mode is not active 1= standby mode is active

7.13 Register 0CH: FAULT_CONDITION

Figure 7-22. FAULT_CONDITION

7	6	5	4	3	2	1	0
SYSTEM_OVP	TS_FAULT	BUB_SHORT	TIMER_FAULT	BUB_OVP	THRM_SD	Reserved	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-00b	

Figure 7-23. FAULT_CONDITION Register Field Descriptions

Bit	Field	Type	Reset	Description
[7]	SYSTEM_OVP	R	0	0=No overvoltage on VOUT pin 1=Overvoltage on VOUT pin
[6]	TS_FAULT	R	0	0= TS pin voltage is within cold/hot temperature threshold 1= TS pin voltage is out of cold/hot temperature threshold
[5]	BUB_SHORT	R	0	0= No short circuit on Li-ion/LiFePO4 battery 1= Short circuit on Li-ion/LiFePO4 battery Note: this bit only active for Li-ion/LiFePO4 battery
[4]	TIMER_FAULT	R	0	0= Within safety time 1= Out of safety time
[3]	BUB_OVP	R	0	0= No overvoltage on battery 1= Overvoltage on battery
[2]	THRM_SD	R	0	0=no thermal shutdown 1= thermal shutdown (Tj > 175degC)
[1:0]	Reserved	R	00b	Reserved

7.14 Register 0DH: STATUS_PIN_SET

Figure 7-24. STATUS_PIN_SET

7	6	5	4	3	2	1	0
INC_BST	INC_ABST	INC_ADN	INC_TSD	INC_TSFAULT	Reserved		
R-1b	R-0b	R-0b	R-0b	R-0b	R-000b		

Figure 7-25. STATUS_PIN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
[7]	INC_BST	R/W	1	0= BST_ACTIVE status is not included in the STATUS pin output, STATUS pin pulls low when entering boost mode 1= BST_ACTIVE status is included in the STATUS pin output Check Section 7.12 for discriptions of BST_ACTIVE signal
[6]	INC_ABST	R/W	0	0= ALRT_BST_ACTIVE status is not included in the STATUS pin output, STATUS pin pulls low when boost mode is entered since last read 1= ALRT_BST_ACTIVE status is included in the STATUS pin output Check Section 7.12 for discriptions of ALRT_BST_ACTIVE signal
[5]	INC_ADN	R/W	0	0= ALRT_CHGR_MODE_DONE status is not included in the STATUS pin output, STATUS pin pulls low when charger operation is done since last read 1= ALRT_CHGR_MODE_DONE status is included in the STATUS pin output Check Section 7.9 for discriptions of ALRT_CHGR_MODE_DONE signal
[4]	INC_TSD	R/W	0	0= THRM_SD status is not included in the STATUS pin output, STATUS pin pulls low when thermal shutdown is triggered 1= THRM_SD status is included in the STATUS pin output Check Section 7.13 for discriptions of THRM_SD signal
[3]	INC_TSFAULT	R/W	0	0= TS_FAULT status is not included in the STATUS pin output, STATUS pin pulls low when TS_FAULT is triggered 1= TS_FAULT status is included in the STATUS pin output Check Section 7.13 for discriptions of TS_FAULT signal
[2:0]	Reserved	R	000b	Reserved

7.15 Register 0EH: SW_RST

SW_RST (software reset) is a write-only register/command that resets the entire part to its original default conditions at the end of the I2C SW_RST transaction (i.e., the data-byte ACK). Execution only occurs if DIN[7:0]=0x00. The effect of a SW_RST is identical to power-cycling the part.

TPS61381-Q1 also support hardware reset, when the two EN pins are both low(EN_BST=0 AND EN_CHGR=0), the entire registers are reset to its original default conditions.

Figure 7-26. SW_RST

7	6	5	4	3	2	1	0
CHIP_ID							
W-00000000b							

Table 7-5. SW_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:0]	SW_RST	W	00000000b	resets the entire part to its original default conditions

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TPS61381-Q1 is a bi-directional boost converter with CC/CV charger and battery health detection function. The device provides an integrated power solution in back-up power system, like T-box and e-call applications. The following design procedure can be used to design TBOX system with TPS61381-Q1.

8.2 Typical Application

Figure 8-1 shows a typical application circuit for the TPS61381-Q1. This device is designed to charge BUB when VBAT is normal when VBAT is normal and boost BUB energy to Vsystem when VBAT is disconnected.

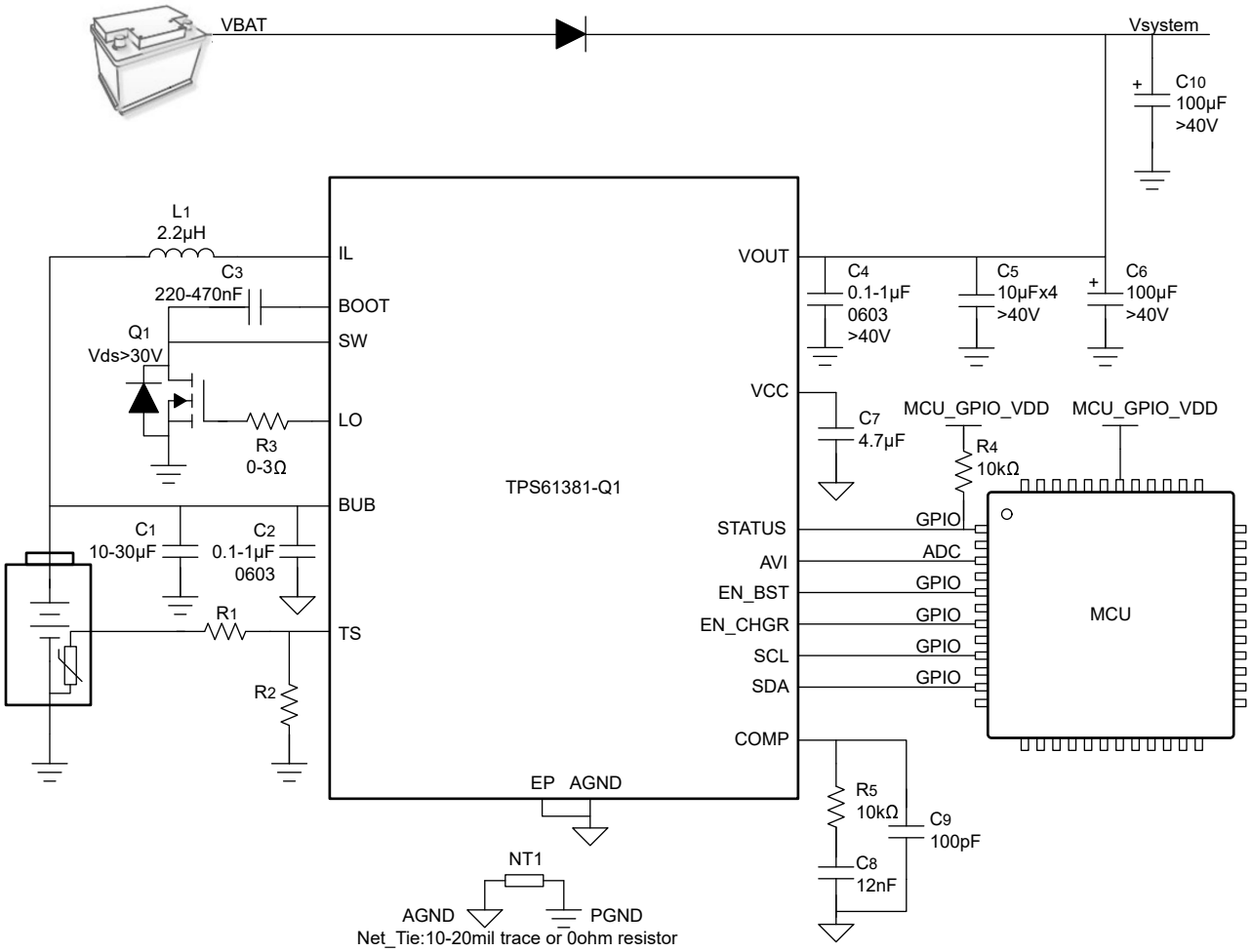


Figure 8-1. Typical TBOX Application

8.2.1 Design Requirements

The following table provides the parameters for our detailed design procedure example:

Table 8-1. Design Requirements

PARAMETERS	VALUES
Car Battery Input Voltage:	Typical: 6~18V, load damp: up to 40V
Back-up Battery	3s NiMH
Back-up Battery Voltage:	3 ~ 4.5V
Charging Current:	100mA
Charging Time	8h
Battery Health Detection Current:	500mA
Boost Output Voltage:	6.2V
Boost Output Current:	4A
Mode Selection	Automatic Charger and Boost Mode
Voltage Drop during Mode Transient	<=200mV

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the External MOSFET

TPS61381-Q1 requires an external MOSFET (Q1) as its boost low side switch and SOH discharge switch. The external MOSFET is selected depending on its thermal performance, V_{DS} voltage and I_d current.

- TPS61381-Q1 supports only n-channel MOSFET as Q1.
- Recommend Qgd< 5nC. Qgd should not exceed 10nC at most.
- Vplateau<4V.
- Rdson low as possible. Recommend Rdson less than 15mohm at most
- The drain-source breakdown voltage, V(BR)DSS >= 30V
- The continuous drain current should be larger than the maximum peak current in the boost mode:

$$I_{peak} = \frac{I_{OUT}}{(1-D)\cdot eff} + \frac{V_{BUB}\cdot D}{2L\cdot f_{SW}} \quad (7)$$

where

- I_{OUT} is the maximum load current in boost mode.
- D is the duty cycle of boost operation
- eff is the boost mode efficiency
- L is the boost inductance
- f_{sw} is the switching frequency in boost mode
- V_{BUB} is the input voltage on BUB pin

8.2.2.2 Inductor Selection

A boost converter normally requires two main passive components for storing energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency), transient behavior, and loop stability, which makes the inductor the most critical component in application.

When selecting the inductor and the inductance, the other important parameters are:

- The maximum current rating (RMS and peak current should be considered)
- The series resistance
- Operating temperature

The TPS61381-Q1 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 2 A, the slew rate of its slope compensation may not be adequate, and the loop can be unstable. Therefore, it is recommended to make the peak-to-peak current ripple between 1.2A to 2 A when selecting the inductor.

The inductance can be calculated by:

$$L = \frac{V_{BUB}\left(1 - \frac{V_{BUB} \cdot eff}{V_{OUT}}\right)}{\Delta I_L \cdot f_{sw}} \quad (8)$$

So, TI suggests 2.2µH for 400kHz switching frequency.

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have ±20%, or even ±30%, tolerance with no current bias. When the inductor current approaches the saturation level, the inductance can decrease 20% to 35% from the value at 0-A bias current, depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, switching frequency, and input and output voltages. The peak current can be calculated by:

$$I_{peak} = \frac{I_{OUT}}{(1 - D) \cdot eff} + \frac{V_{BUB} \cdot D}{2L \cdot f_{sw}} \quad (9)$$

Select the inductor with a saturation current rating higher than the maximum inductor current.

where

- I_{peak} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- eff is the efficiency
- V_{BUB} is the input voltage
- L is the inductance
- f_{SW} is the switching frequency

The heat rating current (RMS) is can be calculated with:

$$I_{LRMS} = \sqrt{\left(I_{BUB}^2 + \Delta I_L{}^2\right)/12} \quad (10)$$

where

- I_{LRMS} is the RMS current of the inductor
- I_{BUB} is the input current of the inductor
- ΔI_L is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature-related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. Table 8-2 lists some recommended inductors. In this application example, the Coilcraft inductor XGL6060-222 is selected for its small size, high saturation current, and small DCR.

Table 8-2. Recommended Inductors for the TPS61381-Q1

PART NUMBER	L (µH)	DCR TYPICAL(mΩ)	SATURATION CURRENT (A)	HEAT RATING CURRENT (A)	SIZE (L × W × H)	VENDOR(1)
XGL6060-222MED	2.2	4.3	12.1 (20% Drop)	20.7 (ΔT 40K)	6.51 × 6.71 × 6.1	Coilcraft
XGL1060-222MED	2.2	3.8	21.5 (20% Drop)	25.3 (ΔT 40K)	10.0 × 11.3 × 6.0	Coilcraft
IHLP-4040DZ-ER2R2	2.2	8.2	25.6 (20% Drop)	12.0 (ΔT 40K)	10.16 × 10.195 × 4.0	Vishay
IHLP-6767DZ-ER2R2	2.2	4.57	17.5 (20% Drop)	26 (ΔT 40K)	17.15 × 11.94 × 4.0	Vishay
B82464D6222M000	2.2	9	11.8 (10% Drop) 13.85 (30% Drop)	6 (ΔT 40K)	10.4 × 10.4 × 6.3	TDK
7843340220	2.2	10	14.7 (30% Drop)	8.4 (ΔT 50K)	8.1 × 8.1 ×9.0	Würth Elektronik
784373680022	2.2	7.8	25.7 (30% Drop)	13.6 (ΔT 50K)	10 × 10.85 ×3.8	Würth Elektronik

(1) See the *Third-Party Products* disclaimer

8.2.2.3 Capacitor in Back-Up Battery Side

The capacitance in the back-up battery side affects BUB loop stability. The effective capacitance should be between 5µF to 10µF BUB loop functions needs to be applied. If BUB loop function is not required, then the capacitance in BUB side can be big without limit.

Care must be taken when evaluating a ceramic capacitor's effective capacitance. For ceramic capacitors, the derating under dc bias voltage, aging, and ac signal should be taken into consideration. Taking Murata GCM21BR71C475KA73K as an example, the capacitor's effective capacitance reduces by 56% when 8V DC voltage is applied.

If back up battery is connected to the IC through long cable, TI recommend adding extra 100-200uF electrolytic capacitors on BUB side. This capacitor helps supress LC ringing caused by parasite inductance on back up battery cable. Note that the electrolytic capacitor cannot replace ceramic capacitor and 5µF to 10µF ceramic capacitor still needs to be placed near the IC.

8.2.2.4 Selecting the Output Capacitor

Main consideration for designing the output capacitor is the requirements for the output voltage drop when main battery fails and the device transition into boost mode. The minimum Cout can be calculated by:

$$C_{out} > \frac{I_{outmax} \times 20us}{\Delta V_{outmax}} \quad (11)$$

Where

- C_{OUT} is the output capacitance
- I_{OUTMAX} is the maximum output current
- ΔV_{OUTMAX} is the maximum output voltage drop allowed when transition into boost mode

20us is the maximum transition time for the device to enter boost mode and start switching

The output ripple voltage another factor that affects the Cout selection. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} > \frac{I_{outmax} \times (V_{out} - V_{BUB})}{f_{sw} \times \Delta V \times V_{out}} \quad (12)$$

Where

- I_{OUT} is the output current
- V_{OUT} is the output DC voltage
- V_{BUB} is the back up battery voltage
- ΔV is the output voltage ripple required
- $f_{sw}$is the switching frequency

Typically, a combination of ceramic capacitors and bulk electrolytic capacitors is needed to provide low ESR, high ripple current, and small output voltage ripple.

Ceramic capacitors has DC-bias derating that significantly reduce the effective capacitance when a DC-voltage is applied. So please check the DC-bias curve at Boost Vout target voltage when calculating the capacitance.

Electrolytic capacitors has large ESR and the ESR of electrolytic capacitor can increase by over 10 times under low temperature condition and seriously affect loop stability. So please make sure low temperature ESR is considered when calculating loop stability. Poly-hybrid capacitors usually has smaller ESR under low temperature and is therefore more recommended.

Based on the application requirement, this application choose 100uF electrolytic capacitor with four 10uF ceramic capacitors in parallel.

8.2.2.5 Loop Stability and Compensation Design

The TPS61381-Q1 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network, comprised of resistor R5, and ceramic capacitors C8 and C9, is connected to the COMP pin. Compensation parameter need to be calculated case by case. Following section gives an example about how to calculate the compensation network parameters with the selected inductor and output capacitor.

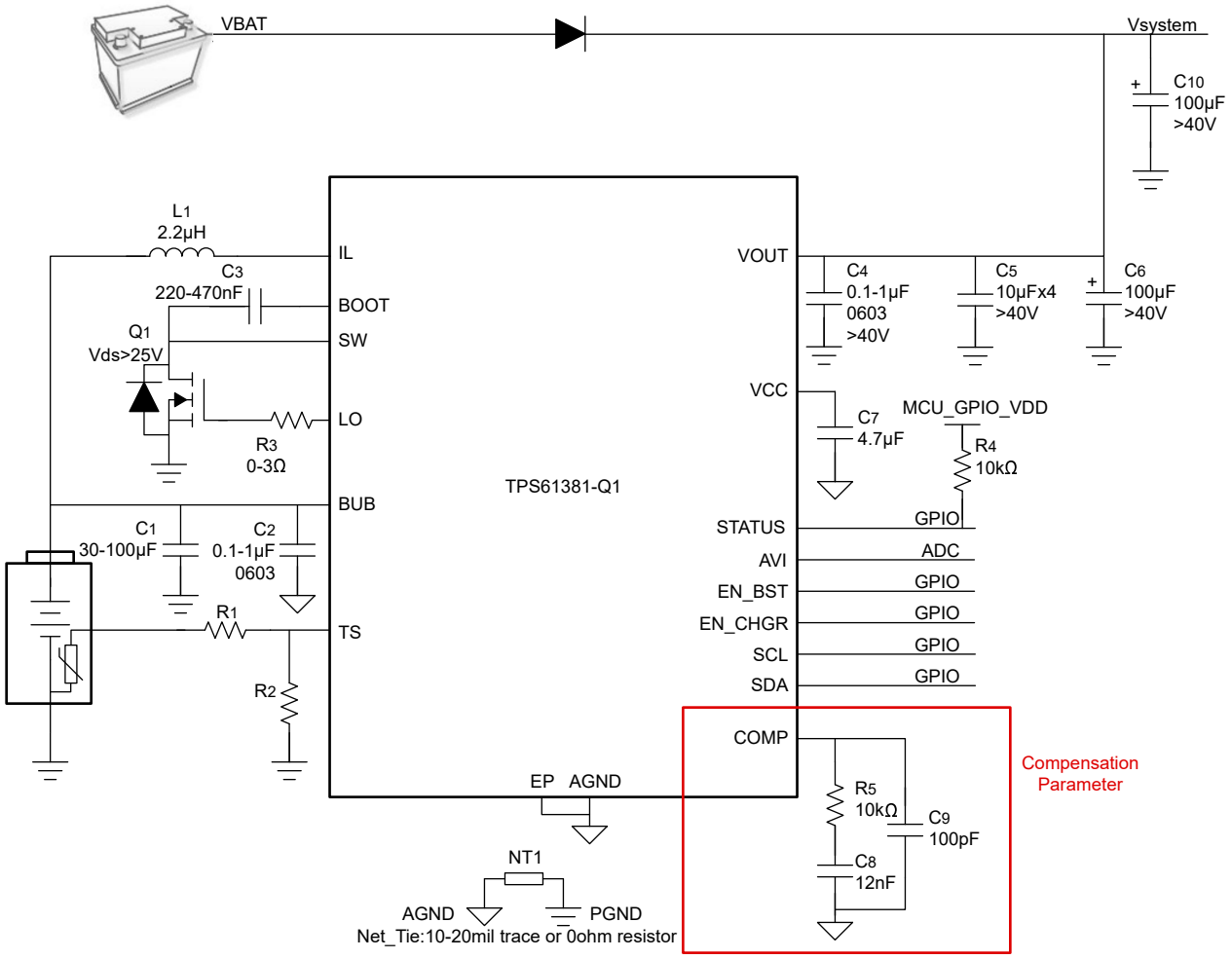


Figure 8-2. TPS61381-Q1 Compensation Design

8.2.2.5.1 Small Signal Analysis

The TPS61381-Q1 uses the fixed frequency peak current mode control with an internal adaptive slope compensation to avoid subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. The image below shows the equivalent small signal elements of a boost converter.

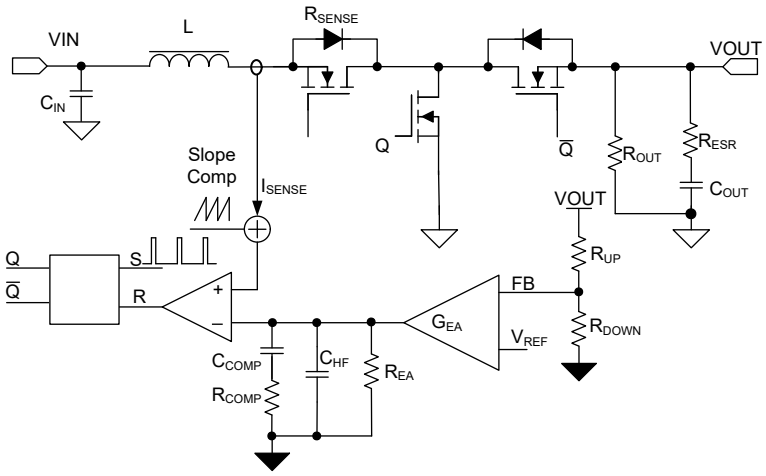


Figure 8-3. TPS61381-Q1 Control Equivalent Circuitry Model

The small signal of power stage can be given by:

$$K_{PS}(s) = \frac{R_{out}(1-D)}{2R_{sense}} \times \frac{\left(1+\frac{s}{2\pi \times f_{zESR}}\right)\left(1-\frac{s}{2\pi \times f_{zRHP}}\right)}{\left(1+\frac{s}{2\pi \times f_{pPS}}\right)} \quad (13)$$

where

- D is the duty cycle
- R_{out} is the output load resistance
- R_{sense} is the equivalent internal current sense resistor, which is typically 6mΩ

The single pole of the power stage can be given by:

$$f_{pPS} = \frac{2}{2\pi \times C_{out} \times R_{out}} \quad (14)$$

where

- C_{out} is the output capacitance. For a boost converter having multiple identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor can be given by:

$$f_{zESR} = \frac{1}{2\pi \times C_{out} \times R_{ESR}} \quad (15)$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero can be given by:

$$f_{zRHP} = \frac{R_{out}(1-D)^2}{2\pi \times L} \quad (16)$$

where

- D is the duty cycle
- R_{out} is the output load resistor
- L is the inductance

Equation 17 shows the equation for feedback resistor network and the compensation network.

$$H_{COMP}(s) = G_{comp} \times R_{EA} \times \frac{R_{up}+R_{down}}{R_{down}} \times \frac{\left(1+\frac{s}{2\pi \times f_{zCOMP}}\right)}{\left(s1+\frac{s}{2\pi \times f_{pCOMP1}}\right)\left(1+\frac{s}{2\pi \times f_{pCOMP2}}\right)} \quad (17)$$

where

- G_{COMP} is the gain of the error amplifier, typically G_{EA} = 24uS
- R_{EA} is the output impedance of the error amplifier, typically R_{EA} = 5 MΩ
- f_{pCOMP1}, f_{pCOMP2} is the pole's frequency of the compensation
- f_{zCOMP} is the zero's frequency of the compensation network

f_{pCOMP1} can be given by:

$$f_{pCOMP1} = \frac{1}{2\pi \times R_{EA} \times C_{COMP}} \quad (18)$$

where

- C_{COMP} is the compensation capacitor

f_{pCOMP2} can be given by:

$$f_{pCOMP2} = \frac{1}{2\pi \times R_{COMP} \times C_{HF}} \quad (19)$$

where

- C_{HF} is the high frequency bypass capacitor on COMP pin
- R_{COMP} is the resistor of the compensation network

f_{zCOMP} can be given by:

$$f_{zCOMP} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (20)$$

where

- C_{COMP} is the zero capacitor compensation
- R_{COMP} is the resistor of the compensation network

8.2.2.5.2 Loop Compensation Design

With the previous analysis on small signal models, we can calculate the compensation network parameters with the given inductor and output capacitor parameters. This section gives an example on calculating loop compensation.

1. **Set the Crossover Frequency, f_C .**

   The first step is to set the loop crossover frequency, f_C. The higher the crossover frequency, the faster the loop response is. It is generally accepted that the loop gain crosses over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{zRHP}.

2. **Set the Compensation Resistance, R_{COMP} .**

   For a well compensated boost system, the f_C is determined by R_{COMP}. For a properly designed boost system, f_{zCOMP} should be placed below f_C to ensure phase margin. And for common R_{COMP} range, R_{COMP} should be far smaller than the amplifier output resistance R_{EA}, which makes R_{COMP} | | R_{EA} ~ = R_{COMP}. Therefore, in the equation below, the initial gain R_{COMP} × G_{COMP} × K_{FB} is determined by R_{COMP}. Therefore the f_c can be calculated by the equation that the close loop total gain $T_{(s)}$ = K_{PS}(s) + H_{COMP}(s) is zero at f_C.

$$H_{COMP} = 20lg\left(G_{COMP} \times R_{COMP} \times \frac{R_{down}}{R_{up} + R_{down}}\right) = -K_{PS}(f_c) \quad (21)$$

   where

   - K_{PS} is the gain of the power stage
   - G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 24 µS

3. **Set the Compensation Zero capacitor, C_{COMP} .**

   The compensation zero should be placed at the power stage pole f_{pPS} to compensate the phase drop near f_{pPS}. Set f_Z = f_P, the C_{COMP} can be calculated .

$$C_{COMP} = \frac{R_{out} \times C_{out}}{2R_{COMP}} \quad (22)$$

4. **Set the Compensation Pole Capacitor, C_{HF} .**

   The compensation pole should be placed to elimiate the ESR zero produced by R_{ESR} and C_{out}. Set f_{pCOMP2} = f_{zESR}, and get:

$$C_{HF} = \frac{R_{ESR} \times C_{out}}{R_{COMP}} \quad (23)$$

5. **Check Phase Margin and Gain Margin**

   The calculated compensation parameters does not always ensure stability. Especially when the Cout has big ESR which bring f_{zESR} into bandwidth. TI provide excel calculation tool which generates bode plot after all compensation parameters are selected. So please check the bode plot for stability after step 1-4. TI recommend Phase margin > 60deg and gain margin > 10db. Reduce desired f_c and re-calculate compensation in step1-4 if the margin does not meet requirement.

	Boost Compensation Calculation		
71	Boost loop Calculation		
72	Vin	2.50	V
73	Vout	5.50	V
74	Iout	1.50	A
75	fp_PS	368	Hz
76	fz_RHP	43122	Hz
77	fz_ESR	39789	Hz
78	f(BW) desired	2	kHz
79	*R3 recommended*	10.11	kΩ
80	R3 actual	12	kΩ
81	*C7 recommended*	42.78	nF
82	C7 actual	12.0	nF
83	fz_COMP	947	Hz
84	*C6 recommended*	462.70	pF
85	C6 actual	33	pF
86	fp1_COMP	3	Hz
87	fp2_COMP	307249	Hz
88	f(BW) actural	6310	Hz
89	Phase Margin	72	°
90	Phase Cross Frequency	50119	Hz
91	Gain Margin	15	dB
92	Slope Compensation	Good	
94	Check Stability		

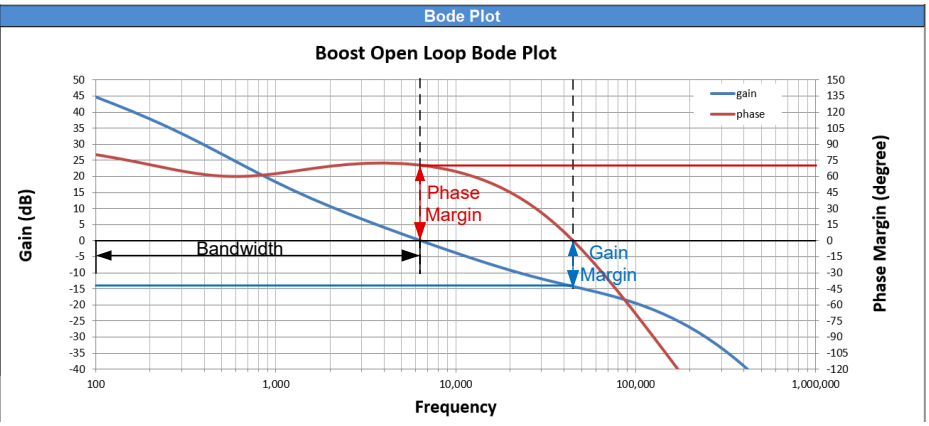
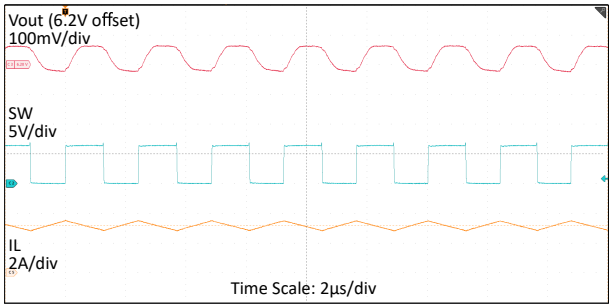


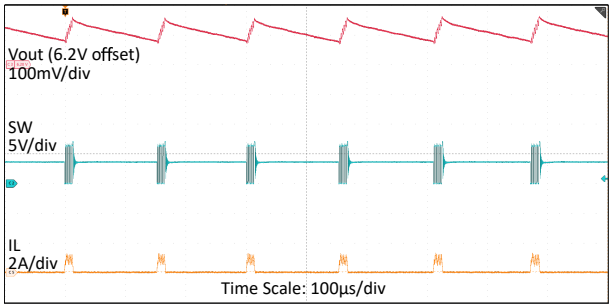
Figure 8-4. Evaluate Loop Stability

8.2.3 Application Curves



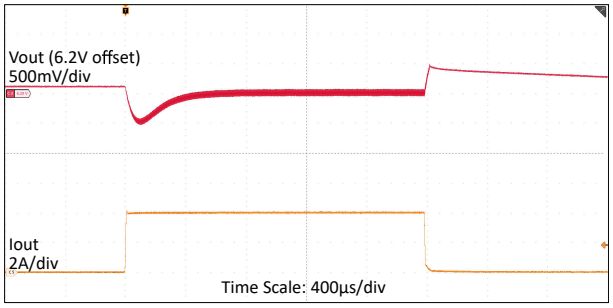
V_{BUB} = 3.6V V_{OUT} = 6.2V I_{OUT} = 4A

Figure 8-5. Boost Switching at Heavy Load



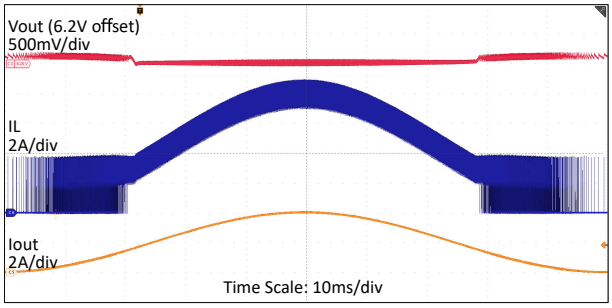
V_{BUB} = 3.6V V_{OUT} = 6.2V I_{OUT} = 100mA

Figure 8-6. Boost Switching at Light Load



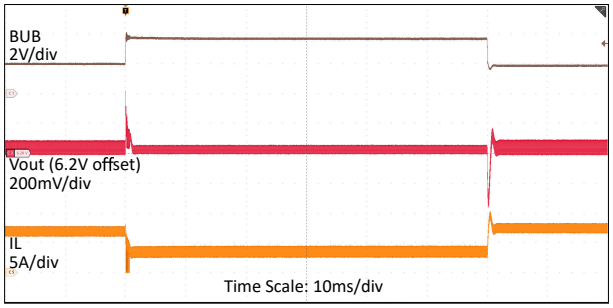
V_{BUB} = 3.6V V_{OUT} = 6.2V I_{OUT} = 10mA to 4A

Figure 8-7. Load Transient at Boost Mode



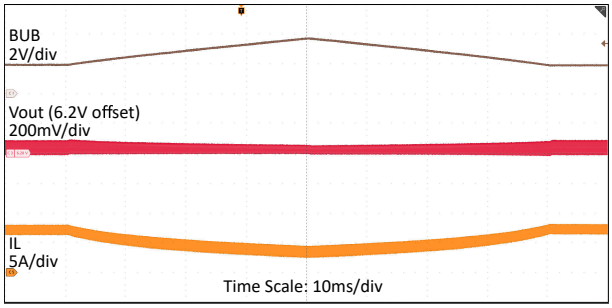
V_{BUB} = 3.6V V_{OUT} = 6.2V I_{OUT} = 10mA to 4A

Figure 8-8. Load Sweep at Boost Mode



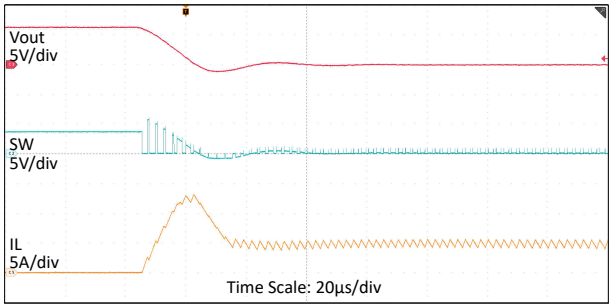
V_{BUB} = 2.5V to 4V V_{OUT} = 6.2V I_{OUT} = 2A

Figure 8-9. Line Transient at Boost Mode



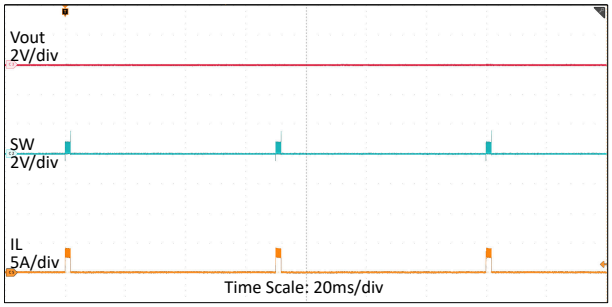
V_{BUB} = 2.5V to 4V V_{OUT} = 6.2V I_{OUT} = 2A

Figure 8-10. Line Sweep at Boost Mode



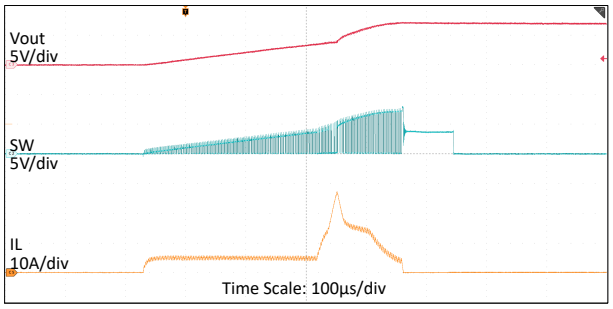
V_{BUB} = 3.6V V_{OUT} = 6.2V

Figure 8-11. Boost Output Short Protection



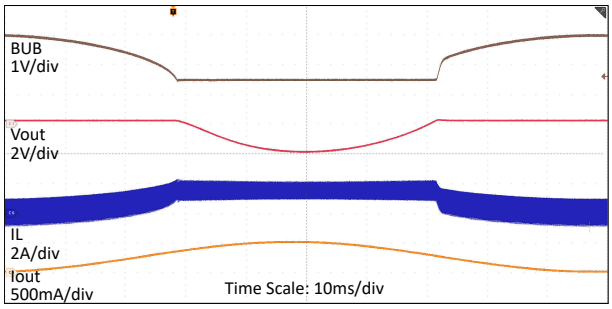
V_{BUB} = 3.6V V_{OUT} = 6.2V

Figure 8-12. Boost Output Short Hiccup



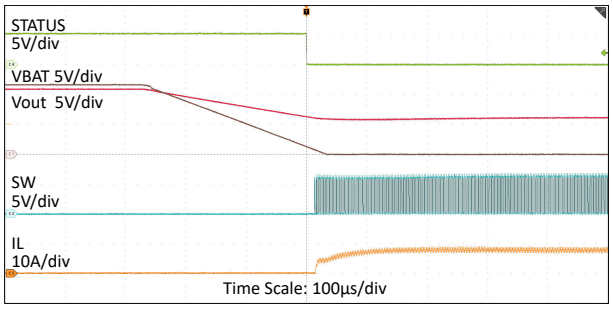
V_{BUB} = 3.6V V_{OUT} = 6.2V

Figure 8-13. Boost Output Short Recovery



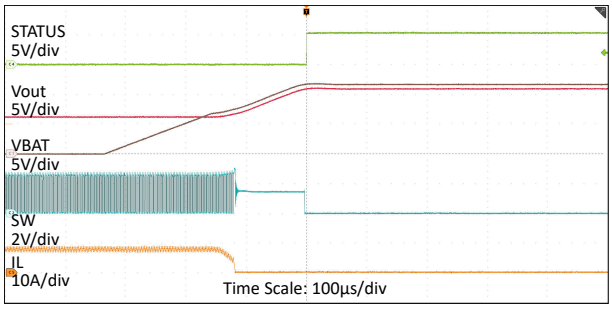
V_{BUB} = 4V R_{BUB} = 1Ω I_{OUT} = 0A to 500mA

Figure 8-14. BUB Loop



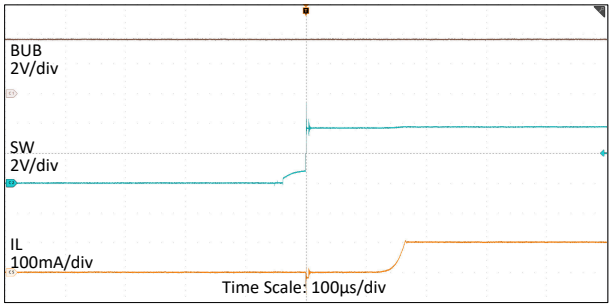
V_{BUB} = 3.6V V_{OUT} = 6.2V V_{BAT} = 12V-0V I_{OUT} = 4A

Figure 8-15. Transition into Boost Mode (12V Battery Interruption)



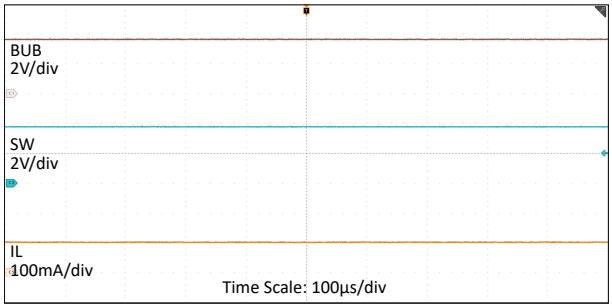
V_{BUB} = 3.6V V_{OUT} = 6.2V V_{BAT} = 0V-12V I_{OUT} = 4A

Figure 8-16. Transition into Standby Mode (12V Battery Recovery)



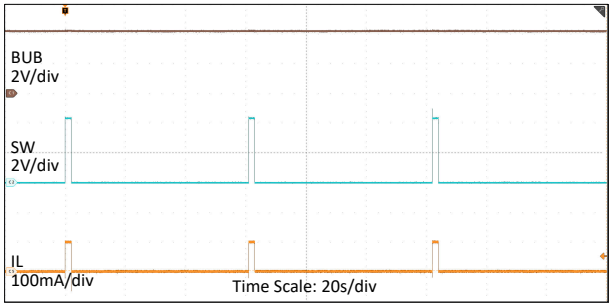
V_{BAT} = 12V V_{BUB} = 3.6V I_{CC} = 100mA

Figure 8-17. Charger Start up



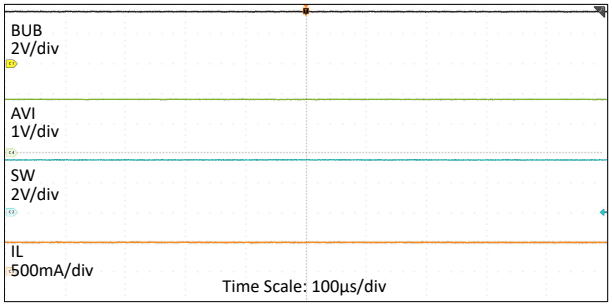
V_{BAT} = 12V V_{BUB} = 3.6V I_{CC} = 100mA

Figure 8-18. Charger Steady State



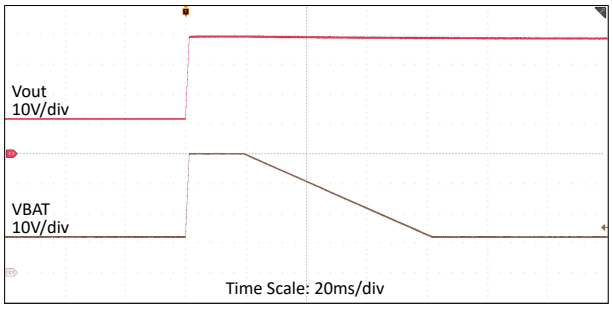
V_{BAT} = 12V V_{BUB} = 3.6V I_{CC} = 100mA

Figure 8-19. NiMH Intermittent Charge



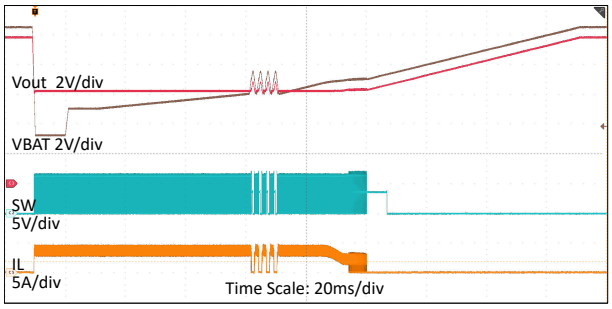
V_{BUB} = 3.6V $I_{Discharge}$ = 500mA AVI = BUB/2

Figure 8-20. SOH Steady State



V_{BAT} = 12V to 40V V_{BUB} = 3.6V I_{OUT} = 0A

Figure 8-21. 12V Battery Load Dump



V_{BUB} = 3.6V V_{OUT} = 6.2V I_{OUT} = 2A

Figure 8-22. 12V Battery Cold Crank

8.3 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with the following equation.

$$I_{BUB} = \frac{V_{out} \times I_{out}}{V_{BUB} \times \eta} \quad (24)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can result in LC resonant circuit. This can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 47µF to 100µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the excellent performance of the design. Bad PCB layout generates extral noise and therefore disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly in some preliminary tests, bad PCB layout still affects reliability and increases risk under mass production. Furthermore, the EMI performance of the regulator is dependent on the PCB layout to a great extent.

In a boost converter, the most EMI-critical PCB feature is the loop formed by the output capacitor and low side MOSFET ground. This loop carries discontinuous currents with high di/dt which generates high voltage spikes on layout parasitic inductance. Excessive transient voltages can disrupt the proper operation of the converter, affect EMI and even damage the MOSFET. In order to reduce parasitic inductance on layout, ceramic Cout need to be placed as close to Vout pin as possible (within 1mm) and low side MOSFET Q1 should be placed as close to SW pin as possible. TI also recommend a smaller Cout (100nF-1uF, 0603 package) closest to the Vout pin to bypass the high frequency noise. Avoid connecting this smaller Cout through vias.

Besides Cout loop, GND connection is also very important to avoid switching noise form affecting the IC. There are risks that the IC internal circuit get out of control or even damage if AGND is not connected correctly. Make sure that there's a separate AGND from PGND and connect VCC, COMP , AGND pin, thermal pad to AGND. AGND need to be connected to PGND by single point (net-tie, 0ohm resistor or 10-20mil width trace). The net-tie should be connected by a seprate, short trace between low side MOSFET source (PGND) and AGND pad of VCC capacitor. View Section 8.4.2 for detailed routing eaxmple on GND connection.

Place the VCC capacitor close to the VCC pin and AGND pin: This capacitor must be routed with short, wide traces to the VCC pin and AGND pin.

Make layer 2 of the PCB a ground plane: This plane operates as a noise shield and as a heat dissipation path. Using layer 2 as GND plane reduces the enclosed area of the Cout loop and reduces parasitic inductance.

Provide wide polygon pour for IL, SW, VOUT, and PGND(Low side MOSFET source): These paths must be as wide and direct as possible to reduce any voltage drops on the input or output paths of the converter to maximize efficiency.

Provide enough copper plane for proper heat sinking: Enough copper area must be applied to ensure low $R_{\theta JA}$ under heavy load and high temperature. Apply at least 4-layer board with two-ounce copper the top and bottom PCB layers. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces can be used for all pins except where noise considerations dictate minimization of area

8.4.2 Layout Example

According to the previous analysis on GND connection. The net-tie between AGND and PGND should be connected between source of the low side MOSFET and AGND pad of VCC capacitor. Driver current return path is cut out from PGND copper and routed seprately in pararllel with the gate trace as differential pairs so that their mutual inductance can eliminate parasite inductance. Also, VCC Cap should be placed closed to the IC as possible.

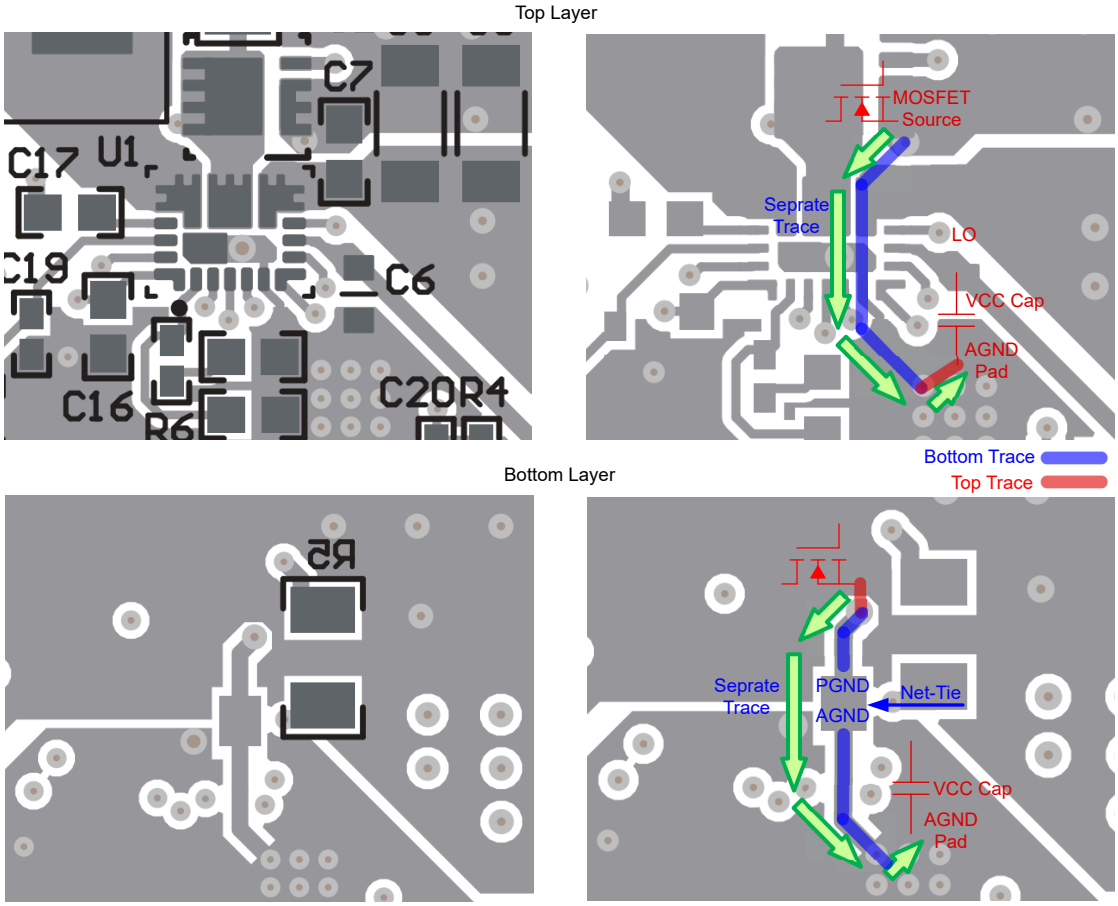


Figure 8-23. GND Connection Layout Example

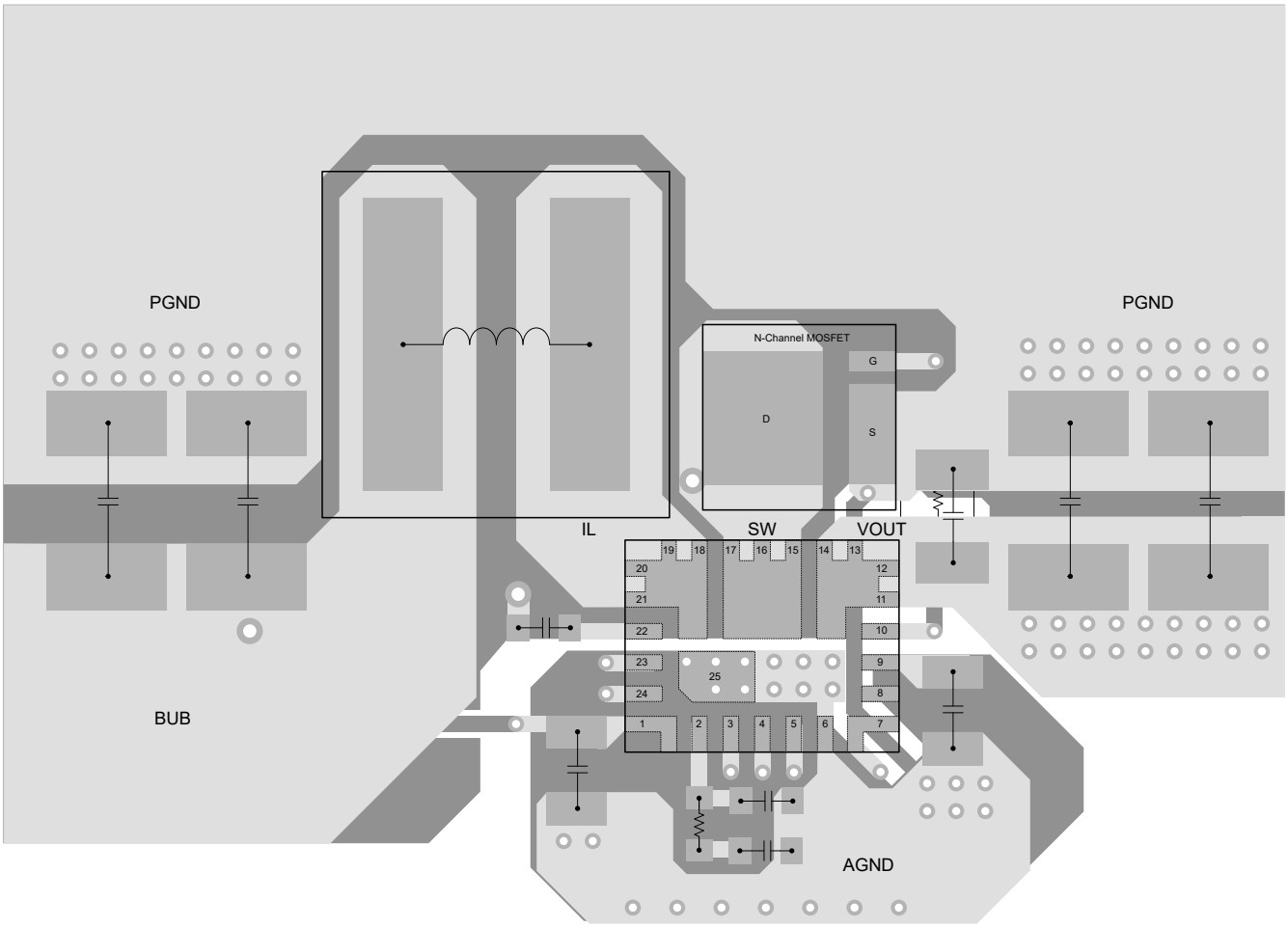


Figure 8-24. TPS61381Q typical layout top layer

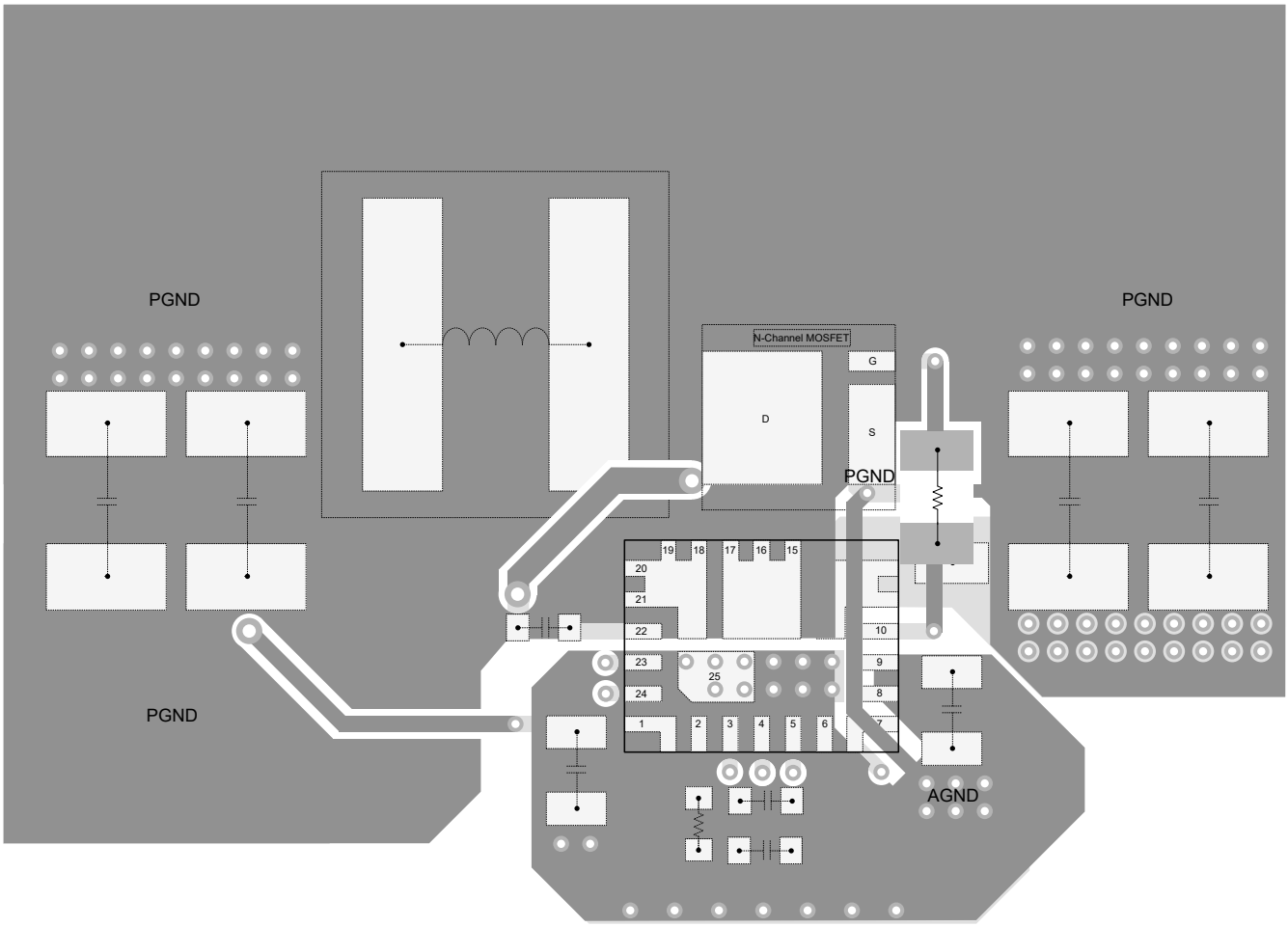


Figure 8-25. TPS61381Q typical layout top bottom

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Performing Accurate PFM Mode Efficiency Measurements Application Report*
- Texas Instruments, *Accurately Measuring Efficiency of Ultra-low-IQ Devices Technical Brief*
- Texas Instruments, *IQ: What it is, What it isn't, and How to Use it Techanical Brief*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
March 2024	*	Initial release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61381QRAVRQ1	Active	Production	WQFN-FCRLF (RAV) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	S61381Q
TPS61381QRAVRQ1.A	Active	Production	WQFN-FCRLF (RAV) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	S61381Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

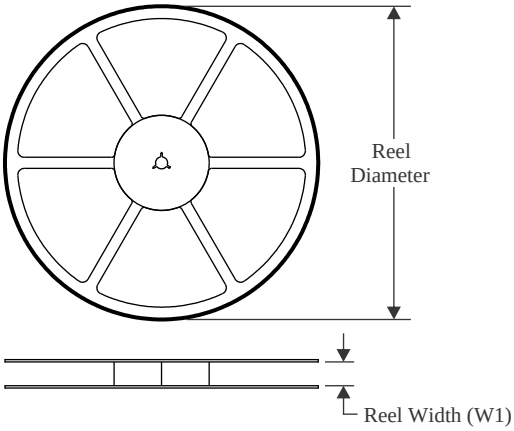
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

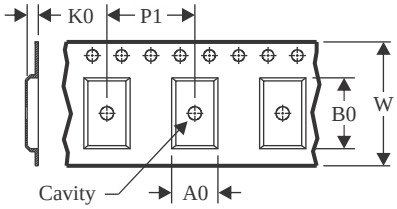
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

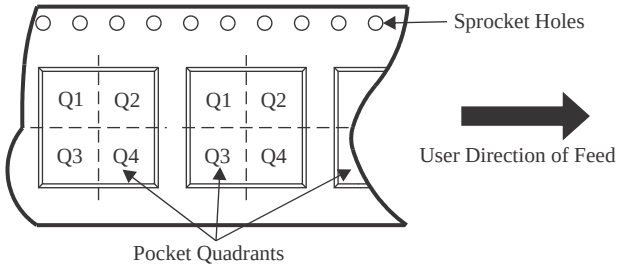


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

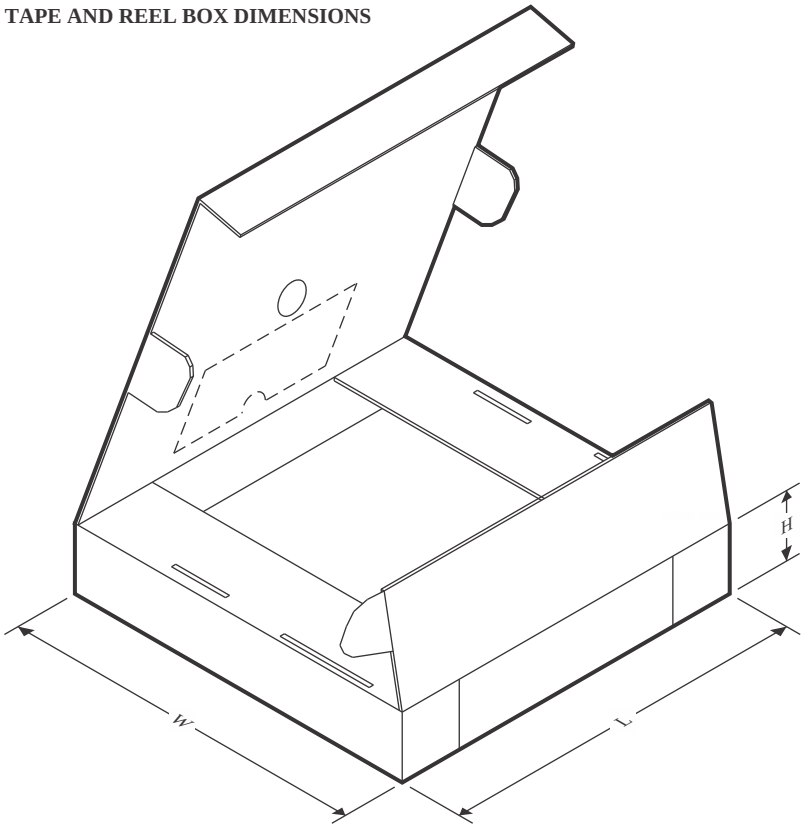
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61381QRAVRQ1	WQFN-FCRLF	RAV	24	3000	330.0	12.4	3.3	4.3	0.85	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

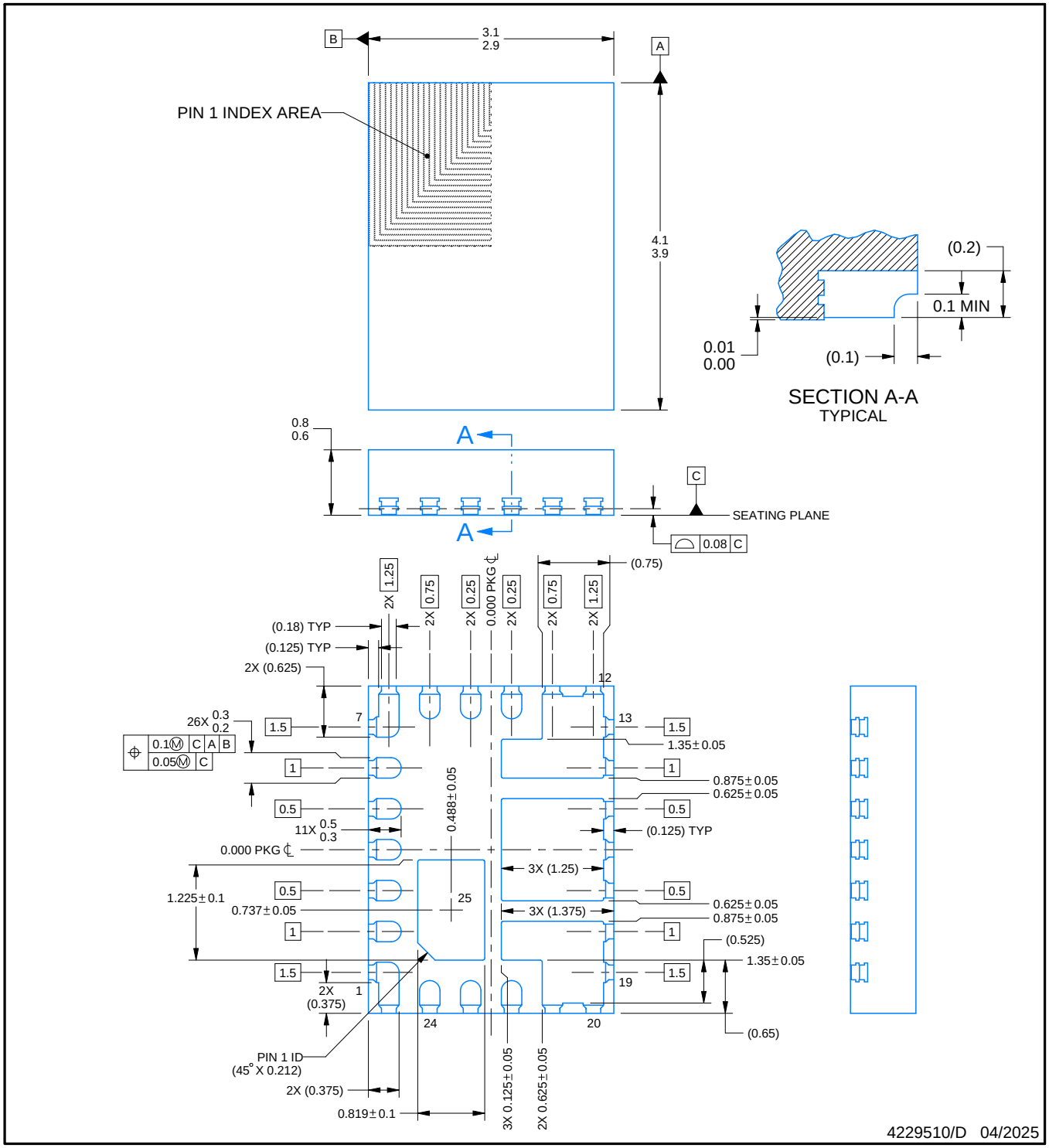
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61381QRAVRQ1	WQFN-FCRLF	RAV	24	3000	346.0	346.0	33.0

PACKAGE OUTLINE

RAV0024A

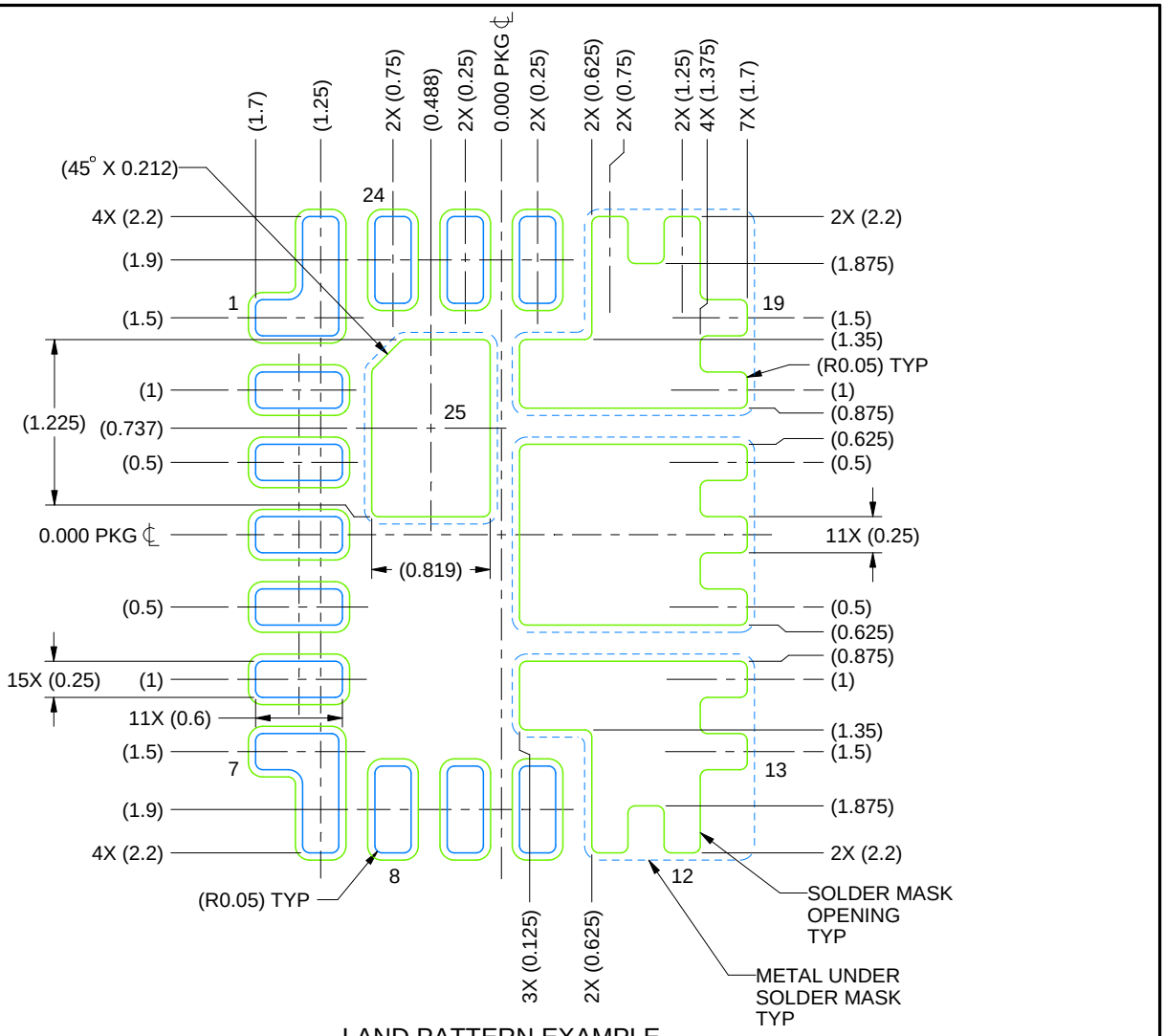
WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

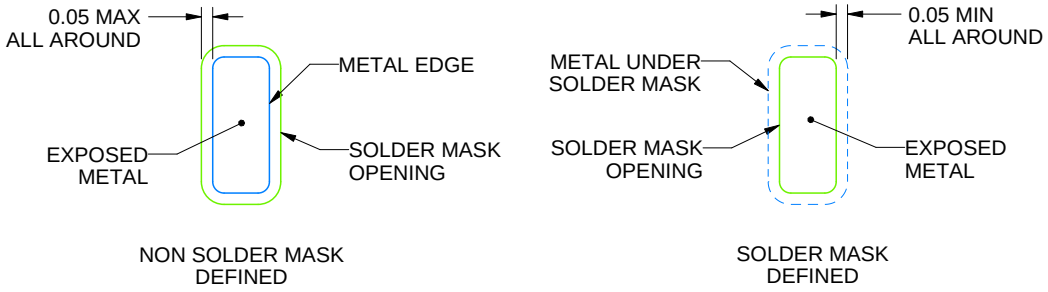


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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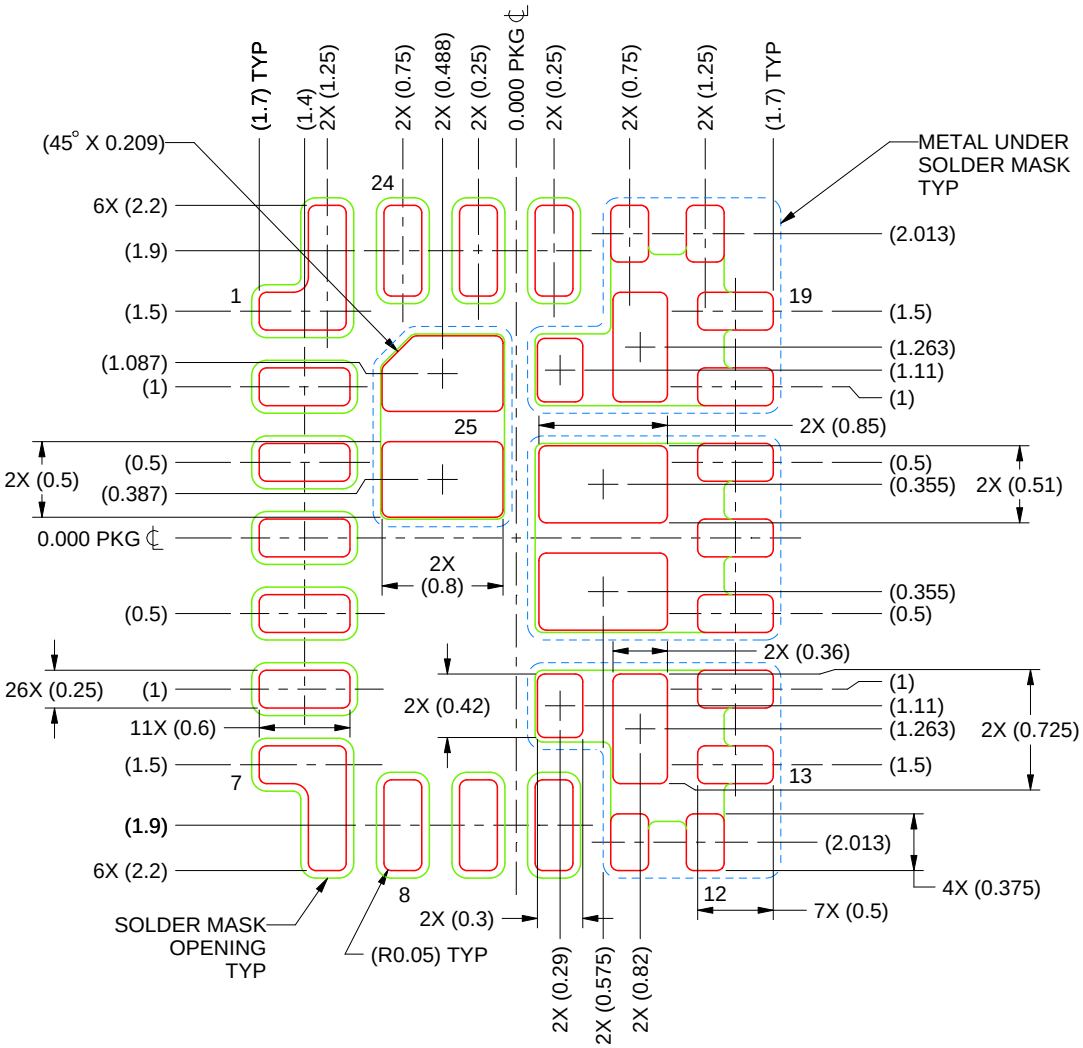
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
FUSED PAD 11 - 14 & 18-20: 62%
FUSED PAD 15-17: 68%
PAD 25: 79%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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