2-Gbps DIFFERENTIAL SWITCH 8-Bit, 1:2 MULTIPLEXER/DEMULTIPLEXER WITH 3-SIDE BAND SIGNALS

Check for Samples: TS3DV20812

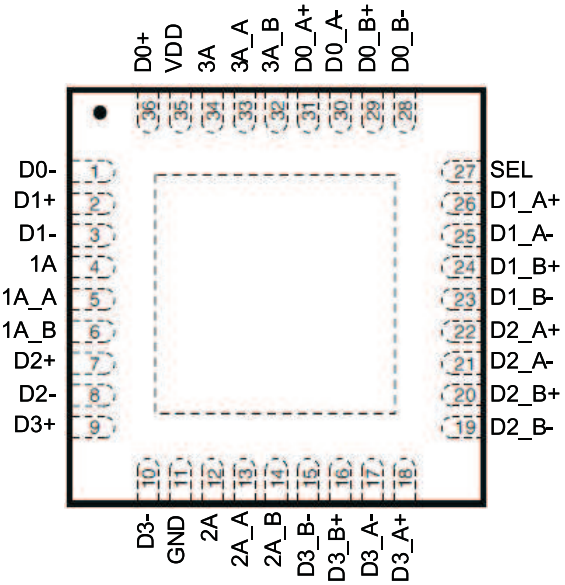
FEATURES

- Four High-Speed Bidirectional Differential Pair Channel MUX/DEMUX
- Supports up to 2 Gbps Data Rate
- V_{DD} Operating Range 2.5 V or 3.3
  - -0 V to 3.3 V Rail To Rail at 2.5 V
  - -0 V to 5 V Rail To Rail at 3.3V
- I_{OFF} partial Powerdown and Back-Drive Protection.
- 5-V Input Tolerant on Control Pin
- Supports Both AC- and DC-Coupled Signals
- Low Crosstalk: -38 dB at 825 MHz, 2.5 V or 3.3 V
- Insertion Loss: -1.5 dB at 825 MHz, 2.5 V or 3.3 V
- Off Isolation -24.67 dB at 825 MHz
- Low Bit-to-Bit Skew within Pair 5 ps Maximum
- Channel-to-Channel Skew: 30 ps Maximum
- Propagation Delay Times: 250 ps Maximum
- ESD Performance Tested per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

APPLICATIONS

- HDMI/DVI Video MUX
- Panel LVDS Bus MUX
- LVDS, LVPECL, CML
- Analog Signals VGA
- Gigabit LAN Signal MUX
- Serial Backplane Signal MUX
- Optical Module
- Central Office Telecommunication
- Wireless Base Station
- High-Speed Logic Data I/O MUX

RHH PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

TS3DV20812 is a High Speed Data Rate up to 2Gbps for Differential Signal Passive bi-directional Multiplexer and De-multiplexer for I/O rails up to 5V Level with Low Crosstalk and Insertion Loss.

TS3DV20812 can be used in either HDMI/DVI sink side or source side with 4-differential pair supporting the high speed and control pins.

The Ioff and back drive protection allowing to connect the external cable and prevent the back flow current when the Vcc is into 0V.

The 3 side band signals can be used in DDC (SDAL, SCL) and CEC Signal MUX.

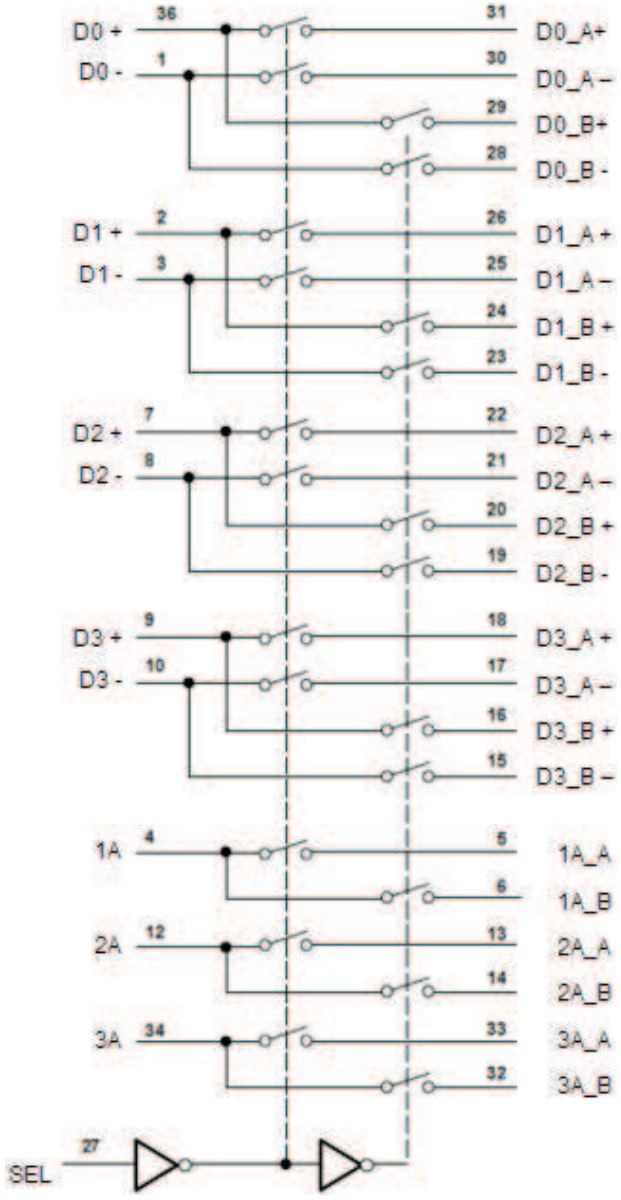
TS3DS20812 is characterized for operation from -40C to 85C.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RHH	Tape and reel	TS3DV20812RHH	TBD

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

LOGIC DIAGRAM



FUNCTION TABLE

INPUT SEL	DIFFERENTIAL SIGNAL I/Os	FUNCTIONS	
		A-PORT	B-PORT
L	Dn (±), nA (AUX (±), HPD, CAD/CEC)	DnA (±), nA_A	High-impedance mode
H		High-impedance mode	DnB (±), nA_B

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)	SEL	–0.5	7	V
		I/O	–0.5	7	V
V_{IO}	Switch I/O voltage range (all three I/O ports)(4)	D0-D3, Aux, HPD, CAD/CEC	–0.5	V_{CC} + 0.5	V
		A port and B port	–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	V_O < 0		–50	mA
I_{IO}	Continuous output current(5)	ON-state switch		±128	mA
	Continuous current through VDD or GND			±100	mA
Θ_{JA}	Package thermal impedance(6)	RHH package		31.8	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for V_{IO}.
(5) I_I and I_O are used to denote specific conditions for I_{IO}.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2.25	3. 6	V
V_{IH}	High-level control input voltage	SEL	2	5.5	V
V_{IL}	Low-level control input voltage	SEL	0	0.8	V
$V_{I/O}$	Input/output voltage	All ports	0	5.5	V
V_{ANALOG}	Analog signal range	Differential signal range	0	V_{DD}	V
V_I	Input tolerant	SEL	0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

for high-frequency switching over recommended operating free-air temperature range V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 3.6 V,	I_{IN} = –18 mA			–0.7	–1.2	V
I_{IH}	SEL	V_{DD} = 3.6 V,	V_{IN} = V_{DD}				±1	µA
I_{IL}	SEL	V_{DD} = 3.6 V,	V_{IN} = GND				±1	µA
I_{OFF}		V_{DD} = 06 V,	V_O = 0 to 3.6 V ,	V_I = 0 , V_{IN} = 0			1	µA
I_{CC}		V_{DD} = 3.6 V,	I_{IO} = 0	Switch ON or OFF		250	500	µA
C_{IN}	SEL	f = 10 MHz ,	V_{IN} = 0			2	2.5	pF
C_{OFF}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is OFF		2.5	4	pF
C_{ON}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is ON		8		pF
r_{ON}		V_{DD} = 3.6 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		4	6	Ω
$r_{ON(flat)}$ (3)		V_{DD} = 3.6 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.5		Ω
Δ r_{ON} (4)		V_{DD} = 3.6 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.4	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°.
(3) r_{ON}(flat) is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center (D0 to Dn) ports to any other port.

ELECTRICAL CHARACTERISTICS

for high-frequency switching over recommended operating free-air temperature range V_{DD} = 2.5 V ± 0.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 2.5 V ,	I_{IN} = –18 mA			–0.7	–1.2	V
I_{IH}	SEL	V_{DD} = 2.5 V ,	V_{IN} = V_{DD}				±1	µA
I_{IL}	SEL	V_{DD} = 2.5 V ,	V_{IN} = GND				±1	µA
I_{OFF}		V_{DD} = 06 V,	V_O = 0 to 2.5 V ,	V_I = 0 , V_{IN} = 0			1	µA
I_{CC}		V_{DD} = 2.5 V ,	I_{IO} = 0	Switch ON or OFF		250	500	µA
C_{IN}	SEL	f = 10 MHz ,	V_{IN} = 0			2	2.5	pF
C_{OFF}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is OFF		2.5	4	pF
C_{ON}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is ON		8		pF
r_{ON}		V_{DD} = 2.5 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		4	6	Ω
$r_{ON(flat)}$ (3)		V_{DD} = 2.5 V	V_I = 1.5 V and V_{DD},	I_O = –40 mA		0.5		Ω
Δ r_{ON} (4)		V_{DD} = 2.5 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.4	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 2.5 V (unless otherwise noted), T_A = 25°.
(3) r_{ON}(flat) is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center (D0 to Dn) ports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 9 and Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	Dn	D_A or D_B		149		ps
t_{PZH}, t_{PZL}	SEL	D_A or D_B	0.5		15	ns
t_{PHZ}, t_{PLZ}	SEL	D_A or D_B	0.9		12	ns
SEL to switch turn on time		D_A or D_B		9	14	ns
SEL to switch turn off time		D_A or D_B		5	11	ns
$t_{sk(o)}$ (3)	Dn (+)(-), DA(+)(-), DB(+)(-)			22	28	ps
$t_{sk(o)}$	Dn (all), DnA(all), DnB(All)			19	25	ps
$t_{sk(p)}$(4)				22	31	ps

(1) All typical values are at V_{DD} = 2.5 V (unless otherwise noted), T_A = 25°.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port to any other port.
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 2.5V ± 0.25 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 9 and Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	Dn	D_A or D_B		149		ps
t_{PZH}, t_{PZL}	SEL	D_A or D_B	0.5		14	ns
t_{PHZ}, t_{PLZ}	SEL	D_A or D_B	0.9		15	ns
SEL to switch turn on time		D_A or D_B		9	17	ns
SEL to switch turn off time	D_A or D_B	D_A or D_B		5	18	ns
$t_{sk(o)}$ (3)	Dn (+)(-), DA(+)(-), DB(+)(-)			22	31	ps
$t_{sk(o)}$	Dn (all), DnA(all), DnB(All)			19	23	ps
$t_{sk(p)}$(4)				22	33	ps

(1) All typical values are at V_{DD} = 2.5 V (unless otherwise noted), T_A = 25°.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port to any other port.
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 50 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Differential crosstalk	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 11	-34.67	dB
O_{IRR}	Differential OFF isolation	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 12	-19.09	dB
I_{LOSS}	Differential insertion loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, seeFigure 13	-2.84	dB
I_{RETURN}	Differential return loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 13	-9.43	dB
DR	Data rate		2.20	Gbps
BW	Differential bandwidth		1.10	Ghz

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 2.5 V ± 0.25 V, R_L = 50 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Differential crosstalk	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 7	-34.94	dB
O_{IRR}	Differential OFF isolation	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 8	-18.39	dB
I_{LOSS}	Differential insertion loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 9	-3.07	dB
I_{RETURN}	Differential return loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 9	-9.56	dB
DR	Data rate		2.20	Gbps
BW	Differential bandwidth		1.10	Ghz

TYPICAL PERFORMANCE

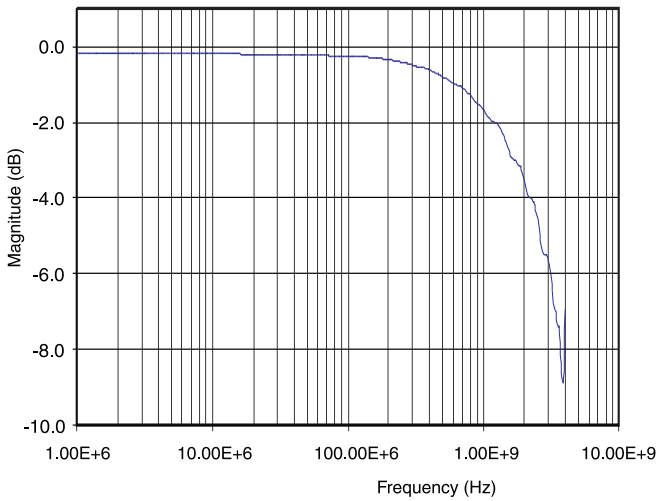


Figure 1. Differential Gain vs Frequency

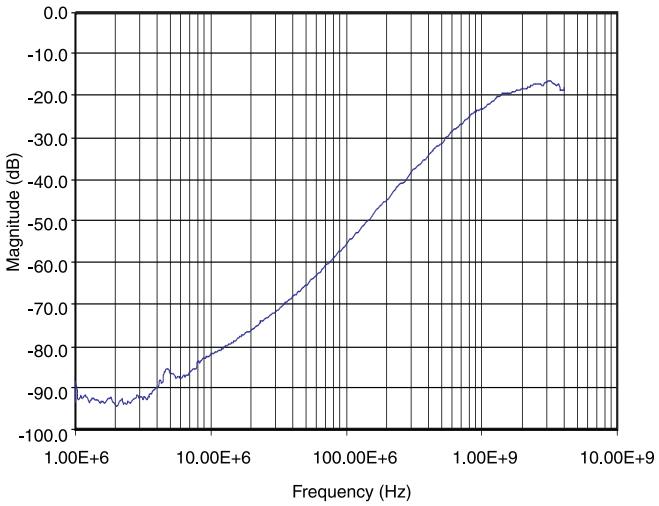


Figure 2. Differential Off Isolation vs Frequency

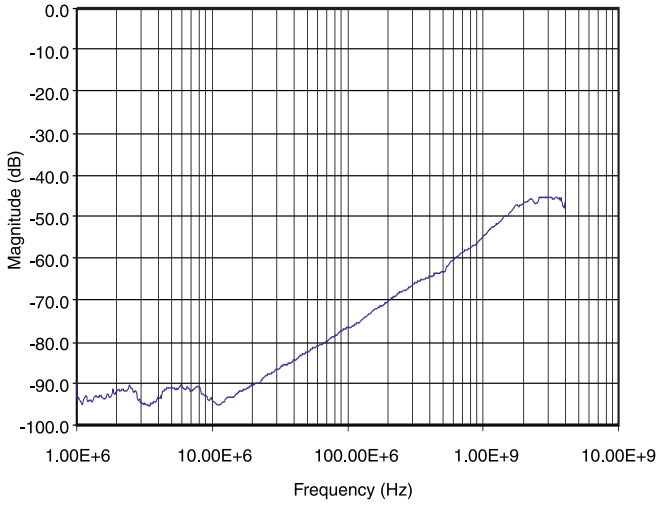


Figure 3. Differential Crosstalk vs Frequency

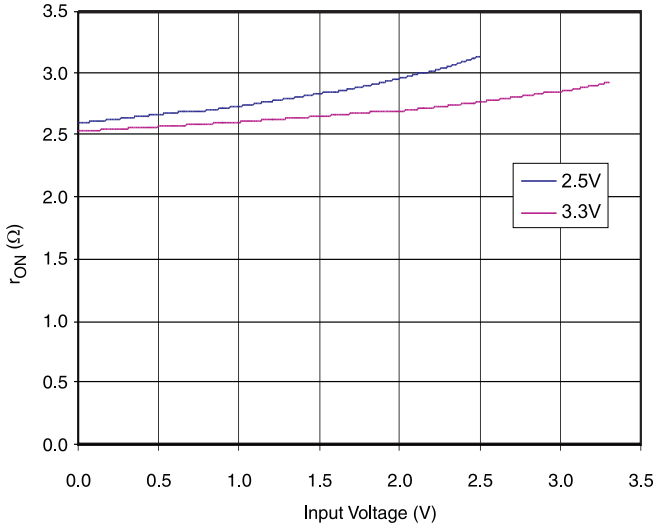


Figure 4. r_{ON} vs V_{COM} (Differential Switch)

APPLICATION INFORMATION

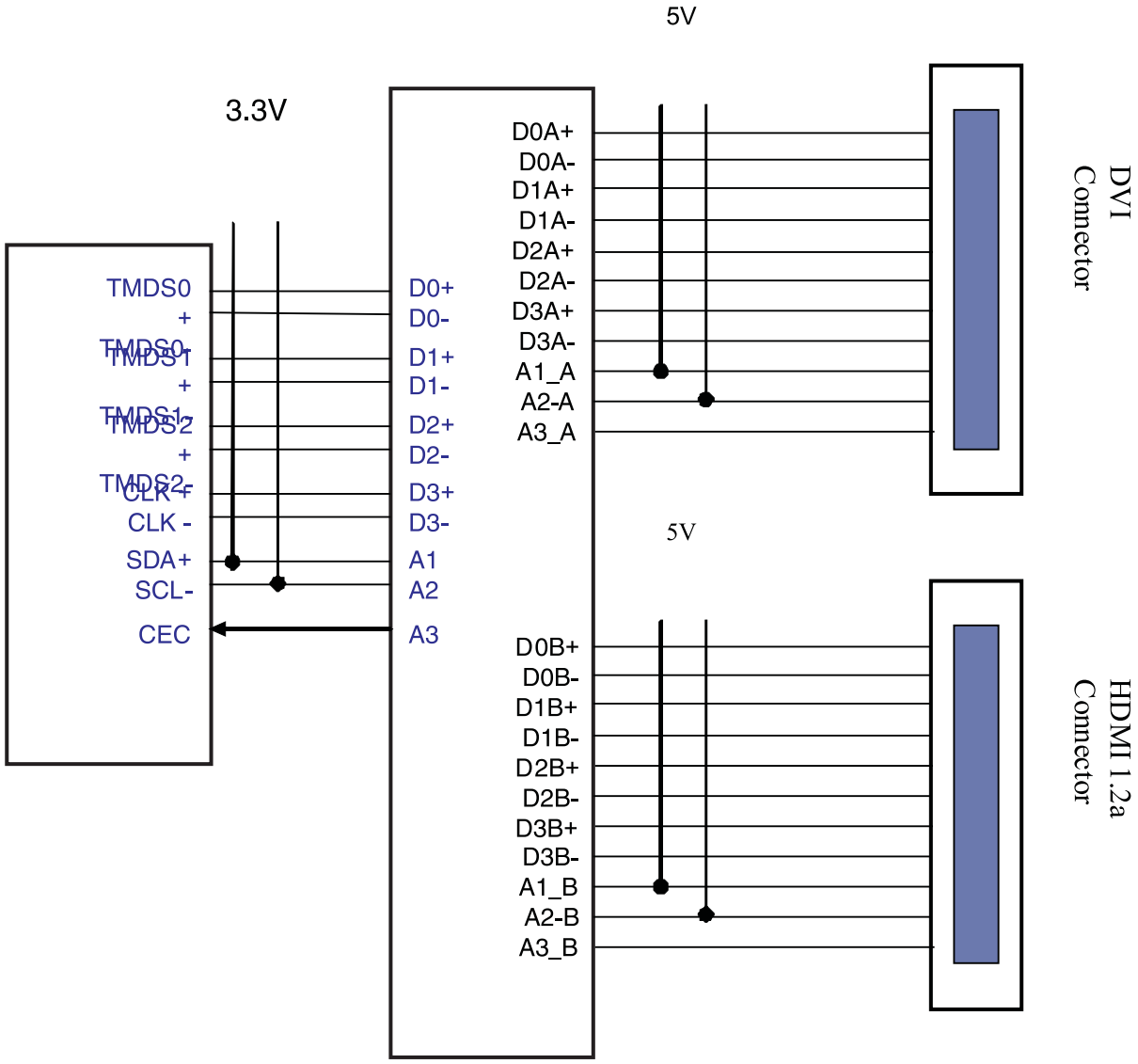


Figure 5. Typical Application Switching HDMI 1.2a and DVI

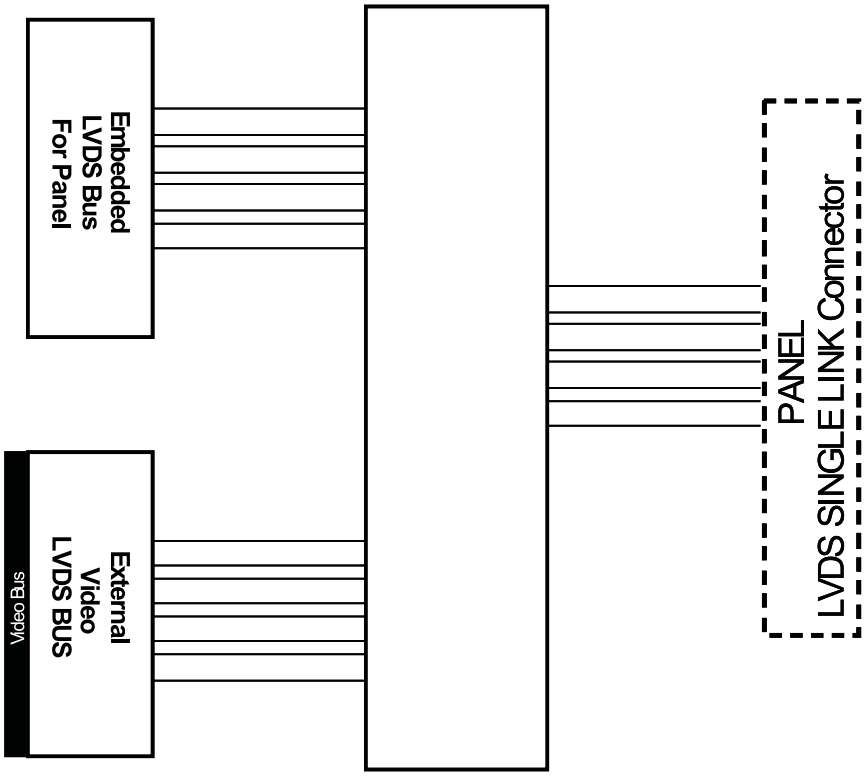
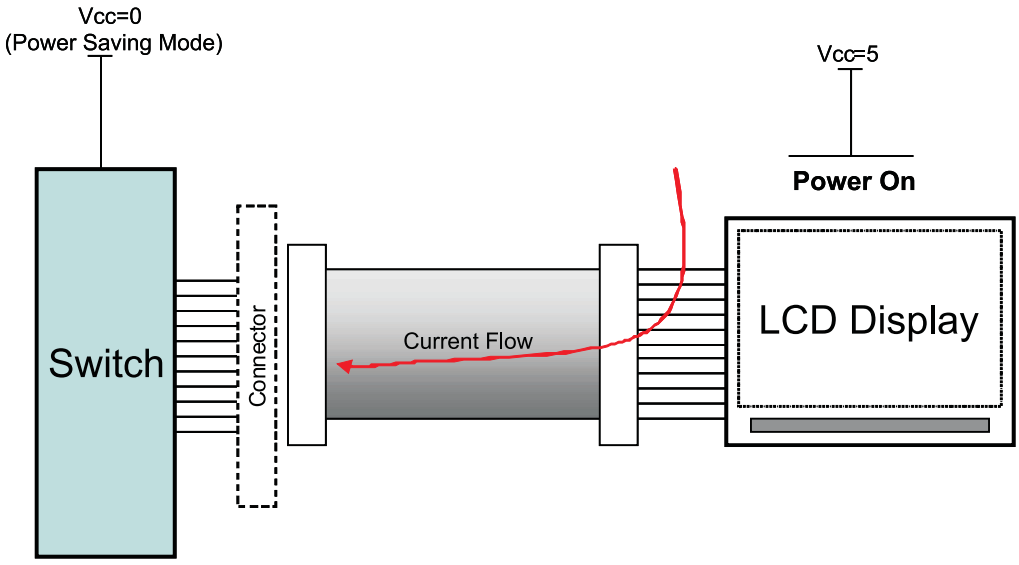


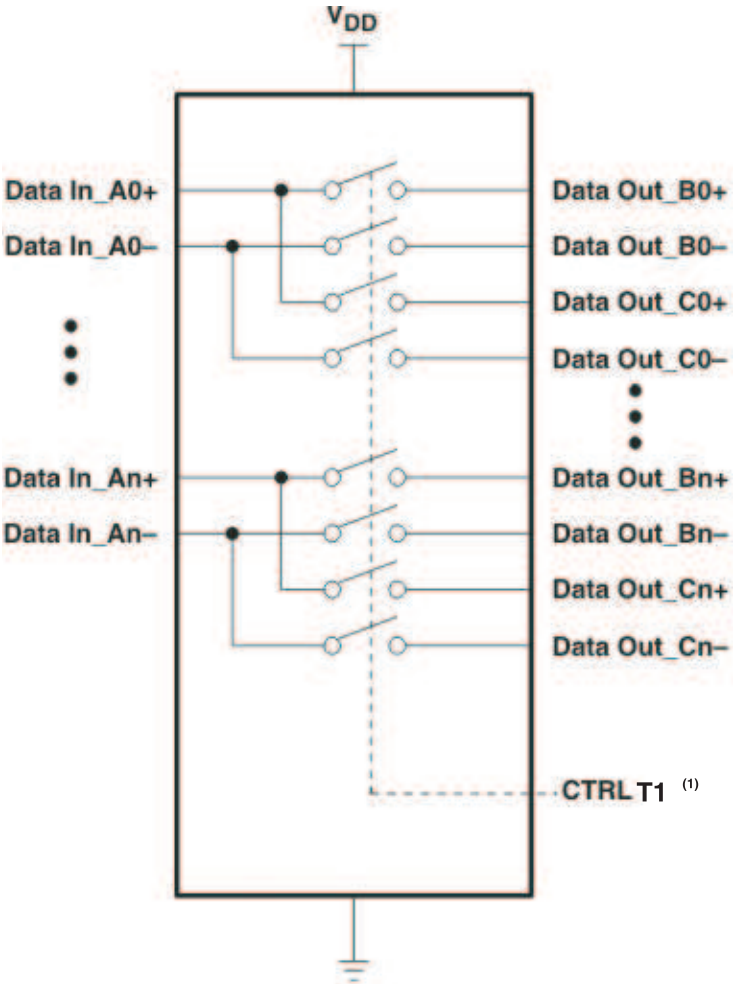
Figure 6. Typical Application for Dual LVDS



A. The switch already has I_{OFF} circuit and it will reduce the current flow leakage limit to 10 μA maximum and it will prevent the damage from back drive current flow from the power-on circuit.

Figure 7. I_{OFF} (Back Drive Protection)

PARAMETER MEASUREMENT INFORMATION

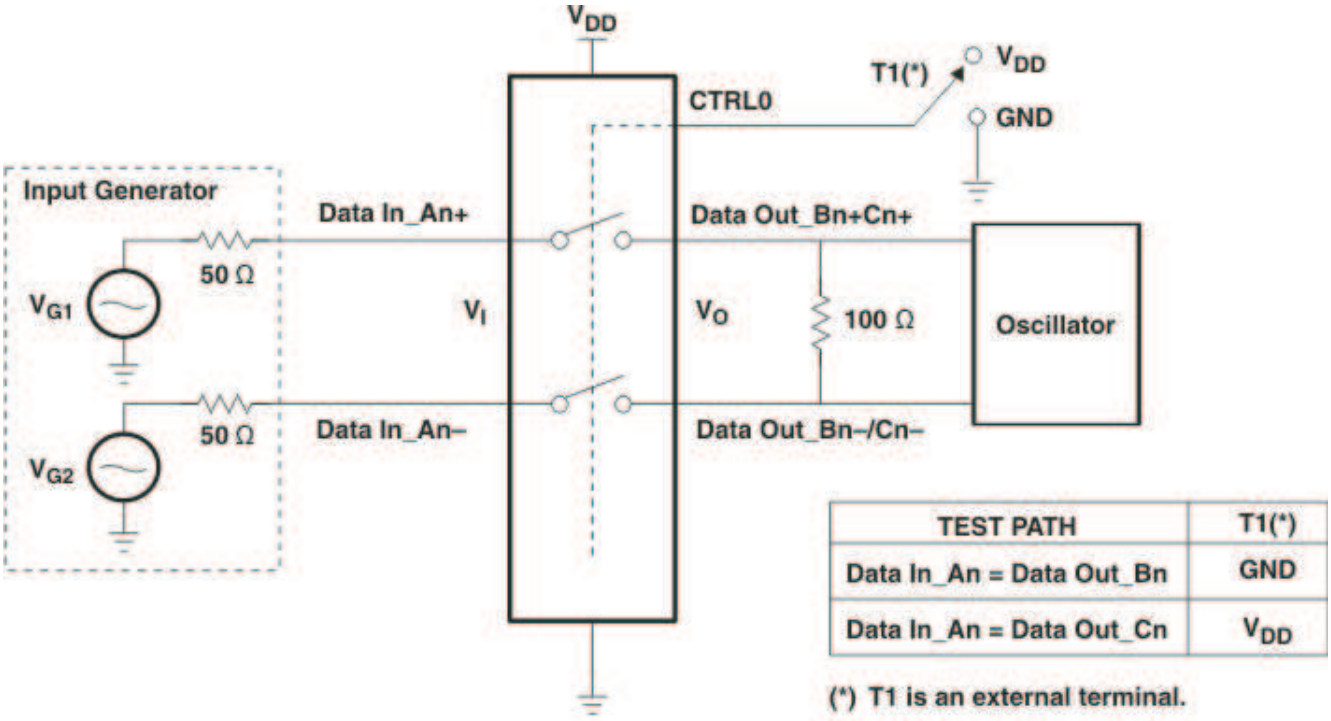


TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

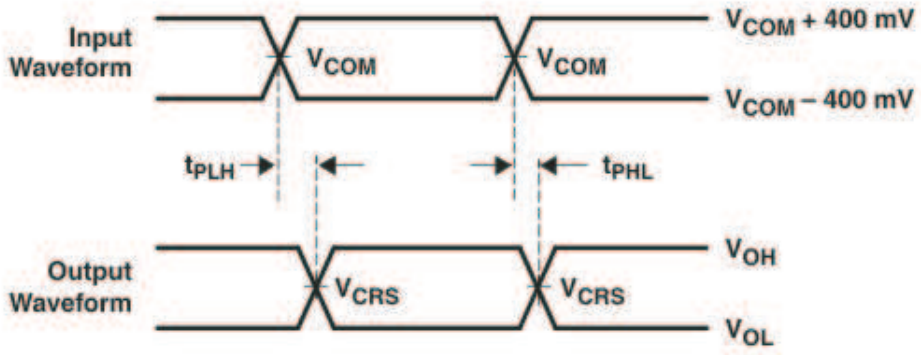
Figure 8. Differential Signaling Device

PARAMETER MEASUREMENT INFORMATION (continued)



TEST PATH	T1(*)
Data In_An = Data Out_Bn	GND
Data In_An = Data Out_Cn	V_{DD}

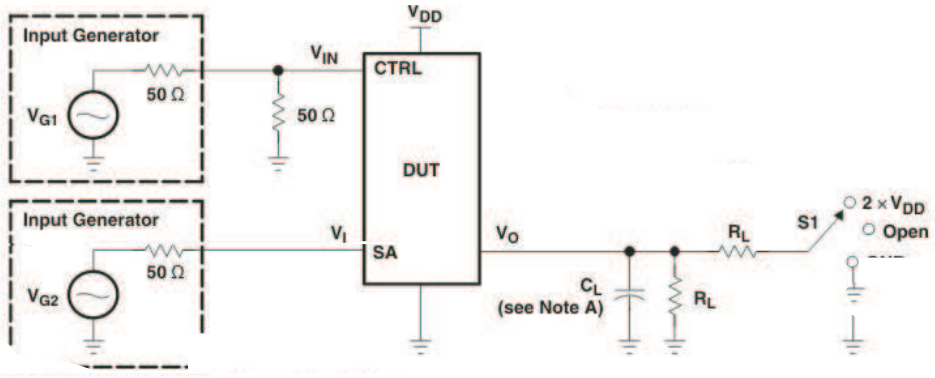
(*) T1 is an external terminal.



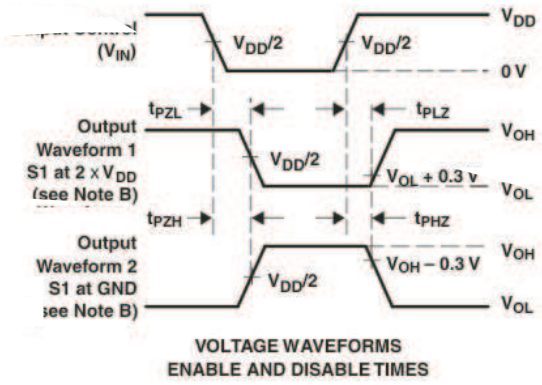
V_{COM} = 1.5 V
V_{CRS} is the cross-point of the differential signal.
$t_{sk} = |t_{PLHn} - t_{PHLn}|$

Figure 9. Test Circuit for Propagation Delay and Intra-Pair Skew

PARAMETER MEASUREMENT INFORMATION (continued)



TEST	V_{DD}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ±300 mV	2 × V_{DD}	100 Ω	GND	No load	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ±300 mV	GND	100 Ω	V_{DD}	No load	0.3 V

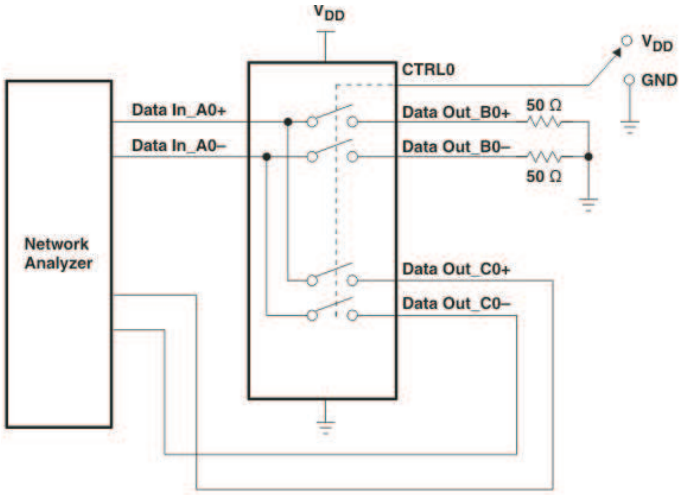


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 ohm, tr ≤ 2.5 ns, tf ≤ 2.5 ns
D. The outputs are measured one at a time, with one transition per measurement.
E. tPLZ and tPHZ are the same as tdis.
F. tPZL and tPZH are the same as ten.

Figure 10. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



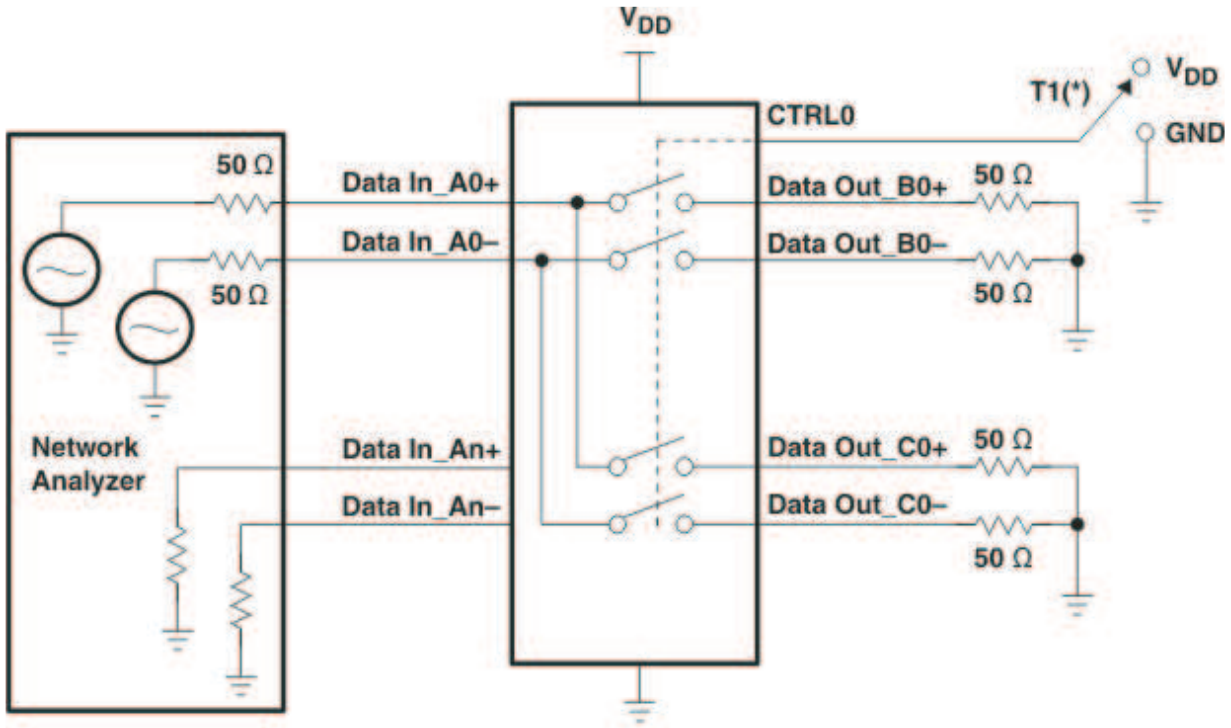
TEST	VNA MEASUREMENT
Differential insertion loss	S_{21}
Differential return loss	S_{11}
Common-mode insertion loss	S_{21}

TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

Figure 11. Differential Crosstalk Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



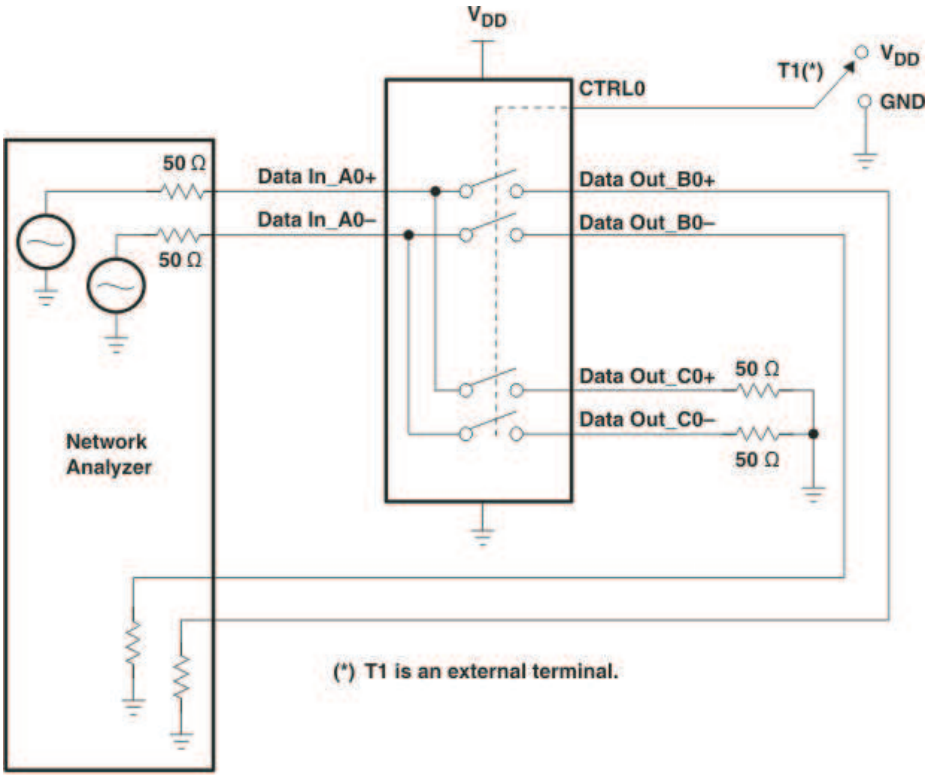
(*) T1 is an external terminal.

TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

Figure 12. Differential OFF Isolation Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

Figure 13. Differential Insertion Loss, Return Loss, and Common-Mode Insertion Loss Test Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3DV20812RHHR	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SY812
TS3DV20812RHHR.B	Active	Production	VQFN (RHH) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	SY812

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

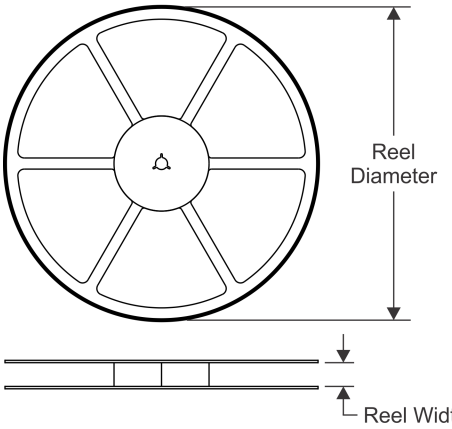
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

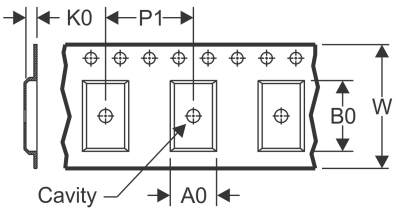
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

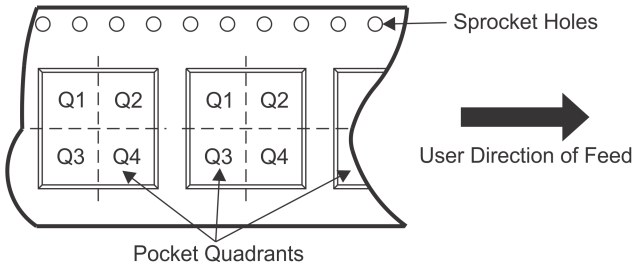


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

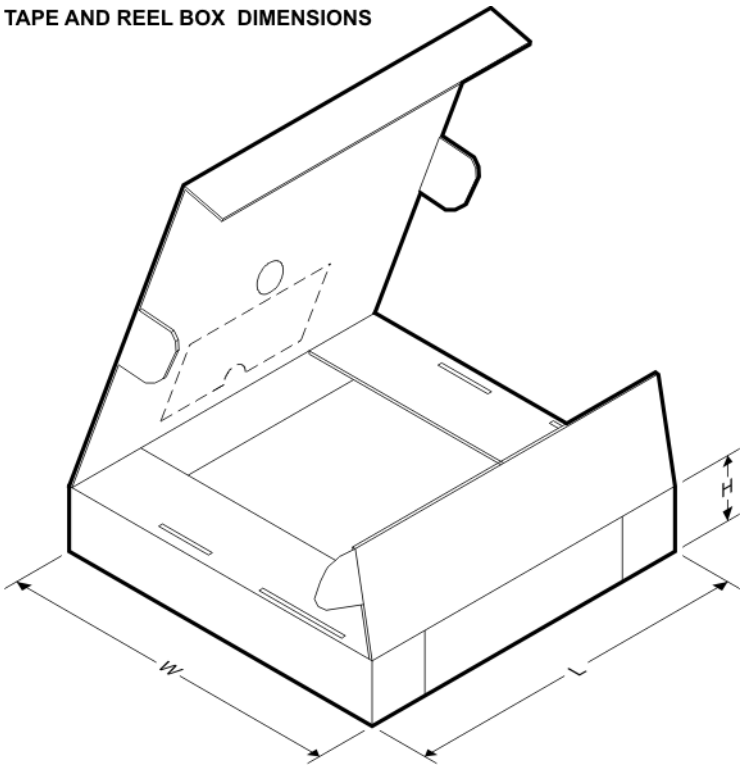
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV20812RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV20812RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

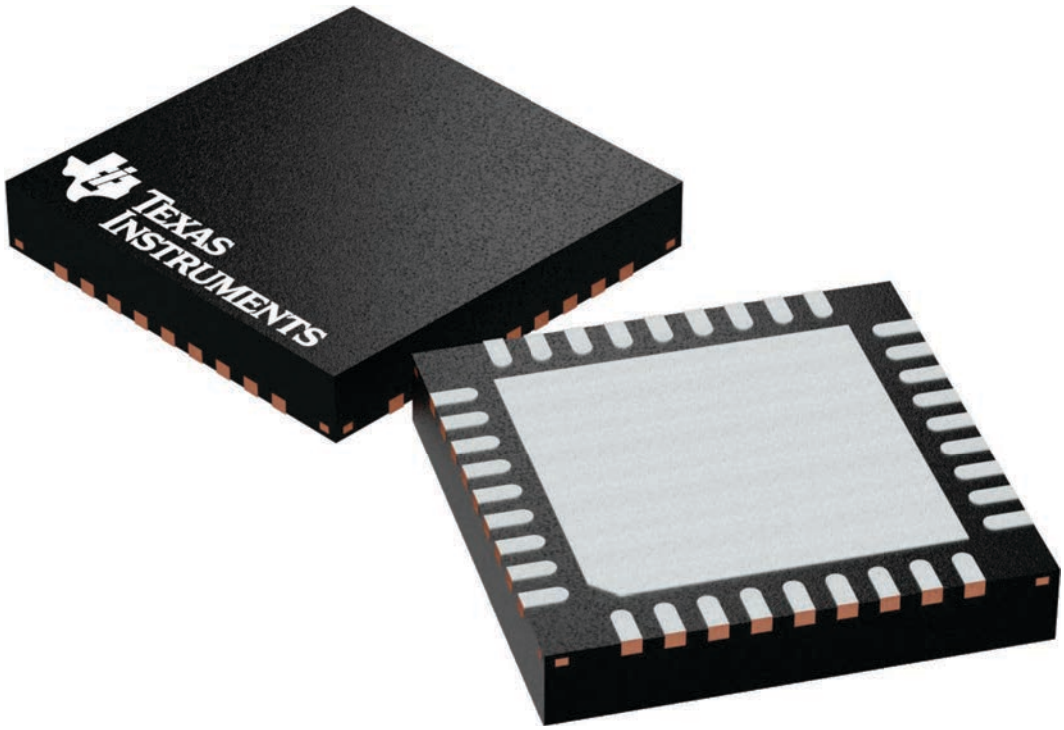
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



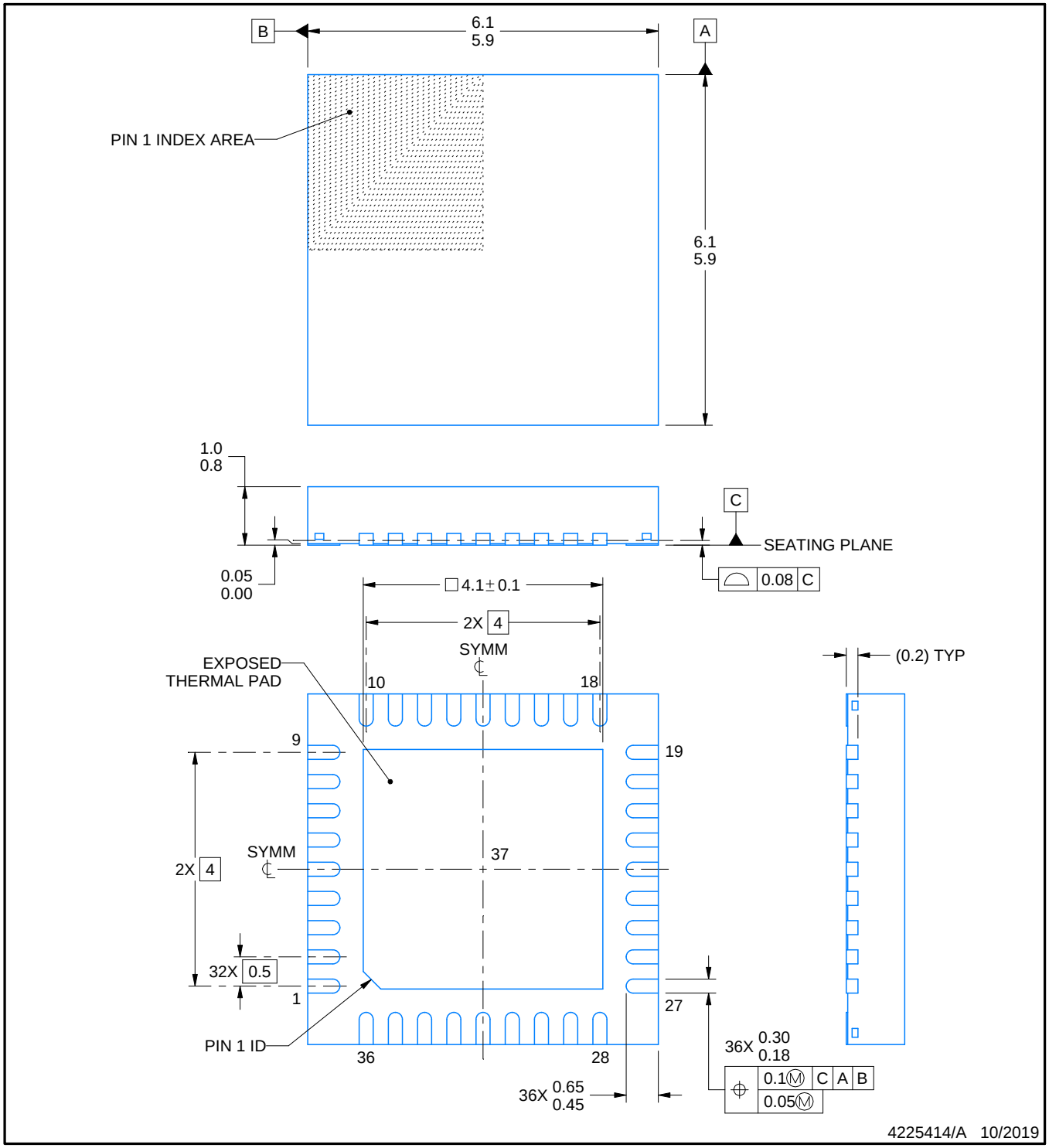
4225440/A

RHH0036B

PACKAGE OUTLINE

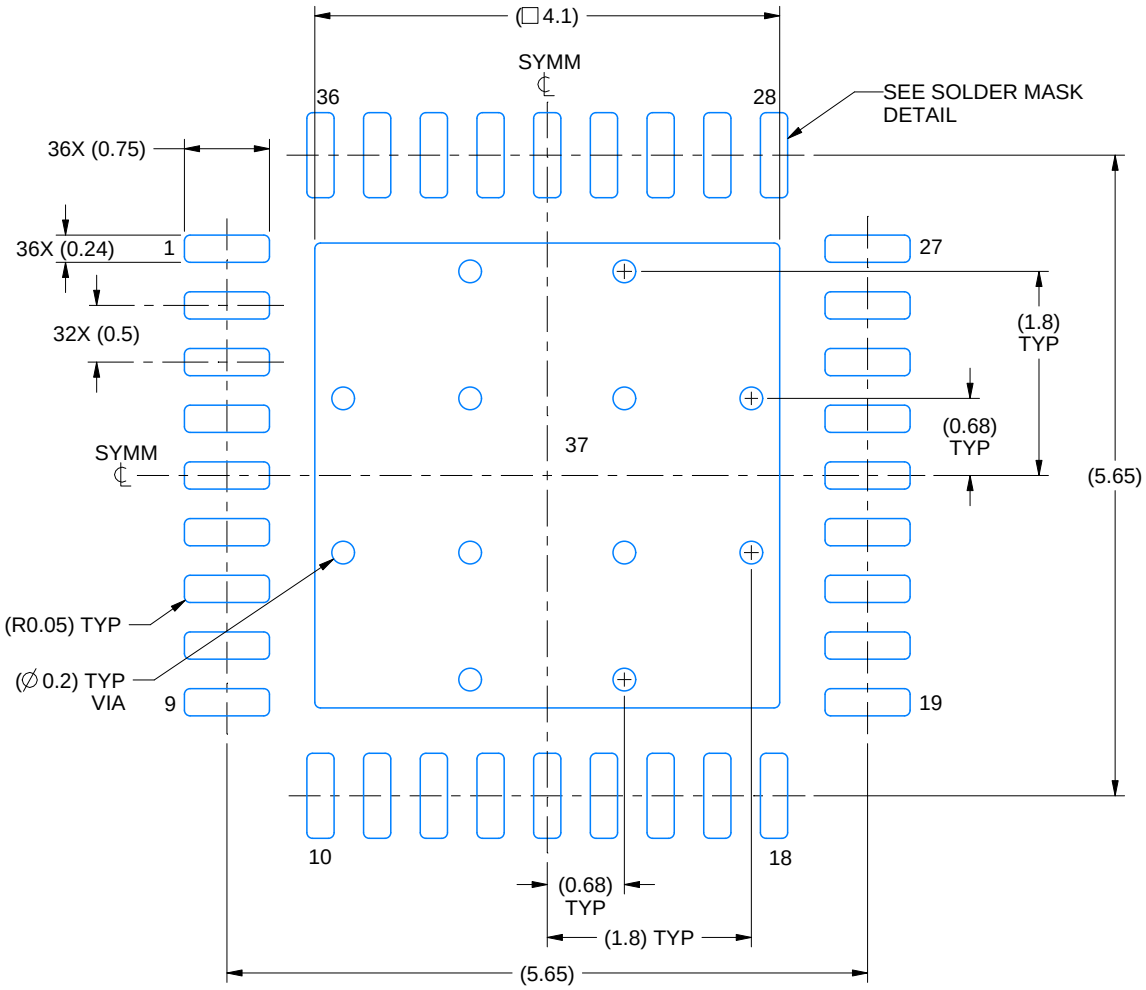
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

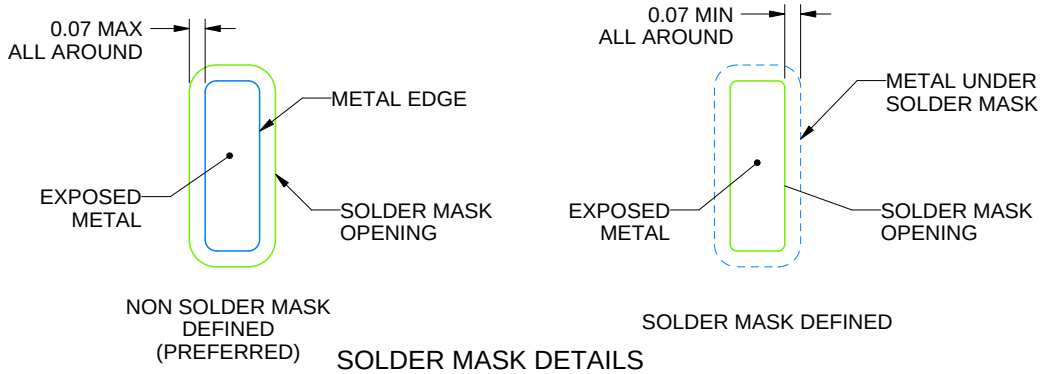


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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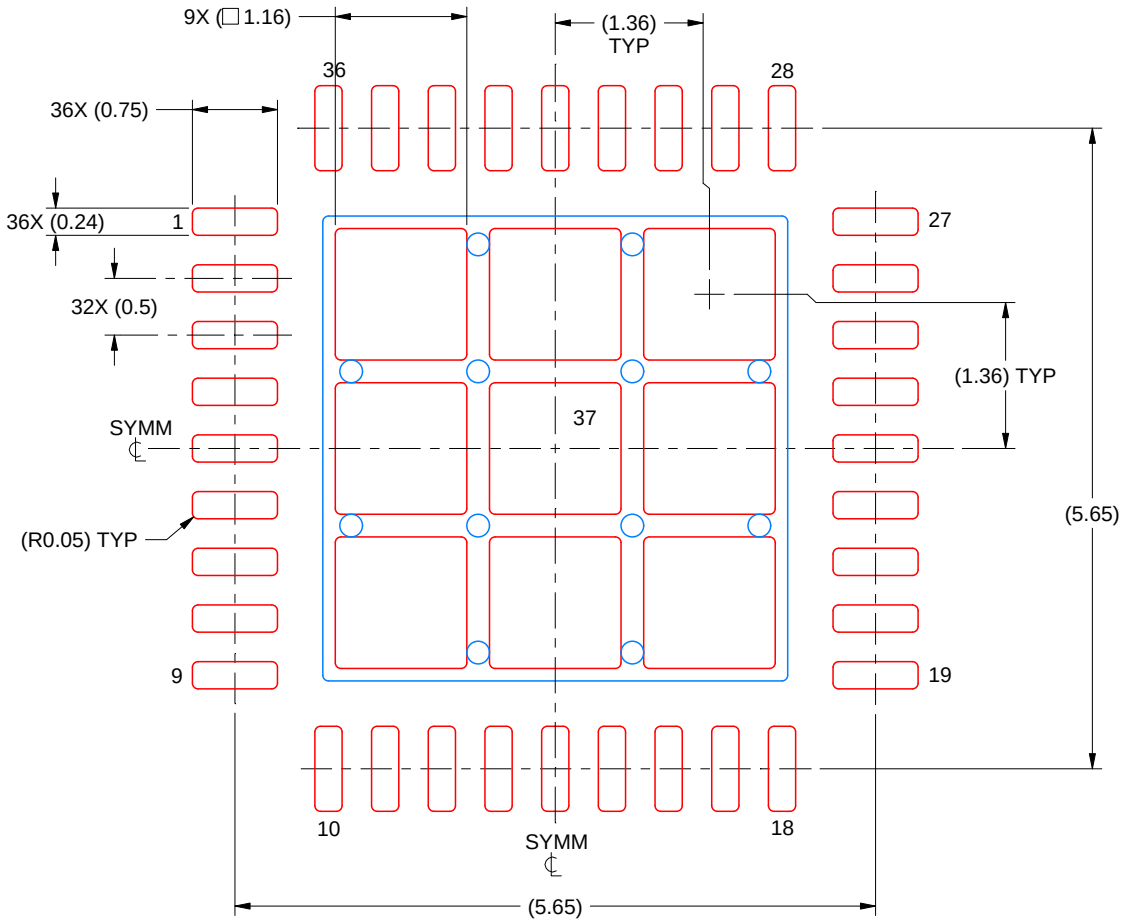
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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