16-BIT 250-KSPS SAMPLING CMOS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **105dB SFDR at 250-kHz Sample Rate**
- **Standard ±10-V Input Range**
- **±1.5 LSB Max INL**
- **±1 LSB Max DNL, 16-Bits No Missing Codes**
- **±2 mV Max Bipolar Zero Error With ±0.4 PPM/°C Drift**
- **±0.1% FSR Max Full-Scale Error With ±2 PPM/°C Drift**
- **Single 5-V Supply Operation**
- **Pin-Compatible With ADS7805 (Low Speed) and 12-Bit ADS8504/7804**
- **Uses Internal or External Reference**
- **Full Parallel Data Output**
- **70-mW Typ Power Dissipation at 250 KSPS**
- **28-Pin SSOP and SOIC Packages**

APPLICATIONS

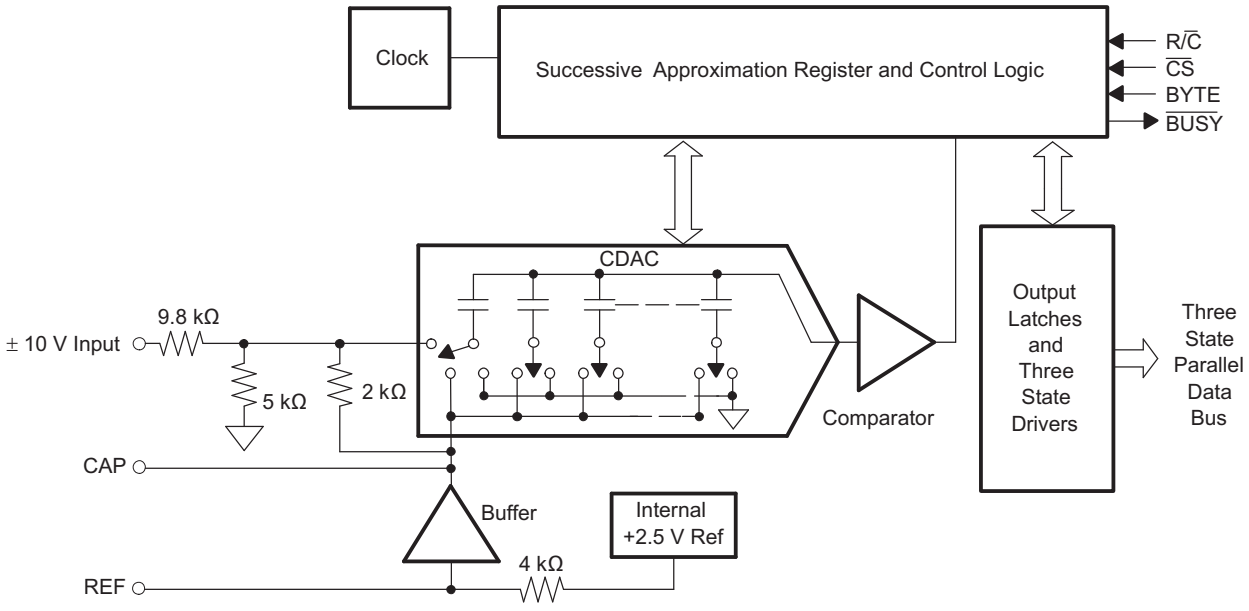
- **Industrial Process Control**
- **Data Acquisition Systems**
- **Digital Signal Processing**
- **Medical Equipment**
- **Instrumentation**

DESCRIPTION

The ADS8505 is a complete 16-bit sampling A/D converter using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and 3-state output drivers.

The ADS8505 is specified at a 250-kHz sampling rate over the full temperature range. Precision resistors provide an industry standard ±10-V input range, while the innovative design allows operation from a single +5-V supply, with power dissipation under 100 mW.

The ADS8505 is available in 28-pin SOIC and 28-pin SSOP packages, both fully specified for operation over the industrial –40°C to 85°C temperature range.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	NO MISSING CODE	MINIMUM SINAD (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8505IB	±1.5	16	86	–40°C to 85°C	SO-28	DW	ADS8505IBDW	Tube, 20
							ADS8505IBDWR	Tape and Reel, 1000
					SSOP-28	DB	ADS8505IBDB	Tube, 50
							ADS8505IBDBR	Tape and Reel, 2000
ADS8505I	±4	15	83	–40°C to 85°C	SO-28	DW	ADS8505IDW	Tube, 20
							ADS8505IDWR	Tape and Reel, 1000
					SSOP-28	DB	ADS8505IDB	Tube, 50
							ADS8505IDBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)(2)

		UNIT
Analog inputs	V_{IN}	±25V
	REF	$+V_{ANA}$ + 0.3 V to AGND2 – 0.3 V
	CAP	Indefinite short to AGND2, momentary short to V_{ANA}
Ground voltage differences	DGND, AGND1, AGND2	±0.3 V
	V_{ANA}	6 V
	V_{DIG} to V_{ANA}	0.3 V
	V_{DIG}	6 V
Digital inputs		–0.3 V to $+V_{DIG}$ + 0.3 V
Maximum junction temperature		165°C
Internal power dissipation		825 mW
Lead temperature (soldering, 10s)		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (unless otherwise noted)

PARAMETER	TEST CONDITIONS	ADS8505I			ADS8505IB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				16			16	Bits
ANALOG INPUT								
Voltage range			±10			±10		V
Impedance			11.5			11.5		kΩ
Capacitance			50			50		pF
THROUGHPUT SPEED								
Conversion cycle	Acquire and convert			4			4	µs
Throughput rate		250			250			kHz

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS8505I			ADS8505IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY									
INL	Integral linearity error		–4		4	–1.5		1.5	LSB(1)
DNL	Differentiall linearity error		–2		2	–1		1	LSB(1)
	No missing codes		15			16			Bits
	Transition noise(2)			0.77			0.77		LSB
	Full-scale error(3)(4)	Int. ref.	–0.5		0.5	–0.25		0.25	%FSR
	Full-scale error drift	Int. ref.		±7			±7		ppm/°C
	Full-scale error(3)(4)	Ext. 2.5-V ref.	–0.25		0.25	–0.1	±0.01	0.1	%FSR
	Full-scale error drift	Ext. 2.5-V ref.		±2			±2		ppm/°C
	Bipolar zero error(3)		–5		5	–2		2	mV
	Bipolar zero error drift			±0.4			±0.4		ppm/°C
	Power supply sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75 V < V_D < +5.25 V	–8		8	–8		8	LSB
AC ACCURACY									
SFDR	Spurious free dynamic range	f_I = 20 kHz	92	98		96	105		dB(5)
THD	Total harmonic distortion	f_I = 20 kHz		–98	–92		–103	–96	dB
SINAD	Signal-to-(noise + distortion)	f_I = 20 kHz	83	88		86	88		dB
		–60-dB Input		30			32		dB
SNR	Signal-to-noise ratio	f_I = 20 kHz	83	88		86	88		dB
	Full-power bandwidth(6)			500			500		kHz
SAMPLING DYNAMICS									
	Aperture delay			5			5		ns
	Transient response	FS Step			2			2	µs
	Overvoltage recovery(7)			150			150		ns
REFERENCE									
	Internal reference voltage		2.48	2.5	2.52	2.48	2.5	2.52	V
	Internal reference source current (must use external buffer)			1			1		µA
	Internal reference drift			8			8		ppm/°C
	External reference voltage range for specified linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
	External reference current drain	Ext. 2.5-V ref.			100			100	µA
DIGITAL INPUTS									
	Logic levels								
V_{IL}	Low-level input voltage		–0.3		0.8	–0.3		0.8	V
V_{IH}	High-level input voltage		2.0		V_{DIG} +0.3 V	2.0		V_{DIG} +0.3 V	V
I_{IL}	Low-level input current				±10			±10	µA
I_{IH}	High-level input current				±10			±10	µA
DIGITAL OUTPUTS									
	Data format (parallel 16-bits)								
	Data coding (binary 2's complement)								
V_{OL}	Low-level output voltage	I_{SINK} = 1.6 mA			0.4			0.4	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500 mA	4			4			V
	Leakage current	Hi-Z state, V_{OUT} = 0 V to V_{DIG}			±5			±5	µA
	Output capacitance	Hi-Z state			15			15	pF

(1) LSB means least significant bit. For the 16-bit, ±10-V input ADS8505, one LSB is 305 µV.
(2) Typical rms noise at worst case transitions and temperatures.
(3) As measured with fixed resistors shown in Figure 27. Adjustable to zero with external potentiometer.
(4) Full-scale error is the worst case of –full-scale or +full-scale deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) All specifications in dB are referred to a full-scale ±10-V input.
(6) Full-power bandwidth is defined as the full-scale input frequency at which signal-to-(noise + distortion) degrades to 60 dB, or 10 bits of accuracy.
(7) Recovers to specified performance after 2 x FS input overvoltage.

ELECTRICAL CHARACTERISTICS (continued)

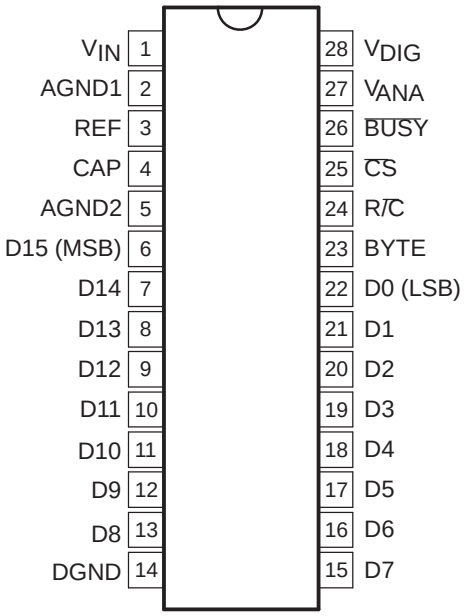
T_A = –40°C to 85°C, f_s = 250 kHz, V_{DIG} = V_{ANA} = 5 V, using internal reference (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADS8505I			ADS8505IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL TIMING									
	Bus access timing				83			83	ns
	Bus relinquish timing				83			83	ns
POWER SUPPLIES									
V_{DIG}	Digital input voltage	Must be ≤ V_{ANA}	4.75	5	5.25	4.75	5	5.25	V
V_{ANA}	Analog input voltage		4.75	5	5.25	4.75	5	5.25	V
I_{DIG}	Digital input current			2	5		2	5	mA
I_{ANA}	Analog input current			12	15		12	15	mA
	Power dissipation	f_S = 250 kHz		70	100		70	100	mW
TEMPERATURE RANGE									
	Specified performance		–40		85	–40		85	°C
	Derated performance(8)		–55		125	–55		125	°C
	Storage		–65		150	–65		150	°C
THERMAL RESISTANCE (Θ_{JA})									
	SSOP			62			62		°C/W
	SO			46			46		°C/W

(8) The internal reference may not be started correctly beyond the industrial temperature range (–40°C to 85°C), therefore use of an external reference is recommended.

DEVICE INFORMATION

DB OR DW PACKAGE
(TOP VIEW)



DEVICE INFORMATION (continued)

Terminal Functions

TERMINAL		DIGITAL I/O	DESCRIPTION
NAME	DB/DW NO.		
AGND1	2		Analog ground. Used internally as ground reference point.
AGND2	5		Analog ground.
$\overline{BUSY}$	26	O	At the start of a conversion, $\overline{BUSY}$ goes low and stays low until the conversion is completed and the digital outputs have been updated.
BYTE	23	I	Selects 8 most significant bits (low) or 8 least significant bits (high).
CAP	4		Reference buffer capacitor. 2.2-µF Tantalum capacitor to ground.
$\overline{CS}$	25	I	Internally ORed with R/$\overline{C}$. If R/$\overline{C}$ is low, a falling edge on $\overline{CS}$ initiates a new conversion.
DGND	14		Digital ground.
D15 (MSB)	6	O	Data bit 15. Most significant bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D14	7	O	Data bit 14. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D13	8	O	Data bit 13. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D12	9	O	Data bit 12. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D11	10	O	Data bit 11. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D10	11	O	Data bit 10. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D9	12	O	Data bit 9. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D8	13	O	Data bit 8. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D7	15	O	Data bit 7. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D6	16	O	Data bit 6. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D5	17	O	Data bit 5. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D4	18	O	Data bit 4. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D3	19	O	Data bit 3. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D2	20	O	Data bit 2. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D1	21	O	Data bit 1. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
D0 (LSB)	22	O	Data bit 0. Least significant bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low.
R/$\overline{C}$	24	I	With $\overline{CS}$ low and $\overline{BUSY}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion. With $\overline{CS}$ low, a rising edge on R/$\overline{C}$ enables the parallel output.
REF	3		Reference input/output. 2.2-µF Tantalum capacitor to ground.
V_{ANA}	27		Analog supply input. Nominally +5 V. Decouple to ground with 0.1-µF ceramic and 10-µF tantalum capacitors.
V_{DIG}	28		Digital supply input. Nominally +5 V. Connect directly to pin 27. Must be ≤ V_{ANA}.
V_{IN}	1		Analog input. See Figure 28.

TYPICAL CHARACTERISTICS

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

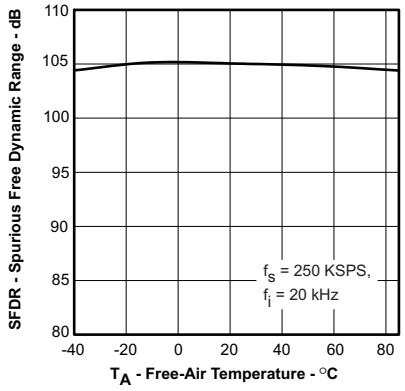


Figure 1.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

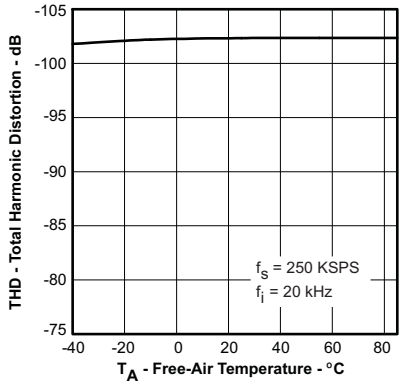


Figure 2.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

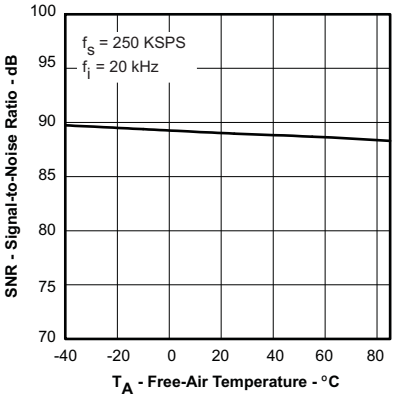


Figure 3.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

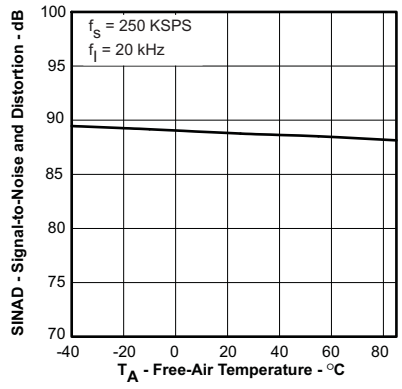


Figure 4.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

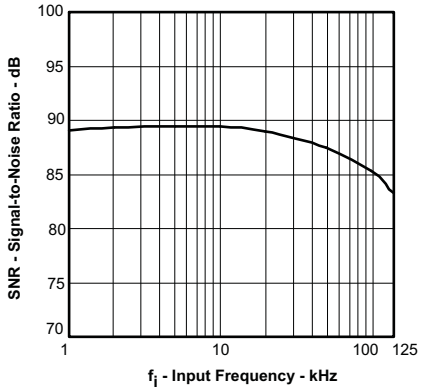


Figure 5.

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

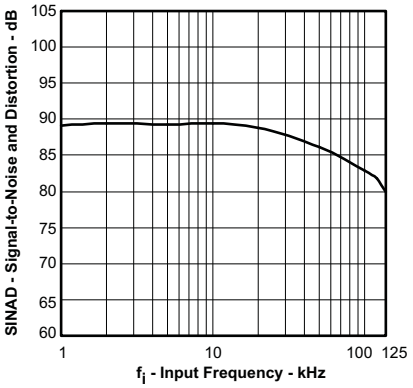


Figure 6.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

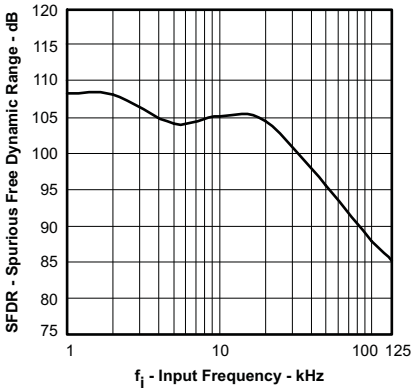


Figure 7.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

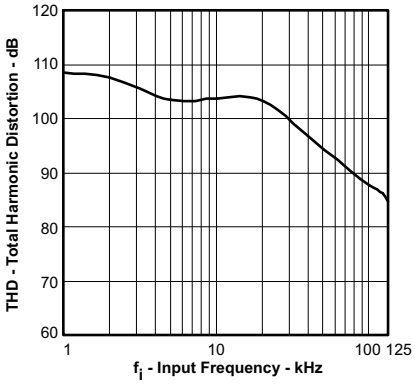


Figure 8.

INTERNAL REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

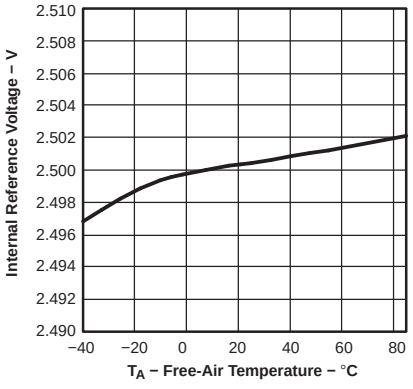


Figure 9.

TYPICAL CHARACTERISTICS (continued)

BIPOLAR ZERO SCALE ERROR vs FREE-AIR TEMPERATURE

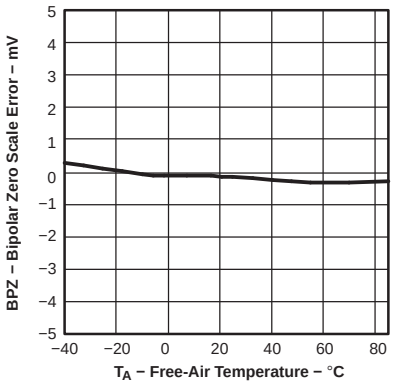


Figure 10.

NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

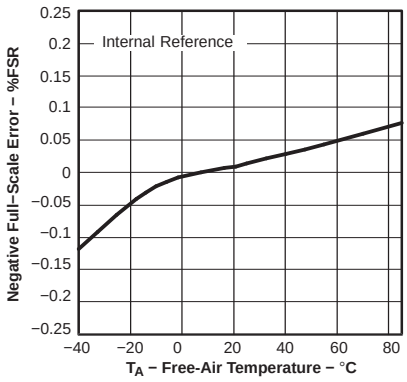


Figure 11.

NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

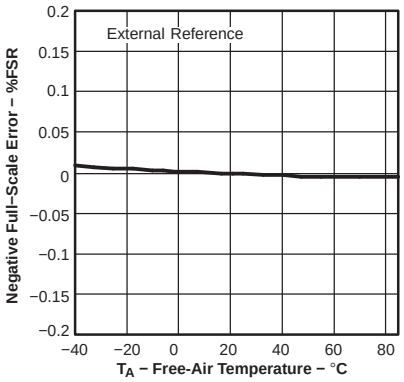


Figure 12.

POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

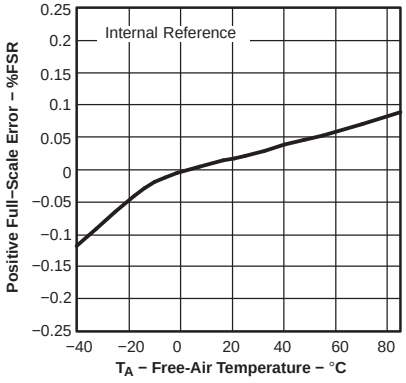


Figure 13.

POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

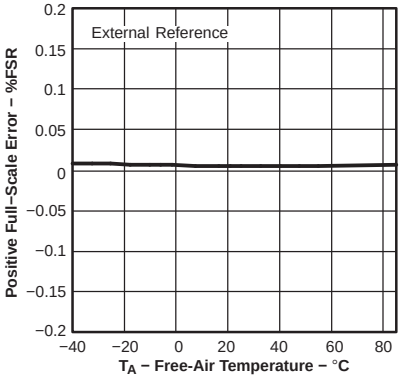


Figure 14.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

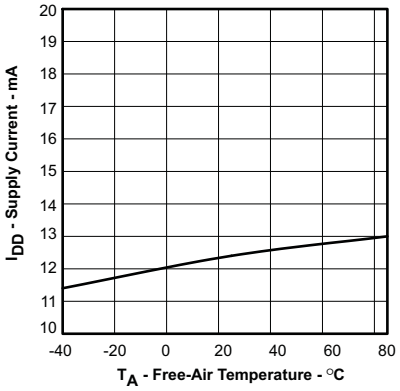


Figure 15.

HISTOGRAM

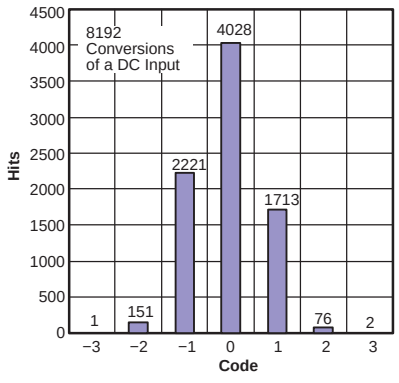


Figure 16.

PERFORMANCE vs CAP PIN CAPACITOR ESR

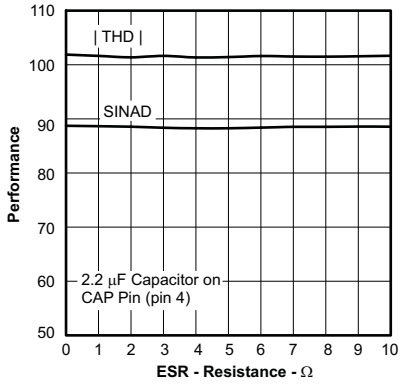


Figure 17.

TYPICAL CHARACTERISTICS (continued)

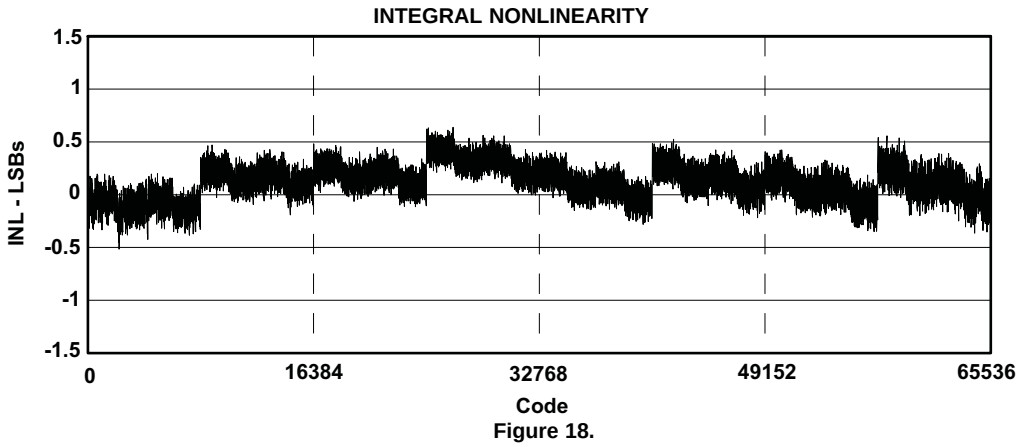


Figure 18.

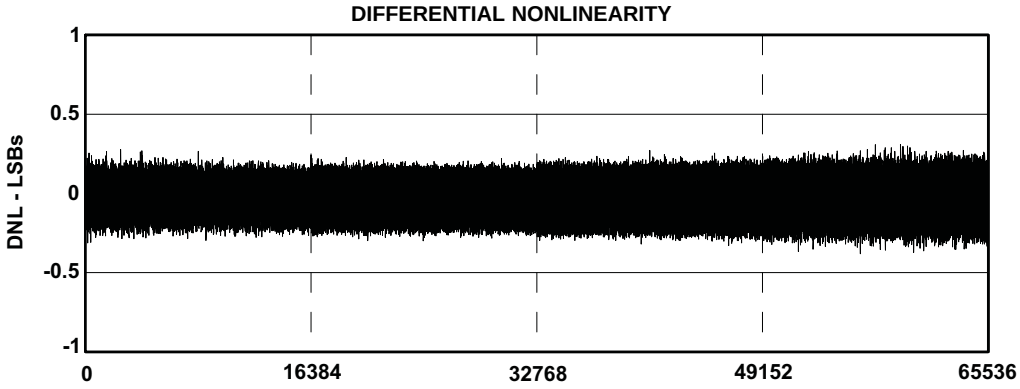


Figure 19.

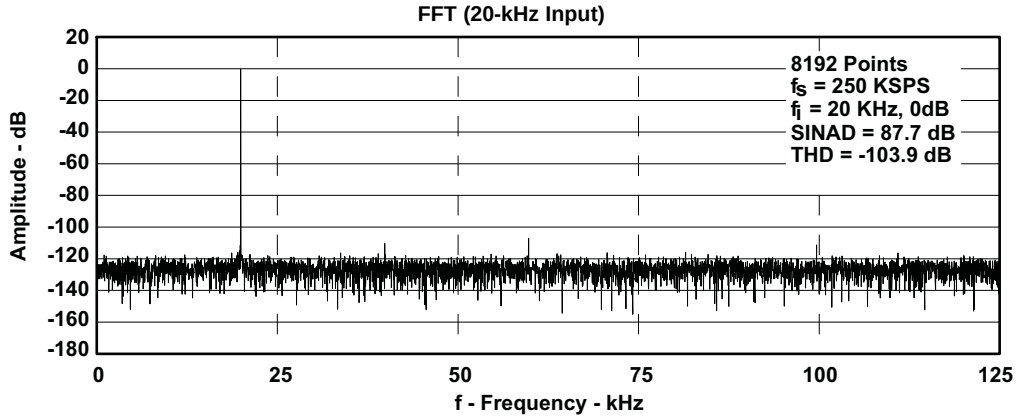


Figure 20.

BASIC OPERATION

Figure 21 shows a basic circuit to operate the ADS8505 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) low for a minimum of 40 ns (1.75 µs max) initiates a conversion. $\overline{BUSY}$ (pin 26) goes low and stays low until the conversion is completed and the output registers are updated. Data is output in binary 2's complement format with the MSB on pin 6. $\overline{BUSY}$ going high can be used to latch the data.

BASIC OPERATION (continued)

The ADS8505 begins tracking the input signal at the end of the conversion. Allowing 4 µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the CALIBRATION section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) low for a minimum of 40 ns immediately puts the sample/hold of the ADS8505 in the hold state and starts conversion *n*. $\overline{BUSY}$ (pin 26) goes low and stays low until conversion *n* is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ low will abort the conversion in progress and reset the ADC (see Figure 26).

The ADS8505 begins tracking the input signal at the end of the conversion. Allowing 4 µs between convert commands assures accurate acquisition of a new signal. Refer to Table 1 for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figure 23 through Figure 25 for the timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally ORed and level triggered. There is not a requirement which input goes low first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion *n*, be sure the less critical input is low at least 10 ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied low using R/$\overline{C}$ to control the read and convert modes. The parallel output becomes active whenever R/$\overline{C}$ goes high. Refer to the READING DATA section.

Table 1. Control Line Functions for Read and Convert

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion *n*. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion *n*. Databus enters Hi-Z state.
0	1	↑	Conversion *n* completed. Valid data from conversion *n* on the databus.
↓	1	1	Enables databus with valid data from conversion *n*.
↓	1	0	Enables databus with valid data from conversion *n-1*(1). Conversion *n* in progress.
0	↑	0	Enables databus with valid data from conversion *n-1*(1). Conversion *n* in progress.
0	0	↑	Data is invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be high when $\overline{BUSY}$ goes high.
X	↓	0	Conversion *n* is halted. Causes ADC to reset.(2)

(1) See Figure 23 and Figure 24 for constraints on data valid from conversion *n-1*.
(2) See Figure 26 for details on ADC reset.

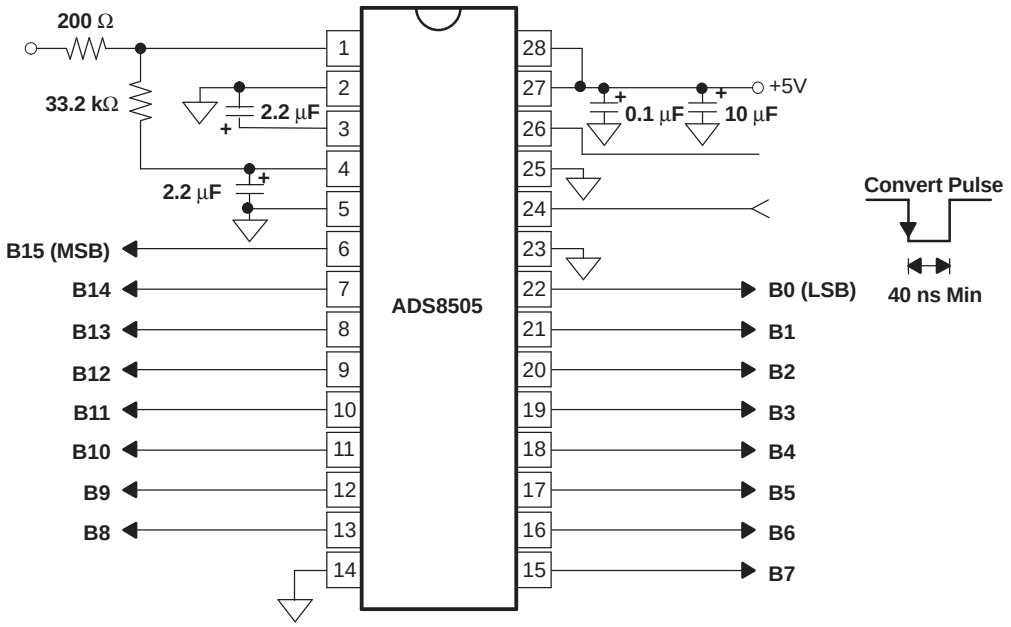


Figure 21. Basic Operation

READING DATA

The ADS8505 outputs full or byte-reading parallel data in binary 2's complement data output format. The parallel output is active when R/$\overline{C}$ (pin 24) is high and $\overline{CS}$ (pin 25) is low. Any other combination of $\overline{CS}$ and R/$\overline{C}$ 3-states the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table 2 for ideal output codes and Figure 22 for bit locations relative to the state of BYTE.

Table 2. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY 2'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full-scale range	±10 V		
Least significant bit (LSB)	305 µV		
Full scale (10 V-1 LSB)	9.999695 V	0111 1111 1111 1111	7FFF
Midscale	0 V	0000 0000 0000 0000	0000
One LSB below midscale	-305 µV	1111 1111 1111 1111	FFFF
–Full scale	-10 V	1000 0000 0000 0000	8000

PARALLEL OUTPUT (After a Conversion)

After conversion *n* is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) goes high. Valid data from conversion *n* is available on D15-D0 (pins 6-13 and 15-22). $\overline{BUSY}$ going high can be used to latch the data. Refer to Table 3, Figure 23, Figure 24, and Figure 25 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion *n* has been initiated, valid data from conversion *n-1* can be read and is valid up to t_2 (2.2 µs typ) after the start of conversion *n*. Do not attempt to read data from t_2 (2.2 µs typ) after the start of conversion *n* until $\overline{BUSY}$ (pin 26) goes high; this may result in reading invalid data. Refer to Table 3, Figure 23, Figure 24, and Figure 25 for timing specifications.

Note: For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading converter performance.

The number of control lines can be reduced by tying $\overline{CS}$ low while using the falling edge of R/$\overline{C}$ to initiate conversions and the rising edge of R/$\overline{C}$ to activate the output mode of the converter. See Figure 23.

Table 3. Conversion Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{w1}	Pulse duration, convert	40		1750	ns
t_a	Access time, data valid after R/$\overline{C}$ low		2.2	3.2	µs
t_{pd}	Propagation delay time, $\overline{BUSY}$ from R/$\overline{C}$ low		15	25	ns
t_{w2}	Pulse duration, $\overline{BUSY}$ low			2.2	µs
t_{d1}	Delay time, $\overline{BUSY}$ after end of conversion		5		ns
t_{d2}	Delay time, aperture		5		ns
t_{conv}	Conversion time			2.2	µs
t_{acq}	Acquisition time	1.8			µs
t_{dis}	Disable time, bus	10	30	83	ns
t_{d3}	Delay time, $\overline{BUSY}$ after data valid	35	50		ns
t_v	Valid time, previous data remains valid after R/$\overline{C}$ low	1.5	2		µs
$t_{conv} + t_{acq}$	Throughput time			4	µs
t_{su}	Setup time, R/$\overline{C}$ to $\overline{CS}$	10			ns
t_c	Cycle time between conversions	4			µs
t_{en}	Enable time, bus	10	30	83	ns
t_{d4}	Delay time, BYTE	5	10	30	ns

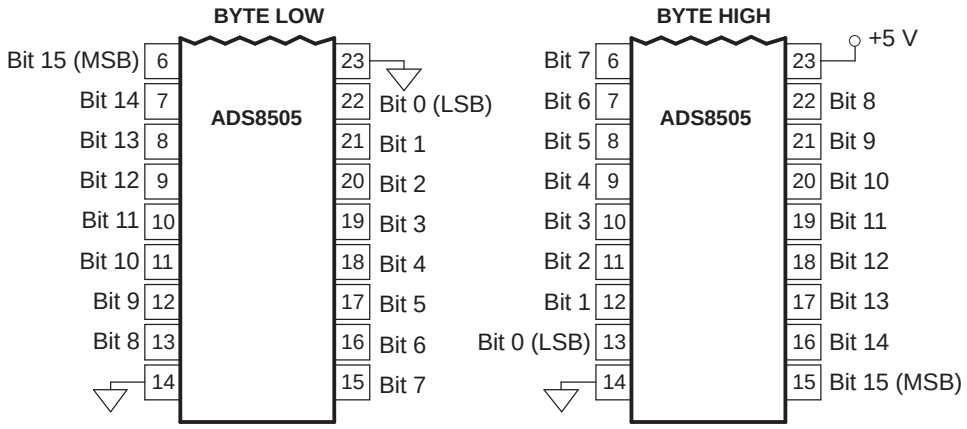


Figure 22. Bit Locations Relative to State of BYTE (Pin 23)

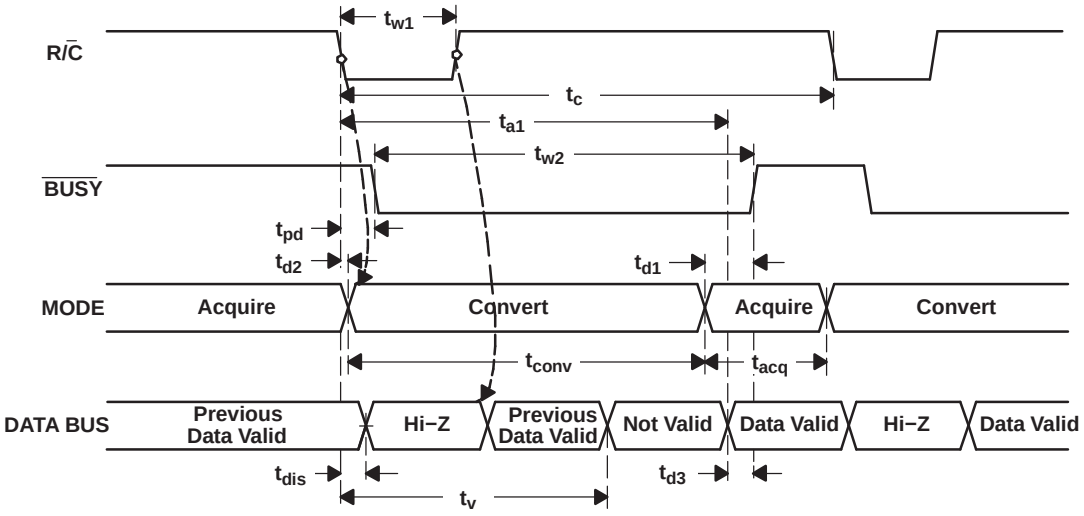


Figure 23. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied Low)

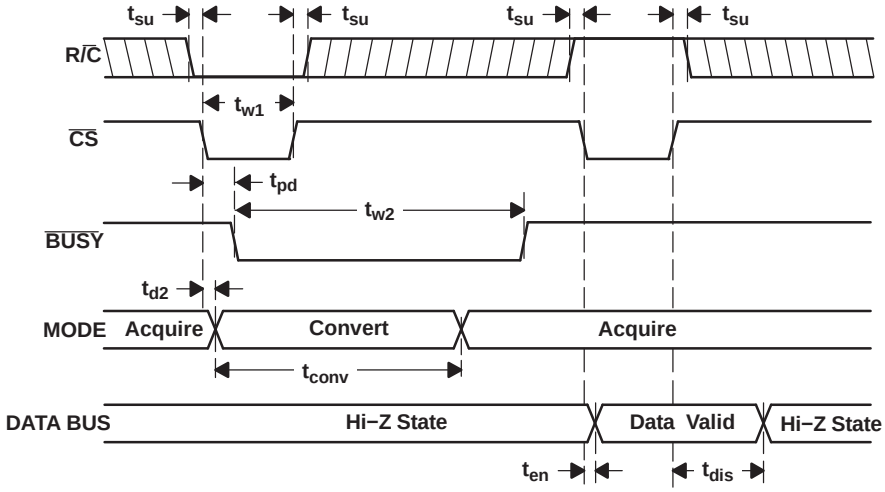


Figure 24. Using $\overline{CS}$ to Control Conversion and Read Timing

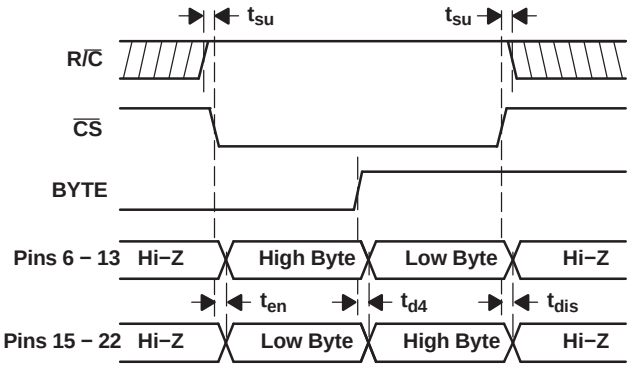


Figure 25. Using $\overline{CS}$ and BYTE to Control Data Bus

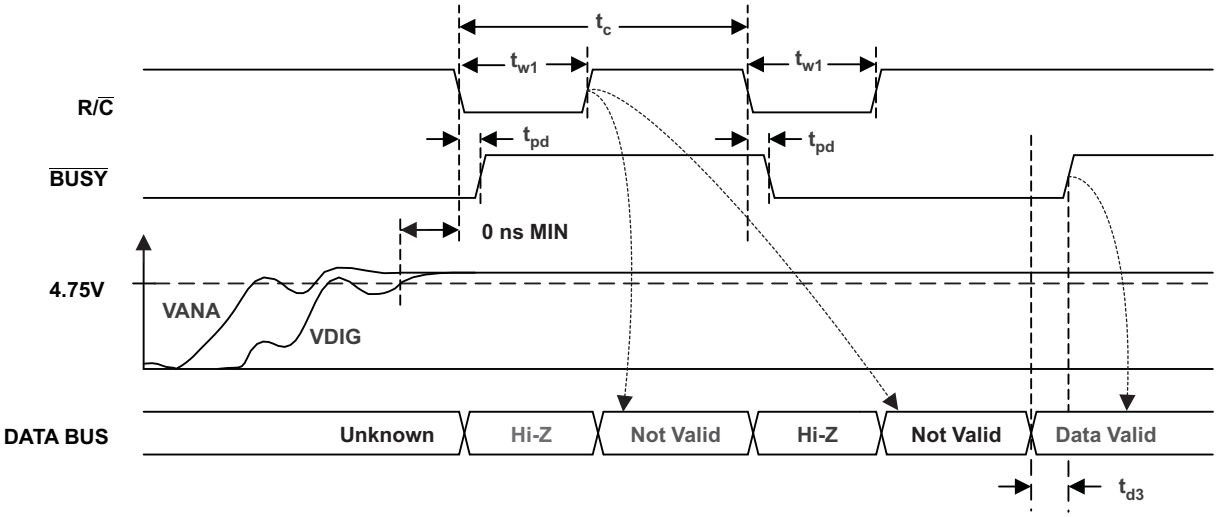


Figure 26. ADC Reset

ADC RESET

The ADC reset function of the ADS8505 can be used to terminate the current conversion cycle. Bringing R/$\overline{C}$ low for at least 40 ns while BUSY is low will initiate the ADC reset. To initiate a new conversion, R/$\overline{C}$ must return to the high state and remain high long enough to acquire a new sample (see Table 3, t_c) before going low to initiate the next conversion sequence. In applications that do not monitor the BUSY signal, it is recommended that the ADC reset function be implemented as part of a system initialization sequence.

INPUT RANGES

The ADS8505 offers a standard ±10-V input range. Figure 28 shows the necessary circuit connections for the ADS8505 with and without hardware trim. Offset and full-scale error specifications are tested and specified with the fixed resistors shown in Figure 28(b). Full-scale error includes offset and gain errors measured at both +FS and –FS. Adjustments for offset and gain are described in the CALIBRATION section of this data sheet.

Offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain are corrected in software (refer to the CALIBRATION section).

The nominal input impedance of 11.5 kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection assured to at least ±25 V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

The input signal must be referenced to AGND1. This minimizes the ground loop problem typical to analog designs. The analog signal should be driven by a low impedance source. A typical driving circuit using an OPA627 or OPA132 is shown in Figure 27.

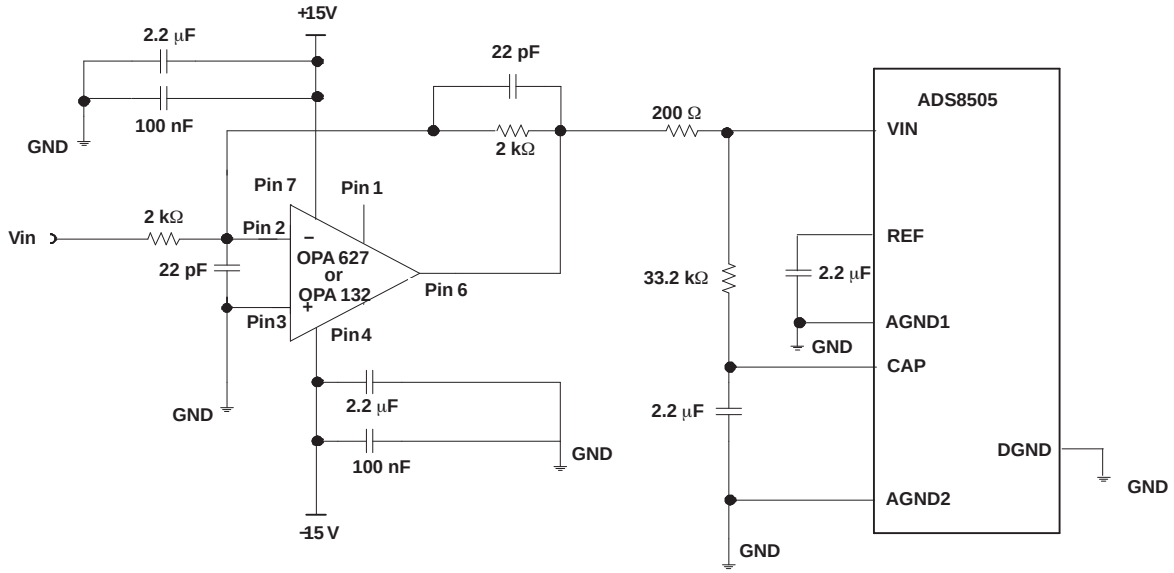


Figure 27. Typical Driving Circuit (±10 V, No Trim)

APPLICATION INFORMATION

CALIBRATION

The ADS8505 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

Hardware Calibration

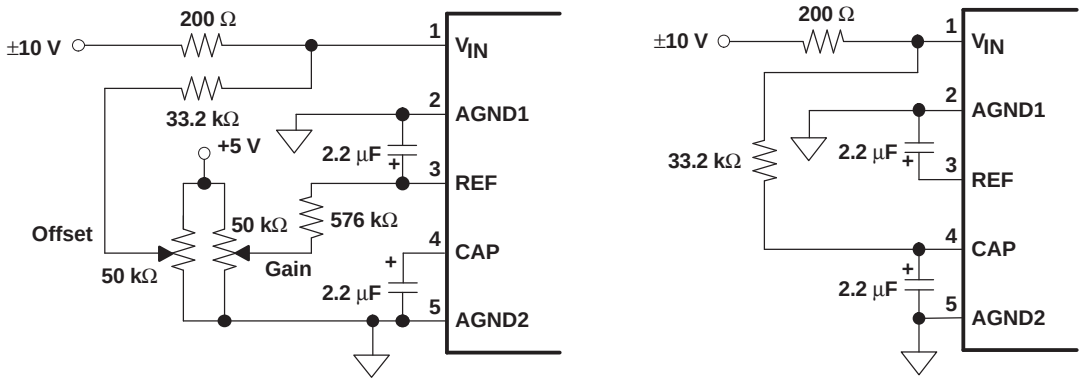
To calibrate the offset and gain of the ADS8505, install the proper resistors and potentiometers as shown in Figure 28(a).

Software Calibration

To calibrate the offset and gain of the ADS8505 in software, no external resistors are required. See the No Calibration section for details on the effects of the external resistors.

No Calibration

See Figure 28(b) for circuit connections. The external resistors shown in Figure 28(b) may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply.



(a) ±10 V With Hardware Trim

(b) ±10 V Without Hardware Trim

Note: Use 1% metal film resistors.

Figure 28. Circuit Diagram With and Without External Resistors

REFERENCE

The ADS8505 can operate with its internal 2.5-V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full-scale error (FSE = ±0.5%).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5-V reference. A 2.2-µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low-pass filter to bandlimit noise on the reference. Using a smaller value capacitor introduces more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external ac or dc loads.

The range for the external reference is 2.3 V to 2.7 V and determines the actual LSB size. Increasing the reference voltage increases the full-scale range and the LSB size of the converter which can improve the SNR.

APPLICATION INFORMATION (continued)

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2-μF capacitor can be placed between the CAP pin and ground. Because the internal reference buffer is internally compensated, the external capacitor is not necessary for compensation of the reference buffer. This relaxes the performance requirements of the capacitor and makes the performance of the ADC less sensitive to the capacitor.

The output of the buffer is capable of driving up to 2 mA of current to a dc load. A dc load requiring more than 2 mA of current from the CAP pin begins to degrade the linearity of the ADS8505. Using an external buffer allows the internal reference to be used for larger dc loads and ac loads. Do not attempt to directly drive an ac load with the output voltage on CAP. This causes performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5-V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS8505 uses 90% of its power for the analog circuitry. The ADS8505 should be considered as an analog component.

The +5-V power for the A/D should be separate from the +5 V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5-V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12-V or +15-V supplies are present, a simple +5-V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5-V source.

GROUNDING

Three ground pins are present on the ADS8505. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample/hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op-amp to oscillate. The FET switch on the ADS8505, compared to the FET switches on other CMOS A/D converters, releases 5% to 10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op-amp sufficient for the signal in an application is sufficient to drive the ADS8505.

The resistive front end of the ADS8505 also provides an assured ±25-V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS8505 does have 3-state outputs for the parallel port, but intermediate latches should be used if the bus is to be active during conversions. If the bus is not active during conversion, the 3-state outputs can be used to isolate the A/D from other peripherals on the same bus. The 3-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS8505 has an internal LSB size of 38 μV. Transients from fast switching signals on the parallel port, even when the A/D is 3-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September, 2005) to A Revision	Page
• Added SFDR value	1
• Changed 3.0 to 1.5 Max INL	1
• Changed 3.0 to 1.5 Minimum Relative Accuracy	2
• Changed REF and CAP - reversed	2
• Changed INL, SFDR, THD, SNR values	2
• Changed SFDR-TA, THD-TA, SINAD-TA, SNR-fi, SINAD-fi SFDR-fi, THD-fi, IDD-TA, CAP ESR, INL, DNL, and FFT curves	6
• Changed CAP description	16

Changes from A Revision (October, 2006) to B Revision	Page
• Deleted text from basic operation description	8
• Changed text in starting a conversion description	9
• Changed operation descriptions and R/$\overline{C}$ in table	9
• Added SAR Reset timing	13
• Added ADC RESET section	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8505IBDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8505I B	Samples
ADS8505IBDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8505I B	Samples
ADS8505IBDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8505I B	Samples
ADS8505IBDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8505I B	Samples
ADS8505IDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8505I	Samples
ADS8505IDWG4	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8505I	Samples
ADS8505IDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8505I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

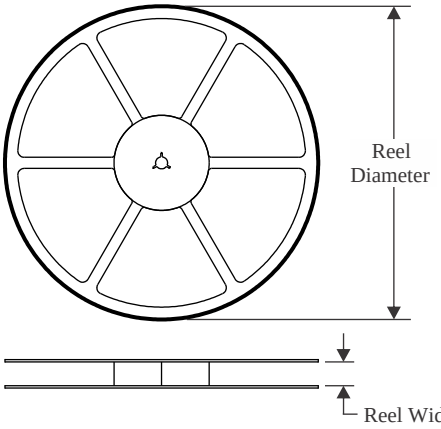
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

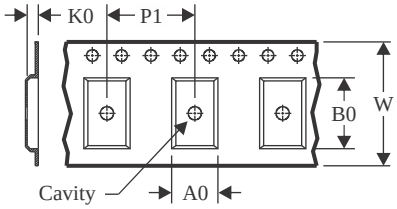
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

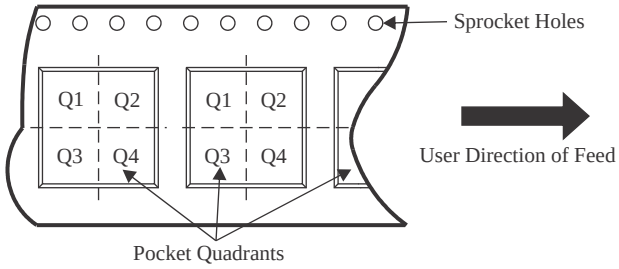


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

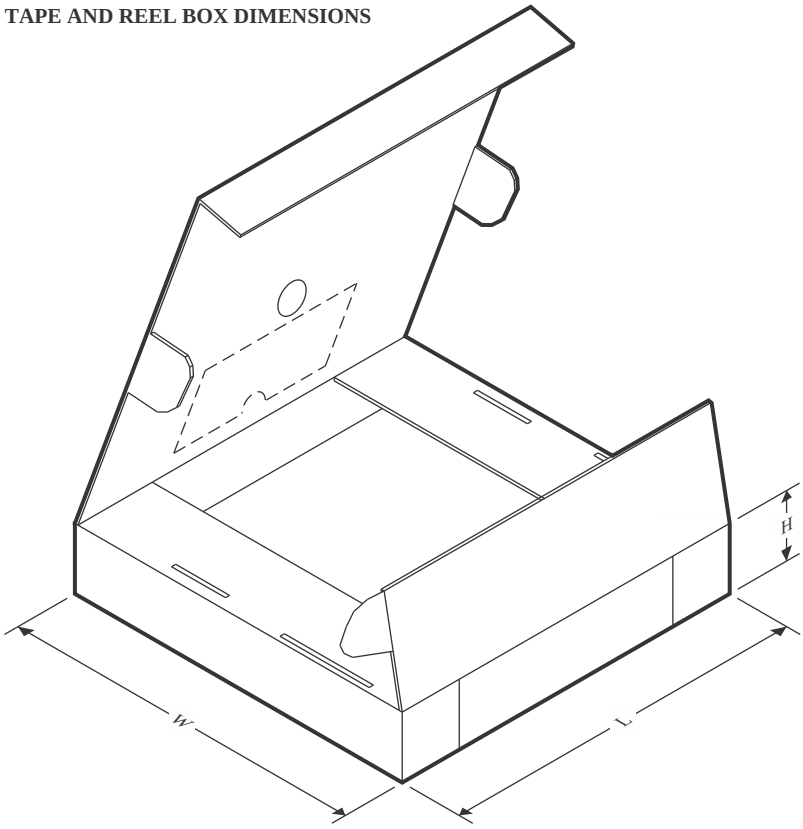
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8505IBDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
ADS8505IBDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
ADS8505IDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

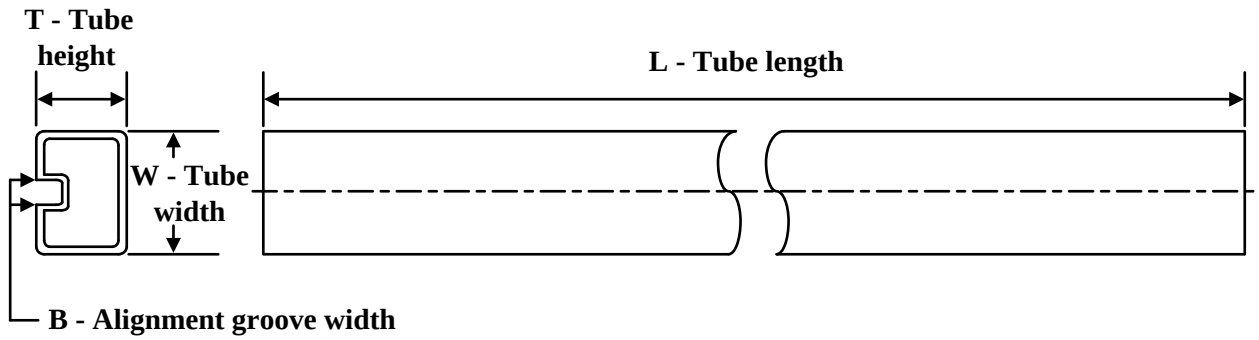
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8505IBDBR	SSOP	DB	28	2000	350.0	350.0	43.0
ADS8505IBDWR	SOIC	DW	28	1000	350.0	350.0	66.0
ADS8505IDWR	SOIC	DW	28	1000	350.0	350.0	66.0

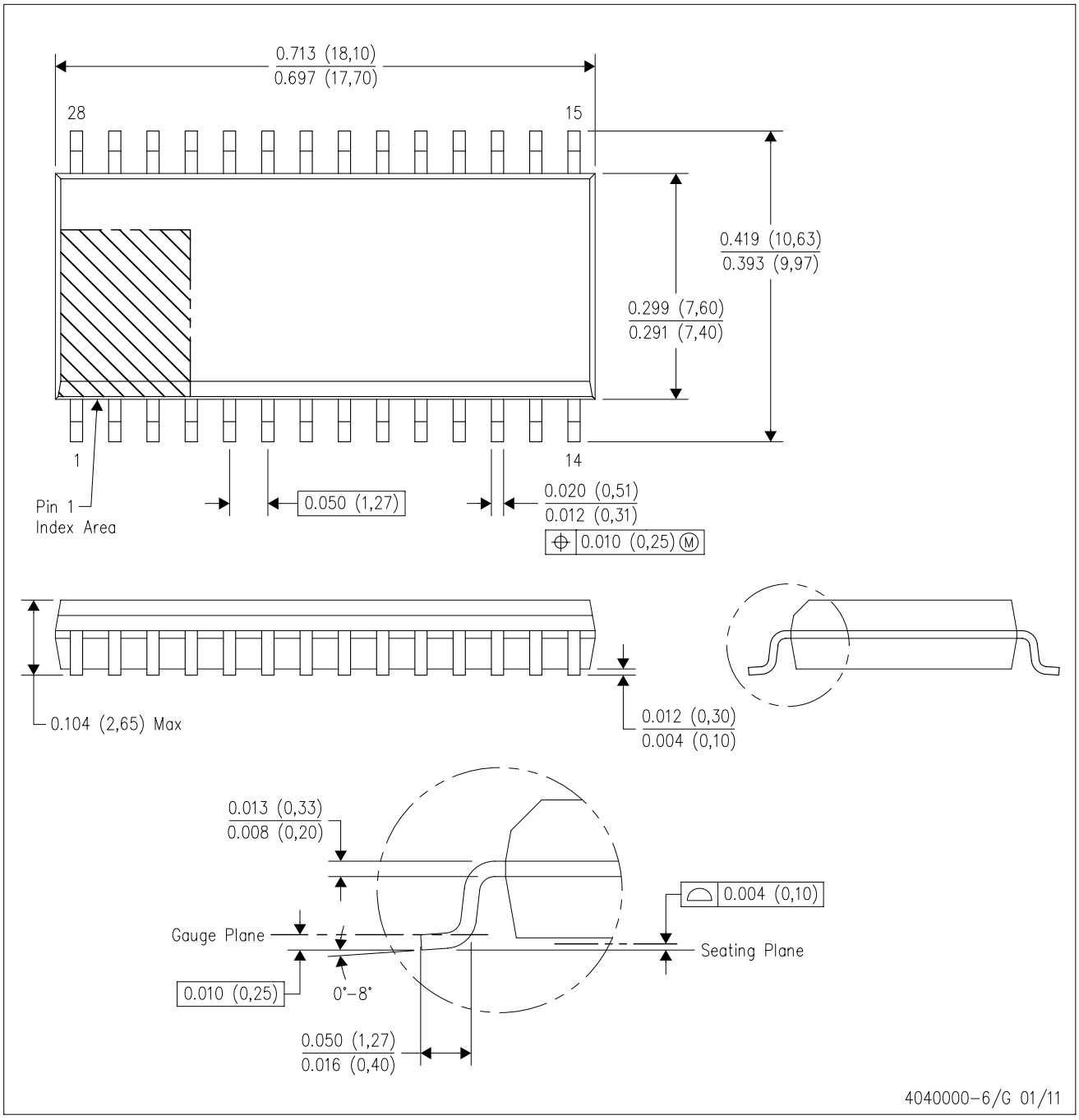
TUBE



*All dimensions are nominal

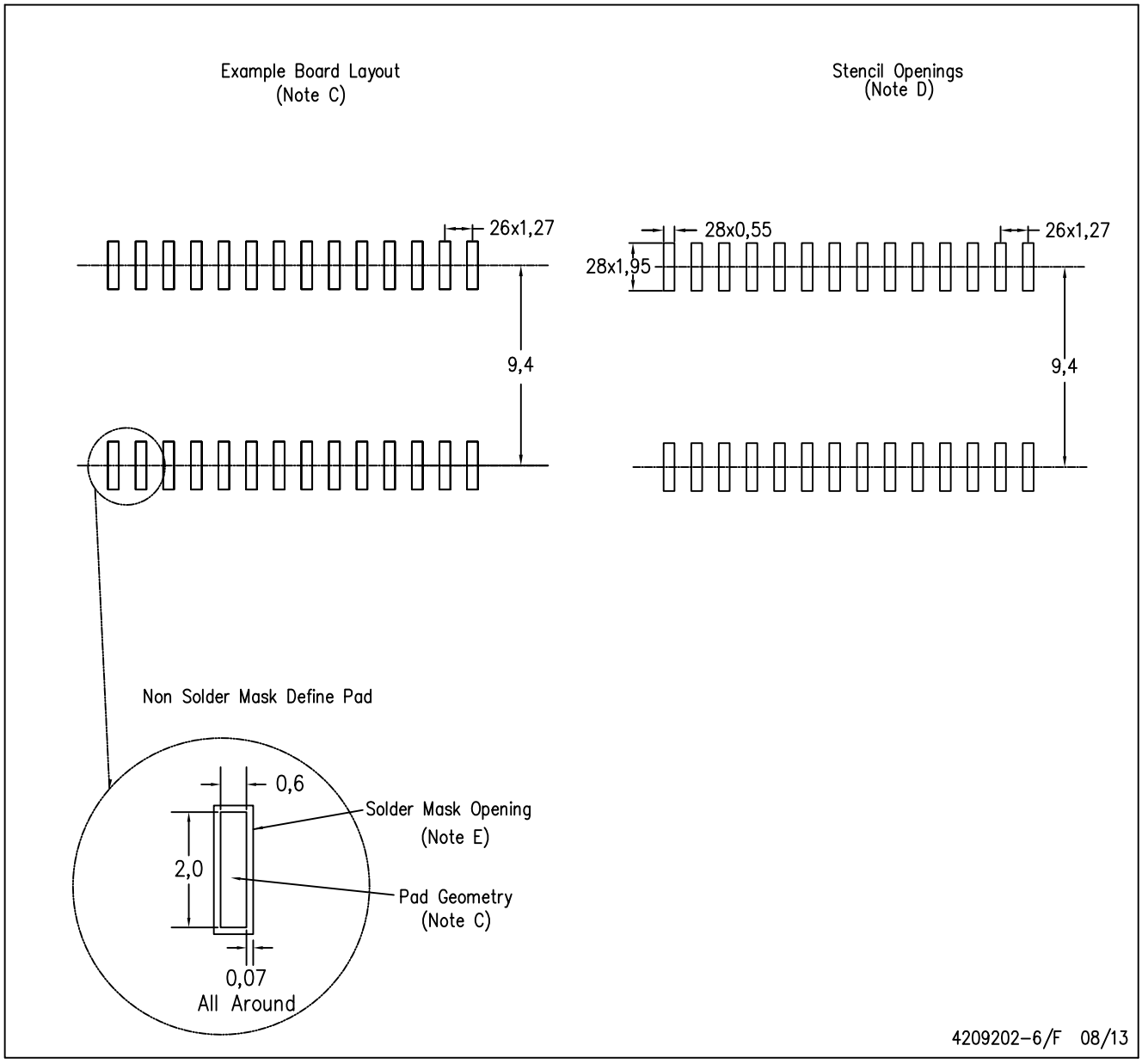
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS8505IBDB	DB	SSOP	28	50	530	10.5	4000	4.1
ADS8505IBDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
ADS8505IDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
ADS8505IDWG4	DW	SOIC	28	20	506.98	12.7	4826	6.6

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



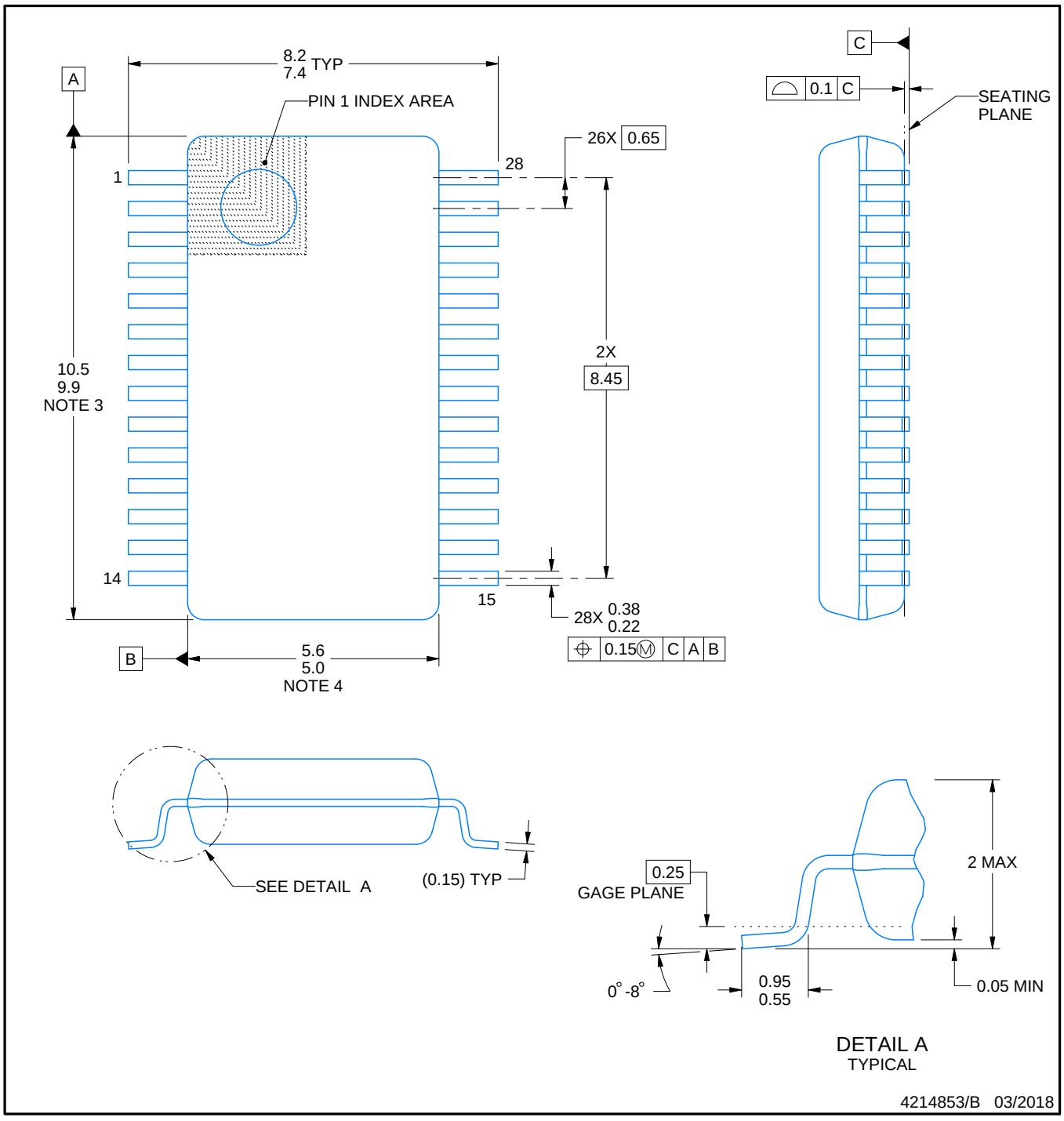
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0028A

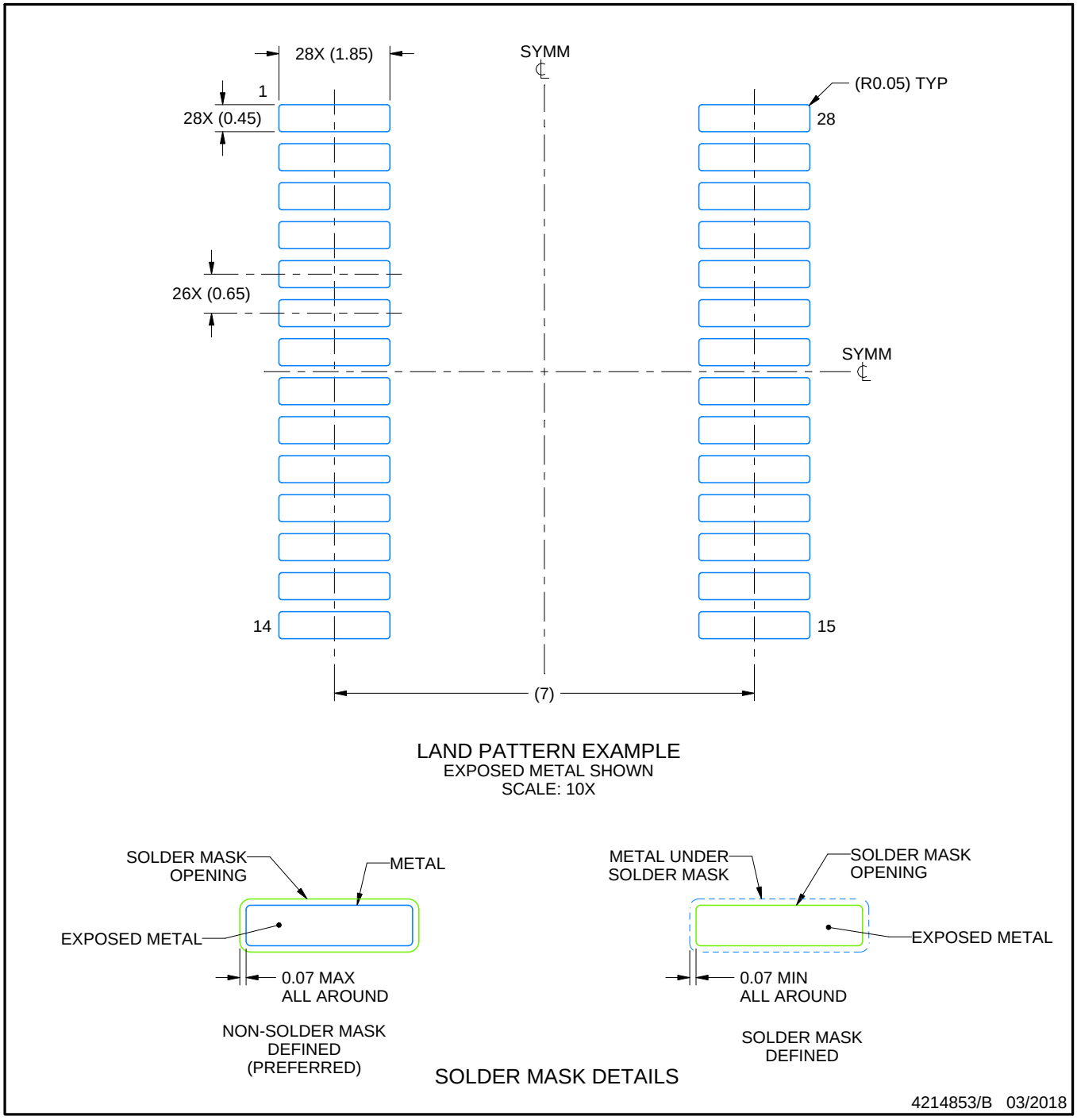
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



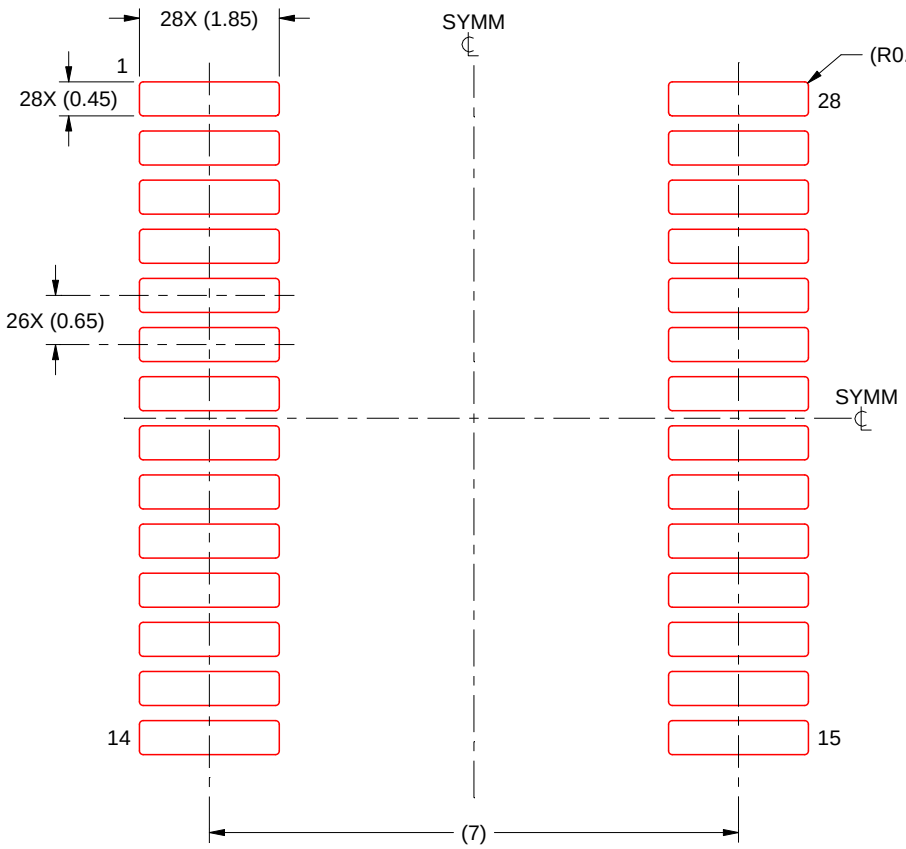
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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