AM625SIP – AM6254 Sitara™ Processor with Integrated LPDDR4 SDRAM

1 Features

Processor Cores:

- Up to Quad 64-bit Arm® Cortex®-A53 microprocessor subsystem at up to 1.4GHz
  - Quad-core Cortex-A53 cluster with 512KB L2 shared cache with SECDED ECC
  - Each A53 Core has 32KB L1 DCache with SECDED ECC and 32KB L1 ICache with Parity protection
- Single-core Arm® Cortex®-M4F MCU at up to 400MHz
  - 256KB SRAM with SECDED ECC
- Dedicated Device/Power Manager

Multimedia:

- Display subsystem
  - Dual display support
  - 1920x1080 @ 60fps for each display
  - 1x 2048x1080 + 1x 1280x720
  - Up to 165MHz pixel clock support with Independent PLL for each display
  - OLDI (4 lanes LVDS - 2x) and DPI (24-bit RGB LVCMOS)
  - Support safety feature such as freeze frame detection and MISR data check
- 3D Graphics Processing Unit
  - 1 pixel per clock or higher
  - Fillrate greater than 500Mpixels/sec
  - >500 MTexels/s, >8GFLOPs
  - Supports at least 2 composition layers
  - Supports up to 2048x1080 @60fps
  - Supports ARGB32, RGB565 and YUV formats
  - 2D graphics capable
  - OpenGL ES 3.1, Vulkan 1.2
- One Camera Serial interface (CSI-Rx) - 4 Lane with DPHY
  - MIPI® CSI-2 v1.3 Compliant + MIPI D-PHY 1.2
  - Support for 1,2,3 or 4 data lane mode up to 1.5Gbps per lane
  - ECC verification/correction with CRC check + ECC on RAM
  - Virtual Channel support (up to 16)
  - Ability to write stream data directly to DDR via DMA

Memory Subsystem:

- Up to 816KB of On-chip RAM
  - 64KB of On-chip RAM (OCSRAM) with SECDED ECC , Can be divided into smaller banks in increments of 32KB for as many as 2 separate memory banks
  - 256KB of On-chip RAM with SECDED ECC in SMS Subsystem
  - 176KB of On-chip RAM with SECDED ECC in SMS Subsystem for TI security firmware
  - 256KB of On-chip RAM with SECDED ECC in Cortex-M4F MCU subsystem
  - 64KB of On-chip RAM with SECDED ECC in Device/Power Manager Subsystem
- DDR Subsystem (DDRSS)
  - Integrated 512MB LPDDR4 SDRAM
  - Supports speeds up to 1600MT/s
  - 16-Bit data bus with inline ECC

Security:

- Secure boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure watchdog/timer/IPC
  - Secure storage support
  - Replay Protected Memory Block (RPMB) support
- Dedicated Security Controller with user programmable HSM core and dedicated security DMA & IPC subsystem for isolated processing
- Cryptographic acceleration supported
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
    - Supports cryptographic cores
  - AES – 128-/192-/256-Bit key sizes
  - SHA2 – 224-/256-/384-/512-Bit key sizes
  - DRBG with true random number generator
  - PKA (Public Key Accelerator) to Assist in RSA/ECC processing for secure boot
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging

PRU Subsystem:

- Dual-core Programmable Real-Time Unit Subsystem (PRUSS) running up to 333MHz
- Intended for driving GPIO for cycle accurate protocols such as additional:
  - General Purpose Input/Output (GPIO)
  - UARTs
  - I^2C
  - External ADC
- 16KByte program memory per PRU with SECDED ECC
- 8KB data memory per PRU with SECDED ECC
- 32KB general purpose memory with SECDED ECC
- CRC32/16 HW accelerator
- Scratch PAD memory with 3 banks of 30 x 32-bit registers
- 1 Industrial 64-bit timer with 9 capture and 16 compare events, along with slow and fast compensation
- 1 interrupt controller (INTC), minimum of 64 input events supported

High-Speed Interfaces:

- Integrated Ethernet switch supporting (total of 2 external ports)
  - RMII(10/100) or RGMII (10/100/1000)
  - IEEE1588 (Annex D, Annex E, Annex F with 802.1AS PTP)
  - Clause 45 MDIO PHY management
  - Packet Classifier based on ALE engine with 512 classifiers
  - Priority based flow control
  - Time sensitive networking (TSN) support
  - Four CPU H/W interrupt Pacing
  - IP/UDP/TCP checksum offload in hardware
- Two USB2.0 Ports
  - Port configurable as USB host, USB peripheral, or USB Dual-Role Device (DRD mode)
  - Integrated USB VBUS detection

General Connectivity:

- 9x Universal Asynchronous Receiver-Transmitters (UART)
- 5x Serial Peripheral Interface (SPI) controllers
- 6x Inter-Integrated Circuit (I^2C) ports
- 3x Multichannel Audio Serial Ports (McASP)
  - Transmit and Receive Clocks up to 50 MHz
  - Up to 16/10/6 Serial Data Pins across 3x McASP with Independent TX and RX Clocks
  - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and Similar Formats
  - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 Formats)
  - FIFO Buffers for Transmit and Receive (256 Bytes)
  - Support for audio reference output clock
- 3x enhanced PWM modules (ePWM)
- 3x enhanced Quadrature Encoder Pulse modules (eQEP)
- 3x enhanced Capture modules (eCAP)
- General-Purpose I/O (GPIO), All LVCMOS I/O can be configured as GPIO
- 3x Controller Area Network (CAN) modules with CAN-FD support
  - Conforms w/ CAN Protocol 2.0 A, B and ISO 11898-1
  - Full CAN FD support (up to 64 data bytes)
  - Parity/ECC check for Message RAM
  - Speed up to 8Mbps

Media and Data Storage:

- 3x Multi-Media Card/Secure Digital® (MMC/SD®/SDIO) interface
  - 1x 8-bit eMMC interface up to HS200 speed
  - 2x 4-bit SD/SDIO interface up to UHS-I
  - Compliant with eMMC 5.1, SD 3.0 and SDIO Version 3.0
- 1× General-Purpose Memory Controller (GPMC) up to 133 MHz
  - Flexible 8- and 16-Bit Asynchronous Memory Interface With up to four Chip (22-bit address) Selects (NAND, NOR, Muxed-NOR, and SRAM)
  - Uses BCH Code to Support 4-, 8-, or 16-Bit ECC
  - Uses Hamming Code to Support 1-Bit ECC
  - Error Locator Module (ELM)
    - Used With the GPMC to Locate Addresses of Data Errors From Syndrome Polynomials Generated Using a BCH Algorithm
    - Supports 4-, 8-, and 16-Bit Per 512-Byte Block Error Location Based on BCH Algorithms
- OSPI/QSPI with DDR / SDR support
  - Support for Serial NAND and Serial NOR flash devices
  - 4GBytes memory address support
  - XIP mode with optional on-the-fly encryption

Power Management:

- Low power modes supported by Device/Power Manager
  - Partial IO support for CAN/GPIO/UART wakeup
  - DeepSleep
  - MCU Only
  - Standby
  - Dynamic frequency scaling for Cortex-A53

Optimal Power Management Solution:

- Recommended TPS65219 Power Management ICs (PMIC)
  - Companion PMIC specially designed to meet device power supply requirements
  - Flexible mapping and factory programmed configurations to support different use cases

Boot Options:

- UART
- I^2C EEPROM
- OSPI/QSPI Flash
- GPMC NOR/NAND Flash
- Serial NAND Flash
- SD Card
- eMMC
- USB (host) boot from Mass Storage device
- USB (device) boot from external host (DFU mode)
- Ethernet

Technology / Package:

- 16-nm technology
- 13mm x 13mm, 0.5-mm pitch, 425-pin FCCSP BGA (AMK)

2 Applications

- Human Machine Interfaces (HMI)
- Medical equipment, Patient monitoring, and Portable medical devices
- Appliance user interface and connectivity
- Electric Vehicle Service Equipment (EVSE) / Vehicle to Infrastructure (V2X)
- Smart home gateways
- Embedded security: Control & Access panels

3 Description

AM625SIP is a System In Package (SIP) derivative of the ALW packaged AM6254 device, with the addition of an integrated LPDDR4 SDRAM. This document only defines differences or exceptions to the ALW packaged AM6254 device defined in **AM62x Sitara Processors Datasheet** (revision B or later).

The AM625SIP (System in Package) Sitara™ MPU with integrated LPDDR4 is an application processor built for Linux development. The system in package integrates 512MB of LPDDR4 with the AM6254 device which has 4x Arm® Cortex®-A53 performance and embedded features, such as: dual-display support, 3D graphics acceleration, along with an extensive set of peripherals that make the System in package well-suited for a broad range of industrial applications while offering intelligent features and optimized power architecture. Additionally, the AM625SIP offers a simplified hardware design, increased robustness, optimized size/system BOM, and power consumption savings all enabling faster software and hardware development.

Some of these applications include:

- Industrial HMI
- Medical equipment, Patient monitoring, and Portable medical devices
- Smart home gateways & Appliances
- Embedded security: Control & Access panels

The 3-port Gigabit Ethernet switch has one internal port and two external ports with Time-Sensitive Networking (TSN) support. An additional PRU module on the device enables real-time I/O capability for customer's own use cases. In addition, the extensive set of peripherals included in AM625SIP enables system-level connectivity, such as: USB, MMC/SD, Camera interface, OSPI, CAN-FD and GPMC for parallel host interface to an external ASIC/FPGA. The AM625SIP device also supports secure boot for IP protection with the built-in Hardware Security Module (HSM) and employs advanced power management support for portable and power-sensitive applications

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AM625SIP	AMK (FCCSP BGA, 425)	13mm × 13mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

3.1 Functional Block Diagram

Figure 3-1 shows the functional block diagram for the device.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM62x Software Build Sheet* located in the Downloads tab option provided at **Processor-SDK-AM62x**.

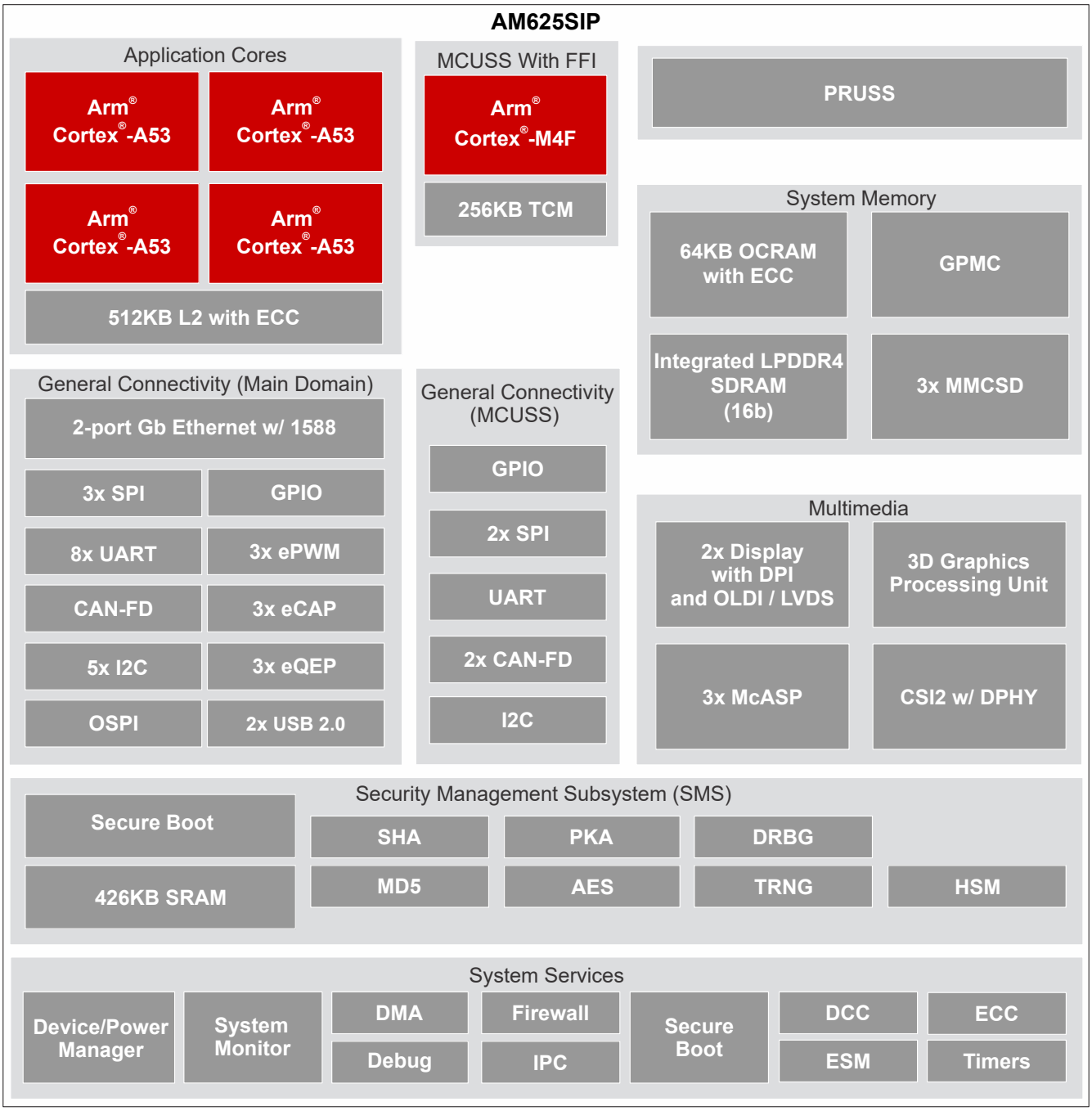

Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1 shows a comparison between devices, highlighting the differences.

Note

Availability of features listed in this table are a function of shared IO pins, where IO signals associated with many of the features are multiplexed to a limited number of pins. The SysConfig tool should be used to assign signal functions to pins. This will provide a better understanding of limitations associated with pin multiplexing.

Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), search for the *AM62x Software Build Sheet* located in the Downloads tab option provided at **Processor-SDK-AM62x**.

Table 4-1. Device Comparison

FEATURES	REFERENCE NAME	AM625SIP	AM625 (1)
		AM6254	**AM6254**
WKUP_CTRL_MMR_CFG0_JTAG_USER_ID[31:13](2) Register bit values by device "Features" code (See Device Naming Convention for more information on device features)			
	C:	-	0x1D123
	G:	-	0x1D127
	L:	0x1F120	-
PROCESSORS AND ACCELERATORS			
Speed Grades (See Device Speed Grades)		T	T, S, K, G
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Quad Core	
Arm Cortex-M4F in MCU domain	Arm M4F	Single Core No Functional Safety	Single Core Functional Safety (Optional)
3D Graphics Engine (OpenGL ES 3.1, Vulkan 1.2)	3D Graphics engine	Yes	
Device Management Subsystem	WKUP_R5F	Single core	
Crypto Accelerators	Security	Yes	
PROGRAM AND DATA STORAGE			
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	64KB (with SECDED ECC)	
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB	
DDR4/LPDDR4 DDR Subsystem	DDRSS	Integrated 512MB LPDDR4 SDRAM	16-bit data with inline ECC; up to 8GB using DDR4 or up to 4GB using LPDDR4
General-Purpose Memory Controller	GPMC	Up to 1GB with ECC	
PERIPHERALS			
Display Subsystem	DSS	1x DPI	
		1x LVDS	
Modular Controller Area Network Interface with Full CAN-FD Support	MCAN	3	
General-Purpose I/O	GPIO	Up to 170	
Inter-Integrated Circuit Interface	I2C	6	
Multichannel Audio Serial Port	MCASP	3	
Multichannel Serial Peripheral Interface	MCSPI	5	
Multi-Media Card/ Secure Digital Interface	MM/CSD	1x eMMC (8-bits)	
		2x SD/SDIO (4-bits)	
Flash Subsystem (FSS)(3)	OSPI0/QSPI0	Yes(3)	
Programmable Real-Time Unit Subsystem	PRUSS	2x PRU Cores	2x PRU Cores (Optional)

Table 4-1. Device Comparison (continued)

FEATURES	REFERENCE NAME	AM625SIP	AM625 (1)
		AM6254	AM6254
Industrial Communication Subsystem Support(4)	PRUSS	No	
Gigabit Ethernet Interface	CPSW3G	Yes	
General-Purpose Timers	TIMER	12 (4 in MCU Channel)	
Enhanced Pulse-Width Modulator Module	EPWM	3	
Enhanced Capture Module	ECAP	3	
Enhanced Quadrature Encoder Pulse Module	EQEP	3	
Universal Asynchronous Receiver and Transmitter	UART	9	
CSI2-RX Controller with DPHY	CSI-RX	1	
USB2.0 Controller with PHY	USB 2.0	2	

(1) This column is only provided as a quick reference of device feature relative to the AM625 family of devices. Refer to the **AM62x Sitara Processors Datasheet** for more information on AM625 feature codes, speed grades, and optional features.
(2) For more details about the WKUP_MMR0_JTAG_USER_ID register and DEVICE_ID bit field, see the device TRM.
(3) One flash interface, configured as OSPI0 or QSPI0.
(4) Industrial Communication Subsystem support is not available for this family of devices.

4.1 Related Products

Sitara™ processors are a broad family of scalable processors based on Arm® Cortex®-A cores with flexible accelerators, peripherals, connectivity, and unified software support – perfect for sensors to servers. Sitara processors have the reliability and functional safety support required for use in industrial and automotive applications.

Sitara™ microcontrollers are best-in-class Arm®-based 32-bit microcontrollers (MCUs) offering a scalable portfolio of high-performance and power-efficient devices to help meet your system needs. Bring capabilities such as functional safety, power efficiency, real-time control, advanced networking, analytics, and security to your designs.

AM64x Sitara™ processors target industrial applications such as Factory Automation and Control (FAC), and motor control that utilize Linux application processing cores (Cortex®-A53), real-time processing cores (Cortex®-R5F), and Industrial Communication Subsystems (PRU_ICSSGs) to support protocols such as EtherCAT, Profinet, or EtherNet/IP. AM64x implements one CPSW3G and two PRU_ICSSGs for supporting up to five gigabit Ethernet ports. The device also supports an extensive set of peripherals including a single lane of PCIe Gen2 or USB SuperSpeed Gen1, functional safety options, secure boot, and run-time security.

AM623 Sitara™ processors are an Internet of Things (IoT) and gateway SoC with Arm® Cortex®-A53-based object and gesture recognition. The low-cost AM623 Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance, embedded features such as dual-display support, and an extensive set of peripherals make the AM623 device well-suited for a broad range of industrial and automotive applications.

AM625 Sitara™ processors are a human-machine-interaction SoC with Arm® Cortex®-A53-and full-HD dual display. The low-cost AM625 Sitara™ MPU family of application processors are built for Linux® application development. With scalable Arm® Cortex®-A53 performance, embedded features such as dual-display support, 3D graphics acceleration, and an extensive set of peripherals make the AM625 device well-suited for a broad range of industrial and automotive applications.

AM62A3 Sitara™ and **AM62A7 Sitara™** processors are an embedded vision SoC that utilizes 1-4x Cortex A-53 ARM Cores and 1 or 2 TOPS analytics hardware accelerator. This scalable, high performance AM62Ax Sitara MPU family of application processors are built for Linux application development. AM62Ax is well suited for a broad range of industrial and automotive applications with embedded features such as h.264/h.265 encode/decode, secure boot, image signal processing and a deep learning accelerator.

Products to complete your design:

- Ethernet PHYs
- Power Management / PMICs
- Clocks and timing
- Power Switches
- CAN Transceivers
- ESD Protection

For more details of how these devices are implemented in a system design and a bill of materials for specific part number recommendations, see the SK-AM62-SIP EVM schematic.

5 Terminal Configuration and Functions

5.1 Pin Diagrams

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

Figure 5-1 shows a top view of the ball locations for the 425-ball grid array (FCCSP BGA) package to quickly locate signal names and ball grid numbering. The pin diagram in this document is intended to be used with *Pin Attributes and Signal Descriptions* section of this document along with the *Pin Attributes* through *Pin Connectivity Requirements* tables found in the **AM62x Sitara Processors Datasheet**.

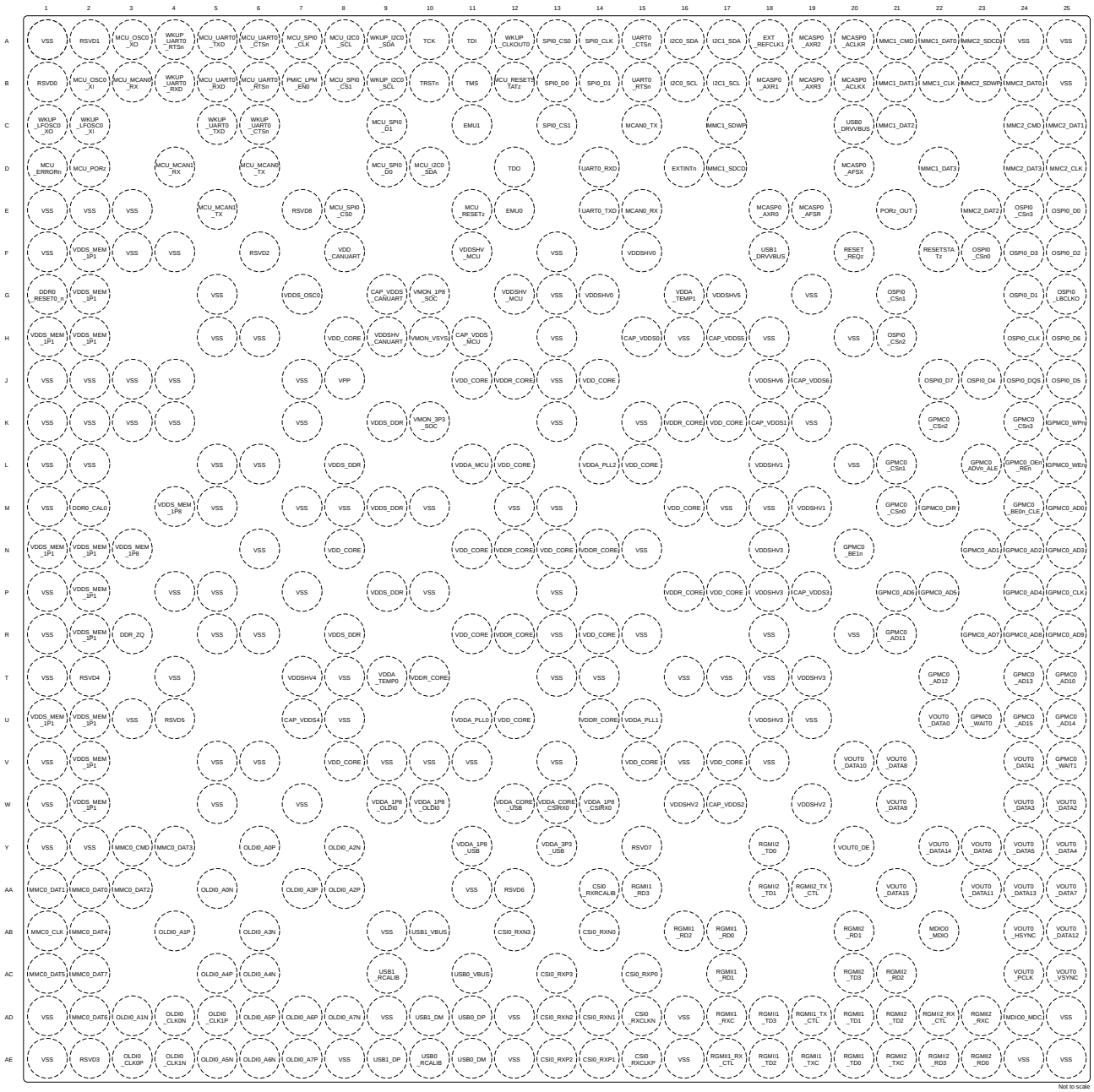

Figure 5-1. AMK FCCSP BGA Package (Top View)

5.2 Pin Attributes and Signal Descriptions

This section describes the AM625SIP device pins which have different power or signal functions relative to the ALW packaged AM6254 device. The AM6254 DDRSS0 signals in the ALW package that would normally connect to an external SDRAM were connected directly to an integrated LPDDR4 SDRAM in the AM625SIP device, and the pins associated with these signals were reassigned to different power or signal functions. Table 5-1 contains a list of ball numbers that were reassigned to new power or signal functions along with their new ball name and signal description.

Table 5-1. Reassigned DDRSS0 Pins on the AMK Package

BALL NUMBER	BALL NAME	Signal Description
M9	VDDS_DDR	DDR PHY IO supply
F2	VDDS_MEM_1P1	SDRAM IO supply (Sources the SDRAM VDD2 and VDDQ power rails)
G2		
H1		
H2		
N1		
N2		
P2		
R2		
U1		
U2		
V2		
W2		
M4	VDDS_MEM_1P8	SDRAM Core supply (Sources the SDRAM VDD1 power rail)
N3		
R3	DDR_ZQ	SDRAM Calibration Reference(1) (Connects to the SDRAM ZQ Calibration Reference)

Table 5-1. Reassigned DDRSS0 Pins on the AMK Package (continued)

BALL NUMBER	BALL NAME	Signal Description
E1	VSS	Ground (Connects to the SDRAM VSS and VSSQ grounds)
E2		
E3		
F1		
F3		
F4		
G5		
H5		
H6		
J1		
J2		
J3		
J4		
K1		
K2		
K3		
K4		
L1		
L2		
L5		
L6		
M1		
M5		
N6		
P1		
P4		
P5		
R1		
R5		
R6		
T1		
T4		
U3		
V1		
V5		
V6		
W1		
W5		
Y1		

(1) An external 240 Ω ±1% resistor must be connected between this pin and VDDS_MEM_1P1. The maximum power dissipation for the resistor is 8.33 mW.

6 Specifications

6.1 Absolute Maximum Ratings

Note

The values defined in the *Absolute Maximum Ratings* table were taken from the integrated LPDDR4 SDRAM datasheet. For additional absolute maximum rating details associated with the integrated LPDDR4 SDRAM, see the Integrated Silicon Solution (ISSI®) **IS43/46LQ16256B Datasheet**

over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER		MIN	MAX	UNIT
VDDS_MEM_1P1	SDRAM IO supply	–0.4	1.5	V
VDDS_MEM_1P8	SDRAM Core supply	–0.4	2.1	V
T_{STG}	Storage temperature	–55	150	℃

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Section 6.3, *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Note

The values defined in the *Recommended Operating Conditions* table were taken from the integrated LPDDR4 SDRAM datasheet. For additional recommended operating condition details associated with the integrated LPDDR4 SDRAM, see the Integrated Silicon Solution (ISSI®) **IS43/46LQ16256B Datasheet**

over operating junction temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN(1)	NOM	MAX(1)	UNIT
VDDS_MEM_1P1(2)	SDRAM IO supply		1.06	1.10	1.17	V
VDDS_MEM_1P8	SDRAM Core supply		1.70	1.80	1.95	V
T_J	Operating junction temperature range	Industrial	–40		95	°C

(1) The voltage at the device ball must never drop below the MIN voltage or rise above the MAX voltage for any amount of time during normal device operation.
(2) VDDS_MEM_1P1 must be sourced from the same power source as VDDS_DDR.

6.4 Operating Performance Points

This section describes maximum operating conditions of the device in Table 6-1 and describes each Operating Performance Point (OPP) for processor clocks and device core clocks in Table 6-2.

Table 6-1. Device Speed Grades

Speed Grade	VDD_CORE (V)(1)	MAXIMUM OPERATING FREQUENCY (MHz)								MAXIMUM TRANSITION RATE (MT/s)
		A53SS (Cortex-A53x)	GPU	PRU	Main Infra (CBA)	MCUSS (Cortex-M4F)	Device/ Power Manager (Cortex-R5F)	SMS Subsystem (Dual Cortex-M4F)	OCSRAM	LPDDR4
T	0.75/0.85	1250	500	333	250	400	400	400	400	1600
	0.85	1400								

(1) Nominal operating voltage, see *Recommended Operating Conditions*.

Table 6-2. Device Operating Performance Points

OPP	A53SS(1)	FIXED OPERATING FREQUENCY OPTIONS (MHz)(2)							MT/s
		GPU	PRU	MAIN INFRA (CBA)	MCUSS	DEVICE/ POWER MANAGER	SMS / SMS CBA	OCSRAM	LPDDR4
High	From ARM0 PLL Bypass to Speed Grade Maximum	500	333, 250, or 200	250	400 or 200	400	400	400	From DDR PLL Bypass(3) to 1600
Low		N/A		125		133	133	133	

(1) Default operating frequency, set by software at boot. Supports Dynamic Frequency Scaling after boot.
(2) Fixed operating frequency, set by software at boot.
(3) The DDR PLL output, which sources DDR0_CK0 and DDR0_CK0_n, is typically defined in units of frequency. So the "DDR PLL Bypass" transaction rate is equal to 2x the DDR PLL output frequency when operating in bypass mode.

6.5 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Section 6.3, *Recommended Operating Conditions*.

6.5.1 Thermal Resistance Characteristics for AMK Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	AMK PACKAGE °C/W(1) (2)	AIR FLOW (m/s)(3)
T1	$R\Theta_{JC}$	Junction-to-case	5.1	N/A
T2	$R\Theta_{JB}$	Junction-to-board	5.2	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	18.7	0
T4		Junction-to-moving air	12.6	1
T5			11.5	2
T6			11.0	3
T7	Ψ_{JT}	Junction-to-package top	0.3	0
T8			0.4	1
T9			0.5	2
T10			0.5	3
T11	Ψ_{JB}	Junction-to-board	5.1	0
T12			4.8	1
T13			4.7	2
T14			4.7	3

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(3) m/s = meters per second.

6.6 Timing and Switching Characteristics

6.6.1 Power Supply Requirements

This section describes the power supply requirements to ensure proper device operation.

Note

All power balls must be supplied with the voltages specified in the *Recommended Operating Conditions* section.

6.6.1.1 Power Supply Sequencing

This section describes the device power sequence requirements for the VDDS_MEM_1P1 and VDDS_MEM_1P8 power rails relative to the other device power rails, which have been defined in the *Power-Up Sequencing* and *Power-Down Sequencing* sections of the **AM62x Sitara Processors Datasheet**.

The VDDS_MEM_1P1 power rail should be sourced from the same power supply that is sourcing VDDS_DDR. Therefore, the VDDS_MEM_1P1 power rail should ramp up and down with the power rails associated with waveform E.

The VDDS_MEM_1P8 power rail should ramp up and down with the power rails associated with waveform C.

For additional power sequence requirement details associated with the integrated LPDDR4 SDRAM, see the Integrated Silicon Solution (ISSI®) **IS43/46LQ16256B Datasheet** .

7 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Peripheral- and Interface-Specific Design Information

7.1.1 Integrated LPDDR4 SDRAM Information

The integrated LPDDR4 SDRAM is equivalent to an Integrated Silicon Solution (ISSI®) part number IS43LQ16256. For more information, refer to the **IS43/46LQ16256B Datasheet**.

8 Device and Documentation Support

8.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM6254ATLHJAMK). Texas Instruments recommends two of three possible prefix designators for related support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null (BLANK) Production version of the silicon die that is fully qualified and meets final electrical specifications.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM625SIP devices in the AMK package type, see the Package Option Addendum at the end of this document, the TI website (ti.com), or contact your TI sales representative.

8.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

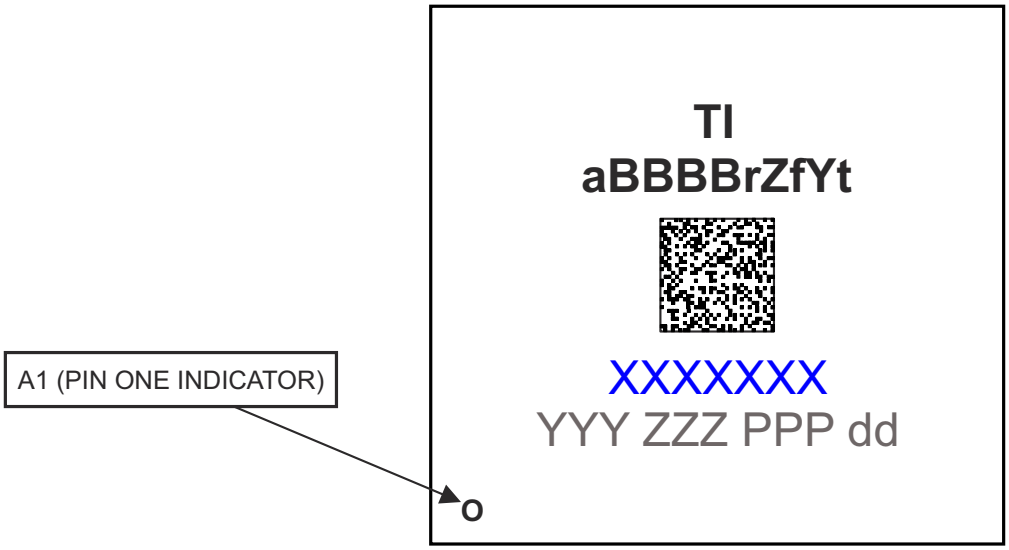

Figure 8-1. Printed Device Reference

8.1.2 Device Naming Convention

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK(1)	Production
–	Part Number Prefix	AM	Not symbolized
BBBB	Base production part number	6254	See Table 4-1, Device Comparison
r	Device revision	A	SR1.0
Z	Device Speed Grade	T	See Table 6-1, Device Speed Grades
f	Features (see Table 4-1)	L	Feature code "C" AM6254 device with Integrated 512MB LPDDR4 SDRAM
Y	Security / Functional Safety	G	Non-secure / No Functional Safety
		1 to 9	Secure with Dummy Key / No Functional Safety
		H to R	Secure with Production Key / No Functional Safety
t	Temperature(2)	J	–40°C to 95°C - Industrial (see Section 6.3, *Recommended Operation Conditions*)
	2D Barcode	Varies	Optional 2D barcode, provides additional device information
		BLANK	
xxxxxxx			Lot Trace Code (LTC)
YYY			Production Code, For TI use only
ZZZ			Production Code, For TI use only
PPP	Package Designator	AMK	FCCSP BGA (425-pin)
dd			Pre-Production Code, For TI use only
•			Pin one designator

(1) BLANK in the symbol or part number is collapsed so there are no gaps between characters.
(2) Applies to device max junction temperature.

8.2 Tools and Software

The following Development Tools support development for TI's Embedded Processing platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. The tool includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Tool is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool generates output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements. The **Cloud-based SysConfig-PinMux Tool** is also available.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the AM625SIP devices.

Technical Reference Manual

AM62x Sitara Processors Technical Reference Manual: Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM625SIP family of devices.

Errata

AM62x Sitara Processors Silicon Errata: Describes the known exceptions to the functional specifications for the device.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

Code Composer Studio™ and TI E2E™ are trademarks of Texas Instruments.
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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from November 16, 2023 to June 16, 2024 (from Revision * (NOVEMBER 2023) to Revision A (JUNE 2024)) — **Page**

- **Global**: Changed the document product status from "Advance Information" (AI) to "Production Data" (PD).... 1

10 Mechanical, Packaging, and Orderable Information

10.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM6254ATLHJAMKR	ACTIVE	FCCSP	AMK	425	1000	RoHS (In Work) & Green	Call TI	Level-3-260C-168 HR	-40 to 95	6254ATLHJ 131 SIP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

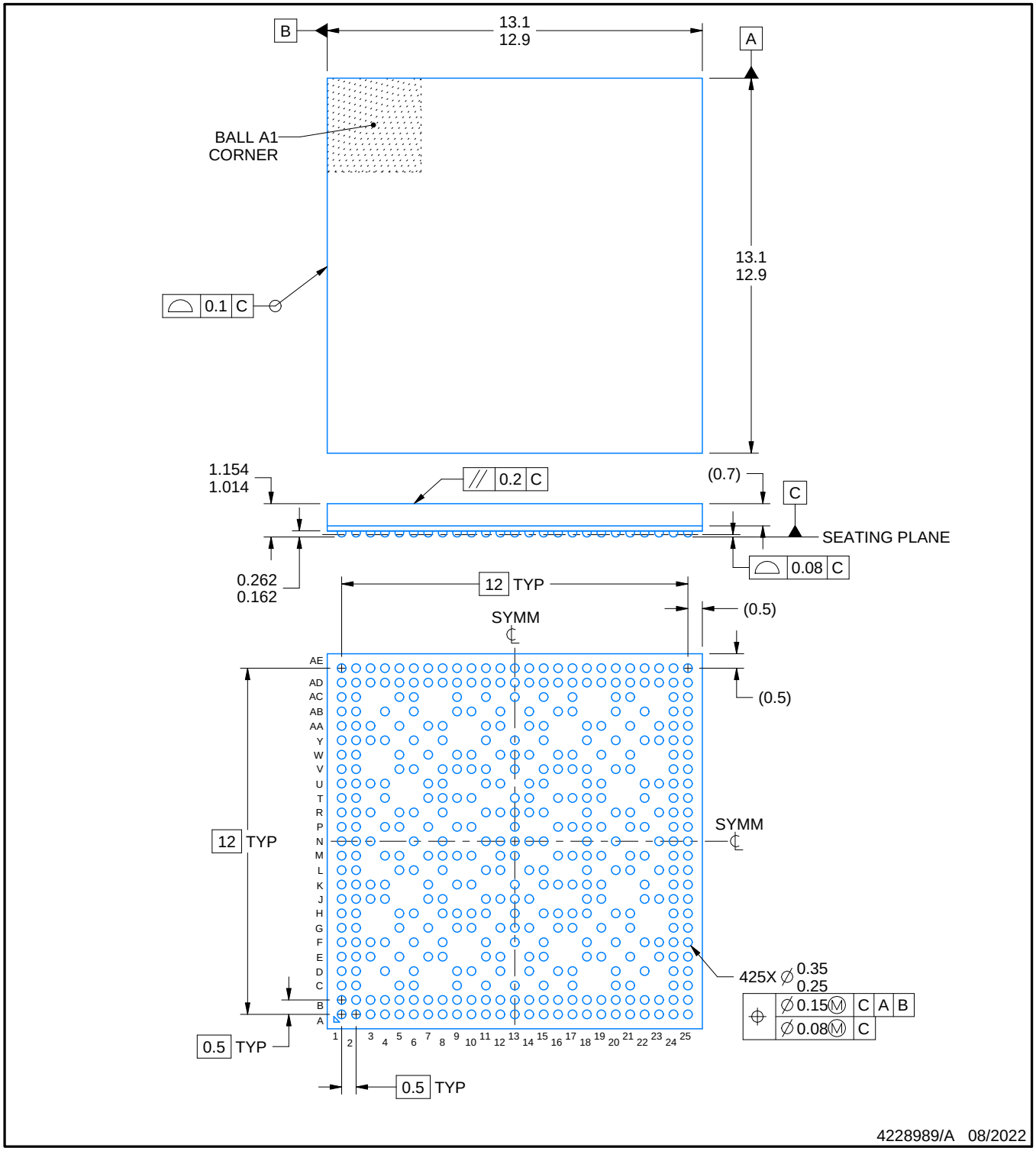
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

AMK0425A

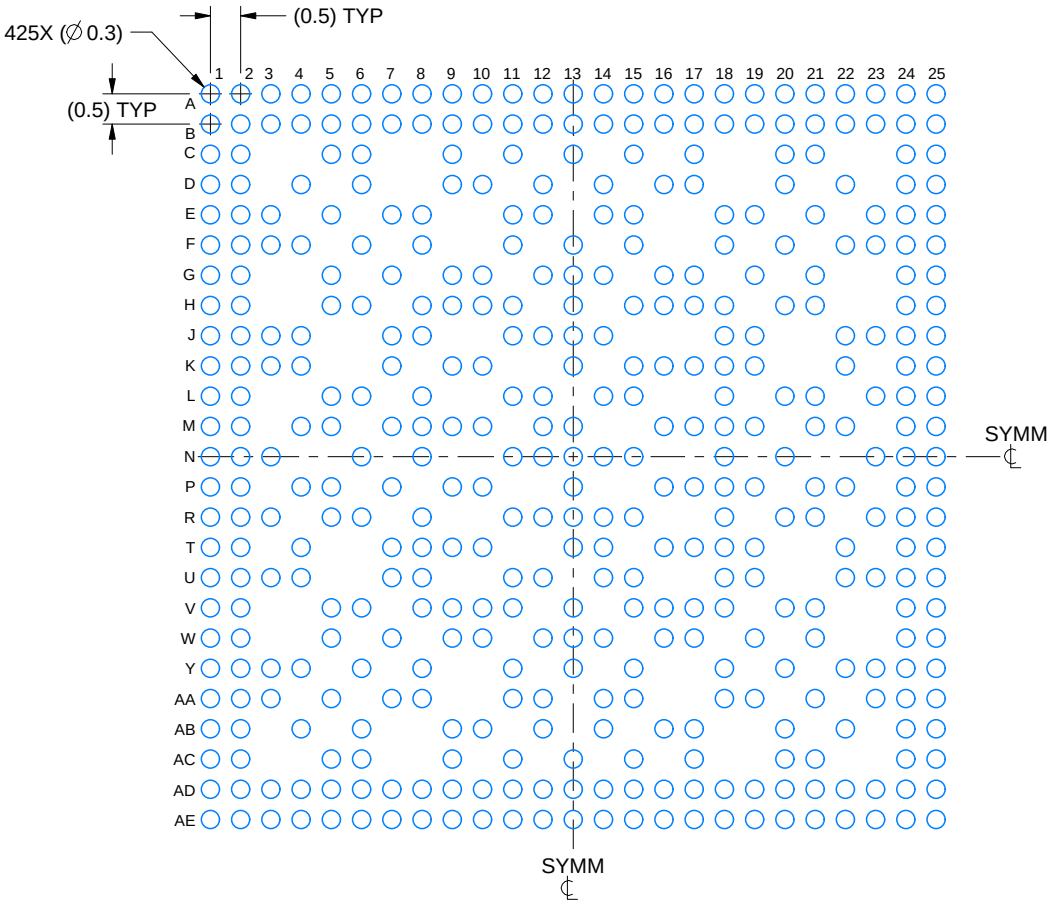
FCBGA - 1.154 mm max height

PLASTIC BALL GRID ARRAY

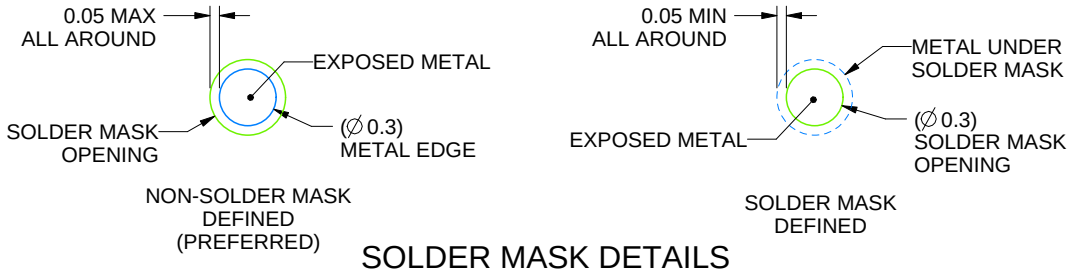


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

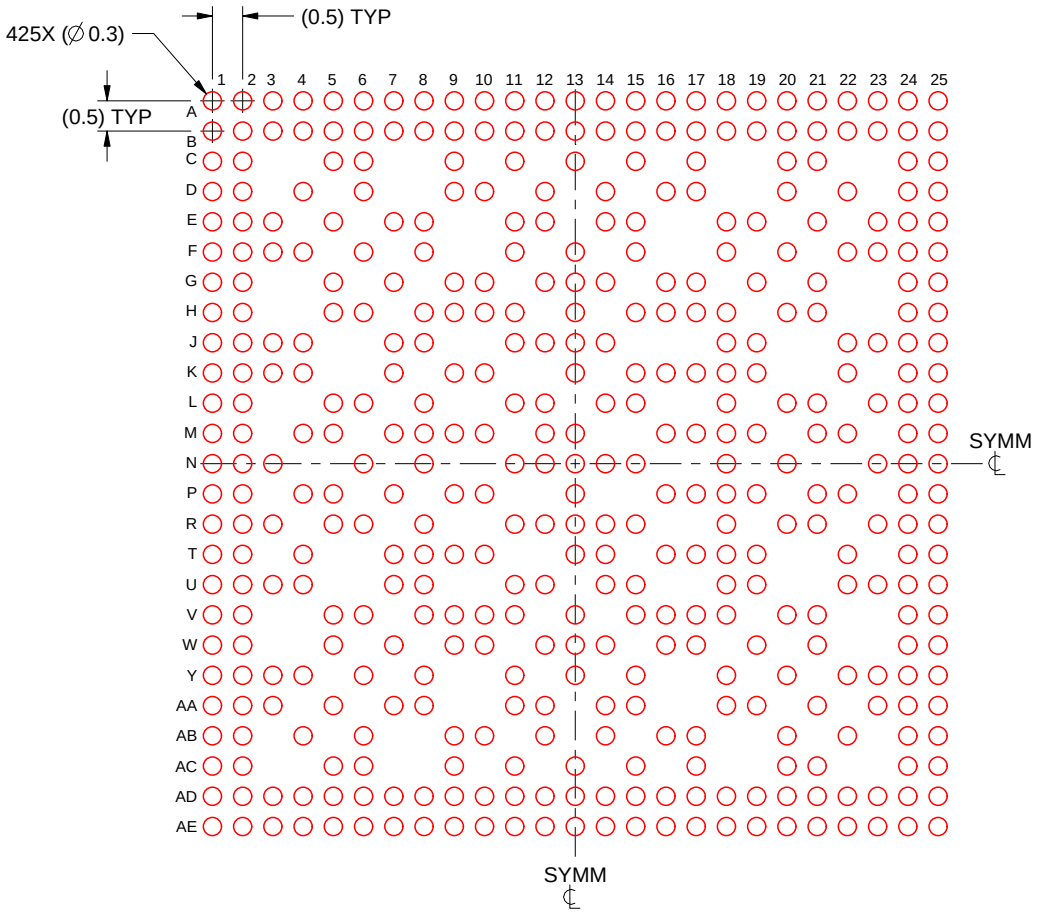


SOLDER MASK DETAILS
NOT TO SCALE

4228989/A 08/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4228989/A 08/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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