AMC0x03M2510 Precision, ±250mV Input Isolated Delta-Sigma Modulators With Internal Clock

1 Features

- Linear input voltage range: ±250mV
- Supply voltage range:
  - High-side (AVDD): 3.0V to 5.5V
  - Low-side (DVDD): 2.7V to 5.5V
- Low DC errors:
  - Offset error: ±200μV (maximum)
  - Offset drift: ±2μV/°C (maximum)
  - Gain error: ±0.2% (maximum)
  - Gain drift: ±30ppm/°C (maximum)
- High CMTI: 150V/ns (minimum)
- Missing high-side supply detection
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings:
  - AMC0203M2510: Basic isolation
  - AMC0303M2510: Reinforced Isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577
- Fully specified over the extended industrial temperature range: –40°C to +125°C

2 Applications

- Motor drives
- Photovoltaic inverters
- Server power-supply units (PSU)
- Energy storage systems

3 Description

The AMC0x03M2510 is a precision, galvanically isolated delta-sigma (ΔΣ) modulator with a ±250mV input and internal clock. The input is optimized for connection to low-impedance shunt resistors commonly used for current-sensing applications.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to 5kV$_{RMS}$ (DWV package) and basic isolation up to 3kV$_{RMS}$ (D package) (60s).
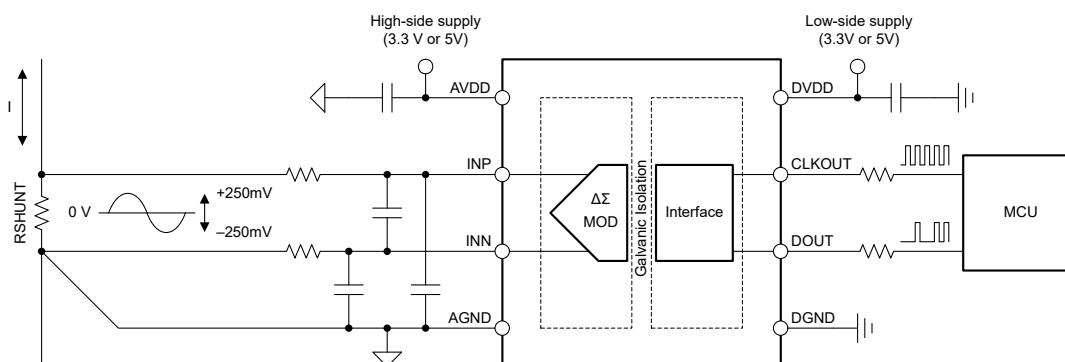
The output bitstream of the AMC0x03M2510 is synchronized to the internally generated 10MHz clock. Combined with a sinc3, OSR 256 filter, the device achieves 12.8 effective bits of resolution or 80dB of dynamic range, at a 39kSPS sample rate.

The AMC0x03M2510 comes in 8-pin, wide- and narrow-body SOIC packages. The device is fully specified over the temperature range from –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
AMC0203M2510	D (SOIC 8)	4.9mm × 6mm
AMC0303M2510	DWV (SOIC 8)	5.85mm × 11.50mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* .
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Typical Application

Table of Contents

4 Device Comparison Table

PARAMETER	AMC0203M2510	AMC0303M2510
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

5 Pin Configuration and Functions

AVDD	1 ⭕	8 DVDD
INP	2	7 CLKOUT
INN	3	6 DOUT
AGND	4	5 DGND

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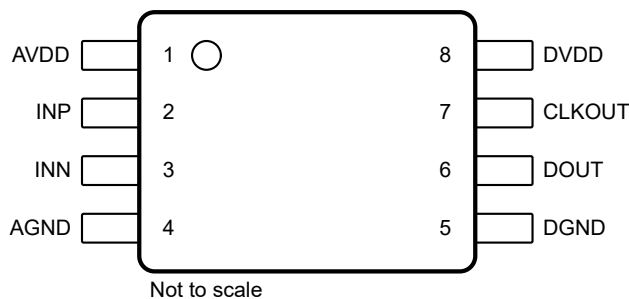
Figure 5-1. DWV and D Packages, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	AVDD	High-side power	Analog (high-side) power supply[1]
2	INP	Analog input	Noninverting analog input[2]
3	INN	Analog Input	Inverting analog input[2]
4	AGND	High-side ground	Analog (high-side) ground
5	DGND	Low-side ground	Digital (low-side) ground
6	DOUT	Digital output	Modulator data output
7	CLKOUT	Digital output	Modulator clock output
8	DVDD	Low-side power	Digital (low-side) power supply[1]

(1)   See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2)   See the *Input Filter Design* section for input filter design.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Power-supply voltage	High-side AVDD to AGND	−0.3	6.5	V
	Low-side DVDD to DGND	−0.3	6.5	
Analog input voltage	INP, INN to AGND	AGND − 4	AVDD + 0.5	V
Digital output voltage	DOUT, CLKOUT to DGND	DGND − 0.5	DVDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	−10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	−65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	High-side power supply	AVDD to AGND	3	5.0	5.5	V
DVDD	Low-side power supply	DVDD to DGND	2.7	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} - V_{INN}$		±320		mV
V_{FSR}	Specified linear differential input voltage	$V_{IN} = V_{INP} - V_{INN}$	−250		250	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to AGND	−0.16		1	V
$C_{IN, EXT}$	Minimum external capacitance connected to the input	from INP to INN		10		nF
TEMPERATURE RANGE						
T_A	Specified ambient temperature		−40		125	°C

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.4 Thermal Information (D Package)

THERMAL METRIC[1]		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Thermal Information (DWV Package)

THERMAL METRIC[1]		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	AVDD = DVDD = 5.5V	63	mW
P_{D1}	Maximum power dissipation (high-side)	AVDD = 5.5V	30	mW
P_{D2}	Maximum power dissipation (low-side)	DVDD = 5.5V	33	mW

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1130	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	800	V_{RMS}
		At DC voltage	1130	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage[3]	Tested in air, 1.2/50μs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[4]	Tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge[5]	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, $t_{ini} = 60s$, $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10s$	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, $t_{ini} = 60s$, $V_{pd(m)} = 1.3 \times V_{IORM}$, $t_m = 10s$	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, $t_{ini} = 1s$, $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m = 1s$	≤ 5	
		Method b2, at routine test (100% production)[7], $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$, $t_{ini} = t_m = 1s$	≤ 5	
C_{IO}	Barrier capacitance, input to output[6]	$V_{IO} = 0.5V_{PP}$ at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output[6]	$V_{IO} = 500V$ at $T_A = 25°C$	> 10^{12}	Ω
		$V_{IO} = 500V$ at $100°C ≤ T_A ≤ 125°C$	> 10^{11}	
		$V_{IO} = 500V$ at $T_S = 150°C$	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 6000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage[3]	Tested in air, 1.2/50μs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[4]	Tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge[5]	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)}$ = 1.2 x V_{IOTM}, t_{ini} = 1s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)[7] $V_{pd(ini)}$ = $V_{pd(m)}$ = 1.2 × V_{IOTM}, t_{ini} = t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output[6]	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output[6]	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

6.11 Safety Limiting Values (D Package)

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 116.5°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			195	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 116.5°C/W, T_J = 150°C, T_A = 25°C			1070	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.12 Safety Limiting Values (DWV Package)

Safety limiting[1] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			220	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1210	mW
T_S	Maximum safety temperature				150	°C

(1)   The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.

$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

6.13 Electrical Characteristics

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5 V, V_{INP} = –250mV to 250mV, V_{INN} = 0V, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{IN}	Effective input sampling capacitance			1.8		pF
R_{IN}	Input impedance		50	55	60	kΩ
I_{INP}	Input current	V_{IN} = (V_{INP} – V_{INN}) = $V_{FSR, MAX}$		4.5		µA
I_{INN}	Input current	V_{IN} = (V_{INP} – V_{INN}) = $V_{FSR, MAX}$		–4.5		µA
CMTI	Common-mode transient immunity		150			V/ns
DC ACCURACY						
E_O	Offset error[1] [2]	INP = INN = AGND, T_A = 25°C	–200	±9	200	µV
TCE_O	Offset error temperature drift[4]		–2		2	µV/°C
E_G	Gain error	T_A = 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error temperature drift[2] [5]		–30	±10	30	ppm/°C
INL	Integral nonlinearity[3]	Resolution: 16 bits	–4	±1	4	LSB
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
	DC output noise	INP = INN = AGND		6.5		µV$_{RMS}$
CMRR	Common-mode rejection ratio	INP = INN, f_{IN} = 0Hz, $V_{CM\ min}$ ≤ V_{IN} ≤ $V_{CM\ max}$		–92		dB
		INP = INN, f_{IN} from 0.1Hz to 10 kHz, $V_{CM\ min}$ ≤ V_{IN} ≤ $V_{CM\ max}$		–97		
PSRR	Power-supply rejection ratio	INP = INN = AGND, AVDD from 3.0V to 5.5V, DC		–87		dB
		INP = INN = AGND, AVDD from 3.0V to 5.5V, 10kHz / 100mV ripple		–87		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 35Hz		80		dB
THD	Total harmonic distortion[6]	3.0V ≤ AVDD ≤ 5.5V, f_{IN} = 1kHz		–108	–81	dB
DIGITAL INPUT (CMOS Logic With Schmitt-Trigger)						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
DIGITAL OUTPUT (CMOS)						
C_{LOAD}	Output load capacitance			15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –4mA	DVDD – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
POWER SUPPLY						
I_{AVDD}	High-side supply current			4.5	5.5	mA
I_{DVDD}	Low-side supply current	C_{LOAD} = 15pF		4.1	6.0	mA
$AVDD_{UV}$	High-side undervoltage detection threshold	AVDD rising	2.4	2.6	2.8	V
		AVDD falling	1.9	2.05	2.2	

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.13 Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –40°C to 125°C, AVDD = 3.0V to 5.5V, DVDD = 2.7V to 5.5 V, V_{INP} = –250mV to 250mV, V_{INN} = 0V, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, AVDD = 5V, and DVDD = 3.3V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DVDD$_{UV}$	Low-side undervoltage detection threshold	DVDD rising	2.3	2.5	2.7	V
		DVDD falling	1.9	2.05	2.2	

(1) This parameter is input referred.
(2) The typical value includes one sigma statistical variation.
(3) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCE_O = (E_{O,MAX} – E_{O,MIN})$ / TempRange where $E_{O,MAX}$ and $E_{O,MIN}$ refer to the maximum and minimum E_O values measured within the temperature range (–40 to 125℃).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G (ppm) = ((E_{G,MAX} - E_{G,MIN})$ / TempRange$) x 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125℃).
(6) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.

6.14 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Internal clock frequency		9.4	10	10.6	MHz
d_{CLK}	Internal clock duty cycle	$d_{CLK} = t_{HIGH} / t_{CLK}$, $t_{CLK} = 1/f_{CLK}$	45%	50%	55%	
t_H	DOUT hold time after rising edge of CLKOUT	C_{LOAD} = 15pF	7			ns
t_D	DOUT delay time after rising edge of CLKOUT	C_{LOAD} = 15pF			16	ns
t_r	DOUT and CLKOUT rise time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15 pF		2.5	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15 pF		3.0	6	
t_f	DOUT and CLKOUT fall time	10% to 90%, 2.7V ≤ DVDD ≤ 3.6V, C_{LOAD} = 15 pF		2.7	6	ns
		10% to 90%, 4.5V ≤ DVDD ≤ 5.5V, C_{LOAD} = 15 pF		3.3	6	
t_{START}	Device start-up time	AVDD step from 0 to 3.0V with DVDD ≥ 2.7V to bitstream valid, 0.1% settling		100		µs

6.15 Timing Diagrams
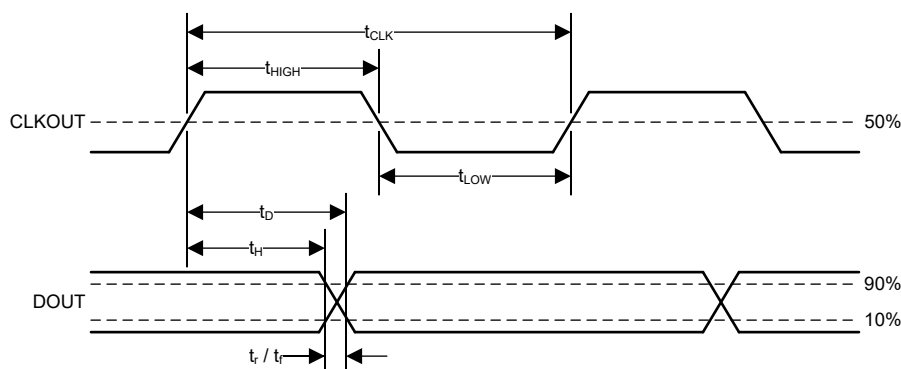
Figure 6-1. Digital Interface Timing
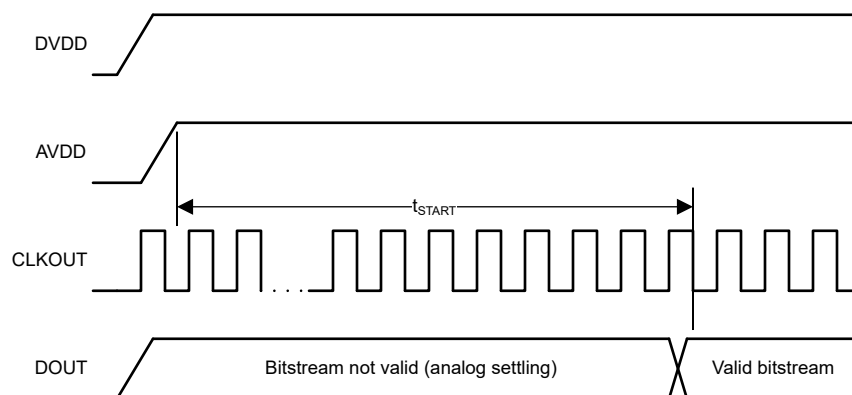
Figure 6-2. Device Start-Up Timing

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.16 Insulation Characteristics Curves
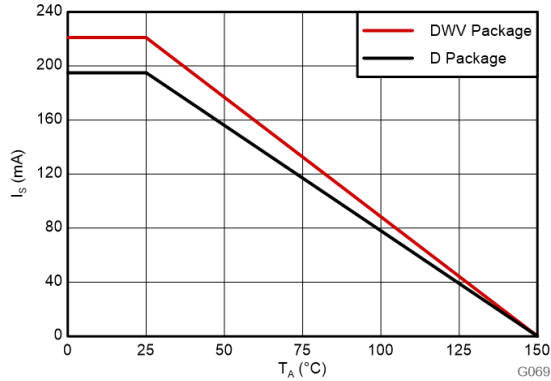
Figure 6-3. Thermal Derating Curve for Safety-Limiting Current per VDE
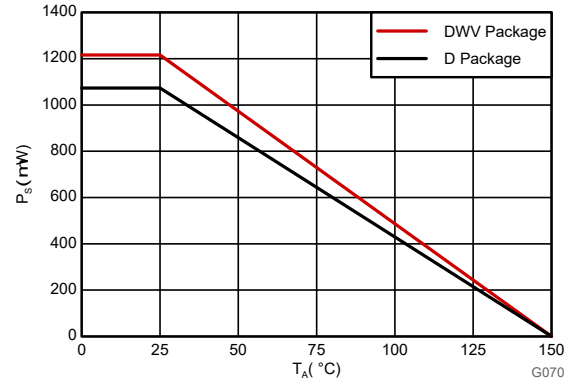
Figure 6-4. Thermal Derating Curve for Safety-Limiting Power per VDE
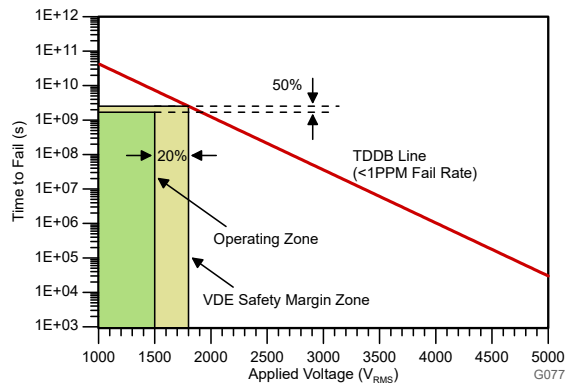
T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, projected operating lifetime ≥50 years

Figure 6-5. Isolation Capacitor Lifetime Projection (Reinforced Isolation)
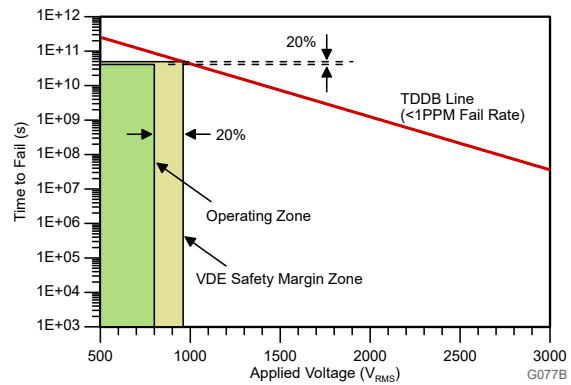
T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 800V_{RMS}, projected operating lifetime >>100 years

Figure 6-6. Isolation Capacitor Lifetime Projection (Basic Isolation)

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.17 Typical Characteristics

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –250mV to +250mV, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)
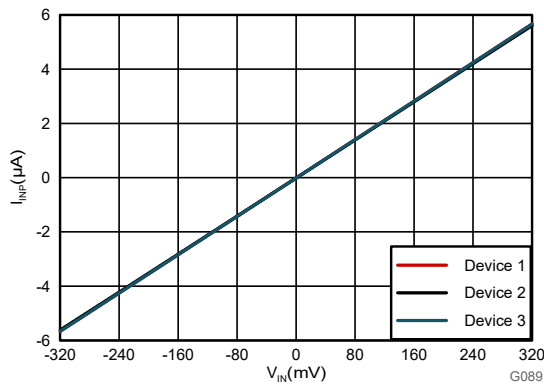
Figure 6-7. Input Current vs Input Voltage (INP Pin)
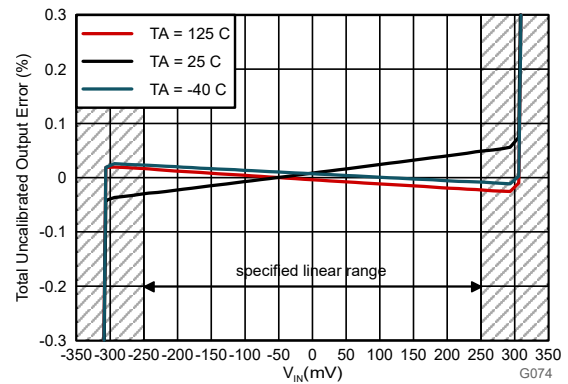
Total uncalibrated output error (in %) is defined as:

$$[(\text{Output Code} / 2^{16}) - ((V_{IN} + 320\text{mV}) / 640\text{mV})] \times 100,$$
$$\text{where } V_{IN} = (V_{INP} - V_{INN})$$

Figure 6-8. Total Uncalibrated Output Error vs Input Voltage
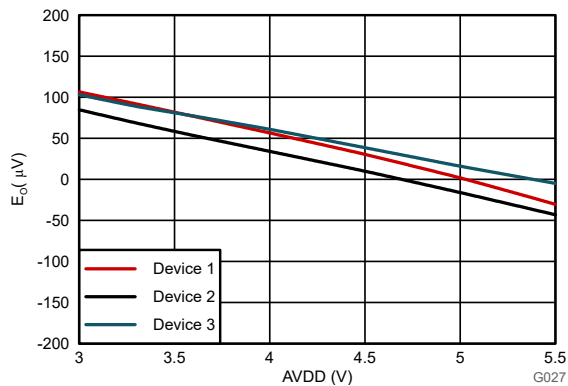
Figure 6-9. Offset Error vs High-Side Supply Voltage
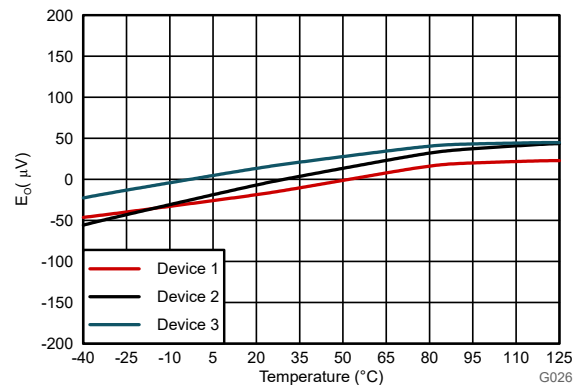
Figure 6-10. Offset Error vs Temperature
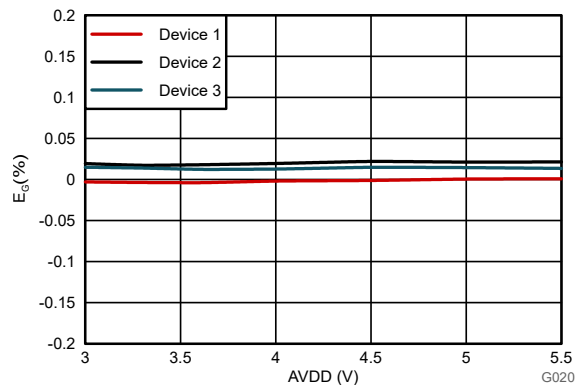
Figure 6-11. Gain Error vs High-Side Supply Voltage
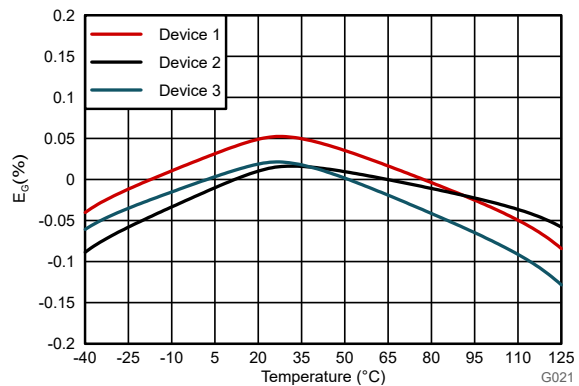
Figure 6-12. Gain Error vs Temperature

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –250mV to +250mV, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)
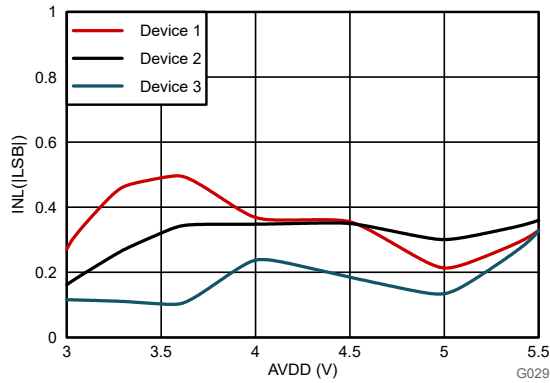

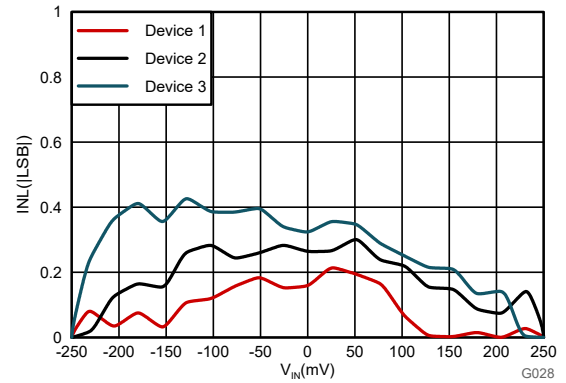**Figure 6-13. Integral Nonlinearity vs High-Side Supply Voltage**

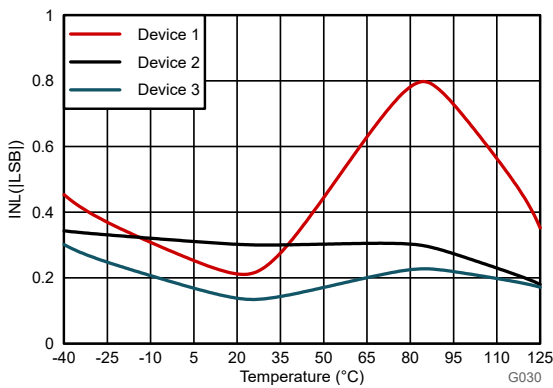**Figure 6-14. Integral Nonlinearity vs Input Voltage**
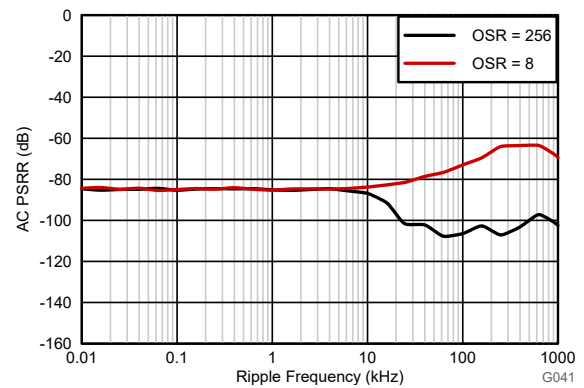

Figure 6-15. Integral Nonlinearity vs Temperature

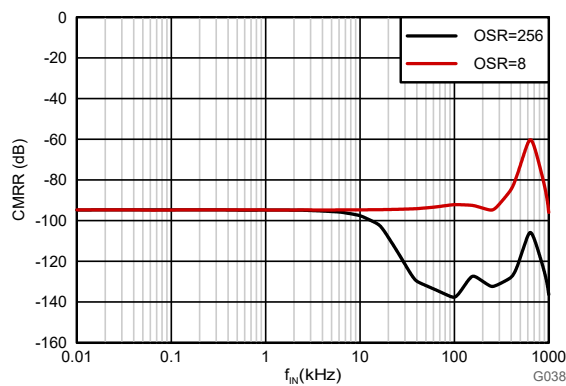**Figure 6-16. Power-Supply Rejection Ratio vs Ripple Frequency**

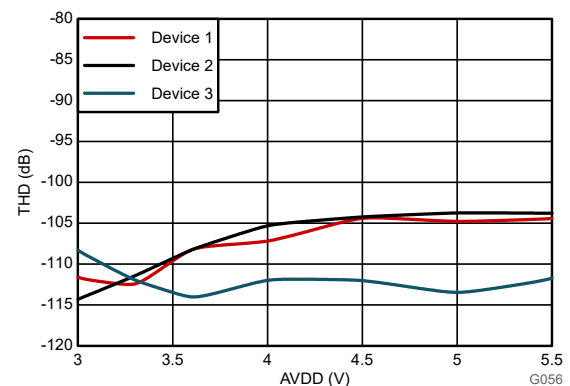**Figure 6-17. Common-Mode Rejection Ratio vs Input Signal Frequency**

Figure 6-18. Total Harmonic Distortion vs High-Side Supply Voltage

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –250mV to +250mV, INN = AGND, and sinc[3] filter with OSR = 256 (unless otherwise noted)
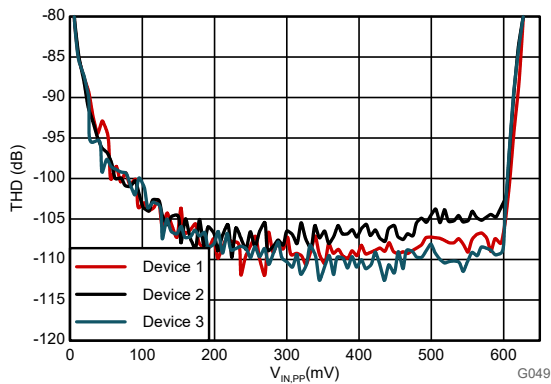

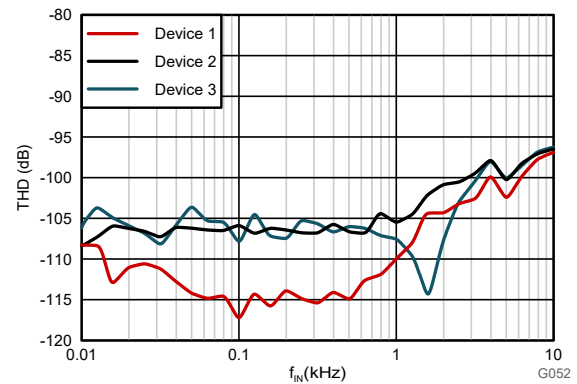**Figure 6-19. Total Harmonic Distortion vs Input Signal Amplitude**

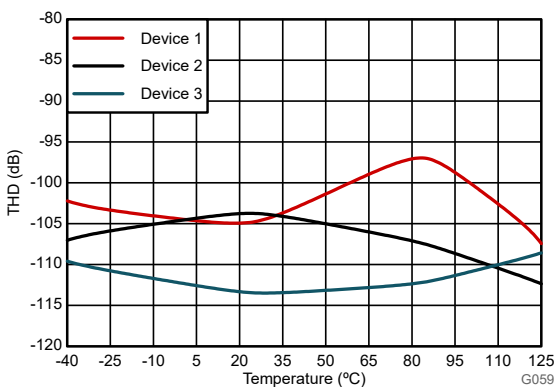**Figure 6-20. Total Harmonic Distortion vs Input Signal Frequency**

Figure 6-21. Total Harmonic Distortion vs Temperature
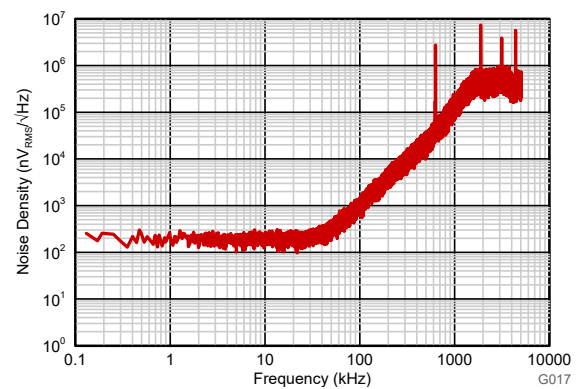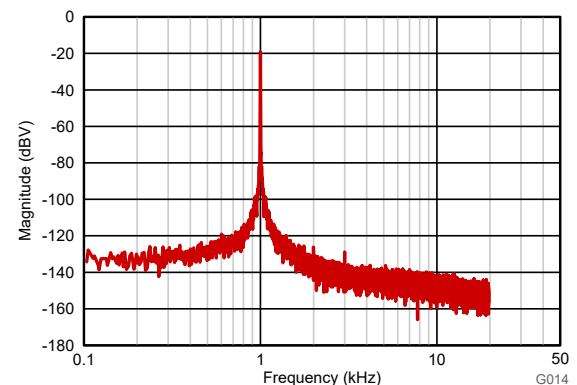

sinc[3], OSR = 1, frequency bin width = 1Hz

Figure 6-22. Noise Density With Both Inputs Shorted to HGND
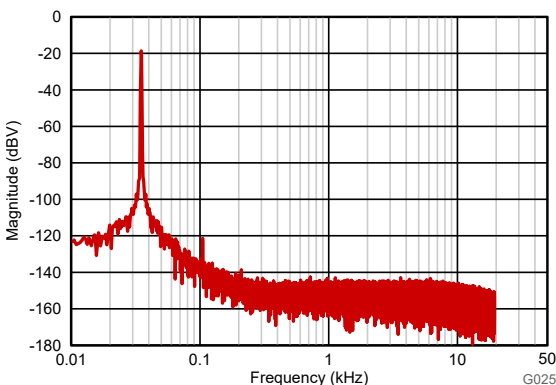
sinc[3], OSR = 256, V_{IN} = 500mV$_{PP}$

Figure 6-23. Frequency Spectrum With 35Hz Input Signal

sinc[3], OSR = 256, V_{IN} = 500mV$_{PP}$

Figure 6-24. Frequency Spectrum With 1kHz Input Signal

Product Folder Links: *AMC0203M2510 AMC0303M2510*

6.17 Typical Characteristics (continued)

at AVDD = 5V, DVDD = 3.3V, V_{INP} = –250mV to +250mV, INN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted)

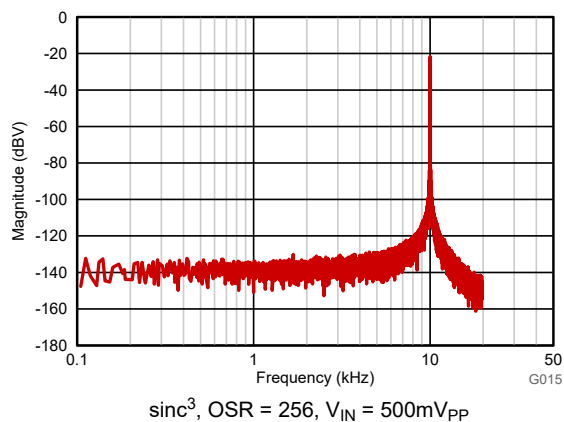sinc^3, OSR = 256, V_{IN} = 500mV$_{PP}$

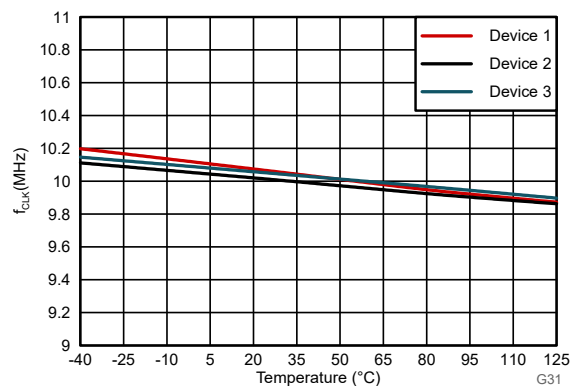**Figure 6-25. Frequency Spectrum With 10kHz Input Signal**

Figure 6-26. Internal Clock Frequency vs Temperature
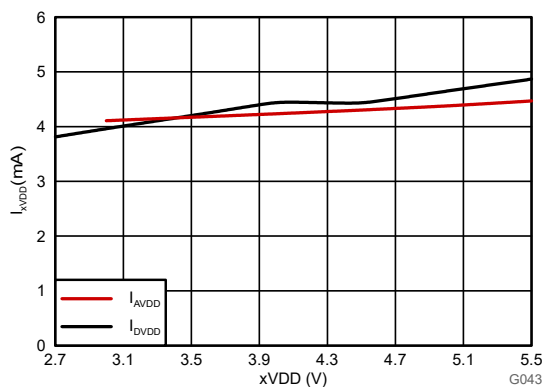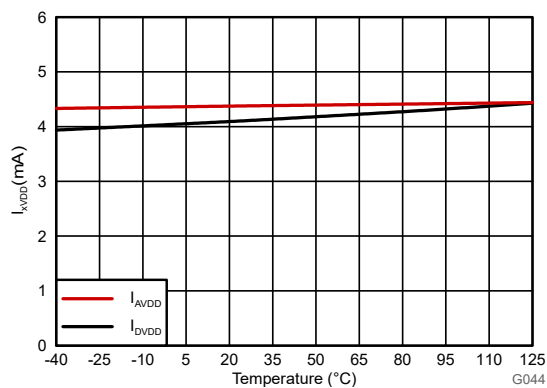
Figure 6-27. Supply Current vs Supply Voltage

Figure 6-28. Supply Current vs Temperature

Product Folder Links: *AMC0203M2510 AMC0303M2510*

7 Detailed Description

7.1 Overview

The AMC0x03M2510 is a single-channel, second-order, CMOS, delta-sigma (ΔΣ) modulator designed for high resolution shunt-based current sensing. The differential analog input is implemented with a switched-capacitor circuit. The isolated output of the converter (DOUT) provides a stream of digital ones and zeros synchronous to the internally generated clock available at the CLKOUT pin. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies; therefore, use a digital low-pass digital filter, such as a Sinc filter at the device output to increase overall performance. This filter also converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). Use a microcontroller (µC) or field-programmable gate array (FPGA) to implement the filter.

The overall performance (speed and resolution) depends on the selection of an appropriate oversampling ratio (OSR) and filter type. A higher OSR results in higher resolution while operating at a lower refresh rate. A lower OSR results in lower resolution, but provides data at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of analog-to-digital conversion results with a dynamic range exceeding 80dB with OSR = 256.

The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity; see the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The AMC0x03M2510 uses an on-off keying (OOK) modulation scheme to transmit data across the isolation barrier. This modulation and the isolation barrier characteristics, result in high reliability in noisy environments and high common-mode transient immunity.

7.2 Functional Block Diagram
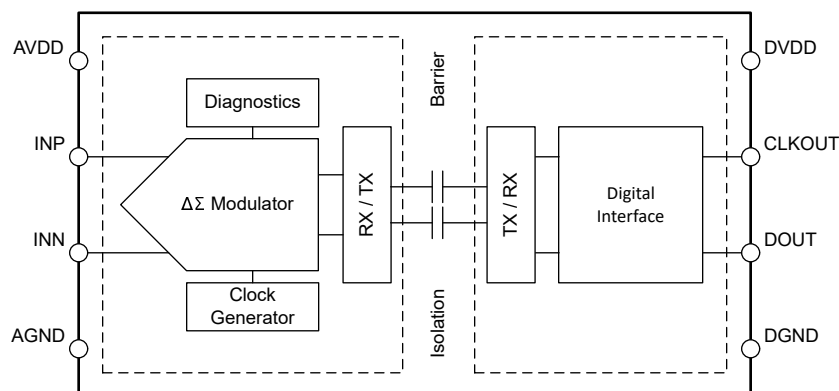
7.3 Feature Description

7.3.1 Analog Input

As shown in Figure 7-1, input of the AMC0x03M2510 has a fully differential, switched-capacitor circuit. The AMC0x03M2510 has a dynamic input impedance of 55kΩ at 10MHz .

The sampling capacitor is continuously charged and discharged with a frequency of f_{CLK}. With the S1 switches closed, C_{IND} charges to the voltage difference across V_{INP} and V_{INN}. For the discharge phase, both S1 switches open first and then both S2 switches close. C_{IND} discharges to approximately AGND + 0.8V during this phase.
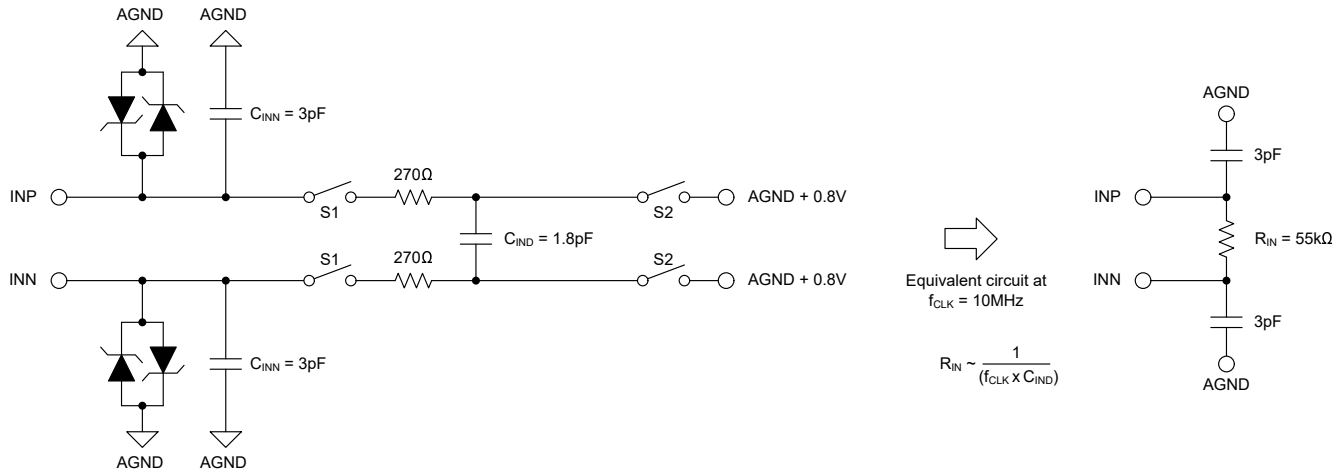
Figure 7-1. Equivalent Input Circuit

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. There are two restrictions on the analog input signals (INP and INN).

- First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, limit the input current to the absolute maximum value. This is to prevent device input electrostatic discharge (ESD) diode damage due to high current.
- Second, keep the differential analog input voltage within the specified full-scale range (V_{FSR}) and input common-mode voltage range (V_{CM}) ranges. V_{FSR} and V_{CM} are specified in the *Recommended Operating Conditions* table. The device noise and linearilty performance is guaranteed only in this range.

7.3.2 Modulator

Figure 7-2 conceptualizes the second-order, switched-capacitor, feed-forward ΔΣ modulator implemented in the AMC0x03M2510. The output V_5 of the 1-bit, digital-to-analog converter (DAC) is subtracted from the input voltage $V_{IN} = (V_{INP} - V_{INN})$. This subtraction provides an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage. The result of the second integration is an output voltage V_3 that is summed with V_{IN} and the V_2 output. V_{IN} is the input signal and V_2 is the first integrator. Depending on the value of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5. Thus, causing the integrators to progress in the opposite direction and forcing the integrator output value to track the average value of the input.

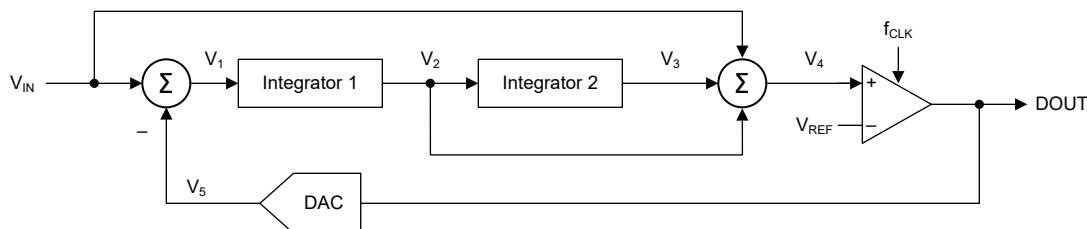**Figure 7-2. Block Diagram of the Second-Order Modulator**

For reduced offset and offset drift, the integrators are chopper-stabilized with the chopping frequency set at $f_{CLK}/16$. Figure 7-3 shows the spur at 625KHz that is generated by the chopping frequency for a modulator clock of 10MHz.

sinc^3 filter, OSR = 1, f_{CLK} = 10MHz, f_{IN} = 1kHz
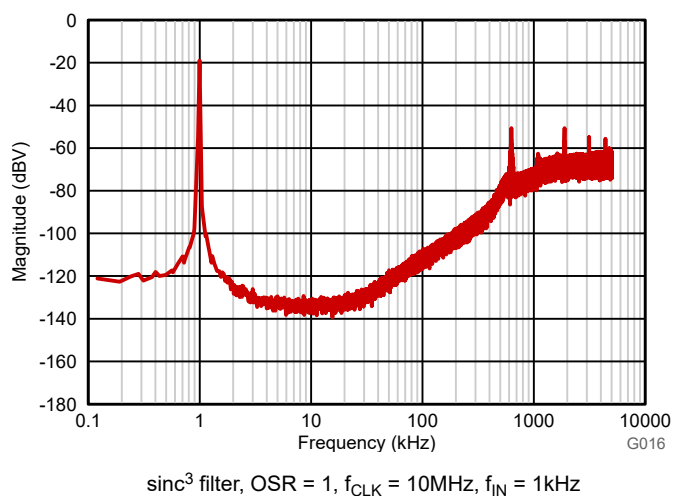
Figure 7-3. Quantization Noise Shaping

7.3.3 Isolation Channel Signal Transmission

As shown in Figure 7-4, the AMC0x03M2510 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) is illustrated in the *Functional Block Diagram* . TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x03M2510 is 480MHz.

The AMC0x03M2510 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

Figure 7-4. OOK-Based Modulation Scheme

Product Folder Links: *AMC0203M2510 AMC0303M2510*

7.3.4 Digital Output

An input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time. An input of 250mV ($V_{INP} - V_{INN}$) produces a stream of ones and zeros. This stream is high 90.0% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982. An input of –250mV produces a stream of ones and ze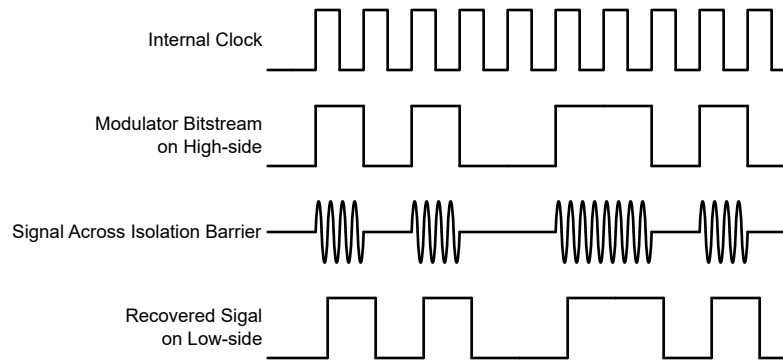ros that are high 10.0% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 6554. These input voltages are also the specified linear range of the AMC0x03M2510. If the input voltage value exceeds this range, the output of the modulator shows increasing nonlinear behavior as the quantization noise increases. The modulator output clips with a constant stream of zeros at an input ≤–320mV. The modulator output also clips with a constant stream of ones at an input ≥320mV. In this case, however, the AMC0x03M2510 generates a single 1 or 0 every 128 clock cycles to indicate proper device function. A single 1 is generated if the input is at negative full-scale and a 0 is generated if the input is at positive full scale. See the *Output Behavior in Case of a Full-Scale Input* section for more details. Figure 7-5 shows the input voltage versus the output modulator signal.
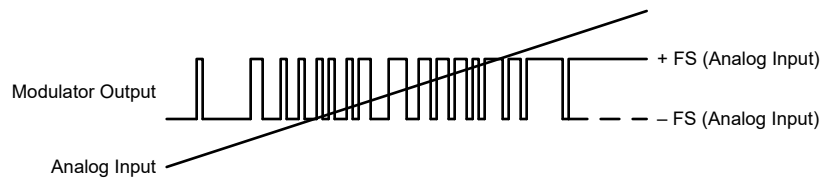
Figure 7-5. Modulator Output vs Analog Input

The following equation calculates the density of ones in the output bitstream for any input voltage V_{IN} = ($V_{INP} - V_{INN}$) value. The only exception is a full-scale input signal. See the *Output Behavior in Case of a Full-Scale Input* section.

$$\rho = (|V_{Clipping}| + V_{IN}) / (2 \times V_{Clipping}) \tag{1}$$

7.3.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC0x03M2510, the device generates a single one or zero every 128 bits at DOUT. Figure 7-6 shows a timing diagram of this process. A single 1 or 0 is generated depending on the actual polarity of the signal being sensed. A full-scale signal is defined as $|V_{INP} - V_{INN}| \geq |V_{Clipping}|$. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level. See the *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB)* application note for code examples of diagnosing the digital bitstream.

Figure 7-6. Full-Scale Output of the AMC0x03M2510

7.3.4.2 Output Behavior in Case of a Missing High-Side Supply

If the high-side supply (AVDD) is missing, the device provides a constant bitstream of logic 0's at the output, and DOUT is permanently low. Figure 7-7 shows a timing diagram of this process. A one is not generated every 128 clock pulses, which differentiates this condition from a valid negative fullscale input. This feature helps identify high-side power-supply problems on the board. See the *Diagnosing Delta-Sigma Modulator Bitstream Using C2000™ Configurable Logic Block (CLB) application note* for code examples of diagnosing the digital bitstream.
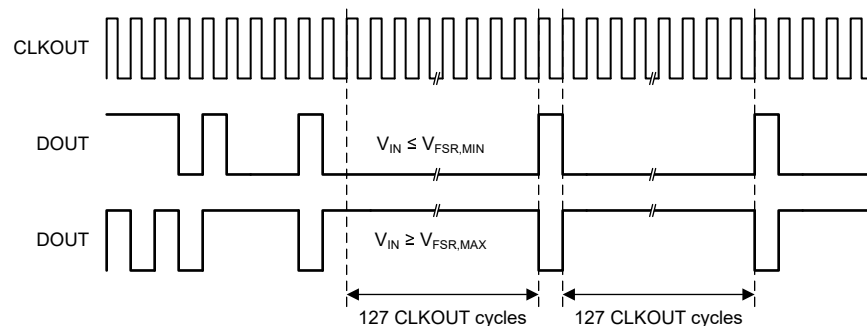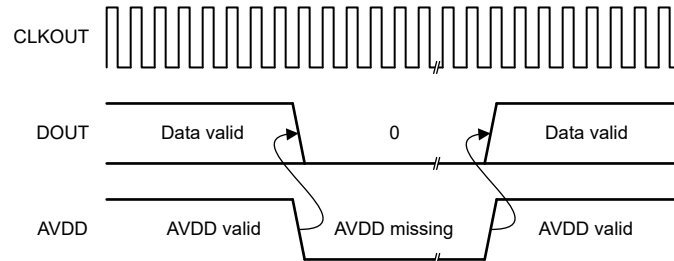
Figure 7-7. Output of the AMC0x03M2510 in Case of a Missing High-Side Supply

7.4 Device Functional Modes

The AMC0x03M2510 operates in one of the following states:

- OFF-state: The low-side of the device (DVDD) is below the DVDD$_{UV}$ threshold. The device is not responsive. DOUT is Hi-Z state. Internally, DOUT and CLKOUT are clamped to DVDD and DGND by ESD protection diodes.
- Missing high-side supply: The low-side of the device (DVDD) is supplied and within the limits listed in the *Recommended Operating Conditions* . The high-side supply (AVDD) is below the AVDD$_{UV}$ threshold. The device outputs a constant bitstream of logic 0's, as described in the *Output Behavior in Case of a Missing High-Side Supply* section.
- Analog input overrange (positive full-scale input): AVDD and DVDD are within the recommended operating conditions. However, the analog input voltage V_{IN} = (V_{INP} – V_{INN}) is above the maximum clipping voltage ($V_{Clipping, MAX}$). The device outputs a logic 0 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
- Analog input underrange (negative full-scale input): AVDD and DVDD are within the recommended operating conditions. However, the analog input voltage V_{IN} = (V_{INP} – V_{INN}) is below the minimum clipping voltage ($V_{Clipping, MIN}$). The device outputs a logic 1 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
- Normal operation: AVDD, DVDD, and V_{IN} are within the recommended operating conditions. The device outputs a digital bitstream, as explained in the *Digital Output* section.

Table 7-1 lists the operational modes.

Table 7-1. Device Operational Modes

OPERATINAL MODE	AVDD	DVDD	V_{IN}	DEVICE RESPONSE
OFF	Don't care	V_{DVDD} < DVDD$_{UV}$	Don't care	DOUT is Hi-Z state. Internally, DOUT and CLKOUT are clamped to DVDD and DGND by ESD protection diodes.
Missing high-side supply	V_{AVDD} < AVDD$_{UV}$	Valid[1]	Don't care	The device outputs a constant bitstream of logic 0's, as described in the *Output Behavior in Case of a Missing High-Side Supply* section.
Input overrange	Valid[1]	Valid[1]	V_{IN} > $V_{Clipping, MAX}$	The device outputs a logic 0 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
Input underrange	Valid[1]	Valid[1]	V_{IN} < $V_{Clipping, MIN}$	The device outputs a logic 1 every 128 clock cycles, as described in the *Output Behavior in Case of a Full-Scale Input* section.
Normal operation	Valid[1]	Valid[1]	Valid[1]	Normal operation

(1) *Valid* denotes the value is within the recommended operating conditions.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The AMC0x03M2510 has low analog input voltage range, high accuracy, low temperature drift, and high common-mode transient immunity. The AMC0x03M2510 is primarily designed for shunt-based, current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC0x03M2510 is preferred for isolated current sensing in motor drives, frequency inverters, and uninterruptible power-supply applications.

8.2 Typical Application

The following image shows the AMC0x03M2510 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop. The AMC0x03M2510 high-side circuitry senses the voltage drop across the shunt resistor, then digitizes and transfers data across the isolation barrier to the low side. Low-side circuitry outputs the digital bitstream on the DOUT pin that is synchronized to the clock signal that is output on the CLKOUT pin. The digital bitstream is processed by a low-pass digital filter in a microcontroller (MCU) or FPGA.

The differential input, digital output, and high common-mode transient immunity (CMTI) of the AMC0x03M2510 provide reliable and accurate operation even in high-noise environments.
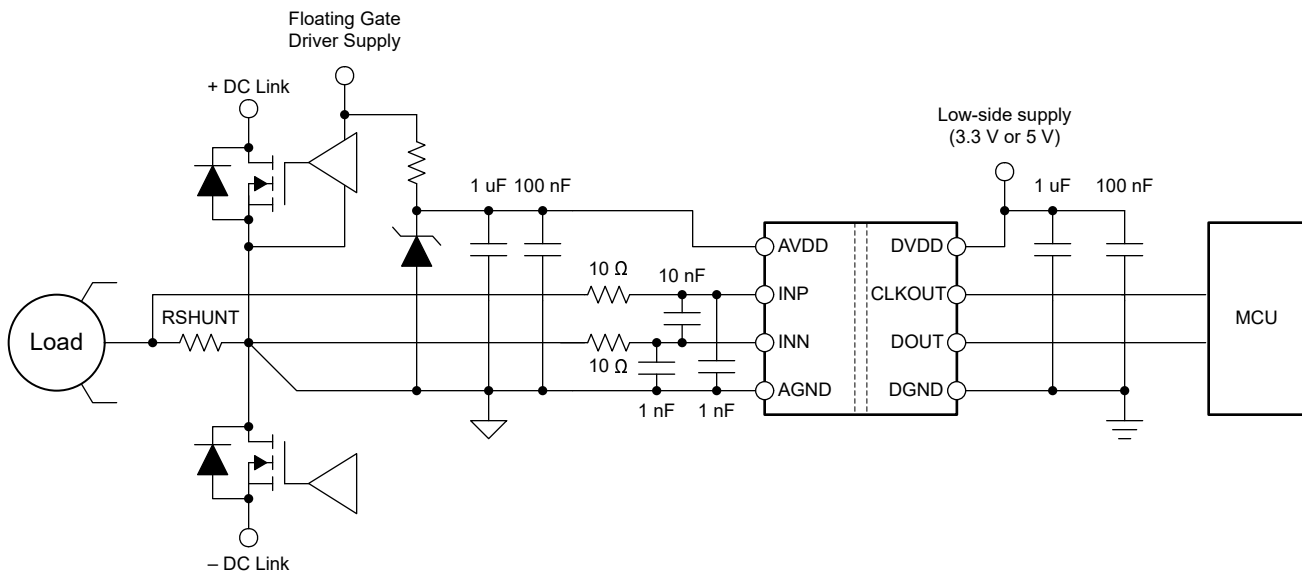

Figure 8-1. Using the AMC0x03M2510 for Current Sensing in a Typical Application

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage drop across RSHUNT for a linear response	±250mV(maximum)

8.2.2 Detailed Design Procedure

In the *Typical Application* figure, the high-side power supply (VDD1) for the AMC0x03M2510 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC0x03M2510 (INN). If a four-pin shunt is used, the inputs of the AMC0x03M2510 are connected to the inner leads. GND1 is then connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. Do not short GND1 to INN directly at the device input; see the *Layout Example* section for more details.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current:

$$V_{SHUNT} = I \times RSHUNT \tag{2}$$

Select a RSHUNT value to satisfy the following two conditions:

- First, the voltage drop caused by the nominal current range does not exceed the recommended differential input voltage range of $V_{SHUNT} \leq \pm 250mV$.
- Secondly, the voltage drop caused by the maximum allowed overcurrent does not exceed the input voltage that causes a clipping output. Keep $V_{SHUNT} \leq V_{Clipping}$.

Product Folder Links: *AMC0203M2510 AMC0303M2510*

8.2.2.1 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the device to improve signal-to-noise performance of the signal path. Input noise with a frequency close to the ΔΣ modulator sampling frequency (typically 10MHz) is folded back into the low-frequency range by the modulator. The purpose of the RC filter at the input is to attenuate high-frequency noise below the desired noise level of the measurement. Design the input filter such that:

- The filter capacitance (C5) is a minimum of 10nF
- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (f_{CLK}) of the ΔΣ modulator
- The dynamic input bias current does not generate a significant voltage drop across the DC impedances (R1, R2) relative to the common-mode input voltage range
- The impedances measured from the analog inputs are equal (R1 equals R2)

Place capacitors C6 and C7 to improve common-mode rejection at high frequencies (>1MHz) and to improve offset voltage performance. For best performance, verify C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering.

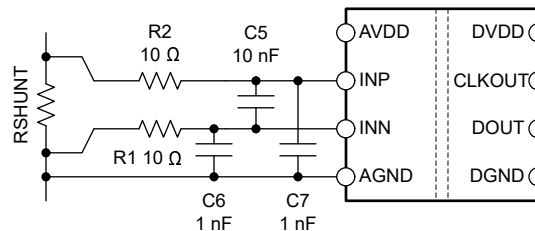For most applications, the structure shown in Figure 8-2 achieves excellent performance.

Figure 8-2. Input Filter

8.2.2.2 Bitstream Filtering

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word, that is proportional to the input voltage. Equation 3 represents a sinc³-type filter, which is a very simple filter built with minimal effort and hardware.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3$$

(3)

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All characterization in this document is also done with a sinc³ filter. This filter has an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

The *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications application note* provides an example code. This example code implements a sinc³ filter in an FPGA. This application note is available for download at www.ti.com.

For modulator output bitstream filtering, a device from TI's C2000 or Sitara microcontroller families is recommended. These families support multichannel dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel. One path provides high-accuracy results for the control loop and the other provides a fast-response path for overcurrent detection.

A *delta sigma modulator filter calculator* is available for download at www.ti.com. This calculator aids in filter design and selecting the right OSR and filter order to achieve the desired output resolution and filter response time.

8.2.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. The following figure shows the ENOB of the AMC0x03M2510 with different oversampling ratios.
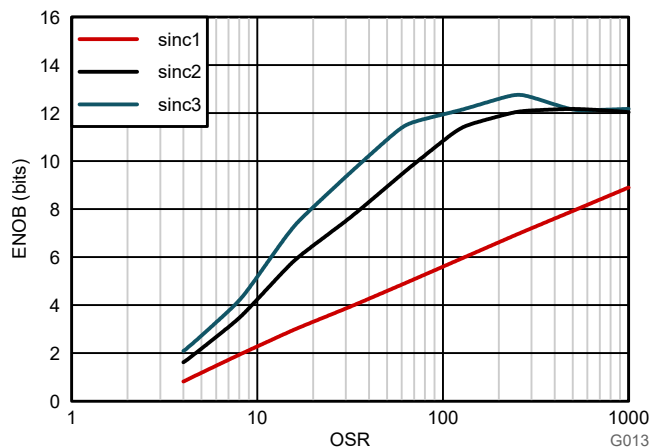
Figure 8-3. Measured Effective Number of Bits vs Oversampling Ratio

8.3 Best Design Practices

Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not short GND1 to INN directly at the device input. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. See the *Layout Example* section for more details.

Do not leave the inputs of the AMC0x03M2510 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current potentially drives the inputs to a positive value that exceeds the operating common-mode input voltage. This condition causes the device to output the fail-safe voltage described in the section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the *Recommended Operating Conditions* table.

8.4 Power Supply Recommendations

In a typical application, the high-side power supply (AVDD) for the AMC0x03M2510 is generated from the low-side supply (DVDD) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC0x03M2510 does not require any specific power-up sequencing. The high-side power supply (AVDD) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (DVDD) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 8-4 shows a decoupling diagram for the AMC0x03M2510.
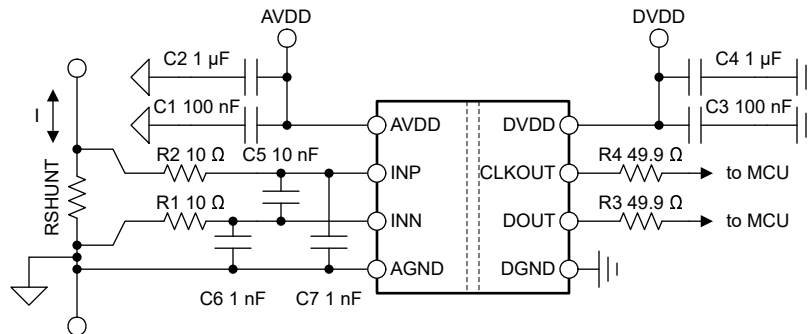
Figure 8-4. Decoupling of the AMC0x03M2510

Verify capacitors provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

8.5 Layout

8.5.1 Layout Guidelines

The *Layout Example* section provides a layout recommendation detailing the critical placement of the decoupling and filter capacitors. Place decoupling and filter capacitors as close as possible to the AMC0x03M2510 input pins.

8.5.2 Layout Example

Figure 8-5. Recommended Layout of the AMC0x03M2510

Product Folder Links: *AMC0203M2510 AMC0303M2510*

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:
- Texas Instruments, *Isolation Glossary* application note
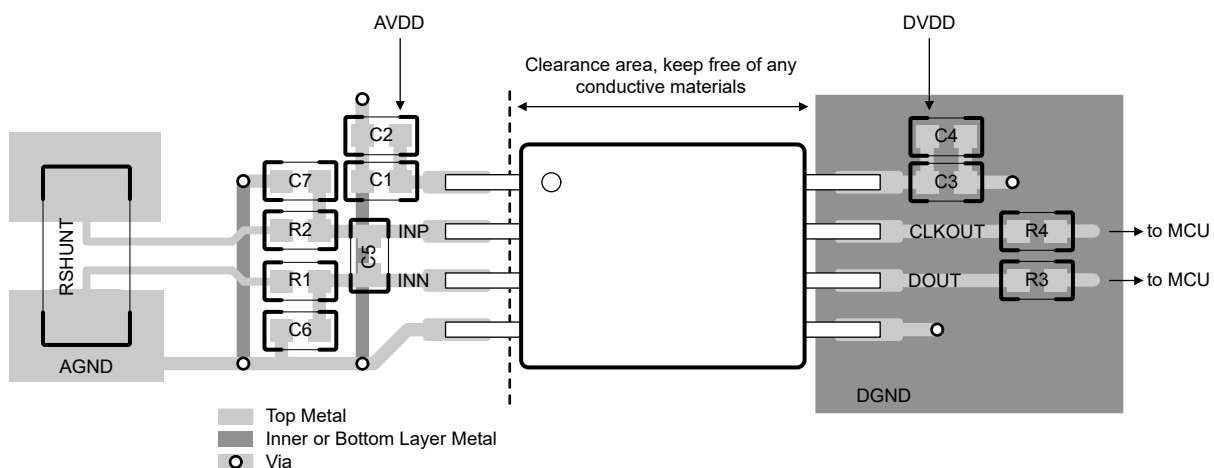- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *AMC1306 to AMC0306 Migration Guide* application brief
- Texas Instruments, *Clock Edge Delay Compensation With Isolated Modulators Digital Interface to MCUs* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity*
- Texas Instruments, *Combining the ADS1202 With an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note
- Texas Instruments, *Delta Sigma Modulator Filter Calculator* design tool

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *AMC0203M2510 AMC0303M2510*

11.1 Mechanical Data

PACKAGE OUTLINE

DWV0008A

SOIC - 2.8 mm max height
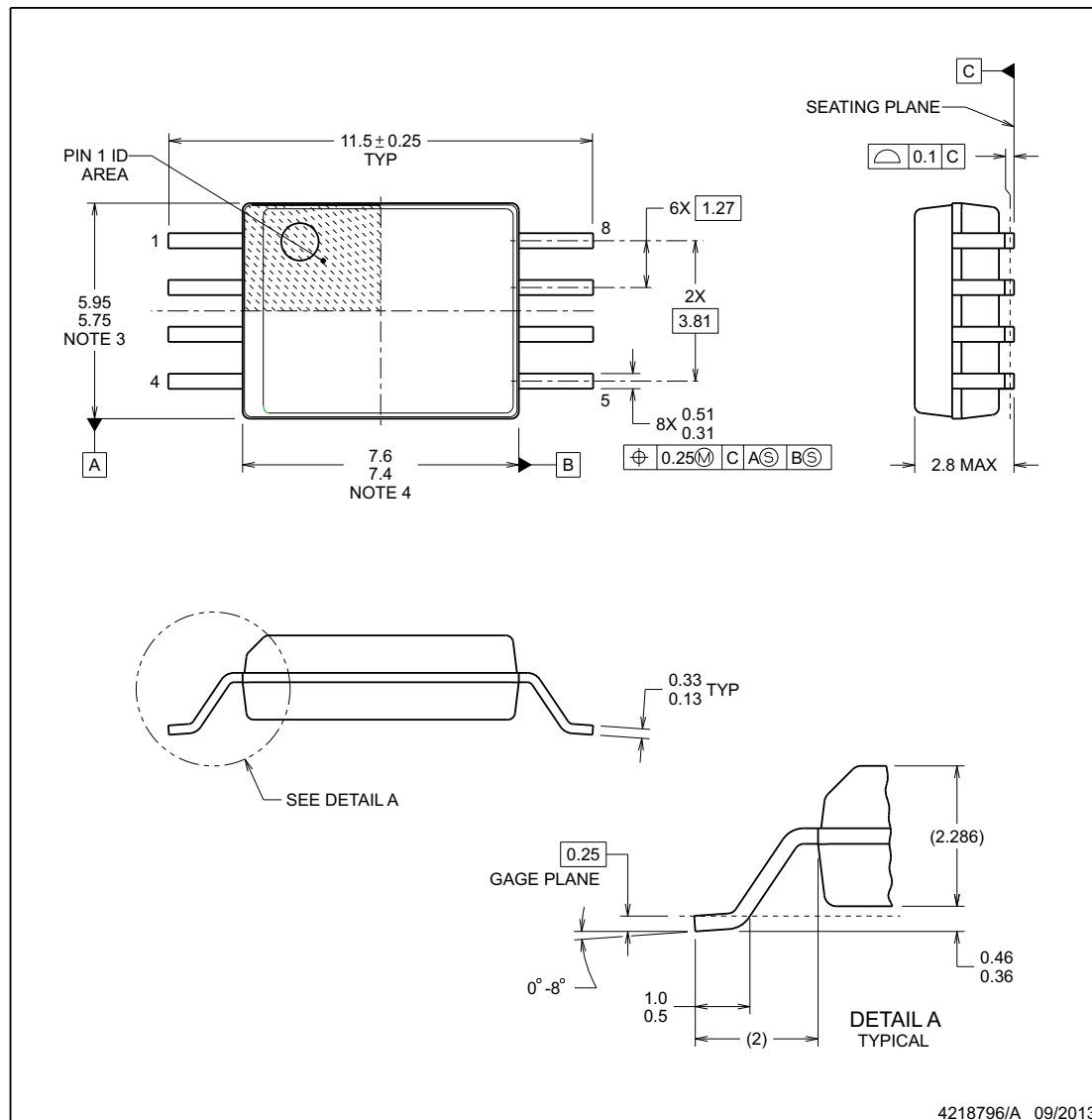
SOIC

4218796/A   09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

DWV0008A

SOIC - 2.8 mm max height
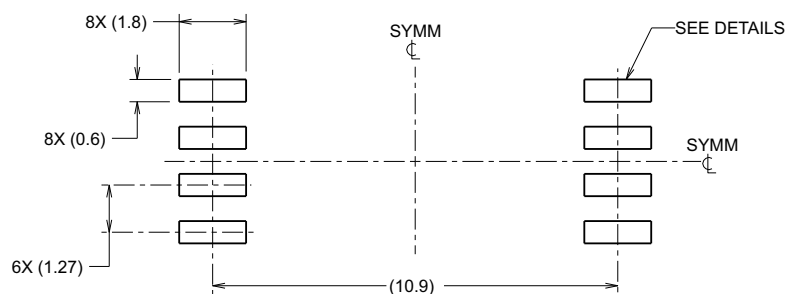
SOIC

8X (1.8)

SYMM

SEE DETAILS

8X (0.6)

SYMM

6X (1.27)

(10.9)

LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218796/A   09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Product Folder Links: *AMC0203M2510 AMC0303M2510*
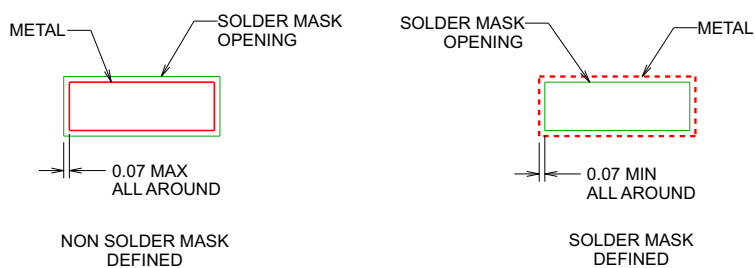
EXAMPLE STENCIL DESIGN

DWV0008A

SOIC - 2.8 mm max height
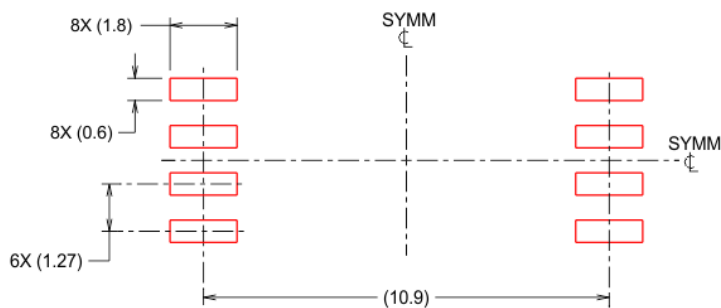
SOIC

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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INSTRUMENTS
www.ti.com

Product Folder Links: AMC0203M2510 AMC0303M2510

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

.228-.244   TYP
[5.80-6.19]

PIN 1 ID AREA

6X .050
[1.27]

2X
.150
[3.81]

.189-.197
[4.81-5.00]
NOTE 3

.150-.157
[3.81-3.98]
NOTE 4

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25]Ⓜ C A B

SEATING PLANE

.004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019
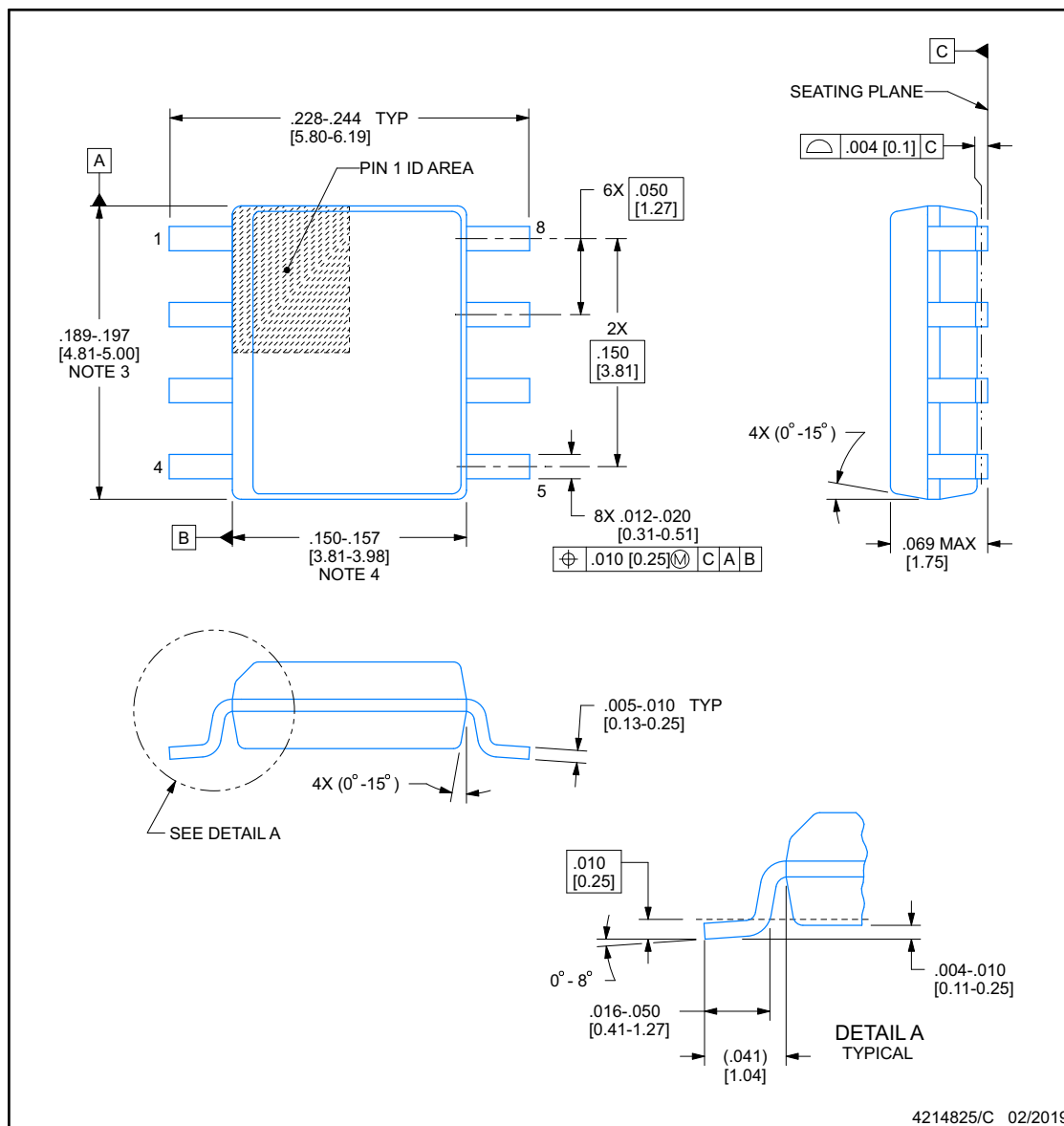
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
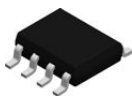5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

8X (.061) [1.55]

SYMM

SEE DETAILS

8X (.024) [0.6]

SYMM

(R.002) TYP [0.05]

6X (.050) [1.27]

(.213) [5.4]
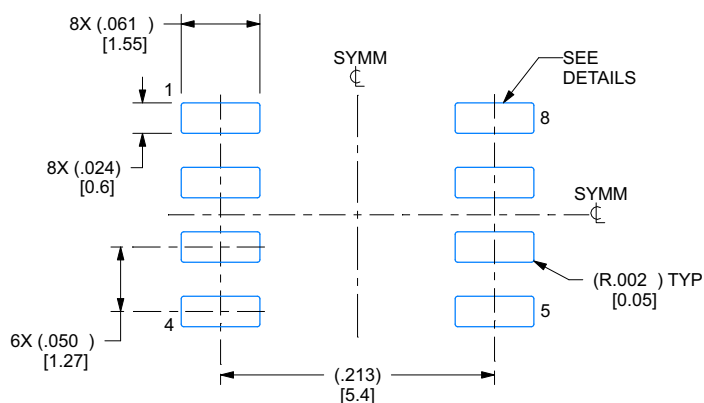
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL UNDER SOLDER MASK

EXPOSED METAL

EXPOSED METAL

.0028 MAX [0.07] ALL AROUND

.0028 MIN [0.07] ALL AROUND

NON SOLDER MASK DEFINED

SOLDER MASK DEFINED
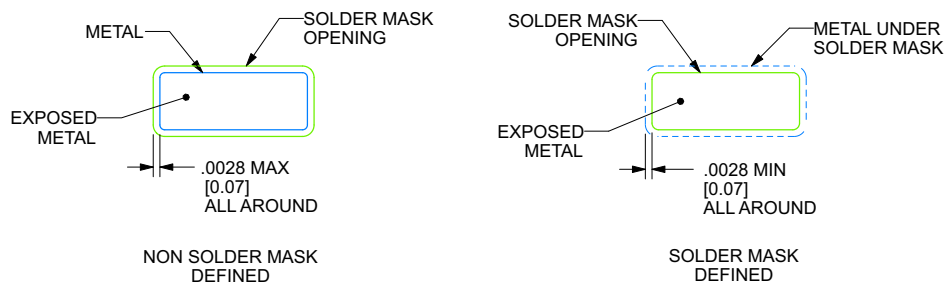
SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Product Folder Links: *AMC0203M2510 AMC0303M2510*

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

8X (.061)
[1.55]

1

8X (.024)
[0.6]

SYMM

8

SYMM

(R.002) TYP
[0.05]

6X (.050)
[1.27]

4

5

(.213)
[5.4]
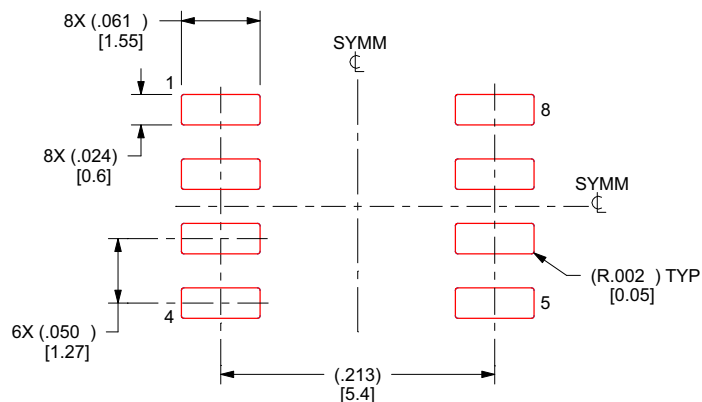
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

TEXAS INSTRUMENTS

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Submit Document Feedback

Product Folder Links: *AMC0203M2510 AMC0303M2510*

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC0303M2510DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	303M2510

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

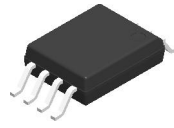| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC0303M2510DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

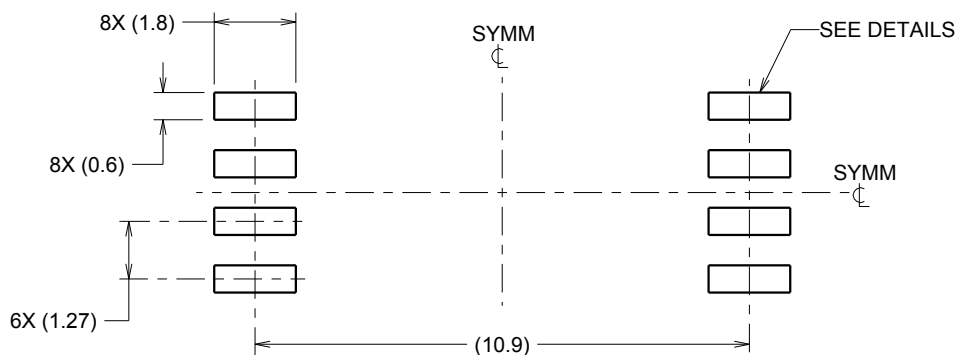| Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC0303M2510DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0

DWV0008A

SOIC - 2.8 mm max height

SOIC
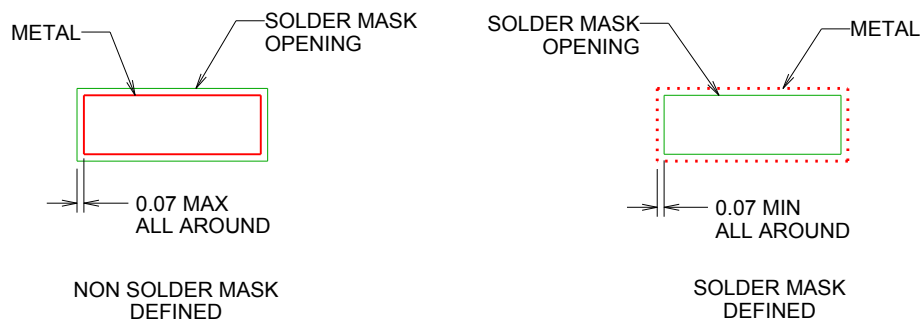

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

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8X (1.8)

SYMM

SEE DETAILS

8X (0.6)

SYMM

6X (1.27)

(10.9)

LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

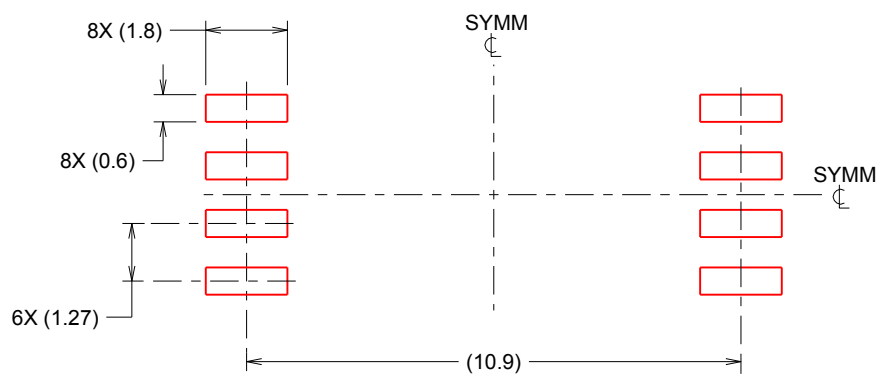NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218796/A   09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (1.8)

SYMM

8X (0.6)

SYMM

6X (1.27)

(10.9)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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