AMC23C15-Q1 Automotive, Dual, Fast Response, Reinforced Isolated Window Comparator With Adjustable Threshold

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Wide high-side supply range: 3V to 27V
- Low-side supply range: 2.7V to 5.5V
- Dual window comparator:
  - Window comparator 1: ±5mV to ±300mV adjustable threshold
  - Window comparator 2: ±60mV fixed threshold
- Supports positive-comparator mode:
  - Cmp0: 600mV to 2.7V adjustable threshold
  - Cmp2: 60mV fixed threshold
  - Cmp1 and Cmp3: Disabled
- Reference current for threshold adjustment: 100µA, ±1%
- Trip threshold error: ±1% (max) at 250mV
- Open-drain outputs
- Propagation delay: 280ns (typ)
- High CMTI: 15V/ns (min)
- Safety-related certifications:
  - 7000V_{PK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000V_{RMS} isolation for 1 minute per UL1577

2 Applications

- Overcurrent or overvoltage detection in:
  - Solid-state relays (SSR)
  - Motor drives
  - Frequency inverters
  - Solar inverters
  - DC/DC converters

3 Description

The AMC23C15-Q1 is a dual, isolated window comparator with a short response time. The open-drain outputs are separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5kV_{RMS} according to VDE 0884-17 and UL1577, and supports a working voltage of up to 1kV_{RMS}.

Both comparators have windows that are centered around 0V, meaning that the comparators trip if the input exceeds the thresholds in a positive or negative direction. One comparator has fixed thresholds of ±60mV. The second comparator has adjustable thresholds from ±5mV to ±300mV through a single external resistor.

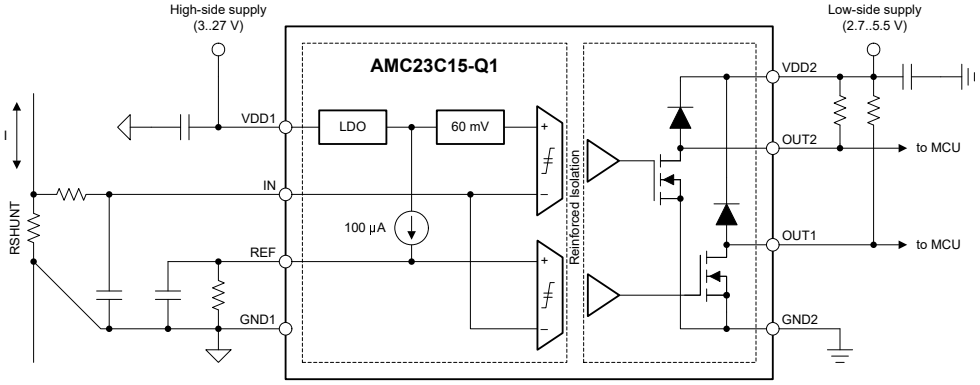
The AMC23C15-Q1 also supports a positive-comparator only mode. When the voltage on the REF pin is greater than 550mV, the negative comparators are disabled and only the positive comparators are functional. The reference voltage in this mode can be as high as 2.7V. This mode is particularly useful for monitoring positive voltage supplies.

The AMC23C15-Q1 is offered in a wide-body 8-pin SOIC package, is AEC-Q100 qualified for automotive applications, and supports the temperature range from –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC23C15-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

Table of Contents

4 Pin Configuration and Functions

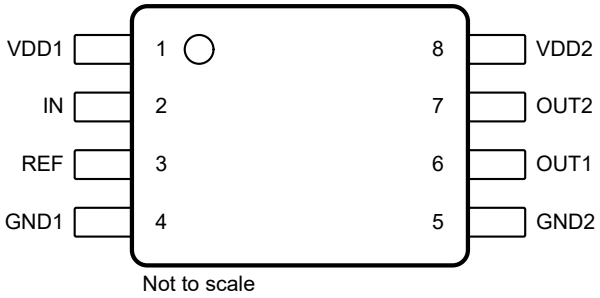


Figure 4-1. DWV Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply.(1)
2	IN	Analog input	Common analog input pin for window comparator 1 and 2.
3	REF	Analog input	Reference pin that defines the trip threshold for window comparator 1. The voltage on this pin also affects the hysteresis of comparator Cmp0, as explained in the *Reference Input* section. This pin is internally connected to a 100-µA current source. Connect a resistor from REF to GND1 to define the trip threshold, and a capacitor from REF to GND1 to filter the reference voltage. For best transient noise immunity, place the capacitor as closely to the pin as possible. This pin can also be driven by an external voltage source.
4	GND1	High-side ground	High-side ground.
5	GND2	Low-side ground	Low-side ground.
6	OUT1	Digital output	Open-drain output of window comparator 1. Connect to an external pullup resistor or leave unconnected (floating) when not used.
7	OUT2	Digital output	Open-drain output of window comparator 2. Connect to an external pullup resistor or leave unconnected (floating) when not used.
8	VDD2	Low-side power	Low-side power supply.(1)

(1) See the *Layout* section for power-supply decoupling recommendations.

5 Specifications

5.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	–0.3	30	V
	VDD2 to GND2	–0.3	6.5	
Analog input voltage	REF to GND1	–0.5	6.5	V
	IN to GND1	–6	5.5	
Digital output voltage	OUT1, OUT2 to GND2	–0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification Level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V_{VDD1}	High-side power-supply voltage	VDD1 to GND1	3.0	5	25	V
V_{VDD2}	Low-side power supply voltage	VDD2 to GND2	2.7	3.3	5.5	V
ANALOG INPUT						
V_{IN}	Input voltage	IN to GND1, VDD1 ≤ 4.3 V	–0.4		VDD1 – 0.3	V
		IN to GND1, VDD1 > 4.3 V	–0.4		4	
V_{REF}	Reference voltage, window comparator mode	REF to GND1	20(2)		300	mV
	Reference voltage, positive-comparator mode	Low hysteresis mode	20(2)		450	
		High hysteresis mode (Cmp0 only)	600		2700(1)	
	Reference voltage headroom	VDD1 – V_{REF}	1.4			V
	Filter capacitance on REF pin		20	100		nF
DIGITAL OUTPUTS						
	Digital output voltage	OUT1, OUT2 to GND2	GND2		VDD2	V
	Sink current	OUT1, OUT2	0		4	mA
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40	25	125	°C

(1) Reference voltages (V_{REF}) >1.6V require $V_{VDD1} > V_{VDD1,MIN}$ to maintain minimum headroom ($V_{VDD1} – V_{REF}$) of 1.4V.
(2) The device has been tested with V_{REF} as low as 5mV. The device remains functional but relative switching threshold accuracy can decrease because of offset errors.

5.4 Thermal Information

THERMAL METRIC(1)		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = 25 V, VDD2 = 5.5 V	110	mW
		VDD1 = VDD2 = 5.5 V	34	
		VDD1 = VDD2 = 3.6 V	22	
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 25 V	98	mW
		VDD1 = 5.5 V	21	
		VDD1 = 3.6 V	14	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5 V	12	mW
		VDD2 = 3.6 V	8	

5.6 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-III	
		Rated mains voltage ≤ 1000V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1410	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1000	V_{RMS}
		At DC voltage	1410	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production test)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)}$ = V_{IOTM}, t_{ini} = 60s, $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)}$ = 1.2 x V_{IOTM}, t_{ini} = 1s, $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)}$ = $V_{pd(m)}$ = 1.2 × V_{IOTM}, t_{ini} = t_m = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1MHz	≅ 1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification test), V_{TEST} = 1.2 × V_{ISO}, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

5.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDD1 = VDD2 = 5.5 V, T_J = 150°C, T_A = 25°C			220	mA
		$R_{\theta JA}$ = 102.8°C/W, VDD1 = VDD2 = 3.6 V, T_J = 150°C, T_A = 25°C			340	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1220	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

5.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to 125°C, VDD1 = 3.0 V to 25 V, VDD2 = 2.7 V to 5.5 V, V_{REF} = 20 mV to 2.7 V[1], and V_{IN} = –400 mV to 4 V[3] ; typical specifications are at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, and V_{REF} = 250 mV (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
R_{IN}	Input resistance	IN pin, 0 ≤ V_{IN} ≤ 4 V		1		GΩ
I_{BIAS}	Input bias current	IN pin, 0 ≤ V_{IN} ≤ 4 V[4]		0.1	25	nA
		IN pin, –400 mV ≤ V_{IN} ≤ 0 V[5]	–310	–0.5		
C_{IN}	Input capacitance	IN pin		4		pF
REFERENCE PIN						
I_{REF}	Reference current	REF to GND1, 20 mV < V_{REF} ≤ 2.7 V	99	100	101	µA
V_{MSEL}	Mode selection threshold [2]	V_{REF} rising	500	550	600	mV
		V_{REF} falling	450	500	550	
	Mode selection threshold hysteresis			50		mV
60-mV FIXED-THRESHOLD COMPARATORS (CMP2 and CMP3)						
V_{IT+}	Positive-going trip threshold	Cmp2		64		mV
E_{IT+}	Positive-going trip threshold error	Cmp2	–3.5		3.5	mV
$V_{IT–}$	Negative-going trip threshold	Cmp2		60		mV
$E_{IT–}$	Negative-going trip threshold error	Cmp2	–3.5		3.5	mV
$V_{IT–}$	Negative-going trip threshold	Cmp3		–64		mV
$E_{IT–}$	Negative-going trip threshold error	Cmp3	–4.5		4.5	mV
V_{IT+}	Positive-going trip threshold	Cmp3		–60		mV
E_{IT+}	Positive-going trip threshold error	Cmp3	–4.5		4.5	mV
V_{HYS}	Trip threshold hysteresis	Cmp2 and Cmp3; (V_{IT+} – $V_{IT–}$)		4		mV
VARIABLE-THRESHOLD COMPARATORS (CMP0 AND CMP1)						
V_{IT+}	Positive-going trip threshold	Cmp0		V_{REF} + V_{HYS}		mV
E_{IT+}	Positive-going trip threshold error	Cmp0, (V_{IT+} – V_{REF} – V_{HYS}), V_{REF} = 20 mV, V_{HYS} = 4 mV	–2		2	mV
		Cmp0, (V_{IT+} – V_{REF} – V_{HYS}), V_{REF} = 250 mV, V_{HYS} = 4 mV	–2		2	
		Cmp0, (V_{IT+} – V_{REF} – V_{HYS}), V_{REF} = 2 V, V_{HYS} = 25 mV	–5		5	
$V_{IT–}$	Negative-going trip threshold	Cmp0		V_{REF}		mV
$E_{IT–}$	Negative-going trip threshold error	Cmp0, ($V_{IT–}$ – V_{REF}), V_{REF} = 20 mV	–2.5		2.5	mV
		Cmp0, ($V_{IT–}$ – V_{REF}), V_{REF} = 250 mV	–2.5		2.5	
		Cmp0, ($V_{IT–}$ – V_{REF}), V_{REF} = 2 V	–5		5	
$V_{IT–}$	Negative-going trip threshold	Cmp1		–V_{REF} – V_{HYS}		mV
$E_{IT–}$	Negative-going trip threshold error	Cmp1, ($V_{IT–}$ + V_{REF} + V_{HYS}), V_{REF} = 20 mV, V_{HYS} = 4 mV	–3		3	mV
		Cmp1, ($V_{IT–}$ + V_{REF} + V_{HYS}), V_{REF} = 250 mV, V_{HYS} = 4 mV	–3		3	
V_{IT+}	Positive-going trip threshold	Cmp1		–V_{REF}		mV
E_{IT+}	Positive-going trip threshold error	Cmp1, (V_{IT+} + V_{REF}), V_{REF} = 20 mV	–3.5		3.5	mV
		Cmp1, (V_{IT+} + V_{REF}), V_{REF} = 250 mV	–3.5		3.5	
V_{HYS}	Trip threshold hysteresis	Cmp0 and Cmp1, (V_{IT+} – $V_{IT–}$), V_{REF} ≤ 450 mV		4		mV
		Cmp0 only, (V_{IT+} – $V_{IT–}$), V_{REF} ≥ 600 mV		25		
DIGITAL OUTPUTS						
V_{OL}	Low-level output voltage	I_{SINK} = 4 mA		80	250	mV
I_{LKG}	Open-drain output leakage current	VDD2 = 5 V, V_{OUT} = 5 V		5	100	nA
CMTI	Common-mode transient immunity	|V_{IN} – V_{REF}| ≥ 4 mV, R_{PULLUP} = 10 kΩ	15	40		V/ns

5.9 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to 125°C, VDD1 = 3.0 V to 25 V, VDD2 = 2.7 V to 5.5 V, V_{REF} = 20 mV to 2.7 V(1), and V_{IN} = –400 mV to 4 V(3) ; typical specifications are at T_A = 25°C, VDD1 = 5 V, VDD2 = 3.3 V, and V_{REF} = 250 mV (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold	VDD1 rising			3	V
		VDD1 falling			2.9	
$VDD1_{POR}$	VDD1 power-on reset threshold	VDD1 falling			2.3	V
$VDD2_{UV}$	VDD2 undervoltage detection threshold	VDD2 rising			2.7	V
		VDD2 falling			2.1	
I_{DD1}	High-side supply current	3.0 V ≤ VDD1 ≤ 3.4 V			4.0	mA
		3.4 V < VDD1 ≤ 25 V		3.2	4.3	
I_{DD2}	Low-side supply current			1.8	2.2	mA

(1) Reference voltages >1.6 V require VDD1 > $VDD1_{MIN}$. See the *Recommended Opertion Conditions* table for details.
(2) The voltage level V_{REF} determines if the device operates as window-comparator with positive and negative thresholds or as simple comparator with positive thresholds only. See the *Reference Input* section for more details.
(3) But not exceeding the maximum input voltage specified in the *Recommended Opertion Conditions* table.
(4) The typical value is measured at V_{IN} = 0.4 V.
(5) The typical value is measured at V_{IN} = –400 mV.

5.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-DRAIN OUTPUTS						
t_{pH}	Propagation delay time, $\|V_{IN}\|$ rising (1)	VDD2 = 3.3 V, V_{REF} = 250 mV, $V_{OVERDRIVE}$ = 10 mV, C_L = 15 pF		280	410	ns
		VDD2 = 3.3 V, V_{REF} = 2 V, $V_{OVERDRIVE}$ = 50 mV, C_L = 15 pF		240	370	
t_{pL}	Propagation delay time, $\|V_{IN}\|$ falling (1)	VDD2 = 3.3 V, V_{REF} = 250 mV, $V_{OVERDRIVE}$ = 10 mV, C_L = 15 pF		280	410	ns
		VDD2 = 3.3 V, V_{REF} = 2 V, $V_{OVERDRIVE}$ = 50 mV, C_L = 15 pF		240	370	
t_f	Output signal fall time	R_{PULLUP} = 4.7 kΩ, C_L = 15 pF		2		ns
MODE SELECTION						
t_{HSEL}	Comparator hysteresis selection deglitch time	Cmp0, V_{REF} rising or falling		10		µs
t_{DIS13}	Comparator disable deglitch time	Cmp1 and Cmp3, V_{REF} rising		10		µs
t_{EN13}	Comparator enable deglitch time	Cmp1 and Cmp3, V_{REF} falling		100		µs
START-UP TIMING						
$t_{LS\ ,STA}$	Low-side start-up time	VDD2 step to 2.7 V, VDD1 ≥ 3.0 V		40		µs
$t_{HS\ ,STA}$	High-side start-up time	VDD1 step to 3.0 V, VDD2 ≥ 2.7 V		45		µs
$t_{HS,BLK}$	High-side blanking time			200		µs
$t_{HS,FLT}$	High-side-fault detection delay time			100		µs

(1) Valid for OUT1 and OUT2

5.11 Timing Diagrams

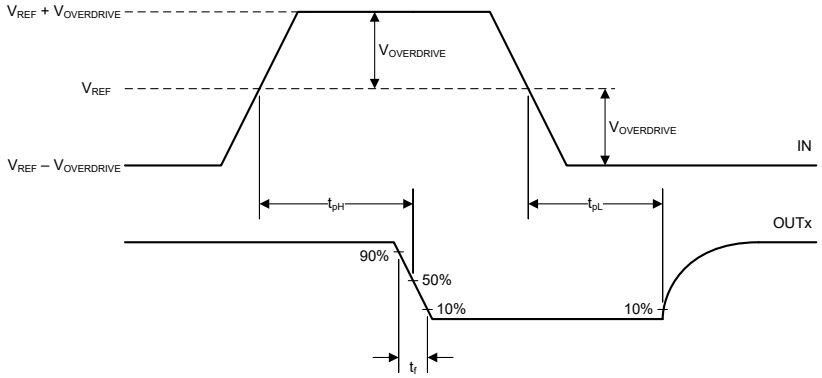


Figure 5-1. Rise, Fall, and Delay Time Definition

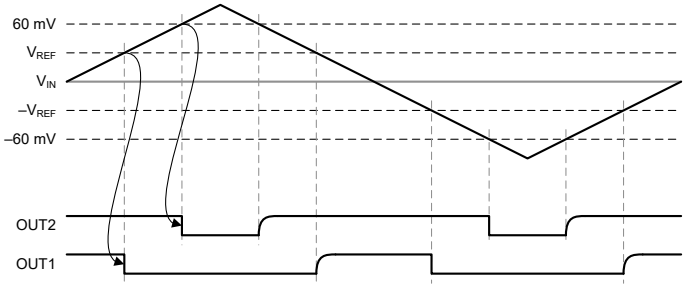


Figure 5-2. Functional Timing Diagram

5.12 Insulation Characteristics Curves

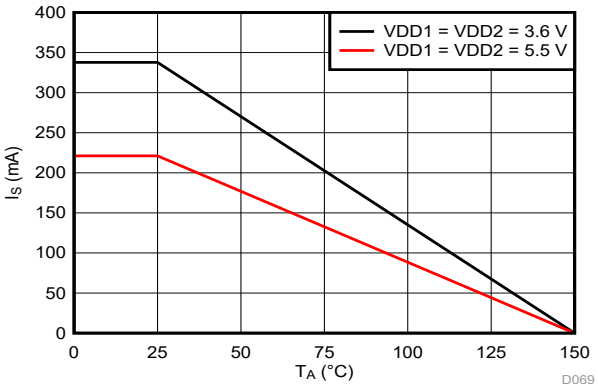


Figure 5-3. Thermal Derating Curve for Safety-Limiting Current per VDE

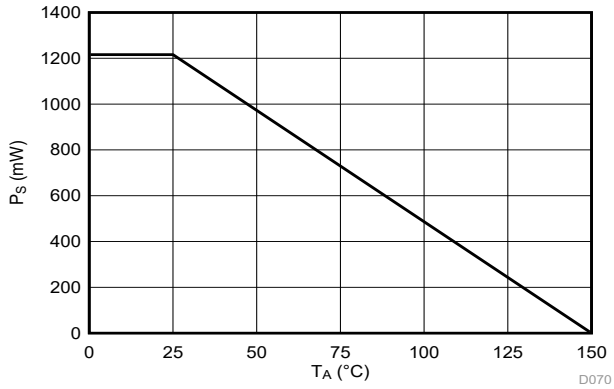
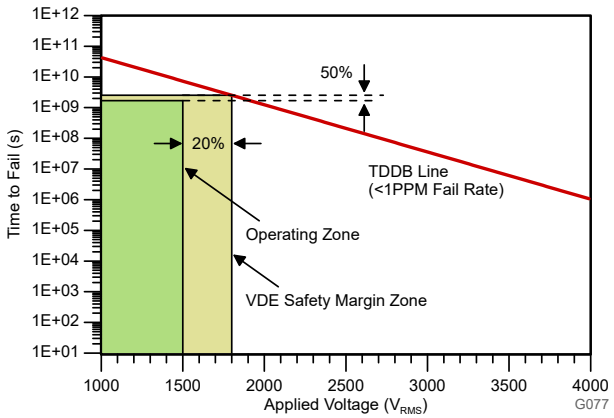


Figure 5-4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1000V_{RMS}, operating lifetime > 400 years

Figure 5-5. Reinforced Isolation Capacitor Lifetime Projection

5.13 Typical Characteristics

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

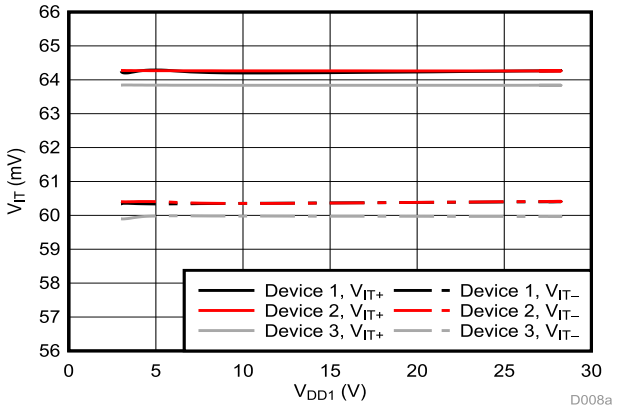


Figure 5-6. Cmp2 Trip Threshold vs Supply Voltage

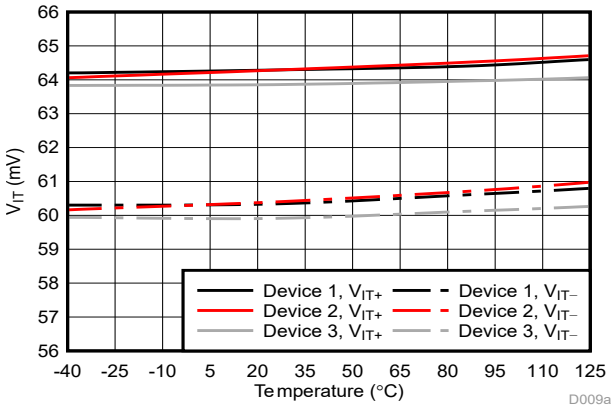


Figure 5-7. Cmp2 Trip Threshold vs Temperature

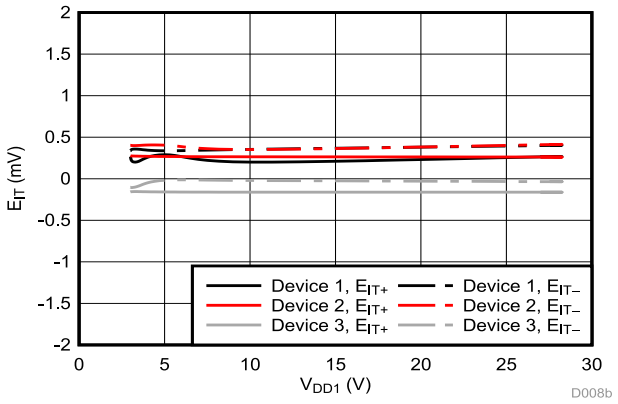


Figure 5-8. Cmp2 Trip Threshold Error vs Supply Voltage

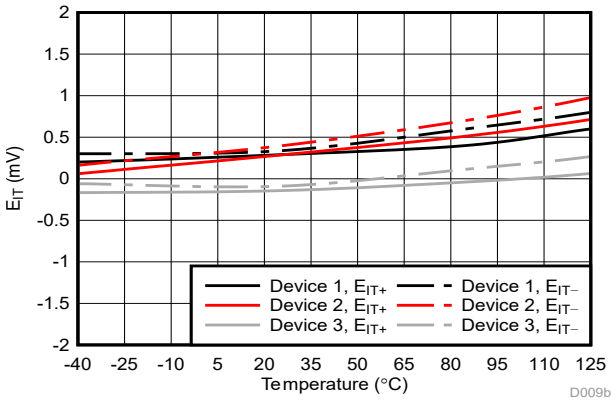


Figure 5-9. Cmp2 Trip Threshold Error vs Temperature

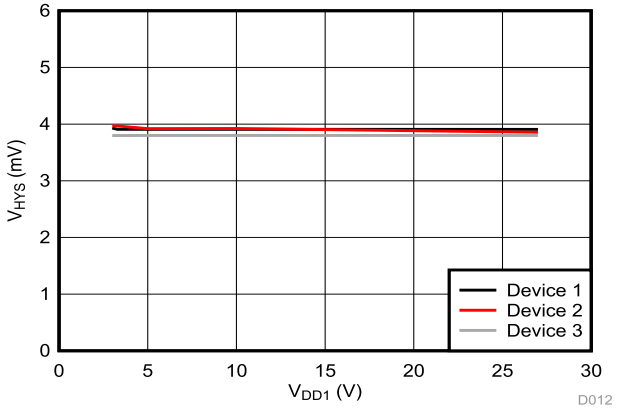


Figure 5-10. Cmp2 Trip Threshold Hysteresis vs Supply Voltage

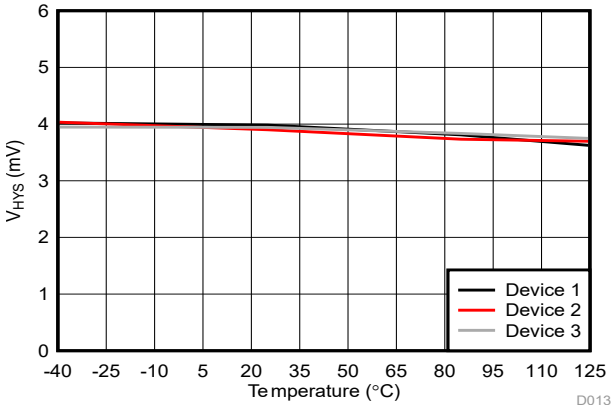


Figure 5-11. Cmp2 Trip Threshold Hysteresis vs Temperature

5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

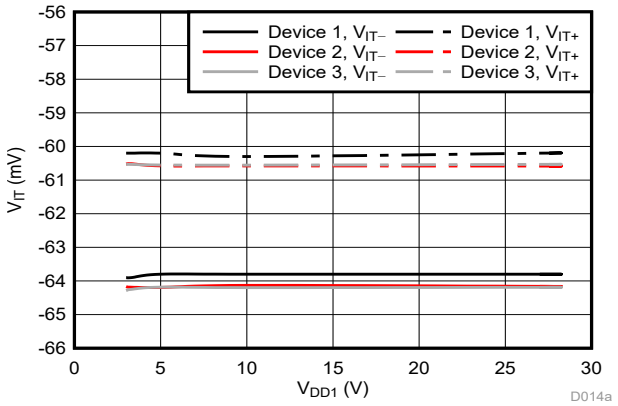


Figure 5-12. Cmp3 Trip Threshold vs Supply Voltage

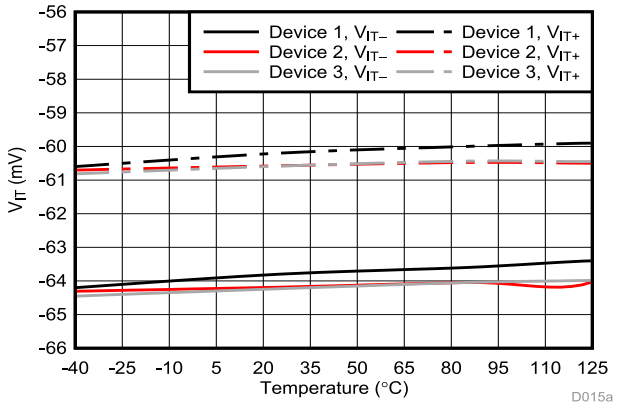


Figure 5-13. Cmp3 Trip Threshold vs Temperature

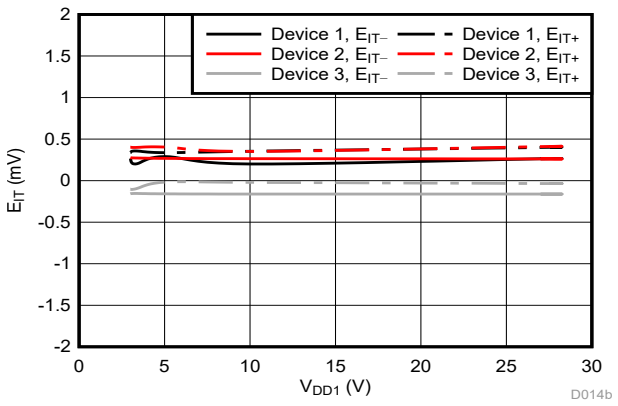


Figure 5-14. Cmp3 Trip Threshold Error vs Supply Voltage

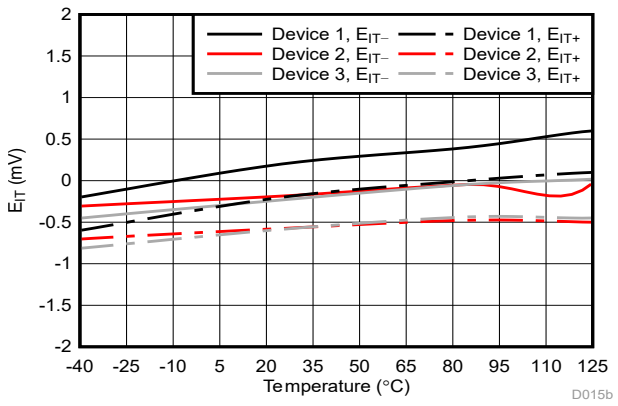


Figure 5-15. Cmp3 Trip Threshold Error vs Temperature

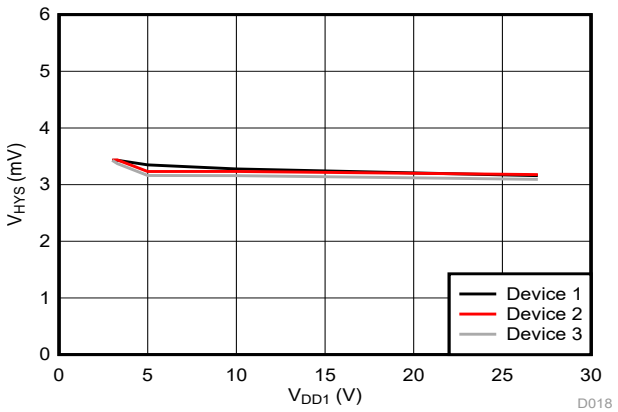


Figure 5-16. Cmp3 Trip Threshold Hysteresis vs Supply Voltage

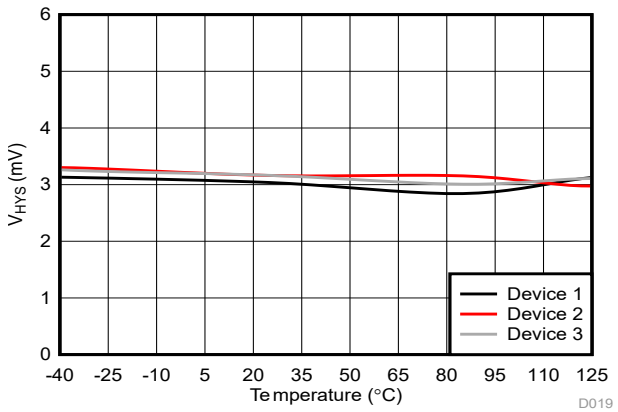
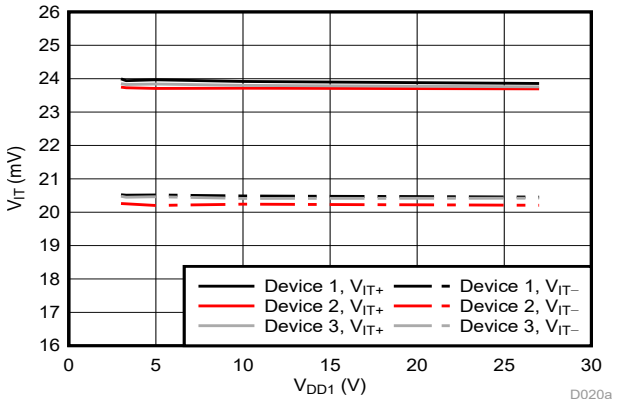


Figure 5-17. Cmp3 Trip Threshold Hysteresis vs Temperature

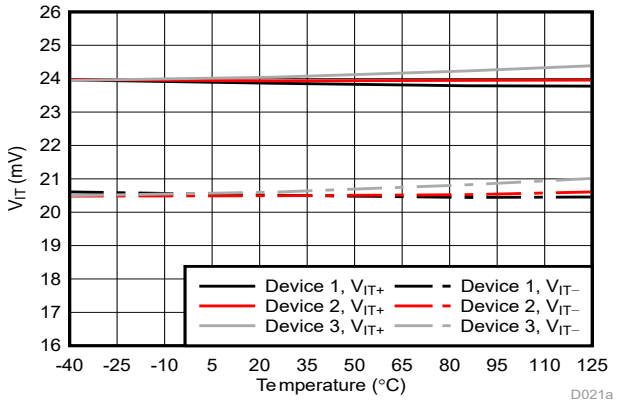
5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)



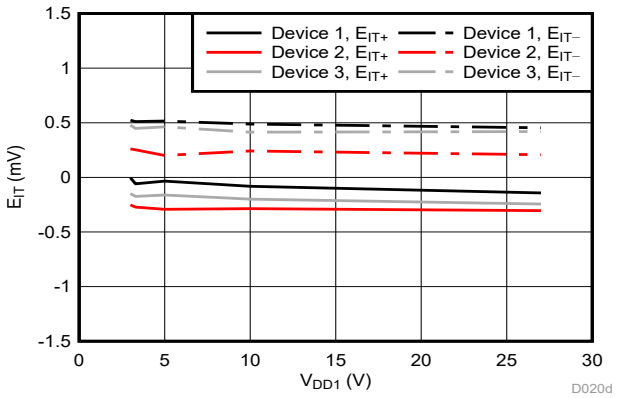
V_{REF} = 20mV

Figure 5-18. Cmp0 Trip Threshold vs Supply Voltage



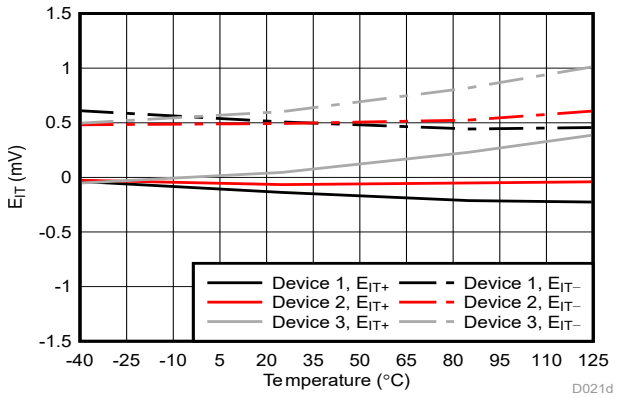
V_{REF} = 20mV

Figure 5-19. Cmp0 Trip Threshold vs Temperature



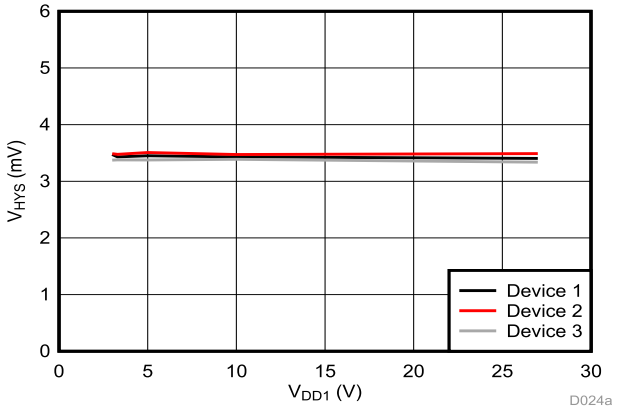
V_{REF} = 20mV

Figure 5-20. Cmp0 Trip Threshold Error vs Supply Voltage



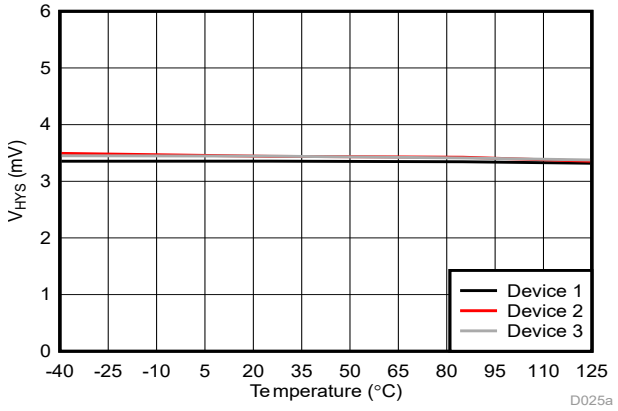
V_{REF} = 20mV

Figure 5-21. Cmp0 Trip Threshold Error vs Temperature



V_{REF} = 20mV

Figure 5-22. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

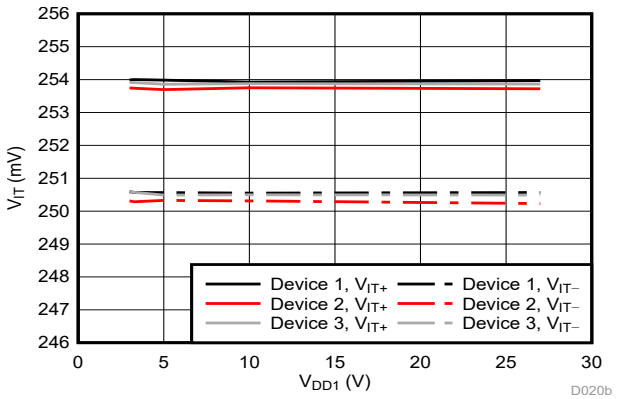


V_{REF} = 20mV

Figure 5-23. Cmp0 Trip Threshold Hysteresis vs Temperature

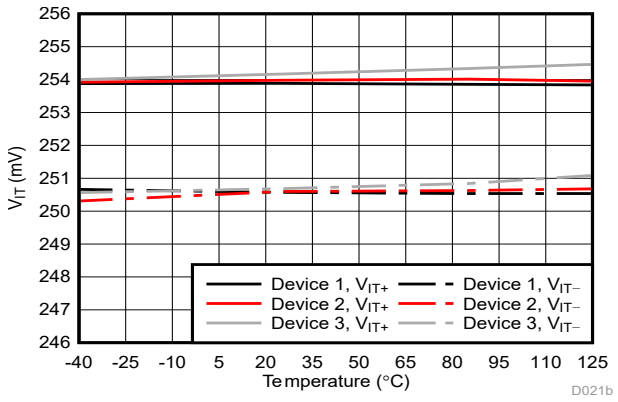
5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)



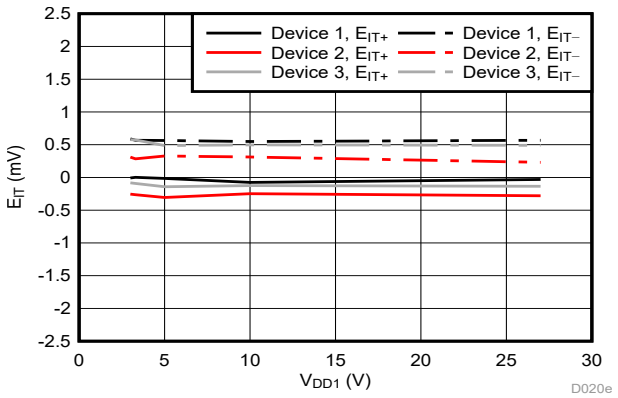
V_{REF} = 250mV

Figure 5-24. Cmp0 Trip Threshold vs Supply Voltage



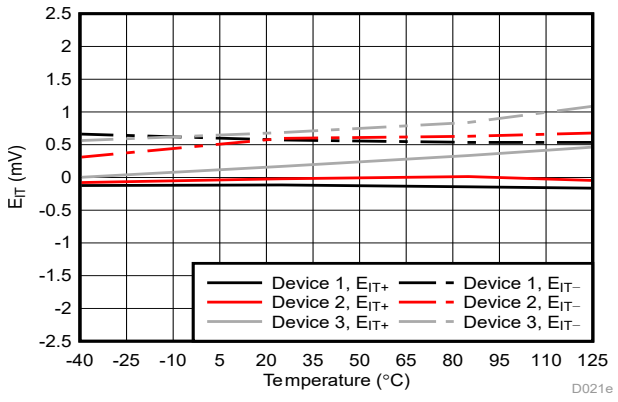
V_{REF} = 250mV

Figure 5-25. Cmp0 Trip Threshold vs Temperature



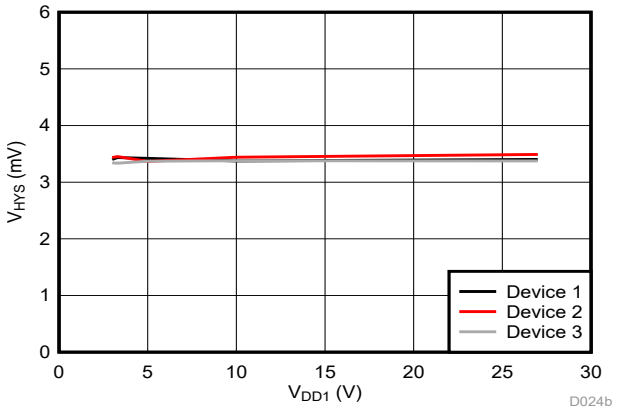
V_{REF} = 250mV

Figure 5-26. Cmp0 Trip Threshold Error vs Supply Voltage



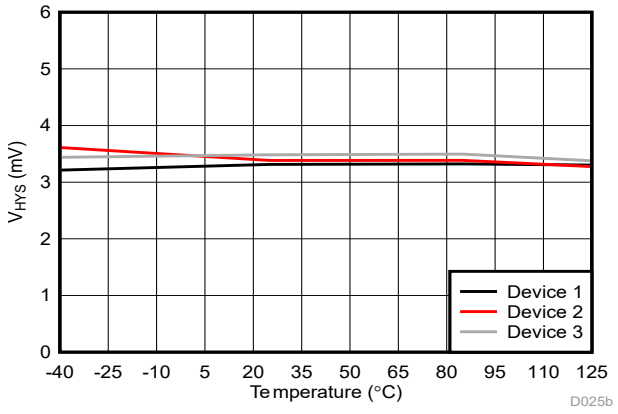
V_{REF} = 250mV

Figure 5-27. Cmp0 Trip Threshold Error vs Temperature



V_{REF} = 250mV

Figure 5-28. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

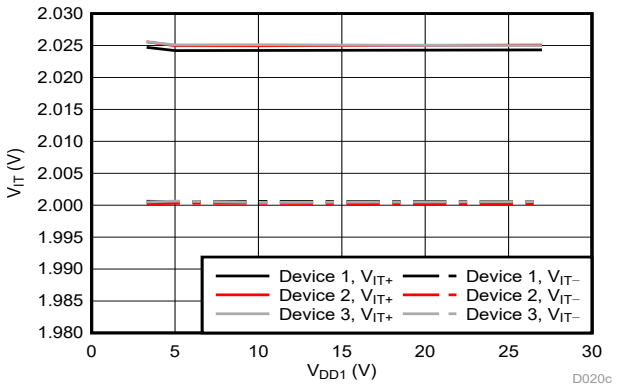


V_{REF} = 250mV

Figure 5-29. Cmp0 Trip Threshold Hysteresis vs Temperature

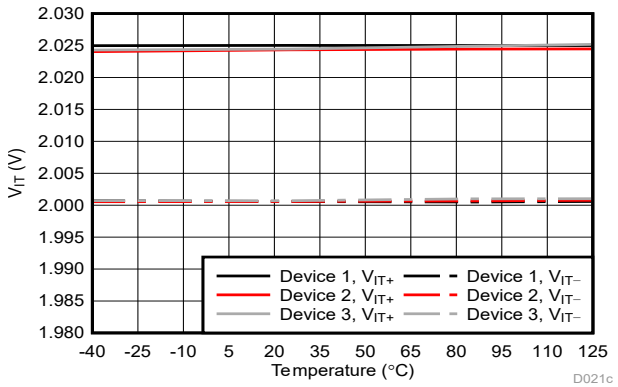
5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)



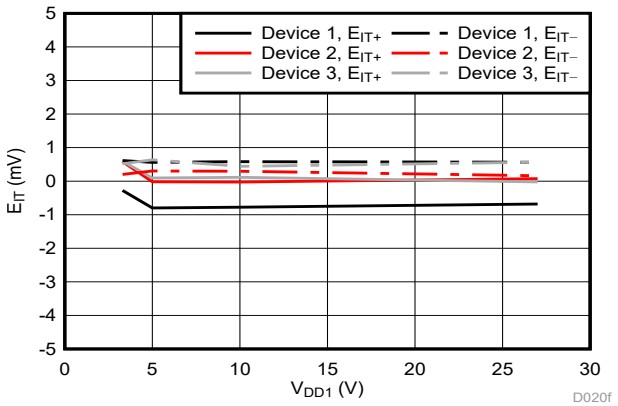
V_{REF} = 2V

Figure 5-30. Cmp0 Trip Threshold vs Supply Voltage



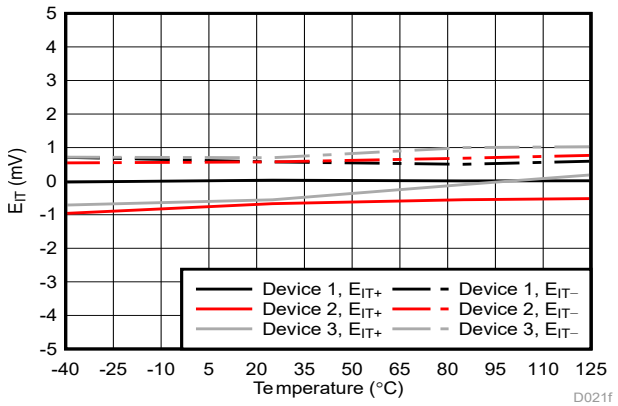
V_{REF} = 2V

Figure 5-31. Cmp0 Trip Threshold vs Temperature



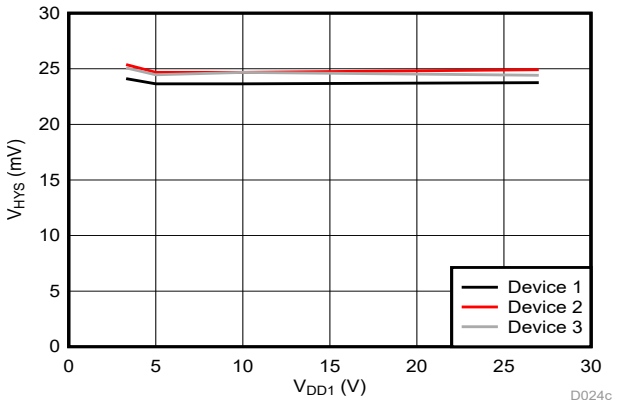
V_{REF} = 2V

Figure 5-32. Cmp0 Trip Threshold Error vs Supply Voltage



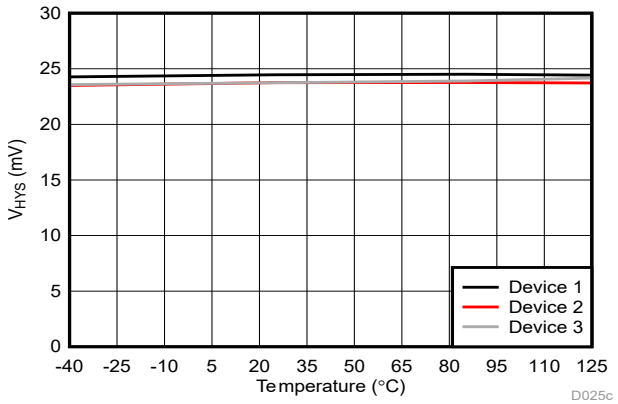
V_{REF} = 2V

Figure 5-33. Cmp0 Trip Threshold Error vs Temperature



V_{REF} = 2V

Figure 5-34. Cmp0 Trip Threshold Hysteresis vs Supply Voltage

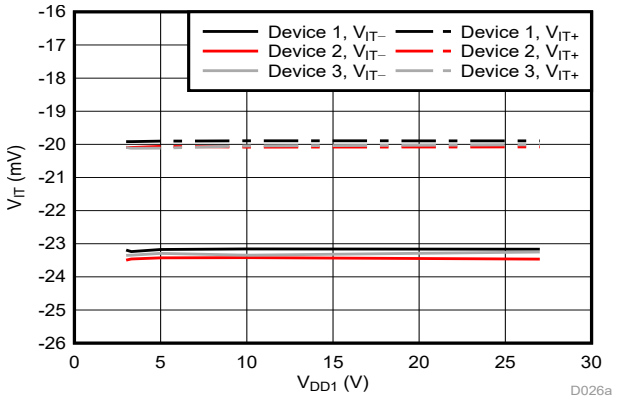


V_{REF} = 2V

Figure 5-35. Cmp0 Trip Threshold Hysteresis vs Temperature

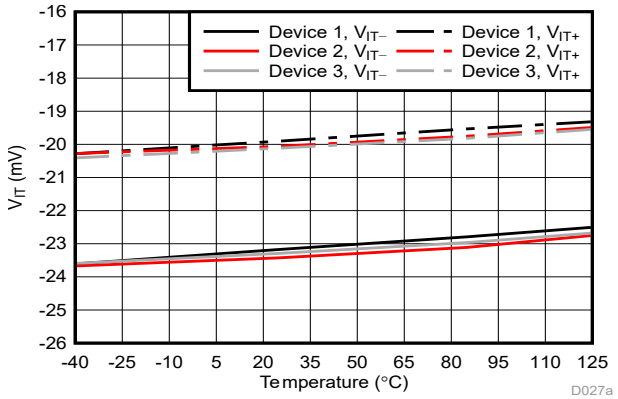
5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)



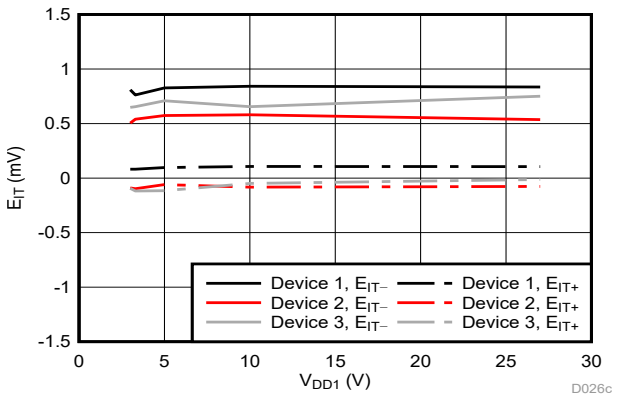
V_{REF} = 20mV

Figure 5-36. Cmp1 Trip Threshold vs Supply Voltage



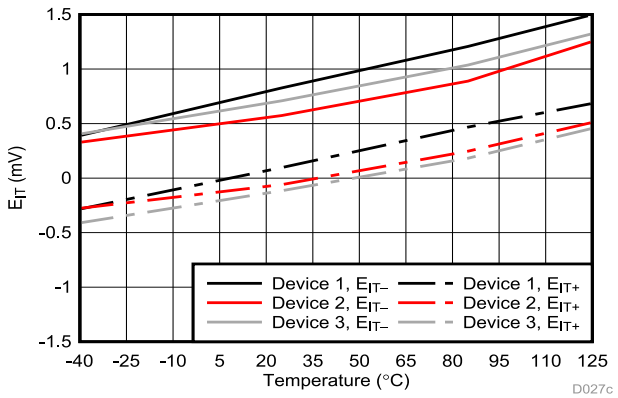
V_{REF} = 20mV

Figure 5-37. Cmp1 Trip Threshold vs Temperature



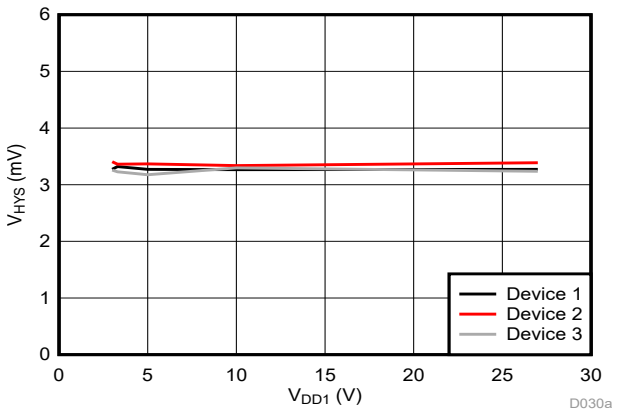
V_{REF} = 20mV

Figure 5-38. Cmp1 Trip Threshold Error vs Supply Voltage



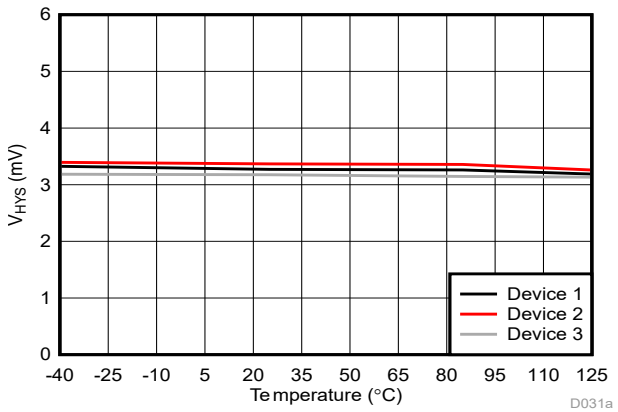
V_{REF} = 20mV

Figure 5-39. Cmp1 Trip Threshold Error vs Temperature



V_{REF} = 20mV

Figure 5-40. Cmp1 Trip Threshold Hysteresis vs Supply Voltage

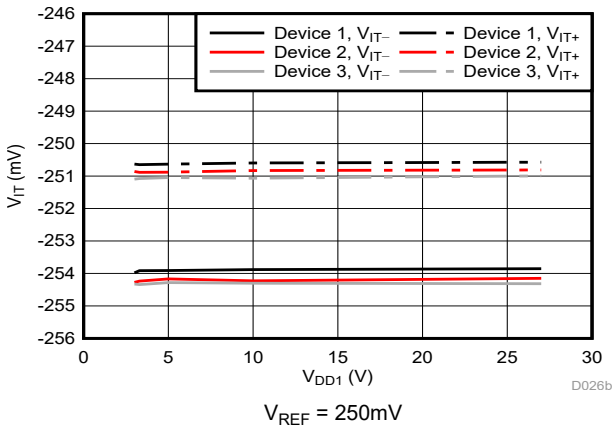


V_{REF} = 20mV

Figure 5-41. Cmp1 Trip Threshold Hysteresis vs Temperature

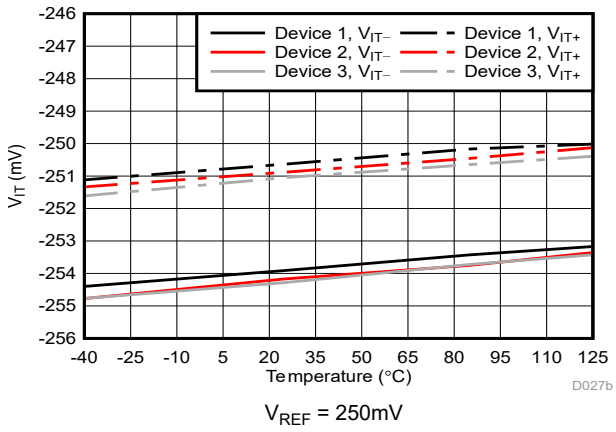
5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)



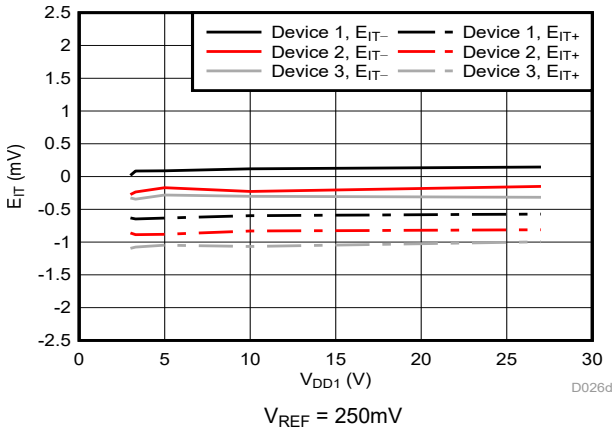
V_{REF} = 250mV

Figure 5-42. Cmp1 Trip Threshold vs Supply Voltage



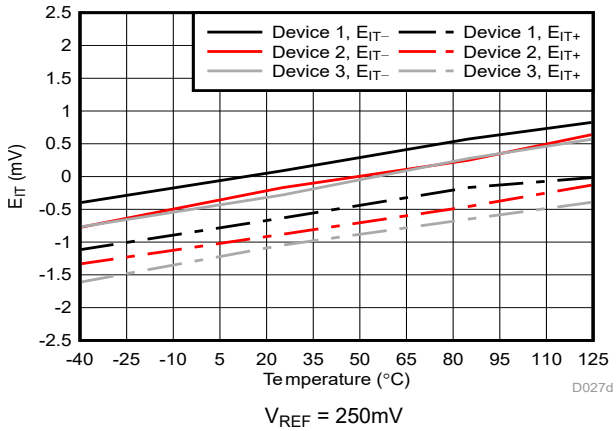
V_{REF} = 250mV

Figure 5-43. Cmp1 Trip Threshold vs Temperature



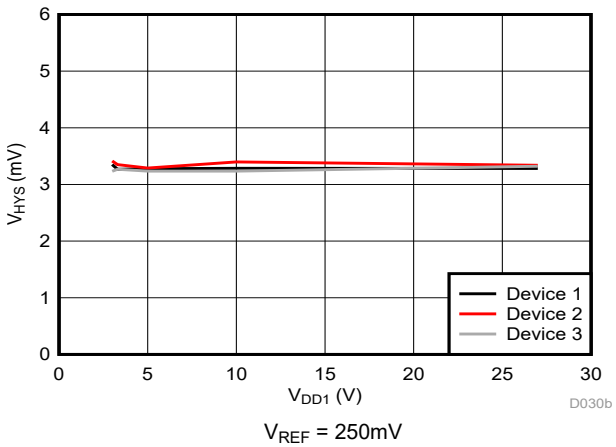
V_{REF} = 250mV

Figure 5-44. Cmp1 Trip Threshold Error vs Supply Voltage



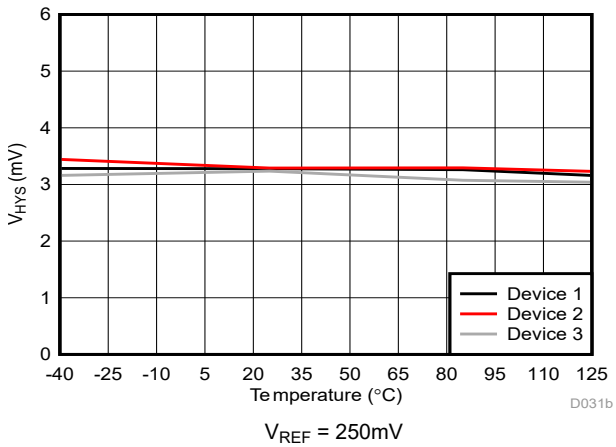
V_{REF} = 250mV

Figure 5-45. Cmp1 Trip Threshold Error vs Temperature



V_{REF} = 250mV

Figure 5-46. Cmp1 Trip Threshold Hysteresis vs Supply Voltage



V_{REF} = 250mV

Figure 5-47. Cmp1 Trip Threshold Hysteresis vs Temperature

5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

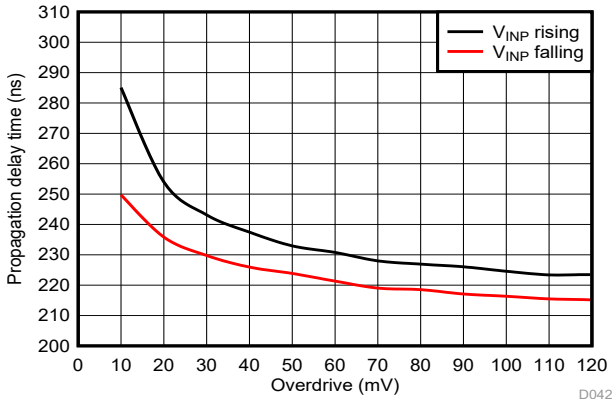


Figure 5-48. Cmp2 Propagation Delay vs Overdrive

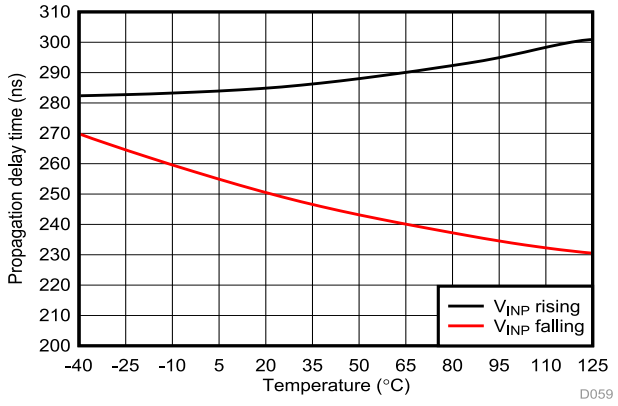


Figure 5-49. Cmp2 Propagation Delay vs Temperature

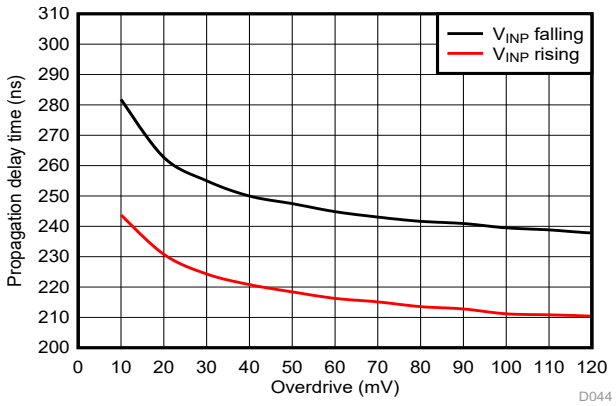


Figure 5-50. Cmp3 Propagation Delay vs Overdrive

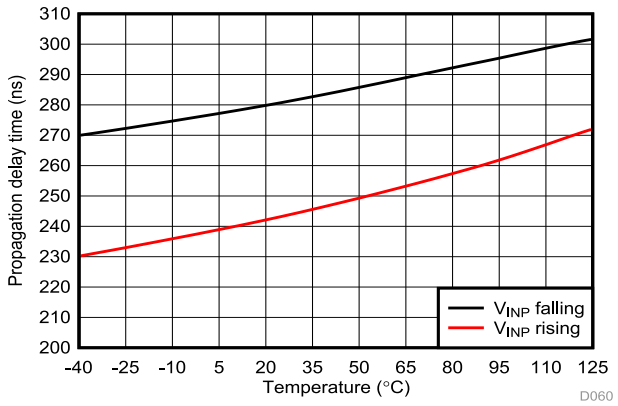


Figure 5-51. Cmp3 Propagation Delay vs Temperature

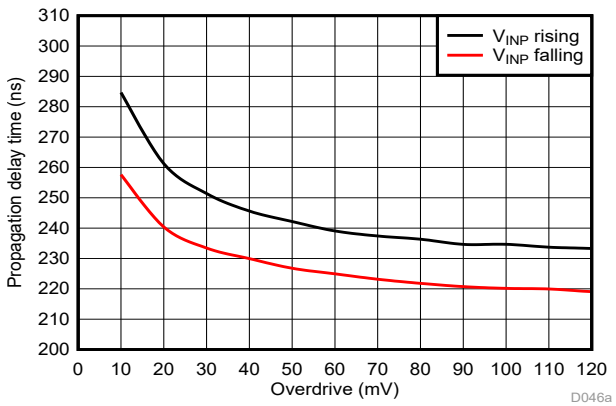


Figure 5-52. Cmp0 Propagation Delay vs Overdrive

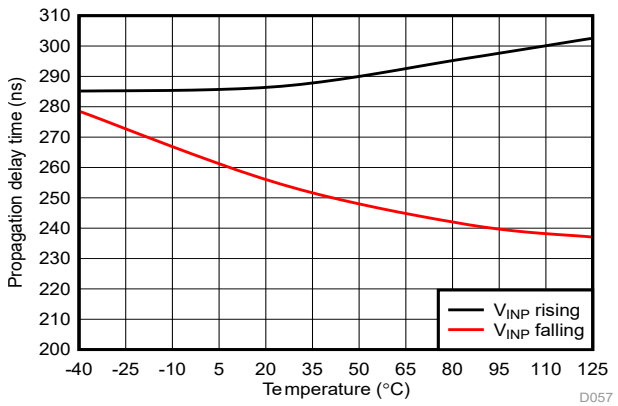


Figure 5-53. Cmp0 Propagation Delay vs Temperature

5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

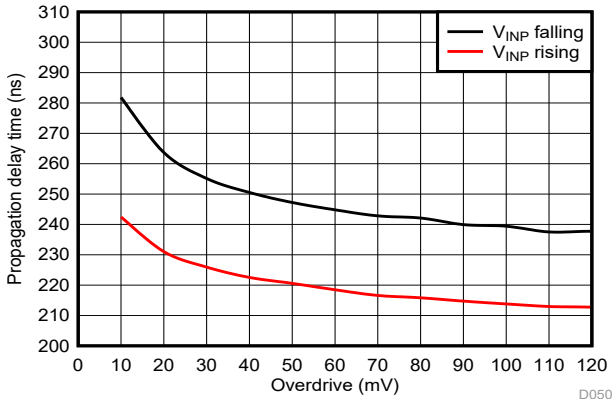
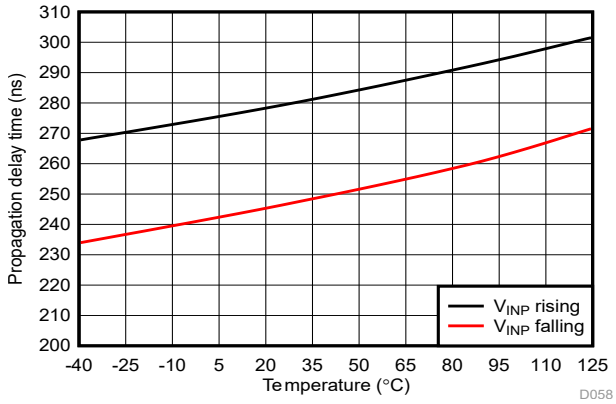


Figure 5-54. Cmp1 Propagation Delay vs Overdrive



$V_{OVERDRIVE}$ = 10mV

Figure 5-55. Cmp1 Propagation Delay vs Temperature

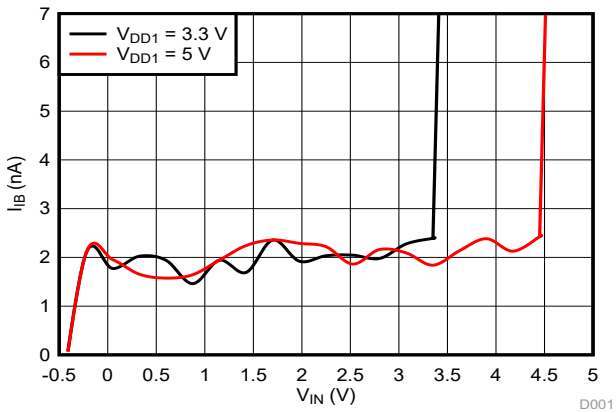
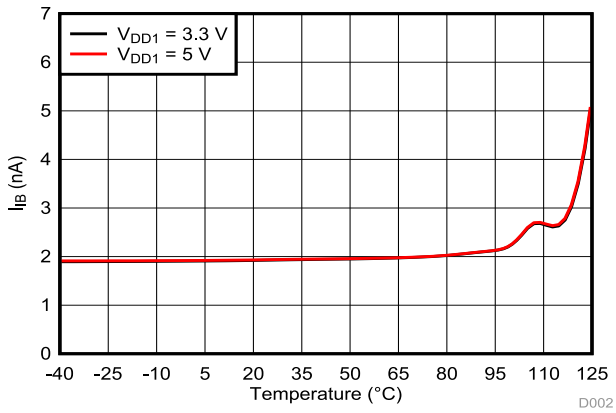


Figure 5-56. Input Bias Current vs Input Voltage



V_{IN} = 2V

Figure 5-57. Input Bias Current vs Temperature

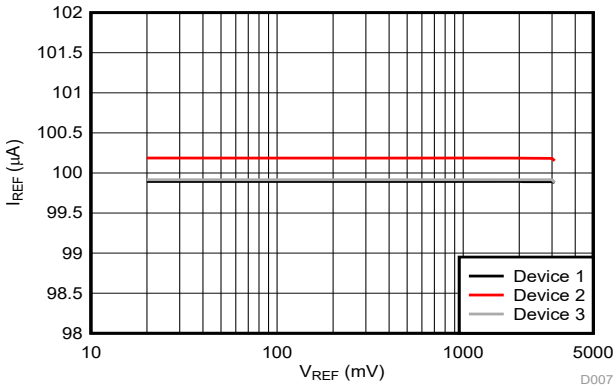


Figure 5-58. Reference Current vs Reference Voltage

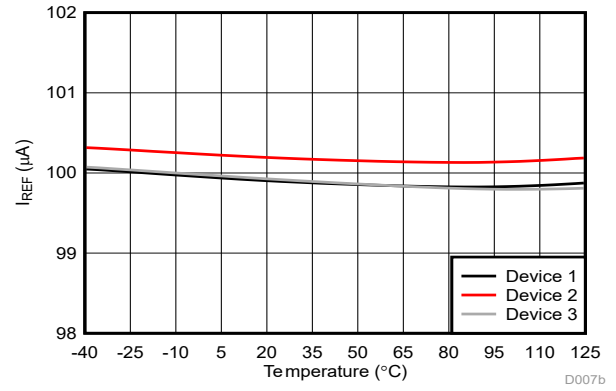


Figure 5-59. Reference Current vs Temperature

5.13 Typical Characteristics (continued)

At VDD1 = 5V and VDD2 = 3.3V (unless otherwise noted)

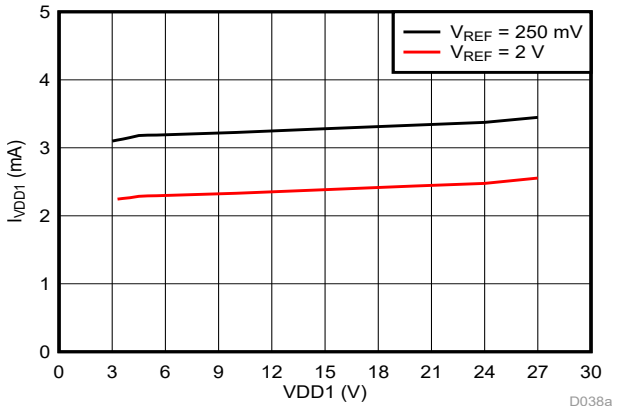


Figure 5-60. High-Side Supply Current vs Supply Voltage

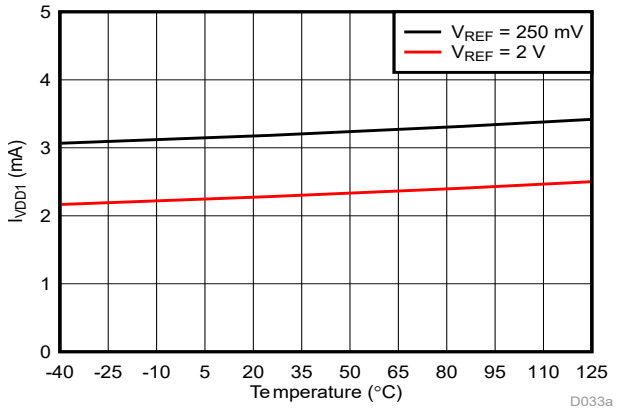


Figure 5-61. High-Side Supply Current vs Temperature

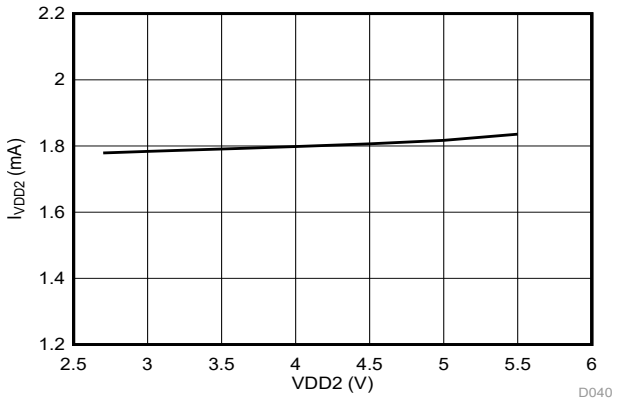


Figure 5-62. Low-Side Supply Current vs Supply Voltage

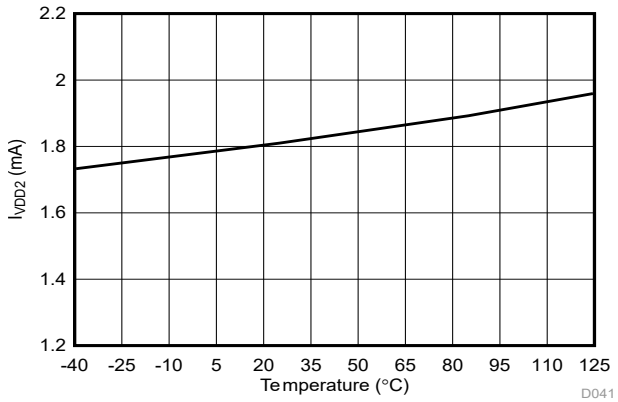


Figure 5-63. Low-Side Supply Current vs Temperature

6 Detailed Description

6.1 Overview

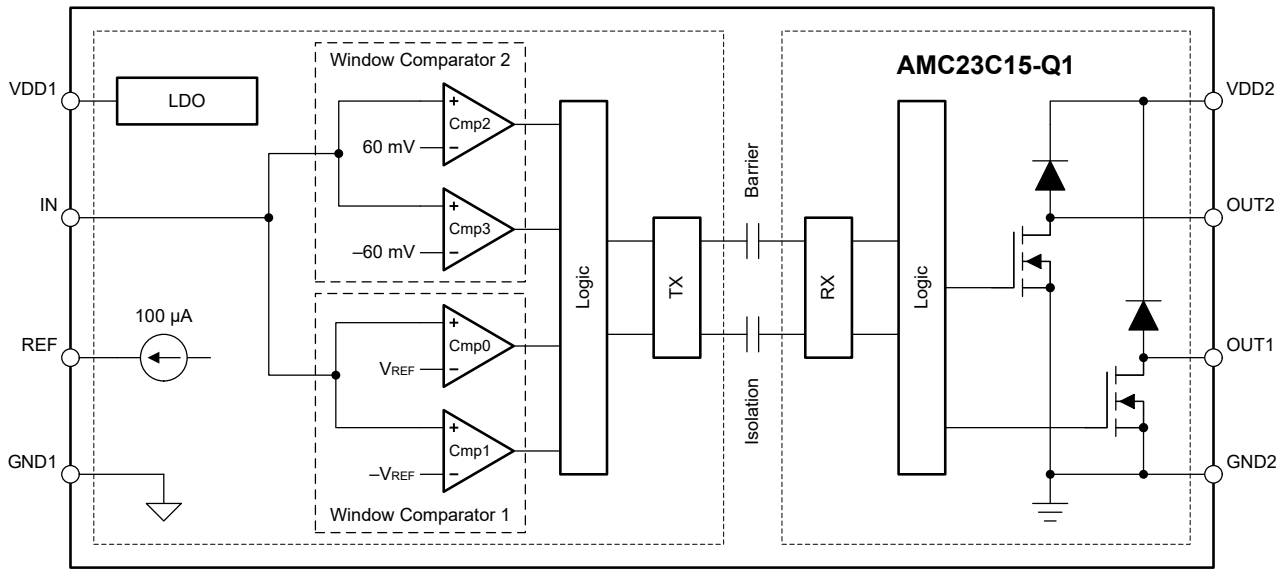
The AMC23C15-Q1 is a dual, isolated window comparator with open-drain outputs. Window comparator 1 is comprised of comparator Cmp0 and Cmp1 and window comparator 2 is comprised of Cmp2 and Cmp3. Cmp0 and Cmp2 compare the input voltage (V_{IN}) against the respective positive thresholds (V_{IT+}) and Cmp1 and Cmp3 compare the input voltage (V_{IN}) against the respective negative thresholds ($V_{IT–}$). The respective V_{IT+} and $V_{IT–}$ thresholds are of equal magnitude but opposite signs, therefore both window comparators have windows that are centered around 0V. Window comparator 2 has fixed thresholds of ±60mV. Window comparator 1 has adjustable thresholds from ±5mV to ±300mV through an internally generated 100µA reference current and a single external resistor.

The open-drain outputs are actively pulled low when the input voltage (V_{IN}) is outside the respective comparison window, but are otherwise in a high-impedance state.

When the voltage on the REF pin is greater than V_{MSEL}, the device operates in positive-comparator mode. This mode is particularly useful for monitoring positive voltage supplies. Both negative comparators (Cmp1 and Cmp3) are disabled and only the positive comparators (Cmp0 and Cmp2) are functional. The reference voltage in this mode can be as high as 2.7V.

Galvanic isolation between the high- and low-voltage side of the device is achieved by transmitting the comparator states across a SiO_2-based, reinforced capacitive isolation barrier. This isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation scheme used in the AMC23C15-Q1 to transmit data across the isolation barrier, and the isolation barrier characteristics, result in high reliability and common-mode transient immunity.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input

The AMC23C15-Q1 has a single input that drives both window comparators. Window comparator 1 has an adjustable threshold and window comparator 2 has a fixed threshold.

The positive comparators trip when the input voltage (V_{IN}) rises above the respective V_{IT+} threshold that is defined as the reference value plus the internal hysteresis voltage (for example, 64mV for the fixed-threshold comparator). The positive comparators release when V_{IN} drops below the respective $V_{IT–}$ threshold that equals the reference value (for example, 60mV for the fixed-threshold comparator). The negative comparators trip when V_{IN} drops below the respective $V_{IT–}$ threshold that is defined as the negative reference value minus the internal hysteresis voltage (for example, –64mV for the fixed-threshold comparator). The negative comparators release when V_{IN} rises above the respective V_{IT+} threshold that equals the negative reference value (for example –60mV for the fixed-threshold comparator).

The difference between V_{IT+} and $V_{IT–}$ is referred to as the *comparator hysteresis* and is 4mV for reference voltages below 450mV. The integrated hysteresis makes the AMC23C15-Q1 less sensitive to input noise and provides stable operation in noisy environments without having to add external positive feedback to create hysteresis. The hysteresis of Cmp0 increases to 25mV for reference values (V_{REF}) greater than 600mV. See the *Reference Input* description for more details.

Figure 6-1 shows a timing diagram of the relationship between hysteresis and switching thresholds.

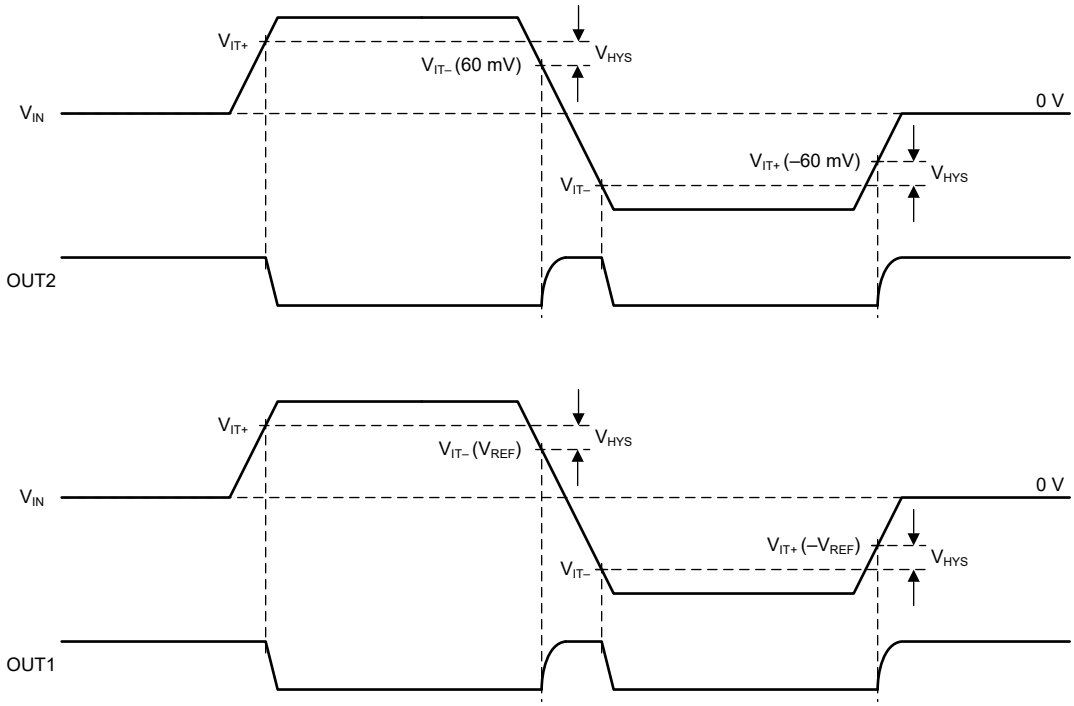


Figure 6-1. Switching Thresholds and Hysteresis

6.3.2 Reference Input

The voltage on the REF pin determines the trip threshold of window comparator 1. The internal precision current source forces a 100µA current through an external resistor connected from the REF pin to GND1. The resulting voltage across the resistor (V_{REF}) equals the magnitude of the positive and negative trip thresholds, see Figure 6-1. Place a 100nF capacitor parallel to the resistor to filter the reference voltage. This capacitor must be charged by the 100µA current source during power-up and the charging time can exceed the high-side blanking time ($t_{HS,BLK}$). In this case, as shown in Figure 6-2, window comparator 1 can output an incorrect state after the high-side blanking time has expired until V_{REF} reaches the final value. See the *Power-Up and Power-Down Behavior* section for more details on power-up behavior.

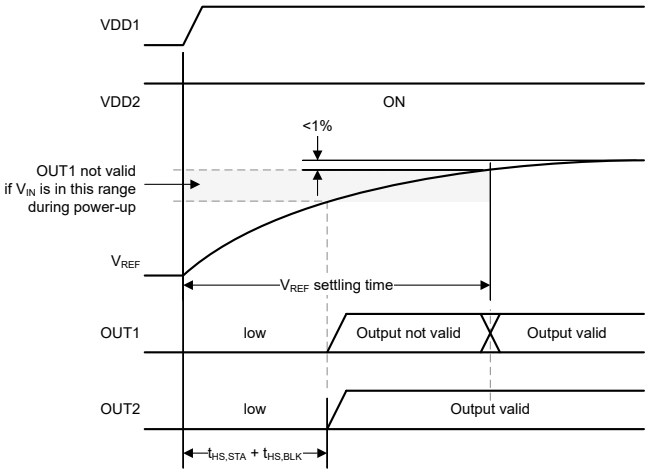


Figure 6-2. Output Behavior for Long Settling Times of the Reference Voltage

The voltage on the REF pin also determines the functionality of the negative comparators (Cmp1, Cmp3) and the hysteresis of the positive comparator (Cmp0) shown in the *Functional Block Diagram*. If V_{REF} exceeds the V_{MSEL} threshold defined in the *Electrical Characteristics* table, both negative comparators (Cmp1 and Cmp3) are disabled and the hysteresis of Cmp0 is increased from 4mV (typical) to 25mV. Positive-comparator mode is intended for voltage-monitoring applications that require higher input voltages and higher noise immunity.

The reference pin can be driven by an external voltage source to change the comparator thresholds during operation. However, do not drive V_{REF} dynamically across the V_{MSEL} threshold during normal operation because doing so changes the hysteresis of the Cmp0 comparator and can lead to unintentional switching of the OUT1 output.

Figure 6-3 shows a mode selection timing diagram.

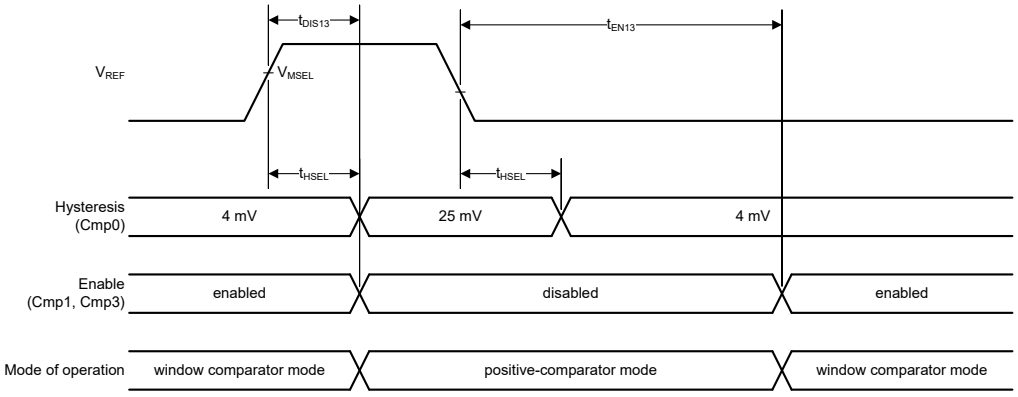


Figure 6-3. Mode Selection

6.3.3 Isolation Channel Signal Transmission

The AMC23C15-Q1 uses an on-off keying (OOK) modulation scheme, as shown in Figure 6-4, to transmit the comparator output states across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the data for the logic that drives the open-drain output buffers. The AMC23C15-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

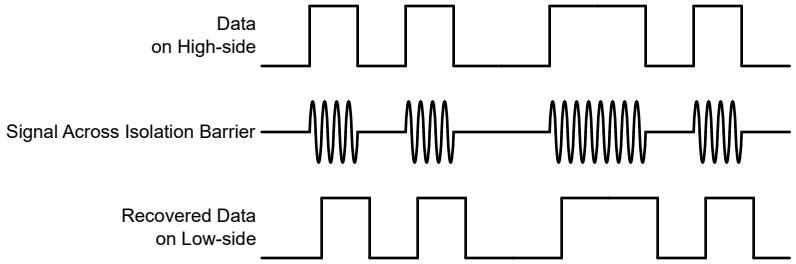


Figure 6-4. OOK-Based Modulation Scheme

6.3.4 Open-Drain Digital Outputs

The AMC23C15-Q1 has two open-drain outputs, one for each window comparator. As illustrated in Figure 6-1, OUT1 is actively pulled low when $|V_{IN}|$ exceeds the threshold values defined by the voltage on the REF pin. OUT2 is actively pulled low when $|V_{IN}|$ exceeds the threshold values defined by the internal 60mV reference.

The open-drain outputs are diode-connected to the VDD2 supply, see the *Functional Block Diagram*, which means the outputs cannot be pulled more than 500mV above the VDD2 supply before significant current begins to flow into the OUTx pins. In particular, the open-drain outputs are clamped to one diode voltage above ground if VDD2 is at the GND2 level. This behavior is indicated by the gray shadings in Figure 6-5 through Figure 6-10.

On a system level, the CMTI performance of an open-drain signal line depends on the value of the pullup resistor. During a common-mode transient event with a high slew rate (high dV/dt), the open-drain signal line can be pulled low because of parasitic capacitive coupling between the high side and the low side of the printed circuit board (PCB). The effect of the parasitic coupling on the signal level is a function of the pullup strength and a lower value pullup resistor results in better CMTI performance. The AMC23C15-Q1 is characterized by a relatively weak pullup resistor value of 10kΩ to make sure that the specified CMTI performance is met in a typical application with a 4.7kΩ or lower pullup resistor.

6.3.5 Power-Up and Power-Down Behavior

Both open-drain outputs power up in a high-impedance (Hi-Z) state when the low-side supply (VDD2) turns on. After power-up, if the high-side is not functional yet, both outputs are actively pulled low. As shown in Figure 6-5, this condition happens after the low-side start-up time plus the high-side fault detection delay time ($t_{LS,STA}$ + $t_{HS,FLT}$). Similarly, if the high-side supply drops below the undervoltage threshold ($VDD1_{UV}$), as described in Figure 6-8, for more than the high-side fault detection delay time during normal operation, both outputs are pulled low. This delay allows the system to shut down reliably when the high-side supply is missing.

Communication start between the high-side and low-side of the comparator is delayed by the high-side blanking time ($t_{HS,BLK}$, a time constant implemented on the high-voltage side) to allow the internal 60-mV reference and the voltage on the REF pin to settle and to avoid unintentional switching of the comparator outputs during power-up.

Figure 6-5 through Figure 6-10 depict typical power-up and power-down scenarios.

In Figure 6-5, the low-side supply (VDD2) turns on but the high-side supply (VDD1) remains off. Both outputs power up in the default Hi-Z state. After $t_{HS,FLT}$, both outputs are pulled low indicating a no-power fault on the high side.

In Figure 6-6, the high-side supply (VDD1) turns on long after the low-side supply (VDD2) turns on. Both outputs are initially in an active-low state, see Figure 6-5. After the high-side supply is enabled, there is a duration of $t_{HS,\ STA}$ + $t_{HS,BLK}$ before the device assumes normal operation and both outputs reflect the current state of the window comparators.

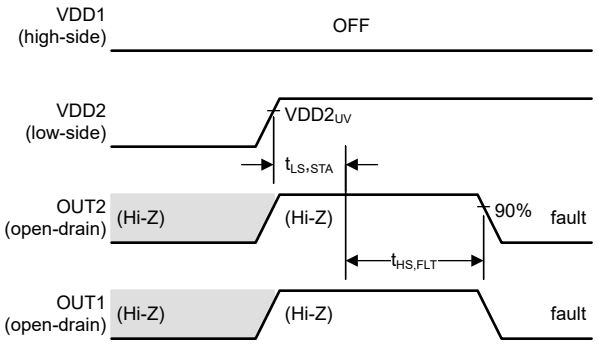


Figure 6-5. VDD2 Turns On, VDD1 Stays Off

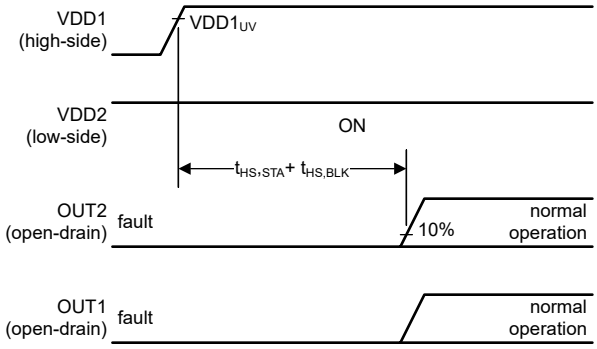


Figure 6-6. VDD2 is On; VDD1 Turns On (Long Delay)

In Figure 6-7, the low-side supply (VDD2) turns on, followed by the high-side supply (VDD1) with only a short delay. Both outputs are initially in a Hi-Z state. The high-side fault detection delay ($t_{HS,FLT}$) is shorter than the high-side blanking time ($t_{HS,BLK}$), and therefore both outputs are pulled low after $t_{HS,\ FLT}$, indicating that the high-side is not operational yet. After the high-side blanking time ($t_{HS,BLK}$) elapses, the device assumes normal operation and both outputs reflect the current state of the window comparators.

In Figure 6-8, the high-side supply (VDD1) turns off, followed by the low-side supply (VDD2). After the high-side fault detection delay time ($t_{HS,FLT}$), both outputs are actively pulled low. As soon as VDD2 drops below the $VDD2_{UV}$ threshold, both outputs enter a Hi-Z state.

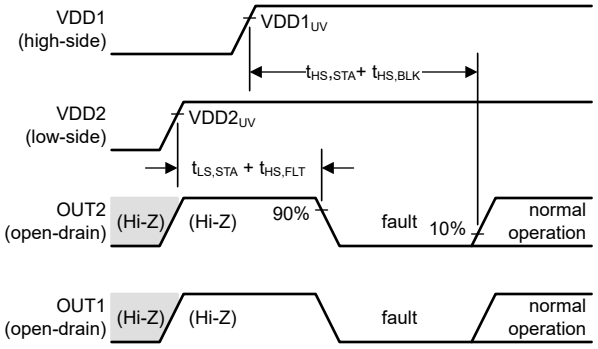


Figure 6-7. VDD2 Turns On, Followed by VDD1 (Short Delay)

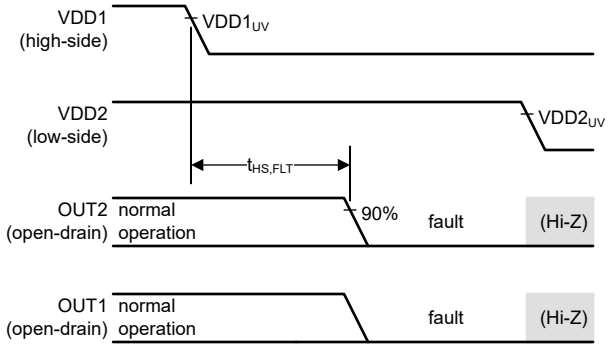


Figure 6-8. VDD1 Turns Off, Followed by VDD2

In Figure 6-9, the low-side supply (VDD2) turns on after the high-side is fully powered up (the delay between VDD1 and VDD2 is greater than ($t_{HS,STA}$ + $t_{HS,BLK}$)). Both outputs start in a Hi-Z state. After the low-side start-up time ($t_{LS,STA}$), the device enters normal operation.

In Figure 6-10, the low-side supply (VDD2) turns off, followed by the high-side supply (VDD1). As soon as VDD2 drops below the $VDD2_{UV}$ threshold, both outputs enter a Hi-Z state.

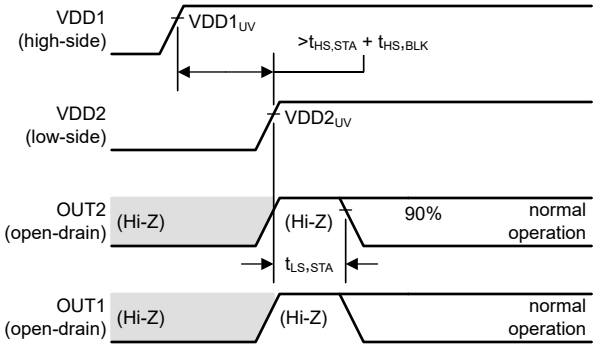


Figure 6-9. VDD1 Turns On, Followed by VDD2 (Long Delay)

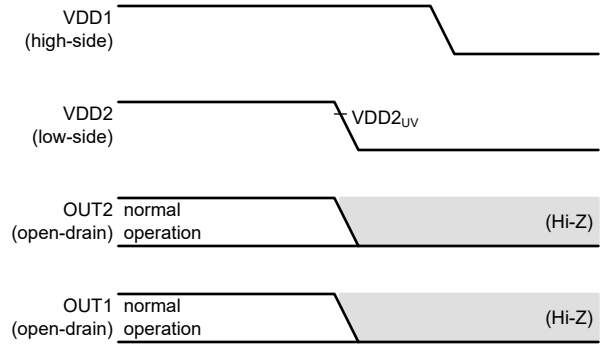


Figure 6-10. VDD2 Turns Off, Followed by VDD1

6.3.6 VDD1 Brownout and Power-Loss Behavior

Brownout is a condition where the VDD1 supply drops below the specified operating voltage range but the device remains functional. Power loss is a condition where the VDD1 supply drops below a level where the device stops being functional. Depending on the duration and the voltage level, a brownout condition can or can not be noticeable at the output of the device. A power-loss condition is always signaled on the output of the isolated comparator.

Figure 6-11 through Figure 6-13 show typical brownout and power-loss scenarios.

In Figure 6-11, VDD1 droops below the undervoltage detection threshold ($VDD1_{UV}$) but recovers before the high-side-fault detection delay time ($t_{HS,FLT}$) expires. The brownout event has no effect on the comparator outputs.

In Figure 6-12, VDD1 droops below the undervoltage detection threshold ($VDD1_{UV}$) for more than the high-side-fault detection delay time ($t_{HS,FLT}$). The brownout condition is detected as a fault and both outputs are pulled low after a delay equal to $t_{HS,FLT}$. The device resumes normal operation as soon as VDD1 recovers above the $VDD1_{UV}$ threshold.

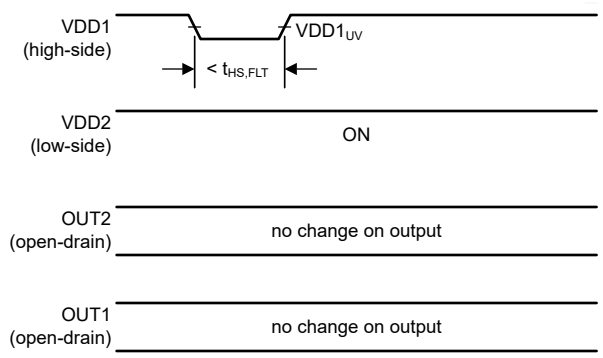


Figure 6-11. Output Response to a Short Brownout Event on VDD1

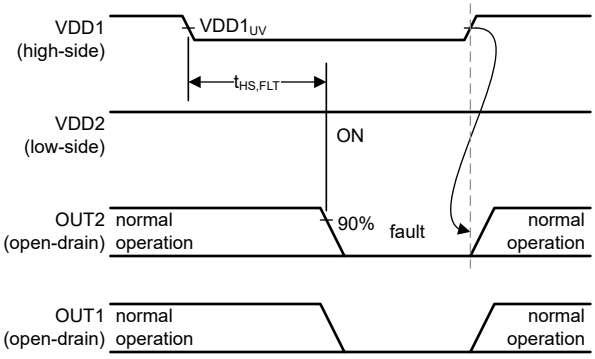


Figure 6-12. Output Response to a Long Brownout Event on VDD1

In Figure 6-13, VDD1 droops below the power-on-reset (POR) threshold ($VDD1_{POR}$). The power-loss condition is detected as a fault and both outputs are pulled low after a delay equal to $t_{HS,FLT}$. The device resumes normal operation after a delay equal to $t_{HS,STA}$ + $t_{HS,BLK}$ after VDD1 recovers above the $VDD1_{UV}$ threshold.

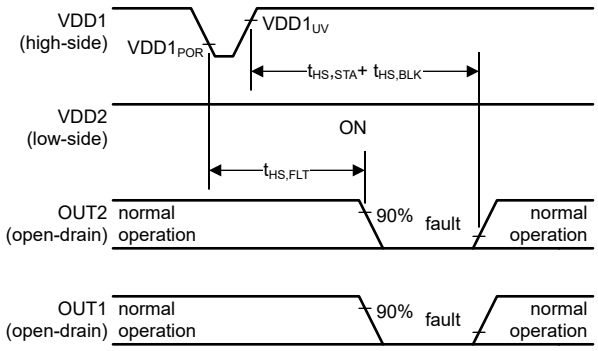


Figure 6-13. Output Response to a Power-Loss Event on VDD1

6.4 Device Functional Modes

The AMC23C15-Q1 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

The four comparators on the high-side (Cmp0 to Cmp3) function as two independent window comparators when the voltage on the REF pin is below the V_{MSEL} threshold. If the voltage on the REF pin exceeds the V_{MSEL} threshold, the negative comparators (Cmp1 and Cmp3) are disabled, and Cmp0 and Cmp2 function as two independent positive comparators, as described in the *Reference Input* section.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

With low response time, high common-mode transient immunity (CMTI), and a reinforced isolation barrier, the AMC23C15-Q1 is designed to provide fast and reliable overcurrent and overvoltage detection for high-voltage applications in harsh and noisy environments.

7.2 Typical Application

7.2.1 Overcurrent and Short-Circuit Current Detection

Fast overcurrent and short-circuit current detection is a common requirement in circuit breakers and solid state relays (SSR), and can be implemented with a single AMC23C15-Q1 isolated window comparator as shown in Figure 7-1.

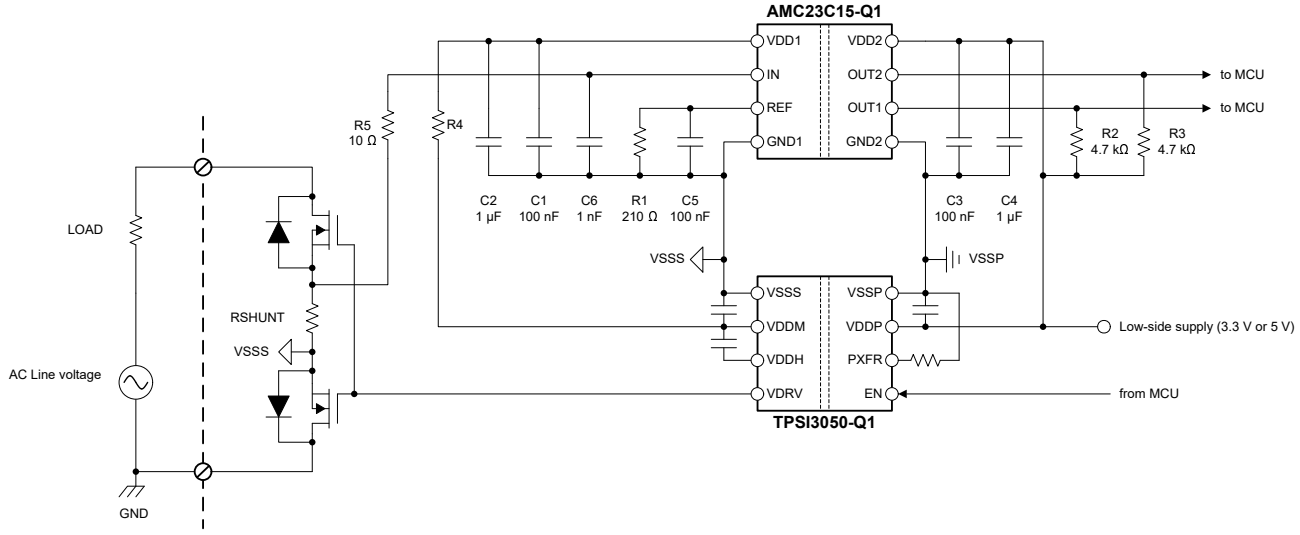


Figure 7-1. Using the AMC23C15-Q1 for Overcurrent and Short-Circuit Detection

The load current flowing through a shunt resistor (RSHUNT) connected in series with two back-to-back NMOS power switches of an SSR, and produces a voltage drop that is sensed by the AMC23C15-Q1. This voltage is compared against an adjustable threshold for overcurrent detection and a fixed, 60-mV threshold for short-circuit detection, respectively. The sense voltage can be positive or negative in respect to VSSS, which is the ground reference for the isolated comparator, depending on the direction of current flow. The absolute value of the trip threshold for overcurrent detection is set by the external resistor R1. The trip threshold for short-circuit

detection is fixed by the internal 60-mV reference. Overcurrent conditions are signaled on OUT1, and short-circuit conditions are signaled on OUT2. For a detailed description and a reference design of a SSR, see the *Overcurrent and Overtemperature Protection for Solid-State Relays Reference Design* design guide available for download on www.ti.com.

As depicted in Figure 7-1, the integrated LDO of the AMC23C15-Q1 allows direct connection of the high-side supply input (VDD1) to the VDDM supply that is generated by the isolated switch driver TPSI3050-Q1. No additional isolated power supply or regulator is required to power the high-side of the isolated comparator, which makes the solution very space and cost efficient. The fast response time and high common-mode transient immunity (CMTI) of the AMC23C15-Q1 provide reliable and accurate operation even in high-noise environments.

7.2.1.1 Design Requirements

Table 7-1 lists the parameters for the application example in Figure 7-1.

Table 7-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3 V to 25 V
Low-side supply voltage	2.7 V to 5.5 V
Shunt-resistor value	1 mΩ
Overcurrent detection threshold	±25 A
Short-circuit current detection threshold	±60 A

7.2.1.2 Detailed Design Procedure

The value of the shunt resistor in this example is 1 mΩ, determined by the internal 60-mV reference of the AMC23C15-Q1 and the desired 60-A short-circuit detection threshold.

At the desired 25-A overcurrent detection level, the voltage drop across the shunt resistor is 1 mΩ × 25 A = 25 mV. The positive-going trip threshold of window comparator 1 is V_{REF} + V_{HYS}, where V_{HYS} is 4 mV as specified in the *Electrical Characteristics* table, and V_{REF} is the voltage across R1 that is connected between the REF and GND1 pins. R1 is calculated as (V_{TRIP} – V_{HYS}) / I_{REF} = (25 mV – 4 mV) / 100 µA = 210 Ω and matches a value from the E96 series (1% accuracy).

A 10-Ω, 1-nF RC filter (R5, C6) is placed at the input of the comparator to filter the input signal and reduce noise sensitivity. This filter adds 10 Ω × 1 nF = 10 ns of propagation delay that must be considered when calculating the overall response time of the protection circuit. Larger filter constants are preferable to increase noise immunity if the system can tolerate the additional delay.

Table 7-2 summarizes the key parameters of the design.

Table 7-2. Overcurrent and Short-Circuit Detection Design Example

PARAMETER	VALUE
Reference resistor value (R1)	210 Ω
Reference capacitor value (C5)	100 nF
Reference voltage	21 mV
Reference voltage settling time (to 90% of final value)	50 µs
Overcurrent trip threshold (rising)	25 mV / 25.0 A
Overcurrent trip threshold (falling)	21 mV / 21 A
Short-circuit current trip threshold (rising)	64 mV / 64 A
Short-circuit current trip threshold (falling)	60 mV / 60.0 A

7.2.2 Application Curves

Figure 7-2 shows the typical response of the AMC23C15-Q1 to a bipolar, triangular input waveform with an amplitude of 140mV$_{PP}$. OUT1 switches when VIN crosses the ±50mV level determined by the REF pin voltage that is biased to 50mV in this example. OUT2 switches when VIN crosses the ±60mV level determined by the fixed internal reference value.

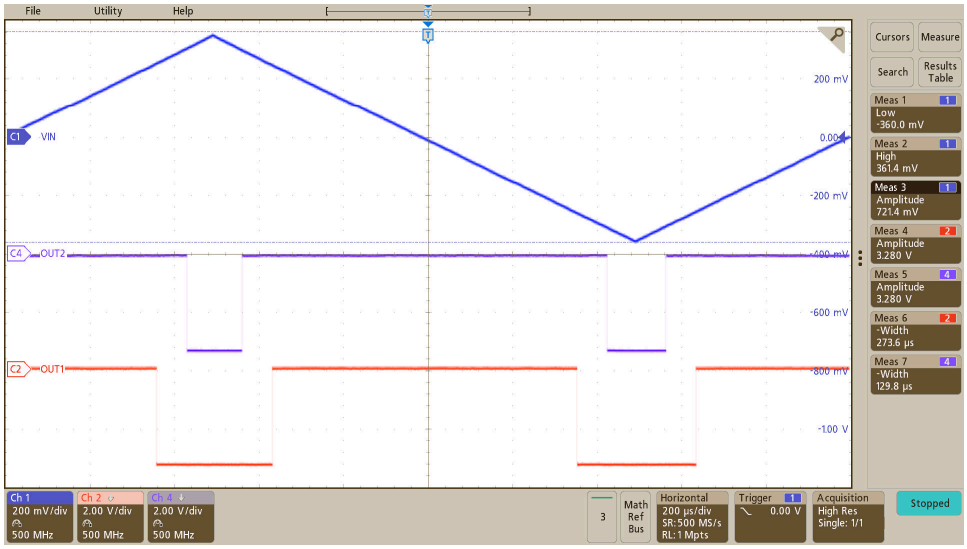


Figure 7-2. Output Response of the AMC23C15-Q1 to a Triangular Input Waveform

The integrated LDO of the AMC23C15-Q1 greatly relaxes the power-supply requirements on the high-voltage side and allows powering the device from non-regulated transformer, charge pump, and bootstrap supplies. As given by the following images, the internal LDO provides a stable operating voltage to the internal circuitry, allowing the trip thresholds to remain mostly undisturbed even at ripple voltages of 2V$_{PP}$ and higher.

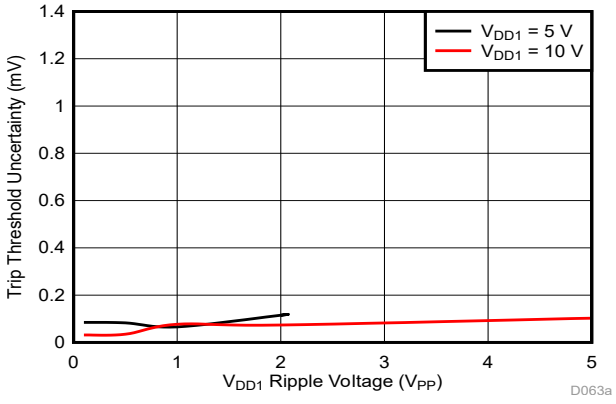


Figure 7-3. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp0, f_{RIPPLE} = 10kHz)

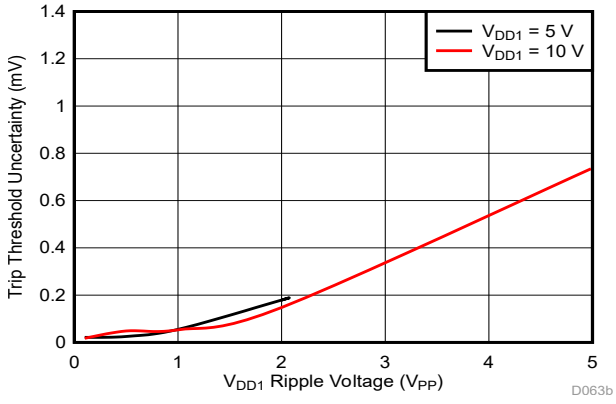


Figure 7-4. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp1, f_{RIPPLE} = 10kHz)

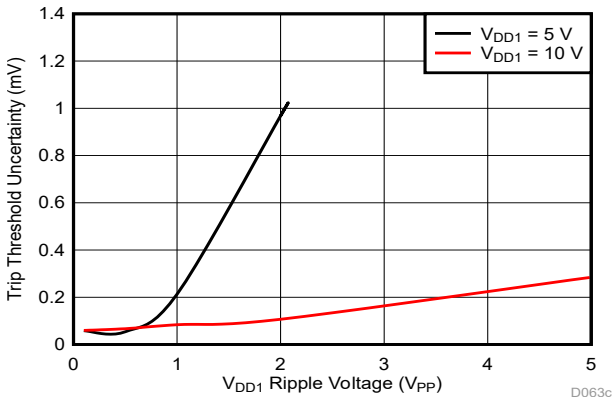


Figure 7-5. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp2, f_{RIPPLE} = 10kHz)

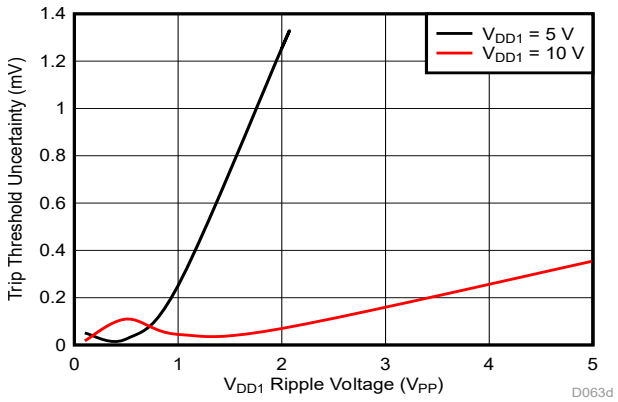


Figure 7-6. Trip Threshold Sensitivity to VDD1 Ripple Voltage (Cmp3, f_{RIPPLE} = 10kHz)

7.3 Best Design Practices

Keep the connection between the low-side of the sense resistor and the GND1 pin of the AMC23C15-Q1 short and low impedance. Any voltage drop in the ground line adds error to the voltage sensed at the input of the comparator and leads to inaccuracies in the trip thresholds.

For best common-mode transient immunity, place the filter capacitor C5 as closely to the REF pin as possible as illustrated in Figure 7-8. Use a low-value pullup resistor (<10kΩ) on the open-drain output, as explained in the *Open-Drain Digital Outputs* section, to minimize the effect of capacitive coupling on the open-drain signal line during a common-mode transient event.

Do not exceed the 300mV V_{REF} limit specified in the *Recommended Operating Conditions* table for bidirectional current-sensing applications. Do not operate the device with the REF pin biased close to the V_{MSEL} threshold (450mV to the 600mV range) to avoid dynamic switching of the Cmp0 hysteresis as explained in the *Reference Input* section.

The AMC23C15-Q1 provides a limited 200µs blanking time ($t_{HS,BLK}$) to allow the reference voltage (V_{REF}) to settle during start-up. For many applications, the reference voltage takes longer to settle than the 200µs blanking time and the output of the comparator can possibly glitch during system start-up as described in Figure 6-2. Consider the reference voltage settling time in the overall system start-up design.

7.4 Power Supply Recommendations

The AMC23C15-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 7-7 shows a decoupling schematic for the AMC23C15-Q1.

For high VDD1 supply voltages (>5.5V) place a 10Ω resistor (R4) in series with the VDD1 power supply for additional filtering.

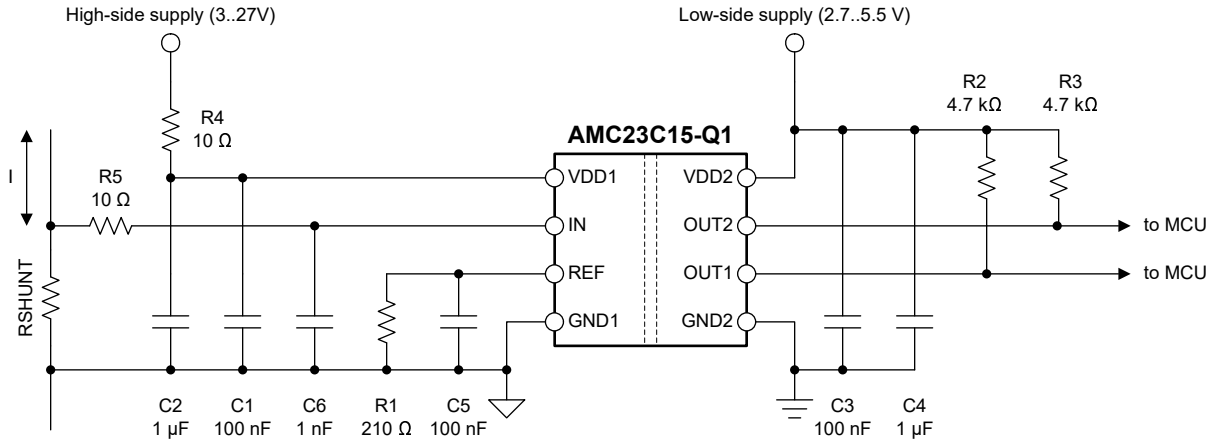


Figure 7-7. Decoupling of the AMC23C15-Q1

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of the nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

7.5 Layout

7.5.1 Layout Guidelines

Figure 7-8 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC23C15-Q1 supply pins) and placement of the other components required by the device.

7.5.2 Layout Example

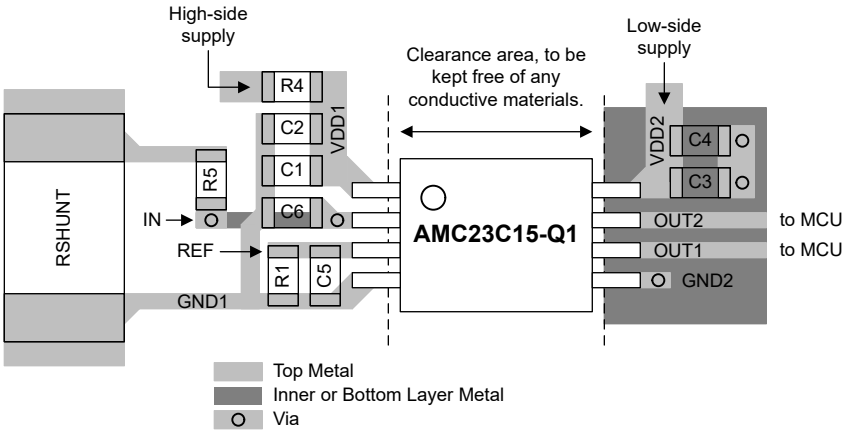


Figure 7-8. Recommended Layout of the AMC23C15-Q1

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application note
- Texas Instruments, *TPSI3050-Q1 Automotive Reinforced Isolated Switch Driver with Integrated 10V Gate Supply* data sheet
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 27, 2023 to September 30, 2024 (from Revision * (March 2023) to Revision A (December 2024)) **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC23C15QDWVRQ1	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MC23C15Q
AMC23C15QDWVRQ1.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	MC23C15Q
AMC23C15QDWVRQ1.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AMC23C15-Q1 :

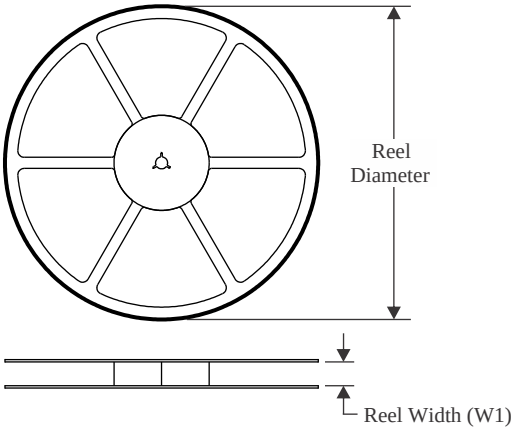
- Catalog : AMC23C15

NOTE: Qualified Version Definitions:

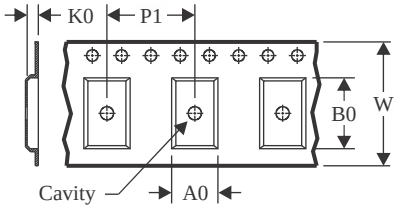
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

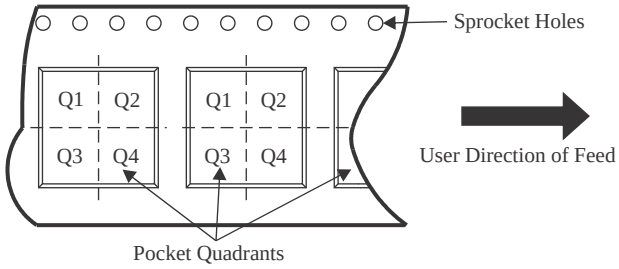


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

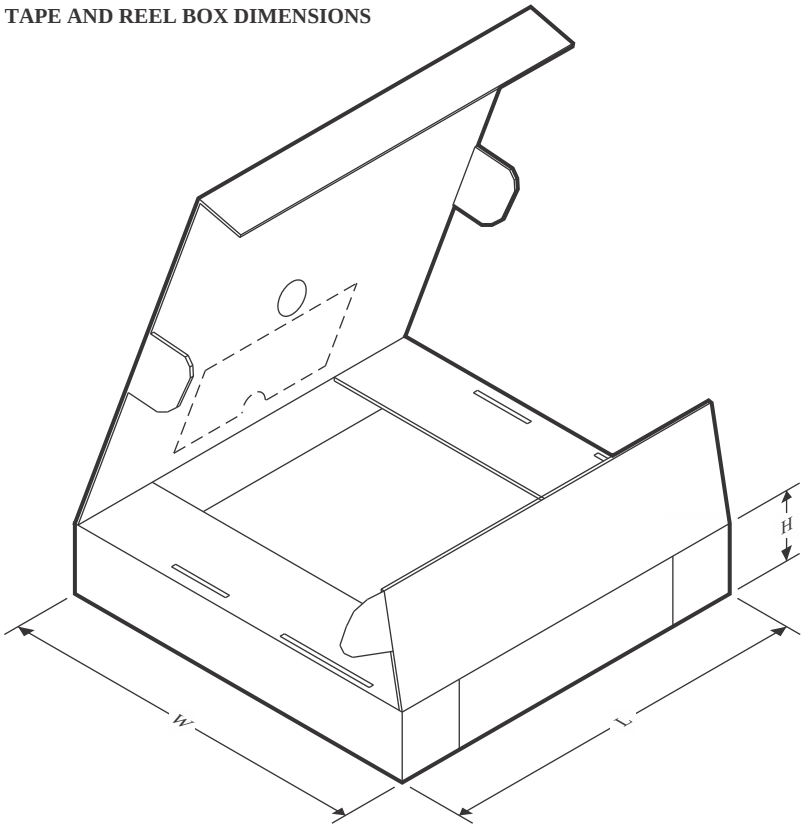
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

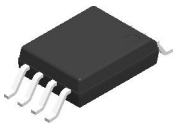
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC23C15QDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

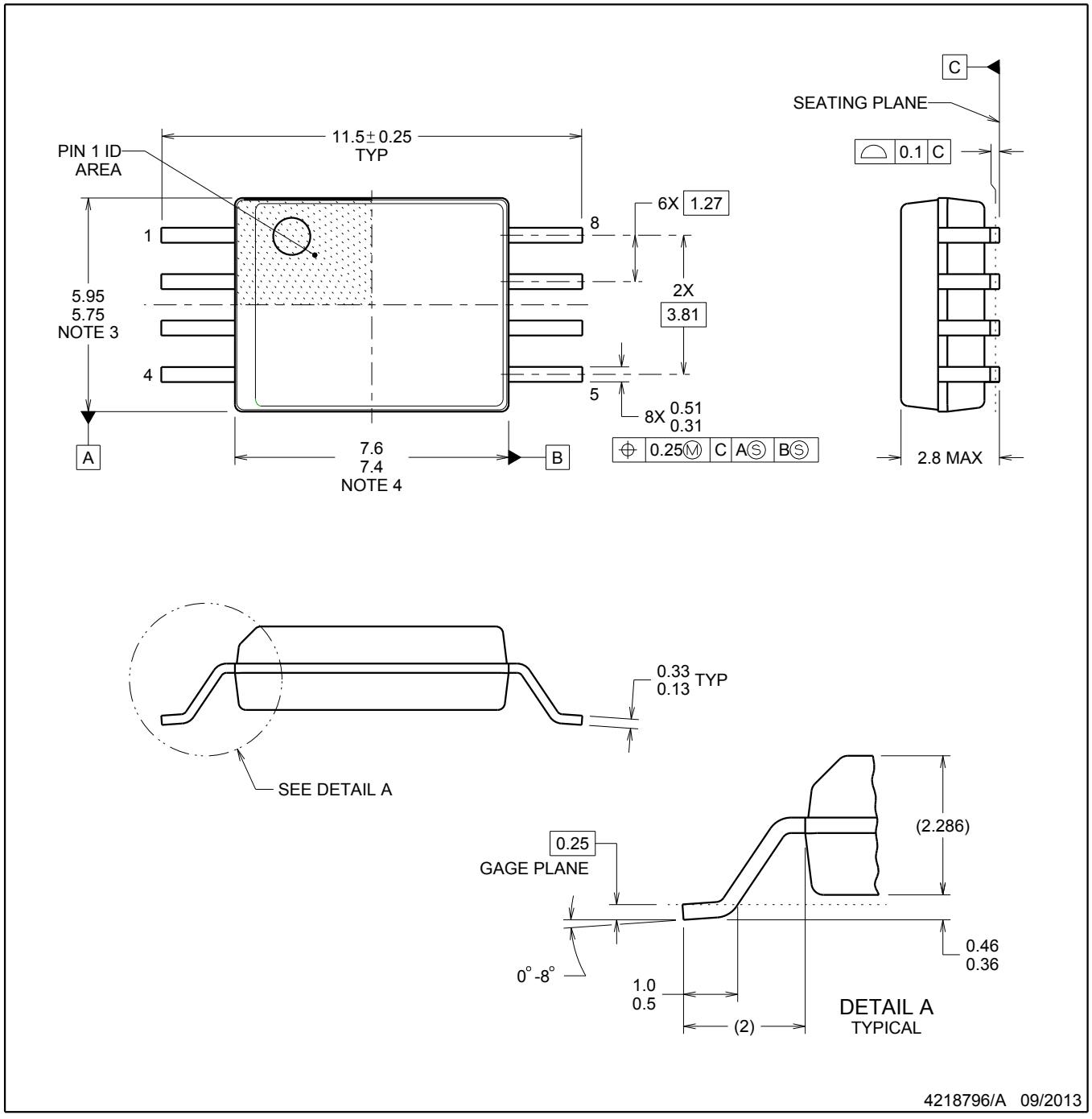
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC23C15QDWVRQ1	SOIC	DWV	8	1000	350.0	350.0	43.0



DWV0008A

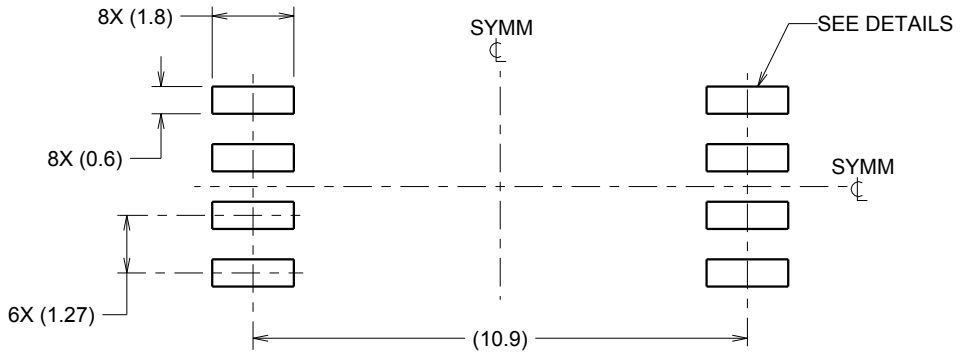
SOIC - 2.8 mm max height

SOIC

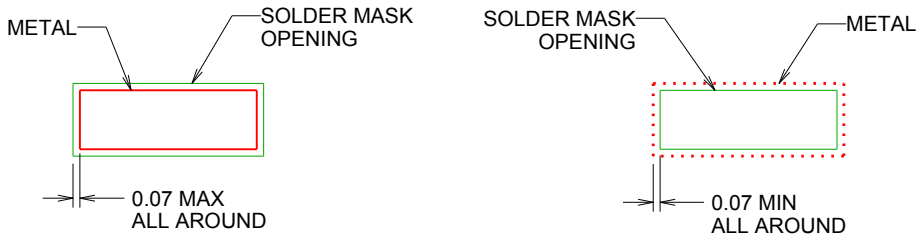


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

4218796/A 09/2013

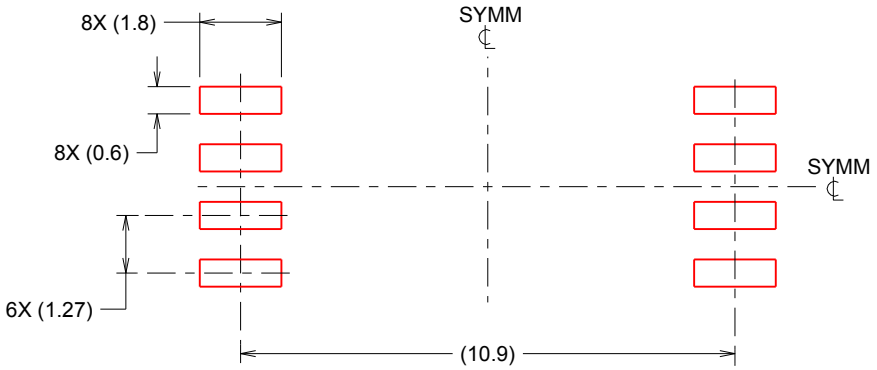
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025