

AWRL6843/AWRL6844 Single-Chip 57 to 64GHz Automotive Radar Sensor

1 Features

- FMCW Transceiver
 - Integrated PLL, transmitter, receiver, baseband and ADC
 - 57 - 64GHz coverage with 7GHz continuous bandwidth
 - 4 receive channels and 3 to 4 transmit channels (AWRL6843 with 3 channels and AWRL6844 with 4 channels)
 - 12.5dBm typical output power per TX
 - 12.5dB typical noise figure
 - -90.5dBc/Hz typical phase noise at 1MHz
 - FMCW operation
 - 10MHz IF bandwidth, real-only Rx channels
 - Ultra-accurate chirp engine based on fractional-N PLL
 - Per transmitter binary phase shifter
- Processing elements
 - Arm® R5F® core with double precision FPU (200MHz)
 - Hardware Accelerator (HWA 1.2) for FFT, log magnitude, and CFAR operations (200MHz)
 - C66x DSP (450MHz) for processing Radar data
- Supports multiple low-power modes
 - Idle mode and deep sleep mode
- Power management
 - 1.8V and 3.3V IO support
 - Built-in LDO network for enhanced PSRR
 - Two power rails for 1.8V IO mode, Three power rails for 3.3V IO mode
- FCCSP package having 17 x 17 BGA grid, 207 BGA balls; Package size: 9.1mm x 9.1mm
- Built-in calibration and self-test
 - Built-in Firmware (ROM)
 - Self-Contained on chip calibration system
- Host Interfaces
 - 3 x UART
 - 2 x CAN-FD
 - 2 x SPI
 - LIN
- LVDS for data transfer of raw ADC sample capture
- Other interfaces available to user application
 - QSPI
 - I2C
 - JTAG
 - 8 x GPIOs
 - PWM Interface
 - 4 x GPADCs
- Device security (on Secure device variants)
 - Programmable embedded hardware security module (HSM)
 - Secure authenticated and encrypted boot support
 - Customer programmable root keys, symmetric keys (256 bit), asymmetric keys (up to RSA-4K or ECC-512) with key revocation capability
 - Cryptographic hardware accelerators: PKA with ECC/RSA, AES (up to 256 bit), SHA (up to 512 bit), TRNG/DRBG and SM2, SM3, SM4(Chinese Crypto Algorithms)
 - Product Cybersecurity Compliance
 - ISO21434 compliant up to CAL2 targeted
 - Developed for cybersecurity-relevant applications
 - Documentation will be available to aid cybersecurity system design
- Internal memory
 - On-Chip RAM - 2.5MBytes (2MBytes for AWRL6843) including
 - R5F TCMA RAM - 512KB
 - R5F TCMB RAM - 256KB
 - DSS L2 RAM - 384KB
 - DSS L3 RAM - 512KB (available only in AWRL6844)
 - DSS L3 Shared RAM - 896KB (can be shared with TCMs)
- Functional Safety-Compliant Targeted
 - Developed for Functional Safety Applications
 - Documentation will be available to aid functional safety system design
 - Hardware integrity up to ASIL B targeted as per ISO26262 standard
- AEC Q-100 qualified
- Clock source
 - 40.0MHz crystal for primary clock
 - Supports externally driven clock (Square/Sine) at 40.0MHz
 - 32kHz internal oscillator for low power operations
- Operating temperature range
 - Junction Temperature Range: -40°C to 140°C



2 Applications

- Interior cabin sensing
- Child presence detection
- Vehicle occupancy detection, localization and classification
- Vehicle occupant vital sign monitoring
- Intruder detection
- Seat belt reminder

3 Description

The AWRL684x mmWave Sensor device is TI's low power and Hardware Security Module (HSM) enabled integrated single chip mmWave sensor based on FMCW radar technology. The device is capable of operation in the 57GHz to 63.9GHz band with 7GHz continuous chirp bandwidth and is designed for various automotive in-cabin use cases. The device also takes advantage of a low power architecture to enable power-constrained applications. The device is split into the following four switchable power domains:

1. **RF/Analog Sub-System:** This block includes all the RF and Analog components required to transmit and receive the RF signals.
2. **Front-End Controller Sub-System (FECSS):** This block contains a processor that is responsible for the radar front-end configuration, control and calibration.
3. **Application Sub-System (APPSS):** APPSS provisions the user with programmable ARM Cortex-R5F MCU for custom application development and automotive interfaces. APPSS includes TOPSS, HSM, clocking and power management sub-blocks.
4. **DSP Sub-Systems (DSS):** DSS incorporates TI's high-performance C66x DSP is integrated in it for radar signal processing. The DSS also includes hardware accelerator block (HWA 1.2) supplements the DSP and ARM Cortex-R5F by offloading common radar processing such as FFT, constant false alarm rate (CFAR), scaling, and compression.

The AWRL684x is specifically designed to be able to dynamically control the power states of the above-mentioned power domains based on application requirements. The device also features various low-power states and that are achieved by turning off internal IP blocks of the device. AWRL684x device also provides the option of retaining memory during these low power states to retain critical information such as application image and RF profiles across different power modes.

A Hardware Security Module (HSM) is also provisioned in the device (available with secure part variants). The HSM consists of a programmable Arm Cortex-M4 core and the necessary infrastructure to provide a secure zone of operation within the device.

Additionally, the device is built with TI's low power 45nm RF CMOS process and enables unprecedented levels of integration in an extremely small form factor. AWRL684x is designed for low power, self-monitored, ultra-accurate radar systems in the automotive space for applications like child presence detection, occupancy localization & classification and low power intrusion monitoring.

Packaging Information

| PART NUMBER ⁽¹⁾ | PACKAGE | BODY SIZE ⁽¹⁾ | TRAY / TAPE AND REEL | DESCRIPTION |
|----------------------------|------------------|--------------------------|----------------------|--|
| AWRL6843DBGANCQR1 | ANC (FCCSP, 207) | 9.1mm x 9.1mm | Tape and Reel | Automotive production variant. ASIL-B targeted. Deep Sleep enabled. General purpose variant. |
| AWRL6843DBSANCQR1 | ANC (FCCSP, 207) | 9.1mm x 9.1mm | Tape and Reel | Automotive production variant. ASIL-B targeted. Deep Sleep enabled. Secure Variant - ISO21434 compliant up to CAL2 targeted. |

Packaging Information (continued)

| PART NUMBER ⁽¹⁾ | PACKAGE | BODY SIZE ⁽¹⁾ | TRAY / TAPE AND REEL | DESCRIPTION |
|----------------------------|------------------|--------------------------|-------------------------|--|
| AWRL6844DBGANCRQ1 | ANC (FCCSP, 207) | 9.1mm x 9.1mm | Tape and Reel | Automotive production variant. ASIL-B targeted. Deep Sleep enabled. General purpose variant. |
| AWRL6844DBSANCRQ1 | ANC (FCCSP, 207) | 9.1mm x 9.1mm | Tape and Reel | Automotive production variant. ASIL-B targeted. Deep Sleep enabled. Secure Variant - ISO21434 compliant up to CAL2 targeted. |

(1) For more information, see , [Device Nomenclature](#) and [Mechanical, Packaging, and Orderable Information](#)

4 Functional Block Diagram

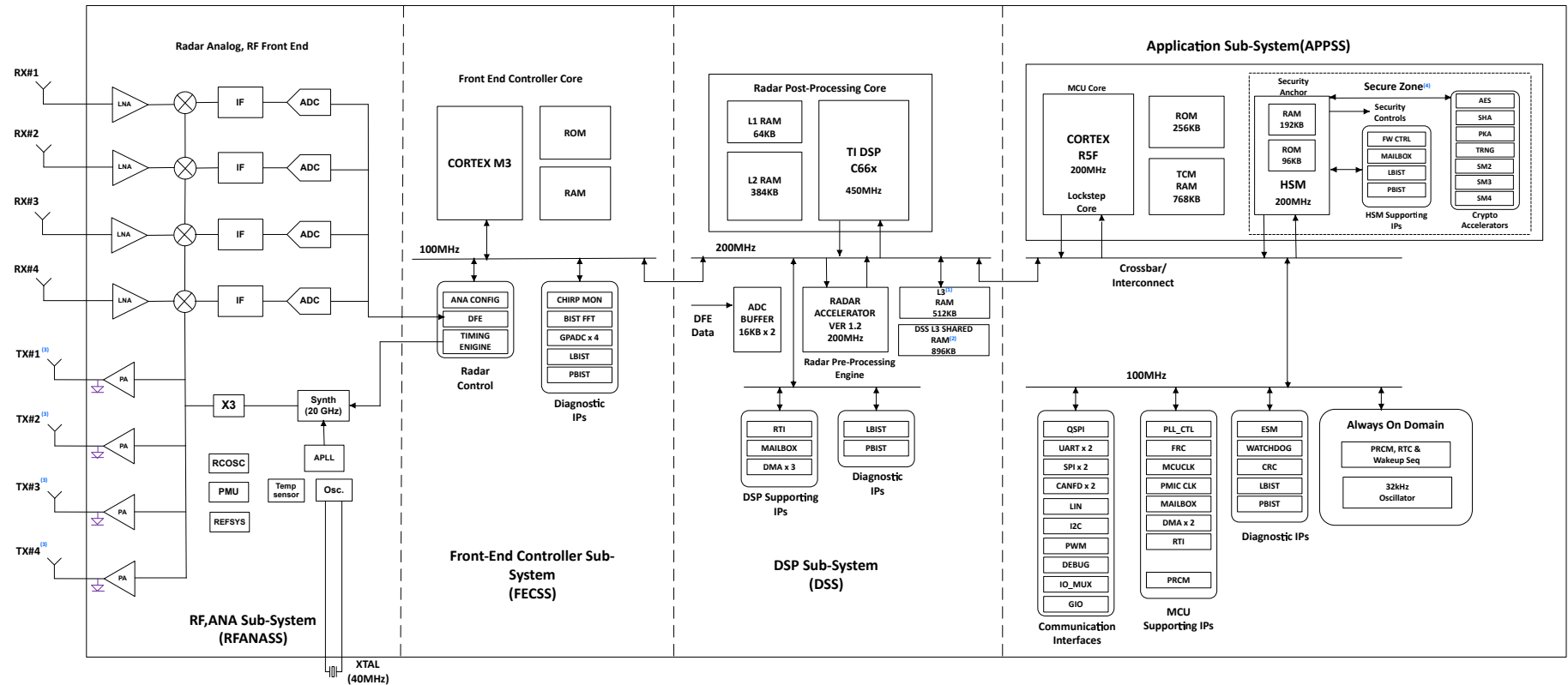


Figure 4-1. Functional Block Diagram

1. 512KB of DSS L3 Native RAM available only in AWRL6844
2. 896KB of DSS L3 Shared RAM Memory location is listed in [Table 4-1](#)
3. The AWRL6843 device has four transmitter antennas out of which any group of 3 transmitter antennas can be used (TX1, TX2, TX3), (TX1, TX2, TX4), (TX1, TX3, TX4) & (TX2, TX3, TX4).
4. Applicable to secure device variants only.

Table 4-1. Shared Memory Allocation

| Memory | Allocation |
|--------|--------------------|
| 512KB | DSS L3, APPSS TCMA |
| 256KB | DSS L3, APPSS TCMB |
| 128KB | DSS L3, FECSS |

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5 Device Comparison

The following table compares the features of radar devices.

Table 5-1. Device Features Comparison

| FUNCTION | AWRL6844 | AWRL6843 | AWR6843 | AWR6843AOP | AWRL6432 |
|--|---|--------------------------------|-----------------------------|-----------------------------|------------------------------------|
| Antenna on Package (AOP) | - | - | - | Yes | - |
| Number of receivers | 4 | 4 | 4 | 4 | 3 |
| Number of transmitters | 4 | 3 | 3 | 3 | 2 |
| RF frequency range | 57 to 64GHz | 57 to 64GHz | 60 to 64GHz | 60 to 64GHz | 57 to 64GHz |
| On-chip memory | 2.5MB | 2MB | 1.75MB | 1.75MB | 1MB |
| Max I/F (Intermediate Frequency) (MHz) | 10 | 10 | 10 | 10 | 5 |
| Max real sampling rate (Msps) | 25 | 25 | 25 | 25 | 12.5 |
| Max Complex Sampling rate (Msps) | - | - | 12.5 | 12.5 | - |
| Low Power Deep Sleep Mode | Yes | Yes | - | - | Yes |
| Safety and Security | | | | | |
| Functional Safety -Compliance | ASIL-B Targeted ⁽¹⁾ | ASIL-B Targeted ⁽¹⁾ | ASIL-B | ASIL-B | ASIL-B |
| Cybersecurity - Compliance | CAL2 targeted | CAL2 targeted | - | - | - |
| Device Security ⁽²⁾ | Yes (Secure Boot supported) | Yes (Secure Boot supported) | Yes (Secure Boot supported) | Yes (Secure Boot supported) | Yes (Authenticated Boot supported) |
| Hardware Security Module (HSM) | Yes | Yes | - | - | - |
| Processors | | | | | |
| MCU | R5F® | R5F® | R4F® | R4F® | M4F® |
| DSP | C66x | C66x | C674x | C674x | - |
| HWA | HWA 1.2 | HWA 1.2 | HWA1.1 | HWA1.1 | HWA 1.2 |
| Peripherals | | | | | |
| Serial Peripheral Interface (SPI) ports | 2 | 2 | 2 | 2 | 2 |
| Quad Serial Peripheral Interface (QSPI) | Yes | Yes | Yes | Yes | Yes |
| Inter-Integrated Circuit (I2C) interface | 1 | 1 | 1 | 1 | 1 |
| Controller Area Network (CAN-FD) interface | 2 | 2 | 2 | 2 | 1 |
| DSP Trace | - | - | Yes | Yes | - |
| PWM | Yes | Yes | Yes | Yes | Yes |
| Hardware In Loop (HIL/DMM) | - | - | Yes | Yes | - |
| GPADC | 4 | 4 | 6 | 6 | 2 |
| ADC Raw Data Capture | LVDS | LVDS | LVDS | LVDS | RDIF |
| LIN | Yes | Yes | - | - | Yes |
| UART | 3 ⁽³⁾ | 3 ⁽³⁾ | 2 | 2 | 2 |
| JTAG | Yes | Yes | Yes | Yes | Yes |
| Per Chirp configurable TX phase shifter | BPM Only | BPM Only | Yes ⁽⁴⁾ | Yes ⁽⁴⁾ | BPM Only |
| Product status | Product Preview (PP), Advance Information (AI), or Production Data (PD) | PD ⁽⁵⁾ | PD ⁽⁵⁾ | PD ⁽⁵⁾ | PD ⁽⁵⁾ |

- (1) As the certification can get secured at different times and post certificate the target will be updated to “compliant” from “compliance targeted” only in related data sheets, please refer to the respective data sheets for most recent compliance status.
- (2) Device security features including Secure Boot and Customer Programmable Keys are available in select devices for only select part variants as indicated by the Device Type identifier in Section 3, Device Information table.
- (3) 3 UART instances are available, including 2 UART instance from APPSS and 1 UART instnce from DSS
- (4) 6 bits linear Phase Shifter.

- (5) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty.

5.1 Related Products

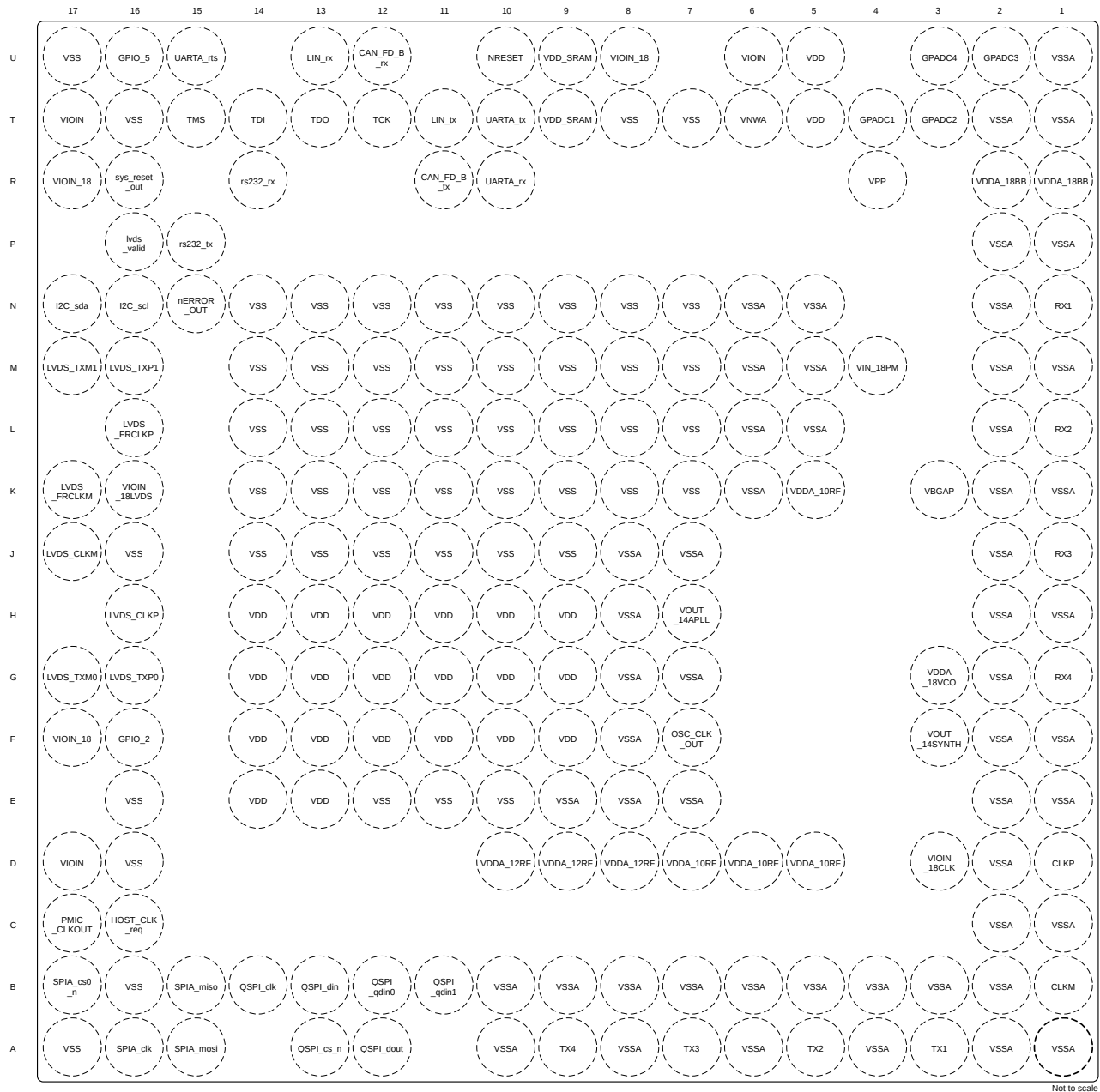
For information about other devices in this family of products or related products see the links that follow.

- mmWave Sensors** TI's mmWave sensors rapidly and accurately sense range, angle and velocity with less power using the smallest footprint mmWave sensor portfolio for automotive applications.
- Automotive mmWave Sensors** TI's automotive mmWave sensor portfolio offers high-performance radar front end to ultra-high resolution, small and low-power single-chip radar solutions. TI's scalable sensor portfolio enables design and development of ADAS, in-cabin and near field system solution for every performance, application and sensor configuration ranging from comfort functions to safety functions in all vehicles.
- Companion Products for AWRL684x** Review products that are similar to this product.

6 Terminal Configurations and Functions

6.1 Pin Diagrams

FCCSP Pin Diagram (Top View)



6.2 Signal Descriptions

Note

All digital IO pins of the device (except NRESET) are non-failsafe; hence, care needs to be taken that they are not driven externally without the VIO supply being present to the device.

LVDS interface is intended for debugging and development purposes, not for production use

T13 and C17 pins also serves as a Sense On Power lines and impacts boot mode SOP0 and SOP1 respectively. For more details refer to the [Pin Attributes](#).

Table 6-1. Analog Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|--------------------|----------|-------------------------|---------|
| CLKM | A | XTAL CLKM pin | B1 |
| CLKP | A | XTAL CLKP pin | D1 |
| GPADC1 | A | GPADC input 1 | T4 |
| GPADC2 | A | GPADC input 2 | T3 |
| GPADC3 | A | GPADC input 3 | U2 |
| GPADC4 | A | GPADC input 4 | U3 |
| NRESET | A | NRESET input | U10 |
| OSC_CLK_OUT | A | Oscillator Clock output | F7 |
| RX1 | A | RX channel 1 | N1 |
| RX2 | A | RX channel 2 | L1 |
| RX3 | A | RX channel 3 | J1 |
| RX4 | A | RX channel 4 | G1 |
| TX1 ⁽¹⁾ | A | TX channel 1 | A3 |
| TX2 ⁽¹⁾ | A | TX channel 2 | A5 |
| TX3 ⁽¹⁾ | A | TX channel 3 | A7 |
| TX4 ⁽¹⁾ | A | TX channel 4 | A9 |
| VBGAP | A | BandGap reference pin | K3 |

(1) The AWRL6843 device has four transmitter antennas out of which any group of 3 transmitter antennas can be used (TX1, TX2, TX3), (TX1, TX2, TX4), (TX1, TX3, TX4) & (TX2, TX3, TX4).

Table 6-2. CAN Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|-------------------|---------|
| CAN_FD_B_rx | I | CAN Receive Data | U12 |
| CAN_FD_B_tx | O | CAN Transmit Data | R11 |
| CAN_FD_rx | I | CAN Receive Data | R10 |
| CAN_FD_tx | O | CAN Transmit Data | T10 |

Table 6-3. Clock Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|--|-------------------------|
| MCU_CLKOUT | O | MCU clock output | C16, N15, N17 |
| PMIC_CLKOUT | O | PMIC clock output | C17, N16 |
| RTC_CLK_in | I | RTC clock input . This is used as wakeup source for exiting from deep sleep. For more details, refer to the Technical Reference Manual . | B13, F16, N15, T15, U15 |

Table 6-4. EPWM Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|------------------|------------------------------|
| ePWMA | O | EPWM Output A | B15, B17, N16, T14, U12, U15 |
| ePWMB | O | EPWM Output B | A15, A16, N17, R11, T12, U16 |
| ePWMSYNCl | I | EPWM Sync Input | N16, P15, T15, U16 |
| ePWMSYNCO | O | EPWM Sync Output | N17, T15 |

Table 6-5. GPIO Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|------------------------------|----------|
| GPIO_0 | IO | General Purpose Input/Output | A15, U12 |
| GPIO_1 | IO | General Purpose Input/Output | B15, R11 |
| GPIO_2 | IO | General Purpose Input/Output | F16, P16 |
| GPIO_3 | IO | General Purpose Input/Output | R10, R16 |
| GPIO_4 | IO | General Purpose Input/Output | N15, N16 |
| GPIO_5 | IO | General Purpose Input/Output | N17, U16 |
| GPIO_6 | IO | General Purpose Input/Output | U13, U15 |
| GPIO_7 | IO | General Purpose Input/Output | C16, T11 |

Table 6-6. I2C Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|-------------|------------------------------|
| I2C_scl | IO | I2C Clock | A16, B12, C16, N16, P15, T10 |
| I2C_sda | IO | I2C Data | B11, B17, F16, N17, R10, R14 |

Table 6-7. JTAG Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|------------------|---------|
| TCK | I | JTAG Test Clock | T12 |
| TDI | I | Test Data Input | T14 |
| TDO | O | Test Data Out | T13 |
| TMS | I | Test Mode Select | T15 |

Table 6-8. LIN Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|-------------------|-----------------------------------|
| LIN_rx | I | LIN Receive Data | F16, P16, R10, R14, U13, U16 |
| LIN_tx | O | LIN Transmit Data | C16, C17, P15, R16, T10, T11, U15 |

Table 6-9. LVDS Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|-------------------------------|---------|
| LVDS_CLKM | O | Differential Clock | J17 |
| LVDS_CLKP | O | Differential Clock | H16 |
| LVDS_FRCLKM | O | Differential Frame Clock | K17 |
| LVDS_FRCLKP | O | Differential Frame Clock | L16 |
| LVDS_TXM0 | O | Differential Data Out - Lane0 | G17 |
| LVDS_TXP0 | O | Differential Data Out - Lane0 | G16 |

Table 6-9. LVDS Signal Descriptions (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|---------------------------------------|---------|
| LVDS_TXM1 | O | Differential Data Out - Lane1 | M17 |
| LVDS_TXP1 | O | Differential Data Out - Lane1 | M16 |
| LVDS_Valid | O | When high, indicating valid LVDS data | P16 |

Table 6-10. Power Supply Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|--------------|----------|---|---|
| VDD | PWR | 1.2V Core supply | E13, E14, F10, F11, F12, F13, F14, F9, G10, G11, G12, G13, G14, G9, H10, H11, H12, H13, H14, H9, T5, U5 |
| VDDA_10RF | PWR | 1.0V internal LDO output. | D5, D6, D7, K5 |
| VDDA_12RF | PWR | 1.2V RF Supply | D10, D8, D9 |
| VDDA_18BB | PWR | 1.8V analog supply | R1, R2 |
| VDDA_18VCO | PWR | 1.8V analog supply | G3 |
| VDD_SRAM | PWR | 1.2V SRAM supply | T9, U9 |
| VIN_18PM | PWR | 1.8V core supply | M4 |
| VIOIN | PWR | 1.8V / 3.3V IO supply | D17, T17, U6 |
| VIOIN_18 | PWR | 1.8V IO supply | F17, R17, U8 |
| VIOIN_18CLK | PWR | 1.8V analog supply | D3 |
| VIOIN_18LVDS | PWR | 1.8V supply for LVDS port | K16 |
| VNWA | PWR | 1.2V VNWA supply. Always connected to SRAM supply | T6 |
| VOUT_14APLL | PWR | 1.4V internal LDO output | H7 |
| VOUT_14SYNTH | PWR | 1.4V internal LDO output | F3 |
| VPP | PWR | Voltage supply for fuse chain | R4 |
| VSS | GND | Ground | A17, B16, D16, E10, E11, E12, E16, J10, J11, J12, J13, J14, J16, J9, K10, K11, K12, K13, K14, K7, K8, K9, L10, L11, L12, L13, L14, L7, L8, L9, M10, M11, M12, M13, M14, M7, M8, M9, N10, N11, N12, N13, N14, N7, N8, N9, T16, T7, T8, U17 |
| VSSA | GND | Ground | A1, A10, A2, A4, A6, A8, B10, B2, B3, B4, B5, B6, B7, B8, B9, C1, C2, D2, E1, E2, E7, E8, E9, F1, F2, F8, G2, G7, G8, H1, H2, H8, J2, J7, J8, K1, K2, K6, L2, L5, L6, M1, M2, M5, M6, N2, N5, N6, P1, P2, T1, T2, U1 |

Table 6-11. QSPI Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|-------------|---------|
| QSPI_clk | IO | QSPI Clock | B14 |

Table 6-11. QSPI Signal Descriptions (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|------------------|---------|
| QSPI_cs_n | O | QSPI Chip Select | A13 |
| QSPI_din | I | QSPI Data bit 1 | B13 |
| QSPI_dout | IO | QSPI Data bit 0 | A12 |
| QSPI_qdin0 | I | QSPI Data bit 2 | B12 |
| QSPI_qdin1 | I | QSPI Data bit 3 | B11 |

Table 6-12. RS232 Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|---------------------|---------|
| rs232_rx | I | RS232 Receive Data | R14 |
| rs232_tx | O | RS232 Transmit Data | P15 |

Table 6-13. SPIA Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|--------------------|---------------|
| SPIA_clk | IO | SPIA Clock | A16 |
| SPIA_cs0_n | IO | SPIA Chip Select 0 | B17 |
| SPIA_cs1_n | IO | SPIA Chip Select 1 | C17, F16, P16 |
| SPIA_miso | IO | SPIA MISO | B15 |
| SPIA_mosi | IO | SPIA MOSI | A15 |

Table 6-14. SPIB Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|--------------------|-------------------------|
| SPIB_clk | IO | SPIB Clock | A16, B14, N16, P16 |
| SPIB_cs0_n | IO | SPIB Chip Select 0 | A13, B17, N15, R16 |
| SPIB_cs1_n | IO | SPIB Chip Select 1 | N17, P15 |
| SPIB_miso | IO | SPIB MISO | B13, B15, C16, P16, R14 |
| SPIB_mosi | IO | SPIB MOSI | A12, A15, N17 |

On SPIB only certain IOSET combinations are supported due to timing constraints. [Table 6-15](#) lists the valid IOSET combinations for SPIB

Table 6-15. Valid IOSET Combinations for SPIB Signal

| Signal Name | IOSET1 | IOSET2 | IOSET3 | IOSET4 |
|-------------|--------|--------|--------|--------|
| SPIB_clk | PAD_AA | PAD_AG | PAD_BC | PAD_BC |
| SPIB_cs0_n | PAD_AB | PAD_AH | PAD_BB | PAD_BB |
| SPIB_mosi | PAD_AC | PAD_AI | PAD_BD | PAD_BD |
| SPIB_miso | PAD_AD | PAD_AJ | PAD_BA | PAD_AX |

Table 6-16. System Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|--------------|----------|--|----------|
| HOST_CLK_req | O | Host clock request output. This signal provides an indication to external MCU/host to provide a clock through the CLKP pin. This signal is used in external clock mode. Please refer to Input Clocks and Oscillators for more details. | C16 |
| nERROR_OUT | O | nERROR output signal. Open drain fail safe output signal. This is used to indicate some severe criticality fault has happened. Recovery would be through reset. | N15, P16 |

Table 6-16. System Signal Descriptions (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|---------------------|----------|--|-------------------------|
| PRCM_PMIC_DeepSleep | O | Deep sleep indication output. This signal provides an indication of device's deepsleep state. | P16, T11 |
| SYNC_in | I | Sync input. This is used for synchronized frame triggering. For more details, refer to the Synchronized Frame Triggering | B11, N15, P16, R10, U16 |
| sys_reset_out | O | System reset indication output. This is used for indicating when SOC undergoes a reset. | F16, R11, R16, T15 |
| WU_reqin | I | Wakeup Request input. This is used as wakeup source for exiting from deep sleep. | B12, N15, R16, T10, U15 |

Table 6-17. UARTA Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|---------------------|----------|
| UARTA_rts | O | UARTA RTS output | U15 |
| UARTA_rx | I | UARTA Receive Data | N16, R10 |
| UARTA_tx | O | UARTA Transmit Data | N17, T10 |

Table 6-18. UARTB Signal Descriptions

| SIGNAL NAME | PIN TYPE | DESCRIPTION | BGA PIN |
|-------------|----------|---------------------|---------------|
| UARTB_rx | I | UARTB Receive Data | R10, R14, T11 |
| UARTB_tx | O | UARTB Transmit Data | P15, T10, U13 |

Table 6-19. DSS UARTA Signal Descriptions

| SIGNAL NAME | DESCRIPTION | PIN TYPE | BGA PIN |
|----------------|---|----------|---------------|
| HWASS_UARTA_RX | Debug UART instance in DSS. DSS UARTA Receive Data | I | U12, R14, R10 |
| HWASS_UARTA_TX | Debug UART instance in DSS. DSS UARTA Transmit Data | O | R11, P15, T10 |

Table 6-20. Pin Attributes

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | PULL UP/ DOWN TYPE ⁽⁸⁾ | BALL STATE DURING RST ⁽⁹⁾ | BALL RESET AFTER RST ⁽¹⁰⁾ |
|--------------------------------|--------------------------|------------------------------|---------------------------------|---|---------------------|---------------------|---|--|---|
| U12 | CAN_FD_B_rx | CAN_FD_B_rx | PADAY_CFG_REG | 0x5A00 0060 | 0 | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | HWASS_UARTA_rx | | | 1 | I | | | |
| | | ePWMA | | | 2 | O | | | |
| | | GPIO_0 | | | 3 | IO | | | |
| R11 | CAN_FD_B_tx | CAN_FD_B_tx | PADAZ_CFG_REG | 0x5A00 0064 | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | HWASS_UARTA_tx | | | 1 | O | | | |
| | | ePWMb | | | 2 | O | | | |
| | | GPIO_1 | | | 3 | IO | | | |
| | | sys_reset_out | | | 4 | O | | | |
| B1 | CLKM | CLKM | | | | A | | | |
| D1 | CLKP | CLKP | | | | A | | | |
| T4 | GPADC1 | GPADC1 | | | | A | | | |
| T3 | GPADC2 | GPADC2 | | | | A | | | |
| U2 | GPADC3 | GPADC3 | | | | A | | | |
| U3 | GPADC4 | GPADC4 | | | | A | | | |
| F16 | GPIO_2 | GPIO_2 | PADAL_CFG_REG | 0x5A00 002C | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | LIN_rx | | | 1 | I | | | |
| | | sys_reset_out | | | 2 | O | | | |
| | | I2C_sda | | | 3 | IO | | | |
| | | SPIA_cs1_n | | | 4 | IO | | | |
| | | RSVD | | | 5 | I | | | |
| | | RTC_CLK_in | | | 6 | I | | | |
| U16 | GPIO_5 | GPIO_5 | PADAV_CFG_REG | 0x5A00 0054 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | SYNC_in | | | 1 | I | | | |
| | | LIN_rx | | | 2 | I | | | |
| | | ePWMb | | | 3 | O | | | |
| | | ePWMSYNCl | | | 4 | I | | | |
| C16 | HOST_CLK_req | HOST_CLK_req ⁽¹²⁾ | PADAX_CFG_REG | 0x5A00 005C | 0 | O | PU/PD | Off / Off / Off | Off / SS / Off |
| | | GPIO_7 | | | 1 | IO | | | |
| | | MCU_CLKOUT ⁽¹²⁾ | | | 2 | O | | | |
| | | LIN_tx | | | 3 | O | | | |
| | | RSVD | | | 4 | I | | | |
| | | SPIB_miso | | | 5 | IO | | | |
| | | I2C_scl | | | 6 | IO | | | |
| N16 | I2C_scl | I2C_scl | PADBC_CFG_REG | 0x5A00 0070 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | PMIC_CLKOUT | | | 1 | O | | | |
| | | UARTA_rx | | | 2 | I | | | |
| | | GPIO_4 | | | 3 | IO | | | |
| | | RSVD | | | 4 | O | | | |
| | | ePWMA | | | 5 | O | | | |
| | | ePWMSYNCl | | | 6 | I | | | |
| | | SPIB_clk | | | 7 | IO | | | |
| N17 | I2C_sda | I2C_sda | PADBD_CFG_REG | 0x5A00 0074 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | MCU_CLKOUT | | | 1 | O | | | |
| | | UARTA_tx | | | 2 | O | | | |
| | | GPIO_5 | | | 3 | IO | | | |
| | | RSVD | | | 4 | O | | | |
| | | ePWMb | | | 5 | O | | | |
| | | ePWMSYNCO | | | 6 | O | | | |
| | | SPIB_cs1_n | | | 7 | IO | | | |
| | | SPIB_mosi | | | 8 | IO | | | |

Table 6-20. Pin Attributes (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | PULL UP/ DOWN TYPE ⁽⁸⁾ | BALL STATE DURING RST ⁽⁹⁾ | BALL RESET AFTER RST ⁽¹⁰⁾ |
|--------------------------------|--------------------------|-----------------------------|---------------------------------|---|---------------------|---------------------|---|--|---|
| U13 | LIN_rx | LIN_rx | PADBE_CFG_REG | 0x5A00 0078 | 0 | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | UARTB_tx | | | 1 | O | | | |
| | | GPIO_6 | | | 2 | IO | | | |
| T11 | LIN_tx | LIN_tx | PADBF_CFG_REG | 0x5A00 007C | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | UARTB_rx | | | 1 | I | | | |
| | | GPIO_7 | | | 2 | IO | | | |
| | | PRCM_PMIC_DeepSleep | | | 3 | O | | | |
| P16 | lvds_valid | LVDS_VALID | PADBA_CFG_REG | 0x5A00 0068 | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | nERROR_OUT | | | 1 | O | | | |
| | | LIN_rx | | | 2 | I | | | |
| | | GPIO_2 | | | 3 | IO | | | |
| | | RSVD | | | 4 | O | | | |
| | | SPIA_cs1_n | | | 5 | IO | | | |
| | | SPIB_miso | | | 6 | IO | | | |
| | | SPIB_clk | | | 7 | IO | | | |
| | | SYNC_in | | | 8 | I | | | |
| | | PRCM_PMIC_DeepSleep | | | 9 | O | | | |
| N15 | nERROR_OUT | nERROR_OUT | PADAU_CFG_REG | 0x5A00 0050 | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | GPIO_4 | | | 1 | IO | | | |
| | | SYNC_in | | | 2 | I | | | |
| | | SPIB_cs0_n | | | 3 | IO | | | |
| | | WU_reqin | | | 4 | I | | | |
| | | RTC_CLK_in | | | 5 | I | | | |
| | | MCU_CLKOUT | | | 6 | O | | | |
| U10 | NRESET | NRESET | | | | A | | | |
| F7 | OSC_CLK_OUT | OSC_CLK_OUT | | | | A | | | |
| C17 | PMIC_CLKOUT | SOP[1] | PADAK_CFG_REG | 0x5A00 0028 | During Power-Up | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | PMIC_CLKOUT ⁽¹²⁾ | | | 0 | O | | | |
| | | LIN_tx | | | 1 | O | | | |
| | | SPIA_cs1_n | | | 2 | IO | | | |
| B14 | QSPI_clk | QSPI_clk | PADAA_CFG_REG | 0x5A00 0000 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | SPIB_clk | | | 1 | IO | | | |
| A13 | QSPI_cs_n | QSPI_cs_n | PADAB_CFG_REG | 0x5A00 0004 | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | SPIB_cs0_n | | | 1 | IO | | | |
| B13 | QSPI_din | QSPI_din | PADAD_CFG_REG | 0x5A00 000C | 0 | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | SPIB_miso | | | 1 | IO | | | |
| | | RTC_CLK_in | | | 2 | I | | | |
| A12 | QSPI_dout | QSPI_dout | PADAC_CFG_REG | 0x5A00 0008 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | SPIB_mosi | | | 1 | IO | | | |
| B12 | QSPI_qdin0 | QSPI_qdin0 | PADAE_CFG_REG | 0x5A00 0010 | 0 | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | I2C_scl | | | 1 | IO | | | |
| | | WU_reqin | | | 2 | I | | | |
| B11 | QSPI_qdin1 | QSPI_qdin1 | PADAF_CFG_REG | 0x5A00 0014 | 0 | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | I2C_sda | | | 1 | IO | | | |
| | | SYNC_in | | | 2 | I | | | |
| R14 | rs232_rx | rs232_rx | PADAP_CFG_REG | 0x5A00 003C | 0 | I | PU/PD | Off / Off / Up | On / Off / Up |
| | | I2C_sda | | | 1 | IO | | | |
| | | UARTB_rx | | | 2 | I | | | |
| | | LIN_rx | | | 3 | I | | | |
| | | RSVD | | | 4 | O | | | |
| | | SPIB_miso | | | 5 | IO | | | |
| | | HWASS_UARTA_rx | | | 6 | I | | | |

Table 6-20. Pin Attributes (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | PULL UP/ DOWN TYPE ⁽⁸⁾ | BALL STATE DURING RST ⁽⁹⁾ | BALL RESET AFTER RST ⁽¹⁰⁾ |
|--------------------------------|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|---|--|---|
| P15 | rs232_tx | rs232_tx | PADA0_CFG_REG | 0x5A00 0038 | 0 | O | PU/PD | Off / Off / Off | Off / SS / Off |
| | | I2C_scl | | | 1 | IO | | | |
| | | UARTB_tx | | | 2 | O | | | |
| | | LIN_tx | | | 3 | O | | | |
| | | ePWMSYNCl | | | 4 | I | | | |
| | | RSVD | | | 5 | O | | | |
| | | SPIB_cs1_n | | | 6 | IO | | | |
| | | HWASS_UARTA_tx | | | 7 | O | | | |
| N1 | RX1 | RX1 | | | | A | | | |
| L1 | RX2 | RX2 | | | | A | | | |
| J1 | RX3 | RX3 | | | | A | | | |
| G1 | RX4 | RX4 | | | | A | | | |
| A16 | SPIA_clk | SPIA_clk | PADAG_CFG_REG | 0x5A00 0018 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | ePWMb | | | 1 | O | | | |
| | | I2C_scl | | | 2 | IO | | | |
| | | SPIB_clk | | | 3 | IO | | | |
| B17 | SPIA_cs0_n | SPIA_cs0_n | PADAH_CFG_REG | 0x5A00 001C | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | ePWMa | | | 1 | O | | | |
| | | I2C_sda | | | 2 | IO | | | |
| | | SPIB_cs0_n | | | 3 | IO | | | |
| B15 | SPIA_miso | SPIA_miso | PADAJ_CFG_REG | 0x5A00 0024 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | GPIO_1 | | | 1 | IO | | | |
| | | ePWMa | | | 2 | O | | | |
| | | SPIB_miso | | | 3 | IO | | | |
| A15 | SPIA_mosi | SPIA_mosi | PADAI_CFG_REG | 0x5A00 0020 | 0 | IO | PU/PD | Off / Off / Off | Off / Off / Off |
| | | GPIO_0 | | | 1 | IO | | | |
| | | ePWMb | | | 2 | O | | | |
| | | SPIB_mosi | | | 3 | IO | | | |
| | | RSVD | | | 4 | O | | | |
| | | LVDS_VALID | | | 5 | O | | | |
| R16 | sys_reset_out | sys_reset_out | PADBB_CFG_REG | 0x5A00 006C | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | WU_reqin | | | 1 | I | | | |
| | | LIN_tx | | | 2 | O | | | |
| | | GPIO_3 | | | 3 | IO | | | |
| | | RSVD | | | 4 | O | | | |
| | | SPIB_cs0_n | | | 5 | IO | | | |
| T12 | TCK | TCK | PADAT_CFG_REG | 0x5A00 004C | 0 | I | PU/PD | Off / Off / Down | On / Off / Down |
| | | ePWMb | | | 1 | O | | | |
| T14 | TDI | TDI | PADAR_CFG_REG | 0x5A00 0044 | 0 | I | PU/PD | Off / Off / Down | On / Off / Down |
| | | ePWMa | | | 1 | O | | | |
| T13 | TDO | SOP[0] | PADAS_CFG_REG | 0x5A00 0048 | During Power-Up | I | PU/PD | Off / Off / Off | Off / SS / Off |
| | | TDO | | | 0 | O | | | |
| T15 | TMS | TMS | PADAQ_CFG_REG | 0x5A00 0040 | 0 | I | PU/PD | Off / Off / Up | On / Off / Up |
| | | sys_reset_out | | | 1 | O | | | |
| | | RSVD | | | 2 | | | | |
| | | RSVD | | | 3 | | | | |
| | | RSVD | | | 4 | | | | |
| | | RSVD | | | 5 | | | | |
| | | RTC_CLK_in | | | 6 | I | | | |
| | | ePWMSYNCl | | | 7 | I | | | |
| | | ePWMSYNCO | | | 8 | O | | | |
| A3 | TX1 | TX1 | | | | A | | | |

Table 6-20. Pin Attributes (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | PULL UP/ DOWN TYPE ⁽⁸⁾ | BALL STATE DURING RST ⁽⁹⁾ | BALL RESET AFTER RST ⁽¹⁰⁾ |
|---|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|---|--|---|
| A5 | TX2 | TX2 | | | | A | | | |
| A7 | TX3 | TX3 | | | | A | | | |
| A9 | TX4 | TX4 | | | | A | | | |
| U15 | UARTA_rts | UARTA_rts | PADAW_CFG_REG | 0x5A00 0058 | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | GPIO_6 | | | 1 | IO | | | |
| | | LIN_tx | | | 2 | O | | | |
| | | RSVD | | | 3 | | | | |
| | | WU_reqin | | | 4 | I | | | |
| | | ePWMa | | | 5 | O | | | |
| | | RTC_CLK_in | | | 6 | I | | | |
| R10 | UARTA_rx | UARTA_rx | PADAM_CFG_REG | 0x5A00 0030 | 0 | I | PU/PD | Off / Off / Off | Off / Off / Off |
| | | GPIO_3 | | | 1 | IO | | | |
| | | LIN_rx | | | 2 | I | | | |
| | | CAN_FD_rx | | | 3 | I | | | |
| | | SYNC_in | | | 4 | I | | | |
| | | UARTB_rx | | | 5 | I | | | |
| | | I2C_sda | | | 6 | IO | | | |
| | | RSVD | | | 7 | O | | | |
| | | HWASS_UARTA_rx | | | 8 | I | | | |
| T10 | UARTA_tx | UARTA_tx | PADAN_CFG_REG | 0x5A00 0034 | 0 | O | PU/PD | Off / Off / Off | Off / Off / Off |
| | | LIN_tx | | | 1 | O | | | |
| | | CAN_FD_tx | | | 2 | O | | | |
| | | RSVD | | | 3 | | | | |
| | | WU_reqin | | | 4 | I | | | |
| | | UARTB_tx | | | 5 | O | | | |
| | | I2C_scl | | | 6 | IO | | | |
| | | RSVD | | | 7 | O | | | |
| | | HWASS_UARTA_tx | | | 8 | O | | | |
| K3 | VBGAP | VBGAP | | | | A | | | |
| E13, E14, F10, F11, F12, F13, F14, F9, G10, G11, G12, G13, G14, G9, H10, H11, H12, H13, H14, H9, T5, U5 | VDD | VDD | | | | PWR | | | |
| D5, D6, D7, K5 | VDDA_10RF | VDDA_10RF | | | | PWR | | | |
| D10, D8, D9 | VDDA_12RF | VDDA_12RF | | | | PWR | | | |
| R1, R2 | VDDA_18BB | VDDA_18BB | | | | PWR | | | |
| G3 | VDDA_18VCO | VDDA_18VCO | | | | PWR | | | |
| T9, U9 | VDD_SRAM | VDD_SRAM | | | | PWR | | | |
| M4 | VIN_18PM | VIN_18PM | | | | PWR | | | |
| D17, T17, U6 | VIOIN | VIOIN | | | | PWR | | | |
| F17, R17, U8 | VIOIN_18 | VIOIN_18 | | | | PWR | | | |
| D3 | VIOIN_18CLK | VIOIN_18CLK | | | | PWR | | | |
| K16 | VIOIN_18LVDS | VIOIN_18LVDS | | | | PWR | | | |
| T6 | VNWA | VNWA | | | | PWR | | | |
| H7 | VOOUT_14APLL | VOOUT_14APLL | | | | PWR | | | |
| F3 | VOOUT_14SYNTH | VOOUT_14SYNTH | | | | PWR | | | |
| R4 | VPP | VPP | | | | PWR | | | |

Table 6-20. Pin Attributes (continued)

| BGA BALL NUMBER ⁽¹⁾ | BALL NAME ⁽²⁾ | SIGNAL NAME ⁽³⁾ | PINCNTL REGISTER ⁽⁴⁾ | PINCNTL REGISTER ADDRESS ⁽⁵⁾ (11) | MODE ⁽⁶⁾ | TYPE ⁽⁷⁾ | PULL UP/ DOWN TYPE ⁽⁸⁾ | BALL STATE DURING RST ⁽⁹⁾ | BALL RESET AFTER RST ⁽¹⁰⁾ |
|--|--------------------------|----------------------------|---------------------------------|---|---------------------|---------------------|---|--|---|
| A17, B16, D16, E10, E11, E12, E16, J10, J11, J12, J13, J14, J16, J9, K10, K11, K12, K13, K14, K7, K8, K9, L10, L11, L12, L13, L14, L7, L8, L9, M10, M11, M12, M13, M14, M7, M8, M9, N10, N11, N12, N13, N14, N7, N8, N9, T16, T7, T8, U17 | VSS | VSS | | | | GND | | | |
| A1, A10, A2, A4, A6, A8, B10, B2, B3, B4, B5, B6, B7, B8, B9, C1, C2, D2, E1, E2, E7, E8, E9, F1, F2, F8, G2, G7, G8, H1, H2, H8, J2, J7, J8, K1, K2, K6, L2, L5, L6, M1, M2, M5, M6, N2, N5, N6, P1, P2, T1, T2, U1 | VSSA | VSSA | | | | GND | | | |

(1) **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.

(2) **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).

(3) **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

(4) **PINCNTL_REGISTER:** APPSS Register name for PinMux Control

(5) **PINCNTL ADDRESS:** APPSS Address for PinMux Control

(6) **MODE:** Multiplexing mode number: value written to PinMux Cntl register to select specific Signal name for this Ball number. Mode column has bit range value.

(7) **TYPE:** Signal type and direction:

- I = Input
- O = Output
- IO = Input or Output

(8) **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

- Pull Up: Internal pullup
- Pull Down: Internal pulldown
- An empty box means No pull.

(9) **BALL STATE DURING RST:** State of Ball during reset in the format of RX/TX/Pull Status

- RX (Input buffer)
 - Off: The input buffer is **disabled**.
 - On: The input buffer is **enabled**.
- TX (Output buffer)
 - Off: The output buffer is **disabled**.
 - Low: The output buffer is **enabled** and drives V_{OL} .
- Pull Status (Internal pull resistors)
 - Off: Internal pull resistors are turned **off**.
 - Up: Internal **pull-up** resistor is turned on.
 - Down: Internal **pull-down** resistor is turned on.
 - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

(10) **BALL STATE AFTER RST:** State of Ball after reset in the format of RX/TX/Pull Status

- RX (Input buffer)
 - Off: The input buffer is **disabled**.
 - On: The input buffer is **enabled**.
- TX (Output buffer)
 - Off: The output buffer is **disabled**.
 - SS: The subsystem selected with MUXMODE determines the output buffer state.
- Pull status (Internal pull resistors)
 - Off: Internal pull resistors are turned **off**.
 - Up: Internal **pull-up resistor** is turned on.
 - Down: Internal **pull-down resistor** is turned on.
 - NA: No internal pull resistor.
- An empty box, NA, or "-" means Not Applicable.

- (11) Pin Mux Control Value maps to lower 4 bits of register.
(12) Restricted use. Not available during deepsleep

7 Specifications

7.1 Absolute Maximum Ratings

| PARAMETERS ^{(1) (2)} | | MIN | MAX | UNIT |
|--------------------------------|--|--|-------------|------|
| VDD | 1.2V digital power supply | −0.5 | 1.4 | V |
| VIOIN | I/O supply (3.3V or 1.8V): All CMOS I/Os operate on the same VIOIN voltage level | −0.5 | 3.8 | V |
| VIOIN_18 | 1.8V supply for CMOS IO | −0.5 | 2 | V |
| VIOIN_18CLK | 1.8V supply for clock module | −0.5 | 2 | V |
| VDDA_18BB | 1.8V Analog baseband power supply | −0.5 | 2 | V |
| VDDA_18VCO | 1.8V RF VCO supply | −0.5 | 2 | V |
| VIOIN_18LVDS | 1.8V supply for LVDS port | −0.5 | 2 | V |
| VPP | Voltage supply for fuse chain | −0.5 | 2 | V |
| RX1-4 | Externally applied power on RF inputs | | 10 | dBm |
| TX1-4 | Externally applied power on RF outputs ⁽³⁾ | | 10 | dBm |
| Input and output voltage range | Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Steady State) | −0.3V | VIOIN + 0.3 | V |
| | Dual-voltage LVCMOS inputs, operated at 3.3 V/1.8 V (Transient Overshoot/Undershoot) or external oscillator input | VIOIN + 20% up to 20% of signal period | | |
| CLKP, CLKM | Input ports for reference crystal | −0.5 | 2 | V |
| Clamp current | Input or Output Voltages 0.3 V above or below their respective power rails. Limit clamp current that flows through the internal diode protection cells of the I/O. | −20 | 20 | mA |
| T _J | Operating junction temperature range | −40 | 140 | °C |
| T _{STG} | Storage temperature range after soldered onto PC board | −55 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to V_{SS}, unless otherwise noted.
- (3) This value is for an externally applied signal level on the TX. Additionally, a reflection coefficient up to $\Gamma = 1$ can be applied on the TX output.

7.2 ESD Ratings

| | | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------------|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AECQ100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins | ±750 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Power-On Hours (POH)

| JUNCTION TEMPERATURE (T _J) (1) | OPERATING CONDITION | NOMINAL CVDD VOLTAGE (V) | POWER-ON HOURS [POH] (HOURS) |
|---|---------------------|--------------------------|------------------------------|
| –40°C | 50% duty cycle | 1.2 | 1200 (6%) |
| 75°C | | | 4000 (20%) |
| 95°C | | | 13000 (65%) |
| 130°C | | | 1600 (8%) |
| 140°C | | | 200 (1%) |

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

7.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|--------------------|---|-------------|-----|-----------|------|
| VDD | 1.2V digital power supply | 1.14 | 1.2 | 1.26 | V |
| VIOIN | I/O supply (3.3V or 1.8V): All CMOS I/Os would operate on this supply. | 3.135 | 3.3 | 3.465 | V |
| | | 1.71 | 1.8 | 1.89 | |
| VIOIN_18 | 1.8V supply for CMOS IO | 1.71 | 1.8 | 1.89 | V |
| VIOIN_18CLK | 1.8V supply for clock module | 1.71 | 1.8 | 1.89 | V |
| VDDA_18BB | 1.8V Analog baseband power supply | 1.71 | 1.8 | 1.89 | V |
| VDDA_18VCO | 1.8V RF VCO supply | 1.71 | 1.8 | 1.89 | V |
| VIOIN_18LVDS | 1.8V supply for LVDS port | 1.71 | 1.8 | 1.89 | V |
| V _{IH} | Voltage Input High (1.8V mode) | 1.17 | | | V |
| | Voltage Input High (3.3V mode) | 2.25 | | | |
| V _{IL} | Voltage Input Low (1.8V mode) | | | 0.3*VIOIN | V |
| | Voltage Input Low (3.3V mode) | | | 0.62 | |
| V _{OH} | High-level output threshold (I _{OH} = 6 mA) | VIOIN – 450 | | | mV |
| V _{OL} | Low-level output threshold (I _{OL} = 6mA) | | | 450 | mV |
| NRESET SOP[1:0] | V _{IL} (1.8V Mode) | | | 0.2 | V |
| | V _{IH} (1.8V Mode) | 0.96 | | | |
| | V _{IL} (3.3V Mode) | | | 0.3 | |
| | V _{IH} (3.3V Mode) | 1.57 | | | |

7.5 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for secure boot devices. During the process of writing the customer specific keys or other fields like software version etc. in the efuse, the user needs to provide the VPP supply.

7.5.1 Recommended Operating Conditions for OTP eFuse Programming

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNIT |
|------------------------|--|------|--------------------|------|-------|
| VPP | Supply voltage range for the eFuse ROM domain during normal operation | | NC ⁽²⁾ | | |
| | Supply voltage range for the eFuse ROM domain during OTP programming ⁽¹⁾ | 1.65 | 1.7 | 1.75 | V |
| Duration of VPP Supply | If VPP voltage is supplied for more than recommended Hours, it can cause reliability issue | | | 24 | Hours |
| I(VPP) | | | | 50 | mA |
| Decoupling Capacitor | | | 0.1 ⁽³⁾ | | uF |

(1) During normal operation, no voltage should be applied to VPP. This can be typically achieved by disabling the external regulator attached to the VPP terminal.

(2) NC: No Connect

(3) Applicable to secure device variants. VPP pin can be floated for general purpose device variants.

Note

Power up sequence: VPP must be ramped up at the end i.e after all other rails ramp up is done

7.5.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.

7.5.3 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, in these cases of faulty EFUSE programmability, TI WILL HAVE NO LIABILITY.

7.6 Power Supply Specifications

7.6.1 3.3V I/O Topology

Table 7-1 describes the power rails from an external power supply block to the device via 3.3V I/O topology.

Table 7-1. Power Supply Rails Characteristics: 3.3V I/O Topology

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOs IN THE DEVICE |
|--------|---|--|
| 3.3V | Digital I/Os | Input: VIOIN |
| 1.8V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS | Input: VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIN_18PM, VIOIN_18LVDS LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.2V | Core Digital and SRAMs, RF, VNWA | Input: VDD, VNWA, VDD_SRAM, VDDA_12RF LDO Output: VDDA_10RF |

7.6.2 1.8V I/O Topology

Table 7-2 describes the power rails from an external power supply block to the device via 1.8V I/O topology.

Table 7-2. Power Supply Rails Characteristics: 1.8V I/O Topology

| SUPPLY | DEVICE BLOCKS POWERED FROM THE SUPPLY | RELEVANT IOs IN THE DEVICE |
|--------|---|---|
| 1.8 V | Synthesizer and APLL VCOs, crystal oscillator, IF Amplifier stages, ADC, LVDS | Input: VIOIN, VIN_18PM, VDDA_18VCO, VIOIN_18CLK, VDDA_18BB, VIOIN_18, VIOIN_18LVDS LDO Output: VOUT_14SYNTH, VOUT_14APLL |
| 1.2 V | Core Digital and SRAMs, RF, VNWA | Input: VDD, VDD_SRAM, VNWA, VDDA_12RF LDO Output: VDDA_10RF |

7.6.3 System Topologies

The following the system topologies are supported.

- Topology 1: Peripheral Mode, under the control of external MCU
- Topology 2: Autonomous mode, with connection to a remote host via LIN/CAN

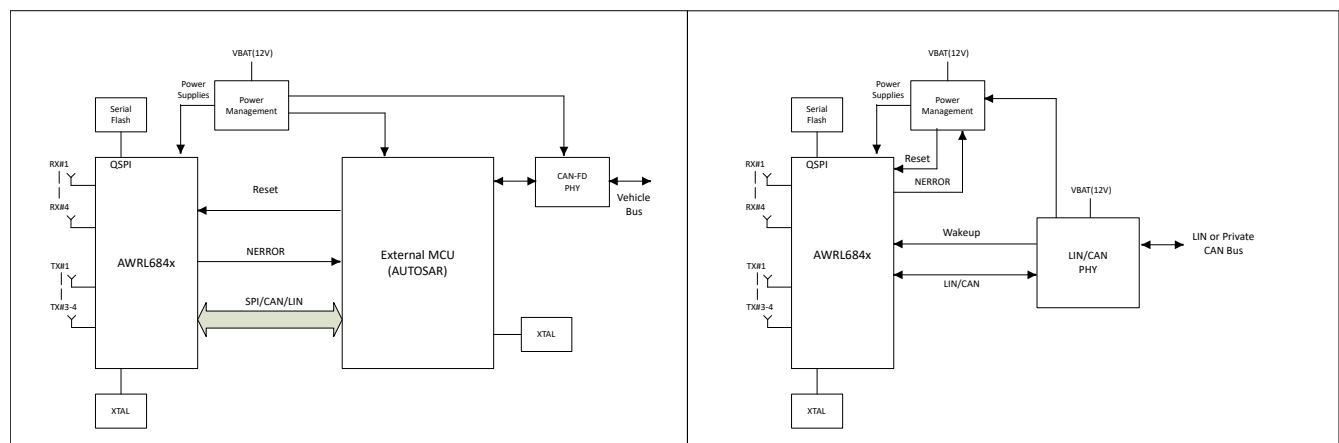


Figure 7-1. System Topologies (Left : Topology 1, Right : Topology 2)

In Topology 1: Peripheral mode, the AWRL684x is controlled by external MCU and most of the processing is done on *external* MCU. In this case, the computational and power requirements are relatively higher and the external MCU can stay active most of the time.

In Topology 2: Autonomous mode, the AWRL684x can be used as full sensor along with R5F application processor. In this case the internal application processor does all the processing and interrupts the host processor to communicate to take action based on the sensor data. Most of the processing happens on the

internal MCU of the AWRL684x chip and only high level desired results are communicated to external host via LIN/CAN.

7.6.3.1 I/O Topologies

The device can either be powered using two rails (1.8 V and 1.2 V) or with three rails (3.3 V, 1.8 V and 1.2 V).

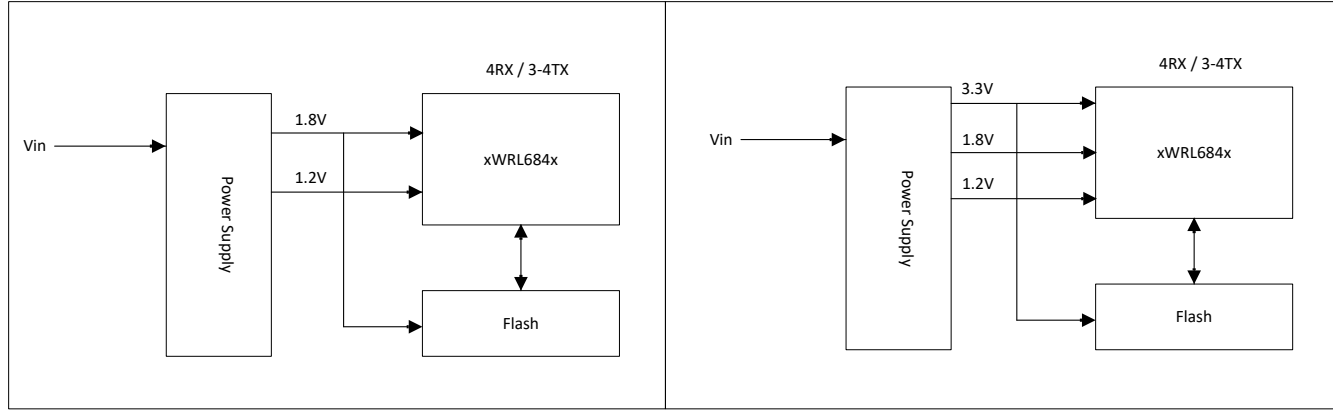


Figure 7-2. I/O Topologies (Left: 1.8V I/O Topology, Right: 3.3V I/O Topology)

7.6.4 RF Supply Decoupling Capacitor and Layout Conditions

This section depicts the recommended values of de-coupling capacitors and range of allowable parasitic inductance and resistance in particular sections of the RF Supplies(1.2V RF and 1V RF LDO). We recommended to use X7R type capacitors which has a lower variation across temperature. The minimum and maximum values of the capacitor captured in below table. The table includes variation of a given capacitor due to DC bias, tolerance and temperature variation.

Note

1. If the parasitic values are not kept within the specified range, performance of the device can degrade.
2. The working range of the chosen capacitor can not exceed the specified range.

7.6.4.1 1.2V RF Supply Rail

1.2V RF BGA pins require two decoupling capacitors with typical values of 22uF.

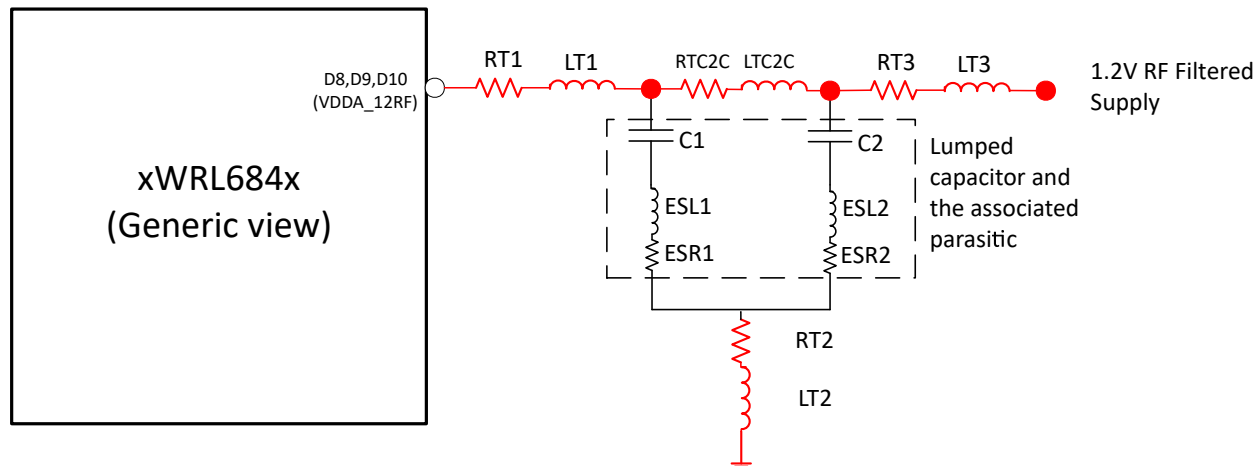


Figure 7-3. Parasitic offered by different portion of the input path for two capacitors

The parasitic offered by different portion of the output path is illustrated in Figure 7-3. As shown in figure, the output path can be divided into four portions:

Filtered Supply to second capacitor: “RT3” and “LT3” are the parasitic resistance and inductance offered by the 1.2V RF filtered supply to the second capacitor lead.

Along the second capacitor: “ESL2” and “ESR2” are the effective series inductance and resistance of the second decoupling capacitor. “RT2” and “LT2” are the ground trace resistance and inductance respectively of the second capacitor ground trace.

Second capacitor lead to first capacitor lead: “RTC2C” and “LTC2C” are the resistance and inductance of the trace between two capacitors.

Along the first capacitor: “ESL1” and “ESR1” are the effective series inductance and resistance of the first decoupling capacitor. “RT2” and “LT2” are the ground trace resistance and inductance respectively of the first capacitor ground trace.

First capacitor to Balls: “RT1” and “LT1” are the parasitic resistance and inductance offered by the the first capacitor lead to ball.

Note

Both 22uF capacitors are recommended to be placed close to the respective VDDA_12RF BGA ball.

7.6.4.1.1 1.2V RF Rail

Ball name: VDDA_12RF

Table 7-3. 1.2V RF Rail

| | | Min | Typ | Max | Unit |
|------------------------------|---|-----|---------------------|-----|------|
| Recommended value(s) of C | C1 | | 22.0 ⁽¹⁾ | | uF |
| | C2 | | 22.0 ⁽¹⁾ | | uF |
| Allowed parasitic inductance | 1 st Capacitor lead (LT1) to Ball | | | 0.8 | nH |
| | Along 1 st Capacitor (ESL1 + LT2) | | | 0.7 | |
| | Along the 2 nd Capacitor (ESL2 + LT2) | | | 0.7 | |
| | Between 2 nd Capacitor and filtered supply (LT3) | | | 1.0 | |

Table 7-3. 1.2V RF Rail (continued)

| | | Min | Typ | Max | Unit |
|------------------------------|---|-----|-----|------|------|
| Allowed parasitic resistance | 1 st Capacitor lead (RT1) to Ball | | | 1.5 | mOhm |
| | Along 1 st Capacitor (ESR1 + RT2) | | | 6.5 | |
| | Along the 2 nd Capacitor (ESR2 + RT2) | | | 6.5 | |
| | Between 2 nd Capacitor and filtered supply (RT3) | 2.0 | | 17.0 | |

(1) Capacitor is required to maintain capacitance between 10.5uF and 22.2uF at 1.2V DC bias across operating temperature range

Place two decoupling capacitors as close as possible to the VDDA_12RF BGA balls and position them adjacent to each other to minimize parasitics between two capacitor leads (RTC2C & LTC2C). The recommended decoupling capacitor placement relative to the BGA balls and to each other is illustrated in the [Figure 7-4](#). Refer to [Altium AWRL6844 EVM Design Files](#) for more details.

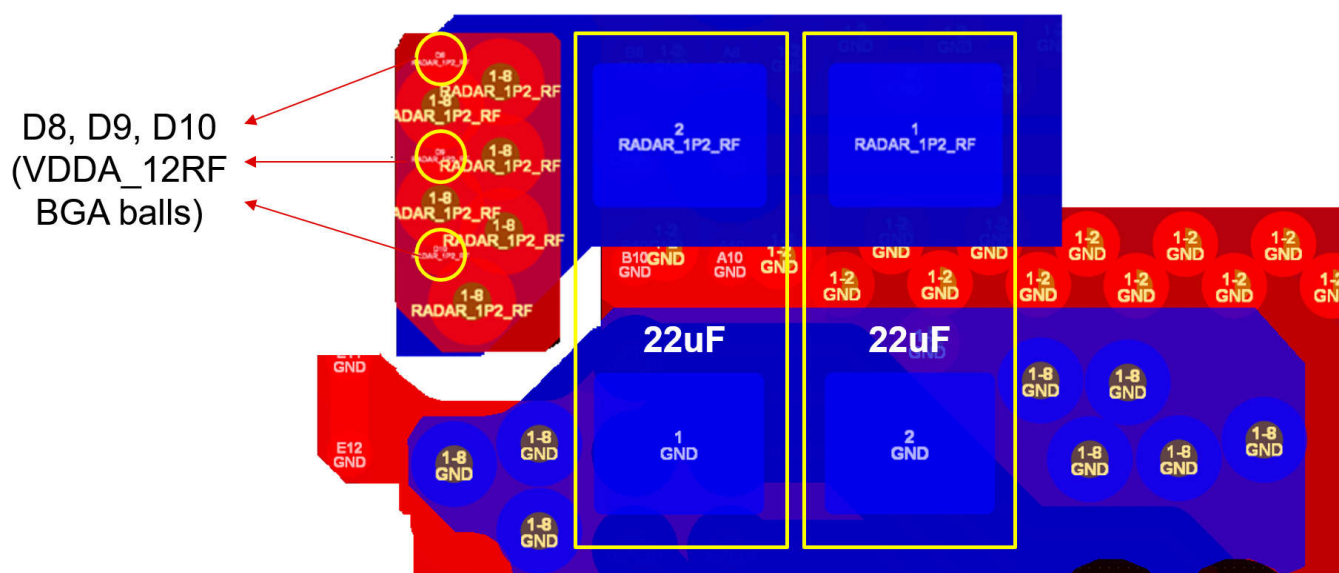


Figure 7-4. EVM Layout example

7.6.4.2 1.0V RF LDO

1.0V RF LDO require two decoupling capacitors with typical values of 10uF and 22uF.

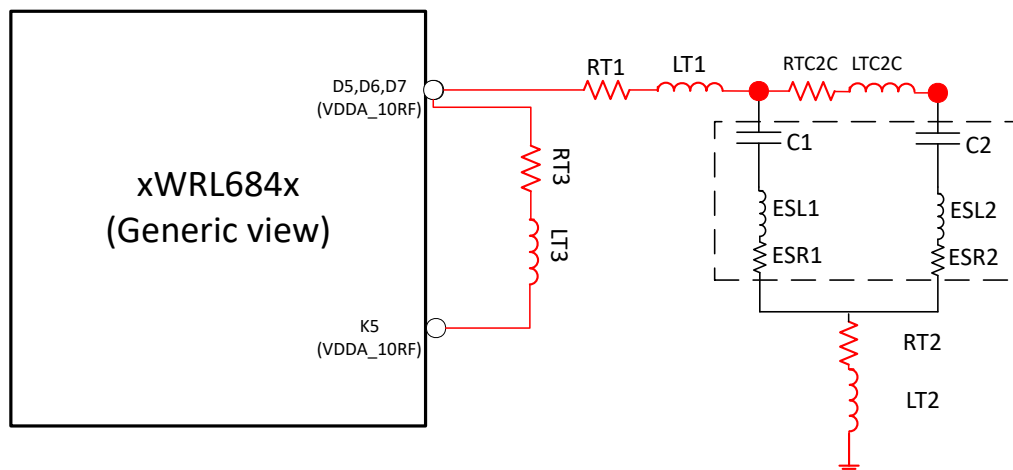


Figure 7-5. Parasitic offered by different portion of the output path for two capacitors

The parasitic offered by different portion of the output path is illustrated in Figure 7-5. As shown in figure, the output path can be divided into four portions:

Ball to first capacitor: “RT1” and “LT1” are the parasitic resistance and inductance offered by the ball to the first capacitor lead.

Along the first capacitor: “ESL1” and “ESR1” are the effective series inductance and resistance of the first decoupling capacitor. “RT2” and “LT2” are the ground trace resistance and inductance respectively of the first capacitor ground trace.

First capacitor lead to second capacitor lead: “RTC2C” and “LTC2C” are the resistance and inductance of the trace between two capacitors.

Along the second capacitor: “ESL2” and “ESR2” are the effective series inductance and resistance of the second decoupling capacitor. “RT2” and “LT2” are the ground trace resistance and inductance respectively of the second capacitor ground trace.

D5,D6 and D7 BGA balls to K5 BGA ball “RT3” and “LT3” are the parasitic resistance and inductance offered from D5,D6 and D7 BGA balls to K5 BGA ball.

Note

Recommended to avoid placing any capacitors on K5 ball.

Both the capacitors (10uF and 22uF) are recommended to be placed close to the respective VDDA_10RF BGA ball.

Place the output decoupling capacitors of 1.0V RF LDO on the same layer of PCB (either on top or on the bottom layer of PCB).

7.6.4.2.1 1.0V RF LDO

Ball name: VDDA_10RF

Table 7-4. 1.0V RF LDO Output

| | | Min | Typ | Max | Unit |
|------------------------------|----|-----|---------------------|-----|------|
| Recommended value(s) of C | C1 | | 22.0 ⁽¹⁾ | | uF |
| | C2 | | 10.0 ⁽²⁾ | | uF |

Table 7-4. 1.0V RF LDO Output (continued)

| | | Min | Typ | Max | Unit |
|------------------------------|---|-----|-----|-----|------|
| Allowed parasitic inductance | Ball to 1 st Capacitor lead (LT1) + Along 1 st Capacitor (ESL1 + LT2) | 1.1 | | 2.3 | nH |
| | Ball to 1 st Capacitor lead (LT1) + Along the 2 nd Capacitor (ESL2 + LT2) | 1.1 | | 2.3 | |
| | From D5, D6, D7 BGA balls to K5 BGA ball | | | 0.1 | |
| Allowed parasitic resistance | Ball to 1 st Capacitor lead (RT1) + Along 1 st Capacitor (ESR1 + RT2) | 4.5 | | 8.5 | mOhm |
| | Ball to 1 st Capacitor lead (RT1) + Along the 2 nd Capacitor (ESR2 + RT2) | 4.5 | | 8.5 | |
| | From D5, D6, D7 BGA balls to K5 BGA ball | | | 50 | |

- (1) Capacitor is required to maintain capacitance between 10.8uF and 22.9uF at 1.0V DC bias across operating temperature range
(2) Capacitor is required to maintain capacitance between 4.5uF and 9.9uF at 1.0V DC bias across operating temperature range

Place two decoupling capacitors as close as possible to the VDDA_10RF BGA balls and position them adjacent to each other to minimize parasitics between two capacitor leads (RTC2C & LTC2C). The recommended decoupling capacitor placement relative to the BGA balls and to each other is illustrated in the [Figure 7-6](#). Refer to [Altium AWRL6844 EVM Design Files](#) for more details.

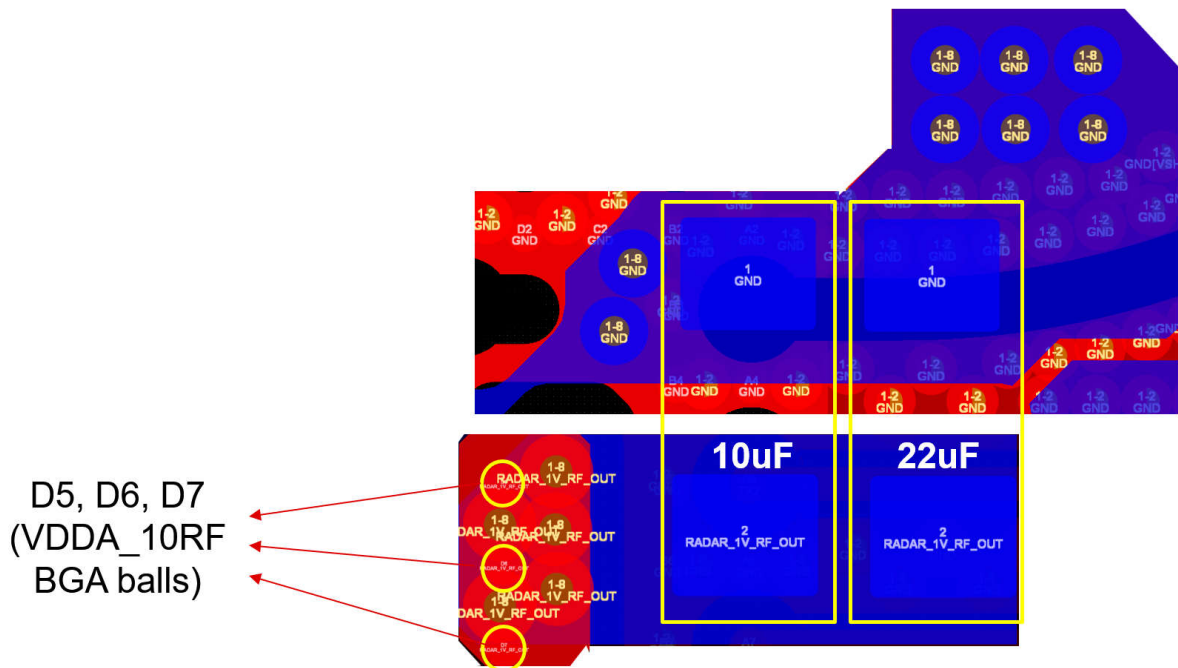


Figure 7-6. EVM Layout Example

Connect D5, D6 and D7 VDDA10_RFR BGA balls to K5 VDDA10_RF BGA ball using a wider copper plane. An example of the recommended layout illustrated in the [Figure 7-7](#). Refer to [Altium AWRL6844 EVM Design Files](#) for more details.

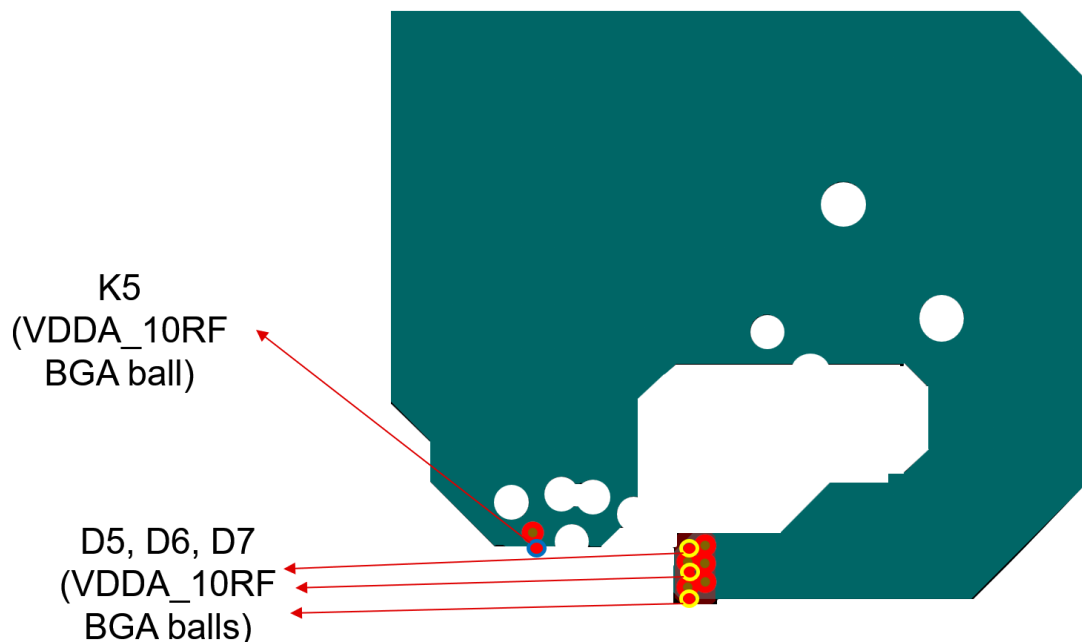


Figure 7-7. EVM Layout Example

7.6.5 Noise and Ripple Specifications

The 1.8V power supply ripple specifications mentioned in Table 7-5 are defined to meet a target spur level of -105dBc (RF Pin = -15dBm) at the RX. The spur and ripple levels have a dB-to-dB relationship, for example, a 1dB increase in supply ripple leads to a $\approx 1\text{dB}$ increase in spur level. Values quoted are peak-peak levels for a sinusoidal input applied at the specified frequency. These values are being optimized and are subject to change.

Table 7-5. Noise and Ripple Specifications

| FREQ (kHz) | NOISE SPECIFICATION | | RIPPLE SPECIFICATION | |
|------------|---|---|----------------------|-------------|
| | 1.8V ($\mu\text{V}/\sqrt{\text{Hz}}$) | 1.2V ($\mu\text{V}/\sqrt{\text{Hz}}$) | 1.8V (mVpp) | 1.2V (mVpp) |
| 10 | 6.057 | 44.987 | 0.035 | 1.996 |
| 100 | 2.677 | 26.801 | 0.760 | 2.233 |
| 200 | 2.388 | 28.393 | 0.955 | 3.116 |
| 500 | 0.757 | 9.559 | 0.504 | 1.152 |
| 1000 | 0.419 | 1.182 | 0.379 | 0.532 |
| 2000 | 0.179 | 1.256 | 0.153 | 0.561 |
| 5000 | 0.0798 | 0.667 | 0.079 | 0.297 |
| 10000 | 0.0178 | 0.104 | 0.017 | 0.046 |

7.7 Power Save Modes

Table 7-6 lists the supported power states.

Table 7-6. Device Power States

| Power State | Details |
|-------------|---|
| Active | Active Power State is when RF/chirping activity is ongoing |
| Processing | Processing Power State is when data is being processed and RF turned off ⁽¹⁾ |
| Idle | Idle Power State is during inter-frame/inter-burst/inter-chirp idle time |

Table 7-6. Device Power States (continued)

| Power State | Details |
|-------------|--|
| Deep Sleep | Lowest possible power state of the device where the critical contents of the device can be retained (Application Image, Chirp Profile etc) without needing device reboot. Device can enter this state after the frame processing is complete in order to save power significantly. Deep sleep exit can be through a number of external wakeup sources and internal timing maintenance. |

(1) The power consumed here also includes the Hardware Accelerator Power Consumption.

7.7.1 Typical Power Consumption Numbers

[Table 7-7](#) and [Table 7-8](#) lists the typical power consumption in different power topologies for each power save modes for a nominal device at 25C ambient temperature and nominal voltage conditions with all the I/Os parked properly.

[Table 7-9](#) and [Table 7-10](#) lists the typical use case power consumption in different power topologies for a nominal device at 25C ambient temperature and nominal voltage conditions with all the I/Os parked properly.

Table 7-7. Estimated Power Consumed in 3.3V I/O Topology

| Power Mode | | Power Consumption (mW) |
|--------------------|--|------------------------|
| Active (1Tx , 4Rx) | Average frequency = 60GHz, Tx backoff = 0dB, RX gain = 40dB, ADC Sampling rate: 25Msps, DSP is power gated, HWA and R5F are configured according to SDK Out-of-Box demo. | 1145 |
| Processing | LPDS is disabled, HWA at 200MHz running FFT similar to OOB , 32 chirps and 256 samples per chirp, R5F is processing the data at 200MHz (100% activity), DSP is Powered off | 335 |
| Idle | R5F running on 40Mhz (XTAL) in Wait For Interrupt , FECSS and DSS (DSP + HWA) are powered off | 28 |
| Deep sleep | All power domains are OFF except 32kHz time maintenance, Memory retained = 896KB | 4.04 |

Table 7-8. Estimated Power Consumed in 1.8V I/O Topology

| Power Mode | | Power Consumption (mW) |
|--------------------|--|------------------------|
| Active (1Tx , 4Rx) | Average frequency = 60GHz, Tx backoff = 0dB, RX gain = 40dB, ADC Sampling rate: 25Msps, DSP is power gated, HWA and R5F are configured according to SDK Out-of-Box demo. | 1145 |
| Processing | LPDS is disabled, HWA at 200MHz running FFT similar to OOB , 32 chirps and 256 samples per chirp, R5F is processing the data at 200MHz (100% activity), DSP is Powered off | 335 |
| Idle | R5F running on 40Mhz (XTAL) in Wait For Interrupt , FECSS and DSS (DSP + HWA) are powered off | 28 |

Table 7-8. Estimated Power Consumed in 1.8V I/O Topology (continued)

| Power Mode | | Power Consumption (mW) |
|------------|--|------------------------|
| Deep sleep | All power domains are OFF except 32kHz time maintenance, Memory retained = 896KB | 3.91 |

Table 7-9. Use-Case Power Consumed in 3.3V I/O Topology

| Parameter | | Condition | Typical (mW) |
|---|---|-----------------|--------------|
| Average Power Consumption (1% Duty Cycle) | RF Front End Configuration : Simultaneous 4TX and 4RX Start frequency = 58GHz Ramp End time = 22.7us Chirp Idle Time = 7us Number of chirps per burst = 48 Chirp accumulation = 2 Burst Periodicity = 3122us Number of bursts per frame = 1 Frame period = 200ms HWA and R5F are configured according to SDK Out-of-Box demo. DSP is powered OFF. Device configured to go to deep sleep state during available idle time. | 5Hz Update Rate | 36 |
| Average Power Consumption (0.1% Duty Cycle) | RF Front End Configuration : 1TX, 1RX Start frequency = 58GHz Ramp End time = 22.7us Chirp Idle Time = 7us Number of chirps per burst = 4 Chirp accumulation = 0 Burst Periodicity = 254us Number of bursts per frame = 3 Frame period = 250ms HWA and R5F are configured according to SDK Out-of-Box demo. DSP is powered OFF. Device configured to go to deep sleep state during available idle time. | 4Hz Update Rate | 13 |

Table 7-10. Use-Case Power Consumed in 1.8V I/O Topology

| Parameter | | Condition | Typical (mW) |
|---|---|-----------------|--------------|
| Average Power Consumption (1% Duty Cycle) | RF Front End Configuration : Simultaneous 4TX and 4RX Start frequency = 58GHz Ramp End time = 22.7us Chirp Idle Time = 7us Number of chirps per burst = 48 Chirp accumulation = 2 Burst Periodicity = 3122us Number of bursts per frame = 1 Frame period = 200ms HWA and R5F are configured according to SDK Out-of-Box demo. DSP is powered OFF. Device configured to go to deep sleep state during available idle time. | 5Hz Update Rate | 36 |

Table 7-10. Use-Case Power Consumed in 1.8V I/O Topology (continued)

| Parameter | Condition | Typical (mW) |
|---|---|--------------|
| Average Power Consumption (0.1% Duty Cycle) | RF Front End Configuration : 1TX, 1RX Start frequency = 58GHz Ramp End time = 22.7us Chirp Idle Time = 7us Number of chirps per burst = 4 Chirp accumulation = 0 Burst Periodicity = 254us Number of bursts per frame = 3 Frame period = 250ms HWA and R5F are configured according to SDK Out-of-Box demo. DSP is powered OFF. Device configured to go to deep sleep state during available idle time. | 13 |

7.8 Peak Current Requirement per Voltage Rail

Table 7-11 provides the max split rail current numbers.

Table 7-11. Maximum Peak Current per Voltage Rail

| I/O Voltage ⁽³⁾ | Maximum Current (mA) (1) (2) | | |
|----------------------------|--|--|--|
| | 1.2V: total current drawn by all nodes driven by 1.2V rail | 1.8V: total current drawn by all nodes driven by 1.8V rail | 3.3V: total current drawn by all nodes driven by 3.3V rail |
| 3.3V | 2560 | 200 | 100 |
| 1.8V | 2560 | 300 | NA |

- (1) Exercise full functionality of device, including 4TX, 4RX simultaneous operation, HWA, DSP, R5F and various host comm/interface peripherals active (CAN, LIN, I2C, GPADC), test across full temperature range
- (2) The specified current values are at typical supply voltage level.
- (3) The exact VIOIN current depends on the peripherals used and their frequency of operation.

7.9 RF Specification

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|-----------------|---|---------------|-----|-------|------|--------|
| Receiver | Noise figure | 57 to 63.9GHz | | 12.5 | | dB |
| | 1-dB compression point (Out Of Band) ⁽¹⁾ | | | -15 | | dBm |
| | Maximum gain | | | 46 | | dB |
| | Gain range | | | 10 | | dB |
| | Gain step size | | | 2 | | dB |
| | IF bandwidth ⁽²⁾ | | | | 10 | MHz |
| | ADC sampling rate (real) | | | | 25 | Msps |
| | ADC resolution | | | 12 | | Bits |
| Transmitter | S11 | | | -7 | | dB |
| | Output Power | | | 12.5 | | dBm |
| | Power backoff range | | | | 20 | dB |
| | Backoff step size | | | 1 | | dB |
| Clock subsystem | S11 | | | -7.5 | | dB |
| | Frequency range | | 57 | | 63.9 | GHz |
| | Ramp rate | | | | 400 | MHz/μs |
| | Phase noise at 1MHz offset | 57 to 63.9GHz | | -90.5 | | dBc/Hz |

(1) 1-dB Compression Point (Out Of Band) is measured by feed a Continuous wave Tone well below the lowest HPF cut-off frequency.

(2) The analog IF stages include high-pass filtering, with configurable first-order high-pass corner frequency. The set of available HPF corners is summarized as follows:

| |
|--|
| Available HPF Corner Frequencies (kHz) |
|--|

| |
|---------------------|
| 175, 350, 700, 1400 |
|---------------------|

The filtering performed by the digital baseband chain is targeted to provide less than ± 0.5 dB pass-band ripple/droop.

Figure 7-8 shows typical variations of noise figure and in-band P1dB parameters with respect to receiver gain programmed. This is small signal noise figure and applicable when the in-band RX ADC input is less than -2dBm (+/-8192 ADC codes in 16-bit mode). Users are recommended to operate within this level to avoid ADC saturation effects.

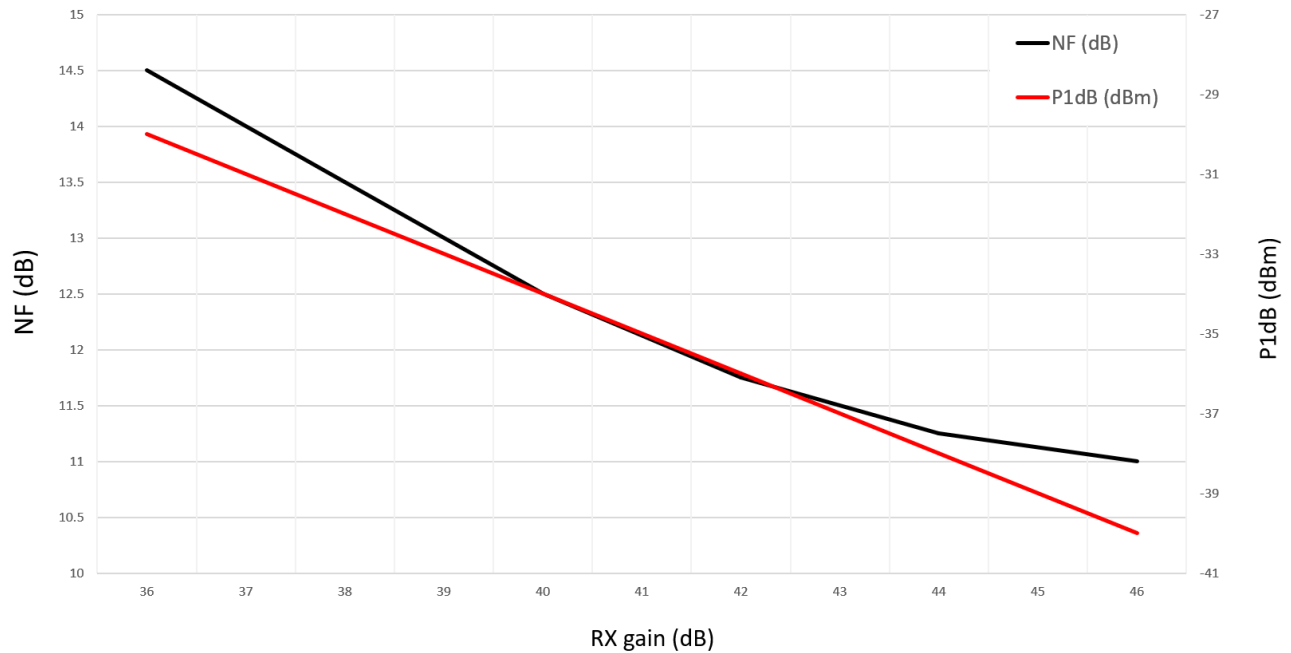


Figure 7-8. Noise Figure, In-band P1dB vs Receiver Gain

7.10 Supported DFE Features

- TX output back-off
 - From 0dB to 20dB TX back-off in steps of 1dB is supported
 - Binary Phase Modulation supported on each TX
- RX gain
 - Real only RX channels
 - Total RX gain range of 36dB to 46dB, in 2dB steps
- VCO
 - Single VCO covering entire RF sweep bandwidth up to 7GHz.
- High-pass filter
 - First-order high pass filter only. Supports corner frequency options 175kHz, 350kHz, 700 KHz, 1400kHz
- Low-pass filter
 - Max IF bandwidth supported is 10MHz
 - Two filtering options supported
 - 90% visibility – IF bandwidth is 90% of Nyquist (has longer settling time due to larger filter length)
 - 80% visibility – IF bandwidth is 80% of Nyquist and is 30% faster due to quicker settling time, compared with 90% visibility
- Supported ADC sampling rates
 - 2.0, 2.5, 3.334, 4.0, 5.0, 8.0, 10.0, 13.334, 15.384, 20.0, 25Msps
- Timing Engine
 - Support for chirps, bursts and frames
 - Longer frame idle time gives more power saving than a longer burst idle time. Further, a longer chirp idle time gives lesser power saving than a longer burst idle time. For more details please refer power calculator in the [mmWave sensing estimator](#).
 - Chirp accumulation (averaging) can be enabled when chirping in succession to reduce memory requirement and boost SNR.
 - Provision for per-chirp dithering of parameters
 - The AWRL684x device supports both TDM and BPM mode of operation.
 - Refer to [Figure 7-9](#) for chirp profile supported by timing engine.

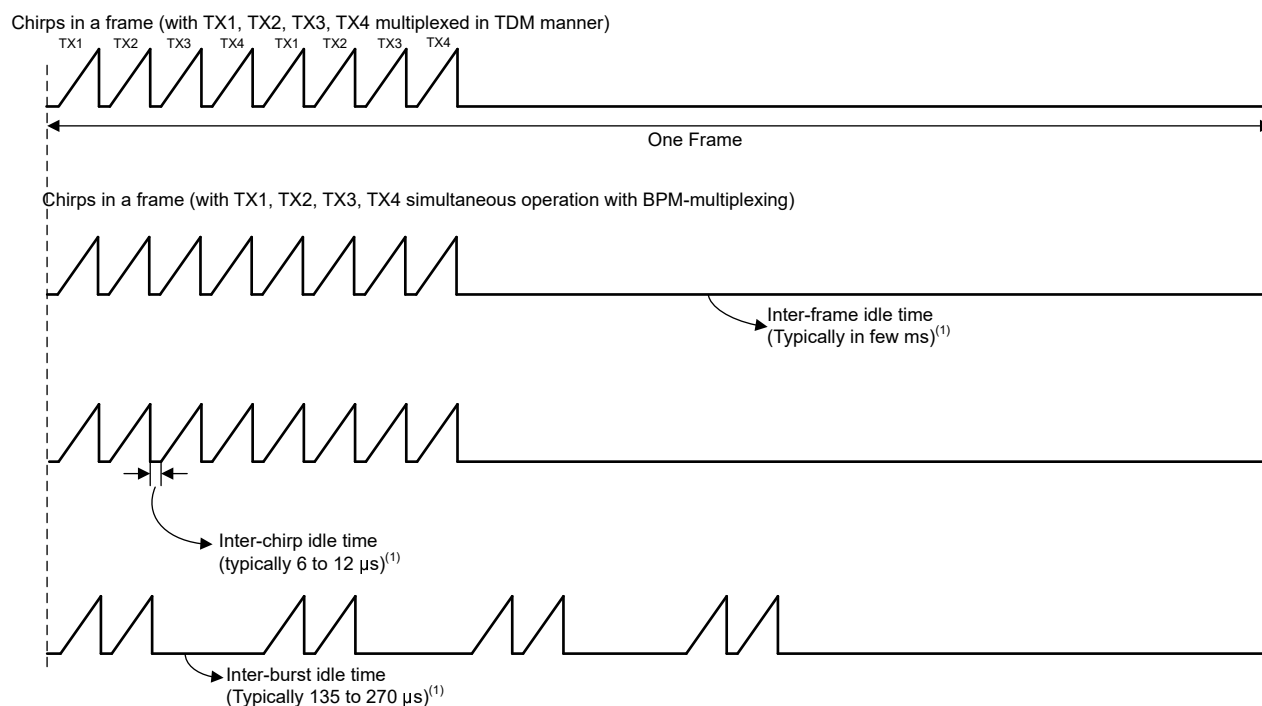


Figure 7-9. Chip Profile Supported by Timing Engine

1. Refer to ICD(Interface Control Document) available in [MMWAVE-L-SDK](#) for more details.

7.11 CPU Specifications

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TYP | UNIT |
|--|---|--------------------|------|
| DSP Subsystem (C66x Family) | Clock Speed | 450 | MHz |
| | L1 Memory | 64 | KB |
| | L2 Memory | 384 | KB |
| | L3 Memory dedicated for DSS | 512 ⁽¹⁾ | KB |
| Application Subsystem (R5F Family) | Clock Speed | 200 | MHz |
| | Tightly Coupled Memory - A (Program + Data) | 512 | KB |
| | Tightly Coupled Memory - B (Program + Data) | 256 | KB |
| Shared Memory | DSS L3 Shared Memory | 896KB | KB |

- (1) 512 KB of dedicated DSS L3 memory only available in AWRL6844

7.12 Thermal Resistance Characteristics

Table 7-12. Thermal Resistance Characteristics for FCCSP Package [ANC0207A]

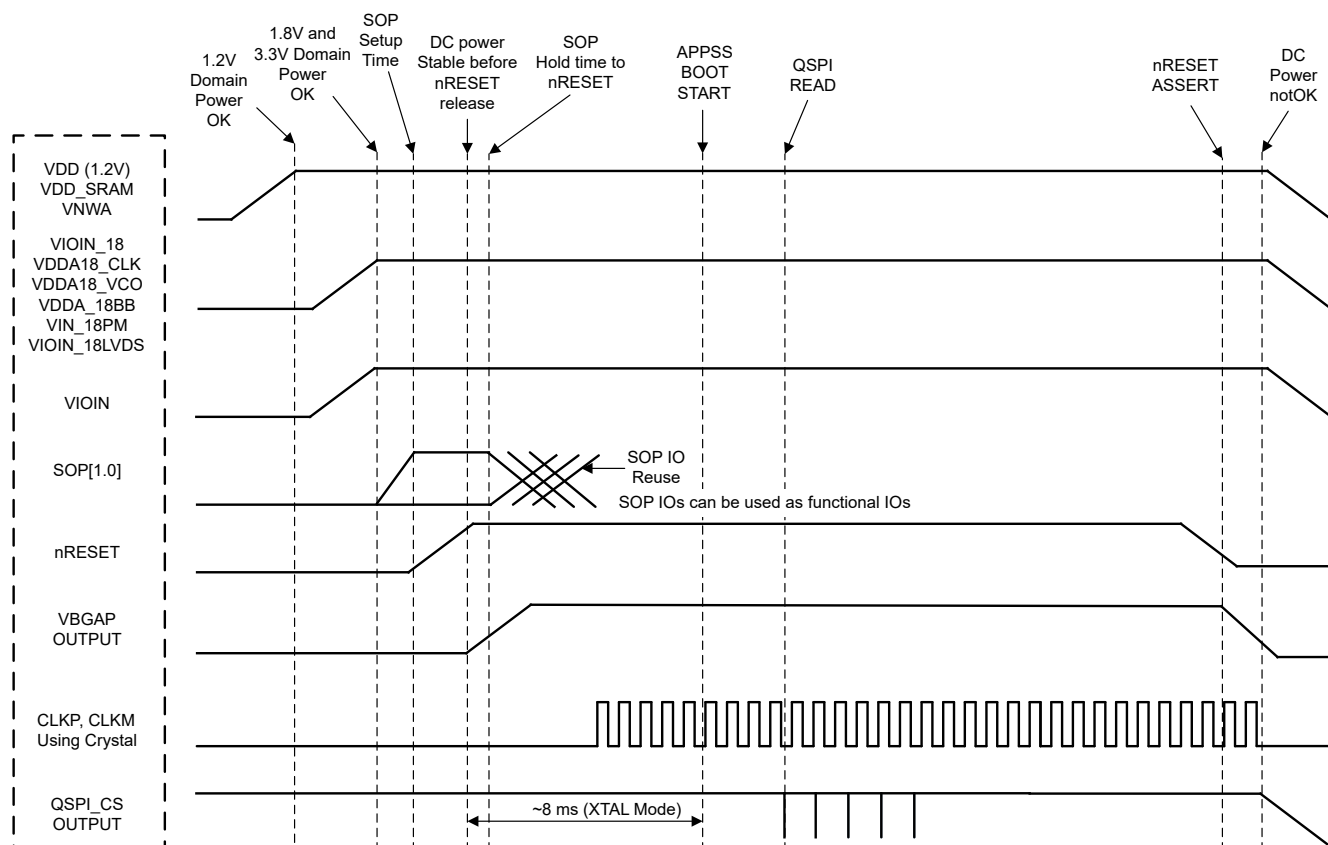
| THERMAL METRICS ⁽¹⁾ (4) | | °C/W ⁽²⁾ (3) |
|------------------------------------|-------------------------|-------------------------|
| RO _{JC} | Junction-to-case | 3.9 |
| RO _{JB} | Junction-to-board | 3.8 |
| RO _{JA} | Junction-to-free air | 19.2 |
| Psi _{JT} | Junction-to-package top | 0.1 |
| Psi _{JB} | Junction-to-board | 3.8 |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) °C/W = degrees Celsius per watt.
- (3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [RO_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
 - JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
 - JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 - JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*
- (4) Test Condition: Power=1.305W at 25°C

7.13 Timing and Switching Characteristics

7.13.1 Power Supply Sequencing and Reset Timing

The AWRL684x device expects all external voltage rails to be stable before reset is deasserted. [Figure 7-10](#) describes the device wake-up sequence.



A. Ensure that the 1.2V rail is ramped up and stable before 1.8V rail.

Figure 7-10. Device Wake-up Sequence

7.13.2 Synchronized Frame Triggering

The AWRL684x device supports a hardware based mechanism to trigger radar frames. An external host can pulse the SYNC_IN signal to start radar frames. The typical time difference between the rising edge of the external pulse and the frame transmission on air (T_{lag}) is about 160 ns. There is also an additional programmable delay that the user can set to control the frame start time. The periodicity of the external SYNC_IN pulse should be always greater than the programmed frame periodic in the frame configurations in all instances.

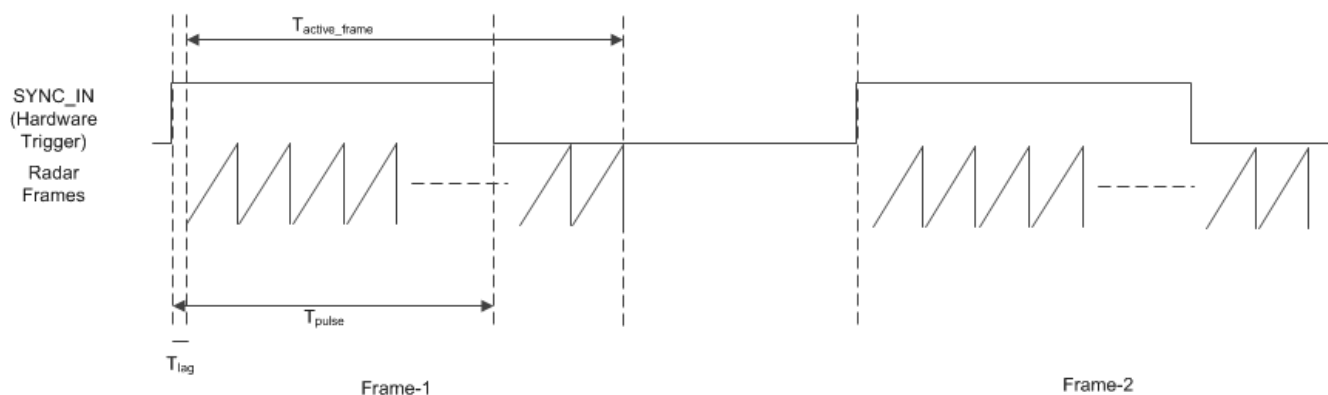


Figure 7-11. Sync In Hardware Trigger

Table 7-13. Frame Trigger Timing

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---------------------------|-----------------------|--------------|-------------------------------------|------|
| T _{active_frame} | Active frame duration | User defined | | ns |
| T _{pulse} | | 25 | < T _{active_frame} or 4000 | |

7.13.3 Input Clocks and Oscillators

7.13.3.1 Clock Specifications

The AWRL684x requires external clock source (that is, a 40MHz crystal or external oscillator to CLKP) for initial boot and as a reference for an internal APLL hosted in the device. An external crystal connected to the device pins [Figure 7-12](#) shows the crystal implementation.

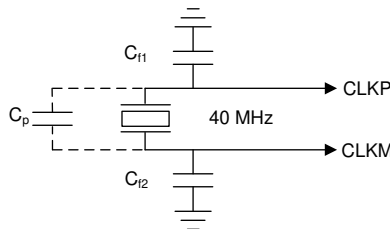


Figure 7-12. Crystal Implementation

Note

The load capacitors, C_{f1} and C_{f2} in [Figure 7-12](#), should be chosen such that [Equation 1](#) is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator CLKP and CLKM pins.

$$C_L = C_{f1} \times \frac{C_{f2}}{C_{f1} + C_{f2}} + C_P \quad (1)$$

[Table 7-14](#) lists the electrical characteristics of the clock crystal.

Table 7-14. Crystal Electrical Characteristics (Oscillator Mode)

| NAME | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---------------------|--|--------------------|-----|--------------------|------|
| f _p | Parallel resonance crystal frequency | | 40 | | MHz |
| C _L | Crystal load capacitance | 5 | 8 | 12 | pF |
| ESR | Crystal ESR | | | 50 | Ω |
| Temperature range | Expected temperature range of operation | –40 ⁽⁴⁾ | | 140 ⁽⁴⁾ | °C |
| Frequency tolerance | Crystal frequency tolerance ^{(1) (2) (3)} | –200 | | 200 | ppm |
| Drive level | | | 50 | 200 | μW |

(1) The crystal manufacturer's specification must satisfy this requirement.

(2) Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.

(3) Crystal tolerance affects radar sensor accuracy.

(4) This is subjected to system level requirements. AWRL684x can support operating junction temperature range of –40°C to 140°C

In the case where an external clock is used as the clock resource, the signal is fed to the CLKP pin only; CLKM is grounded. The phase noise requirement is very important when a 40MHz clock is fed externally. [Table 7-15](#) lists the electrical characteristics of the external clock signal.

Table 7-15. External Clock Mode Specifications

| PARAMETER | | SPECIFICATION | | | UNIT |
|--|-----------------------|---------------|-----|------|---------|
| | | MIN | TYP | MAX | |
| Input Clock: External AC-coupled sine wave or DC-coupled square wave Phase Noise referred to 40 MHz | Frequency | | 40 | | MHz |
| | AC-Amplitude | 700 | | 1200 | mV (pp) |
| | DCV _{il} | 0.00 | | 0.20 | V |
| | DCV _{ih} | 1.6 | | 1.95 | V |
| | Phase Noise at 1kHz | | | −132 | dBc/Hz |
| | Phase Noise at 10kHz | | | −143 | dBc/Hz |
| | Phase Noise at 100kHz | | | −152 | dBc/Hz |
| | Phase Noise at 1MHz | | | −153 | dBc/Hz |
| | Duty Cycle | 35 | | 65 | % |
| | Frequency Tolerance | −200 | | 200 | ppm |

7.13.4 MultiChannel buffered / Standard Serial Peripheral Interface (McSPI)

The McSPI module is a multichannel transmit/receive, controller/peripheral synchronous serial bus

7.13.4.1 McSPI Features

The McSPI modules include the following main features:

- Serial clock with programmable frequency, polarity, and phase for each channel
- Wide selection of SPI word lengths, ranging from 4 to 32 bits
- Up to four channels in controller mode, or single channel in receive mode
- Controller multichannel mode:
 - Full duplex/half duplex
 - Transmit-only/receive-only/transmit-and-receive modes
 - Flexible input/output (I/O) port controls per channel
 - Programmable clock granularity
 - Per channel configuration for clock definition, polarity enabling, and word width
- Single interrupt line for multiple interrupt source events
- Enable the addition of a programmable start-bit for McSPI transfer per channel (start-bit mode)
- Supports start-bit write command
- Supports start-bit pause and break sequence
- Programmable shift operations (1-32 bits)
- Programmable timing control between chip select and external clock generation
- Built-in FIFO available for a single channel

7.13.4.2 SPI Timing Conditions

Table 7-16 presents timing conditions for McSPI

Table 7-16. McSPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t _R | Input rise time | 1 | | 3 | ns |
| t _F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C _{LOAD} | Output load capacitance | 2 | | 15 | pF |

7.13.4.3 SPI—Controller Mode

7.13.4.3.1 Timing and Switching Requirements for SPI - Controller Mode

Table 7-17 and Table 7-17 present timing requirements for SPI - Controller Mode.

Table 7-17. SPI Timing Requirements - Controller Mode

| NO. ⁽¹⁾ | | | MODE | MIN | MAX | UNIT |
|--------------------|-------------------------------|--|------|-----|-----|------|
| SM4 | t _{su} (MISO-SPICLK) | Setup time, SPI_D[x] valid before SPI_CLK active edge ⁽¹⁾ | | 5 | | ns |
| SM5 | t _h (SPICLK-MISO) | Hold time, SPI_D[x] valid after SPI_CLK active edge ⁽¹⁾ | | 3 | | ns |

Table 7-18. SPI Switching Characteristics - Controller Mode

| NO. ⁽¹⁾ | | | MODE | MIN | MAX | UNIT |
|--------------------|------------------------------|---|------|---|-----|------|
| SM1 | t _c (SPICLK) | Cycle time, SPI_CLK ^{(1) (2)} | | 24.6 ⁽³⁾ | | ns |
| SM2 | t _w (SPICLKL) | Typical Pulse duration, SPI_CLK low ⁽¹⁾ | | -1 + 0.5P ⁽³⁾ ⁽⁴⁾ | | ns |
| SM3 | t _w (SPICLKH) | Typical Pulse duration, SPI_CLK high ⁽¹⁾ | | -1 + 0.5P ⁽⁴⁾ | | ns |
| SM6 | t _d (SPICLK-SIMO) | Delay time, SPI_CLK active edge to SPI_D[x] transition ⁽¹⁾ | | -2 | 5 | ns |

Table 7-18. SPI Switching Characteristics - Controller Mode (continued)

| NO. ⁽¹⁾ | | | MODE | MIN | MAX | UNIT |
|--------------------|-------------------|---|---|-----------------------|-----|------|
| SM7 | $t_{sk}(CS-SIMO)$ | Delay time, SPI_CS[x] active to SPI_D[x] transition | | 5 | | ns |
| SM8 | $t_d(SPICLK-CS)$ | Delay time, SPI_CS[x] active to SPI_CLK first edge | Controller_PHA0_POL 0; Controller_PHA0_POL 1; ⁽⁵⁾ | -4 + B ⁽⁶⁾ | | ns |
| | | | Controller_PHA1_POL 0; Controller_PHA1_POL 1; ⁽⁵⁾ | -4 + A ⁽⁷⁾ | | ns |
| SM9 | $t_d(SPICLK-CS)$ | Delay time, SPI_CLK last edge to SPI_CS[x] inactive | Controller_PHA0_POL 0; Controller_PHA0_POL 1; ⁽⁵⁾ | -4 + A ⁽⁷⁾ | | ns |
| | | | Controller_PHA1_POL 0; Controller_PHA1_POL 1; ⁽⁵⁾ | -4 + B ⁽⁶⁾ | | ns |
| SM11 | Cb | Capacitive load for each bus line | | 3 | 15 | pF |

- (1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data
- (2) Related to the SPI_CLK maximum frequency
- (3) 20 ns cycle time = 50 MHz
- (4) P = SPICLK period
- (5) SPI_CLK phase is programmable with the PHA bit of the SPI_CH(i)CONF register
- (6) $B = (TCS + .5) \times TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register and Fratio = Even ≥ 2 .
- (7) When $P = 20.8$ ns, $A = (TCS + 1) \times TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.
When $P > 20.8$ ns, $A = (TCS + 0.5) \times Fratio \times TSPICLKREF$, where TCS is a bit field of the SPI_CH(i)CONF register.

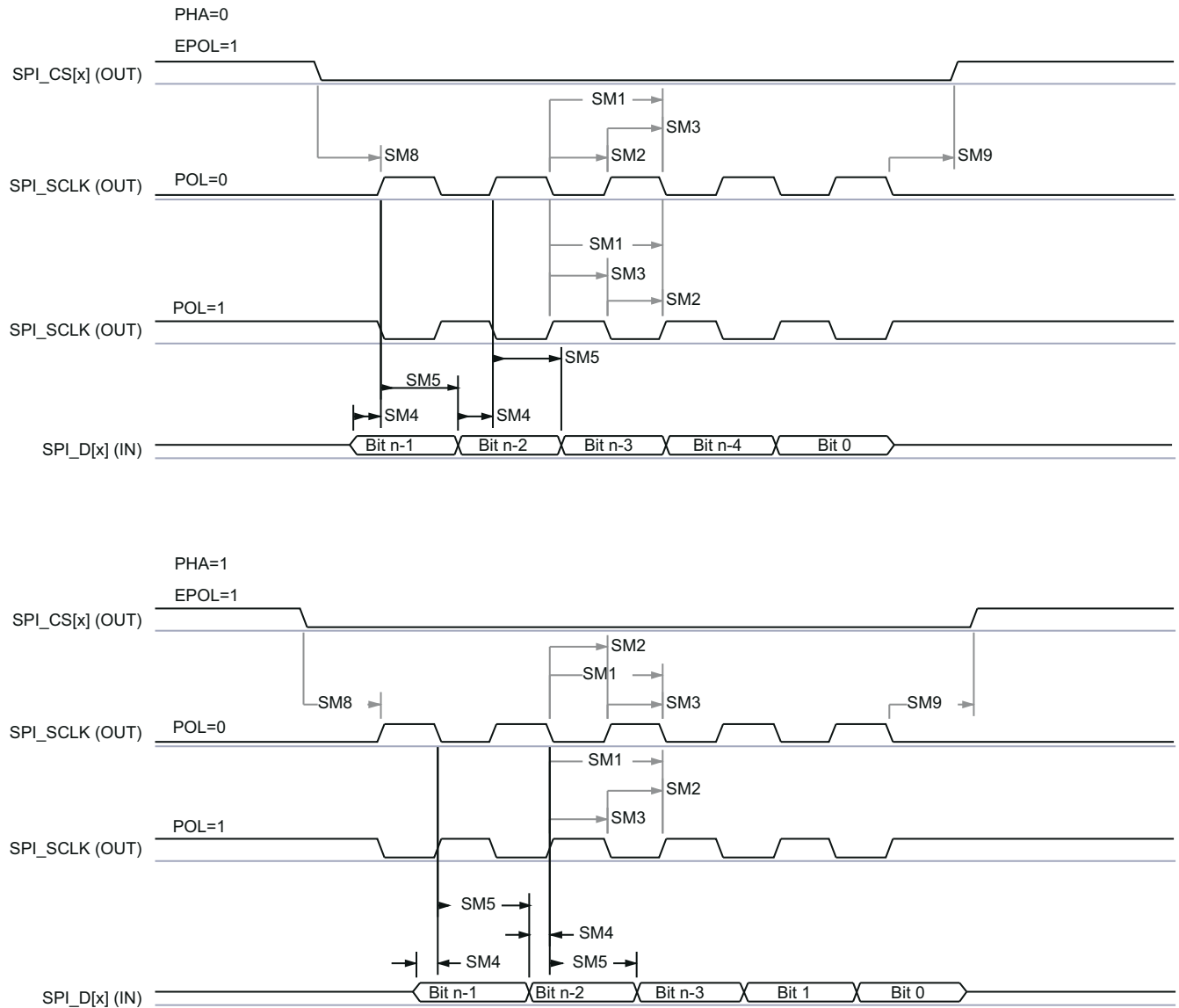
This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are being used to drive output data and capture input data

Note

Supported frequency of Radar SPIA Peripheral mode is 40MHz in full cycle and 20MHz in Half cycle mode.

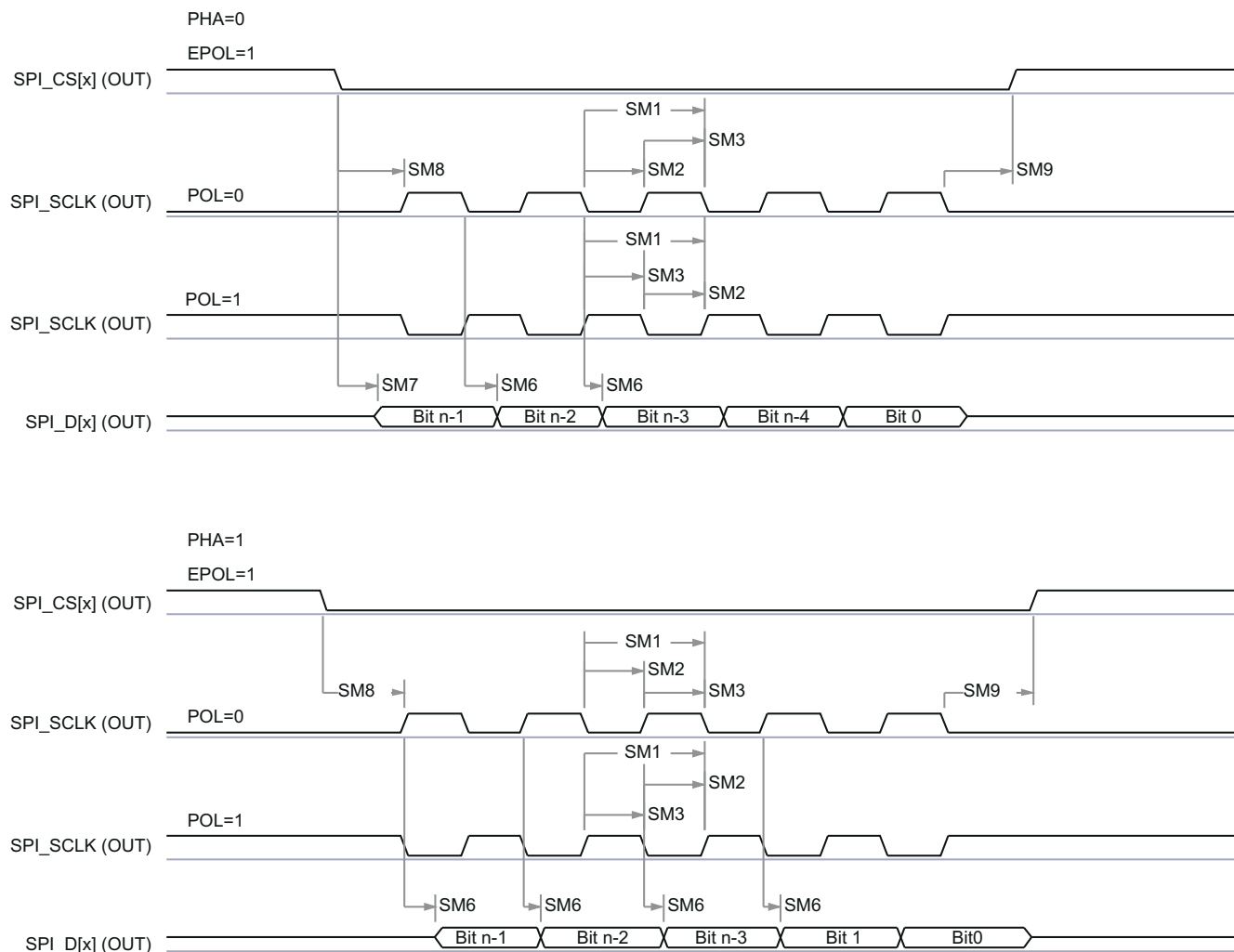
Supported frequency of Radar SPIB Peripheral mode is 20MHz in full cycle and 10MHz in Half cycle mode. Refer to [Section 6.2.1](#) for valid IOSET combinations of SPIB.

7.13.4.3.2 Timing and Switching Characteristics for SPI Output Timings—Controller Mode



SPRSP08_TIMING_McSPI_02

Figure 7-13. SPI Timing -Controller Mode Receive



SPRSP08_TIMING_McSPI_01

Figure 7-14. SPI Timing- Controller Mode Transmit**7.13.4.4 SPI—Peripheral Mode****7.13.4.4.1 Timing and Switching Requirements for SPI - Peripheral Mode**

Table 7-19 and Table 7-20 present timing requirements for SPI -Peripheral Mode.

Table 7-19. SPI Timing Requirements - Peripheral Mode

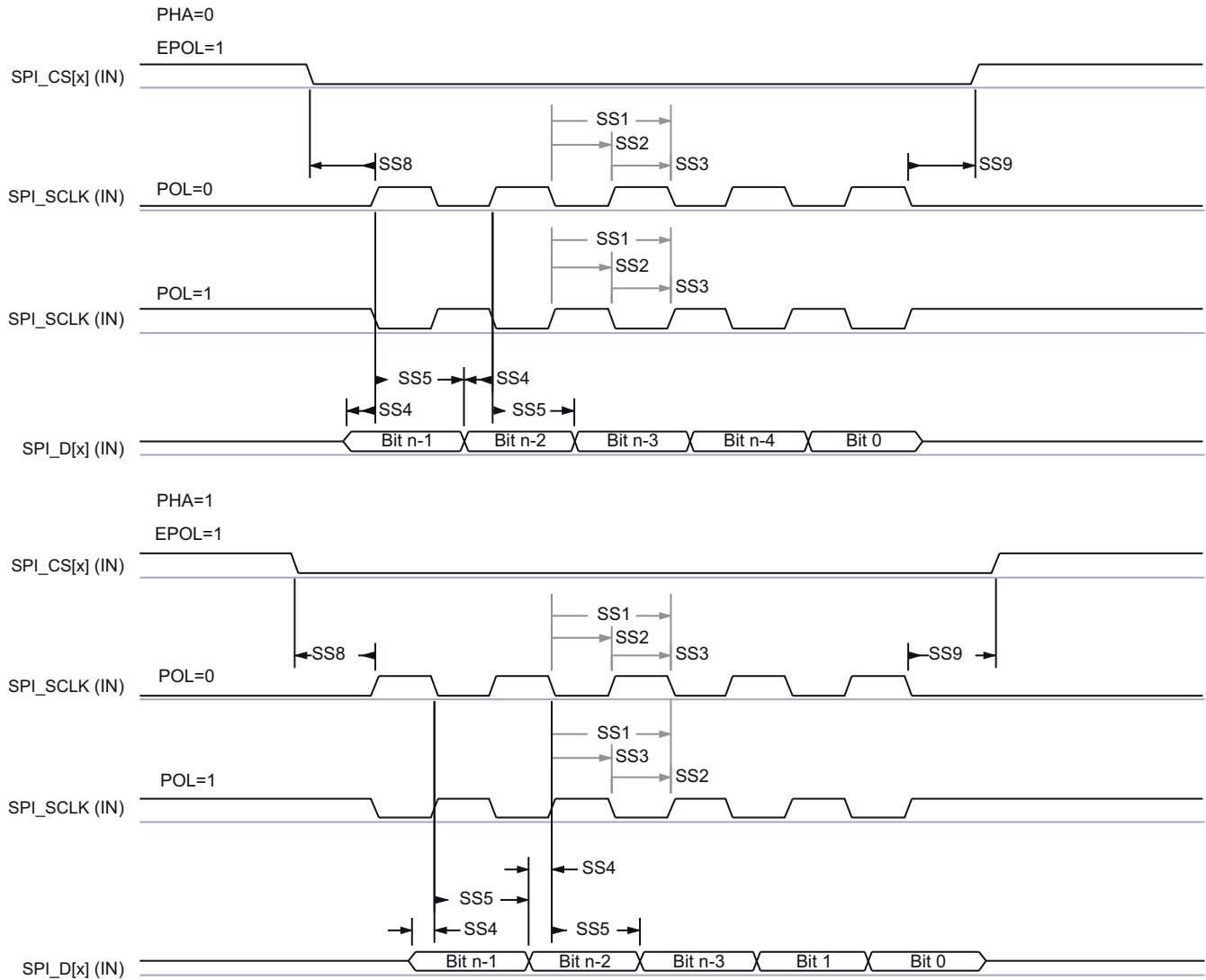
| NO. ⁽¹⁾ | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|--------------------|------------------------------|---|----------------------|-----|------|
| SS1 | $t_c(\text{SPICLK})$ | Cycle time, SPI_CLK | 24.6 | | ns |
| SS2 | $t_w(\text{SPICLK}_L)$ | Typical Pulse duration, SPI_CLK low | $0.45 \cdot P^{(2)}$ | | ns |
| SS3 | $t_w(\text{SPICLK}_H)$ | Typical Pulse duration, SPI_CLK high | $0.45 \cdot P^{(2)}$ | | ns |
| SS4 | $t_{su}(\text{SIMO-SPICLK})$ | Setup time, SPI_D[x] valid before SPI_CLK active edge | 3 | | ns |
| SS5 | $t_h(\text{SPICLK-SIMO})$ | Hold time, SPI_D[x] valid after SPI_CLK active edge | 1 | | ns |
| SS8 | $t_{su}(\text{CS-SPICLK})$ | Setup time, SPI_CS[x] valid before SPI_CLK first edge | 5 | | ns |
| SS9 | $t_h(\text{SPICLK-CS})$ | Hold time, SPI_CS[x] valid after SPI_CLK last edge | 5 | | ns |
| SS10 | sr | Input Slew Rate for all pins | 1 | 3 | ns |
| SS11 | Cb | Capacitive load on D0 and D1 | 2 | 15 | pF |

Table 7-20. SPI Switching Characteristics Peripheral Mode

| NO. | PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|-----|----------------------|--|------|------|------|
| SS6 | $t_{d(SPICLK-SOMI)}$ | Delay time, SPI_CLK active edge to McSPI_somi transition | 0 | 5.77 | ns |
| SS7 | $t_{sk(CS-SOMI)}$ | Delay time, SPI_CS[x] active edge to McSPI_somi transition | 5.77 | | ns |

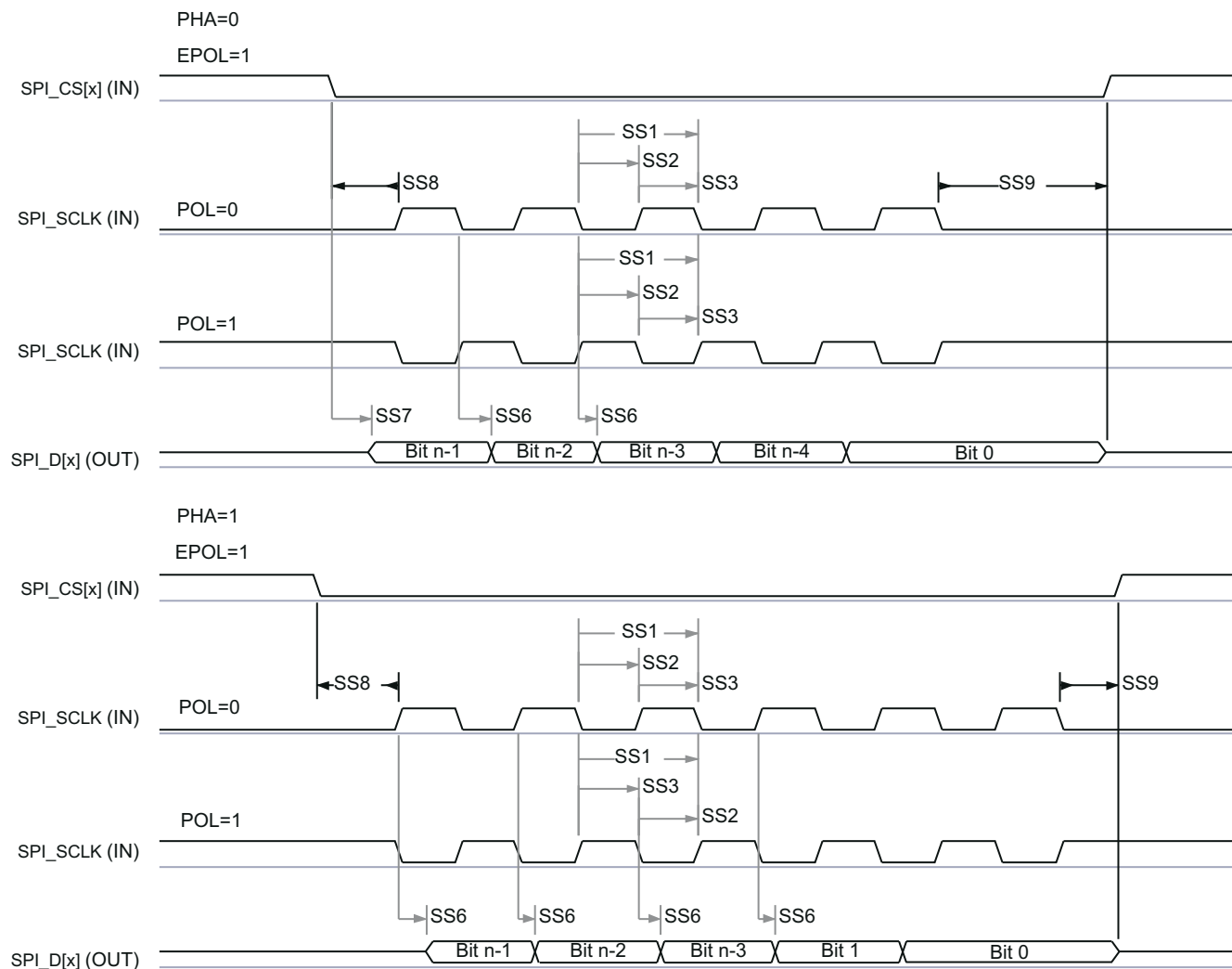
- (1) P = This timing applies to all configurations regardless of SPI_CLK polarity and which clock edges are used to drive output data and capture input data.
(2) P = SPICLK period.

7.13.4.4.2 Timing and Switching Characteristics for SPI Output Timings—Secondary Mode



SPRSP08_TIMING_McSPI_04

Figure 7-15. SPI Timing - Peripheral mode Receive



SPRSP08_TIMING_McSPI_03

Figure 7-16. SPI Timing - Peripheral mode Transmit

7.13.5 LVDS Instrumentation and Measurement Peripheral

The device supports LVDS interfaces for raw data capture. Please see the device TRM for information regarding configuring and programming options for LVDS interfaces.

7.13.5.1 LVDS Interface Configuration

The supported LVDS lane configuration is (LVDS_TXP/M), one Bit Clock lane (LVDS_TXxx_CLKP/M) and one Frame clock lane (LVDS_TXxx_FRCLKP/M). The LVDS interface supports programmable data rates with the maximum being 800 Mbps (400 MHz DDR Clock).

Note that the bit clock is in DDR format and hence the number of toggles in the clock is equivalent to data.

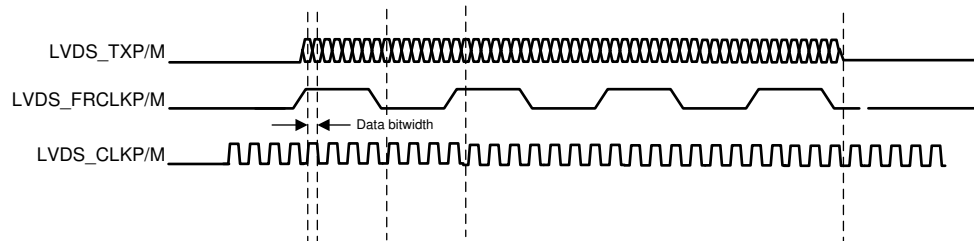


Figure 7-17. LVDS Interface Lane Configuration And Relative Timings

7.13.5.2 LVDS Interface Timings

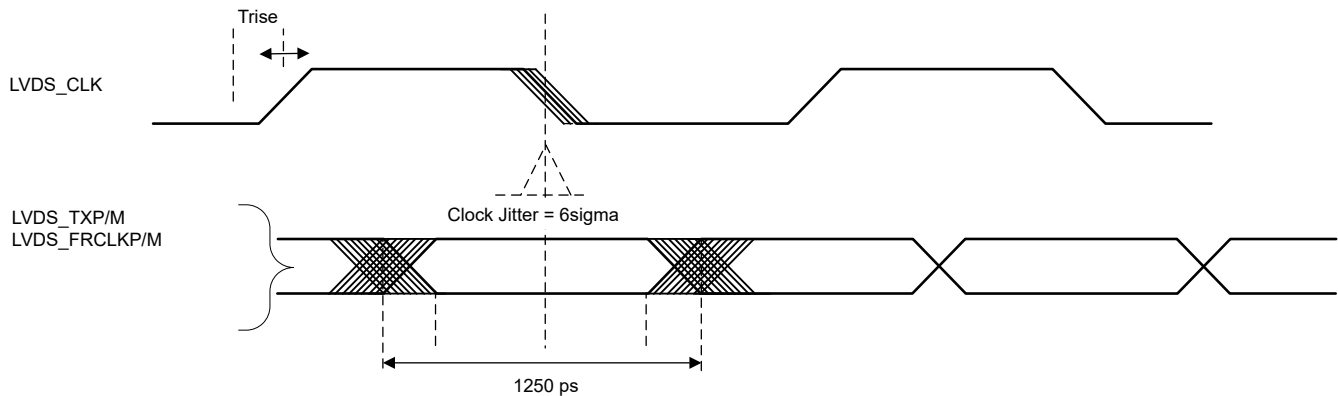


Figure 7-18. Timing Parameters

Table 7-21. LVDS Electrical Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|---|------|--------|------|------|
| Duty Cycle Requirements | max 1pF lumped capacitive load on LVDS lanes | 48% | | 52% | |
| Output Differential Voltage | peak-to-peak single-ended with 100Ω resistive load between differential pairs | 250 | | 450 | mV |
| Output Offset Voltage | | 1125 | | 1275 | mV |
| Trise and Tfall | 20%-80%, 800Mbps | | 371.25 | | ps |
| Jitter (pk-pk) | 800Mbps | | 90 | | ps |

7.13.6 LIN

The LIN module can be programmed to work either as an SCI or as a LIN. The SCI hardware features are augmented to achieve LIN compatibility. The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-/ multiple- with a message identification for multicast transmission between any network nodes.

The LIN has following features:

- Compatibility with LIN 1.3 , 2.0, and 2.1 protocols
- Configurable Baud Rate up to 20 kpbs
- Two external pins: LIN_RX and LIN_TX.
- Multi-buffered receive and transmit units
- Identification masks for message filtering
- Automatic Controller header generation
 - Programmable synchronization break field
 - Synchronization field
 - Identifier field
- Peripheral automatic synchronization
 - Synchronization break detection
 - Optional baud rate update
 - Synchronization validation
- 231 programmable transmission rates with 7 fractional bits
- Wake up on LIN_RX dominant level from transceiver
- Automatic wake up support
 - Wakeup signal generation
 - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
 - Bit error
 - Bus error
 - No-response error
 - Checksum error
 - Synchronization field error
 - Parity error
- Capability to use Direct Memory Access (DMA) for transmit and receive data.
- 2 Interrupt lines with priority encoding for:
 - Receive
 - Transmit
 - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator
- Update wakeup/go to sleep

Table 7-22. LIN Timing Requirements

| | | MIN | TYP | MAX | UNIT |
|---------|---------------------|-----|-----|-----|-------|
| f(baud) | Supported baud rate | 1 | | 20 | kBaud |

7.13.7 General-Purpose Input/Output

7.13.7.1 Switching Characteristics for Output Timing versus Load Capacitance (C_L)

Table 7-23 lists the switching characteristics of output timing relative to load capacitance.

Table 7-23. Switching Characteristics for Output Timing versus Load Capacitance (C_L)

| PARAMETER ^{(1) (2)} | | TEST CONDITIONS | | VIOIN = 1.8V | VIOIN = 3.3V | UNIT |
|------------------------------|---------------|------------------|-----------------------|--------------|--------------|------|
| t _r | Max rise time | Slew control = 0 | C _L = 20pF | 2.8 | 3.0 | ns |
| | | | C _L = 50pF | 6.4 | 6.9 | |
| | | | C _L = 75pF | 9.4 | 10.2 | |
| t _f | Max fall time | | C _L = 20pF | 2.8 | 2.8 | ns |
| | | | C _L = 50pF | 6.4 | 6.6 | |
| | | | C _L = 75pF | 9.4 | 9.8 | |

Table 7-23. Switching Characteristics for Output Timing versus Load Capacitance (C_L) (continued)

| PARAMETER ⁽¹⁾ (2) | | TEST CONDITIONS | | VIOIN = 1.8V | VIOIN = 3.3V | UNIT |
|------------------------------|---------------|------------------|-----------------------|--------------|--------------|------|
| t _r | Max rise time | Slew control = 1 | C _L = 20pF | 3.3 | 3.3 | ns |
| | | | C _L = 50pF | 6.7 | 7.2 | |
| | | | C _L = 75pF | 9.6 | 10.5 | |
| t _f | Max fall time | | C _L = 20pF | 3.1 | 3.1 | ns |
| | | | C _L = 50pF | 6.6 | 6.6 | |
| | | | C _L = 75pF | 9.6 | 9.6 | |

- (1) Slew control, which is configured by PADxx_CFG_REG, changes behavior of the output driver (faster or slower output slew rate).
(2) The rise/fall time is measured as the time taken by the signal to transition from 10% and 90% of VIOIN voltage.

7.13.8 Controller Area Network - Flexible Data-rate (CAN-FD)

The CAN-FD module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict. The device integrates two CAN-FD (CAN with Flexible Data-rate) which enables support of a typical use case where one CAN-FD interface is used as an ECU network interface while the other as a local network interface, providing communication with the neighboring sensors.

The CAN-FD has the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1
- Full CAN FD support (up to 64 data bytes per frame)
- AUTOSAR and SAE J1939 support
- Up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, up to 32 elements
- Configurable Transmit Queue, up to 32 elements
- Configurable Transmit Event FIFO, up to 32 elements
- Up to 64 dedicated Receive Buffers
- Two configurable Receive FIFOs, up to 64 elements each
- Up to 128 11-bit filter elements
- Internal Loopback mode for self-test
- Mask-able interrupts, two interrupt lines
- Two clock domains (CAN clock / Host clock)
- Parity / ECC support - Message RAM single error correction and double error detection (SECCDED) mechanism
- Full Message Memory capacity (4352 words).

7.13.8.1 Dynamic Characteristics for the CANx TX and RX Pins

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------------|---|-----|-----|-----|------|
| $t_d(\text{CAN_FD_tx})$ | Delay time, transmit shift register to CAN_FD_tx pin ⁽¹⁾ | | | 15 | ns |
| $t_d(\text{CAN_FD_rx})$ | Delay time, CAN_FD_rx pin to receive shift register ⁽¹⁾ | | | 15 | ns |

(1) These values do not include rise/fall times of the output buffer.

7.13.9 Serial Communication Interface (SCI)

The SCI has the following features:

- Standard universal asynchronous receiver-transmitter (UART) communication
- Supports full- or half-duplex operation
- Standard non-return to zero (NRZ) format
- Double-buffered receive and transmit functions in compatibility mode
- Supports two individually enabled interrupt lines: level 0 and level 1
- Configurable frame format of 3 to 13 bits per character based on the following:
 - Data word length programmable from one to eight bits
 - Additional address bit in address-bit mode
 - Parity programmable for zero or one parity bit, odd or even parity
 - Stop programmable for one or two stop bits
- Asynchronous or iso-synchronous communication modes with no CLK pin
- Two multiprocessor communication formats allow communication between more than two devices
- Sleep mode is available to free CPU resources during multiprocessor communication and then wake up to receive an incoming message
- Capability to use Direct Memory Access (DMA) for transmit and receive data
- Five error flags and Seven status flags provide detailed information regarding SCI events
- Two external pins: RS232_RX and RS232_TX

- Multi-buffered receive and transmit units

7.13.9.1 SCI Timing Requirements

| | MIN | TYP | MAX | UNIT |
|--|-----|----------------------|---------------------|-------|
| f(baud) Supported baud rate at 20pF | | 115.2 ⁽¹⁾ | 1250 ⁽²⁾ | kBaud |

- (1) Maximum supported standard baud rate.
(2) Maximum supported custom baud rate.

7.13.10 Inter-Integrated Circuit Interface (I2C)

The inter-integrated circuit (I2C) module is a multi-controller communication module providing an interface between devices compliant with Philips Semiconductor I2C-bus specification version 2.1 and connected by an I2C-bus™. This module will support any target or controller I2C compatible device.

The I2C has the following features:

- Compliance to the Philips I2C bus specification, v2.1 (The I2C Specification, Philips document number 9398 393 40011)
 - Bit/Byte format transfer
 - 7-bit and 10-bit device addressing modes
 - START byte
 - Multi-controller transmitter/ target receiver mode
 - Multi-controller receiver/ target transmitter mode
 - Combined controller transmit/receive and receive/transmit mode
 - Transfer rates of 100kbps up to 400kbps (Phillips fast-mode rate)
- Free data format
- Two DMA events (transmit and receive)
- DMA event enable/disable capability
- Module enable/disable capability
- The SDA and SCL are optionally configurable as general purpose I/O
- Slew rate control of the outputs
- Open drain control of the outputs
- Programmable pullup/pulldown capability on the inputs
- Supports Ignore NACK mode

Note

This I2C module does not support:

- High-speed (HS) mode
- C-bus compatibility mode
- The combined format in 10-bit address mode (the I2C sends the target address second byte every time it sends the target address first byte)

7.13.10.1 I2C Timing Requirements

| | | STANDARD MODE ⁽¹⁾ | | FAST MODE | | UNIT |
|---------------------|---|------------------------------|---------------------|-----------|-----|---------|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(SCL)}$ | Cycle time, SCL | 10 | | 2.5 | | μ s |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μ s |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μ s |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | 4.7 | | 1.3 | | μ s |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | 4 | | 0.6 | | μ s |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | 250 | | 100 | | ns |
| $t_{h(SCLL-SDA)}$ | Hold time, SDA valid after SCL low | 0 | 3.45 ⁽¹⁾ | 0 | 0.9 | μ s |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μ s |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | μ s |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| C_b (2) (3) | Capacitive load for each bus line | | 400 | | 400 | pF |

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices has only to be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
- (3) C_b = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

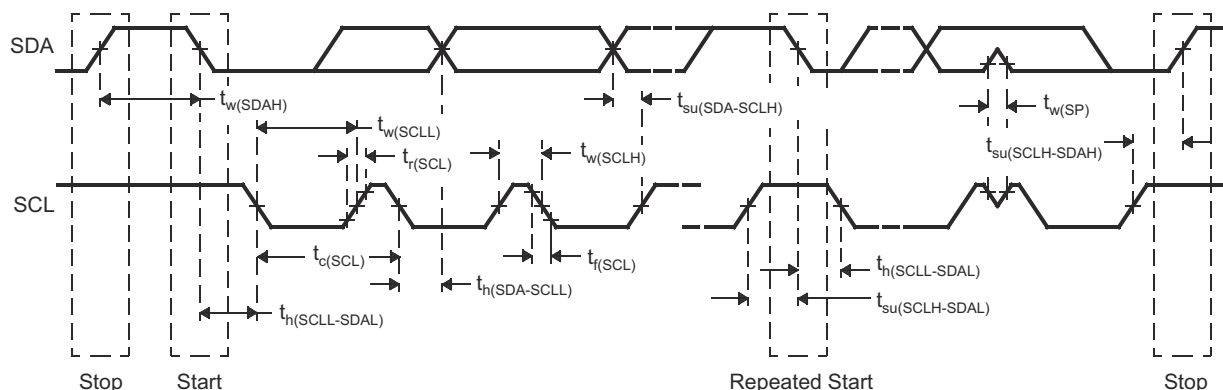


Figure 7-19. I2C Timing Diagram

Note

- A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal. E.A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r \text{ max} + t_{su(SDA-SCLH)}$.

7.13.11 Quad Serial Peripheral Interface (QSPI)

The quad serial peripheral interface (QSPI) module is a kind of SPI module that allows single, dual, or quad read access to external SPI devices. This module has a memory mapped register interface, which provides a direct interface for accessing data from external SPI devices and thus simplifying software requirements. The QSPI works as a controller only. The QSPI in the device is primarily intended for fast booting from quad-SPI flash memories.

The QSPI supports the following features:

- Programmable clock divider
- Six-pin interface
- Programmable length (from 1 to 128 bits) of the words transferred
- Programmable number (from 1 to 4096) of the words transferred
- Optional interrupt generation on word or frame (number of words) completion
- Programmable delay between chip select activation and output data from 0 to 3 QSPI clock cycles

Section 7.13.11.2 and Section 7.13.11.3 assume the operating conditions stated in Section 7.13.11.1.

7.13.11.1 QSPI Timing Conditions

| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

7.13.11.2 Timing Requirements for QSPI Input (Read) Timings

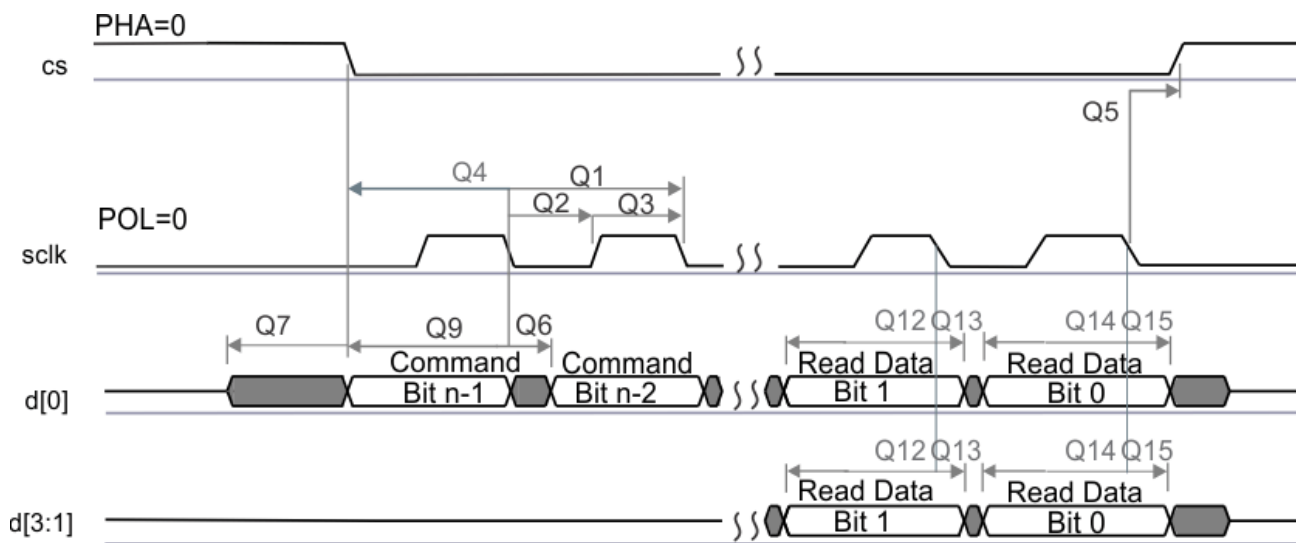
| | | MIN ^{(1) (2)} | TYP | MAX | UNIT |
|------------------|---|------------------------|-----|-----|------|
| $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | 5 | | | ns |
| $t_h(SCLK-D)$ | Hold time, d[3:0] valid after falling sclk edge | 1 | | | ns |
| $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | 5 – P ⁽³⁾ | | | ns |
| $t_h(SCLK-D)$ | Hold time, final d[3:0] bit valid after final falling sclk edge | 1 + P ⁽³⁾ | | | ns |

- (1) Clock Mode 0 (clk polarity = 0 ; clk phase = 0) is the mode of operation.
- (2) The Device captures data on the falling clock edge in Clock Mode 0, as opposed to the traditional rising clock edge. Although non-standard, the falling-edge-based setup and hold time timings have been designed to be compatible with standard SPI devices that launch data on the falling edge in Clock Mode 0.
- (3) P = SCLK period in ns.

7.13.11.3 QSPI Switching Characteristics

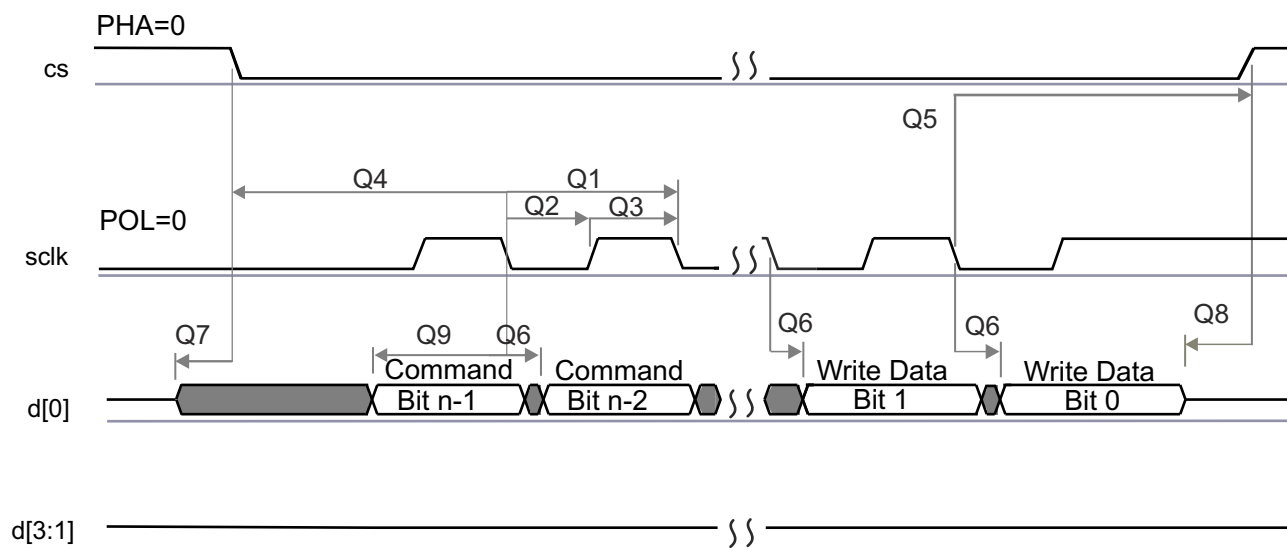
| NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|-----|--------------------|---|---------------------------|-----|-----------------------------|------|
| Q1 | $t_{c(SCLK)}$ | Cycle time, sclk | 12.5 | | | ns |
| Q2 | $t_{w(SCLKL)}$ | Pulse duration, sclk low | $Y \cdot P - 3^{(1)(2)}$ | | | ns |
| Q3 | $t_{w(SCLKH)}$ | Pulse duration, sclk high | $Y \cdot P - 3^{(1)(2)}$ | | | ns |
| Q4 | $t_{d(CS-SCLK)}$ | Delay time, sclk falling edge to cs active edge | $-M \cdot P - 1^{(2)(3)}$ | | $-M \cdot P + 2.5^{(2)(3)}$ | ns |
| Q5 | $t_{d(SCLK-CS)}$ | Delay time, sclk falling edge to cs inactive edge | $N \cdot P - 1^{(2)(3)}$ | | $N \cdot P + 2.5^{(2)(3)}$ | ns |
| Q6 | $t_{d(SCLK-D1)}$ | Delay time, sclk falling edge to d[1] transition | -2 | | 4 | ns |
| Q7 | $t_{ena(CS-D1LZ)}$ | Enable time, cs active edge to d[1] driven (lo-z) | $-P - 4^{(2)}$ | | $-P + 1^{(2)}$ | ns |
| Q8 | $t_{dis(CS-D1Z)}$ | Disable time, cs active edge to d[1] tri-stated (hi-z) | $-P - 4^{(2)}$ | | $-P + 1^{(2)}$ | ns |
| Q9 | $t_{d(SCLK-D1)}$ | Delay time, sclk first falling edge to first d[1] transition (for PHA = 0 only) | $-2 - P^{(2)}$ | | $4 - P^{(2)}$ | ns |
| Q12 | $t_{su(D-SCLK)}$ | Setup time, d[3:0] valid before falling sclk edge | 5 | | | ns |
| Q13 | $t_{h(SCLK-D)}$ | Hold time, d[3:0] valid after falling sclk edge | 1 | | | ns |
| Q14 | $t_{su(D-SCLK)}$ | Setup time, final d[3:0] bit valid before final falling sclk edge | $5 - P^{(2)}$ | | | ns |
| Q15 | $t_{h(SCLK-D)}$ | Hold time, final d[3:0] bit valid after final falling sclk edge | $1 + P^{(2)}$ | | | ns |

- (1) The Y parameter is defined as follows: If DCLK_DIV is 0 or ODD then, Y equals 0.5. If DCLK_DIV is EVEN then, Y equals (DCLK_DIV/2) / (DCLK_DIV+1). For best performance, it is recommended to use a DCLK_DIV of 0 or ODD to minimize the duty cycle distortion. All required details about clock division factor DCLK_DIV can be found in the device-specific Technical Reference Manual.
- (2) P = SCLK period in ns.
- (3) M = QSPI_SPI_DC_REG.DDx + 1, N = 2



SPRS85v TIMING QSPI 02

Figure 7-20. QSPI Read (Clock Mode 0)



SPRS85v_TIMING_OSPi1_04

Figure 7-21. QSPI Write (Clock Mode 0)

7.13.12 JTAG Interface

Section 7.13.12.2 and Section 7.13.12.3 assume the operating conditions stated in Section 7.13.12.1.

7.13.12.1 JTAG Timing Conditions

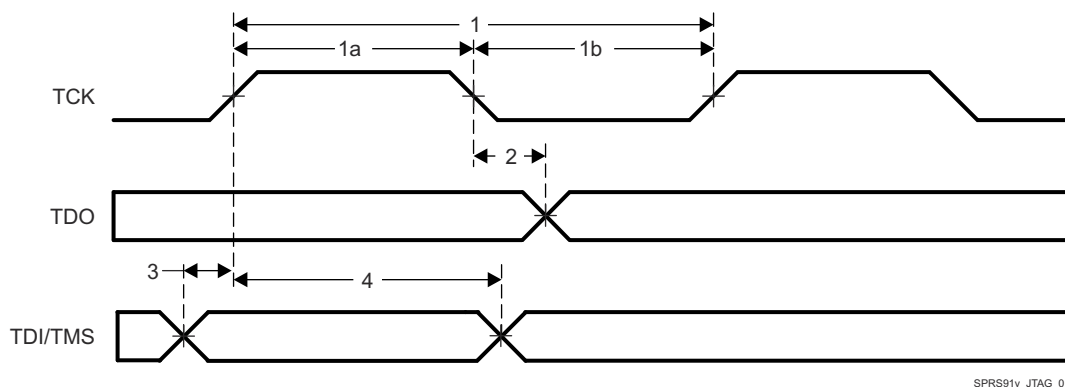
| | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Input Conditions | | | | | |
| t_R | Input rise time | 1 | | 3 | ns |
| t_F | Input fall time | 1 | | 3 | ns |
| Output Conditions | | | | | |
| C_{LOAD} | Output load capacitance | 2 | | 15 | pF |

7.13.12.2 Timing Requirements for IEEE 1149.1 JTAG

| NO. | | | MIN | TYP | MAX | UNIT |
|-----|-------------------|---|-------|-----|-----|------|
| 1 | $t_c(TCK)$ | Cycle time TCK | 66.66 | | | ns |
| 1a | $t_w(TCKH)$ | Pulse duration TCK high (40% of t_c) | 20 | | | ns |
| 1b | $t_w(TCKL)$ | Pulse duration TCK low(40% of t_c) | 20 | | | ns |
| 3 | $t_{su}(TDI-TCK)$ | Input setup time TDI valid to TCK high | 2.5 | | | ns |
| | $t_{su}(TMS-TCK)$ | Input setup time TMS valid to TCK high | 2.5 | | | ns |
| 4 | $t_h(TCK-TDI)$ | Input hold time TDI valid from TCK high | 18 | | | ns |
| | $t_h(TCK-TMS)$ | Input hold time TMS valid from TCK high | 18 | | | ns |

7.13.12.3 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG

| NO. | | PARAMETER | MIN | TYP | MAX | UNIT |
|-----|------------------|----------------------------------|-----|-----|-----|------|
| 2 | $t_d(TCKL-TDOV)$ | Delay time, TCK low to TDO valid | 0 | | 15 | ns |



SPRS91v_JTAG_01

Figure 7-22. JTAG Timing

8 Detailed Description

8.1 Overview

The AWRL684x device is a complete SOC which includes mmWave front end, customer programmable MCU, C66x DSP for advanced signal processing and analog baseband signal chain with four transmitters(3 transmitters for AWRL6843) and four receivers. This device is applicable as a radar-on-a-chip in use-cases with provision for memory, processing capacity, and application code size.

8.2 Functional Block Diagram

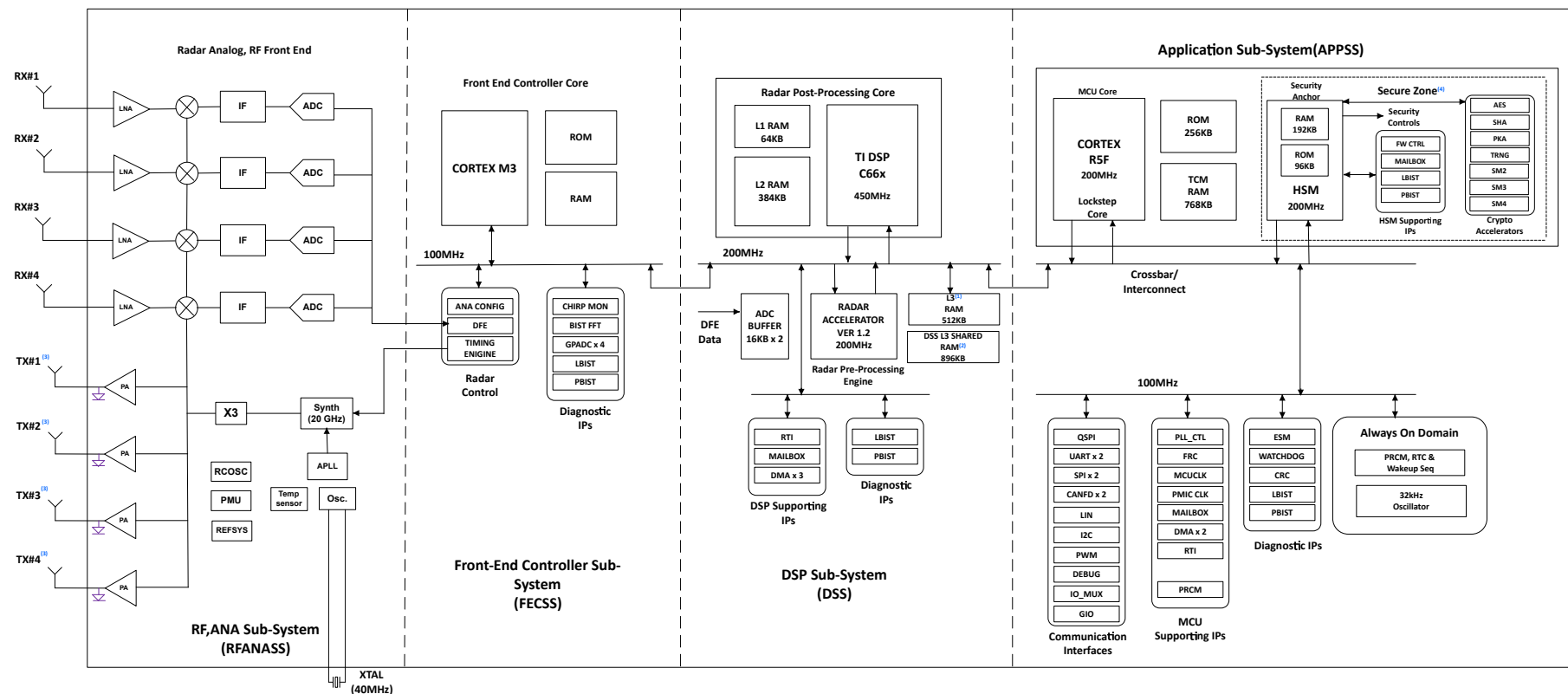


Figure 8-1. Functional Block Diagram

1. 512KB of DSS L3 Native RAM available only in AWRL6844
2. 896KB of DSS L3 Shared RAM Memory location is listed in [Table 8-1](#)
3. The AWRL6843 device has four transmitter antennas out of which any group of 3 transmitter antennas can be used (TX1, TX2, TX3), (TX1, TX2, TX4), (TX1, TX3, TX4) & (TX2, TX3, TX4).
4. Applicable to secure device variants only.

Table 8-1. Shared Memory Allocation

| Memory | Allocation |
|--------|--------------------|
| 512KB | DSS L3, APPSS TCMA |
| 256KB | DSS L3, APPSS TCMB |
| 128KB | DSS L3, FECSS |

8.3 Subsystems

8.3.1 RF and Analog Subsystem

The RF and analog subsystem includes the RF and analog circuitry – namely, the synthesizer, PA, LNA, mixer, IF, and ADC. This subsystem also includes the crystal oscillator and temperature sensors. TXs can be operated simultaneously for beam forming in BPM mode or individually in TDM mode. Similarly, the device allows configuring the number of transmit and receive channels based on application and power requirements. For system power saving, AWRL684x device provides duty cycling options to put RF and analog subsystems into low power mode configuration.

8.3.2 Clock Subsystem

The AWRL684x clock subsystem generates 57 to 63.9GHz from an input reference from a crystal. It has a built in oscillator circuit followed by a clean-up PLL and a RF synthesizer circuit. The output of the RF synthesizer is then processed by an X3 multiplier to create the required frequency in the 57 to 63.9GHz spectrum. The RF synthesizer output is modulated by the timing engine block to create the required waveforms for sensor operation. The clean-up PLL also provides a reference clock for the host processor after system wakeup. The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

The clean-up PLL also provides a reference clock for the host processor after system wakeup.

The clock subsystem also has built-in mechanisms for detecting the presence of a crystal and monitoring the quality of the generated clock.

Figure 8-2 describes the clock subsystem.

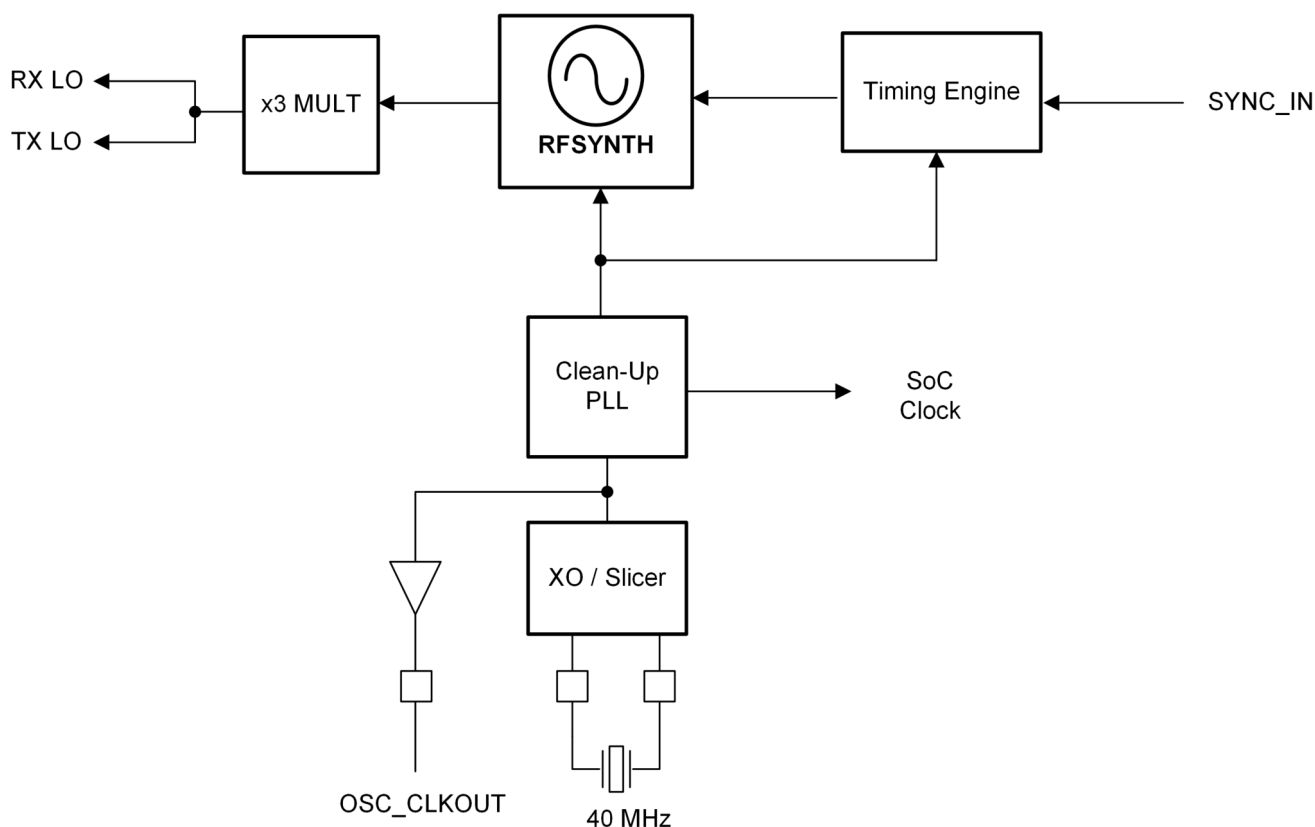


Figure 8-2. Clock Subsystem

8.3.3 Transmit Subsystem

The AWRL6844 transmit subsystem consists of four parallel transmit chains and AWRL6843 transmit subsystem consists of three parallel transmit chains, each with independent phase and amplitude control. The device supports binary phase modulation for MIMO radar.

The transmit chains also support programmable backoff for system optimization.

Figure 8-3 describes the transmit subsystem.

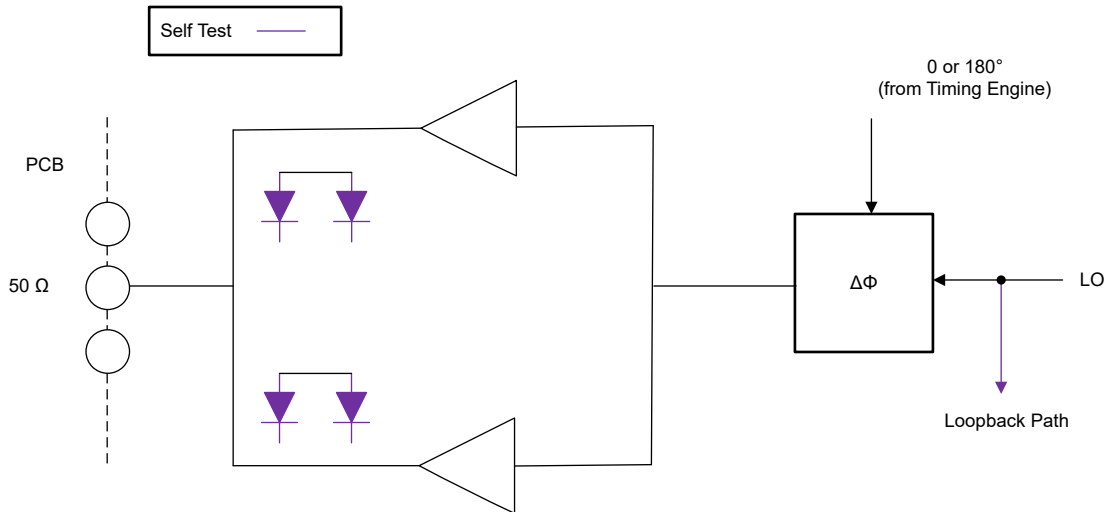


Figure 8-3. Transmit Subsystem (Per Channel)

8.3.4 Receive Subsystem

The AWRL684x receive subsystem consists of four parallel channels. A single receive channel consists of an LNA, mixer, IF filtering, ADC conversion, and decimation. All four receive channels can either operate simultaneously or can be powered down individually based on system power needs and application design. The AWRL684x device supports a real baseband architecture, which uses real mixer, single IF and ADC chains to provide output for each receiver channel. The device is targeted for fast chirp systems. The band-pass IF chain has configurable lower cutoff frequencies above 175kHz and can support bandwidths up to 10MHz.

Figure 8-4 describes the receive subsystem.

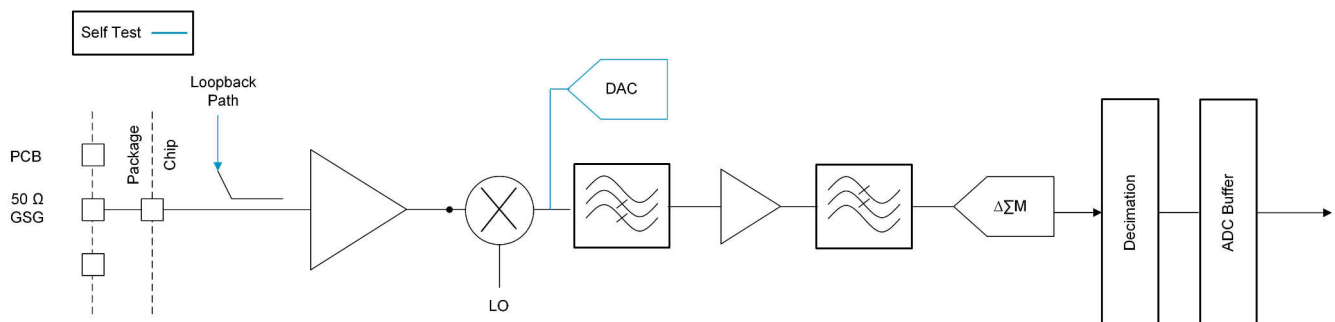


Figure 8-4. Receive Subsystem (Per Channel)

8.3.5 Processor Subsystem

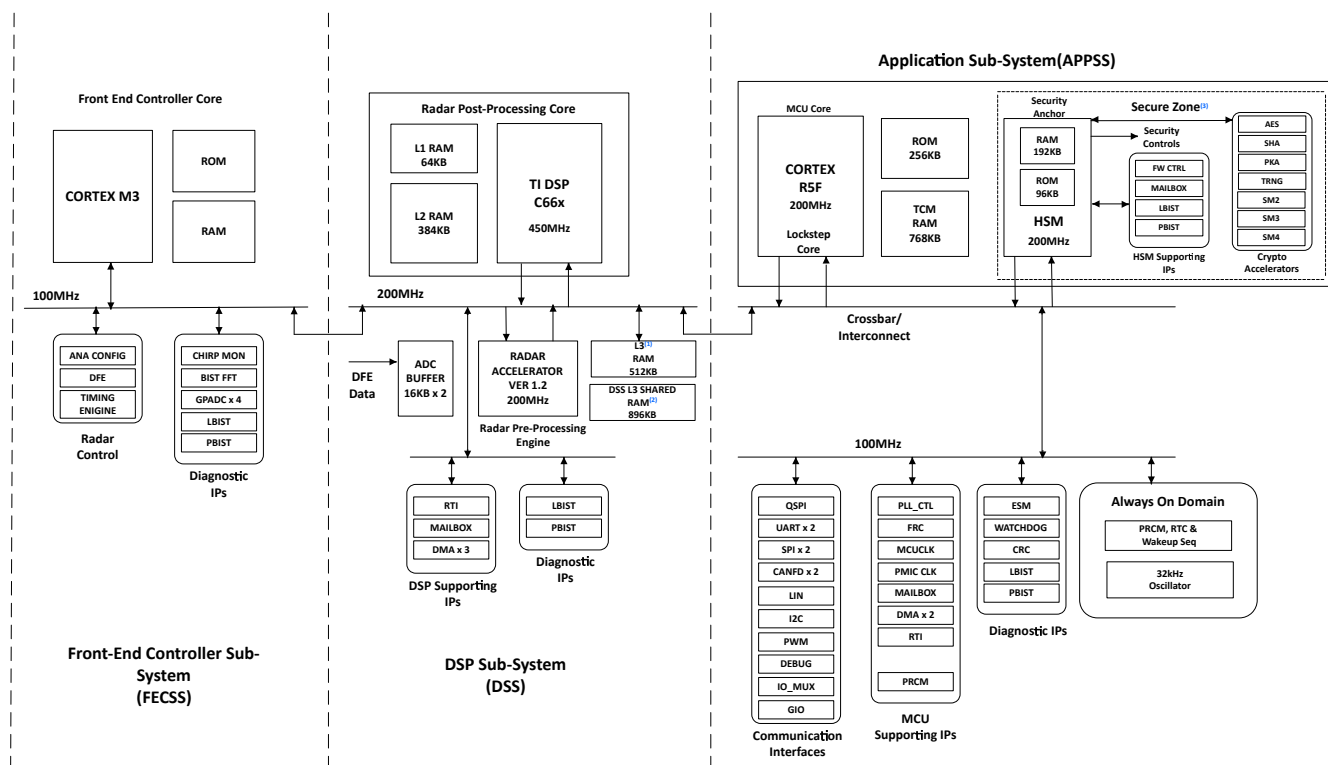


Figure 8-5. Processor Subsystem

1. 512KB of DSS L3 Native RAM available only in AWRL6844
2. 896KB of DSS L3 Shared RAM Memory location is listed in [Table 4-1](#)
3. Applicable to secure device variants only.

Figure 8-5 shows the block diagram for customer programmable processor subsystems in the AWRL684x device. At a high level there are two customer programmable subsystems, as shown separated by a dotted line in the diagram. The DSP Subsystem which contains TI's high-performance C66x DSP, HWA, a high-bandwidth interconnect for high performance (128-bit, 200MHz), and associated peripherals data transfer. LVDS interface for Measurement data output, L3 Radar data cube memory, the ADC buffers, the CRC engine, and data handshake memory (additional memory provided on interconnect).

The right side of the diagram shows the Application Subsystem. The Application Subsystem controls all the device peripherals and house-keeping activities of the device. The Application Subsystem contains Cortex-R5F processor and associated peripherals and house-keeping components such as DMAs, CRC and Peripherals (I²C, UART, SPI, CAN, PMIC clocking module, PWM, LIN, and others) connected to Main Interconnect through Peripheral Central Resource (PCR interconnect).

8.3.6 Automotive Interface

The AWRL684x communicates with the automotive network over the following main interfaces:

- CAN-FD
- LIN

8.3.7 Host Interface

The host interface can be provided through a SPI, LIN, UART, or CAN-FD interface.

The AWRL684x device communicates with the host radar processor over the following main interfaces:

- Reference Clock – Reference clock available for host processor after device wakeup
- Control – 4-port standard SPI (peripheral) for host control . All radio control commands (and response) flow through this interface.
- Reset – Active-low reset for device wakeup from host.
- Host Interrupt - an indication that the mmWave sensor needs host interface
- Error – Used for notifying the host in case the radio controller detects a fault

8.3.8 Application Subsystem Cortex-R5F

The Application Sub-System includes an ARM Cortex -R5F processor clocked with a maximum operating frequency of 200 MHz. User applications executing on this processor control the overall operation of the device, including radar control through well-defined API messages, radar signal processing (assisted by C66x DSP and radar hardware accelerator), and peripherals for external interfaces.

See the [Technical Reference Manual](#) for a complete description and memory map.

8.3.9 DSP Subsystem

The DSP subsystem includes TI's standard TMS320C66x megamodule and several blocks of internal memory (L1, and L2). For complete information including memory map, please refer to [Technical Reference Manual](#).

8.3.10 Hardware Accelerator (HWA1.2) Features

- Fast FFT computation, with programmable 2^N sizes, up to 1024-point complex FFT
- Internal FFT bit-width of 24 bits (each for I and Q) for good Signal-to-Quantization-Noise Ratio (SQNR) performance
- Fully programmable butterfly scaling at every radix-2 stage for user flexibility
- Built-in capabilities for pre-FFT processing – Ex: DC estimation and subtraction
- DC estimation & subtraction, Interference estimation & zero-out, Real window, Complex pre-multiplication
- Magnitude (absolute value) and Log-magnitude computation
- Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses
- Chaining and looping mechanism to sequence a set of operations one after another with minimal intervention from the main processor
- Peak detection – CFAR (CFAR-CA, CFAR-OS) detector
- Basic statistics, including Sum and 1D Max
- Compression engine for radar cube memory optimization

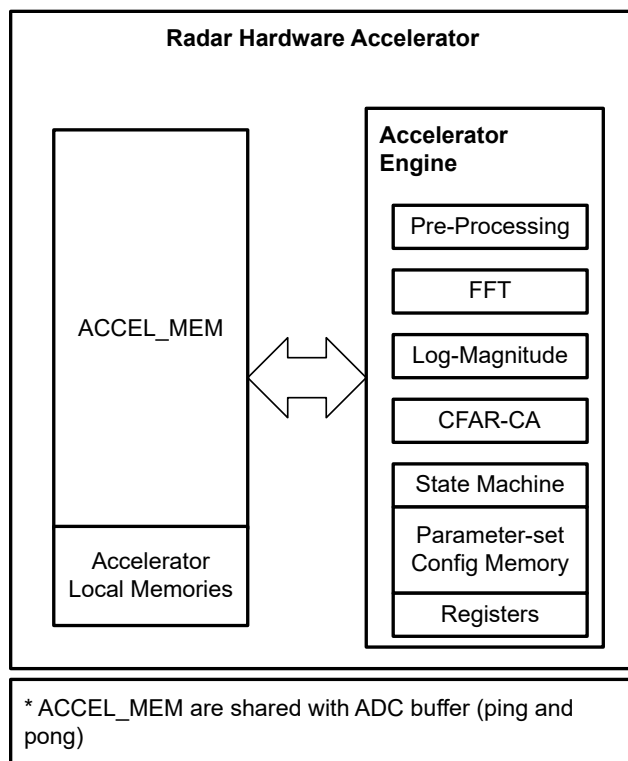


Figure 8-6. HWA 1.2 Functional Block Diagram

8.3.10.1 Hardware Accelerator Feature Differences Between HWA1.1 in xWRx843, HWA1.2 in xWRLx432 and HWA1.2 in xWRL684x

| Feature | | HWA1.0, HWA1.1 (xWR1843, xWR6843) | HWA1.2 (xWRL6432, xWRL1432) | HWA1.2 (xWRL684x) |
|---|--------------------|--|--|--|
| FFT features | FFT sizes | 1024, 512, 256, ... | 1024, 512, 256, ... | 1024, 512, 256, ... |
| | Internal bit-width | 24-bit I, 24-bit Q | 24-bit I, 24-bit Q | 24-bit I, 24-bit Q |
| | | Configurable butterfly scaling at each stage | Configurable butterfly scaling at each stage | Configurable butterfly scaling at each stage |
| | FFT stitching | up to 4096 point | up to 4096 point | up to 4096 point |
| FFT benchmark for four 256-pt FFTs | | 1312 clock cycles (6.56µs at 200MHz) | 1320 clock cycles (16.5 µs at 80MHz) | 1320 clock cycles (6.6µs at 200MHz) |
| No. of parameter-sets | | 16 | 32 | 32 |
| Local memory | | 64KB | 64KB | 64KB |
| Input and Output formatter | | <ul style="list-style-type: none"> A and B-dim addressing of local memory Programmable scaling | <ul style="list-style-type: none"> A and B-dim addressing of local memory Programmable scaling | <ul style="list-style-type: none"> A and B-dim addressing of local memory Programmable scaling |

| Feature | HWA1.0, HWA1.1 (xWR1843, xWR6843) | HWA1.2 (xWRL6432, xWRL1432) | HWA1.2 (xWRL684x) |
|--|--|---|---|
| Pre-FFT processing | <ul style="list-style-type: none"> Interference zero out with fixed threshold, based on magnitude Complex multiplication (7 modes) Real window coefficients | <ul style="list-style-type: none"> DC estimation and subtraction Interference zero out with adaptive statistics, based on mag, mag-diff. Interference count indication. Complex multiplication (7 modes) Real window coefficients | <ul style="list-style-type: none"> DC estimation and subtraction Interference zero out with adaptive statistics, based on mag, mag-diff. Interference count indication. Complex multiplication (7 modes) Real window coefficients |
| Post-FFT processing | Log-magnitude (0.3dB accuracy) | Log-magnitude (0.06dB accuracy) | Log-magnitude (0.06dB accuracy) |
| Compression and De-compression support | Not available in HWA1.0 (xWR1843), Available in HWA1.1 (xWR6843) | Available | Available |
| Detection | CFAR-CA (linear and log modes) | <ul style="list-style-type: none"> CFAR-CA (linear and log modes) CFAR-OS (window size up to 32 on each side) | <ul style="list-style-type: none"> CFAR-CA (linear and log modes) CFAR-OS (window size up to 32 on each side) |
| Statistics | 1D Sum, 1D Max | 1D Sum, 1D Max | 1D Sum, 1D Max |

8.4 Other Subsystems

8.4.1 Security – Hardware Security Module

A Hardware Security Module (HSM), which performs a secure zone operation, is provisioned in the device (*operational only in select part variants*). A programmable Arm Cortex-M4 core is available to implement the crypto-agility requirements.

The cryptographic algorithms can be accelerated using the hardware modules in the HSM. Functions include acceleration of AES, SHA, Chinese crypto algorithms (SM2, SM3 and SM4) and public key accelerator (PKA) to perform math operations for asymmetric key cryptographic requirements and true random number generation.

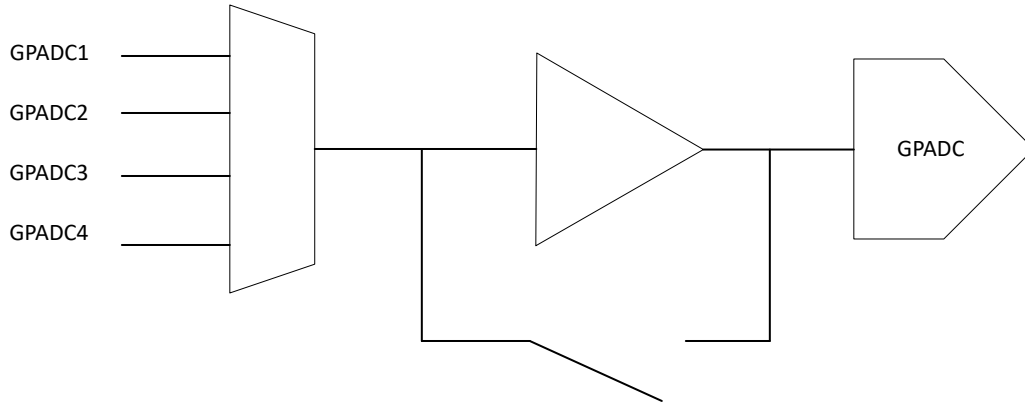
The APP subsystem (APPSS) Cortex-R5F processor interfaces with the HSM subsystem to perform the cryptographic operations required for the secure boot and secure runtime communications.

Further details on Security can be found in the concerned collaterals. Please reach out to your local TI sales representative for more information.

8.4.2 GPADC Channels (Service) for User Application

The AWRL684x device includes provision for an ADC service for user application, where the GPADC engine present inside the device can be used to measure up to four external voltages. The GPADC1, GPADC2, GPADC3 and GPADC4 pins are used for this purpose.

- GPADC itself is controlled by TI firmware running inside the FEC subsystem and access to it for customer's external voltage monitoring purpose is via 'APPSS' calls routed to the FEC subsystem. This API could be linked with the user application running on APPSS Cortex R5F.
- Device Firmware package (DFP) provides APIs to configure and measure these signals. The API allows configuring the settling time (number of ADC samples to skip) and number of consecutive samples to take. Average of the readings will be reported for each of the monitored voltages.

**Figure 8-7. GPADC Path**

GPADC structures are used for measuring the output of internal temperature sensors. The accuracy of these measurements is $\pm 7^{\circ}\text{C}$.

8.4.3 GPADC Parameters

| PARAMETER | TYP | UNIT |
|---|-----------|------|
| ADC supply | 1.8 | V |
| ADC unbuffered input voltage range | 0 – 1.8 | V |
| ADC buffered input voltage range ⁽¹⁾ | 0.4 – 1.3 | V |
| ADC resolution | 8 | bits |
| ADC offset error | ± 5 | LSB |
| ADC gain error | ± 5 | LSB |
| ADC DNL | $-1/+2.5$ | LSB |
| ADC INL | ± 2.5 | LSB |
| ADC sample rate ⁽²⁾ | 831 | Ksps |
| ADC sampling time ⁽²⁾ | 300 | ns |
| ADC internal cap | 10 | pF |
| ADC buffer input capacitance | 2 | pF |
| ADC input leakage current | 3 | uA |

(1) Outside of given range, the buffer output will become nonlinear.

(2) GPADC itself is controlled by TI firmware running inside the BIST subsystem. For more details please refer to the API calls.

8.5 Memory Partitioning Options

AWRL6844 devices will have a total memory of 2.5MB. AWRL6843 devices will have a total memory of 2MB. [Table 8-2](#) lists some of the available memory partition options. Memory partition options are not limited to [Table 8-2](#)

Table 8-2. Memory Partition Options

| Memory | AWRL6844 | | AWRL6843 | |
|-------------------------------|----------|-------------|----------|-------------|
| | Default | Alternative | Default | Alternative |
| DSS L2 | 384KB | 384KB | 384KB | 384KB |
| DSPSS L3 Native | 512KB | 512KB | 0KB | 0KB |
| L3 Memory (Shared with TCMA) | 512KB | 0KB | 512KB | 0KB |
| L3 Memory (Shared with TCMB) | 256KB | 0KB | 256KB | 0KB |
| L3 Memory (Shared with FECSS) | 128KB | 0KB | 128KB | 0KB |
| DSPSS L3 Total | 1408KB | 512KB | 896KB | 0KB |
| APPSS Native - TCMA | 512KB | 512KB | 512KB | 512KB |

Table 8-2. Memory Partition Options (continued)

| Memory | AWRL6844 | | AWRL6843 | |
|---------------------|----------|-------------|----------|-------------|
| | Default | Alternative | Default | Alternative |
| APPSS Native - TCMB | 256KB | 256KB | 256KB | 256KB |
| APPSS Shared - TCMA | 0KB | 512KB | 0KB | 512KB |
| APPSS Shared - TCMB | 0KB | 256KB | 0KB | 256KB |
| APPSS Total | 768KB | 1536KB | 768KB | 1536KB |
| FECSS | 0KB | 128KB | 0KB | 128KB |
| Total Device Memory | 2560KB | 2560KB | 2048KB | 2048KB |

The entire RAM is retainable. Additionally, each memory cluster can be independently turned off (if needed). The clusters are defined as below

Memory Retention Options

Table 8-3. APPSS

| Un-Switchable memory | | Switchable memory | | | Switchable memory - Shared with DSS L3 (DSS Bank 1) | | |
|----------------------|------------|-------------------|------------|---------------|---|------------|---------------|
| | | Group1 | | | Group2 | | Group3 |
| 256KB | | 512KB | | | 512KB | | 256KB |
| Cluster #1 | Cluster #2 | Cluster #5 | Cluster #6 | Cluster #7 | Cluster #8 | Cluster #9 | Cluster #10 |
| TCMA | TCMA | TCMA | TCMA | TCMB0 + TCMB1 | TCMA Bank0 | TCMA Bank1 | TCMB0 + TCMB1 |
| 128KB | 128KB | 128KB | 128KB | 128KB + 128KB | 256KB | 256KB | 128KB + 128KB |

Table 8-4. DSS

| Switchable Memory | | | | | | Switchable Memory - Shared with FECSS |
|-------------------|-----------|-----------|-----------|--------------------|--------------------|---------------------------------------|
| Group 4 | | Group 5 | | Group 6 | | Group 4 |
| 144KB | | 304KB | | 512KB | | 128KB |
| Cluster#2 | Cluster#3 | Cluster#4 | Cluster#5 | Cluster#6 | Cluster#7 | Cluster#1 |
| DSP L2 | HWA | DSP L2 | DSP L1 | DSS L3 (DSS Bank0) | DSS L3 (DSS Bank0) | DSS L3 (DSS Bank0) |
| 144KB | | 240KB | 64KB | 256KB | 256KB | 128KB |

8.6 Boot Modes

As soon as device reset is de-asserted, the processor of the APPSS starts executing its bootloader from an on-chip ROM memory.

The bootloader operates in three basic modes and these are specified on the user hardware (Printed Circuit Board) by configuring what are termed as "Sense on power" (SOP) pins. These pins on the device boundary are scanned by the bootloader firmware and choice of mode for bootloader operation is made.

Table 8-5 enumerates the relevant SOP combinations and how these map to bootloader operation.

Table 8-5. SOP Combinations

| SOP1 | SOP0 | BOOTLOADER MODE AND OPERATION |
|------|------|---|
| 0 | 0 | Flashing Mode / Device Management Mode Device Bootloader spins in loop to allow flashing of user application (or device firmware patch - Supplied by TI) to the serial flash. |

Table 8-5. SOP Combinations (continued)

| SOP1 | SOP0 | BOOTLOADER MODE AND OPERATION |
|------|------|--|
| 0 | 1 | Functional Mode / Application Mode Device Bootloader loads user application from QSPI Serial Flash to internal RAM and switches the control to it. |
| 1 | 1 | Debug Mode / Development Mode Bootloader is bypassed and R5F processor is halted. This allows user to connect emulator at a known point. |

9 Monitoring and Diagnostics

For details on monitoring and functional safety implementation, refer to the [Technical Reference Manual](#).

Refer to the *Device Safety Manual* or other relevant collaterals for more details on applicability of all diagnostics mechanisms.

10 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Application information can be found on [AWR Application web page](#).

10.2 Reference Schematic

Please check the device product page for latest Hardware design information under Design Kits - typically, at Design and Development

Listed for convenience are: Design Files, Schematics, Layouts, and Stack up for PCB

- [Altium AWRL6844 EVM Design Files](#)
- [AWRL6844 EVM Schematic Drawing, Assembly Drawing, and Bill of Materials](#)

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions follow.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *AWRL6844*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ABL), the temperature range (for example, blank is the default commercial temperature range). [Device Nomenclature](#), provides a legend for reading the complete device name for any *AWRL684x* device.

For orderable part numbers of *AWRL684x* devices in the ANC package types, see the Package Option Addendum of this document (when available), the TI website (www.ti.com), or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the [AWRL684x Device Errata](#) .

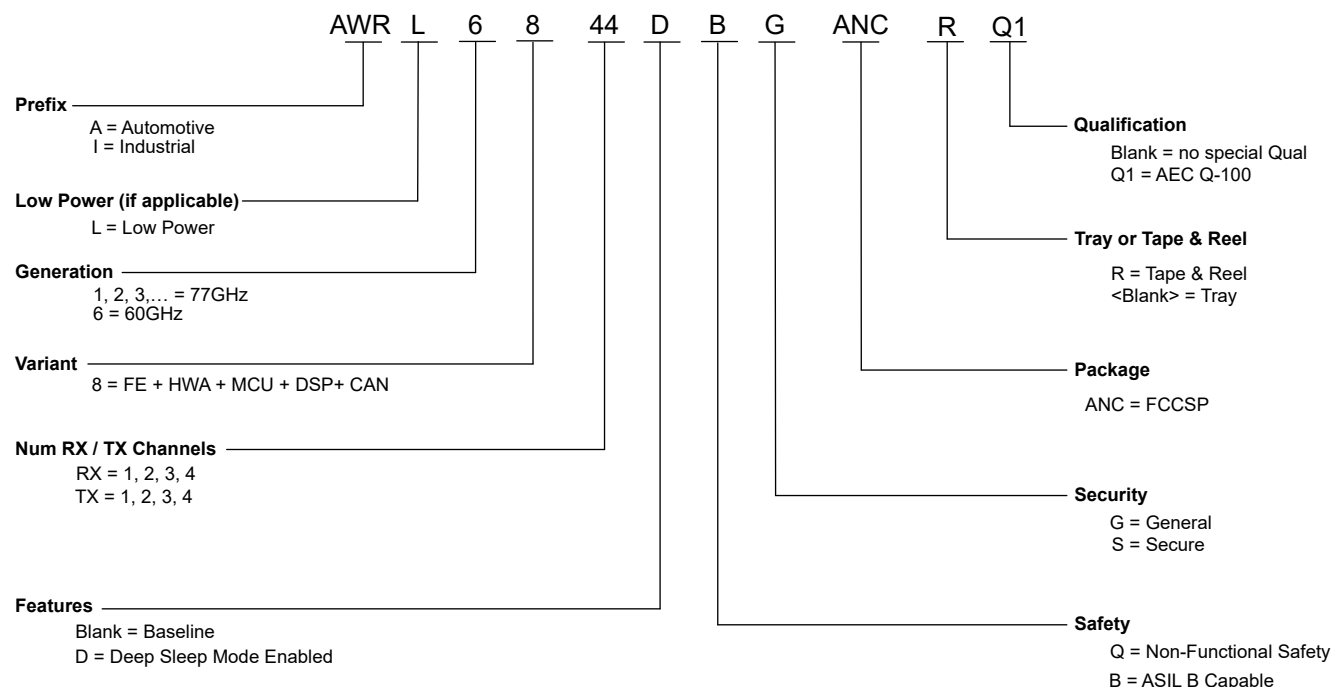


Figure 11-1. Device Nomenclature

11.2 Tools and Software

MMWAVE-L-SDK This SDK contains examples, libraries and tools to develop RTOS and no-RTOS based applications for ARM R5F and C66 CPUs and related peripherals.

Models

AWRL684x BSDL model Boundary scan database of testable input and output pins for IEEE 1149.1 of the specific device.

AWRL684x IBIS model IO buffer information model for the IO buffers of the device. For simulation on a circuit board, see IBIS Open Forum.

11.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the peripherals, and other technical collateral follows.

Errata

AWRL6843/44 Device Errata . Describes known advisories, limitations, and cautions on silicon and provides workarounds.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help—straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

| | |
|-----------------------------|--|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |
|-----------------------------|--|

12 Revision History

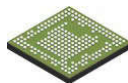
Changes from January 1, 2025 to December 31, 2026 (from Revision * (January 2025) to Revision A (December 2025))

| | Page |
|--|------|
| • (Features) : Updated typical output power per TX to 12.5dBm..... | 1 |
| • (Features) : Updated typical phase noise at 1MHz offset to -90.5dBc/Hz..... | 1 |
| • (Features) : Added LIN interface under host interfaces..... | 1 |
| • (Features) : Added product cybersecurity compliance information..... | 1 |
| • (Packaging Information) : Pre-production part numbers removed..... | 2 |
| • (Functional Block Diagram) : Added crypto accelerators and Secure zone..... | 4 |
| • (Functional Block Diagram) : Added Always on Domain..... | 4 |
| • (Functional Block Diagram figure notes) : Added available transmitter antenna info for AWRL6843 | 4 |
| • (Device Comparison) : Production status changed from AI to PD..... | 7 |
| • (Device Comparison) : Added HWA versions..... | 7 |
| • (Device Comparison) : Added cybersecurity compliance..... | 7 |
| • (Signal Descriptions) : Added DSS UARTA signal description | 11 |
| • (Analog Signal Descriptions) : Added available transmitter antenna info for AWRL6843 | 11 |
| • (Valid IOSET Combinations for SPIB Signal) : Updated additional SPIB IOSET combinations..... | 14 |
| • (System Signal Descriptions) : Updated System Signal Descriptions..... | 14 |
| • (System Signal Descriptions) : Updated BGA pins available for PRCM_PMIC_Deepsleep and WU_reqin.... | 14 |
| • (Recommended Operating Conditions for OTP eFuse Programming) : Added decoupling capacitor recommendation..... | 24 |
| • (RF Supply Decoupling Capacitor and Layout Conditions) : Updated parasitics requirements for 1.2V RF rail and 1.0V RF LDO output..... | 27 |
| • (RF Supply Decoupling Capacitor and Layout Conditions) : Added min-max capacitor requirements for 1.2V RF rail and 1.0V RF LDO output..... | 27 |
| • (RF Supply Decoupling Capacitor and Layout Conditions) : Added layout guidellines for for 1.2V RF rail and 1.0V RF LDO output..... | 27 |
| • (Typical Power Consumption Numbers) : Introduction updated with the status of I/Os | 33 |
| • (Typical Power Consumption Numbers) : Estimated Power Consumed in 3.3V IO Mode table - updated power consumption numbers..... | 33 |
| • (Typical Power Consumption Numbers) : Estimated Power Consumed in 3.3V IO Mode table - updated configuration with more details..... | 33 |
| • (Typical Power Consumption Numbers) : Estimated Power Consumed in 1.8V IO Mode table added..... | 33 |
| • (Typical Power Consumption Numbers) : Use-Case Power Consumed in 3.3V I/O Topology - updated power consumption numbers..... | 33 |

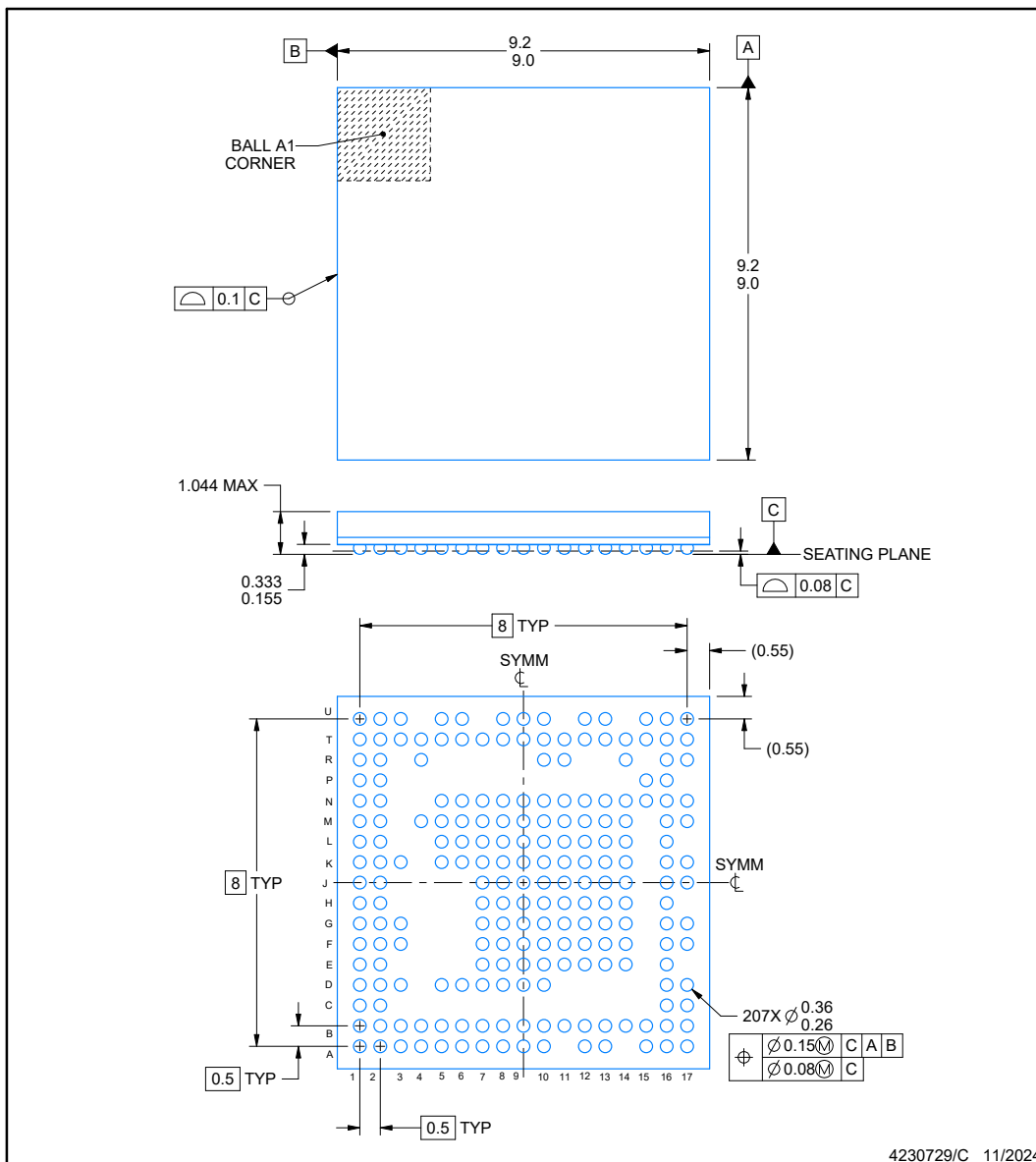
| | |
|--|----|
| • (Typical Power Consumption Numbers) : Use-Case Power Consumed in 3.3V I/O Topology - updated configuration with more details..... | 33 |
| • (Typical Power Consumption Numbers) : Use-Case Power Consumed in 1.8V IO Mode table added..... | 33 |
| • (Peak Current Requirement per Voltage Rail) : Maximum Peak Current per Voltage Rail table - updated peak current numbers..... | 35 |
| • (RF Specification) : Updated typical TX output power to 12.5dBm..... | 36 |
| • (RF Specification) : Updated typical phase noise at 1MHz offset to -90.5dBc/Hz..... | 36 |
| • (RF Specification) : Updated receiver S11 to -7dB..... | 36 |
| • (RF Specification) : Updated transmitter S11 to -7.5dB..... | 36 |
| • (RF Specification) : Added a plot of Noise Figure, In-band P1dB vs Receiver Gain..... | 36 |
| • (Supported DFE Features) : Updated RX gain range to 36dB to 46dB..... | 38 |
| • (Supported DFE Features) : Chip Profile Supported by Timing Engine figure - Updated typical inter-chirp idle time to 6 to 12uS..... | 38 |
| • (Supported DFE Features) : Chip Profile Supported by Timing Engine figure - Updated typical inter-burst idle time to 135 to 270uS..... | 38 |
| • (Power Supply Sequencing and Reset Timing) : Updated Device Wake-up Sequence diagram to sequence 1.2V rail before 1.8V rail..... | 39 |
| • (Functional Block Diagram) : Added crypto accelerators and Secure zone..... | 60 |
| • (Functional Block Diagram) : Added Always on Domain..... | 60 |
| • (Functional Block Diagram figure notes) : Added available transmitter antenna info for AWRL6843 | 60 |
| • (GPADC Channels (Service) for User Application) : Updated the introduction related to GPADC readings to the reflect actual GPADC measurement info..... | 67 |
| • (Memory Partitioning Options) : Updated DSS L3 total memory to 896KB in default option and 0KB to alternative option for AWRL6843..... | 68 |

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, see the left-hand navigation.

**ANC0207A****PACKAGE OUTLINE****FCCSP - 1.044 mm max height**

PLASTIC BALL GRID ARRAY



4230729/C 11/2024

NOTES:

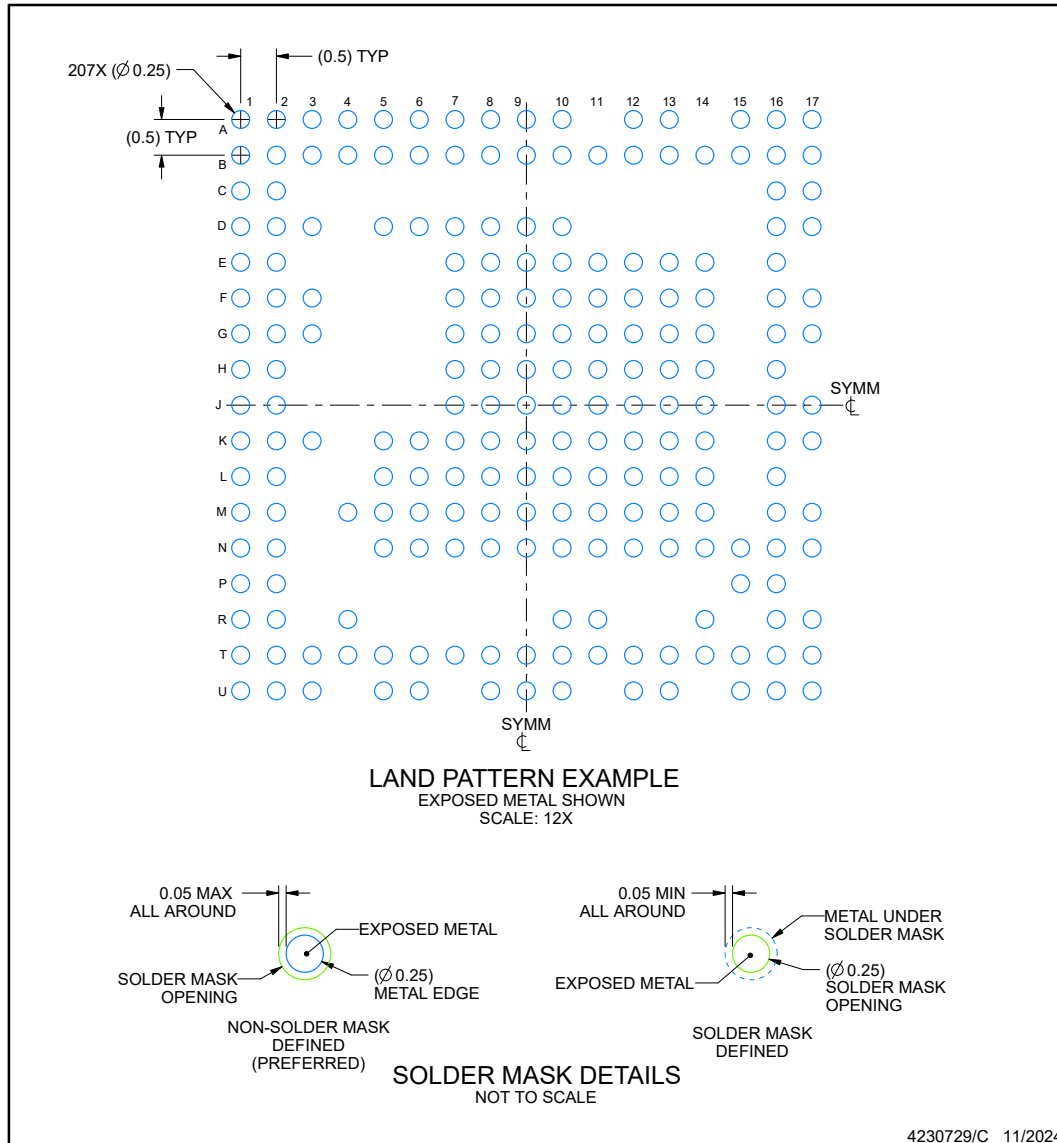
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ANC0207A

FCCSP - 1.044 mm max height

PLASTIC BALL GRID ARRAY

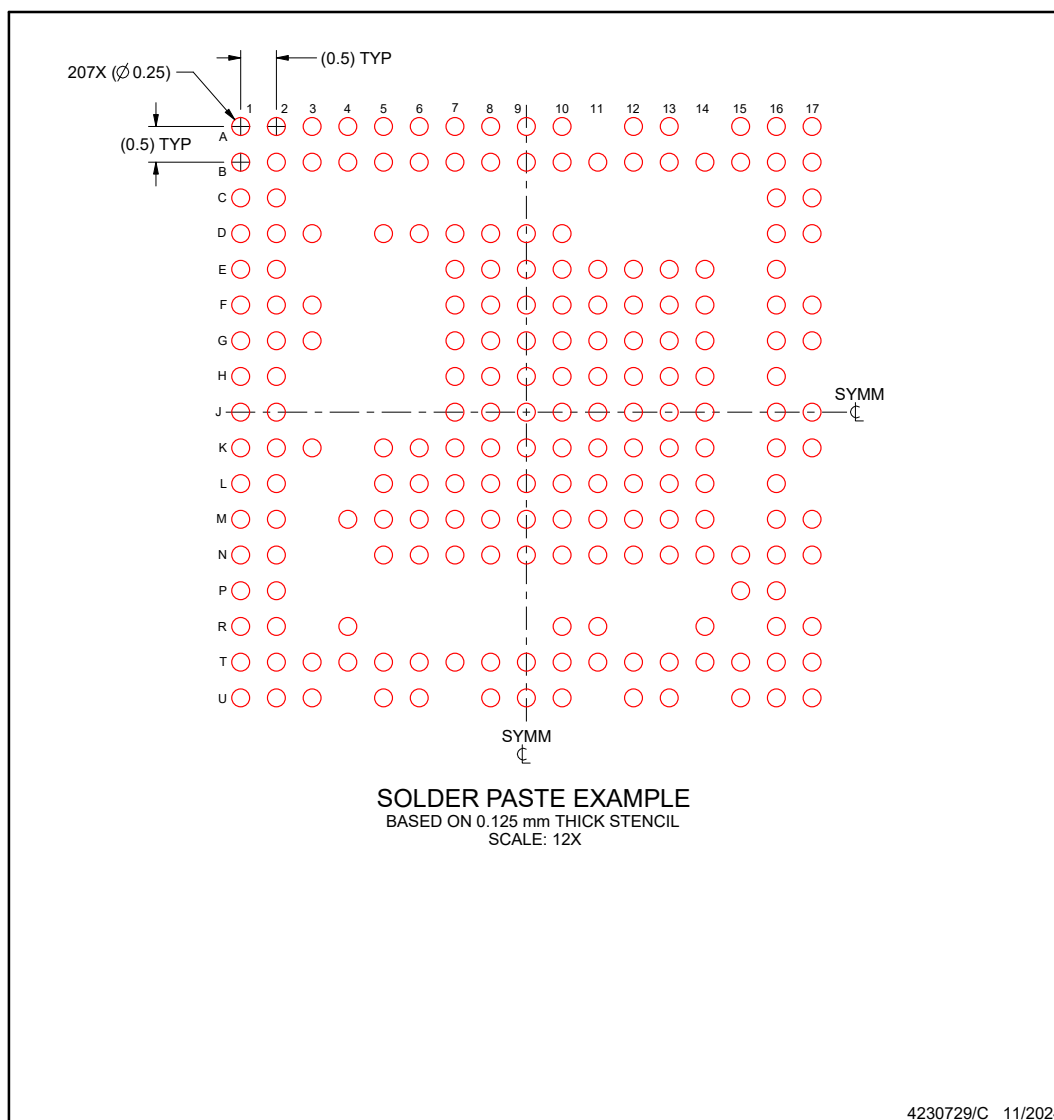


NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN**ANC0207A****FCCSP - 1.044 mm max height**

PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-------------------|------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| XA6844DBGANC | Active | Preproduction | FCCSP (ANC) 207 | 96 JEDEC TRAY (10+1) | - | Call TI | Call TI | -40 to 140 | |
| XA6844DBGANC.B | Active | Preproduction | FCCSP (ANC) 207 | 96 JEDEC TRAY (10+1) | - | Call TI | Call TI | -40 to 140 | |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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