SMBus-Controlled Multi-Chemistry Battery Charger With Input Current Detect Comparator and Charge Enable Pin

Check for Samples: bq24745

FEATURES

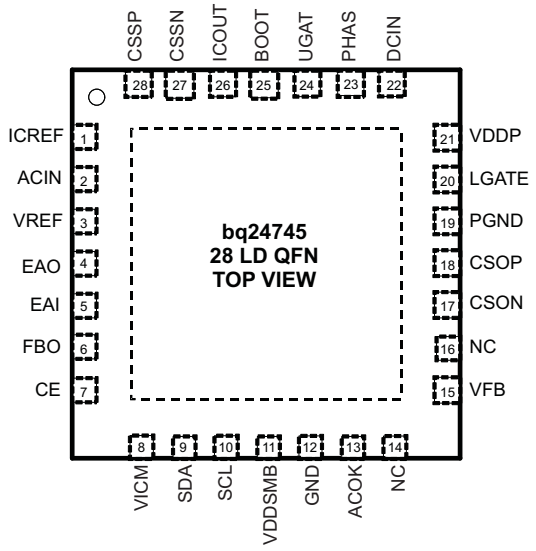
- NMOS-NMOS Synchronous Buck Converter with 300-kHz Frequency and >95% Efficiency
- 30-ns Minimum Driver Dead-Time and 99.5% Maximum Effective Duty Cycle
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
  - ±2% Input Current Sense Amp Accuracy
- Integration
  - Input Current Comparator, With Adjustable Threshold and Hysteresis
  - Internal Soft-Start
- Safety
  - Dynamic Power Management (DPM)
- Up to 19.2-V Battery Voltage
- 7-V–24-V AC/DC-Adapter Operating Range
- Simplified SMBus Control Interface
  - Charge Voltage DAC (1.024 V–19.2 V)
  - Charge Current DAC (128 mA–8.064 A)
  - Adapter Current Limit DPM DAC (256 mA–11.008 A)
- Status and Monitoring Outputs
  - AC/DC Adapter Present With Adjustable Voltage Threshold
  - Input Current Comparator With Adjustable Threshold and Hysteresis
  - Current Sense Amplifier for Current Drawn From Input Source
- Charge Any Battery Chemistry: Li+, NiCd, NiMH, Lead Acid, Etc.
- Charge Enable Pin
- < 10-µA Battery Current With Adapter Removed
- < 1-mA Input DCIN Current With Adapter Present and Charge Disabled
- 28-Pin, 5-mm × 5-mm QFN Package

APPLICATIONS

- Notebook and Ultra-Mobile Computers
- Portable Data-Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Backup Systems

DESCRIPTION

The bq24745 is a high-efficiency, synchronous battery charger with an integrated input-current comparator, offering low component count for space-constrained, multi-chemistry battery-charging applications. The input-current, charge-current, and charge-voltage DACs allow very high regulation accuracies that can be easily programmed by the system power-management microcontroller using the SMBus interface. The bq24745 charges two, three, or four series Li+ cells, and is available in a 28-pin, 5-mm × 5 mm QFN package.



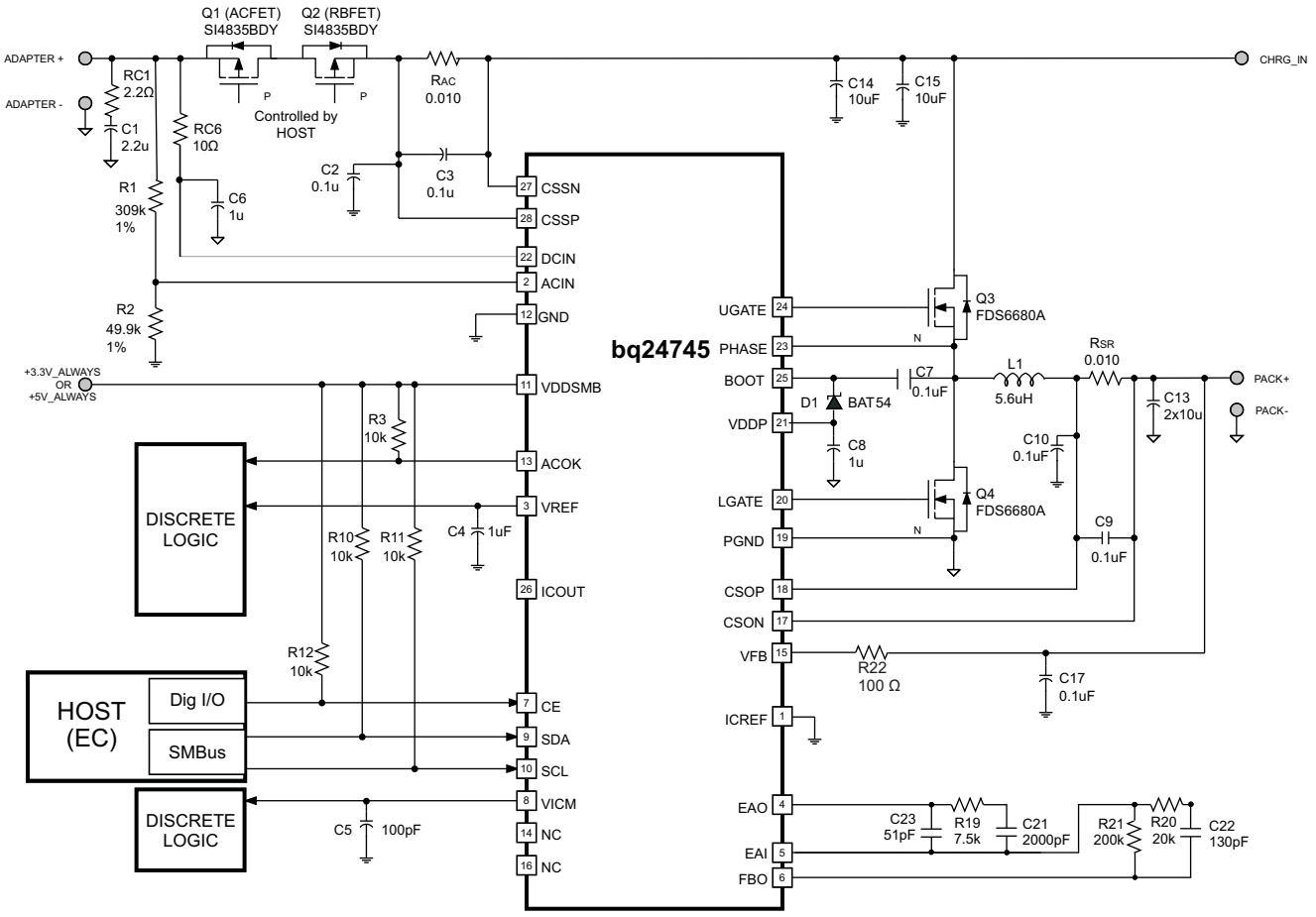
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The bq24745 features dynamic power management (DPM) and input power limiting. These features reduce battery-charge current when the input power limit is reached to avoid overloading the ac adaptor when supplying the load and the battery charger simultaneously. A highly accurate current-sense amplifier enables precise measurement of input current from the ac adapter, allowing monitoring the overall system power. If the adapter current is above the programmed low-power threshold, a signal is sent to host so that the system optimizes its performance to the power available from the adapter. An integrated comparator monitors the input current through the current-sense amplifier, and indicates when the input current exceeds a programmable threshold limit.

TYPICAL APPLICATIONS

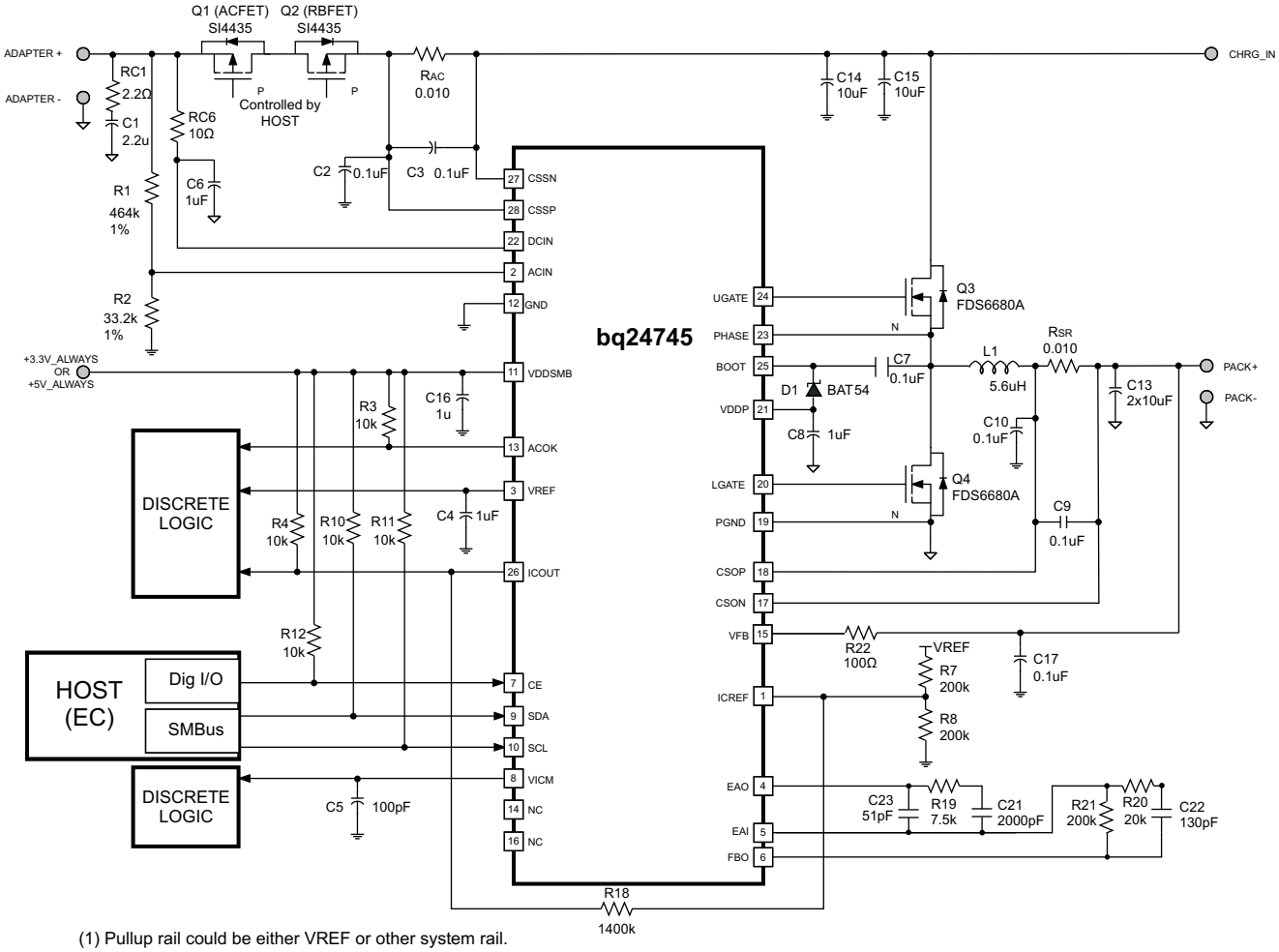
V_{IN} = 20 V, V_{BAT} = 4-cell Li-Ion, I_{CHARGE} = 4.5 A



(1) Pullup rail could be either VREF or other system rail.

Figure 1. Typical System Schematic Using External Input-Current Comparator (Discrete Logic) Instead of Internal Comparator

V_{IN} = 20 V, V_{BAT} = 4-cell Li-Ion, I_{CHARGE} = 4.5 A, $VICM_{er\_limit}$ = 6 A, for ICOUT Input Current comparator.



(1) Pullup rail could be either VREF or other system rail.

Figure 2. Typical System Schematic Using Internal Input-Current Comparator

ORDERING INFORMATION

PART NUMBER	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24745	28-pin 5-mm × 5-mm QFN	bq24745RHDR	3000
		bq24745RHDT	250

PACKAGE THERMAL DATA

PACKAGE	θ_{JA}	T_A = 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN – RHD(1)	36°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Table 1. PIN FUNCTIONS – 28-PIN QFN

PIN		FUNCTION
NO.	NAME	
1	ICREF	Input-current comparator voltage reference input. Connect a resistor divider from VREF to ICREF and from ICREF to GND to program the reference for the ICOUT comparator. The ICREF pin voltage is compared to the VICM pin voltage and the logic output is given on the ICOUT open-drain pin. Connecting a positive feedback resistor from the ICREF pin to the ICOUT pin programs the hysteresis.
2	ACIN	Adapter-detected voltage-set input. Program the adapter-detect threshold by connecting a resistor divider from the adapter input to ACIN pin to GND. Adapter voltage is detected if the ACIN-pin voltage is greater than 2.4 V. The VICM current-sense amplifier, ICOUT comparator, and ACOK output are active when the ACIN pin voltage is greater than 0.6 V.
3	VREF	3.3-V regulated voltage output. Place a 1-µF ceramic capacitor from VREF to the GND pin close to the IC. This voltage could be used for ratiometric programming of voltage and current regulation and for programming the ICREF threshold.
4	EAO	Error amplifier output for compensation. Connect the feedback-compensation components from EAO to EAI. Typically, a capacitor in parallel with a series resistor and capacitor. This node is internally compared to the PWM sawtooth oscillator signal.
5	EAI	Error amplifier input for compensation. Connect the feedback compensation components from EAI to EAO. Connect the input compensation from FBO to EAI.
6	FBO	Feedback output for compensation. Connect the input compensation from FBO to EAI. Typically, a resistor in parallel with a series resistor and capacitor.
7	CE	Charge enable active-high logic input. HI enables charge. LO disables charge.
8	VICM	Adapter current-sense-amplifier output. The VICM voltage is 20 times the differential voltage across CSSP-CSSN. Place a 100-pF (max) or less ceramic decoupling capacitor from VICM to GND.
9	SDA	SMBus data input. Connect to the SMBus data line from the host controller. A 10-kΩ pullup resistor to the host controller power rail is needed.
10	SCL	SMBus clock input. Connect to the SMBus clock line from the host controller. A 10-kΩ pullup resistor to the host controller power rail is needed.
11	VDDSMB	Input voltage for SMBus logic. Connect a 3.3-V supply rail or 5-V rail to the VDDSMB pin. Connect a 0.1-µF ceramic capacitor from VDDSMB to GND for decoupling.
12	GND	Analog ground. On PCB layout, connect to the analog ground plane, and only connect to PGND through the thermal pad underneath the IC.
13	ACOK	Valid adapter active-high detect logic open-drain output. Pulled HI when Input voltage is above the ACIN programmed threshold. Connect a 10-kΩ pullup resistor from the ACOK pin to pull up the supply rail.
14	NC	No connect. Pin floating internally.
15	VFB	Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal to the VFB pin to sense the battery pack voltage accurately. Place a 0.1-µF capacitor from VFB to GND close to the IC to filter high-frequency noise.
16	NC	No Connect. Pin floating internally.
17	CSON	Charge-current sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from the CSON pin to GND for common-mode filtering. A 0.1-µF ceramic capacitor is placed from CSON to CSOP to provide differential-mode filtering.
18	CSOP	Charge-current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from CSOP pin to GND for common-mode filtering. A 0.1-µF ceramic capacitor is placed from CSON to CSOP to provide differential-mode filtering.
19	PGND	Power ground. On PCB layout, connect directly to the source of the low-side power MOSFET, and to the to ground connection of the input and output capacitors of the charger. Only connect to GND through the thermal pad underneath the IC.
20	LGATE	PWM low-side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
21	VDDP	PWM low-side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from VDDP to the PGND pin, close to the IC. Use for high-side driver bootstrap voltage by connecting a small signal Schottky diode from VDDP to BOOT.
22	DCIN	IC-power positive supply. Connect to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse blocking power P-channel MOSFET. Place a 1-µF ceramic capacitor from DCIN to the GND pin close to the IC. Place a 10-Ω resistor from the adapter input to the DCIN pin to limit inrush current.
23	PHASE	PWM high-side driver negative supply. Connect to the phase-switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-µF bootstrap capacitor from PHASE to BOOT.
24	UGATE	PWM high-side driver output. Connect to the gate of the high-side power MOSFET with a short trace.

Table 1. PIN FUNCTIONS – 28-PIN QFN (continued)

PIN		FUNCTION
NO.	NAME	
25	BOOT	PWM high-side driver positive supply. Connect a 0.1-µF bootstrap ceramic capacitor from BOOT to PHASE. Connect a small bootstrap Schottky diode from VDDP to BOOT.
26	ICOUT	Input-current comparator active-high open-drain logic output. Place a 10-kΩ pullup resistor from the ICOUT pin to the pullup voltage rail. Place a positive-feedback resistor from the ICOUT pin to the ICREF pin for programming hysteresis. The output is HI when the VICM pin voltage is lower than the ICREF pin voltage. The output is LO when VICM pin voltage is higher than ICREF pin voltage.
27	CSSN	Adapter current-sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from the CSSN pin to GND for common-mode filtering. A 0.1-µF ceramic capacitor is placed from CSSN to CSSP to provide differential-mode filtering.
28	CSSP	Adapter current-sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from the CSSP pin to GND for common-mode filtering. A 0.1-µF ceramic capacitor is placed from CSSN to CSSP to provide differential-mode filtering.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Voltage range	DCIN, CSOP, CSON, CSSP, CSSN, VFB, ACOK	–0.3 to 30	V
	PHASE	–1 to 30	
	EAI, EAO, FBO, VDDP, LGATE, ACIN, VICM, ICOUT, ICREF, CE	–0.3 to 7	
	VDDSMB, SDA, SCL	–0.3 to 6	
	VREF	–0.3 to 3.6	
	BOOT, UGATE with respect to GND and PGND	–0.3 to 36	
Maximum difference voltage: CSOP–CSON, CSSP–CSSN		–0.5 to 0.5	
Junction temperature range		–40 to 155	°C
Storage temperature range		–55 to 155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, and negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	PHASE	–0.7		24	V
	DCIN, CSOP, CSON, CSSP, CSSN, VFB, ACOK	0		24	
	VDDP, LGATE	0		6.5	
	VREF			3.3	
	EAI, EAO, FBO, ACIN, VICM, ICOUT, ICREF, CE	0		5.5	
	BOOT, UGATE with respect to GND and PGND	0		30	
	VDDSMB, SDA, SCL	0		5.5	
Maximum difference voltage: CSOP–CSON, CSSP–CSSN		–0.3		0.3	
Junction temperature range		–40		125	°C
Storage temperature range		–55		150	°C

ELECTRICAL CHARACTERISTICS

7 V ≤ V_{DCIN} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{DCIN_OP}	DCIN input-voltage operating range		7		24	V
CHARGE VOLTAGE REGULATION						
V_{VFB_OP}	VFB input-voltage range		0		DCIN	V
$V_{VFB\_REG\_ACC}$	VFB charge-voltage regulation accuracy	ChargeVoltage() = 0x41A0	16.716	16.8	16.884	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x3130	12.529	12.592	12.655	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x20D0	8.350	8.4	8.450	V
			–0.6%		0.6%	
		ChargeVoltage() = 0x1060	4.154	4.192	4.230	V
			–0.9%		0.9%	
$V_{VFB\_REG\_RNG}$	Charge-voltage regulation range	T_J = 0 to 125°C, 1.024 V–19.2 V, Max DAC value is 19.2 V	1.024		19.2	V
CHARGE CURRENT REGULATION						
$V_{IREG\_CHG\_RNG}$	Charge-current regulation differential-voltage range	V_{IREG_CHG} = V_{CSOP} – V_{CSON}, max. DAC value is 80.64 mV	0		80.64	mV
$I_{CHRG\_REG\_ACC}$	Charge-current regulation accuracy	ChargeCurrent() = 0x0F80		3968		mA
			–3%		3%	
		ChargeCurrent() = 0x0800		2048		mA
			–5%		5%	
		ChargeCurrent() = 0x0200		512		mA
			–25%		25%	
		ChargeCurrent() = 0x0080		128		mA
			–33%		33%	
INPUT CURRENT REGULATION						
$V_{IREG\_DPM\_RNG}$	Adapter-current regulation differential-voltage range	V_{IREG_DPM} = V_{CSSP} – V_{CSSN}, max. DAC value is 110.084 mV	0		110.1	mV
$I_{INPUT\_REG\_ACC}$	Input-current regulation accuracy	InputCurrent() ≥ 0x0800		4096		mA
			–3%		3%	
		InputCurrent() = 0x0400		2048		mA
			–5%		5%	
		InputCurrent() = 0x0100		512		mA
			–25%		25%	
		InputCurrent() = 0x0080		256		mA
			–33%		33%	
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{ACIN} > 0.6 V, 0 – 30 mA	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, V_{ACIN} > 0.6 V	35		80	mA
VDDP REGULATOR						
V_{VDDP_REG}	VDDP regulator voltage	V_{ACIN} > 0.6 V, 0 – 50 mA	5.7	6	6.3	V
I_{VDDP_LIM}	VDDP current limit	V_{VDDP} = 0 V, V_{ACIN} > 0.6 V	90		135	mA
		V_{VDDP} = 5 V, V_{ACIN} > 0.6 V	80			

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{DCIN} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADAPTER CURRENT SENSE AMPLIFIER						
V_{CSSP/N_OP}	Input common-mode range	Voltage on CSSP/CSSN	0		24	V
V_{VICM}	VICM output-voltage range		0		2.25	V
I_{VICM}	VICM output current		0		1	mA
A_{VICM}	Current-sense amplifier voltage gain	A_{VICM} = V_{VICM}/ V_{IREG_DPM}		20		V/V
	Adapter-current sense accuracy	V_{IREG_DPM} = V(CSSP–CSSN) ≥ 40 mV	–2%		2%	
		V_{IREG_DPM} = V(CSSP–CSSN) = 20 mV	–3%		3%	
		V_{IREG_DPM} = V(CSSP–CSSN) = 5 mV	–25%		25%	
		V_{IREG_DPM} = V(CSSP–CSSN) = 1.5 mV	–33%		33%	
I_{VICM_LIM}	Output-current limit	V_{VICM} = 0 V	1			mA
C_{VICM_MAX}	Maximum output load capacitance	For stability with 0-mA to 1-mA load			100	pF
ACIN COMPARATOR INPUT UNDERVOLTAGE)						
$V_{DCIN\_VFB\_OP}$	Differential voltage from DCIN to VFB		–20		24	V
V_{ACIN_CHG}	ACIN rising threshold	Min. voltage to enable charging, V_{ACIN} rising	2.376	2.4	2.424	V
$V_{ACIN\_CHG\_HYS}$	ACIN falling hysteresis	V_{ACIN} falling		40		mV
	ACIN rising deglitch(1)	V_{ACIN} rising	50	100	150	µs
	ACIN falling deglitch	V_{ACIN} falling		1		µs
V_{ACIN_BIAS}	Adapter present rising threshold	Min voltage to enable all bias, V_{ACIN} rising	0.56	0.62	0.68	V
$V_{ACIN\_BIAS\_HYS}$	Adapter present falling hysteresis	V_{ACIN} falling		20		mV
	ACIN rising deglitch (1)	V_{ACIN} rising		200		µs
	ACIN falling deglitch	V_{ACIN} falling		1		
DCIN / VFB COMPARATOR (REVERSE DISCHARGING PROTECTION)						
$V_{DCIN-VFB\_FALL}$	DCIN to VFB falling threshold	V_{DCIN} – V_{VFB} to turn off ACFET	140	185	240	mV
$V_{DCIN-VFB\_\_HYS}$	DCIN to VFB hysteresis			50		mV
	DCIN to VFB rising deglitch	V_{DCIN} – V_{VFB} > $V_{DCIN-VFB\_RISE}$		1		ms
	DCIN to VFB falling deglitch	V_{DCIN} – V_{VFB} < $V_{DCIN-VFB\_FALL}$		3.3		µs
VFB OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Overvoltage rising threshold	As percentage of V_{VFB_REG}		104		%
V_{OV_FALL}	Overvoltage falling threshold	As percentage of V_{VFB_REG}		102		
VFB SHORT (UNDERVOLTAGE and TRICKLE CHARGE) COMPARATOR						
$V_{VFB\_SHORT\_RISE}$	VFB short rising threshold		2.6	2.7	2.9	V
$V_{VFB\_SHORT\_HYS}$	VFB short falling hysteresis			215		mV
	VFB short rising deglitch	V_{VFB} > V_{VFB_SHORT} + $V_{VFB\_SHORT\_HYS}$ Detection delay		1.5		µs
	VFB short falling deglitch	V_{VFB} < V_{VFB_SHORT}		3.3		µs
$I_{TRKL\_REG\_ACC}$	Trickle-charge current-regulation accuracy in BATSHORT	V_{VFB} < V_{VFB_SHORT}	60	200	300	mA
$I_{LOW\_MAX\_REG}$	Maximum charge current regulation at low voltage (<4 V)	V_{VFB_SHORT} < V_{VFB} < 4		3		A
CHARGE OVERCURRENT COMPARATOR						
V_{OC}	Charge overcurrent falling threshold	As percentage of I_{REG_CHG}		145%		
	Minimum current limit (CSOP–CSON)			50		mV
	Internal filter pole frequency			160		kHz
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
UVLO	AC undervoltage rising threshold	Measure on DCIN pin	3.5	4	4.5	V
V_{UVLO_HYS}	AC undervoltage hysteresis, falling			260		mV
INPUT CURRENT COMPARATOR						
V_{ICCOMP_OFFSET}	Input current-comparator offset voltage		-6.8	0.12	6.8	mV

(1) Verified by design.

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{DCIN} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling			20		
PWM HIGH SIDE DRIVER (UGATE)						
$R_{DS\_HI\_ON}$	High-side driver (HSD) turnon resistance	V_{BOOT} – V_{PHASE} = 5.5 V			6	Ω
$R_{DS\_HI\_OFF}$	High-side driver turnoff resistance	V_{BOOT} – V_{PHASE} = 5.5 V			1	Ω
$V_{BOOT\_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BOOT} – V_{PHASE} when low-side refresh pulse is requested	4			V
I_{BOOT_LEAK}	BOOT leakage current when charge enabled	High side is on; charge enabled			200	µA
PWM LOW SIDE DRIVER (LGATE)						
$R_{DS\_LO\_ON}$	Low-side driver (LSD) turnon resistance				6	Ω
$R_{DS\_LO\_OFF}$	Low-side driver turnoff resistance				1	Ω
PWM DRIVERS TIMING						
	Driver dead time	Dead time when switching between LGATE and UGATE , no load at LGATE and UGATE	30			ns
PWM OSCILLATOR						
F_{SW}	PWM switching frequency		240		360	kHz
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of DCIN		6.67		%DCIN
QUIESCENT CURRENT						
I_{OFF_STATE}	Total off-state battery current from CSOP, CSON, VFB, DCIN, BOOT, PHASE, etc	V_{VFB} = 16.8 V, V_{ACIN} < 0.6 V, V_{DCIN} > 5 V, 0°C ≤ T_J ≤ 85°C		7	10	µA
I_{BAT_ON}	Battery on-state quiescent current	V_{VFB} = 16.8 V, 0.6V < V_{ACIN} < 2.4 V, V_{DCIN} > 5 V		0.7	1	mA
$I_{BAT\_LOAD\_CD}$	Internal battery load current, charge disabled	Charge is disabled: V_{VFB} = 16.8 V, V_{ACIN} > 2.4 V, V_{DCIN} > 5 V		0.7	1	mA
$I_{BAT\_LOAD\_CE}$	Internal battery load current, charge enabled	Charge is enabled: V_{VFB} = 16.8 V, V_{ACIN} > 2.4 V, V_{DCIN} > 5 V	6	10	12	mA
I_{AC}	Adapter quiescent current	Charge disabled, V_{DCIN} = 20 V		0.7	1	mA
I_{AC_SWITCH}	Adapter switching quiescent current	Charge enabled, V_{DCIN} = 20 V, converter running		25		mA
INTERNAL SOFT START (8 Steps to Regulation Current ICHG)						
	Soft-start steps			8		step
	Soft-start step time			1.5		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power up	Delay from when adapter is detected to when the charger is allowed to turn on		1.5		ms
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE SYNCHRONOUS TO NON-SYNCHRONOUS)						
V_{UCP}	Cycle-by-cycle synchronous to non-synchronous transition threshold	Cycle-by-cycle, (CSOP-CSON) voltage, falling, LGATE turns off and latches off until next cycle	5	10	15	mV
	Blankout time after LGATE turns on	Blankout comparator after LGATE turns on		100		ns
LOGIC INPUT PIN CHARACTERISTICS (CE)(2) Pull-up CE with ≥2.2 kΩ resistor or directly to VREF.						
V_{IN_LO}	Input low-threshold voltage				0.8	V
V_{IN_HI}	Input high-threshold voltage		2.1			
V_{BIAS}	Input bias current	V = 0 TO V_{VDDP}			1	µA
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS (ACOK, ICOUT)						
V_{OUT_LO}	Output low saturation voltage	Sink current = 5 mA			0.5	V
VDDSMB INPUT SUPPLY FOR SMBus						
V_{VDDSMB_RANGE}	VDDSMB input voltage range		2.7		5.5	V
$V_{VDDSMB\_UVLO\_Threshold\_Rising}$	VDDSMB undervoltage lockout threshold voltage, rising	V_{VDDSMB} rising	2.4	2.5	2.6	V
$V_{VDDSMB\_UVLO\_Hyst\_Rising}$	VDDSMB undervoltage lockout hysteresis voltage, falling	V_{VDDSMB} falling	100	150	200	V

(2) Pull up CE with ≥ 2-kΩ resistor, or connect directly to VREF.

ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{DCIN} ≤ 24 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVDDSMB_Iq	VDDSMB quiescent current	V_{VDDSMB} = SCL = SDA = 5.5 V, 0°C ≤ T_J ≤ 85°C		20	27	µA

ELECTRICAL CHARACTERISTICS

7 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, –20°C<T_J <125°C, ref = AGND (unless otherwise noted)(1)

PARAMETER [SMB TIMING SPECIFICATION (VDD = 2.7 V to 5.5 V) (see Figures 4 and 5)]		MIN	TYP	MAX	UNIT
SMBus TIMING CHARACTERISTICS					
t_R	SCLK/SDATA rise time			1	µs
t_F	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse duration high	4		50	µs
$t_{W(L)}$	SCLK pulse duration low	4.7			µs
$t_{SU(STA)}$	Setup time for START condition	4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	4			µs
$t_{SU(DAT)}$	Data setup time	250			ns
$t_{H(DAT)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition	4.7			µs
$F_{S(CL)}$	Clock frequency	10		100	kHz
HOST COMMUNICATION FAILURE					
$t_{timeout}$	SMBus bus release timeout	22	25	35	ms
t_{WDI}	Watchdog timeout period	140	170	210	s
OUTPUT BUFFER CHARACTERISTICS					
$V_{(SDAL)}$	Output LO voltage at SDA, $I_{(SDA)}$ = 3 mA			0.4	V

(1) Devices participating in a transfer time out when any clock low exceeds the 2- ms minimum time-out period. Devices that have detected a time-out condition must reset the communication no later than the 35-ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified, as it incorporates the cumulative stretch limit for both a master (10 ms) and a slave (25 ms).

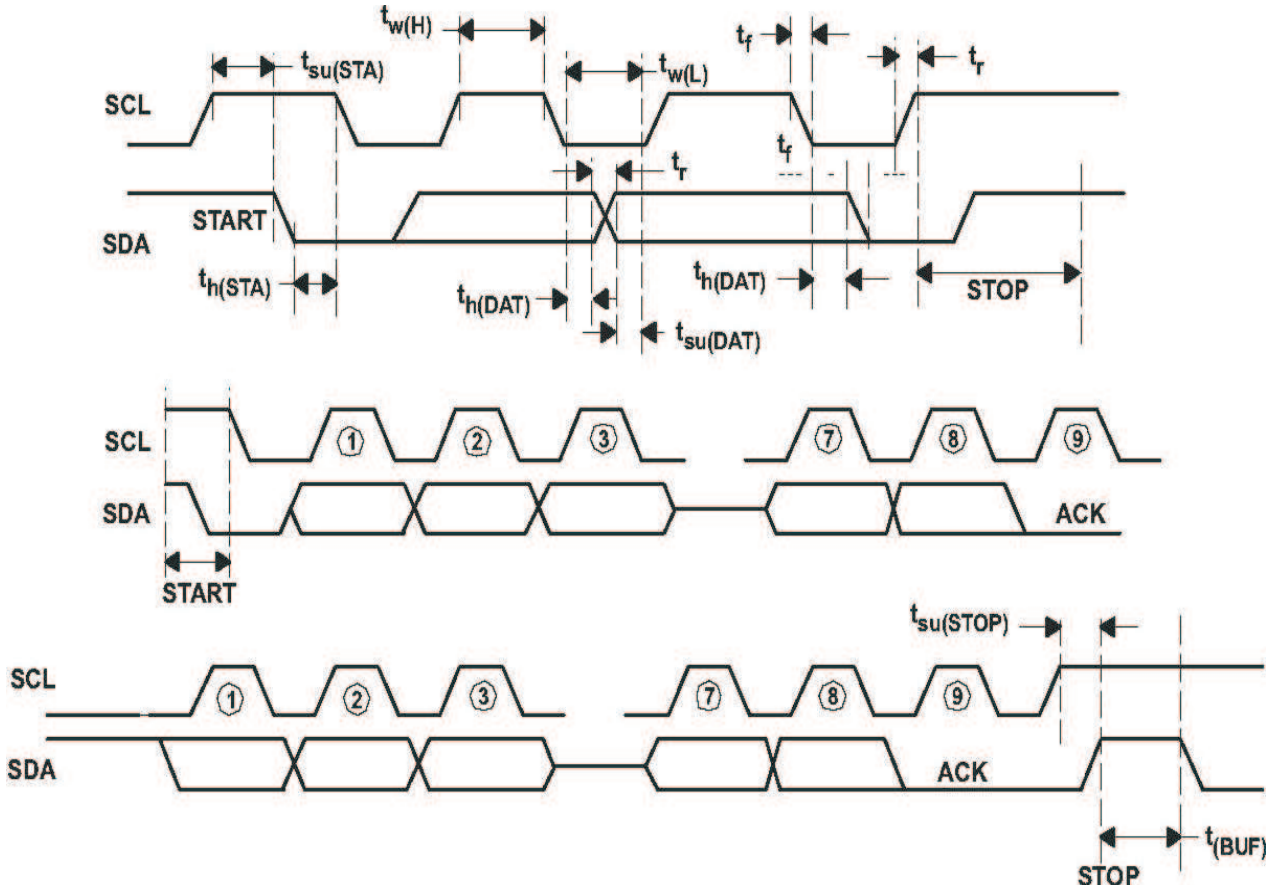


Figure 3. SMBus Communication Timing Waveforms

TYPICAL CHARACTERISTICS

VREF LOAD AND LINE REGULATION vs LOAD CURRENT

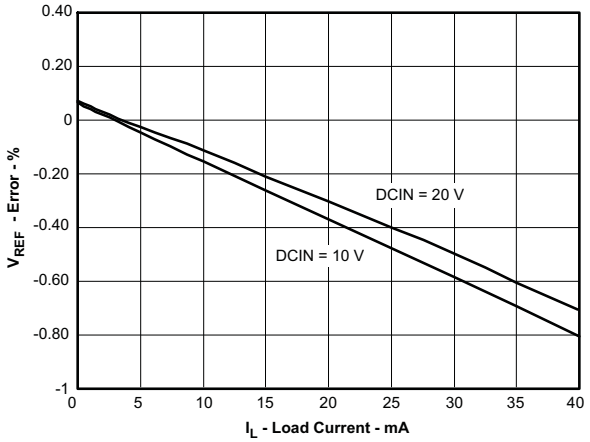


Figure 4.

VDDP LOAD AND LINE REGULATION vs LOAD CURRENT

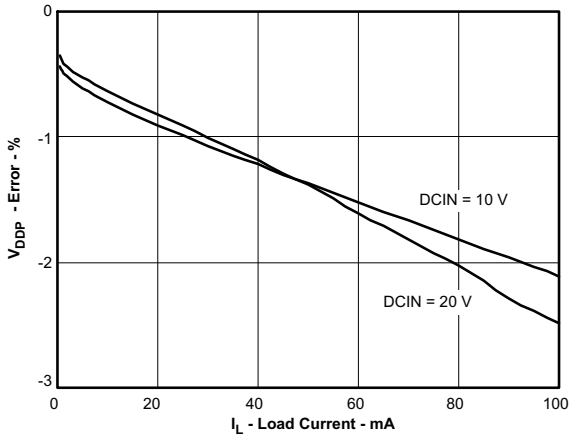


Figure 5.

TYPICAL CHARACTERISTICS (continued)

VFB (BATTERY) VOLTAGE REGULATION ACCURACY vs CHARGE CURRENT

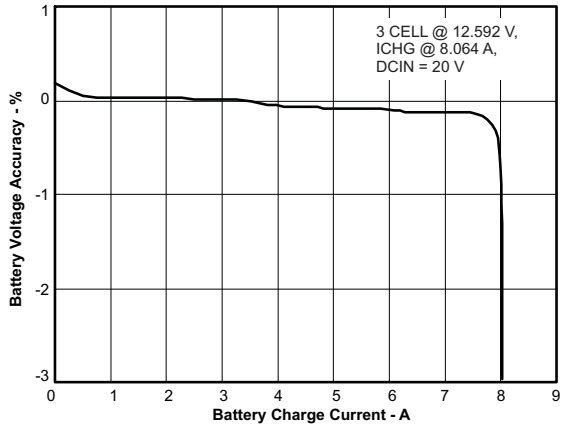


Figure 6.

VFB (BATTERY) VOLTAGE REGULATION ACCURACY vs DAC VBAT SETPOINT

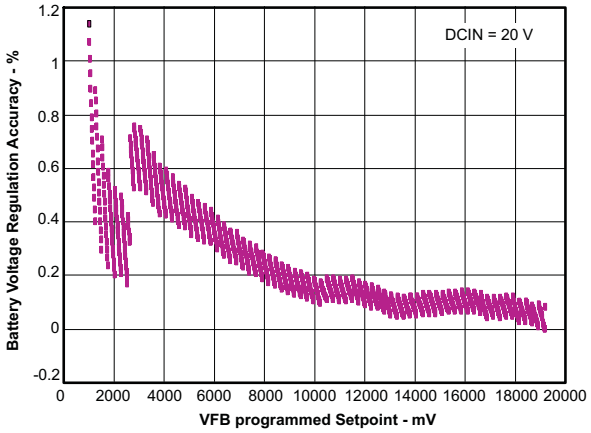


Figure 7.

CHARGE CURRENT REGULATION ACCURACY vs DAC ICHRG SETPOINT

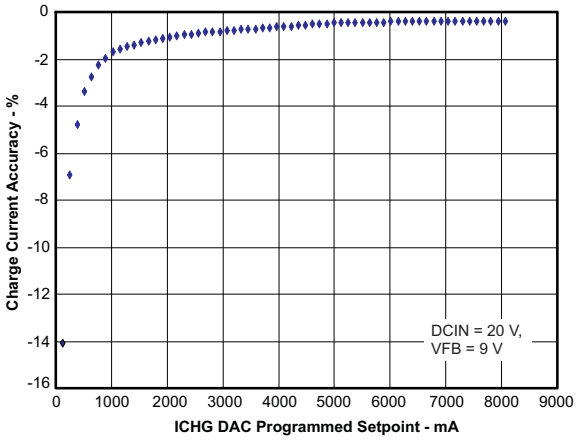


Figure 8.

CHARGE CURRENT REGULATION ACCURACY vs VFB (BATTERY) VOLTAGE

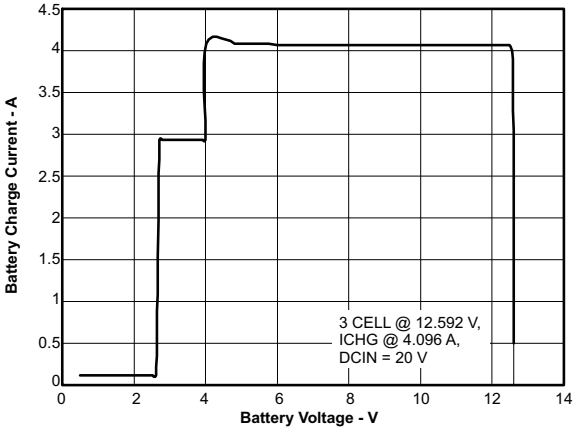


Figure 9.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT REGULATION (DPM) ACCURACY vs DAC IDPM SETPOINT

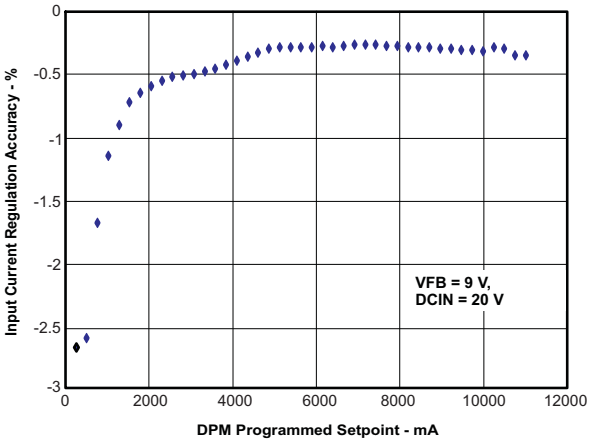


Figure 10.

VICM INPUT CURRENT-SENSE AMPLIFIER ACCURACY INPUT CHARGE CURRENT

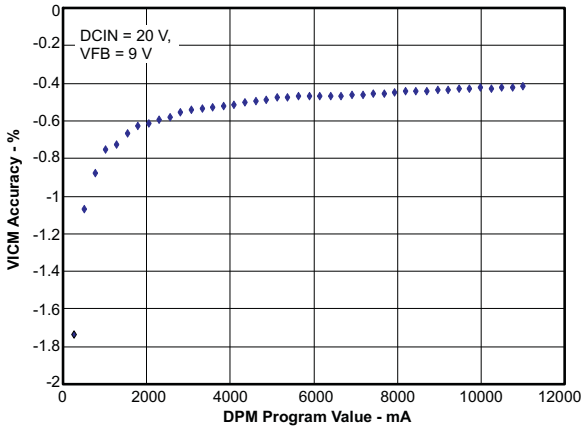


Figure 11.

INPUT CURRENT REGULATION (DPM) AND CHARGE CURRENT vs SYSTEM CURRENT

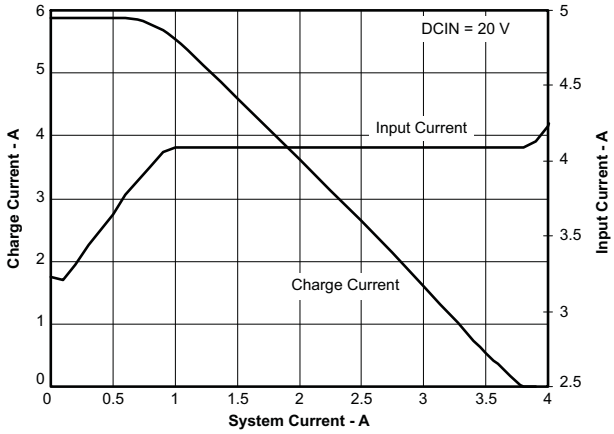


Figure 12.

INPUT CURRENT REGULATION (DPM) TRANSIENT SYSTEM LOAD RESPONSE CCM TO CCM

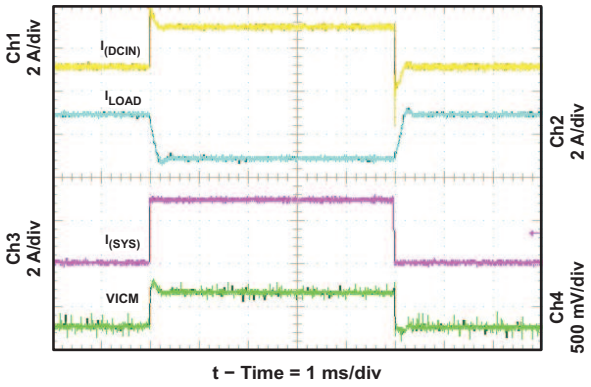


Figure 13.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT REGULATION (DPM) TRANSIENT
SYSTEM LOAD RESPONSE
CCM TO DCM

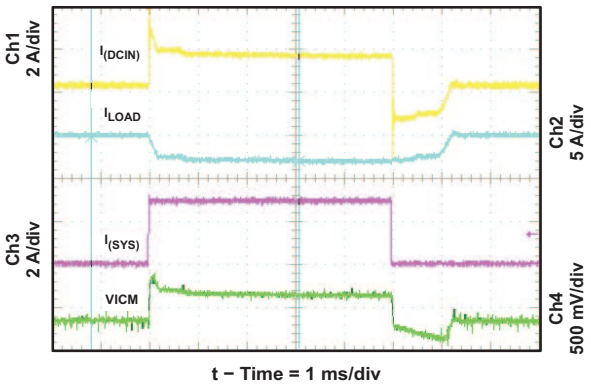


Figure 14.

CHARGE CURRENT REGULATION ACCURACY
VFB (BATTERY) VOLTAGE

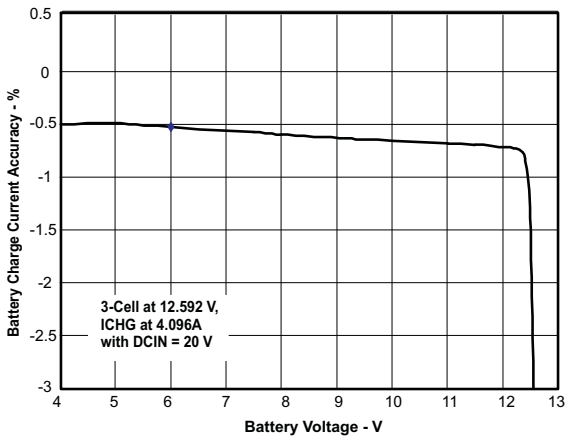


Figure 15.

EFFICIENCY
BATTERY CHARGE CURRENT

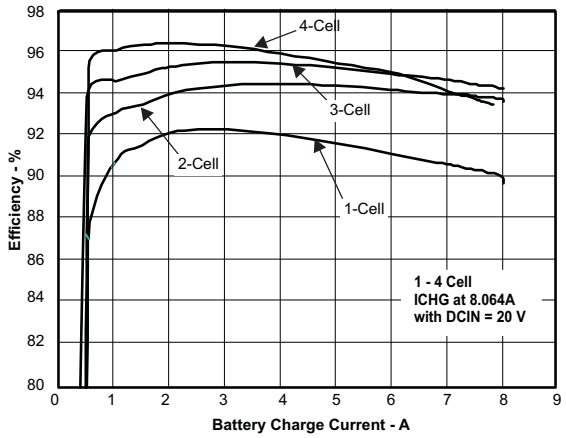


Figure 16.

BATTERY REMOVAL (From Constant-Current Mode)

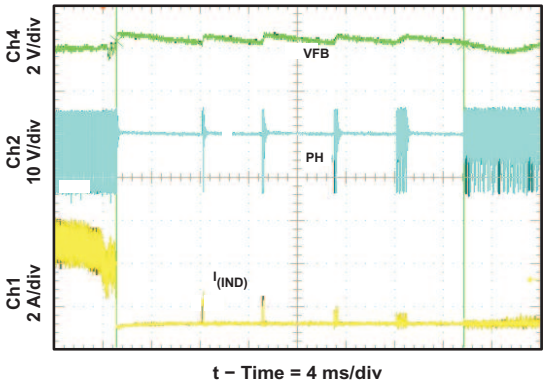


Figure 17.

CHARGER WHEN ADAPTER INSERTED

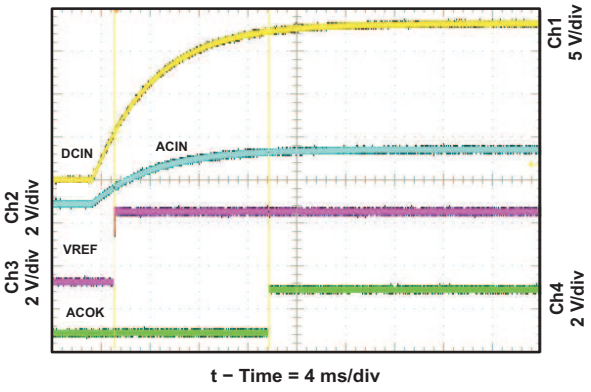


Figure 18.

ADAPTER REMOVED WHILE CHARGING

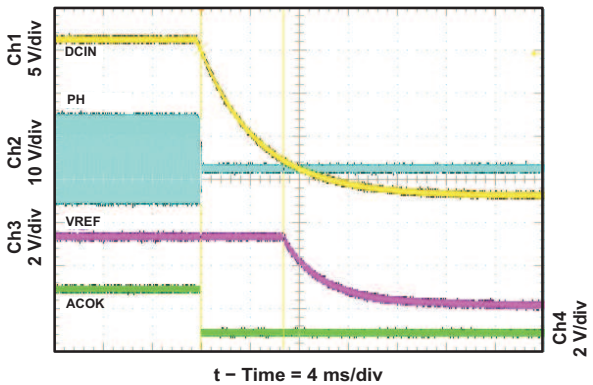
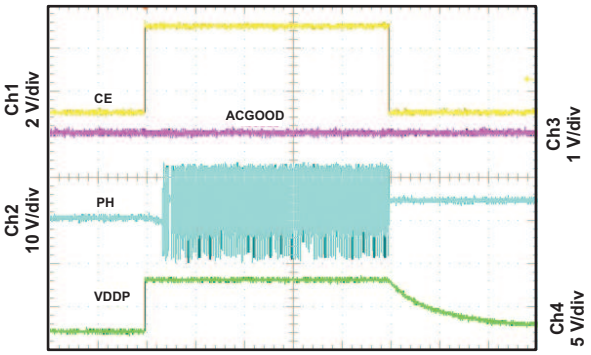


Figure 19.

TYPICAL CHARACTERISTICS (continued)

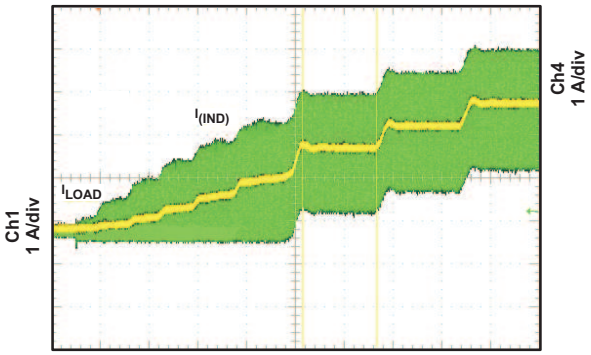
CHARGE ENABLE/DISABLE



t – Time = 10 ms/div

Figure 20.

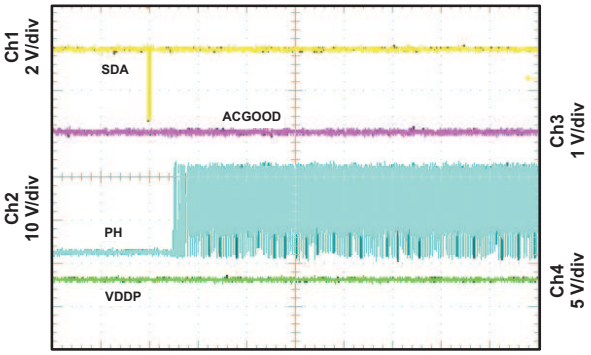
SOFT-START, INDUCTOR CURRENT AND CHARGE CURRENT



t – Time = 1 ms/div

Figure 21.

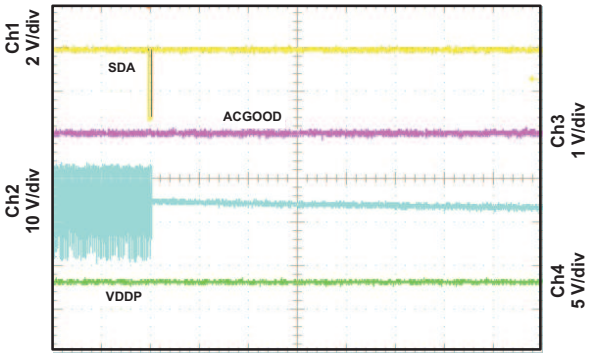
CHARGE ENABLED BY SMBus



t – Time = 10 ms/div

Figure 22.

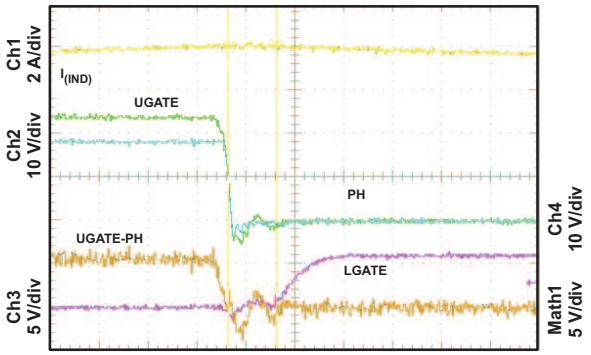
CHARGE DISABLED BY SMBus



t – Time = 10 ms/div

Figure 23.

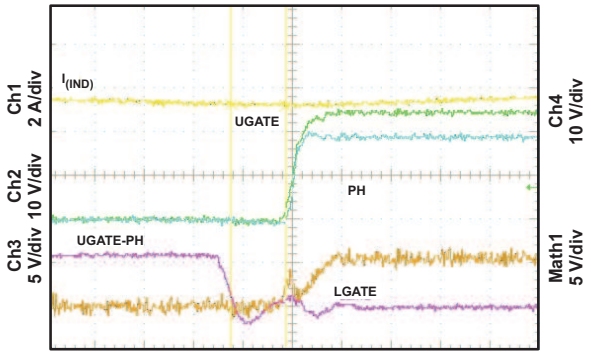
DEAD-TIME BETWEEN UGATE OFF AND LGATE ON



t – Time = 40 ns/div

Figure 24.

DEAD-TIME BETWEEN LGATE OFF AND UGATE ON



t – Time = 40 ns/div

Figure 25.

TYPICAL CHARACTERISTICS (continued)

NEAR 100% DUTY CYCLE BOOTSTRAP RECHARGE PULSE

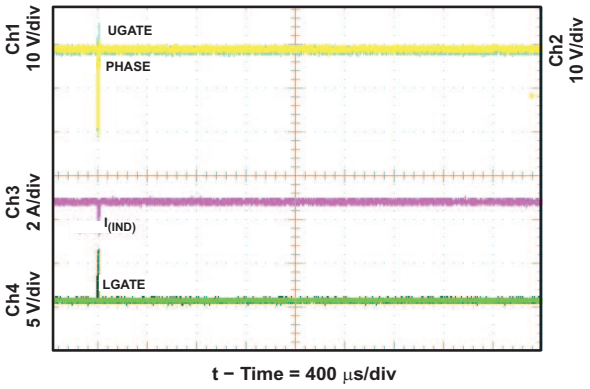


Figure 26.

BATTERY SHORTED CHARGER RESPONSE, OVERCURRENT PROTECTION (OCP) AND CHARGE CURRENT REGULATION

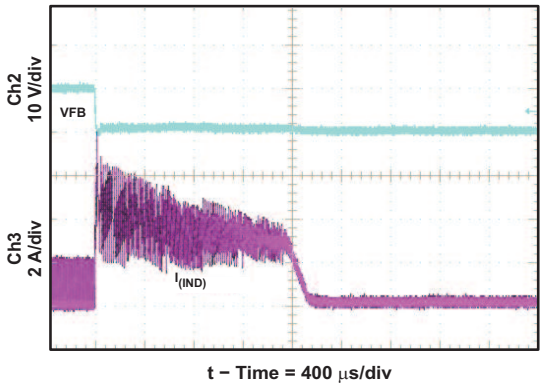


Figure 27.

CONTINUOUS CONDUCTION MODE (CCM) SWITCHING WAVEFORMS, ICHARGE = 3986 mA

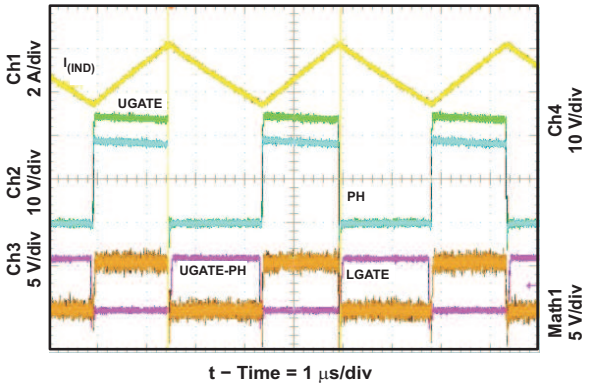


Figure 28.

DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING WAVEFORMS, ICHARGE = 256 mA

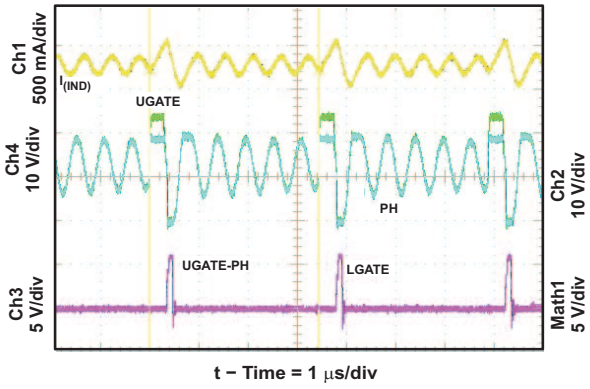


Figure 29.

OFF-STATE BATTERY CURRENT (LOW Iq) vs VFB (BATTERY) VOLTAGE

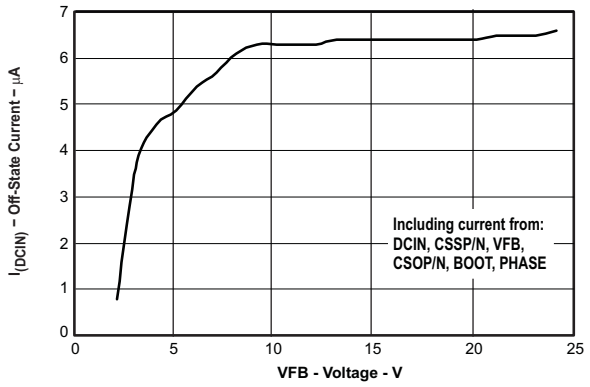


Figure 30.

OFF-STATE DCIN CURRENT (LOW Iq) vs DCIN INPUT VOLTAGE (With Adapter Connected)

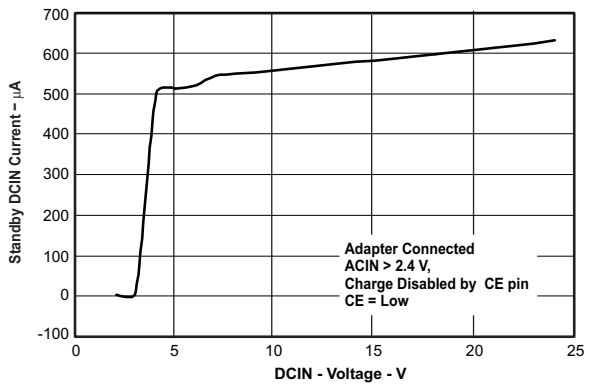


Figure 31.

TYPICAL CHARACTERISTICS (continued)

PROGRAMMABLE REFERENCE AND HYSTERESIS INPUT CURRENT COMPARATOR (With Pulsed Current)

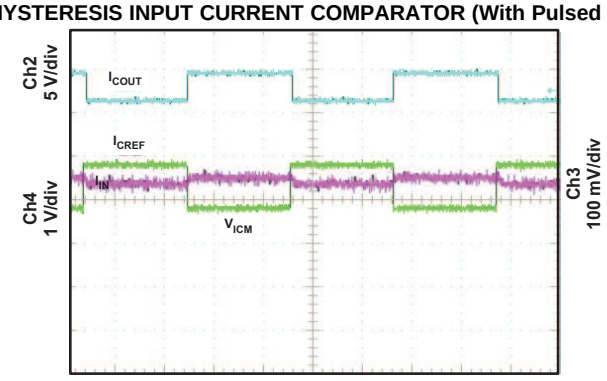
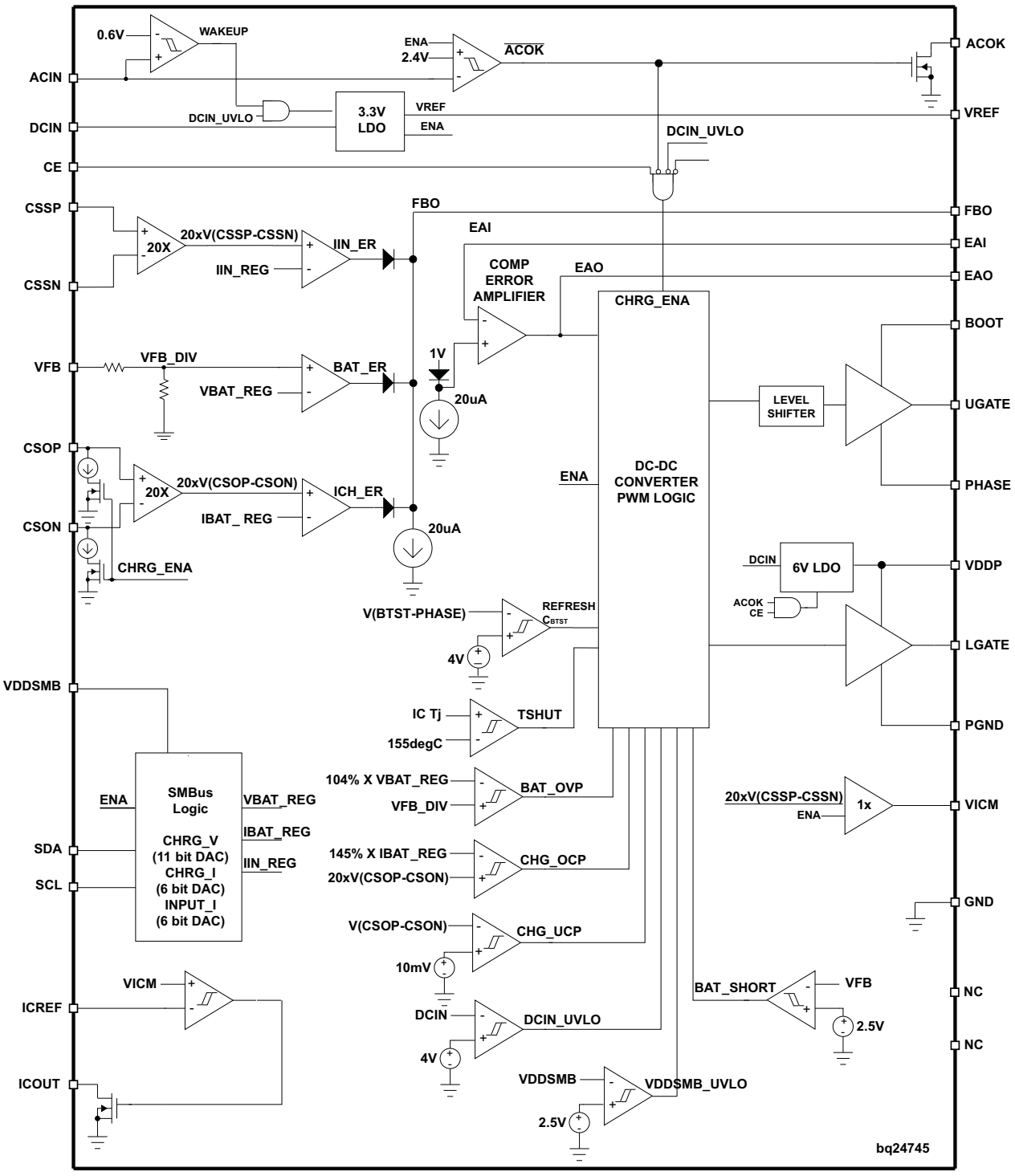


Figure 32.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

SMBus Interface

The bq24745 operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface.

Battery-Charger Commands

The bq24745 supports five battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2. ManufacturerID() and DeviceID() can be used to identify the bq24745. On the bq24745, the ManufacturerID() command always returns 0x0040 and the DeviceID() command always returns 0x0006.

Table 2. Battery Charger SMBus Registers

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	POR STATE	POR Voltage/Current
0x14	ChargeCurrent()	Read or write	6-bit charge-current setting	0x0000	0 mV
0x15	ChargeVoltage()	Read or write	11-bit charge-voltage setting	0x0000	0 mA
0x3F	InputCurrent()	Read or write	6-bit input-current setting	0x0080	256 mA (10-mΩ R_{AC})
0xFE	ManufacturerID()	Read-only	Manufacturer ID	0x0040	–
0xFF	DeviceID()	Read-only	Device ID	0x0006	–

SMBus

The bq24745 receives control inputs from the SMBus interface. The bq24745 uses a simplified subset of the commands documented in System Management Bus Specification V1.1, which can be downloaded from www.smbus.org. The bq24745 uses the SMBus Read-Word and Write-Word protocols (Figure 33) to communicate with the smart battery. The bq24745 performs only as an SMBus slave device with address 0b0001 001_ (0x12) and does not initiate communication on the bus. In addition, the bq24745 has two identification (ID) registers (0xFE): a 16-bit device ID register and a 16-bit manufacturer ID register (0xFF).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors (10 kΩ, typ.) for SDA and SCL to achieve rise times according to the SMBus specifications.

Communication starts when the master signals a START condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figure 34 and Figure 35 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the bq24745 because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

Preset to 0b0001001 D7 D0 D15 D8

ChargeCurrent() = 0x14
ChargeVoltage() = 0x15
InputCurrent() = 0x3F

b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

Preset to 0b0001001 Register Preset to 0b0001010 D7 D0 D15 D8

ChargeMode() = 0x14
ChargeMode() = 0x15
ChargeMode() = 0x3F

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 33. SMBus Write-Word and Read-Word Protocols

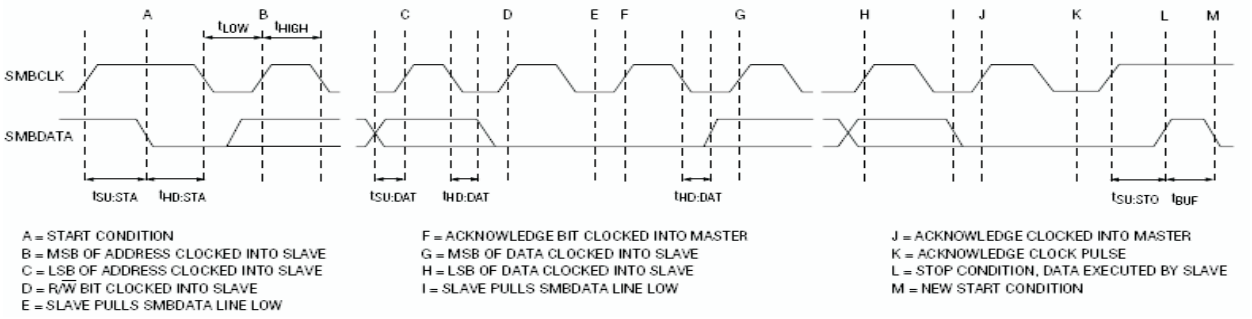
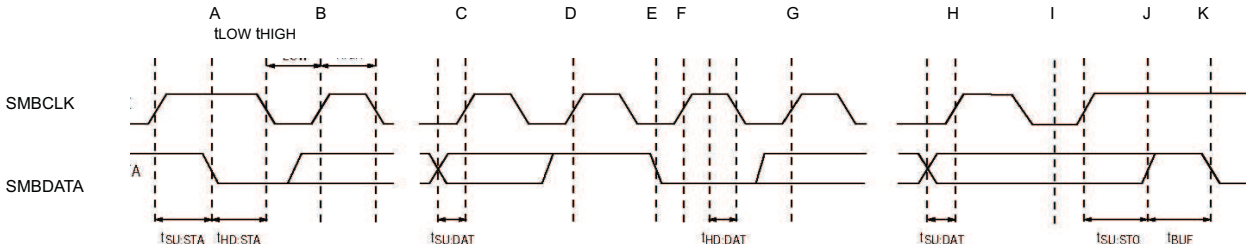


Figure 34. SMBus Write Timing



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/W BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO MASTER
H = LSB OF DATA CLOCKED INTO MASTER
I = ACKNOWLEDGE CLOCK PULSE
J = STOP CONDITION
K = NEW START CONDITION

Figure 35. SMBus Read Timing

BATTERY VOLTAGE REGULATION

The bq24745 uses a high-accuracy voltage regulator for charging voltage. The battery voltage regulation setting is programmed by the host microcontroller (µC), through the SMBus interface that sets an 11-bit DAC. The battery termination voltage is a function of the battery chemistry. Consult the battery manufacturer to determine this voltage.

The VFB pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, or directly on the output capacitor. A 0.1-µF ceramic capacitor from VFB to GND is recommended to be as close to the VFB pin as possible to decouple high-frequency noise.

To set the output charge-voltage regulation limit, use the SMBus to write a 16-bit ChargeVoltage() command using the data format listed in Table 3. The ChargeVoltage() command uses the Write-Word protocol (see Figure 33). The command code for ChargeVoltage() is 0x15 (0b0001 0101). The bq24745 provides a 1.024-V to 19.200-V charge voltage range, with 16-mV resolution. Setting ChargeVoltage() below 1.024 V or above 19.2 V clears the DAC and terminates charge.

On reset, the ChargeVoltage() and ChargeCurrent() values are cleared (0) and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() commands are sent. During reset, both high-side and low-side FETs remain off until the charger is started.

Table 3. Charge Voltage Register (0x15)

BIT	BIT NAME	DESCRIPTION
0	–	Not used
1	–	Not used
2	–	Not used
3	–	Not used
4	Charge voltage, DACV 0	0 = Adds 0 mV of charger voltage 1 = Adds 16 mV of charger voltage(1)
5	Charge voltage, DACV 1	0 = Adds 0 mV of charger voltage 1 = Adds 32 mV of charger voltage(1)
6	Charge voltage, DACV 2	0 = Adds 0 mV of charger voltage 1 = Adds 64 mV of charger voltage(1)
7	Charge voltage, DACV 3	0 = Adds 0 mV of charger voltage 1 = Adds 128 mV of charger voltage(1)
8	Charge voltage, DACV 4	0 = Adds 0 mV of charger voltage 1 = Adds 256 mV of charger voltage(1)
9	Charge voltage, DACV 5	0 = Adds 0 mV of charger voltage 1 = Adds 512 mV of charger voltage(1)
10	Charge voltage, DACV 6	0 = Adds 0 mV of charger voltage 1 = Adds 1,024 mV of charger voltage

(1) Must be used in conjunction with other bits for a minimum output of 1024 mV

Table 3. Charge Voltage Register (0x15) (continued)

BIT	BIT NAME	DESCRIPTION
11	Charge voltage, DACV 7	0 = Adds 0 mV of charger voltage 1 = Adds 2,048 mV of charger voltage
12	Charge voltage, DACV 8	0 = Adds 0 mV of charger voltage 1 = Adds 4,096 mV of charger voltage
13	Charge voltage, DACV 9	0 = Adds 0 mV of charger voltage 1 = Adds 8,192 mV of charger voltage
14	Charge voltage, DACV 10	0 = Adds 0 mV of charger voltage 1 = Adds 16,384 mV of charger voltage
15	–	Not used

CHARGE CURRENT REGULATION

The ChargeCurrent() SMBus 6-bit DAC register sets the maximum charging current. Battery current is sensed by resistor R_{SR} connected between the CSOP and CSON pins. The maximum full-scale differential voltage between CSOP and CSON is 80.64 mV. Thus, for a 0.010-Ω sense resistor, the maximum charging current is 8.064 A.

The CSOP and CSON pins are used to measure the voltage across R_{SR}, which has a default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor results in a larger sense voltage and higher regulation accuracy, but at the expense of higher conduction loss.

To set the charge current, use the SMBus to write a 16-bit ChargeCurrent() command using the data format listed in Table 4. The ChargeCurrent() command uses the Write-Word protocol (see Figure 33). The command code for ChargeCurrent() is 0x14 (0b0001 0100). When using a 10-mΩ sense resistor, the bq24745 provides a charge current range of 128 mA to 8.064 A, with 128-mA resolution. Set ChargeCurrent() to 0 to terminate charging. Setting ChargeCurrent() below 128 mA, or above 8.064 A, clears DAC and terminates charge.

The bq24745 includes a foldback current limit when the battery voltage is low. If the battery voltage is less than 3.6 V but above 2.5 V, any charge current limit above 3 A is clamped at 3 A. If the battery voltage is less than 2.5 V, the charge current is set to 220 mA until that voltage rises above 2.7 V. The ChargeCurrent() register is preserved and becomes active again when the battery voltage is higher than 2.7 V. This function effectively provides a fold-back current limit, which protects the charger during short circuit and overload.

On reset, the ChargeVoltage() and ChargeCurrent() values are cleared (0) and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() commands are sent. During reset, both high-side and low-side FETs remain off until the charger is started.

Table 4. Charge Current Register (0x14), Using 10-mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
0	–	Not used
1	–	Not used
2	–	Not used
3	–	Not used
4	–	Not used
5	–	Not used
6	–	Not used
7	Charge current, DACI 0	0 = Adds 0 mA of charger current 1 = Adds 128 mA of charger current
8	Charge current, DACI 1	0 = Adds 0 mA of charger current 1 = Adds 256 mA of charger current
9	Charge current, DACI 2	0 = Adds 0 mA of charger current 1 = Adds 512 mA of charger current
10	Charge current, DACI 3	0 = Adds 0 mA of charger current 1 = Adds 1,024 mA of charger current
11	Charge current, DACI 4	0 = Adds 0 mA of charger current 1 = Adds 2,048 mA of charger current

Table 4. Charge Current Register (0x14), Using 10-mΩ Sense Resistor (continued)

BIT	BIT NAME	DESCRIPTION
12	Charge current, DACI 5	0 = Adds 0 mA of charger current 1 = Adds 4,096 mA of charger current
13	–	Not used
14	–	Not used
15	–	Not used

INPUT ADAPTER CURRENT REGULATION

The total input current from an ac adapter or other dc source is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the system are powered up or down. Without dynamic power management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the input current regulator reduces the charging current to keep the input current from exceeding the limit set by the Input Current SMBus 6-bit DAC register. With high-accuracy limiting, the current capability of the ac adaptor can be lowered, reducing system cost.

The CSSP and CSSN pins are used to sense R_{AC} with a default value of 10 mΩ. However, resistors of other values can also be used. A larger a sense resistor results in a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

The total input current, from a wall cube or other dc source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the bq24745 decreases the charge current to provide priority to system load current. As the system supply rises, the available charge current drops linearly to zero.

$$I_{INPUT} = I_{SYSTEM} + \left[\frac{I_{LOAD} \times V_{BATTERY}}{V_{IN} \times \eta} \right] + I_{BIAS} \quad (1)$$

where η is the efficiency of the dc-dc converter (typically 85% to 95%).

To set the input current limit, use the SMBus to write a 16-bit InputCurrent() command using the data format listed in Table 5. The InputCurrent() command uses the Write-Word protocol (see Figure 33). The command code for InputCurrent() is 0x3F (0b0011 1111). When using a 10-mΩ sense resistor, the bq24745 provides an input-current limit range of 256 mA to 11.008 A, with 256-mA resolution. InputCurrent() settings from 1 mA to 256 mA clears DAC and terminates charge. On reset the input current limit is 256 mA.

Table 5. Input Current Register (0x3F), Using 10-mΩ Sense Resistor.

BIT	BIT NAME	DESCRIPTION
0	–	Not used
1	–	Not used
2	–	Not used
3	–	Not used
4	–	Not used
5	–	Not used
6	–	Not used
7	Charge current, DACS 0	0 = Adds 0 mA of charger current 1 = Adds 256 mA of charger current
8	Charge current, DACS 1	0 = Adds 0 mA of charger current 1 = Adds 512 mA of charger current
9	Charge current, DACS 2	0 = Adds 0 mA of charger current 1 = Adds 1,024 mA of charger current
10	Charge current, DACS 3	0 = Adds 0 mA of charger current 1 = Adds 2,048 mA of charger current
11	Charge current, DACS 4	0 = Adds 0 mA of charger current 1 = Adds 4,096 mA of charger current

Table 5. Input Current Register (0x3F), Using 10-mΩ Sense Resistor. (continued)

BIT	BIT NAME	DESCRIPTION
12	Charge current, DACS 5	0 = Adds 0 mA of charger current 1 = Adds 8,192 mA of charger current; 11,008 mA max
13	–	Not used
14	–	Not used
15	–	Not used

ADAPTER DETECT AND POWER UP

An external resistor voltage divider attenuates the adapter voltage before it goes to ACIN. The adapter-detect threshold should typically be programmed to a value greater than the maximum battery voltage and lower than the minimum allowed adapter voltage. The ACIN divider should be placed before the input power path selector in order to sense the true adapter input voltage.

If DCIN is below 4 V, the charger is disabled.

If ACIN is below 0.6 V but DCIN is above 4.5 V, AC and VICM are disabled and pulled down to GND. The total quiescent current is less than 10 µA.

Once ACIN rises above 0.6 V and DCIN is above 4.5 V, VREF goes to 3.3 V and all the bias circuits are enabled. ACOK low indicates ACIN still below 2.4 V, and the valid adaptor is not available. VICM becomes valid to reflect the adapter current.

When ACIN keeps rising and passes 2.4 V, a valid ac adapter is present. 100 µs later, the following occurs:

- ACOK becomes high through an external pullup resistor to the host digital voltage rail.
- The charger turns on if all the conditions are satisfied. (see *Enable and Disable Charging*)

ENABLE AND DISABLE CHARGING

The following conditions must be valid before charging is enabled:

- Not in UVLO (DCIN > 4.5 V, and VDDSMB >2.5 V)
- Adapter is detected (ACIN > 2.4 V).
- Adapter – Battery voltage is higher than the $V_{DCIN-VFB}$ comparator threshold.
- 200-µs delay is complete after adapter detection.
- SMBus ChargeVoltage(),ChargeCurrent() and InputCurrent() DAC registers are inside the valid range.
- CE is HIGH.
- 2-ms delay is complete after adapter is detected and CE goes HIGH.
- VDDP and VREF are valid.
- Not in thermal shutdown (TSHUT)

Any of the following conditions stops ongoing charging:

- SMBus ChargeVoltage(), ChargeCurrent(), or InputCurrent() DAC register is outside the valid range.
- CE is LOW.
- Adapter is removed (DCIN <4 V).
- VDDSMB supply is removed. (VDDSMB <2.35 V)
- Adapter – Battery voltage is less than $V_{DCIN-VFB}$ comparator threshold.
- Battery is over voltage.
- In thermal shutdown: TSHUT IC temperature threshold is above 155°C.

AUTOMATIC INTERNAL SOFT-START CHARGER CURRENT

The charger automatically soft-starts the output regulation current every time the charger is enabled to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping up the charge regulation current in eight evenly divided steps up to the programmed charge current. Each step lasts around 1.6 ms, for a typical rise time of 12.8 ms. No external components are needed for this function. The regulation limits can be changed in the middle of charging without soft start.

CONVERTER OPERATION

The synchronous buck PWM converter uses a fixe- frequency (300 kHz) voltage mode with feed-forward control scheme. A type-III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter selected gives a characteristic resonant frequency that is used to determine the compensation to ensure there is sufficient phase margin for the target bandwidth.

The resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}}$$

An internal sawtooth ramp is compared to the internal EAO error control signal to vary the duty cycle of the converter. The ramp height is one-fifteenth of the input adapter voltage, making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 200 mV in order to allow zero-percent duty cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the sawtooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate-drive logic allows achieving 99.98% duty cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BOOT pin to PHASE pin voltage falls below 4 V for more than three cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PHASE node down and recharge the BOOT capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BOOT-PHASE) voltage is detected to fall low again due to leakage current discharging the BOOT capacitor below 4 V, and the recharge pulse is reissued.

The fixed-frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping the frequency out of the audible noise region. The type-III compensation provides phase boost near the cross-over frequency, giving sufficient phase margin.

CONTINUOUS AND DISCONTINUOUS CONDUCTION MODES

In continuous-conduction mode (CCM), the inductor current always flows to charge the battery, and the charger always operates in synchronized mode. At the beginning of each clock cycle, the high-side n-channel power MOSFET turns on, and the turnon time is set by the voltage on EAO pin. After the high-side power MOSFET turns off, the low-side n-channel power MOSFET turns on. During CCM, the low-side n-channel power MOSFET stays on until the end of the clock cycle. The internal gate-drive logic ensures there is break-before-make switching to prevent shoot-through currents. During the 25-ns dead time where both FETs are off, the back diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn on keeps the power dissipation low, and allows safely charging at high currents. With type-III compensation, the loop has a fixed 2-pole system.

Before the ripple valley current gets close to zero, the low-side FET must turn off before current goes negative, or flows from the battery to the PHASE node, to avoid battery boosting the system. After the high-side n-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side n-channel power MOSFET turns on for a blank-out time. After the blank-out time is over, if the $V_{CSOP-CSON}$ voltage falls below the UCP threshold (typical 10 mV), the low-side power MOSFET turns off and stays off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. After the low-side MOSFET turns off, the inductor current flows through back-gate diode until it reaches zero. The negative inductor current is blocked by the diode, and the inductor current becomes discontinuous. This mode is called discontinuous-conduction mode (DCM).

During the DCM mode, the loop response automatically changes and has a single-pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage. At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 40-ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance.

Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (no 40-ns recharge pulse) either, and there is no discharge from the battery unless the BOOT to PHASE voltage discharges below 4 V. In that case, it pulses once to recharge the bootstrap capacitor.

REFRESH BTST CAPACITOR

If the BOOT pin to PHASE pin voltage falls below 4 V for more than three cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on for 40 ns to pull the PHASE node down and recharge the BOOT capacitor. The 40-ns low-side MOSFET on-time is required protect from ringing noise, and to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle.

UCP (CHARGE UNDERCURRENT), USING SENSE RESISTOR

In the bq24745, the cycle-by-cycle UCP allows using very small inductors seamlessly, even if they have large ripple current. Every cycle when the low-side MOSFET turns-on, if the CSOP-CSON voltage falls below 10 mV (inductor current falls below 1 A if using a 10-mΩ sense resistor), the low-side MOSFET is latched off until the next cycle begins and resets the latch.

The converter automatically detects when to turn off the low-side MOSFET every cycle. The converter goes into discontinuous conduction mode (DCM) when the current falls below 1/2 the inductor peak-to-peak current ripple. The inductor current ripple is given by

$$I_{DCM} < \frac{I_{RIPPLE}}{2}$$

$$\text{and} \quad I_{RIPPLE} = \frac{(V_{IN}-V_{BAT}) \times \left(\frac{V_{BAT}}{V_{IN}}\right) \times \left(\frac{1}{f_S}\right)}{L_{out}} \tag{2}$$

where

V_{IN}: adapter voltage = DCIN voltage
V_{VFB}: output voltage = VFB voltage
f_S: switching frequency = 300 kHz
L_{OUT}: output inductor

For proper cycle-by-cycle UCP sensing, the output filter capacitor should sit on CSON. Only a 0.1-µF capacitor is on CSOP, close to the device input.

AVERAGE CHARGE OVERCURRENT, USING SENSE AMPLIFIER

The charger has average overcurrent protection using the $V_{CSON-CSOP}$ voltage across the charge-current sense resistor. It monitors the charge current, and prevents the current from exceeding 145% of the programmed regulated charge current. If the charge current limit falls below 3.3 A (on 10 mΩ), the overcurrent limit is fixed at 5 A. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold. There is an internal 160-kHz filter pole, to filter the switching frequency and prevent false tripping. This adds a small delay, depending on the amount of overdrive over the threshold.

BATTERY OVERVOLTAGE PROTECTION, USING REMOTE SENSING VFB

The converter does not allow switching when the battery voltage at VFB exceeds 104% of the regulation voltage set-point. Once the VFB voltage returns below 102% of the regulation voltage, switching resumes. This allows quick response to an overvoltage condition, such as occurs when the load is removed or the battery is disconnected. A current sink from CSOP and CSON to GND is on only during charging and allows discharging the stored output inductor energy that is transferred to the output capacitors.

BATTERY TRICKLE CHARGING

The bq24745 automatically reduces the charge current limit to a fixed 220 mA to trickle-charge the battery when the voltage on the VFB pin falls below 2.5 V. The charge current returns to the value programmed on the ChargeCurrent(0x14) register when the VFB pin voltage rises above 2.7 V.

This function provides a safe trickle charge to close deeply discharged open packs.

HIGH-ACCURACY VICM USING CURRENT-SENSE AMPLIFIER (CSA)

An industry standard, high-accuracy current-sense amplifier (CSA) is used to monitor the input current by the host or some discrete logic through the analog voltage output of the VICM pin. The CSA amplifies the input sensed voltage of CSSP-CSSN by 20× through the VICM pin. The VICM output is a voltage source 20 times the input differential voltage. Once DCIN is above 4.5 V and ACIN is above 0.6 V, VICM no longer stays at ground, but becomes active. A user wanting to lower the voltage could use a resistor divider from VICM to GND and still achieve accuracy over temperature.

A 100-pF capacitor connected on the output is recommended for decoupling high-frequency noise.

VDDSMB INPUT SUPPLY

The VDDSMB input provides bias power to the SMBus interface logic. Connect VDDSMB to an external 3.3-V or 5-V supply rail. SMBus communication can start between host and charger when the VDDSMB voltage is above 2.5 V and the VREF voltage is at 3.3 V. Bypass VDDSMB to GND with a 0.1-µF or greater ceramic capacitor.

INPUT UNDERVOLTAGE LOCKOUT (UVLO)

The system must have a minimum 4.5-V DCIN voltage to allow proper operation. When the DCIN voltage is below 4 V, VREF LDO stays inactive, even with ACIN above 0.6 V. VREF turns on when DCIN > 4.5 V and ACIN > 0.6 V. To enable VDDP requires DCIN > 4.5 V, ACIN > 2.4 V, and CE = HIGH.

VDDP GATE DRIVE REGULATOR

An integrated low-dropout (LDO) linear regulator provides a 6-V supply derived from DCIN for high efficiency, and delivers over 90 mA of load current. The LDO powers the gate drivers of the n-channel switching MOSFETs. Bypass VDDP to PGND with a 1-µF or greater ceramic capacitor. During thermal shutdown, the VDDP LDO is disabled.

INPUT CURRENT COMPARATOR TRIP DETECTION

In order to optimize the system performance, the host monitors the adapter current. Once the adapter current is above a threshold set via ICREF, the ICOUT pin sends a signal to the HOST. The signal alarms the host that input power has exceeded the programmed limit, allowing the host to throttle back system power by reducing clock frequency, lowering rail voltages, or disabling certain parts of the system. The ICOUT pin is an open-drain output. Connect a pullup resistor to ICOUT. The output is logic HI when the VICM output voltage (VICM = 20 × $V_{CSSP-CSSN}$) is lower than the ICREF input voltage. The ICREF threshold is set by an external resistor divider using VREF. The hysteresis can be programmed by a positive feedback resistor from the ICOUT pin to the ICREF pin.

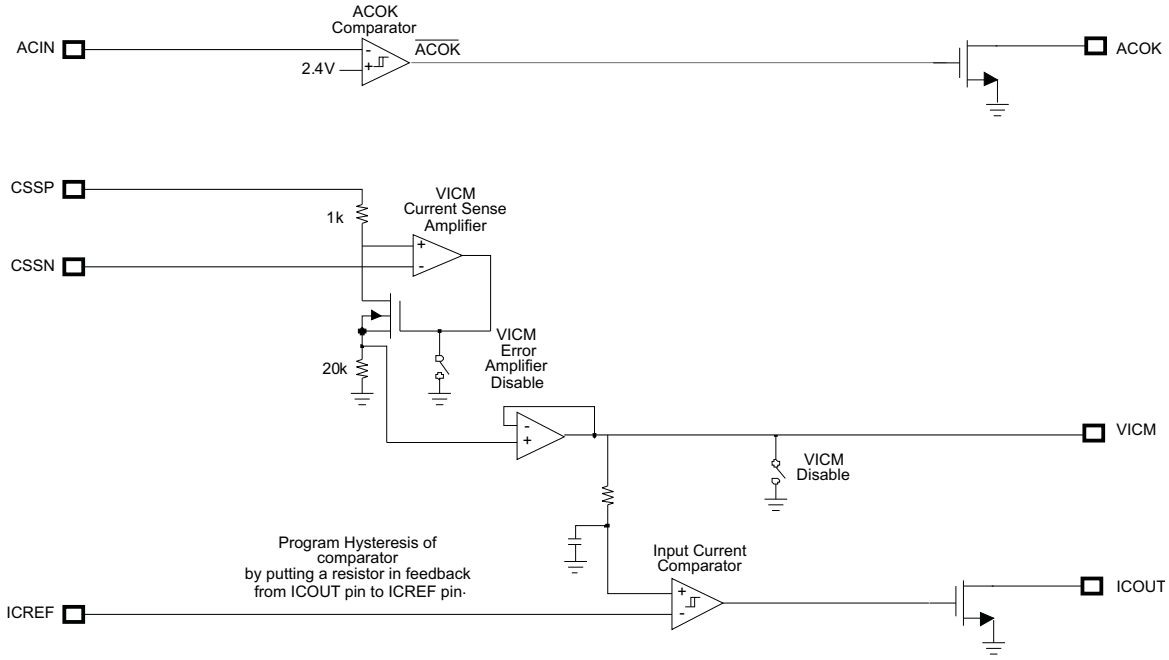


Figure 36. ACOK, ICREF, and ICOUT Logic

OPEN-DRAIN STATUS OUTPUTS (ACOK, ICOUT PINS)

Two status outputs are available; both require external pullup resistors to pull the pins to the system digital rail for a high level.

The ACOK open-drain output goes high when ACIN is above 2.4 V. It indicates that a functional adapter is providing a valid input voltage.

The ICOUT open-drain output goes low when the input current is higher than the threshold programmed via the ICREF pin. Hysteresis can be programmed by adding a resistor from the ICREF pin to the ICOUT pin.

THERMAL SHUTDOWN PROTECTION

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep the junction temperature low. As an added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 155°C. VDDP LDO is disabled as well during thermal shutdown. The charger stays off until the junction temperature falls below 135°C. Once the temperature drops below 135°C, the VDDP LDO is enabled. If all the conditions described in the *Enable and Disable Charging* section are valid, charge soft-starts again.

CHARGER TIME-OUT

The bq24745 includes a timer to terminate charging if the charger does not receive a ChargeVoltage() or ChargeCurrent() command within 170 s. If a time-out occurs, both ChargeVoltage() and ChargeCurrent() commands must be resent to re-enable charging.

CHARGE TERMINATION FOR Li-Ion OR Li-Polymer

The primary termination method for Li-Ion and Li-Polymer is minimum current. Secondary temperature termination (see the *Charge Current Regulation* section) also provides additional safety. The host controls the charge initiation and the termination. A battery pack gas gauge assists the hosts on setting the voltages and determining when to terminate based on the battery-pack state of charge.

REMOTE SENSE

The bq24745 has a dedicated remote sense pin, VFB, which allows the rejection of board resistance and selector resistance. To use remote sensing fully, connect VFB directly to the battery interface through an unshared battery-sense Kelvin trace, and place a 0.1-µF ceramic capacitor near the VFB pin to GND (see Figure 1).

Remote Kelvin sensing provides higher regulation accuracy by eliminating parasitic voltage drops. Remote sensing cancels the effect of impedance in series with the battery. This impedance normally causes the battery charger to enter constant-voltage mode prematurely.

Component List for Typical System Circuit of Figure 2

Part Designator	Qty	Description
Q1, Q2,	3	P-channel MOSFET, –30-V, –7.5-A, SO-8, Vishay-Siliconix, Si4435
Q3, Q4	2	N-channel MOSFET, 30-V, 12.5-A, SO-8, Fairchild, FDS6680A
RAC, RSR	2	Sense resistor, 10-mW, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 5.6-uH, 7-A, 31-mΩ Vishay, IHLP2525CZ01-2R
D1	1	Diode, dual Schottky, 30-V, 200-mA, SOT23, Fairchild, BAT54C
C1	1	Capacitor, ceramic, 2.2-µF, 35-V, 10%, X7R
C6	1	Capacitor, ceramic, 1-µF, 35-V, 10%, X7R
2xC13, C14, C15	4	Capacitor, ceramic, 10-µF, 35-V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C6, C16, C4, C8	4	Capacitor, ceramic, 1-µF, 25-V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C2, C3, C7, C9, C10, C17	6	Capacitor, ceramic, 0.1-µF, 50-V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C5	1	Capacitor, ceramic, 100- pF, 25-V, 10%, X7R, 0805, Kemet
C23	1	Capacitor, ceramic, 51-pF, 25-V, 10%, X7R, 0805, Kemet
C21	1	Capacitor, ceramic, 2000-pF, 25-V, 10%, X7R, 0805, Kemet
C22	1	Capacitor, ceramic, 130-pF, 25-V, 10%, X7R, 0805, Kemet
R3, R4, R10, R11, R12	5	Resistor, chip, 10-kΩ, 1/16-W, 5%, 0402
R1	1	Resistor, chip, 309-kΩ, 1/16-W, 1%, 0402
R2	1	Resistor, chip, 49.9-kΩ, 1/16-W, 1%, 0402
RC1	1	Resistor, thick film chip paralleling, 2× 3.9-Ω, 25-V, 1210
RC6	1	Resistor, thick film chip , 10-Ω, 1206
R19	1	Resistor, chip, 7.5-kΩ, 1/16-W, 5%, 0402
R20	1	Resistor, chip, 20-kΩ, 1/16-W, 1%, 0402
R21	1	Resistor, chip, 200-kΩ, 1/16-W, 5%, 0402
R22	1	Resistor, chip, 100-Ω, 1/16-W, 1%, 0402
R7, R8	2	Resistor, chip, 200-kΩ, 1/16-W, 1%, 0402
R18	1	Resistor, chip, 1.4-MΩ, 1/16-W, 1%, 0402

GLOSSARY

VICM Output Voltage of Input Current Monitor

ICREF Input Current Reference - sets the threshold for the input current limit

DPM Dynamic Power Management

CSOP, CSON Current Sense Output of battery positive and negative

These pins are used with an external low-value series resistor to monitor the current to and from the battery pack.

CSSP, CSSN Current Sense Supply positive and negative

These pins are used with an external low-value series resistor to monitor the current from the adapter supply.

POR Power-on reset

REVISION HISTORY

NOTE: Page numbers of previous versions may differ from the current version.

Changes from Original (December 2007) to Revision A — **Page**

- Changed The data sheet title From: SMBus-Controlled Multi-Chemistry Battery Charger With Input Current Detect Comparator To: SMBus-Controlled Multi-Chemistry Battery Charger With Input Current Detect Comparator and Charge Enable Pin 1
- Deleted Features Bullet: Cells Pin Supports Two to Four Li-Ion Cells 1
- Deleted Condition above Figure 1: $VICM_{er\_limit}$ = 6 A 2
- Added text to the condition above Figure 2: "for ICOUT Input Current comparator" 3
- Changed ICREF text in the PIN FUNCTIONS table From: Input current comparator voltage reference input. Connect a resistor-divider from VREF to ICREF, and GND to program the reference for the LOPWR comparator To: Input current comparator voltage reference input. Connect a resistor-divider from VREF to ICREF, and GND to program the reference for the ICOUT comparator 4

Changes from Revision A (October 2008) to Revision B — **Page**

- Deleted "Level 2" from title 1
- Deleted "Input Overvoltage Protection (OVP)" Features bullet 1
- Changed Feature bullet from "6 V-24 V" to "7 V-24 V" 1
- Changed "10-µ" to "10-µA" Battery Current 1
- Changed last sentence of first paragraph of DESCRIPTION by deleting "one," from the text string. 1
- Changed Figure 1 graphic entity 2
- Changed Figure 2 graphic entity 3
- Changed T_A from "70°C" to "40°C" in the Package Thermal Data table. 3
- Changed θ_{JA} from "39°C/W" to "36°C/W" in the Package Thermal Data table. 3
- Changed "ACOUT" to "ICOUT" and deleted "ICREF input" from Pin 2 functional description. 4
- Deleted "optional" from Pins 17, 18, 27, and 28 functional description in the Pin Functions table. 4
- Added text to Pin 22 functional description. 4
- Changed Pin 22 functional description from "100-Ω" resistor to "10-Ω" resistor in the Pin Functions table. 4
- Added "ACOK" specification to first row of Absolute Maximum Ratings table. 5
- Added "SDA" and "SCL" specification to fourth row of Absolute Maximum Ratings table, and changed maximum voltage from "7 V" to "6 V" 5
- Deleted "GND" and "PGND" specification from Absolute Maximum Ratings table 5
- Added "ACOK" specification to Recommended Operating Conditions table 5
- Added "VDDSMB", "SDA", and "SCL" specifications to Recommended Operating Conditions table 5
- Changed VFB SHORT (....) COMPARATOR specification parameter text from ""VFB short rising hysteresis" to "VFB short falling hysteresis" 7
- Changed Functional Block Diagram graphic entity 17
- Changed Detailed Description -- re-write for clarification 18
- Changed Figure 33 graphic entity 19
- Changed Figure 34 graphic entity legend 19
- Changed Figure 35 graphic entity legend 20
- Changed Figure 36 graphic entity 27
- Deleted "Q5" from Component List table. 28
- Added description for C1 and C6 in the Component List table. 28
- Changed "R9" to "R19" in Component List 28
- Added R20 to Component List 28

- Changed "R11" to "R21" in Component List 28
- Added R22 to Component List 28

Changes from Revision B (April 2010) to Revision C **Page**

- Changed Table 5 , Bit 7 description from "128mA" to "256mA"; Bit 8 description from "256mA" to "512mA"; Bit 9 description from "512mA" to "1024mA"; Bit 10 description from "1024mA" to "2048mA"; Bit 11 description from "2048mA" to "4096mA"; and Bit 12 description from "4096mA" to "8192 mA". 22

Changes from Revision C (April 2011) to Revision D **Page**

- Corrected pin numbers on pins CSSN, CSSP, CSON, and CSOP in Figure 1 2
- Corrected pin numbers on pins CSSN, CSSP, CSON, and CSOP in Figure 2 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24745RHDR	NRND	VQFN	RHD	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 0	BQ 24745	
BQ24745RHDT	NRND	VQFN	RHD	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 0	BQ 24745	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

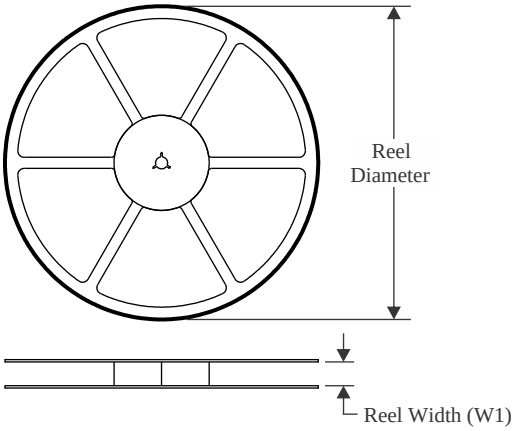
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

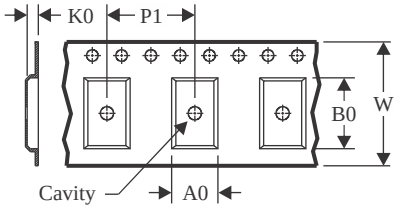
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

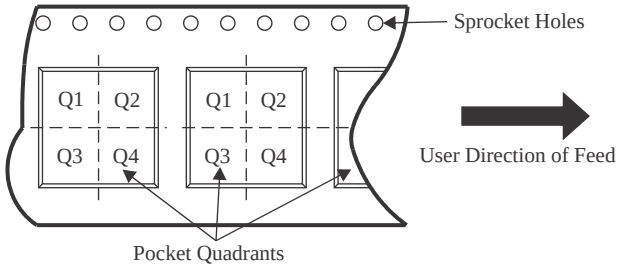


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

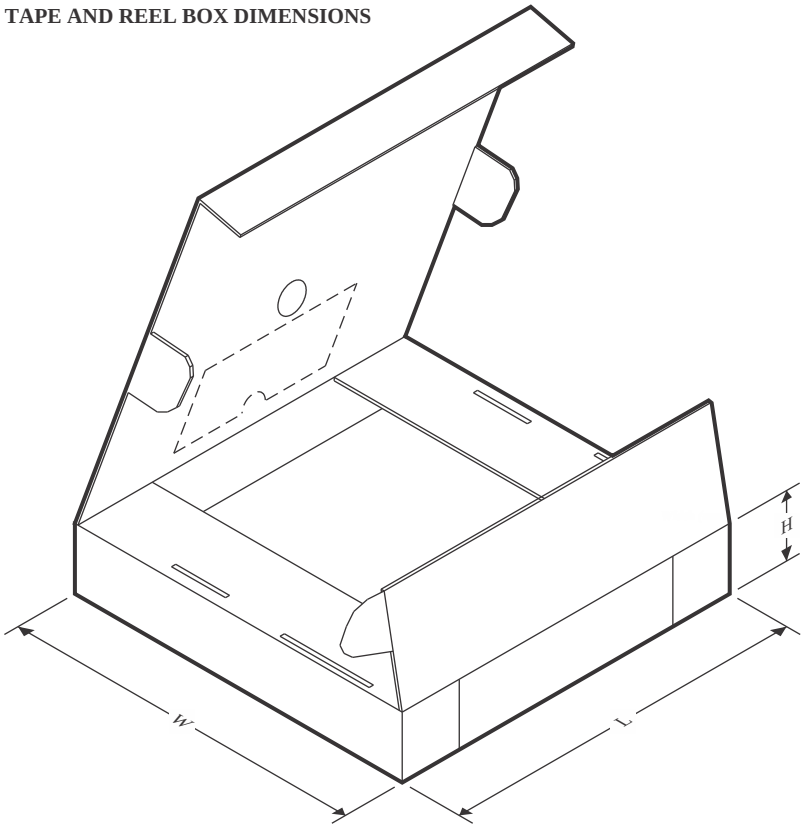
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24745RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
BQ24745RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24745RHDR	VQFN	RHD	28	3000	346.0	346.0	33.0
BQ24745RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

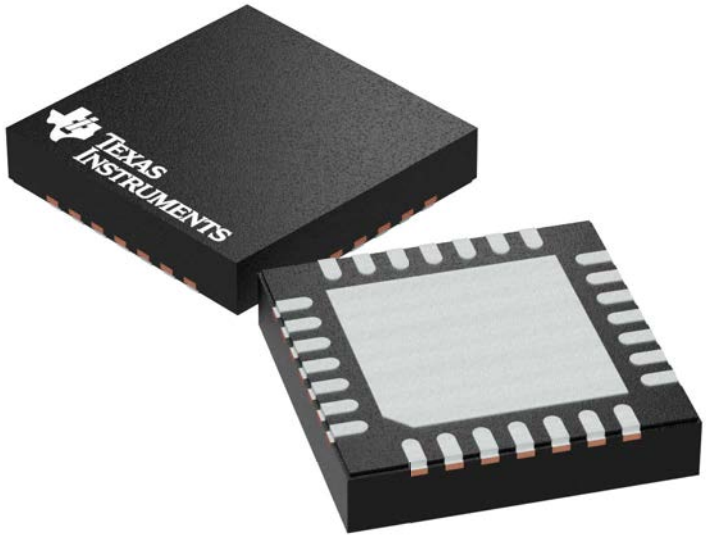
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

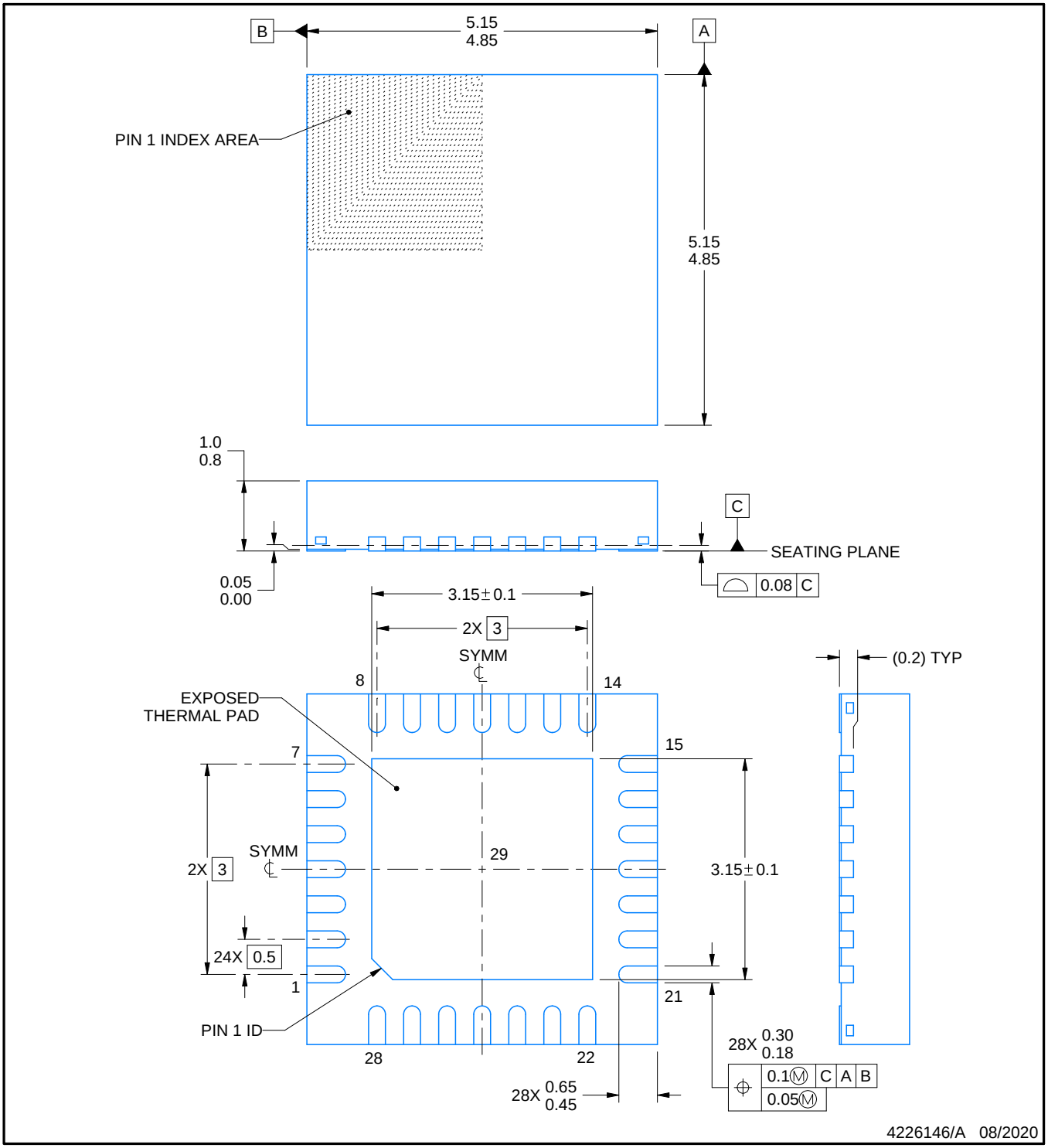
4204400/G

RHD0028B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

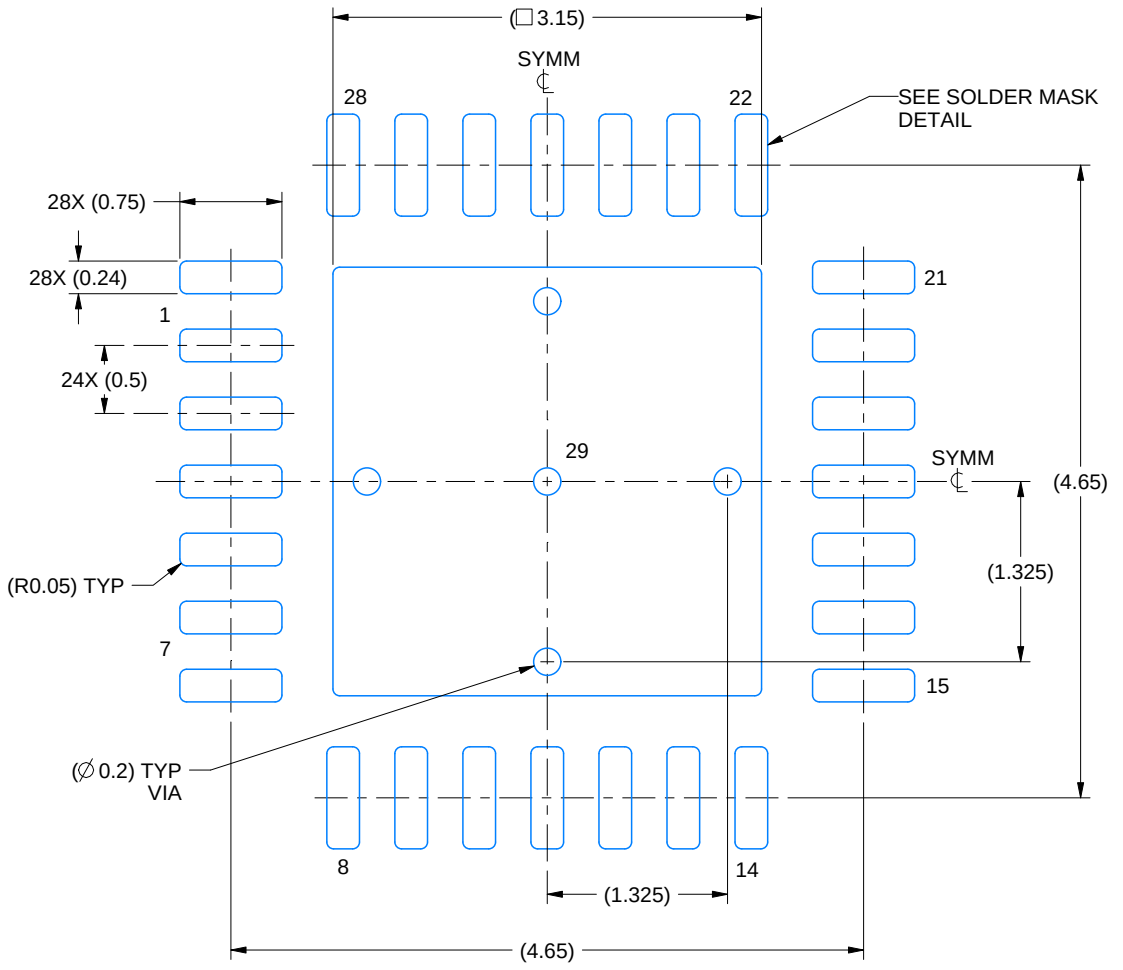
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

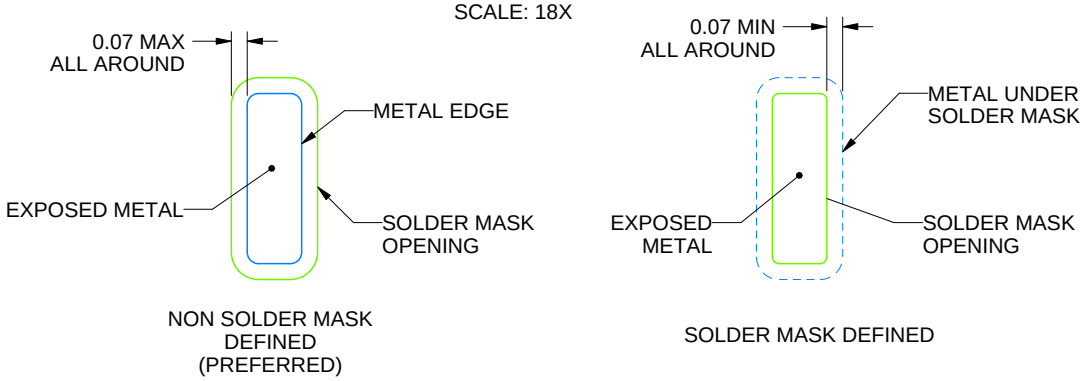
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

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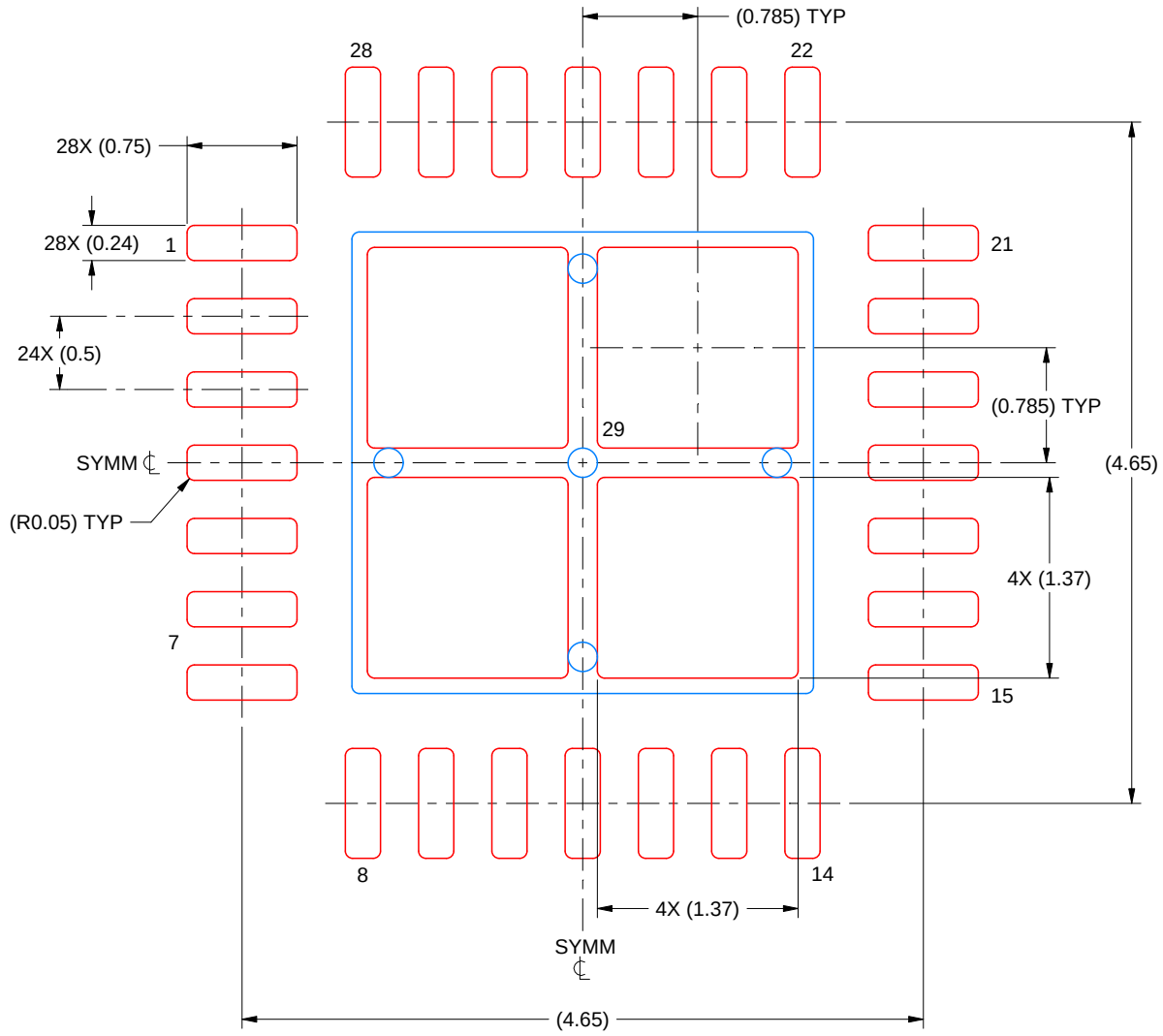
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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