

# CC274xR-Q1, CC274xP-Q1 AutomotiveSimpleLink™ Bluetooth® Low Energy Wireless MCU

## 1 Features

### Wireless MCU processing elements

- Arm® Cortex®-M33 processor (96MHz) with FPU (floating point unit), TrustZone®-M support, and CDE (custom datapath extension) for machine learning acceleration
- Algorithm Processing Unit (APU) (96MHz)
  - Mathematical accelerator for efficient vector and matrix operations
  - Bluetooth® Channel Sounding post-processing support for IFFT and advanced super-resolution algorithms such as Multiple Signal Classification (MUSIC)

### Wireless MCU memory

- Up to 1MB of in-system programmable flash
- Up to 162KB of SRAM
- 32KB of System ROM with secure boot root of trust (RoT) and a serial (SPI/UART) bootloader
- Serial wire debug (SWD)

### Qualified for automotive application

- AEC-Q100 Grade 2 qualified:
  - $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  junction temperature
- HBM ESD Classification Level 2 (ESD HBM level 1C on RF pin, per AEC-Q100 Rev. J)
- CDM ESD Classification Level C2A (ESD CDM level C1 on RF pin, per AEC-Q100 Rev. J)

### MCU peripherals

- 23 GPIOs, digital peripherals can be routed to multiple GPIOs:
  - Two SWD IO pads, multiplexed with GPIOs
  - Two LFXT IO pads, multiplexed with GPIOs
  - 19 DIOs (analog or digital IOs)
- All GPIOs with wakeup and interrupt capabilities
- 3 × 16-bit and 1 × 32-bit general-purpose timers, quadrature decode mode support
- Real-time clock (RTC)
- Watchdog timer
- System timer for radio, RTOS, and application operations for Bluetooth® channel sounding postprocessing
- 12-bit ADC, up to 1.2MSPS, eight external inputs
- Temperature sensor and battery monitor
- 1× low-power comparator
- 2× UART with LIN capability
- 2× SPI
- 1× I<sup>2</sup>C
- 1× I<sup>2</sup>S

- 1× CAN-FD controller with CAN/CAN-FD ISO 16845-1:2016 certification compliance

### Security enablers

- ISO21434 Automotive Cybersecurity Compliant
- Hardware Security Module (HSM) with proprietary controller and dedicated memories supporting accelerated cryptographic operations and secure key storage:
  - AES (up to 256 bits) crypto accelerator
  - ECC (up to 521 bits), RSA (up to 3072 bits) public key accelerator
  - SHA-2 (up to 512 bits) accelerator
  - True random number generator
  - HSM firmware update support
  - Differential power analysis (DPA) countermeasures for AES and ECC
- Separate AES 128-bit cryptographic accelerator (LAES) for latency-critical link-layer operations
- Secure boot and secure firmware updates
- Cortex®-M33 TrustZone-M, MPU, memory firewalls for software isolation
- Voltage glitch monitor (VGM)

### Low-power consumption (VDD<sub>S</sub> at 3.3V)

- On-chip buck DC/DC converter
- RX current: 6.1mA
- TX current at 0dBm: 7.7mA
- TX current at +10dBm: 24.5mA (R variant)
- TX current at +20dBm: 143mA (P variant)
- Active mode MCU 96MHz (CoreMark®): 6.8mA
- Standby: 0.9µA (low power mode, RTC on, full SRAM retention)
- Shutdown: 160nA

### Wireless protocol support

- Bluetooth® Core 6.0 Qualified
  - Support for Bluetooth® Channel Sounding (High Accuracy Distance Measurement)

### High-performance radio

- 2.4GHz RF transceiver compatible with Bluetooth® Low Energy specification
- Output power up to +10dBm (R variant)
- Output power up to +20dBm (P variant)
- Integrated BALUN
- Integrated RF switch
- Receiver sensitivity:
  - Bluetooth® LE 125kbps:  $-103.5\text{dBm}$
  - Bluetooth® LE 1Mbps:  $-97\text{dBm}$



## Regulatory compliance

- Designed for systems targeting compliance with worldwide radio frequency regulations
  - EN 300 328 (Europe)
  - FCC CFR47 Part 15 (US)
  - ARIB STD-T66 (Japan)

## Development tools and software

- LP-EM-CC2745R10-Q1, LP-EM-CC2755P10 LaunchPad™ Development Kit
- BP-EM-CS Multiple antenna board for Bluetooth® Channel Sounding
- SimpleLink™ Low Power F3 Software Development Kit (SDK)
  - Fully qualified Bluetooth® software protocol stack in the SDK
    - Up to 32 concurrent multirole connections
    - Bluetooth® Low Energy 6.0 Support
    - CCC Digital Key 3 / ICCE Bluetooth® APIs support for secure car access systems

- Automotive SPICE (ASPICE) compliance for SDK components, including the Bluetooth® LE stack
- SysConfig system configuration tool
- SmartRF™ Studio for simple radio configuration

## Operating ranges

- Junction temperature T<sub>j</sub>: –40°C to 125°C
- Wide supply voltage range 1.71V to 3.8V

## Package

- 6mm × 6mm QFN40 with wettable flanks
- RoHS-compliant package

## 2 Applications

- Automotive
  - [Car access and security systems](#)
    - Digital key
    - [Phone as a key \(PaaK\)](#)
    - [Passive entry passive start \(PEPS\)](#)
    - [Remote keyless entry \(RKE\)](#)

## 3 Description

The SimpleLink™ CC274xR-Q1 and CC274xP-Q1 devices are AEC-Q100 complaint wireless microcontrollers (MCUs) supporting Bluetooth® Low Energy 6.0 for automotive applications. These devices are optimized for low-power wireless communication in applications such as car access, including passive entry passive start (PEPS), phone as a key (PaaK), and remote keyless entry (RKE). The key features of this device include:

- Support for features in Bluetooth® 6.0 and earlier versions:
  - LE Coded PHYs (Long Range), LE 2Mbit PHY (high speed), advertising extensions, multiple advertisement sets, CSA#2, as well as backward compatibility with earlier Bluetooth® Low Energy specifications
- Bluetooth® Channel Sounding technology support and an Algorithm Processing Unit (APU) to enable high accuracy, low cost, and a secure phase-based ranging mechanism for distance estimation
  - APU enables latency and power-efficient execution of distance-ranging signal processing algorithms, including FFT, super-resolution complex algorithms like Multiple Signal Classification (MUSIC), and neural network algorithms.
- Arm® Custom Data Extension (CDE) instruction support for machine learning acceleration
- Fully qualified Bluetooth® software protocol stack included with the SimpleLink™ Low Power F3 Software Development Kit (SDK)
- Advanced security features for connected wireless MCUs:
  - An isolated HSM environment with a dedicated controller handling accelerated cryptographic and random number generation operations
  - Secure boot and firmware updates with the root of trust enabled by an immutable system ROM
  - Arm® Cortex M33 TrustZone-M based trusted execution environment support
  - Secure key storage support with HSM and TrustZone-M
  - Hardware fault sensors to mitigate low-cost, low-effort, non-invasive physical attack threats like voltage glitch injection
  - Dedicated AES-128 HW accelerator for handling timing-critical link-layer encryption/decryption operations
- Ultra-low standby current with full 162KB SRAM retention and RTC operation that enables significant battery life extension, especially for applications with longer sleep intervals
- Extended temperature support with the lowest standby current
- Integrated BALUN and integrated RF switch to support both transmit and receive operations on the same RF pin, even in the P version; thereby, enabling a reduced bill-of-material (BOM) board layout
- Excellent radio sensitivity and robustness (selectivity and blocking) performance for Bluetooth® Low Energy

The CC274xR/P-Q1 devices are part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, Bluetooth® Low Energy, Thread, Zigbee, Sub1GHz MCUs, and host MCUs that all share a common, easy-to-use development environment with a single core software development kit (SDK) and a rich toolset. A one-time integration of the SimpleLink™ platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit [SimpleLink™ MCU platform](#).

**Table 3-1. Device Information**

| PART NUMBER        | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|--------------------|------------------------|-----------------------------|
| CC2745R10E0WRHARQ1 | QFN40                  | 6.0mm × 6.0mm               |
| CC2745R10E1WRHARQ1 | QFN40                  | 6.0mm × 6.0mm               |
| CC2745P10E0WRHARQ1 | QFN40                  | 6.0mm × 6.0mm               |
| CC2745R74E0WRHARQ1 | QFN40                  | 6.0mm × 6.0mm               |
| CC2744R74E0WRHARQ1 | QFN40                  | 6.0mm × 6.0mm               |

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

## 4 Functional Block Diagram

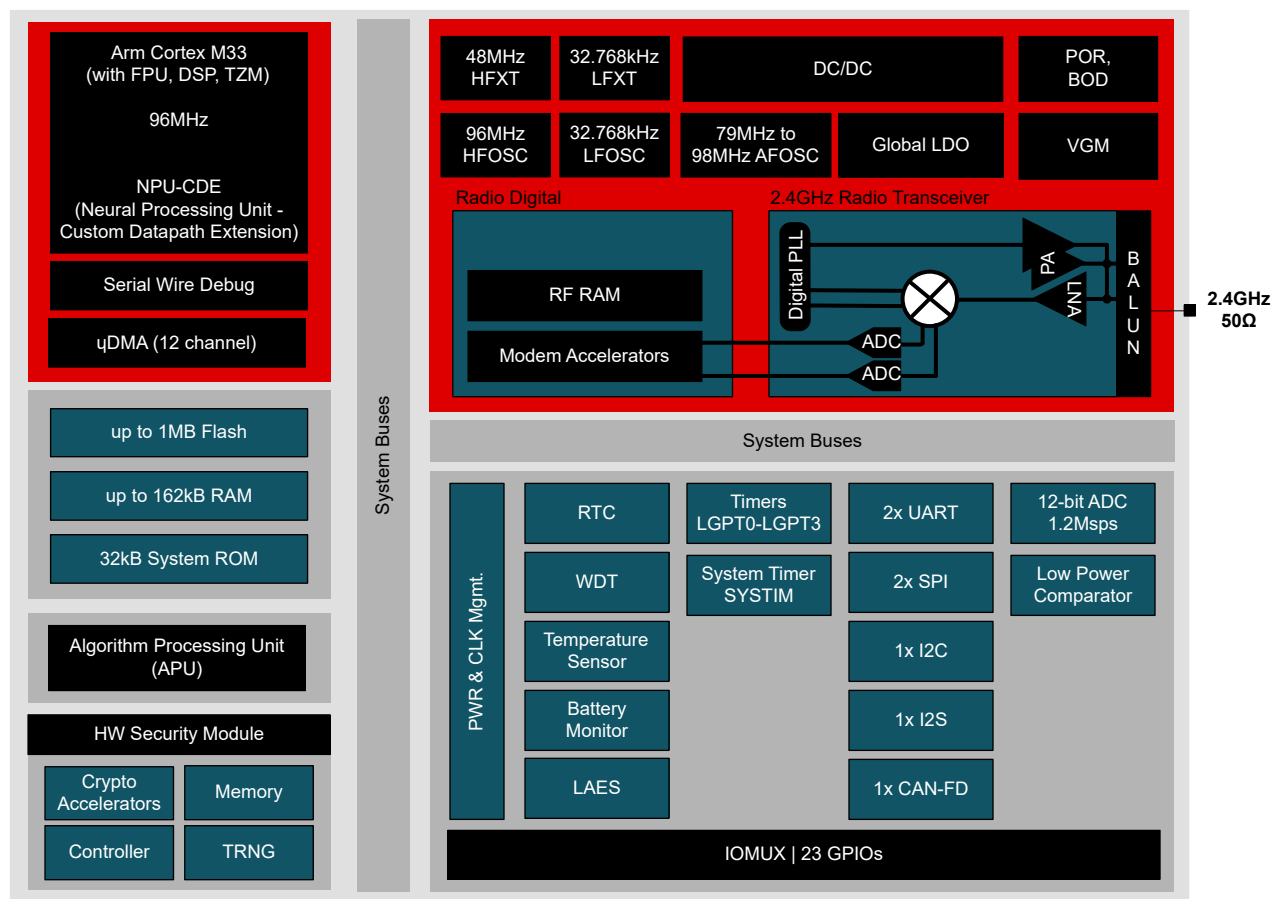


Figure 4-1. Functional Block Diagram

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## 5 Device Comparison

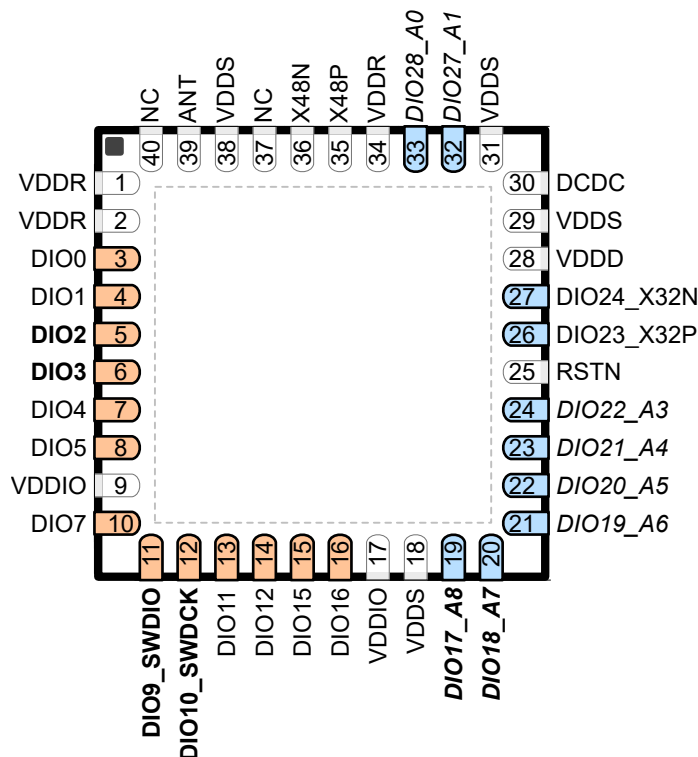
| IP                                                                              | CC2745P10-Q1        | CC2745R10-Q1        | CC2745R7-Q1        | CC2744R7-Q1        |
|---------------------------------------------------------------------------------|---------------------|---------------------|--------------------|--------------------|
| CM33 (MCU)                                                                      | ✓                   | ✓                   | ✓                  | ✓                  |
| APU (Algorithm Processing Unit)<br>(Bluetooth Channel Sounding Post-processing) | ✓                   | ✓                   | ✓                  | ✓                  |
| CAN-FD Controller                                                               | ✓                   | ✓                   | ✓                  |                    |
| HSM                                                                             | ✓                   | ✓                   | ✓                  | ✓                  |
| VGM                                                                             | ✓                   | ✓                   | ✓                  | ✓                  |
| 2x UART, 2x SPI, 1x I <sup>2</sup> C,<br>1x I <sup>2</sup> S                    | ✓                   | ✓                   | ✓                  | ✓                  |
| +10dBm PA                                                                       | ✓                   | ✓                   | ✓                  | ✓                  |
| +20dBm PA                                                                       | ✓                   |                     |                    |                    |
| ADC12                                                                           | ✓                   | ✓                   | ✓                  | ✓                  |
| Flash (KB)                                                                      | 1024 <sup>(1)</sup> | 1024 <sup>(1)</sup> | 864 <sup>(1)</sup> | 864 <sup>(1)</sup> |
| SRAM (KB) (parity disabled)                                                     | 162                 | 162                 | 128                | 128                |
| SRAM (KB) (parity enabled)                                                      | 144                 | 144                 | 128                | 128                |
| GPIO                                                                            | 23                  | 23                  | 23                 | 23                 |
| QFN PKG Size (mm x mm)                                                          | 6 x 6               | 6 x 6               | 6 x 6              | 6 x 6              |

(1) 96KB of the device flash memory is reserved for HSM firmware.

## 6 Pin Configuration and Functions

### 6.1 Pin Diagrams

#### 6.1.1 Pin Diagram—RHA package



**Figure 6-1. RHA (6mm × 6mm) Pinout, 0.5mm Pitch (Top View)**

The following I/O pins marked in [Figure 6-1](#) in **bold** have high-drive capabilities:

- Pin 5, **DIO2**
- Pin 6, **DIO3**
- Pin 11, **DIO9\_SWDIO**
- Pin 12, **DIO10\_SWDCCK**
- Pin 19, **DIO17\_A8**
- Pin 20, **DIO18\_A7**

The following I/O pins marked in [Figure 6-1](#) in *italics* have analog capabilities:

- Pin 19, *DIO17\_A8*
- Pin 20, *DIO18\_A7*
- Pin 21, *DIO19\_A6*
- Pin 22, *DIO20\_A5*
- Pin 23, *DIO21\_A4*
- Pin 24, *DIO22\_A3*
- Pin 32, *DIO27\_A1*
- Pin 33, *DIO28\_A0*

The following I/O pins marked in [Figure 6-1](#) in *orange color* are supplied by VDDIO:

- Pin 3, DIO0
- Pin 4, DIO1
- Pin 5, DIO2
- Pin 6, DIO3
- Pin 7, DIO4
- Pin 8, DIO5
- Pin 10, DIO7
- Pin 11, DIO9\_SWDIO
- Pin 12, DIO10\_SWDCCK
- Pin 13, DIO11
- Pin 14, DIO12
- Pin 15, DIO15
- Pin 16, DIO16

The following I/O pins marked in [Figure 6-1](#) in *blue color* are supplied by VDDS:

- Pin 19, DIO17\_A8
- Pin 20, DIO18\_A7
- Pin 21, DIO19\_A6
- Pin 22, DIO20\_A5
- Pin 23, DIO21\_A4
- Pin 24, DIO22\_A3
- Pin 26, DIO23\_X32P
- Pin 27, DIO24\_X32N
- Pin 32, DIO27\_A1
- Pin 33, DIO28\_A0

## 6.2 Signal Descriptions

### 6.2.1 Signal Descriptions—RHA Package

**Table 6-1. Signal Descriptions—RHA Package**

| PIN          |     | I/O | TYPE    | DESCRIPTION                                                                                                   |
|--------------|-----|-----|---------|---------------------------------------------------------------------------------------------------------------|
| NAME         | NO. |     |         |                                                                                                               |
| VDDR         | 1   | —   | Power   | Internal supply, must be powered from the internal DC/DC converter or the GLDO <sup>(1)</sup> (2) (3)         |
| VDDR         | 2   | —   | Power   | Internal supply, must be powered from the internal DC/DC converter or the internal LDO <sup>(1)</sup> (2) (3) |
| DIO0         | 3   | I/O | Digital | GPIO                                                                                                          |
| DIO1         | 4   | I/O | Digital | GPIO                                                                                                          |
| DIO2         | 5   | I/O | Digital | GPIO, high-drive capability                                                                                   |
| DIO3         | 6   | I/O | Digital | GPIO, high-drive capability                                                                                   |
| DIO4         | 7   | I/O | Digital | GPIO                                                                                                          |
| DIO5         | 8   | I/O | Digital | GPIO                                                                                                          |
| VDDIO        | 9   | —   | Power   | 1.71V to 3.8V split rail I/O supply <sup>(4)</sup>                                                            |
| DIO7         | 10  | I/O | Digital | GPIO                                                                                                          |
| DIO9_SWDIO   | 11  | I/O | Digital | GPIO, SWD interface: mode select or SWDIO, high-drive capability                                              |
| DIO10_SWDCCK | 12  | I/O | Digital | GPIO, SWD interface: serial wire clock, high-drive capability                                                 |
| DIO11        | 13  | I/O | Digital | GPIO                                                                                                          |
| DIO12        | 14  | I/O | Digital | GPIO                                                                                                          |
| DIO15        | 15  | I/O | Digital | GPIO                                                                                                          |
| DIO16        | 16  | I/O | Digital | GPIO                                                                                                          |

**Table 6-1. Signal Descriptions—RHA Package (continued)**

| PIN        |     | I/O | TYPE              | DESCRIPTION                                                                                                                                                   |
|------------|-----|-----|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME       | NO. |     |                   |                                                                                                                                                               |
| VDDIO      | 17  | —   | Power             | 1.71V to 3.8V split rail I/O supply <sup>(4)</sup>                                                                                                            |
| VDDS       | 18  | —   | Power             | 1.71V to 3.8V supply <sup>(4)</sup>                                                                                                                           |
| DIO17_A8   | 19  | I/O | Digital or Analog | GPIO, analog capability, high-drive capability                                                                                                                |
| DIO18_A7   | 20  | I/O | Digital or Analog | GPIO, analog capability, high-drive capability                                                                                                                |
| DIO19_A6   | 21  | I/O | Digital or Analog | GPIO, analog capability                                                                                                                                       |
| DIO20_A5   | 22  | I/O | Digital or Analog | GPIO, analog capability                                                                                                                                       |
| DIO21_A4   | 23  | I/O | Digital or Analog | GPIO, analog capability                                                                                                                                       |
| DIO22_A3   | 24  | I/O | Digital or Analog | GPIO, analog capability                                                                                                                                       |
| RSTN       | 25  | I   | Digital           | Reset, active low. No internal pullup resistor                                                                                                                |
| DIO23_X32P | 26  | I/O | Digital or Analog | GPIO, 32kHz crystal oscillator pin 1, optional TCXO input                                                                                                     |
| DIO24_X32N | 27  | I/O | Digital or Analog | GPIO, 32kHz crystal oscillator pin 2                                                                                                                          |
| VDDD       | 28  | —   | Power             | Internal 1.32V regulated core-supply. Connect an external 1µF decoupling capacitor. <sup>(1)</sup>                                                            |
| VDDS       | 29  | —   | Power             | 1.71V to 3.8V supply <sup>(4)</sup>                                                                                                                           |
| DCDC       | 30  | —   | Power             | Switching node of internal DC/DC converter <sup>(4)</sup>                                                                                                     |
| VDDS       | 31  | —   | Power             | 1.71V to 3.8V supply. Connect an external 10µF decoupling capacitor. <sup>(4)</sup>                                                                           |
| DIO27_A1   | 32  | I/O | Digital or Analog | GPIO, analog capability                                                                                                                                       |
| DIO28_A0   | 33  | I/O | Digital or Analog | GPIO, analog capability                                                                                                                                       |
| VDDR       | 34  | —   | Power             | Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10µF decoupling capacitor. <sup>(1) (2) (3)</sup> |
| X48P       | 35  | —   | Analog            | 48MHz crystal oscillator pin 1                                                                                                                                |
| X48N       | 36  | —   | Analog            | 48MHz crystal oscillator pin 2                                                                                                                                |
| NC         | 37  | —   | —                 | No Connect                                                                                                                                                    |
| VDDS       | 38  | —   | Power             | 1.71V to 3.8V supply <sup>(4)</sup>                                                                                                                           |
| ANT        | 39  | —   | RF                | 2.4GHz TX, RX                                                                                                                                                 |
| NC         | 40  | —   | —                 | No Connect <sup>(6)</sup>                                                                                                                                     |
| EGP        | —   | —   | GND               | Ground – exposed ground pad <sup>(5)</sup>                                                                                                                    |

(1) Do not supply external circuitry from this pin.

(2) VDDR pins 1, 2, and 34 must be tied together on the PCB.

(3) Output from internal DC/DC and LDO is trimmed to 1.5V.

(4) For more details, see the technical reference manual listed in [Documentation Support](#).

(5) EGP is the only ground connection for the device. A good electrical connection to the device ground on the printed circuit board (PCB) is imperative for proper device operation.

(6) This pin is not connected to the die. In the LP-EM-CC2745R10-Q1, LP-EM-CC2755P10 reference design, this pin is connected to ground to give better shielding on the antenna path.

## 6.3 Connections for Unused Pins and Modules

### 6.3.1 Connections for Unused Pins and Modules—RHA Package

**Table 6-2. Connections for Unused Pins—RHA Package**

| FUNCTION       | SIGNAL NAME      | PIN NUMBER         | ACCEPTABLE PRACTICE <sup>(1)</sup> | PREFERRED PRACTICE <sup>(1)</sup> |
|----------------|------------------|--------------------|------------------------------------|-----------------------------------|
| GPIO (digital) | DIO <sub>n</sub> | 3–8<br>10<br>13–16 | NC, GND, or VDDS                   | NC                                |

**Table 6-2. Connections for Unused Pins—RHA Package (continued)**

| FUNCTION                       | SIGNAL NAME          | PIN NUMBER     | ACCEPTABLE PRACTICE <sup>(1)</sup> | PREFERRED PRACTICE <sup>(1)</sup> |
|--------------------------------|----------------------|----------------|------------------------------------|-----------------------------------|
| SWD                            | DIO9_SWDIO           | 11             | NC, GND, or VDD5                   | NC <sup>(3)</sup>                 |
|                                | DIO10_SWDCCK         | 12             | NC, GND, or VDD5                   | NC <sup>(4)</sup>                 |
| GPIO (digital or analog)       | DIO <sub>n</sub> _Am | 19–24<br>32–33 | NC, GND, or VDD5                   | NC                                |
| 32.768kHz crystal              | DIO23_X32P           | 26             | NC or GND                          | NC                                |
|                                | DIO24_X32N           | 27             |                                    |                                   |
| DC/DC converter <sup>(2)</sup> | DCDC                 | 30             | NC                                 | NC                                |
|                                | VDD5                 | 18, 29, 31, 38 | VDD5                               | VDD5                              |
| Split Rail I/O supply          | VDDIO                | 9, 17          | VDD5                               | VDD5                              |

(1) NC = No connect

(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected, and the 10µF decoupling capacitor must be kept on the VDDR net.

(3) By default, an internal pullup is enabled on SWDIO.

(4) By default, an internal pulldown is enabled on SWDCCK.

## 6.4 Peripheral Pin Mapping

### 6.4.1 RHA Peripheral Pin Mapping

**Table 6-3. RHA (QFN40) Peripheral Pin Mapping**

| PIN NO. | PIN NAME | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION |
|---------|----------|-------------|----------------------------|------------------|------------------|
| QFN40   |          |             |                            |                  |                  |
| 1       | VDDR     | VDDR        | —                          | N/A              | N/A              |
| 2       | VDDR     | VDDR        | —                          | N/A              | N/A              |
| 3       | DIO0     | GPIO0       | I/O                        | 0                | I/O              |
|         |          | T0C0        |                            | 1                | I/O              |
|         |          | T1F         |                            | 2                | O                |
|         |          | T3C0N       |                            | 3                | O                |
|         |          | LPCO        |                            | 4                | O                |
|         |          | T1C0        |                            | 5                | I/O              |
| 4       | DIO1     | GPIO1       | I/O                        | 0                | I/O              |
|         |          | CAN0TX      |                            | 1                | O                |
|         |          | T1C0        |                            | 2                | I/O              |
|         |          | T2C0        |                            | 3                | I/O              |
|         |          | UART0TXD    |                            | 4                | O                |
|         |          | T1C1        |                            | 5                | I/O              |
|         |          | DTB15       |                            | 7                | O                |
| 5       | DIO2     | GPIO2       | I/O                        | 0                | I/O              |
|         |          | CAN0RX      |                            | 1                | I                |
|         |          | T1C1        |                            | 2                | I/O              |
|         |          | T0PE        |                            | 3                | O                |
|         |          | UART0RXD    |                            | 4                | I                |
|         |          | T1C2        |                            | 5                | I/O              |
|         |          | DTB14       |                            | 7                | O                |

**Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)**

| PIN NO.<br>QFN40 | PIN NAME     | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION |
|------------------|--------------|-------------|----------------------------|------------------|------------------|
| 6                | DIO3         | GPIO3       | I/O                        | 0                | I/O              |
|                  |              | SPI0SCLK    |                            | 1                | I/O              |
|                  |              | I2S0SCLK    |                            | 2                | I/O              |
|                  |              | T2PE        |                            | 3                | O                |
|                  |              | UART1TXD    |                            | 4                | O                |
|                  |              | T2C0        |                            | 5                | I/O              |
|                  |              | DTB13       |                            | 7                | O                |
| 7                | DIO4         | GPIO4       | I/O                        | 0                | I/O              |
|                  |              | SPI0PICO    |                            | 1                | I/O              |
|                  |              | SPI0POCI    |                            | 2                | I/O              |
|                  |              | T1C2        |                            | 3                | I/O              |
|                  |              | UART1RXD    |                            | 4                | I                |
|                  |              | T2C1        |                            | 5                | I/O              |
|                  |              | DTB12       |                            | 7                | O                |
| 8                | DIO5         | GPIO5       | I/O                        | 0                | I/O              |
|                  |              | SPI0POCI    |                            | 1                | I/O              |
|                  |              | SPI0PICO    |                            | 2                | I/O              |
|                  |              | T2C1        |                            | 3                | I/O              |
|                  |              | T3C1N       |                            | 4                | O                |
|                  |              | T2C2        |                            | 5                | I/O              |
|                  |              | DTB11       |                            | 7                | O                |
| 9                | VDDIO        | VDDIO       | —                          | N/A              | N/A              |
| 10               | DIO7         | GPIO7       | I/O                        | 0                | I/O              |
|                  |              | SPI0CSN     |                            | 1                | I/O              |
|                  |              | T2C2        |                            | 2                | I/O              |
|                  |              | I2S0WS      |                            | 3                | I/O              |
|                  |              | T3C2N       |                            | 4                | O                |
|                  |              | DTB10       |                            | 7                | O                |
| 11               | DIO9_SWDIO   | GPIO9       | I/O                        | 0                | I/O              |
|                  |              | T0C1        |                            | 1                | I/O              |
|                  |              | T2C0N       |                            | 2                | O                |
|                  |              | I2S0SD0     |                            | 3                | I/O              |
|                  |              | T0PE        |                            | 4                | O                |
|                  |              | I2C0SCL     |                            | 5                | I/O              |
| 12               | DIO10_SWDCCK | GPIO10      | I/O                        | 0                | I/O              |
|                  |              | T0C2        |                            | 1                | I/O              |
|                  |              | T2C1N       |                            | 2                | O                |
|                  |              | I2S0SD1     |                            | 3                | I/O              |
|                  |              | T2PE        |                            | 4                | O                |
|                  |              | I2C0SDA     |                            | 5                | I/O              |

**Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)**

| PIN NO.<br>QFN40 | PIN NAME | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION |
|------------------|----------|-------------|----------------------------|------------------|------------------|
| 13               | DIO11    | GPIO11      | I/O                        | 0                | I/O              |
|                  |          | SPI1POCI    |                            | 1                | I/O              |
|                  |          | SPI1PICO    |                            | 2                | I/O              |
|                  |          | SWO         |                            | 3                | O                |
|                  |          | T3C0        |                            | 4                | I/O              |
|                  |          | T1F         |                            | 5                | O                |
|                  |          | DTB9        |                            | 7                | O                |
| 14               | DIO12    | GPIO12      | I/O                        | 0                | I/O              |
|                  |          | SPI1PICO    |                            | 1                | I/O              |
|                  |          | SPI1POCI    |                            | 2                | I/O              |
|                  |          | T2C2N       |                            | 3                | O                |
|                  |          | T3C1        |                            | 4                | I/O              |
|                  |          | T3C2        |                            | 5                | I/O              |
|                  |          | DTB8        |                            | 7                | O                |
| 15               | DIO15    | GPIO15      | I/O                        | 0                | I/O              |
|                  |          | SPI1SCLK    |                            | 1                | I/O              |
|                  |          | T3C2        |                            | 2                | I/O              |
|                  |          | T1C0N       |                            | 3                | O                |
|                  |          | LPCO        |                            | 4                | O                |
|                  |          | T3C1        |                            | 5                | I/O              |
| 16               | DIO16    | GPIO16      | I/O                        | 0                | I/O              |
|                  |          | I2S0MCLK    |                            | 1                | O                |
|                  |          | SPI1CSN     |                            | 2                | I/O              |
|                  |          | EXTCI       |                            | 3                | I                |
|                  |          | T1F         |                            | 4                | I                |
|                  |          | T3C0        |                            | 5                | I/O              |
|                  |          | DTB7        |                            | 7                | O                |
| 17               | VDDIO    | VDDIO       | —                          | N/A              | N/A              |
| 18               | VDDS     | VDDS        | —                          | N/A              | N/A              |
| 19               | DIO17_A8 | GPIO17      | I/O                        | 0                | I/O              |
|                  |          | I2S0SCLK    |                            | 1                | I/O              |
|                  |          | UART0RTS    |                            | 2                | O                |
|                  |          | CAN0TX      |                            | 3                | O                |
|                  |          | T0C0        |                            | 4                | I/O              |
|                  |          | LRFD0       |                            | 5                | O                |
|                  |          | ADC8        |                            | 6                | I                |
|                  |          | DTB6        |                            | 7                | O                |

**Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)**

| PIN NO.<br>QFN40 | PIN NAME | SIGNAL NAME    | SIGNAL TYPE <sup>(1)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION |
|------------------|----------|----------------|----------------------------|------------------|------------------|
| 20               | DIO18_A7 | GPIO18         | I/O                        | 0                | I/O              |
|                  |          | I2S0WS         |                            | 1                | I/O              |
|                  |          | UART0CTS       |                            | 2                | I                |
|                  |          | CAN0RX         |                            | 3                | I                |
|                  |          | T0C1           |                            | 4                | I/O              |
|                  |          | LRFD1          |                            | 5                | O                |
|                  |          | ADC7           |                            | 6                | I                |
|                  |          | DTB5           |                            | 7                | O                |
| 21               | DIO19_A6 | GPIO19         | I/O                        | 0                | I/O              |
|                  |          | SPI0CSN        |                            | 1                | I/O              |
|                  |          | UART0TXD       |                            | 2                | O                |
|                  |          | UART0RXD       |                            | 3                | I                |
|                  |          | I2S0SD0        |                            | 4                | I/O              |
|                  |          | LRFD2          |                            | 5                | O                |
|                  |          | ADC6/LPC+      |                            | 6                | I                |
|                  |          | DTB4           |                            | 7                | O                |
| 22               | DIO20_A6 | GPIO20         | I/O                        | 0                | I/O              |
|                  |          | SPI0SCLK       |                            | 1                | I/O              |
|                  |          | UART0RXD       |                            | 2                | I                |
|                  |          | UART0TXD       |                            | 3                | O                |
|                  |          | I2S0SD1        |                            | 4                | I/O              |
|                  |          | LRFD3          |                            | 5                | O                |
|                  |          | ADC5/LPC+/LPC- |                            | 6                | I                |
|                  |          | DTB3           |                            | 7                | O                |
| 23               | DIO21_A4 | GPIO21         | I/O                        | 0                | I/O              |
|                  |          | SPI0PICO       |                            | 1                | I/O              |
|                  |          | UART1TXD       |                            | 2                | O                |
|                  |          | I2C0SCL        |                            | 3                | I/O              |
|                  |          | T1C1N          |                            | 4                | O                |
|                  |          | LRFD4          |                            | 5                | O                |
|                  |          | ADC4/LPC+/LPC- |                            | 6                | I                |
|                  |          | DTB2           |                            | 7                | O                |
| 24               | DIO22_A3 | GPIO22         | I/O                        | 0                | I/O              |
|                  |          | SPI0POCI       |                            | 1                | I/O              |
|                  |          | UART1RXD       |                            | 2                | I                |
|                  |          | I2C0SDA        |                            | 3                | I/O              |
|                  |          | T1C2N          |                            | 4                | O                |
|                  |          | LRFD5          |                            | 5                | O                |
|                  |          | ADC3           |                            | 6                | I                |
|                  |          | DTB1           |                            | 7                | O                |
| 25               | RTSN     | RSTN           | —                          | N/A              | N/A              |

**Table 6-3. RHA (QFN40) Peripheral Pin Mapping (continued)**

| PIN NO.<br>QFN40 | PIN NAME   | SIGNAL NAME | SIGNAL TYPE <sup>(1)</sup> | PIN MUX ENCODING | SIGNAL DIRECTION |
|------------------|------------|-------------|----------------------------|------------------|------------------|
| 26               | DIO23_X32P | GPIO23      | I/O                        | 0                | I/O              |
|                  |            | SPI1CSN     |                            | 1                | I/O              |
|                  |            | UART1RTS    |                            | 2                | O                |
|                  |            | LFCl        |                            | 3                | I                |
|                  |            | T0C2        |                            | 4                | I/O              |
|                  |            | T1C0        |                            | 5                | I/O              |
|                  |            | LFXT_P      |                            | 6                | I                |
| 27               | DIO24_X32N | GPIO24      | I/O                        | 0                | I/O              |
|                  |            | SPI1SCLK    |                            | 1                | I/O              |
|                  |            | UART1CTS    |                            | 2                | I                |
|                  |            | T0C0N       |                            | 3                | O                |
|                  |            | LPCO        |                            | 4                | O                |
|                  |            | T0C0        |                            | 5                | I/O              |
|                  |            | LFXT_N      |                            | 6                | I                |
| 28               | VDDD       | VDDD        | —                          | N/A              | N/A              |
| 29               | VDDS       | VDDS        | —                          | N/A              | N/A              |
| 30               | DCDC       | DCDC        | —                          | N/A              | N/A              |
| 31               | VDDS       | VDDS        | —                          | N/A              | N/A              |
| 32               | DIO27_A1   | GPIO27      | I/O                        | 0                | I/O              |
|                  |            | SPI1PICO    |                            | 1                | I/O              |
|                  |            | I2C0SCL     |                            | 2                | I/O              |
|                  |            | CKMIN       |                            | 3                | I                |
|                  |            | T0C1N       |                            | 4                | O                |
|                  |            | LRFD6       |                            | 5                | O                |
|                  |            | ADC1/AREF+  |                            | 6                | I                |
|                  |            | DTB0        |                            | 7                | O                |
| 33               | DIO28_A0   | GPIO28      | I/O                        | 0                | I/O              |
|                  |            | SPI1POCI    |                            | 1                | I/O              |
|                  |            | I2C0SDA     |                            | 2                | I/O              |
|                  |            | T3C0N       |                            | 3                | O                |
|                  |            | T0C2N       |                            | 4                | O                |
|                  |            | LRFD7       |                            | 5                | O                |
|                  |            | ADC0/AREF-  |                            | 6                | I                |
| 34               | VDDR       | VDDR        | —                          | N/A              | N/A              |
| 35               | X48P       | X48P        | —                          | N/A              | N/A              |
| 36               | X48N       | X48N        | —                          | N/A              | N/A              |
| 37               | NC         | NC          | —                          | N/A              | N/A              |
| 38               | VDDS       | VDDS        | —                          | N/A              | N/A              |
| 39               | ANT        | ANT         | —                          | N/A              | N/A              |
| 40               | NC         | NC          | —                          | N/A              | N/A              |
| —                | EGP        | GND         | —                          | N/A              | N/A              |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 6.5 Peripheral Signal Descriptions

### 6.5.1 RHA Peripheral Signal Descriptions

**Table 6-4. RHA (QFN40) Peripheral Signal Descriptions**

| FUNCTION      | SIGNAL NAME | Pin No.<br>QFN40 | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                                                                            |
|---------------|-------------|------------------|----------|------------------|----------------------------------------------------------------------------------------|
| ADC           | ADC0        | 33               | I/O      | I                | ADC channel 0 input                                                                    |
|               | ADC1        | 32               |          |                  | ADC channel 1 input                                                                    |
|               | ADC3        | 24               |          |                  | ADC channel 3 input                                                                    |
|               | ADC4        | 23               |          |                  | ADC channel 4 input                                                                    |
|               | ADC5        | 22               |          |                  | ADC channel 5 input                                                                    |
|               | ADC6        | 21               |          |                  | ADC channel 6 input                                                                    |
|               | ADC7        | 20               |          |                  | ADC channel 7 input                                                                    |
|               | ADC8        | 19               |          |                  | ADC channel 8 input                                                                    |
| ADC Reference | AREF+       | 32               | I/O      | I                | ADC external voltage reference, positive terminal                                      |
|               | AREF-       | 33               |          |                  | ADC external voltage reference, negative terminal                                      |
| CAN-FD        | CAN0TX      | 4                | I/O      | O                | CAN0 transmit data output                                                              |
|               |             | 19               |          |                  |                                                                                        |
|               | CAN0RX      | 5                | I/O      | I                | CAN0 receive data input                                                                |
|               |             | 20               |          |                  |                                                                                        |
| Clock         | X32P        | 26               | I/O      | I                | 32kHz crystal oscillator pin 1                                                         |
|               | X32N        | 27               | I/O      | I                | 32kHz crystal oscillator pin 2                                                         |
|               | X48P        | 35               | —        | I                | 48MHz crystal oscillator pin 1, Optional TCXO input                                    |
|               | X48N        | 36               | —        | I                | 48MHz crystal oscillator pin 2                                                         |
|               | CKMIN       | 32               | I/O      | I                | HFOSC tracking loop reference clock input                                              |
|               | LFCI        | 26               | I/O      | I                | GPIO input for low frequency clock input (LFXT bypass clock from pin) or optional TCXO |
| Comparator    | LPCO        | 3                | I/O      | O                | Low power comparator output                                                            |
|               |             | 15               |          |                  |                                                                                        |
|               |             | 27               |          |                  |                                                                                        |
|               | LPC+        | 21               | I/O      | I                | Low power comparator positive input terminal                                           |
|               |             | 22               |          |                  |                                                                                        |
|               |             | 23               |          |                  |                                                                                        |
|               | LPC-        | 22               |          |                  | Lower power comparator negative input terminal                                         |
|               |             | 23               |          |                  |                                                                                        |

**Table 6-4. RHA (QFN40) Peripheral Signal Descriptions (continued)**

| FUNCTION         | SIGNAL NAME | Pin No. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                     |
|------------------|-------------|---------|----------|------------------|---------------------------------|
|                  |             | QFN40   |          |                  |                                 |
| Digital Test Bus | DTB0        | 32      | I/O      | O                | Digital test bus output 0       |
|                  | DTB1        | 24      |          |                  | Digital test bus output 1       |
|                  | DTB2        | 23      |          |                  | Digital test bus output 2       |
|                  | DTB3        | 22      |          |                  | Digital test bus output 3       |
|                  | DTB4        | 21      |          |                  | Digital test bus output 4       |
|                  | DTB5        | 20      |          |                  | Digital test bus output 5       |
|                  | DTB6        | 19      |          |                  | Digital test bus output 6       |
|                  | DTB7        | 16      |          |                  | Digital test bus output 7       |
|                  | DTB8        | 14      |          |                  | Digital test bus output 8       |
|                  | DTB9        | 13      |          |                  | Digital test bus output 9       |
|                  | DTB10       | 10      |          |                  | Digital test bus output 10      |
|                  | DTB11       | 8       |          |                  | Digital test bus output 11      |
|                  | DTB12       | 7       |          |                  | Digital test bus output 12      |
|                  | DTB13       | 6       |          |                  | Digital test bus output 13      |
|                  | DTB14       | 5       |          |                  | Digital test bus output 14      |
|                  | DTB15       | 4       |          |                  | Digital test bus output 15      |
| GPIO             | GPIO0       | 3       | I/O      | I/O              | General-purpose input or output |
|                  | GPIO1       | 4       |          |                  |                                 |
|                  | GPIO2       | 5       |          |                  |                                 |
|                  | GPIO3       | 6       |          |                  |                                 |
|                  | GPIO4       | 7       |          |                  |                                 |
|                  | GPIO5       | 8       |          |                  |                                 |
|                  | GPIO7       | 10      |          |                  |                                 |
|                  | GPIO9       | 11      |          |                  |                                 |
|                  | GPIO10      | 12      |          |                  |                                 |
|                  | GPIO11      | 13      |          |                  |                                 |
|                  | GPIO12      | 14      |          |                  |                                 |
|                  | GPIO15      | 15      |          |                  |                                 |
|                  | GPIO16      | 16      |          |                  |                                 |
|                  | GPIO17      | 19      |          |                  |                                 |
|                  | GPIO18      | 20      |          |                  |                                 |
|                  | GPIO19      | 21      |          |                  |                                 |
|                  | GPIO20      | 22      |          |                  |                                 |
|                  | GPIO21      | 23      |          |                  |                                 |
|                  | GPIO22      | 24      |          |                  |                                 |
|                  | GPIO23      | 26      |          |                  |                                 |
|                  | GPIO24      | 27      |          |                  |                                 |
|                  | GPIO27      | 32      |          |                  |                                 |
|                  | GPIO28      | 33      |          |                  |                                 |

**Table 6-4. RHA (QFN40) Peripheral Signal Descriptions (continued)**

| FUNCTION           | SIGNAL NAME | Pin No. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                                             |
|--------------------|-------------|---------|----------|------------------|---------------------------------------------------------|
|                    |             | QFN40   |          |                  |                                                         |
| I <sup>2</sup> C   | I2C0SCL     | 11      | I/O      | I/O              | I <sup>2</sup> C clock                                  |
|                    |             | 23      |          |                  |                                                         |
|                    |             | 32      |          |                  |                                                         |
|                    | I2C0SDA     | 12      | I/O      | I/O              | I <sup>2</sup> C data                                   |
|                    |             | 24      |          |                  |                                                         |
|                    |             | 33      |          |                  |                                                         |
| I <sup>2</sup> S   | I2S0MCLK    | 16      | I/O      | O                | I <sup>2</sup> S main clock                             |
|                    | I2S0SCLK    | 6       | I/O      | I/O              | I <sup>2</sup> S serial clock                           |
|                    |             | 19      |          |                  |                                                         |
|                    | I2S0WS      | 10      | I/O      | I/O              | I <sup>2</sup> S word select                            |
|                    |             | 20      |          |                  |                                                         |
|                    | I2S0SD0     | 11      | I/O      | I/O              | I <sup>2</sup> S serial data 0                          |
|                    |             | 21      |          |                  |                                                         |
|                    | I2S0SD1     | 12      | I/O      | I/O              | I <sup>2</sup> S serial data 1                          |
|                    |             | 22      |          |                  |                                                         |
|                    | EXTCI       | 16      | I/O      | I                | I <sup>2</sup> S external clock                         |
| LRF Digital Output | LRFD0       | 19      | I/O      | O                | LRF digital output 0                                    |
|                    | LRFD1       | 20      |          |                  | LRF digital output 1                                    |
|                    | LRFD2       | 21      |          |                  | LRF digital output 2                                    |
|                    | LRFD3       | 22      |          |                  | LRF digital output 3                                    |
|                    | LRFD4       | 23      |          |                  | LRF digital output 4                                    |
|                    | LRFD5       | 24      |          |                  | LRF digital output 5                                    |
|                    | LRFD6       | 32      |          |                  | LRF digital output 6                                    |
|                    | LRFD7       | 33      |          |                  | LRF digital output 7                                    |
| Power              | VDDR        | 1       | —        | —                | Internal supply                                         |
|                    |             | 2       |          |                  |                                                         |
|                    |             | 34      |          |                  |                                                         |
|                    | VDDS        | 18      | —        | —                | 1.71V to 3.8V DIO supply                                |
|                    |             | 29      |          |                  |                                                         |
|                    |             | 31      |          |                  |                                                         |
|                    |             | 38      |          |                  |                                                         |
|                    | VDDD        | 28      | —        | —                | For decoupling of internal 1.32V regulated core-supply. |
|                    | VDDIO       | 9       | —        | —                | 1.71V to 3.8V split rail I/O supply                     |
|                    |             | 17      |          |                  |                                                         |
|                    | DCDC        | 30      | —        | —                | Switching node of internal DC/DC converter              |
| Reset              | RSTN        | 25      | —        | —                | Global master device reset (active low)                 |
| RF                 | ANT         | 39      | —        | —                | 50-ohm RF port                                          |

**Table 6-4. RHA (QFN40) Peripheral Signal Descriptions (continued)**

| FUNCTION | SIGNAL NAME | Pin No. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                       |
|----------|-------------|---------|----------|------------------|-----------------------------------|
|          |             | QFN40   |          |                  |                                   |
| SPI      | SPI0SCLK    | 6       | I/O      | I/O              | SPI0 clock                        |
|          |             | 22      |          |                  |                                   |
|          | SPI0POCI    | 7       | I/O      | I/O              | SPI0 peripheral out controller in |
|          |             | 8       |          |                  |                                   |
|          |             | 24      |          |                  |                                   |
|          | SPI0CSN     | 10      | I/O      | I/O              | SPI0 chip-select                  |
|          |             | 21      |          |                  |                                   |
|          | SPI0PICO    | 7       | I/O      | I/O              | SPI0 peripheral in controller out |
|          |             | 8       |          |                  |                                   |
|          |             | 23      |          |                  |                                   |
|          | SPI1SCLK    | 15      | I/O      | I/O              | SPI1 clock                        |
|          |             | 27      |          |                  |                                   |
|          | SPI1POCI    | 13      | I/O      | I/O              | SPI1 peripheral out controller in |
|          |             | 14      |          |                  |                                   |
|          |             | 33      |          |                  |                                   |
|          | SPI1CSN     | 16      | I/O      | I/O              | SPI1 chip select                  |
|          |             | 26      |          |                  |                                   |
|          | SPI1PICO    | 13      | I/O      | I/O              | SPI1 peripheral in controller out |
|          |             | 14      |          |                  |                                   |
|          |             | 32      |          |                  |                                   |
| SWD      | SWDIO       | 11      | I/O      | I/O              | Serial wire data input/output     |
|          | SWDCK       | 12      | I/O      | I                | Serial wire clock input           |
| Trace    | SWO         | 13      | I/O      | O                | Serial wire output                |

**Table 6-4. RHA (QFN40) Peripheral Signal Descriptions (continued)**

| FUNCTION                           | SIGNAL NAME | Pin No. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                                     |
|------------------------------------|-------------|---------|----------|------------------|-------------------------------------------------|
|                                    |             | QFN40   |          |                  |                                                 |
| Timers - Capture/Compare           | T0C0        | 3       | I/O      | I/O              | Capture input-0 / compare output-0 of Timer-0   |
|                                    |             | 19      |          |                  |                                                 |
|                                    |             | 27      |          |                  |                                                 |
|                                    | T0C1        | 11      |          |                  | Capture input-1 / compare output-1 of Timer-0   |
|                                    |             | 20      |          |                  |                                                 |
|                                    | T0C2        | 12      |          |                  | Capture input-2 / compare output-2 of Timer-0   |
|                                    |             | 26      |          |                  |                                                 |
|                                    | T1C0        | 3       | I/O      | I/O              | Capture input-0 / compare output-0 of Timer-1   |
|                                    |             | 4       |          |                  |                                                 |
|                                    |             | 26      |          |                  |                                                 |
|                                    | T1C1        | 4       |          |                  | Capture input-1 / compare output-1 of Timer-1   |
|                                    |             | 5       |          |                  |                                                 |
|                                    | T1C2        | 5       |          |                  | Capture input-2 / compare output-2 of Timer-1   |
|                                    |             | 7       |          |                  |                                                 |
|                                    | T2C0        | 4       | I/O      | I/O              | Capture input-0 / compare output-0 of Timer-2   |
|                                    |             | 6       |          |                  |                                                 |
|                                    | T2C1        | 7       |          |                  | Capture input-1 / compare output-1 of Timer-2   |
|                                    |             | 8       |          |                  |                                                 |
|                                    | T2C2        | 8       |          |                  | Capture input-2 / compare output-2 of Timer-2   |
|                                    |             | 10      |          |                  |                                                 |
|                                    | T3C0        | 13      | I/O      | I/O              | Capture input-0 / compare output-0 of Timer-3   |
|                                    |             | 16      |          |                  |                                                 |
|                                    | T3C1        | 14      |          |                  | Capture input-1 / compare output-1 of Timer-3   |
|                                    |             | 15      |          |                  |                                                 |
|                                    | T3C2        | 14      |          |                  | Capture input-2 / compare output-2 of Timer-3   |
|                                    |             | 15      |          |                  |                                                 |
| Timers - Complementary Capture/PWM | T0C0N       | 27      | I/O      | O                | Complementary compare/PWM output-0 from Timer-0 |
|                                    | T0C1N       | 32      |          |                  | Complementary compare/PWM output-1 from Timer-0 |
|                                    | T0C2N       | 33      |          |                  | Complementary compare/PWM output-2 from Timer-0 |
|                                    | T1C0N       | 15      | I/O      | O                | Complementary compare/PWM output-0 from Timer-1 |
|                                    | T1C1N       | 23      |          |                  | Complementary compare/PWM output-1 from Timer-1 |
|                                    | T1C2N       | 24      |          |                  | Complementary compare/PWM output-2 from Timer-1 |
|                                    | T2C0N       | 11      | I/O      | O                | Complementary compare/PWM output-0 from Timer-2 |
|                                    | T2C1N       | 12      |          |                  | Complementary compare/PWM output-1 from Timer-2 |
|                                    | T2C2N       | 14      |          |                  | Complementary compare/PWM output-2 from Timer-2 |
|                                    | T3C0N       | 3       | I/O      | O                | Complementary compare/PWM output-0 from Timer-3 |
|                                    |             | 33      |          |                  |                                                 |
|                                    | T3C1N       | 8       |          |                  | Complementary compare/PWM output-1 from Timer-3 |
|                                    | T3C2N       | 10      |          |                  | Complementary compare/PWM output-2 from Timer-3 |
| Timers - Fault input               | T1F         | 3       | I/O      | I                | Fault input for Timer-1                         |
|                                    |             | 13      |          |                  |                                                 |
|                                    |             | 16      |          |                  |                                                 |

**Table 6-4. RHA (QFN40) Peripheral Signal Descriptions (continued)**

| FUNCTION                 | SIGNAL NAME | Pin No. | PIN TYPE | SIGNAL DIRECTION | DESCRIPTION                            |
|--------------------------|-------------|---------|----------|------------------|----------------------------------------|
|                          |             | QFN40   |          |                  |                                        |
| Timers - Prescaler Event | T0PE        | 5       | I/O      | O                | Prescaler event output from Timer-0    |
|                          |             | 11      |          |                  |                                        |
|                          | T2PE        | 6       | I/O      | O                | Prescaler event output from Timer-2    |
|                          |             | 12      |          |                  |                                        |
| UART                     | UART0TXD    | 4       | I/O      | O                | UART0 TX data                          |
|                          |             | 21      |          |                  |                                        |
|                          |             | 22      |          |                  |                                        |
|                          | UART0RXD    | 5       | I/O      | I                | UART0 RX data                          |
|                          |             | 21      |          |                  |                                        |
|                          |             | 22      |          |                  |                                        |
|                          | UART0CTS    | 20      | I/O      | I                | UART0 clear-to-send input (active low) |
|                          | UART0RTS    | 19      | I/O      | O                | UART0 request-to-send (active low)     |
|                          | UART1TXD    | 6       | I/O      | O                | UART1 TX data                          |
|                          |             | 23      |          |                  |                                        |
|                          | UART1RXD    | 7       | I/O      | I                | UART1 RX data                          |
|                          |             | 24      |          |                  |                                        |
|                          | UART1CTS    | 27      | I/O      | I                | UART1 clear-to-send input (active low) |
|                          | UART1RTS    | 26      | I/O      | O                | UART1 request-to-send (active low)     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                     |                                                  | MIN  | MAX                                                       | UNIT |
|---------------------|--------------------------------------------------|------|-----------------------------------------------------------|------|
| V <sub>DDS</sub>    | Supply voltage                                   | −0.3 | 4.1                                                       | V    |
| V <sub>DIO</sub>    | Split rail I/O supply voltage                    | −0.3 | 4.1                                                       | V    |
| V <sub>in_dio</sub> | Voltage on any digital pin <sup>(3) (4)</sup>    | −0.3 | V <sub>DDS</sub> + 0.3 or V <sub>DIO</sub> + 0.3, max 4.1 | V    |
| V <sub>in_x48</sub> | Voltage on crystal oscillator pins X48P and X48N | −0.3 | 1.24                                                      | V    |
| V <sub>in_adc</sub> | Voltage on ADC input                             | 0    | V <sub>DDS</sub>                                          | V    |
| V <sub>in_rf</sub>  | Input level, RF pins                             |      | 10                                                        | dBm  |
| I <sub>in_dio</sub> | Input clamp current on any DIO pin               |      | ±2                                                        | mA   |
| T <sub>stg</sub>    | Storage temperature                              | −55  | 150                                                       | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to ground, unless otherwise noted.
- (3) Including analog capable DIOs
- (4) For list of digital IO pins that are powered by V<sub>DDS</sub> or V<sub>DIO</sub>, refer to the *Pin Configurations and Functions* section in the data sheet.

### 7.2 ESD and MSL Ratings

|      |                            |                                                                 |                 | VALUE            | UNIT |
|------|----------------------------|-----------------------------------------------------------------|-----------------|------------------|------|
| VESD | Electrostatic discharge    | Human body model (HBM), per AEC Q100-002 <sup>(1) (3) (4)</sup> | pins except ANT | ±2000            | V    |
|      |                            |                                                                 | ANT pin         | ±1000            | V    |
|      |                            | Charged device model (CDM), per AEC Q100-011 <sup>(2) (4)</sup> | pins except ANT | ±500             | V    |
|      |                            |                                                                 | ANT pin         | ±250             | V    |
| MSL  | Moisture Sensitivity Level |                                                                 |                 | 2 <sup>(5)</sup> |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
- (3) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (4) The ANT pin is an RF type pin, per *Absolute Maximum Ratings* table and complies with recommended ESD limits per JEP and AEC specifications listed above.
- (5) The Moisture Sensitivity Level rating is according to the IPC/JEDEC J-STD-020 industry standard classifications.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

|                                                            | MIN  | MAX | UNIT  |
|------------------------------------------------------------|------|-----|-------|
| Operating ambient temperature <sup>(1) (2)</sup>           | −40  | 125 | °C    |
| Operating junction temperature <sup>(1) (2)</sup>          | −40  | 125 | °C    |
| Operating supply voltage (V <sub>DDS</sub> )               | 1.71 | 3.8 | V     |
| Operating split rail IO supply voltage (V <sub>DIO</sub> ) | 1.71 | 3.8 | V     |
| Rising supply voltage slew rate                            | 0    | 100 | mV/μs |
| Falling supply voltage slew rate <sup>(3)</sup>            | 0    | 1   | mV/μs |

- (1) Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.
- (2) For thermal resistance characteristics refer to *Thermal Resistance Characteristics* table in this document.
- (3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 10μF V<sub>DDS</sub> input capacitor must be used to enable compliance with this slew rate.

## 7.4 DC/DC

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDs}} = 3.0\text{V}$  with DC/DC enabled (unless otherwise noted)

| PARAMETER                                             | TEST CONDITIONS                                      | MIN | TYP | MAX | UNIT          |
|-------------------------------------------------------|------------------------------------------------------|-----|-----|-----|---------------|
| VDDS supply voltage for DCDC operation <sup>(1)</sup> |                                                      | 2.2 | 3.0 | 3.8 | V             |
| Inductor at VDDR pin                                  | Typical value of the component on PCB <sup>(2)</sup> |     | 6.8 |     | $\mu\text{H}$ |
| Load capacitor at VDDR pin                            | Typical value of the component on PCB <sup>(2)</sup> |     | 10  |     | $\mu\text{F}$ |

- (1) When the supply voltage drops below the DCDC operation min voltage, the device smoothly transitions to use the on-chip GLDO regulator.  
(2) The capacitor and inductor tolerances of up to  $\pm 50\%$  across temperature and overall part tolerance are considered.

## 7.5 GLDO

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDs}} = 3.0\text{V}$

| PARAMETER                              | TEST CONDITIONS                                      | MIN  | TYP | MAX | UNIT          |
|----------------------------------------|------------------------------------------------------|------|-----|-----|---------------|
| VDDS supply voltage for GLDO operation |                                                      | 1.71 | 3.0 | 3.8 | V             |
| Load capacitor at VDDR pin             | Typical value of the component on PCB <sup>(1)</sup> |      | 10  |     | $\mu\text{F}$ |

- (1) Capacitor tolerance of up to  $\pm 50\%$  across temperature and overall part tolerance is considered.

## 7.6 Power Supply and Modules

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                         | TEST CONDITIONS                    | MIN | TYP  | MAX | UNIT |
|---------------------------------------------------|------------------------------------|-----|------|-----|------|
| <b>VDDS BOD (brown-out detector)</b>              |                                    |     |      |     |      |
| Untrimmed brownout rising threshold               | Before initial boot <sup>(1)</sup> |     | 1.62 |     | V    |
| Trimmed brownout rising threshold <sup>(1)</sup>  |                                    |     | 1.68 |     | V    |
| Trimmed brownout falling threshold <sup>(1)</sup> |                                    |     | 1.67 |     | V    |
| <b>VDDS POR (power-on-reset)</b>                  |                                    |     |      |     |      |
| POR power-up level                                |                                    |     | 1.5  |     | V    |
| POR power-down level                              |                                    |     | 1.45 |     | V    |

- (1) The brown-out detector is trimmed at initial boot. The value is kept until device is reset by a POR reset or the RSTN pin.

## 7.7 Battery Monitor

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ , unless otherwise noted.

| PARAMETER  | TEST CONDITIONS | MIN  | TYP | MAX | UNIT |
|------------|-----------------|------|-----|-----|------|
| Resolution |                 |      | 22  |     | mV   |
| Range      |                 | 1.71 |     | 3.8 | V    |
| Accuracy   | VDDS = 3.0V     |      | 30  |     | mV   |

## 7.8 BATMON Temperature Sensor

Measured on the LP-EM-CC2745R10-Q1 reference design with  $V_{\text{DDs}} = 3.0\text{V}$  (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                          | MIN | TYP       | MAX | UNIT             |
|------------|------------------------------------------|-----|-----------|-----|------------------|
| Resolution | $T_c = 25^\circ\text{C}$                 |     | 1.7       |     | $^\circ\text{C}$ |
| Accuracy   | $-40^\circ\text{C}$ to $0^\circ\text{C}$ |     | $\pm 4.0$ |     | $^\circ\text{C}$ |
| Accuracy   | $0^\circ\text{C}$ to $125^\circ\text{C}$ |     | $\pm 2.5$ |     | $^\circ\text{C}$ |

## 7.9 Power Consumption—Power Modes

Measured on the LP-EM-CC2745R10-Q1 reference design  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{V}$ , DC/DC enabled (unless otherwise noted)

| PARAMETER                                  |                  | TEST CONDITIONS                                                                                                       | MIN | TYP  | MAX | UNIT          |
|--------------------------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------|-----|------|-----|---------------|
| <b>Core Current Consumption with DCDC</b>  |                  |                                                                                                                       |     |      |     |               |
| $I_{\text{core}}$                          | Active           | MCU running CoreMark from Flash at 96MHz                                                                              |     | 7.2  |     | mA            |
| $I_{\text{core}}$                          | Active           | MCU running CoreMark from Flash at 96MHz, VDD5 = 3.3V                                                                 |     | 6.8  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash disabled, DMA disabled                                                         |     | 1.5  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash disabled, DMA disabled, VDD5 = 3.3V                                            |     | 1.45 |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash disabled, DMA enabled                                                          |     | 1.7  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash disabled, DMA enabled, VDD5 = 3.3V                                             |     | 1.6  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash enabled, DMA disabled                                                          |     | 1.9  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash enabled, DMA disabled, VDD5 = 3.3V                                             |     | 1.8  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash enabled, DMA enabled                                                           |     | 2.2  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and SRAM powered, flash enabled, DMA enabled, VDD5 = 3.3V                                              |     | 2.1  |     | mA            |
| $I_{\text{core}}$                          | Standby          | RTC running, full SRAM retention<br>LFOSC, DCDC recharge current setting ( $i_{\text{peak}}^{(1)} = 0$ )              |     | 0.95 |     | $\mu\text{A}$ |
| $I_{\text{core}}$                          | Standby          | RTC running, full SRAM retention<br>LFOSC, DCDC recharge current setting ( $i_{\text{peak}}^{(1)} = 0$ ), VDD5 = 3.3V |     | 0.9  |     | $\mu\text{A}$ |
| $I_{\text{core}}$                          | Standby          | RTC running, full SRAM retention<br>LFXT DCDC recharge current setting ( $i_{\text{peak}}^{(1)} = 0$ )                |     | 1.0  |     | $\mu\text{A}$ |
| $I_{\text{core}}$                          | Standby          | RTC running, full SRAM retention<br>LFXT DCDC recharge current setting ( $i_{\text{peak}}^{(1)} = 0$ ), VDD5 = 3.3V   |     | 0.9  |     | $\mu\text{A}$ |
| <b>Core Current consumption with GLDO</b>  |                  |                                                                                                                       |     |      |     |               |
| $I_{\text{core}}$                          | Active           | MCU running CoreMark from Flash at 96 MHz, DC/DC disabled                                                             |     | 11.2 |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and RAM powered, flash disabled, DMA disabled, DC/DC disabled                                          |     | 2.45 |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and RAM powered, flash disabled, DMA enabled, DC/DC disabled                                           |     | 2.75 |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and RAM powered, flash enabled, DMA disabled, DC/DC disabled                                           |     | 2.8  |     | mA            |
| $I_{\text{core}}$                          | Idle             | Supply Systems and RAM powered, flash enabled, DMA enabled, DC/DC disabled                                            |     | 3.4  |     | mA            |
| $I_{\text{core}}$                          | Standby          | RTC running, full SRAM retention, DC/DC disabled<br>LFOSC, default GLDO recharge current setting                      |     | 1.5  |     | $\mu\text{A}$ |
| $I_{\text{core}}$                          | Standby          | RTC running, full SRAM retention, DC/DC disabled<br>LFXT, default GLDO recharge current setting                       |     | 1.6  |     | $\mu\text{A}$ |
| <b>Reset, Shutdown Current Consumption</b> |                  |                                                                                                                       |     |      |     |               |
| $I_{\text{core}}$                          | Reset            | Reset. RSTN pin asserted or VDD5 below power-on-reset threshold                                                       |     | 170  |     | nA            |
| $I_{\text{core}}$                          | Shutdown         | Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled                                 |     | 160  |     | nA            |
| <b>Peripheral Current Consumption</b>      |                  |                                                                                                                       |     |      |     |               |
| $I_{\text{peri}}$                          | RF               | Delta current with clock enabled, RF subsystem idle                                                                   |     | 80   |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | Timers           | Delta current with clock enabled, module is idle <sup>(2)</sup>                                                       |     | 6.5  |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | I <sup>2</sup> C | Delta current with clock enabled, module is idle                                                                      |     | 11   |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | SPI              | Delta current with clock enabled, module is idle <sup>(3)</sup>                                                       |     | 5    |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | UART             | Delta current with clock enabled, module is idle <sup>(4)</sup>                                                       |     | 43   |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | I <sup>2</sup> S | Delta current with clock enabled, module is idle                                                                      |     | 190  |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | CRYPTO (LAES)    | Delta current with clock enabled, module is idle                                                                      |     | 10   |     | $\mu\text{A}$ |
| $I_{\text{peri}}$                          | APU              | Delta current with clock enabled, module is idle                                                                      |     | 186  |     | $\mu\text{A}$ |

(1)  $i_{\text{peak}}$  refers to the programmable DCDC peak current setting used to vary the maximum DCDC load support.

(2) Only one LGPT timer instance enabled

(3) Only one SPI peripheral instance enabled

(4) Only one UART peripheral instance enabled

## 7.10 Power Consumption—Radio Modes (R variant)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$  with DC/DC enabled (unless otherwise noted)

| PARAMETER       |                        | TEST CONDITIONS                                                                                          | MIN | TYP  | MAX | UNIT |
|-----------------|------------------------|----------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| $I_{\text{RX}}$ | Radio receive current  | 2440MHz, 1Mbps, system bus off <sup>(1)</sup>                                                            |     | 6.7  |     | mA   |
| $I_{\text{RX}}$ | Radio receive current  | 2440MHz, 1Mbps, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>                           |     | 6.1  |     | mA   |
| $I_{\text{RX}}$ | Radio receive current  | 2440MHz, 1Mbps, DC/DC disabled, system bus off <sup>(1)</sup>                                            |     | 11.7 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | -8dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 5.7  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | -8dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 5.3  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | 0dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                      |     | 8.4  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | 0dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>     |     | 7.7  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | 0dBm output power setting<br>2440MHz DC/DC disabled, system bus off <sup>(1)</sup>                       |     | 14.7 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +4dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 10.6 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +4dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 9.7  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +6dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 19.4 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +6dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 17.7 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +8dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 22.3 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +8dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 20.3 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +8dBm output power setting<br>2440MHz DC/DC disabled                                                     |     | 38.6 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +10dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                    |     | 27.1 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +10dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>   |     | 24.5 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +10dBm output power setting<br>2440MHz DC/DC disabled, system bus off <sup>(1)</sup>                     |     | 46.5 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +12 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 52   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +12 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 52   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +14 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 62   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +14 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 62   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +16 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 75   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +16 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 75   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +18 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 99   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +18 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 101  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 127  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 132  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz DC/DC disabled, system bus off <sup>(1)</sup>                   |     | 136  |     | mA   |

## 7.10 Power Consumption—Radio Modes (R variant) (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$  with DC/DC enabled (unless otherwise noted)

| PARAMETER       |                        | TEST CONDITIONS                                                                                                         | MIN | TYP | MAX | UNIT |
|-----------------|------------------------|-------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz DC/DC disabled, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 143 |     | mA   |

(1) System bus off refers to device idle mode, DMA disabled and flash disabled.

## 7.11 Power Consumption—Radio Modes (P variant)

Measured on the LP-EM-CC2755P10 (P variant) reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$  with DC/DC enabled (unless otherwise noted)

| PARAMETER       |                        | TEST CONDITIONS                                                                                          | MIN | TYP  | MAX | UNIT |
|-----------------|------------------------|----------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| $I_{\text{RX}}$ | Radio receive current  | 2440MHz, 1Mbps, system bus off <sup>(1)</sup>                                                            |     | 6.8  |     | mA   |
| $I_{\text{RX}}$ | Radio receive current  | 2440MHz, 1Mbps, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>                           |     | 6.2  |     | mA   |
| $I_{\text{RX}}$ | Radio receive current  | 2440MHz, 1Mbps, DC/DC disabled, system bus off <sup>(1)</sup>                                            |     | 11.7 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | -8dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 6.2  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | -8dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 5.8  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | 0dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                      |     | 9.3  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | 0dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>     |     | 8.6  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | 0dBm output power setting<br>2440MHz DC/DC disabled, system bus off <sup>(1)</sup>                       |     | 15.8 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +4dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 10.8 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +4dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 10.0 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +6dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 21.9 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +6dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 20.0 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +8dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                     |     | 25.8 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +8dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>    |     | 23.5 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +8dBm output power setting<br>2440MHz DC/DC disabled                                                     |     | 44.4 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +10dBm output power setting<br>2440MHz, system bus off <sup>(1)</sup>                                    |     | 30.7 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +10dBm output power setting<br>2440MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>   |     | 28.2 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +10dBm output power setting<br>2440MHz DC/DC disabled, system bus off <sup>(1)</sup>                     |     | 53   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +12 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 52   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +12 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 52   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +14 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                  |     | 62   |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +14 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 62   |     | mA   |

Measured on the LP-EM-CC2755P10 (P variant) reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$  with DC/DC enabled (unless otherwise noted)

| PARAMETER       |                        | TEST CONDITIONS                                                                                                         | MIN | TYP | MAX | UNIT |
|-----------------|------------------------|-------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $I_{\text{TX}}$ | Radio transmit current | +16 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                                 |     | 75  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +16 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>                |     | 75  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +18 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                                 |     | 99  |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +18 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>                |     | 101 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz, system bus off <sup>(1)</sup>                                                 |     | 127 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup>                |     | 132 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz DC/DC disabled, system bus off <sup>(1)</sup>                                  |     | 136 |     | mA   |
| $I_{\text{TX}}$ | Radio transmit current | +20 dBm output power setting<br>2440 MHz DC/DC disabled, $V_{\text{DDS}} = 3.3\text{V}$ , system bus off <sup>(1)</sup> |     | 143 |     | mA   |

(1) System bus off refers to device idle mode, DMA disabled and flash disabled.

## 7.12 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and  $V_{\text{DDS}} = 3.0\text{V}$  (unless otherwise noted)

| PARAMETER                                                                     | TEST CONDITIONS                             | MIN  | TYP | MAX | UNIT             |
|-------------------------------------------------------------------------------|---------------------------------------------|------|-----|-----|------------------|
| Flash sector size                                                             |                                             |      | 2   |     | KB               |
| Supported flash erase cycles before failure, full bank <sup>(1) (2)</sup>     |                                             | 30   |     |     | k Cycles         |
| Supported flash erase cycles before failure, single sector <sup>(3)</sup>     |                                             | 60   |     |     | k Cycles         |
| Maximum number of write operations per row before sector erase <sup>(4)</sup> |                                             |      |     | 83  | Write Operations |
| Flash retention                                                               | 105°C                                       | 11.4 |     |     | Years            |
| Flash retention                                                               | 125°C                                       | 10   |     |     | Years            |
| Flash sector erase current <sup>(5)</sup>                                     |                                             |      | 5.8 |     | mA               |
| Flash sector erase time <sup>(6)</sup>                                        | 0 erase cycles                              |      | 2.2 |     | ms               |
| Flash write current <sup>(5)</sup>                                            | full sector at a time                       |      | 6.6 |     | mA               |
| Flash write time <sup>(6)</sup>                                               | full sector (2KB) at a time, 0 erase cycles |      | 8   |     | ms               |

- (1) A full bank erase is counted as a single erase cycle on each sector.
- (2) Aborting flash during erase or program modes is not a safe operation.
- (3) Up to 16 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles.
- (4) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
- (5) Current consumption when device is performing erase or write operations to a flash sector. DC/DC enabled ( $i_{\text{peak}} = 0$ ). All peripherals are disabled.
- (6) This number is dependent on flash aging and increases over time and erase cycles.

## 7.13 Thermal Resistance Characteristics

| THERMAL METRIC        | THERMAL METRIC                            | PACKAGE    | UNIT                |
|-----------------------|-------------------------------------------|------------|---------------------|
|                       |                                           | RHA (VQFN) |                     |
|                       |                                           | 40 PINS    |                     |
| R <sub>θJA</sub>      | Junction-to-ambient thermal resistance    | 26.4       | °C/W <sup>(1)</sup> |
| R <sub>θJC(top)</sub> | Junction-to-case (top) thermal resistance | 14.7       | °C/W <sup>(1)</sup> |

### 7.13 Thermal Resistance Characteristics (continued)

| THERMAL METRIC       | THERMAL METRIC                               | PACKAGE    | UNIT                |
|----------------------|----------------------------------------------|------------|---------------------|
|                      |                                              | RHA (VQFN) |                     |
|                      |                                              | 40 PINS    |                     |
| $R_{\theta JB}$      | Junction-to-board thermal resistance         | 8.1        | °C/W <sup>(1)</sup> |
| $\Psi_{JT}$          | Junction-to-top characterization parameter   | 0.2        | °C/W <sup>(1)</sup> |
| $\Psi_{JB}$          | Junction-to-board characterization parameter | 8.1        | °C/W <sup>(1)</sup> |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.6        | °C/W <sup>(1)</sup> |

(1) °C/W = degrees Celsius per watt.

### 7.14 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER       | MIN  | TYP | MAX  | UNIT |
|-----------------|------|-----|------|------|
| Frequency bands | 2360 |     | 2500 | MHz  |

## 7.15 Bluetooth Low Energy—Receive (RX)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{DDS} = 3.0\text{V}$ ,  $f_{RF} = 2440\text{MHz}$  with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER                                            | TEST CONDITIONS                                                                                                                                                     | MIN | TYP                      | MAX | UNIT |
|------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------------|-----|------|
| <b>125kbps (LE Coded)</b>                            |                                                                                                                                                                     |     |                          |     |      |
| Receiver sensitivity                                 | BER = $10^{-3}$                                                                                                                                                     |     | -103.5                   |     | dBm  |
| Receiver saturation                                  | BER = $10^{-3}$                                                                                                                                                     |     | 10                       |     | dBm  |
| Frequency error tolerance                            | Difference between the incoming carrier frequency and the internally generated carrier frequency                                                                    |     | $> (-250 / 250)^{(1)}$   |     | kHz  |
| Data rate error tolerance                            | Difference between incoming data rate and the internally generated data rate (37-byte packets)                                                                      |     | $> (-90 / 90)^{(1)}$     |     | ppm  |
| Data rate error tolerance                            | Difference between incoming data rate and the internally generated data rate (255-byte packets)                                                                     |     | $> (-90 / 90)^{(1)}$     |     | ppm  |
| Co-channel rejection <sup>(2)</sup>                  | Wanted signal at -79dBm, modulated interferer in channel, BER = $10^{-3}$                                                                                           |     | -1.5                     |     | dB   |
| Selectivity, $\pm 1\text{MHz}^{(2)}$                 | Wanted signal at -79dBm, modulated interferer at $\pm 1\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 8.5 / 4.5 <sup>(3)</sup> |     | dB   |
| Selectivity, $\pm 2\text{MHz}^{(2)}$                 | Wanted signal at -79dBm, modulated interferer at $\pm 2\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 42 / 31 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 3\text{MHz}^{(2)}$                 | Wanted signal at -79dBm, modulated interferer at $\pm 3\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 42 / 40 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 4\text{MHz}^{(2)}$                 | Wanted signal at -79dBm, modulated interferer at $\pm 4\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 44 / 42 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 6\text{MHz}^{(2)}$                 | Wanted signal at -79dBm, modulated interferer at $\geq \pm 6\text{MHz}$ , BER = $10^{-3}$                                                                           |     | 49 / 43 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 7\text{MHz}$                       | Wanted signal at -79dBm, modulated interferer at $\geq \pm 7\text{MHz}$ , BER = $10^{-3}$                                                                           |     | 51 / 45 <sup>(3)</sup>   |     | dB   |
| Selectivity, Image frequency <sup>(2)</sup>          | Wanted signal at -79dBm, modulated interferer at image frequency, BER = $10^{-3}$                                                                                   |     | 31                       |     | dB   |
| Selectivity, Image frequency $\pm 1\text{MHz}^{(2)}$ | Note that Image frequency + 1MHz is the co-channel - 1MHz. Wanted signal at -79dBm, modulated interferer at $\pm 1\text{MHz}$ from image frequency, BER = $10^{-3}$ |     | 4.5 / 40 <sup>(3)</sup>  |     | dB   |
| <b>500kbps (LE Coded)</b>                            |                                                                                                                                                                     |     |                          |     |      |
| Receiver sensitivity                                 | BER = $10^{-3}$                                                                                                                                                     |     | -99                      |     | dBm  |
| Receiver saturation                                  | BER = $10^{-3}$                                                                                                                                                     |     | 10                       |     | dBm  |
| Frequency error tolerance                            | Difference between the incoming carrier frequency and the internally generated carrier frequency                                                                    |     | $> (-250 / 250)^{(1)}$   |     | kHz  |
| Data rate error tolerance                            | Difference between incoming data rate and the internally generated data rate (37-byte packets)                                                                      |     | $> (-90 / 90)^{(1)}$     |     | ppm  |
| Data rate error tolerance                            | Difference between incoming data rate and the internally generated data rate (255-byte packets)                                                                     |     | $> (-90 / 90)^{(1)}$     |     | ppm  |
| Co-channel rejection <sup>(2)</sup>                  | Wanted signal at -72dBm, modulated interferer in channel, BER = $10^{-3}$                                                                                           |     | -3.5                     |     | dB   |
| Selectivity, $\pm 1\text{MHz}^{(2)}$                 | Wanted signal at -72dBm, modulated interferer at $\pm 1\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 8 / 4.5 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 2\text{MHz}^{(2)}$                 | Wanted signal at -72dBm, modulated interferer at $\pm 2\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 40 / 28 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 3\text{MHz}^{(2)}$                 | Wanted signal at -72dBm, modulated interferer at $\pm 3\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 40 / 38 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 4\text{MHz}^{(2)}$                 | Wanted signal at -72dBm, modulated interferer at $\pm 4\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 42 / 40 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 6\text{MHz}^{(2)}$                 | Wanted signal at -72dBm, modulated interferer at $\geq \pm 6\text{MHz}$ , BER = $10^{-3}$                                                                           |     | 46 / 41 <sup>(3)</sup>   |     | dB   |
| Selectivity, $\pm 7\text{MHz}$                       | Wanted signal at -72dBm, modulated interferer at $\geq \pm 7\text{MHz}$ , BER = $10^{-3}$                                                                           |     | 48 / 42 <sup>(3)</sup>   |     | dB   |
| Selectivity, Image frequency <sup>(2)</sup>          | Wanted signal at -72dBm, modulated interferer at image frequency, BER = $10^{-3}$                                                                                   |     | 28                       |     | dB   |

## 7.15 Bluetooth Low Energy—Receive (RX) (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ ,  $f_{\text{RF}} = 2440\text{MHz}$  with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER                                             | TEST CONDITIONS                                                                                                                                                     | MIN | TYP                           | MAX | UNIT |
|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------------------|-----|------|
| Selectivity, Image frequency $\pm 1\text{MHz}^{(2)}$  | Note that Image frequency + 1MHz is the co-channel – 1MHz. Wanted signal at –72dBm, modulated interferer at $\pm 1\text{MHz}$ from image frequency, BER = $10^{-3}$ |     | 4.5 / 38 <sup>(3)</sup>       |     | dB   |
| <b>1Mbps (LE 1M)</b>                                  |                                                                                                                                                                     |     |                               |     |      |
| Receiver sensitivity                                  | BER = $10^{-3}$                                                                                                                                                     |     | –97                           |     | dBm  |
| Receiver saturation                                   | BER = $10^{-3}$                                                                                                                                                     |     | 10                            |     | dBm  |
| Frequency error tolerance                             | Difference between the incoming carrier frequency and the internally generated carrier frequency                                                                    |     | > (–250 / 250) <sup>(1)</sup> |     | kHz  |
| Data rate error tolerance                             | Difference between incoming data rate and the internally generated data rate,                                                                                       |     | > (–90 / 90) <sup>(1)</sup>   |     | ppm  |
| Co-channel rejection <sup>(2)</sup>                   | Wanted signal at –67dBm, modulated interferer in channel, BER = $10^{-3}$                                                                                           |     | –5.5                          |     | dB   |
| Selectivity, $\pm 1\text{MHz}^{(2)}$                  | Wanted signal at –67dBm, modulated interferer at $\pm 1\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 7.8 / 5.6 <sup>(3)</sup>      |     | dB   |
| Selectivity, $\pm 2\text{MHz}^{(2)}$                  | Wanted signal at –67dBm, modulated interferer at $\pm 2\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 39 / 26 <sup>(3)</sup>        |     | dB   |
| Selectivity, $\pm 3\text{MHz}^{(2)}$                  | Wanted signal at –67dBm, modulated interferer at $\pm 3\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 36 / 36 <sup>(3)</sup>        |     | dB   |
| Selectivity, $\pm 4\text{MHz}^{(2)}$                  | Wanted signal at –67dBm, modulated interferer at $\pm 4\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 46 / 34 <sup>(3)</sup>        |     | dB   |
| Selectivity, $\pm 5\text{MHz}$ or more <sup>(2)</sup> | Wanted signal at –67dBm, modulated interferer at $\geq \pm 5\text{MHz}$ , BER = $10^{-3}$                                                                           |     | 56                            |     | dB   |
| Selectivity, image frequency <sup>(2)</sup>           | Wanted signal at –67dBm, modulated interferer at image frequency, BER = $10^{-3}$                                                                                   |     | 26                            |     | dB   |
| Selectivity, image frequency $\pm 1\text{MHz}^{(2)}$  | Note that Image frequency + 1MHz is the co-channel – 1MHz. Wanted signal at –67dBm, modulated interferer at $\pm 1\text{MHz}$ from image frequency, BER = $10^{-3}$ |     | 5.6 / 36 <sup>(3)</sup>       |     | dB   |
| Out-of-band blocking <sup>(4)</sup>                   | 30 MHz to 2000 MHz                                                                                                                                                  |     | –10                           |     | dBm  |
| Out-of-band blocking                                  | 2003MHz to 2399MHz                                                                                                                                                  |     | –10                           |     | dBm  |
| Out-of-band blocking                                  | 2484MHz to 2997MHz                                                                                                                                                  |     | –10                           |     | dBm  |
| Out-of-band blocking                                  | 3000MHz to 12.75GHz (excluding VCO frequency)                                                                                                                       |     | –2                            |     | dBm  |
| Intermodulation                                       | Wanted signal at 2402MHz, –64dBm. Two interferers at 2405MHz and 2408MHz respectively, at the given power level                                                     |     | –38                           |     | dBm  |
| Spurious emissions, 30MHz to 1000MHz <sup>(5)</sup>   | Measurement in a 50 $\Omega$ single-ended load.                                                                                                                     |     | < –59                         |     | dBm  |
| Spurious emissions, 1GHz to 12.75GHz <sup>(5)</sup>   | Measurement in a 50 $\Omega$ single-ended load.                                                                                                                     |     | < –47                         |     | dBm  |
| RSSI dynamic range <sup>(6)</sup>                     |                                                                                                                                                                     |     | 67                            |     | dB   |
| RSSI accuracy                                         |                                                                                                                                                                     |     | $\pm 4$                       |     | dB   |
| RSSI resolution                                       |                                                                                                                                                                     |     | 1                             |     | dB   |
| <b>2Mbps (LE 2M)</b>                                  |                                                                                                                                                                     |     |                               |     |      |
| Receiver sensitivity                                  | Measured at SMA connector, BER = $10^{-3}$                                                                                                                          |     | –93                           |     | dBm  |
| Receiver saturation                                   | Measured at SMA connector, BER = $10^{-3}$                                                                                                                          |     | 10                            |     | dBm  |
| Frequency error tolerance                             | Difference between the incoming carrier frequency and the internally generated carrier frequency                                                                    |     | > (–250 / 250) <sup>(1)</sup> |     | kHz  |
| Data rate error tolerance                             | Difference between incoming data rate and the internally generated data rate (255-byte packets)                                                                     |     | > (–90 / 90) <sup>(1)</sup>   |     | ppm  |
| Co-channel rejection <sup>(2)</sup>                   | Wanted signal at –67dBm, modulated interferer in channel, BER = $10^{-3}$                                                                                           |     | –7                            |     | dB   |
| Selectivity, $\pm 2\text{MHz}^{(2)}$                  | Wanted signal at –67dBm, modulated interferer at $\pm 2\text{MHz}$ , Image frequency is at –2MHz, BER = $10^{-3}$                                                   |     | 9.5 / 6 <sup>(3)</sup>        |     | dB   |
| Selectivity, $\pm 4\text{MHz}^{(2)}$                  | Wanted signal at –67dBm, modulated interferer at $\pm 4\text{MHz}$ , BER = $10^{-3}$                                                                                |     | 37 / 29 <sup>(3)</sup>        |     | dB   |

## 7.15 Bluetooth Low Energy—Receive (RX) (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ ,  $f_{\text{RF}} = 2440\text{MHz}$  with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER                                                     | TEST CONDITIONS                                                                                                                                                               | MIN | TYP                      | MAX | UNIT |
|---------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|--------------------------|-----|------|
| Selectivity, $\pm 6\text{MHz}$ <sup>(2)</sup>                 | Wanted signal at $-67\text{dBm}$ , modulated interferer at $\pm 6\text{MHz}$ , $\text{BER} = 10^{-3}$                                                                         |     | 40 / 36 <sup>(3)</sup>   |     | dB   |
| Selectivity, image frequency <sup>(2)</sup>                   | Wanted signal at $-67\text{dBm}$ , modulated interferer at image frequency, $\text{BER} = 10^{-3}$                                                                            |     | 6                        |     | dB   |
| Selectivity, image frequency $\pm 2\text{MHz}$ <sup>(2)</sup> | Note that Image frequency + 2MHz is the Co-channel. Wanted signal at $-67\text{dBm}$ , modulated interferer at $\pm 2\text{MHz}$ from image frequency, $\text{BER} = 10^{-3}$ |     | $-7 / 29$ <sup>(3)</sup> |     | dB   |
| Out-of-band blocking <sup>(4)</sup>                           | 30MHz to 2000MHz                                                                                                                                                              |     | $-10$                    |     | dBm  |
| Out-of-band blocking                                          | 2003MHz to 2399MHz                                                                                                                                                            |     | $-10$                    |     | dBm  |
| Out-of-band blocking                                          | 2484MHz to 2997MHz                                                                                                                                                            |     | $-10$                    |     | dBm  |
| Out-of-band blocking                                          | 3000MHz to 12.75GHz (excluding VCO frequency)                                                                                                                                 |     | $-2$                     |     | dBm  |
| Intermodulation                                               | Wanted signal at 2402MHz, $-64\text{dBm}$ . Two interferers at 2408 and 2414MHz respectively, at the given power level                                                        |     | $-38$                    |     | dBm  |

(1) Actual performance exceeding Bluetooth specification listed here

(2) Numbers given as I/C dB

(3)  $X / Y$ , where X is  $+N$  MHz and Y is  $-N$  MHz

(4) Excluding one exception at  $F_{\text{wanted}} / 2$ , per Bluetooth Specification

(5) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)

(6) The device will saturate at  $-30\text{dBm}$ .

## 7.16 Bluetooth Low Energy—Transmit (TX)

Measured on the LP-EM-CC2745R10-Q1 (R variant) or LP-EM-CC2755P10 (P variant) reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ ,  $f_{\text{RF}} = 2440\text{MHz}$  with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| VARIANT                   | PARAMETER                       | TEST CONDITIONS                                                      | MIN | TYP | MAX | UNIT |
|---------------------------|---------------------------------|----------------------------------------------------------------------|-----|-----|-----|------|
| <b>General Parameters</b> |                                 |                                                                      |     |     |     |      |
| R variant                 | Max output power                | Delivered to a single-ended $50\Omega$ load through integrated balun |     | 10  |     | dBm  |
|                           | Output power programmable range | Delivered to a single-ended $50\Omega$ load through integrated balun |     | 30  |     | dB   |
| P variant                 | Max output power                | Delivered to a single-ended $50\Omega$ load through integrated balun |     | 20  |     | dBm  |
|                           | Output power programmable range | Delivered to a single-ended $50\Omega$ load through integrated balun |     | 40  |     | dB   |

## 7.17 Bluetooth Channel Sounding

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.3\text{V}$ ,  $f_{\text{RF}} = 2440\text{MHz}$ , Tx output power =  $+10\text{dBm}$  with DC/DC enabled (unless otherwise noted)

| PARAMETER                 | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT          |
|---------------------------|------------------------------------------------|-----|-----|-----|---------------|
| <b>General Parameters</b> |                                                |     |     |     |               |
|                           | Supported PHY data rate                        | 1   |     | 2   | Mbps          |
| T_IP1                     | Range of Interlude Time between Packets        | 40  |     | 145 | $\mu\text{s}$ |
| T_IP2                     | Range of Interlude Time between CS Tones       | 40  |     | 145 | $\mu\text{s}$ |
| T_FCS                     | Range of Time for Frequency Change Spacing     | 100 |     | 150 | $\mu\text{s}$ |
| T_PM                      | Range of Time for Phase Measurement            | 10  |     | 40  | $\mu\text{s}$ |
| T_SW                      | Range of Antenna switch time                   | 0   |     | 10  | $\mu\text{s}$ |
| T_GD                      | Guard Time between modulated bits and CS Tones |     | 10  |     | $\mu\text{s}$ |
| T_FM                      | Time for Frequency Measurement                 |     | 80  |     | $\mu\text{s}$ |

## 7.17 Bluetooth Channel Sounding (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.3\text{V}$ ,  $f_{\text{RF}} = 2440\text{MHz}$ , Tx output power = +10dBm with DC/DC enabled (unless otherwise noted)

| PARAMETER |                         | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|-----------------|-----|-----|-----|------|
| N_AP      | Number of Antenna Paths |                 | 1   |     | 4   |      |

## 7.18 2.4GHz RX/TX CW

Measured on the LP-EM-CC2745R10-Q1 (R variant) or LP-EM-CC2755R10 (P variant) reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ ,  $f_{\text{RF}} = 2440\text{MHz}$  with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| VARIANT                                 | PARAMETER                                     | TEST CONDITIONS                                      | MIN             | TYP | MAX   | UNIT |
|-----------------------------------------|-----------------------------------------------|------------------------------------------------------|-----------------|-----|-------|------|
| <b>Spurious emissions and harmonics</b> |                                               |                                                      |                 |     |       |      |
| R Variant,<br>P Variant                 | Spurious emissions <sup>(1) (3)</sup>         | f < 1GHz, outside restricted bands                   | +10dBm setting  |     | < -36 | dBm  |
|                                         |                                               | f < 1GHz, restricted bands ETSI, MIIT                |                 |     | < -54 | dBm  |
|                                         |                                               | f < 1GHz, restricted bands FCC                       |                 |     | < -55 | dBm  |
|                                         |                                               | f > 1GHz, including harmonics (ETSI)                 |                 |     | < -30 | dBm  |
|                                         |                                               | f > 1GHz (2300 - 2390 MHz, 2483.5 - 2500 MHz) (MIIT) |                 |     | < -40 | dBm  |
|                                         |                                               | f > 1GHz (2390 - 2400 MHz) (MIIT)                    |                 |     | < -30 | dBm  |
|                                         | Harmonics <sup>(1)</sup>                      | Second harmonic                                      |                 |     | < -42 | dBm  |
|                                         |                                               | Third harmonic                                       |                 |     | < -42 | dBm  |
| P Variant                               | Spurious emissions <sup>(1) (2) (3) (4)</sup> | f < 1 GHz, outside restricted bands                  | +20 dBm setting |     | < -36 | dBm  |
|                                         |                                               | f < 1GHz, restricted bands ETSI, MIIT                |                 |     | < -54 | dBm  |
|                                         |                                               | f < 1 GHz, restricted bands FCC                      |                 |     | < -55 | dBm  |
|                                         |                                               | f > 1GHz, including harmonics (ETSI)                 |                 |     | < -30 | dBm  |
|                                         |                                               | f > 1GHz (2300 - 2390 MHz, 2483.5 - 2500 MHz) (MIIT) |                 |     | < -40 | dBm  |
|                                         |                                               | f > 1GHz (2390 - 2400 MHz) (MIIT)                    |                 |     | < -30 | dBm  |
|                                         | Harmonics <sup>(1)</sup>                      | Second harmonic                                      |                 |     | < -42 | dBm  |
|                                         |                                               | Third harmonic                                       |                 |     | < -42 | dBm  |

- (1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), MIIT (China), and ARIB STD-T66 (Japan).
- (2) To enable margins for passing FCC band edge requirements at 2483.5MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper BLE channel(s).
- (3) To enable margin for passing MIIT band edge requirements at 2400 MHz and 2483.5 MHz, a lower than maximum output-power setting may be used when operating at the lower and upper BLE channels
- (4) To enable margin for passing ETSI band edge requirements at 2400 MHz, a lower than maximum output-power setting may be used when operating at the lower BLE channel

## 7.19 Timing and Switching Characteristics

### 7.19.1 Reset Timing

| PARAMETER         | MIN | TYP | MAX | UNIT |
|-------------------|-----|-----|-----|------|
| RSTN low duration | 1   |     |     | μs   |

### 7.19.2 Wakeup Timing

Measured over operating free-air temperature with  $V_{DD5} = 3.0V$  (unless otherwise noted). The times listed here do not include any software overhead (unless otherwise noted).

| PARAMETER                                    |                                                                                                                   | TEST CONDITIONS                                                                  | MIN | TYP     | MAX | UNIT |
|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----|---------|-----|------|
| MCU, Reset/Shutdown to Active <sup>(1)</sup> |                                                                                                                   | GLDO default charge current setting, VDDR capacitor fully charged <sup>(2)</sup> |     | 350–450 |     | μs   |
| MCU, Standby to Active                       | MCU, Standby to Active <sup>(3)</sup> (ready to execute code from flash), VGM disabled coming out of standby mode | DC/DC enabled, default recharge current configuration                            |     | 43      |     | μs   |
| MCU, Standby to Active                       | MCU, Standby to Active <sup>(3)</sup> (ready to execute code from flash), VGM disabled coming out of standby mode | GLDO enabled, default recharge current configuration                             |     | 43      |     | μs   |
| MCU, Standby to Active                       | MCU, Standby to Active (ready to execute code from flash), VGM enabled coming out of standby mode                 | DC/DC enabled, default recharge current configuration                            |     | 80      |     | μs   |
| MCU, Standby to Active                       | MCU, Standby to Active (ready to execute code from flash), VGM enabled coming out of standby mode                 | GLDO enabled, default recharge current configuration                             |     | 80      |     | μs   |
| MCU, Idle to Active                          |                                                                                                                   | Flash enabled in idle mode                                                       |     | 3       |     | μs   |
|                                              |                                                                                                                   | Flash disabled in idle mode                                                      |     | 15      |     | μs   |

- (1) Wakeup time includes system ROM bootcode execution time (excluding any system ROM secure boot operations). The wakeup time is dependent on the remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.
- (2) This is the best case Reset/Shutdown mode to Active mode time including system ROM bootcode operation (excluding any system ROM secure boot operations) for the specified GLDO charge current setting considering the VDDR capacitor is fully charged and is not discharged during the reset and shutdown events; that is, when the device is in reset / shutdown modes for only a very short period of time
- (3) Dependent on VDDR capacitor voltage level

## 7.19.3 Clock Specifications

### 7.19.3.1 48MHz Crystal Oscillator (HFXT)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.

|                              | PARAMETER                                                                                                        | MIN | TYP              | MAX | UNIT          |
|------------------------------|------------------------------------------------------------------------------------------------------------------|-----|------------------|-----|---------------|
|                              | Crystal frequency                                                                                                |     | 48               |     | MHz           |
| $g_m$                        | Oscillator Transconductance <sup>(1)</sup>                                                                       |     | 16.5             |     | mA/V          |
| ESR                          | Equivalent series resistance <sup>(2) (3)</sup><br>$C_L = 9\text{ pF}$ , $C_0 \leq 1\text{ pF}$                  |     |                  | 45  | $\Omega$      |
|                              | Equivalent series resistance <sup>(2) (3)</sup><br>$C_L = 8\text{ pF}$ , $C_0 \leq 1\text{ pF}$                  |     |                  | 55  | $\Omega$      |
|                              | Equivalent series resistance <sup>(2) (3)</sup><br>$C_L = 7\text{ pF}$ , $C_0 \leq 1\text{ pF}$                  |     |                  | 70  | $\Omega$      |
|                              | Equivalent series resistance <sup>(2) (3)</sup><br>$5\text{ pF} < C_L \leq 6\text{ pF}$ , $C_0 \leq 1\text{ pF}$ |     |                  | 90  | $\Omega$      |
| $C_L$                        | Crystal load capacitance <sup>(4)</sup>                                                                          | 5   | 7 <sup>(5)</sup> | 9   | pF            |
| Start-up time <sup>(6)</sup> | Until clock is qualified.                                                                                        |     | 130              |     | $\mu\text{s}$ |

- (1) Negative resistance is the oscillator's ability to counteract the losses in the crystal, thereby sustaining oscillations at the crystal's resonant frequency.  
Negative resistance  $R_N = -g_m / ((2\pi f)^2 * (2 * (C_L + C_0))^2)$ .  $R_N$  corresponds to the total series resistance (ESR + additional series R) that prevents the oscillations from starting at the XTAL pins. XTAL startup margin =  $R_N / \text{ESR}_{\text{max}}$ . For more information, see App Note [SWRA495](#).
- (2) The max ESR value will be reduced if the crystal has a shunt capacitance of  $C_0 > 1\text{ pF}$
- (3) XTAL startup margin  $\geq 10$
- (4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations.
- (5) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
- (6) Start-up time using the TI-provided power driver. Start-up time may increase if the driver is not used.

### 7.19.3.2 96MHz RC Oscillator (HFOSC)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.

|                                 | MIN                                                     | TYP | MAX | UNIT      |
|---------------------------------|---------------------------------------------------------|-----|-----|-----------|
| Center Frequency                |                                                         | 96  |     | MHz       |
| Uncalibrated frequency accuracy | Frequency accuracy until HFXT tracking loop is enabled. |     |     | $\pm 3\%$ |

### 7.19.3.3 80/90/98MHz RC Oscillator (AFOSC)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.

|                  | MIN | TYP                     | MAX | UNIT |
|------------------|-----|-------------------------|-----|------|
| Center Frequency |     | 80<br>90.3168<br>98.304 |     | MHz  |

### 7.19.3.4 32kHz Crystal Oscillator (LFXT)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.

|                                    | MIN | TYP    | MAX | UNIT       |
|------------------------------------|-----|--------|-----|------------|
| Crystal frequency                  |     | 32.768 |     | kHz        |
| Supported crystal load capacitance | 6   |        | 12  | pF         |
| ESR (Equivalent Series Resistance) |     | 30     | 100 | k $\Omega$ |

### 7.19.3.5 32kHz RC Oscillator (LFOSC)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.

|                      | MIN | TYP                   | MAX | UNIT |
|----------------------|-----|-----------------------|-----|------|
| Calibrated frequency |     | 32.768 <sup>(1)</sup> |     | kHz  |

### 7.19.3.5 32kHz RC Oscillator (LFOSC) (continued)

Measured on the LP-EM-CC2745R10-Q1 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.

|                |                                                      | MIN | TYP                 | MAX | UNIT |
|----------------|------------------------------------------------------|-----|---------------------|-----|------|
| Clock accuracy | Sleep clock accuracy when using LFOSC <sup>(2)</sup> |     | ±500 <sup>(3)</sup> |     | ppm  |

- (1) When using LFOSC as a source for the low-frequency system clock (LFCLK), the accuracy of the LFCLK-derived Real Time Clock (RTC) can be improved by measuring LFOSC relative to HFXT and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
- (2) Suitable for crystal-less operation of both Bluetooth LE peripheral and central roles with periodic RTC calibration using device HW and SW that is configured through the TI SysConfig tool. For further guidance, please reach out to Texas Instruments for support.
- (3) The actual value is lower than ±500ppm prescribed by Bluetooth LE sleep clock accuracy specification.

## 7.20 Peripheral Characteristics

### 7.20.1 UART

#### 7.20.1.1 UART Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT  |
|-----------|-----|-----|-----|-------|
| UART rate |     |     | 3   | MBaud |

### 7.20.2 SPI

#### 7.20.2.1 SPI Characteristics

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

| PARAMETERS                               |                     | TEST CONDITIONS                                                                               | MIN | TYP | MAX | UNIT |
|------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------|-----|-----|-----|------|
| f <sub>SCLK</sub><br>1/t <sub>sclk</sub> | SPI clock frequency | Contoller and Peripheral Mode <sup>(1)</sup><br>2.7V ≤ VDD <sub>S</sub> < 3.8V <sup>(2)</sup> |     |     | 12  | MHz  |
|                                          |                     | Controller and Peripheral Mode <sup>(1)</sup><br>VDD <sub>S</sub> < 2.7V <sup>(2)</sup>       |     |     | 8   |      |
| DC <sub>SCLK</sub>                       | SCLK Duty Cycle     |                                                                                               | 45% | 50% | 55% |      |

(1) Assume interfacing with ideal SPI controller and SPI peripheral devices

(2) If VDDIO supply is used to power the specific pins whose DIOs are configured for SPI operation, then, the supply range applies to VDDIO in this case.

#### 7.20.2.2 SPI Controller Mode

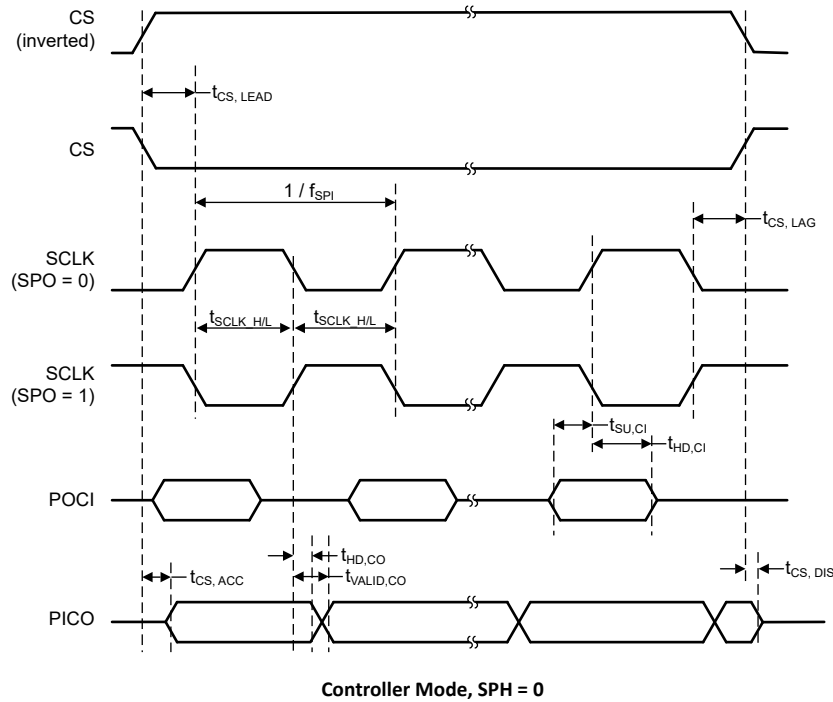
Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

| PARAMETERS            |                                                     | TEST CONDITIONS                                | MIN                       | TYP                  | MAX                       | UNIT |
|-----------------------|-----------------------------------------------------|------------------------------------------------|---------------------------|----------------------|---------------------------|------|
| t <sub>SCLK_H/L</sub> | SCLK high or low time                               |                                                | (t <sub>SPI</sub> /2) - 1 | t <sub>SPI</sub> / 2 | (t <sub>SPI</sub> /2) + 1 | ns   |
| t <sub>CS.LEAD</sub>  | CS lead-time, CS active to clock                    |                                                | 1                         |                      |                           | SCLK |
| t <sub>CS.LAG</sub>   | CS lag time, last clock to CS inactive              |                                                | 1                         |                      |                           | SCLK |
| t <sub>CS.ACC</sub>   | CS access time, CS active to PICO data out          |                                                |                           |                      | 1                         | SCLK |
| t <sub>CS.DIS</sub>   | CS disable time, CS inactive to PICO high impedance |                                                |                           |                      | 1                         | SCLK |
| t <sub>HD.CI</sub>    | POCI input data hold time                           |                                                | 0                         |                      |                           | ns   |
| t <sub>VALID.CO</sub> | PICO output data valid time <sup>(1)</sup>          | SCLK edge to PICO valid, C <sub>L</sub> = 20pF |                           |                      | 13                        | ns   |
| t <sub>HD.CO</sub>    | PICO output data hold time <sup>(2)</sup>           | C <sub>L</sub> = 20pF                          | 0                         |                      |                           | ns   |

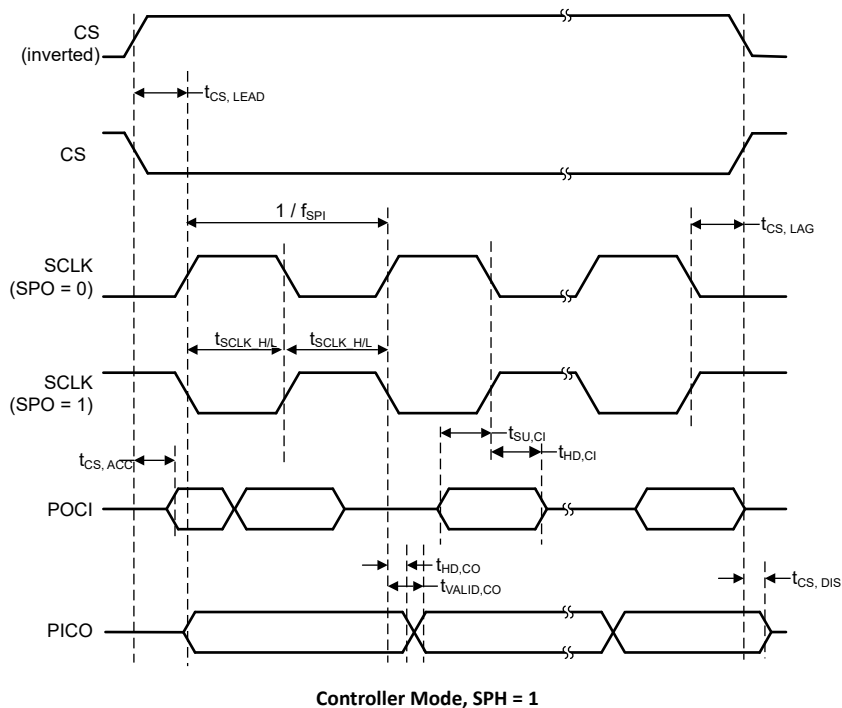
(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge

(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

### 7.20.2.3 SPI Timing Diagrams—Controller Mode



**Figure 7-1. SPI Timing Diagram—Controller Mode, SPH = 0**



**Figure 7-2. SPI Timing Diagram—Controller Mode, SPH = 1**

### 7.20.2.4 SPI Peripheral Mode

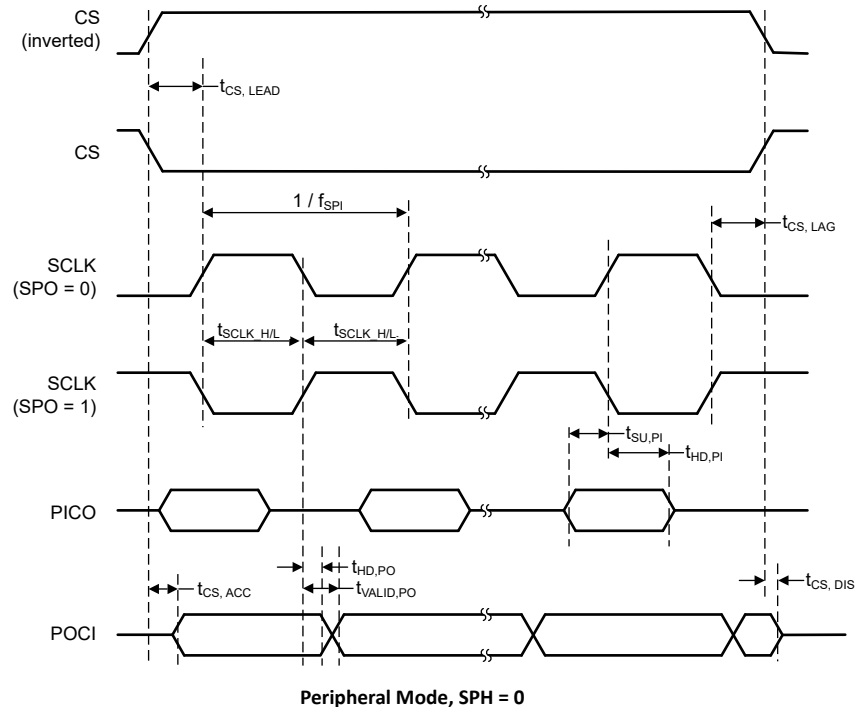
Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

| PARAMETERS     |                                                     | TEST CONDITIONS                              | MIN | TYP | MAX | UNIT |
|----------------|-----------------------------------------------------|----------------------------------------------|-----|-----|-----|------|
| $t_{CS,LEAD}$  | CS lead-time, CS active to clock                    |                                              | 1   |     |     | SCLK |
| $t_{CS,LAG}$   | CS lag time, Last clock to CS inactive              |                                              | 1   |     |     | SCLK |
| $t_{CS,ACC}$   | CS access time, CS active to POCI data out          | VDDS = 3.3V                                  |     |     | 35  | ns   |
| $t_{CS,ACC}$   | CS access time, CS active to POCI data out          | VDDS = 1.8V                                  |     |     | 50  | ns   |
| $t_{CS,DIS}$   | CS disable time, CS inactive to POCI high impedance | VDDS = 3.3V                                  |     |     | 35  | ns   |
| $t_{CS,DIS}$   | CS disable time, CS inactive to POCI high impedance | VDDS = 1.8V                                  |     |     | 50  | ns   |
| $t_{SU,PI}$    | PICO input data setup time                          |                                              | 13  |     |     | ns   |
| $t_{HD,PI}$    | PICO input data hold time                           |                                              | 0   |     |     | ns   |
| $t_{VALID,PO}$ | POCI output data valid time <sup>(1)</sup>          | SCLK edge to MISO valid, $C_L = 20pF$ , 3.3V |     |     | 35  | ns   |
| $t_{VALID,PO}$ | POCI output data valid time <sup>(1)</sup>          | SCLK edge to MISO valid, $C_L = 20pF$ , 1.8V |     |     | 50  | ns   |
| $t_{HD,PO}$    | POCI output data hold time <sup>(2)</sup>           | $C_L = 20pF$                                 | 0   |     |     | ns   |

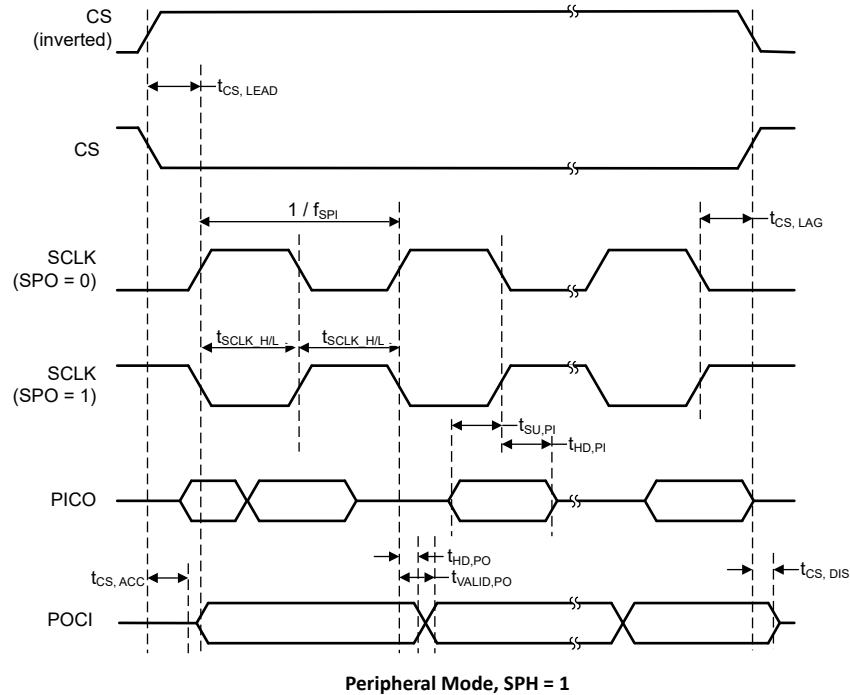
(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge

(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

### 7.20.2.5 SPI Timing Diagrams—Peripheral Mode



**Figure 7-3. SPI Timing Diagram—Peripheral Mode, SPH = 0**



**Figure 7-4. SPI Timing Diagram—Peripheral Mode, SPH = 1**

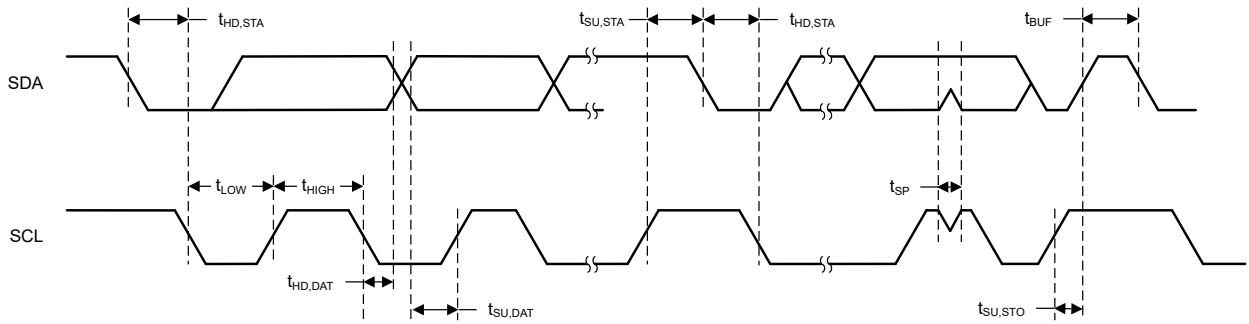
## 7.20.3 I<sup>2</sup>C

### 7.20.3.1 I<sup>2</sup>C Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETERS          |                                                              | TEST CONDITIONS           | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------------------------------------------|---------------------------|-----|-----|-----|------|
| f <sub>SCL</sub>    | SCL clock frequency                                          |                           | 0   |     | 400 | kHz  |
| t <sub>HD,STA</sub> | Hold time (repeated) START                                   | f <sub>SCL</sub> = 100kHz | 4.0 |     |     | μs   |
| t <sub>HD,STA</sub> | Hold time (repeated) START                                   | f <sub>SCL</sub> > 100kHz | 0.6 |     |     | μs   |
| t <sub>SU,STA</sub> | Setup time for a repeated START                              | f <sub>SCL</sub> = 100kHz | 4.7 |     |     | μs   |
| t <sub>SU,STA</sub> | Setup time for a repeated START                              | f <sub>SCL</sub> > 100kHz | 0.6 |     |     | μs   |
| t <sub>HD,DAT</sub> | Data hold time                                               |                           | 0   |     |     | μs   |
| t <sub>SU,DAT</sub> | Data setup time                                              | f <sub>SCL</sub> = 100kHz | 250 |     |     | ns   |
| t <sub>SU,DAT</sub> | Data setup time                                              | f <sub>SCL</sub> > 100kHz | 100 |     |     | ns   |
| t <sub>SU,STO</sub> | Setup time for STOP                                          | f <sub>SCL</sub> = 100kHz | 4.0 |     |     | μs   |
| t <sub>SU,STO</sub> | Setup time for STOP                                          | f <sub>SCL</sub> > 100kHz | 0.6 |     |     | μs   |
| t <sub>BUF</sub>    | Bus free time between STOP and START conditions              | f <sub>SCL</sub> = 100kHz | 4.7 |     |     | μs   |
| t <sub>BUF</sub>    | Bus free time between STOP and START conditions              | f <sub>SCL</sub> > 100kHz | 1.3 |     |     | μs   |
| t <sub>SP</sub>     | Pulse duration of spikes suppressed by input deglitch filter |                           | 50  |     |     | ns   |

### 7.20.3.2 I<sup>2</sup>C Timing Diagram



**Figure 7-5. I<sup>2</sup>C Timing Diagram**

### 7.20.4 I<sup>2</sup>S

#### 7.20.4.1 I<sup>2</sup>S Controller Mode

Over operating free-air temperature range (unless otherwise noted)

| PARAMETERS               |                                                                   | TEST CONDITIONS          | MIN | TYP | MAX   | UNIT |
|--------------------------|-------------------------------------------------------------------|--------------------------|-----|-----|-------|------|
| f <sub>EXTCl</sub>       | External clock input frequency                                    |                          |     |     | 24    | MHz  |
| EXTCl <sub>DC</sub>      | External clock input duty cycle                                   |                          | 40% |     | 60%   |      |
| f <sub>MCLK</sub>        | MCLK clock output frequency                                       |                          |     |     | 24    | MHz  |
| MCLK <sub>DC</sub>       | MCLK clock duty cycle                                             |                          | 46% |     | 52%   |      |
| f <sub>SCLK</sub>        | SCLK clock output frequency                                       | VDD <sub>S</sub> = 1.71V |     |     | 3.27  | MHz  |
| f <sub>SCLK</sub>        | SCLK clock output frequency                                       | VDD <sub>S</sub> = 3.8V  |     |     | 6.145 | MHz  |
| SCLK <sub>DC</sub>       | SCLK clock duty cycle                                             |                          | 46% |     | 54%   |      |
| t <sub>WS,valid</sub>    | WS data output valid time (Falling edge of SCLK to WS data valid) |                          | 42  |     | 49    | ns   |
| t <sub>SDOUT,valid</sub> | SD data output valid time (Falling edge of SCLK to SD data valid) |                          | 37  |     | 62    | ns   |
| t <sub>SDIN,setup</sub>  | SD data input setup time (before rising edge of SCLK)             |                          | 9   |     |       | ns   |
| t <sub>SDIN,hold</sub>   | SD data input hold time (after rising edge of SCLK)               |                          | 5   |     |       | ns   |

#### 7.20.4.2 I<sup>2</sup>S Peripheral Mode

Over operating free-air temperature range (unless otherwise noted)

| PARAMETERS               |                                                                   | TEST CONDITIONS          | MIN | TYP | MAX   | UNIT |
|--------------------------|-------------------------------------------------------------------|--------------------------|-----|-----|-------|------|
| f <sub>SCLK</sub>        | SCLK clock input frequency                                        | VDD <sub>S</sub> = 1.71V |     |     | 3.1   | MHz  |
| f <sub>SCLK</sub>        | SCLK clock input frequency                                        | VDD <sub>S</sub> = 3.8V  |     |     | 6.145 | MHz  |
| SCLK <sub>DC</sub>       | SCLK clock duty cycle                                             | VDD <sub>S</sub> = 1.71V | 35% |     | 65%   |      |
| SCLK <sub>DC</sub>       | SCLK clock duty cycle                                             | VDD <sub>S</sub> = 3.8V  | 40% |     | 60%   |      |
| t <sub>SDOUT,valid</sub> | SD data output valid time (Falling edge of SCLK to SD data valid) |                          | 26  |     | 47    | ns   |
| t <sub>WS,setup</sub>    | WS data input setup time (before rising edge of SCLK)             |                          | 15  |     |       | ns   |
| t <sub>WS,hold</sub>     | WS data input hold time (after rising edge of SCLK)               |                          | 0   |     |       | ns   |
| t <sub>SDIN,setup</sub>  | SD data input setup time (before rising edge of SCLK)             |                          | 9   |     |       | ns   |

### 7.20.4.2 I<sup>2</sup>S Peripheral Mode (continued)

Over operating free-air temperature range (unless otherwise noted)

| PARAMETERS             |                                                     | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|-----------------------------------------------------|-----------------|-----|-----|-----|------|
| t <sub>SDIN,hold</sub> | SD data input hold time (after rising edge of SCLK) |                 | 5   |     |     | ns   |

### 7.20.5 CAN-FD

#### 7.20.5.1 CAN-FD Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETERS                                     |                             | TEST CONDITIONS                       | MIN | TYP | MAX | UNIT |
|------------------------------------------------|-----------------------------|---------------------------------------|-----|-----|-----|------|
| CAN_TX_LOAD                                    | MCAN TX load capacitance    |                                       | 4   |     | 10  | pF   |
| CAN_RX_t <sub>R</sub><br>CAN_RX_t <sub>F</sub> | MCAN RX rise and fall times | See <sup>(1)</sup>                    | 10  |     | 75  | ns   |
| t <sub>p</sub> (CAN_TX)                        | Propagation delay           | Transmit shift register to CAN_TX pin |     |     | 10  | ns   |
| t <sub>p</sub> (CAN_RX)                        | Propagation delay           | CAN_RX pin to receive shift register  |     |     | 5   | ns   |

(1) Min value applicable to faster bitrates (5Mbps). Max value (t<sub>R</sub>/t<sub>F</sub>,max= 75ns) applicable to slower bit rates (unless there is an active slope control to slow it down for slower data rates)

### 7.20.6 GPIO

#### 7.20.6.1 GPIO DC Characteristics

| PARAMETER                                           | TEST CONDITIONS                                                   | MIN                  | TYP  | MAX  | UNIT |
|-----------------------------------------------------|-------------------------------------------------------------------|----------------------|------|------|------|
| <b>T<sub>A</sub> = 25°C, V<sub>DD5</sub> = 1.8V</b> |                                                                   |                      |      |      |      |
| GPIO VOH at 10 mA load                              | high-drive GPIOs only, max drive setting                          | 1.15                 | 1.54 |      | V    |
| GPIO VOL at 10 mA load                              | high-drive GPIOs only, max drive setting                          |                      | 0.25 | 0.5  | V    |
| GPIO VOH at 2 mA load                               | standard drive GPIOs                                              | 1.27                 | 1.60 |      | V    |
| GPIO VOL at 2 mA load                               | standard drive GPIOs                                              |                      | 0.19 | 0.35 | V    |
| GPIO pullup current                                 | Input mode, pullup enabled, V <sub>pad</sub> = 0V                 | 39                   | 66   | 109  | μA   |
| GPIO pulldown current                               | Input mode, pulldown enabled, V <sub>pad</sub> = V <sub>DD5</sub> | 10                   | 21   | 40   | μA   |
| GPIO low-to-high input transition, with hysteresis  | I <sub>H</sub> = 1, transition voltage for input read as 0 → 1    | 0.91                 | 1.11 | 1.27 | V    |
| GPIO high-to-low input transition, with hysteresis  | I <sub>H</sub> = 1, transition voltage for input read as 1 → 0    | 0.59                 | 0.75 | 0.91 | V    |
| GPIO input hysteresis                               | I <sub>H</sub> = 1, difference between 0 → 1 and 1 → 0 points     | 0.26                 | 0.35 | 0.44 | V    |
| <b>T<sub>A</sub> = 25°C, V<sub>DD5</sub> = 3.0V</b> |                                                                   |                      |      |      |      |
| GPIO VOH at 10mA load                               | high-drive GPIOs only, max drive setting (add MMR bits)           | 2.47                 |      |      | V    |
| GPIO VOL at 10mA load                               | high-drive GPIOs only, max drive setting (add MMR bits)           |                      |      | 0.25 | V    |
| GPIO VOH at 2mA load                                | standard drive GPIOs                                              | 2.52                 |      |      | V    |
| GPIO VOL at 2mA load                                | standard drive GPIOs                                              |                      |      | 0.20 | V    |
| <b>T<sub>A</sub> = 25°C, V<sub>DD5</sub> = 3.8V</b> |                                                                   |                      |      |      |      |
| GPIO pullup current                                 | Input mode, pullup enabled, V <sub>pad</sub> = 0V                 | 170                  | 262  | 393  | μA   |
| GPIO pulldown current                               | Input mode, pulldown enabled, V <sub>pad</sub> = V <sub>DD5</sub> | 60                   | 110  | 172  | μA   |
| GPIO low-to-high input transition, with hysteresis  | I <sub>H</sub> = 1, transition voltage for input read as 0 → 1    | 1.76                 | 1.98 | 2.27 | V    |
| GPIO high-to-low input transition, with hysteresis  | I <sub>H</sub> = 1, transition voltage for input read as 1 → 0    | 1.26                 | 1.52 | 1.79 | V    |
| GPIO input hysteresis                               | I <sub>H</sub> = 1, difference between 0 → 1 and 1 → 0 points     | 0.40                 | 0.47 | 0.54 | V    |
| <b>T<sub>A</sub> = 25°C</b>                         |                                                                   |                      |      |      |      |
| VIH                                                 | Lowest GPIO input voltage reliably interpreted as a High          | 0.8×V <sub>DD5</sub> |      |      | V    |

### 7.20.6.1 GPIO DC Characteristics (continued)

| PARAMETER       | TEST CONDITIONS                                          | MIN | TYP | MAX                  | UNIT |
|-----------------|----------------------------------------------------------|-----|-----|----------------------|------|
| V <sub>IL</sub> | Highest GPIO input voltage reliably interpreted as a Low |     |     | 0.2×V <sub>DD5</sub> | V    |

## 7.20.7 ADC

### 7.20.7.1 Analog-to-Digital Converter (ADC) Characteristics

T<sub>c</sub> = 25°C, V<sub>DD5</sub> = 3.0V, unless otherwise noted.<sup>(1)</sup>

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER                                          | TEST CONDITIONS                                                      | MIN                                                                                                                    | TYP   | MAX                 | UNIT   |
|----------------------------------------------------|----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------|---------------------|--------|
| <b>ADC Power Supply and Input Range Conditions</b> |                                                                      |                                                                                                                        |       |                     |        |
| V <sub>(Ax)</sub>                                  | Analog input voltage range                                           | All ADC analog input pins Ax                                                                                           | 0     | V <sub>DD5</sub>    | V      |
| I <sub>(ADC)</sub> single-ended mode               | Operating supply current into V <sub>DD5</sub> terminal              | RES = 0x0 (12Bit mode), Fs = 1.2MSPS, Internal reference OFF (ADC.REFCFG_REFEN = 0), VeREF+ = V <sub>DD5</sub>         | 480   |                     | μA     |
|                                                    |                                                                      | RES = 0x0 (12Bit mode), Fs = 266ksps, Internal reference ON (ADC.REFCFG_REFEN = 1), REFVSEL = 2.5V                     | 365   |                     |        |
| C <sub>I GPIO</sub>                                | Input capacitance into a single terminal                             |                                                                                                                        | 5     | 7                   | pF     |
| R <sub>I GPIO</sub>                                | Input MUX ON-resistance                                              |                                                                                                                        | 0.5   | 1                   | kΩ     |
| <b>ADC Switching Characteristics</b>               |                                                                      |                                                                                                                        |       |                     |        |
| F <sub>S</sub> ADCREF                              | ADC sampling frequency when using the internal ADC reference voltage | ADC.REFCFG_REFEN = 1, RES = 0x0 (12Bits), V <sub>DD5</sub> = 1.71V to V <sub>DD5</sub> max                             |       | 267 <sup>(2)</sup>  | ksps   |
| F <sub>S</sub> ADCREF                              | ADC sampling frequency when using the internal ADC reference voltage | ADC.REFCFG_REFEN = 1, RES = 0x1 (10Bits), V <sub>DD5</sub> = 1.71V to V <sub>DD5</sub> max                             |       | 308 <sup>(2)</sup>  | ksps   |
| F <sub>S</sub> ADCREF                              | ADC sampling frequency when using the internal ADC reference voltage | ADC.REFCFG_REFEN = 1, RES = 0x2 (8Bits), V <sub>DD5</sub> = 1.71V to V <sub>DD5</sub> max                              |       | 400 <sup>(2)</sup>  | ksps   |
| F <sub>S</sub> EXTREF                              | ADC sampling frequency when using the external ADC reference voltage | ADC.REFCFG_REFEN = 0, VeREF+ = V <sub>DD5</sub> , RES = 0x0 (12Bits), V <sub>DD5</sub> = 1.71V to V <sub>DD5</sub> max |       | 1.2 <sup>(2)</sup>  | MSPS   |
| F <sub>S</sub> EXTREF                              | ADC sampling frequency when using the external ADC reference voltage | ADC.REFCFG_REFEN = 0, VeREF+ = V <sub>DD5</sub> , RES = 0x1 (10Bits), V <sub>DD5</sub> = 1.71V to V <sub>DD5</sub> max |       | 1.33 <sup>(2)</sup> | MSPS   |
| F <sub>S</sub> EXTREF                              | ADC sampling frequency when using the external ADC reference voltage | ADC.REFCFG_REFEN = 0, VeREF+ = V <sub>DD5</sub> , RES = 0x2 (8Bits), V <sub>DD5</sub> = 1.71V to V <sub>DD5</sub> max  |       | 1.6 <sup>(2)</sup>  | MSPS   |
| N <sub>CONVERT</sub>                               | Clock cycles for conversion                                          | RES = 0x0 (12Bits)                                                                                                     | 14    |                     | cycles |
| N <sub>CONVERT</sub>                               | Clock cycles for conversion                                          | RES = 0x1 (10Bits)                                                                                                     | 12    |                     | cycles |
| N <sub>CONVERT</sub>                               | Clock cycles for conversion                                          | RES = 0x2 (8Bits)                                                                                                      | 9     |                     | cycles |
| t <sub>sample</sub>                                | Sampling time                                                        | RES = 0x0 (12-bit), R <sub>S</sub> = 25Ω, C <sub>pext</sub> = 10pF. ±0.5 LSB settling                                  | 166.6 |                     | ns     |
| t <sub>VSUPPLY/3(sample)</sub>                     | Sample time required when V <sub>supply</sub> /3 channel is selected |                                                                                                                        | 20    |                     | μs     |
| <b>ADC Linearity Parameters</b>                    |                                                                      |                                                                                                                        |       |                     |        |
| E <sub>I</sub>                                     | Integral linearity error (INL) for single-ended inputs               | 12-bit Mode, V <sub>R+</sub> = VeREF+ = V <sub>DD5</sub> , V <sub>DD5</sub> = 1.71-->3.8                               | ±2    |                     | LSB    |
| E <sub>D</sub>                                     | Differential linearity error (DNL)                                   | 12-bit Mode, V <sub>R+</sub> = VeREF+ = V <sub>DD5</sub> , V <sub>DD5</sub> = 1.71-->3.8                               | ±1    |                     | LSB    |
| E <sub>O</sub>                                     | Offset error                                                         | External reference, V <sub>R+</sub> = VeREF+ = V <sub>DD5</sub> , V <sub>DD5</sub> = 1.71-->3.8                        | -3    | 3                   | mV     |
| E <sub>O</sub>                                     | Offset error                                                         | Internal reference, V <sub>R+</sub> = REFVSEL = 2.5V                                                                   | -3    | 3                   | mV     |
| E <sub>G</sub>                                     | Gain error                                                           | External Reference, V <sub>R+</sub> = VeREF+ = V <sub>DD5</sub> , V <sub>DD</sub> = 1.71-->3.8                         | ±2    |                     | LSB    |
| E <sub>G</sub>                                     | Gain error                                                           | Internal reference, V <sub>R+</sub> = REFVSEL = 2.5V                                                                   | ±40   |                     | LSB    |
| <b>ADC Dynamic Parameters</b>                      |                                                                      |                                                                                                                        |       |                     |        |
| ENOB                                               | Effective number of bits                                             | ADC.REFCFG_REFEN = 0, VeREF+ = V <sub>DD5</sub> = 3.3V, VeREF- = 0V, RES = 0x2 (8-bit)                                 | 8     |                     | bit    |
| ENOB                                               | Effective number of bits                                             | ADC.REFCFG_REFEN = 0, VeREF+ = V <sub>DD5</sub> = 3.3V, VeREF- = 0V, RES = 0x1 (10-bit)                                | 9.9   |                     | bit    |
| ENOB                                               | Effective number of bits                                             | ADC.REFCFG_REFEN = 0, VeREF+ = V <sub>DD5</sub> = 3.3V, VeREF- = 0V, RES = 0x0 (12-bit)                                | 11.2  |                     | bit    |
| ENOB                                               | Effective number of bits                                             | ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x2 (8-bit)                                                        | 8     |                     | bit    |

### 7.20.7.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

$T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted.<sup>(1)</sup>

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER                                            |                                                                        | TEST CONDITIONS                                                                                                             | MIN   | TYP              | MAX              | UNIT          |
|------------------------------------------------------|------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|-------|------------------|------------------|---------------|
| ENOB                                                 | Effective number of bits                                               | ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x1 (10-bit)                                                            |       | 9.6              |                  | bit           |
| ENOB                                                 | Effective number of bits                                               | ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)                                                            |       | 10.4             |                  | bit           |
| ENOB                                                 | Effective number of bits                                               | VDDS reference, RES = 0x0 (12-bit)                                                                                          |       | 11.2             |                  | bit           |
| SINAD                                                | Signal-to-noise and distortion ratio                                   | ADC.REFCFG_REFEN = 0, $V_{\text{REF+}} = V_{\text{DDS}} = 3.3\text{V}$ , $V_{\text{REF-}} = 0\text{V}$ , RES = 0x0 (12-bit) |       | 69.18            |                  | dB            |
| SINAD                                                | Signal-to-noise and distortion ratio                                   | ADC.REFCFG_REFEN = 1, REFVSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)                                                            |       | 64.37            |                  | dB            |
| SINAD                                                | Signal-to-noise and distortion ratio                                   | VDDS reference, RES = 0x0 (12-bit)                                                                                          |       | 69.18            |                  | dB            |
| <b>ADC External Reference</b>                        |                                                                        |                                                                                                                             |       |                  |                  |               |
| EXTREF                                               | Positive external reference voltage input                              | ADC.REFCFG_REFEN=0, ADC reference sourced from external reference pin ( $V_{\text{REF+}}$ )                                 | 1.4   |                  | $V_{\text{DDS}}$ | V             |
| EXTREF                                               | Negative external reference voltage input                              | ADC.REFCFG_REFEN=0, ADC reference sourced from external reference pin ( $V_{\text{REF-}}$ )                                 |       |                  | 0                | V             |
| <b>ADC Supply Monitor</b>                            |                                                                        |                                                                                                                             |       |                  |                  |               |
| ADC Internal Input: $V_{\text{SUPPLY}} / 3$ Accuracy | $V_{\text{supply}}$ voltage divider accuracy for supply monitoring     | ADC input channel: $V_{\text{supply}}$ monitor                                                                              | -1.5% |                  | 1.5%             |               |
| ADC Internal Input: $I_{V_{\text{supply}} / 3}$      | $V_{\text{supply}}$ voltage divider current consumption                | ADC input channel $V_{\text{supply}}$ monitor. $V_{\text{supply}}=V_{\text{DDS}}=3.3\text{V}$                               |       | 10               |                  | $\mu\text{A}$ |
| <b>ADC Internal and VDDS Reference</b>               |                                                                        |                                                                                                                             |       |                  |                  |               |
| VDDREF                                               | Positive ADC reference voltage                                         | ADC reference sourced from VDDS                                                                                             |       | $V_{\text{DDS}}$ |                  | V             |
| ADCREF                                               | Internal ADC Reference Voltage                                         | ADC.REFCFG_REFEN = 1, REFVSEL = 0, $V_{\text{DDS}} = 1.71\text{V} - V_{\text{DDSMAX}}$                                      |       | 1.4              |                  | V             |
|                                                      |                                                                        | ADCREF_EN = 1, REFVSEL = 1, $V_{\text{DDS}} = 2.7\text{V} - V_{\text{DDSMAX}}$                                              |       | 2.5              |                  | V             |
| $I_{\text{ADCREF}}$                                  | Operating supply current into VDDA terminal with internal reference ON | ADC.REFCFG_REFEN = 1, $V_{\text{DDA}} = 1.7\text{V}$ to $V_{\text{DDAMAX}}$ , REFVSEL = {0,1}                               |       | 80               |                  | $\mu\text{A}$ |
| $t_{\text{ON}}$                                      | Internal ADC Reference Voltage power on-time                           | ADC.REFCFG_REFEN = 1                                                                                                        |       | 2                |                  | $\mu\text{s}$ |

(1) Using IEEE Std 1241-2010 for terminology and test methods

(2) Measured with 48MHz HFXT

## 7.20.8 Comparators

### 7.20.8.1 Low power comparator

$T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{V}$  (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS                                                                          | MIN | TYP      | MAX       | UNIT          |
|--------------------------|------------------------------------------------------------------------------------------|-----|----------|-----------|---------------|
| Input voltage range      |                                                                                          | 0   |          | $V_{DD5}$ | V             |
| Clock frequency          |                                                                                          |     | 32       |           | KHz           |
| Voltage divider accuracy | Input voltage range is between $V_{DD5}/4$ and $V_{DD5} \times 3/4$                      |     | 97%      |           |               |
| Offset                   | Measured at $V_{DD5} / 2$ (Errors seen when using two external inputs )                  |     | $\pm 15$ |           | mV            |
| Decision time            | Step from $-50\text{mV}$ to $50\text{mV}$                                                |     | 1        | 3         | Clock Cycle   |
| Comparator enable time   | COMP_LP disable $\rightarrow$ enable, VIN+, VIN– from pins, Overdrive $\geq 20\text{mV}$ |     | 80       |           | $\mu\text{s}$ |
| Current consumption      | Including using $V_{DD5}/2$ as internal reference at VIN– comparator terminal            |     | 370      |           | nA            |

## 7.20.9 Voltage Glitch Monitor

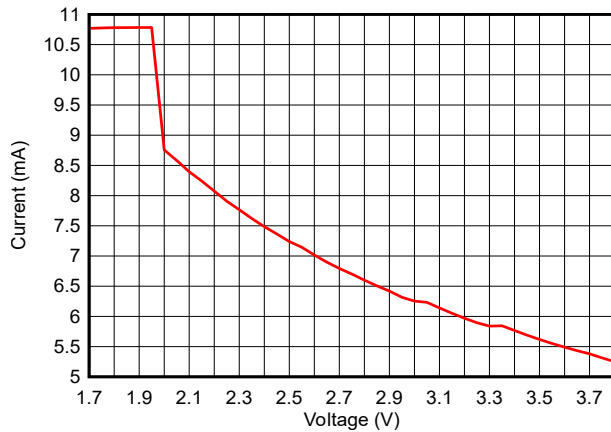
Over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                 | TEST CONDITIONS               | MIN | TYP | MAX | UNIT          |
|-------------------------------------------|-------------------------------|-----|-----|-----|---------------|
| <b>VGM</b>                                |                               |     |     |     |               |
| Current consumption from $V_{DD5}$ supply | VGM enabled                   |     | 60  |     | $\mu\text{A}$ |
| Turn-on time                              | From VGM enabled to VGM ready |     | 50  |     | $\mu\text{s}$ |

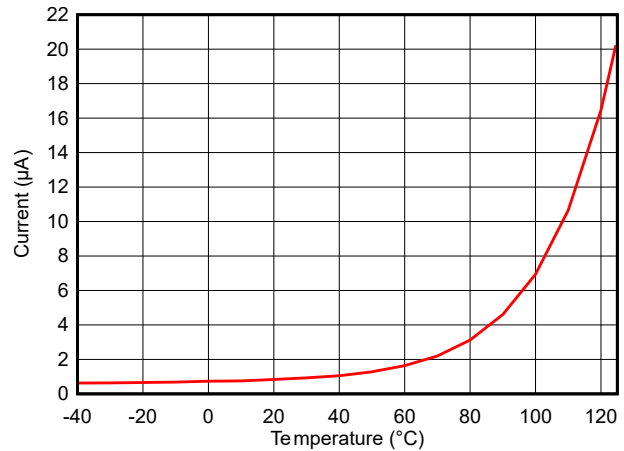
## 7.21 Typical Characteristics

All measurements in this section are done with  $T_c = 25^\circ\text{C}$  and  $V_{\text{DDS}} = 3.0\text{V}$ , unless otherwise noted. See [Recommended Operating Conditions](#) for device limits. Values exceeding these limits are for reference only.

### 7.21.1 MCU Current

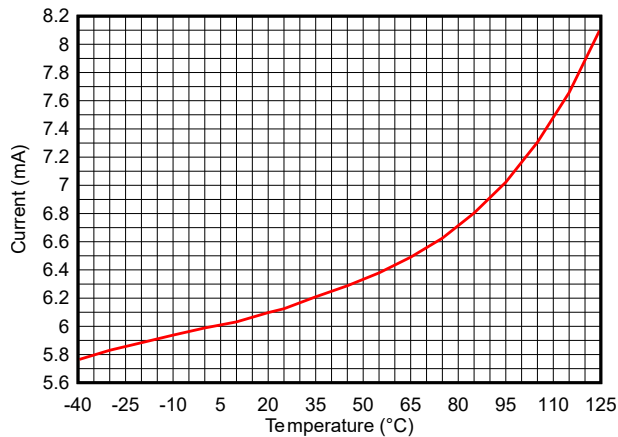


**Figure 7-6. Active Mode (MCU) Current vs Supply Voltage ( $V_{\text{DDS}}$ ) (Running CoreMark)**

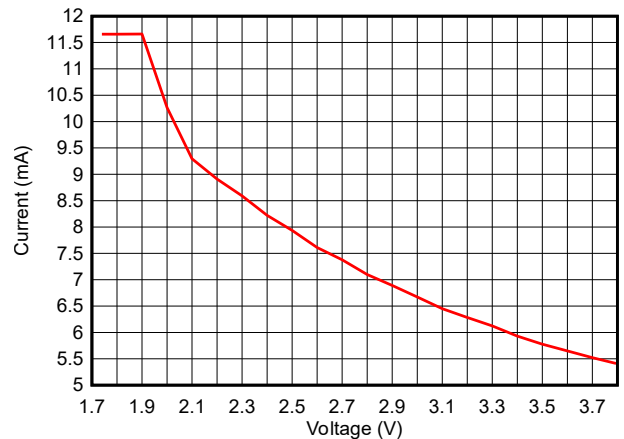


**Figure 7-7. Standby Mode (MCU) Current vs Temperature (SRAM and partial register retention, RTC enabled),  $V_{\text{DDS}} = 3.3\text{V}$**

### 7.21.2 RX Current

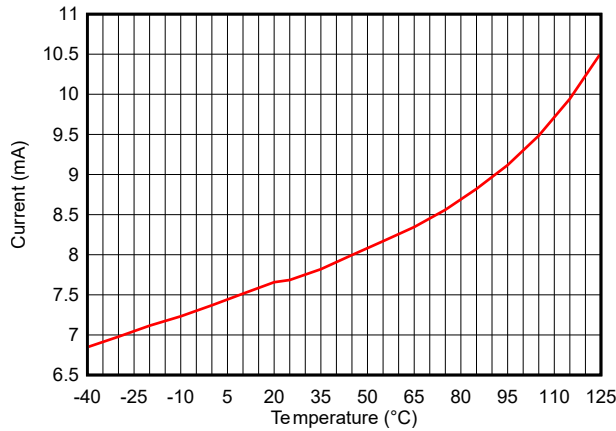


**Figure 7-8. RX Current vs Temperature (BLE 1Mbps, 2.44GHz),  $V_{\text{DDS}} = 3.3\text{V}$**

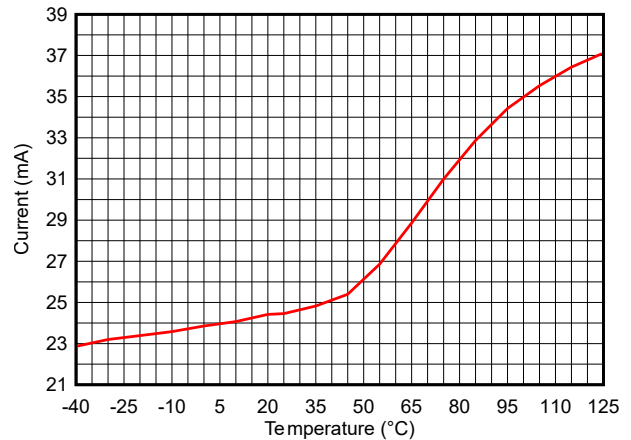


**Figure 7-9. RX Current vs Supply Voltage ( $V_{\text{DDS}}$ ) (BLE 1Mbps, 2.44GHz)**

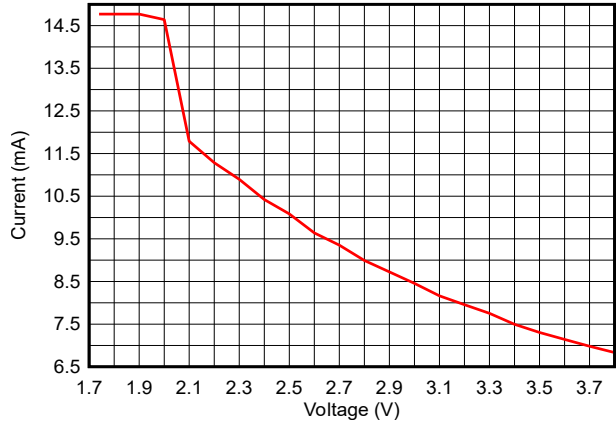
### 7.21.3 TX Current



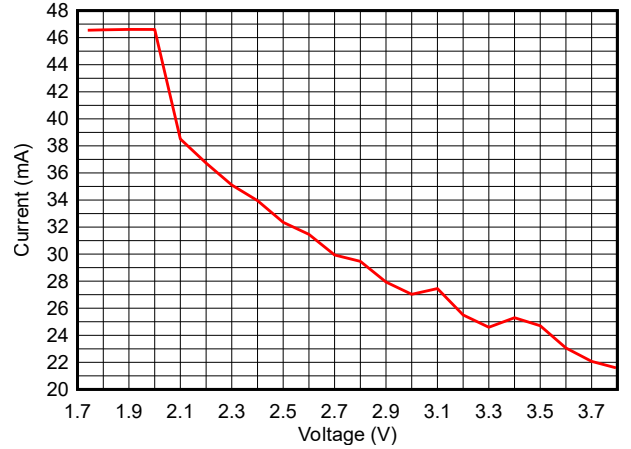
**Figure 7-10. TX Current vs Temperature (BLE 1Mbps, 2.44GHz, 0dBm), VDDS = 3.3V**



**Figure 7-11. TX Current vs Temperature (BLE 1Mbps, 2.44GHz, +10dBm), VDDS = 3.3V**



**Figure 7-12. TX Current vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, 0dBm)**



**Figure 7-13. TX Current vs Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, +10dBm)**

#### Note

The DCDC load support increases with VDDS supply voltage up to a specific supply threshold. Beyond this threshold the load support typically drops before increasing again until the next threshold. For high TX output power settings, the load on VDDR can exceed the DCDC load support and the extra load is supplied by internal GLDO. This manifests as multiple slight peaks on the TX current curve as a function of increasing VDDS supply voltage.

Table 7-1 shows typical TX current and output power for different output power settings.

**Table 7-1. Typical TX Current and Output Power (R variant)**2.4GHz, VDDS = 3.3V, DC/DC enabled, Temperature = 25°C (Measured on [LP-EM-CC2745R10-Q1](#))

| txPowerTable Index | TX Power Setting [dBm] (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
|--------------------|-----------------------------------------|----------------------------|----------------------------------|
| 1                  | 10                                      | 10                         | 24.5                             |
| 2                  | 9                                       | 9                          | 22.3                             |
| 3                  | 8                                       | 7.9                        | 20.3                             |
| 4                  | 7.5                                     | 7.3                        | 19.5                             |
| 5                  | 7                                       | 6.8                        | 18.8                             |
| 6                  | 6.5                                     | 6.25                       | 18                               |
| 7                  | 6                                       | 5.9                        | 17.7                             |
| 8                  | 5.5                                     | 5.4                        | 17.2                             |
| 9                  | 5                                       | 4.9                        | 10.8                             |
| 10                 | 4.5                                     | 4.6                        | 10                               |
| 11                 | 4                                       | 4.1                        | 9.7                              |
| 12                 | 3.5                                     | 3.6                        | 9.3                              |
| 13                 | 3                                       | 3.2                        | 9.0                              |
| 14                 | 2.5                                     | 2.6                        | 8.7                              |
| 15                 | 2                                       | 2.1                        | 8.7                              |
| 16                 | 1.5                                     | 1.7                        | 8.5                              |
| 17                 | 1                                       | 1.1                        | 8.2                              |
| 18                 | 0.5                                     | 0.65                       | 8.0                              |
| 19                 | 0                                       | 0.1                        | 7.7                              |
| 20                 | -4                                      | -3.9                       | 5.8                              |
| 21                 | -8                                      | -7.9                       | 5.3                              |
| 22                 | -12                                     | -11.8                      | 5.0                              |
| 23                 | -16                                     | -15.9                      | 4.8                              |
| 24                 | -20                                     | -20                        | 4.7                              |

**Table 7-2. Typical TX Current and Output Power (P variant)**

| 2.4GHz, VDDS = 3.3V, DC/DC enabled, Temperature = 25°C (Measured on LP-EM-CC2755P10) |                                         |                            |                                  |
|--------------------------------------------------------------------------------------|-----------------------------------------|----------------------------|----------------------------------|
| txPowerTable Index                                                                   | TX Power Setting [dBm] (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 1                                                                                    | 20                                      | 19.8                       | 132                              |
| 2                                                                                    | 19                                      | 18.8                       | 110                              |
| 3                                                                                    | 18                                      | 18.2                       | 101                              |
| 4                                                                                    | 17                                      | 17.2                       | 89                               |
| 5                                                                                    | 16                                      | 16                         | 75                               |
| 6                                                                                    | 15                                      | 15.2                       | 71                               |
| 7                                                                                    | 14                                      | 14.1                       | 62                               |
| 8                                                                                    | 13                                      | 13                         | 56                               |
| 9                                                                                    | 12                                      | 12.4                       | 52                               |
| 10                                                                                   | 11                                      | 10.9                       | 34                               |
| 11                                                                                   | 10                                      | 9.9                        | 28.2                             |
| 12                                                                                   | 9                                       | 8.9                        | 25.3                             |
| 13                                                                                   | 8                                       | 8                          | 23.5                             |
| 14                                                                                   | 7                                       | 6.9                        | 21.6                             |
| 15                                                                                   | 6                                       | 5.9                        | 20                               |
| 16                                                                                   | 5                                       | 4.9                        | 18.6                             |
| 17                                                                                   | 4                                       | 4.2                        | 10                               |
| 18                                                                                   | 3                                       | 3.4                        | 9.7                              |
| 19                                                                                   | 2                                       | 2.4                        | 9.1                              |
| 20                                                                                   | 2                                       | 1.4                        | 9.0                              |
| 21                                                                                   | 0                                       | 0.5                        | 8.6                              |
| 22                                                                                   | -4                                      | -3.6                       | 6.4                              |
| 23                                                                                   | -8                                      | -7.3                       | 6.2                              |
| 24                                                                                   | -12                                     | -11.5                      | 5.6                              |
| 25                                                                                   | -16                                     | -15.2                      | 5.5                              |
| 26                                                                                   | -20                                     | -19.3                      | 5.2                              |

## 7.21.4 RX Performance

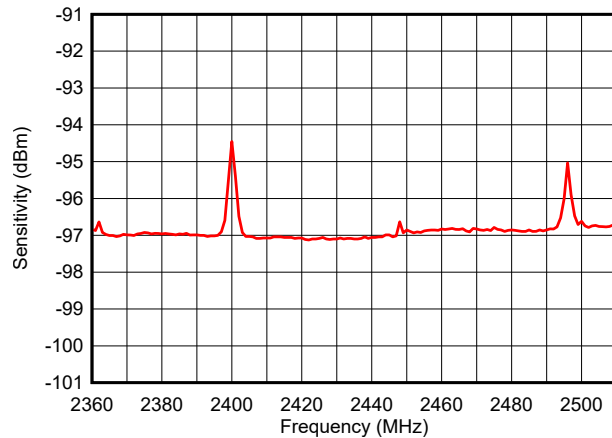


Figure 7-14. Sensitivity vs Frequency (BLE 1Mbps)

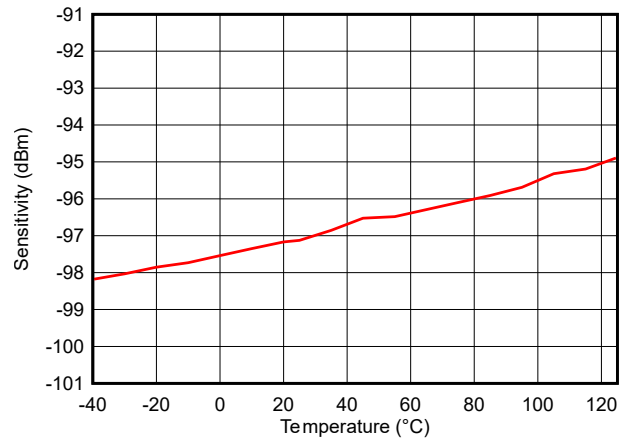


Figure 7-15. Sensitivity vs Temperature (BLE 1Mbps, 2.44GHz)

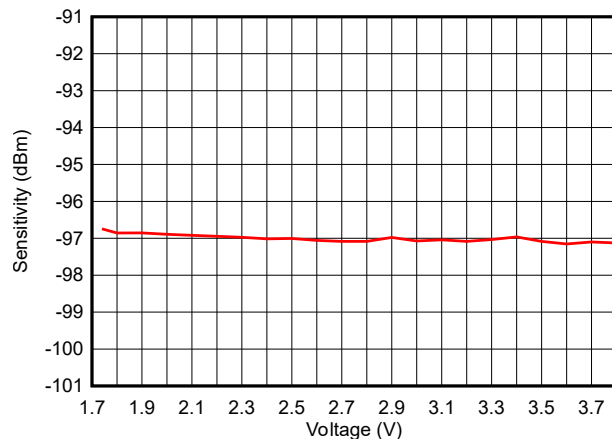


Figure 7-16. Sensitivity vs Supply Voltage (VDD) (BLE 1Mbps, 2.44GHz)

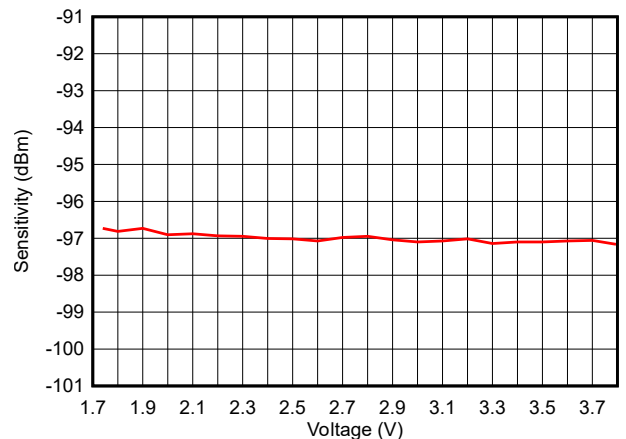


Figure 7-17. Sensitivity vs Supply Voltage (VDD) (BLE 1Mbps, 2.44GHz, DC/DC Disabled)

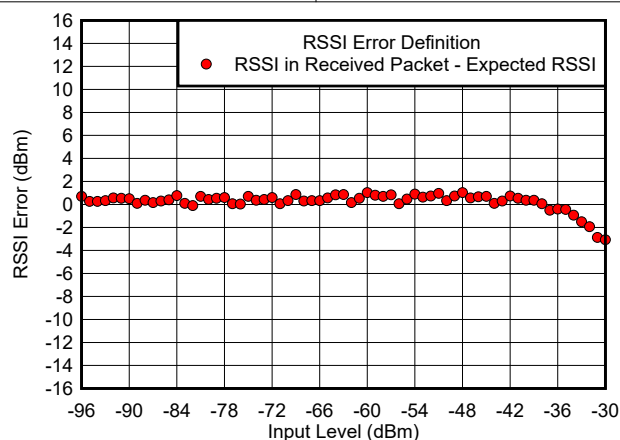
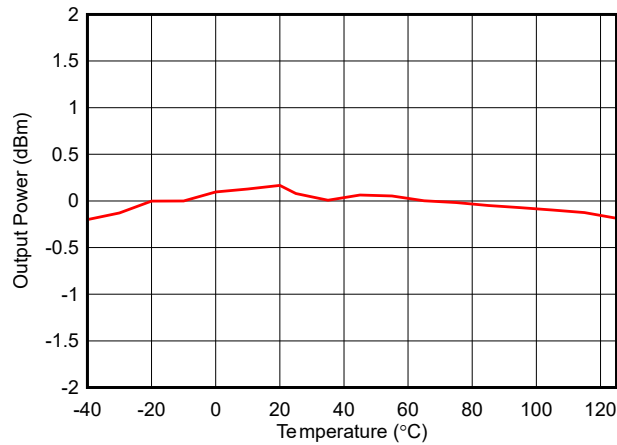
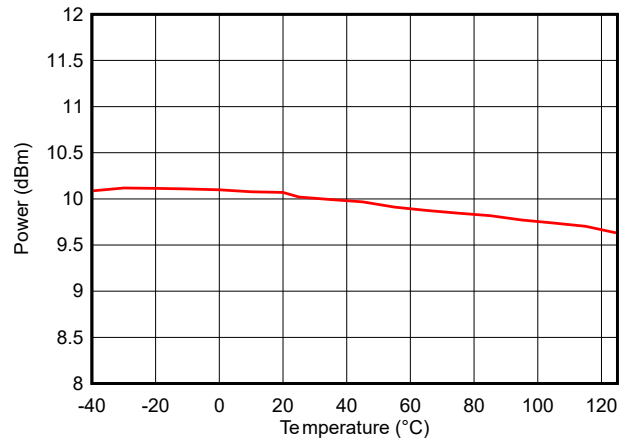


Figure 7-18. RSSI Error vs Input Level (dBm)

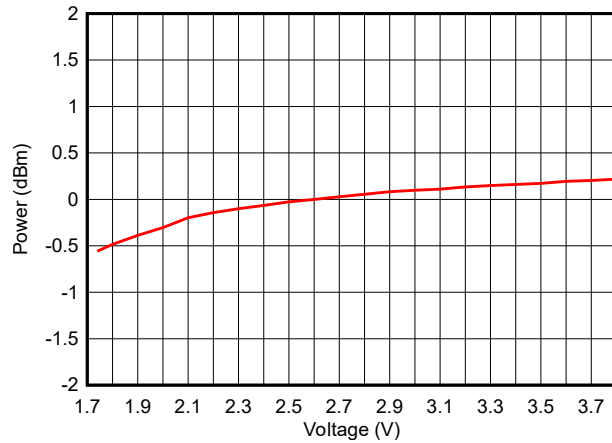
### 7.21.5 TX Performance



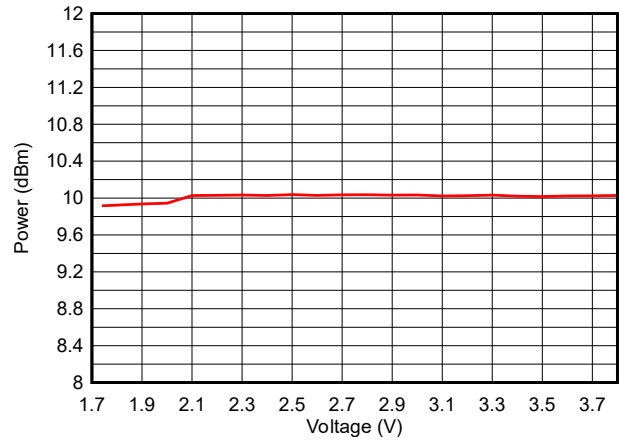
**Figure 7-19. Output Power vs Temperature (BLE 1Mbps, 2.44GHz, 0dBm)**



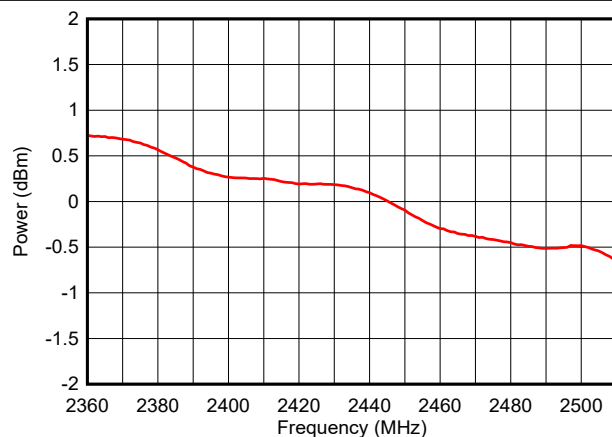
**Figure 7-20. Output Power vs Temperature (BLE 1Mbps, 2.44GHz, +10dBm)**



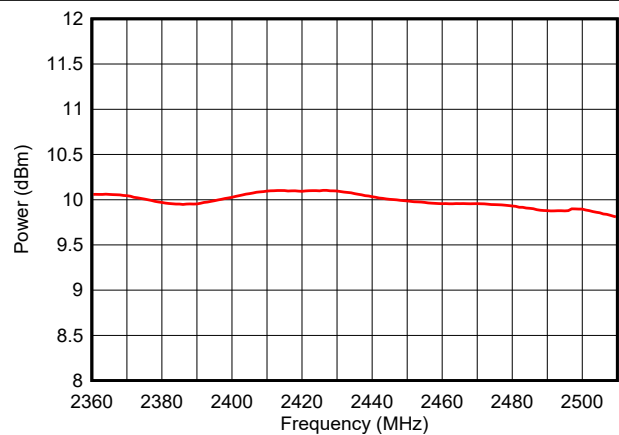
**Figure 7-21. Output Power vs Supply Voltage (VDDs) (BLE 1Mbps, 2.44GHz, 0dBm)**



**Figure 7-22. Output Power vs Supply Voltage (VDDs) (BLE 1Mbps, 2.44GHz, +10dBm)**

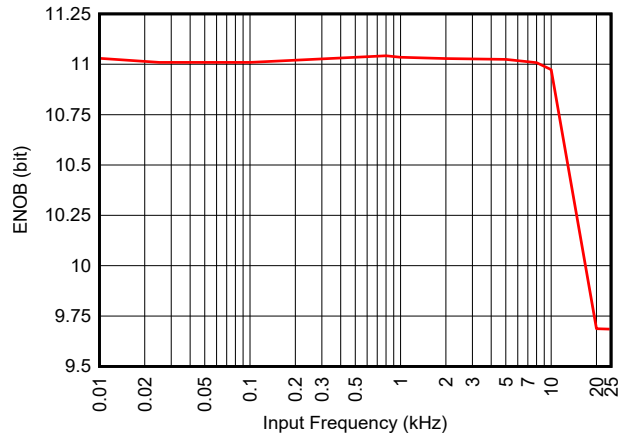


**Figure 7-23. Output Power vs Frequency (BLE 1Mbps, 0dBm)**

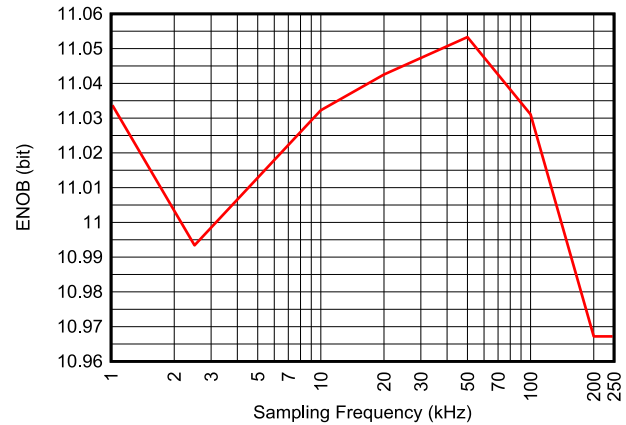


**Figure 7-24. Output Power vs Frequency (BLE 1Mbps, +10dBm)**

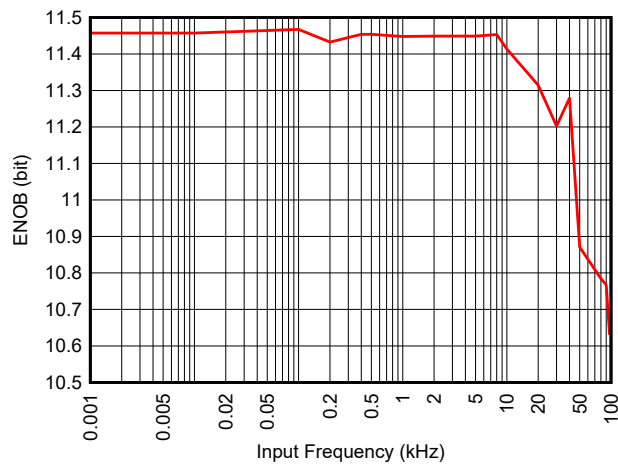
## 7.21.6 ADC Performance



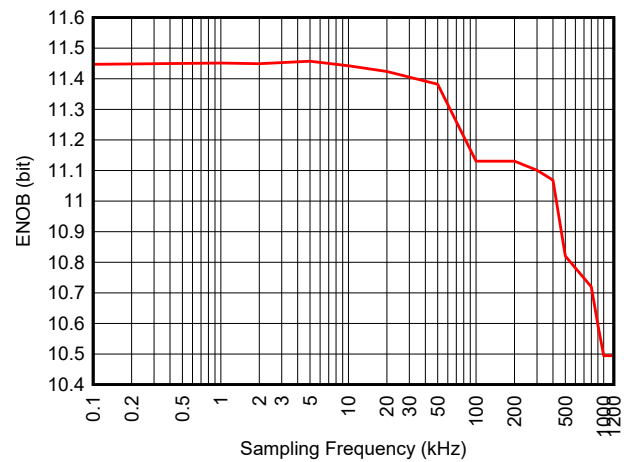
**Figure 7-25. ENOB vs Input Frequency (Internal Reference)**



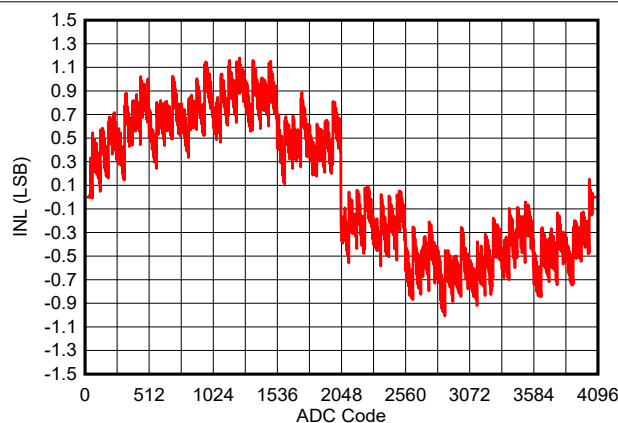
**Figure 7-26. ENOB vs Sampling Frequency ( $V_{in}=3V$  Ramp Wave, Internal Reference,  $F_{in}=F_s/10$ )**



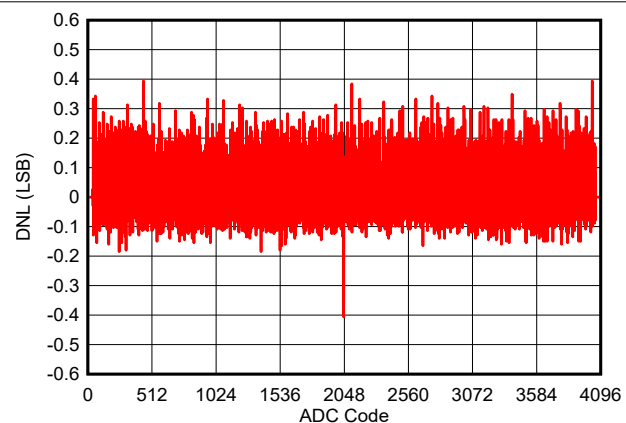
**Figure 7-27. ENOB vs Input Frequency (External Reference = 3.0V)**



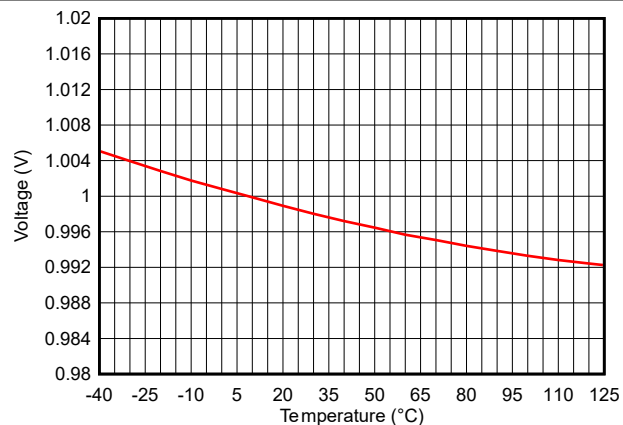
**Figure 7-28. ENOB vs Sampling Frequency ( $V_{in}=3V$  Ramp Wave, Internal Reference, 200ksps)**



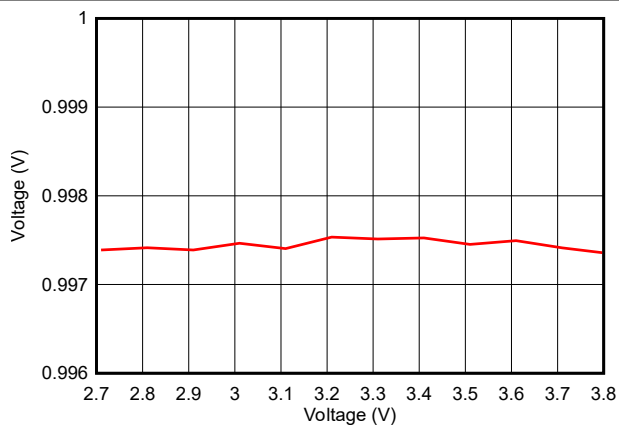
**Figure 7-29. INL vs ADC Code ( $V_{in}=3V$  Ramp Wave, Internal Reference, 200ksps)**



**Figure 7-30. DNL vs ADC Code ( $V_{in}=3V$  Sine Wave, Internal Reference, 200ksps)**



**Figure 7-31. ADC Accuracy vs Temperature**  
( $V_{in}=1V$ , Internal Reference, 200ksps)



**Figure 7-32. ADC Accuracy vs Supply Voltage**  
( $V_{in}=1V$ , Internal Reference, 200ksps)

## 8 Detailed Description

### 8.1 Overview

Section 4 shows the core modules of the CC274x devices.

### 8.2 System CPU

The CC27xx SimpleLink™ Wireless MCU contains an Arm® Cortex®-M33 system CPU, which runs the application, the protocol stacks, and the radio. The Cortex-M33 processor achieves an optimal blend of real-time determinism, energy efficiency, software productivity, and system security. The 32-bit processor core is built with the mainline extension Armv8-M architecture designed for low-latency processing. The Cortex-M33 processor offers multiple benefits to developers, including:

- Real-time deterministic, high-performance interrupt handling with 32-bit performance
- Security foundation with the addition of TrustZone-M technology
- Low-power processing with ease of software development

The Cortex-M33 processor offers multiple benefits to developers, making it ideal for automotive, IoT, and embedded applications that require efficient security or digital signal control. Some of the features include:

- Armv8-M architecture with mainline extension
- Thumb/Thumb-2 subset instruction support
- 3-stage pipeline
- Software security:
  - TrustZone-M for Armv8-M, with Security Attribution Unit (SAU) of up to eight regions
  - Stack limit boundaries and checking
- DSP extension: including all the V8.1-M DSP/SIMD instructions
- Floating Point Unit (FPU): single precision floating point unit, IEEE 754 compliant
- Memory Protection Unit (MPU) with eight regions for the secure state (MPU\_S) and eight regions for the non-secure state (MPU\_NS)
- 24-bit SysTick timer for each security domain
- Integrated Nested Vectored Interrupt Controller (NVIC) supporting Non-Maskable Interrupt (NMI)
- Low-power sleep modes
  - Arm® SLEEP maps to the device's idle power mode
  - Arm® DEEPSLEEP maps to the device's standby power mode
- Serial Wire Debug ports with up to eight breakpoints and four watchpoints
- Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (ITM)
- 96MHz operation on CC27xx with 1.41DMIPS/MHz and 3.85 CoreMark® / MHz (running CoreMark® from flash) performance
- Arm® CDE (Custom Data Extension) instruction support for machine learning acceleration

Additionally, the CC27xx devices are compatible with all Arm® tools and software.

### 8.3 Radio (RF Core)

The low-power RF Core (LRF) implements a high-performance and highly flexible RF subsystem containing RF and baseband circuitry in addition to a software-defined digital radio (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing-critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry, such as RF switches or range extenders, autonomously.

The modem is highly configurable and has the flexibility to support future standards. It is not programmable by customers but is instead loaded with precompiled images provided in the radio driver in the SimpleLink™ Low Power F3 software development kit (SDK). This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory; thus, image loading from flash only occurs once after boot, and no patching is required when exiting power modes.

#### 8.3.1 Bluetooth® Low Energy

The RF Core offers full support for Bluetooth® Low Energy, including the high-speed 2Mbps physical layer and the 500kbps and 125kbps long-range PHYs (Coded PHY) through the TI-provided Bluetooth® stack or through a standardized host controller interface.

The RF Core and the TI-provided Bluetooth® stack support the Bluetooth® 6 Channel Sounding feature to enable a new high-accuracy and low-cost distance measurement method between two Bluetooth® LE devices.

### 8.4 Memory

The CC27xx devices support up to 1MB of nonvolatile (Flash) memory to provide storage for code and data. The flash memory is in-system programmable and erasable. Dual flash banks (up to 512kB each) are supported to enable reading/execution from one flash bank when erasing/writing to the other flash bank. Special flash memory sectors contain Customer Configuration (CCFG) and Security Configuration (SCFG) sections that are used by system ROM bootcode and TI-provided drivers to configure the device. The CCFG and SCFG configurations are generated using the device configuration Sysconfig tool.

Up to 162KB of ultra-low leakage system static RAM (SRAM) can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. Parity checking for detecting bit errors in memory is an optional feature that is built-in to reduce chip-level soft errors and increase reliability. With the SRAM parity enabled, the SRAM size is limited to 144KB.

Upon regular device boot, the user application can use hardware mechanisms for SRAM clearing. To improve code execution speed and reduce power consumption when executing code from nonvolatile memory, a 4-way set-associative 8KB cache is enabled by default to cache and prefetch instructions read by the system CPU.

The system ROM includes device bootcode firmware that is the first piece of code that executes upon device power-up or reset. The system ROM handles the execution of device start-up routines, initial device trimming, and device security features, including secure boot operations and device lifecycle management. The system ROM also contains a serial (SPI and UART) bootloader that can be used for the initial programming of the device. The system ROM firmware includes open-source MCUBoot software that is licensed under APACHE-2.0. See the corresponding license terms and notice information in [Software License and Notice](#) section. Some system ROM firmware is licensed under the BSD-3-clause license.

### 8.5 Hardware Security Module (HSM)

The CC27xx devices have an integrated hardware security module (HSM) supporting an isolated environment for cryptographic, key management, secure counters, and random number generation operations. Selected algorithms are protected from differential power analysis (DPA) side channel attacks. Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), the system enables secure and future-proof automotive and IoT applications to be easily built on the platform.

The following cryptographic functions using energy-efficient accelerators and RNG functions are accelerated by the HSM:

- Key Agreement Schemes
  - Elliptic Curve Diffie-Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Diffie Hellman with static or ephemeral keys (DH and DHE)
- Signature Processing
  - Elliptic Curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
  - Edwards-Curve Digital Signature Algorithm (EdDSA)
  - RSA PKCS #1 v1.5
  - RSA PSS
- Message Authentication Codes
  - AES CBC-MAC
  - AES CMAC
  - HMAC with SHA2-224, SHA2-256, SHA2-384, and SHA2-512
- Block Cipher Modes of Operation
  - AES CCM and AES CCM\* (CCM-Star)
  - AES GCM
  - AES ECB
  - AES CBC
  - AES CTR
- Hash Algorithms
  - SHA2-224
  - SHA2-256
  - SHA2-384
  - SHA2-512
- Random Number Generation
  - TRNG (True Random Number Generator)
  - AES-CTR DRBG (Deterministic Random Bit Generator)

Cryptographic key sizes and types include:

- Advanced Encryption Standard (AES) key sizes of 128, 192, and 256 bits
- RSA key sizes up to 3072 bits (Sign and Verify supported), and up to 4096 bits (verify only)
- Diffie-Hellman key sizes of 2048 bits and 3072 bits
- Elliptic Curve Support
  - Short Weierstrass
    - NIST-P224 (secp224r1), NIST-P256 (secp256r1), NIST-P384 (secp384r1), NIST-P521 (secp521r1)
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
  - Montgomery
    - Curve25519
  - Twisted Edwards form
    - Ed25519

DPA countermeasures are implemented for:

- AES operations
- ECDSA operations

The HSM executes the HSM firmware from a secured flash region. 96KB of the device flash memory is reserved for the HSM firmware. The HSM firmware is verified by the HSM ROM during the HSM boot process. Secure firmware update of the HSM firmware image on-chip is handled by the system ROM bootcode and the HSM ROM.

The HSM also has a data RAM region that is not accessible to the rest of the system (system CPU, DMA, debug access, and so on). The data RAM region is retained in low-power modes, supporting quick power-up of the

HSM and retention of key material. In addition to the storage of key material in data RAM, the HSM supports importing and exporting wrapped key material (NIST SP800-38F) with a key unique to the device, known as a HW Unique Key (HUK). This allows keys to be securely stored anywhere in the system's nonvolatile (Flash) memory.

The HSM is accessible to the application running on the system CPU in a controlled manner via the HSM mailbox interface. The HSM is a bus controller in the device and can access the system memory directly, enabling better efficiency for moving data during cryptographic operations.

The SimpleLink Low Power F3 software development kit (SDK) includes the encrypted and authenticated HSM firmware needed to be programmed on-chip for the HSM operation and drivers for all HSM functions.

## 8.6 Cryptography

The CC27xx devices also integrate LAES, an AES-128 cryptography hardware accelerator (outside the HSM), to support latency-critical link-layer encryption/decryption operations prescribed by the wireless protocols. It also has the benefit of being lower power and improves the availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The AES hardware accelerator supports the following block cipher modes and message authentication codes:

- AES ECB encrypt-only
- AES CBC encrypt-only
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)

Software implementation of AES GCM cipher mode using LAES for low-level cryptographic operations is supported. The AES hardware accelerator can be fed with plaintext/ciphertext from either the CPU or using DMA. Sustained throughput of one 16-byte ECB block per 23 cycles is possible, corresponding to > 30Mbps.

## 8.7 Timers

A large selection of timers is available as part of the CC27xx devices. These timers are:

### Real-Time Clock (RTC)

The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock. The RTC is active in STANDBY and ACTIVE power states. Upon asynchronous device resets (that is, reset pin, exit from shutdown, LF clock loss, and so on), the RTC is reset. However, upon internally generated synchronous device resets (for example, WDT, debug reset, system reset request, and so on), the RTC is not reset.

The RTC accumulates the time elapsed since its last reset on each LFCLK. It is also possible to update the RTC value as part of the RTC configuration to match a different time base. The RTC counter is incremented by LFCLK at a rate between 30kHz and 34kHz, depending on the LF clock source. LFINC indicates the period of LFCLK in  $\mu$ s with an additional granularity of 16 fractional bits and is used to increment time in the RTC. Hardware measurement circuitry can automatically measure the LFCLK period whenever HFXT is running and update LFINC.

The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multichannel and higher resolution SYSTIM remain in synchronization with the RTC's time base.

The RTC has two channels: one compare channel and one capture channel, which is capable of waking the device out of the standby power state. The RTC compare channel is typically used only by system software and only during the standby power state.

## System Timer (SYSTIM)

The SYSTIM is a 34-bit, 6-channel wrap-around timer with a per-channel selectable 32b time slice with either a 1 $\mu$ s resolution and 1h11m35s range or 250ns resolution and 17m54s range. One channel is reserved for system software, three channels are reserved for radio software, and two channels are freely available to user applications. All user-available channels support both capture and single-shot compare (posting an event) operations.

For software convenience, a hardware synchronization mechanism automatically ensures that the RTC and SYSTIM share a common time base. Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel will immediately trigger if the submitted event is in the immediate past (4.294s with 1 $\mu$ s resolution and 1.049s with 250ns resolution).

## General Purpose Timers (LGPT)

The CC27xx devices provide four LGPTs with 3  $\times$  16-bit timers and 1  $\times$  32-bit timers, all running on up to 48MHz. The LGPTs support a wide range of features such as:

- Three capture/compare channels
- One-shot or periodic counting
- Pulse width modulation (PWM)
- Time counting between edges and edge counting
- Input filter implemented on each of the channels for all timers
- IR generation feature using Timer-0 and Timer-1
- Dead band feature available on Timer-1

The timer capture/compare and PWM signals are connected to IOs through the IO controller module (IOC), and the internal timer event connections to CPU, DMA, and other peripherals are through the event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA, and ADC. Two LGPTs support quadrature decoder mode to enable buffered decoding of quadrature-encoded sensor signals. The LGPTs are available in device Active and Idle power modes.

**Table 8-1. Timer Comparison**

| CC27xx GP TIMER FEATURE         | TIMER 0 | TIMER 1 | TIMER 2 | TIMER 3 |
|---------------------------------|---------|---------|---------|---------|
| Counter Width                   | 16-bit  | 16-bit  | 16-bit  | 32-bit  |
| Quadrature Decoder              | Yes     | No      | Yes     | No      |
| Park Mode on Fault              | No      | Yes     | No      | No      |
| Programmable Deadband Insertion | No      | Yes     | No      | No      |

## Watchdog Timer

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. Upon counter expiry, the watchdog timer resets the device when periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 32kHz clock rate and operates in device active, idle, and standby modes, and cannot be stopped once enabled.

## 8.8 Algorithm Processing Unit (APU)

The APU is a generic mathematical acceleration module that operates with single-precision floating-point numbers (IEEE 754 format) and is optimized to work with complex numbers. The APU runs at 96MHz, operates autonomously from the main CPU in the system, and can be used to offload numerically intensive operations. This module handles efficient vector (and matrix) operations and sustains one complex Multiply-and-Add operation per clock cycle. These operations are extensively used in advanced post-processing algorithms needed for accurate phase-based distance estimation using the Bluetooth® LE Channel Sounding mechanism; thereby, optimizing the overall channel-sounding-based distance estimation latency and energy efficiency.

The APU has 8KB of local data memory (separate from the system RAM) where the application can read/write data. The APU incorporates a programmable core to handle advanced APIs developed for the APU hardware accelerator submodules. The SimpleLink™ Low Power F3 software development kit (SDK) includes the APU APIs that are executed by the APU programmable core within RAM-based local program memory (separate from the system RAM and VCE data RAM).

The user application handles chain-calling the different APU APIs and moving data in/out of the APU local data memory. The SimpleLink™ Low Power F3 software development kit (SDK) supports SW drivers and examples to enable APU operations.

## 8.9 Serial Peripherals and I/O

The CC27xx devices provide 2xUART, 2xSPI, 1xI2C, 1xCAN-FD, and 1xI2S serial peripherals.

The UART module implements universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3Mbps and IRDA SIR mode of operation.

The SPI module supports the SPI controller and peripherals up to 12MHz with configurable phase and polarity.

The I<sup>2</sup>C module communicates with devices compatible with the I<sup>2</sup>C standard. The I<sup>2</sup>C interface can handle 100kHz and 400kHz operation and can serve as both controller and target.

The CAN-FD module communicates with devices supporting Classic CAN (1Mbps) and CAN Flexible Data (FD) (up to 5Mbps) modes. CAN-FD supports faster data speed, higher data capacity (up to 64B payload size per CAN frame), and dynamic switching between different data rates and longer or shorter messages; thereby, enabling several system operational advantages compared to classic CAN.

The I<sup>2</sup>S interface handles digital audio and can also interface with pulse-density modulation microphones (PDM).

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open-source.

Some GPIOs have high-drive capabilities, which are marked in bold in [RHA \(6mm × 6mm\) Pinout, 0.5mm Pitch \(Top View\)](#).

VDDIO split rail I/O supply enables using a different I/O supply rail compared to the main VDDSS supply rail. This enables applications to interface with other system components at a different voltage level compared to the main VDDSS power supply level. GPIOs supplied by VDDIO and VDDSS supplies are listed in orange or blue, respectively, in [RHA \(6mm × 6mm\) Pinout, 0.5mm Pitch \(Top View\)](#). The voltage rails supplied on VDDSS and VDDIO pins can ramp up and down in any order, independent of each other, and any combination of VDDSS and VDDIO supplies being unpowered can be supported indefinitely. This simplifies the system-level power supply design, where it is not needed to control the availability or ramp-up/down sequence of these supplies at the VDDIO and VDDSS pins.

For more information, see the [CC27xx SimpleLink™ Wireless MCU Technical Reference Manual](#).

## 8.10 Battery and Temperature Monitor

A combined temperature and battery voltage monitor are available in the CC27xx devices. The battery and temperature monitor allow an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when the temperature or supply voltage goes outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

## 8.11 Voltage Glitch Monitor (VGM)

The CC27xx devices support the VGM on-chip to mitigate security risks from low-cost and low-effort physical non-invasive fault attacks.

The VGM is enabled by default during device boot time operations. After the device boot operations, the VGM can be kept enabled or optionally disabled during device runtime operations based on application security needs.

## 8.12 $\mu$ DMA

The device includes a direct memory access ( $\mu$ DMA) controller. The  $\mu$ DMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The  $\mu$ DMA controller can perform transfers between memory and memory or between memory and peripherals. The  $\mu$ DMA controller supports triggers from the various on-chip peripherals and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

For applications using TrustZone-M, upon device bootup, the  $\mu$ DMA is configured as a secure peripheral by default and can be configured as a non-secure peripheral by the application. The  $\mu$ DMA channels cannot individually be configured as secure or non-secure peripherals, and so, the application is required to select at compile time if the SDK shall configure the  $\mu$ DMA controller as a secure or non-secure peripheral. The SimpleLink Low Power F3 SDK  $\mu$ DMA drivers support using the  $\mu$ DMA as a non-secure peripheral for application operations.

Some features of the  $\mu$ DMA controller include the following (this is not an exhaustive list):

- Channel operation of up to 12 channels, with 8 channels having a dedicated peripheral interface (multiplexed) and 4 channels having the ability to be triggered through configurable events. Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

## 8.13 Debug

On-chip debugging is supported through the serial wire debug (SWD) interface, which is an Arm® bi-directional 2-wire protocol that communicates with the SWD controller and enables complete debug functionality. SWD is fully compatible with the Texas Instruments XDS family of debug probes. The Cortex M33 core supports advanced debugging features, including Data Watchpoint and Trace unit (DWT), which supports watchpoints and system profiling for the CM33 processor. The Cortex M33 core also supports Instrumentation Trace Macrocell (ITM), which supports print-style debugging to trace operating system (OS) and application events and provides diagnostic system information.

## 8.14 Power Management

To minimize power consumption, the CC27xx devices support multiple power modes and power management features (see [Table 8-2](#)).

**Table 8-2. Power Modes**

| MODE                                                | SOFTWARE CONFIGURABLE POWER MODES <sup>(1)</sup> |                      |                            |           | RESET PIN HELD |
|-----------------------------------------------------|--------------------------------------------------|----------------------|----------------------------|-----------|----------------|
|                                                     | ACTIVE                                           | IDLE                 | STANDBY                    | SHUTDOWN  |                |
| CPU                                                 | Active                                           | Off                  | Off                        | Off       | Off            |
| Flash                                               | On                                               | Available            | Off                        | Off       | Off            |
| SRAM                                                | On                                               | On                   | Retention                  | Off       | Off            |
| Radio                                               | Available                                        | Available            | Off                        | Off       | Off            |
| Supply System                                       | On                                               | On                   | Duty Cycled                | Off       | Off            |
| CPU register retention                              | Full                                             | Full                 | Full <sup>(2)</sup>        | No        | No             |
| SRAM retention                                      | Full                                             | Full                 | Full                       | Off       | Off            |
| 96 MHz high-speed clock (HFCLK)                     | HFOSC <sup>(3)</sup>                             | HFOSC <sup>(3)</sup> | Duty Cycled <sup>(4)</sup> | Off       | Off            |
| 80/90/98 MHz Auxiliary Frequency Oscillator (AFOSC) | AFOSC                                            | AFOSC                | Off <sup>(5)</sup>         | Off       | Off            |
| 32 kHz low-speed clock (LFCLK)                      | LFXT or LFOSC                                    | LFXT or LFOSC        | LFXT or LFOSC              | Off       | Off            |
| Peripherals                                         | Available                                        | Available            | IOC, BATMON, RTC, LPCOMP   | Off       | Off            |
| Wake-up on RTC                                      | N/A                                              | Available            | Available                  | Off       | Off            |
| Wake-up on pin edge                                 | N/A                                              | Available            | Available                  | Available | Off            |
| Wake-up on reset pin                                | On                                               | On                   | On                         | On        | On             |
| Brownout detector (BOD)                             | On                                               | On                   | Duty Cycled                | Off       | Off            |
| Power-on reset (POR)                                | On                                               | On                   | On                         | On        | On             |
| Watchdog timer (WDT)                                | Available                                        | Available            | Available                  | Off       | Off            |

- (1) "Available" indicates that the specific IP or feature can be enabled by the user application in the corresponding device operating modes. "On" indicates that the specific IP or feature is turned on, irrespective of the user application configuration of the device in the corresponding device operating mode. "Off" indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode.
- (2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode.
- (3) In active and idle power modes, the HFOSC tracking loop is enabled by default, thereby enabling 48MHz HFXT as well.
- (4) If LFOSC HW calibration is enabled in standby mode, then, HFOSC tracking loop requiring HFXT is duty-cycled. If not, only HFOSC is duty-cycled during recharge cycles.
- (5) AFOSC standby behavior is controlled by AFOSCCTL.AUTODIS. When set, AFOSC is disabled when entering standby. Enabling AFOSC again on standby exit must be done by software.

In the **Active** mode, both of MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU.

In **Idle** mode, the CPU is in sleep, but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on the state of the DMA and debug subsystem.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. Pin Reset will also drive the device from Standby to Active. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a wake from shutdown pin wakes up the device and functions as a reset trigger. The CPU can differentiate between a reset

in this way and a reset-by-reset pin or power-on reset, or thermal shutdown reset, by reading the reset status register. The only states retained in this mode are the latched I/O state, the 3V register bank, and the flash memory contents.

---

**Note**

The power, RF, and clock management for the CC27xx devices require specific configuration and handling by software for optimized performance. This configuration and handling are implemented in the TI-provided drivers that are part of the SimpleLink Low Power F3 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with FreeRTOS, device drivers, and examples are offered free of charge in source code.

---

## 8.15 Clock Systems

The CC27xx devices have the following internal system clocks.

- The 96MHz HFCLK is used as the main system (MCU and peripherals) clock. This is driven by the internal 96MHz RC Oscillator (HFOSC), which can track its accuracy against an external 48MHz crystal (HFXT). The HFOSC tracking loop is enabled by default by the system ROM bootcode. Radio and ADC operate with the external 48MHz crystal oscillator.
- The 32.768kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer after exiting Standby power mode. LFCLK can be driven by the internal 30-34kHz RC Oscillator (LFOSC), a 32.768kHz watch-type crystal, or a clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32kHz LFCLK signal to other devices, thereby reducing the overall system cost.
- The 80/90.3168/98.304 MHz AFOSC (Auxiliary Frequency Oscillator) is used as the high-frequency clock for generating needed frequencies to support for CAN-FD and audio I<sup>2</sup>S operations. The AFOSC tracks the HFOSC, which in turn, tracks its accuracy against the external 48MHz crystal (HFXT). AFOSC can generate 80, 90.3168, and 98.304MHz clock frequencies with a 10ppb tracking accuracy from HFOSC.

## 8.16 Network Processor

Depending on the product configuration, the CC27xx device can function as a wireless network processor (WNP—a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC—with the application and protocol stack running on the system CPU inside the device).

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

## 8.17 Integrated BALUN, High Power PA (Power Amplifier)

For applications that need an increased RF link budget, the CC27xx high-power PA device variants (“P” devices) can support RF transmit output power operation up to +20dBm EIRP (Effective Isotropic Radiated Power). To optimize the system BOM components for applications using the integrated high-power PA, the “P” devices support an integrated RF switch with a single RF pin capable of transmitting and receiving signals on the same pin.

The CC27xx “R” devices support the regular PA (CC27xxRx) with radio transmit output power up to +10dBm EIRP. Both the CC27xx “R” and the “P” variants support an integrated BALUN with a single-ended 50-ohm RF pin, thereby reducing the number of external components needed for the antenna interface.

## 9 Application, Implementation, and Layout

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Reference Designs

Follow these reference designs very closely when implementing designs using the device.

Special attention must be paid to RF component placement, decoupling capacitors, and DC/DC regulator components, as well as ground connections for all of these.

#### [LP-EM-CC2745R10-Q1 Design Files](#)

The CC2745R10-Q1 LaunchPad Design Files contain detailed schematics and layouts to build application-specific boards using the device.

#### [Sub1GHz and 2.4GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag](#)

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169MHz to 2.4GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868MHz and 915MHz combined with 2.4GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

## 9.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see [Semiconductor and IC Package Thermal Metrics](#).

There are two recommended ways to derive the junction temperature from other measured temperatures:

1. From the package temperature:

$$T_J = \psi_{JT} \times P + T_{\text{case}} \quad (1)$$

2. From the board temperature:

$$T_J = \psi_{JB} \times P + T_{\text{board}} \quad (2)$$

P is the power dissipated from the device and can be calculated by multiplying the current consumption with the supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

### Example:

In this example, we assume a simple use case where the radio is transmitting continuously at 0dBm output power. Let us assume we want to maintain a junction temperature of 105°C and the supply voltage is 3.3V. Using Equation 1, the temperature difference between the top of the case and junction temperature is calculated. To calculate P, look up the current consumption for TX 0dBm at 105°C from the plot [Figure 7-10](#). At 105°C, the current consumption is approximately 9.5mA. This means that P is 9.5mA × 3.3V = 31.35mW.

The maximum case temperature is then calculated as:

$$T_{\text{case}} < T_J - 0.2^{\circ}\text{C}/\text{W} \times 31.35 \text{ mW} = 104.99^{\circ}\text{C} \quad (3)$$

For various application use cases, current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, and so on. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in the [Measuring CC13xx and CC26xx Current Consumption](#) application report.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

### 10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

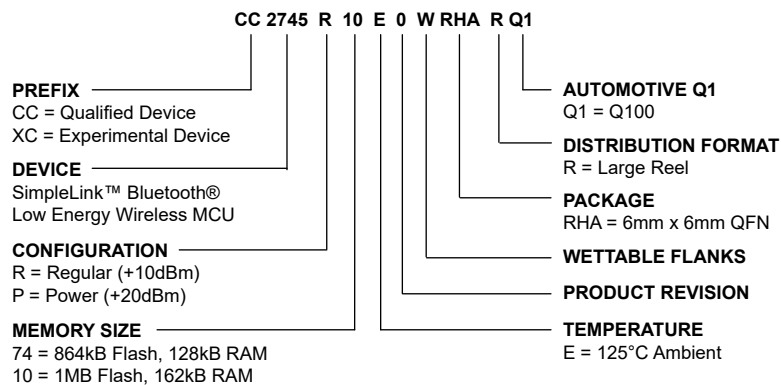
- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use the production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the devices are demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate is still undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RHA*).

For orderable part numbers of devices in the RHA (6mm × 6mm) package type, see the *Package Option Addendum* of this document, the Device Information in [Section 3](#), the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.



**Figure 10-1. Device Nomenclature**

### 10.2 Tools and Software

The CC274xR/P-Q1 devices are supported by a variety of software and hardware development tools.

#### Development Kit [CC2745R10-Q1](#) [LaunchPad™](#) [Development Kit](#)

The CC2745R10-Q1 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2745R10-Q1 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4GHz Bluetooth Low Energy wireless applications for up to +10dBm transmit output power. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display, and more.

## CC2755P10 LaunchPad™ Development Kit

The CC2755P10 LaunchPad™ Development Kit features the SimpleLink Wireless MCU with an integrated High Power Amplifier for Bluetooth Low Energy applications.

It can support up to +20dBm transmit output power.

## Software

### SimpleLink™ low- power software development kit (SDK)

The SimpleLink low-power software development kit (SDK) provides a complete package for the development of wireless applications on the CC27xx family of devices. The SDK includes a comprehensive software package for the CC274xR/P-Q1 device, including the following protocol stacks:

- Bluetooth Low Energy

The SimpleLink low-power SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit <https://www.ti.com/simplelink>.

## Development Tools

### Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface, taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI, resulting in a compelling, feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for Free-RTOS.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

### IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C, and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™, and Segger J-Link™. IAR is also supported out of the box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32KB size-limited version is available through [iar.com](http://iar.com).

### SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generating configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application, through a command line interface to enable more automation, or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests send and receive packets between nodes
- Antenna and radiation tests set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

## CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

### 10.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software, and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more about [Simplelink](#).

### 10.2.2 Software License and Notice

The system ROM firmware includes open-source MCUBoot software licensed under APACHE-2.0. See the following links for more information:

- [MCUBoot Apache 2.0 license terms](#)
- [MCUBoot notice information](#)

### 10.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes, and similar, navigate to the device product folder ([C274xR10-Q1](#)) and ([C2745P10-Q1](#)). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

#### TI Resource Explorer

[TI Resource Explorer](#) Software examples, libraries, executables, and documentation are available for your device and development board.

#### Errata

##### [CC274xR/Px-Q1 Silicon Errata](#)

The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and describes how to recognize a device revision.

#### Application Reports

All application reports for the CC274xR-Q1 devices are found on the device product folder ([CC274xR10-Q1](#)).

All application reports for the CC2745P10-Q1 device are found on the device product folder ([CC2745P10-Q1](#)).

#### Technical Reference Manual (TRM)

##### [CC27xx SimpleLink™ Wireless MCU TRM](#)

The TRM provides a detailed description of all modules and peripherals available in the device family.

### 10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 10.5 Trademarks

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## 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

### TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from June 16, 2025 to November 5, 2025 (from Revision C (June 2025) to Revision D (November 2025))

|                                                                                                       | Page |
|-------------------------------------------------------------------------------------------------------|------|
| • Updated to Bluetooth 6.0 .....                                                                      | 0    |
| • Added the P device variant, CC2745P10-Q1.....                                                       | 1    |
| • Added the P device variant, and updated the device information table.....                           | 2    |
| • Added P device "Power Consumption-Radio Modes (P variant)" table.....                               | 25   |
| • Added P variant specifications in "Bluetooth Low Energy-Transmit (Tx)" table.....                   | 30   |
| • Added China MIIT limits to "Spurious emissions and harmonics" table for both R and P variants ..... | 31   |
| • Added P variant specifications in "2.4GHz Rx/Tx CW" table.....                                      | 31   |
| • Added P device variant current and output power table.....                                          | 45   |
| • Added the P device variant LaunchPad.....                                                           | 63   |
| • Added the P device variant product links.....                                                       | 65   |

### Changes from May 1, 2025 to June 16, 2025 (from Revision B (May 2025) to Revision C (June 2025))

|                                                | Page |
|------------------------------------------------|------|
| • Updated the Device Information table.....    | 2    |
| • Removed "Sensor Controller" Section.....     | 52   |
| • Updated radio description.....               | 53   |
| • Changed temperature calculation example..... | 62   |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CC2744R74E0WRHARQ1</a> | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | CC2744Q1<br>R74     |
| <a href="#">CC2745P10E0WRHARQ1</a> | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | CC2745Q1<br>P10     |
| CC2745R10E0WRHARQ1                 | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | CC2745Q1<br>R10     |
| CC2745R10E0WRHARQ1.A               | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | CC2745Q1<br>R10     |
| CC2745R10E0WRHARQ1.B               | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | CC2745Q1<br>R10     |
| <a href="#">CC2745R10E1WRHARQ1</a> | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | CC2745Q1<br>R10     |
| <a href="#">CC2745R74E0WRHARQ1</a> | Active        | Production           | VQFN (RHA)   40 | 4000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | CC2745Q1<br>R74     |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

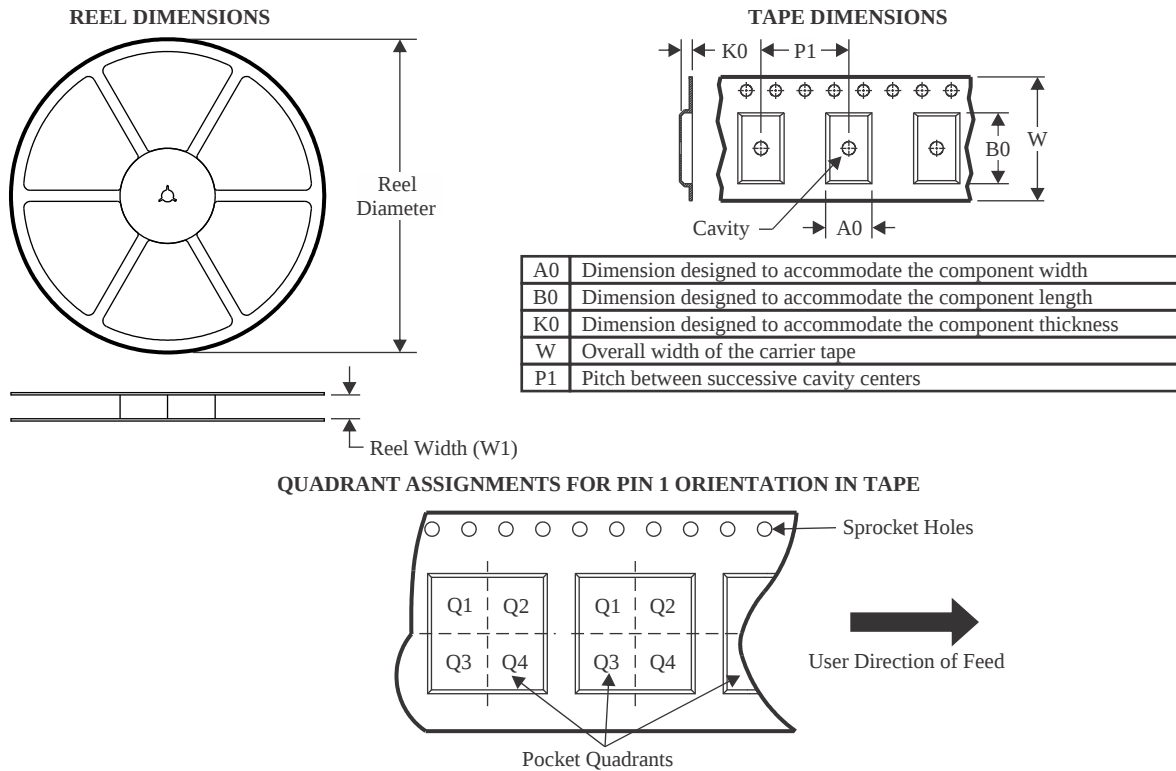
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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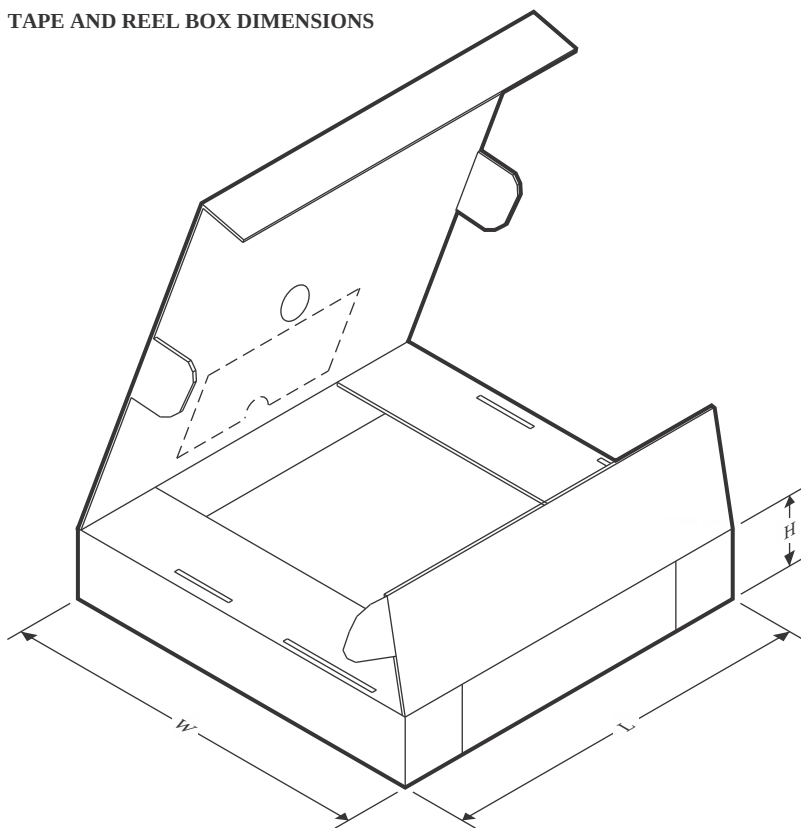
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC2744R74E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CC2744R74E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.25    | 6.25    | 1.05    | 12.0    | 16.0   | Q2            |
| CC2745P10E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CC2745R10E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.25    | 6.25    | 1.05    | 12.0    | 16.0   | Q2            |
| CC2745R10E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CC2745R10E1WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.25    | 6.25    | 1.05    | 12.0    | 16.0   | Q2            |
| CC2745R10E1WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CC2745R74E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.1     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC2744R74E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 367.0       | 367.0      | 35.0        |
| CC2744R74E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 336.6       | 336.6      | 31.8        |
| CC2745P10E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 367.0       | 367.0      | 35.0        |
| CC2745R10E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 336.6       | 336.6      | 31.8        |
| CC2745R10E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 367.0       | 367.0      | 35.0        |
| CC2745R10E1WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 336.6       | 336.6      | 31.8        |
| CC2745R10E1WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 367.0       | 367.0      | 35.0        |
| CC2745R74E0WRHARQ1 | VQFN         | RHA             | 40   | 4000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

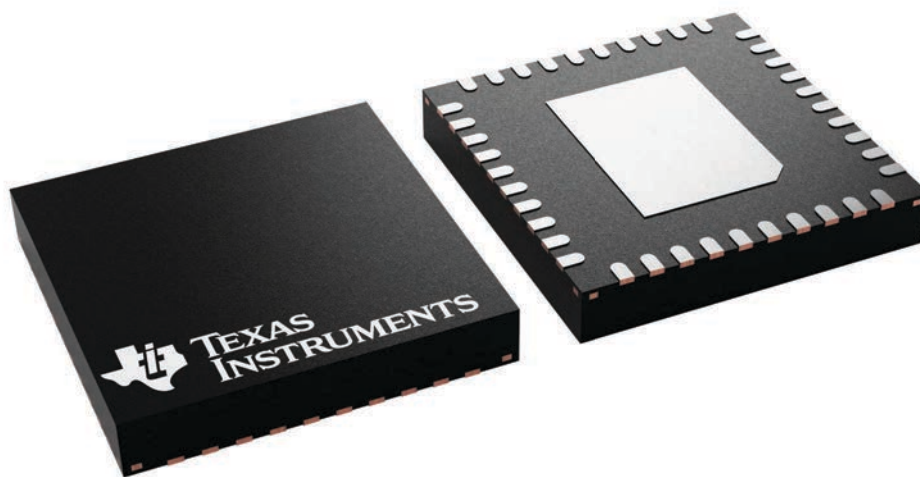
**RHA 40**

**VQFN - 1 mm max height**

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



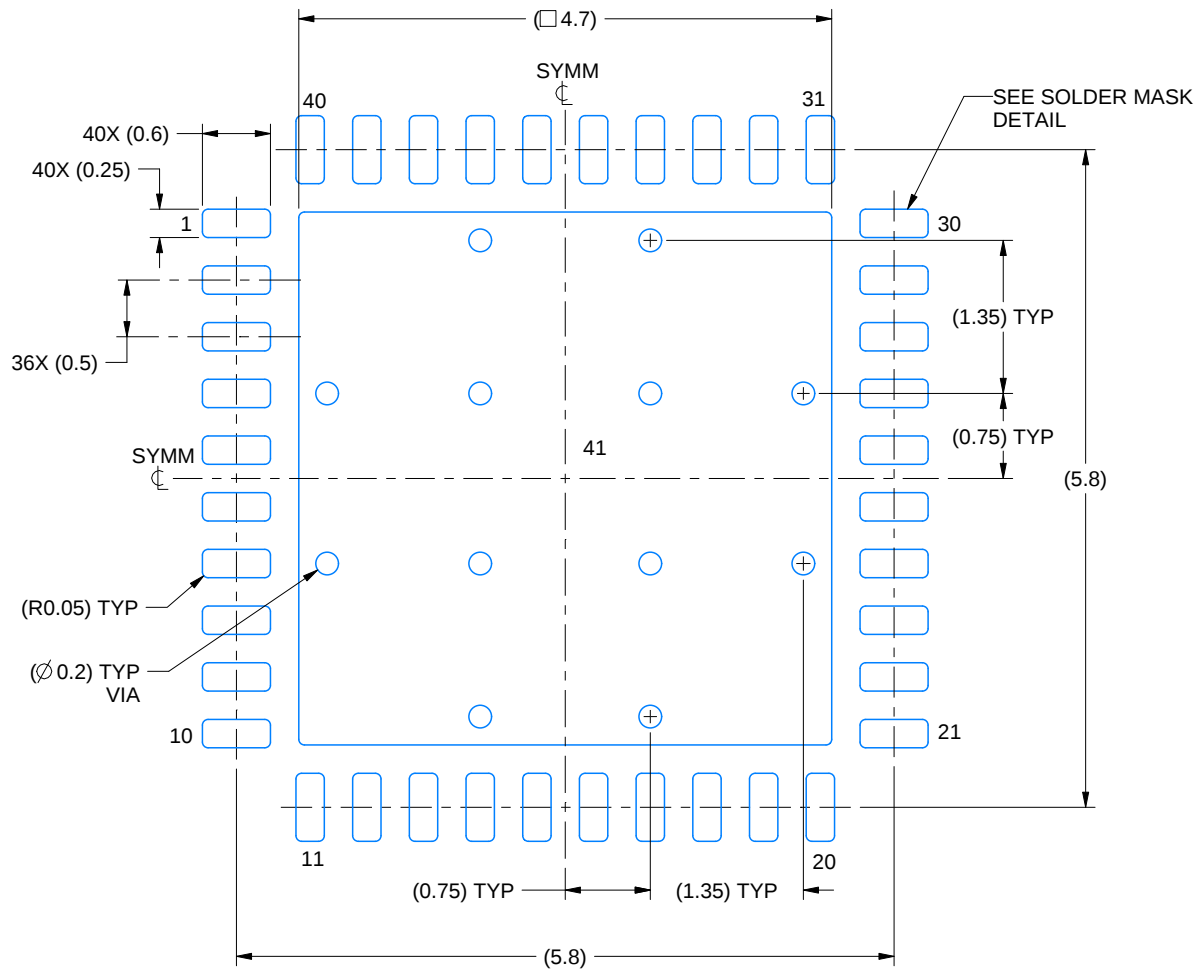
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

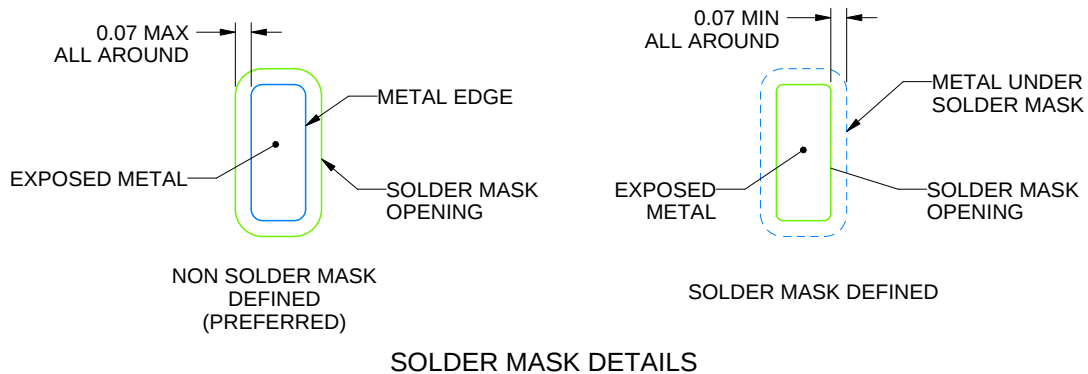
RHA0040T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4230430/A 01/2024

NOTES: (continued)

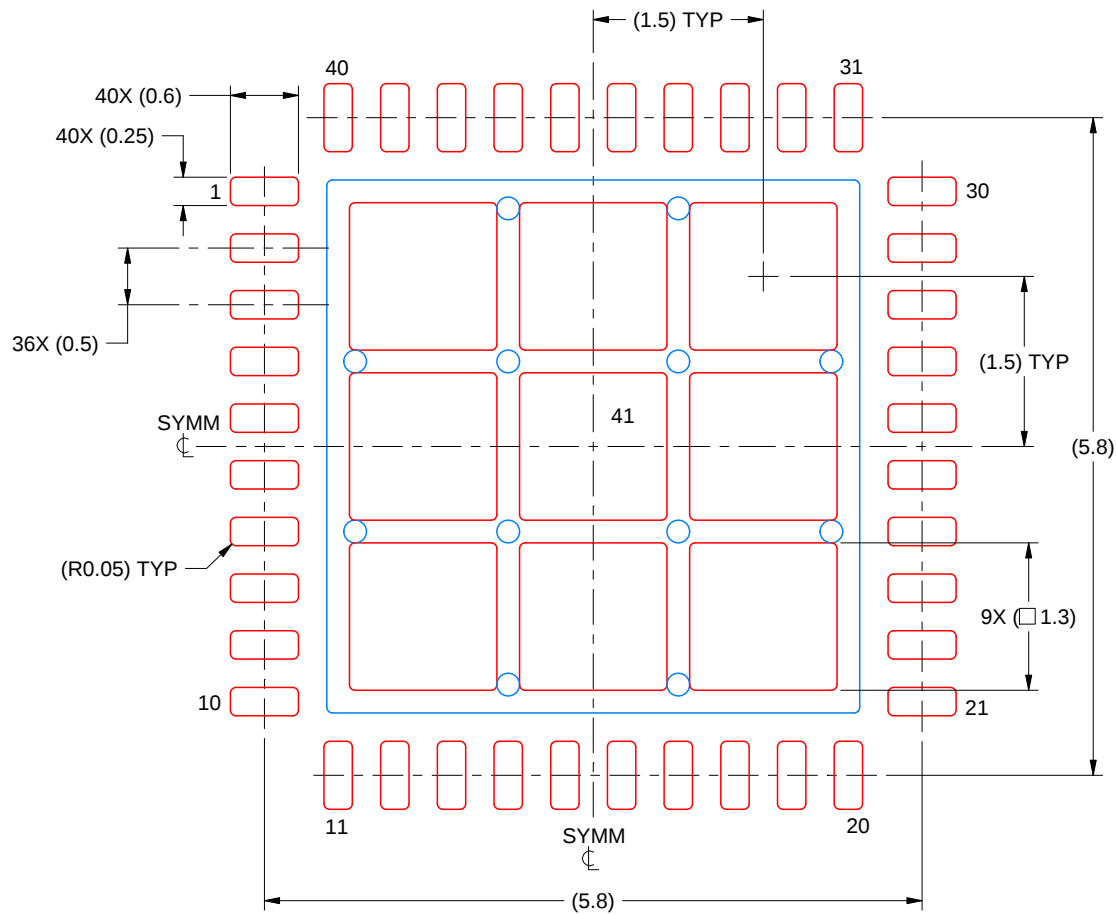
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHA0040T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 15X

EXPOSED PAD 41  
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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