CC3200MOD SimpleLink™ Wi-Fi® and Internet-of-Things Module, Solution, Single-Chip Wireless MCU

1 Features

- CC3200MOD is a Wi-Fi® module consisting of CC3200R1M2RGC single-chip wireless microcontroller (MCU)
- Fully integrated module includes all required clocks, SPI Flash, and passives
- Modular FCC, IC, TELEC, and CE certifications save customer effort, time, and money
- Wi-Fi Alliance members can request certificate transfer of Wi-Fi CERTIFIED™ modules
- 1.27-mm pitch QFM package for easy assembly and low-cost PCB design
- Applications MCU subsystem:
  - Arm® Cortex®-M4 core at 80 MHz
  - Embedded memory:
    - Integrated serial Flash
    - RAM (up to 256KB)
    - Peripheral drivers in ROM
  - Hardware crypto engine for advanced hardware security including:
    - AES, DES, and 3DES
    - SHA and MD5
    - CRC and Checksum
  - 8-Bit parallel camera
  - One Multichannel Audio Serial Port (McASP) interface with support for I2S format
  - One SD (MMC) interface
  - 32-channel Micro Direct Memory Access (µDMA)
  - Two Universal Asynchronous Receivers and Transmitters (UARTs)
  - Two Serial Peripheral Interfaces (SPIs)
  - One Inter-integrated Circuit (I^2C)
  - Four General-Purpose Timers (GPTs)
  - 16-Bit Pulse-Width Modulation (PWM) mode
  - One Watchdog Timer Module
  - 4-channel, 12-bit Analog-to-Digital Converters (ADCs)
  - Up to 25 individually programmable GPIO pins
- Wi-Fi network processor subsystem:
  - 802.11 b/g/n radio, baseband, and medium access control
  - TCP/IP Stack
    - Eight simultaneous TCP, UDP, or RAW sockets
    - Two simultaneous TLS v1.2 or SSL 3.0 sockets
  - ARP, ICMP, DHCP, DNS, and mDNS support
  - HTTP server with built-in programmable HTML page for over-the-network device configuration
  - Powerful crypto engine for fast, secured WLAN connections with 256-bit encryption
  - Station, Access Point, and Wi-Fi Direct® Modes
  - WPA2 personal and enterprise security
  - SimpleLink™ connection manager for managing Wi-Fi security states
  - TX power:
    - 17.0 dBm at 1 DSSS
    - 17.25 dBm at 11 CCK
    - 13.5 dBm at 54 OFDM
  - RX sensitivity:
    - –94.7 dBm at 1 DSSS
    - –87.0 dBm at 11 CCK
    - –73.0 dBm at 54 OFDM
  - Application Throughput:
    - UDP: 16 Mbps
    - TCP: 13 Mbps
- Power-management subsystem:
  - Integrated DC/DC converter with a wide-supply voltage:
    - V_{BAT}: 2.3 to 3.6 V
  - Low-power consumption At 3.6 V:
    - Hibernate with Real-Time Clock (RTC): 7 µA
    - Low-Power Deep Sleep: <275 µA
    - RX Traffic: 59 mA at 54 OFDM
    - TX Traffic: 229 mA at 54 OFDM
  - Package and operating conditions:
    - 1.27-mm pitch, 63-Pin, 20.5-mm × 17.5-mm QFM package for easy assembly and low-cost PCB design
    - Operating temperature range: –20°C to +70°C
- Additional integrated components:
  - 40.0-MHz crystal
  - 32.768-kHz crystal (RTC)
  - 8-Mbit SPI Serial Flash

  - RF filter and passive components
- QFM package:
  - 1.27-mm pitch, 63-pin, 20.5-mm × 17.5-mm QFM package for easy assembly and low-cost PCB design
- Operating temperature:
  - Ambient temperature range: –40°C to +85°C
- Module supports SimpleLink Developer's Ecosystem

2 Applications

- Internet-of-Things (IoT)
- Home appliances
- Building automation
- Security systems
- Smart energy
- Internet Gateway
- Industrial control
- Smart Plug and Metering
- Wireless communications
- Wearables

3 Description

Start your design with the industry's first programmable FCC, IC, CE, and Wi-Fi CERTIFIED™ wireless MCU module with built-in Wi-Fi® connectivity. Created for the IoT, the SimpleLink™ CC3200MOD is a wireless MCU module that integrates an Arm® Cortex®-M4 MCU, allowing customers to develop an entire application with one device. With on-chip Wi-Fi, Internet, and robust security protocols, no prior Wi-Fi experience is required for faster development. The CC3200MOD integrates all required system-level hardware components including clocks, SPI Flash, RF switch, and passives into an QFM package for easy assembly and low-cost PCB design. The CC3200MOD is provided as a complete platform solution including software, sample applications, tools, user and programming guides, reference designs, and the TI E2E™ support community.

The applications MCU subsystem contains an industry-standard Arm® Cortex®-M4 core running at 80 MHz.

The device includes a wide variety of peripherals, including a fast parallel camera interface, I2S, SD/MMC, UART, SPI, I2C, and four-channel ADC. The CC3200 family includes flexible embedded RAM for code and data; ROM with external serial Flash bootloader and peripheral drivers; and SPI Flash for Wi-Fi network processor service packs, Wi-Fi certificates, and credentials.

The Wi-Fi network processor subsystem features a Wi-Fi Internet-on-a chip™ and contains an additional dedicated Arm® MCU that completely off-loads the applications MCU. This subsystem includes an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for fast, secure Internet connections with 256-bit encryption. The CC3200MOD supports station, access point, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security and WPS 2.0. The Wi-Fi Internet-on-a-chip includes embedded TCP/IP and TLS/SSL stacks, HTTP server, and multiple Internet protocols. The power-management subsystem includes integrated DC/DC converters supporting a wide range of supply voltages. This subsystem enables low-power consumption modes, such as the hibernate with RTC mode requiring less than 7 µA of current.

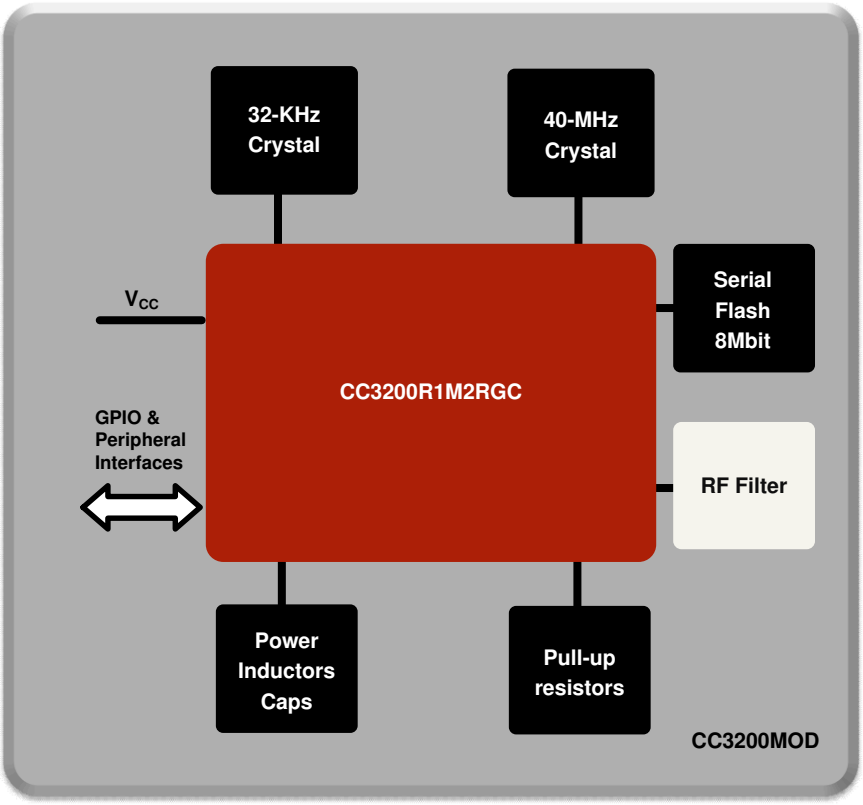
Table 3-1. Module Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC3200MODR1M2AMOB	QFM (63)	20.50 mm × 17.50 mm

(1) For more information, see Section 13.

4 Functional Block Diagrams

Figure 4-1 shows the functional block diagram of the CC3200MOD module.



For 3200MOD module pin multiplexing details, see the *CC3200 SimpleLink™ Wi-Fi® Wireless and Internet-of-Things Solution, a Single-Chip Wireless MCU* data sheet.

Figure 4-1. CC3200MOD Module Functional Block Diagram

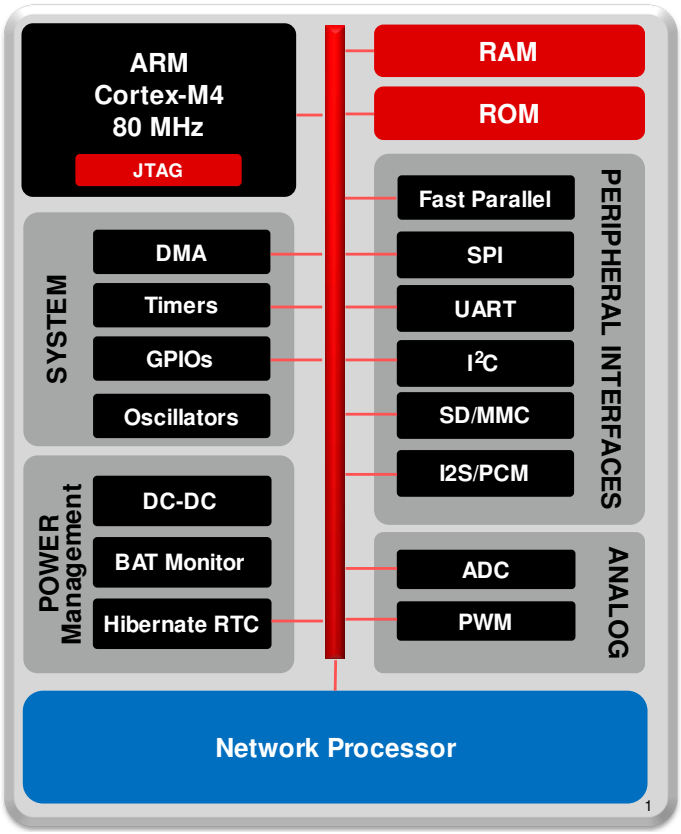


Figure 4-2. CC3200 Hardware Overview

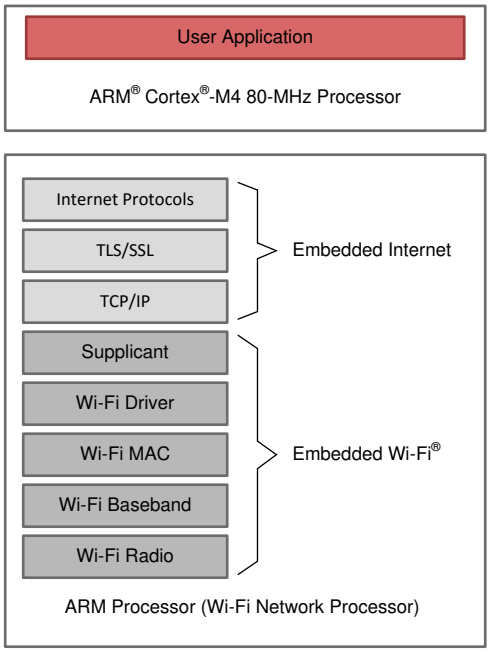


Figure 4-3. CC3200 Software Overview

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 5, 2020 to September 22, 2020 (from Revision B (May 2020) to Revision C (September 2020))	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed SPQ value for CC3200MODR1M2AMOBR throughout Section 13.2	55

6 Device Comparison

Table 6-1 shows the features supported across different CC3x20 modules.

Table 6-1. Device Features Comparison

FEATURE	DEVICE				
	CC3120MOD	**CC3220MODS**	**CC3220MODSF**	**CC3220MODAS**	**CC3220MODASF**
On-board chip	CC3120	CC3220S	CC3220SF	CC3220S	CC3220SF
On-board ANT	No	No	No	Yes	Yes
sFlash	32-Mbit	32-Mbit	32-Mbit	32-Mbit	32-Mbit
Regulatory certifications	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC	FCC, IC, CE, MIC, SRRC
Wi-Fi Alliance® Certification	Yes	Yes	Yes	Yes	Yes
Input voltage	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V	2.3 V to 3.6 V
Package	17.5 mm × 20.5 mm QFM	17.5 mm × 20.5 mm QFM	17.5 mm × 20.5 mm QFM	25.0 mm × 20.5 mm QFM	25.0 mm × 20.5 mm QFM
Operating temperature range	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C	–40°C to +85°C
Classification	Wi-Fi Network Processor	Wireless Microcontroller	Wireless Microcontroller	Wireless Microcontroller	Wireless Microcontroller
Standard	802.11 b/g/n	802.11 b/g/n	802.11 b/g/n	802.11 b/g/n	802.11 b/g/n
Frequency	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
TCP/IP Stack	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6
Sockets	16	16	16	16	16
Integrated MCU	–	Arm® Cortex®-M4 at 80 MHz	Arm® Cortex®-M4 at 80 MHz	Arm® Cortex®-M4 at 80 MHz	Arm® Cortex®-M4 at 80 MHz
ON-CHIP APPLICATION MEMORY					
RAM	–	256KB	256KB	256KB	256KB
Flash	–	–	1MB	–	1MB
PERIPHERALS AND INTERFACES					
Universal Asynchronous Receiver/Transmitter (UART)	1	2	2	2	2
Serial Port Interface (SPI)	1	1	1	1	1
Multichannel Audio Serial Port (McASP)- I2S or PCM	–	2-ch	2-ch	2-ch	2-ch
Inter-Integrated Circuit (I^2C)	–	1	1	1	1
Analog-to-digital converter (ADC)	–	4-ch, 12-bit	4-ch, 12-bit	4-ch, 12-bit	4-ch, 12-bit
Parallel interface (8-bit PI)	–	1	1	1	1
General-purpose timers	–	4	4	4	4
Multimedia card (MMC / SD)	–	1	1	1	1

Table 6-1. Device Features Comparison (continued)

FEATURE	DEVICE				
	CC3120MOD	CC3220MODS	CC3220MODSF	CC3220MODAS	CC3220MODASF
SECURITY FEATURES					
Wi-Fi level of security	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)	WEP, WPS, WPA / WPA2 PSK WPA2 (802.1x)
Secure sockets (SSL v3 or TLS 1.0 / 1.1/ 1.2)	6	6	6	6	6
Additional networking security	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key	Unique Device Identity Trusted Root-Certificate Catalog TI Root-of-Trust Public key
Hardware acceleration	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines	Hardware Crypto Engines
Secure boot	–	Yes	Yes	Yes	Yes
Enhanced Application Level Security	–	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming

6.1 Related Products

For information about other devices in this family of products or related products see the links below.

The SimpleLink™ MCU Portfolio	offers a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi®, Bluetooth® low energy, Sub-1GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications.
Companion Products	Review products that are frequently purchased or used in conjunction with this product.
SimpleLink™ Wi-Fi® Family	The SimpleLink Wi-Fi Family offers several Internet-on-a chip solutions, which address the need of battery operated, security enabled products. Texas instruments offers a single chip wireless microcontroller and a wireless network processor which can be paired with any MCU, to allow developers to design new wi-fi products, or upgrade existing products with wi-fi capabilities.
BoosterPack™ Plug-In Modules	BoosterPack™ Plug-In Modules extend the functionality of TI LaunchPad Kit. Application specific BoosterPack Plug in modules allow you to explore a broad range of applications, including capacitive touch, wireless sensing, LED Lighting control, and more. Stack multiple BoosterPack modules onto a single LaunchPad kit to further enhance the functionality of your design.
Reference Designs for CC3200 and CC3220 Devices	TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.
SimpleLink™ Wi-Fi® CC3220 SDK	The SimpleLink Wi-Fi CC3220 SDK contains drivers for the CC3220 programmable MCU, sample applications, and documentation required to start development with CC3220 solutions.

7 Terminal Configuration and Functions

7.1 CC3200MOD Pin Diagram

Figure 7-1 shows the pin diagram for the CC3200MOD module.

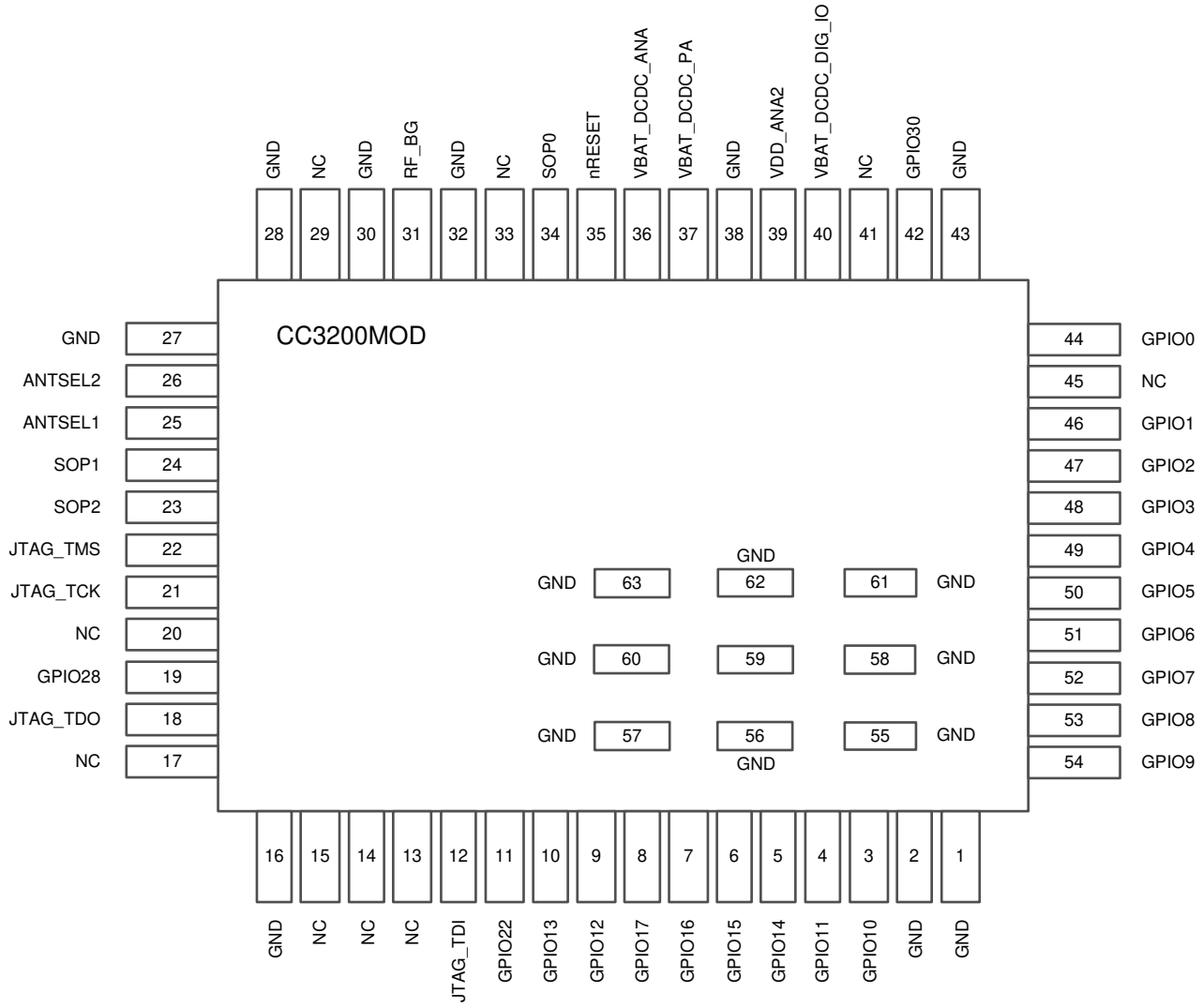


Figure 7-1 shows the approximate location of pins on the module. For the actual mechanical diagram, see Section 13.

Figure 7-1. CC3200MOD Pin Diagram Bottom View

7.2 Pin Attributes

Section 7.2.1 lists the pin descriptions of the CC3200MOD module. *DEVICE PIN NO.* refers to the pin number of the VQFN device, CC3200, which is stated here because the VQFN pin is referred to in the software design kit (SDK).

7.2.1 Module Pin Attributes

MODULE PIN		TYPE	DEVICE PIN NO.	MODULE PIN DESCRIPTION
NO.	NAME			
1	GND	–	–	Ground
2	GND	–	–	Ground
3	GPIO10	I/O	1	GPIO(1)
4	GPIO11	I/O	2	GPIO(1)
5	GPIO14	I/O	5	GPIO(1)
6	GPIO15	I/O	6	GPIO(1)
7	GPIO16	I/O	7	GPIO(1)
8	GPIO17	I/O	8	GPIO(1)
9	GPIO12	I/O	3	GPIO(1)
10	GPIO13	I/O	4	GPIO(1)
11	GPIO22	I/O	15	GPIO(1)
12	JTAG_TDI	I/O	16	GPIO(1)
13	NC	–	13	Reserved for TI
14	NC	–	14	Reserved for TI
15	NC	–	11	Reserved for TI
16	GND	–	–	Ground
17	NC	–	12	Reserved for TI
18	JTAG_TDO	I/O	17	GPIO(1)
19	GPIO28	I/O	18	GPIO(1)
20	NC	–	23	Unused. Do not connect.
21	JTAG_TCK	I/O	19	JTAG TCK input. Needs 100-kΩ pulldown resistor to ground. Not adding the 100K resistor can cause higher current in LPDS mode.(1)
22	JTAG_TMS	I/O	20	JTAG TMS input. Leave unconnected if not used on product.(1)
23	SOP2	–	21	Add 2.7-kΩ pulldown resistor to ground needed for functional mode. Connect to test point to be pulled high for entering the UART load mode for flashing.
24	SOP1	–	34	Reserved. Do not connect.
25	ANTSEL1	I/O	29	Antenna selection control(1)
26	ANTSEL2	I/O	30	Antenna selection control(1)
27, 28	GND	-	–	Ground
29	NC	-	27, 28	Reserved for TI
30	GND	-	–	Ground
31	RF_BG	I/O	31	2.4-GHz RF input/output
32	GND	–	–	Ground
33	NC	–	38	Reserved for TI
34	SOP0	–	35	Optional 10-kΩ pullup if user chooses to use SWD debug mode instead of 4-wire JTAG
35	nRESET	I	32	Power on reset. Does not require external RC circuit
36	VBAT_DCDC_ANA	–	37	Power supply for the device, can be connected to battery (2.3 V to 3.6 V)

MODULE PIN		TYPE	DEVICE PIN NO.	MODULE PIN DESCRIPTION
NO.	NAME			
37	VBAT_DCDC_PA	–	39	Power supply for the device, can be connected to battery (2.3 V to 3.6 V)
38	GND	–	–	Ground
39	NC	–	47	Leave unconnected
40	VBAT_DCDC_DIG_IO	–	10, 44, 54	Power supply for the device, can be connected to battery (2.3 V to 3.6 V)
41	NC	–	25, 36, 48	Reserved for TI
42	GPIO30	I/O	53	GPIO(1)
43	GND	–	–	Ground
44	GPIO0	I/O	50	GPIO(1)
45	NC	–	51	Reserved for TI
46	GPIO1	I/O	55	GPIO(1)
47	GPIO2	I/O	57	GPIO(1)
48	GPIO3	I/O	58	GPIO(1)
49	GPIO4	I/O	59	GPIO(1)
50	GPIO5	I/O	60	GPIO(1)
51	GPIO6	I/O	61	GPIO(1)
52	GPIO7	I/O	62	GPIO(1)
53	GPIO8	I/O	63	GPIO(1)
54	GPIO9	I/O	64	GPIO(1)
55, 56, 57, 58, 59, 60, 61, 62, 63	GND	–	–	Thermal Ground

(1) For pin multiplexing details, refer to the *CC3200 SimpleLink™ Wi-Fi® Wireless and Internet-of-Things Solution, a Single-Chip Wireless MCU* data sheet.

7.3 Pin Attributes and Pin Multiplexing

The module makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at module reset) and register control.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used. Table 7-1 describes the general pin attributes and presents an overview of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers. The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. Drive strength is individually configurable for each pin.
- All I/Os support 10-µA pullup and pulldown resistors.
- These pulls are not active and all of the I/Os remain floating while the device is in Hibernate state.
- The VIO and VBAT supply must be tied together at all times.
- All digital I/Os are nonfail-safe.

Table 7-1. Pin Multiplexing

GENERAL PIN ATTRIBUTES					FUNCTION					PAD STATES		
PIN ALIAS	USE	SELECT AS WAKEUP SOURCE	CONFIG ADDL ANALOG MUX	MUXED WITH JTAG	DIG. PIN MUX CONFIG REG	DIG. PIN MUX CONFIG MODE VALUE	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL DIRECTION	LPDS[1]	HIB[2]	nRESET = 0
GPIO10	I/O	No	No	No	GPIO_PAD_CONFIG_10 (0x4402 E0C8)	0	GPIO10	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						1	I2C_SCL	I2C Clock	O (Open Drain)	Hi-Z		
						3	GT_PWM06	Pulse-Width Modulated O/P	O	Hi-Z		
						7	UART1_TX	UART TX Data	O	1		
						6	SDCARD_CLK	SD Card Clock	O	0		
						12	GT_CCP01	Timer Capture Port	I	Hi-Z		
GPIO11	I/O	Yes	No	No	GPIO_PAD_CONFIG_11 (0x4402 E0CC)	0	GPIO11	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						1	I2C_SDA	I2C Data	I/O (Open Drain)	Hi-Z		
						3	GT_PWM07	Pulse-Width Modulated O/P	O	Hi-Z		
						4	pXCLK (XVCLK)	Free Clock To Parallel Camera	O	0		
						6	SDCARD_CMD	SD Card Command Line	I/O	Hi-Z		
						7	UART1_RX	UART RX Data	I	Hi-Z		
						12	GT_CCP02	Timer Capture Port	I	Hi-Z		
						13	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
GPIO12	I/O	No	No	No	GPIO_PAD_CONFIG_12 (0x4402 E0D0)	0	GPIO12	General Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						3	McACLK	I2S Audio Port Clock O	O	Hi-Z		
						4	pVS (VSYNC)	Parallel Camera Vertical Sync	I	Hi-Z		
						5	I2C_SCL	I2C Clock	I/O (Open Drain)	Hi-Z		

Table 7-1. Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES					FUNCTION					PAD STATES		
PIN ALIAS	USE	SELECT AS WAKEUP SOURCE	CONFIG ADDL ANALOG MUX	MUXED WITH JTAG	DIG. PIN MUX CONFIG REG	DIG. PIN MUX CONFIG MODE VALUE	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL DIRECTION	LPDS[1]	HIB[2]	nRESET = 0
						7	UART0_TX	UART0 TX Data	O	1		
						12	GT_CCP03	Timer Capture Port	I	Hi-Z		
GPIO13	I/O	Yes	No	No	GPIO_PAD_CONFIG_13 (0x4402 E0D4)	0	GPIO13	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	I2C_SDA	I2C Data	I/O (Open Drain)			
						4	pHS (HSYNC)	Parallel Camera Horizontal Sync	I			
						7	UART0_RX	UART0 RX Data	I			
						12	GT_CCP04	Timer Capture Port	I			
GPIO14	I/O		No	No	GPIO_PAD_CONFIG_14 (0x4402 E0D8)	0	GPIO14	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	I2C_SCL	I2C Clock	I/O (Open Drain)			
						7	GSPI_CLK	General SPI Clock	I/O			
						4	pDATA8 (CAM_D4)	Parallel Camera Data Bit 4	I			
						12	GT_CCP05	Timer Capture Port	I			
GPIO15	I/O		No	No	GPIO_PAD_CONFIG_15 (0x4402 E0DC)	0	GPIO15	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	I2C_SDA	I2C Data	I/O (Open Drain)			
						7	GSPI_MISO	General SPI MISO	I/O			
						4	pDATA9 (CAM_D5)	Parallel Camera Data Bit 5	I			
						13	GT_CCP06	Timer Capture Port	I			
						8	SDCARD_ DATA0	SD Card Data	I/O			
GPIO16	I/O		No	No	GPIO_PAD_CONFIG_16 (0x4402 E0E0)	0	GPIO16	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
										Hi-Z		
										Hi-Z		
						7	GSPI_MOSI	General SPI MOSI	I/O	Hi-Z		
						4	pDATA10 (CAM_D6)	Parallel Camera Data Bit 6	I	Hi-Z		
						5	UART1_TX	UART1 TX Data	O	1		
						13	GT_CCP07	Timer Capture Port	I	Hi-Z		
						8	SDCARD_CLK	SD Card Clock	O	O		
GPIO17	I/O	Wake-Up Source	No	No	GPIO_PAD_CONFIG_17 (0x4402 E0E4)	0	GPIO17	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	UART1_RX	UART1 RX Data	I			
						7	GSPI_CS	General SPI Chip Select	I/O			
						4	pDATA11 (CAM_D7)	Parallel Camera Data Bit 7	I			

Table 7-1. Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES					FUNCTION					PAD STATES		
PIN ALIAS	USE	SELECT AS WAKEUP SOURCE	CONFIG ADDL ANALOG MUX	MUXED WITH JTAG	DIG. PIN MUX CONFIG REG	DIG. PIN MUX CONFIG MODE VALUE	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL DIRECTION	LPDS[1]	HIB[2]	nRESET = 0
						8	SDCARD_ CMD	SD Card Command Line	I/O			
GPIO22	I/O	No	No	No	GPIO_PAD_CONFIG_22 (0x4402 E0F8)	0	GPIO22	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						7	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
						5	GT_CCP04	Timer Capture Port	I			
TDI	I/O	No	No	MUXed with JTAG TDI	GPIO_PAD_CONFIG_23 (0x4402 E0FC)	1	TDI	JTAG TDI. Reset Default Pinout.	I	Hi-Z	Hi-Z	Hi-Z
						0	GPIO23	General-Purpose I/O	I/O			
						2	UART1_TX	UART1 TX Data	O	1		
						9	I2C_SCL	I2C Clock	I/O (Open Drain)	Hi-Z		
TDO	I/O	Wake-Up Source	No	MUXed with JTAG TDO	GPIO_PAD_CONFIG_ 24 (0x4402 E100)	1	TDO	JTAG TDO. Reset Default Pinout.	O	Hi-Z	Hi-Z	Hi-Z
						0	GPIO24	General-Purpose I/O	I/O			
						5	PWM0	Pulse Width Modulated O/P	O			
						2	UART1_RX	UART1 RX Data	I			
						9	I2C_SDA	I2C Data	I/O (Open Drain)			
						4	GT_CCP06	Timer Capture Port	I			
						6	McAFSX	I2S Audio Port Frame Sync	O			
GPIO28	I/O		No		GPIO_PAD_CONFIG_ 28 (0x4402 E110)	0	GPIO28	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
TCK	I/O	No	No	MUXed with JTAG/ SWD-TCK		1	TCK	JTAG/SWD TCK Reset Default Pinout	I	Hi-Z	Hi-Z	Hi-Z
						8	GT_PWM03	Pulse Width Modulated O/P	O			
TMS	I/O	No	No	MUXed with JTAG/ SWD-TMSC	GPIO_PAD_CONFIG_ 29 (0x4402 E114)	1	TMS	JATG/SWD TMS Reset Default Pinout	I/O	Hi-Z	Hi-Z	Hi-Z
						0	GPIO29	General-Purpose I/O				
SOP2	O Only	No	No	No	GPIO_PAD_CONFIG_ 25 (0x4402 E104)	0	GPIO25	General-Purpose I/O	O	Hi-Z	Driven Low	Hi-Z
						9	GT_PWM02	Pulse Width Modulated O/P	O	Hi-Z		
						2	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
						See [5]	SOP2	Sense-On-Power 2	I			
ANTSEL1	O Only	No	User config not required [6]	No	GPIO_PAD_CONFIG_26 (0x4402 E108)	0	ANTSEL1[3]	Antenna Selection Control	O	Hi-Z	Hi-Z	Hi-Z

Table 7-1. Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES					FUNCTION					PAD STATES		
PIN ALIAS	USE	SELECT AS WAKEUP SOURCE	CONFIG ADDL ANALOG MUX	MUXED WITH JTAG	DIG. PIN MUX CONFIG REG	DIG. PIN MUX CONFIG MODE VALUE	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL DIRECTION	LPDS(1)	HIB(2)	nRESET = 0
ANTSEL2	O Only	No	User config not required (6)	No	GPIO_PAD_CONFIG_27 (0x4402 E10C)	0	ANTSEL2(3)	Antenna Selection Control	O	Hi-Z	Hi-Z	Hi-Z
SOP1	Config Sense	N/A	N/A	N/A	N/A		SOP1	Sense On Power 1				
SOP0	Config Sense	N/A	N/A	N/A	N/A		SOP0	Sense On Power 0				
GPIO0	I/O	No	User config not required (6)	No	GPIO_PAD_CONFIG_0 (0x4402 E0A0)	0	GPIO0	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						12	UART0_CTS	UART0 Clear To Send Input (Active Low)	I	Hi-Z	Hi-Z	Hi-Z
						6	McAXR1	I2S Audio Port Data 1 (RX or TX)	I/O	Hi-Z		
						7	GT_CCP00	Timer Capture Port	I	Hi-Z		
						9	GSPI_CS	General SPI Chip Select	I/O	Hi-Z		
						10	UART1_RTS	UART1 Request To Send O (Active Low)	O	1		
						3	UART0_RTS	UART0 Request To Send O (Active Low)	O	1		
						4	McAXR0	I2S Audio Port Data 0 (RX or TX)	I/O	Hi-Z		
GPIO30	I/O	No	User config not required (6)	No	GPIO_PAD_CONFIG_30 (0x4402 E118)	0	GPIO30	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						9	UART0_TX	UART0 TX Data	O	1		
						2	McACLK	I2S Audio Port Clock O	O	Hi-Z		
						3	McAFSX	I2S Audio Port Frame Sync	O	Hi-Z		
						4	GT_CCP05	Timer Capture Port	I	Hi-Z		
						7	GSPI_MISO	General SPI MISO	I/O	Hi-Z		
GPIO1	I/O	No	No	No	GPIO_PAD_CONFIG_1 (0x4402 E0A4)	0	GPIO1	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						3	UART0_TX	UART0 TX Data	O	1		
						4	pCLK (PIXCLK)	Pixel Clock From Parallel Camera Sensor	I	Hi-Z		
						6	UART1_TX	UART1 TX Data	O	1		
						7	GT_CCP01	Timer Capture Port	I	Hi-Z		
GPIO2	Analog Input (up to 1.8 V), Digital I/O	Wake-Up Source	See (7)	No	GPIO_PAD_CONFIG_2 (0x4402 E0A8)	See (4)	ADC_CH0	ADC Channel 0 Input (1.5-V max)	I		Hi-Z	Hi-Z
						0	GPIO2	General-Purpose I/O	I/O	Hi-Z		
						3	UART0_RX	UART0 RX Data	I	Hi-Z		
						6	UART1_RX	UART1 RX Data	I	Hi-Z		
						7	GT_CCP02	Timer Capture Port	I	Hi-Z		
GPIO3	Analog Input (up	No	See (7)	No	GPIO_PAD_CONFIG_3 (0x4402 E0AC)	See (4)	ADC_CH1	ADC Channel 1 Input (1.5-V max)	I		Hi-Z	Hi-Z

Table 7-1. Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES					FUNCTION					PAD STATES		
PIN ALIAS	USE	SELECT AS WAKEUP SOURCE	CONFIG ADDL ANALOG MUX	MUXED WITH JTAG	DIG. PIN MUX CONFIG REG	DIG. PIN MUX CONFIG MODE VALUE	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL DIRECTION	LPDS[1]	HIB[2]	nRESET = 0
	to 1.8 V), Digital I/O					0	GPIO3	General-Purpose I/O	I/O	Hi-Z		
						6	UART1_TX	UART1 TX Data	O	1		
						4	pDATA7 (CAM_D3)	Parallel Camera Data Bit 3	I	Hi-Z		
GPIO4	Analog Input (up to 1.8 V), Digital I/O	Wake-up Source	See [7]	No	GPIO_PAD_CONFIG_4 (0x4402 E0B0)	See [4]	ADC_CH2	ADC Channel 2 Input (1.5-V max)	I		Hi-Z	Hi-Z
						0	GPIO4	General-Purpose I/O	I/O	Hi-Z		
						6	UART1_RX	UART1 RX Data	I	Hi-Z		
						4	pDATA6 (CAM_D2)	Parallel Camera Data Bit 2	I	Hi-Z		
GPIO5	Analog Input (up to 1.8 V), Digital I/O	No	See [7]	No	GPIO_PAD_CONFIG_5 (0x4402 E0B4)	See [4]	ADC_CH3	ADC Channel 3 Input (1.5-V max)	I		Hi-Z	Hi-Z
						0	GPIO5	General-Purpose I/O	I/O	Hi-Z		
						4	pDATA5 (CAM_D1)	Parallel Camera Data Bit 1	I	Hi-Z		
						6	McAXR1	I2S Audio Port Data 1 (RX or TX)	I/O	Hi-Z		
						7	GT_CCP05	Timer Capture Port	I	Hi-Z		
GPIO6	No	No	No	No	GPIO_PAD_CONFIG_6 (0x4402 E0B8)	0	GPIO6	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						5	UART0_RTS	UART0 Request To Send O (Active Low)	O	1		
						4	pDATA4 (CAM_D0)	Parallel Camera Data Bit 0	I	Hi-Z		
						3	UART1_CTS	UART1 Clear To Send Input (Active Low)	I	Hi-Z		
						6	UART0_CTS	UART0 Clear To Send Input (Active Low)	I	Hi-Z		
						7	GT_CCP06	Timer Capture Port	I	Hi-Z		
GPIO7	I/O	No	No	No	GPIO_PAD_CONFIG_7 (0x4402 E0BC)	0	GPIO7	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						13	McACLKX	I2S Audio Port Clock O	O	Hi-Z		
						3	UART1_RTS	UART1 Request To Send O (Active Low)	O	1		
						10	UART0_RTS	UART0 Request To Send O (Active Low)	O	1		
						11	UART0_TX	UART0 TX Data	O	1		
GPIO8	I/O	No	No	No	GPIO_PAD_CONFIG_8 (0x4402 E0C0)	0	GPIO8	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z
						6	SDCARD_IRQ	Interrupt from SD Card (Future support)	I			
						7	McAFSX	I2S Audio Port Frame Sync	O			
						12	GT_CCP06	Timer Capture Port	I			
GPIO9	I/O	No	No	No	GPIO_PAD_CONFIG_9	0	GPIO9	General-Purpose I/O	I/O	Hi-Z	Hi-Z	Hi-Z

Table 7-1. Pin Multiplexing (continued)

GENERAL PIN ATTRIBUTES					FUNCTION					PAD STATES		
PIN ALIAS	USE	SELECT AS WAKEUP SOURCE	CONFIG ADDL ANALOG MUX	MUXED WITH JTAG	DIG. PIN MUX CONFIG REG	DIG. PIN MUX CONFIG MODE VALUE	SIGNAL NAME	SIGNAL DESCRIPTION	SIGNAL DIRECTION	LPDS(1)	HIB(2)	nRESET = 0
					(0x4402 E0C4)	3	GT_PWM05	Pulse Width Modulated O/P	O			
						6	SDCARD_ DATA0	SD Cad Data	I/O			
						7	McAXR0	I2S Audio Port Data (Rx or Tx)	I/O			
						12	GT_CCP00	Timer Capture Port	I			

(1) LPDS state: The state of unused I/Os is Hi-Z. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
(2) Hibernate mode: The state of the I/Os is Hi-Z. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
(3) To minimize leakage in some serial Flash vendors during LPDS, TI recommends that the user application always enables internal weak pulldowns on FLASH_SPI_DIN, FLASH_SPI_DOUT, and FLASH_SPI_CLK pins.
(4) For details on proper use, see *Drive Strength and Reset States for Analog-Digital Multiplexed Pins*.
(5) Pin is one of three that must have a passive pullup or pulldown resistor onboard to configure the chip hardware power-up mode. For this reason, the pin must be output only when used for digital functions.
(6) Device firmware automatically enables the digital path during ROM boot.
(7) Requires user configuration to enable the analog switch of the ADC channel. (Switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

7.4 Recommended Pin Multiplexing Configurations

Table 7-2 lists the recommended pin multiplexing configurations.

Table 7-2. Recommended Pin Multiplexing Configurations

CC3220MODx RECOMMENDED PINOUT GROUPING USE – EXAMPLES(1)											
	Home Security High-end Toys	Wi-Fi Audio ++ Industrial	Sensor-Tag	Home Security Toys	Wi-Fi Audio ++ Industrial	Wi-Fi Remote w/ 7×7 keypad and audio	Sensor Door-Lock Fire-Alarm Toys w/o Cam	Industrial Home Appliances	Industrial Home Appliances Smart-Plug	Industrial Home Appliances	GPIOs
	Cam + I2S (TX or RX) + I2C + SPI + SWD + UART-TX + (App Logger) 2 GPIO + 1 PWM + *4 overlaid wake up from Hib	I2S (TX and RX) + 1-Ch ADC + 1× 4-wire UART + 1× 2-wire UART + 1-bit SD Card + SPI + I2C + SWD + 3 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib	I2S (TX and RX) + 2-Ch ADC + 2-wire UART + SPI + I2C + SWD + 2 PMW + 6 GPIO + 3 GPIO with Wake-From-Hib	Cam + I2S (TX or RX) + I2C + SWD + UART-TX + (App Logger) 4 GPIO + 1 PWM + *4 overlaid wake up from HIB	I2S (TX and RX) + 1 Ch ADC + 2× 2-wire UART + 1-bit SD Card + SPI + I2C + SWD + 4 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib	I2S (TX and RX) + 1-Ch ADC + UART (TX Only) I2C + SWD + 15 GPIO + 1 PWM + 1 GPIO with Wake-From-Hib	I2S (TX or RX) + 2-Ch ADC + 2-wire UART + SPI + I2C + 3 PMW + 3 GPIO with Wake-From-Hib + 5 GPIO SWD +	4-Ch ADC + 1× 4-wire UART + 1× 2-wire UART + SPI + I2C + SWD + 1 PWM + 6 GPIO + 1 GPIO with Wake-From-Hib	3-Ch ADC + 2-wire UART + SPI + I2C + SWD + 3 PWM + 9 GPIO + 2 GPIO with Wake-From-Hib	2-Ch ADC + 2-wire UART + I2C + SWD + 3 PWM + 11 GPIO + 5 GPIO with Wake-From-Hib	
Pin	**Pinout 11**	**Pinout 10**	**Pinout 9**	**Pinout 8**	**Pinout 7**	**Pinout 6**	**Pinout 5**	**Pinout 4**	**Pinout 3**	**Pinout 2**	**Pinout 1**
GPIO_30	GSPI-MISO	MCASP-ACLKX	MCASP-ACLKX	GPIO_30	GPIO_30	GPIO_30	GPIO_30	UART0-TX	GPIO_30	UART0-TX	GPIO_30
GPIO_0	GSPI-CS	McASP-D1 (RX)	McASP-D1	McASP-D1	McASP-D1	McASP-D1	McASP-D1	UART0-CTS	GPIO_0	GPIO_0	GPIO_0
GPIO_1	pCLK (PIXCLK)	UART0-TX	UART0-TX	PIXCLK	UART0-TX	UART0-TX	UART0-TX	GPIO-1	UART0-TX	GPIO_1	GPIO_1
GPIO_2	(wake) GPIO2	UART0-RX	UART0-RX	(wake) GPIO2	UART0-RX	GPIO_2	UART0-RX	ADC-0	UART0-RX	(wake) GPIO_2	(wake) GPIO_2
GPIO_3	pDATA7 (D3)	UART1-TX	ADC-CH1	pDATA7 (D3)	UART1-TX	GPIO_3	ADC-1	ADC-1	ADC-1	ADC-1	GPIO_3
GPIO_4	pDATA6 (D2)	UART1-RX	(wake) GPIO_4	pDATA6 (D2)	UART1-RX	GPIO_4	(wake) GPIO_4	ADC-2	ADC-2	(wake) GPIO_4	(wake) GPIO_4
GPIO_5	pDATA5 (D1)	ADC-3	ADC-3	pDATA5 (D1)	ADC-3	ADC-3	ADC-3	ADC-3	ADC-3	ADC-3	GPIO_5
GPIO_6	pDATA4 (D0)	UART1-CTS	GPIO_6	pDATA4 (D0)	GPIO_6	GPIO_6	GPIO_6	UART0-RTS	GPIO_6	GPIO_6	GPIO_6
GPIO_7	McASP-ACLKX	UART1-RTS	GPIO_7	McASP-ACLKX	McASP-ACLKX	McASP-ACLKX	McASP-ACLKX	GPIO_7	GPIO_7	GPIO_7	GPIO_7
GPIO_8	McASP-AFSX	SDCARD-IRQ	McASP-AFSX	McASP-AFSX	SDCARD-IRQ	GPIO_8	GPIO_8	GPIO_8	GPIO_8	GPIO_8	GPIO_8
GPIO_9	McASP-D0	SDCARD-DATA	GT_PWM 5	McASP-D0	SDCARD-DATA	GPIO_9	GT_PWM 5	GT_PWM 5	GT_PWM 5	GT_PWM 5	GPIO_9
GPIO_10	UART1-TX	SDCARD-CLK	GPIO_10	UART1-TX	SDCARD-CLK	GPIO_10	GT_PWM 6	UART1-TX	GT_PWM 6	GPIO_10	GPIO_10
GPIO_11	(wake) pXCLK (XVCLK)	SDCARD-CMD	(wake) GPIO_11	(wake) pXCLK (XVCLK)	SDCARD-CMD	GPIO_11	(wake) GPIO_11	UART1-RX	(wake) GPIO_11	(wake) GPIO_11	(wake) GPIO_11
GPIO_12	pVS (VSYNC)	I2C-SCL	I2C-SCL	pVS (VSYNC)	I2C-SCL	GPIO_12	I2C-SCL	I2C-SCL	I2C-SCL	GPIO_12	GPIO_12

Table 7-2. Recommended Pin Multiplexing Configurations (continued)

CC3220MODx RECOMMENDED PINOUT GROUPING USE – EXAMPLES[1]											
GPIO_13	(wake) pHS (HSYNC)	I2C-SDA	I2C-SDA	(wake) pHS (HSYNC)	I2C-SDA	GPIO_13	I2C-SDA	I2C-SDA	I2C-SDA	(wake) GPIO_13	(wake) GPIO_13
GPIO_14	pDATA8 (D4)	GSPI-CLK	GSPI-CLK	pDATA8 (D4)	GSPI-CLK	I2C-SCL	GSPI-CLK	GSPI-CLK	GSPI-CLK	I2C-SCL	GPIO_14
GPIO_15	pDATA9 (D5)	GSPI-MISO	GSPI-MISO	pDATA9 (D5)	GSPI-MISO	I2C-SDA	GSPI-MISO	GSPI-MISO	GSPI-MISO	I2C-SDA	GPIO_15
GPIO_16	pDATA10 (D6)	GSPI-MOSI	GSPI-MOSI	pDATA10 (D6)	GSPI-MOSI	GPIO_16	GSPI-MOSI	GSPI-MOSI	GSPI-MOSI	GPIO_16	GPIO_16
GPIO_17	(wake) pDATA11 (D7)	GSPI-CS	GSPI-CS	(wake) pDATA11 (D7)	GSPI-CS	GPIO_17	GSPI-CS	GSPI-CS	GSPI-CS	(wake) GPIO_17	(wake) GPIO_17
GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22	GPIO_22
GPIO_23	I2C-SCL	GPIO_23	GPIO_23	I2C-SCL	GPIO_23	GPIO_23	GPIO_23	GPIO_23	GPIO_23	GPIO_23	GPIO_23
GPIO_24	I2C-SDA	(wake) GPIO_24	(wake) GPIO_24	I2C-SDA	(wake) GPIO_24	(wake) GPIO_24	(wake) GPIO_24	(wake) GPIO_24	(wake) GPIO_24	GT-PWM0	(wake) GPIO_24
JTAG_TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK	SWD-TCK
JTAG_TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS	SWD-TMS
GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28	GPIO_28
GPIO_25	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GT_PWM2	GPIO_25 out only

(1) Pins marked *wake* can be configured to wake up the chip from HIBERNATE or LPDS state. In the current silicon revision, any wake pin can trigger wake up from HIBERNATE. The wake-up monitor in the hibernate control module logically ORs these pins applying a selection mask. However, wake up from LPDS state can be triggered only by one of the wake-up pins that can be configured before entering LPDS. The core digital wake-up monitor use a mux to select one of these pins to monitor.

7.4.1 ADC Reference Accuracy Specifications

The ADC accuracy is 1% at room temperature and 2% across temperature.

7.5 Drive Strength and Reset States for Analog-Digital Multiplexed Pins

Table 7-3 describes the use, drive strength, and default state of analog- and digital-multiplexed pins at first-time power up and reset (nRESET pulled low).

Table 7-3. Drive Strength and Reset States for Analog-Digital Multiplexed Pins

PIN	BOARD LEVEL CONFIGURATION AND USE	DEFAULT STATE AT FIRST POWER UP OR FORCED RESET	STATE AFTER CONFIGURATION OF ANALOG SWITCHES (ACTIVE, LPDS, and HIB POWER MODES)	MAXIMUM EFFECTIVE DRIVE STRENGTH (mA)
25	Connected to the enable pin of the RF switch (ANT_SEL1). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
26	Connected to the enable pin of the RF switch (ANT_SEL2). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
44	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
42	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
47	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
48	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
49	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4
50	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os.	4

7.6 Pad State After Application of Power to Chip, but Before Reset Release

When a stable power is applied to the CC3200 device for the first time or when supply voltage is restored to the proper value following a prior period with supply voltage below 1.5 V, the level of the digital pads are undefined in the period starting from the release of nRESET and until the DIG_DCDC of the CC3220x chip powers up. This period is less than approximately 10 ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins are required to have a definite value during this pre-reset period, an appropriate pullup or pulldown must be used at the board level. The recommended value of this external pull is 2.7 kΩ.

8 Specifications

8.1 Absolute Maximum Ratings

All measurements are referenced at the module pins unless otherwise indicated. All specifications are over process and voltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
V_{BAT} and V_{IO}	–0.5	3.8	V
Digital I/O	–0.5	V_{BAT} + 0.5	V
RF pin	–0.5	2.1	V
Analog pins	–0.5	2.1	V
Operating temperature (T_A)	–40	85	°C
Storage temperature (T_{stg})	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)		±1000	V
		Charged device model (CDM), per JESD22-C101(2)	All pins	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Power-On Hours (POH)

NOTE: This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

OPERATING CONDITION	JUNCTION TEMPERATURE (T_j)	POWER-ON HOURS [POH] (hours)
20% active mode 80% sleep mode	$T_{Ambient}$ up to 85°C	87600(1)

(1) The CC3200MOD device can be operated reliably for 10 years.

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	TYP	MAX	UNIT
V_{BAT} and V_{IO}	2.3	3.3	3.6	V
Operating temperature	–20	25	70	°C
Ambient thermal slew	–20		20	°C/minute

(1) To ensure WLAN performance, the ripple on the power supply must be less than ±300 mV. The ripple should not cause the supply to fall below the brownout voltage.

8.5 Power Consumption Summary

8.5.1 Current Consumption

T_A = 25 °C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS[1] [5]			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		278		mA
				TX power level = 4		194		
			6 OFDM	TX power level = 0		254		
				TX power level = 4		185		
			54 OFDM	TX power level = 0		229		
				TX power level = 4		166		
		RX	1 DSSS			59		
			54 OFDM			59		
	NWP idle connected[3]					15.3		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		275		mA
				TX power level = 4		191		
			6 OFDM	TX power level = 0		251		
				TX power level = 4		182		
			54 OFDM	TX power level = 0		226		
				TX power level = 4		163		
		RX	1 DSSS			56		
			54 OFDM			56		
	NWP idle connected[3]					12.2		
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		272		mA
				TX power level = 4		188		
			6 OFDM	TX power level = 0		248		
				TX power level = 4		179		
			54 OFDM	TX power level = 0		223		
				TX power level = 4		160		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS[2]					0.275		
	NWP idle connected[3]					0.875		
MCU hibernate	NWP hibernate					7		µA
Peak calibration current [4]		V_{BAT} = 3.3 V				450		mA
		V_{BAT} = 2.3 V				620		

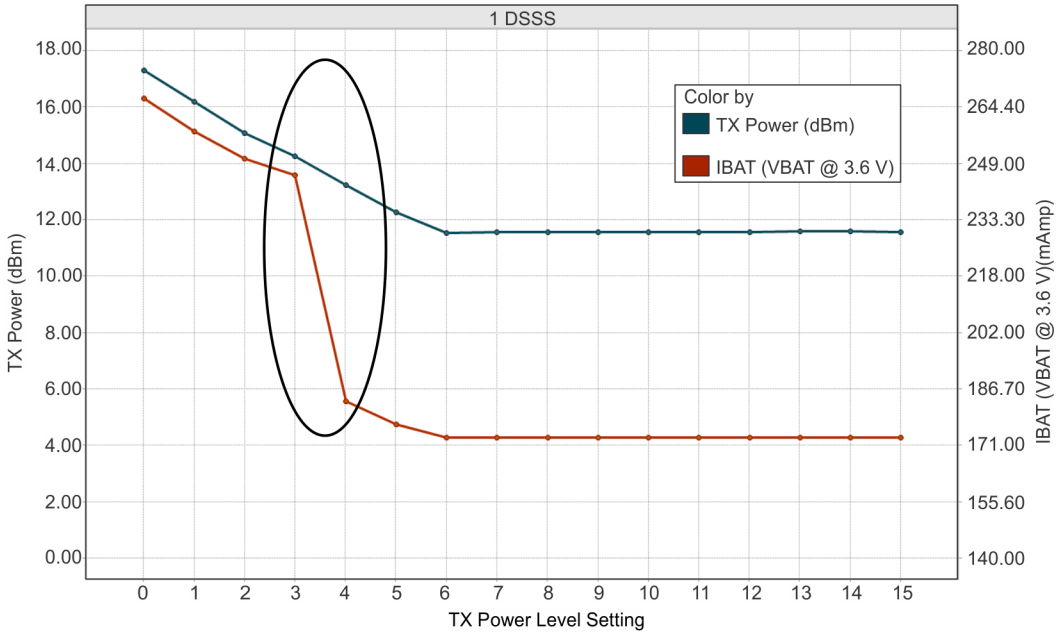
(1) TX power level = 0 implies maximum power (see Figure 8-1 through Figure 8-3). TX power level = 4 implies output power backed off approximately 4 dB.

(2) The LPDS number reported is with retention of 64KB MCU SRAM. The CC3200 device can be configured to retain 0KB, 64KB, 128KB, 192KB or 256KB SRAM in LPDS. Each 64KB retained increases LPDS current by 4 µA.

(3) DTIM = 1

(4) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. Calibration is performed sparingly, typically when coming out of Hibernate and only if temperature has changed by more than 20°C or the time elapsed from prior calibration is greater than 24 hours.

(5) The CC3200 system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.



Note: The area enclosed in the circle represents a significant reduction in current when transitioning from TX power level 3 to 4. In the case of lower range requirements (13-dBm output power), TI recommends using TX power level 4 to reduce the current.

Figure 8-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

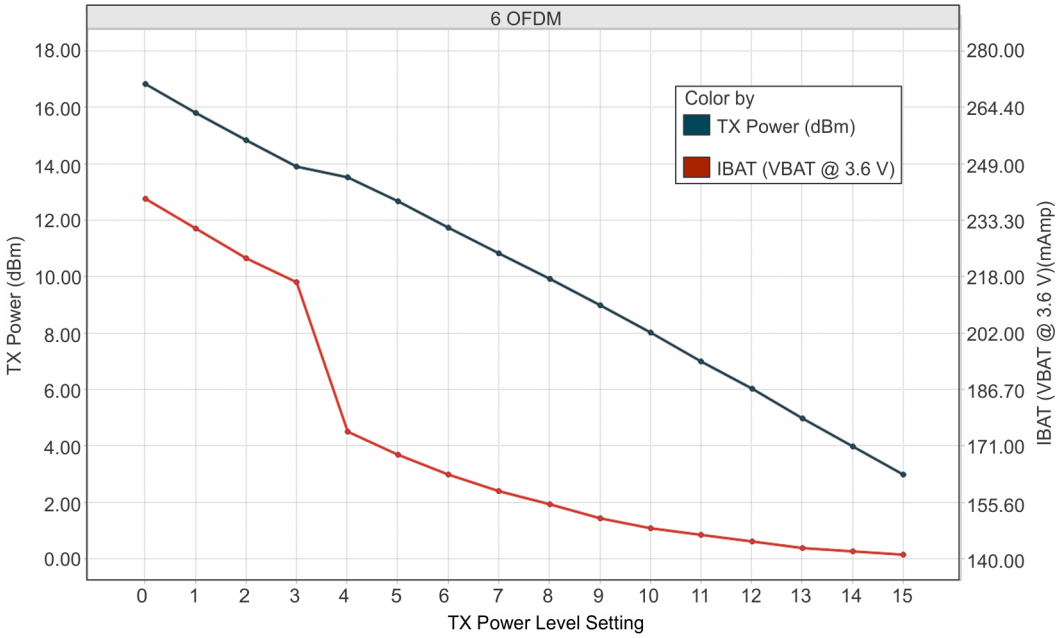


Figure 8-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

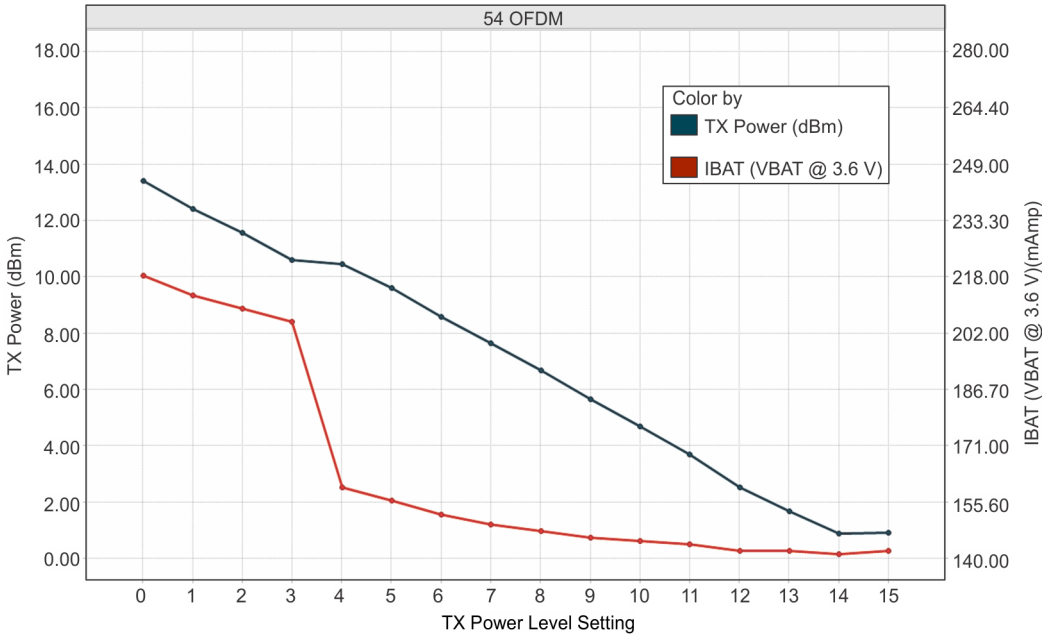


Figure 8-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

8.6 Brownout and Blackout Conditions

The module enters a brownout condition whenever the input voltage dips below $V_{BROWNOUT}$ (see Figure 8-4 and Figure 8-5). This condition must be considered during design of the power supply routing, especially if operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (four contacts for a 2× AA battery), and the wiring and PCB routing resistance.

Note

When the module is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

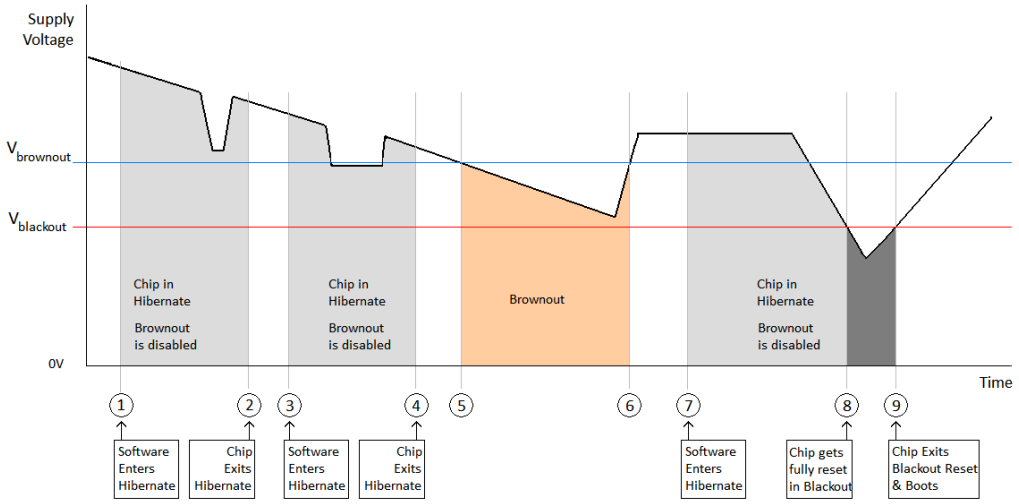


Figure 8-4. Brownout and Blackout Levels (1 of 2)

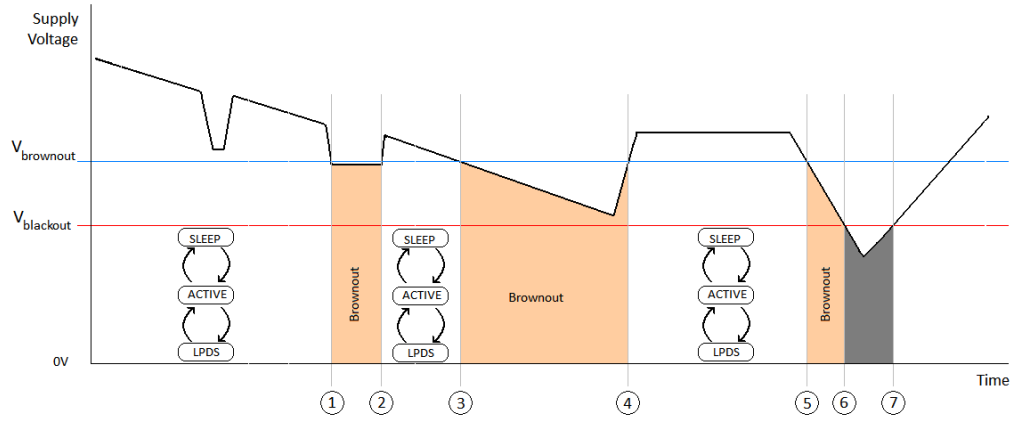


Figure 8-5. Brownout and Blackout Levels (2 of 2)

In the brownout condition, all sections of the CC3200MOD shut down within the module except for the Hibernate block (including the 32-kHz RTC clock), which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the module are lost. $V_{brownout}$ = 2.1 V and $V_{blackout}$ = 1.67 V

Table 8-1 lists the brownout and blackout voltage levels.

Table 8-1. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

8.7 WLAN RF Characteristics

8.7.1 WLAN Receiver Characteristics

T_A = 25°C, V_{BAT} = 2.3 to 3.6 V. Parameters measured at module pin on channel 7 (2442 MHz).

PARAMETER	RATE	MIN	TYP	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g or 11n rates) (10% PER)(1)	1 DSSS		–94.7		dBm
	2 DSSS		–92.6		
	11 CCK		–87.0		
	6 OFDM		–89.0		
	9 OFDM		–88.0		
	18 OFDM		–85.0		
	36 OFDM		–79.5		
	54 OFDM		–73.0		
	MCS7 (Mixed Mode)		–69.0		
Maximum input level (10% PER)	802.11b		–3.0		dBm
	802.11g		–9.0		

(1) Sensitivity is 1 dB worse on channel 13 (2472 MHz).

8.7.2 WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.3 V to 3.6 V. Parameters measured at module pin on channel 7 (2442 MHz).(1)

PARAMETER	RATE	MIN	TYP	MAX	UNIT
Max RMS Output Power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		17.0		dBm
	2 DSSS		17.0		
	11 CCK		17.25		
	6 OFDM		16.25		
	9 OFDM		16.25		
	18 OFDM		16		
	36 OFDM		15		
	54 OFDM		13.5		
	MCS7 (mixed mode)		12		
Transmit center frequency accuracy		–20		20	ppm

(1) Channel-to-channel variation is up to 2 dB. The edge channels (2412 MHz and 2462 MHz) have reduced TX power to meet FCC emission limits.

8.8 Reset Requirement

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	Operation mode level		0.65 × V_{BAT}		V
V_{IL}	Shutdown mode level(1)	0	0.6		V
	Minimum time for nReset low for resetting the module	5			ms
T_r and T_f	Rise and fall times		20		µs

(1) The nRESET pin must be held below 0.6 V for the module to register a reset.

8.9 Thermal Resistance Characteristics for MOB and MON Packages

NAME	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s)(3)
$R\Theta_{JC}$	Junction-to-case	9.08	0.00
$R\Theta_{JB}$	Junction-to-board	10.34	0.00
$R\Theta_{JA}$	Junction-to-free air	11.60	0.00
Psi_{JT}	Junction-to-package top	9.08	0.00
Psi_{JB}	Junction-to-board	10.19	0.00

(1) °C/W = degrees Celsius per watt.

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.

(3) m/s = meters per second.

8.10 Timing and Switching Characteristics

8.10.1 nRESET

Figure 8-6 shows the reset timing diagram for the 32K crystal first-time power-up and reset.

Table 8-2 describes the timing requirements for the first-time power-up and reset removal.

Table 8-2. First-Time Power-Up and Reset Removal Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T1	Supply settling time	The time for which the nRESET pin must be held low after supply stabilizes		3		ms
T2	Hardware wake-up time	Time taken by the hardware to initialize		25		ms
T3	Firmware initiation time	Time taken by the ROM firmware to initialize the hardware (Includes 32-KHz oscillator wake-up time)		1.1		s
T4	Code download time	Time taken to download the code from the serial Flash to on-chip RAM	Image size (KB) × 0.75 ms			

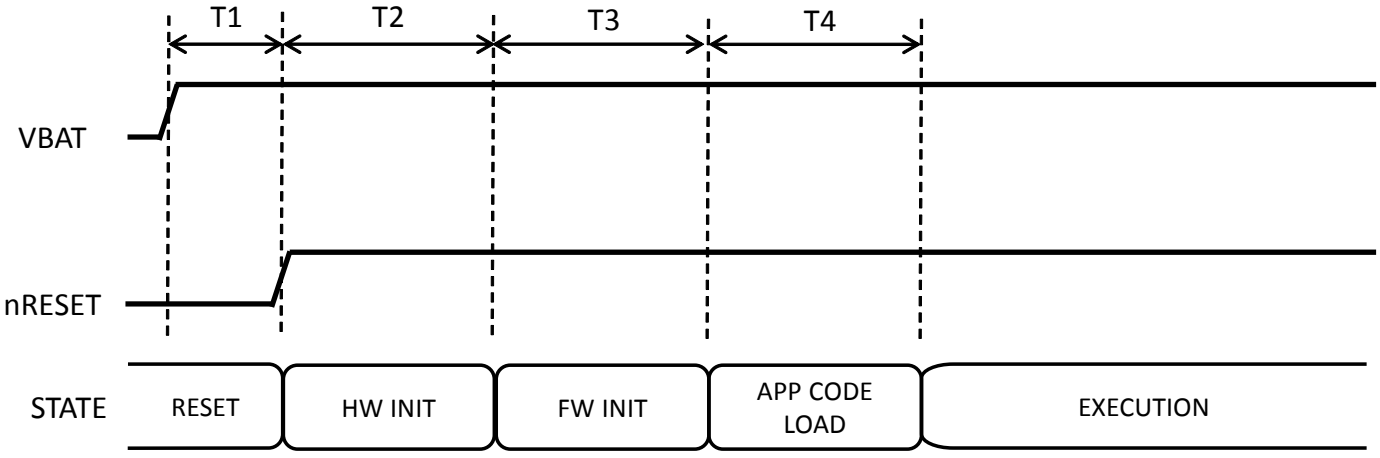


Figure 8-6. First-Time Power-Up and Reset Removal Timing Diagram

8.10.2 Wake Up From Hibernate Timing

Table 8-3 lists the software hibernate timing requirements.

Note

The 32.768-kHz crystal is kept enabled by default when the module goes to hibernate.

Table 8-3. Software Hibernate Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{HIB_MIN}	Minimum hibernate time	The time for which the device must be held in hibernate mode		10		ms
T2	Hardware wake-up time	Time taken by the hardware to initialize		25		ms
T3	Firmware initiation time	Time taken by the ROM firmware to initialize the hardware		3		ms
T4	Code download time	Time taken to download the code from the serial flash to on-chip RAM		Image size (KB) × 0.75 ms		

Figure 8-7 shows the timing diagram for wake up from the hibernate state.

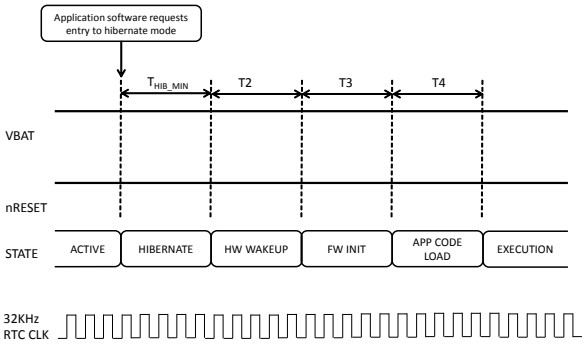


Figure 8-7. Wake Up From Hibernate Timing Diagram

9 Detailed Description

9.1 Overview

The CC3200MOD is a Wi-Fi® internet-on-a chip module that consists of an Arm® Cortex®-M4 processor with a rich set of peripherals for diverse application requirements, a Wi-Fi network processor, and power-management subsystems. The device optimizes bus matrix and memory management to provide an advantage to the application developer.

9.2 Functional Block Diagram

Figure 9-1 shows the functional block diagram of the CC3200MOD SimpleLink™ Wi-Fi® solution.

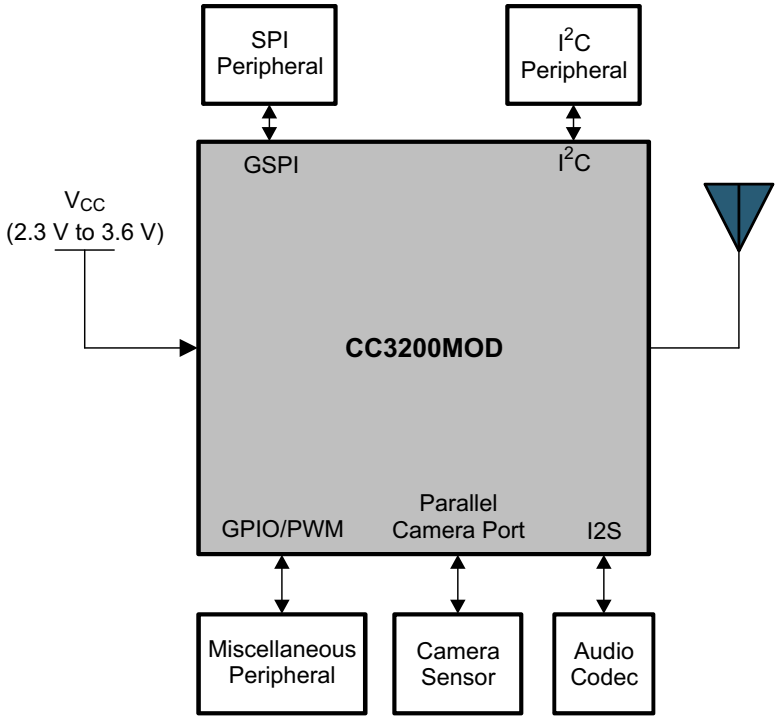


Figure 9-1. Functional Block Diagram

9.3 Arm® Cortex®-M4 Processor Core Subsystem

The high-performance Arm® Cortex®-M4 processor provides a low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Cortex®-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm® Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for ARMv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels

  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Low-cost debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted
  - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

9.4 CC3200 Device Encryption

Figure 9-2 shows a standard MCU for the CC3200 device. Application image and user data files are not encrypted. Network certificates are encrypted using a device-specific key.

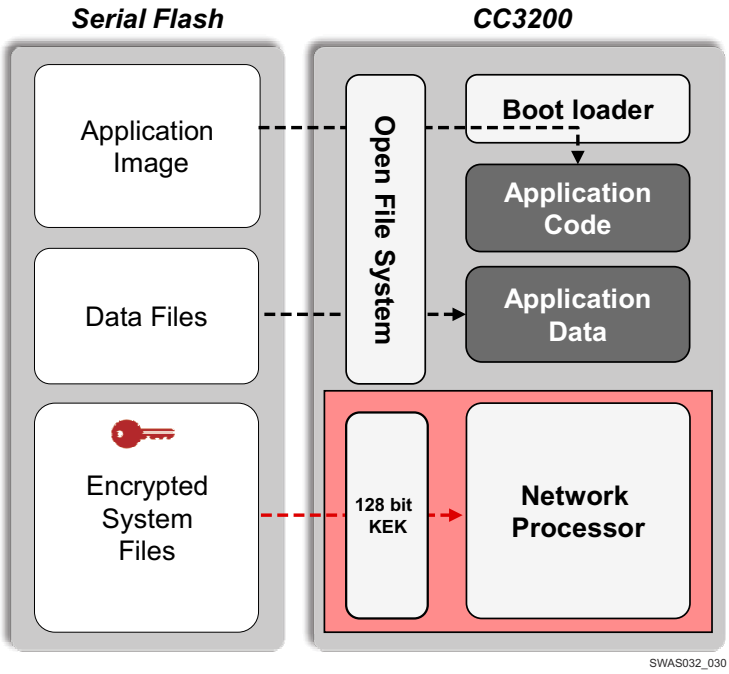


Figure 9-2. CC3200 Standard MCU

9.5 Wi-Fi® Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated Arm® MCU to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3200 device supports station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security in addition to WPS 2.0. The Wi-Fi network processor includes an embedded IPv4 TCP/IP stack.

Table 9-1 summarizes the NWP features.

Table 9-1. Summary of Features Supported by the NWP Subsystem

ITEM	DOMAIN	CATEGORY	FEATURE	DETAILS
1	TCP/IP	Network Stack	IPv4	Baseline IPv4 stack
2	TCP/IP	Network Stack	TCP/UDP	Base protocols
3	TCP/IP	Protocols	DHCP	Client and server mode
4	TCP/IP	Protocols	ARP	Support ARP protocol
5	TCP/IP	Protocols	DNS/mDNS	DNS Address resolution and local server
6	TCP/IP	Protocols	IGMP	Up to IGMPv3 for multicast management
7	TCP/IP	Applications	mDNS	Support multicast DNS for service publishing over IP
8	TCP/IP	Applications	mDNS-SD	Service discovery protocol over IP in local network
9	TCP/IP	Applications	Web Sever/HTTP Server	URL static and dynamic response with template
10	TCP/IP	Security	TLS/SSL	TLS v1.2 (client/server) / SSL v3.0
11	TCP/IP	Security	TLS/SSL	For the supported Cipher Suite, go to SimpleLink Wi-Fi CC3200 SDK.
12	TCP/IP	Sockets	RAW Sockets	User-defined encapsulation at WLAN MAC/PHY or IP layers
13	WLAN	Connection	Policies	Allows management of connection and reconnection policy
14	WLAN	MAC	Promiscuous mode	Filter-based Promiscuous mode frame receiver
15	WLAN	Performance	Initialization time	From enable to first connection to open AP less than 50 ms
16	WLAN	Performance	Throughput	UDP = 16 Mbps
17	WLAN	Performance	Throughput	TCP = 13 Mbps
18	WLAN	Provisioning	WPS2	Enrollee using push button or PIN method.
19	WLAN	Provisioning	AP Config	AP mode for initial product configuration (with configurable Web page and beacon Info element)
20	WLAN	Provisioning	SmartConfig	Alternate method for initial product configuration
21	WLAN	Role	Station	802.11 b/g/n Station with legacy 802.11 power save
22	WLAN	Role	Soft AP	802.11 b/g single station with legacy 802.11 power save
23	WLAN	Role	P2P	P2P operation as GO
24	WLAN	Role	P2P	P2P operation as CLIENT
25	WLAN	Security	STA-Personal	WPA2 personal security
26	WLAN	Security	STA-Enterprise	WPA2 enterprise security
27	WLAN	Security	STA-Enterprise	EAP-TLS
28	WLAN	Security	STA-Enterprise	EAP-PEAPv0/TLS
29	WLAN	Security	STA-Enterprise	EAP-PEAPv1/TLS
30	WLAN	Security	STA-Enterprise	EAP-PEAPv0/MSCHAPv2
31	WLAN	Security	STA-Enterprise	EAP-PEAPv1/MSCHAPv2
32	WLAN	Security	STA-Enterprise	EAP-TTLS/EAP-TLS
33	WLAN	Security	STA-Enterprise	EAP-TTLS/MSCHAPv2

Table 9-1. Summary of Features Supported by the NWP Subsystem (continued)

ITEM	DOMAIN	CATEGORY	FEATURE	DETAILS
34	WLAN	Security	AP-Personal	WPA2 personal security

9.6 Power-Management Subsystem

The CC3220MODx and CC3220MODAx power-management subsystems contain DC/DC converters to accommodate the differing voltage or current requirements of the system.

The CC3220MODx is a fully integrated module-based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

The CC3200 power-management subsystem contains DC/DC converters to accommodate the differing voltage or current requirements of the system. The module can operate from an input voltage ranging from 2.3 V to 3.6 V and can be directly connected to 2× AA Alkaline batteries.

The CC3200MOD is a fully integrated module-based WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the module to operate from a wide variety of input sources. For maximum flexibility, the module can operate in the modes described in the following sections.

9.6.1 VBAT Wide-Voltage Connection

In the wide-voltage battery connection, the module can be directly connected to two AA alkaline batteries. All other voltages required to operate the module are generated internally by the DC/DC converters. This scheme is the most common mode for the module because it supports wide-voltage operation from 2.3 to 3.6 V.

In the wide-voltage battery connection, the module is powered directly by the battery or preregulated 3.3-V supply. All other voltages required to operate the device are generated internally by the DC/DC converters. This scheme is the most common mode for the device because it supports wide-voltage operation from 2.3 to 3.6 V.

9.7 Low-Power Operating Mode

From a power-management perspective, the CC3220MODx and CC3220MODAx module comprise the following two independent subsystems:

- Arm® Cortex®-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Arm® Cortex®-M4 application processor runs the user application loaded from an external serial Flash, or internal Flash (in CC3220MODSF). The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem and can be in one of the five modes described in Table 9-2.

Table 9-2. User Program Modes

APPLICATION PROCESSOR (MCU) MODE(1)	DESCRIPTION
MCU active mode	MCU executing code at 80-MHz state rate
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3 ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source.
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC keeps running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15 ms plus the time to load the application from serial Flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO (GPIO0 to GPIO6).
MCU shutdown mode	The lowest power mode system-wise. All device logics are off, including the RTC. The wake-up time in this mode is longer than hibernate at about 1.1 s. To enter or exit the shutdown mode, the state of the nRESET line is changed (low to shut down, high to turn on).

(1) Modes are listed in order of power consumption, with highest power modes listed first.

The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see Table 9-3).

Table 9-3. Networking Subsystem Modes

NETWORK PROCESSOR MODE	DESCRIPTION
Network active mode (processing layer 3, 2, and 1)	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing not required.
Network active listen mode	Special power optimized active mode for receiving beacon frames (no other frames supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power save operation. The CC3220MODx and CC3220MODAx NWPs automatically goes into LPDS mode between beacons and then wakes to active listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats.
Network LPDS mode	Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake up.
Network disabled	The network is disabled

The operation of the application and network processor ensures that the module remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.

- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

9.8 Memory

9.8.1 External Memory Requirements

The CC3200 device maintains a proprietary file system on the SFLASH. The CC3200 file system stores the service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always located at the beginning of the SFLASH. The applications microcontroller must access the SFLASH memory area allocated to the file system directly through the CC3200 file system. The applications microcontroller must not access the SFLASH memory area directly.

The file system manages the allocation of SFLASH blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on SFLASH using human-readable file names rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system (see Figure 9-2).

All file types can have a maximum of 128 supported files in the file system. All files are stored in blocks of 4KB and thus use a minimum of 4KB of flash space. Encrypted files with fail-safe support and optional security are twice the original size and use a minimum of 8KB. Encrypted files are counted as fail safe in terms of space. The maximum file size is 16MB.

Table 9-4. CC3200 SFLASH Size Recommendations

ITEM	TYPICAL FAIL-SAFE	TYPICAL NONFAIL-SAFE
File system	20KB	20KB
Service pack	224KB	112KB
System and configuration files	216KB	108KB
MCU code	512KB	256KB
Total	4Mb	2Mb
Recommended	16Mb	8Mb

The CC3200 device supports JEDEC specification SFDP (serial flash device parameters). The following SFLASH devices are verified for functionality with the CC3200 device in addition to the ones in the reference design:

- Micron (N25Q128-A13BSE40): 128 Mb
- Spansion (S25FL208K): 8 Mb
- Winbond (W25Q16V): 16 Mb
- Adesto (AT25DF081A): 8 Mb
- Macronix (MX25L12835F-M2): 128 Mb

For compatibility with the CC3200 device, the SFLASH device must support the following commands:

- Command 0x9F (read the device ID [JEDEC]). Procedure: SEND 0x9F, READ 3 bytes.
- Command 0x05 (read the status of the SFLASH). Procedure: SEND 0x05, READ 1 byte. Assume bit 0 is busy and bit 1 is write enable.
- Command 0x06 (set write enable). Procedure: SEND 0x06, read status until write-enable bit is set.
- Command 0xC7 (chip erase). Procedure: SEND 0xC7, read status until busy bit is cleared.
- Command 0x03 (read data). Procedure: SEND 0x03, SEND 24-bit address, read *n* bytes.
- Command 0x02 (write page). Procedure: SEND 0x02, SEND 24-bit address, write *n* bytes ($0 < n < 256$).
- Command 0x20 (sector erase). Procedure: SEND 0x20, SEND 24-bit address, read status until busy bit is cleared. Sector size is always assumed to be 4K.

9.8.2 Internal Memory

The CC3200 device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. To select the appropriate SRAM configuration, see the device variants listed in the orderable addendum at the end of this datasheet. The micro direct memory

access (µDMA) controller can transfer data to and from SRAM and various peripherals. The CC3200 ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3200 API list in *Section 12.3*.

9.8.2.1 SRAM

The CC3200 family provides up to 256KB of zero-wait-state, on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is located at offset 0x2000 0000 of the device memory map.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide in *Section 12.3*.

9.8.2.2 ROM

The internal zero-wait-state ROM of the CC3200 module is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial Flash memory is empty). The DriverLib software library of the CC3200 controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce Flash memory requirements and free the Flash memory to be used for other purposes.

9.8.2.3 Memory Map

Table 9-5 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document in *Section 12.3*.

Table 9-5. Memory Map

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x0000 0000	0x0007 FFFF	On-chip ROM (Bootloader + DriverLib)	
0x2000 0000	0x2003 FFFF	Bit-banded on-chip SRAM	
0x2200 0000	0x23FF FFFF	Bit-band alias of 0x2000 0000 through 0x200F FFFF	
0x4000 0000	0x4000 0FFF	Watchdog timer A0	
0x4000 4000	0x4000 4FFF	GPIO port A0	
0x4000 5000	0x4000 5FFF	GPIO port A1	
0x4000 6000	0x4000 6FFF	GPIO port A2	
0x4000 7000	0x4000 7FFF	GPIO port A3	
0x4000 C000	0x4000 CFFF	UART A0	
0x4000 D000	0x4000 DFFF	UART A1	
0x4002 0000	0x400 07FF	I^2C A0 (Master)	
0x4002 0800	0x4002 0FFF	I^2C A0 (Slave)	
0x4003 0000	0x4003 0FFF	General-purpose timer A0	
0x4003 1000	0x4003 1FFF	General-purpose timer A1	
0x4003 2000	0x4003 2FFF	General-purpose timer A2	
0x4003 3000	0x4003 3FFF	General-purpose timer A3	
0x400F 7000	0x400F 7FFF	Configuration registers	
0x400F E000	0x400F EFFF	System control	
0x400F F000	0x400F FFFF	µDMA	
0x4200 0000	0x43FF FFFF	Bit band alias of 0x4000.0000 through 0x400F.FFFF	

Table 9-5. Memory Map (continued)

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x4401 C000	0x4401 EFFF	McASP	
0x4402 0000	0x4402 0FFF	SSPI	Used for external serial flash
0x4402 1000	0x4402 2FFF	GSPI	Used by application processor
0x4402 5000	0x4402 5FFF	MCU reset clock manager	
0x4402 6000	0x4402 6FFF	MCU configuration space	
0x4402 D000	0x4402 DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402 E000	0x4402 EFFF	MCU shared configuration	
0x4402 F000	0x4402 FFFF	Hibernate configuration	
0x4403 0000	0x4403 FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)(1)	
0x4403 0000	0x4403 0FFF	DTHE registers and TCP checksum(1)	
0x4403 5000	0x4403 5FFF	MD5/SHA(1)	
0x4403 7000	0x4403 7FFF	AES(1)	
0x4403 9000	0x4403 9FFF	DES(1)	
0xE000 0000	0xE000 0FFF	Instrumentation trace Macrocell™	
0xE000 1000	0xE000 1FFF	Data watchpoint and trace (DWT)	
0xE000 2000	0xE000 2FFF	Flash patch and breakpoint (FPB)	
0xE000 E000	0xE000 EFFF	Nested vectored interrupt controller (NVIC)	
0xE004 0000	0xE004 0FFF	Trace port interface unit (TPIU)	
0xE004 1000	0xE004 1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004 2000	0xE00F FFFF	Reserved	

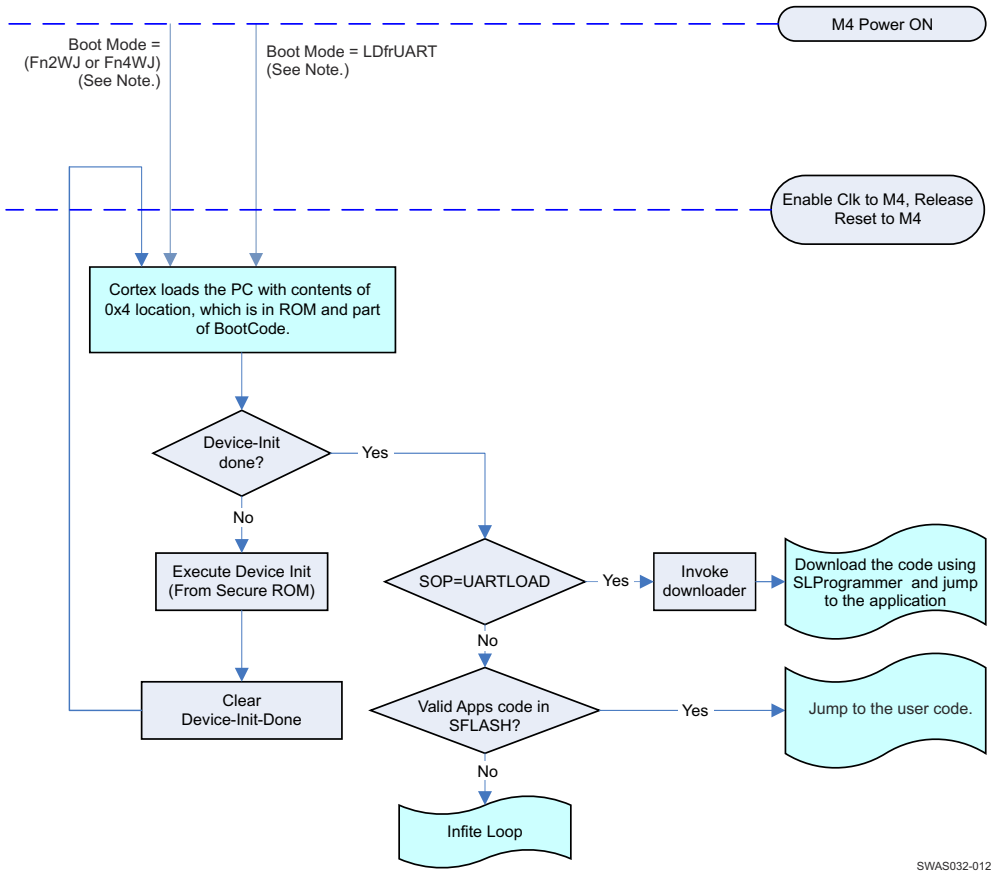
(1) Available with CC3200R1-S2RTD[T/R] part number

9.9 Boot Modes

9.9.1 Overview

The boot process of the application processor includes two phases. The first phase consists of unrestricted access to all register space and configuration of the specific device setting. In the second phase, the application processor executes user-specific code.

Figure 9-3 shows the bootloader flow chart.



Note: For definitions of the SoP mode functional configurations, see Table 9-6.

Figure 9-3. Bootloader Flow Chart

9.9.2 Invocation Sequence and Boot Mode Selection

The following sequence of events occurs during the Cortex® processor boot:

1. After power-on-reset (POR), the processor starts execution.
2. The processor jumps to the first few lines (FFL) of code in the ROM to determine if the current boot is the first device-init boot or the second MCU boot. The determination is based on the Device-Init flag in a secure register. The Device-Init flag is set while out of POR. The registers in the secure region are accessible only in the device-init mode.
3. If the current boot is the first boot, the processor executes the device-init code from ROM.
4. At the end of the boot, the processor clears the Device-Init flag and changes the master ID of the processor and the DMA. These registers are part of the secure region.
5. The processor resets itself, initiating a second boot.
6. During the second boot, the processor rereads the Device-Init flag, the bit is cleared, and the processor obtains a different master ID.
7. After executing FFL and the unsecure boot code, the processor jumps to the developer code (application).
8. For the rest of the operation (until the next power cycle), the Cortex® mode is designated the MCU. During this phase, access to the secure region is restricted.

9.9.3 Boot Mode List

The CC3200 device implements a sense-on-power (SoP) scheme to determine the device operation mode. The device can be configured to power up in one of the three following modes:

- Fn4WJ: Functional mode with a 4-wire JTAG mapped to fixed pins
- Fn2WJ: Functional mode with a 2-wire SWD mapped to fixed pins
- LDfrUART: UART load mode to Flash the system during development and in OEM assembly line (for example, serial Flash connected to the CC3200R device)

SoP values are sensed from the device pin during power up. This encoding determines the boot flow. Before the device is taken out of reset, the SoP values are copied to a register and then determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping for some of the pins (JTAG, SWD, UART0) Table 9-6 provides the pull configurations.

Table 9-6. CC32x0 Functional Configurations

NAME	SOP2	SOP1	SOP0	SOP MODE	COMMENT
UARTLOAD	Pullup	Pulldown	Pulldown	LDfrUART	Factory/Lab Flash/SRAM load through UART. Device waits indefinitely for UART to load code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.
FUNCTIONAL_2WJ	Pulldown	Pulldown	Pullup	Fn2WJ	Functional development mode. In this mode, 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection.
FUNCTIONAL_4WJ	Pulldown	Pulldown	Pulldown	Fn4WJ	Functional development mode. In this mode, 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection.

There is an internal pull resistor for SOP0 and SOP1 with value of 100 kΩ. There is no need for any external pulls. TI recommends a 2.7-kΩ pull resistor for SOP2. SOP2 can be used by the application for other functions after chip power-up is complete. However, to avoid spurious SOP values from being sensed at power-up, TI strongly recommends that the SOP2 pin be used only for output signals. On the other hand, the SOP0 and SOP1 pins are multiplexed with WLAN analog test pins and are not available for other functions.

10 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Device Connection and Layout Fundamentals

10.1.1 Power Supply Decoupling and Bulk Capacitors

Depending upon routing resistors and battery type, TI recommends adding two 100-µF ceramic capacitors to help provide the peak current drawn by the CC3200 module.

10.1.2 Reset

The module features an internal RC circuit to reset the module during power ON. An external circuit is not required unless an external MCU controls the CC3200 module. The nRESET pin must be held below 0.6 V for at least 5 ms for the module to successfully reset.

10.1.3 Unused Pins

All unused pins can be left unconnected without any concern to leakage current.

10.1.4 General Layout Recommendations

1. Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
2. Do **not** run signal traces underneath the module on a layer where the module is mounted.
3. RF traces must have 50-Ω impedance.
4. RF trace bends must be made with gradual curves, and 90 degree bends must be avoided.
5. RF traces must **not** have sharp corners.
6. There must be no traces or ground under the antenna section.
7. RF traces must have via stitching on the ground plane beside the RF trace on both sides.
8. RF traces must be as short as possible. The antenna, RF traces, and the module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

10.1.5 Do's and Don'ts

Note

If an external device drives a positive voltage to the signal pads and the CC3200MOD is not powered, DC current is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3200MOD can occur. To prevent current draw, TI recommends any one of the following:

- All devices interfaced to the CC3200MOD must be powered from the same power rail as the chip.
- Use level-shifters between the module and any external devices fed from other independent rails.
- The nRESET pin of the CC3200MOD must be held low until the VBAT supply to the module is driven and stable. This is automatically done within the module if this pin is left unconnected.

10.2 Reference Schematics

Figure 10-1 shows the reference schematic for the CC3200MOD module.

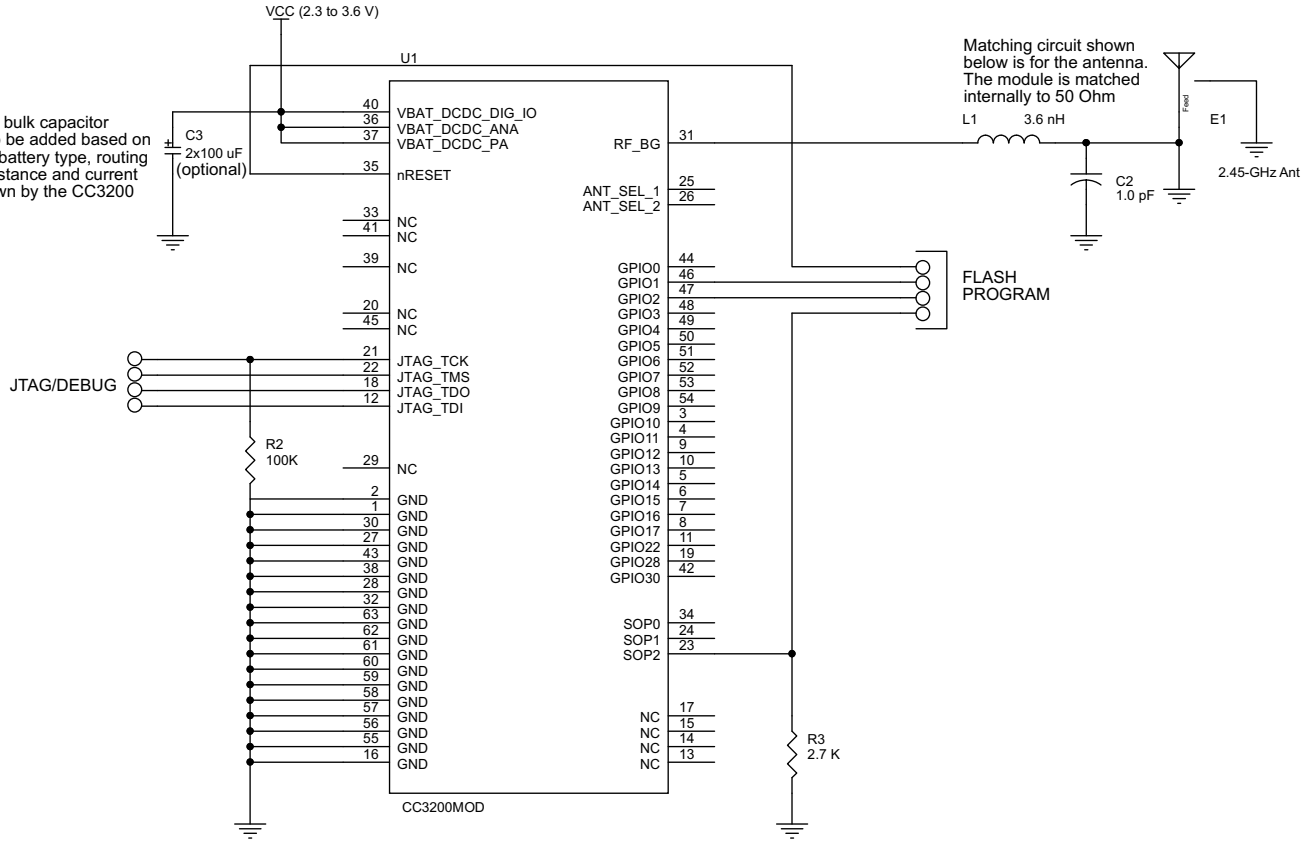


Figure 10-1. CC3200MOD Module Reference Schematic

10.3 Design Requirements

Table 10-1 provides the bill of materials.

Table 10-1. Bill of Materials (1)

QTY	PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	U1	CC3200MOD	Texas Instruments	CC3200MODR1M2AMOB	SimpleLink™ Wi-Fi® and Internet-of-Things Module Solution, a Single-Chip Wireless MCU, MOB0063A (SIP MODULE-63)
1	E1	2.45-GHz Ant	Taiyo Yuden	AH316M245001-T	Antenna Bluetooth WLAN ZigBee® WIMAX
1	C2	1.0 pF	Murata Electronics North America	GJM1555C1H1R0BB01D	CAP CER 1 pF 50 V NP0 0402
1	L1	3.6 nH	Murata Electronics North America	LQP15MN3N6B02D	INDUCTOR 3.6 NH 0.1 NH 0402

(1) Resistors are not shown here. Any resistor of 5% tolerance can be used.

10.4 Detailed Design Procedure

The design procedure considerations follow:

- The bulk capacitor is to be added based on the battery type, routing resistance and current drawn by the CC3200
- For more details on brownout consideration, see Section 8.6. The module enters a brownout condition whenever the input voltage dips below $V_{BROWNOUT}$ (see Figure 8-4 and Figure 8-5). This condition must be considered during design of the power supply routing, specifically if operating from a battery.

10.5 Layout Recommendations

10.5.1 RF Section (Placement and Routing)

Figure 10-2 shows the RF sectional layout.

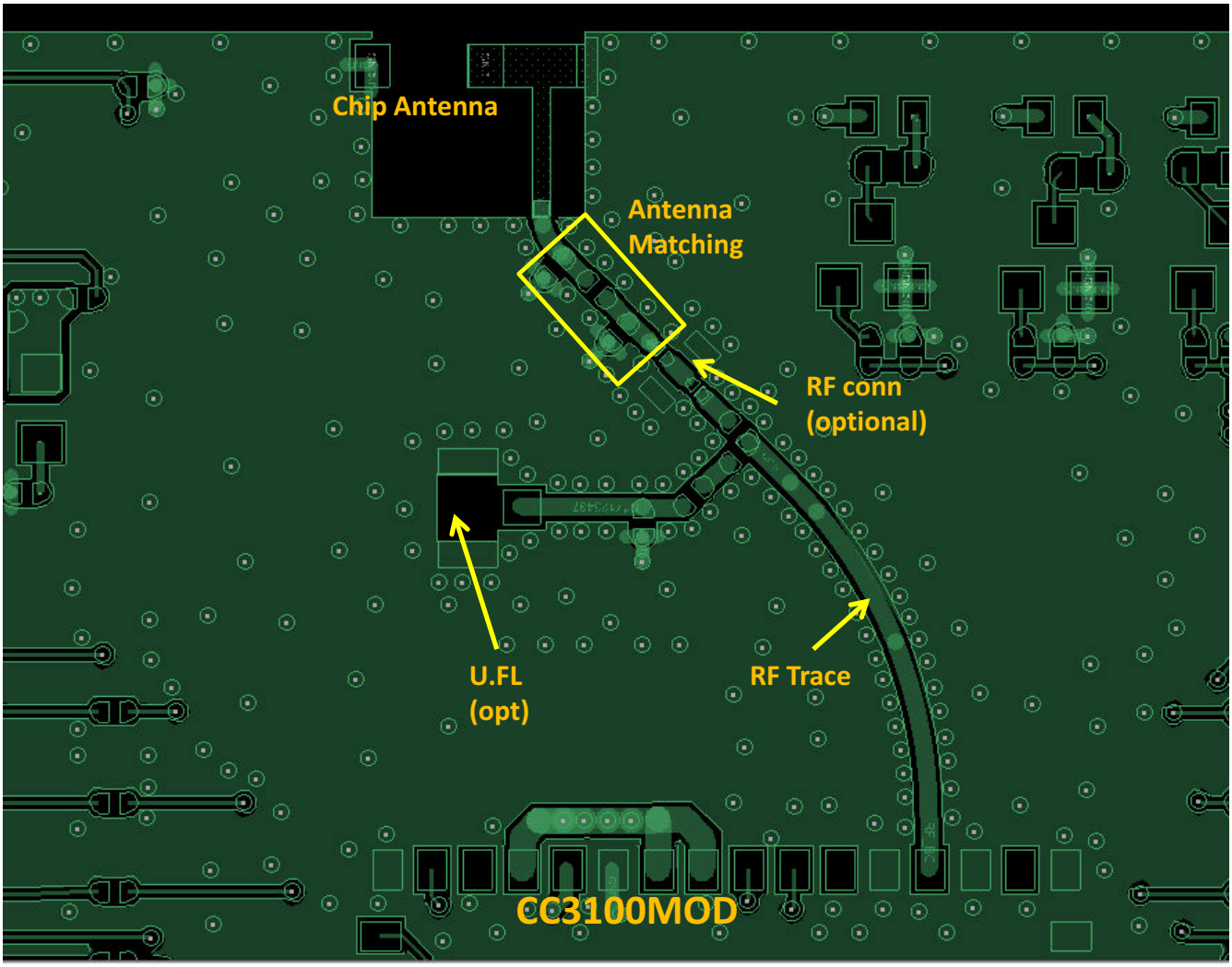


Figure 10-2. RF Section Layout

The RF section of this wireless device gets top priority in terms of layout. The RF section must be laid out correctly to ensure optimum performance from the device. A poor layout can cause low-output power, EVM degradation, sensitivity degradation, and mask violations.

10.5.2 Antenna Placement and Routing

The antenna is the element used to convert the guided waves on the PCB traces to the free space electromagnetic radiation. The placement and layout of the antenna are the keys to increased range and data rates.

The points listed in Table 10-2 must be observed for the antenna.

Table 10-2. Antenna Guidelines

SR NO.	GUIDELINES
1	Place the antenna on an edge or corner of the PCB.
2	Ensure that no signals are routed across the antenna elements on all the layers of the PCB.
3	Most antennas, including the chip antenna used on the booster pack, require ground clearance on all the layers of the PCB. Ensure that the ground is cleared on inner layers as well.
4	Ensure that there is provision to place matching components for the antenna. These must be tuned for best return loss when the complete board is assembled. Any plastics or casing must also be mounted while tuning the antenna because this can impact the impedance.
5	Ensure that the antenna impedance is 50 Ω because the device is rated to work only with a 50-Ω system.
6	In case of printed antenna, ensure that the simulation is performed with the solder mask in consideration.
7	Ensure that the antenna has a near omnidirectional pattern.
8	The feed point of the antenna is required to be grounded. This is only for the antenna type used on the CC3200MOD Launchpad. See the specific antenna data sheets for the recommendations.
9	To use the FCC certification of the module, refer to CC31xx & CC32xx Radio Certifications wiki page on CC3200 Radio certification

Table 10-3. Recommended Components

CHOICE	PART NUMBER	MANUFACTURER	NOTES
1	AH316M245001-T	Taiyo Yuden	Can be placed on edge of the PCB and uses much less PCB space

10.5.3 Transmission Line

The RF signal from the device is routed to the antenna using a Coplanar Waveguide with ground (CPW-G) structure. The CPW-G structure offers the maximum isolation across filter gap and the best possible shielding to the RF lines. In addition to the ground on the L1 layer, placing GND vias along the line also provides additional shielding.

Figure 10-3 shows the coplanar waveguide.

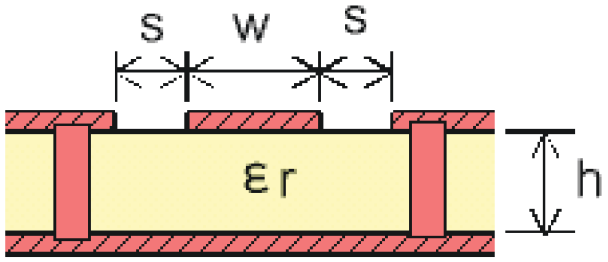


Figure 10-3. Coplanar Waveguide (Cross Section) With GND and Via Stitching

Figure 10-4 shows the top view of the CPW with GND.

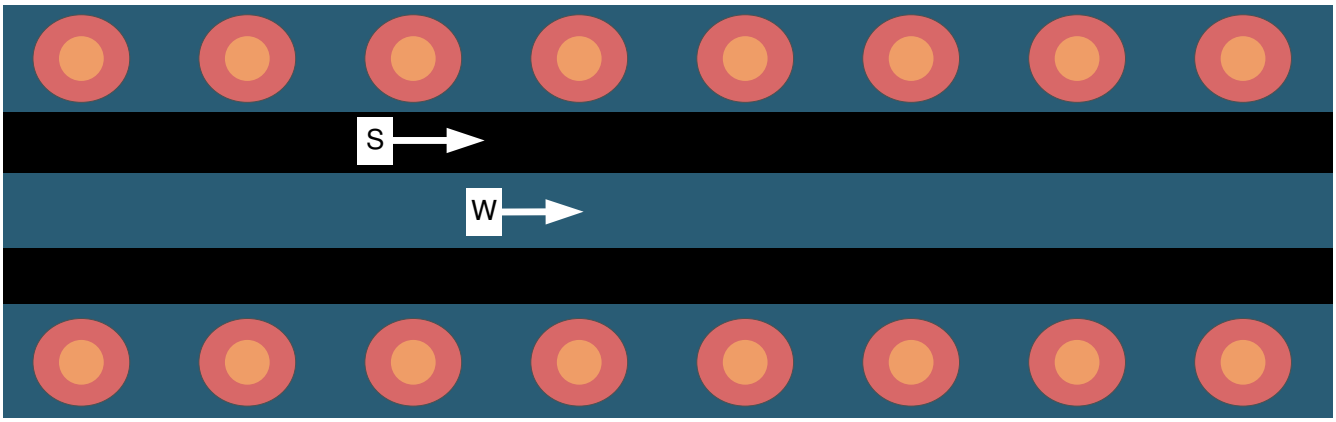


Figure 10-4. CPW With GND (Top View)

Table 10-4 and Table 10-5 provide the recommended values for 2-layer boards and 4-layer boards, respectively.

Table 10-4. Recommended PCB Values for 2-Layer Boards (L1 to L2 = 40 mils) (1)

PARAMETER	VALUE	UNIT
W	35	mils
S	6	mils
H	40	mils
Er (FR-4 substrate)	3.9	

(1) The CC3200MOD Launchpad uses a 4 layer stack-up to route other components on the board. Customer can choose a two-layer stack-up based on the values shown here.

Table 10-5. Recommended PCB Values for 4-Layer Boards (L1 to L2 = 10 mils)

PARAMETER	VALUE	UNITS
W	20	mils
S	18	mils
H	10	mils
Er (FR-4 substrate)	4	

11 Environmental Requirements and Specifications

11.1 PCB Bending

The PCB bending specification will maintain planeness at a thickness of less than 0.1 mm.

11.2 Handling Environment

11.2.1 Terminals

The product is mounted with motherboard through land-grid array (LGA). To prevent poor soldering, do not make skin contact with the LGA portion.

11.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product to malfunction.

11.3 Storage Condition

11.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product will be 12 months from the date the bag is sealed.

11.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

11.4 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12 to 24 hours

Baking times: 1 time

11.5 Soldering and Reflow Condition

- Heating method: Conventional convection or IR convection
- Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method
- Solder paste composition: Sn/3.0 Ag/0.5 Cu
- Allowable reflow soldering times: 2 times based on the reflow soldering profile (see Figure 11-1)
- Temperature profile: Reflow soldering will be done according to the temperature profile (see Figure 11-1)
- Peak temperature: 245°C

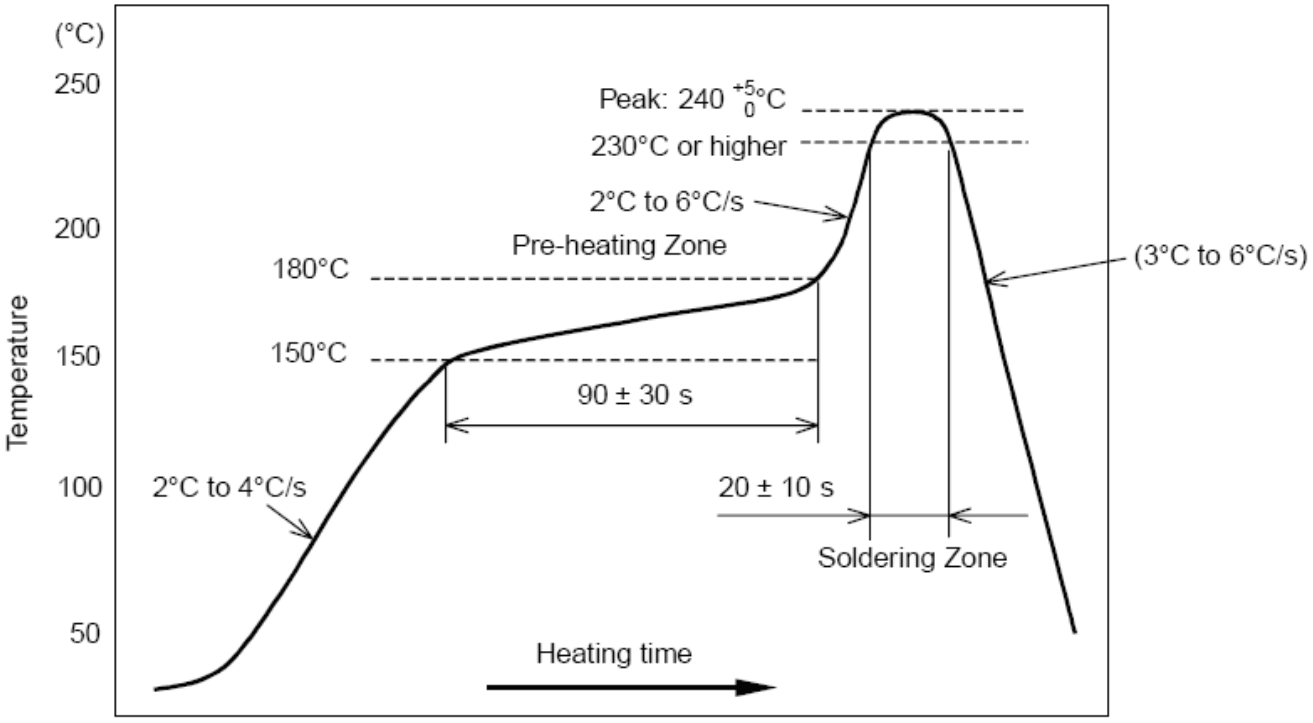


Figure 11-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)

Note

TI does not recommend the use of conformal coating or similar material on the SimpleLink™ module. This coating can lead to localized stress on the solder connections inside the module and impact the module reliability. Use caution during the module assembly process to the final PCB to avoid the presence of foreign material inside the module.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the CC3200MOD applications:

Software Development Tools: Code Composer Studio Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any CC3200MOD application.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the CC3200MOD platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

TI Designs and Reference Designs

The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jumpstart your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

12.1.2 Firmware Updates

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in his or her module for production. To stay informed, sign up for the SDK Alert Me button on the tools page or www.ti.com/tool/cc3200sdk .

12.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3200MOD and support tools (see Figure 12-1).

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *CC3200MOD*). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

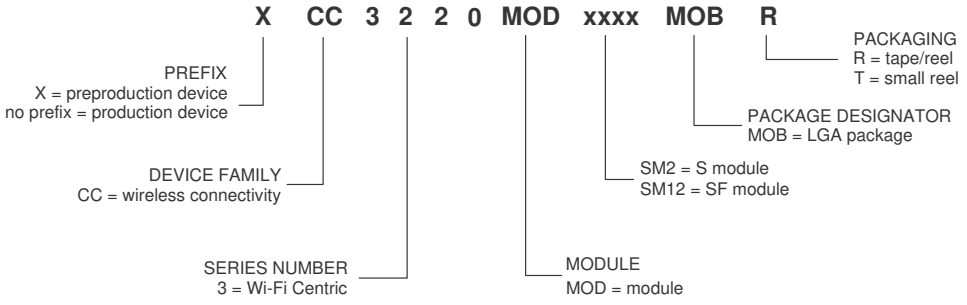


Figure 12-1. CC3200MOD Module Nomenclature

For orderable part numbers of CC3200MOD devices in the QFM package type, see Section 13.2, see ti.com, or contact your TI sales representative.

12.3 Documentation Support

The following documents describe the CC3200MOD processor and MPU. These documents are available online at www.ti.com.

SimpleLink™ Wi-Fi® CC3200 and Internet-of-Things Solution, a Single Chip Wireless MCU Technical Reference Manual

CC3200 Peripheral Driver Library User's Guide Documentation

12.4 Trademarks

Wi-Fi CERTIFIED™ is a trademark of Wi-Fi Alliance.
SimpleLink™ and Internet-on-a chip™ are trademarks of TI.
E2E™, Code Composer Studio™, DSP/BIOS™, and XDS™ are trademarks of Texas Instruments.
BoosterPack™ is a trademark of Texas Instruments.
Macrocell™ is a trademark of Kappa Global Inc.
Wi-Fi® and Wi-Fi Direct® are registered trademarks of Wi-Fi Alliance.
Thumb® is a registered trademark of Arm Limited.
ZigBee® is a registered trademark of ZigBee Alliance.
All other trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

13.1 Mechanical Drawing

Note

Maximum height of the module is 2.45 mm, because it includes a paper label on the top side. [1.5 + 0.88 + 0.07].

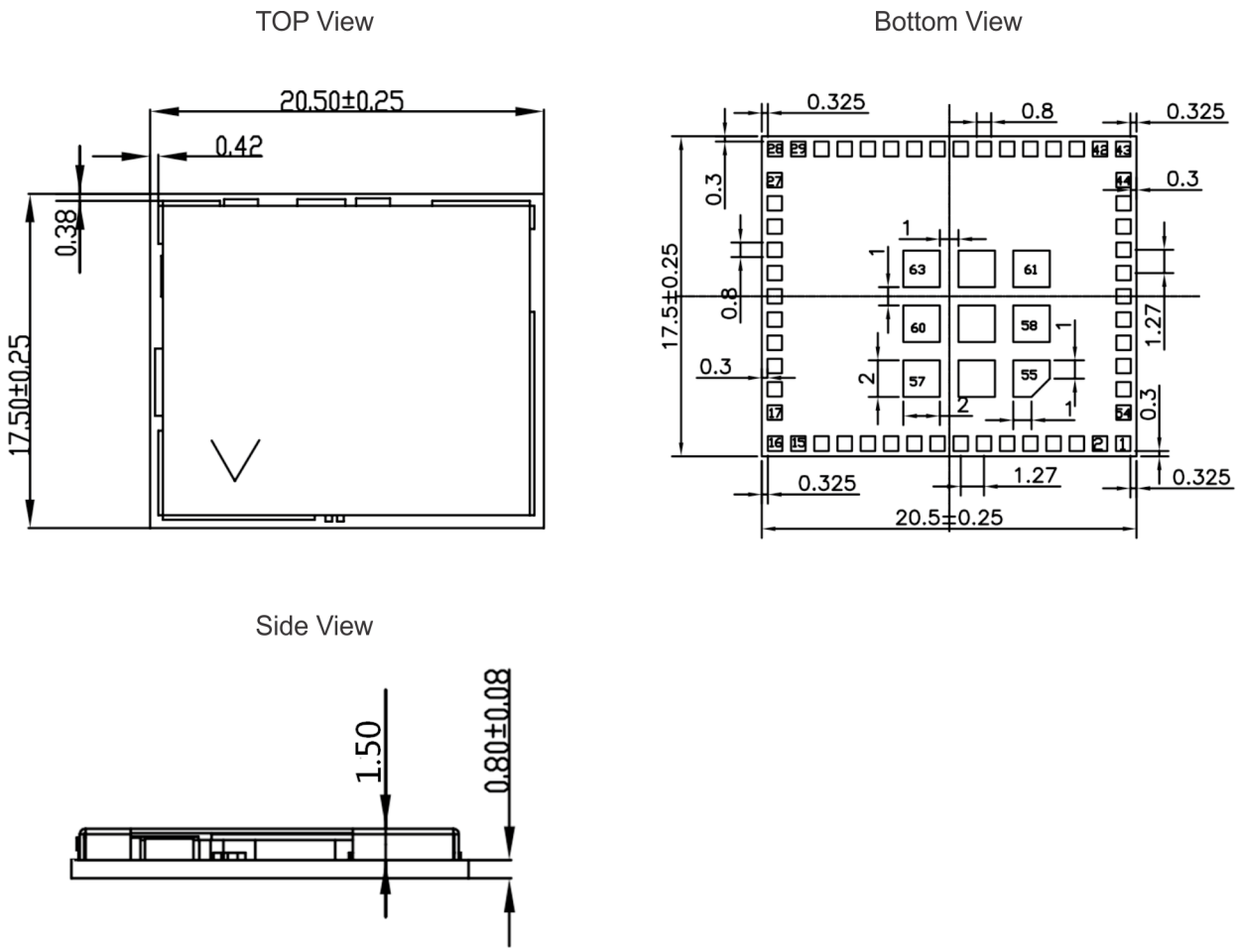


Figure 13-1. Mechanical Drawing

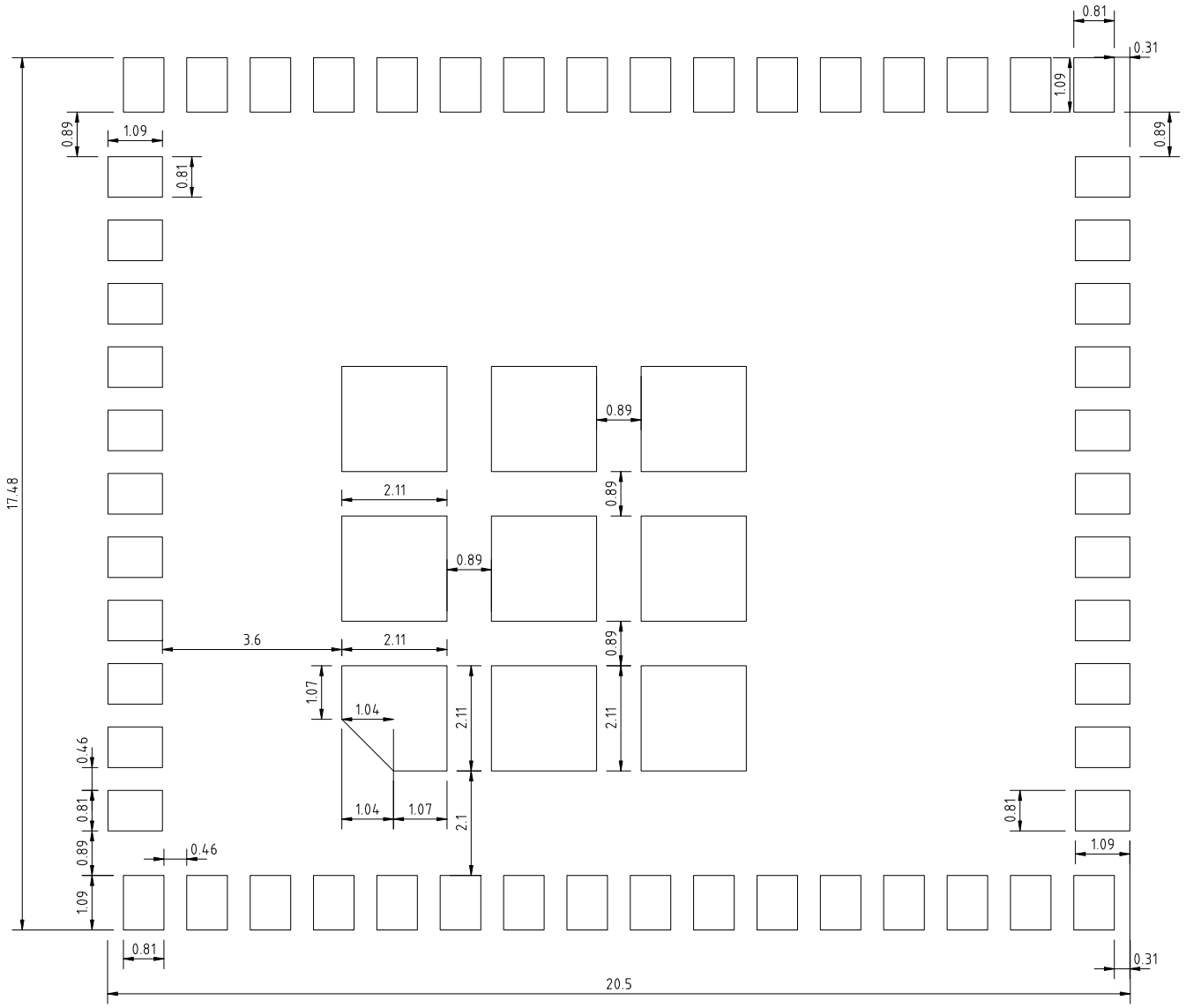


Figure 13-2. Land Pattern Drawing

Note

1. All dimensions are in mm.
2. Solder mask should be the same or 5% larger than the dimension of the pad
3. Solder paste must be the same as the pin for all peripheral pads. For ground pins, make the solder paste 20% smaller than the pad.

13.2 Package Option

We offer two reel size options for flexibility: a 750-unit reel and a 250-unit reel.

13.2.1 Packaging Information

Orderable Device	Status (1)	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL, Peak Temp (3)	Op Temp (°C)	Device Marking(4) (5)
CC3200MODR1M2AMOBR	ACTIVE	MOB	63	750	RoHS Exempt	Ni Au	3, 250°C	–20 to 70	CC3200MODR1M2AMOB
CC3200MODR1M2AMOBT	ACTIVE	MOB	63	250	RoHS Exempt	Ni Au	3, 250°C	–20 to 70	CC3200MODR1M2AMOB

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

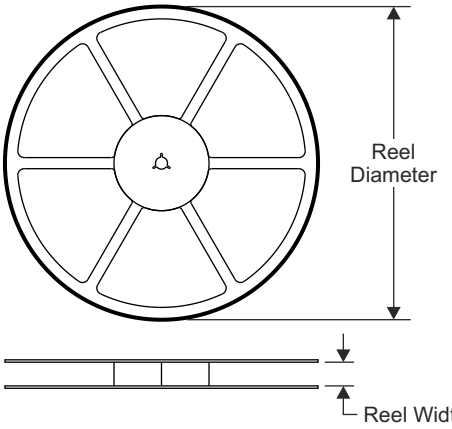
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

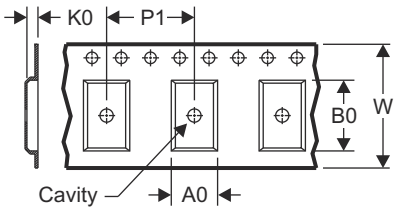
(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

13.2.2 Tape and Reel Information

REEL DIMENSIONS

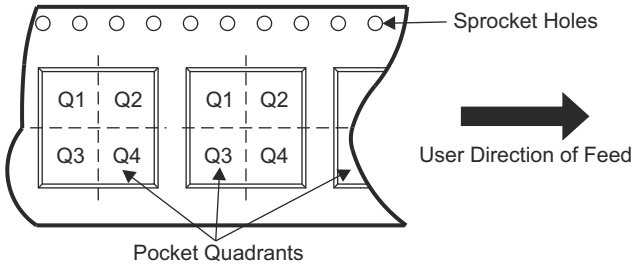


TAPE DIMENSIONS



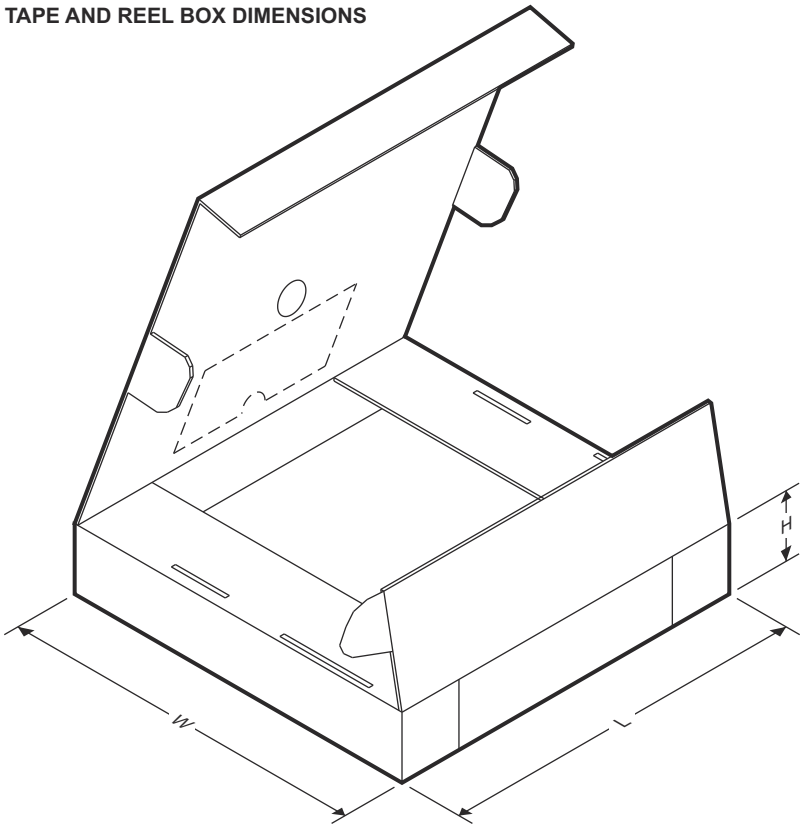
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3200MODR1M2AMOBR	MOB	63	750	330.0±2.0	44.0	17.85±0.10	20.85±0.10	2.50±0.10	24.00±0.10	44.00±0.30	Q1
CC3200MODR1M2AMOBT	MOB	63	250	330.0±2.0	44.0	17.85±0.10	20.85±0.10	2.50±0.10	24.00±0.10	44.00±0.30	Q1

TAPE AND REEL BOX DIMENSIONS



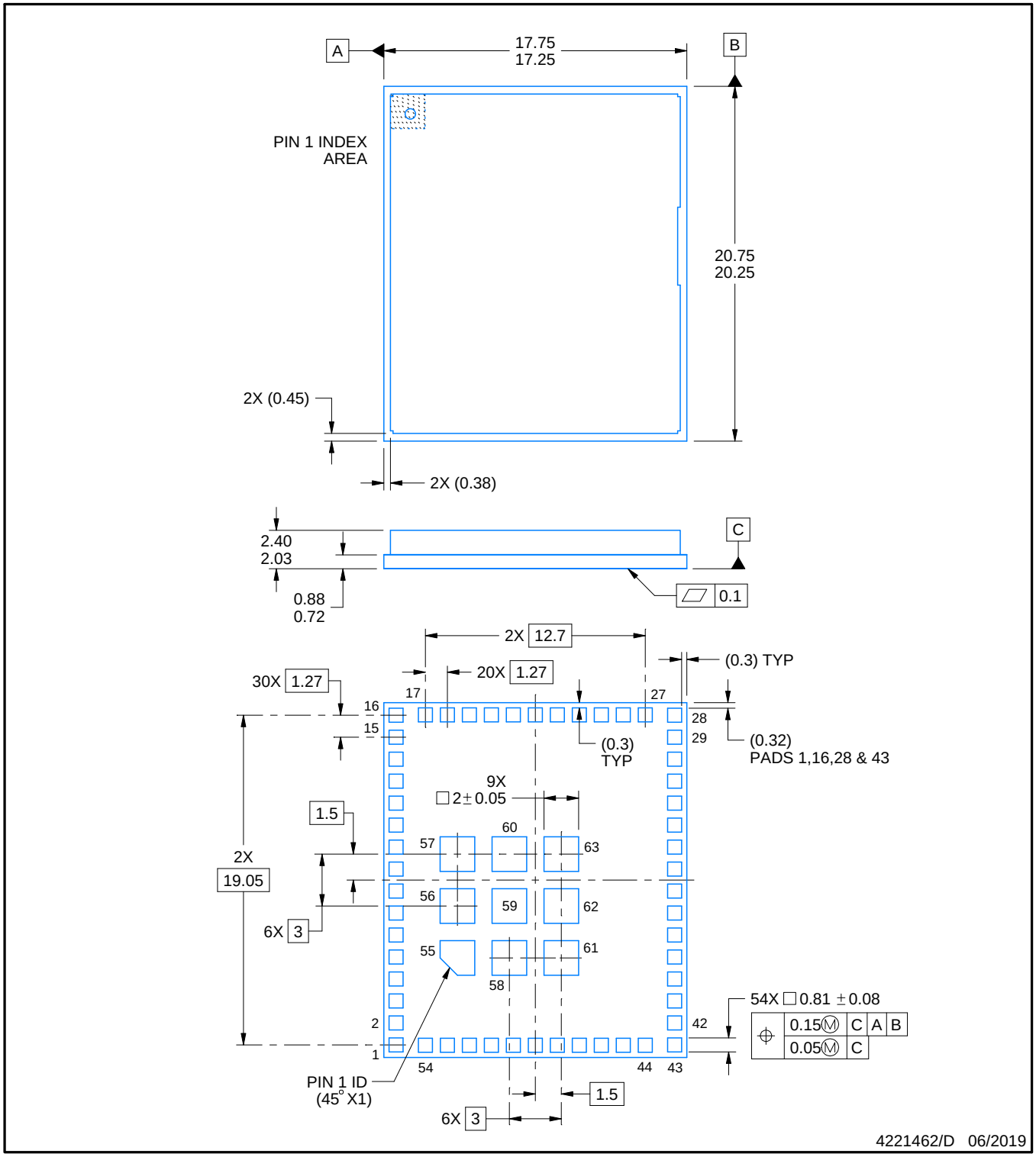
Device	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3200MODR1M2AMOBR	MOB	63	750	354.0	354.0	55.0
CC3200MODR1M2AMOBT	MOB	63	250	354.0	354.0	55.0

PACKAGE OUTLINE

MOB0063A

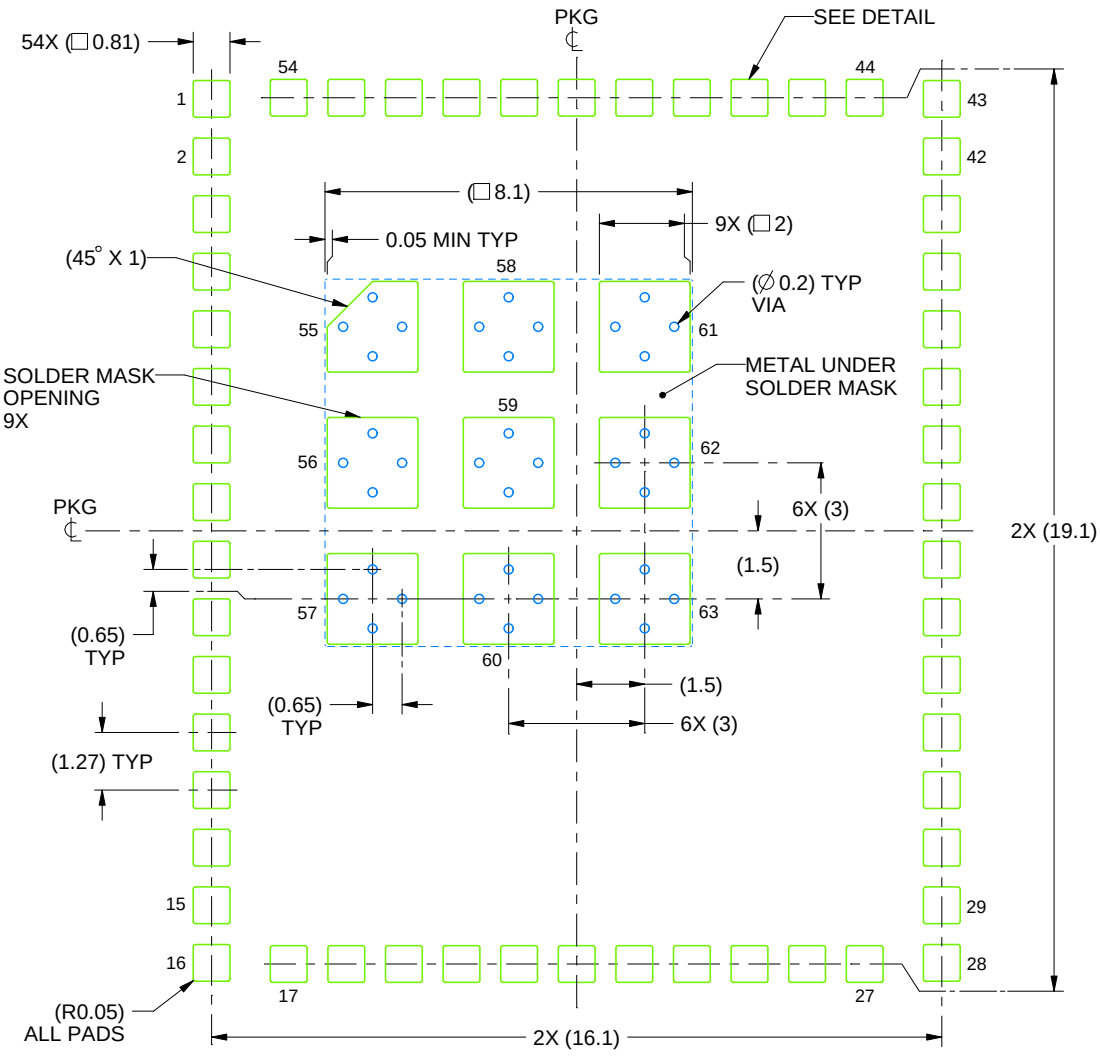
QFM - 2.4 mm max height

QUAD FLAT MODULE

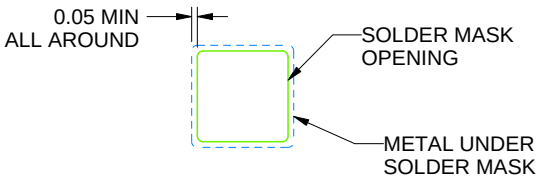


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:6X

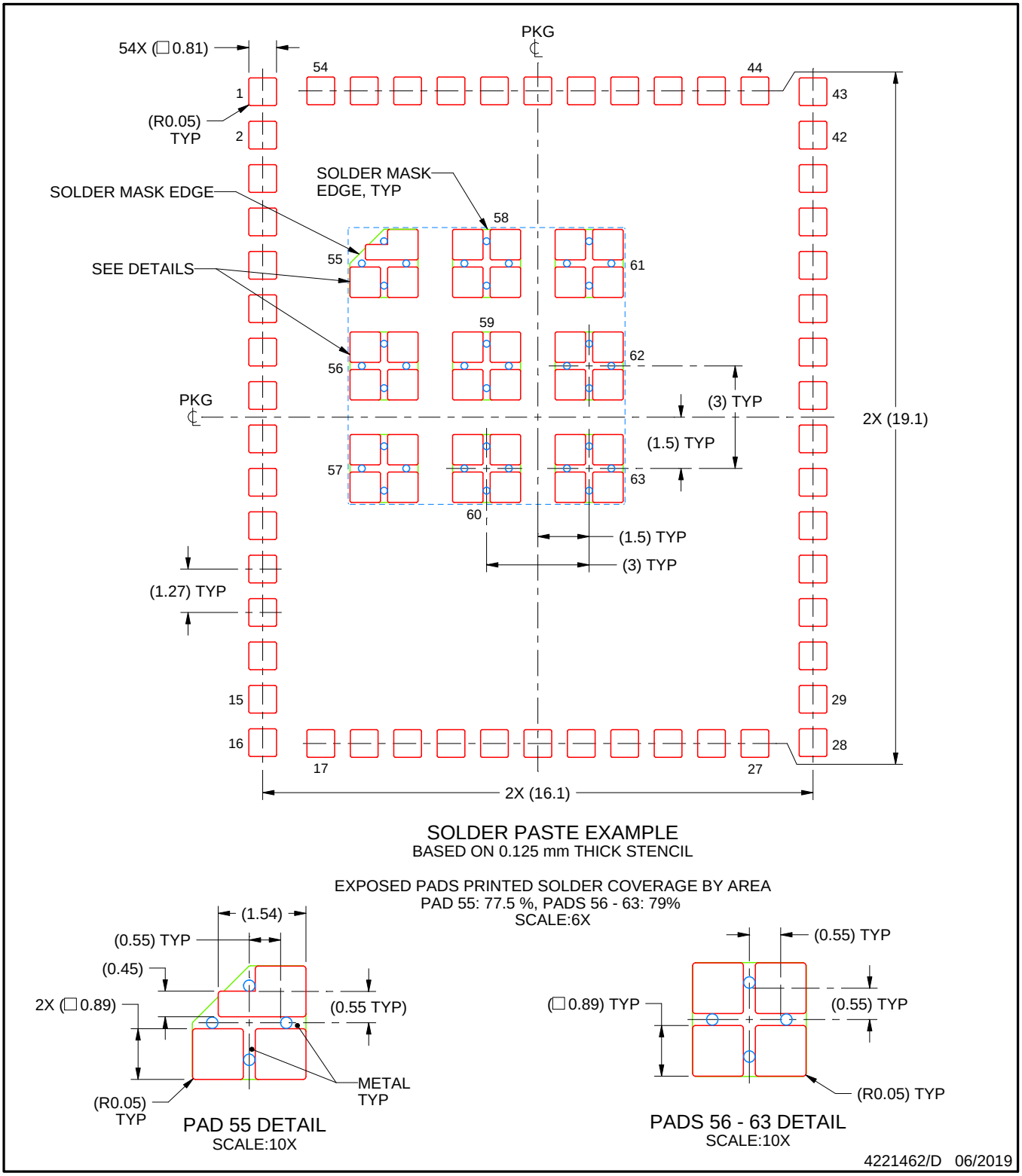


SIGNAL PADS DETAIL

4221462/D 06/2019

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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