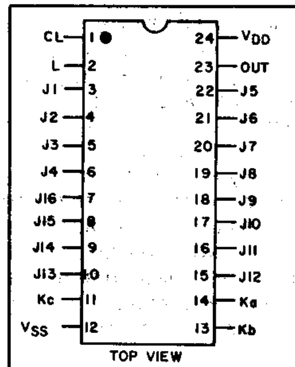
TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS109B – Revised June 2003

CD4059A Types

CMOS Programmable Divide-by-"N" Counter

Standard "A"-Series Types (3-to-15-Volt Rating)



TERMINAL DIAGRAM

■ CD4059 standard "A"-Series types are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam Inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number from which counting-down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table 1. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the master preset mode before the ÷5 mode is selected.

Whenever the master preset mode is used, control signals Kb=0 and Kc=0 must be applied for at least 3 full clock pulses.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig.1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used the counter jumps back to the "JAM" count when the output pulse appears.

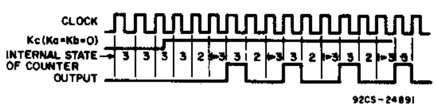


Fig.1 – Total count of 3.

A "1" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "0". If the Latch Enable is "0", the output pulse will remain high for only 1 cycle of the clock-input signal.

As illustrated in the sample applications, this device is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-"N" counters are an integral part of the synthesizer phase-locked-loop subsystem. The CD4059A can also be used to perform the synthesizer "Fixed Divide-by-R" counting function. It is also useful in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time out" timers.

Operational and Performance Features:

- **Synchronous Programmable ÷ N Counter: N = 3 to 9999 or 15,999**
- **Presettable down-counter**
- **Fully static operation**
- **Mode-select control of initial decade counting function (÷ 10,8,5,4,2)**
- **T^2L drive capability**
- **Master preset initialization**
- **Latchable ÷ N output**
- **Quiescent current specified to 15 volts**
- **Max. input leakage current of 1 μA at 15 volts, full package-temperature range**
- **1 volt noise margin, full package-temperature range**
- **5-V and 10-V parametric ratings**

Applications

- **Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.**
- **Fixed or programmable frequency division**
- **"Time out" timer for consumer-application industrial controls**
- **Companion Application Note, ICAN-6374, "Application of the CMOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"**

The CD4059A-series types are supplied in 24-lead dual-in-line plastic packages (E suffix), and 24-lead small-outline packages (M and M96 suffixes).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... -0.5V to +15V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5V to V_{DD} +0.5V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearly to 100mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits -55°	-40°	+85°	+125°	+25° Min.	Typ.	Max.	Units
Quiescent Device Current, I_L Max.			5	10	10	700	300	–	0.02	10	µA
			10	20	20	200	400	–	0.02	20	
			15	–	–	–	–	–	–	500	
Output Voltage: Low Level, V_{OL} Max.		0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
High Level, V_{OH} Min.		0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
Noise Immunity: Inputs Low, V_{NL} Min.			5	1.5				1.5	2.25	–	V
			10	3				3	4.5	–	
Inputs High, V_{NH} Min.			5	1.5				1	2.25	–	
			10	3				3	4.5	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1							V
	9		10	1							
Inputs High, V_{NMH} Min.	0.5		5	1							
	1		10	1							
Output Drive Current: N-Channel (Sink) I_{DN} Min.	0.4		5	2.5	2.3	1.6	1.4	2	4	–	mA
	0.5		10	5	4.7	3.3	2.8	4	9	–	
P-Channel (Source) I_{DP} Min.	2.5		5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	4.6		5	-0.5	-0.45	-0.36	-0.3	-0.4	-0.8	–	
	9.5		10	-1.1	-1	-0.75	-0.65	-0.9	-1.8	–	
Input Leakage Current:* I_{IL}, I_{IH} Max.			15	±1					$±10^{-5}$	±1	µA

* Any Input

OPERATING CONDITIONS AT T_A = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	–	3	12	V
Clock Pulse Width	5	200	–	ns
	10	100	–	
Clock Input Frequency	5	–	1.5	MHz
	10	–	3	
Clock Input Rise and Fall Time	5	–	15	µs
	10	–	5	

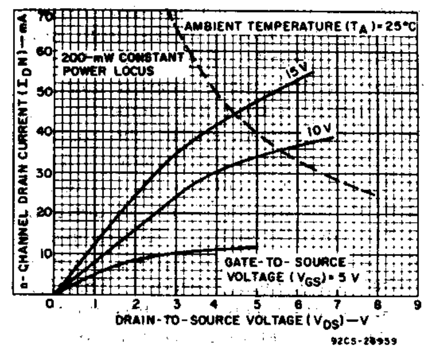


Fig.2 – Minimum output n-channel drain characteristics.

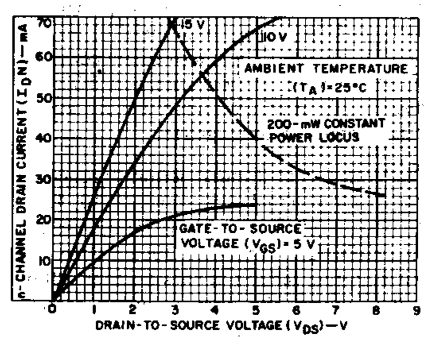


Fig.3 – Typical output n-channel drain characteristics.

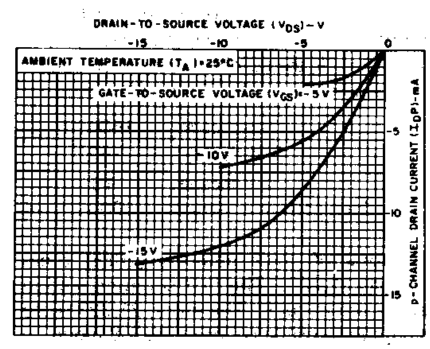
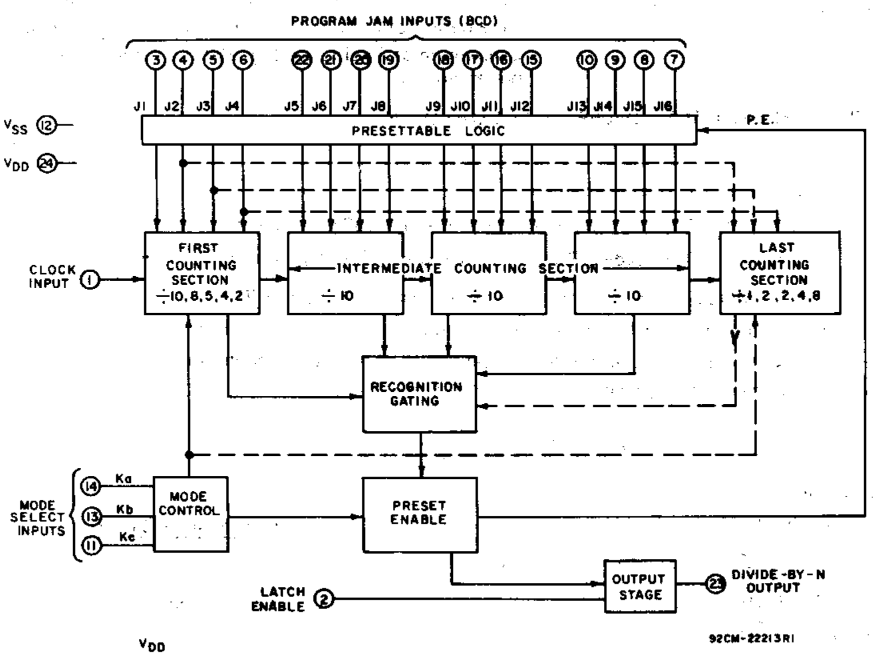
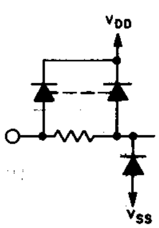


Fig.4 – Minimum output p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C, C_L = 50 pF, Input t_r,t_f = 20 ns, R_L = 200 kΩ

CHARACTERISTIC		CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES			UNITS
			Min.	Typ.	Max.	
Propagation Delay Time; t_{PHL}, t_{PLH}		5	–	180	360	ns
		10	–	90	180	
Transition Time:	t_{THL}	5	–	35	70	ns
		10	–	20	40	
	t_{TLH}	5	–	100	200	
		10	–	50	100	
Maximum Clock Input Frequency, f_{CL}		5	1.5	3	–	MHz
		10	3	6	–	
Average Input Capacitance, C_I (any input)		–	–	5	–	pF





ALL INPUTS (TERMS. 1-11, 13-22) PROTECTED BY CMOS PROTECTION NETWORK

Fig.5 — Functional block diagram.

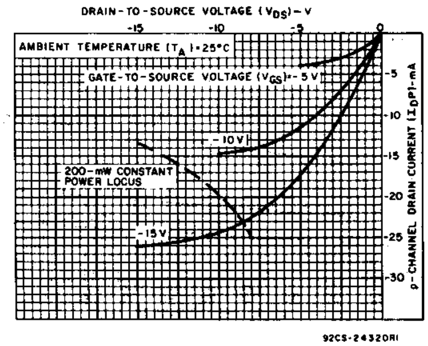


Fig.6 — Typical output p-channel drain characteristics.

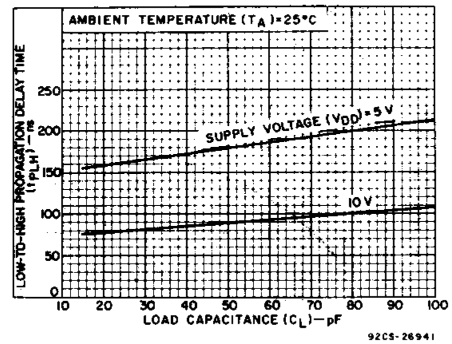


Fig.7 — Typical low-to-high propagation delay time vs. load capacitance.

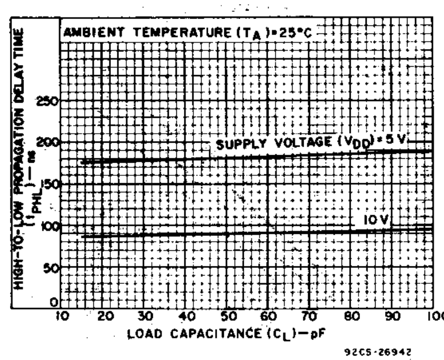


Fig.8 — Typical high-to-low propagation delay time vs. load capacitance.

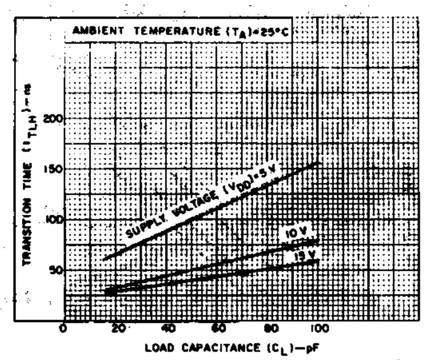


Fig.9 — Typical low-to-high transition time vs. load capacitance.

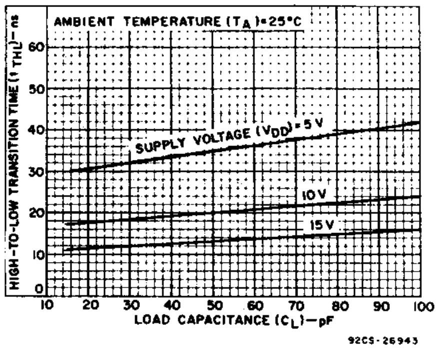


Fig.10 – Typical high-to-low transition time vs. load capacitance.

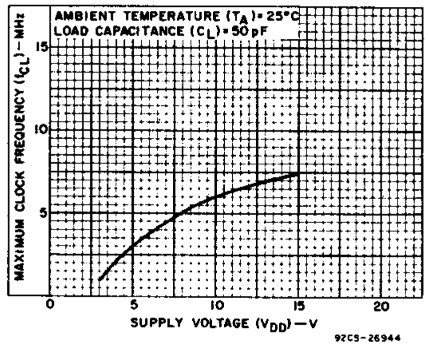


Fig.11 – Typical max. clock frequency vs. supply voltage.

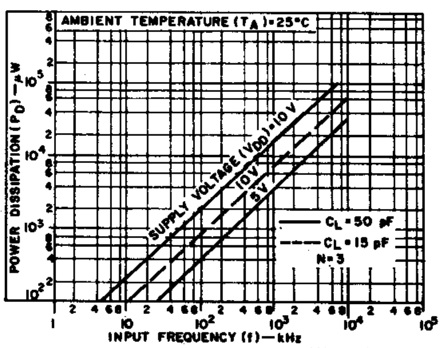


Fig.12 – Typical power dissipation vs. input frequency.

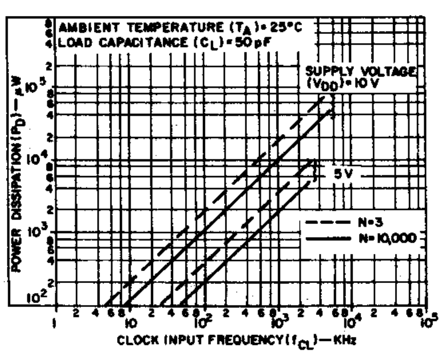


Fig.13 – Typical power dissipation vs. clock input frequency.

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Di-vides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	–	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			–	–

X = Don't Care

▲ J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "O" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts. See Fig. 21 for a suggested external preset circuit.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

$$N = [MODE^*] \quad [1000 \times \text{Decade 5 Preset} + 100X\ \text{Decade 4 Preset} + 10X\ \text{Decade 3 Preset} + 1X\ \text{Decade 2 Preset}] + \text{Decade 1 Preset} \qquad (1)$$

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \qquad (2)$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values
5 | 8479
Mode ↗ ↖ N

MODE SELECT = 5

Ka	Kb	Kc
1	0	1

PROGRAM JAM INPUTS (BCD)

4		1		5				9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

MODE SELECT = 8

B) N = 12382, Mode = 8

1547 + 6
8 | 12382

Ka	Kb	Kc
0	0	1

PROGRAM JAM INPUTS

6			1	7				4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6

N = 12382

MODE SELECT = 10

C) N = 8479, Mode = 10

$$10 \overline{)8479} = 0847 + 9$$

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

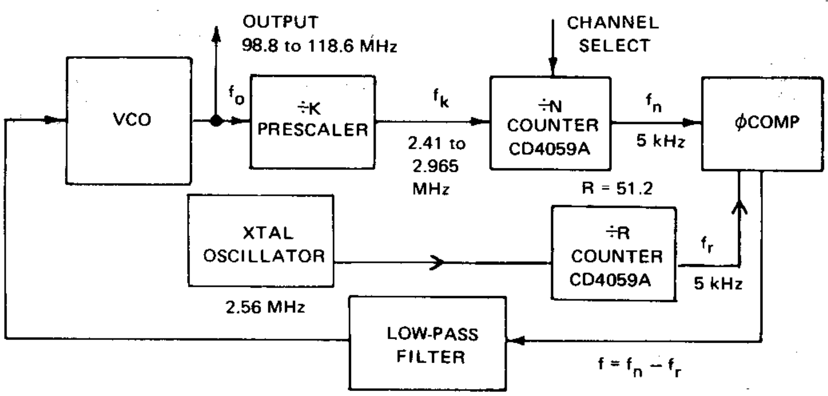
9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9

N = 8479

DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER



1) Calculating Min & Max "N" Values :

Output Freq. Range (f_o) = 98.8 to 118.6 MHz

Channel Spacing Freq. (f_c) = 200 kHz

Division Factor (k) = 40

$$\text{Reference Freq. (fr)} = \frac{f_c}{k} = \frac{200}{40}\ \text{kHz} = 5\ \text{kHz}$$

$$f_k = \frac{f_o}{40}\ :\ f_k\text{Max.} = \frac{118.6\ \text{MHz}}{40} = 2.965\ \text{MHz};\ f_k\text{Min} = \frac{98.8\ \text{MHz}}{40} = 2.47\ \text{MHz}$$

$$\therefore\ N = \frac{f_o}{f_c}$$

$$N_{Max} = \frac{118.6\ \text{MHz}}{200\ \text{kHz}} = 593 \qquad N_{Min} = \frac{98.8\ \text{MHz}}{200\ \text{kHz}} = 494 \qquad R = \frac{2.56\ \text{MHz}}{5\ \text{kHz}} = 512$$

"CASCADING" VIA OTHER COUNTERS

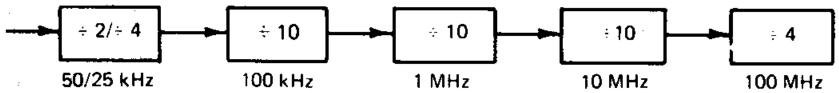
Fig. 14 shows a BCD-switch compatible arrangement suitable for ÷ 8 and ÷ 5 modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

The clock of the CD4013A may be driven directly from the output of the CD4059A, as shown by dashed option (1), or by the inverted output of the CD4059A, option (2). If option (2) is used the CD4029A cannot count cycles shorter than 3. If option (1) is used propagation delay problems may occur at high counting speeds.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I.. The dual flip-flop wired to produce a ÷ 3 count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the ÷ N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

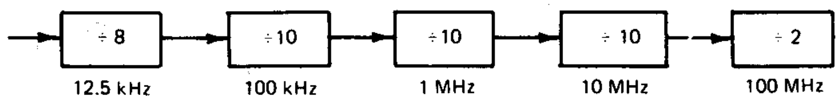
2) ÷ N Counter Configuration for UHF – 220 to 400 MHz
Channel Spacing: 50 kHz or 25 kHz



$$N_{Max} = \frac{400\text{ MHz}}{25\text{ kHz}} = 16{,}000 \qquad N_{Max} = \frac{400\text{ MHz}}{50\text{ kHz}} = 8{,}000$$

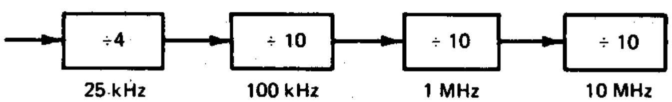
$$N_{Min} = \frac{220\text{ MHz}}{25\text{ kHz}} = 8{,}800 \qquad N_{Min} = \frac{220\text{ MHz}}{50\text{ kHz}} = 4{,}400$$

3) ÷ N Counter Configuration to VHF – 116 MHz
Channel Spacing = 12.5 kHz



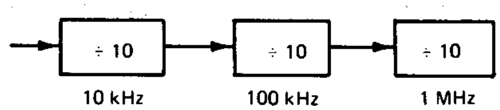
$$N_{Max} = \frac{160\text{ MHz}}{12.5\text{ kHz}} = 12{,}800 \qquad N_{Min} = \frac{116\text{ MHz}}{12.5\text{ kHz}} = 9{,}300$$

4) ÷ N Counter Configuration for VHF – 30 to 80 MHz
Channel Spacing: 25 kHz



$$N_{Max} = \frac{80\text{ MHz}}{25\text{ kHz}} = 3{,}200 \qquad N_{Min} = \frac{30\text{ MHz}}{25\text{ kHz}} = 1200$$

5) ÷ N Counter Configuration for AM – 995 to 2055 kHz
Channel Spacing = 10 kHz



$$N_{Max} = \frac{2055\text{ kHz}}{10\text{ kHz}} = 205 \qquad N_{Min} = \frac{995\text{ kHz}}{10\text{ kHz}} = 99$$

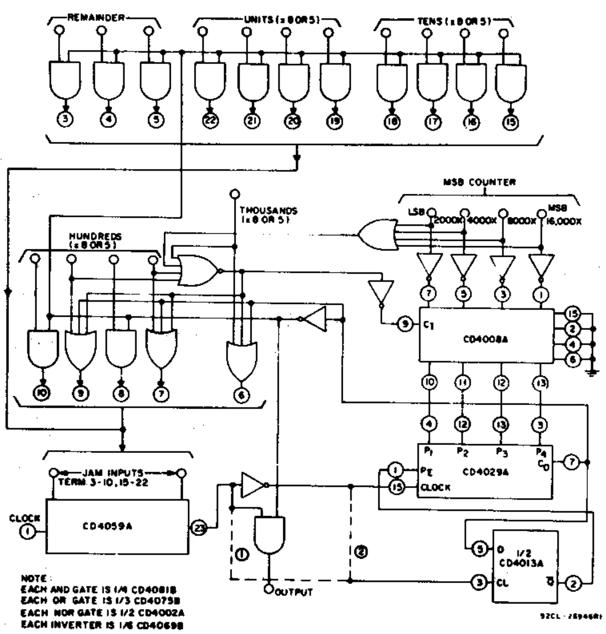


Fig.14 – BCD switch-compatible ÷N system of the most general kind.

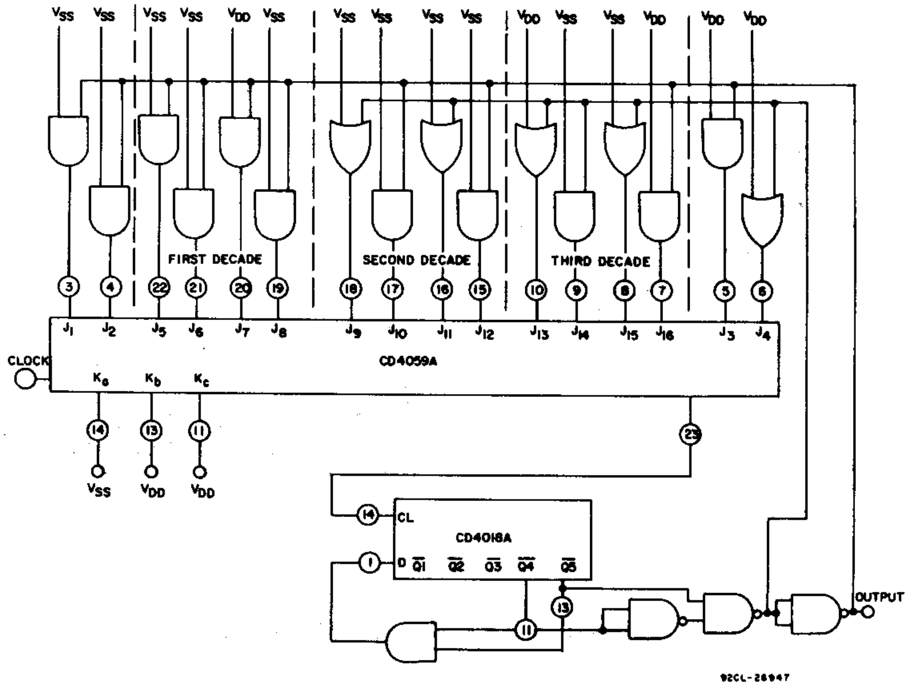


Fig.15 – Dividing by any number from 88,003 to 103,999.

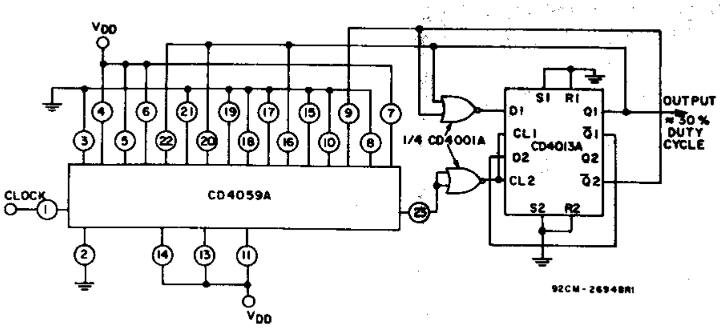


Fig.16 – Division by 47,690 in ÷2 mode.

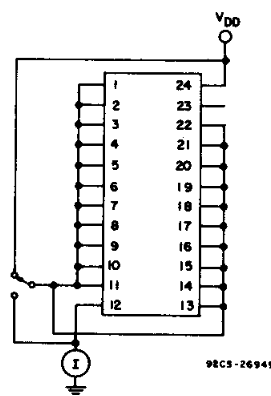


Fig.17 – Quiescent device current test circuit.

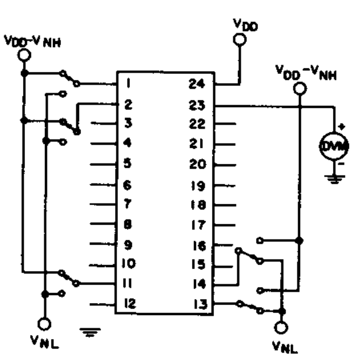


Fig.18 – Noise immunity test circuit.

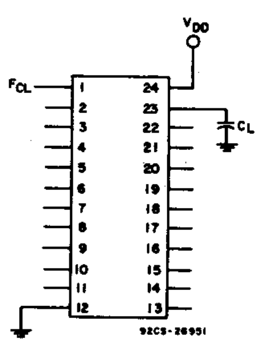


Fig.19 – Power dissipation test circuit (all ÷ modes).

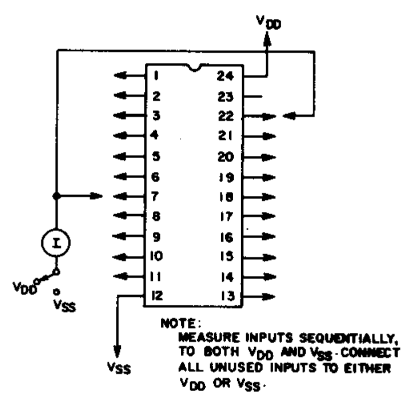
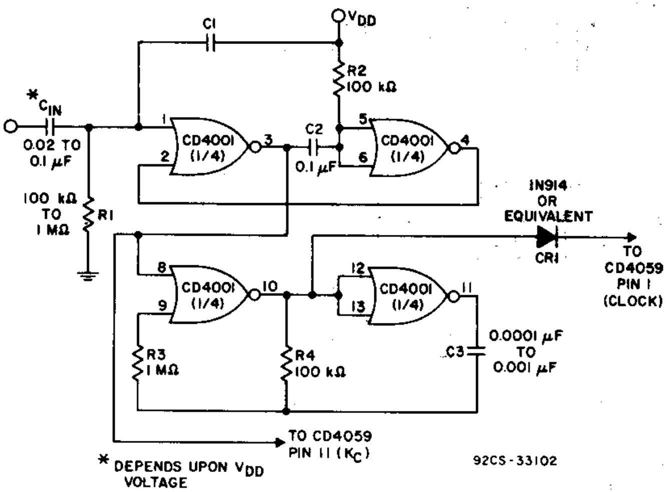
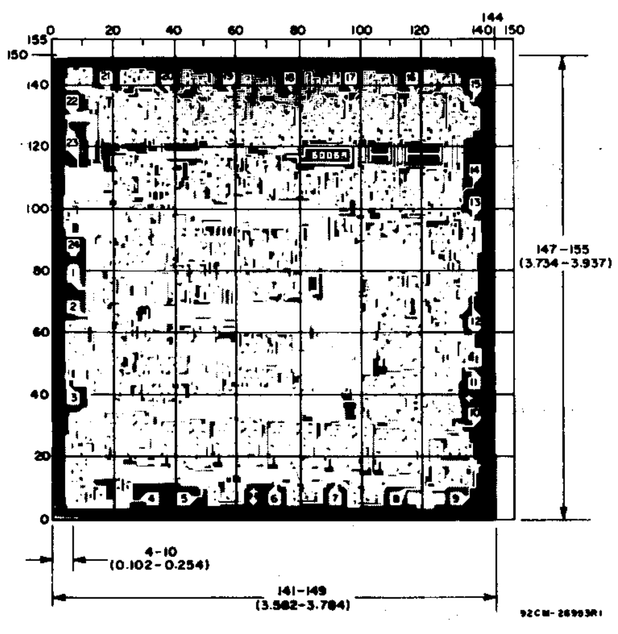


Fig.20 – Input leakage current test circuit.



For changing from any mode other than mode 5 (with power on), apply positive pulse to C_{in}. This circuit automatically selects master preset mode (K_b = 0, K_c = 0) before going into the select conditions for mode 5 (K_a = 1, K_b = 0, K = 1). The selection of C_1 and C_2 is critical. C_1 is determined by the VDD voltage--the lower VDD's need larger C_1's. C_2 must be 0.1 μF or larger.

Fig.21 - CD4059A mode 5 power on master preset circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4059AH.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4059AD3	Last Time Buy	Production	CDIP SB (JD) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4059AD/3
CD4059AD3.A	Last Time Buy	Production	CDIP SB (JD) | 24	15 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4059AD/3
CD4059AM	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4059AM
CD4059AM.A	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4059AM
CD4059AMG4	Active	Production	SOIC (DW) | 24	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4059AM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

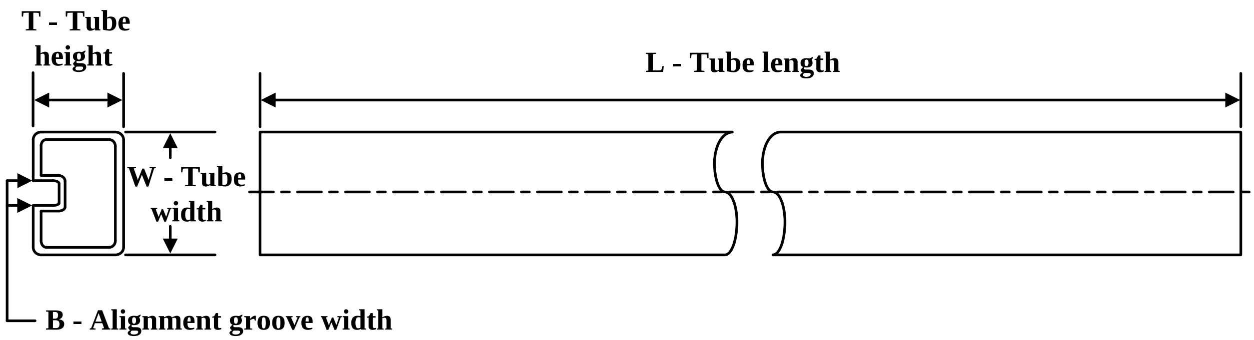
OTHER QUALIFIED VERSIONS OF CD4059A, CD4059A-MIL :

- Catalog : CD4059A
- Military : CD4059A-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE

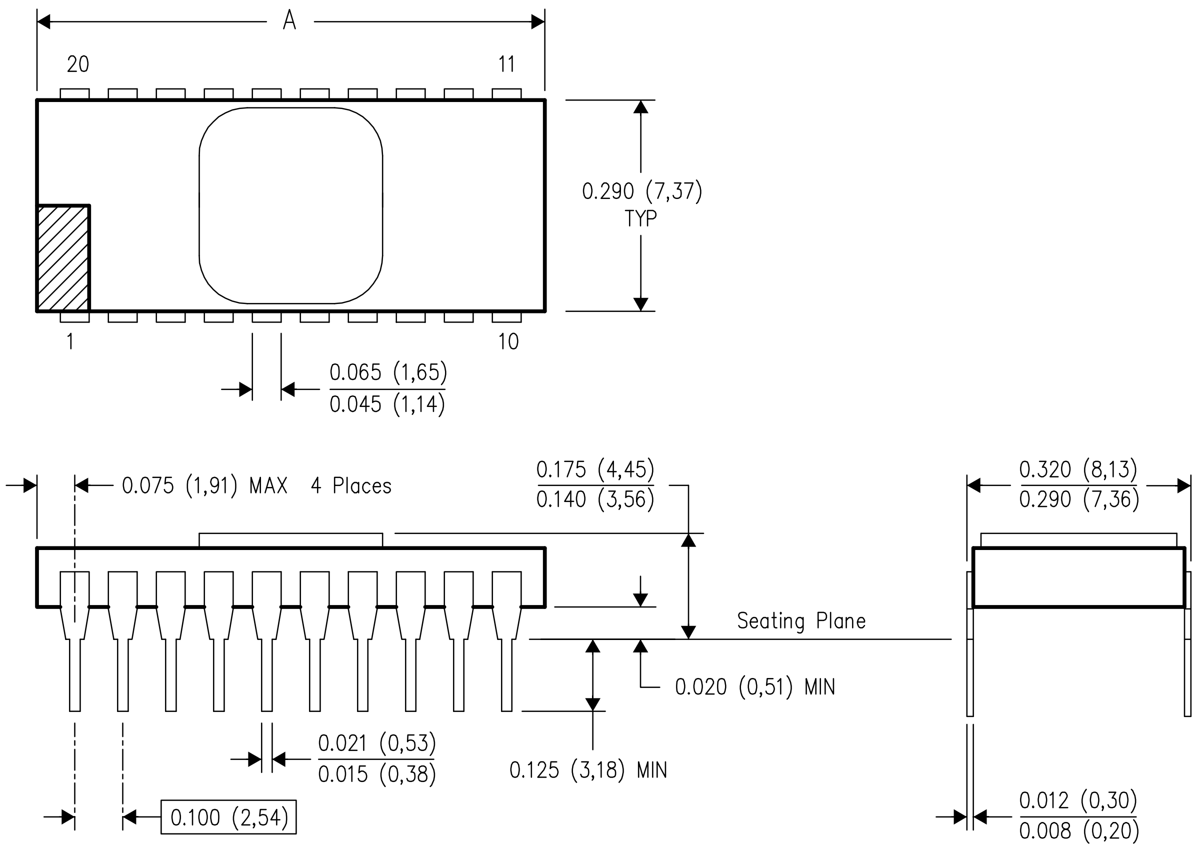


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4059AM	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4059AM.A	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD4059AMG4	DW	SOIC	24	25	506.98	12.7	4826	6.6

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN

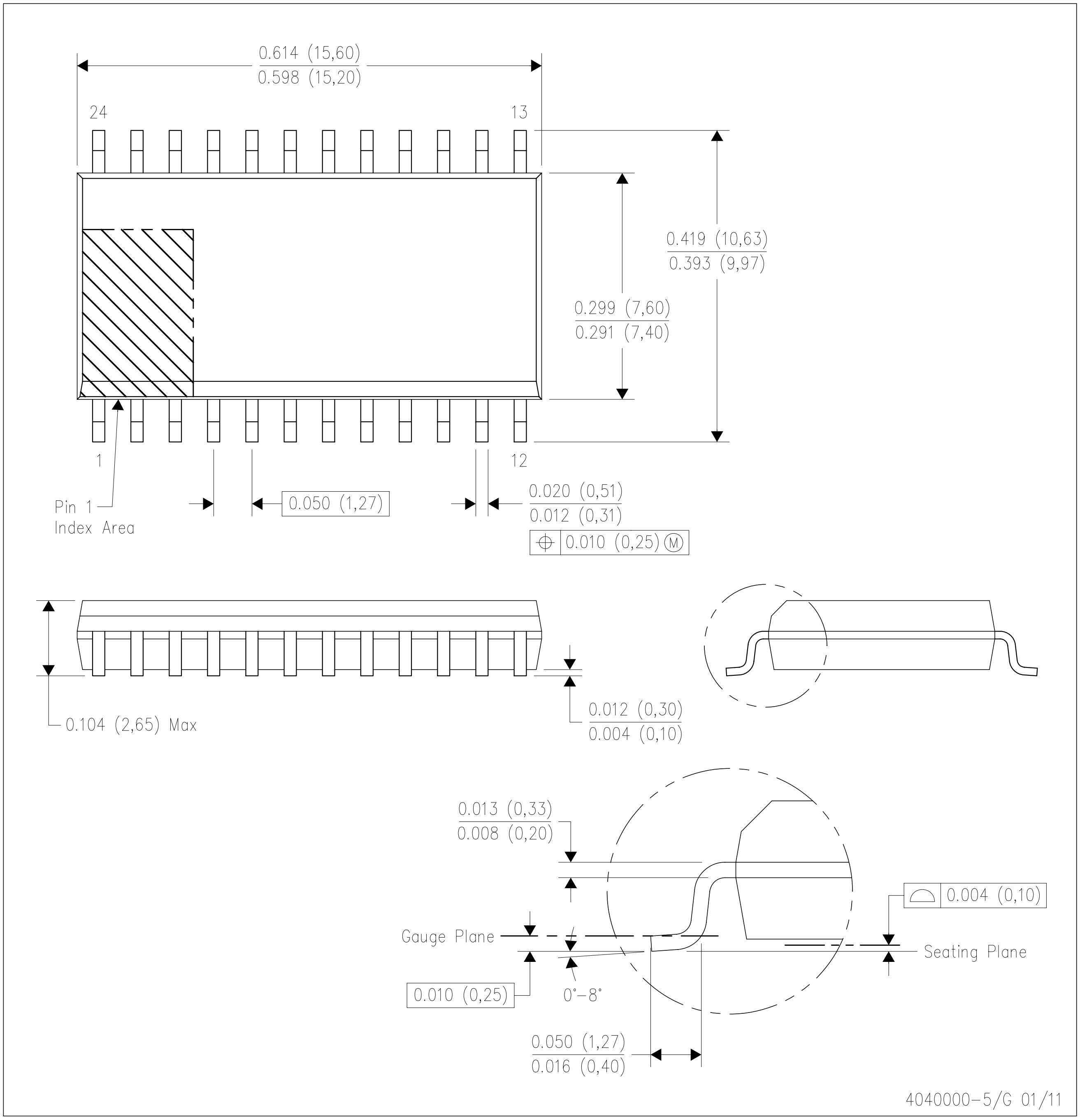


DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

DW (R-PDSO-G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AD.