

CD4518B, CD4520B Types

CMOS Dual Up-Counters

High-Voltage Types (20-Volt Rating)

CD4518B Dual BCD Up-Counter
CD4520B Dual Binary Up-Counter

■ CD4518 Dual BCD Up-Counter and CD4520 Dual Binary Up-Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines.

The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

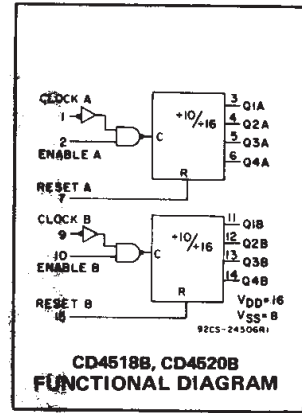
The CD4518B and CD4520B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	
Voltages referenced to V _{SS} Terminal) -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS -0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ±10mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55°C to +100°C 500mW
For T _A = +100°C to +125°C Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T _A) -55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg}) -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max +265°C

Features:

- Medium-speed operation – 6-MHz typical clock frequency at 10 V_{DD}
- Positive- or negative-edge triggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V
2 V at V_{DD} = 10 V
2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



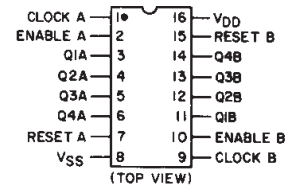
Applications:

- Multistage synchronous counting
- Multistage ripple counting
- Frequency dividers

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care 1 ≡ High State 0 ≡ Low State



**CD4518B, CD4520B
TERMINAL ASSIGNMENT**

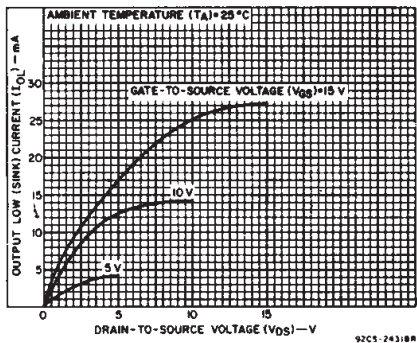


Fig. 1 – Typical output low (sink) current characteristics.

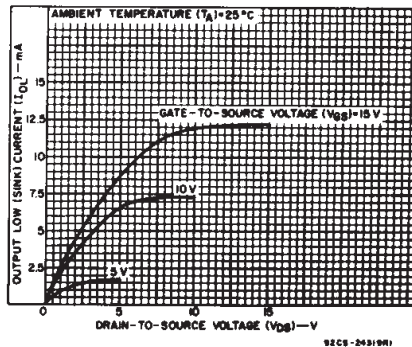


Fig. 2 – Minimum output low (sink) current characteristics.

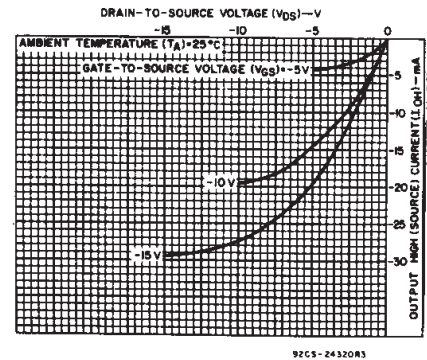


Fig. 3 – Typical output high (source) current characteristics.

CD4518B, CD4520B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55			+25				
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0,04	5	μA
	—	0,10	10	10	10	300	300	—	0,04	10	
	—	0,15	15	20	20	600	600	—	0,04	20	
	—	0,20	20	100	100	3000	3000	—	0,08	100	
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0,05			—			0	V
	—	0,10	10	0,05			—			0	
	—	0,15	15	0,05			—			0	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4,95			4,95			5	V
	—	0,10	10	9,95			9,95			10	
	—	0,15	15	14,95			14,95			15	
Input Low Voltage, V _{IL} Max.	0,5, 4,5	—	5	1,5			—			1,5	V
	1,9	—	10	3			—			3	
	1,5, 13,5	—	15	4			—			4	
Input High Voltage, V _{IH} Min.	0,5, 4,5	—	5	3,5			3,5			—	V
	1,9	—	10	7			7			—	
	1,5, 13,5	—	15	11			11			—	
Input Current I _{IN} Max.	—	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA

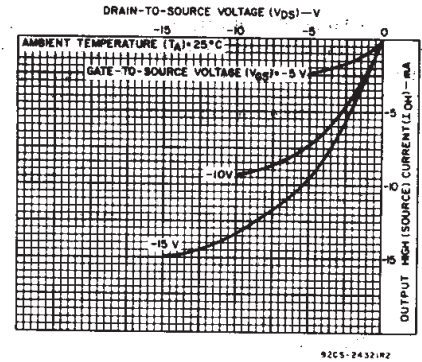


Fig. 4 — Minimum output high (source) current characteristics.

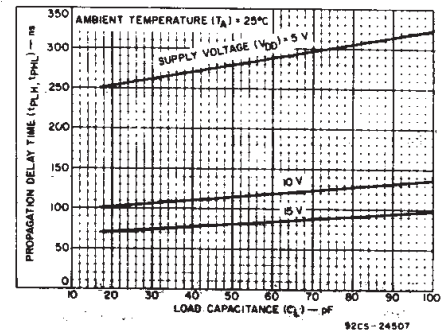


Fig. 5 — Typical propagation delay vs. load capacitance, clock or enable to output.

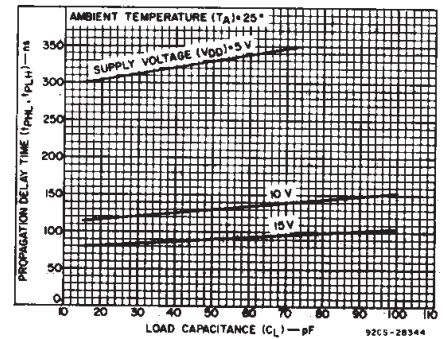


Fig. 6 — Typical propagation delay time vs. load capacitance, reset to output.

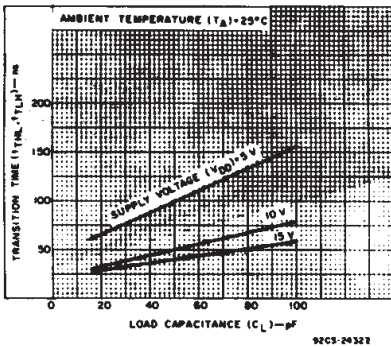


Fig. 7 — Typical transition time vs. load capacitance.

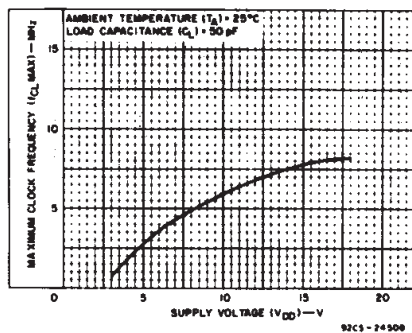


Fig. 8 — Typical maximum-clock-frequency vs. supply voltage.

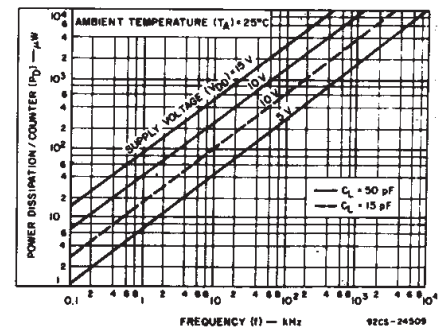


Fig. 9 — Typical power dissipation characteristics.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4518B, CD4520B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply Voltage Range (For T_A =Full Package Temperature Range)		3	18	V
Enable Pulse Width, t_W	5	400	—	ns
	10	200	—	
	15	140	—	
Clock Pulse Width, t_W	5	200	—	ns
	10	100	—	
	15	70	—	
Clock Input Frequency, f_{CL}	5		1.5	MHz
	10	dc	3	
	15		4	
Clock Rise or Fall Time, t_{rCL} or t_{fCL} :	5	—	15	μs
	10	—	5	
	15	—	5	
Reset Pulse Width, t_W	5	250	—	ns
	10	110	—	
	15	80	—	

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$:

Input $t_r, t_f = 20 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		V _{DD} V	Min.	Typ.		Max.
Propagation Delay Time, t_{PHL} , t_{PLH} : Clock or Enable to Output		5	—	280	560	ns
		10	—	115	230	
		15	—	80	160	
Reset to Output		5	—	330	650	ns
		10	—	130	225	
		15	—	90	170	
Transition Time, t_{THL} , t_{TLH}		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Maximum Clock Input Frequency, f_{CL}		5	1.5	3	—	MHz
		10	3	6	—	
		15	4	8	—	
Minimum Clock Pulse Width, t_W		5		100	200	ns
		10		50	100	
		15		35	70	
Clock Rise or Fall Time, t_r or t_f :		5	—	—	15	μs
		10, 15	—	—	5	
Minimum Reset Pulse Width, t_W		5	—	125	250	ns
		10	—	55	110	
		15	—	40	80	
Minimum Enable Pulse Width, t_W		5	—	200	400	ns
		10	—	100	200	
		15	—	70	140	
Input Capacitance, C_{iN}	Any Input		5	7.5	pF	

TEST CIRCUITS

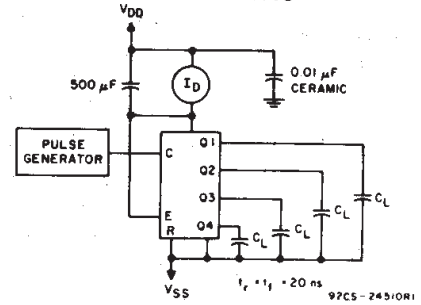


Fig. 10 — Dynamic power dissipation.

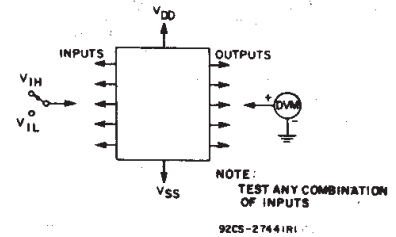


Fig. 11 — Input voltage.

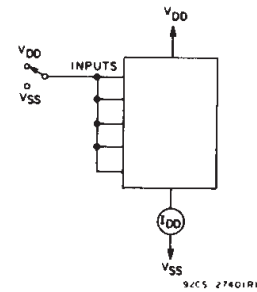


Fig. 12 — Quiescent device current test circuit.

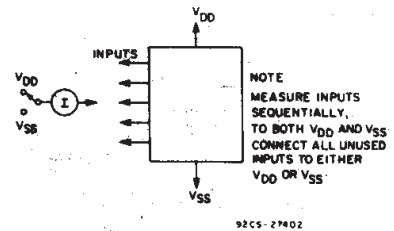


Fig. 13 — Input leakage-current test circuit.

CD4518B, CD4520B Types

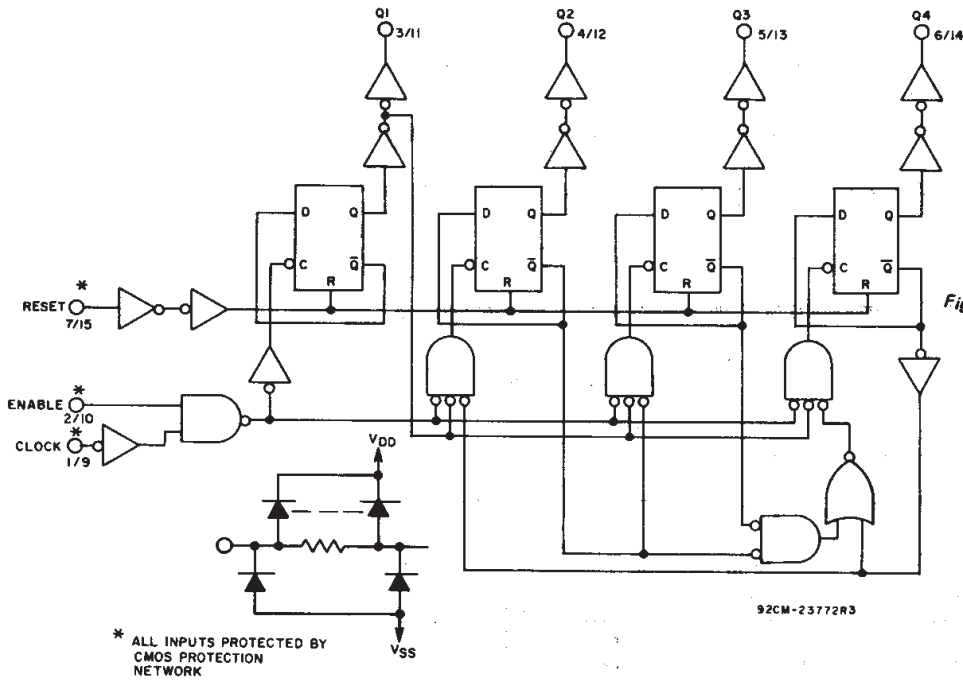


Fig. 14 — Decade counter (CD4518B) logic diagram for one of two identical counters.

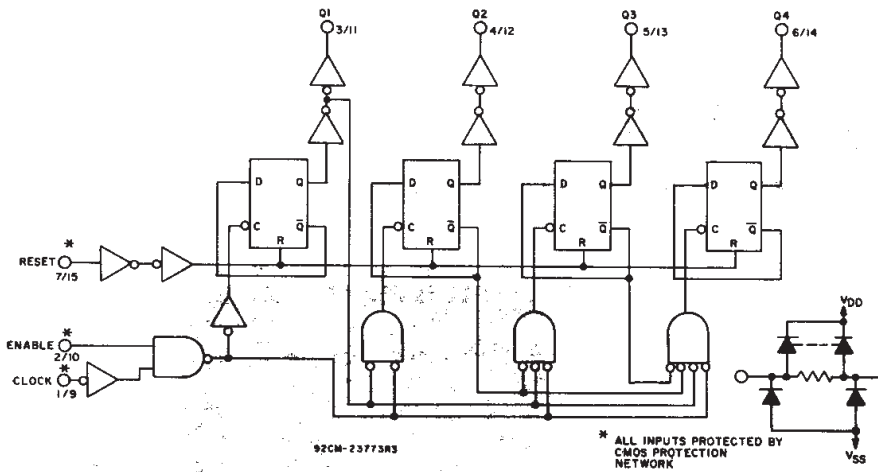


Fig. 15 — Binary counter (CD4520B) logic diagram for one of two identical counters.

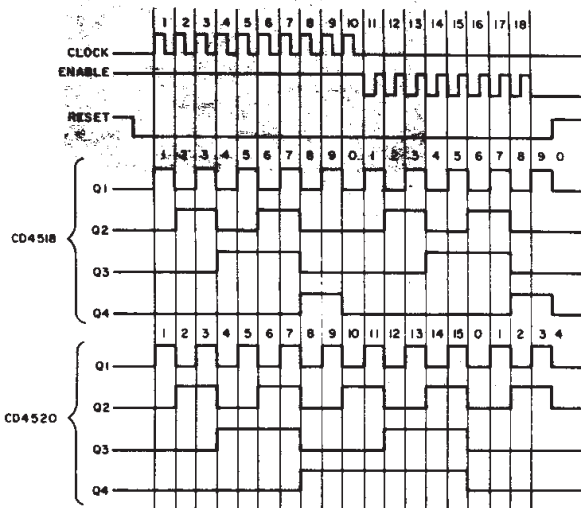


Fig. 16 — Timing diagrams for CD4518B and CD4520B.

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HIGH VOLTAGE ICs

CD4518B, CD4520B Types

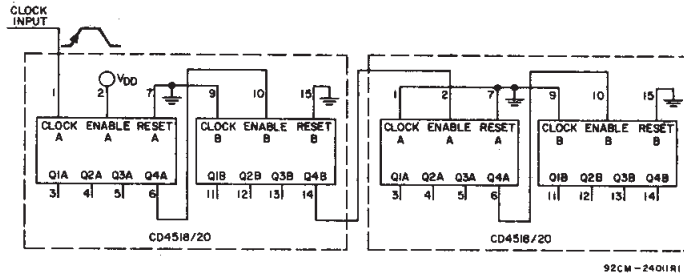
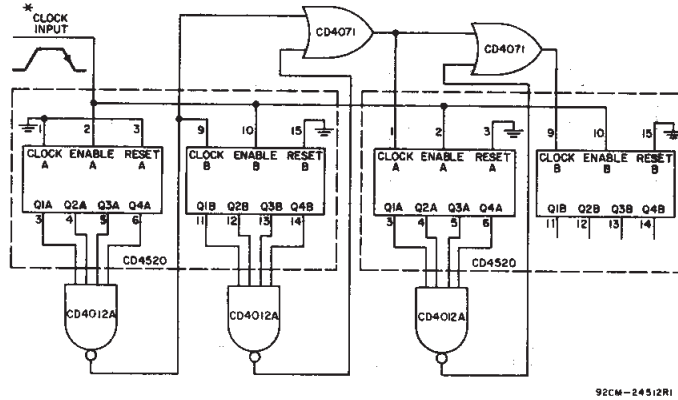
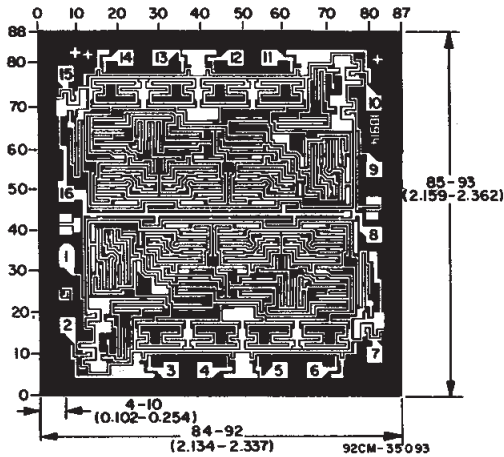


Fig. 17 - Ripple cascading of four counters with positive edge triggering.

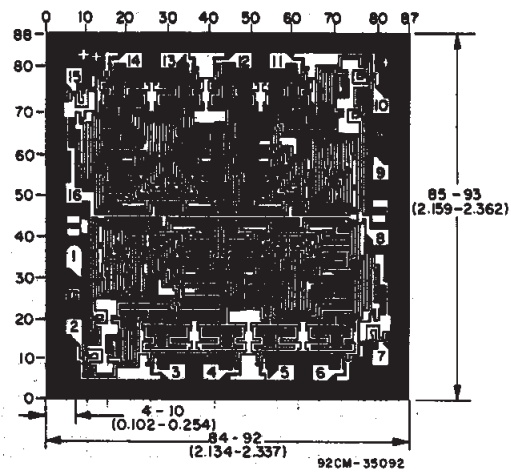


*NOTE:
FOR SYNCHRONOUS CASCADING, THE CLOCK TRANSITION TIME SHOULD BE MADE LESS THAN OR EQUAL TO THE SUM OF THE FIXED PROPAGATION DELAY AT 15 pF AND THE TRANSITION TIME OF THE OUTPUT DRIVER STAGE FOR THE ESTIMATED CAPACITATIVE LOAD.

Fig. 18 - Synchronous cascading of four binary counters with negative edge triggering.



Dimensions and pad layout for CD4518BH chip.



Dimensions and pad layout for CD4520BH chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7702301EA	NRND	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7702301EA CD4520BF3A
CD4518BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4518BE
CD4518BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4518BE
CD4518BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4518BE
CD4518BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4518BF
CD4518BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4518BF
CD4518BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4518BF3A
CD4518BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4518BF3A
CD4518BM	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4518BM
CD4518BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4518BM
CD4518BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4518BM
CD4518BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4518B
CD4518BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4518B
CD4518BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM518B
CD4518BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM518B
CD4518BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM518B
CD4520BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4520BE
CD4520BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4520BE
CD4520BEE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4520BE
CD4520BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4520BF
CD4520BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4520BF
CD4520BF3A	NRND	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7702301EA CD4520BF3A
CD4520BF3A.A	NRND	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7702301EA CD4520BF3A
CD4520BM	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4520BM
CD4520BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4520BM
CD4520BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4520BM
CD4520BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4520B

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4520BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4520B
CD4520BPW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	CM520B
CD4520BPWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM520B
CD4520BPWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM520B

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4518B, CD4518B-MIL, CD4520B, CD4520B-MIL :

● Catalog : [CD4518B](#), [CD4520B](#)

- Military : [CD4518B-MIL](#), [CD4520B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

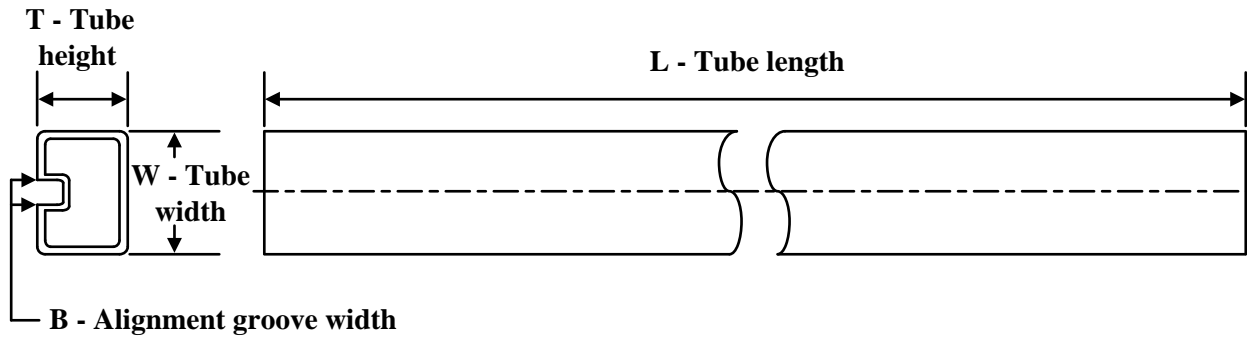

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4518BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4518BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4518BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD4520BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4520BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD4520BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4518BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4518BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4518BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD4520BM96	SOIC	D	16	2500	340.5	336.1	32.0
CD4520BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD4520BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4518BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4518BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4518BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4518BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4518BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4518BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4520BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4520BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4520BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4520BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4520BEE4	N	PDIP	16	25	506	13.97	11230	4.32
CD4520BEE4	N	PDIP	16	25	506	13.97	11230	4.32



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

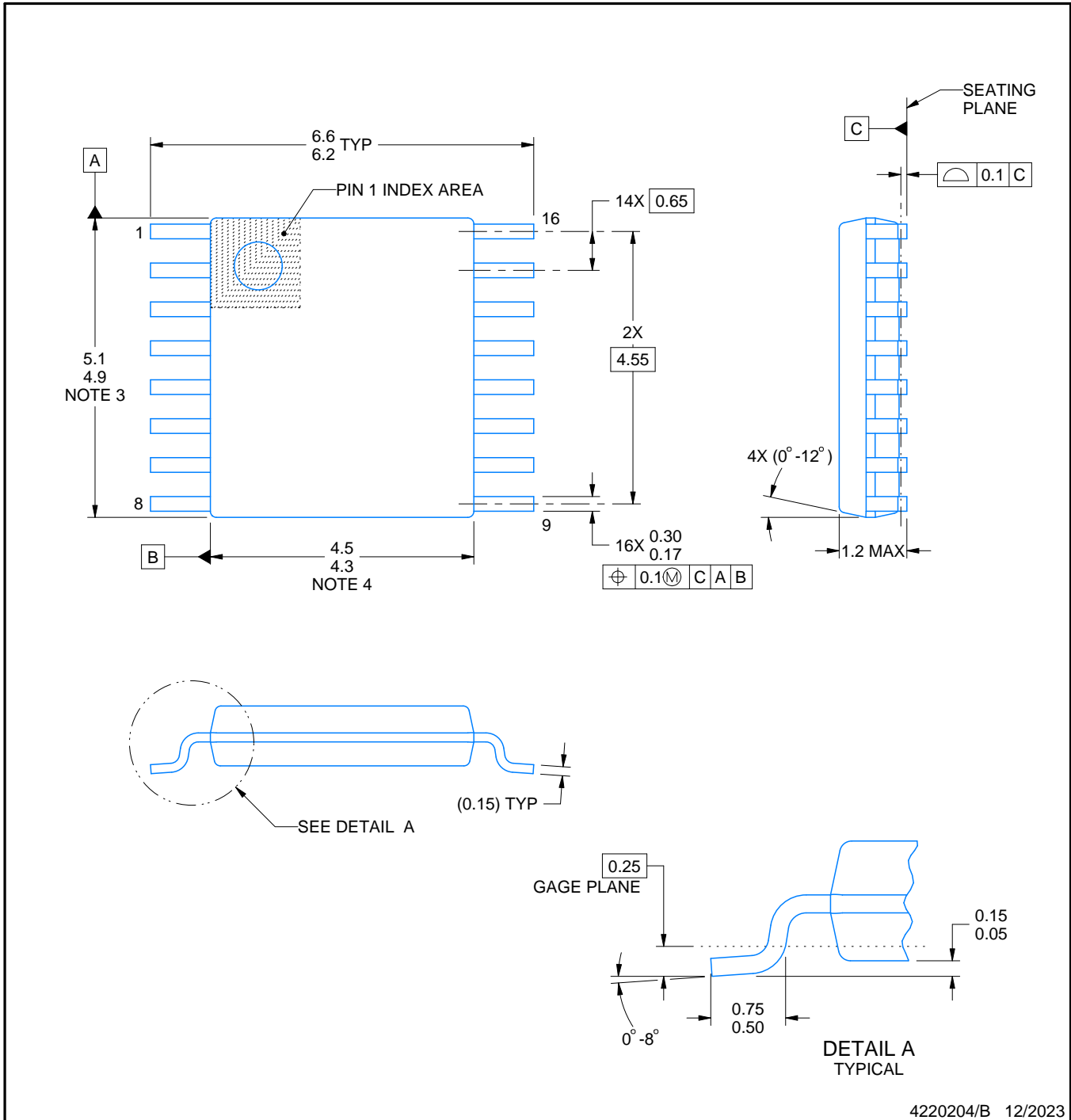
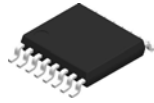


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

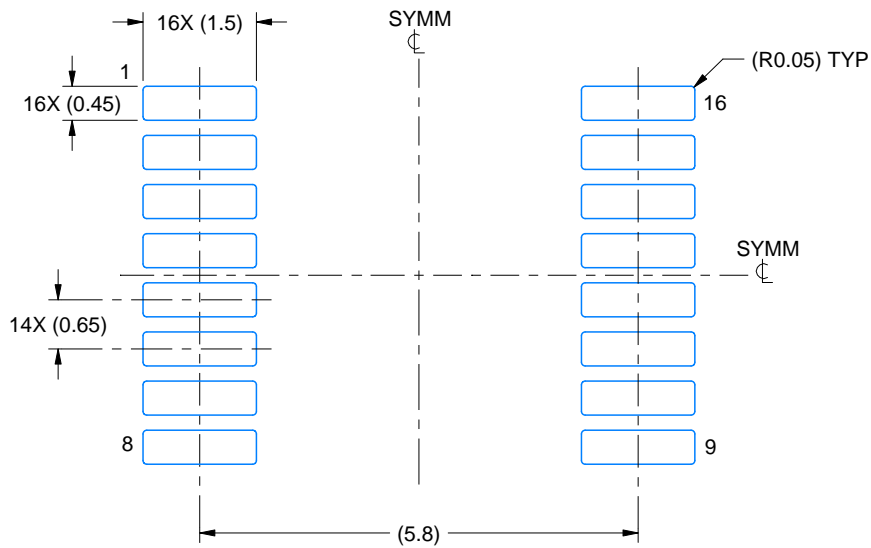
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

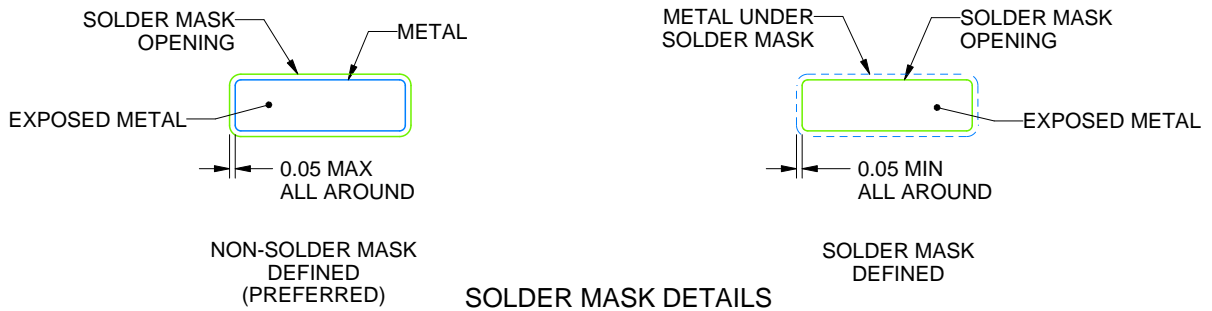
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

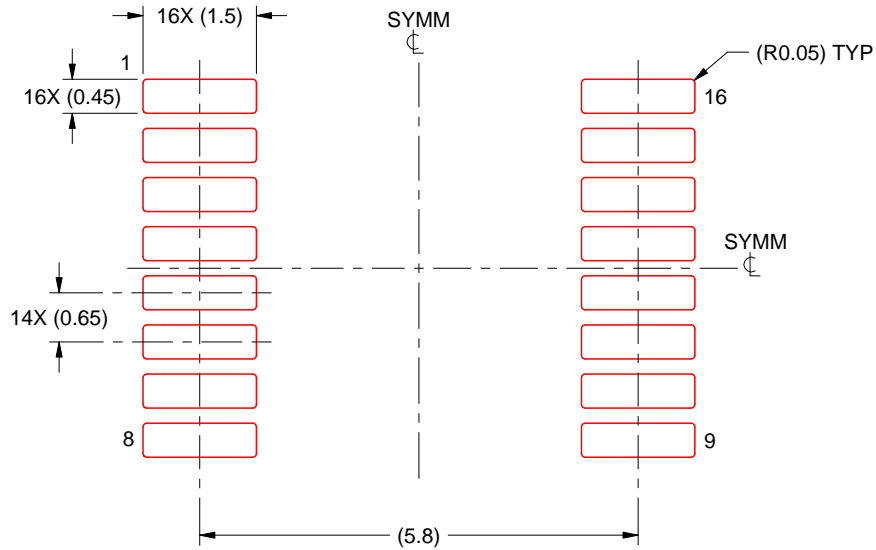
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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